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Single bismuth atom transistor for solid state atomic clock applications

Supervisor:
Dott.ssa Monica Bollani
Co-supervisor:
Dott. Enrico Prati

Author:
Luca Fagiani
Student ID: 899529

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Abstract

The purpose of this master thesis is the realization of a multigate transistor with a nanometric inner channel, used for atomic clock applications due to the single bismuth donor atoms implanted in its proximity.
In this work are shown in detail all the fabrication steps that bring to the device realization, whose final aim is to work as an electrostatic detector by using the channel to take over the charge of the donor atoms at 3K.
The material used is a silicon-on-insulator(SOI) of 145 nm, on which are performed at first electron beam lithography and dry etching for create the Si-based transistor structure. Then two ion beam implantations are done, one of Sb to obtain the doping of the source and the drain, the second one of single Bi atoms, performed in Melbourne, to place the donor atoms next to the transistor channel. After that e-beam evaporation tool create the oxide and the metal layers.
Another successful doping method for source and drain regions is performed in parallel with the Spin-on-Dopant (SOD).
The electrical characterization is done both at room temperature and at cryogenic temperature; the preliminary results shows a correct transistor behaviour at 3 K that gives high expectation on the next measurements for the detection of the charge state of bismuth atoms.

Sommario

Lo scopo di questa tesi magistrale è la realizzazione di un transistor multigate con un canale nanometrico interno, che vista la presenza di singoli atomi donori di bismuto nelle sue vicinanze, viene usato per applicazioni di orologi atomici.
In questo lavoro sono mostrati nel dettaglio tutti gli step di fabbricazione che portano alla realizzazione del dispositivo, il cui scopo finale è di lavorare come un rilevatore elettrostatico di cariche usando il canale per osservare la carica degli atomi donori a 3 K.
Il materiale usato è un silicon-on-insulator(SOI) di 145 nm, sul quale sono inizialmente praticate litografia elettronica e dry etching per creare la struttura base del transistor in silicio. Successivamente due impiantazioni con fascio di ioni son state fatte, la prima in antimonio per dopare le regioni del source e del drain; mentre la seconda, fatta a Melbourne, consisteva nell'impiantare singoli atomi di bismuto in modo da posizionare i donori accanto al canale del transistor. Successivamente attraverso l'evaporatore sono stati creati i strati di ossido e di metallo per completare il dispositivo.
Un altro efficace metodo di doping per il source e il drain è quello performato parallelamente con il cosiddetto Spin-on-Dopant(SOD).
La caratterizzazione elettrica è stata svolta sia a temperatura ambiente che a temperature criogeniche. I risultati preliminari mostrano un corretto comportamente del trasistor a 3 K che permette di avere alte aspettative riguardo le imminenti misure pianificate per rilevare la stato di carica degli atomi di bismuto.

Introduction

The fabrication of a transistor it has been one of the most endearing challenges of the 20th century; the first news about the possibility of create this device come in 1959 from the Bell's lab. It was immediately understood its importance for several applications as switches [39], amplifiers [47], power generator [40] and that brought to a continue evolution in terms of performances but also in the fabrication techniques. In 1965 the researcher Moore made a correct prevision, nowadays known as Moore's law, anticipating that the number of transistor for the same chip area would have doubled each 24 months, so they passed from millimetric size of 60's to the contemporary 10 nanometers [13].
The key role in this research belongs to silicon, the most common semiconducting element on earth, which has been the chosen material from the first moment and still is, due to its abundance, capability to withstand high temperature and large electrical activities without suffering breakdown and the possibility to easily dope it with atoms of groups III or IV to increase its conductivity. As already said, in the last decades all the technology systems move into the nanoscale dimension and consequently go to the quantum mechanics phenomena. The immediate consequence of this fact is the possibility of study new different phenomena but also different and more complicated characteristics to be managed. Basically we move from a device that was able to manage a flow of mA [45] to a single electron transistor(SET) [24], that is the most advanced transistor built, that allow the control of the passage of a single electron between source and drain.
But we don't stop there, because from SET technology,in the recent years, has begun several studies about the presence of donors atom near the MOSFET channel [25], in particular about the possibility of using them as a solid state q-bit system that could help one of the biggest challenge of the future years, the realization of an architecture for the functioning of a quantum computer.

The purpose of this thesis, which inserts in the context of the quantum device fabrication, is the optimization of the design and the procedures for the fabrication of a nanometric multigate field-effect transistor using a single atom doping of Bi near the channel region. The final aim is to detect the charge state of the donor atom employing the channel as an electrostatic detector. The work has been performed in collaboration with Melbourne University and CNR laboratory located in Catania.
The idea of using bismuth atoms as dopant near the channel comes from the last discoveries about the surprising properties that this material has in silicon [49] and that are discussed in chapter 2. Anyway the selective implantation of Bi, performed by the Prof Jamieson's group in Melbourne represents one of the last step of a long and complicate fabrication process. The chosen material to perform this device is a silicon-on-insulator(SOI), which is a layered silicon-insulator-silicon substrate, used in semiconductor manufacturing instead of a traditional silicon substrate, generally with the purpose of reducing parasitic device capacitance[5].
Nanofabrication consists into a long process in which you have to find the optimal value for each parameter in order to achieve the correct nanometric dimension; this long work allows us to create a final MOSFET device with an intrinsic inner channel of $50nm$. Some of the key passages of this process that have to be briefly underline are: first of all the Reactive Ion Etching recipe, in order to have our transistor correctly realized over the insulator box and that often represents a big issue and then the creation of ultraprecise and small masks of 200 x 200 nm for the selective implantation of bismuth.
Furthermore two different techniques has been performed to dope the source and the drain regions of the MOSFET. While the main silicon samples has been doped with an Sb ion beam implantation, performed in Catania, another cheaper and directly available in LNESS lab doping technique has been carried out for other samples with the so called Spin On Dopant(SOD). Both the techniques bring to a successful doped silicon device, even if in the SOD case some problems have come to light.
At the end, room and cryogenic temperature measurements are performed in LNESS, using a cryostat, to check the transistor quality obtained. The promising results viewed ad 3K brought to decision to perform more specific measurements to detect the charge donor state in the weeks after the drawing up of this thesis.

The structure of this work tries to recreate the logical path that has been followed in my master thesis.
First the theoretical aspect is reported: chapter one presents the silicon transistor theory, from MOSFET to the single electron transistor and introduces properties of bismuth donor atoms in silicon in the atomic clock domain.
In chapter two, the diffusion theory and the Hall effect are described; both of them are fundamental to describe the spin on dopant process.
Chapter three described the fabrication technique followed for the realization of the device together with several images that allow to understand each step; there is also a section that described in detail the process of the ion beam implantation performed.
Finally, in chapter four the results obtained are presented and discussed, together with a presentation of the work in progress and the future steps of the project.
Before the conclusion an appendix described all the lithography technique the technology setup used to obtain these results. The thesis ends with a summary of the goals and the accomplishments.

Chapter 1

From MOSFETs to quantum clock theory

1.1 MOSFET: theory and working principle

The MOSFET is by far the most diffused semiconductor device in ICs. It is the basic building block of digital, analog, and memory circuits. Its small size allows the making of inexpensive and dense circuits [6]. In the figure 1.1 it is possible to see its general outlook. The acronym MOS stands for metal-oxide-semiconductor that is the fundamental central block, next to it we find the two *pn* junctions, source and drain, that supply the electron and the holes to the transistor and due to a voltage difference drains them away. The name FET, field-effect-transistor, is related to the possibility to turn on and off the transistor through an electric field that passes into the oxide. A transistor is a device that presents a high input resistance to the signal source, drawing little input power, and a low resistance to the output circuit, capable of supplying a large current to drive the circuit load [6].
The region between the source and drain junctions is called the channel region, which has a length L and a width W. The MOSFET is a four terminal device, the terminals designated are gate, bulk, source and drain. Under normal operation the source-substrate and drain-substrate junctions are reverse- or zero-biased, and the terminal identified as source, in the case of an n-channel MOSFET, has the lowest reverse bias [4].
The aim of the MOSFET is the ability to control the voltage and current flow

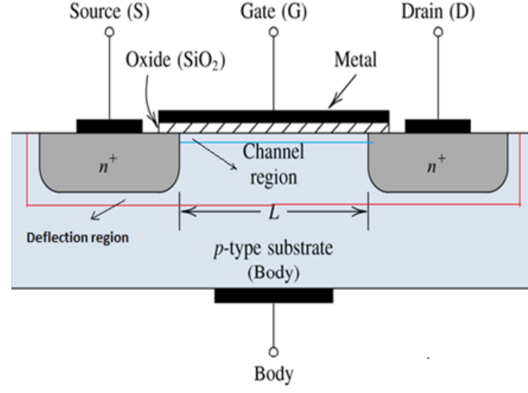

Figure 1.1: Mosfet block diagram

between the source and drain. It works almost as a switch. The silicon semiconductor substrate plays a fundamental role, in fact its surface below the oxide layer can be inverted from p-type to n-type by applying a positive or negative gate voltages respectively. If a positive gate-source voltage is applied, the holes present under the oxide layer are pushed with a repulsive force downward with the substrate and so the inversion layer populated by electrons is finally formed. The transistor is said to be off if the gate potential is such that there is no inversion layer. The positive voltage also attracts electrons from the n^+ source and drain regions into the channel. Now, if a voltage is applied between the drain and source, the current flows freely between them and the gate voltage controls the electrons in the channel. Instead of positive voltage if we apply negative voltage, a hole channel will be formed under the oxide layer. Once the channel is formed, the behaviour of the current between source and drain (I_{DS}) that flows in it, is described by this equation:

$$I_{DS} = \frac{W}{L} C_{OX} \mu_{NS} (V_{GS} - V_t - \frac{m}{2} V_{DS}) V_{DS} \tag{1.1}$$

It shows that I_{DS} is proportional to W (channel width), μ_{NS} (electron mobility), V_{DS}/L (the average field in the channel), and $C_{OX}(V_G$ - V_t - $mV_{DS}/2)$, which may be interpreted as the average inversion charge (Q_{inv}) in the channel. When the voltage between source and drain V_{DS} is very small, the ($mV_{DS}/2$) term is negligible and $I_{DS} \propto V_{DS}$, i.e., the transistor behaves as a resistor. As V_{DS} increases, the average inverse charge decreases and dI_{DS}/dV_{DS} decreases. By differentiating Eq.(1.1) with respect V_{DS}, it can be shown that dI_{DS}/V_{DS} becomes zero at a certain V_{DS}.

$$\frac{dI_{DS}}{dV_{DS}} = 0 = \frac{W}{L} C_{OX} \mu_{NS} (V_{GS} - V_T - \frac{m}{2} V_{DS}) \ \ at \ \ V_{DS} = V_{dsat} \tag{1.2}$$

$$V_{dsat} = \frac{V_{GS} - V_T}{m} \tag{1.3}$$

V_{DSAT} is called the drain saturation voltage, beyond which the drain current is saturated, it changes value with the gate voltage (V_G). The I-V curves (Fig1.2) can be divided in two different regions, one with $V_{DS} << V_{dsat}$ is the linear region, and the other one is the saturation region. Other Authors refer to the regions as the ohmic region and the active region [18].

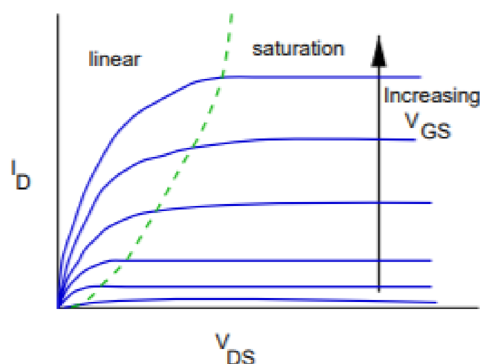

Figure 1.2: I-V curve of MOSFET. The green line represents the delimitation between the ohmic region and the saturation one, it changes with the value of V_G.

1.2 Single Electron Transistor

Miniaturization has brought today's electronic devices in scale very close to the size where quantum phenomena will dominate the operation of the device hence changing its whole properties [26]. One of the most fascinating nanodevices is the single electron transistor (SET). The operation of SETs is based on the manipulation of only a single electron from source to drain through an ultra-small quantum-dot controlled by gate. Since the typical dot size, which is the critical size of the device, is less than 10 nm, they have high potential to form ultrahigh-density integrated system.[14]. This device exploits the quantum mechanical phenomenon of tunneling and it can perform as a switch or as an amplifier, similarly

to common FETs, but it can also control the transport of single electrons[30] and holes [44]. The SET, similarly to the FET, can be used in its amplifier mode as an electrometer to measure the charge or charge variations of a specific system with a very high energy and charge sensitivity that comes close to the theoretical quantum limit [9]. Before introducing the functioning of the SET, a brief introduction of Coulomb Blockade principle has to be done.
Let's start considering a small conductive dot connected to ground (a large reservoir as source) via tunnel junction as the simplest single-electron device. Applying voltage to the gate electrode, which is capacitatively coupled to the dot, it is possible to observe electron tunnelling phenomena. It brings an increase of the electrostatic (Coulomb charging) energy of:

$$\Delta U = \frac{e^2}{2C_{dot}} \tag{1.4}$$

where e is the elementary charge and C_{dot} is the total capacitance of the dot. If the electric flux from the dot is all terminated at gate and ground, C_{dot} is the sum of gate capacitance C_G and tunnel junction capacitance C_T. When the dot becomes sufficiently small (C_{dot} is small) and ΔU starts to exceed the thermal energy, an external gate bias is required to overcome the Coulomb repulsion of the barrier. This effect is called Coulomb blockade and it is the basic of the operation of SETs. In this regime the electrons can be added singularly, increasing the incoming flux with fixed steps; this regime cannot work at room temperature because of the high amount of thermal energy $k_bT >> \Delta U$. In general, a SET is a three-terminal device having gate, source, and drain electrodes as a MOSFET (Fig 1.3). The three reservoirs are capacitatively coupled to a small conductive dot. The reservoirs of source and drain are separated by the tunnel junctions from the dot, such flow is controlled by the gate that moves the energy level of the quantum dot.
To describe the drain current characteristics of SET, at first has to be presented the the total energy $E(n)$ of the system, where n are the electrons in the dot, expressed as:

$$E(n) = U(n) + \sum_{k=1}^{n} \epsilon_k = \frac{(ne - V_G C_G - C_D V_{DS})^2}{2C_{dot}} \tag{1.5}$$

where $U(n)$ is the electrostatic energy of n electrons, ϵ_k is the k-th quantum energy level in the dot, C_D is the drain capacitance to the dot and V_{DS} is the

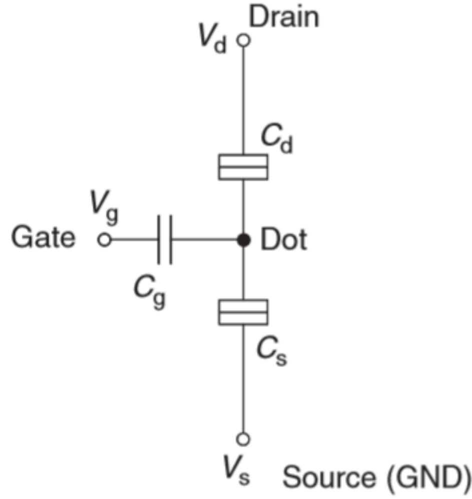

Figure 1.3: Equivalent circuit diagram of a SET. Gate,source and drain electrodes are capacitively coupled to a small conductive dot. Figure reproduced from [33]

drain source voltage. In particular, this discreteness of quantum energy levels ϵ_k should be considered in the case of semiconductor dot. The electrochemical potential of the $n-th$ electron in the dot is defined as a difference of the total free energy of the system when electron number changes from $n-1$ to n

$$\mu = E(n) - E(n-1) \tag{1.6}$$

Considering V_{DS} negligible, the value of the electrochemical potential is basic to understand the possibility to tunnel from source to drain through the island, as it's possible to observe in the figure 1.4.

$$\mu_{n+1} > \mu_s \geq \mu_n \geq \mu_d > \mu_{n-1} \tag{1.7}$$

μ_s and μ_d are the electrochemical potential of the source and the drain, in the figure (1.4.a) the values of both of them allows the presence of n or $n-1$ electrons in the dot and a passage of current. In the figure (1.4.b) the electron cannot move form the quantum dot due to the too high level of the electrochemical potential of the source and drain, given the so called Coulomb Blockade effect.
Now, the number of electrons in the dot is fixed to n. By increasing gate voltage V_{GS}, an oscillation on the I_D is observed due to the alternately satisfaction of the Coulomb Blockade and the single electron tunneling condition (Fig1.5). Whenever gate voltage V_{GS} comes to the valley of the oscillation, the number of electrons in the dot increases by 1 and the interval between each peak ΔV_G is

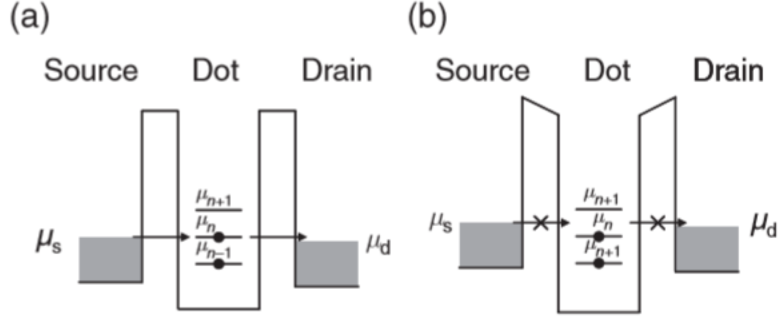

Figure 1.4: Potential profile of a SET. (a) Single electron tunneling condition. Electron can tunnel into the dot from source and tunnel out to drain one by one. (b) SET is in Coulomb blockade condition. Electron tunneling is denied. From Ref. [33]

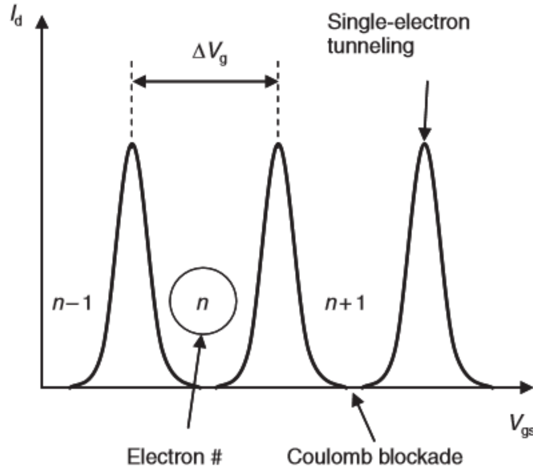

Figure 1.5: A schematic diagram of Coulomb blockade oscillations. Figure reproduced from [33]

determined by the following expression (where E_A is the addition energy) :

$$\Delta V = \frac{C_{dot}}{eC_G} E_A \tag{1.8}$$

After having seen the variation of I_D in function of the voltage gate, let's analyze what is the behaviour in function of V_{DS}. Two different working regimes can be found: the first happens when we are in one of the peaks of the Coulomb blockade oscillation; I_D is going to increase monotonously with V_{DS}. If the system is in one of the valley of the oscillation, the I_D is blocked until a certain V_{DS} where μ_d goes below μ_n, as shown in Figure 1.6.
The last distinctive curve of the SET and probably the one usually observed is the so called stability diagram. The Coulomb Blockade phenomena is completely

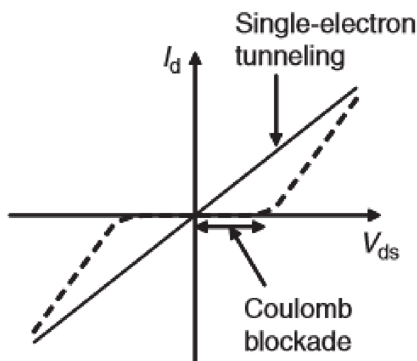

Figure 1.6: I_{DS}–V_{DS} characteristics curve in a Coulomb Blockade regime. V_G will be at single-electron tunneling condition in the solid line whereas dashed line shows V_G at Coulomb blockade condition. No current present without a sufficient drain bias. Taken from[33]

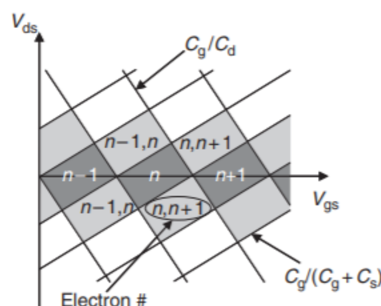

Figure 1.7: A schematic view of Coulomb blockade diagram (contour plot of I_{DS} as a function of V_G and V_{DS}) in an SET. The Coulomb Blockade region are represented by black diamonds, where I is suppressed; the current flow in the light grey region. The slopes of the falling side and the rising side of the diamonds are given by C_G/C_D and $C_G/(C_G + C_S)$. From Ref. [33]

described analyzing this plot (Fig.1.7). The dark grey rhombus indicates where the current is blocked so the Coulomb Blockade is activated; while the light grey region describes the single electron tunneling parts which the current flows from source to drain.

1.3 Silicon quantum technology and SET detecting charge

Silicon has been chosen as a promising material for the research on the solid state quantum computing research, in fact its properties fit perfectly with the manipulation of electron spins bound to single donors, that represents a solid

platform for quantum information processing [23]. To analyze the behaviour of donors in the silicon bulk, several common techniques has been used like classical electrical measurements and electron spin resonant (ESR) spectroscopy, but in the case of nanodevices, presence of material interfaces, confinement in potential wells has to be considered [10]. That's why to detect charge and the spin at the single donor level on silicon, a particularly silicon SET is used to detect them. By starting from this point, the main aim of this master thesis is the realization of this multigateFET doped with Bi atoms near the intrinsic channel. In the previous section it was possible to understand the behaviour of a single electron transistor, so we have seen how the variation of the applied voltage gate modified the energy level of the quantum dot, in order to allow the passage of single electrons. In such condition it has to be considered also the presence of donor atoms in the proximity of the channel that are going to modify the common behaviour of the traditional setup. Due to the small entity of the barriers between the source/drain and the dot, the transit time for electrons is much less than nanoseconds so the passage of individual electrons is not detected. However, if a single donor is implanted in the proximity of the channel, an electron can transfer from the channel to the donor placed nearby at milli- to microsecond timescale. This working regime can be reached only with a multigate system, in fact while the main gain establish a regime of current between source and drain (so not a Blockade Coulomb situation), the other gate (Side gate) decreases the donor atoms energy levels such that the electron transfer is allowed.
From figure 1.8 it is possible to understand exactly the structure of the system. The possibility to control the two gates separately is due to the fact that the coupling with the channel is different. The main point to understand is that due to the wide energy barrier present, the time required to the electron trapped in the donor atom to join back the current flow is of the order of micro- to milliseconds. When an electron is trapped by the donor, no current is detected, so the change in charge state of the donor can be observed from the variations of current flow. Also the average tunnelling time and process statistics has to be analyzed to a have correct analysis and it is done by repeating and averaging measurements. The channel of the transistor is used as a highly sensitive electrometer to detect the charge state of nearby donors down to individual charges.

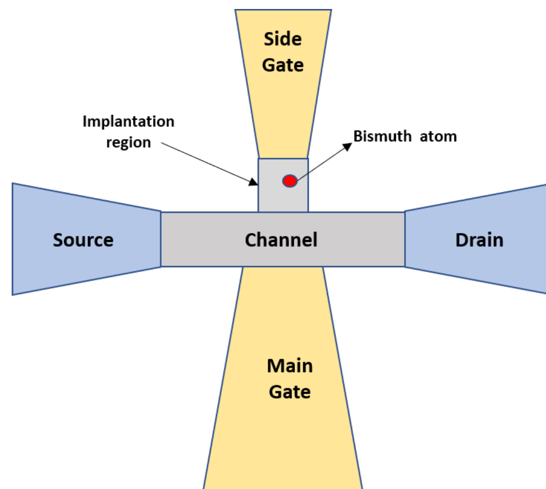

Figure 1.8: Schematic top-view representation of the transistor with its main parts: source, drain, main gate for the control of source-to-drain current, bismuth atom placed in the implantation region, side gate for the control of the electron flow towards the donor atom. The geometry is not in scale.

1.4 Bismuth properties in silicon for atomic clocks and solid state qubits

An atomic clock is a device that uses hyperfine levels transition of the electromagnetic spectrum of atoms to obtain a standard frequency used for ultraprecise measurement of time. The typical resonance transition between the two hyperfine levels is the one of the $^2S_{1/2}$ ground-state of hydrogen or alkali-metal atoms with a single valence electron. A way to detect these transitions consists in a selection state by optical pumping; it can be basically represented by a three level scheme, in which the first two levels are represented by the hyperfine levels and the third level at higher energy is used in order to have continuous cycles of excitation and random relaxation to drive population away from the component being pumped[35]. The fact of using donors of V group in silicon, bismuth in this particular case, is due to have an absorption spectra very similar to hydrogenic free atoms already used for these applications, because they also have a single electron not bounded. In the case of Si:Bi, the electron spin $S = \frac{1}{2}$ coupled to a nuclear spin $I = \frac{9}{2}$ generates two states $F = I + S = 5$ and $F = I - S = 4$, with a splitting energy level due to the hyperfine interaction of 30 μeV, that represent the first two levels of the optical transition already described. Their transition is of the order of the microwave, such states are referred to the neutral donor D^0. The third higher energy state in that configuration is used for the

optical pumping it is represented by the donor-bound-exciton (D^0X) energy, so the incoming photons will be resonant with that D^0-D^0X transition as shown in Figure1.9. Due to the very weak absorption of this transition, the measurement about the D^0X absorption spectrum, that allow the mechanism of the atomic clock measurement, are obtained indirectly, detecting the carriers generated by the Auger decay of the created D^0X, using photoconductivity (PC).

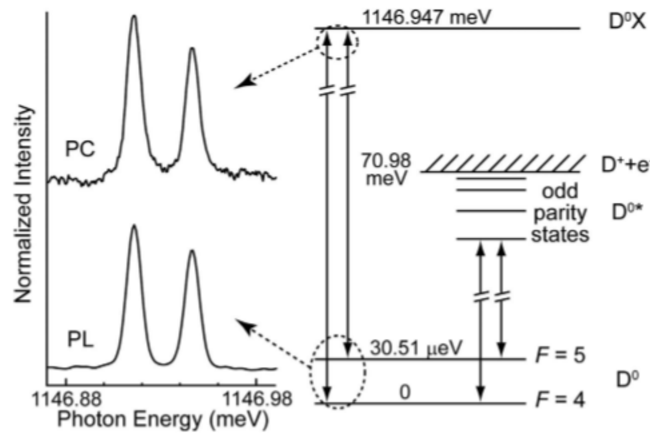

Figure 1.9: On the right: energy levels involved in the selection state by optical pumping. On the top there is the donor bound exciton state D^0X at 1146 meV, on the bottom the two hyperfine levels of the neutral donor D^0 and in the middle there are the states involved in the Rydberg transitions. **On the left**: photoconductivity (PC) and photoluminescence (PL) absorption spectra of Bi D^0X. Taken from Ref.[35]

After a brief description of the working principle of an hypothetical atomic clock made with bismuth donors in silicon, an interesting suggestion to exploit this technology for the qubit domain is below reported.
In fact during the recent years the global research moves toward the possibility to find stable and accessible system used as qubits; several interesting results are obtained in the group V donor in silicon [49], by considering as a qubit the spin of an impurity atom in a crystal. The main problem with the realization of reliable solid-state qubits is that their quantum state tend to be disturbed by their surrounding environment. In the case of silicon, the fluctuation of the local magnetic field due to continuous flips of the nuclear spins of atoms must be limited to increase the so called decoherence time of a qubit.
In order to create a system that is protected by at least the first order of magnetic field variation, a study on the atomic clocks is performed to reach improvement for the spin qubits in silicon; in particular was found that the hyperfine transition of the Si:Bi system used for the atomic clock, remains stable in a certain range

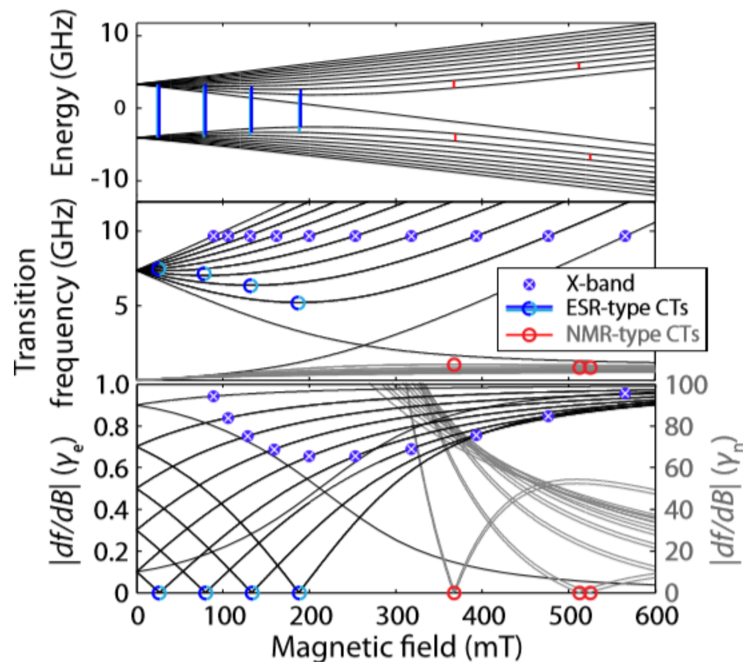

Figure 1.10: The eigenstate energies (top) of Si:Bi dependence in function of magnetic field, the CTs transition compared with the conventional X-band transitions occur at a fixed frequency in the linear regime (middle), and the first-order magnetic field dependence (df/dB) of these transition frequencies (bottom).Taken from [49]

of a magnetic field [49]: these transitions are called "clock transition" (CTs).
In order to study more in detail these transitions, relating them to the magnitude of the magnetic field, electron-spin-resonance(ESR-type) [1] and nuclear-magnetic-resonance(NMR-type) [16] are used. Four ESR-type transitions are present at low magnetic field (<250 mT), as shown in blue in the figure 1.10, observed at 27, 80, 133 and 188 mT, in the range of frequencies 5.2 to 7.3 GHz. By observing the energy of Si:Bi spin system, and in particular, by focusing on these four transitions, it is possible to see that the ground and the excited states are almost flat in that magnetic field region and so they represent the already mentioned stable CTs. Also NMR-type transitions are observed at higher magnetic field, but generally the analysis is based on the ESR due to their large energy splitting even at low field.

Chapter 2

Diffusion and electrical measurement theory

Silicon is one of the most common materials for the microelectronics devices due to its semiconducting properties that allow the conduction of current. The conductive properties are controlled by the presence of small concentrations of impurities, known as dopant. In fact being silicon one of the IV group materials, it has four valence electrons and it needs the presence of substitutional atoms in the bonding arrangement in order to be conductive. There are two types of impurities that can be used to change the conductive properties of a semiconductor: donors (to create a n-type semiconductor) or acceptors (to have a p-type semiconductor). Donors are atoms that belong to group V, so having 5 electrons in their outer orbital, they give this extra electron up to maintain a stable bonding configuration. Acceptors belong to the group three of the periodic table and contain only three valence electrons, so they require an extra electron to reach a stable configuration and these results in the contribution of an hole to the electrical conduction within the silicon. The typical atoms that can be used to create p-type regions are boron and indium. Several methods have been implemented in order to dope a semiconductor: ion implantation [29], solid source dopant [48] [11], chemical vapour deposition [36], and spin on doping [7]. All this method need relatively high temperature (more than 800 ^{o}C) for dopant diffusion and annealing activation [7]. The temperature and time control during the activation step (called also drive-in step) is fundamental for controlling the final doping profile [12]. In many cases these high temperatures treatments damage the samples since they favour the introduction of contaminants [3].

The ion implantation method is based on an ion source, which produces the

wanted dopant charges, accelerating them through an electric field in order to irradiate the wafer. The penetration depth of the ions can be set precisely by modifying the energy of the source and the acceleration voltage. In contrast to diffusion process, doping particles penetrate in the silicon substrate by collisions with atoms and this can create some damages on the silicon crystal structure. This process is usually performed at room temperature, but then it is necessary to do an activation process at high temperature (temperature range 850 ^{o}C - 1000 ^{o}C) to allow the dopant to move to the lattice sites.
Chemical vapour deposition is a widely used technique to form layers of dopant oxides on silicon surfaces. By using this method the characteristic of doped silicon layer (junction depth, dopant level and dopant profile) can be modified controlling the ratio between the oxide and the dopant flow, the temperature and the time of annealing. Instead, in the case of solid source dotation, the dopant atoms are transferred by evaporation from the solid source (to dope with phosphorus scientist use cesium phosphate layers), and then diffuse to the silicon surface during the drive-in step [12].
Doped silicon layers can also be fabricated using a spin-on dopant (SOD). SOD are silicates solutions containing dopant atoms such as phosphorus or boron. According to the manufacturers of SOD, this method guarantees an uniform and consistent doping with high yields. It allows simultaneous diffusion of p-type and n-type dopant and different concentration of the same dopant and doesn't need vacuum condition for the deposition of the layer. SOD must be spin-coated on the silicon substrate, then the samples must be dried in a pre-baking step at low temperature, finally the coated samples have to be heated up for the diffusion of dopant in the silicon layer. After the drive-in step the glassy layer must be removed in a hydrogen fluoride solution. The SOD technique is a cheaper process than the aforementioned methods and it produces layers less affected by the introduction of contaminants during the annealing process [3]. In literature we can find different examples of application of this technique: it is used as an alternative to gases and chemical vapour deposition for the fabrication of single crystal solar cells [27] [42] , for the doping of Ge-layer [3] and for doping of silicon nanopillar solar cells for creating conformal PN junction [7].

2.1 Diffusion theory

Diffusion can be defined as the net transport of molecules or atoms from a region of higher concentration to one of lower concentration, so it described the process of mixing of two different materials.
The diffusion of atoms in a solid structure can be described by the Fick's equations [17]. The first Fick's equation states that:

$$J = -\mathcal{D}\nabla c \tag{2.1}$$

where $\vec{J}$ is the diffusion flux of particle, $\mathcal{D}$ is the diffusivity tensor and ∇_c is the gradient of the concentration of particle that diffuse in the solid. In general $\mathcal{D}$ varies with direction, but if we consider an isotropic material the diffusion flux and the concentration gradient are usually anti-parallel[17].
In addition to the previous law, to completely describe the phenomenon of diffusion is necessary to use a balance equation. For particles that doesn't do any reactions can be used the continuity equation:

$$\frac{\partial c}{\partial t} + \nabla J = 0 \tag{2.2}$$

where t is the time, $\nabla\vec{J}$ the gradient of the diffusion flux and c the concentration of dopant.
From the combination of the first Fick's law (2.1) and of the continuity equation (2.2) it is possible to define the Fick's second equation (also called diffusion equation):

$$\frac{\partial c}{\partial t} = \nabla(\mathcal{D}\nabla c) \tag{2.3}$$

Considering only diffusion in one direction (x direction) and a concentration independent diffusion coefficient (D) the previous diffusion equation equation become:

$$\frac{\partial c}{\partial t} = D\frac{\partial^2 c}{\partial x^2} \tag{2.4}$$

Equation (2.4) is a second order, linear partial differential equation, it requires initial condition and boundary solutions to be solved [17].

2.1.1 Diffusion in a semiconductor

In a semiconductor there can be three different processes of diffusion: dopant atoms may dissolve by occupying interstitials, substitutional sites or both [17]. We have interstitials diffusion when an interstitial atom jumps into a interstitial position (Fig. 2.1 (b)), instead there is the substitutional process when a substitutional atom exchanges lattice position with a vacancy (Fig. 2.1 (a)) [21]. In silicon there is both vacancy and interstitial contribute during the dopant diffusion process, the mix of these two processes is called interstitialcy (Fig. 2.1 (c)).

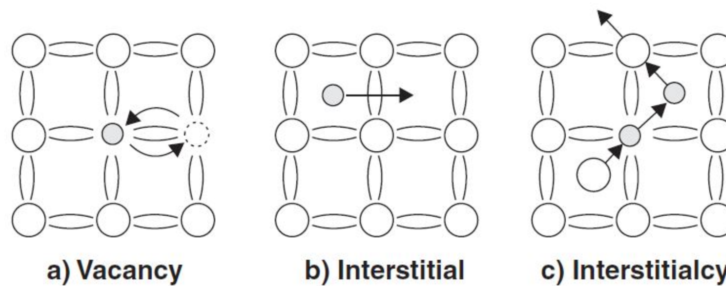

Figure 2.1: Schematic representation of the three possible processes of diffusion. Image taken from [17].

In addition to this, to solve the diffusion equation for doping concentration in a semiconductor, is also necessary to define the type of the source of dopant atoms. The dopant can be considered as an infinite impurity source in contact with a semi-infinite medium (assuming that the substrates thickness is orders of magnitude greater that the diffusion depth of the dopant). In an one-dimensional case, the concentration of dopant inside silicon at position x and time t is given by:

$$c(x,t) = c_0 \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) \tag{2.5}$$

where c_0 is the surface concentration at the top of the layer ($x = 0$) [38] and erfc is the complementary error function which is defined by:

$$\operatorname{erfc} z = 1 - \operatorname{erf} z \tag{2.6}$$

and the error function is defined by the integral of the Gaussian equation. The solution given by (2.5) is usually applicable for the study of the diffusion of a volatile solute in a non volatile solvent, or to study the diffusion of an inex-

haustible diffusion source into a solvent with solubility c_0.
Instead, if the dopant can be modelled by a thin layer with a finite number of atoms per unit area (M) concentrated at $x = 0$ of a semi-infinite sample, the concentration at time t is described by:

$$c(x,t) = \frac{M}{\sqrt{\pi D t}} e^{-\frac{x^2}{4Dt}} \tag{2.7}$$

where $\sqrt{\pi D t}$ is the diffusion length, a characteristic distance for diffusion problem [17].
For Silicon, the diffusion coefficient can be expressed in function of the temperature using the Arrhenius equation:

$$D = D_0 e^{-\frac{E_a}{k_B T}} \tag{2.8}$$

where E_a is the activation energy expressed in eV, k_B is the Boltzmann constant (8.6×10^{-5} eV) and T the annealing temperature. In literature we can find different value of D_0 and E_a. For the diffusion of Phosphorus in Silicon typical diffusion value are:

$$D_0 = 10,5\ \frac{cm^2}{s} \qquad E_a = 3,69\ eV \tag{2.9}$$

2.2 Electrical measurement theory

The experimental determination of the effective doping level and the electron mobility of the samples treated with SOD and rapid thermal annealing method has been done by using two different method of measurement: the Hall bar measurement and the four-probe method.
In general when an electric field $\vec{E}$ is applied to a material, it causes an electric current. The resistivity ρ of the material is defined by the ratio of the electric field and the current density $\vec{J}$. Experimentally, a resistance R is deduced from the ratio of an applied voltage V and a current I. Only when the geometry of the set-up is well known the resistivity can be accurately calculated. The identification of R with the resistance of the sample is usually incorrect as it intrinsically includes contact resistances at the positions of the probes, which are in series with the resistance of the sample [32]. In addition to these, the sample-specific characteristics are intimately related to technical constraints such as the probe geometry and the size of the sample.

2.2.1 Hall Effect

Hall bar measurements are based on the Hall effect. In 1879 Hall found that a magnetic field $\vec{B}$ applied to a conductor (or a semiconductor) perpendicular to the current flow direction produces and electric field perpendicular to the magnetic field and to the current[37]. Considering now the motion of carriers in a uniform magnetic field $\vec{B}$, the force on the carrier is given by the vector expression of the Lorentz force:

$$\vec{F} = q(\vec{E} + \vec{v} \times \vec{B}) \tag{2.10}$$

where q is the charge of the carriers, $\vec{E}$ the electric field, $\vec{v}$ the velocity of the carriers. The direction of this force can be determined by right hand rule: considering also the fact that an electron has a negative charge the direction for an electron is opposite to the one pointed by the thumb [15].
Now we can consider a n-type sample with thickness t, width W and the length L (plan view scheme of a n-type sample in figure 2.2). Assuming that a constant

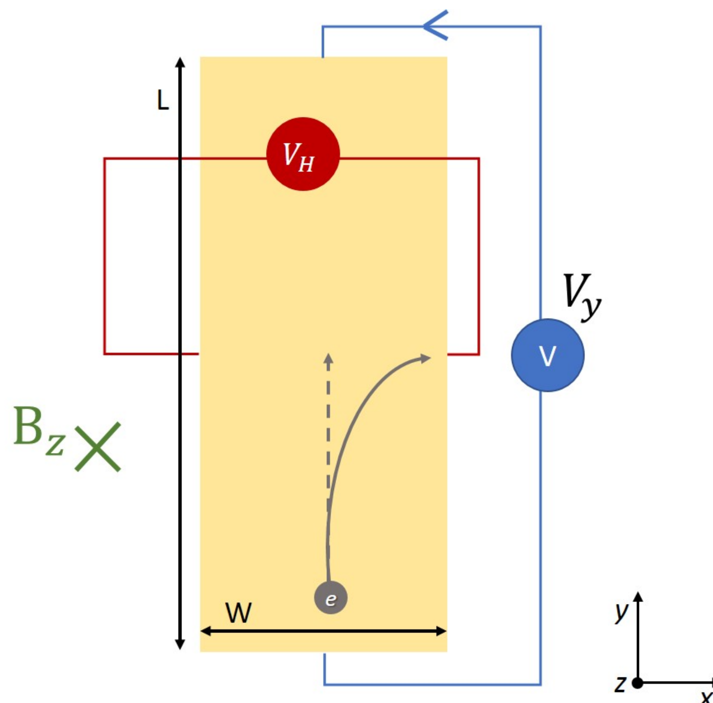

Figure 2.2: Hall effect on a n-type slab of a semiconductor (plan view).

current I, defined by $I = qWLv_x n$ is flowing along the x direction and a constant

magnetic field of intensity B is present along the z direction, due to the presence of the Lorentz force, electrons moves away from the current direction towards the negative y direction. Holes move to the opposite direction. This separation of charge establishes an electric field that opposes to the migration of further charge, so we can measure a steady electric potential as long as the charge is flowing. Considering that there is no net force on the y direction since there is no current flowing and we are in steady state so $\vec{F} = 0$, from the Lorentz force we can find the electric field along the y direction $\vec{E}_y$:

$$E_y = v_x B_z = \frac{BI}{qWLn} \tag{2.11}$$

From the electric field in the y-direction produces the Hall voltage V_H:

$$V_H = -\int_W^0 E_y dy = -\int_W^0 \frac{BI}{qWtn} dy = \frac{BI}{qtn} \tag{2.12}$$

According to this theoretical result, it is possible to find the electron density n in the semiconductor knowing the current, the thickness, the magnetic field, and measuring the Hall voltage.

2.2.2 Hall bar measurement

Hall effects measurement commonly use two samples geometry: a long and narrow hall bar geometries or a circular van der Pauw geometries [32]. Each has advantages and disadvantages. The geometry of the 6-contacts Hall bar in figure 2.3 has been used in this thesis work, in orange there are the gold metallic contacts. According to the number written on the contact of the figure 2.3 the Hall voltage is the drop voltage between the contacts 2 and 3 and also between the contacts 4 and 5:

$$V_H = V_{23} = V_{45} = \frac{BI}{qtn} = \frac{R_H BI}{t} \tag{2.13}$$

were B is the magnetic field, I the current flowing in the sample from contact 1 to contact 6, q the carrier charge, t the thickness of he sample, n the number of carriers and has been used the definition of the Hall coefficient of the material R_H:

$$R_H = \frac{1}{nq} \tag{2.14}$$

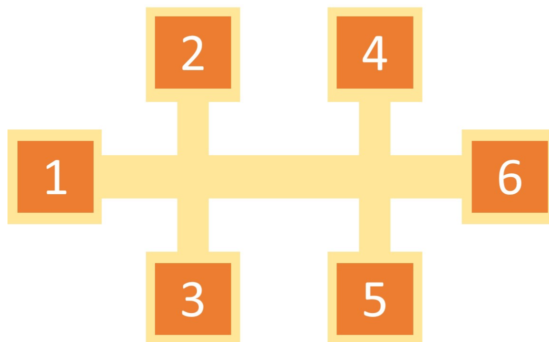

Figure 2.3: Planar view of a schematic reproduction of a Hall bar.

In general, the process of fabrication of a 6-contacts hall bar geometry doesn't allow to create a perfectly symmetric structure. Structure shape, contact positions or generic non-uniformities of the sample have a huge negative influence on the measurements. To solve this problem, there is the possibility to acquire different sets of measurement with opposite magnetic field and then make the average of these values, because the Hall voltage change the sign according to the direction of the magnetic field. The parasitic effects aren't influenced by the direction of it, so they can be removed from the measurements. The following formulas can be used to determine the Hall coefficient R_H:

$$R_{H_{23}} = \frac{(V_{23}^{B+} - V_{23}^{B-})t}{2IB} \qquad R_{H_{45}} = \frac{(V_{45}^{B+} - V_{45}^{B-})t}{2IB} \tag{2.15}$$

The total hall coefficient R_H is given by averaging the two previous value:

$$R_H = \frac{R_{H_{23}} + R_{H_{45}}}{2} \tag{2.16}$$

The knowledge of the Hall coefficient leads to a determination of the carrier type as well as the carrier density (see the equation (2.14)):

$$n = \frac{1}{R_H q} \tag{2.17}$$

It is important to underline that the previous equation are derived under simplifying assumptions of energy-independent scattering mechanisms. If this assumption relax, is necessary to account for the Hall scattering factor, defined by:

$$r = \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \tag{2.18}$$

with τ being the mean time between carrier collisions. The value of r is between 1 and 2 and tends to 1 in the limit of high magnetic field that are very difficult to achieve during Hall bar measurements. From the Hall bar measurement and knowing the resistivity ρ is also possible to calculate the hall mobility μ_H, defined by:

$$\mu_H = \frac{|R_H|}{\rho} \tag{2.19}$$

that differs from the conductivity mobility. The hall scattering factor express the difference between the hall mobility and the conductivity mobility, but in general for most Hall-determined mobilities r is taken as a unity [37]. The resistivity is determined in the absence of the magnetic field by measuring the voltage between the contact 2 and 4 and by 3 and 5 and averaging these values.

$$\rho_{24} = \frac{V_{24}}{I_{56}}\frac{WL}{T} \qquad \rho_{35} = \frac{V_{35}}{I_{56}}\frac{WL}{T} \tag{2.20}$$

averaging these value:

$$\rho = \frac{\rho_{24} + \rho_{35}}{2} \tag{2.21}$$

2.2.3 Ohmic contacts

In order to perform the electrical measurements, is necessary to have a ohmic contact in a metal-semiconductor junction. In such case the carriers are free to flow in or out of the semiconductor so that there is a minimal resistance across the contact. In this way, the influence of the metal-semiconductor junction to the measurement is minimized.

For a n-type semiconductor, like the samples studied in this thesis, this means that the work function of the metal must be close to or smaller than the electron affinity of the semiconductor. A critical step in order to create a ohmic contact is the choice of the metal that has to be deposited: is necessary to take in account the dopant type of the semiconductor, the work function of the metal, the electron affinity and the doping concentration. Current flow between the metal and the semiconductor involves losing of electrons from the contact to the material, resulting in the movement of charges. The tendency of a bulk material to lose electrons is characterized by its work function (Φ) which is an intrinsic property of the material used as a contact [2]. The relative values of the works functions of the two materials in contact establishes the movement of electrons to/from a material:

- if $\Phi_{metal} > \Phi_{semiconductor}$, there is a barrier potential that would have to be supplied by an external source before movement of charges occur;
- if $\Phi_{metal} < \Phi_{semiconductor}$ electrons can easily flow from the metal into the semiconductor.

Hence, a contact can be said to be ohmic if it satisfies one of the following condition:

- no barrier exists between the metal and the semiconductor;
- exists a barrier, but it can be overcome by the electrons (the barrier height is comparable to the ambient thermal energy);
- exists a barrier, but it is narrow enough to allow tunnelling effect.

2.2.4 4-probes method

To avoid the Hall bar fabrication process that requires the use of two different step of optical lithography and the deposition of metal contacts, there is also the possibility to determine the resistivity of uniform flat samples of arbitrary shape and then, using literature data, find the corresponding doping level. To calculate the resistivity the 4-probes method can be used.
In 1958 Van der Pauw demonstrated that there are two resistances R_A and R_B associated with the corresponding contacts shown in figure 2.4. The resistances are defined by the following formula:

$$R_A = \frac{V_{12}}{I_{43}} \qquad R_B = \frac{V_{23}}{I_{14}} \tag{2.22}$$

From these characteristic resistances is possible to determine the sheet resistance R_S and from this value is possible to calculate the bulk electrical resistivity ρ. R_A and R_B are link to R_S through the following equation [37]:

$$e^{-\frac{\pi R_A}{R_S}} + e^{-\frac{\pi R_B}{R_S}} = 1 \tag{2.23}$$

which can be solved numerically for R_S. The solution for symmetric samples (for example a square sample) is:

$$R_S = \frac{\pi}{ln(2)} \frac{R_A + R_B}{2} \tag{2.24}$$

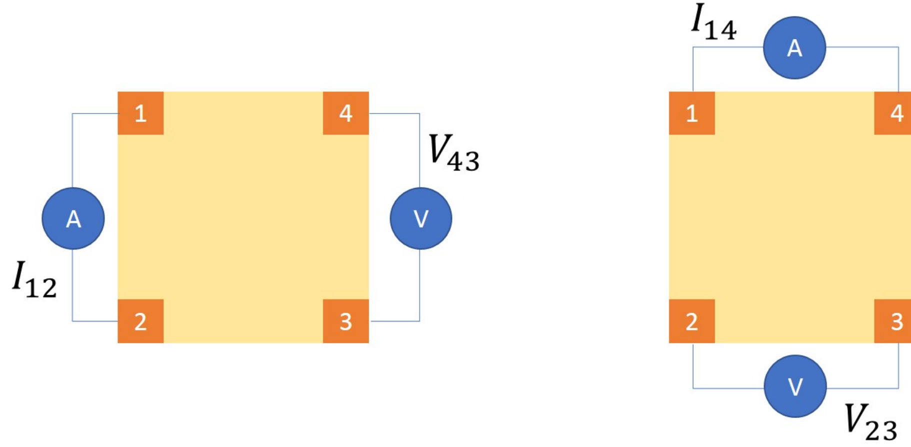

Figure 2.4: Schematic reproduction of the contacts of a square sample for Van Der Pauw resistivity measurements.

so the resistivity of the sample is:

$$\rho = R_S t \tag{2.25}$$

where t is the thickness of the sample. It is important to underline the presence of the 2 factor at the denominator of the equation, it is due to the fact that the contacts are positioned in the middle of the sample and not in the corner of the square samples, as in the classical Van der Pauw configuration [32].
From the measured value of the resistivity of the samples is possible to calculate the concentration value of the carrier in silicon using carrier mobility values derived from experimental data. In this work has been used the Thurber's formula [43]. The simplest equation that gives a fit of the same precision as uncertainty in the experimental data is the third-degree polynomial:

$$log_{10}\left(\frac{P}{P_0}\right) = \frac{A_0 + A_1 x + A_2 x^2 + A_3 x^3}{B_0 + B_1 x + B_2 x^2 + B_3 x^3} \tag{2.26}$$

where P is the product between the electronic charge (in the fitting the value used is 1.602×10^{19}), the resistivity and the electrically active dopant density.

The normalization factor P_0 was taken equal to 1 $\frac{Vs}{cm^2}$ and $A_i,\ B_i$ are the experimental coefficient presented in the table 2.1.

A_0	-3.0951	B_0	1
A_1	-3.2303	B_1	1.0205
A_2	-1.2024	B_2	0.38382
A_3	-0.13679	B_3	0.041338

Table 2.1: Coefficient for the fit for Phosphorus doped Silicon used in the equation 2.26

Chapter 3

Transistor Fabrication Process

The aim of this thesis is the fabrication of a MOSFET with a nanometric channel of size 200 nm x 50 nm, whose general process is shown in figure 3.1.
It is composed by the source on the left, the drain on the right and two gates: the lower one is the main gate, the upper one is the side gate as sketched in figures (3.2)(3.3). Generally six structure for sample are created and they are fabricated on a substrate of 145 nm of Silicon-On-Insulator (SOI) on $1\mu m$ of SiO_2. The general layout is created with the EBL software (E-Line), while the e-beam exposure and the e-beam deflection are controlled by Elphy Quantum Raith.
The first lithography step is the creation of the MESA (Fig.3.4), that corresponds to the Si-based transistor structure. It is made depositing a layer of negative resist AZ 7520, spin-coated on a cleaned SOI surface at 4000 rpm for 30 sec to have a resit thickness of about 150nm. The sample is then annealed at 85°C for 60 sec to evaporate the solvent within which the resist is diluted. After EBL exposure, development takes place in AR 400 37 ion-free developer for 50 seconds followed by 60 seconds in water to stop the process. A second baking is then performed at 85°C for 60 seconds to improve the properties of the negative resist and make it more resistant to the etching process. With the same process also two set of markers are fabricated, both of them are realized in the 100 μm $\times$ 100 μm Write Field to help the further lithography steps, in fact several alignments has to be done for the realization of the masks and the metallization.

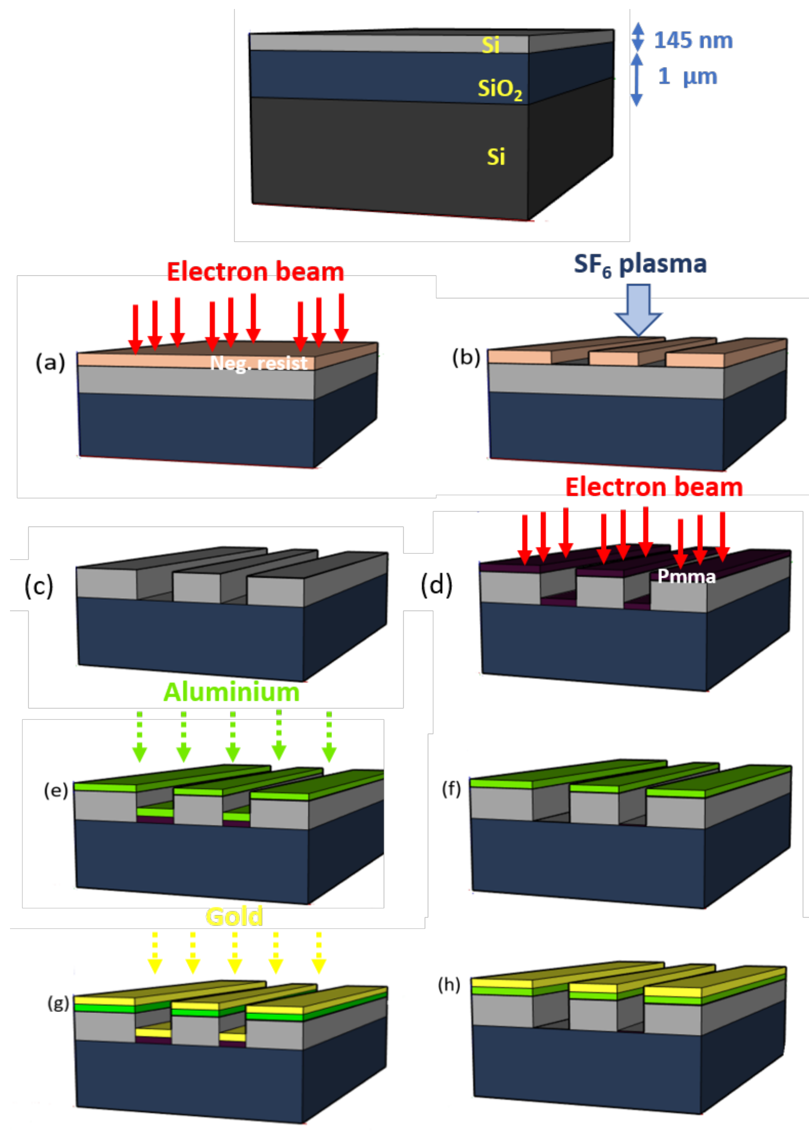

Figure 3.1: Schematic representation of the transistor fabrication process. **On the top** SOI structure of the sample with also the silicon substrate that will be omitted on the next figures; (a) sample spin-coated with negative resist and exposed; (b) patterning transferred on silicon using SF6 plasma (RIE process) on the developed sample; (c) sample after the RIE process; (d) exposure on the spin coated PMMA resist layer; (e) deposition of aluminium for the fabrication of the alumina oxide gate; (f) sample after the alumina lift-off; (g) deposition of metallic contacts (layers of aluminium on the gates and layers of titanium and gold for the source and the drain); (h) sample ready for the measurements after the final lift-off.

A dry etching process, by reactive ion etching (RIE) (A.4) is then performed. The RIE parameters are reported below:

- Gas SF6 250 sccm,
- Pressure= 0.8·10-4 torr,
- Power=50W,
- Duration=20 seconds

After the RIE process, the sample has to be cleaned from the resist not already removed with an ultrasonic bath in acetone for 15 minutes at 40 KHz and an oxygen plasma etching for 20 minutes at 500W. At this point the following step is to dope source and drain zone, so the procedure will continue with the creation of a mask that covers all the structures excepted them. In fact the doping procedure is made with an ion implantation of Sb made by CNR of Catania; this process doesn't have the possibility to select the zone to dope but it irradiates all the surface, so that brings to the creation of the mask. With this procedure the concentration of donors n reaches more than $10^{19} cm^{-3}$.

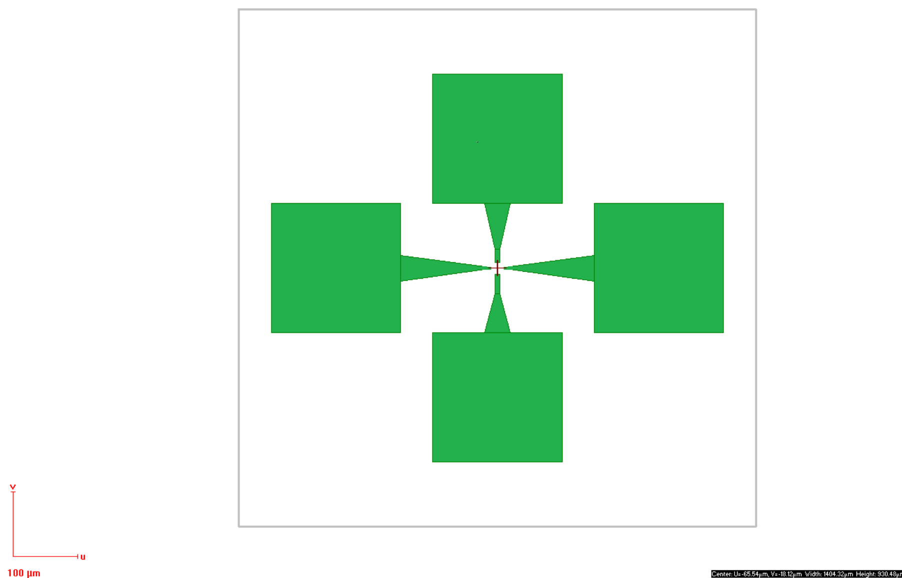

Figure 3.2: Top-view sketch of the desired geometry of the transistor realized using Raith Elphy Quantum PC software.

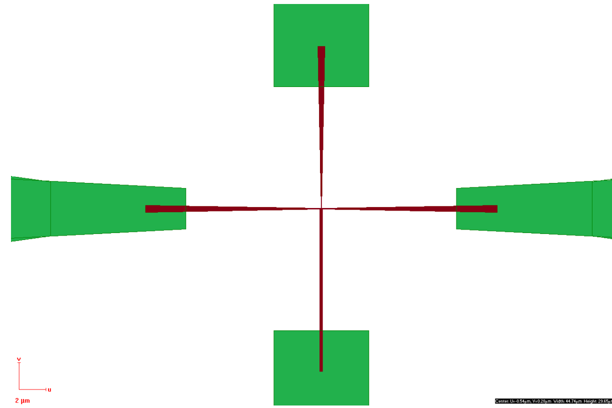

Figure 3.3: Zoom of the central channel of the transistor realized using Raith Elphy Quantum PC software.

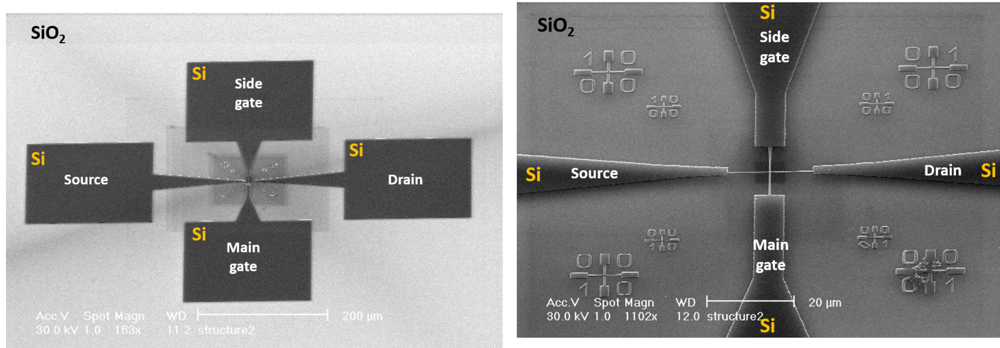

Figure 3.4: On the left: planar view SEM images of the typical MESA structure. The Si structure corresponds to the black areas. **On the right**: a zoom in of the central part of the structure that shows the thin Si channels.

The mask is made of a thick layer of 250 nm of SiO_2 deposited on the top of the sample through an evaporation with e-beam evaporator; to obtain a precise mask that leave uncovered source and drain is performed the so called lift-off technique, as described below. After the deposition of two layer of PMMA, the zone that has to be covered by the material deposited (in this case SiO_2) is exposed and developed. The markers play a key role in this step, in fact the exposition must be very precise to cover the nanometric silicon channel keeping it intrinsic. To obtain a correct lift-off procedure the sample is kept for at least 4 hours in acetone; the resist is kindly removed and the oxide layer together with it. The final result is a silicon dioxide mask that covers the two gate zone and the intrinsic silicon layer in the middle, leaving totally free to be ionized the source and the drain (Fig.3.5.a).

After the ionization procedure an RTA annealing has to be performed to activate and diffuse the Sb donors in silicon [41]; this treatment is performed at 800°C for

5 minutes in N_2. Before continue with the creation of the second oxide mask, the sample will be put in a 5% solution of HF for 1 minute to remove all the silicon dioxide.

An equal procedure is then made for the process of bismuth ion beam implantation, performed by the Prof.Jamieson's group in Melbourne. The only significant difference is the layout of the mask, in fact in this case the only region to be implanted is a 50 nm x 200 nm delineated over the intrinsic silicon channel. This modify makes all the process very complicated and with a low rate of success (Fig 3.5.b). A more detailed description of these two processes is in section (3.1).

After the annealing treatment made in Melbourne and the HF cleaning did in Como now the sample is ready for the more complicate step of the entire fabrication, the realization of a good dielectric layer. For this purpose two different attempts are tried, one with silicon dioxide(SiO_2) and the other one with alumina(Al_2O_3). The first one consists in a deposition of 80nm of SiO_2, but due to the formation of unwanted small cracks in the oxide layer, it doesn't isolate correctly the substrate from the metal subsequently deposited. Completely different result is obtained with the deposition of 15nm of a(Al_2O_3); this is performed depositing 5nm of aluminium in three different consecutive steps, allowing the oxidation between them. This is the most complicate and critical passage of the fabrication process, in fact if the dielectric layer is not well created the leakage current of the gate will be dominant respect to the one of the channel, ruining all the possible measurements.

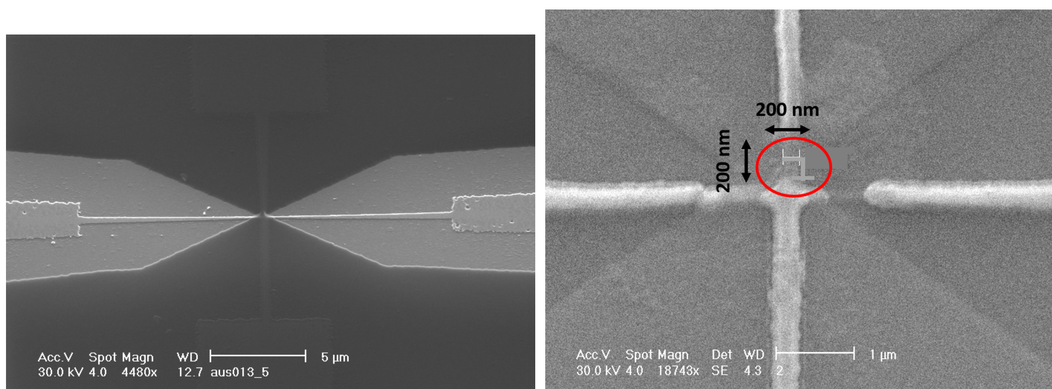

Figure 3.5: On the left: silicon dioxide mask of 250 nm for antimony implantation. The dark grey zone is the mask, while the light grey zones are the ones that will be implanted. **On the right**: silicon dioxide mask of 250 nm for bismuth implantation. The red circle underline the small region that is not covered by the mask and that will be implanted, the lighter grey channel are covered by the mask.

The last part to describe is the process of metallization that will create two gold

pads for the source and the drain, while the main and the side gate will be in aluminium. The two processes are made using the lift-off technique already described for the dioxide mask, and they are obviously performed in two different passages. For source and drain 5 nm of Ti are deposited before proceeding with 100 nm of Au, this is done to facilitate the gold adhesion that will be more critical in the direct case. On the other hand there are no problem for the adhesion of 100 nm of aluminium over the gate, but the main problems are related with the T-shape of the gate. In fact to have better performances a small T-gate of 100 nm is created over the intrinsic channel but due to its dimension the risk of being ruined is high.(Fig.3.6).

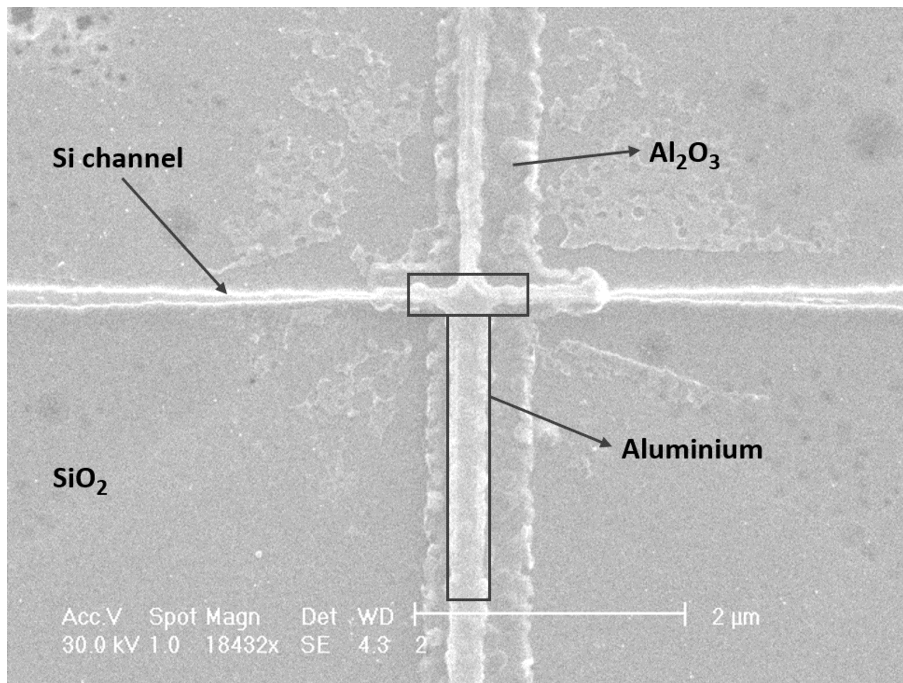

Figure 3.6: Plan view of the the aluminium T-shape gate, it is possible to observe a thinner channel of aluminium over a widerr one that it is the alumina oxide layer.

3.1 Ion Beam Implantation

In order to obtain an high level doping for source and drain zones an Sb implantation is performed by CNR of Catania. This procedure allows to have doped region of n^+, and several simulation has been performed in order to find the correct energy to apply to reach a doping level concentration suitable for an ohmic contact $n \sim 2 * 10^{19} cm^{-3}$. At the end two different profile are performed, one at 140 KeV with a fluence of $1.1 * 10^{14} Sb/cm^2$ and another at 100 KeV with a fluence of $0.85 * 10^{14} Sb/cm^2$, reaching a depth from 50 to 100 nm(Fig 3.7). After the annealing and cleaning process already described, a quick electric test is made to check the correct behaviour of the doped regions.

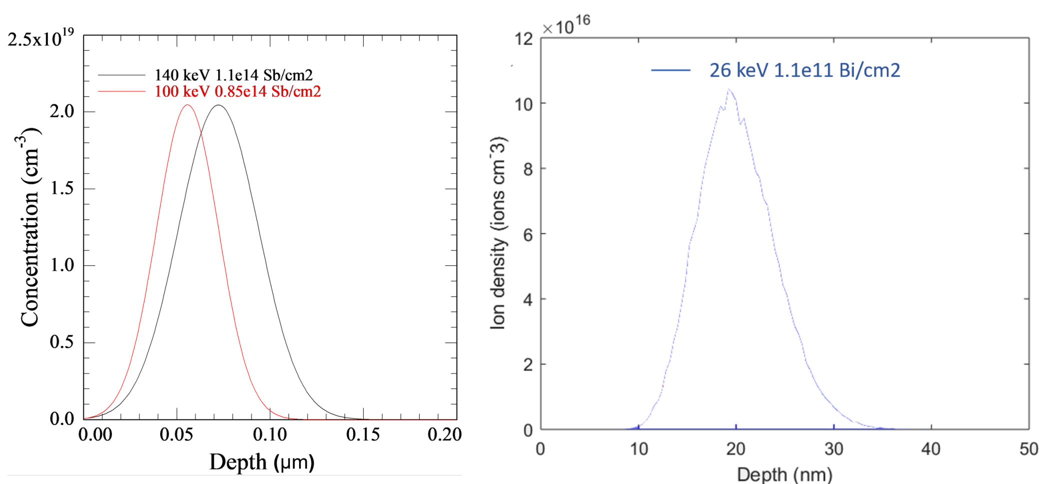

Figure 3.7: On the left: ion implantation profile for Sb. The black curve is the higher energy implantation, while the red curve is the lower. **On the right**: ion implantation profile for Bi. Ion density of $\sim 10^{17}$ ions $/cm^{-3}$, with a depth around 20 nm.

More complicated is the procedure made for the bismuth implantation. In a nanometric region between the main and the side gate, several bismuth ions were implanted with a energy of 26 KeV and a fluency of $10^{11} Bi/cm^{-2}$ in order to have the near-surface implanted region (between 10-30 nm), as described in figure 3.7. About the annealing process, for the given low fluence of near-surface Bi, the suggested annealing treatment is of 1000 °C for 60s ($\sim$ 42% electrical activation yield, diffusion length $\sim 8nm$ [19]), but to avoid segregation problems with Sb, annealed at 800 °C, another method is tried. According to the studies already performed by the Jamieson's group in Melbourne [19] the final decision is to perform the annealing treatment at 800 °C for 5 minutes in Ar, in order to obtain an electrical activation yield of around 30% (Fig .3.8). The final result is similar to the one shown in figure 3.9.

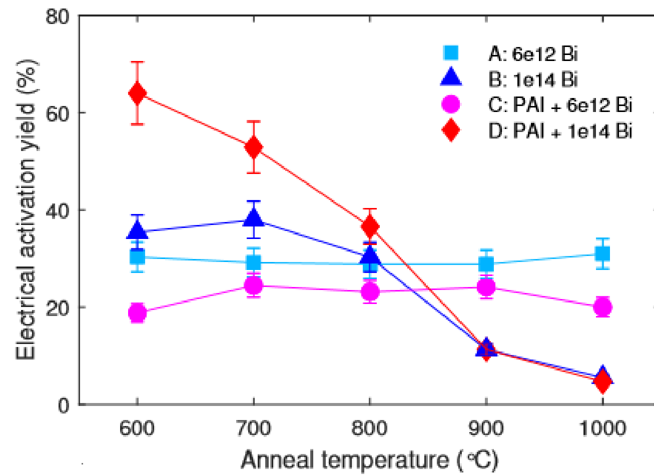

Figure 3.8: The figure shown the electrical activation profile in function of the temperature. The colour represent different implantation fluence, the light blue squares are the better representation of our case, showing a constant 30 % of electrical yield activation. From Ref.[19]

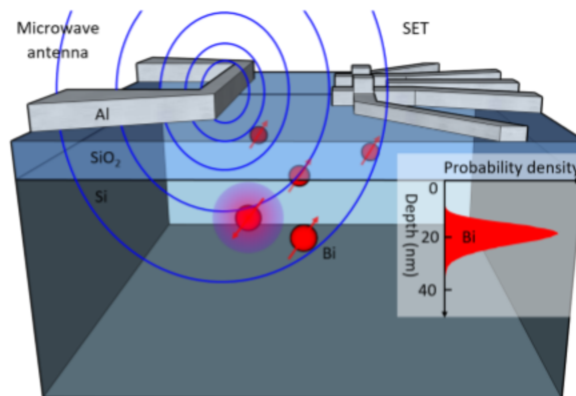

Figure 3.9: A view of a device similar to the one fabricated by ourselves. This view underlines the presence of bismuth single atom near the surface. From Ref.[19]

3.2 Sod Treatment

A completely different method used to reach high level of doping in silicon structures is with the deposition of a layer of Spin On Dopant(SOD). The SOD used in the experiment is the P508 produced by Filmtronics - semiconductors process materials - it is a solution with 8% of phosphorus and with 5% of silicon oxide, as specified from the product datasheet. Before the application, as in the other case of doping previously described, a silicon dioxide mask has to be created in order to avoid to dope unwanted region.

It is manually applied with a polyethylene dropper and spin coated for 30 seconds at velocity of 3000 rpm to obtain a thin and uniform film, all this procedure are made on a controlled environment in order to prevent the cloudiness of the SOD layer. After spin-coating process, the sample does a heat treatment on a hot plate to preclude adverse condensation and to allow the evaporation of volatile solvents: it is baked for 10 minutes at 55 °C and then they are baked for 15 minutes at 120 °C. The sample is now ready for rapid thermal annealing (RTA) process. It is made in a nitrogen atmosphere with a super fast ramp that allows to reach 900°C in 9 seconds, based on which level of doping is wanted the process can be of different lengths and at different temperatures. After the rapid thermal annealing the remainder SOD film has to be removed from the surface of the sample, so the sample is treated in a solution of deionized water and HF (DHF) and rinsed in deionized water. The dilution used is of 5% (HF 50% Vol; 5:45 HF:H2O at room temperature), the bath time changes from 25 seconds to 2 minutes depending on the treatment of the RTA process. After the DHF, to remove completely the spin on dopant layer and to clean the surface from organic matter, the sample is subjected to a oxygen plasma asher treatment for 30 minutes using a power of 1000 watts.

3.3 Problems in fabrication

This paragraph will be a sequence of the several issues that have been found during the different fabrication steps. In fact the fabrication often is a long optimization process, during which you are going to optimize several different parameters that allow you to succeed in reaching nanometric scale with a very high precision. At the beginning, the first parameter to find is always the dose. As described in (A.2.2), it's the parameter that will go to determine the amount of charge that will expose the resist layer. The correct dose was of $60\mu C/cm^2$; lower doses of $40\mu C/cm^2$ give problems of underexposed incomplete structures, while higher doses of $120\mu C/cm^2$ and $150\mu C/cm^2$ create some over-exposition as shown in figure 3.10.b.

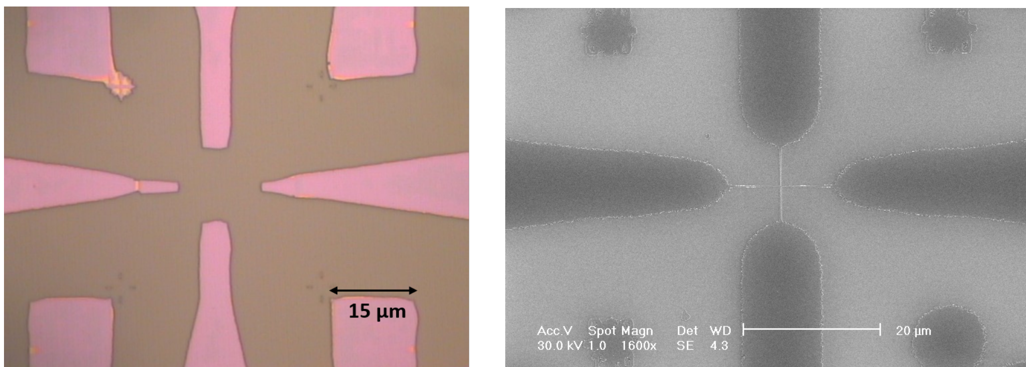

Figure 3.10: On the left: Optical microscope image of an incorrect exposure due to a not well focused beam. **On the right** SEM image of an overexposed structure due to a wrong dose

Another delicate step is the alignment procedure, in order to create complex structures, it is often required to make lithography step over a zone already patterned. To do that several markers are patterned with the structures; by the way due to the nanometric dimension of the certain region, a very high precision is required and can occur some issues as a small shift or an incorrect angle tilt (Fig.3.11.c.). The last common problem that can be found is the one related to an incorrect lift-off procedure (Fig.3.12.d.). Sometimes happens that the metal or the oxide deposited on the top of material, instead of being removed together with the resist, remained there. This phenomena is observed when the the deposited material covers totally the resist and basically stop the action of acetone.

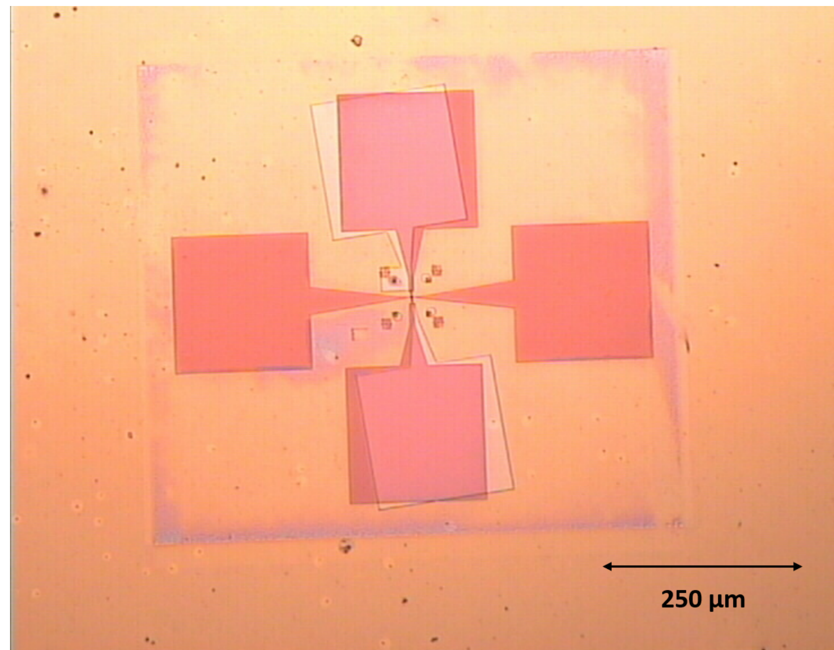

Figure 3.11: Optical microscope image of an incorrect angle tilt. The lighter part is the incorrect exposition that should cover exactly the structure of the pads.

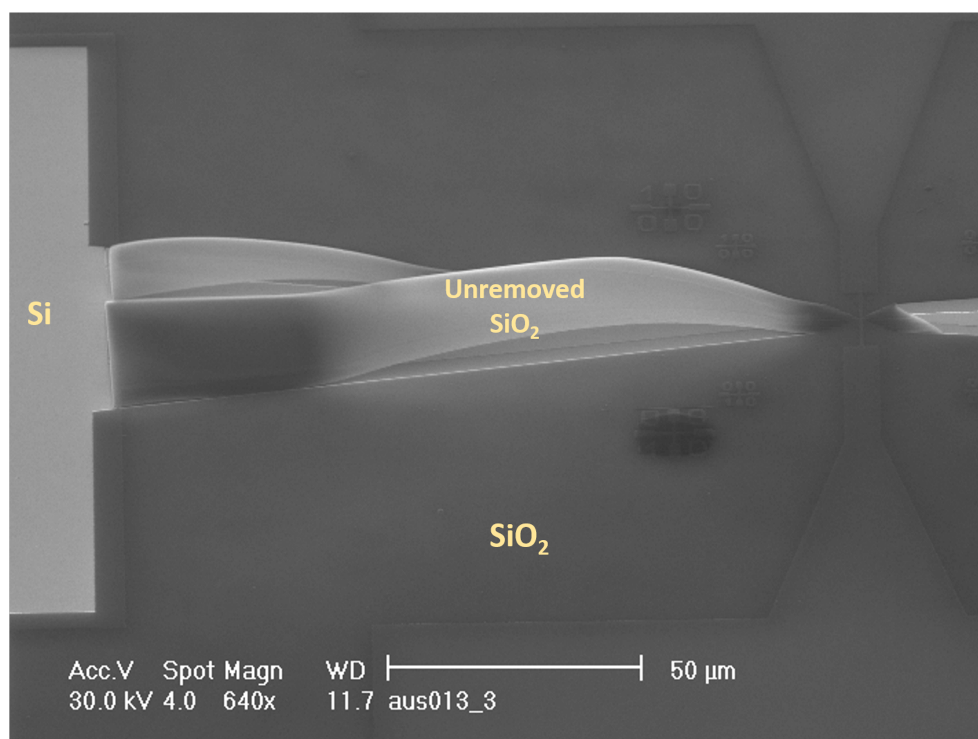

Figure 3.12: SEM image of an incomplete lift-off, the silicon dioxide doesn't go away correctly and it creates a kind of wave over the silicon region where it should be gone.

Chapter 4

Experimental results

In this chapter the most relevant results obtained during the thesis activities are discussed. The fabrication process has been complex and long due to the several collaborations and steps that has been performed in different part of the Italy and the world. Up to now, the electrical characterizations of the single bismuth atom transistor for solid state Atomic Clock applications are double: a first one at room temperature, and a second one at 4K using the cryostat. Both of them can be defined as preliminary, in fact the idea is to check if the device created shows a behaviour similar to a nanoscale transistor, in order to decide if it is convenient to continue with more advanced measurement that should allow to detect also the interaction with bismuth atoms expected. These first results detailed below show a promising behaviour. In the first part of this treatment are analyzed two equal samples that for simplicity will be called sample A and sample B, both of them are doped with a technique of ion implantation beam of antimony. Each sample has six devices of two different types (three equals on each line), that differs for the width of the central channel that is larger of 30 nm in the upper line. In the second part of this chapter, are discussed the results obtained with a sample of the same geometry but doped with spin-on-dopant(SOD) process. Before starting with the description of the results, a couple of image of the final devices are shown in figures (4.1)(4.2).

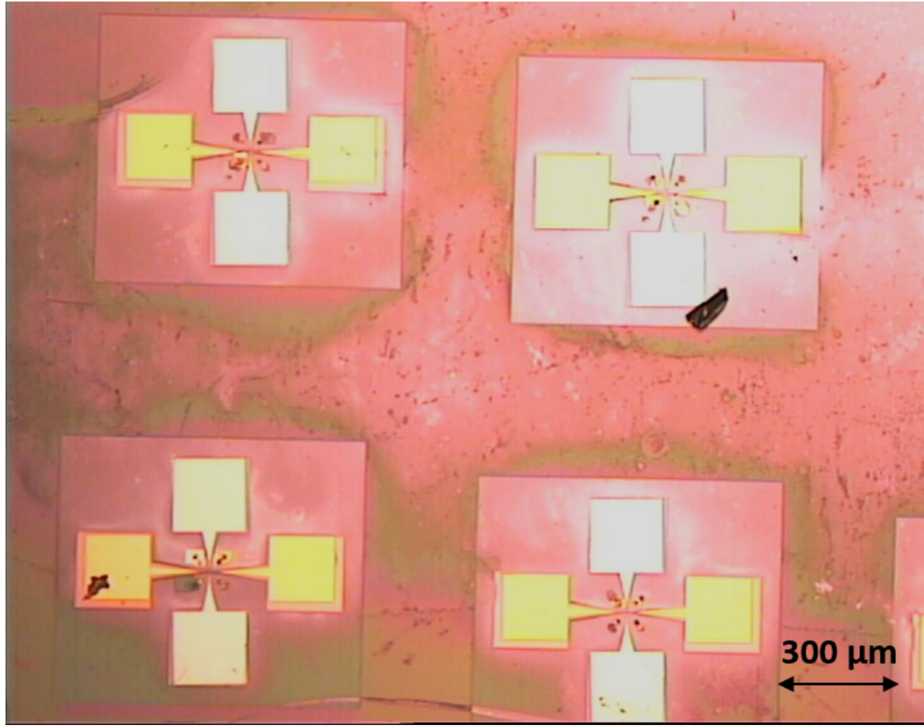

Figure 4.1: Planar view of the final sample obtained with optical microscope. Four structures are shown of two different type, the upper line present an inner channel of 80 nm; the lower line has an inner channel of 50nm.

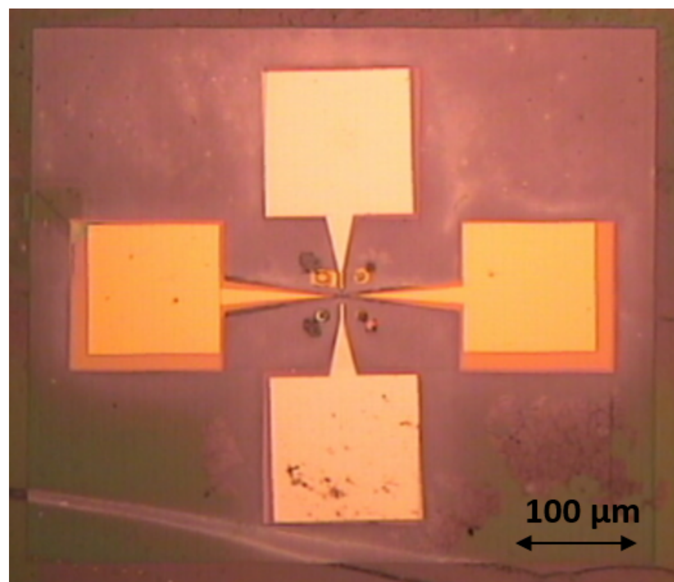

Figure 4.2: Zoom image on one of the structure. The left and the right square pads of 200x200 μm are the source and the drain, covered by gold. The up and the bottom pads are respectively the side gate and the main gate covered by aluminium.

4.1 Sb ion beam implanted sample

4.1.1 Room Temperature Measurements

As briefly introduced before, the first electrical characterization is the one performed at room temperature. In order to see if the device realized it behaves as a mosfet, the first analysis is done applying a difference of voltage just between the source and the drain in order to check if it is sufficiently doped and if the channel links the source and drain contacts. Our analysis is conducted principally on the results obtained of two structures on the sample A, called Structure 2 and Structure 3 for their position. The sample B does not present interesting measurements at room temperature due to the high leakage current presents between gate and source. Anyway it is already important to underline that these devices are built in order to work correctly at cryogenic temperature so, as explained exhaustively later in the next section, the possibility of having these high leakage current won't necessarily be a problem.
The results in figure 4.3 shows that in the range between -0.1V to 0.1V for the source to drain voltage V_{DS} the source to drain current I_{DS} linearly goes up to 300 nA in absolute value. This demonstrates the ohmic connection between source and drain and so the successful doping procedure; another interesting thing to observe is how the curves are perfectly symmetric around 0 V, testifying the absence of offset.

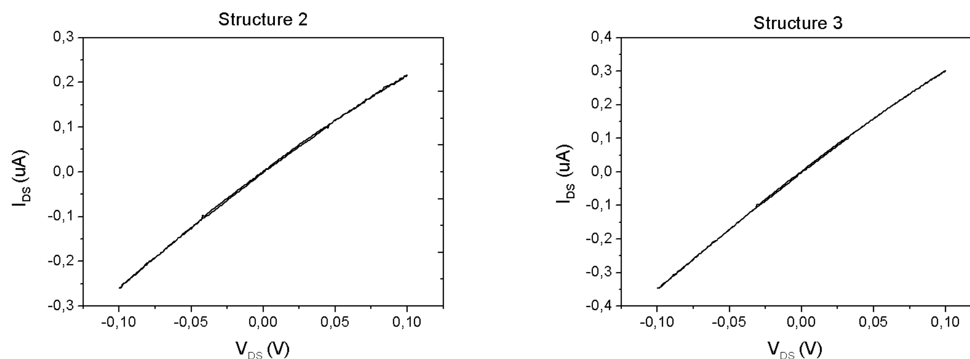

Figure 4.3: The ohmic behaviour of Structure 2 and Structure 3 of Sample A, the current reached is of $250nA$ and $350nA$ respectively.

As discussed in chapter 3, the fabrication of a good dielectric layer is always complicate, and if it is not correctly done it is possible to observe an high leakage current. While for the sample B this problem cannot allow room temperature

measurements, for the structures of Sample A the results about the leakage current are very successful in fact just a maximum of tens of pA is detected, that are more than 2 order of magnitude lower than the source to drain current I_{DS}; these values are comparable with an instrumental noise with a variance $\sigma^2 = 4,13^{-24}A^2$. In order to understand if the device fabricated is properly a transistor the gate voltage V_G must be applied. The measurements in both the structure previously analyzed are obtained keeping constant the V_{DS} at 100 mV and are shown in figure 4.4. Even if it is not possible to delineate a proper characteristic curve in which you can delineate the threshold voltage of the transistor and the different working regions, it is still important to see that the gate voltage can modify and modulate the passage of current in the channel. With a variation of V_G that goes from -0.6mV to 0.6mV for Structure 3 and from -0.4mV to 0.4mV for Structure 2, the ΔI observed for a step of 100mV is around 25nA. The last analysis

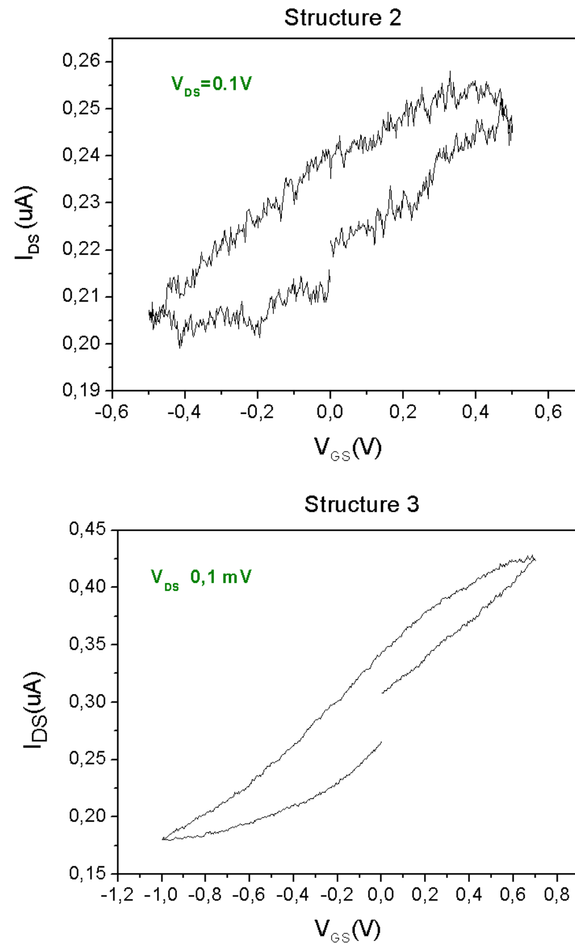

Figure 4.4: The source to drain current I_{DS} in function of the gate voltage V_G. For Structure 2 the values go from 200nA to 250nA, while for Structure 3 they go from 200nA to 450nA. An hysteresis phenomena is observed.

performed at room temperature is a kind of resume of the previous one. In fact the graph(Fig.(4.5)) shows basically two things, the first one is that increasing the V_{DS} the amount of current increases as expected and the second one is that V_G modulates the current also for higher value of V_{DS}. In order to conclude this first analysis it is possible to say that the devices seem to work as a transistor, even if we could not delineate the threshold voltage. This is probably due to the fact that the system is projected for working in a low current regime and so in cryogenic condition.

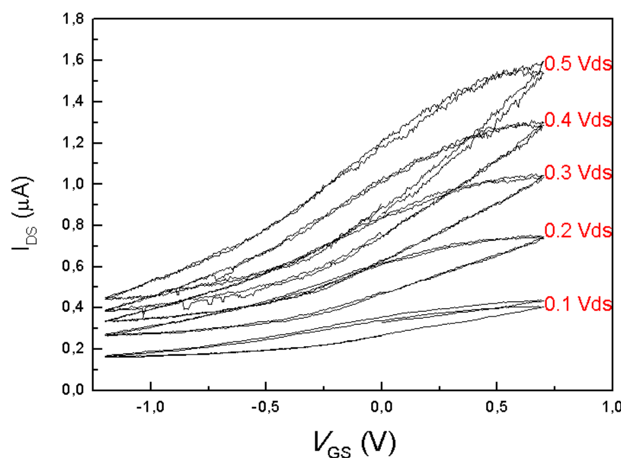

Figure 4.5: I_{DS} in function of V_G. Five different measurements are presented in the same graph in order to observe the difference applying an increased V_{DS}, from 100 mV to 500 mV.

4.1.2 Cryogenic Measurements

The measurements at 3K are performed using the cryostat setup(A.7.2) located in LNESS laboratory. In order to use this experimental setup, the sample must be cut in a $4mm$ x $4mm$ piece to enter in the apposite chip carrier and then have to be bonded. Working in a very low temperature regime, undoped silicon channel reduces its conductivity due to the freeze out of charge carriers at low temperature [46] [34]; so the expected value of current will be lower compared with the room temperature measurements. Due to the noise of the instrumentation that in theory it is not suitable for this kind of measurement, it is very difficult to detect variation of current that is expected in the order of pA. Anyway the Structure 5 of sample B shows a very interesting preliminary behaviour; by plotting the variation

of the I_{DS} in function of the V_G we theoretically expect to see a behaviour closer to the one of figure 1.5. If we observe the different graphs (Fig.4.6)(Fig.4.7), first of all it has to be observed that the magnitude of the current is just of tens pA and that it is possible to delineate the presence of two different working regions: one almost flat, that will be our region of interest, and the other one linear that coincide with the active region of a transistor.
Now, by focusing the attention on the first region (On the right Fig.4.6), it is possible to make a comparison between the step curve and the undulating behaviour expected for a Coulomb Blockade oscillation. In fact the resolution of the system is not high enough to detect the points of the peak of the wave, even if this result is not so clear, it still shows a particular behaviour before the formation of the channel and it is very promising for the next high resolution measurements planned. Anyway this is just a suggestion and that curve trend could be simply a telegraphic noise obtained due to the very low value of the current.

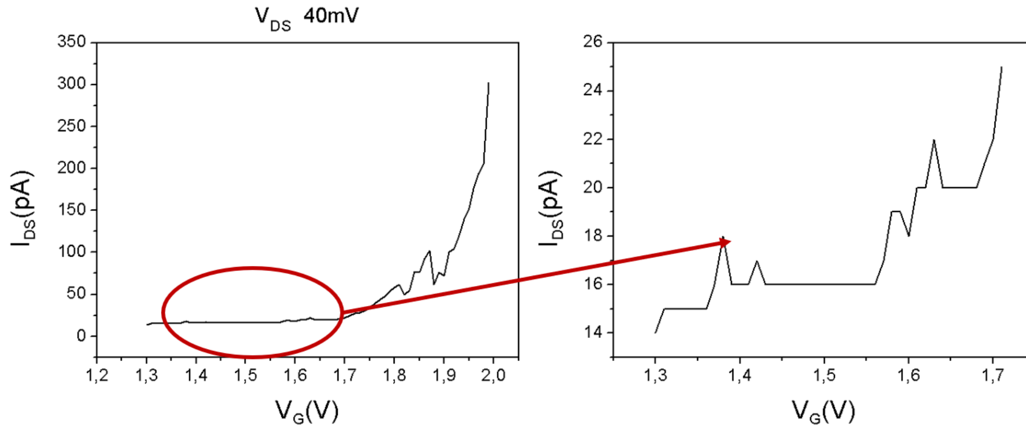

Figure 4.6: On the left: the drain source current I_{DS} of Structure 5 in sample B in function of the gate voltage V_G, with a V_{DS} of 40 mV. **On the right**: a zoom on the initial part of the previous curve in which it is possible to delineate a step behaviour probably due to Coulomb Blockade oscillations.

A system of measurement with an advanced experimental setup provided of a series of amplifier will be surely clarify this fact. All the three measurements, with different V_{DS} ($40meV$,$70meV$,$90meV$), show a typical transistor behaviour and a correct increment of current with the voltage V_{DS} (Fig.4.7). Unfortunately, the analysis about the hypothetical Coulomb Blockade region was possible just for measurement around 40 meV, in fact reducing this value of drain source voltage the noise component becomes too much relevant comparing with the signal, on

the other hand by increasing too much the V_{DS} the system loses the sensitivity to detect properly this small variation of current. About the three measurements performed it is possible to calculate a more or less precise value for the threshold voltage that can be detected around 1.8 V.
The last figure (Fig.4.8) shows that increasing the gate voltage, the system enter in the ohmic region for lower value of V_{DS} as expected. Unfortunately, due to problems with the bonding procedure and non ideals introduced by the fabrication, the other structures of sample B don't show other interesting results.

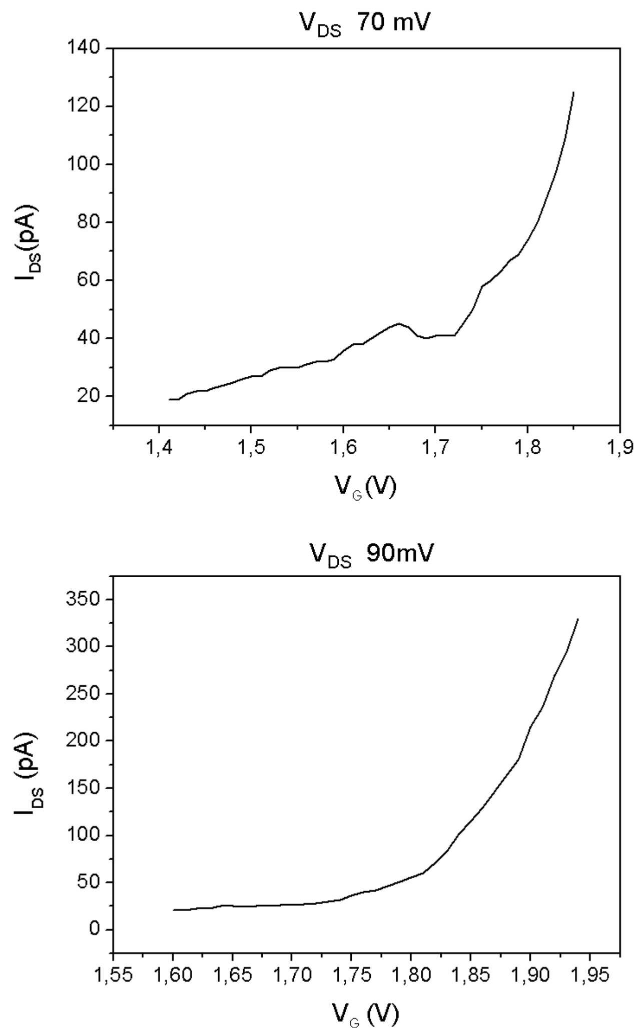

Figure 4.7: Two typical transistor curves obtained for $70mV$ and $90mV$ at cryogenic temperature. In both the case it is possible to suppose a threshold voltage of 1.8V.

By moving now on the sample A an analogue analysis were performed; the result that will be shown come from the Structure 2. In this case it was not possible to reach the detection of current of pA probably due to the high noise produced by

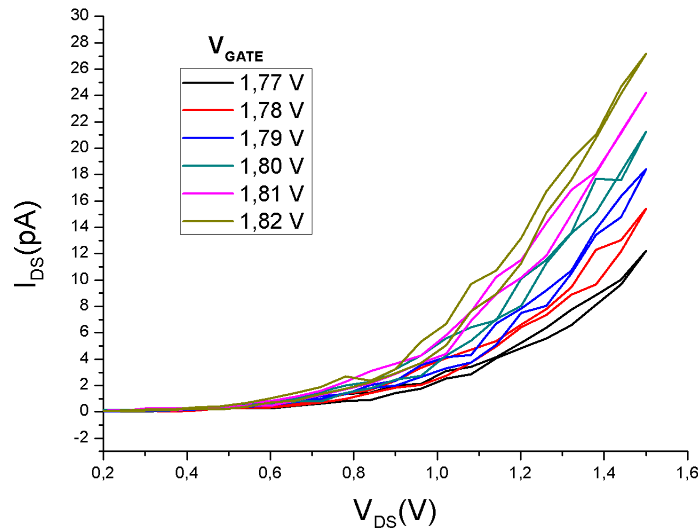

Figure 4.8: The effect given by the variation of the gate voltage V_G on a plot of I_{DS} in function of V_{DS}. The increase of V_G anticipate the formation of the channel.

the instrumentation in contact with this different device, so we move our analysis in order to see if the device fabricated behaves correctly as a transistor also at low temperature trying to detect a suitable value for its threshold voltage. From the two graphs shown in figure 4.9 it is possible to see that in this case, with a $V_{DS} = 100mV, 120mV$ the order of magnitude of the current is of nA, much higher than in the previous sample so it has no sense to look for a Coulomb Blockade trend that it is typical of lower current. Furthermore a leakage current (the red curve Fig.(4.9)) of few nA is observed and it increase faster than the drain current for voltage over 1V make impossible to have reasonable results in that range. Anyway in both the case it is possible to delineate a threshold voltage around 0.78 V, and this value is more or less confirmed also applying a negative drain source voltage $V_{DS} = -100mV$, in fact from figure 4.10 the voltage threshold is a bit lower but comparable, around 0.7 V. The value of current in the figure 4.10 is reported in absolute value in order to make the comparison easier. In order to explain the difference obtained about the threshold voltage in the two samples, we have to bring back it at the difficulties had during the gate oxide fabrication, that even if it is done in the same way for both the structures, it can have some thickness differences that brings to a different threshold value.

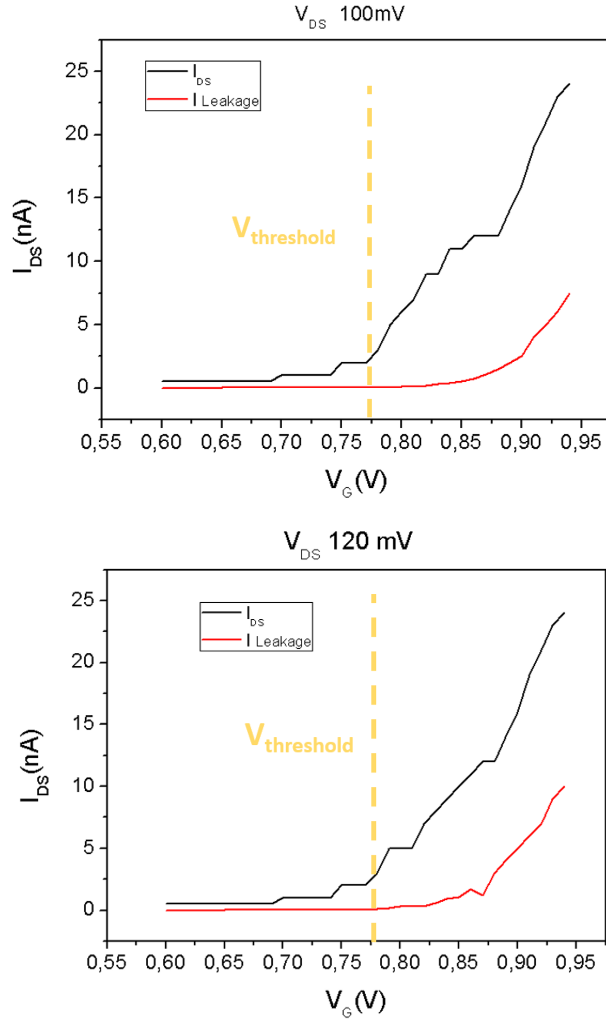

Figure 4.9: Two graphs of I_{DS} in function of V_G for Structure 2 in Sample B for $100mV$ and $120mV$ of V_{DS}. The black curve represent the I_{DS}, the red current is the leakage current I_G and the dashed yellow line represents the point chosen to define the threshold voltage. Despite the relatively high V_{DS} bias, a reminiscent oscillation can be observed around 0.85 V_G

4.1.3 Preview of next planned measurements

It may be useful to recapitulate the measurement situation achieved, we were able to demonstrate to have fabricated nanoscale transistor doped with Sb and Bi that works correctly at cryogenic temperature, showing a typical mosfet trend and with the possibility to find their threshold voltage. Anyway in order to complete our work, the last step to make it is to try to detect the ionization of the bismuth donor charge state. As previously said, a more advanced setup is required in order to observe this phenomena and for reason related to the delay of the helium delivery they will be performed a week after the final draft of

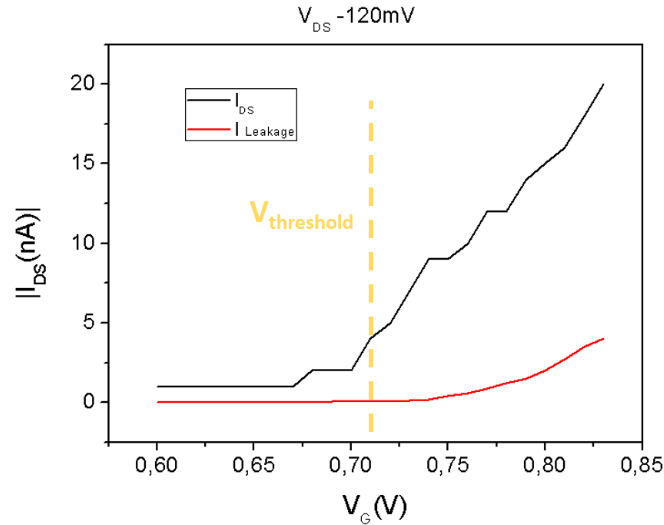

Figure 4.10: I_{DS} in function of V_G for Structure 2 in Sample B for -120mV of V_{DS}.In this case the threshold voltage is lower, around 0,7V. The current values are in absolute value.

this thesis. For the sake of completeness, a typical measurement similar to those required in the next steps of this study is reported. The graph presented on figure 4.11 is the conventional stability diagram (as advanced in Fig. 1.7), it is obtained from a n-type transistor and it describes the value of the source to drain current I_{DS} in function of the variation of the gate voltage V_G and the drain source voltage V_{DS}. By varying the value of V_G keeping constant V_{DS} at 0 V, it is possible to see how the system is moving in different regions of conduction; the darker regions represent where the current is suppressed and so where the Coulomb Blockade effect is active, the yellow regions represent where the electrons are flowing. By looking the entire graph and considering the modulation also of V_{DS}, it is possible to detect the creation of the characteristic diamond region due to the Coulomb Blockade effect.

The graph shown in figure 4.12 is a V_G-V_{bulk} stability diagram in a nanotranistor equipped of a bulk contact, that in our case will be represented by the side gate. It describes the value of the source to drain current I_{DS} in function of the variation of the gate voltage V_{GS} and the bulk voltage V_{bulk} with a constant value of drain source voltage V_{DS}. The purpose of showing this graph is not of focusing on the numerical values but to observe with attention the particular shape of the diagonal lines. First of all when the device is cooled at 4K in the quantum dot regime, the Coulomb blockade of the source/drain current can be shifted along V_G by the change of the ionization state of a single donor. By starting from this

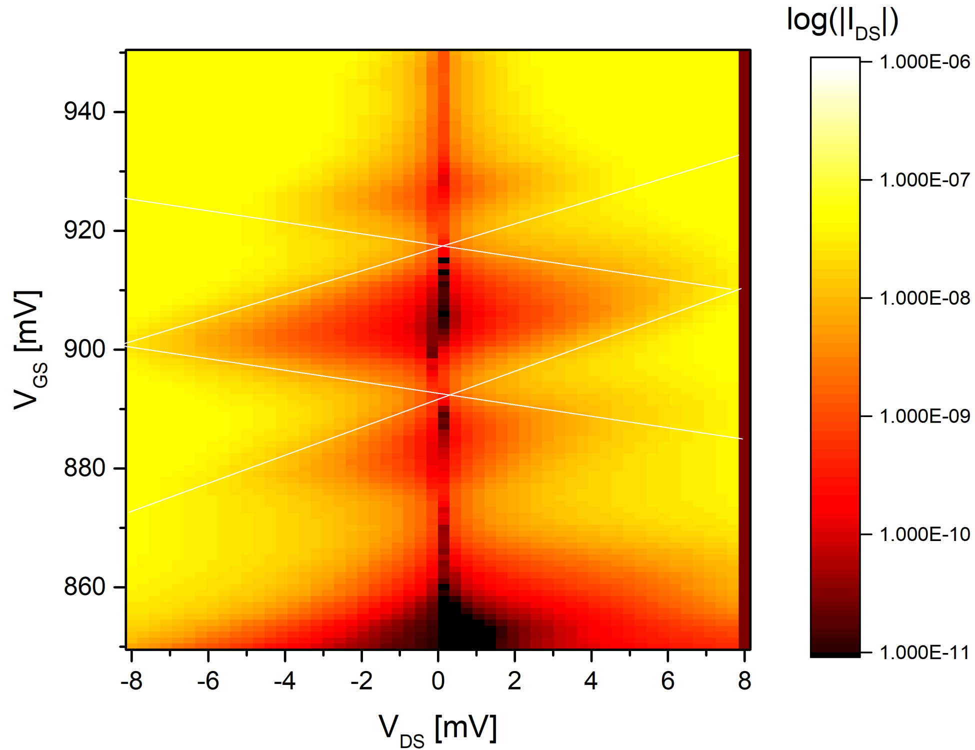

Figure 4.11: Stability diagram of a n-type mos. It is represented how the value of current I_{DS} changes in function of V_G and V_{DS}. It is possible to observe in the middle some orange and red rhombus that represent the Coulomb Blockade region where the current is suppressed. The yellow part are the zones where the electron flows form source to drain.[Data not published].

point it is observed that the stability lines, that represents the working regions of the device, undergo a shift due to the coupling between the donor and the quantum dot, shifting the lines of the quantum dot. In the figure 4.12 the green lines represent the zones of electron conduction, while the blue ones represent the Coulomb Blockade regions; it is possible to observe that some green lines are interrupted and shifted at another value, that probably shows the ionization of the donor atoms.

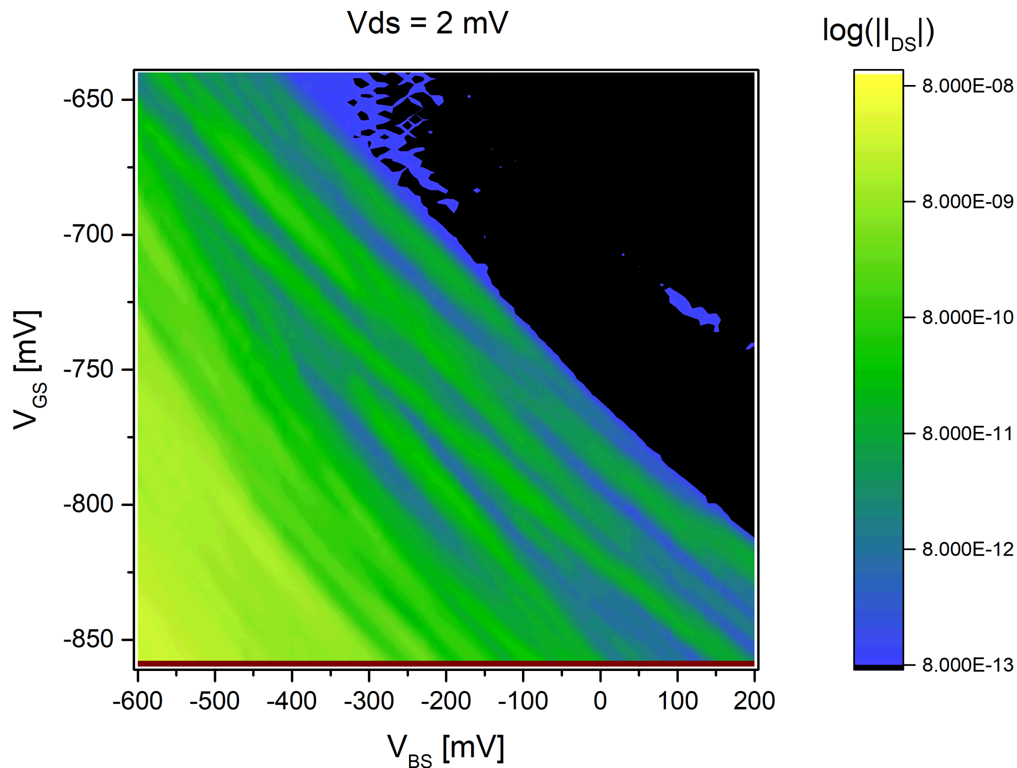

Figure 4.12: Stability diagram of the I_D vs. V_G and V_{side} in the quantum dot region near the ionization of one donor acquired at 4.2 K in a commercial p-type transistor. The green zones represent the region where the current flows while the the current is suppressed in the regions coloured of blue. [Data not published].

4.2 Spin on dopant method and its application into Transistors

Not having in LNESS a dedicated tool for implantation and waiting for the Sb doped samples from Catania, a low cost spin on dopant procedure have been carried out to dope the Si transistor. To understand which is the correct model to use, it is possible to study how the doping level of the sample changes according to the annealing time and temperature of the RTA process, as briefly described in the section (3.2). For these studies some Hall Bar and 4 probe electrical characterizations have been carried out.
Here is reported the analysis for the samples at 880°C , from the graph plotted in figures (4.13)(4.14), obtained from the series of samples annealed at the maximum temperature of 880 °C, is possible to notice that the doping level varies linearly with the square root of time, as highlighted by the linear fit (blue line). The same

Temperature of annealing (°C)	Time of annealing (s)	n_{3D} 4-probes ($\frac{atoms}{cm^3}$)
880	10	$1,30 * 10^{19}$
880	20	$1,93 * 10^{19}$
880	30	$2,84 * 10^{19}$
880	60	$6,02 * 10^{19}$
880	90	$6,96 * 10^{19}$

Table 4.1: Doping value of the samples treated with SOD and RTA process in function of the time. Temperature of annealing: 880 °C. The doping level have been measured using the 4-probes method.

behaviour is predicted by the diffusion model which assumes the presence of an infinite source of dopant. Indeed the doping level is the integral of the diffusion profile of the concentration of dopant normalized with the depth of the silicon layer where the dopant diffuse (x_p).

$$n_{3D} = \frac{1}{x_p}\int_0^{+\infty} c(x,t)dx = \frac{1}{x_p}\frac{2c_0}{\sqrt{\pi}}\sqrt{Dt} \propto \sqrt{t} \tag{4.1}$$

where $c(x,t)$ is the concentration profile described by the equation 2.5 (see section 2.1).

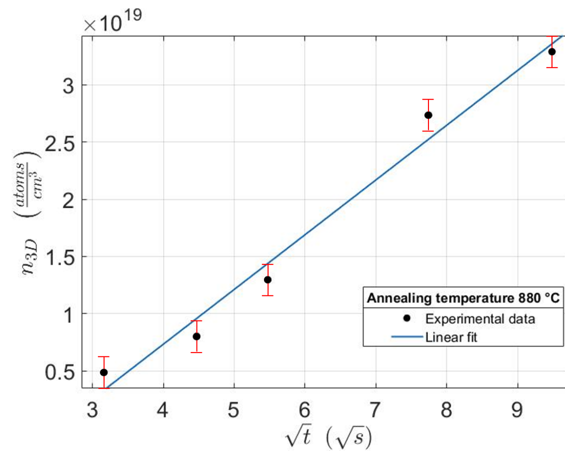

Figure 4.13: Plot of the doping level ($\frac{atoms}{cm^3}$) of the samples (annealed temperature 880 °C) versus the square root of the annealing time ($\sqrt{second}$). The doping level are extracted from the 4 probes measurements.

The choice that is made for actuate this doping procedure on a transistor is the one at 880°C for 60 second, in order to have a concentration of donors over $2 * 10^{19} cm^{-3}$, without reaching the higher temperature that are more difficult to

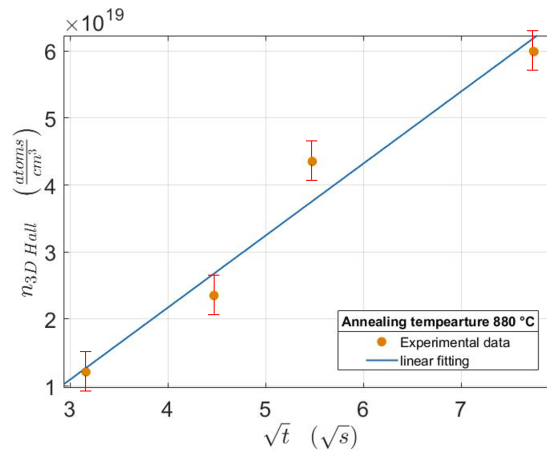

Figure 4.14: Plot of the doping level ($\frac{atoms}{cm^3}$) of the samples (annealed temperature 880 °C) versus the square root of the annealing time ($\sqrt{second}$). The doping level are extracted from Hall bar measurements.

control. Now we can look at the results obtained for this doped transistor, starting with an analysis similar to one made at room temperature. The first result shown in figure 4.15 is simply the electrical check between the source and the drain in order to see if the sample is doped and if the channel links the two parts. By watching the results of hundreds of μA obtained and the ohmic profile described, the doping procedure seems to be successful. After this check about the level of

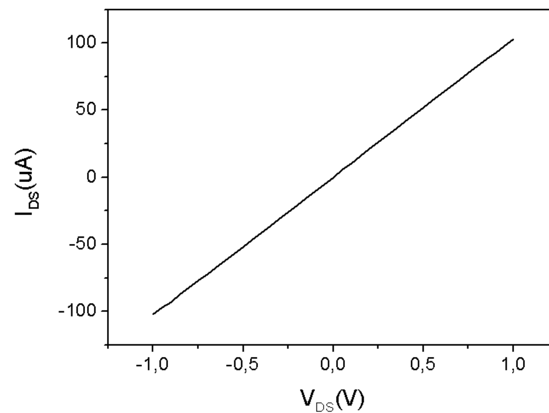

Figure 4.15: The ohmic behaviour of the structures measuring the drain to source current I_{DS} in function of V_{DS} , in this case the current reaches value of hundreds of μA due to the high doping level.

doping achieved, now also the transistor behaviour has to be investigated. The measurements made are shown in figure 4.16 and it is possible to see an increment of the current related with the gate voltage that goes from 0,2V to 1,9V; anyway it is not possible to delineate the presence of different working region, neither a

significant slope of this trend so the increment of current could be related just to a leakage effect.

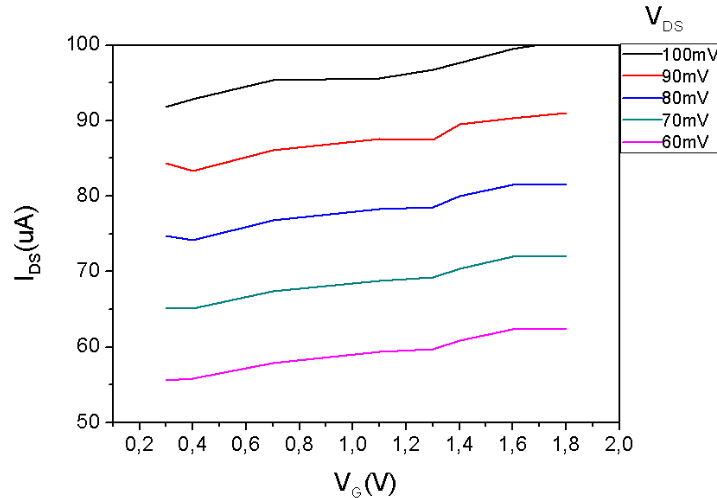

Figure 4.16: Graph that show a possible transistor behaviour in a I_{DS} curve in function of V_G. The different colour indicates different value for the drain to source voltage. Anyway the increase of current seems to be not so relevant and due to leakage effect.

4.2.1 Work in progress for the dielectric problems

If in the case of implanted sample the passage between the room temperature measurement and the cryogenic one, introduce a sensible improvement of the global transistor results due to a sort of freeze of the leakage charges. In the case of SOD doping, it has been observed that the leakage problem remains and it is not a negligible component as in the other case. The reason of this issue has to be searched in the quality of the deposited oxide, in fact as previously described, the technique used to deposit alumina it does not always guarantee an high quality layer and by considering the not perfectly flat surface obtained due to the presence of SOD previously spread on the surface, the formation of crack in the oxide it is more possible than in the implanted case.
In order to avoid this problem two alternative processes have been thought. The first one is related to the use of a more suitable technique for oxide deposition such as atomic layer depositor(ALD). The second option consists into introduce another lithography step; due to the high aspect ratio of the 145 nm channel, the oxide layer could be present some breaks along the height of the channel due

to this thickness difference. The idea is to put a substrate of silica of 100 nm around the channel with a fabrication process (4.17), in this case the aspect ratio will be significantly reduced by 2/3 and the alumina layer has less possibility to be broken.

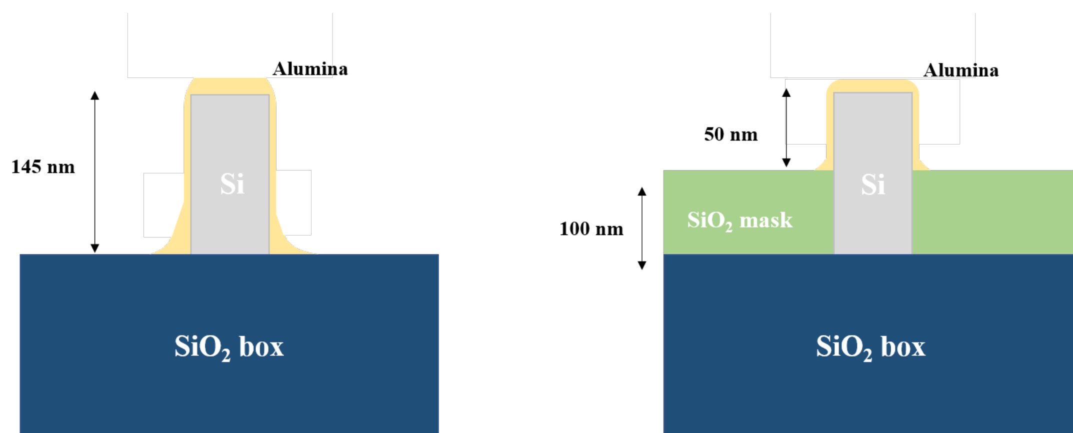

Figure 4.17: On the left: a simple representation of the deposited alumina layer, due to high aspect ratio the lateral walls are very thin and can present some breaks. **On the right**: a representation of the possible solution using a SiO_2 mask of 100 nm in order to have just 50 nm of alumina instead of 150 nm.

Conclusion

This master thesis represents a continuation of the collaboration with the Prof. Jamieson group of Melbourne University, that has the aim to create a nanofet multigate transistor for the realization of an atomic clock based on the presence of bismuth atoms implanted near the Si channel.
The main activity is related to the fabrication process that begins with the creation of the transistor layout. Two facts have to be taken into account, the first one is related on the dimension of the inner channel that has to be nanometric (the width is of 50 nm), in order to have the necessary confinement level to observe single electron transition. The second one is the need of create a multigate system, in this case formed by two gates (the main and the side), in order to control not only the passage of electrons in the channel quantum dot, but also the transition between the dot and the bismuth atom present next to them. This transistor will work as an electrostatic detector able to monitor the charge state of the donor atoms.
For the realization of these devices several fabrication steps have been performed; by starting from the research of the optimal dose and the optimal etching recipe for the inner channel, the process continues with the realization of the precise masks for the implantation of Sb and Bi and it ends with the fabrication of the oxide gate, that it represents another critical passage due to the difficulties related at the alumina deposition with the evaporator, and the final metallization.
Once the device is terminated two kinds of measurement are performed one at room temperature and another one at cryogenic temperature. While the room temperature measurements give just a check about the doping level reached without specific information about the functioning of the device, due to the high leakage currents; the cryogenic ones show that the devices realized have a correct transistor behaviour. Anyway the final aim of our activity is to be able to detect the charge donor state using our device as an electrostatic detector and in order to do that, our transistor has to behave similar to a SET. To perform these kind

of measurements is required a more advanced setup than the cryostat system used in LNESS, because a series of amplifiers and filters are required to achieve very low value of current and voltage. The important thing to understand is that from this type of preliminary analysis we obtained the results expected, that can be considered promising but also surprising as in the case in which seems that has been detected a possible Coulomb Blockade behaviour.
For the realization of a transistor that correctly works at cryogenic temperature, source and drain regions has to be doped over $2 * 10^{19} cm^{-3}$. In parallel with the implantation of Sb performed in Catania, also a cheaper and easy technique of doping it was bringing on in LNESS, the so called spin-on-dopant (SOD). The results about the doping are successful because the level is much above the one required, unfortunately the transistor does not behave correctly and it presents high leakage current also at cryogenic temperature. The reason has to be searched in the difficulties in fabricating a dielectric layer after the SOD removal; in fact the inhomegeneity present on the surface could ruin the alumina layer. That brings to implement other fabrication techniques, for example with the creation of a supplementary SiO_2 mask as a support for the alumina layer or to use other technique for the oxide as the atomic layer deposition(ALD).
Future steps that can bring improvements on the device realization are: one is related to the use of different and more advanced techniques as ALD for all the samples, the other is related to a different design of the layout, in fact a possible solution to reduce the leakage current effect is to eliminate the silicon structure below the main gate, by creating it directly over the channel and over the SiO_2 thermal box. Anyway the most important future step to do it is obviously related to the measurements that will be performed on the future weeks in which we hope to detect the charge state of the donor bismuth atoms.

Appendices

Appendix A

Experimental Setup

A.1 Lithography

Lithography is the process to transfer a pattern to a material [8] and it is the main technique used in microelectronics to fabricate structures. The photolithography is the most widely used technique in the silicon based technology, that uses light on a photoresist layer through an apposite mask. The electron beam lithography appears in the late 60's and consists of a direct writing method, that modifies the resist composition with an electron beam, realizing the patterned structures after the development.

A.2 Electron Beam Lithography

Electron Beam Lithography (EBL) has been considered one of the more versatile technique to produce sub-micronic devices, nanofabrication and masks for other lithographic techniques [8]. It is basically constituted by three main steps that are the exposure of the sensitive material, the development of the resist layer and the pattern transfer. In a direct write EBL system the layout are defined by the electron beam that irradiates and chemically modify the sensitive layer; the final result is obtained after the development. One of the typical machine used for EBL is the Scanning Electron Microscope (SEM), that uses the narrow electron beam of the microscope for design structures on the resist, instead of taking high resolution images. The pattern generator system is completely managed with a computer that allows to control directly the SEM parameters, to create an infinite

number of different layouts and to control totally the lithography execution.
The main problems and difficulties that can be found are related to the optimal condition in which it has to work to obtain high resolution structures, as the high vacuum chamber, the perfect alignment of the electron optics and the correct functionality of the electron gun. Making a comparison with the photolitography, even if it's possible to reach a much higher resolution, due to small electron wavelength λ eq.(A.1), where h is the Planck constant, m is the electron mass and E the kinetic energy of the electron, the production of samples is less reproducible and it's much slower because of the impossibility to have a parallel process.

$$\lambda = \frac{h}{\sqrt{2mE}} \tag{A.1}$$

A.2.1 SEM based system

As mentioned, one of the system configurations for direct writing EBL is based on a SEM and lithographic capabilities attachment. The three main components of the SEM column are the electron source, the objective lenses and the beam deflection unit. Once the beam is formed, the electron optics is responsible of focusing and steering the beam. The process can be redefined as the gaussian circular beam that exposes one unique point at a time [28]. The source electron

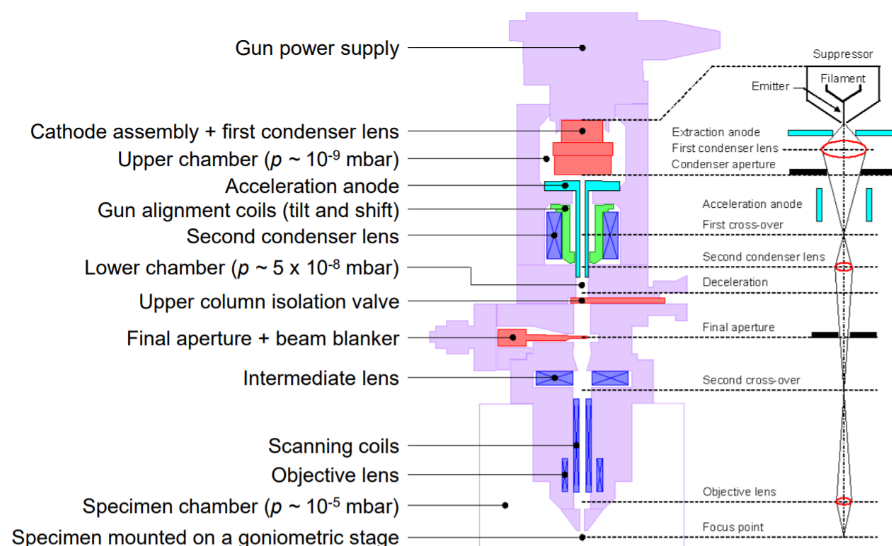

Figure A.1: Detailed scheme of the Philips XL30 SFEG used in LNESS laboratory.

(gun) is usually constituted by a couple of electrodes that extract and accelerate to certain energy the electrons pulled off by the filament, the two types of sources

existing are: the field emission source (FEG) and the thermionic one.
The system used in L-Ness laboratory is a SEM Philips (FEI) XL30 SFEG, the electron source is a field emission source with a tip of tungsten. This is one of the most common system for EBL, that works using the strong electric field produced to pull out electron from the tungsten tip overcoming his low work function. The tungsten is usually coated with a layer of zirconium oxide to reduce the work function barrier. Even if it requires UHV condition, 10^{-9} mbar for the upper chamber and 10^{-6} mbar for the lower one, it is one of the most used system because of the very small size of the source (20-25nm), that allows to reach very high resolution with an high brightness of $\sim 10^8$. (Table A.1)

Source type	Source Size	Vacuum Level	Filament Temp
Thermal Field Emission(W)	$20nm$	10^-8	1800 K

Table A.1: Main SEM parameters

The system of objective lenses has the aim to focus the beam on the specimen; it begins with a Wehnelt cylinder and an opening in the anode at first crossover point followed by two lenses. As reported in figure A.1, the first condenser lens is the one in-charged to reduce significantly the dimension of the beam coming from the tungsten tip, the second one allows to focus the final small beam on the sample surface. The deflection unit is in charge of deviating the beam through the sample surface, within what is called the scan field; ideally are desired the minimum degradation of the beam, i.e. precise deflection, constant beam size and no hysteresis. It is made of a system of coils located along the z-axis, that permits the deflection along x and y. The rest of elements that constitute the column are the apertures, the stigmators and the beam blanker. The apertures are holes of different sizes through which the beam passes, they can interrupt or limit the beam; their function is to determine the amount of beam current, the convergence angle α and so the final resolution. In order to modify the incorrect shape of the beam, that tends to be elliptical due to lens distortion and misalignment; a system of eight poles surrounding the beam is used and it is called stigmator. The SEM microscope in LNESS is equipped with a beam blanker to allow the nanolithography. The beam blanker is a condenser, constituted by a pair of plates with fast response, that avoid unwanted exposition of electron on the sample, through a deflection of the beam.

A.2.2 Exposure Procedure

This technique requires to work in a clean environment, International Standard Organization (ISO) class 5 or better, and to carefully handle the specimen in all the preparation and subsequent phases. Due to the limited depth of focus of the electron beam (few microns), substrates for EBL must have a flat surface, which in turn must be perfectly perpendicular to the incoming beam. The general and basic procedure in the lithography technique, electron or photo one, consists exactly in the same processes that will be described in the following part and schematized in the figure A.2:

- A layer of resist is deposited on the top of the sample in an uniform way with a pipe and then it is spin coated with a velocity of thousands of rpm to reach the correct thickness.
- The beam directly exposes the zone of the resist that have to be modified in order to create the layout.
- The sample is developed in a solution and for the positive resist the zones exposed are removed, while for the negative resist the exposed part is the one which lasts.

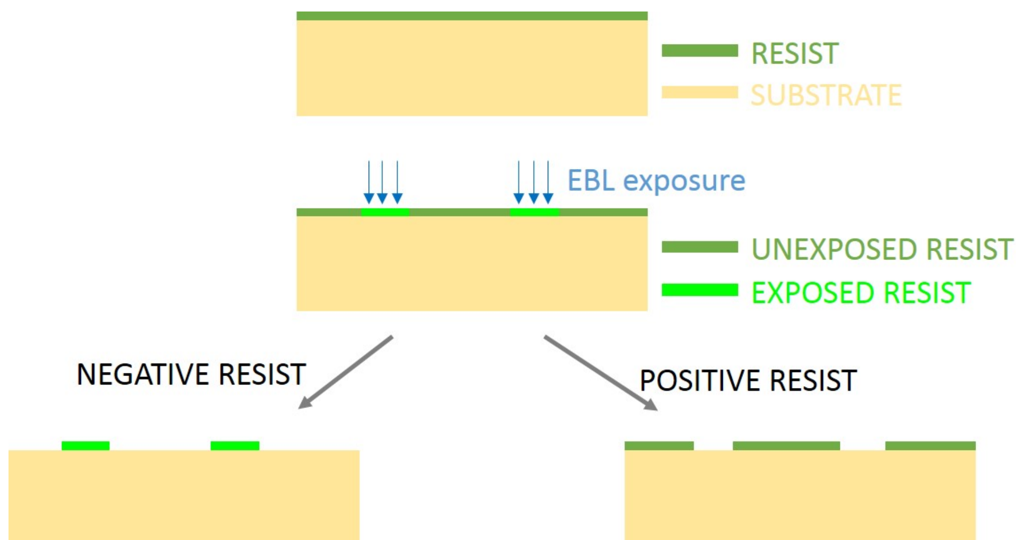

Figure A.2: General EBL process for fabrication

Several parameters has to be determined to obtain a correct exposition.The write field (WF) and the working area (WA) are respectively the zone that the electron

pattern can expose without moving and the real exposed zone, they engrave on the stability and the accuracy of the pattern and so has to be chosen carefully. Another fundamental value to choose is the dose, that is defined as the amount of electronic charge per unit area arriving on the sample surface during the exposure

$$Dose = \frac{Charge(Q)}{(Stepsize)^2} = \frac{It}{s^2} \tag{A.2}$$

Where Q is the charge, s is the step size, I is the beam current and t is the exposure time of the single point, defined as dwell time. Just like the choice of the dose also the resist one is fundamental, the most important properties of a resist are sensitivity and contrast, which are directly linked to the resolution capability of the resist [8]. What is typically done to obtain this parameter is to observe the so called contrast curve shown in figure A.3. The resist sensitivity is define, for the positive resist, as the exposure dose for which the resist layer is fully developed at the bottom, for the negative one is the exposure dose which results in more than half the resist thickness remaining due to cross-linking. For high-resolution e-beam lithography, low-sensitivity resists are preferred [8]. Resist contrast is an inherent property of a resist material, and is defined as the slope of the development curve eq.(A.3), where D_1 is the exposure dose for which the development is finished, while D_0 is the one for which is started.
The interaction of an electron with the atoms of the resist or the substrate, causes inelastic collisions; this brings to the deflection of the primary electron beam, and the generation of secondary electrons responsible for the exposure of the resist. In this thesis work the typical energy used is 30 keV in order to maximize the resolution, in fact the enlargement of the beam decrease with the energy of the electron beam. In the real case, the resolution is limited to approximately 10 nm because of the forward and backward scattering of the electrons in the resist(proximity effect)(Fig.A.4)[20].

$$\gamma = \frac{1}{\log(D_1) - \log(D_0)} \tag{A.3}$$

A.3 Optical Lithography

The optical lithography or photolithography is based on the use of UV light instead of electron. The basic principle is exactly the same of EBL, the light

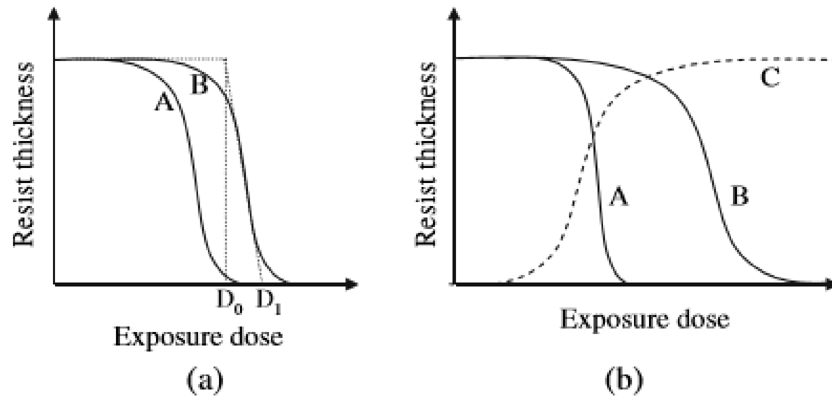

Figure A.3: Resist development curves: (a) resist A is of higher sensitivity than resist B, (b) resist A is of higher contrast than resist B, while resist C is negative

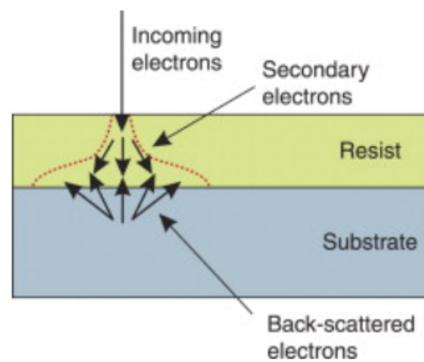

Figure A.4: Influence of the scattered electrons on the illuminated area of the resist. The dashed line indicates the area, affected from the scattered electrons.

beam exposes the photoresist deposited on the sample to modify its chemical composition and to reproduce the desired pattern; but in this case, instead of having a beam blanker that allow the selection of the zone to expose, a mask is placed above the sample. The wavelength of the light source determines the minimum dimension that can be realized due to the diffraction caused by the light passage through the mask and in this case is in the order of $\sim 1\mu m$. The other main disadvantage of the optical lithography is the need for an hard mask, usually made of quartz, with a pattern drawn on it, made for example of chromium, as shown in figure A.5. The photolithography system used in this thesis work is a Karl Suss MA56 mask aligner. The source is a 350 W ultraviolet (UV) mercury lamp, which requires N_2 cooling to avoid overheating. In order to keep the mask and the wafer in the correct position and to facilitate the pneumatic movements, the system is provided also of vacuum and compressed air. There is also an

integrated optical microscope, used for sample positioning and mask alignment; furthermore a system of mirrors and lenses reflects and focuses the generated UV light before the arrival on the specimen. The exposure time can be calculated as:

$$T_{exposure} = \frac{Dose(mJ/cm^2)}{LightIntensity(mW/cm^2)} \tag{A.4}$$

Where the dose in this case, it's the minimum quantity of light absorbed to change the resist solubility, while the light intensity corresponds to the power of the UV source.

Figure A.5: Image of a typical quartz photo-mask used in our clean room.

A.4 Reactive Ion Etching

The best way to transfer the pattern from the resist to the substrate is using a dry reactive ion etching technique (RIE) [31], which involves the use of reactive plasma. The basic functionality of this technique is based on the fact that the resist is used as a sort of mask during which the plasma etch the sample surface, transferring the pattern. The RIE systems is composed by a cylindrical chamber with an holder on the bottom. The chamber is usually grounded and the electrode cathode is continually cooled down with a water refrigeration system at 16°C. The three gases available in the RIE machine located in our laboratory are

(SF_6, CF_4, O_2), while a mass flow-meter controls the amount of them in the chamber; a main rough pump is then used to removed them. By using an oscillating electric field created by a radio frequency(RF) generator, the plasma is generated: the typical power used are between 50-100 W with a standard frequency of 13.56 MHz. The oscillating free electron motion induced by the oscillating electric field, bring to the collision with the atoms of the gas, that become ionized inducing a plasma state. The electrons in the chamber are vertically accelerated and they can be absorbed by the grounded chamber wall, or by the sample, creating an electrostatic potential that will attract the heavier ions. The collisions of the ions with the atoms of the sample are responsible for the removal of the material in the areas not protected by the resist, as shown in figure A.6. The parameters that can be modified are the gas flow, the power of the radiofrequency generator, the gas pressure in the chamber and the process time. To find the correct etching rate, so the nanometer of substrate removes per second, it has to be found the correct balance between the flux of ions and the RF power. An higher RF power increases the electron power and so the probability of ionization, but it has to be compensated with an high gas flow rate in order to not reduce the number of ions. The last parameter to take into account is the pressure in the chamber, that has to reach level of $10^{-1} tor$ in order to have an higher mean free path for electron increasing the ionization rate.

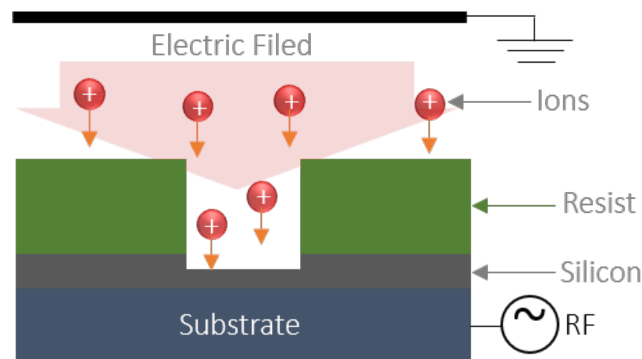

Figure A.6: Basic scheme of a reactive ion etcher. The presence of the electric field moves the ions downward where they react with the substrate atoms

A.5 Electron Beam Evaporation

A fundamental part of the nanofabrication technique is the metalizzation, so the creation of metallic contacts that allow the electrical characterization of the specimens. E-beam (electron beam) evaporation is a thermal evaporation process, and is one of the two most common types of physical vapor deposition (PVD). E-beam evaporation provides for the direct transfer of a larger amount of energy into the source material, enabling the evaporation of metal and dielectric materials with very high melting temperatures, such as gold and silicon dioxide. An highly energized electron beam is generated in a resistive filament accelerated and focused on the crucible, where the material is heated and melted. The evaporated particles of the material start to diffuse inside the chamber going on the sample surface, situated on a circular holder on the top of the crucible. The requisites of pressure are very strict in order to obtain an high quality layer; thanks to three different pump (rotative, turbomolecular and cryo) a pressure of $10^{-6} mbar$ is reached. The current of the electron beam can be set, and depends on the material to evaporate and on the desired deposition rate. Usually the deposition is done at a rate of 0,1 nm/s which is slow enough to obtain a good quality film. The e-beam is also provided of a cooling water system that allows to not overheating the crucible during the evaporation; and also an heating water one is present in order to avoid the condensation in the chamber during the ventilation.

A.6 Rapid Thermal Annealing

Rapid thermal annealing (RTA) is a common process in semiconductor fabrication, based on the fast heating of a sample to very high temperatures. In order to achieve very quick heating, uniformity and temperature precision are penalized [22]. In this thesis activity, RTA was used to activate the dopant atoms present in the SOD layer that covers the surface of the silicon. The RTA used for this work is an AllWin 21 Corp. AccuThermo AW 410, which uses a lamp to heat samples. The structure of the system is very simple, the specimen are inserted in a quartz chamber over a silicon holder, placed above the lamp. The cooling system used to decrease the temperature inside the chamber after the treatment, is based on nitrogen. The parameters which can be set are: the type of gas in the chamber

during the process, the duration of the ramps up and down, the temperature to reach, the duration of the steady state at high temperature and the quantity of gases during the different phases of the process. A mass flow controller is used to bring the gases inside the chamber. The temperature control was based on a pyrometer, that is typically used for the highest temperature and in our case a temperature of 880° is achieved. The pyrometer is a remote-sensing thermometer, which can measure from distance the temperature of a surface, from the spectrum of the thermal radiation emitted. A chiller set at 20°C is used as a temperature reference for the pyrometer. Water cooling to avoid overheating is also provided.

A.7 Electrical characterization

A.7.1 Probe Station

A probe station is a mechanical facility often used in academic research to physically acquire electric signals. The main components are: a metallic plate connected to ground, on which the samples are placed; an optical microscope to ease the correct positioning of the probes; a variable number of probes, typically two or four, connected to micromanipulators, used to precisely position the tip of the probes on the desired points of the specimen, and also to an amperometer and a voltmeter. The probes used for this thesis work are passive probes consisting in thin tungsten needles, that are manually moved but simultaneously observed on the computer display through a connection with the optical microscope. This is very relevant to observe because the presence of the microscope allows to be very precise even if the pads dimension are on the order of μm. Two-probes or four-probes characterization can be done. Two-probes characterization consists in placing the tips of two probes in contact with two different points of the sample and acquire through an apposite Labview software, the voltage difference observed applying a current from the two tips. Four-point-probe-based instrumentation uses separated pairs of current-carrying and voltage-sensing electrodes to make more accurate measurements and to measure the average resistance of a thin layer or sheet by passing current through the outside two points of the probe and measuring the voltage across the inside two points.

A.7.2 Cryostat

In order to characterize the electrical behaviour of the samples at low temperature, Hall measurements and I-V measurement inside a closed-cycle liquid-He cryostat have been performed. Basically the cooling system of the cryostat is composed by two internal circuits. The first one is a compressor that cools down the solenoid, the internal parts and the helium port at a temperature below 4,7 K; also the inlet trap, which is the begin of the circuit, goes below 40 K. In the second part of the system there is the He that has a pressure smaller than the atmospheric one, it comes in contact with the inlet trap, this passage is fundamental to condense all the impurities present in it. In the sample area liquid He is forced to evaporate at a pressure smaller than atmospheric pressure,in this way is possible to reach lower temperature than in the atmospheric condition. After evaporation, helium is pumped away, re-condensed and re-inserted in the external closed circuit. Between the tube and the sample space, there's a needle valve which can be externally modified and it has a key role. If the valve is too close, not enough helium can pass, so the sample is not cooled down and also the temperature of the tube rises. If, on the other side, it is too open, the helium flowing in the sample cannot condensate, loosing its function of cooling down the system. So an equilibrium is necessary to guarantee the correct functioning. The magnetic field is generated by a superconductive solenoid kept below the critical temperature, it's maximum value is around 7.5 T, for which 100A are required. Another particularity of this system is that the samples must be insert in a specific chip carrier which has the dimension of $4mm$ x $4mm$, on which the sample is stitched with an silver glue. The metallic pads on the sample must be bonded to the contacts on sample holder, before the holder is slowly inserted inside the cryostat itself. Slowness is necessary to allow a progressive cooling of the sample and to avoid the heating of the sample area. The temperature of the sample is controlled by a sensor placed nearby, in the sensor area. The minimum temperature which can theoretically be reached is 1,6 K but the measurements for this thesis work have been performed around 4 K.

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