POLITECNICO DI MILANO
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Design of a two-stage Low Noise Microwave Amplifier using AWR Microwave Office

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Ai miei affetti
più cari

Abstract

Low-noise amplifiers (LNAs) are critically important in microwave receiver systems. In this project, a microwave two-stage Low Noise Amplifier (LNA) has been developed.

Our design goal is to design an LNA whose transducer gain is between 18-20 dB, noise figure is less than 1.2 dB, and return loss is greater than 15 dB across 3.8-4.2 GHz frequency band.

In this project, a transistor, with code ATF-21186 at the operating point (Vds= 2 V, Id= 20 mA), is selected as an active device for the key amplification device. A bias circuit is designed and added to the transistor. With the help of Smith Chart, the ideal output matching network, input matching network, and the inter-stage network are developed based on the S parameters of the transistor together with the bias circuit at the central frequency of 4GHz. Then the ideal two-stage LNA is implemented by synthesizing them together. Based on the ideal design, the practical two-stage LNA is developed in 3.8-4.2 GHz. The details of the dimensions for components, as micro-strip lines, are presented. The overall circuit layout for fabrication is also shown and the final results of the response and yield are discussed. Our entire design is analyzed, developed and optimized in the environment of AWR Microwave Office.

Sommario

Gli amplificatori a basso rumore (LNA) sono di fondamentale importanza nei sistemi di ricezione a microonde. In questo progetto è stato sviluppato un amplificatore a basso rumore (LNA) a microonde con due stadi.

Il nostro obiettivo di progettazione è progettare un LNA il cui guadagno del trasduttore è compreso tra 18-20 dB, la cifra di rumore è inferiore a 1,2 dB e la perdita di ritorno è maggiore di 15 dB nella banda di frequenza 3,8-4,2 GHz.

In questo progetto, un transistor, con codice ATF-21186 nel punto operativo (Vds = 2 V, Id = 20 mA), viene selezionato come dispositivo attivo per il dispositivo di amplificazione chiave. Un circuito di polarizzazione è progettato e aggiunto al transistor. Con l'aiuto della Carta di Smith, la rete di adattamento dell'uscita ideale, la rete di adattamento dell'ingresso e la rete inter-stadio sono sviluppate in base ai parametri S del transistor, insieme al circuito di polarizzazione con frequenza centrale di 4 GHz. Quindi, l'LNA a due stadi ideale viene implementato sintetizzandoli insieme. Basato sul design ideale, il pratico LNA a due stadi è sviluppato a 3,8-4,2 GHz. Vengono presentati i dettagli delle dimensioni dei componenti, come linee di micro-strisce. Viene anche mostrato il layout generale del circuito per la fabbricazione e sono discussi i risultati finali della risposta e della resa. Il nostro intero design è analizzato, sviluppato e ottimizzato nell'ambiente di AWR Microwave Office.

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Introduction

This Thesis is structured in the following way:

- Chapter 1 introduces LNAs and the theory necessary to design an LNA.
- Chapter 2 describes the amplifier's design goal and general methodology.
- Chapter 3 provides the selection of the active device and substrate used in LNA.
- Chapter 4 explains the physical implementation of the LNA design.
- Chapter 5 presents the layout of the overall layout of LNA.
- Chapter 6 is about the yield analysis and the final conclusion.

Chapter 1

Introduction and Amplifier Theory

In this chapter, we firstly introduce the importance and role of LNA, in other words, where and why the LNA is used. Secondly, we describe the concepts of the key parameters for design LNA, like Gain, Noise Figure, Stability, Central Frequency and Bandwidth, which are important in theory for design.

1.1 The role of LNA

Low-noise amplifiers (LNAs) are critically important in microwave receiver systems.

In microwave receiver systems, the sensitivity of the receiver varies greatly by the amount of noise generated. In a receiver system, the signals received from the antennas are usually too weak for subsequent operations, such as demodulation. So, amplifiers to amplify these signals are required. However, if during the amplification, the amplifier itself produces noise on the same scale of or even greater than the amplified signals level, it will cause great difficulty in distinguishing the signal from the noise. So, amplifiers that have low noise, that is the so-called low-noise amplifiers (LNAs), are necessary to be put here.

The LNAs are almost located in the first position of a microwave receiver systems. By using LNAs to amplify the expected signal, the difference between the signal and the noise will be quite large compared with using normal amplifiers. As the amplified signal passing through the following components after LNA in the receiver system, like mixers, even additional noise may be

introduced and attached in the following receiver system, the signal will not easily be affected by the noise.[1]

Low-noise microwave amplifiers have been widely used in microwave communication fields. The applications of LNA are in GPS receivers, Cellular phones, Wireless LANs, Satellite communication, etc...[2]

1.2 LNA parameters

A basic LNA topology consists of blocks as an amplifier device (transistor), biased device, input matching network, output matching network as in Figure 1.1:

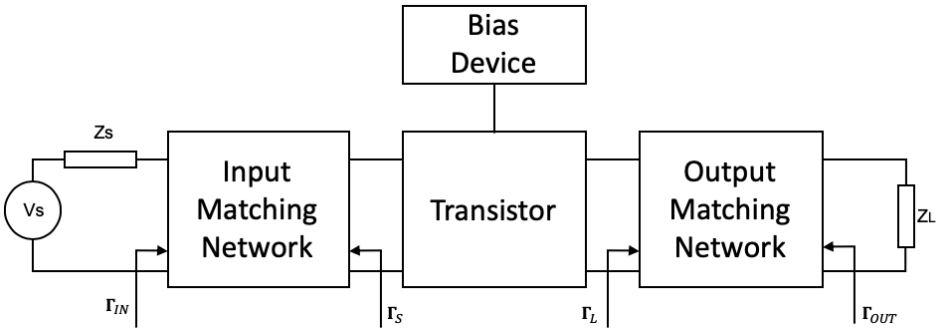


Figure 1.1: LNA System Topology

1.2.1 Transducer Gain

Transducer Gain is an index to quantitatively describe the amplification level of one LNA. Transducer Gain (G_T) is defined as the ratio between the power delivered to the load by the amplifier (P_L) and the power available from the source (P_A):

$$G_T = \frac{P_L}{P_A} \tag{1.1}$$

For a practical LNA, the gain is measured with the source and load impedance both of 50 Ohm as customary. Considering an amplifier as a two-port network as in Figure 1.2, the expression for the G_T can be derived as [3]:

$$G_T = |S_{21}|^2 \frac{(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|(1-\Gamma_S S_{11})(1-\Gamma_L S_{22}) - \Gamma_S \Gamma_L S_{12} S_{21}|^2} \tag{1.2}$$

Also, the reflection coefficients at input and output can be evaluated:

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad \Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{1.3}$$

where:

– S_{11},S_{12},S_{21},S_{22} are the device S-parameters;
– Γ_S and Γ_L are the reflection coefficients at source and load respectively.

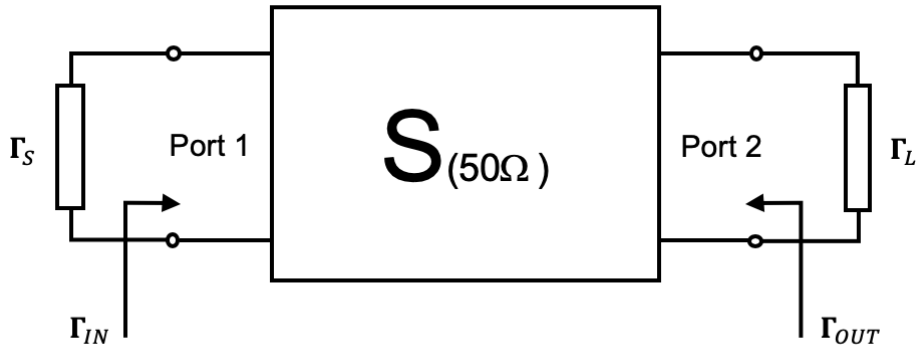


Figure 1.2: Amplifier as Two-Port Network

1.2.2 Noise Figure

Thermal noise, shot noise, and flicker noise are the main sources of Electronic Noise.

Thermal noise is always associated with dissipation phenomena produced by currents and voltages. It is represented by a voltage or current source randomly variable in time. Shot noise arises typically in PN junctions forwardly biased; it is due to the discrete nature of current through the junction, which results randomly variant around the imposed bias value. Flicker noise arises in semiconductor devices, due to impurities and defects in the crystal structure.

In microwave devices, the noise is characterized as Noise Figure (NF). The expression of noise in a two-port network as Figure 1.3, the Noise Figure is defined as the ratio between P_{Nout} and $G_a\ P_{Nin}$ [4], namely

$$NF = \frac{P_{Nout}}{G_a \cdot P_{Nin}} \tag{1.4}$$

where:

– P_{Nout} is the actual noise power at the output;
– G_a is the available power;
– $G_a P_{Nin}$ is the noise power at output if the 2-port would not add noise power.

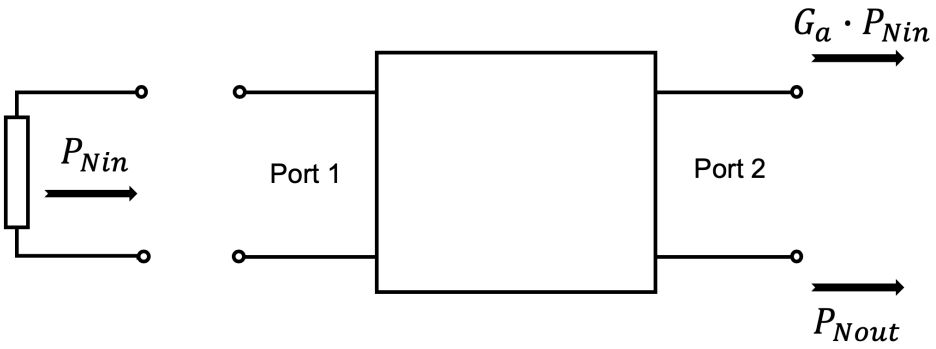


Figure 1.3: Noise Power in a Two-Port Network

In practice, NF is a function of frequency, so the above powers must be assumed per unit band, such as the power densities. Moreover, NF also depends on the source impedance.

More often, the noise figure is expressed in decibels(in dB) NF_{db} as,

$$NF_{db} = 10logNF \tag{1.5}$$

We can get the noise figure as the expression of Γ_S, reflection coefficient of the source, given by

$$NF = (NF)_{min} + 4r_n \frac{|\Gamma_S - \Gamma_{min}|^2}{|1 + \Gamma_{min}|^2 \cdot (1 + |\Gamma_S|^2)} \tag{1.6}$$

where:

– $(NF)_{min}$ is the minimum value of NF;
– Γ_{min} is the value of Γ_S which determines $NF = NF_{min}$;
– r_n is the normalized noise resistance.

All these parameters are frequency-dependent. Typically, they are made directly into *.s2p* data files. The data files are provided available as references for commercial devices by manufacturers or devices vendors.

If we plot the equation expressing NF as a function of Γ_S on the Smith Chart, an NF circle with a certain center and radius will be obtained. Together with the circle of the gain, the proper value of Γ_S can be selected within the common area of two circles.

For cascade stages as in Figure 1.4, the overall noise figure of the cascade stages network is expressed as

$$(NF)_{TOT} = NF_1 + \frac{NF_2 - 1}{G_{a1}} + \frac{NF_3 - 1}{G_{a1}G_{a2}} + ... \tag{1.7}$$

where:

- G_{an} is the available power in the n stage, for n=1,2,3...n;
- NF_n is the noise figure in the n stages, for n=1,2,3...n.

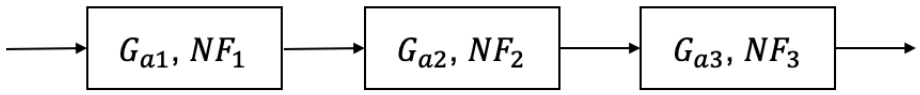


Figure 1.4: Two-Port network with Cascade Stages

It is important to point out that the noise figure is mainly determined by the first stage. So, for designing multiple-stage LNA, setting the LNA in the first stage with the lowest NF is a wise design decision.

The noise figure NF can be represented on the Γ_S complex plane. The noise points with the same value, which is NF= constant, are on the same circle called the equal noise figure circle.

An example is shown in Figure 1.5, where we have 4 circles, which are p1, p2, and p3 from inside to the outside, with corresponding NF1 < NF2 < NF3<NF4. The centers of all equal noise figure circles fall on the line which connects the origin of the Smith chart and Γ_{opt}. The larger the noise figure is, and the larger the radius of the circle is. When Γ_S=Γ_{opt}, F=F_{min}, the noise figure is reduced to a point as the point p1 on the Smith Chart.

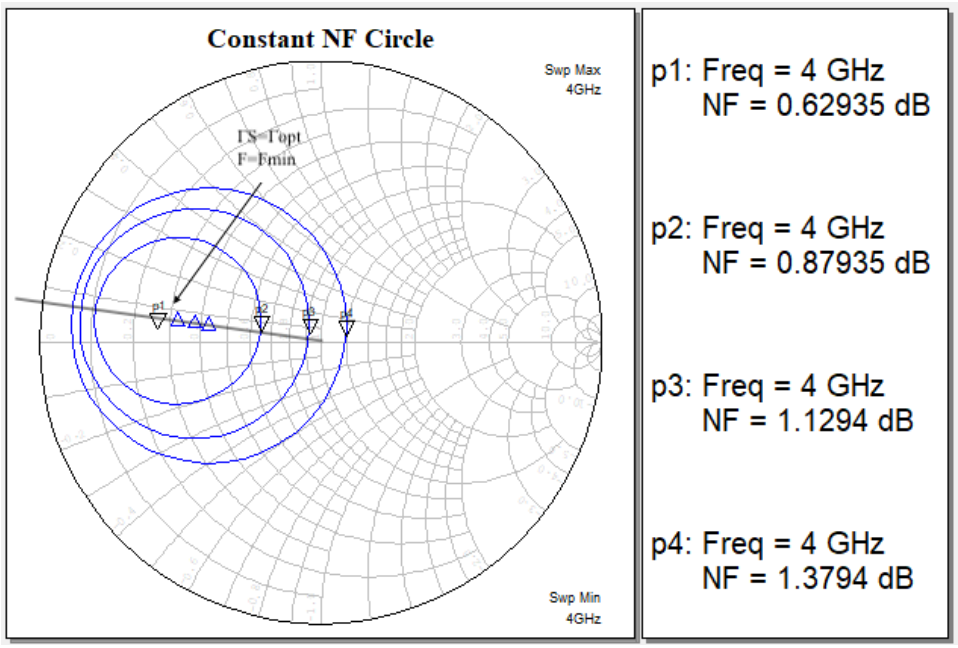


Figure 1.5: Constant NF Circles on Smith Chart

1.2.3 Stability

In certain radio frequency bands and certain impedance environments, amplifier is intending to oscillate. Stability shows how much is this tendency. For example, if we say an LNA is stable, it means the output signal remains a finite amplitude for an input exciting signal with finite amplitude [5].

There are generally three types of stability, as unstable, potentially unstable and unconditionally stable. The oscillators make use of the property of being unstable. For amplifiers, they always work under the other two types of stability, potentially unstable and unconditionally stable. Unconditionally stable means that the amplifier is stable in whatever impedance environment. Potentially unstable means that the amplifier is stable only in certain impedance environments.

It is important that LNA maintains stable in required bandwidth with impedance through our design, which means the designed LNA will not behave like an oscillator. This can be achieved if we use stable techniques to impose the LNA to be unconditionally stable. Or even the LNA is potentially unstable, the input and output reflection coefficients fall in their stable admission regions respectively.

To determine the stability of our amplifier, here we can use the stability factor K. Given the S parameters, the conditions $\Gamma_{in} < 1$, $\Gamma_{out} < 1$ whatever

value of Γ_S, Γ_L if:

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |s_{11} \cdot s_{22} - s_{12} \cdot s_{21}|^2}{2|s_{12} \cdot s_{21}|^2} > 1, \det S < 1 \qquad (1.8)$$

If these equations are verified, the two-port is unconditionally stable. When $k < 1$, the admissible values of Γ_S, Γ_L must, however, satisfy the conditions

$$|\Gamma_{in}| = |s_{11} + \frac{s_{21}s_{12}\Gamma_L}{1 - s_{22}\Gamma_L}| < 1 \quad |\Gamma_{out}| = |s_{22} + \frac{s_{21}s_{12}\Gamma_S}{1 - s_{11}\Gamma_S}| < 1 \qquad (1.9)$$

These constraints, which can be represented graphically on the Smith Chart, allow to identify the admissible values of Γ_S, Γ_L.

By setting the 'less than' symbol to 'equal' symbol in Equation 1.12, we can obtain the circles which define the boundary between the admissible and not admissible regions. An example of the curves is shown in Figure 1.6.

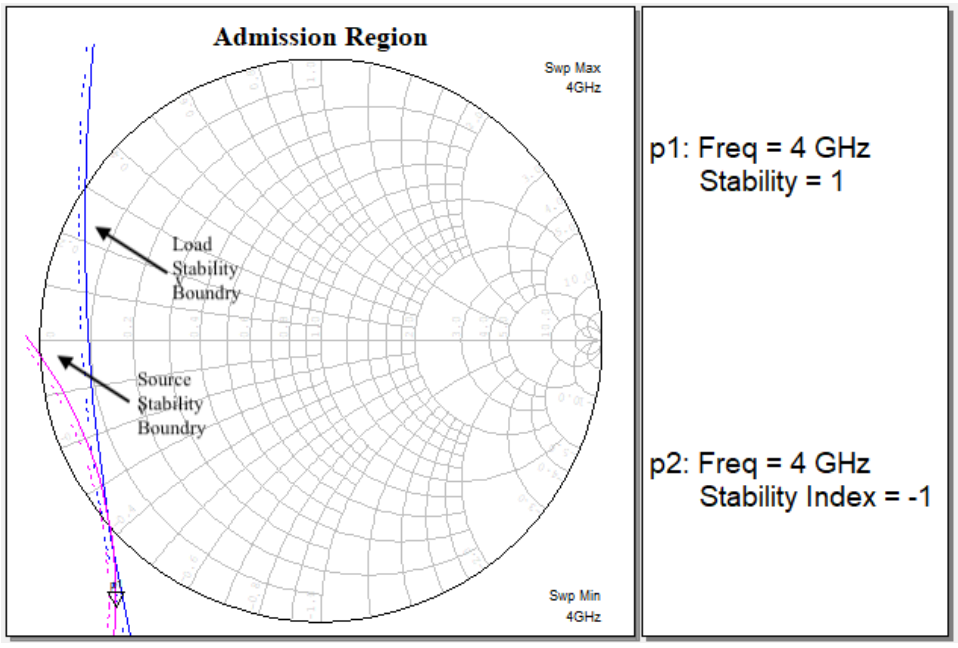


Figure 1.6: Boundary between the Admissible and not Admissible Regions on smith chart

To identify which of the two is the stabile region the values Γ_{in} (Γ_{out}) for ($\Gamma_L(\Gamma_S) = 0$ must be observed. Taking into account that $\Gamma_{in}(\Gamma_{out})$ coincides in this case with $s_{11}(s_{22})$, it has:

The stable region for $\Gamma_L(\Gamma_S)$ is **outside** the instability circle if:

– $||s_{11}|(|s_{22}|)< 1$ and the circle does not enclose the centre of the chart
– $|s_{11}|(|s_{22}|)> 1$ and the circle encloses the centre of the chart

The stable region for $\Gamma_L(\Gamma_S)$ is **inside** the instability circle if:

– $||s_{11}|(|s_{22}|)> 1$ and the circle does not enclose the centre of the chart
– $|s_{11}|(|s_{22}|)< 1$ and the circle encloses the centre of the chart

1.2.4 Central Frequency and passband

The central frequency is the frequency in which the LNA works. With different devices and for different purposes, it can be set to hundreds of 10^6 Hz, or even higher in the microwave band. Central frequency is one of the main indicators of the low-noise amplifier. It is one of the basic references for selecting the proper active device and is on x-axis for displaying graphically some specifications of the circuit components during the design process.

For the passband, to ensure that the signal passes through the amplifying circuit without distortion, the value of the gain must be limited in a range around the central frequency. The passband is the bandwidth of this range.

Chapter 2

Design Goals and Methodology

In this chapter, the design goal for LNA is represented and discussed. Then, the general methodology to design LNA is described. At last, the AWR design environment is briefly introduced.

2.1 LNA Design Goals

In Table 2.1, specifications for LNA are clearly represented. As we can see, the required operation band for the LNA is not in a wide bandwidth range. And the central frequency is at 4 GHz, which lies in the so-called S-band or C-band according to the classification of the radio frequency range.

Table 2.1: LNA Design Goals

Parameter	**Value**
Amplifier band	3.8 - 4.2 GHz
Transducer gain	18 «20
Noise Figure	<1.2 dB
Matching at output (Return Loss)	>15 dB
P1dB	>10 dBm

In the frequency between 3.8 to 4.2 GHz, the transducer gain should be limited in the range between 18 dB to 20 dB. This level of the gain is in state of the art with the development of transistors and amplifiers.

For the noise figure, the largest acceptable value is 1.2 dB. To obtain the noise figure of an amplifier is the primary target, and we should always pay attention to the value of NF after adding new components during our design process.

Also, we need to verify if the return loss is above 15 dB to make sure our amplifier has a good characteristic of power efficiency. This can be done by measuring the S_{22} of the final LNA.

At last, P1dB should be larger than 10 dBm. The P1dB can be used as criteria to select a suitable active device. When we read the datasheet of the transistor, we need also to pay attention to the written value of P1dB around 4 GHz.

Additionally, besides the specifications have discussed above, we should also consider one practical parameter, which is the cost. We hope the budget of the LNA can be as low as possible. So when selecting each component, under the same behavior condition, those with lower costs will be considered primarily.

What's more, because we use AWR Microwave Office for design, components which are collected in its library will be taken firstly in the convenience of continuity under the same design environment. AWR Microwave Office libraries, containing the most popular vendor parts, are directly embedded inside. They are very powerful and easy to use.

2.2 Design Methodology

We design LNA using the S parameters, which is widely used to characterize the two-port network.

S-parameters help in the calculation of maximum available gain, potential instabilities, input and output impedances, and transducer gain. S-parameters also allow the calculation of optimum source and load impedances, to choose the source and load impedances for a specified transducer gain.

With different methods and in different sequences, it is not unique for designing a microwave low noise amplifier. Here our design is composed of steps as follows:

– Firstly, an appropriate choice of active device is of great importance towards a successful design.

  A transistor should be consistent with our specification's goals in Table 2.1, as noise, gain, working frequency. The value of P1dB should be considered simultaneously. We need to point out that because we use the S parameters, the P1dB cannot be measured directly from the final LNA we designed. So, we verify it first when selecting the transistor. In other words, we need to check P1dB in the datasheet specifically

to make sure the right choice of the transistor. Also, the substrate characteristic should be determined. And we synchronize the datafile of transistor and subtract in AWR Microwave Office.

– Secondly, after the transistor has been selected, a biased device in AWR Microwave Office is designed to provide the proper bias.

  A bias device should behave like an open circuit when added to the transistor. A bias device should in some ways helps in maintaining stability and satisfies the noise and gain specifications with the transistor.

– Thirdly, we obtain the ideal design with the help of the Smith Chart.

  Optimum loads Γ_S, Γ_L, which are supposed to fall in the stability admission region on the Smith Chart, are evaluated for the device in the central frequency 4 GHz. And we use the ideal, lossless transmission line to design the input and output matching network in the AWR Microwave Office. The transmission line can produce the impedance effect as the same as that produced by the reactive elements. For multiple-stage LNA, the inter-stage network to connect the transistors also needs to be designed.

– Fourthly, we transform the ideal design to the practical design.

  We replace all the ideal transmission lines to the real microstrip lines and tune the parameters of them so that the LNA can obey all the design specifications in the overall bandwidth of 3.8-4.2 GHz. Thanks to the convenience of AWR Environment, this can be done by the 'tuner' tool.

– Fifthly, we consider the footprint of the active device and lumped elements, for example, the transistor and the DC blocking capacitors. The practical amplifier layout is determined in AWR Microwave Office.

– In the end, with the help of the 'optimizer' tool in AWR Microwave Office, the final amplifier which satisfies the specifications of gain, noise figure and return loss can be determined.

2.3 AWR Microwave Office

The NI AWR Design Environment is a powerful software for engineers to design and analyze the circuits and systems which are used in wireless high-speed wired, broadband, aerospace and defense, and electro-optical applications. Its interface is user-friendly, and the workflow is well- designed.

The main interface is shown as follows [6].

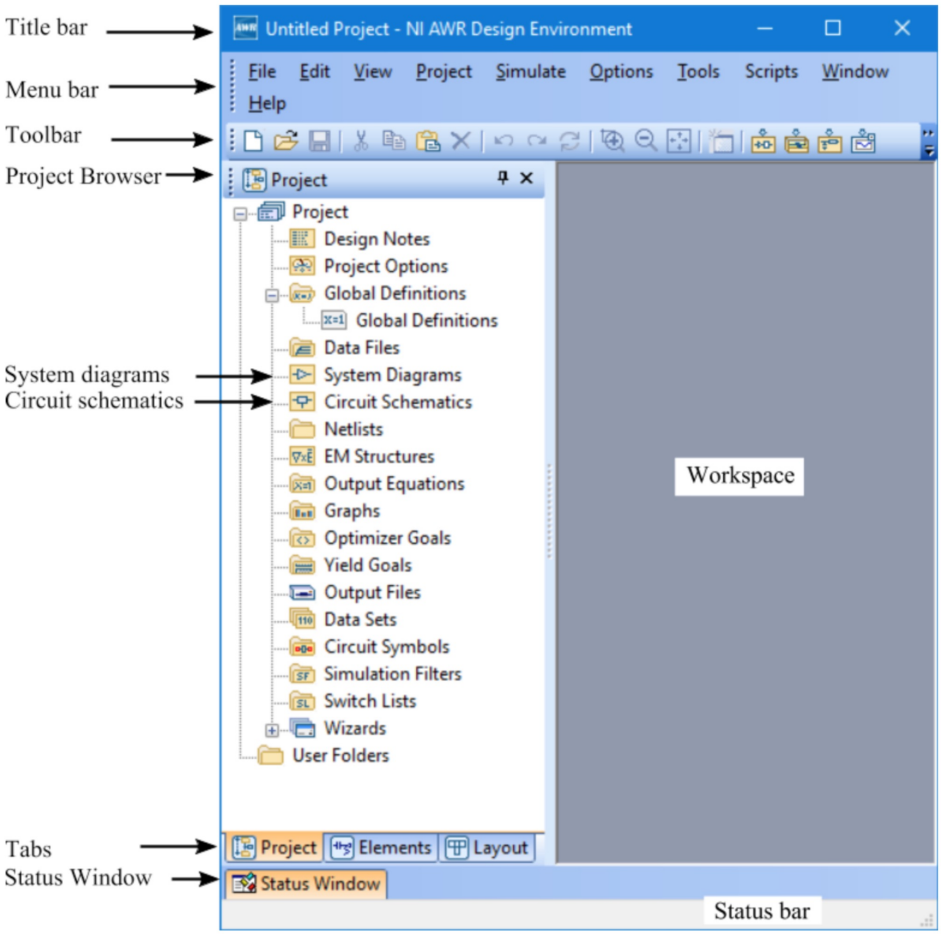


Figure 2.1: NI AWR Design Environment Main Interface

As shown in Figure 2.1, the title bar, menu bar, and toolbar are on the top of the interface. On the right side, it shows the project browser that contains the data file, system diagram, circuit schematics, graph and for optimizer goals, etc... At the bottom of the project browser, three tabs as *Project*, *Element*, and *Layout*, can be switched among themselves during designing. In NI AWR Design Environment, we can create schematics, generate circuit layouts, create system diagrams, perform simulations, display graphs and set optimizer goals.

The basic design flow displays in Figure 2.2. Following this workflow, we can design the wanted LNA logically and efficiently.

Besides, the libraries of AWR Microwave Office are very powerful containing the most popular vendor parts. Once we find the needed parts in the

library, we can directly drag them from the *'Elements'* tab to the schematics diagram.

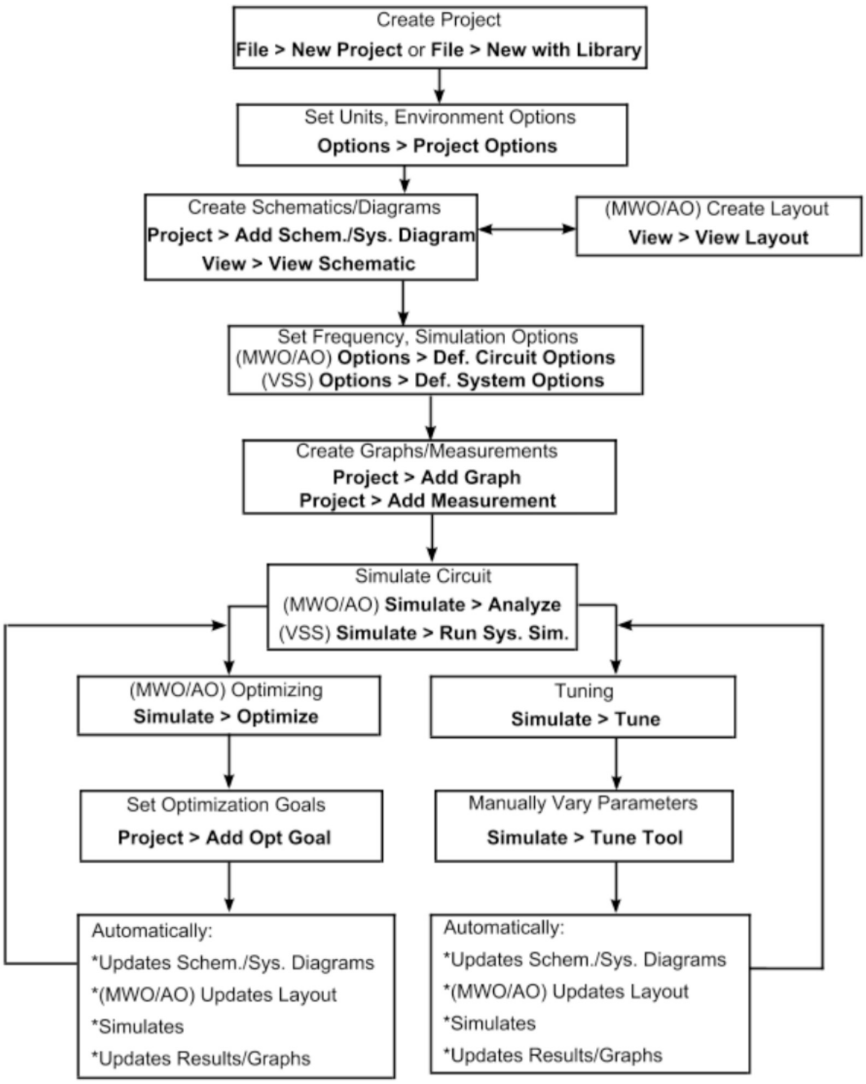


Figure 2.2: NI AWR Design Environment Basic Design Flow

Chapter 3

Component selection

The components selection is of great importance for a successful design. In our project, we need to choose the proper components of active device, substrate characteristic and DC blocking capacitors. In this chapter, we discuss the choice of them.

3.1 Transistor Selection

Many manufacturers produce transistors. These famous manufacturers are, for example, Broadcom, Cree, Freescale, Fujitsu, Hewlett–Packard, MACON, Mimix, Mitsubishi, MwT, Philips, Polyfet, Rohm, SEDI, Semicoa, Raytheon, RFMD, Sirenza, Sony, Toshiba, Transcom, etc... We look through their product lists and datasheets to check the suitable active device, which is supposed to be a silicon transistor in types of BJT, FET or HEMT.

To select the active device, we need to consider transistors' specifications in the global perspective. Some transistors' optimum working frequency is below L-band. For example, some transistors produced by Freescale and Polyfet work below 2GHz. Also, some transistors are not suitable because of their NF. For example, these transistors produced by Cree, Fujitsu, Raytheon, RFMD, Philips, Mitsubishi, Sirenza, Sony, Toshiba, Transcom, etc... whose NF is too high or in lack in the s parameter file. What's more, some transistors as MwT-LN180 by MwT and some serials by MACON, have excellent performance, but the price of them are comparably higher making it unpractical to use in our design.

Among them, the potential active devices for designing our LNA are ATF-54143 by Broadcom, FHC40LG by SEDI, ATF-21186 by Hewlett–Packard. Taking into an integrated consideration, ATF-21186 is

selected for its suitable operating bandwidth (0.5-6GHz), lowest NF (0.59 dB), relatively cheapest price, highest stability K (0.85) at the bias condition of V_{DS}= 2V, I_{DS}= 20 mA. What's more, its P1dB(18.0 dBm) has highest value.

Hewlett–Packard's ATF-21186 is a low cost Gallium Arsenide Schottky barrier-gate field effect transistor housed in a surface mount plastic package. The datasheet(see Appendix A) shows that the maximal gain G_{max} is 11.1 dB at 4GHz. So, in order to reach the design goal of the transducer gain range 18<GT<20 dB, a two-stage LNA is necessary. And the basic building blocks of the two-stage will be shown in Chapter 4.

We can import the data file of ATF-21186 (see Appendix B) in AWR Microwave Office, which is a touchtone file with extension as *'.s2p.'*

We build the schematics of the transistor according to the file above. The maximum gain (Figure 3.1), the minimal NF (Figure 3.2) and stability factor K and Auxiliary Stability Factor B1 (Figure 3.3) of the transistor can be simulated continuously in AWR Microwave Office in band 3.8-4.2GHz in graphs by clicking 'analyze' bottom.

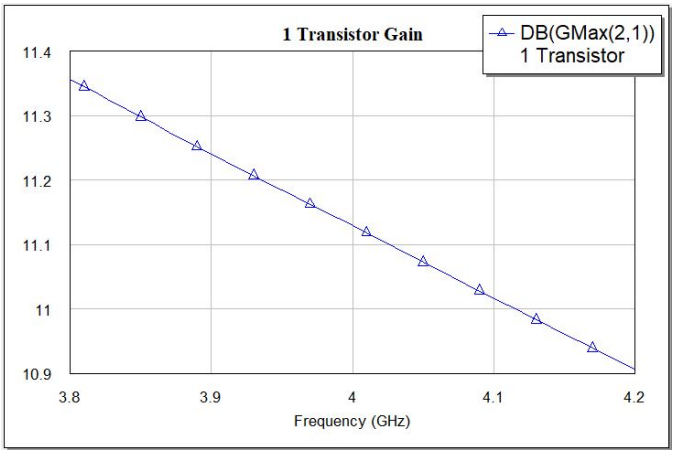


Figure 3.1: Maximum Gain for Transistor

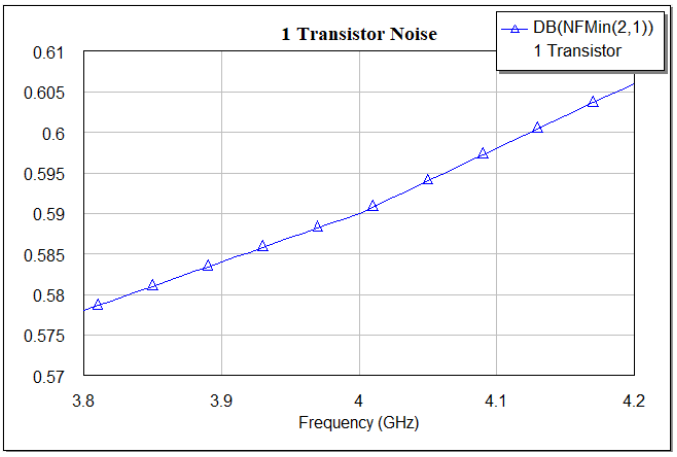


Figure 3.2: Minimal Noise for Transistor

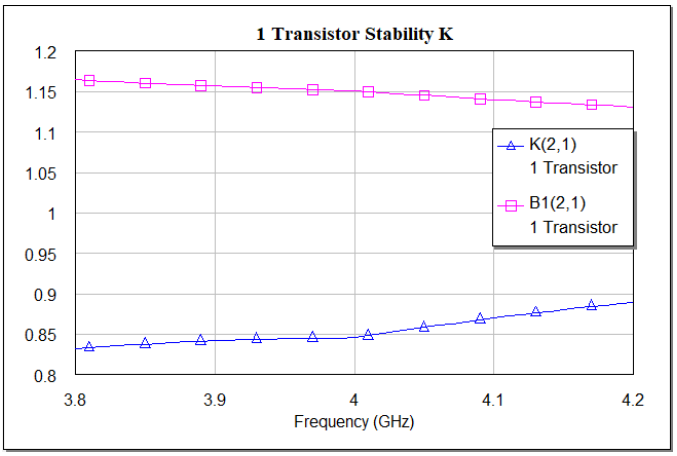


Figure 3.3: Stability Factors for Transistor

3.2 Substrate Selection

Here, we use the standard FR-4 in 21 mils as a substrate. The parameters of the FR-4 is taken from the microstrip substrate library of Modelithics. (see Appendix C)

We have two ways to conclude this substrate in our project. The first one is to load the library of Modelithisc and directly drag it from the library to the schematics diagram, as shown in Figure 3.4. (Following the tabs of Elements, expand *Libraries-> *Modelithics Library->Parts By Type->Substrate-> RF-4*, and in the expanding window below we can select the *RF-4* in 21 mils which is the substrate we need.).

Or we can directly modify parameters of an MSUB component from the

default library.

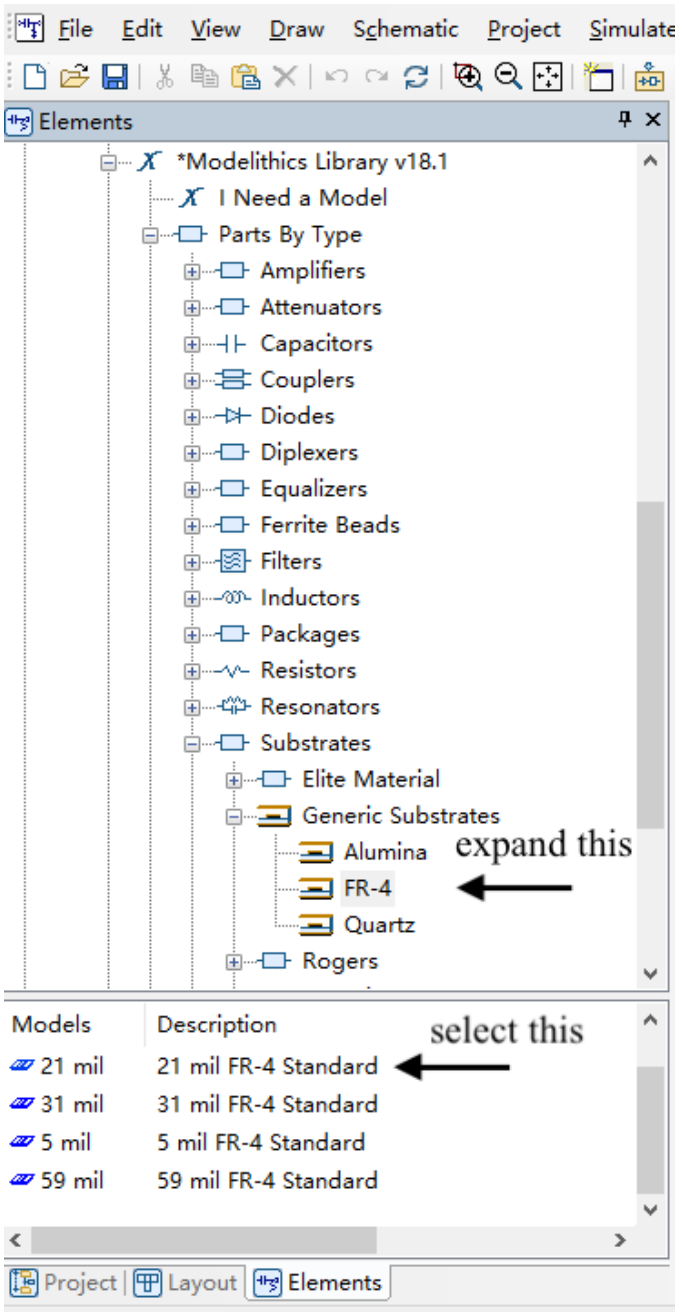


Figure 3.4: RF-4 in the library of AWR Microwave Office

Figure 3.5 shows the parameters of the microstrip substrate in the AWR Microwave Office after implementing either of the two ways.

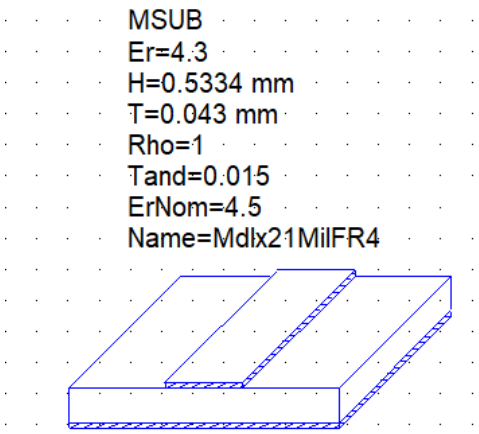


Figure 3.5: RF-4 as MSUB in AWR Microwave Office

3.3 DC Blocking Capacitors Selection

DC Blocking Capacitors are used for blocking the DC voltage and transporting AC voltage. DC blocking capacitors are placed on RF input and output paths of LNA.

For calculating the capacitance C,

$$C = \frac{1}{2\pi f X_c} \tag{3.1}$$

where:

- f is the frequency,
- Z_c is the reactance of the capacitor.

To make sure the capacitor working properly, its reactance value must be much smaller than the resistance value, namely

$$X_c < 0.1R \tag{3.2}$$

Based on the equations, we are able to choose a reactance value of $X_c = 2.65$ at the frequency of 4GHz, so the capacity value is 15pf, which is suitable for our LNA where the transmission line's characteristic impedance is on the order of 50Ω.

Here chooses a capacitor in the product serials of ATC 600S(see appendix D) by ATC Inc., which is 15pf with 10% tolerance. The model of the capacitor is included in the library of AWR Microwave Office and can be simply selected inside the software. (following Libraries ->*AWR web

site->Parts By Type->Lumped Element->Capacitor->ATC->600s, and in the expanding window below select 15pF 10% which is the capacitor model we need)

Figure 3.6 and Figure 3.7 show the path above to select the capacitor.

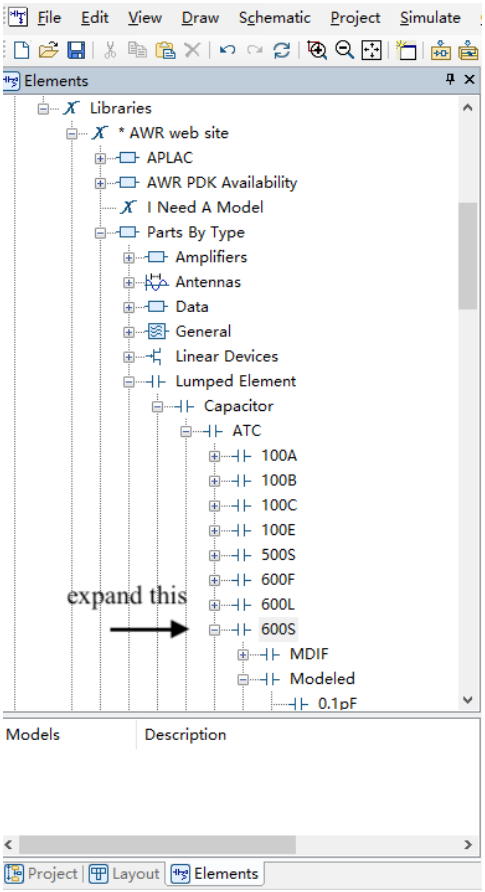


Figure 3.6: ATC 600S in Library of AWR Microwave Office (1)

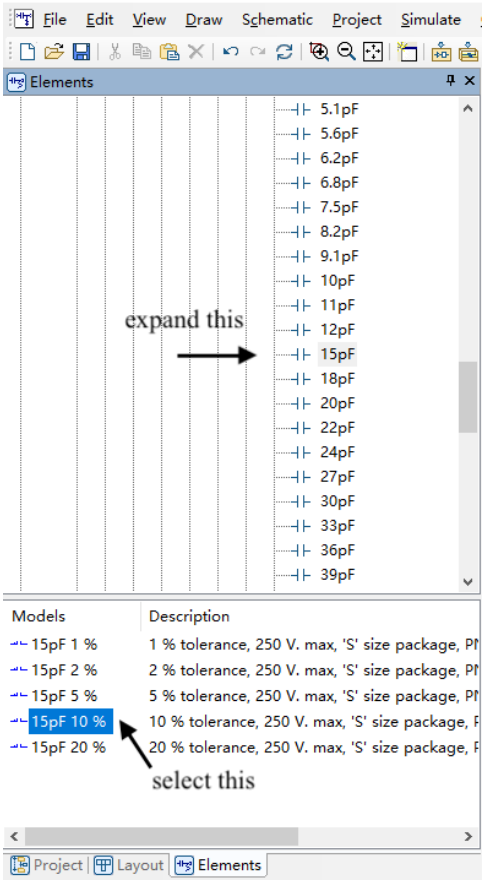


Figure 3.7: ATC 600S in Library of AWR Microwave Office (2)

Chapter 4

Amplifier Design

In this chapter, the figure of basic building blocks of the LNA will be firstly illustrated. And each block will be designed and synthesized together to have the ideal LNA. Then, a real LNA with microstrip lines will be developed based on the ideal one. Finally, the schematic of the LNA which satisfies the design goal will be obtained after turning and optimizing.

4.1 Basic Building Blocks of Two-Stage LNA

As mentioned in chapter 3, a two-stage amplifier is used for achieving the gain requirement in the design goal. Figure 4.1 shows the basic building blocks of the topology as a two-stage LNA, which consists of two transistors, two bias devices, an input matching network, an output matching network, and an inter-stage network. In the rest of this chapter, we will develop these blocks.

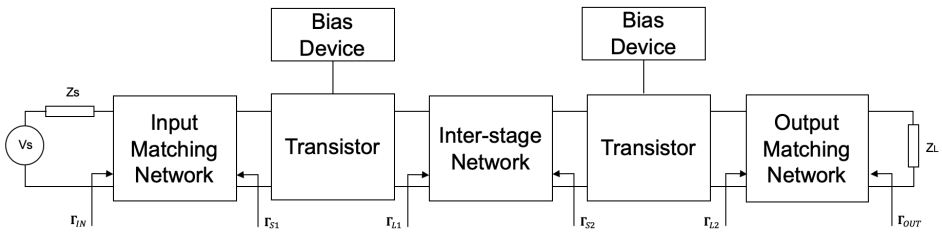


Figure 4.1: a two-stage LNA System Topology

4.1.1 Bias Network

The bias network is an important part in the design of microwave low-noise amplifiers. The bias network should be added to the transistor to provide the bias current and bias voltage and maintains the stable operating state. What's more, the addition of the bias network should not change the performance of the original microwave network, which means that the bias circuit is equivalent to an open circuit isolating the RF signal from the DC signal and preventing it from disturbing the DC source. In practice, many topologies of the bias network can be implemented to achieve this requirement. Here we use the structure of the fan-shaped open stub circuit.

The circuits of the fan-shaped open stub consist of a radial stub, a microstrip line with a length of l/4, and an additional line to connect the DC power source.

4.1.1.1 The radial stub

The radial stub is equivalent to a low impedance. Its radial shape helps in spreading the bandwidth and maintaining the reasonably small size of the circuits.

In AWR Microwave Office, the element 'MRSTUB2W' models a microstrip radial stub that terminates a microstrip line and connects to a single port at the reference plane. Figure 4.2 shows the element 'MRSTUB2W' and its parameters.

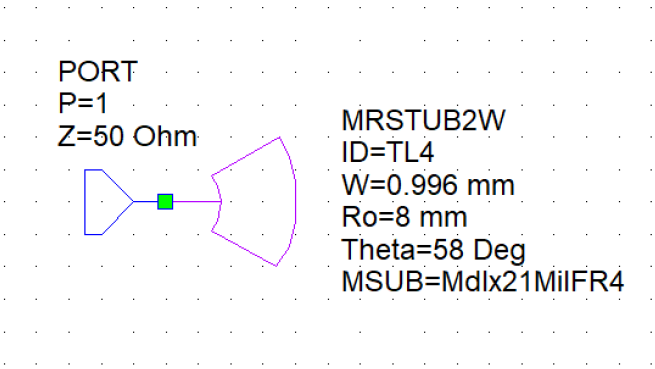


Figure 4.2: Parameters of MRSTUB2W with the Radial Stub

Where:

- W is the width of connecting microstrip line;
- Ro is the outer radius of the stub;

– Theta is the angle of the stub;
– MSUB is the substrate definition, which is consistent with the name of the substrate that we have selected. (see Chapter 3.2).

With the numerical values we used for the parameters in Figure 4.2, the input impedance of the radial stub is small (less than 2 Ohm) as shown in Figure 4.3, which means it acts like a short circuit in the frequency band of 3.8-4.2 GHz as we expected.

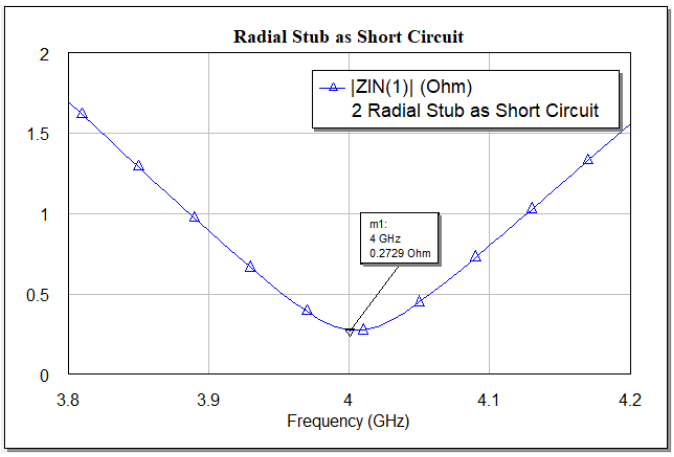


Figure 4.3: Impedance of Radial Stub

4.1.1.2 Fan-Shape Open Stub

The fan-shaped microstrip bias line acts as a bypass capacitor in the LNA. It prevents AC leakage caused by insufficient input impedance looking from the RF section to the DC section. On the other way, it is to prevent the DC bias circuit from affecting the impedance characteristics of the AC circuit.

Figure 4.4 shows the structure of the fan-shaped open stub that we used. A radial stub (ID=TL4, see Chapter 4.1.1), a microstrip line (ID=TL5) with a length of $\frac{1}{4}$ λ as an open line for the RF signal, and an additional line (ID=TL1) acting as port to receive the power from DC source are the key elements of the fan-shaped open stub. Other lines as the three-node junction MTEE$ (ID=TL3) and the microstrip line with ID=TL2 are used to connect the above lines.

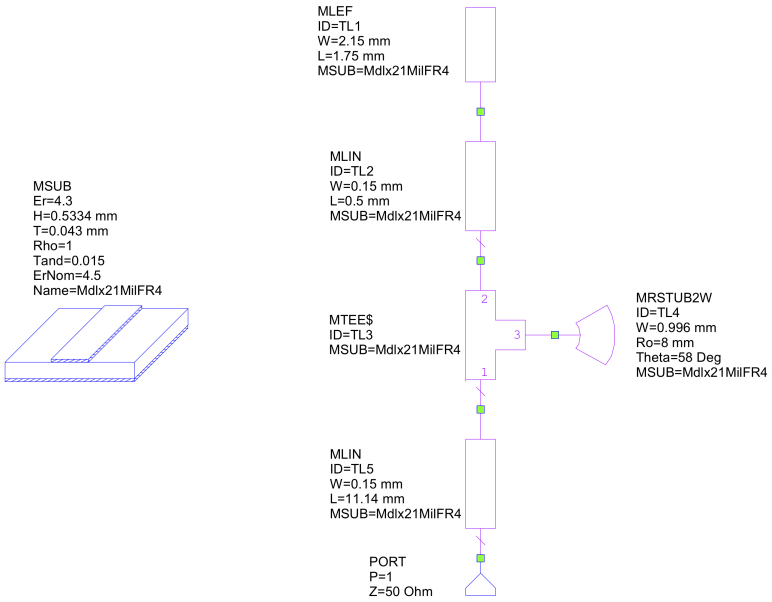


Figure 4.4: Bias Circuits

Usually, the length of the L1 is set to $\frac{1}{4}\ \lambda$, which in our case is 10.44 millimeters. While tuning it to 11.14 millimeters, it shows a better performance shown in Figure 4.5. We can see that the input impedance lies around the **open point** on the Smith Chart in the band of 3.8-4.2 GHz.

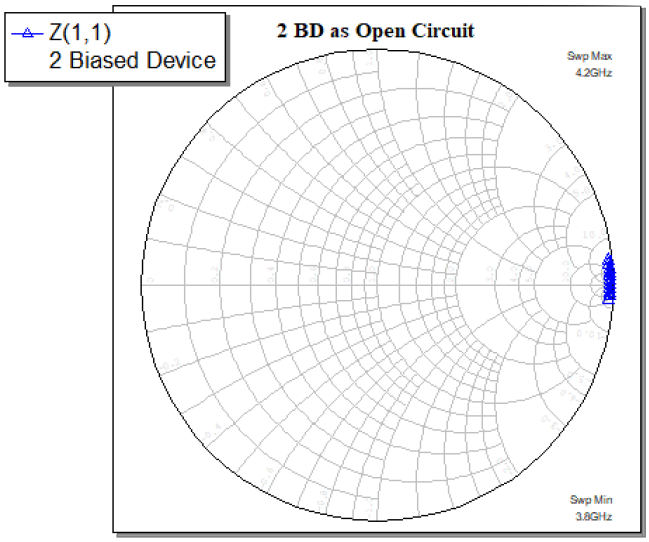


Figure 4.5: Bias as Open Circuit on Smith Chart

Finally, with the **blocking capacitors** (see Chapter 3.3) added on RF input and output paths, the schematic of the transistor with the bias network is shown in Figure 4.6.

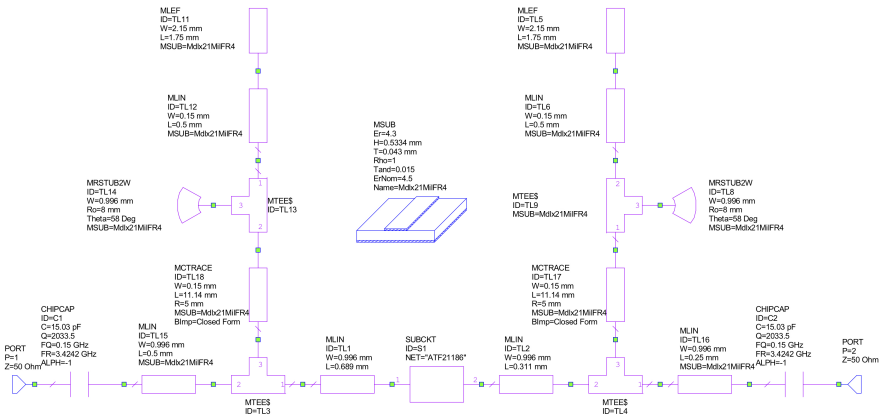


Figure 4.6: Schematics of Transistor with Bias Network

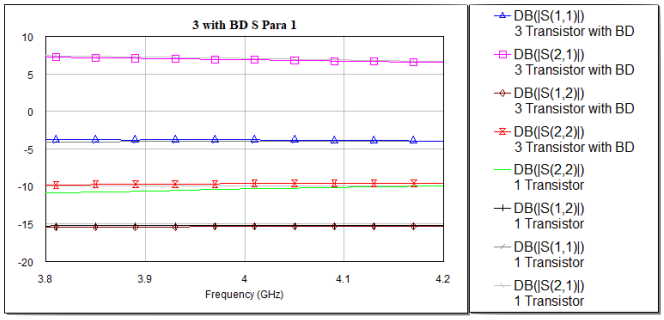


Figure 4.7: Comparison of the S parameters in amplitude

Figure 4.7 shows the comparison of the amplitude of the S parameters between the original transistor and the transistor with the bias network in the 3.8-4.2 GHz band. We can see that the amplitude difference between the S parameters is negligible and the bias network does not adversely affect the performance of the original transistor.

4.1.2 Decision of Γ_S and Γ_L

Table 4.1 shows the scattering parameters of the schematics of transistors with the bias network at 4 GHz.

Table 4.1: The S-Parameters of the Transistor with Bias Network

Parameter	Polar Form	Rectangular Form
S_{11}	$0.6458\angle 146.1$	-0.5362+0.3599i
S_{12}	$0.1706\angle -20.36$	0.1599-0.05934i
S_{21}	$2.212\angle 17.64$	2.108+0.6704i
S_{22}	$0.3295\angle 128.9$	-0.2069+0.2565i

A software called **Electronic Smith Chart** [7], allows us to perform manipulation and calculation related to the smith chart electronically, where we insert S parameters. The state of stability and maximal gain are given by this software in Figure 4.8. As we can see, the device is potentially instable, and the maximal gain is 11.1281 dB.

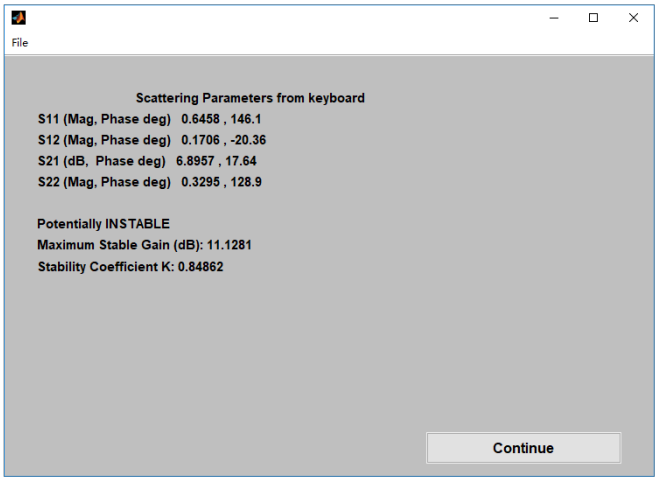


Figure 4.8: Stability and Maximal Gain given by Electronic Smith Chart

Since the LNA is potentially instable, we introduce the available gain G_a, which is defined as the ratio of the power that is available from the device to the power that is available from the source [8].

$$G_a = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{out}|^2} \tag{4.1}$$

Compared with G_T which is the function of Γ_S and Γ_L (see Formula 1.2), G_a only depends on Γ_S. And G_a is always larger than or equal to G_T.

Moreover $G_a = G_T$ is when the conjugate matching condition is imposed: Γ_L=(Γ_{out}) *, namely:

$$\Gamma_L = (\Gamma_{out})^* = \left(S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right)^* \tag{4.2}$$

The curve representing the gain G_a can be drawn on the Smith Chart. The points with the same value of the gain, which is G_a=constant, are on the same circle called the equal gain circle.

Also, the available gain expressed in decibel (in dB) $G_A|_{dB}$ defines as,

$$G_a|_{dB} = 10 log G_a \tag{4.3}$$

For a two-port network with multiple stages as shown in Figure 4.9, the overcall available gain of the cascade-stage network is expressed as the product of each stage, namely:

$$(G_a)_{TOT} = G_{a1}G_{a2} \tag{4.4}$$

in decibel,

$$(G_a|_{dB})_{TOT} = G_{a1}|_{dB} + G_{a2}|_{dB} \tag{4.5}$$

To design the amplifier as potentially instable, Γ_S and Γ_L can be chosen in the way: Γ_S in the stable region, then compute Γ_L for the maximum G_T , and making sure that the resulting Γ_L is inside the stable region also.

On the Smith chart in AWR Microwave Office, the appropriate Γ_S is selected after plotting circles of NF=cost and Ga =cost as in Figure 4.9. We select Γ_S=Γ_{opt} in order to have the lowest NF in the first stage of the amplifier. The corresponding reflection coefficients of Γ_L can be obtained by formulas with the scattering parameters by the conjugate matching condition with Formula 4.2. But here with the help of Electronic Smith Chart software, the results of Γ_L at 4GHz are directly found as in Table 4.2. Γ_S and Γ_L are both in their stability admission region of the generator and load respectively.

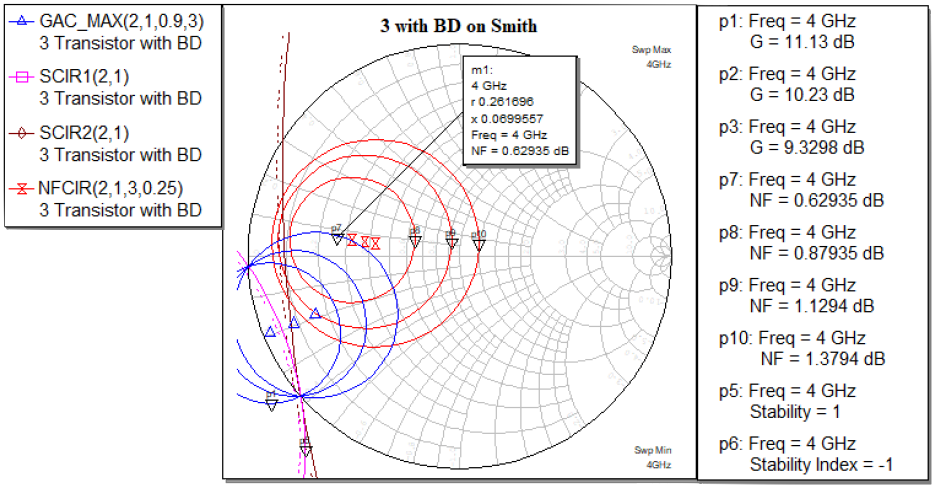


Figure 4.9: Transistor with Bias Device on the Smith Chart

Table 4.2: Reflection Coefficient of the Transistor with Bias Network

Reflection coefficient	**Value**
Γ_S	$0.589\angle 171.416$
Γ_L	$0.611\angle -138.341$

The **Electronic Smith Chart** has also obtained the gain which is 9.413 dB. Consider an amplifier with this gain in the first and second stages, the overall gain would be 18.826 dB, which satisfies the gain requirement of the design goal.

4.1.3 Input matching Network

We use the single stub matching method to design the ideal **input matching network**. Figure 4.10 shows the trace of the single stub method on the smith chart. Figure 4.11 shows its schematic in the AWR Microwave Office.

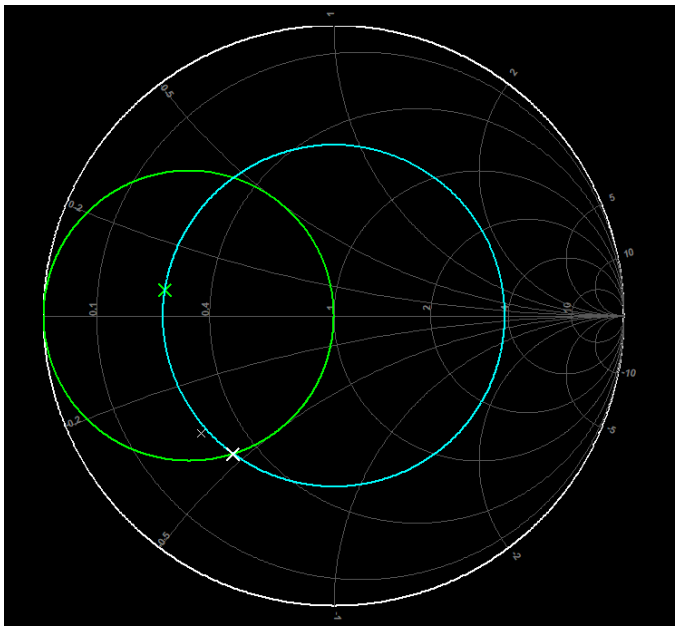


Figure 4.10: Single Stub Method of Output Matching Network on Smith Chart

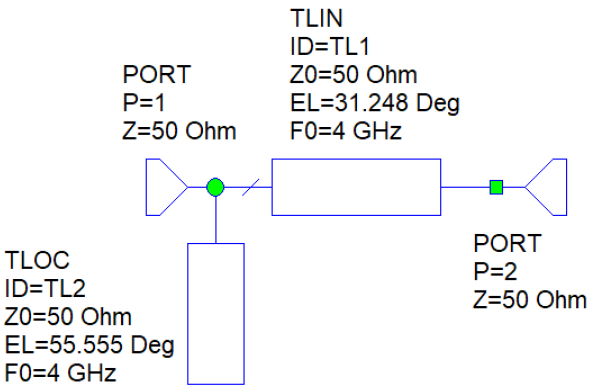


Figure 4.11: Schematic for Input Network

4.1.4 Output Matching Network

We also use the single stub matching method to design the ideal **output matching network**. Figure 4.12 shows the trace of the single stub method on the smith chart. Figure 4.13 shows its schematic in the AWR Microwave Office.

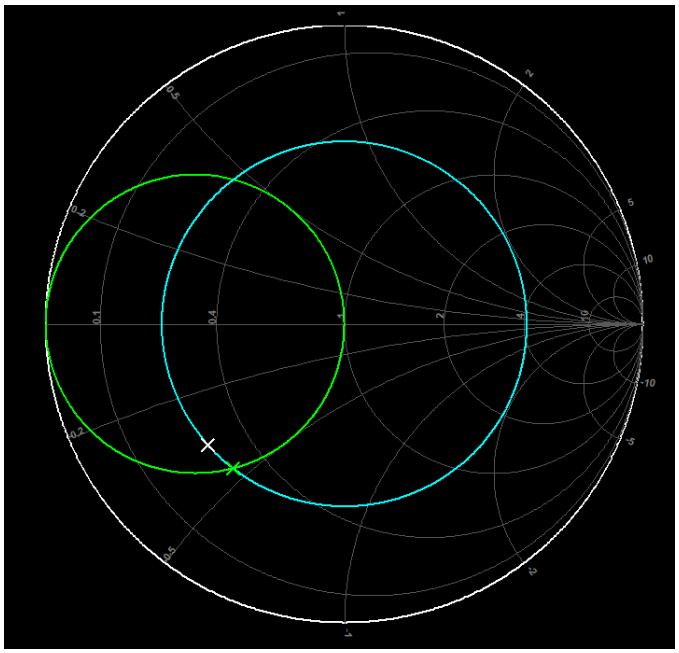


Figure 4.12: Single Stub Method of Output Matching Network on Smith Chart

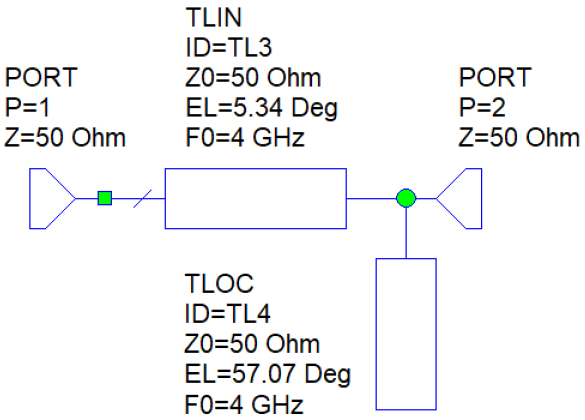


Figure 4.13: Schematic for Output Network

4.1.5 Inter-Stage Network

When designing a multi-stage amplifier, we need to determine the inter-stage connection of the amplifier. Figure 4.14 illustrates the Γ_S (green point) and the Γ_L (yellow point) which are calculated with the S parameters.

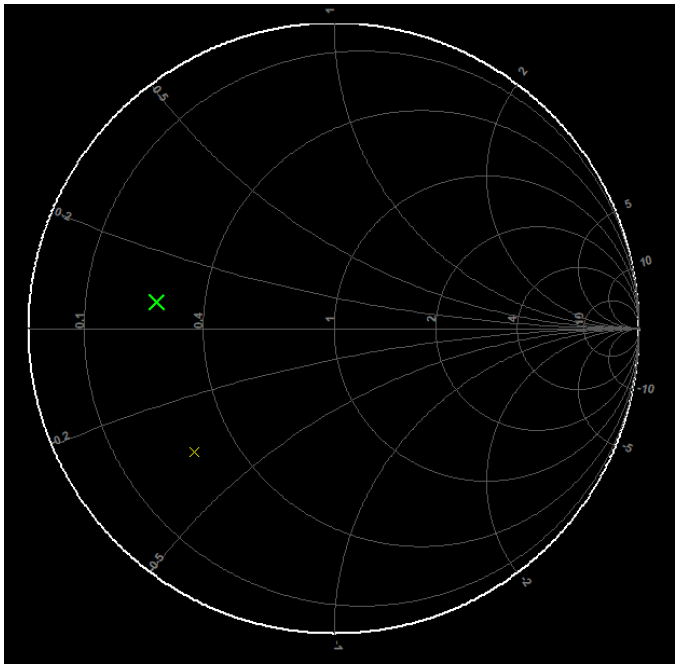


Figure 4.14: Γ_S and Γ_L of the transistor with the bias device on Smith Chart

We use the cross structure to design the inter-stage network. Figure 4.15 shows the schematic of the inter-stage network after turning.

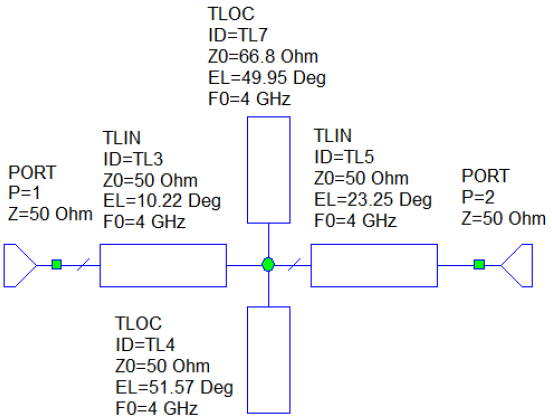


Figure 4.15: Schematic for Inter-Stage Network

Figure 4.16 shows the S_{11} and S_{22} of the inter-stage network in the frequency band 3.8-4.2 GHz. Compared with Figure 4.15, the inter-stage network matches well.

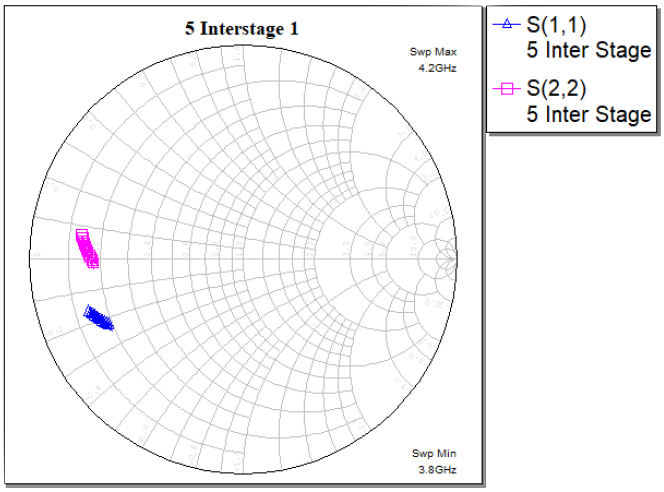


Figure 4.16: S_{11} and S_{22} of the Inter-Stage Network in 3.8-4.2 GHz

4.2 Synthesis of the LNA

Since the above networks are all designed based on the central frequency, which is 4 gigahertz. We want to adopt the whole design to the operating band on 3.8-4.2 GHz. This can be achieved by tuning the physical parameters of the transmission lines. As we mentioned before, the tuning process in AWR Microsoft is simply manually implemented by using the 'tuner tool'.

4.2.1 Introduce the 'Tuner Tool' and 'Tx Line Tool'

4.2.1.1 Tuner Tool

We can use the Tuner to tune a parameter's value in a circuit and observe the resulting response in the graph related to the value. The steps to use the tuning function in the AWR Microwave Office are very easy.

Click the Tune Tool button and select the desired element parameter or equation variable. Then Choose **Simulate** > **Tune** or click the **Tune** button on the toolbar. A "Tuner Dialog Box" will pop up as Figure 4.17. Then the parameter value can be tuned by sliding the tuning bar left or right.

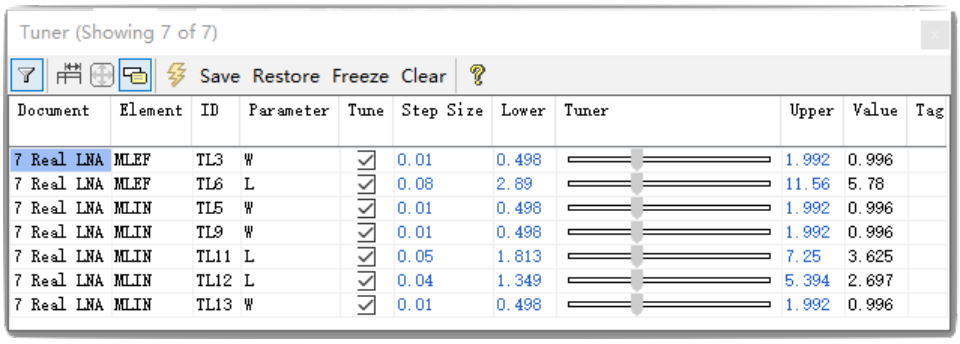


Figure 4.17: An Example of Tuner Dialog Box Window

4.2.1.2 Tx Line Tool

We will use microstrip lines to implement the practical design. Because in general, discrete components are used in the lower frequency band. In the frequency band above gigahertz, the parasitic parameter effect of discrete components becomes obvious. Besides, discrete components can only have nominal values, which limits their application in high-frequency circuits. At this point, distributed parameter elements such as microstrip lines and microstrip stubs are used to constitute matching networks.

The feature of the microstrip line is characterized by its physical dimensions. The 'Tx line', a tool embedded in AWR Microwave Office, is used to calculate the physical dimensions of the microstrip line.

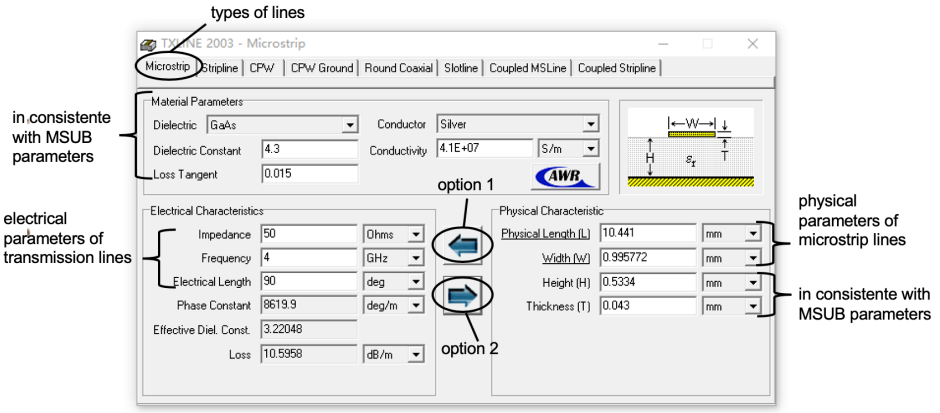


Figure 4.18: Tx Line Window

Figure 4.18 shows the Tx line window. On the top of the window, there are diverse types of lines. Here we choose the microstrip lines. The electrical parameters of the transmission line can be translated into the physical parameters of the microstrip with option 2, vice versa with option 1. The material parameters and the physical characteristic of height and thickness should be consistent with the substrate that we have selected.

4.2.2 Ideal LNA Synthesis

We implement the process of synthesis of the ideal two-stage LNA by the steps:

- Adding each part of networks to the synthesis schematic
- Tuning the added part while keeping other parts fixed
- Value of gain, NF and return loss are all changing simultaneously while tuning
- Pay attention to all the three changing variables
- Keep tuning until the variants satisfy our design goal, if no, go back to the second step.

Figure 4.19 shows the result of the overall tuned schematic of the two-stage low-noise amplifier.

Figure 4.20, Figure 4.21 and Figure 4.22 represent the gain, NF and return loss of the overall tuned schematic respectively.

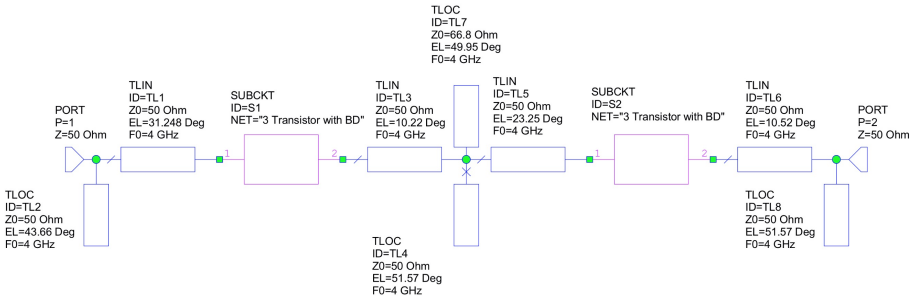


Figure 4.19: Two-Stage LNA Schematic

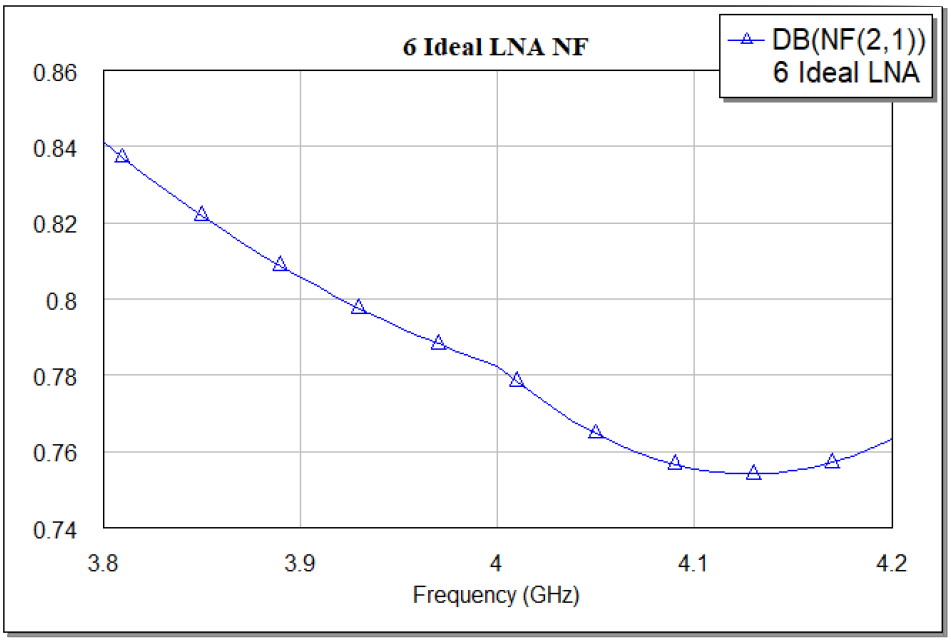


Figure 4.21: NF of LNA

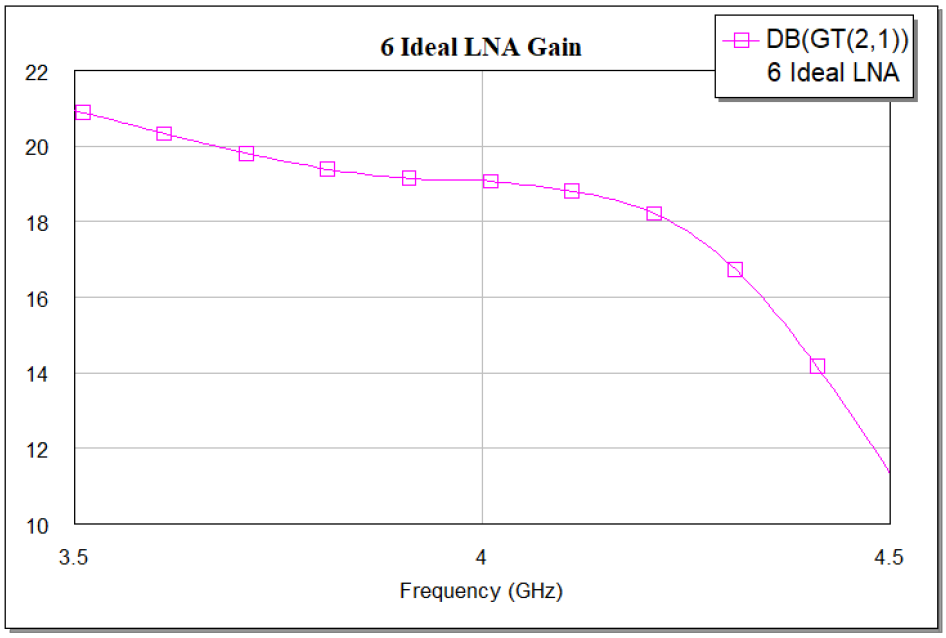


Figure 4.20: Gain of LNA

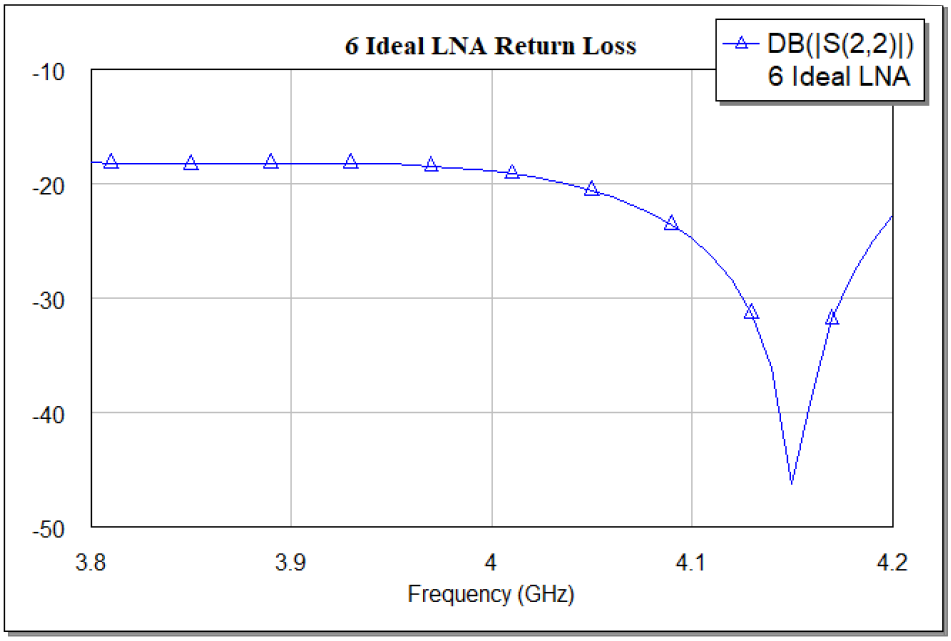


Figure 4.22: Return Loss of LNA

4.2.3 Real LNA Transformation

The above synthesis schematics use the ideal lossless transmission lines. Now we transfer the ideal lossless to the microstrip lines. Unlike lossless transmission lines, the microstrip lines are not ideal, for example, they may have loss and the s parameters may have discontinuities in the junctions. The transformation procedures are:

- The ideal transmission line is replaced with the microstrip line MSTUB (see section 3.2).
- The dimension of this line can be calculated by the TX line tool (see subsubsection 4.2.1.2.
- To connect other additional components in the circuit schematic, some extra microstrip lines are added, such as T-Junctions and Cross-Junctions.

Figure 4.23 shows the result after all the steps, the schematic of LNA with the replaced microstrip lines. Figure 4.24, Figure 4.25 and Figure 4.26 represent the gain, NF and return loss of the overall tuned schematic respectively.

It is easy to see from the plots that the gain and return loss do not satisfy our design goal. This is caused by the loss and discontinuities after introducing the microstrip lines. In the following chapter, we will try to compensate them.

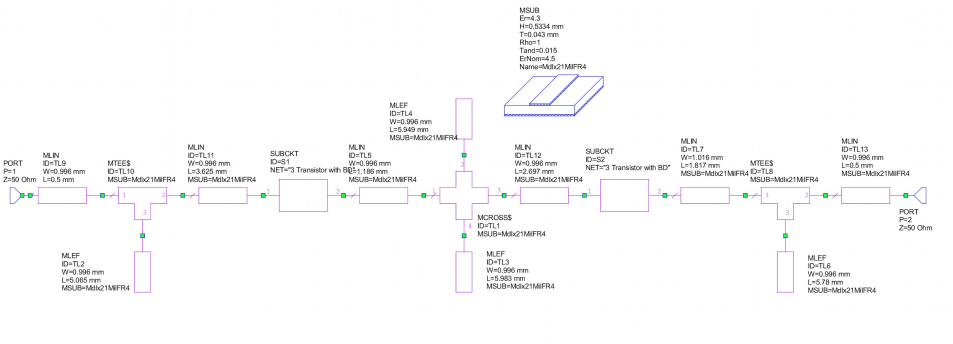


Figure 4.23: LNA with Microstrip Lines

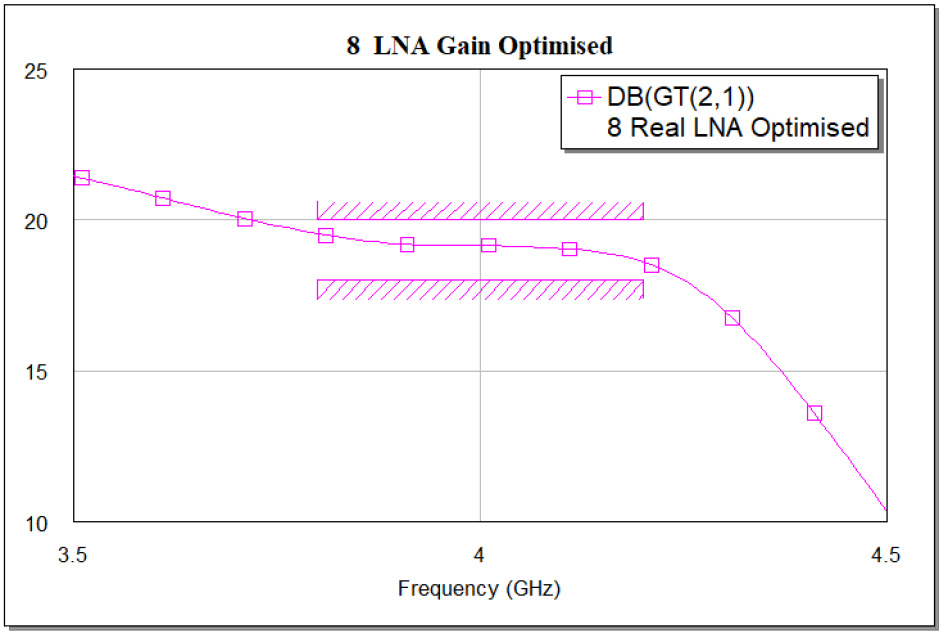


Figure 4.24: Gain of LNA with Microstrip Lines

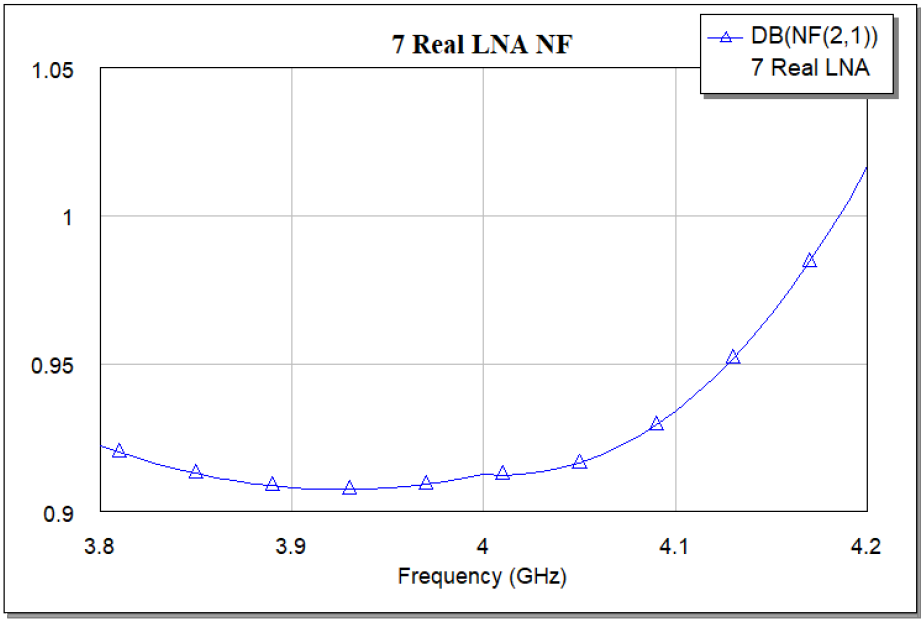


Figure 4.25: NF of LNA with Microstrip Lines

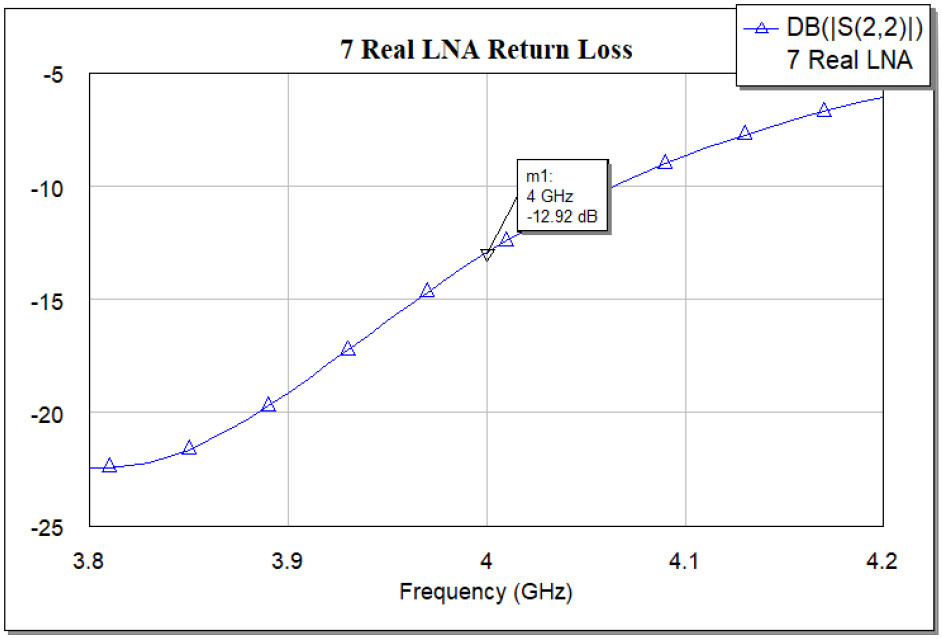


Figure 4.26: Return Loss of LNA with Microstrip Lines

4.3 Final Schematic of the LNA after Turning and Optimizing

Because the gain, NF and return loss (see Figure 4.24, Figure 4.25 and Figure 4.26) do not satisfy our design goal, the overall LNA schematic needs further tuning and optimizing. Since the Tune Tool has already been introduced in **Chapter 4.2.1**, we will say no more about it. Now we focus on the optimizer tool.

Optimization is a process during which the NI AWR Design Environment automatically adjusts designated circuit parameters such as circuit-element values, transmission-line lengths, and similar quantities to achieve user-specified performance goals [9]. The convenience of the operation for optimizing in AWR Microwave Office allows us to easily perform the optimizing process and to achieve our design goal, such as gain, NF and return loss.

The steps for setting the optimization are as follows:

- Setting Element Parameters for Optimization
- Adding Optimization Goals
- Optimization Goals on Graphs
- Performing the Optimization

Setting Element Parameters for Optimization It means we need to specify which element parameters or variables are used for optimization. Through the Equation (**choose Draw** > **Equation**) we can add the equations of the variables with the initial value. Then from the Variable Browser (**choose View** > **Variable Browser**), we tick the variable for optimization in the **Optimize** column. An example is illustrated in Figure 4.27.

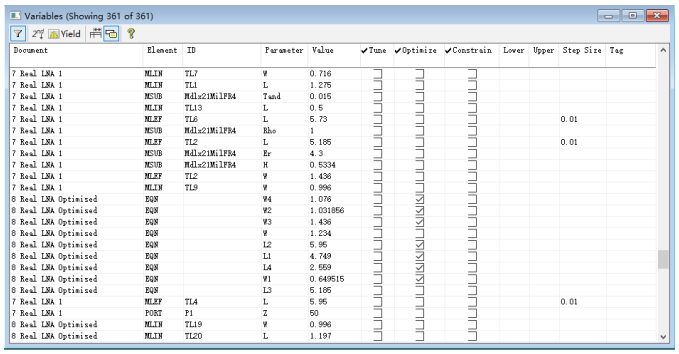


Figure 4.27: The Variable Browser Window

Adding Optimization Goals The **Optimizer Goals** node in the Project Browser contains sub-nodes for each optimization goal that we create for the project. To add an optimization goal, Choose **Project** > **Add Optimizer Goal** and choose **Add Optimizer Goal**. Figure 4.28 shows the optimal goals, which the return loss is set to be less than -15 dB, the gain between 18-20 dB and the NF less than 1.2 dB.

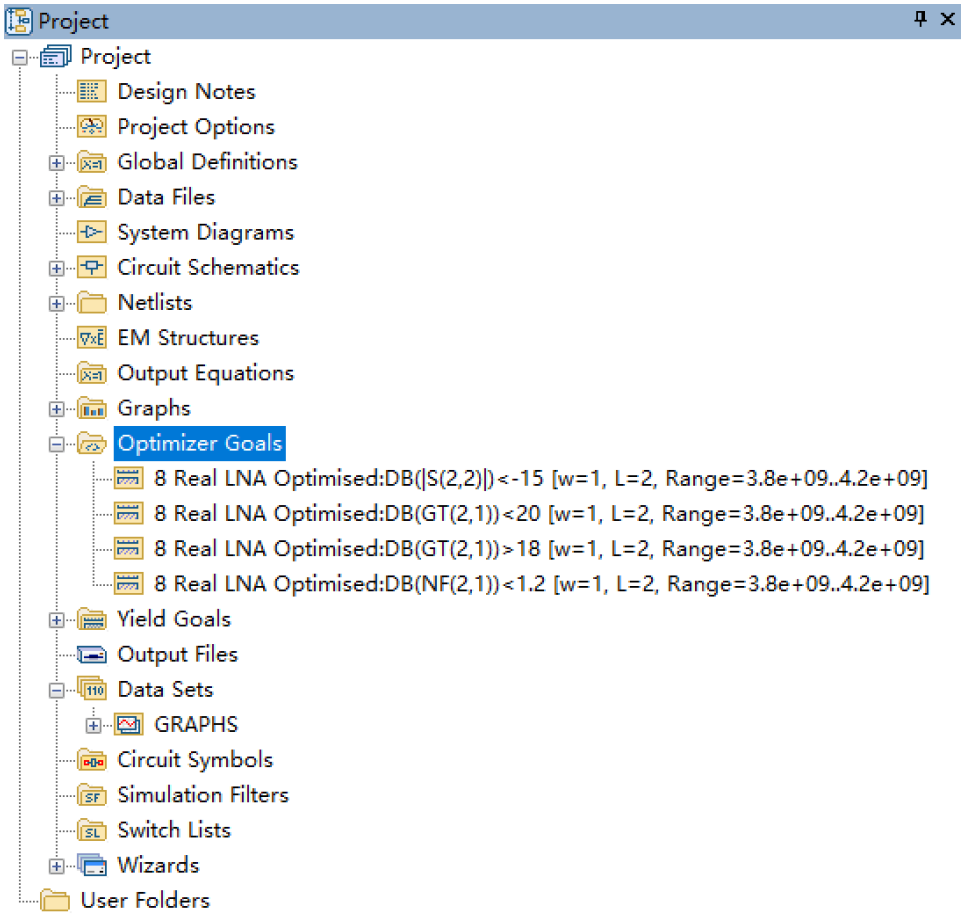


Figure 4.28: Optimizer Goals Setting Window

Optimization Goals on Graphs The goals display in the same color as the measurement. From the graph, we can see clearly the goals and the measurements and understand whether they have matched well.

Performing the Optimization To optimize the circuit, choose **Simulate** > **Optimize**. The optimizers are controlled by entries in the optimizer dialog

box, as in Figure 4.29. Click '**start**' to begin the optimization process. After the optimization process has finished, we get the optimized variables.

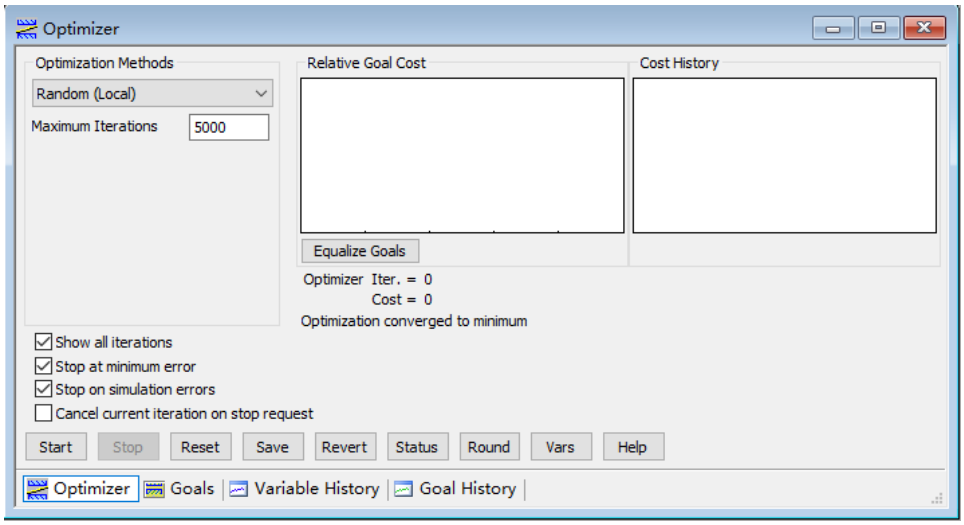


Figure 4.29: Optimizer Dialog Box Window

Figure 4.30 shows the final schematic for the two-stage LNA obtained after the tuning and optimizing. (The results for the variables may be different. The figure shows just an acceptable one from all the possible results.)

To better generate the layout view, we expand the components of Figure 4.30 (The Final Schematic for Two-Stage LNA after Tuning and Optimizing). Figure 4.31 shows the overall schematic of the two-stage LNA with each component shown in detail.

Figure 4.32, Figure 4.33 and Figure 4.34 represent the measurement graphs for transducer gain, NF and return loss for the two-stage LNA, where we have enlarged the measurement frequency range to 3.5-4.5 GHz instead of 3.8-4.2 GHz to observe better the optimization goal. And it is easy to see that measurements in 3.8-4.2 GHz are all in the optimization range.

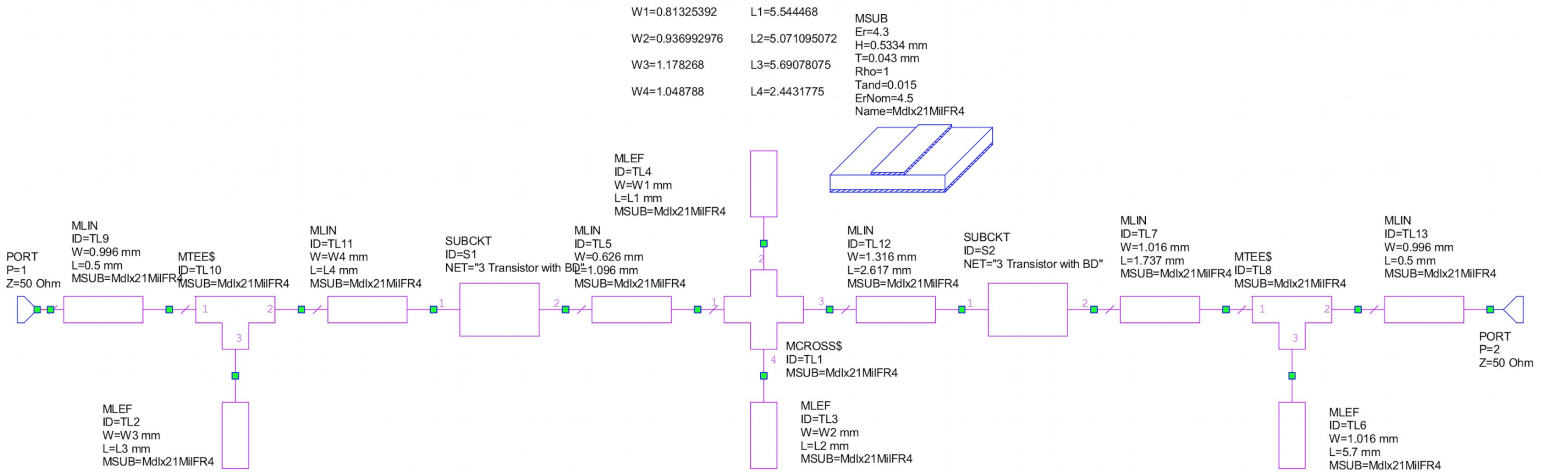


Figure 4.30: The Final Schematic for Two-Stage LNA after Tuning and Optimizing

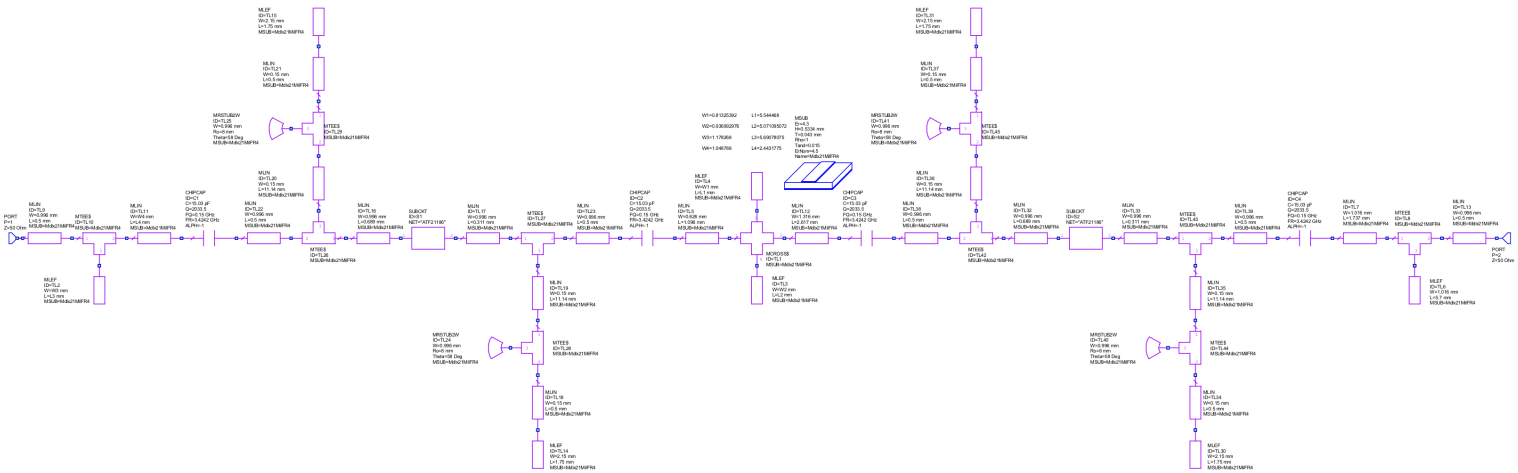


Figure 4.31: Overall Schematic of Two-Stage Low Noise Amplifier

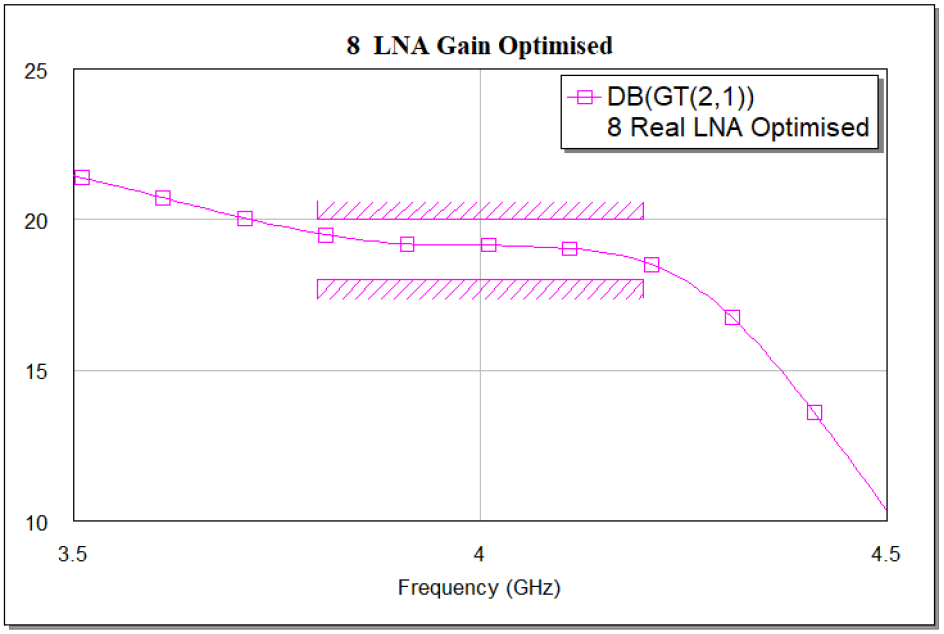


Figure 4.32: Transducer Gain of LNA after Tuning and Optimizing

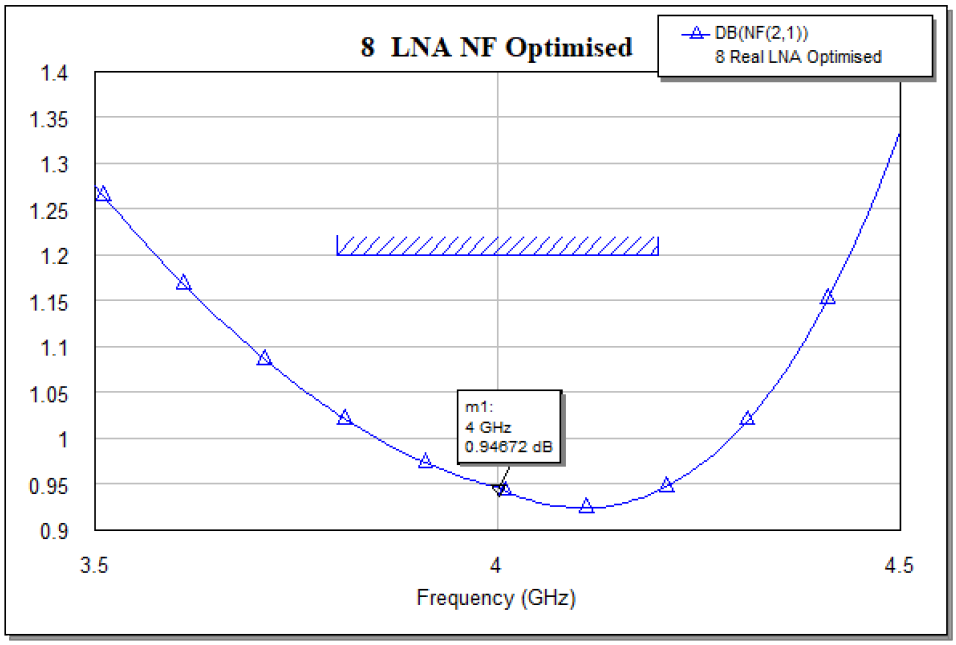


Figure 4.33: NF of LNA after Tuning and Optimizing

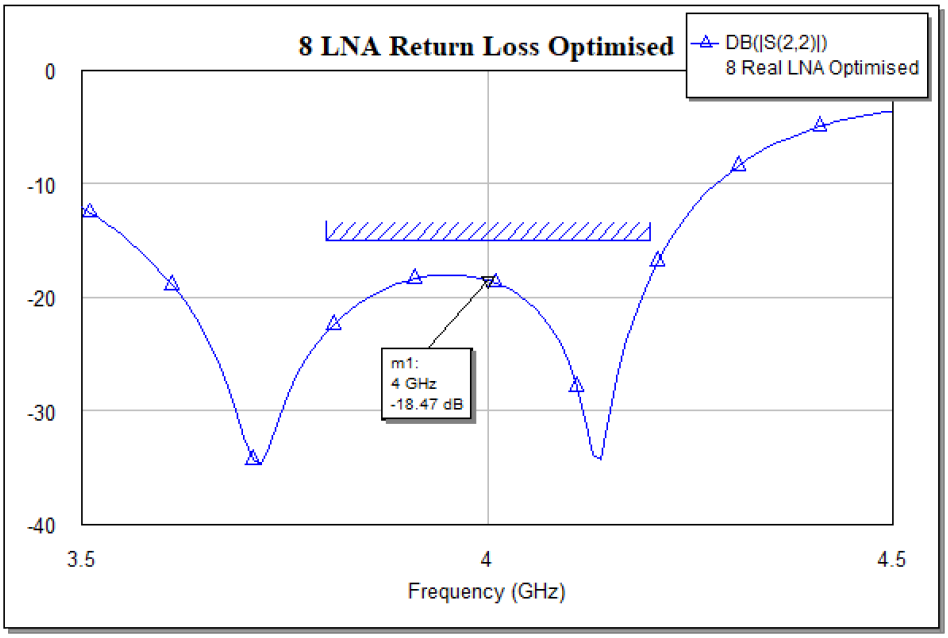


Figure 4.34: Return Loss of LNA after Tuning and Optimizing

Chapter 5

Amplifier Layout

Layout is a view of the physical representation of a circuit, in which each component of the schematic is represented by a layout cell in the AWR Microwave Office. In this chapter, layout cells for **capacitor** and **transistor** will be developed. And the **final layout** of Two-Stage LNA will be presented.

5.1 Layout Objects (Cells)

A layout requires a library of layout cells. In AWR Microwave Office, the foundry library uses four types of layout cells, as **built-in parameterized cells**, **artwork cells**, **user-defined cells**, and **no layout** (ports, for example) [10].

Built-in Parameterized Cells Parameterized cells are layout representations that use the parameter values of the electrical components to render the layout representation. The software has built-in parameterized cells for most of the standard microstrip, stripline, and coplanar waveguide components. Parameterized cells can be easily configured in the Layout Process File (LPF). This file describes the different types of lines and the drawing layers used to construct them. Parameterized cells provide the layout cells for most of the components needed in a foundry library.

Artwork Cells Artwork cells are standard GDSII or DXF cells that have connection points added to them for use as layout cells. Artwork cells are used for non-parameterized geometry such as vias, FETs and bias pads. The creation of artwork cells is simple; the cells are read into or created in the Artwork Cell Editor, and then connection faces are drawn onto the cells and the cells are saved as a library.

User-Defined Cells If a more sophisticated parameterized layout cell is required, then a fully parametric layout cell can be created using standard C++ which is compiled into a DLL that can be easily distributed and shared amongst users. The Cell Wizard, which is part of a layout customization kit, can help generate the C++ source code. In our project, we do not have such kinds of sophisticated cells.

No Layout For some electrical components, we may not want a layout representation associated with the component (such as a parasitic capacitance and ports).

Generally, a foundry library can be created with the **built-in configurable cells** and the **artwork cells**, since only a few parameterized cells typically need to be created for a foundry process. As for our project, the microstrip line's layout is a good example of **Built-in Parameterized Cells**, which uses the width (W) and length (L) parameters to draw a rectangle of width W and length L; Capacitor and transistor's layouts are **as Artwork Cells**; Since we do have sophisticated parameterized cells to define, we will not use **User-Defined Cells**; For cells as no layout, the ports have **no layout** representation in our project. The process for creating these cells will be described later.

5.1.1 Capacitor Layout Cell

The DC blocking capacitor is selected from the Element Libraries (see Chapter 3.3) in the AWR Microwave Office. A GDSII cell file with its layout of the capacitor has been already synchronized from schematic view to layout view. From its schematic view, by choosing **View** > **View Layout**, the corresponding manufacture layout is automatically shown in a pop-up layout view window. Figure 5.1 shows the layout of the capacitor.

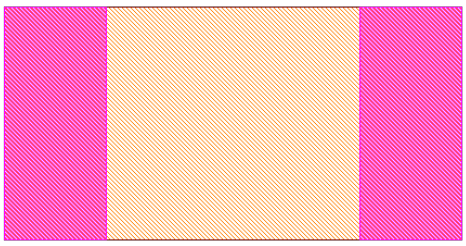


Figure 5.1: Capacitor Layout

5.1.2 Transistor Layout Cell

The package layout of the transistor (ATF-21186) is represented in its manufactory datasheet. (see Appendix A). We need to create the Artwork Cell for the transistor according to the dimension on datasheet because the manufactory has not developed GDSII Cell Library for it. The steps to create the Artwork Cell are:

- Import the **Layer Process File**
- Edit **Database Unit** and default **Grid Size**
- Create the Artwork Cell
- Add Ports to the Artwork Cell
- Assigning the Artwork Cell to transistor

As to the needs of the proposition and the limitations of the coverage for our thesis, the detailed procedures which are needed to operate on computers for achieving these steps above and creating the Transistor Cell are given in Appendix E. Here the completed artwork cell of the transistor is illustrated in Figure 5.2.

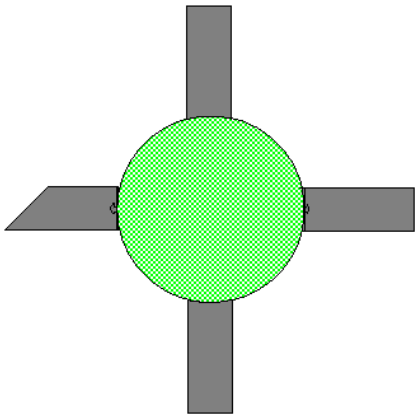


Figure 5.2: Artwork Cell of the Transistor

5.2 Layout of Two-Stage Low Noise Amplifier

In the AWR Microwave Office, a layout representation of a schematic is obtained simply, just by clicking the schematic window to make it alive, then choosing **View** > **View Layout**. A layout window tab will open with an automatically-generated layout view of this schematic. Or the **View Layout** button on the toolbar can be clicked to view the layout on an already opened schematic.

From Figure 4.31 (*Overall Schematic of Two-Stage Low Noise Amplifier*), Choose **View** > **View Layout** to see layout view for fabrication. The layout displays in the workspace. Choose **Edit** > **Select All**, and then **Edit** > **Snap Objects** > **Snap Together** to snap the layout together. The corresponding layout is shown in Figure 5.3.

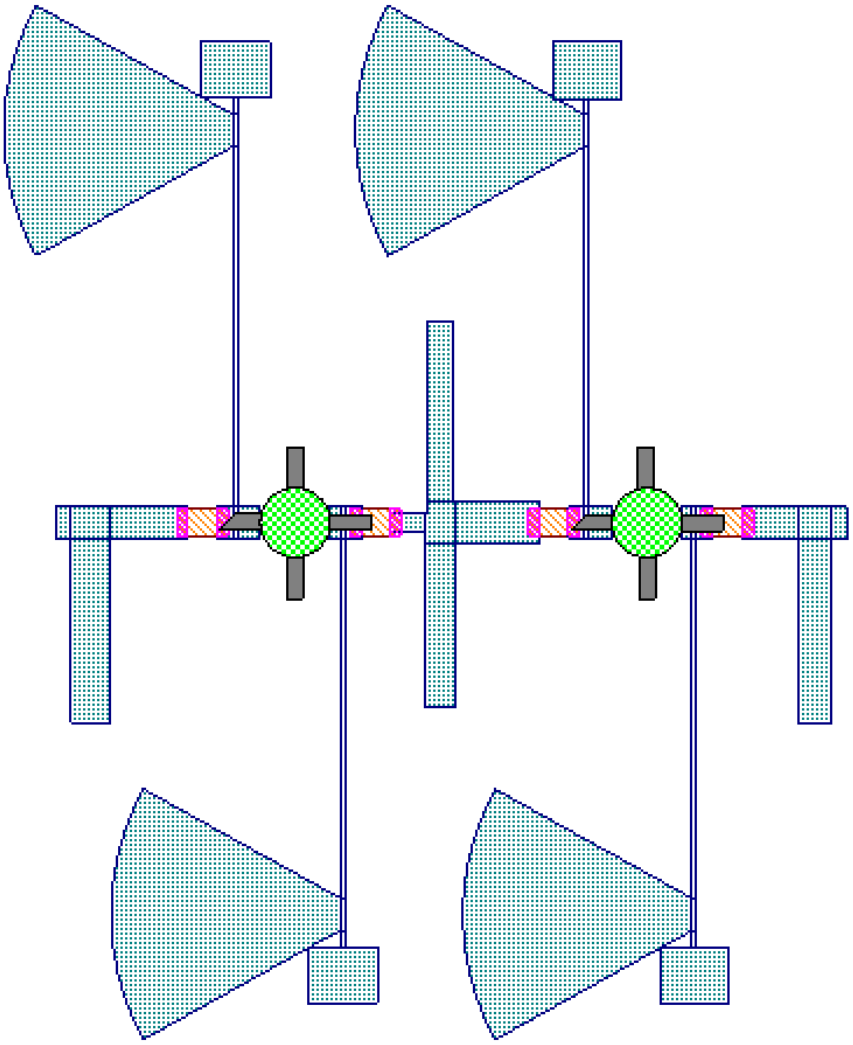


Figure 5.3: Layout of the Two-Stage Low Noise Amplifier

Chapter 6

Conclusion

In this chapter, we will first perform the yield analysis and yield optimization to LNA. Then, we conclude the whole project.

6.1 Yield Analysis

In the fabrication process, the rate of the finished products, in other words, the "yield" is the key factor to reduce production cost and to enhance the production efficiency. After our LNA has been designed, the product failure may happen due to processing errors. However, we can perform the yield analysis on the LNA and adjust the nominal value for parameters to obtain a higher yield.

In AWR Microwave Office, the yield analysis uses the traditional "Monte Carlo" method. In this mode, the parameter values set to have statistical distributions are set to random values based on the parameter's statistical distribution at each iteration.[9]

The process to perform the Yield Analysis in AWR Microwave Office:

- Setting Statistical Properties
- Setting Yield Analysis Goals
- Performing Yield Analysis
- Analyzing the Result and Optimizing the Result

6.1.1 Setting Statistical Properties

We need to consider which variables will produce the processing error and influence the yield value, then we will assign the statistical properties to

them.. The "LNA schematics" (see Figure 4.31) has 74 of its parameters can be set up for yield. The **H**, **Er** of the substrate as MSUB (Figure 3.5), the width **W** and **L** of all the microstrip lines as MLIN, the **W**, **Ro** and **Theta** of the radial stub MRSTUB2W (Figure 4.2). According to transmission line theory and knowledge of the capacitors, the thickness **T** (in element MSUB) of the microstrip line and the capacitance **C** of the blocking capacitors (in element CHIPCAP) have limited influence on the circuit performance (which can be also easily proved with the yield analysis in AWR microwave Office), so we do not consider them here.

We note the easily-confused parameters as "element name" \"parameter name" or directly "parameter", so the 74 parameters are listed as: Mdlx21MilFR4\Er, Mdlx21MilFR4\H, TL12\W, TL13\W, TL14\W, TL15\W, TL16\W, TL17\W, TL18\W, TL19\W, TL20\W, TL21\W, TL22\W, TL23\W, TL12\L, TL13\L, TL14\L, TL15\L, TL16\L, TL17\L, TL18\L, TL19\L, TL20\L, TL21\L, TL22\L, TL23\L, TL24\Ro, TL24\Theta, TL24\W, TL25\Ro, TL25\Theta, TL25\W, TL30\W, TL31\W, TL32\W, TL33\W, TL34\W, TL35\W, TL36\W, TL37\W, TL38\W, TL39\W, TL30\L, TL31\L, TL32\L, TL33\L, TL34\L, TL35\L, TL36\L, TL37\L, TL38\L, TL39\L, TL40\Ro, TL40\Theta, TL40\W, TL41\Ro, TL41\Theta, TL41\W, TL5\W, TL6\W, TL7\W, TL9\W, TL5\L TL6\L, TL7\L, TL9\L , "W1" ,"W2" ,"W3" ,"W4", "L1" ,"L2" ,"L3" ,"L4".The tolerant of the variable will be set as 5%. The distribution will be specified as uniform.

The distribution of the variables in AWR Microwave Office can be set as Uniform, Normal, Log-Normal, Discrete, Normal-Tol and Normal Clipped. The mode of the distribution should be corresponding to the practical processing process. Here we just chose the common distribution as "uniform" for simplicity. To set the statistical properties of variables, open the **Variable** Box and click the **Yield** bottom, then tick the option "**Use Statistics**", insert the value of **Tolerance** and specify the statistical **Distribution** for the corresponding variables listed above. Figure 6.1 shows the example of the statistical settings for parameters.

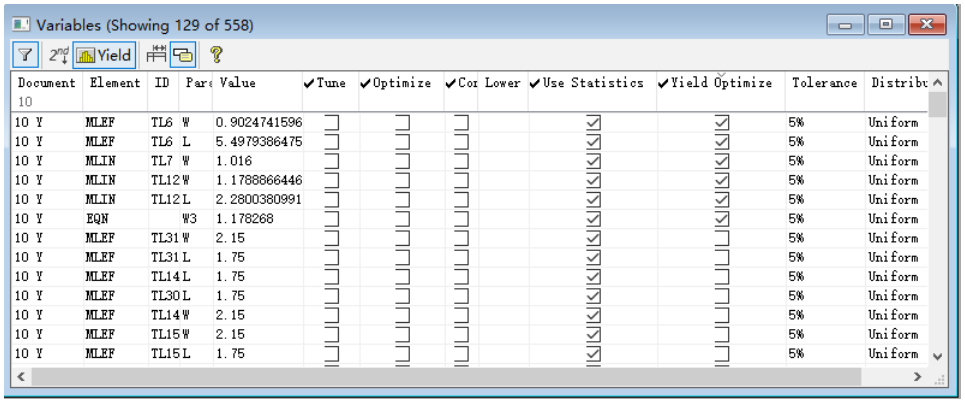


Figure 6.1: The Variable Box Window for Yield

6.1.2 Setting Yield Analysis Goals

The **Yield Goals** node in the Project Browser contains sub-nodes for each yield goal that we expect for the project. To add a yield goal, choose **Project** > **Add Yield Goal** and select **Add Yield Goal**. Figure 6.2 shows the yield goals created according to the design goals, in which the return loss is set to be less than -15 dB, the gain between 18-20 dB and the NF less than 1.2 dB.

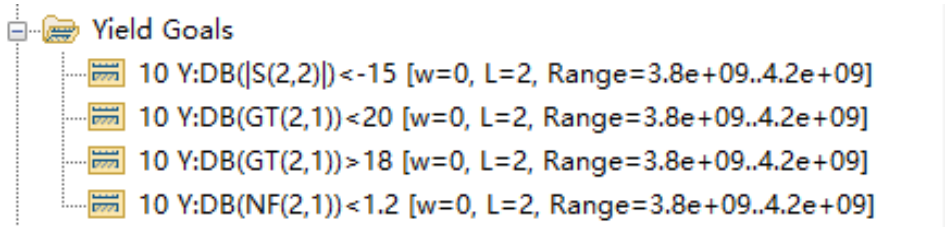


Figure 6.2: The Yield Goal

6.1.3 Performing Yield Analysis

To analysis the yield, choose **Simulate** > **Yield Analysis**. The yield procedure is controlled by the yield dialog box, as in Figure 6.3. Select **Yield Analysis** in the pull-down list of Yield Methods. Click '**start**' to begin the yield analysis. After the optimization process has finished, we get the results.

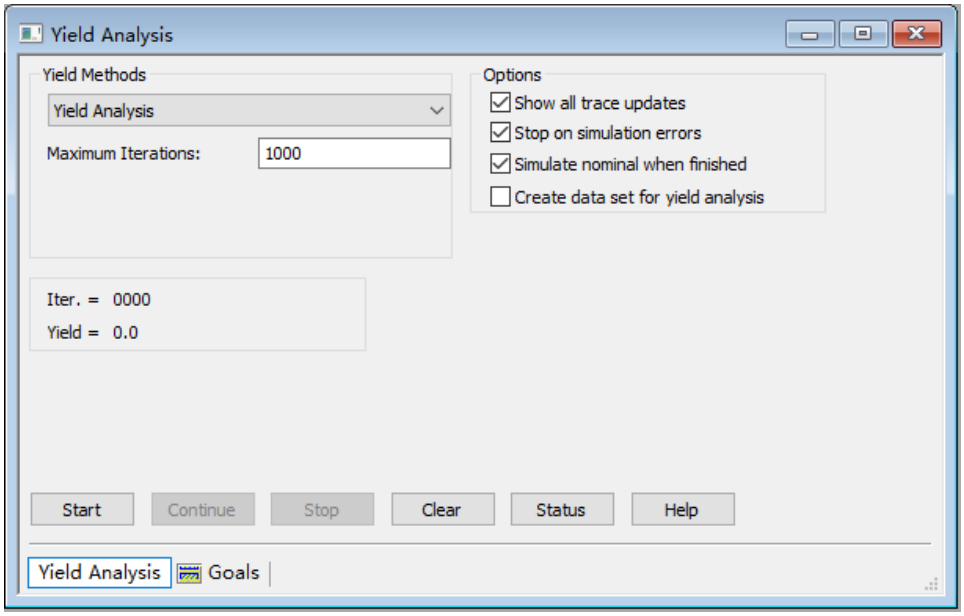


Figure 6.3: The Yield Analysis Control Dialog

On the graphs, the result plot traces for each statistical trial simulated with the Monte Carlo method. The following Figure 6.4, Figure 6.5 and Figure 6.6 show plots of the Gain, Noise and the Return Loss for the LNA. Figure 6.7 shows the yield value (as a percentage) of the LNA with respect to the yield goals we set.

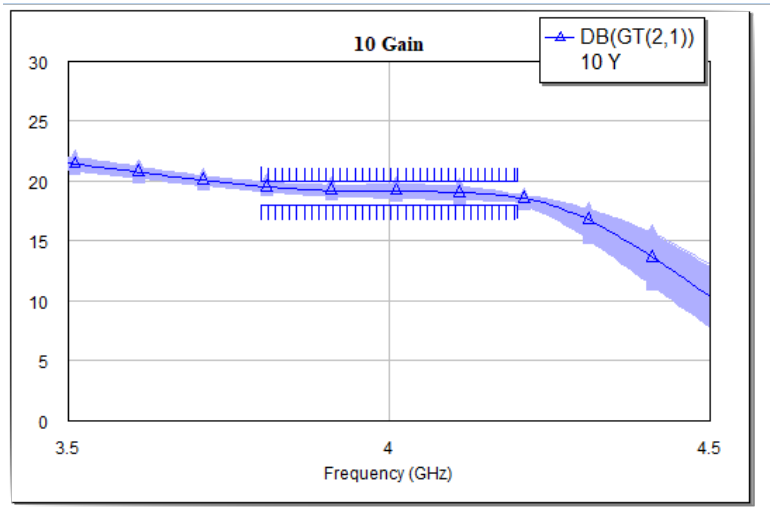


Figure 6.4: Yield Traces for Gain

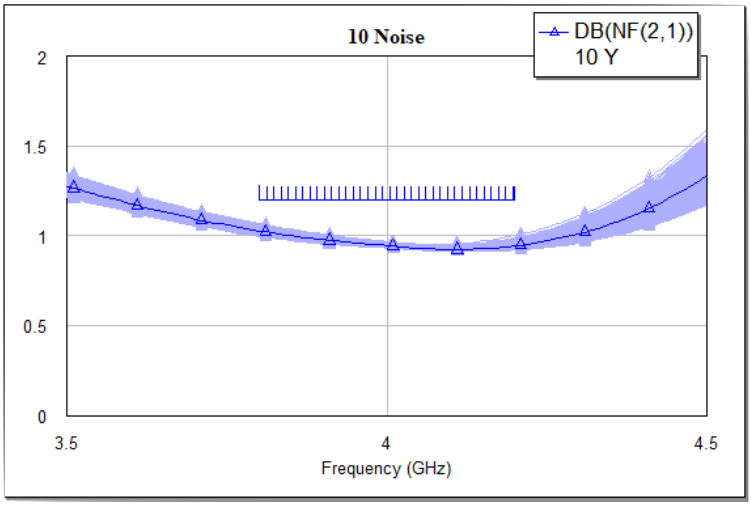


Figure 6.5: Yield Traces for Noise

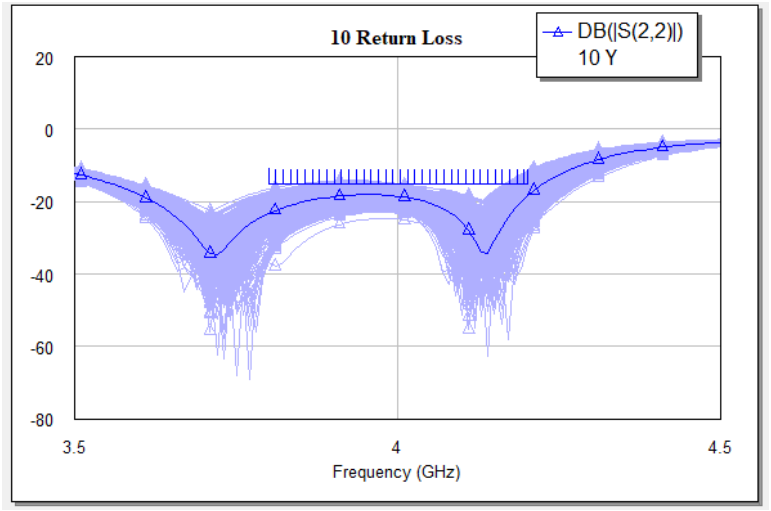


Figure 6.6: Yield Traces for Return Loss

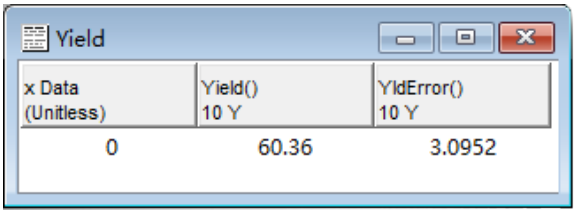


Figure 6.7: Yield Results

6.1.4 Analyzing and Optimizing the Result

As we can see from Figure 6.7, the yield value computed from the yield analysis is 60.36%, which is quite low. Because the optimal design does not give the optimal yield. In the following section, we will try to increase this value by implementing the yield optimization.

By observing the traces of the gain, noise and return loss in Figure 6.4, Figure 6.5 and Figure 6.6, it is easy to find out that the traces of the gain and noise are almost all in the goal range, while many traces of the return loss are lying out of the range. In other words, the Return Loss is the most critical factor that introduces yield degradation.

We need to identify which variables have the biggest influence on the Return Loss so that we can perform the yield optimization to enhance the yield. To do this, we firstly introduce the **sensitivity measurement (YSen)** of all the 74 parameters in the first subsection 6.1.1. The histogram graph of sensitivity determines how sensitive the yield is to the parameter variations. Then we use the **Pareto measurement (YPareto)**, which can help analyze the component sensitivity and the results are rank-ordered from largest to smallest making it very easy to identify which variables have the biggest influence on the Return Loss. Figure 6.8 shows the result of Pareto measurement.

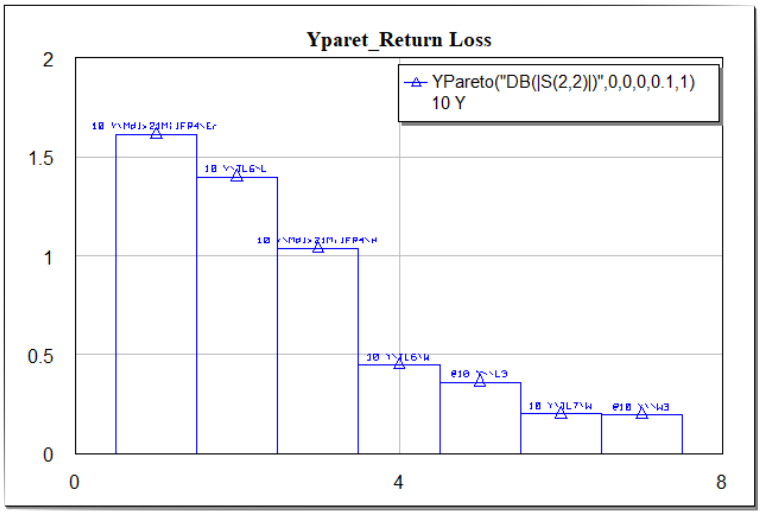


Figure 6.8: Results of the Pareto Measurement

From Figure 6.8, the rank of the top 7 parameters that influences the Return Loss from the biggest to the smallest are Mdlx21MilFR4\Er, TL6\L, Mdlx21MilFR4\H, TL6\W, L3, TL7\W and W3. Mdlx21MilFR4\Er and

Mdlx21MilFR4\H are the **relative dielectric constant** and **thickness** of the substrates. And the TL6\L, TL6\W, L3, TL7\W and W3 are the width or length of the microstrip line. As the designers of the LNA, we cannot control the Er and H of the substrates even they are the critical factor to the Return Loss showing in the yield analysis. However, we can optimize the yield by change the width W and length L of the microstrip line.

We perform the yield optimization on TL6\L, TL6\W, L3 and TL7\W and W3. In the same variable box window, we tick the option of "yield optimize" of the TL6\L and TL6\W, L3, TL7\W in the same dialog with Figure 6.1. And in the same yield analysis control dialog, select **Yield Optimization** in the pull-down list of Yield Methods in the same dialog as Figure 6.3. Besides, by observing Figure 6.6, it is easy to find out that if the whole trances move slightly to the right, the yield will rise. This can be achieved by adjusting the TL12\L, TL12\W, L4 and W4. Table 6.1 below shows the parameters and the corresponding value (we pick the approximate value when the digits are too long after optimization) obtained after the optimization. And Figure 6.9 shows the yield after the yield optimization. We can see from Figure 6.9 that the yield value has increased from 60.36% to 99.234%.

Table 6.1: Parameters and their Values after Yield Optimization

Parameter	**Value (mm)**
TL6\L	5.49794
TL6\W	0.99247
L3	5.02
TL7\W	1.016
W3	1.17827
TL12\L	1.17889
TL12\W	2.36608
L4	2.335
W4	1.1325

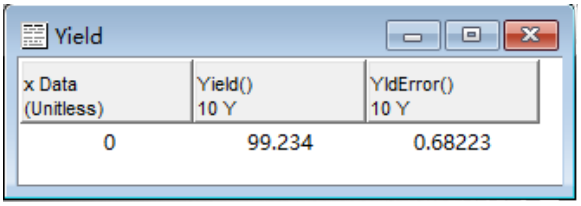


Figure 6.9: Yield after the Yield Optimization

The following Figure 6.10, Figure 6.11 and Figure 6.12 show plots of traces for Gain, Noise and the Return Loss respectively.

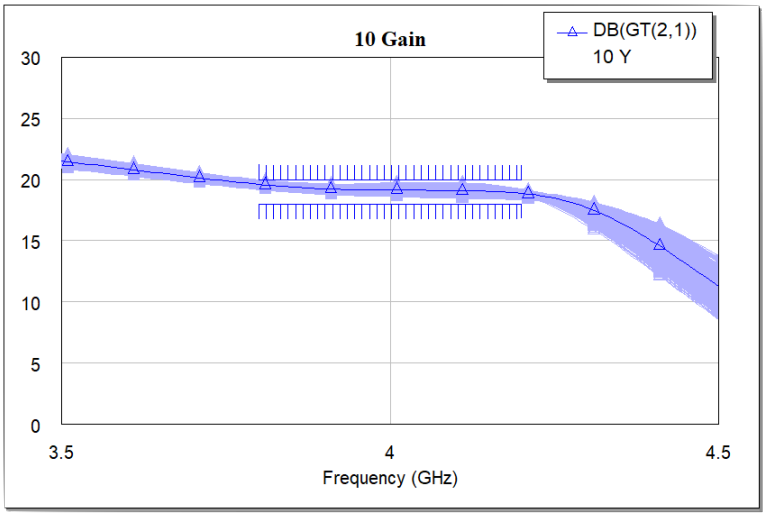


Figure 6.10: Yield Traces for Gain after Optimization

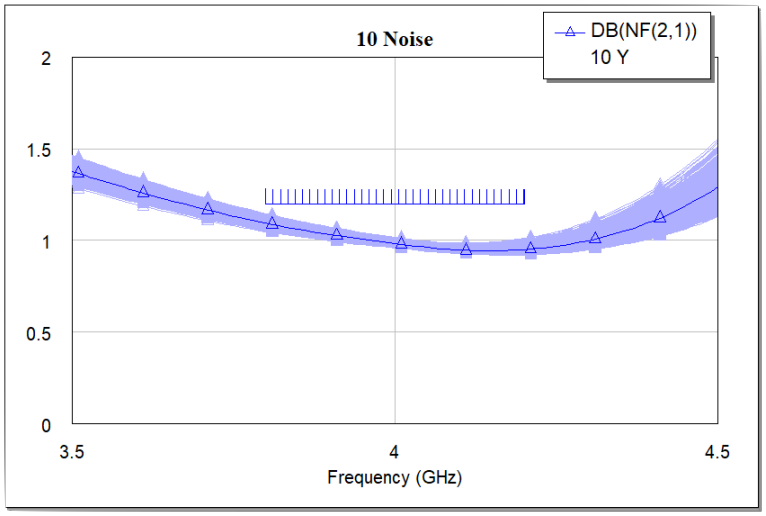


Figure 6.11: Yield Traces for Noise after Optimization

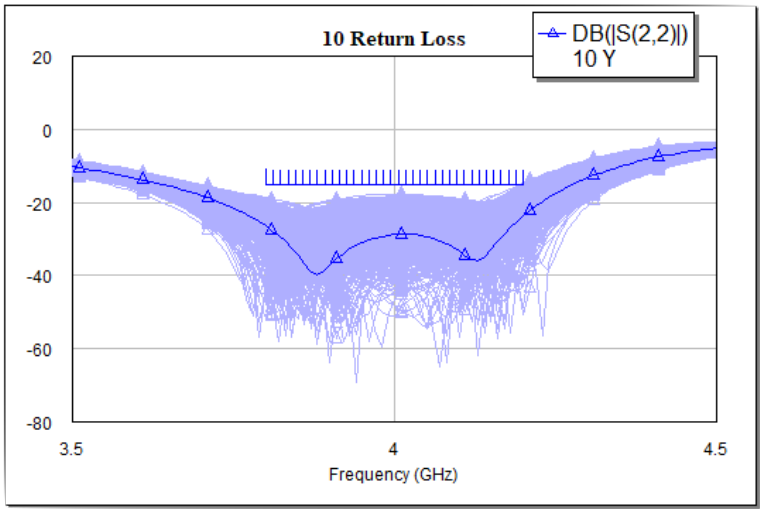


Figure 6.12: Yield Traces for Return Loss after Optimization

In this section, we have made the yield analysis to the LNA and centered the nominal values of the parameters to enhance the yield. However, the fact that we do not know the details for distribution and the tolerances of all the parameters may lead to the inaccuracy in the result. In practice, we should contact the manufacturers and get this information before starting the production process.

6.2 Conclusion of the Project

In this project, a two-stage Low Noise Amplifier (LNA) has been designed, analyzed and optimized.

Low-noise amplifiers work in microwave receiver systems and we develop it logically.

Firstly, a transistor, with code ATF-21186 at the operating point (Vds= 2 V, Id= 20 mA), is selected as an active device for the key amplification device among products from more than 20 famous manufacturer companies, also the substrate and the capacitor are determined from the manufacturer library embedded in AWR Microwave Office as components for LNA.

Secondly, the ideal bias circuit, the input matching network, the output network and the inter-stage network are designed in sequence and added to the transistor. We used the single-stub method for designing the input and output matching circuits. Here the ideal design used the ideal transmission lines.

Thirdly, the practical two-stage LNA is developed based on the ideal design after the tuning and optimization. We replaced the transmission line to the microstrip lines and expanded the project's frequency from the central frequency to the frequency band in the design goal. The physical dimensions of the components are clearly presented.

Fourthly, we created the layout objects for the transistor so that the circuit layout for fabrication is obtained with the help of the AWR Microwave Office Layout View.

In the end, we also made a yield analysis to the LNA and performed the yield optimization for the fabrication use the "Monte Carlo" method. The yield value has increased after the optimization.

The final two-stage low noise amplifier fully satisfies the design goal, that is, transducer gain between 18-20 dB, noise figure less than 1.2 dB, and return loss greater than 15 dB in the frequency band of 3.8-4.2 dB.

Appendix A

ATF-21186 Transistor Datasheet

HEWLETT® PACKARD

0.5–6 GHz General Purpose Gallium Arsenide FET

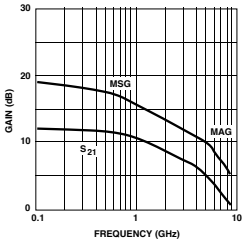
Technical Data

ATF-21186

Features

- **Low Noise Figure:** 0.5 dB Typ. @ 2 GHz
- **High Output Power:** 19 dBm Typ. P_{1dB} @ 2 GHz
- **High MSG:** 13.5 dB Typ. @ 2 GHz
- **Low Cost Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

Note:
1. Refer to "Tape-and-Reel Packaging for Surface Mount Semiconductors".

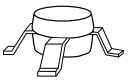


ATF-21186 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 15 mA.

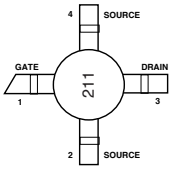
Description

Hewlett–Packard's ATF-21186 is a low cost Gallium Arsenide Schottky barrier-gate field effect transistor housed in a surface mount plastic package. This general purpose device is designed for use in low noise amplifiers, gain stages, driver amplifiers, and oscillators operating over the VHF, UHF, and microwave frequency ranges. High gain with two volt operation makes this part attractive for low voltage, battery operated systems. The low noise figure is appropriate for commercial systems demanding good sensitivity, such as GPS receiver front-ends and MMDS television receivers. The output power is sufficient for use as the driver stage in many hand-held transceivers operating in the 900 MHz through 2.4 GHz bands, including in cellular phones, PCN, and ISM band spread spectrum applications.

85 mil Plastic Surface Mount Package



Pin Configuration



This GaAs FET device has a nominal 0.3 micron gate length using airbridge interconnects between drain fingers. Total gate periphery is 750 microns. Proven gold based metallization systems and nitride passivation assure a rugged, reliable device.

ATF-21186 Absolute Maximum Ratings

Symbol	Parameter	Units	Absolute Maximum[1]
V_{DS}	Drain-Source Voltage	V	5
V_{GS}	Gate-Source Voltage	V	-4
V_{GD}	Gate-Drain Voltage	V	-6
I_{DS}	Drain Current	mA	I_{DSS}
P_T	Power Dissipation[2,3]	mW	400
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to +150

Notes:
1. Operation of this device above any one of these parameters may cause permanent damage.
2. T_{CASE} = 25°C (T_{CASE} is defined to be the temperature at the ends of pins 2 and 4 where they contact the circuit board).
3. Derate at 4.4 mW/°C for T_C > 60 °C.

Thermal Resistance[2]: θ_{jc} = 225°C/W

ATF-21186 Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
NF_o	Optimum Noise Figure V_{DS} = 2 V, I_{DS} = 15 mA	f = 1 GHz f = 2 GHz f = 4 GHz	dB		0.4 0.5 0.6	0.75
G_A	Associated Gain V_{DS} = 2 V, I_{DS} = 15 mA	f = 1 GHz f = 2 GHz f = 4 GHz	dB	12.0	14.2 12.6 9.1	
$P_{1\,dB}$	Power at 1 dB Gain Compression V_{DS} = 3 V, I_{DS} = 70 mA	f = 1 GHz f = 2 GHz f = 4 GHz	dBm		19.0 19.0 18.0	
$G_{1\,dB}$	1 dB Compressed Gain V_{DS} = 3 V, I_{DS} = 70 mA	f = 1 GHz f = 2 GHz f = 4 GHz	dB		18.0 14.0 8.5	
g_m	Transconductance	V_{DS} = 3 V, V_{GS} = 0 V	mS	70	120	
I_{DSS}	Saturated Drain Current	V_{DS} = 3 V, V_{GS} = 0 V	mA	80	120	200
V_P	Pinchoff Voltage	V_{DS} = 3 V, I_{DS} = 1 mA	V	-3.0	-1.5	-0.8

ATF-21186 Typical Performance, T_A = 25°C

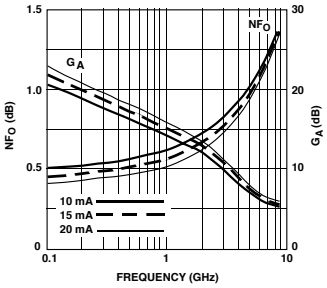


Figure 1. ATF-21186 Optimum Noise Figure and Associated Gain vs. Frequency and I_{DS}, V_{DS} = 2 V.

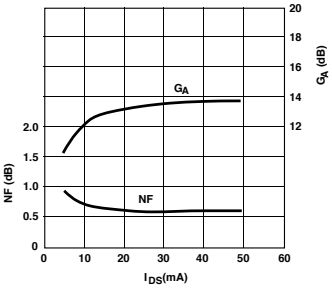


Figure 2. ATF-21186 Optimum Noise Figure and Associated Gain vs. I_{DS}, f = 2 GHz, V_{DS} = 2 V.

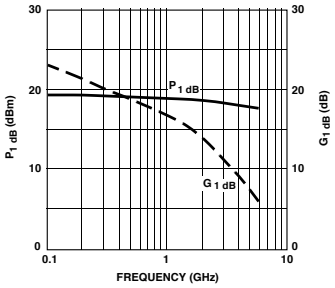


Figure 3. ATF-21186 Power Output at 1 dB Compression and 1 dB Compressed Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 70 mA.

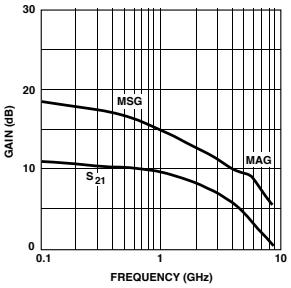


Figure 4. ATF-21186 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 10 mA.

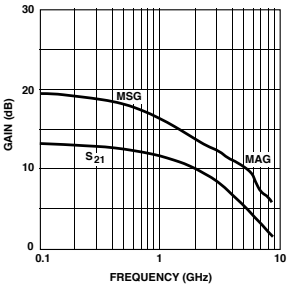


Figure 5. ATF-21186 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{DS} = 2 V, I_{DS} = 20 mA.

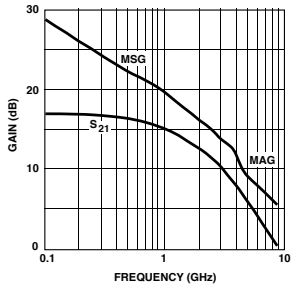


Figure 6. ATF-21186 Insertion Power Gain, Maximum Available Gain, and Maximum Stable Gain vs. Frequency. V_{DS} = 3 V, I_{DS} = 70 mA.

ATF-21186 Typical Scattering Parameters,

Common Source, $Z_o = 50\,\Omega$, $V_{DS} = 2\,V$, $I_{DS} = 10\,mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K	G_{max}[1]
(GHz)	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	—	(dB)
0.5	0.961	-25	11.12	3.599	157	-25.85	0.051	71	0.376	-25	0.22	18.5
1.0	0.910	-49	10.60	3.388	137	-20.36	0.096	57	0.360	-50	0.27	15.5
1.5	0.851	-73	9.96	3.149	118	-17.66	0.131	43	0.339	-73	0.33	13.8
2.0	0.794	-95	9.27	2.906	100	-16.03	0.158	31	0.314	-95	0.40	12.6
2.5	0.743	-118	8.53	2.671	83	-15.04	0.177	19	0.291	-118	0.47	11.8
3.0	0.694	-139	7.71	2.429	67	-14.52	0.188	9	0.272	-143	0.57	11.1
3.5	0.659	-160	6.85	2.201	52	-14.29	0.193	-1	0.270	-169	0.66	10.6
4.0	0.643	180	5.97	1.989	37	-14.29	0.193	-9	0.290	167	0.75	10.1
4.5	0.643	161	5.05	1.789	24	-14.38	0.191	-17	0.324	148	0.83	9.7
5.0	0.658	143	4.12	1.606	11	-14.66	0.185	-24	0.367	133	0.90	9.4
5.5	0.682	128	3.16	1.438	-1	-14.94	0.179	-29	0.410	121	0.95	9.0
6.0	0.707	115	2.19	1.286	-12	-15.29	0.172	-34	0.453	111	1.00	8.7
6.5	0.735	104	1.25	1.155	-23	-15.55	0.167	-38	0.490	102	1.02	7.5
7.0	0.758	95	0.32	1.038	-33	-15.81	0.162	-41	0.526	94	1.05	6.7
7.5	0.780	86	-0.59	0.934	-42	-15.97	0.159	-44	0.559	85	1.08	6.0
8.0	0.801	77	-1.49	0.842	-51	-16.08	0.157	-47	0.595	78	1.08	5.6

Note:

1. G_{max} = MAG for $K \geq 1$ and G_{max} = MSG for $K < 1$

ATF-21186 Typical Noise Parameters,

Common Source, $Z_o = 50\,\Omega$, $V_{DS} = 2\,V$, $I_D = 10\,mA$

Frequency	F_{min}	Γ_{opt}		$R_n/50$	G_a
GHz	dB	Mag.	Ang.	—	dB
0.5	0.37	0.95	11	1.738	13.8
1.0	0.41	0.89	25	0.819	12.3
1.5	0.45	0.84	42	0.553	11.4
2.0	0.49	0.79	60	0.387	11.1
2.5	0.53	0.74	79	0.265	10.4
3.0	0.57	0.71	100	0.179	10.0
3.5	0.61	0.68	120	0.111	9.2
4.0	0.65	0.66	142	0.057	8.7
4.5	0.69	0.64	162	0.028	7.9
5.0	0.73	0.65	-175	0.021	7.4
5.5	0.77	0.68	-155	0.042	7.1
6.0	0.81	0.73	-139	0.095	6.6
6.5	0.85	0.77	-123	0.202	6.4
7.0	0.89	0.81	-111	0.362	6.1
7.5	0.93	0.84	-98	0.596	5.8
8.0	0.97	0.86	-88	0.873	5.4

ATF-21186 Typical Scattering Parameters,

Common Source, $Z_o = 50\,\Omega$, $V_{DS} = 2\,V$, $I_{DS} = 15\,mA$

Freq.	S_{11}		S_{21}			S_{12}			S_{22}		K	G_{max}[1]
(GHz)	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.	—	(dB)
0.5	0.957	-27	12.56	4.248	156	-26.38	0.048	71	0.303	-28	0.22	19.5
1.0	0.898	-53	11.95	3.959	136	-21.11	0.088	57	0.291	-57	0.29	16.5
1.5	0.833	-77	11.19	3.627	116	-18.42	0.120	44	0.277	-82	0.37	14.8
2.0	0.772	-100	10.37	3.300	99	-16.89	0.143	32	0.261	-106	0.45	13.6
2.5	0.721	-123	9.52	2.992	82	-15.86	0.161	22	0.251	-132	0.53	12.7
3.0	0.675	-145	8.59	2.689	66	-15.34	0.171	12	0.247	-158	0.63	12.0
3.5	0.646	-165	7.65	2.413	51	-15.04	0.177	3	0.261	177	0.73	11.3
4.0	0.636	175	6.71	2.164	37	-14.90	0.180	-4	0.292	156	0.81	10.8
4.5	0.642	156	5.74	1.936	24	-14.90	0.180	-11	0.334	139	0.88	10.3
5.0	0.660	139	4.76	1.730	11	-14.99	0.178	-17	0.380	125	0.94	9.9
5.5	0.685	124	3.78	1.545	0	-15.09	0.176	-23	0.424	114	0.98	9.4
6.0	0.712	112	2.80	1.380	-11	-15.24	0.173	-27	0.466	106	1.01	8.5
6.5	0.739	102	1.86	1.239	-21	-15.39	0.170	-32	0.502	97	1.03	7.6
7.0	0.762	92	0.94	1.114	-31	-15.49	0.168	-36	0.537	89	1.04	6.9
7.5	0.783	84	0.04	1.005	-40	-15.55	0.167	-39	0.567	81	1.06	6.3
8.0	0.803	75	-0.84	0.908	-49	-15.60	0.166	-44	0.601	74	1.06	5.9

Note:

1. G_{max} = MAG for $K \geq 1$ and G_{max} = MSG for $K < 1$

ATF-21186 Typical Noise Parameters,

Common Source, $Z_o = 50\,\Omega$, $V_{DS} = 2\,V$, $I_D = 15\,mA$

Frequency	F_{min}	Γ_{opt}		$R_n/50$	G_a
GHz	dB	Mag.	Ang.	—	dB
0.5	0.35	0.950	13	1.633	15.8
1.0	0.39	0.870	27	0.639	14.2
1.5	0.43	0.810	45	0.420	13.4
2.0	0.46	0.760	63	0.302	12.6
2.5	0.50	0.710	82	0.209	11.7
3.0	0.54	0.670	102	0.138	10.8
3.5	0.57	0.635	121	0.088	9.8
4.0	0.61	0.614	143	0.047	9.1
4.5	0.64	0.605	165	0.025	8.5
5.0	0.68	0.612	-172	0.022	8.0
5.5	0.72	0.650	-152	0.042	7.6
6.0	0.75	0.696	-136	0.088	7.2
6.5	0.79	0.742	-121	0.174	7.0
7.0	0.83	0.782	-109	0.301	6.6
7.5	0.86	0.810	-96	0.471	6.3
8.0	0.90	0.840	-86	0.715	6.0

Appendix B

ATF-21186 Transistor Noise and S-Parameter Data

```
!ATF-21186
!S-PARAMETERS at Vds=2V  Id=20mA.   LAST UPDATED 01-30-98

# ghz s ma r 50

0.5   0.955 -29   4.698 156   0.046 71    0.251 -32
1.0   0.888 -55   4.340 134   0.084 57    0.246 -63
1.5   0.819 -80   3.938 115   0.114 44    0.240 -91
2.0   0.756 -104  3.547 97    0.136 33    0.233 -117
2.5   0.704 -127  3.186 80    0.152 23    0.233 -143
3.0   0.662 -149  2.840 65    0.163 14    0.242 -169
3.5   0.638 -170  2.532 50    0.170 6     0.266 168
4.0   0.633 171   2.257 37    0.174 -1    0.304 148
4.5   0.643 153   2.012 24    0.175 -7    0.349 133
5.0   0.663 136   1.793 12    0.176 -13   0.397 121
5.5   0.690 122   1.597 0     0.175 -19   0.441 111
6.0   0.717 110   1.425 -10   0.174 -24   0.482 103
6.5   0.744 100   1.280 -20   0.173 -28   0.517 95
7.0   0.767 91    1.151 -29   0.172 -33   0.550 87
7.5   0.788 83    1.040 -38   0.172 -37   0.579 79
8.0   0.807 74    0.940 -47   0.171 -41   0.611 72

0.5   0.33  0.95  13    1.543
1.0   0.37  0.88  28    0.659
1.5   0.41  0.82  46    0.423
2.0   0.45  0.77  64    0.294
2.5   0.48  0.70  83    0.191
3.0   0.52  0.65  103   0.124
3.5   0.56  0.62  123   0.079
4.0   0.59  0.60  146   0.042
4.5   0.63  0.59  168   0.024
5.0   0.67  0.60  -170  0.023
5.5   0.70  0.64  -150  0.044
6.0   0.74  0.68  -134  0.089
6.5   0.78  0.73  -118  0.176
7.0   0.81  0.77  -107  0.289
7.5   0.85  0.80  -96   0.446
8.0   0.89  0.83  -84   0.654
```

Appendix C

Microstrip Substrate Library

Modelithics

Microstrip Substrate Library

MSUB-LIB-001

Library Features

- Microstrip Substrate Components for Common Board Types
- Substrate Design Parameters:
  - Measurement-based Dielectric Constant
  - Metal Thickness
  - Loss Tangent

Substrate Library

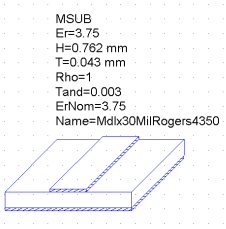
Library Description

The MSUB_LIB_001 is a microstrip substrate (MSUB) library containing drop-in MSUB components with nominal design parameters for microstrip substrate simulations. The provided dielectric constant (Er) values are based on measurements and are average values collected over time. Some board types are known to have greater Er variation in which case an Er range is provided. The default parameters are the typical values used by Modelithics Inc. in microstrip simulations. Dielectric loss tangent values come from manufacturer's data sheets. Typical values for top metal thickness used by Modelithics in simulations is 0.043 mm for soft boards and 0.005 mm for thin-film substrates.

Substrate List

Substrate	Height (mm)	Er	Tand	T (mm)
Alumina 99.6% 5-mil	0.127	9.6	0.0002	0.005
Alumina 99.6% 10-mil	0.254	9.6	0.0002	0.005
Alumina 99.6% 15-mil	0.381	9.6	0.0002	0.005
Elite Material EM-285	0.3556	4.4	0.01	0.043
FR-4 Standard 5-mil	0.127	4.3+/-0.4	0.015	0.043
FR-4 Standard 14-mil	0.3556	4.3+/-0.4	0.015	0.043
FR-4 Standard 21-mil	0.5334	4.3+/-0.4	0.015	0.043
FR-4 Standard 31-mil	0.7874	4.3+/-0.4	0.015	0.043
FR-4 Standard 59-mil	1.4986	4.3+/-0.4	0.015	0.043
Quartz 10-mil	0.254	3.8	0.00006	0.005
Rogers 4003C 8-mil	0.2032	3.90+/-0.15	0.003	0.043
Rogers 4003C 16-mil	0.406	3.80+/-0.05	0.002	0.043
Rogers 4003C 20-mil	0.508	3.75+/-0.05	0.002	0.043
Rogers 4003C 60-mil	1.524	3.65+/-0.03	0.002	0.043
Rogers 4350B 4-mil	0.1016	4.15+/-0.15	0.003	0.043
Rogers 4350B 10-mil	0.254	3.90+/-0.15	0.003	0.043
Rogers 4350B 16-mil	0.4064	3.80+/-0.05	0.003	0.043
Rogers 4350B 20-mil	0.508	3.75+/-0.10	0.003	0.043
Rogers 4350B 30-mil	0.762	3.75+/-0.05	0.003	0.043
Rogers 4350B 60-mil	1.524	3.65+/-0.03	0.003	0.043
Rogers 5880 10-mil	0.254	2.25	0.001	0.043
Rogers 5880 15-mil	0.381	2.25	0.001	0.043
Rogers 6010LM 25-mil	0.635	11.5	0.002	0.043
Rogers 3010 5-mil	0.127	11.5	0.002	0.043
Taconic RF-35 20-mil	0.508	3.7	0.002	0.043
Taconic RF-35 100-mil	2.54	3.5	0.002	0.043

Substrate Representation



Default units in mm

Appendix D

ATC 600S Capacitor Datasheet

ATC 600S Series
Ultra-Low ESR, High Q, NPO
RF & Microwave Capacitors

Features:
- **Lowest ESR in Class**
- Highest Working Voltage in class – 250V
- Standard EIA Size: 0603
- Laser Marking (Optional)
- RoHS Compliant
- High Self Resonance Frequencies

Applications:
- Cellular Base Stations
- Wireless Commuications
- Broadband Wireless Services
- Satellite Communications
- WiMAX (802.16)

Circuit Applications:
- Filter Networks
- High Q Frequency Sources
- Matching Networks
- Tuning, Coupling, Bypass and DC Blocking

ATC 600 SERIES OVERVIEW

ATC Series	ATC Case Size	EIA Case Size
600	L	0402
600	**S**	**0603**
600	F	0805

Electrical Specifications

Capacitance:	0.1 to 100 pF
Tolerances:	See Cap Value Chart
Working Voltage (WVDC):	250 V
Quality Factor (Q):	> 2000 @ 1 MHz
Operating Temperature Range:	-55°C to +125°C (no derating of working voltage)
Temperature coefficient of Capacitance (TCC):	0 ± 30 ppm/°C, -55°C to +125°
Insulation Resistance:	10^5 MΩ min. at +25°C at rated WVDC 10^4 MΩ min. at +125°C at rated WVDC
Dielectric Withstanding Voltage (DWV):	2.5 x WVDC for 5 seconds
Aging:	None
Piezo Effects:	None

Mechanical Specifications

Terminations:	T = Tin Plated over Nickel Barrier* (Standard) TN = Tin Plated over Non-Magnetic Barrier* W = Tin/Lead Solder Plated over Nickel Barrier
Solderability:	Solder coverage > 90% of end termination
Terminal Strength:	4 lbs. Typ., 2 lbs. min.

Environmental Specifications

Life Test:	2000 hours, +125°C at 2X WVDC
Thermal Shock:	5 cycles, -55°C to +125°C
Moisture Resistance:	240 hours, 85% Relative Humidity at +85°C

Military Approval

DSCC Drawing Number 05002

* RoHS Compliant

ATC 600 Series Capacitors are designed and manufactured to meet and exceed the requirements of EIA-198, MIL-PRF-55681 and MIL-PRF-123.

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www.atceramics.com

ATC 001-924; Rev. R, 12/09

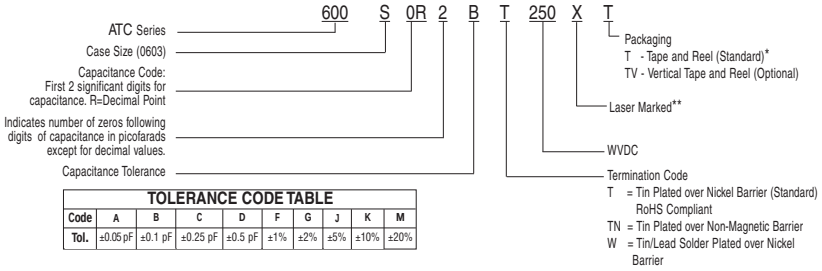
ATC 600S Series Ultra-Low ESR, High Q NPO RF & Microwave Capacitors

Capacitance Values

Value (pF)	Cap Code	Marking	Tolerances
0.1	0R1	A9	A, B
0.2	0R2	H9	A, B
0.3	0R3	M9	A, B, C
0.4	0R4	d9	A, B, C
0.5	0R5	f9	A, B, C
0.6	0R6	m9	A, B, C
0.7	0R7	n9	A, B, C
0.8	0R8	t9	A, B, C
0.9	0R9	y9	A, B, C
1.0	1R0	A0	A, B, C, D
1.1	1R1	B0	A, B, C, D
1.2	1R2	C0	A, B, C, D
1.3	1R3	D0	A, B, C, D
1.5	1R5	E0	A, B, C, D
1.6	1R6	F0	A, B, C, D
1.8	1R8	G0	A, B, C, D
2.0	2R0	H0	A, B, C, D
2.2	2R2	J0	A, B, C, D
2.4	2R4	K0	A, B, C, D
2.7	2R7	L0	A, B, C, D
3.0	3R0	M0	A, B, C, D
3.3	3R3	N0	A, B, C, D
3.6	3R6	P0	A, B, C, D
3.9	3R9	Q0	A, B, C, D
4.3	4R3	R0	A, B, C, D
4.7	4R7	S0	A, B, C, D
5.1	5R1	T0	A, B, C, D
5.6	5R6	U0	A, B, C, D
6.2	6R2	V0	A, B, C, D
6.8	6R8	W0	B, C, J, K
7.5	7R5	X0	B, C, J, K
8.2	8R2	Y0	B, C, J, K
9.1	9R1	Z0	B, C, J, K
10	100	A1	F, G, J, K, M
11	110	B1	F, G, J, K, M
12	120	C1	F, G, J, K, M
15	150	E1	F, G, J, K, M
18	180	G1	F, G, J, K, M
20	200	H1	F, G, J, K, M
22	220	J1	F, G, J, K, M
24	240	K1	F, G, J, K, M
27	270	L1	F, G, J, K, M
30	300	M1	F, G, J, K, M
33	330	N1	F, G, J, K, M
36	360	P1	F, G, J, K, M
39	390	Q1	F, G, J, K, M
43	430	R1	F, G, J, K, M
47	470	S1	F, G, J, K, M
51	510	T1	F, G, J, K, M
56	560	U1	F, G, J, K, M
62	620	V1	F, G, J, K, M
68	680	W1	F, G, J, K, M
75	750	X1	F, G, J, K, M
82	820	Y1	F, G, J, K, M
91	910	Z1	F, G, J, K, M
100	101	A2	F, G, J, K, M

*Non-standard values and custom tolerances are available upon request.

ATC Part Number Code



TOLERANCE CODE TABLE									
Code	A	B	C	D	F	G	J	K	M
Tol.	±0.05 pF	±0.1 pF	±0.25 pF	±0.5 pF	±1%	±2%	±5%	±10%	±20%

*4,000 pieces on 7" reel and 500 pieces on prototype reel. Consult ATC for other options.

The above part number refers to a 600S Series (case size S) 0.2 pF capacitor, B tolerance (±0.1pF), 250 WVDC, with T termination (Tin Plated over Nickel Barrier, RoHS Compliant), Laser Marking and Tape and Reel packaging.

**Marking is optional.

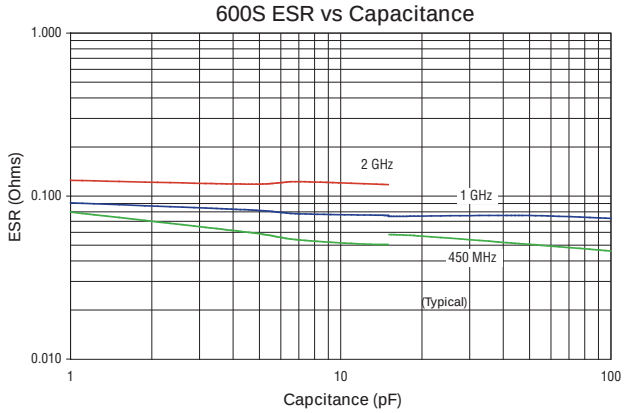
ATC accepts orders for our parts using designations ***with*** or ***without*** the "ATC" prefix. Both methods of defining the part number are equivalent, i.e., part numbers referenced with the "ATC" prefix are interchangeable to parts referenced without the "ATC" prefix. Customers are free to use either in specifying or procuring parts from American Technical Ceramics.

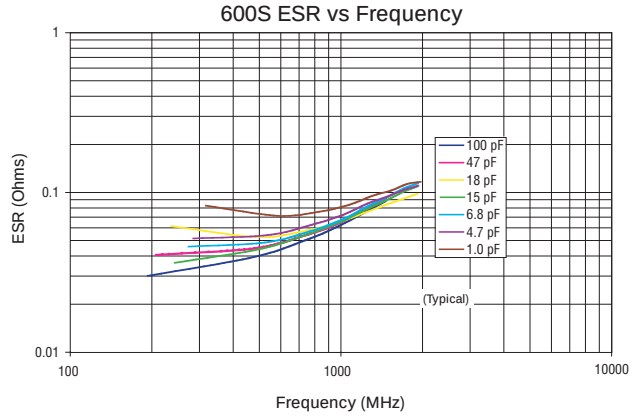
For additional information and catalogs contact your ATC representative or call direct at (631) 622-4700.

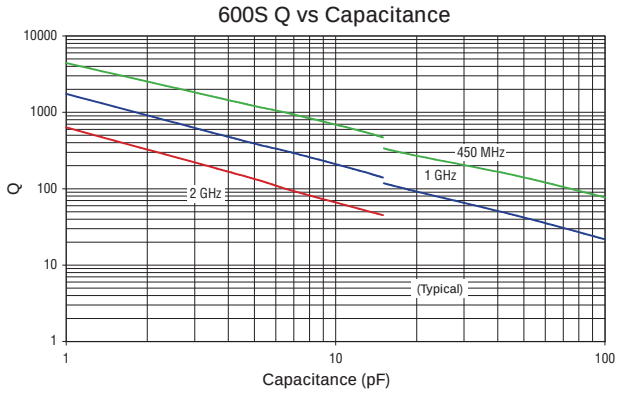
*Consult factory for 500 piece reels for prototyping.

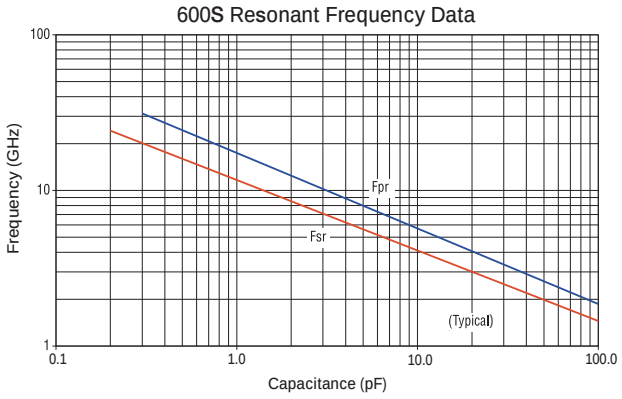
Consult factory for additional performance data.

Typical Performance Data





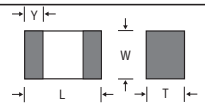




ATC 600 Series Data Sheet Test Condition Description

Capacitors horizontally mounted on 13.3-mil thick Rogers RO4350® softboard, 29-mil wide, 1/2 oz. Cu traces.
FSR = lowest frequency at which S11 response, referenced at capacitor edge, crosses real axis on Smith Chart.
FPR = lowest frequency at which there is a notch in S21 magnitude response.

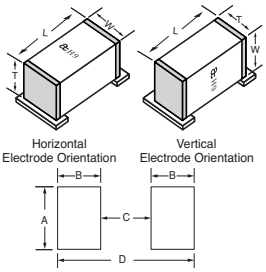
Outline Dimensions



S (0603)	L: .063 ± .006 (1.60 ± .15) W: .032 ± .006 (.81 ± .15)	T: .035 max. (0.89 max.) Y: .014 ± .006 (0.36 ± 0.15)

Inches (mm)

Suggested Mounting Pad Dimensions



Case Sizes L, S and F

Case Size	A Min.	B Min.	C Min.	D Min.
0402 (1005)	.0275 (0.70)	.0354 (0.90)	.0157 (0.40)	.0866 (2.20)
0603 (1608)	.0393 (1.00)	.0433 (1.10)	.0236 (0.60)	.110 (2.80)
0805 (2012)	.0590 (1.50)	.0512 (1.30)	.0236 (0.60)	.1259 (3.20)

Inches (mm)

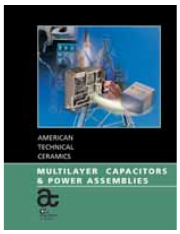
Design Kits

Each Kit contains a selection of standard capacitor values for circuit prototyping.

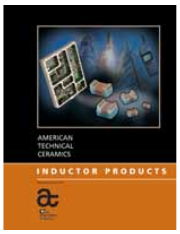
Kit #	Item #	Description	Cap. Value Range (pF)	Cap. Values (pF)	Tol. (pF)	Price
Kit 25T	DK0025T RoHS Compliant	600S Series Ultra-low ESR, High Q Microwave Capacitors 16 different values, 15 pcs. min. per value	0.1 to 2.0	0.1, 0.2, 0.3, 0.4, 0.5, 0.6 0.7, 0.8, 0.9, 1.0, 1.1, 1.2, 1.5	±0.1	$90.00
				1.6, 1.8, 2.0	±0.25	
Kit 26T	DK0026T RoHS Compliant	600S Series Ultra-low ESR, High Q Microwave Capacitors 16 different values, 15 pcs. min. per value	1.0 to 10	1.0, 1.2, 1.5, 1.8, 2.0, 2.2, 2.4, 2.7, 3.0, 3.3	±0.1	$90.00
				3.9, 4.7, 5.6, 6.8, 8.2	±0.25	
				10	±5%	
Kit 27T	DK0027T RoHS Compliant	600S Series Ultra-low ESR, High Q Microwave Capacitors 16 different values, 15 pcs. min. per value	10 to 100	10, 12, 15, 18, 20, 22, 24, 27, 30, 33, 39, 47, 56, 68, 82, 100	±5%	$90.00

For Online Kit Orders, Catalog & Application Notes, **Visit: www.atceramics.com**

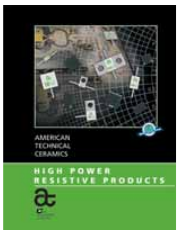
Other ATC Product Catalogs



Multilayer Capacitors
& Power Assemblies



Inductor
Products



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Appendix E

Detailed Procedures for Creating the Transistor Cell

1. Import the **Layer Process File**
   A Layer Process File (LPF) defines the default settings for the Layout View, including drawing layers, layer mappings, 3D views, and EM layer mappings. Here we use the MIC_english.lpf as the LPF for transistor.
   To import it, we can:

   1 Click the **Layer** Tab and display the **Layout Manager**.

   2 Right-click **Layer Setup** in the Layout Manager and choose Import Process Definition. An Import Process Definition dialog box pops up.

   3 Locate the program directory of the LPF file (The default installation directory is: *C:\Program Files\AWR\AWRDE\14 or C:\Program Files(x86)\AWR\AWRDE\14*) and double-click to open it. If the default installation directory has been changed, then locate that directory instead when the program directory is referenced.

   4 Select the MIC-english.lpf file and click **Open**.

2. Edit **Database Unit** and default **Grid Size**
   A database unit is defined as the smallest unit of precision for a layout. This parameter mustn't be changed after it is set. Changing **database units** can cause rounding errors that may lead to problems in the layout file. The **grid size** is important because many IC designs must reside on a grid. The grid must be greater than or equal to the database

unit. Because the grid multiplier's smallest unit is ".1x", we should set the grid to 10 times the database unit to prevent having a smaller grid than the database unit. To set the database unit and grid size, we can:

1 Choose **Options** > **Layout Options**. The Layout Options dialog box displays.

2 On the **Layout** tab, type "**0.001**" in **Grid spacing** and "1e-05" in **Database unit size**.

3 In **Snap together** dropdown list, select **Manual snap on parameter changes**.

4 Tick the **Allow pcell's origin to float**.

We select these parameters considering the layout size of the whole project, especially to make sure that they are in consistence with the layout of the capacitor. What's more, Artwork cells that draw faces that are odd multiples of the database unit size can have problems snapping together since the center of the face is off-grid. The function of the **allow pcell's to float** is to avoid this problem. Figure E.1 shows the settings for the **Layout Options** window.

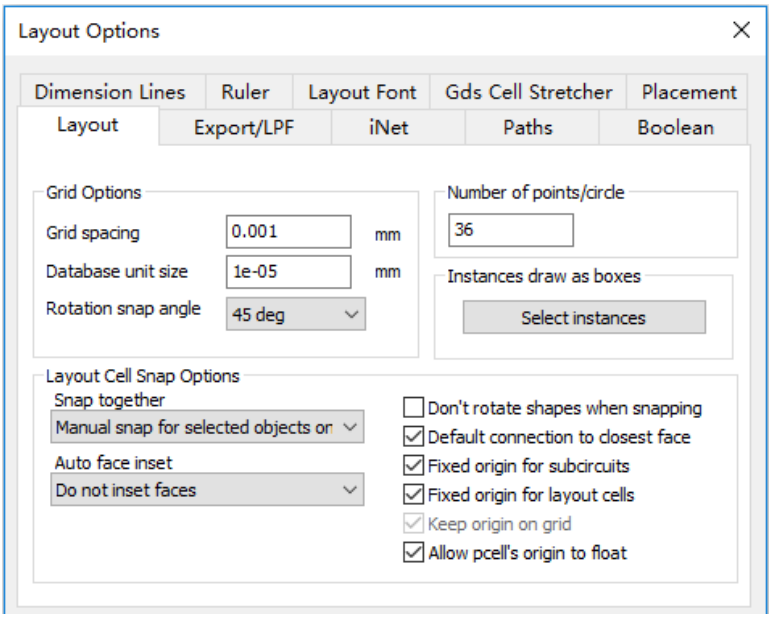

Figure E.1: Layout Options Window

3. Create the Artwork Cell
   To create the artwork cell for the transistor, we can:

- Click the **Layout** tab to open the Layout Manager.
- Right-click **packages** under **Cell Libraries** and choose **New Layout Cell**. The "**Create New Layout Cell**" dialog box displays.
- Name the cell "**ATF21186 Package**" and click **OK**. A drawing window displays in the workspace.
- Click "**ATF21186 Package**" under packages in the upper Layout Manager window, and then click the Package box in the **Actv** column of the Drawing Layer pane to enable Package as the active layer, as shown in the following figure. Figure E.2 shows the selection of Package Box.

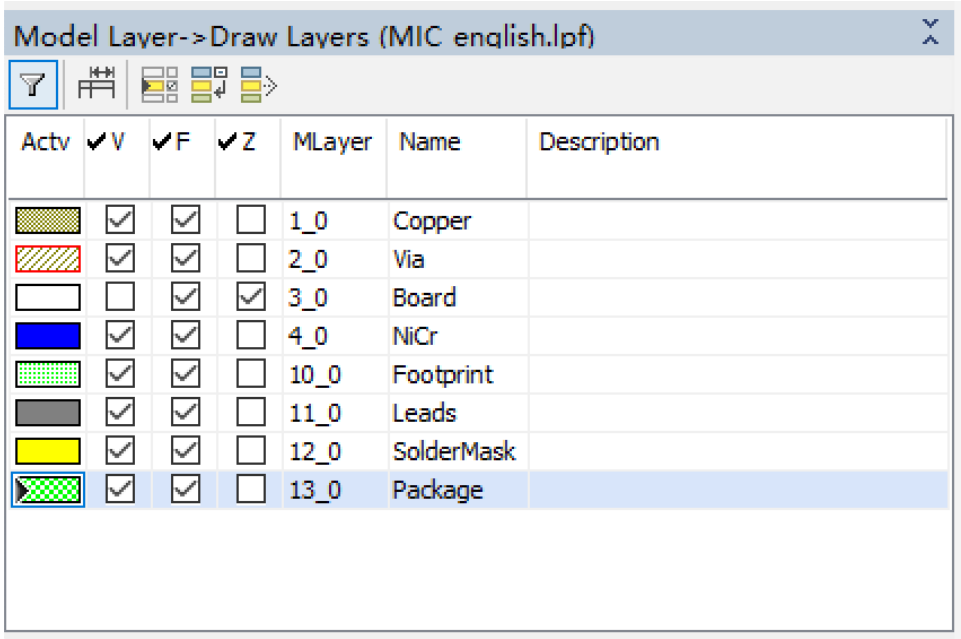

Figure E.2: Selection of Package Box

- Choose **Draw** > **Circle** tool to draw the central circle of the package of the transistor. The size can be measured by the **Measure** tool. By choosing **View** > **Zoom In** or View > **Zoom Out**, the view can be adjusted better.
- Click the Leads box in the left column of the lower pane of the Layout Manager to enable Leads as the active layer. And select tools from the Draw window and draw the four leads of the transistor package. Figure E.3 shows the selection of Leads Box.

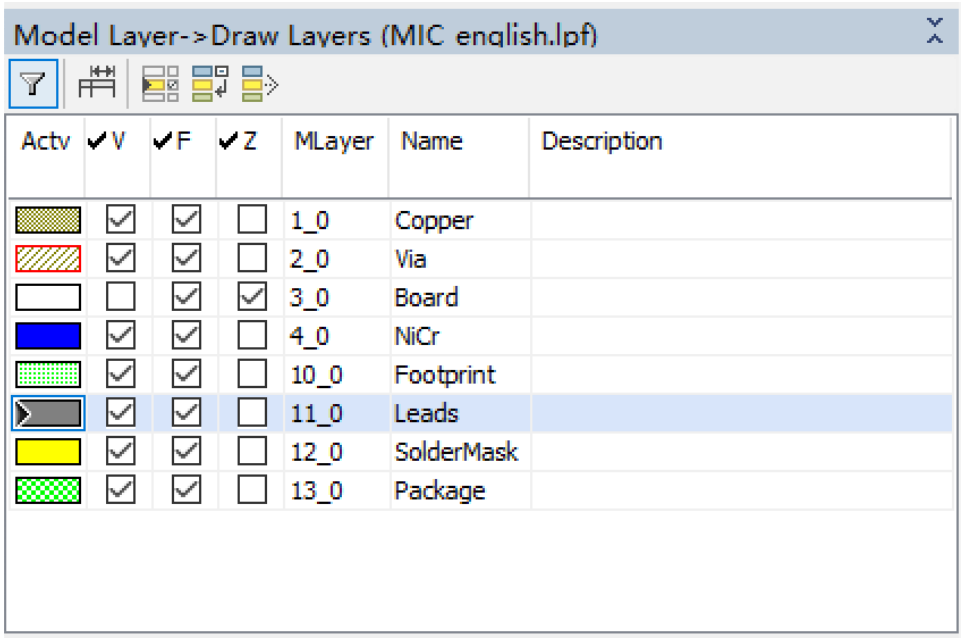

Figure E.3: Selection of Leads Box

4. Add Ports to an Artwork Cell
   Ports in the Artwork Cell Editor define the faces to which other layout cells connect. The orientation of the port arrow determines the direction of connection to the adjacent layout cell. To add ports on the artwork cell we created, we can:

   - Choose **Draw** > **Cell Port**.
   - Move the cursor into the "**ATF21186 Package**" window. To create gravity points for positioning and aligning shapes in the layout, press and hold the **Ctrl** key while moving the cursor over the leads, until a diamond symbol displays. Do not release the **Ctrl** key.
   - With the **Ctrl** key still pressed, click and hold down the mouse button while moving directly the cursor to top vertex. Release the mouse button and the Ctrl key.
   - To successfully run the Connectivity Checker, the port properties of the artwork cell must be set correctly. Select cell port 1, then right-click and open **Shape Properties**. In the Properties dialog box, click the **Layout** tab. In **Model Layers** dropdown list, select **11_0->Leads**, then click **OK**. Figure E.4 shows the layer setting for the port.

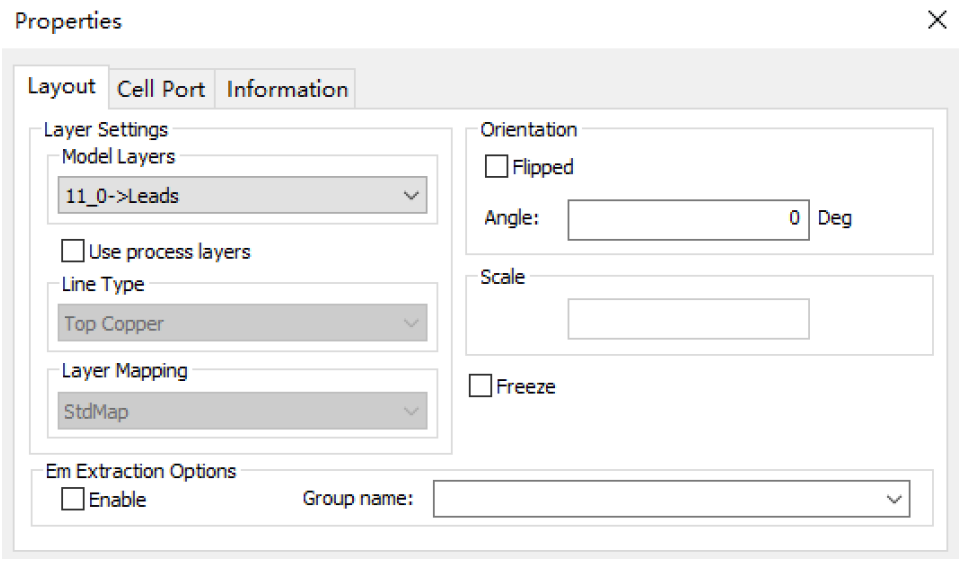

Figure E.4: Layer Setting for Port

   - Repeat these steps to place a port on the opposite side of the

drawing, starting at the top vertex and drawing down.

- Click the **X** at the top right of the "**ATF21186 Package**" window and click **Yes** to save the cell edits. Figure E.5 illustrates the completed artwork cell of the transistor.

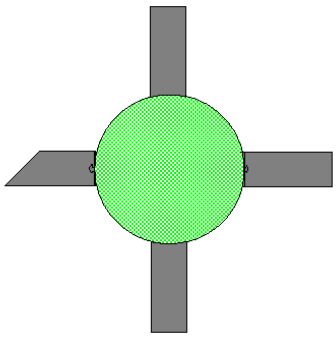

Figure E.5: Artwork Cell of the Transistor

5. Assigning the Artwork Cell to the transistor
   Finally, to assign the artwork cell to the transistor in the schematic, we can:

   - In the schematic as Figure 4.6, right-click the SUBCK1 element (the transistor), choose "**Properties**" in the pop-up window.
   - Select the **Layout** tab on top of the window.
   - Click "**ATF21186**" in **Library Name**, then select "**ATF21186 Package**" from the list of cells, then click **OK**. The example of setting is illustrated in Figure E.6.

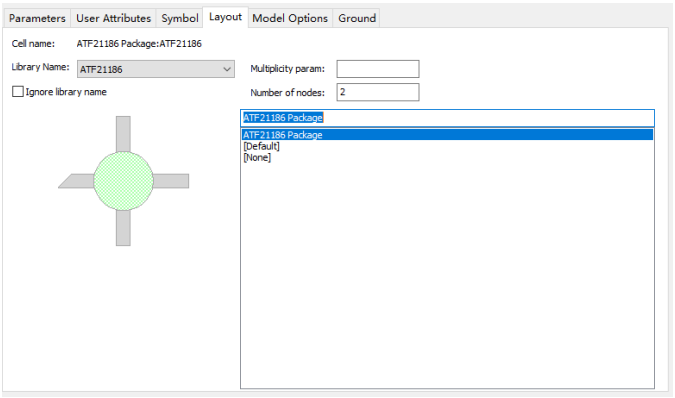

Figure E.6: Layout Tab Settings Example

Bibliography

[1] Yuichi Ichikawa and Masaru Aoki. "High-frequency circuit design in the GHz era". In: *pp58* 59 (2003), pp. 44–45.

[2] Akhil Chandra, Maganti and Enishetty, Rahul. "Design of a Low Noise Amplifier using AWR Microwave Office." In: July 2013.

[3] Ludwig, Reinhold. *RF Circuit Design: Theory & Applications, 2/e*. Pearson Education India, 2000.

[4] Giuseppe Macchiarella. *Amplifier design II Slides of the Course RF Systems*. [Acccessed August 5, 2019]. 2019. URL: http://home.deib.polimi.it/macchiar/RF_Systems_New/Ampli_design_II.pdf.

[5] Giuseppe Macchiarella. *Amplifier design II Slides of the Course RF Systems*. [Retrieved August 5, 2019]. 2019. URL: http://home.deib.polimi.it/macchiar/RF_Systems_New/Ampli_design_I.pdf.

[6] *NI AWR Design Environment Suite. (n.d.)* [Retrieved September 1, 2019]. 2019. URL: https://awrcorp.com/download/faq/english/docs/Getting_Started/gs_desenv.html.

[7] *Files and Utilities. (n.d.)* [Retrieved September 1, 2019]. 2019. URL: http://home.deib.polimi.it/macchiar/indice_file/Page590.html.

[8] Guillermo Gonzalez. *Microwave transistor amplifiers: analysis and design*. Vol. 2. Prentice hall New Jersey, 1997.

[9] *Simulation Basics. (n.d.)* [Retrieved September 1, 2019]. 2019. URL: https://awrcorp.com/download/faq/english/docs/Simulation/sa_basics.html#optimization.

[10] *Layout Overview. (n.d.)* [Retrieved September 6, 2019]. 2019. URL: https://awrcorp.com/download/faq/english/docs/Layout/i481570.html#d0e502.