POLITECNICO DI MILANO

School of Industrial and Information Engineering

Master of Science in Electronics Engineering

Experimental Characterization of an SDD-based Monolithic Multichannel Detection Module for the TRISTAN Project

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Sommario

La ricerca sulla materia oscura è, ai giorni nostri, tutt'ora in corso, al fine di comprenderne i misteri. Essa è un'ipotetica parte della materia che si pensa componga l'85% della massa totale dell'universo. È chiamata oscura perché non interagisce con nessuna radiazione elettromagnetica osservabile, rendendone la sua identificazione particolarmente complessa. La sua presenza potrebbe spiegare alcune osservazioni astrofisiche, quali gli effetti gravitazionali non spiegabili se non con l'esistenza di più materia rispetto a quella visibile. La particella candidata alla composizione della materia oscura occorre che sia, per ovvie ragioni, una particella nuova, e compresa tra quelle massive debolmente interagenti.

La scelta di tale particella potrebbe ricadere sul neutrino attivo, una particella subatomica presente nel modello standard, considerato promettente per via della sua interazione unicamente con la forza nucleare debole e con la gravità. Per supportare tale tesi, è nato l'esperimento KATRIN (KArlsruhe TRItium Neutrino). Il suo scopo è misurare la massa del neutrino attivo dall'osservazione della regione di endpoint dello spettro di decadimento β del trizio. Sulla base dei risultati ottenuti, si è rilevato come i neutrini attivi compongano solo una parte della materia oscura, a causa della loro massa particolarmente esile, rendendo perciò necessaria la ricerca di una nuova particella.

Il neutrino sterile è un altro tipo di neutrino che è stato ipotizzato come tassello mancante del puzzle, per il quale nasce il progetto TRISTAN (TRitium Investigation on STerile to Active Neutrino mixing). Diversamente dall'esperimento KATRIN, che misura solo la regione di endpoint del decadimento β del trizio, TRISTAN osserva lo spettro nella sua interezza, cercando un segno visibile della presenza del neutrino sterile. Anche se essenzialmente diversi, i due esperimenti utilizzano lo stesso tipo di apparato sperimentale, avendo come differenza maggiore il vero e proprio rivelatore. In KATRIN abbiamo un array monolitico di diodi PIN composto da 148 pixels, con una risoluzione di energia di circa 1.4 keV FWHM a 5.9 keV, invece TRISTAN punta ad ottenere un rivelatore basato su SDD di 3486 pixels suddivisi in 21 moduli.

Ciascun modulo contiene una matrice monolitica di 166 SDD con una risoluzione FWHM migliore di 200 eV a 6 keV.

Questa tesi segue lo sviluppo del rivelatore per TRISTAN, in particolare: il design di moduli di rivelazione in preparazione al 166 canali finale, la caratterizzazione dei sistemi di misura tramite un setup di rivelazione del rumore e la caratterizzazione sperimentale di due detector reali, il 12 pixels e il 47 pixels, utilizzando una sorgente radioattiva di ^{55}Fe. Tale caratterizzazione è stata effettuata perché il design del detector finale a 166 pixels necessita di una costruzione passo dopo passo, partendo dal pixel singolo e aumentando gradualmente il numero di pixel tra una fase del progetto e la successiva. In questo modo, tutti i possibili errori derivanti dalla produzione dei rivelatori o delle schede di rivelazione elettronica possono essere studiati e corretti in maniera efficace.

Per meglio delineare la ricerca svolta, la tesi è strutturata come segue:

- *Capitolo I*: introducendo il concetto di materia oscura, il capitolo I presenta gli esperimenti KATRIN e TRISTAN. Essendo TRISTAN l'esperimento cardine di questa tesi, viene presentata anche la sua catena di acquisizione.

- *Capitolo II*: con il capitolo II si prosegue con la presentazione del rivelatore principale di TRISTAN con le sue caratteristiche di funzionamento e le motivazioni per la sua scelta nell'esperimento. Dopodichè, si procede all'introduzione di ETTORE, un ASIC a 12 canali che esegue una prima amplificazione e un primo filtraggio dei segnali provenienti dal rivelatore. Infine, si presentano le funzionalità di SFERA, un ASIC low noise, per lo shaping analogico dei segnali provenienti dal preamplificatore di carica, completamente programmabile. SFERA, seppur non utilizzato nell'esperimento, viene presentato in quanto rappresenta un ottimo candidato come metodo di acquisizione nelle fasi iniziali di caratterizzazione del nuovo rivelatore.

- *Capitolo III*: con il capitolo III si espone la caratterizzazione sperimentale di due setup, il 12 pixels e il 47 pixels. Inizialmente, vi è un'introduzione alle schede dei due setup e alle loro funzionalità. Successivamente, vengono mostrate le misure reali, con tutti i loro passaggi.

- *Capitolo IV*: in questo capitolo si presenta il setup di test del rumore del JFET integrato nel rivelatore. Dopo aver descritto il funzionamento desiderato, viene effettuato uno studio sulle altre sorgenti di rumore. Successivamente, vengono selezionati i componenti discreti e i punti di polarizzazione necessari per un corretto funzionamento del sistema. Infine, vi sono le misure effettuate con il setup connesso ad un rivelatore e le conclusioni ad esse connesse.
- *Capitolo V*: all'interno del capitolo V si ritrova la descrizione della board di test per il setup a 47 pixels. Successivamente vengono mostrati gli schematici e i componenti utilizzati. In conclusione viene posta la descrizione della board funzionante, con allegate le immagini delle misure effettuate.
- *Capitolo VI*: conclusioni e presentazione dei successivi sviluppi e delle attività programmate nel progetto TRISTAN.

Abstract

Even to these days, the research on the dark matter is ongoing, trying to uncover the mysteries of it. Dark matter is a hypothetical form of matter that is thought to account for about 85% of the total mass in the universe. It is called dark because it does not interact with observable electromagnetic radiation, hence its detection is extremely difficult. Its presence can explain some astrophysical observations, like gravitational effects that cannot be explained unless more matter than what can be seen is present. The candidate particle for the dark matter composition must be, for obvious motivations, some new kind and it must be included in the weakly interacting massive particles.

The chosen particle can be the active neutrino, a subatomic particle in the standard model, considered as a promising candidate since it interacts only with the weak nuclear force and gravity. To support this hypothesis, the KATRIN (KArlsruhe TRItium Neutrino) was born. Its aim is to measure the mass of the active neutrino from the measurement of the endpoint region of the tritium β-decay spectrum. Looking at the results, the active neutrinos can only account for a small fraction of dark matter due to their tiny mass. A new particle must be found.

The sterile neutrino is another type of neutrino that has been hypothesized as the missing part of the puzzle, and to find it the TRISTAN (TRitium Investigation on STerile to Active Neutrino mixing) project was born. In contrast to the KATRIN experiment, that measures only the endpoint region of the tritium β-decay, TRISTAN aims at observing the full spectrum of it, searching for the signature of the sterile neutrino. While basically different, the two experiments share almost the same setup, with the major difference in the detection system. In KATRIN we have a monolithic PIN diode array of 148 pixels, with energy resolution of about 1.4 keV FWHM at 5.9 keV, instead TRISTAN aims at having a matrix of 3486 SDD pixels arranged into 21 modules. Each of these modules contains a 166-SDD array with a resolution of $<$200 eV FWHM at 6 keV.

This thesis follow the development of the detector for TRISTAN, in particular:

the design of the detection module in preparation for the final 166-SDD array, the characterization of the detection module through a noise setup and the experimental characterization of the 12-pixel SDD and 47-pixel SDD, using a ^{55}Fe source. This characterization is done because the design of the final 166-pixel detector is being done step by step, starting from a single pixel and increasing gradually the number of pixels depending on the phase of the project. In this way all the possible errors that could arise from the production of the detectors or the readout boards have been studied and fixed in an effective way.

To outline better the research that has been carried out, the thesis is organized as follows:

- *Chapter I*: introducing the concept of dark matter, chapter I presents the KATRIN and TRISTAN experiments. Being TRISTAN the one in which this thesis is focused, we have even a brief presentation of its readout chain.

- *Chapter II*: chapter II continues with the presentation of the main detector of TRISTAN with its functionalities and the reasons for its choice in the experiment. After that we have an overview of ETTORE, a 12-channel ASIC that performs the first amplification and filtering of the signals coming from the detector. Finally, there is the presentation of the functionalities of SFERA, a low-noise fully programmable readout ASIC, for the analog shaping of the signals coming from the charge preamplifier. SFERA is not currently used in the experiment, however it is presented as a good solution for the analog readout during the testing phase of the detectors.

- *Chapter III*: the chapter III shows the experimental characterization of two setups, the 12 channels and the 47 channels. Firstly, all the boards of the two setups are introduced, with an explanation of their features. Then the real measurements, with all the passages that lead to them, are shown.

- *Chapter IV*: a presentation of the noise test setup, for the JFET integrated in SDD pixels, begins this chapter. After describing the desired operation, a study is carried out on the other possible noise sources. Subsequently, the physical components and the bias points, necessary for a correct functioning

of the system, are selected. At the end there are the measurements made with the setup created and the conclusions connected to them.

- *Chapter V*: the description of the test board for the 47-channel ASIC board is present. Subsequently the schematics and the real components used are shown. The chapter closes with a working board, with screenshots and images of the measurements taken.
- *Chapter VI*: this is the conclusion chapter, introducing the future developments on the project and activities related to the TRISTAN project.

1 | The TRISTAN Project

In this chapter we have a description of the role of the neutrino regarding the study of the dark matter and consequently the reasons for the research of its mass. After that there is an exposition of the experiments KATRIN and TRISTAN, international experiments that aim at determining the mass for what regards the active neutrino and of the existence of the so called sterile one. This thesis is focused in particular on the TRISTAN project, presenting the design choices for what regards the detector and the readout chain.

1.1 The Dark Matter and The Neutrino

The main aims of modern observational cosmology are to test whether the cosmological model is correct, to search for discrepancies, and to obtain higher precision measurements of the parameters of this model, so that theories of how the Universe came to have this composition may be tested. Dark matter is a hypothetical form of matter that does not emit electromagnetic radiation and only occurs through gravitational effects. It is therefore not directly observable, and has been theorized to account for discrepancies between experimental observations and the current laws of physics. Thanks to the analysis of the Planck mission's cosmic microwave background data, we have an estimation of the composition of the Universe, and the role that the dark matter has on it. According to this, the dark matter should constitute about 26.8% of the mass-energy in the universe and 84.5% of the total mass, compared to the ordinary matter (4.9%), as shown in fig.1.1 [1]. Until now, there is no experimental evidence of the existence of the dark matter, and there are several theories that provide different hypotheses on its origin. Due to the fact that dark matter almost does not interact with the ordinary matter and the radiation, a promising candidate, who can account for at least a part of the missing mass, is the neutrino. Neutrinos are subatomic particles in the Standard Model of particle physics. It is electroneutral and is called "active" since it interacts (although very

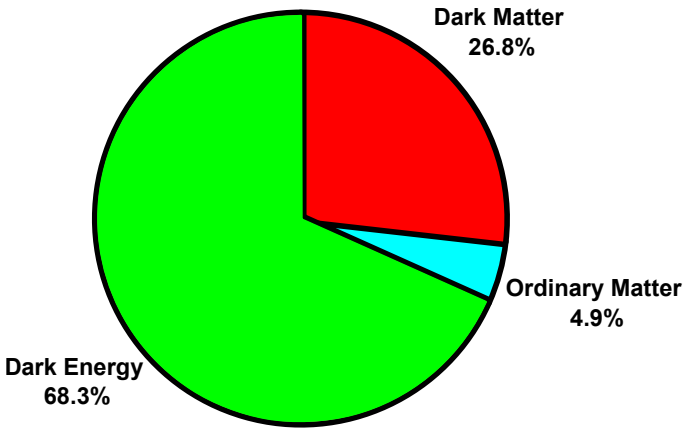


Figure 1.1: *Estimated division of total energy in the universe.*

weakly) with the weak nuclear force and gravitational force. The weak nuclear force, called also weak interaction, is a mechanism between subatomic particles that is responsible for the radioactive decay of atoms. Today the neutrino is the only particle of the Standard Model which was observed exclusively with Left-handed chirality. Chirality is an intrinsic quantum property of a particle that determines whether or not it is subject to weak interaction. For what regards the neutrinos the spin is always opposite to the linear momentum and this is referred to as "left-handed", instead their antiparticle, the antineutrinos, are always "right-handed". This evokes the picture of the right-hand rule for vector angular momentum (fig.1.2). There

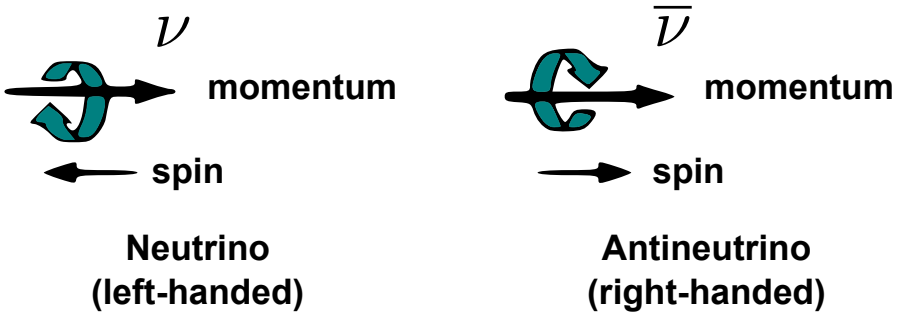


Figure 1.2: *Neutrinos and antineutrinos momentum's difference.*

are three types (or flavors) of neutrinos, electron neutrinos (ν_e), muon neutrinos (ν_μ) and tau neutrinos (ν_τ), and it is known that the neutrinos oscillate between different flavors during the time of flight. With the discovery of this phenomenon,

which earned the Nobel Prize in Physics for Takaaki Kajita and Arthur McDonald in 2015, it is possible to claim that the neutrinos are massive. Einstein's Theory of Relativity states that objects with a certain mass will not be able to reach the speed of light, and consequently objects without mass will always travel at the speed of light. Also, the faster an object travels, the slower time passes, and once an object reaches the speed of light, time will stop for the object (the object will be frozen in time). Since neutrinos oscillate, they are experiencing time (they would not be able to oscillate, or change their types, if time had stopped for them). The fact that neutrinos oscillate means that they travel at a speed that does not reach the speed of light, so this proves that they have a certain mass.

However, the absolute value of this mass is not yet known. In order to find out the answer, the KATRIN experiment (Karlsruhe Tritium Neutrino experiment), is currently in the operational phase in KIT (Karlsruhe Institute of Technology), and it has as objective the measuring of the neutrino mass. In the previous experiments performed in Mainz and Troitsk, the neutrino mass has been set an upper limit of $2.3\,\frac{\mathrm{eV}}{\mathrm{c}^2}$, while KATRIN aims at reducing this limit to $0.2\,\frac{\mathrm{eV}}{\mathrm{c}^2}$ (or measuring the actual mass if it is higher than $0.35\,\frac{\mathrm{eV}}{\mathrm{c}^2}$. However, knowing the upper limit, it is sure that the active neutrino cannot account for all of the dark matters, but only a part of them, in fact a mass of 3 eV would correspond only to 20% of the one of the universe, hence proving that a missing part is present.

The existence of another type of neutrino with right-handed chirality has been hypothesized in numerous theories [2] but it has still not been experimentally verified. This particle is named "sterile" neutrino since it doesn't interact with other particles of the Standard model. Current cosmological observations allow us to hypothesize the sterile neutrino mass in the range $1\,\mathrm{keV} < m_s < 50\,\mathrm{keV}$ [3]: then the sterile neutrino, potentially much more massive than the active one, becomes a good candidate for the dark matter. The TRISTAN experiment (TRitium Investigation on STerile to Active Neutrino mixing), currently in the design phase, aims at the experimental verification of the existence of the sterile neutrino and the measurement of its mass.

1.2 The KATRIN Experiment

The KATRIN (KArlsruhe TRItium Neutrino) experiment aims at measuring the mass of the electron anti-neutrino with a precision of 200 meV by investigating the energy spectrum of electrons emitted from the tritium β-decay. The experiment is since 10 years a collaboration between national and international partners with currently more than 150 scientists, engineers, technicans and students. It has begun running tests in October 2016. Since mid 2018, the regular experiments have started, with an effective data taking time of three years. In this section, the principles and the experimental facilities of KATRIN experiment will be described.

1.2.1 The Neutrino signature

The measurement principle of KATRIN and TRISTAN is based on the tritium β-decay reaction, as shown in fig.1.3. In this reaction the tritium decays into helium

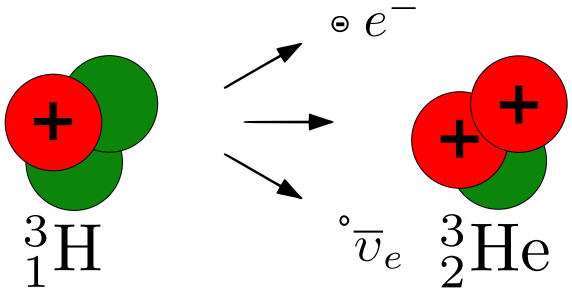


Figure 1.3: *Tritium β-decay reaction.*

by emitting an electron and an electronic anti-neutrino. The energy released by the reaction is distributed between these two particles. In particular, this energy is subdivided into: kinetic energy of the electron, kinetic energy of the neutrino, rest mass of the electron and rest mass of the neutrino. The energies associated to the mass are two constant terms, while the rest of the energy is divided by the two particles according to a certain statistic. Through the high-precision measurement of the kinetic energy spectrum of the electron, shown in fig.1.4, it is possible to obtain the information on the neutrino mass. At the end point of the curve the electron would present its maximum possible kinetic energy, that should be about 18.6 keV, the energy of the Tritium. However as we can see there is a distortion of

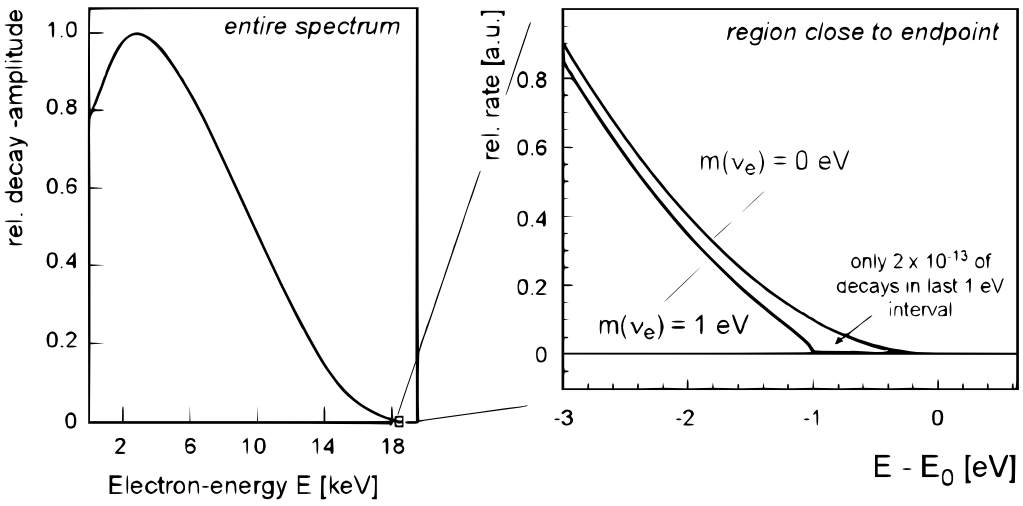


Figure 1.4: *Imprint of neutrino mass on the energy spectrum of β-electrons.*

the spectrum at that position. This means that the neutrino has indeed a certain mass given by the difference between the ideal curve, that assume the mass of the neutrino $m_\nu = 0$, and the sperimental one. In fig.1.4 it is present the difference in the waveform between a massless neutrino and a netrino with m_ν =1 eV. The fraction of β decays falling in the last 1 eV is equal to $2 \cdot 10^{-13}$. Being a really low number, a huge tritium source luminosity and a very high energy resolution are needed, hence the difficult of the experiment. The tritium is an excellent electron emitter for this type of investigation. It is a β radionuclide, an atom instable due to the excess nuclear energy, with the second lowest endpoint energy (18.6 keV) and it has a rather short half-life (12.3 years). Furthermore, the reaction product, helium-3, has a very simple electron shell structure, which simplifies the calculations of the correction to be applied to spectrum due to the interaction between β-electrons and the surrounding gas.

1.2.2 Experimental apparatus

The experimental apparatus for KATRIN, shown in fig.1.5 [4], consists of different sections, with a total length of about 70 meters. The first section (in yellow) performs the calibration and monitoring functions, and it is equipped with an artificial electron source.

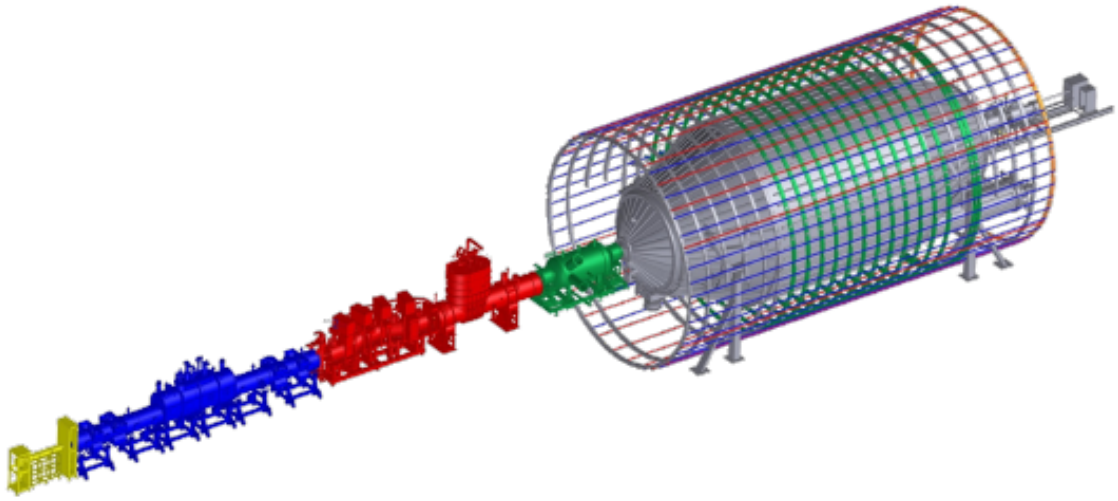


Figure 1.5: *KATRIN's full experimental apparatus with: rear wall (yellow), WGTS (blue), pumping section (red), pre-spectrometer (green), main spectrometer and detector section (both grey).*

Then there is the section (in blue) where the electrons are generated by tritium decay, called Windowless Gaseous Tritium Source (WGTS), as shown in fig.1.6 [5]. It consists of a 10 m long tube with an internal diameter of 90 mm. The tritium gas, with high isotopic purity (greater than 95%) at a temperature of 27 K, is injected into the center of the WGTS tube through capillaries. With a precise injection pressure adjustment, the gas density in the reactor is set to the reference value $\rho = 5 \times 10^{-17}$ molecule/cm^2. The electrons generated by the β-decay reaction are guided by magnetic fields ($B = 3.6$ T) to the end of the tube and then to the spectrometer. Whereas, the helium-3 gas molecules are pumped out from the tube and then sent back into circulation through a closed circuit system. The electron generation rate is 9.5×10^{10} decay/s. In order to obtain a correct measurement of the spectrum, it is necessary to know the gas density with an accuracy of 0.1%. This is mainly because the gas in the tube has an effect on the energy of β-electrons as these β-electrons can encounter single or multiple scattering events with source molecules. These energy losses are measured and taken into account as long as the significant information in the spectrum is not compromised, thanks to a following data processing. The transport section (in red) has two functions: it guides the electrons from the source to the spectrometer through magnetic fields, and at the same time

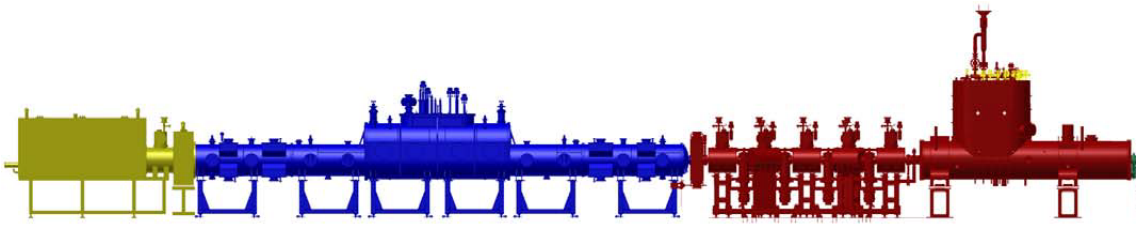


Figure 1.6: *From left to right: KATRIN's rear section, source section and transport section.*

prevents the passing of gas molecules through a pumping system. In this pumping system, a Differential Pumping Section (DPS2F) and a Cryogenic Pumping Section (CPS) work together to guarantee a suppression of the tritium flow by nine orders of magnitude. The differential pumping section (DPS2F), shown in fig.1.7,

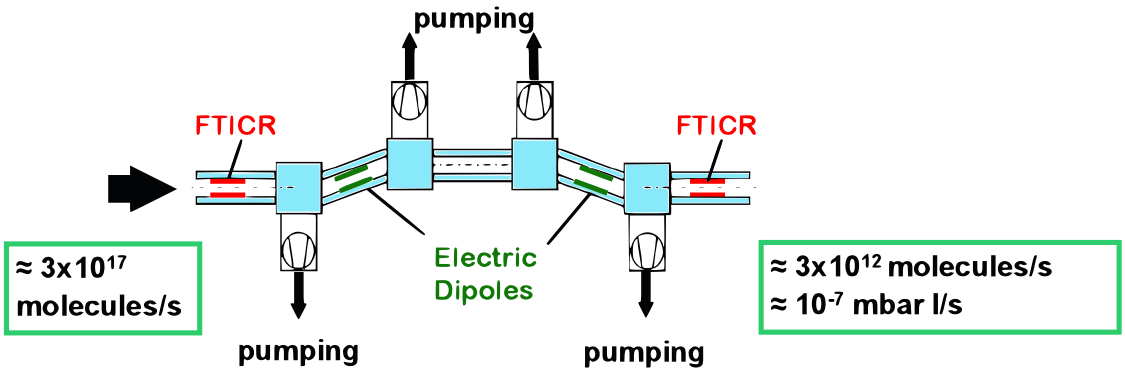


Figure 1.7: *Schematic view of the differential pumping section.*

consists of five 1 m long tubular sections inserted inside a superconducting solenoid, with four turbomolecular pumps extracting the neutral tritium molecules accomplishing a reduction factor of 2.5×10^4. Apart from tritium and electrons, the flux is also composed of ions, which are mostly produced by the tritium decay in positively charged helium. These ions are not affected by the pumping action as they are driven by the magnetic field. Therefore, in order to prevent them from reaching the spectrometer, an alternative strategy is needed: the two sections, WGTS and DPS2F, are bias to a slightly negative voltage so as to attract the ions, whose flow is thus interrupted. The cryogenic pumping section (CPS), shown in fig.1.8,

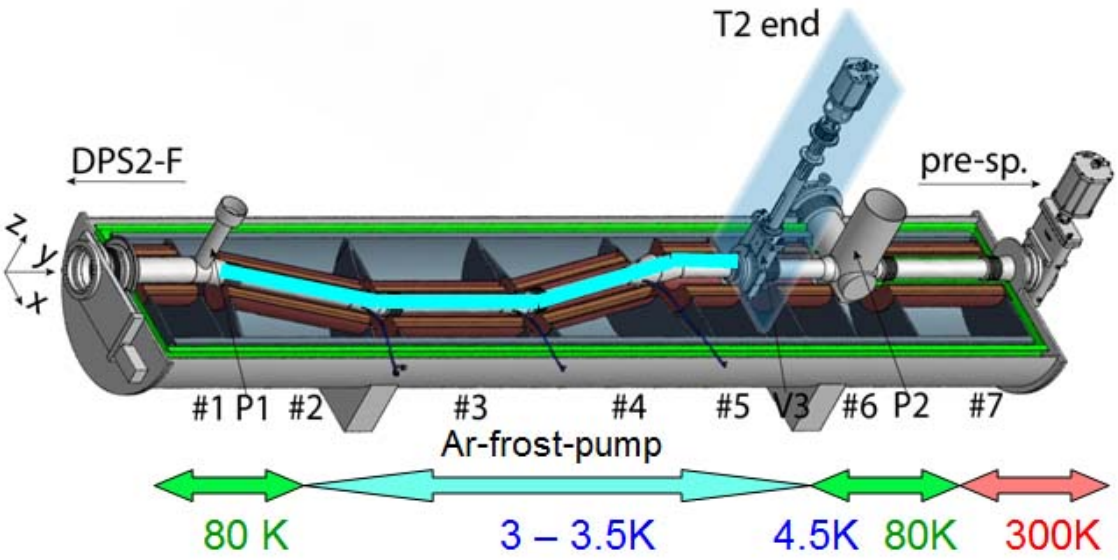


Figure 1.8: *Schematics of cryogenic pumping section.*

exploits the gas condensation phenomenon on cold surfaces for trapping the remaining tritium molecules. As shown in fig.1.9, the inner surface is covered with gold and treated with argon (which facilitates the absorption of tritium) and is maintained at a temperature of about 3 K. In this case the gas contamination is almost zero, and the β-electron flow is guided to the entrance of the spectrometer. The

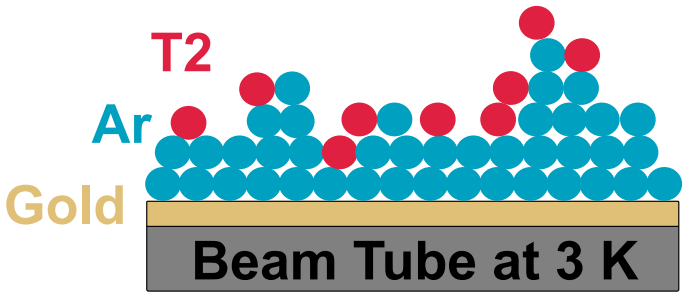


Figure 1.9: *Principle of the absorption of the tritium on argon frost.*

spectrometer is based on the principle of the MAC-E-Filters (Magnetic Adiabatic Collimation combined with Electrostatic Filter), presented in fig.1.10. This type of filter features high luminosity and low background with a high energy resolution, both of which are essential to measure the neutrino mass from the endpoint region of a β-decay spectrum. Two superconducting solenoids are producing a magnetic

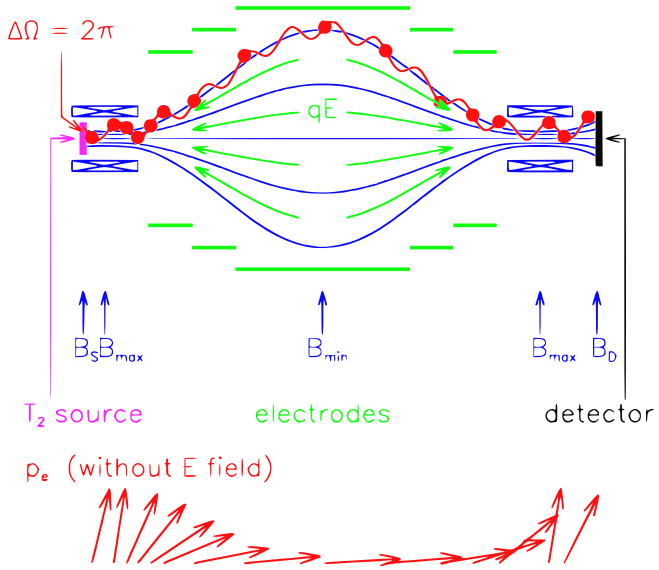


Figure 1.10: *MAC-E-Filter's working principle.*

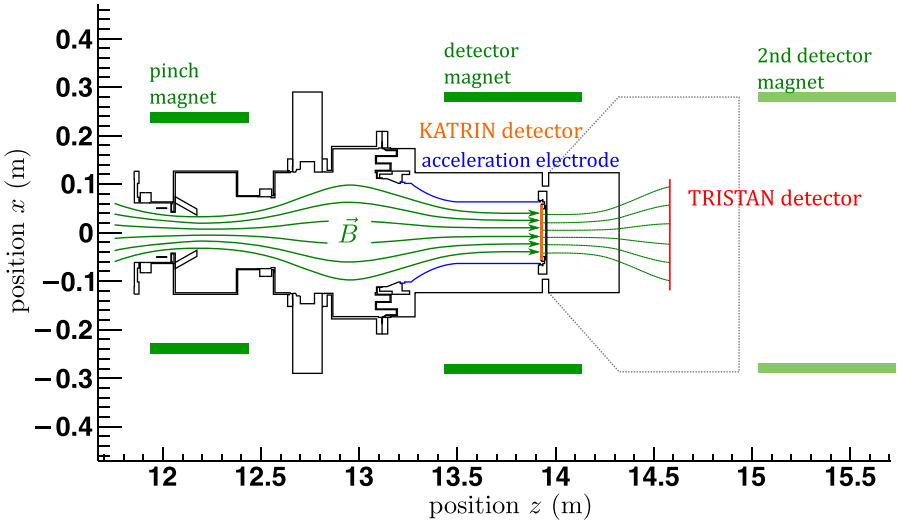


Figure 1.11: *KASSIOPEIA simulation setup of the detector section of the KATRIN experiment. Electrons are guided by the magnetic field lines (green) onto the detector (red). The magnetic field is created by the pinch and detector magnet. An additional magnet can be placed behind the detector to make the field lines intersect perpendicularly with the detector surface. In blue the post-acceleration electrode (PAE) which can be set to up to 20keV is displayed. In orange the current position of the KATRIN focal plane detector is shown and in red the position of the TRISTAN detector is indicated.*

guiding field B. The β-electrons, which are starting from the tritium source in the left solenoid into the forward hemisphere, are guided magnetically on a cyclotron motion around the magnetic field lines into the spectrometer, thus resulting in an accepted solid angle of up to 2π. On their way into the center of the spectrometer the magnetic field B drops by many orders of magnitude. Therefore, the magnetic gradient force transforms most of the cyclotron energy into longitudinal motion. Due to the slowly varying magnetic field B the momentum transforms adiabatically, therefore the magnetic momentum remain nearly constant. To summarize, the β-electrons, isotropically emitted at the source, are transformed into a broad beam of electrons flying almost parallel to the magnetic field lines. This parallel beam of electrons is running against an electrostatic potential formed by a system of cylindrical electrodes. All electrons with enough energy to pass the electrostatic barrier are reaccelerated and collimated onto a detector. Instead, all the others are reflected and lost. Therefore the spectrometer acts as an integrating high-energy pass filter. Varying the electrostatic retarding potential allows to measure the beta spectrum in an integrating mode.

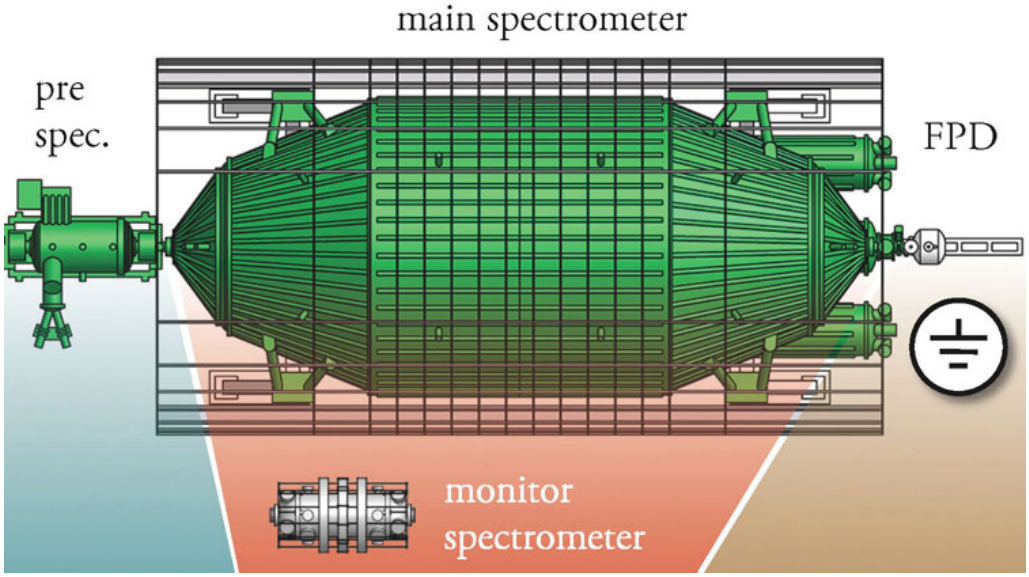


Figure 1.12: *View of KATRIN's spectrometer section.*

The spectrometer section, as shown in fig.1.12, consists of three parts: the pre-spectrometer, the main spectrometer and the monitoring spectrometer.

Figure 1.13: *KATRIN's monitor spectrometer transport through Leopoldshafen to reach the site of the experiment.*

The pre-spectrometer rejects most of low-energy electrons (i.e. below 18.3 keV), which do not carry the information on neutrino mass and so are not useful for the measure. The main spectrometer scan the kinetic energy of electrons to obtain the spectrum in the endpoint, our region of interest (close to 18.6 keV). In fact, it behaves like a high pass filter with an adjustable threshold and the precision of 0.93 eV. The pre-spectrometer and the main spectrometer operate in extreme high vacuum (XHV), with a pressure lower than 10^{-10} mbar.

The monitoring spectrometer is used to check the stability of the bias voltage of the main spectrometer. It has an input of mono-energetic electrons coming from a ^{83m}Kr source that allows to measure the oscillation of supply voltage with high precision. As the power supplies are shared with the main spectrometer, the information on the stability of its bias voltage is therefore obtained.

The last section of the experimental setup includes a solid state Focal Plane Detector (FPD). Before reaching the detector, the electrons, which have been slowed down by the retarding potential of the main spectrometer, are accelerated again to their initial energy. Moreover, it is possible to perform a post-acceleration of electrons up to 30 keV in order to reduce the background effect superimposed on the

signal.

The detector is a monolithic PIN diode array of 148 pixels arranged on a 5"-wafer, with energy resolution of about 1.4 keV FWHM (Full Width at Half Maximum) at 5.9 keV. A photo of this detector is present in fig.1.14 In principle, for the

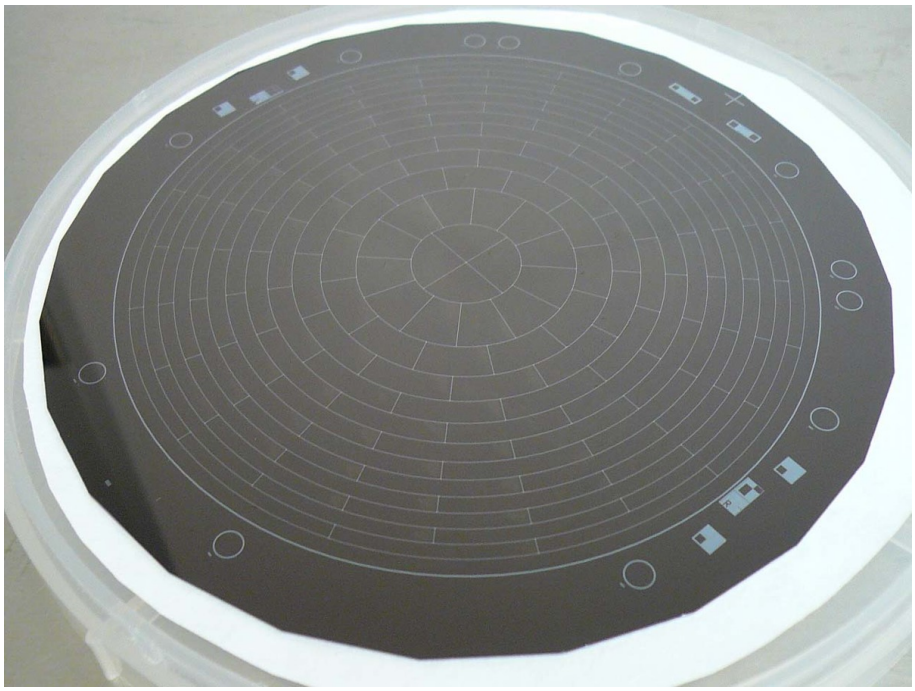


Figure 1.14: *KATRIN's PIN detector.*

measurement of the spectrum, it would be sufficient to use a detector in "electron counter" mode to determine how many electrons have passed through the spectrometer. However, in practice, it is also useful to have the spatial information, for example to correct any non-uniformity of the voltages in the spectrometer, and the energy, typically to be able to distinguish β-electrons from background.

1.3 The TRISTAN Project

The TRISTAN experiment, as mentioned before, aims at discovering the so-called sterile neutrino and to measure its mass. The physical signature of the sterile neutrino, which is a hypothetical particle beyond the Standard Model, could be investigated through observations on the full tritium β-decay spectrum. If the sterile

neutrino is in the keV mass range, then it will be a prime candidate for the dark matter; if it is in the eV mass range, the anomalies in neutrino oscillation experiments have to be resolved.

1.3.1 Signature of sterile neutrino

The electron anti-neutrino, generated in the tritium β-decay reaction, is actually composed of the superimposition of different mass eigenstates. Therefore, the spectrum of the electrons is given by a superposition of the spectra corresponding to the individual flavors. However, the known mass eigenstates have values too close to be distinguished experimentally, so their effect on the measured spectrum is equivalent to a single mass: the mass that is measured in the endpoint region of the spectrum with KATRIN. On the contrary, the presence of an additional eigenstate

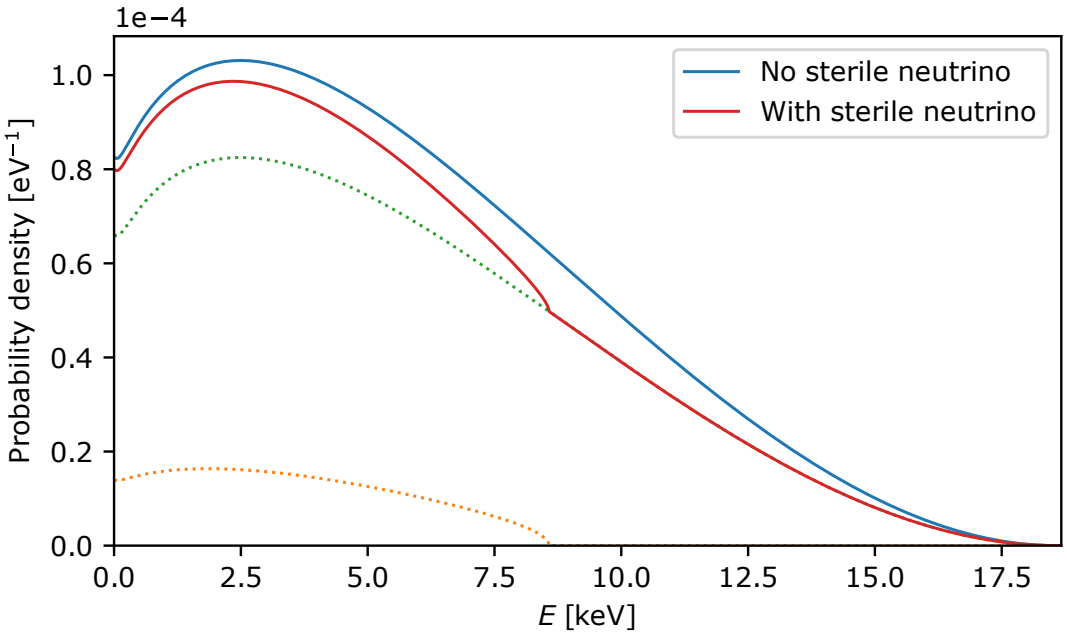


Figure 1.15: *Imprint of sterile neutrino on β-electron spectrum, mixing of a sterile neutrino with $m_s = 10\,\mathrm{keV}$ and $sin^2\theta = 0.2$. The orange dotted line depicts the decay branch into a sterile neutrino, the green dotted line shows the regular decay branch into a light active neutrino. The solid red line is the resulting superposition of the two spectra, which includes a kink-like distortion. As a comparison, the blue dashed line shows a spectrum without a sterile neutrino.*

in the order of keV (below the endpoint), which is the sterile neutrino, would be clearly distinguishable on the spectrum, with a large energy difference compared to the lighter eigenstates. Its signature is a sudden change of slope in the energy spectrum, as shown in fig.1.15. As this spectral distortion is very small, in order of 1 part per million, specific techniques are needed to reveal it precisely, such as the wavelet transform. In addition, an energy resolution of approximately 300 eV at 30 keV is needed [3].

1.3.2 Experimental setup

TRISTAN makes use of the same experimental setup as KATRIN: the β-electron source (WGTS) generates 10^{11} decays per second; the transport section guides electrons to the spectrometer by blocking at the same time the tritium molecules. Finally the electrons are guided to the focal plane detector.

The main advantage of the KATRIN setup for the research of the sterile neutrino is the ultra high β electrons generation rate by the reaction, which allows to obtain the high statistics necessary for the measurement. However, the detector used in KATRIN is not designed to handle such a high rate of electrons, since in KATRIN the retarding potential of the spectrometer is used to scan only the endpoint region of the spectrum, in which the number of electrons is not high. Therefore, the amount of electrons that actually reach the detector is largely reduced (i.e. each pixel is hit with a rate in the order of few electrons per second). For this reason, a new detector for TRISTAN is required. In this case, the β-electrons rate will be greater than 10^8 cps. To limit the count rate on each detector channel to about 100 kcps, the whole detection area of 20 cm diameter is divided into approximately 3500 pixels. As shown in fig.1.16, the detector will be composed of 21 modules, each of which contains a 166-pixel SDD array chip with 4 cm side. Every SDD array is partitioned into 14 groups of 12 pixels.

TRISTAN can be operated in two different ways, in order to reduce systematic uncertainties and avoid false-positive signals:

- **Integral Mode**: as in KATRIN, it is utilized the spectrometer MAC-E-Filter to scan the spectrum varying the retarding potential. The detector must only count the number of β-electrons. It does not need an high energetic resolution

since the energy discrimination is done by the electrostatic filter.

- **Differential Mode**: the retarding potential of the spectrometer is fixed to a low value to allow the passage of the majority of the electrons generated by the WGTS. This mode requires an excellent energy resolution to be able to assign the right energy information to each electron, and a precise understanding of the detector response in a broad energy range and at high counting rates.

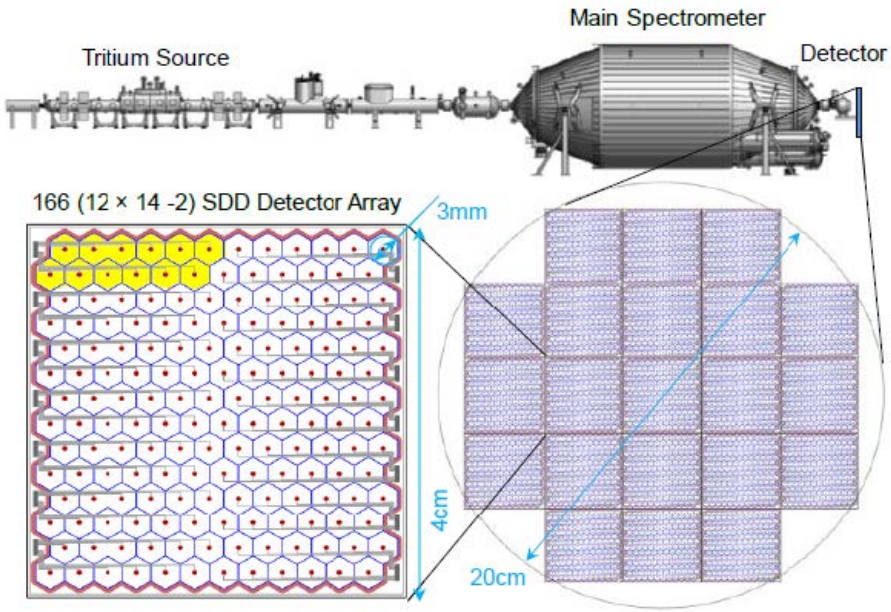
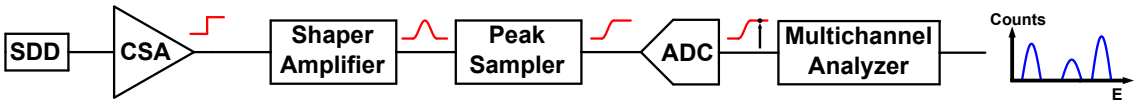


Figure 1.16: *TRISTAN detection system showing 3486 SDD pixels arranged into 21 matrices. Each hexagonal SDD pixel has an approximate diameter of* 3 mm.

It can be demonstrated [3] that the measurement operated in a differential mode is able to utilize the most of the potential of the wavelet transform and therefore allows to obtain a better sensitivity to the sterile neutrino. For a successful application of the wavelet approach, a differential measurement with an energy resolution in order of FWHM = 100 eV - 200 eV is necessary. Therefore, the SDDs have been chosen for their excellent energy resolution (<200 eV FWHM at 10 keV) and very good counting rate capabilities. However, the two measurement modes are prone to different systematic uncertainties and hence the ability to use both of them allow to cross check each other.

1.3.3 Classic readout chain



(a) Analog Read out Chain (ARC).

(b) Digital Read out Chain.

Figure 1.17: *Detector signal read-out chain possibilities.*

In fig.1.17 two typical type of acquisition chains are shown. The first one, called Analog Read out Chain (ARC) have an analog setup. The current signal coming from the detector is amplified and converted into voltage by low-noise Charge Sensitive Amplifier (CSA), then the signal is sent to a Shaping Amplifier (SA), a filter composed by a series of real or complex conjugate poles. The peak of this filter is sampled by a self-triggered sample-and-hold circuit, the so-called peak stretcher (PKS), which, as the name suggest, stores the peak of the signal and maintains it at the output. Successively this peak is converted into a digital signal thanks to an ADC. The analog solution, with respect to a digital one, is able to deal with an higher number of channels in a smaller area, providing smaller power consumption and cost per channel thanks to its multiplexed structure. The second solution is a digital one, that uses a Digital Pulse Processor (DPP) to process the CSA output. The output of the CSA is digitalized by a fast ADC (50-80 MHz). All the other processing stages, as digital filtering, are performed in the digital domain inside an FPGA. DPPs are able to provide higher count rate per channel with respect to the analog solution, as shorter pulse processing times can be reached and several additional processing techniques can be used to increment count rate, limiting pulse pile-up phenomena within the detector. The decision whether to use the digital or the analog solution depends on the application constraints and on the number of the channels involved. As a matter of fact in the TRISTAN experiment the final approach will be the digital one, however its implementation require time and a lot of testing, and it is still needs further investigations. The analog approach has

been chosen for the starting phase of the project, to perform the initial tests on the SDDs' matrices. Fig.1.18 shows a block diagram of the acquisition chain of the signal for one pixel of the TRISTAN detector: the β-electrons reach the detector (Silicon Drift Detector) generating a charge pulse proportional to their energy on the anode capacitance.

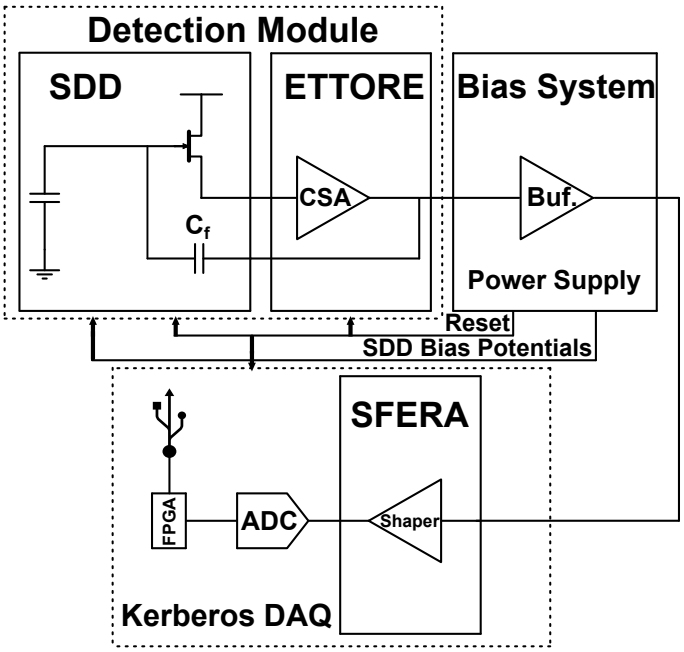


Figure 1.18: *Architecture of the complete acquisition chain. Ettore (front-end CSA) and SFERA (semi-Gaussian shaper) are ASICs realized in* $0.35\,\mu$m *AMS CMOS process. The bias board provides power supply to the ASIC board, manages the reset and provides also filtered high voltages to bias the detector. The FPGA is a Mars AX3 module from Enclustra.*

The ETTORE ASIC, that is the front-end Charge Sensitive preAmplifier (CSA) performs a charge pre-amplification, and at its output are present step-like voltage signals. The information of incident electron energy is contained in the amplitude of each step. This waveform is amplified once more in the bias board to decrease the noise impact of the following circuits. The bias board generates the bias voltages for all the system and transmits the amplified signals of interest to the acquisition system: the shaper first filters the signal using a gaussian filter, then it maintains the peak of the result, ready to be sampled by an ADC. Finally, the FPGA acquire the signal and perform some processing of the data received.

Detailed descriptions on the front-end electronics, including the detector and preamplifier stages, will be presented in chapter II.

1.3.4 Rendering of the final detection system

The target detection system can be seen in fig.1.19.

Figure 1.19: *Target design of the final system for TRISTAN. We can see a rendering of the 21 SDD's modules, with 3486 pixels.*

Each module, having 166 pixels, will be composed by one detector board, two ASIC board and a pair of flex cables to deliver the signals to the following electronics for the readout. The 166 pixels detectors (as in part the 47 pixels prototypes) are cutted at the edges for the backscattering effects, to maintain the electrons energy inside the detector, and for mechanical reasons, to have additional space for the bondings of certain contacts, like the Back Frame (BF) and the Back Contact (BC).

We can see a representation of this in fig.1.20.

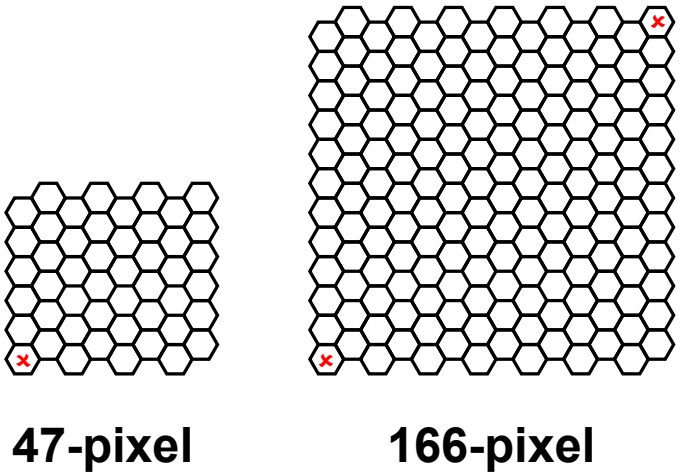


Figure 1.20: *Schematic of the 47 and 166 pixels detectors.*

While the detector boards host the 166-pixel detector, the ASIC boards contain several ETTOREs, that filter and amplify the signals coming from the detector board. The output of the ASICs will be brought to the following electronics using a combination of flex cables and Airborn connectors. We can see a dummy of each single module in fig.1.21. Due to the high magnetic fields that the system has to sustain, all the components have to be made to resist at high magnetic field in the order of 3 T. Along with this, the size constrain are very challenging, since each ASIC board has to carry a total of 200 signals without significant losses and degradations. The difficulties arise having in mind that each signal has to be at a certain distance from the others on the PCB, both horizontally and vertically, and that each via on the board gives an additional capacitive contribution. On top of that, being this setup developed vertically, a custom flex detector board has to be designed, since it has to be able to bend, to be able to be connected to the ASIC board. Given the tight requirements on space and signal integrity, the natural course of action has been the design of preliminary setups, in order to find, fix and even discover all possible errors that may arise from the creation of such a challenging system. These are the motivations why two important setup have been produced: the 12-pixel and the 47-pixel, both described in the following chapters.

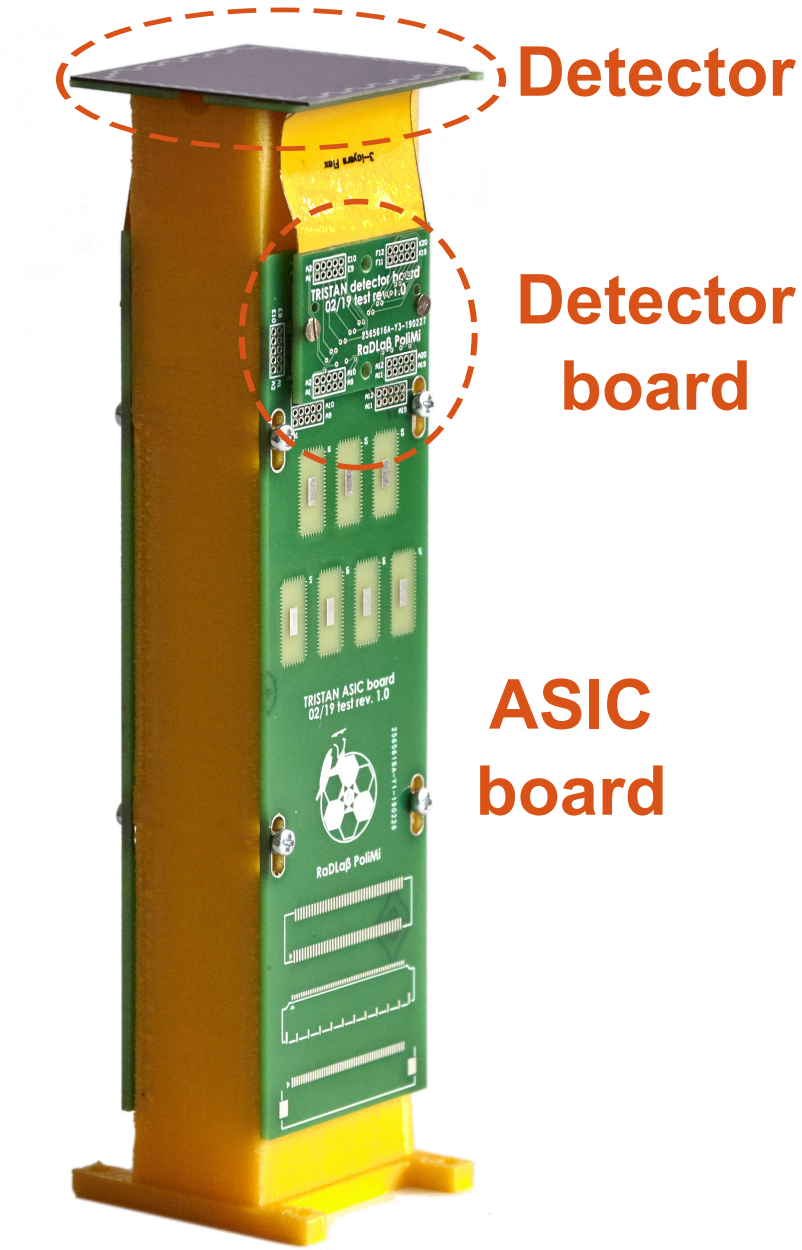


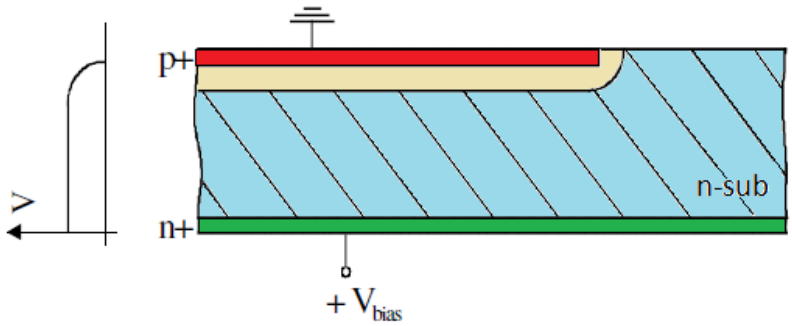
Figure 1.21: *Target design of a single module in TRISTAN. We can see the detector on its corresponding board and the ASIC board with the space needed to bond the ETTORE's chips.*

2 | Front End Electronics

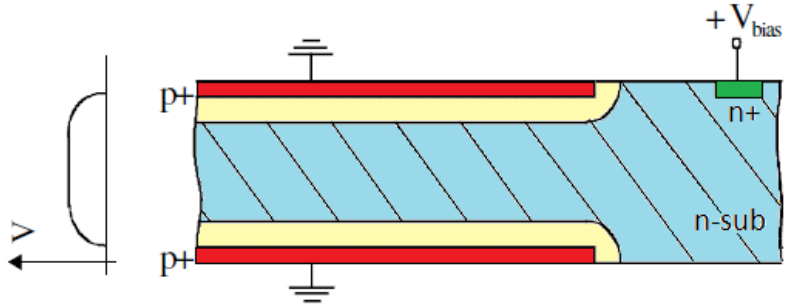
In this chapter, all the front-end electronics are presented, in their physical and behavioural level. First of all there is the choice and the motivations for the selection of the detector, which must have a good energy resolution and must be able to handle high count-rates (as explained in the chapter 1). Then there is the presentation of ETTORE, a 0.35 µm *CMOS AMS ASIC, which acts as charge preamplifier for the detector signal. Finally there is a description of SFERA, a Shaping Amplifier with adjustable peaking times and gains, a good candidate that may be used for the readout of the experiment.*

2.1 SDD for TRISTAN

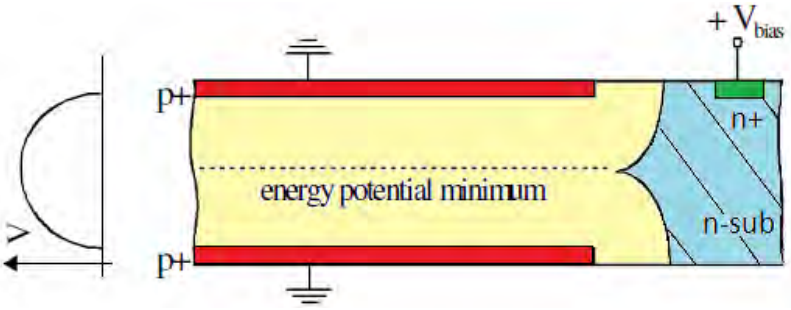
The technology used for the detector of TRISTAN is called SDD, Silicon Drift Detector, first proposed by E.Gatti and P.Rehak in 1983 [6], because it has a good energy resolution and it is capable of a high count rate [7] [8]. As a matter of fact, this technology is characterized by a very low anode capacitance, a very important parameter because it reduces the time of optimum formation of the filter. The working principle is an improvement of the one of a PIN junction. As we can see in fig.2.1, in a classic PIN detector the n^+ and the p^+ junctions are in complete opposite positions in the device, leading to an high anode capacitance. Instead, in a SDD device the pad of the n^+ junction is way smaller, and the p^+ has two surrounding pads. In this way the depletion region of the substrate increases as it is increased the reverse voltage, and the complete depletion is reached for voltages much lower than in the case of a standard PIN device. More importantly, decreasing the total area we have a total capacitance associated with the anode in the order of 100 fF. In fig.2.1(c) we can see the energy potential minimum in which the electrons generated by the radiation in the depleted region of the SDD are collected. To guide this electrons towards the anode, we need an electric field with a direction parallel to the surface of the wafer. The TRISTAN structure is made to allow the



(a) Structure of a traditional PIN detector.



(b) Structure of an unbiased SDD detector.



(c) Structure of a biased SDD detector.

Figure 2.1: *Structure and functionality of a SDD detector.*

segmentation of the electrode p^+ and the polarization voltages of the segment. To guide the electrons in a radial way, it is used a concentric structure, as shown in fig.2.2. With this strategy the potential energy diagram is deformed as in fig.2.3, to collect all the electrons in this hole of potential generated in the anode. Since an electron/hole pair always is generated, the remaining holes are instead collected in the electrodes p^+. To achieve the correct segmentation of the voltages, it is used a

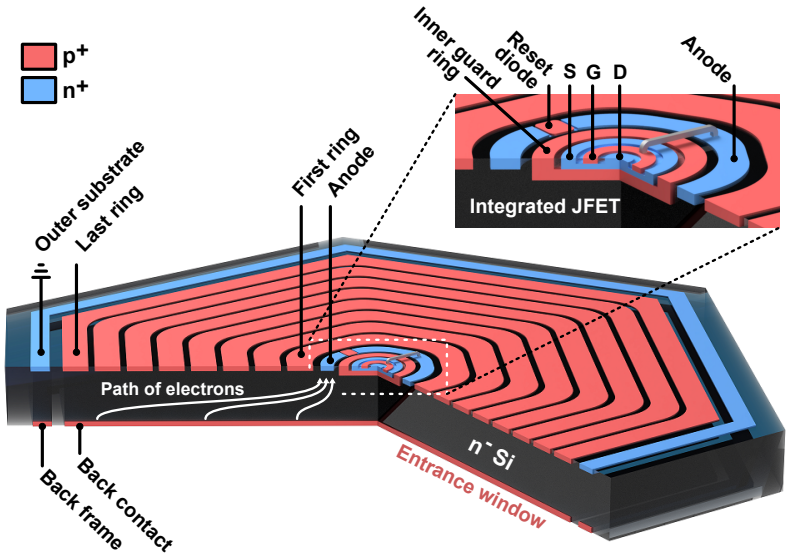


Figure 2.2: *Structure of the circular SDD in TRISTAN.*

simple resistive voltage divider integrated in the SDD. Using the two bias voltages, R_1 and R_X it is possible to have the correct step on all the rings between them. The resistances, integrated in this case, can be made using a series of FET in transdiode configuration. The front-end n-channel JFET is directly integrated on the detector

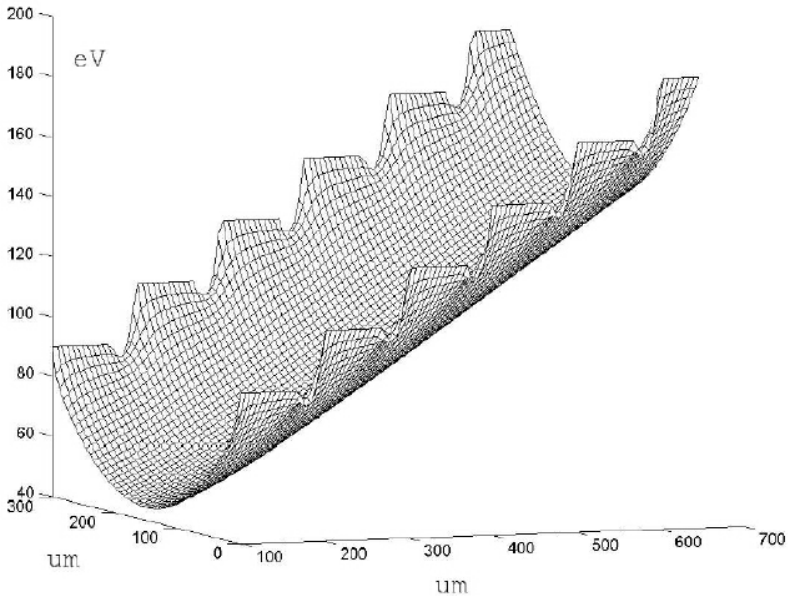


Figure 2.3: *Potential energy in the depleted regions in TRISTAN's SDD.*

wafer and it is present in each pixel, reducing the stray capacitances of the anode due to the fact that the anode has to be connected only to the gate of the JFET, instead of being bonded to an external preamplifier. However, this technology decision reduces the transconductance of the integrated JFET, since the dimensions of the FET are bounded by the technology. The window in which the radiation enters is in the bottom part of fig.2.2. Although SDDs are usually used for photon detection, they can be efficiently used, as recent studies have demonstrated [9], for electron detection applications. The absorption of the photons in a specific energetic range (from hundreds of eV to tens of keV) is caused by the photoelectric effect. A photon of energy E is absorbed inside the silicon generating a photoelectron with the same energy E. This new energetic electron creates electron-hole pairs by scattering until all its kinetics energy is dissipated. In the case of incident electrons on the detector, the electron starts immediately to generate electron-hole pairs. The main difference between the two mechanisms is the point in which the energy E is transmitted from the source to the silicon. In the case of the photons the electron is generated inside the SDD, in its sensitive layer. In this way all the energy E is collected in the SDD and nothing is wasted. The incident electron is coming from the outside, so it is present not only a backscattering effect but even a loss due to the amount of energy absorbed by the dead layer. All these aspects can be easily seen in fig.2.4.

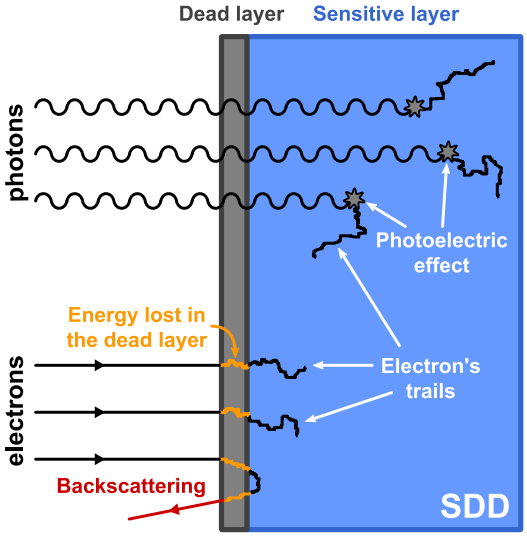


Figure 2.4: *Differences in the absorption of electrons and γ-rays in SDDs.*

An SDD detector which is optimally biased for X-ray operation it is also optimally biased for electron detection, since the biasing is only affecting the internal charge collection dynamics. However, the responses of the two beam, made by electrons and photons respectively, are really different. We can see it in fig.2.5. We can see a broad tail given by the incomplete absorption of the monoenergetic electrons due to backscattered events. In addition it is present a tiny shift of the main electron peak from its 20 keV nominal value, due to the fixed amount of energy lost in the first nanometers of the entrance window. To reconstruct a β-spectrum of an unknown source a proper model of the SDD is required [9].

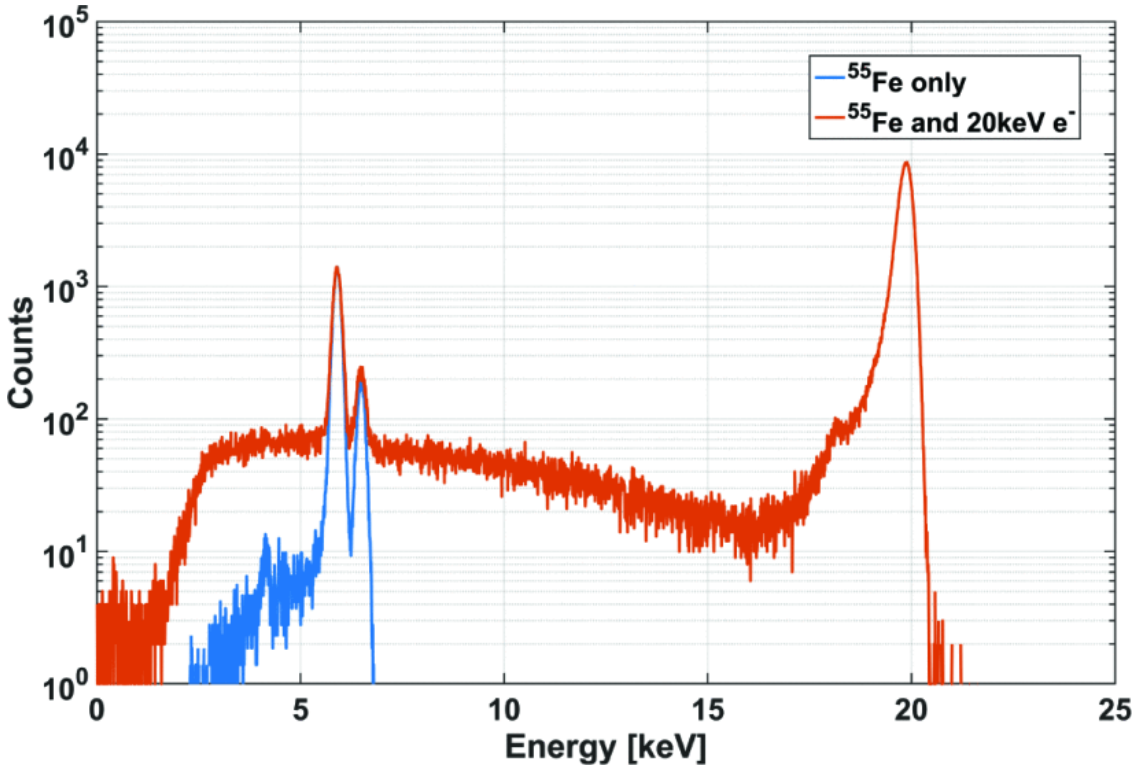


Figure 2.5: *Response of the SDD to photons and to electrons.*

The charge generation events continue to charge the anode capacitance of the gate of the integrated JFET. Combined with the leakage current that gives a ramp with a fixed slope, these effects cause the front-end electronics to saturate, so it is necessary to use a reset mechanism. In the TRISTAN's SDD the reset of this charge is made through a reset diode integrated in the detector, switched on with a periodic

pulse (controlled by the electronics) to remove the accumulated charge in the anode. In fig.2.6 we have a zoom of the SDD's structure, with highlighted function of the pins. We have:

- The source, the gate and the drain of the integrated JFET.
- The anode, that collects the electrons (and the leakage current) on its capacitance. It is connected to the gate of the JFET through a metallic strip. In this way, based on the charge stored on the anode capacitance, it modifies the current signal of the JFET, thus sending our signal of interest to the following electronics.
- The reset diode pad, that activates the diode and discharges the anode capacitance.
- R1, or ring 1, the first of the rings that provides the drift field necessary to focus the incoming electrons to the anode.
- Inner Guard Ring (IGR), as its name, it is a guard ring that maintain low leakage current for the SDD without any breakdown at the high voltages biases caused by the depletion and drift mechanisms.

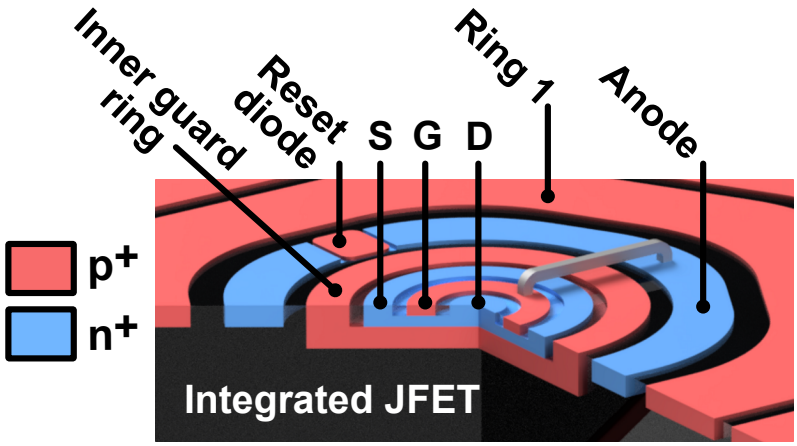


Figure 2.6: *Central part of TRISTAN's SDD, with highlighted rings' functions.*

2.1.1 Detector's prototypes

All the detectors presented in the following have the on-chip connections presented in fig.2.7. During the writing of this thesis, there are present basically 4 SDDs

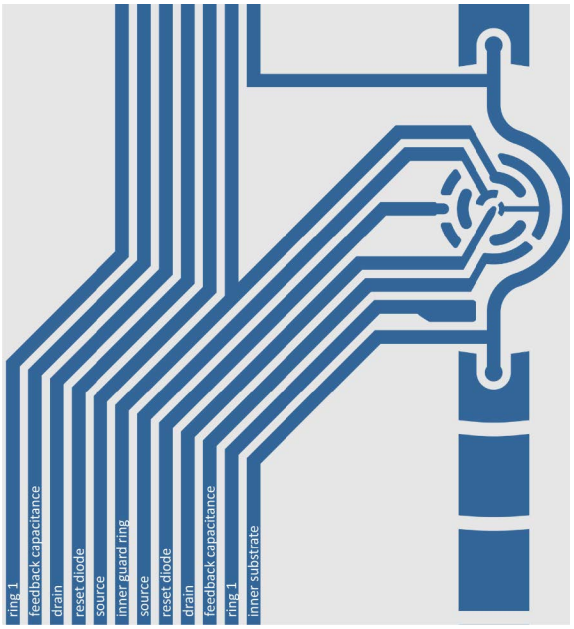


Figure 2.7: *Connections in TRISTAN's SDD.*

geometries, all produced by the MPG-HLL laboratory, in Munich:

- **Single-pixel SDD**

  Each detector has an active area of 10 mm^2 and an integrated n-channel JFET. We can see a photo in fig.2.8 of 4 different samples. The main difference, easily visible, is the presence of an aluminum layer on the entrance window for two of them. This layer is introduced to protect the detector, blocking the low-energy radiation and allowing the passage of X-rays photons. The two samples with this coating were used with an ^{55}Fe source and a custom 2-channel experimental setup. Instead, the remaining ones were used for the measurements with an electron source, with a Scanning Electron Microscope (SEM) in collaboration with Università degli Studi di Milano-Bicocca. Of course the presence of the aluminum coat would have introduced an additional insensitive layer detrimental for electron spectroscopy applications.

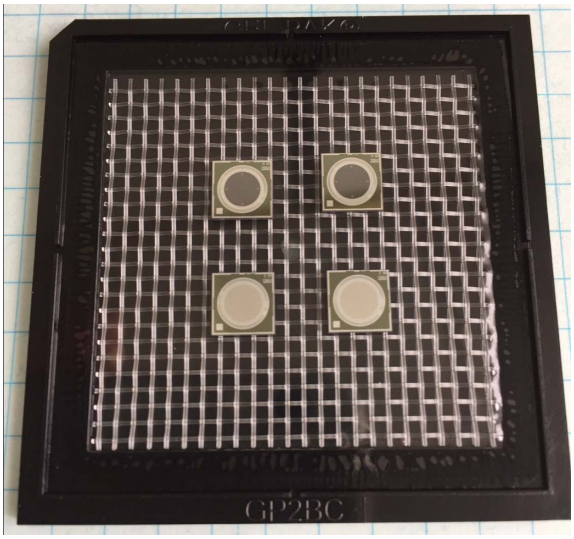


Figure 2.8: *Photo of a single pixel detector for TRISTAN, developed by MPG-HLL. The chip size is* 6 mm×6 mm.

- **7-pixel SDD**

  After a successive test of the single pixel detectors, the seven pixels one was the natural progression. Each one of the seven pixels has an almost hexagonal shape and a characteristic small anode. The pixels are arranged in a gapless fashion so that no dead area inside the array is present. The chip size is 8 mm×8 mm. In fig.2.9 we have a photo of a real sample, in the left there is the entrance window, while in the right the bonded chip.

- **12-pixel SDD** Represented in fig.2.10, the twelve pixel is basically made by 12-single pixel detectors, divided in two columns of 6 pixel each, as a natural evolution. The chip size is 8.25 mm×22 mm.

- **47-pixel SDD** In fig.2.11 and 2.12 we have the comparison of the 47-pixel design with the 12 one, and a real photo of the detector. The chip size is 23.5 mm×22 mm, and the thickness is 0.45 µm. Each group of 12 SDD cells is connected to one common reset line, in order to reset them all at the same time. All the bonding pads are placed on a single edge. It is present a testing JFET at the edge of the chip, in order to test the characteristic of the integrated JFET searching for possible manufacturing errors.

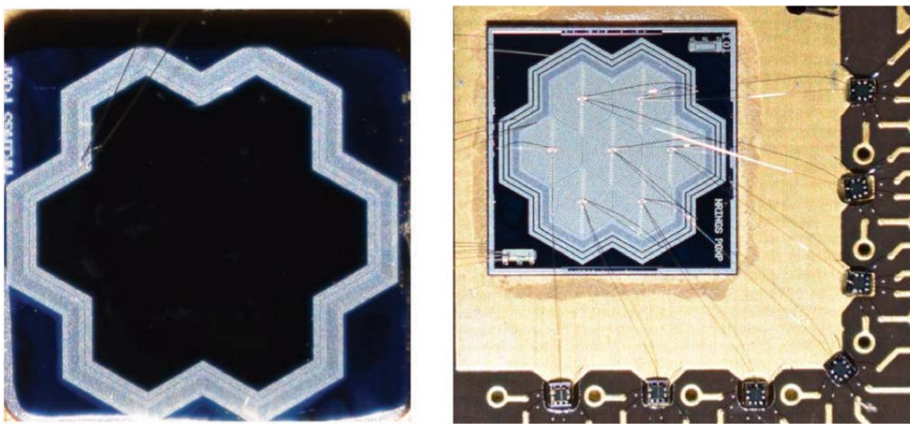


Figure 2.9: *Photo of the 7-ch pixel detector for TRISTAN, developed by MPG-HLL. In the left we have the entrance window side of the detector which has no structuring of the individual cells. In the right, the read-out side of the detector chip, bonded in a working setup. The anodes are bonded to individual preamplifier ASICs, which are arranged around the chip.*

Figure 2.10: *Photo of the 12-ch pixel detector for TRISTAN along with more single pixel detectors, all developed by MPG-HLL.*

Figure 2.11: *TRISTAN 47-ch pixel SDD in comparison with the 12-pixel's one.*

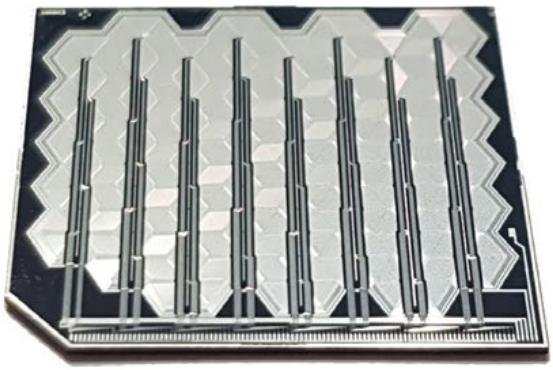


Figure 2.12: *Photo of the 47-ch pixel detector for TRISTAN, always developed by MPG-HLL.*

2.2 ETTORE ASIC

Ettore is a 12-channel ASIC (application-specific integrated circuit), named after a famous Italian physicist, Ettore Majorana, who has contributed significantly to neutrino studies [10]. Ettore is a charge preamplifier designed to readout SDDs with integrated JFET which are operated in a pulsed reset regime. Each channel is composed by a first stage pre-amplifier, a second AC-coupled amplification stage and a comparator, used to detect the preamplifier saturation. It is made with the AMS CMOS 0.35 µm technology and it is born from a collaboration between Politecnico di Milano and XGLab as a prototype for the TRISTAN experiment.

2.2.1 General Characteristics

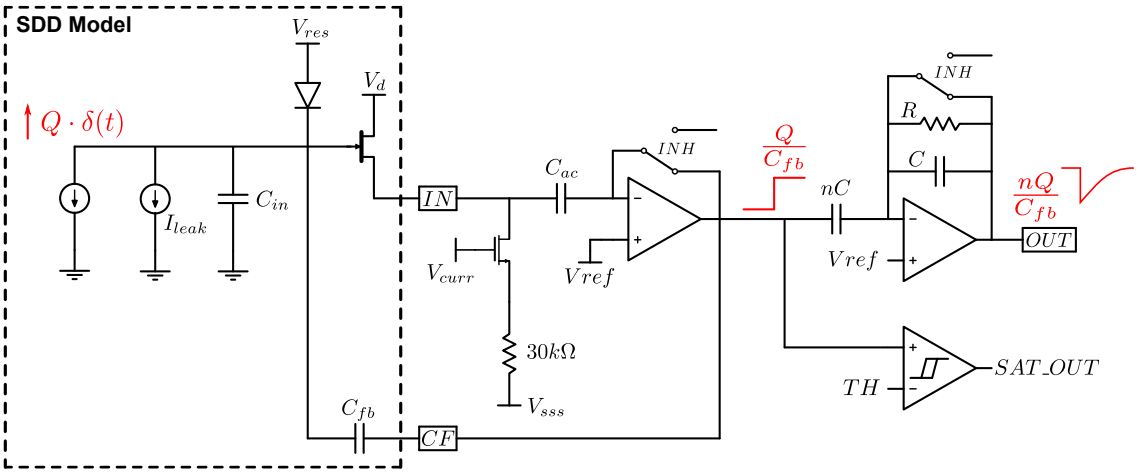


Figure 2.13: *Simplified structure of one ASIC channel; in red it is shown the effect of a delta-like signal with charge Q. We have both the first and second stage represented.*

In fig.2.13 is shown the schematic of a single Ettore's channel connected to a detector pixel, and it is possible to see the signal propagation generated by an event. The first stage has a Charge Sensitive pre-Amplifier architecture that integrates the charge of the detector, stored in the capacitance C_{anode}, on the feedback capacitance C_f. In this architecture, the JFET is used in source follower configuration, then the signal goes to the non inverting terminal of the operational amplifier, through a decoupling capacitor ($C_{AC} = 10\,\text{pF}$), used to cut the DC frequencies. By the use of the negative feedback, the voltage of the SDD's anode is kept constant and the charge is integrated on the capacitance C_f. So the output of the first stage has a ramp like behaviour, as it is possible to observe in fig.2.14. The ramps are due to the continuous integration of the leakage current on the capacitance C_f, while the single charge pulses create the superimposed step-like signals. When the total ramp (formed by the continuous leakage current and the step-like signals) gets close to the supply voltage, a reset signal is given to the reset diode of each pixel, to avoid the saturation and consequently, the loss of the signal. In this way it is possible to discharge the anode of each detector of the accumulated charge till that moment. In the meantime, also the ASIC is reset by an external inhibit signal (INH), to inhibit its operation during the reset phase and to discharge its feedback capacitance C_{fb}.

In order to establish a reset, Ettore is designed to be able to generate a saturation signal through a comparator, which compares the output of the preamplifier with a fixed threshold TH (nominally equal to 2.7 V). When this threshold is exceeded, the comparator generates a signal which goes in a OR block with the rest of the 11 saturation outputs of other ASIC channels. This create a common saturation signal that commands the reset of the ASIC and of the detector as soon as one of the channels saturate. The reset pulses are not generated internally by Ettore, but from the bias board. The signal generated by the comparator of ETTORE is given as input to the bias board, and its rising edge triggers the generation of two different reset pulses: the SDD reset and the ASIC inhibit (INH). The first one during normal operation is at a low voltage, -15 V, to inhibit the reset diode and allowing the integration of the signal. Instead, during the reset phase it reaches around 3 V for few microseconds. The second one, normally grounded, is pulsed to 3.3 V, and it lasts for a bit longer than the SDD's one (few μs more).

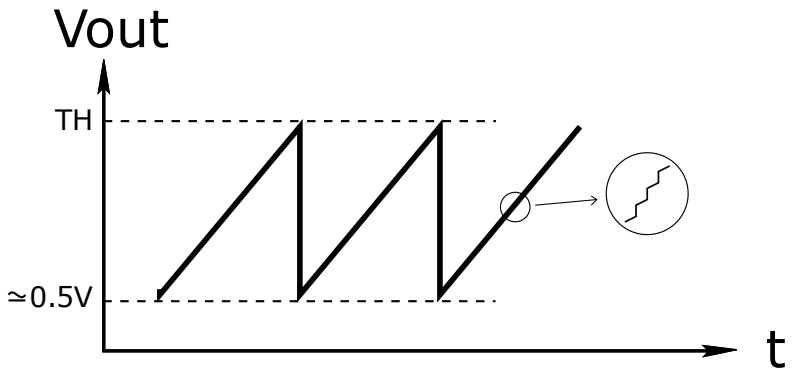


Figure 2.14: *ETTORE first stage output signal, with a zoom on the characteristics step-like signals.*

Another commonly used strategy for the reset of source follower detectors, is the discharge via the avalanche current generated by the JFET in case that a threshold is overcome [11]. This avalanche mechanism is generated by the impact ionization from the source-to-drain electron current (I_{DS}), in presence of a high enough drain-gate voltage (V_{DG} above 6 V) [12]. The holes generated by the ionization are collected at JFET gate and recombined with the signal plus leakage electrons previously collected at the anode. However, this reset current is an additional source of noise, and this is the reason why the first architecture is implemented. In order to disable

the avalanche current, in the used CSA the voltage V_{DG} is kept under this threshold. Alternatively, it is possible to provide a periodic asynchronous reset. The second ETTORE stage performs a derivation operation on the output of the preamplifier, with a time constant of 15 µs and an inverting gain. As an additional characteristic, it is possible to monitor either the signal coming from the first or the second stage: this selection can be done by means of providing a digital signal to a dedicated pad (fig.2.15): when set to a certain value, it allows to read the preamplifier output; if set to GND (default value), the output of the second stage is enabled. Of course, it is also possible to monitor directly the preamplifier output by probing the pad on the feedback capacitor C_f.

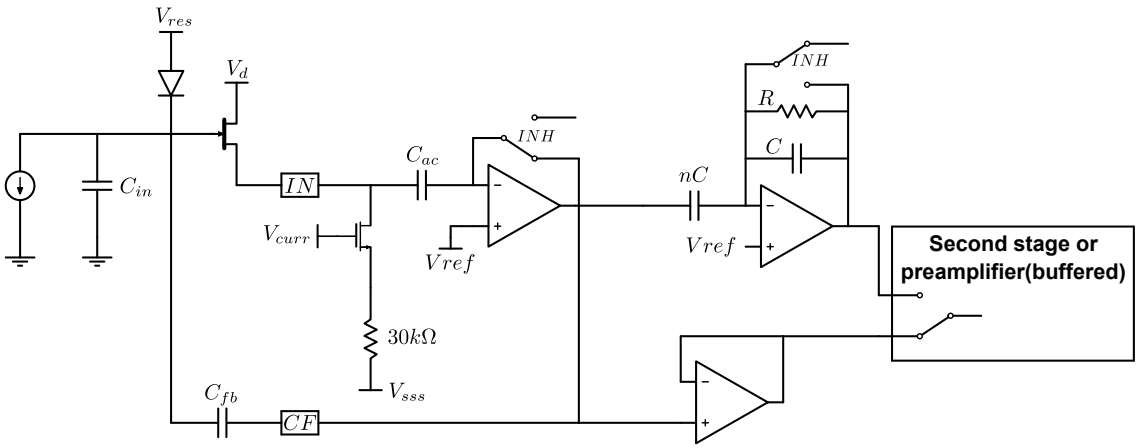


Figure 2.15: *ETTORE first and second stage.*

There is the possibility of "switching off" each ASIC channel by imposing the voltage on the output node to ground, requiring a sensing mechanism on the increase of the amplifier output current. This feature is implemented for both the first and the second stage, increasing the flexibility. The bias system is the part of the system that fix the output node of each ASIC channel to GND. The ASIC has been optimized since the start of the project. In the first version (V1) ETTORE has 12 channels, in particular channel 1 to 7 feature a standard readout, based on a conservative design and guarantees a rise time (10% to 90%) of step signals of about 50 ns; channels 8 to 12 feature a more advanced readout, which employs a more complex compensation strategy, allowing a faster signal processing with lower rise time of 30 ns. All the channels have the same circuit structure, the only differences are in the compensation

strategy of the OTA. The standard readout brought better results, hence the second version of the chip (V2) has all the 12 channels made with this configuration.

2.2.2 First Stage

The first stage of ETTORE, even called Preamplifier stage, is composed by a current generator, a decoupling capacitor and an Operational Transconductance Amplifier (OTA), as we can see in fig.2.16.

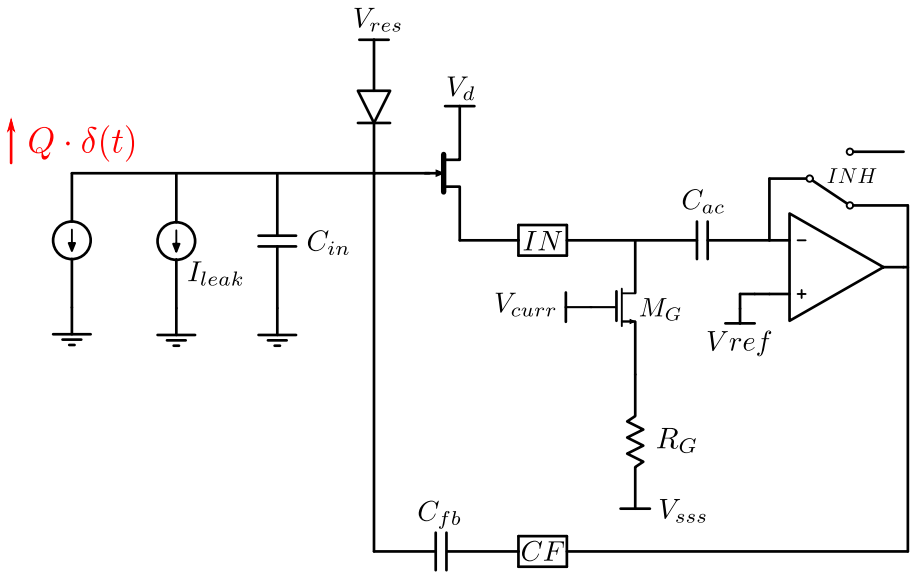


Figure 2.16: *ETTORE first stage schematics.*

As shown in the schematic above, the preamplifier is connected to the SDD via two contacts: the contact named IN is connected to the source of the integrated JFET on the detector; the contact named CF is connected to the feedback capacitor C_f, which is also integrated on the detector. The current generator, composed by an nMOS transistor M_G and the R_G resistor, provides the bias current for the JFET. By adjusting the V_{sss} voltage, this current can be controlled externally. A typical bias current value is 300 µA. The voltage of the JFET gate terminal, coinciding with the SDD anode, is set during the reset period by turning on the reset diode integrated on SDD. Subsequently, during the period in which the signal and the leakage are integrated, this node works as a virtual ground due to the effect of negative feedback, so its voltage remains almost unchanged. The JFET is therefore biased at constant

gate voltage and current. Consequently, the source node will follow the gate voltage as the JFET is in the source-follower configuration. Thanks to the high impedance at the drain terminal of M_G, which works in saturation regime, the voltage at the node IN does not significantly influence the bias current value as long as it is able to guarantee saturation regime the nMOS transistor. The C_{AC} capacitor introduces an AC-coupling in the feedback loop, thus allowing an independent biasing of IN node and the negative terminal of the OTA. The OTA implemented in the ETTORE V1 has the two types of architectures as anticipated before.

Standard one

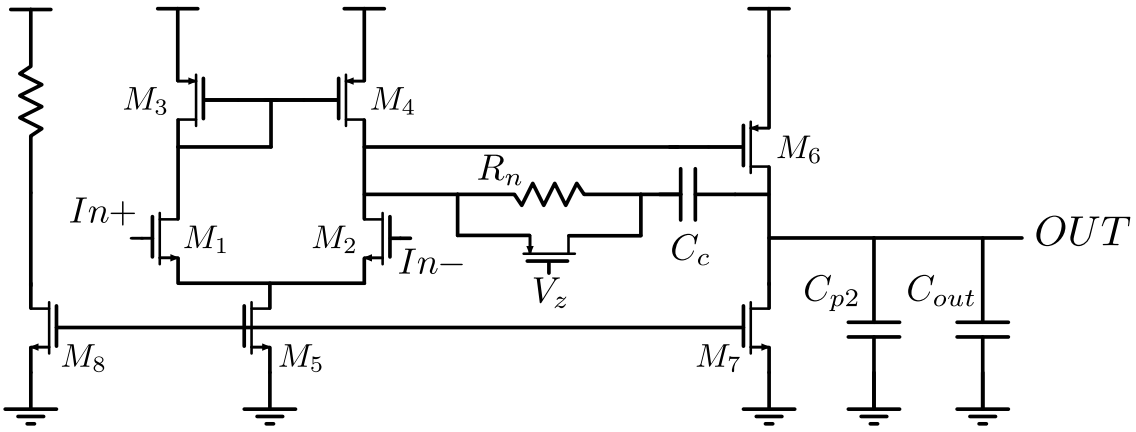


Figure 2.17: *Schematic of the OTA used in the standard preamplifier.*

Fig.2.17 shows the schematic of the OTA of a standard channel, which includes the capacitive output load C_{out} and a parasitic capacitance C_{p2}. In particular, C_{out}, with a value of around 30 pF, features the capacitance load on that node, and C_{p2} represents the capacitive coupling between the long traces of CF branch and the ground plane on the PCB, with maximum estimated value around 40 pF. It is a classical two-stage OTA: the input stage consists of a differential pair with pMOS current mirror load; the second stage is realized through a pMOS transistor in common source configuration. The biasing of the two stages is provided by a current mirror, originating from a reference branch biased by means of a 20 kΩ resistor. Besides, there are also additional transistors helping to cancel the bias currents during the channel power-off status. We can see them in fig.2.18. They

activate in the power-off status, when the OPAMP works as a buffer, to maintain the circuit stable. Basically, reducing the polarization current of the first stage, there is a reduction in the GBWP of the circuit, giving a more robust stability. This is achieved making a single MOS as the parallel of other two. Connecting one of the two directly to the supply, there is a reduction in the current of the equivalent MOS.

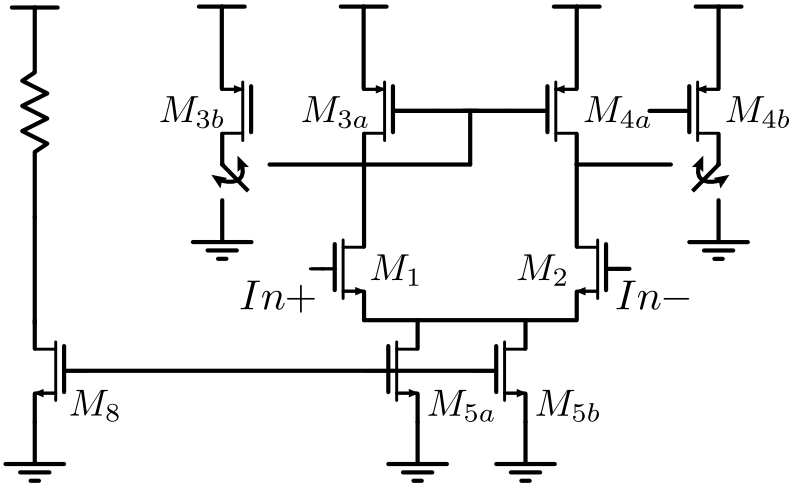


Figure 2.18: *Technique to reduce bias current during reset phase in the first stage of ETTORE.*

As is known, an amplifier of this type, if not compensated, presents a modulus of the transfer function with two dominant poles before the 0 dB crossing, behaviour caused by the parasitics at the output nodes of the first and the second stage. This can lead to the instability of the CSA feedback loop containing the OTA. The most common compensation technique, also used in this case, includes a compensation capacitor C_C between the output nodes of the two stages: in this way the poles are splitted, and through a correct selection of C_C and the design parameters of the amplifiers, it is possible to achieve only one pole before the GBWP frequency. However, the use of C_C also introduces a positive zero, which is detrimental to the phase margin. Therefore, by inserting a nulling resistor R_n, in series to C_C, it is possible to shift this zero even to the left half-plane of complex plane if $R_n > \frac{1}{gm_6}$, which can be used for improving the phase margin. To have a precise value of the resistance R_n, a pMOS transistor, used in the ohmic region and featuring an on-

state channel resistance $r_{ds,on}$, is paralleled to R_n. In this way the zero position is adjusted by acting on the gate voltage V_Z. Thus, the overall nulling resistance is: $R_Z = R_n//r_{ds,on}$.

Here are the main parameters [13]:

- **Total Gain**

$$A_0 = g_{m1}(r_{02}//r_{04}) \cdot g_{m6}(r_{06}//r_{07}) \tag{2.1}$$

- **GBWP**

$$GBWP = \frac{g_{m1}}{2\pi C_C} \tag{2.2}$$

- **Dominant Pole**

$$f_{p1} = \frac{1}{2\pi g_{m6}(r_{02}//r_{04})(r_{06}//r_{07})C_C} \tag{2.3}$$

- **Second Pole**

$$f_{p2} = \frac{g_{m6}}{2\pi(C_{p1} + C_{p2} + C_{out})} \tag{2.4}$$

  Where C_{p1} is the capacitive coupling between the long traces of IN branch and the ground plane on the PCB, featuring the output capacitance of the first stage.

- **Zero**

$$f_z = \frac{g_{m6}}{2\pi C_C(g_{m6}R_Z - 1)} \tag{2.5}$$

Fast one

The schematic of the OTA used in the fast channels is represented in fig.2.19. As we can see, contrary to the standard structure we have a first stage in a folded cascode configuration, a common source and then an Ahuja compensation using the capacitance C_C. The cascode configuration is used to reach an high gain using its

high output resistance, and the usage of C_C, C_{adv} and C_{sf} allow to stabilize the circuit having a good frequency response (around a 10 MHz closed loop pole).

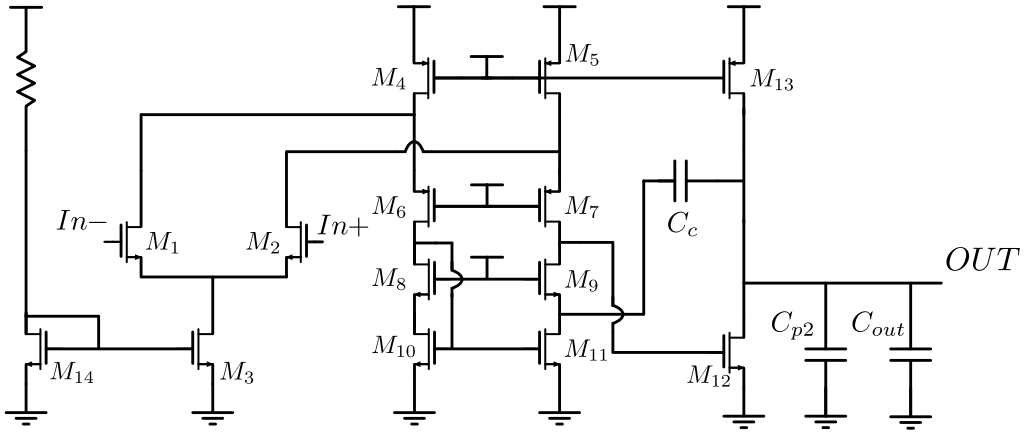


Figure 2.19: *Schematic of the OTA used in the optimized preamplifier.*

As before, the main FOM are:

- **Total Gain**

$$A_0 = g_{m1} \cdot [(g_{m9} r_{09} r_{011}) // (g_{m7} r_{07} r_{02})] \cdot g_{m12} (r_{012} // r_{013}) \tag{2.6}$$

- **GBWP**

$$GBWP = \frac{g_{m1} \cdot [(g_{m9} r_{09} r_{011}) // (g_{m7} r_{07} r_{02})]}{2\pi C_C (g_{m7} r_{07} r_{02})} \tag{2.7}$$

- **Dominant Pole**

$$f_{p1} = \frac{1}{2\pi C_C (g_{m7} r_{07} r_{02}) g_{m12} (r_{012} // r_{013})} \tag{2.8}$$

- **Second Pole**

$$f_{p2} = \frac{g_{m9}}{2\pi (C_{p2} + C_{out})} \tag{2.9}$$

- **Zero**

$$f_z = \frac{g_{m9}}{2\pi C_C} \tag{2.10}$$

2.2.3 Second Stage

The second stage is used to amplify the signals to mitigate the integral non linearity effect (INL) of the following ADCs that have to digitalize the incoming signals. In fact, if a portion of the signal is covered by more bits of the ADC, the INL effect has a minor impact [5]. However, there is the possibility to deactivate this amplification imposing the bit $SELECT\_PRE$ to 3.3 V. In this way the signal goes directly in a buffer stage that brings it directly to the bias board. To avoid the amplification of the signal due to the leakage current, leaving only the step-like ones, the second stage is AC coupled, as we can see in fig.2.20.

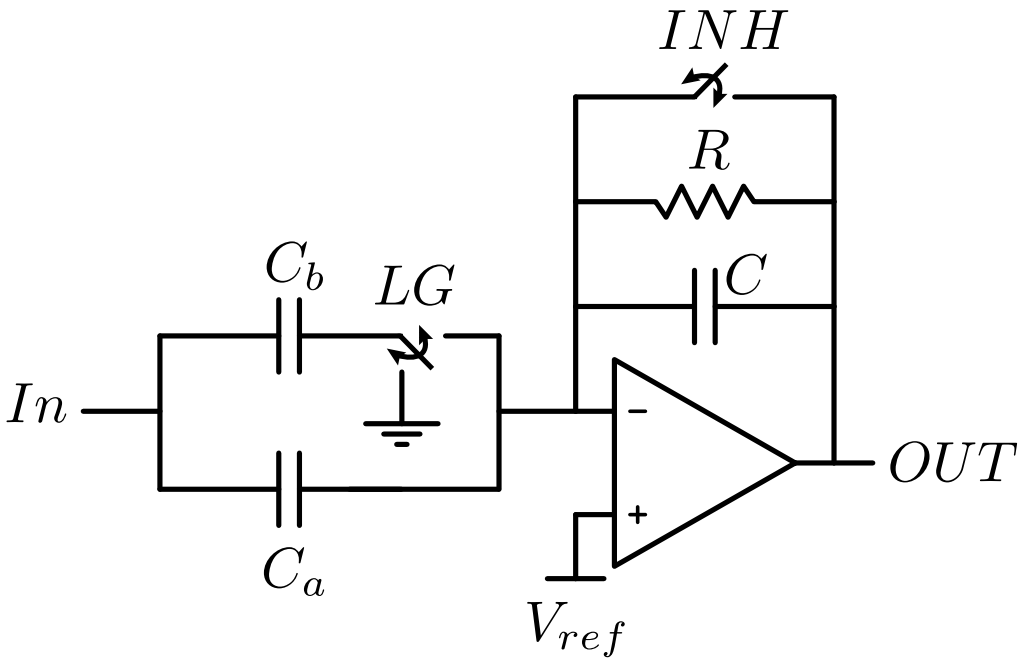


Figure 2.20: *ETTORE second stage schematics, with the presence of the LG bit, used to change the gain of the stage to optimize the dynamics, acting on the value of* C_a

V_{REF} is fixed to 2.7 V by the feedback loop. The transfer function is basically an high-pass filter, so with a step-like signal we find at the output a negative exponential (amplified), with its characteristic τ. This effect and the transfer function of the stage are represented in fig.2.21.

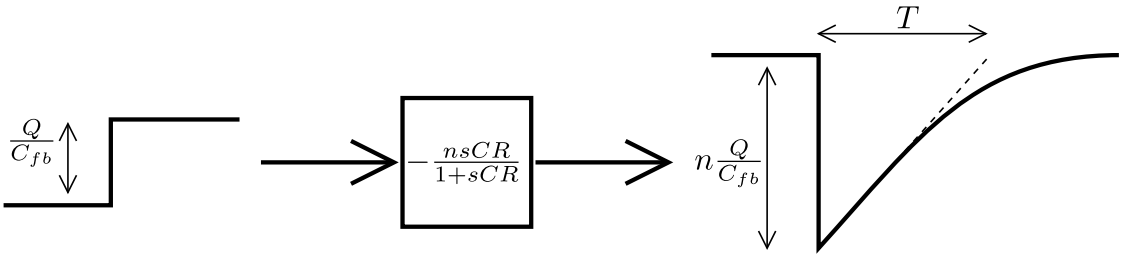


Figure 2.21: *ETTORE second stage effect and transfer function.*

2.3 KERBEROS and SFERA

The readout of the signals coming from ETTORE can be made essentially using two different possibilities. One is the commercial DANTE Digital Pulse Processor, developed by XGLab and used for the measurements in the chapter III. The other one is the custom KERBEROS DAQ, that integrates a custom ASIC developed by our laboratory, an ADC and a FPGA [14]. SFERA, the integrated ASIC, is an analog pulse processor, that is described in the following. KERBEROS is an analog data processor and acquisition platform, able to acquire 48 channels and transmit them via USB or via a D-sub connector. It is powered by a Xilinx Artix 7 FPGA (Field-Programmable Gate Array). All the 48 channels acquisition system is made in a modular fashion, in order to not only allow an easy repairability of the system, but making it even suitable for future upgrades and revisions. In fig.2.22 we can see an image of the complete system. The ADC used for the data conversion is the LTC2386-16 16-bit Successive Approssimation Register (SAR) ADC from Linear Technology. It is able to convert with a throughput of 10 Msps and provides the digital data via a fully differential serial interface. As we can see, both the FPGA module and the carriers for SFERA are made in a SODIMM connector style. This allows to connect or disconnect the modules in a very easy way, and to save a lot of space, thanks to the reduced size of this form factor. Moreover, this module can be operated with a single 3.3 V supply voltage, thus reducing the overall power distribution scheme. The area available on the carrier of SFERA allows its coverage by a metal RF shield by Wurth Electronics and the placement of the voltage regulators as close to the ASIC as possible, thus reducing the supply noise. A representation of the carrier board can be seen in fig.2.23.

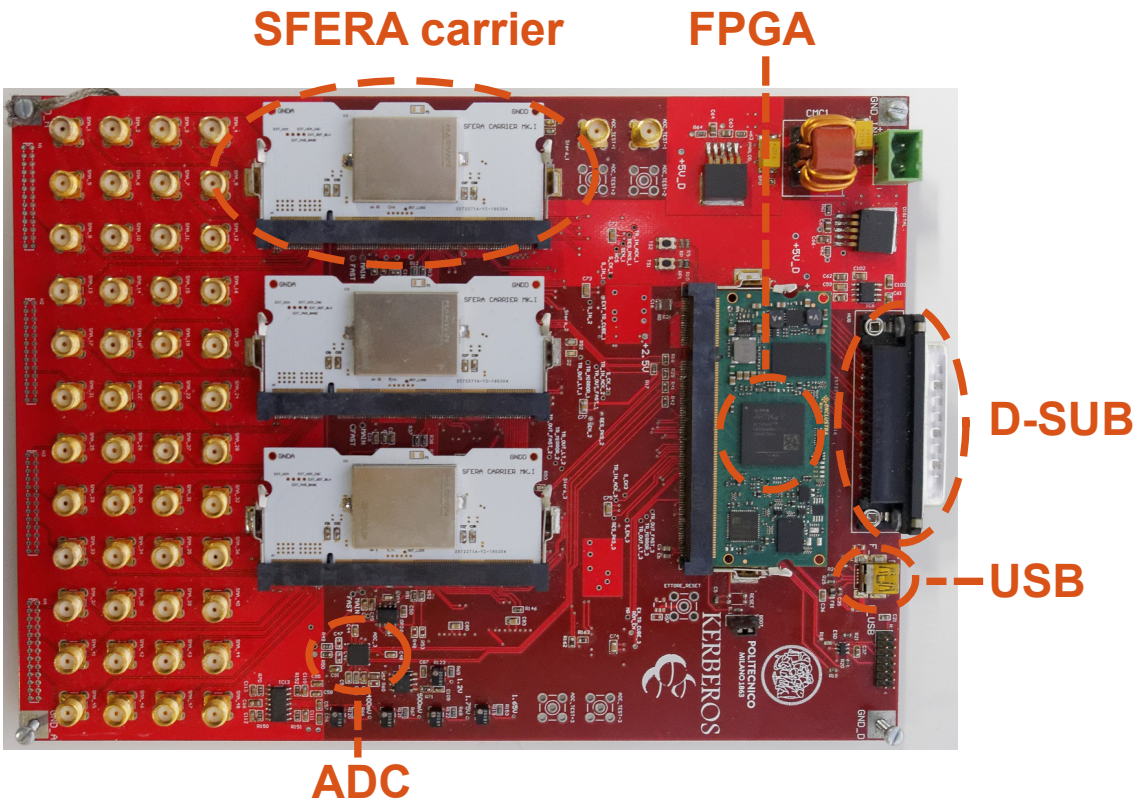


Figure 2.22: *Kerberos system.*

Figure 2.23: *Sfera carrier board.*

SFERA (SDDs Front-End Readout Asic) is a low-noise fully programmable 16-channel readout ASIC designed for both X- and γ-ray spectroscopy and imaging applications. The chip is designed to perform an analog pulse shaping of the signals coming from Silicon Drift Detectors (SDDs) and their charge sensitive amplifiers (CSAs). The idea of developing a general purpose readout front-end which is able, in principle, to meet a wide range of specifications for both X and γ-ray spectroscopy applications has been investigated and subsequently implemented in the design of SFERA. For this reason, SFERA has been adopted in conjunction of ETTORE for the TRISTAN experiment. The technology used is the AMS 0.35 µm 3.3 V CMOS C35B4 because of its excellent characteristics in terms of flicker noise, low cost and also because of the wealth of experience gained with it along the years inside the lab.

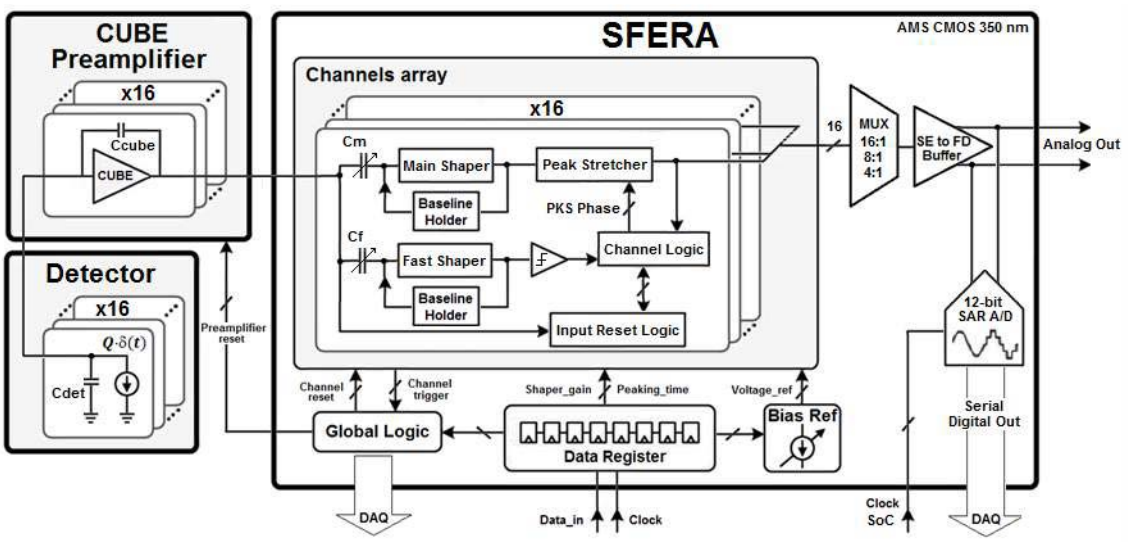


Figure 2.24: *SFERA's main schematic.*

The analog section of the chip, fig.2.24, comprehends 16 readout channels, each of which integrates a shaping amplifier, that will be referred to as main shaper, and an additional 9th order semi-Gaussian SA with the same peak-gains but fixed 200 ns peaking time (the fast shaper), designed to accomplish Pile-Up Rejection (PUR) purposes. Both main and fast shaping amplifier output baseline voltages are stabilized by baseline-holder (BLH) circuits. The main shaper is then followed by a three-phase peak-stretcher (PKS) and by some digital logic dedicated to the

PKS phases synchronization and to properly discard piled-up events. A digital logic section common to all channels (the global logic) is instead responsible for driving the output multiplexer (MUX) in all the different operational modes and furthermore for storing in a 256-bit SRAM internal data register, by means of an SPI (Serial Peripheral Interface) communication control interface, all the static programming bits needed by the Integrated Circuit (IC), used to select gain and peaking time, tune internal comparators thresholds, and to program voltage and current-references. The global logic manages all digital I/O signals from and to the IC, such as the channel comparators triggers, the multiplexer clock and enable, start and end-of-acquisition digital pulses and so on, providing a communication interface with the downstream Data Acquisition System (DAQ) based on integrated transceivers.

2.3.1 Shaping Amplifier

The shaping amplifier in SFERA can in practice be implemented using several circuit architectures. However, the 0.35 µm CMOS technology adopted for the IC does not allow a simple design of high-bandwidth operational amplifiers, required to synthesize the shortest peaking times or, alternatively, the highest poles frequencies. This is why the shaping filter topology of choice for SFERA has been the semi-Gaussian, a good compromise between the three main parameters: high throughput capabilities, ballistic deficit and energy resolution. The semi-Gaussian SA is a time-continuous causal filter, with a response that approximate the one of an ideal gaussian shape, using a 9-th order polynomial transfer function.

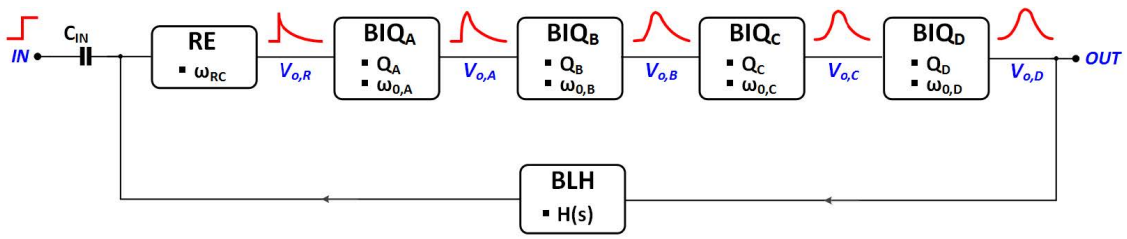


Figure 2.25: *Block diagram of the 9th order semi-Gaussian filter.*

The constrain on the high-throughput capability refers to the pile-up probability which, given a certain input photons rate, decreases with the width of the filter output shaped-pulses. A 9th order semi-Gaussian complex-conjugate poles (CPX)

shaper potentially offers the best performance thanks both to its higher pulse symmetry and lower width around the peak. The ballistic deficit is a phenomenon where given a certain input photon energy, the spectrum energy peak measured is lower than expected due to the non-zero charge collection time at the electrode. This effect relies on the finite drift time of the photo-generated charge travelling towards the SDD anode electrode. Since the electrons cloud is spread in time, the distribution of them can be considered as uniform, and the same is what happens when incident photons are detected far from the SDD's anode. The distance of an event affect the detection, in particular the drift time and the charge collection time. Finally, comparing energy resolution performance offered by different shaping amplifiers topologies, it emerges that the CPX shapers (especially the 7th and 9th order) represent the best candidate for low-noise applications. Taking into account the higher performance both in terms of pile-up immunity, low ballistic deficit and energy-resolution, the analog shaping amplifier that was chosen for SFERA readout channels is the 9th order complex-conjugate poles filter. Nevertheless, it is worth noting that this filter topology typically does not ensure the best power consumption performance because of the high number of filtering stages required to synthesize the 9 poles. Since no strict power constrains have been outlined for the design, allocating an extra power budget for the analog section of the ASIC did not represent a critical choice. As illustrated in fig.2.25, the filter was implemented cascading a real stage (RE), that introduces the real pole of the transfer function, and four biquadratic (BIQ) cells, responsible for one complex-conjugate poles pair each. The real stage, shown in fig2.26 is realized as a single-pole transimpedance active filter with an input AC coupling capacitor (C_{IN}) to cut-off the pre-amplifier output ramp due to the detector leakage integration. Instead for the complex conjugate poles, the design choice have been the multi-feedback cell, MFB or Rauch cell, which is a bi-quadratic cell preferred to Sallen-Key for its insensibility to mismatches. Tuning the filters is possible to set different peaking times (500 ns, 1 µs, 2 µs, 3 µs, 4 µs, 6 µs), for the different applications, and to set the filter gain, in order to be able to handle different input energy (E_{in}) and dynamic ranges (DR).

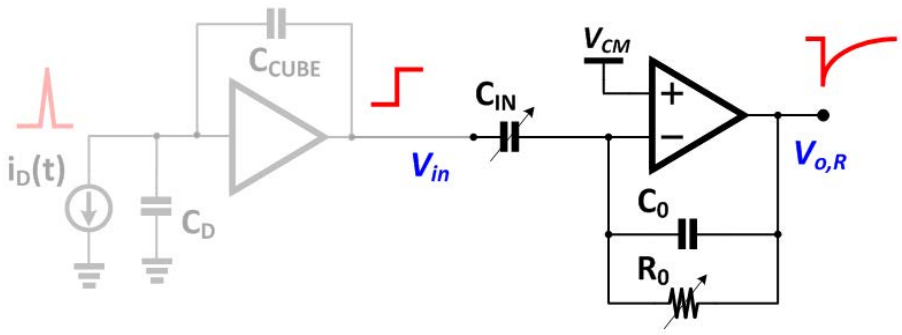


Figure 2.26: *Real stage of SFERA shaping amplifier at the output of a generic pre-amplifier.*

2.3.2 Baseline Holder

The baseline-holder (BLH), as already anticipated, has the task to stabilize the SA DC output voltage baseline to a constant value, set to 500 mV. Process, voltage and temperature (PVT) variations are mitigated by its negative feedback operation, reacting on the real-stage OTA virtual ground. Furthermore, as later addresses, the BLH also avoid the output baseline to shift in case of high input photons rates. The general architecture of the circuit is the one introduce by De Geronimo et al. in [15]. Under a small-signal analysis perspective, the BLH operates as a low-pass filter, cutting the SA input DC current components and leaving almost unchanged its input-current to output-voltage transfer function at higher frequencies, as shown in fig.2.27.

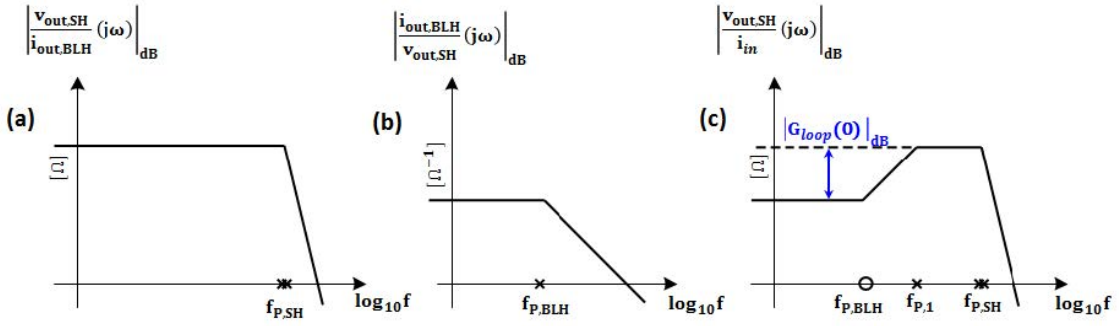


Figure 2.27: *Input-current to output-voltage transfer function of the SA alone (a), input-voltage to output-current transfer function of the BLH (b) and input-current to output-voltage transfer function of the joint SA and BLH system (c).*

The DC loop gain Gloop(0) should be high enough to keep the output voltage-baseline deviation within few mV from its nominal value, but anyway limited to ensure stability. If too high, indeed, the closed-loop pole frequency $f_{P,1} = f_{P,BLH} \cdot Gloop(0)$ would fall close to the SA poles cut-off frequencies thus degrading the phase-margin of the system.

2.3.3 Peak Detector and Pile-up rejection circuit topology

Once an input event has been processed and properly shaped by the analog SA, the peak amplitude of the semi-Gaussian output pulse has to be sampled and then multiplexed before being digitized by the off-chip DAQ system, fig.2.28.

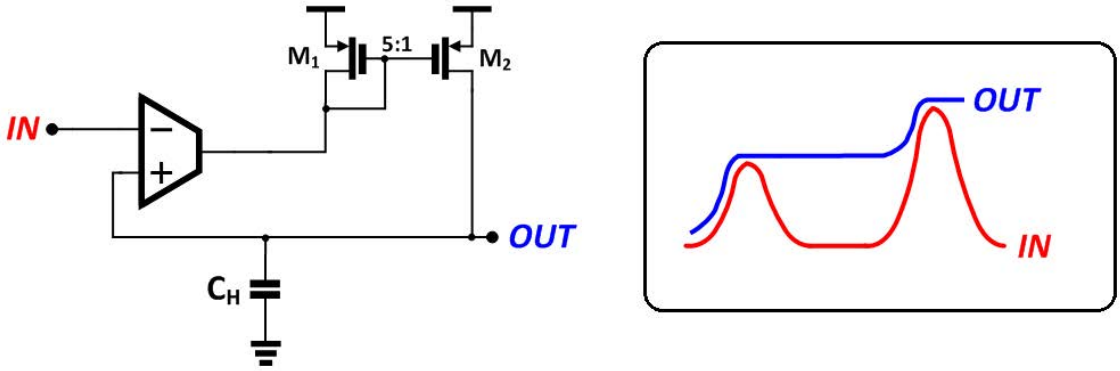


Figure 2.28: *Peak Stretcher in SFERA, pulse-peak holding operation.*

Input events "too" close in time may generate pile-up, corrupting the SA output-pulse peak-amplitude and therefore degrading the spectroscopic performance of the front-end. The higher the event count-rate the more likely to occur pile-up. To overcome this problem, a dedicated logic has been implemented, to detect the peaks of each shaped input and discard events if too close to each other. An effective solution, adopted for SFERA comprises a 3-phase PKS driven by the Pile-Up Rejector(PUR) logic control-signals. The main idea is to start an inspection window whenever an event is detected, and if no other photons are detected during such inspection window, the original event is then properly acquired. In case, instead, one or more additional photons hit the detector during the window, the PKS promptly discards the piled-up SA output pulse, by not stretching its peak, and becomes ready again to track a next pulse. The 3-phase PKS architecture that has been adopted for the

design of SFERA includes the read (RD), write (WR) and track (TRK) phase. The final circuit implementation is shown in the schematic diagram of fig.2.29, while the control signal are explained in fig.2.30.

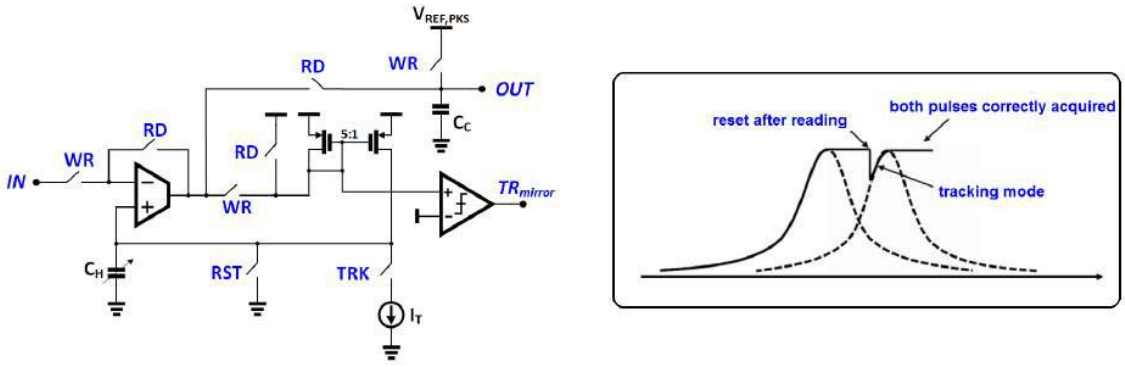


Figure 2.29: *Three phase PKS circuit implementation (right), and its working principle (left).*

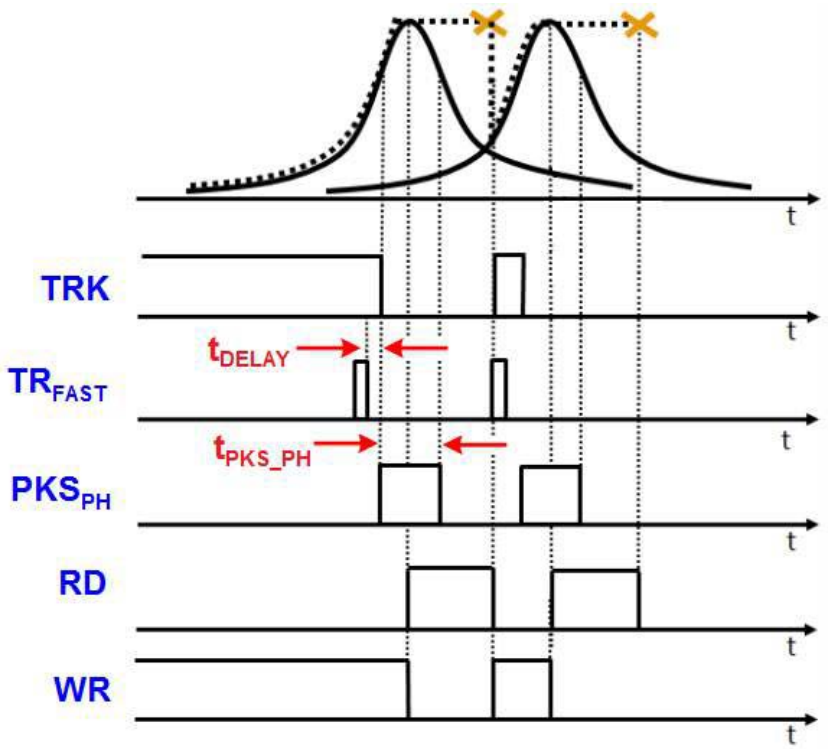


Figure 2.30: *Three phase PKS circuit control signals.*

During the tracking phase both the TRK and WR switches are closed, allowing the system to follow the input, being in a buffer configuration. A dedicated digital logic triggered by the falling edge of TR_{FAST} starts the time coincidence window after a certain t_{DELAY} . If during this interval no other event occurs then the peak can be correctly sampled, otherwise peak is discarded (pile-up has occurred). During the write phase the value of the peak is stored in a capacitor, and during the read obviously it remains untouched. This is the value that is stretched, sampled and multiplexed to the output, and at the end of this phase the PKS must be reset and brought to the tracking phase. The digital logic responsible for the proper synchronization of PKS phases (TRK, WR and RD signals generation) operates jointly to the PUR logic, which basically prevents the PKS to switch from write to read by inhibiting the PKS signal generation in case of pile-up. The PUR section is designed to discard two events if they are too close in time. Its representation is present in fig.2.31.

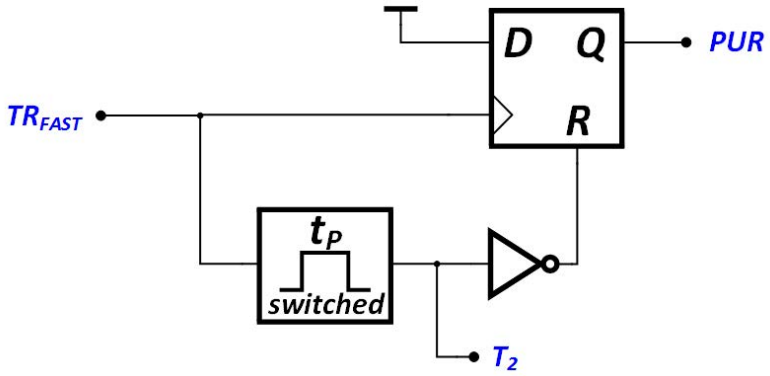


Figure 2.31: *Pile-up rejector schematic.*

Then the analog stretched values from the PKS are fed into an analog multiplexer (MUX) and then subsequently buffered by two single-ended to fully differential output buffers. The multiplexer is organized in such way that output data can be multiplexed in a 16:1 as well as 8:2, 8:1, 4:2 and 4:1 configuration, depending on the target application and according to static programming bits.

2.3.4 Modes of Operation

SFERA has three differents modes of operation, which exploit different data multiplexing strategies: polling-X, polling-γ (or burst mode) and sparse readout(or Siddharta-like). In the first one, the multiplexer performs a fast continuous readout of all the channels in sequential manner. The polling-γ operational mode triggers when an event triggers the detector, such that the MUX sequentially brings out the sampled output voltage-peaks of all the 16 shapers. Finally the sparse readout implements a FIFO data buffer to store each single event as it is detected, as well as the address of the channel where it took place.

Polling X

In the polling-X multiplexing strategy, particularly suitable for high-throughput X-ray applications, the MUX operates a fast sequential readout of the PKS outputs, which is asynchronous and uncorrelated from any peak detection and pile-up rejection operation taking place upstream.

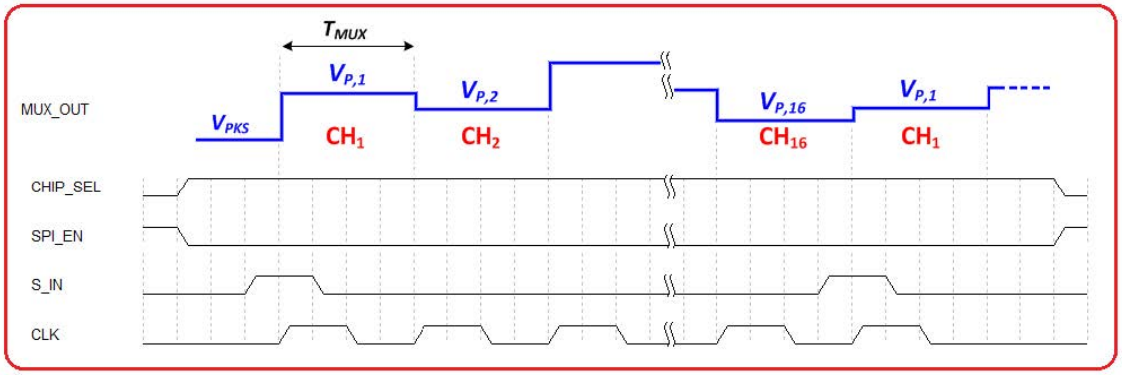


Figure 2.32: *Polling-X readout control signals digital patterns.*

The ASIC-DAQ interface basically consists of four digital signals (S_IN, CLK, $CHIP\_SEL$ and SPI_EN) and the buffers analog output (which is connected to MUX_OUT), as shown in the timing diagram of fig.2.32. The polling-X SFERA MUX digital logic comprises a shift register (SR) in which a logic 1 is right-shifted on each rising edge of a clock signal (CLK) provided by the acquisition. The

S_IN signal, also generated by the external DAQ, is provided to the MUX shift-register input after a number of clock pulses equal to the number of channels being multiplexed and is sampled on the CLK rising edge, so has to load a new logic 1 in such SR, thus giving rise to a new readout sequence. Two additional signals, namely $CHIP\_SEL$ and SPI_EN, are needed to enable some internal global circuitries and the MUX logic respectively.

Polling γ

The polling-γ multiplexing protocol is intended for the use of SFERA in γ-ray spectroscopy and imaging applications, where several detection modules, made of solid-state detectors coupled to monolithic crystal scintillators, need to be readout by multiple ASICs. This operational mode also exploits a sequential readout of all the ASIC 16 channels, that this time is instead synchronous to the event detection. When a γ-ray photon is absorbed by the crystal, the visible light emitted is spread with a certain distribution over the detection units , thus all the electronic readout channels have to be processed to properly reconstruct the γ-ray photon energy. The first SA among all the channels that detects a valid event, which means its output overcomes a voltage threshold typically set slightly above the 500 mV baseline in order to also record small amplitude signals, will generate a TR_OUT_LT pulse.

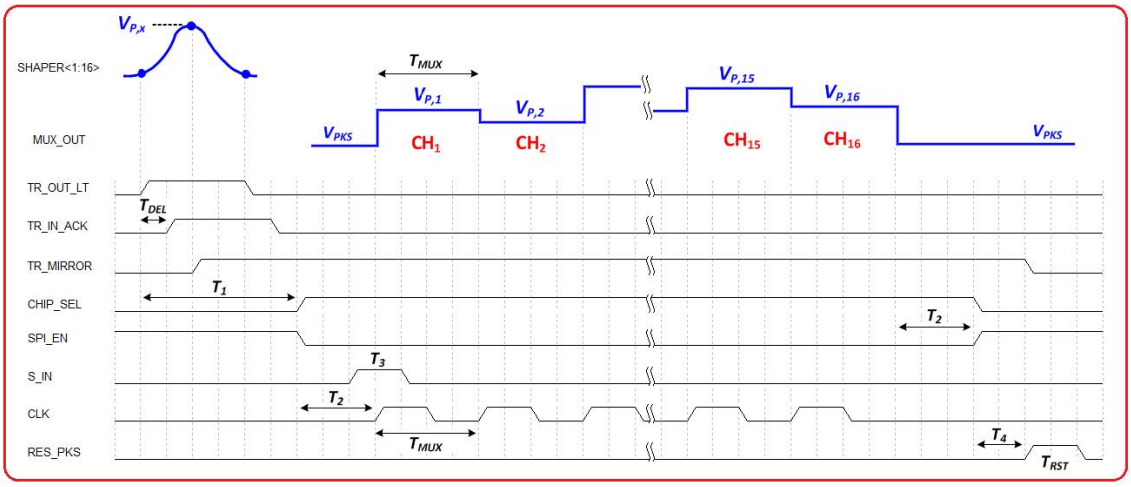


Figure 2.33: *Polling-γ readout control signals digital patterns.*

The TR_OUT_LT trigger is the logic OR of all the TR_MAIN signals produced by the main shapers output comparators. A summary of the waveforms digital patterns involved in the polling-γ 16:1 multiplexing protocol is shown in fig.2.33. Once a channel output shaped-pulse overcomes the aforementioned threshold first, the DAQ communicates to all the chips a TR_IN_ACK pulse to notify the reception of the TR_OUT_LT. Such TR_IN_ACK enables all the peak stretchers to switch from the write to the read phase, giving rise to the TR_MIRROR signal (the logic OR of all the $TR\_MIRRORs$). The latter will remain high until a reset pulse (RES_PKS) is provided at the end of the acquisition. S_IN and CLK signals accomplish the same operation described for the polling-X multiplexing, with the difference that only a single train of clock pulses is provided for each detected event.

Sparse

The sparse readout mode matches the requirement of the TRISTAN experiment, in which only those channels detecting an event need to be output multiplexed. As a matter of fact, is necessary to know the exact times in which each event is triggered, to study the backscattering of electrons on the detector.

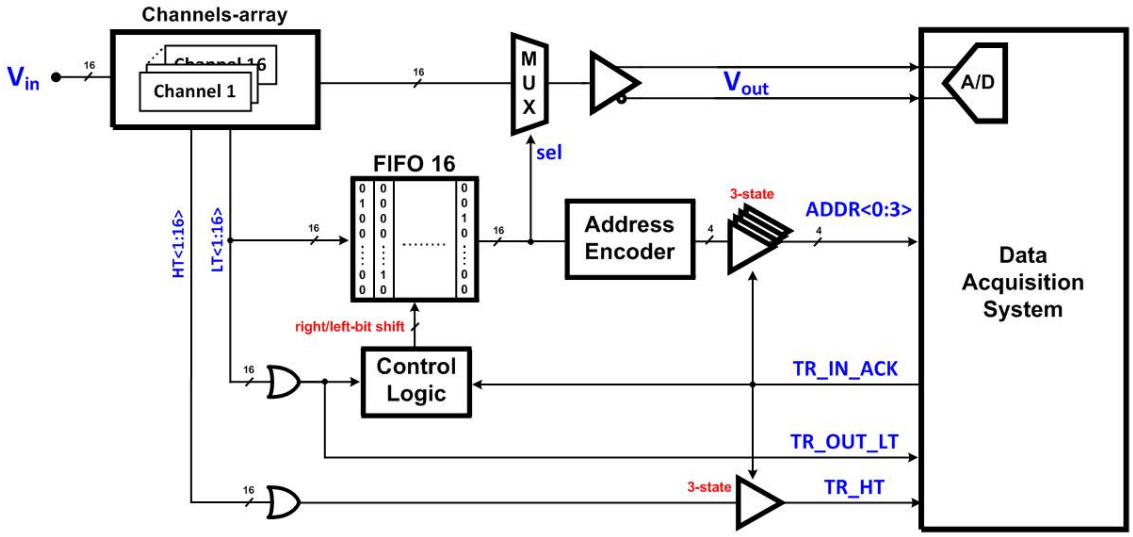


Figure 2.34: *Sparse digital logic block diagram and interface with the DAQ.*

A dedicated digital logic, whose simplified block diagram is shown in fig.2.34, manages the data transfer to the downstream DAQ system, synchronously providing it both the "firing channels" addresses and related stretched pulse-peaks in the same time order the events are detected. In this operational mode, once an electron hits the detector, the arrival is communicated to the data acquisition system by the TR_OUT_LT signal, which is the logic OR of all the TR_{MIRROR} triggers coming from the channel peak-stretchers and indicated with $LT < 1 : 16 >$ (which stands for "low threshold trigger") in the picture. The use of a FIFO multi-bit register accomplishes a dual purpose: implementing the sparsification of events by simultaneously providing the channel address both to the external DAQ and to the analog MUX (using it as selection line), thus ensuring the synchronism with the associated analog output value. The second function is managing high-rate event bursts: as seen in fig.2.35, in the case of multiple events happening in different channels of the chip, at a time distance shorter than the multiplexing time, is possible to record all of them. The peaks and the address are stored into the FIFO queue and shifted-out at a lower speed, allowing the DAQ to properly digitize the related MUX outputs one after the other (fig.2.35). An TR_HT trigger, which is the logic OR of the single channels TR_HT signals and indicated with $HT < 1 : 16 >$ in fig.2.34, is also provided to inform the DAQ about events exceeding the energy range.

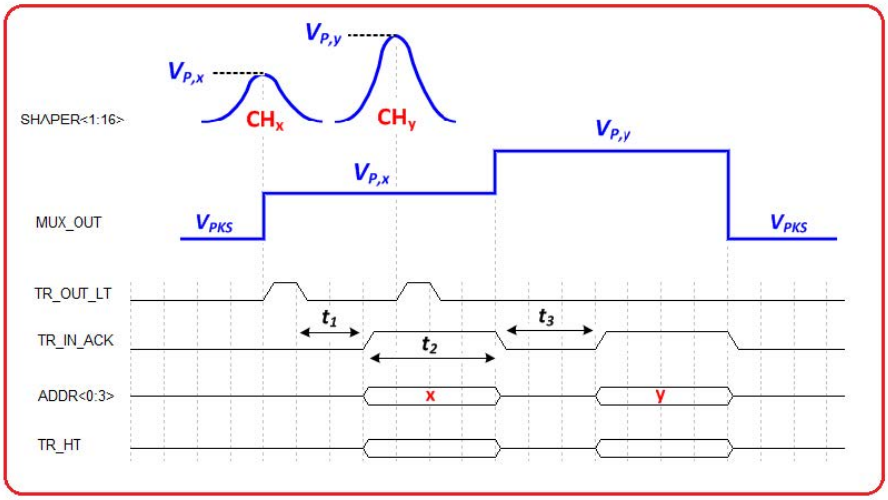


Figure 2.35: *Sparse readout control signals digital patterns.*

3 | 12 and 47-pixel Experimental Characterization

In this chapter we present the characterization of the first 12 and 47-pixel detectors created by MPG-HLL. Along with a description of the two setups, some real photos are provided, and the results achieved in terms of energy resolution.

3.1 Overview of the 12-pixel setup

The full setup is represented in fig.3.1 and in fig.3.2 and it is composed by:

- **Detector Board**, in which it is present our 12-pixel SDD, bonded on a custom PCB with filters and a PT100 sensor;
- **ASIC Board**, connected to the detector's one thanks to a 200-pin connector developed by Samtec. On this board the ETTORE ASIC is mounted, along with filters and voltage regulators;
- **Bias Board**, developed by XGLab, that generates the polarization voltages for the SDDs, the bias and the control bits for the ASIC and allows the correct read-out of the signals thanks to ouput buffers;
- **DANTE DPP**, Digital Pulse Processor, designed for X-ray spectroscopy application by XGLab. It implements a trapezoidal shaping.

All the following PCBs have lead-free solders, because the experiment needs to meet UHV (Ultra High Vacuum) specifications, around 10^{-8} mbar. To reach this vacuum level it is required the use of special materials and various pumping stages. Seals and gaskets used in the UHV system should prevent even minor leaks of any sort. Almost all of these seals are made of metallic materials with knife-edges on both sides cutting into a soft gasket, typically copper. These all-metal seals can maintain integrity to UHV ranges. The materials used in UHV condition need to

stand heating at more than 120 °C for many hours/ days and it should not have an high vapor pressure. So, it is not possible to use common materials, like plastics, glue (screws are used instead) and lead (for the soldering).

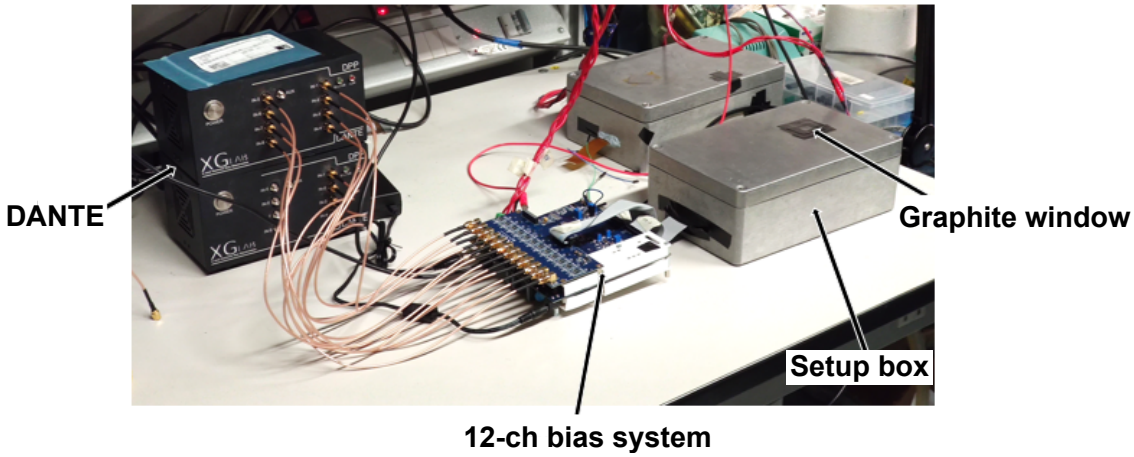


Figure 3.1: *Full setup for the 12 pixels detector.*

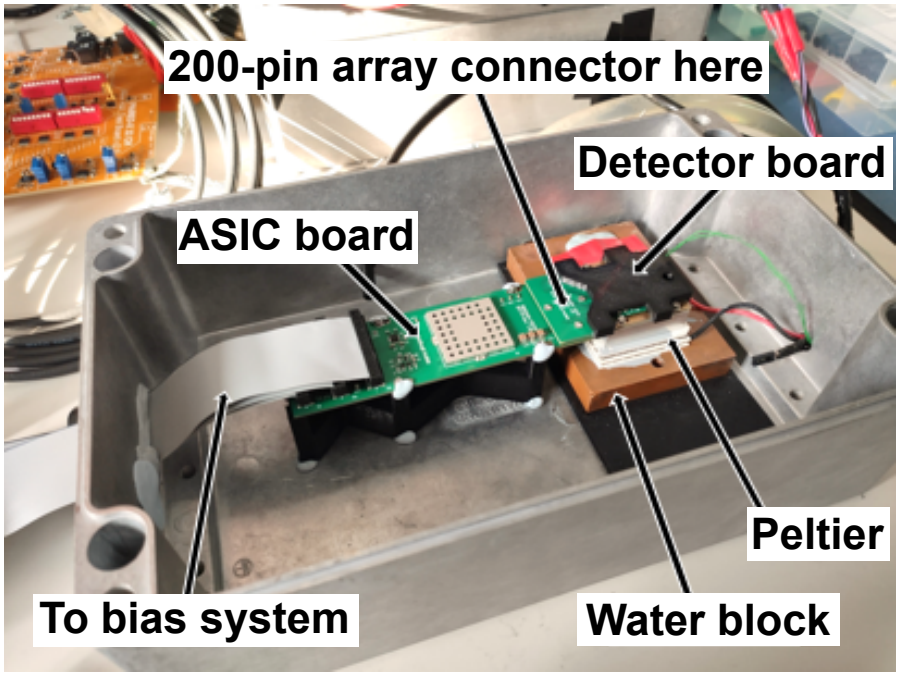


Figure 3.2: *Particular of the setup for the 12 pixels detector, inside the setup box.*

3.1.1 Detector Board

A representation of the Bonded Detector Board is shown in fig.3.3. The dimensions are 35 mm x 55 mm.

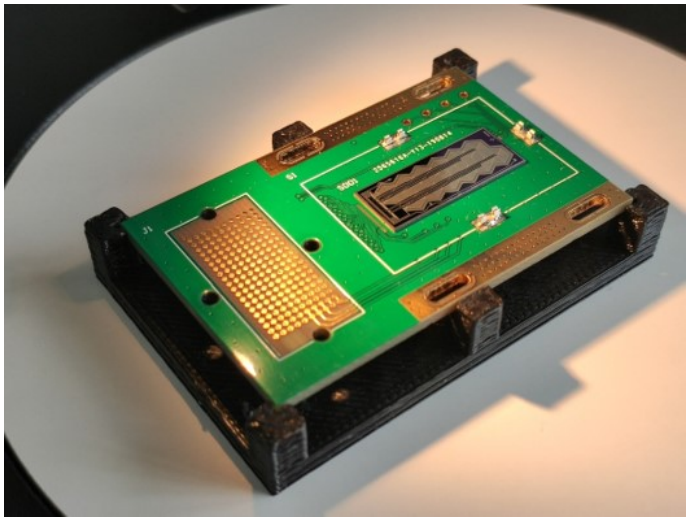


Figure 3.3: *12 pixels Detector Board.*

The polarization voltages for the SDDs come from the ASIC board thanks to the Samtec connector. The choice of a 200-pin connector having 4 cm of space is not trivial and the choice is justified by the fact that it does not require any kind of solders, increasing the UHV compatibility and reducing failure's risks. However, the alignment of the pins requires more caution. This voltages are all filtered using RC networks to avoid additional noises. The pads for each pixel which are connected to the corresponding channel of ETTORE are basically two: IN and CF. They are the source contact of the integrated JFET and the terminal of the feedback capacitor. In fig.3.4 there is a simple representation of these connections.

The total bondings for this board are 39, 2 for what regards the top part, 37 for the bottom one. In this number there are present the 24 pads for the IN and CF contacts of all the 12 channels, along with the ones for the correct biasing of the JFET and 4 additional ones for a test JFET made with the same technology of the integrated one. There is a hole in the PCB board to allow the X-rays or electrons to reach the entrance window of the SDD, with an outline that have enough space to glue the detector on site. A representation of the physical bonding is in fig.3.5.

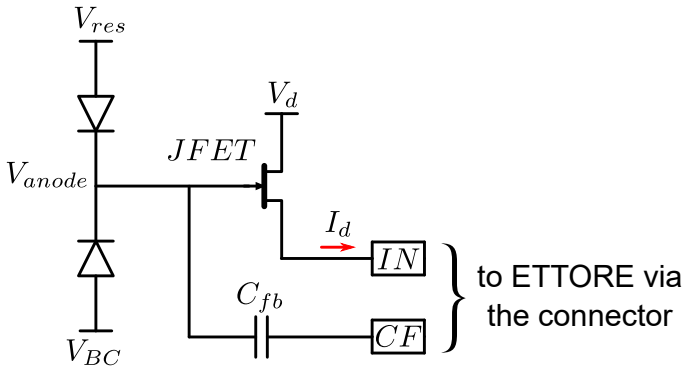


Figure 3.4: *IN and CF pads of the 12 pixels Detector Board.*

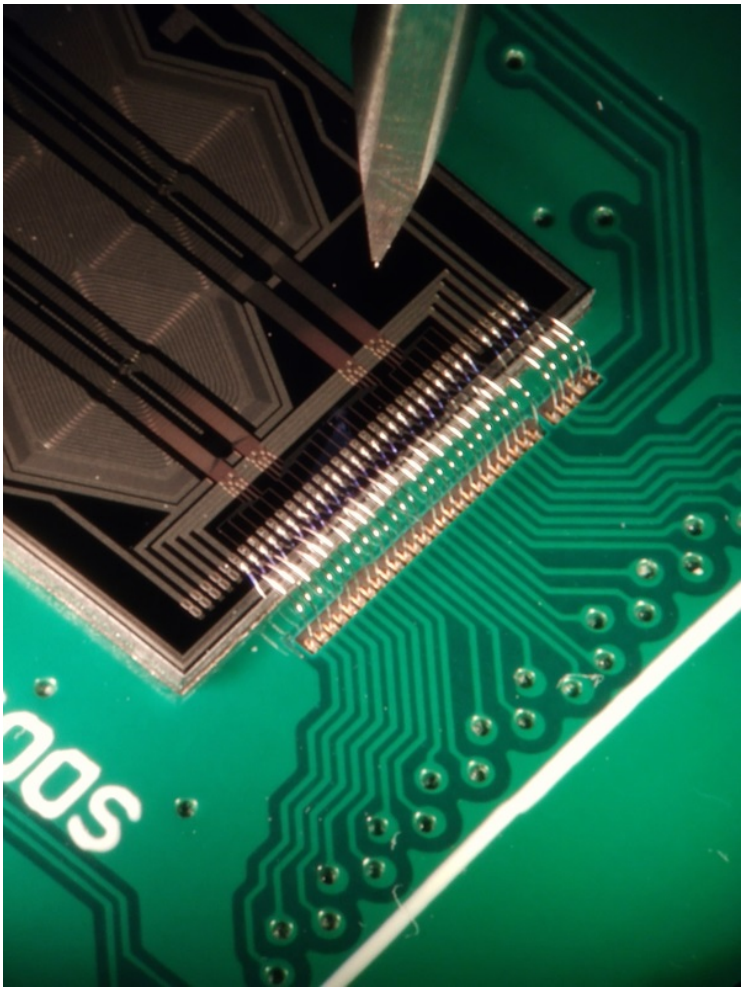


Figure 3.5: *Real bonding detail of the 12-pixel detector.*

An aluminum block is used to connect the Peltier module with this board, in order to cool it down and to have the possibility to perform tests at a temperature of $-38°$ Celsius. Its U-shape, seen in fig.3.6, is useful in terms of space for the components and the bondings. The cooling efficacy is improved thanks to the opening of the solder mask in correspondence of the contact area with the aluminum u-block. A lot of vias are present to decrease the thermal resistance of the PCB layers.

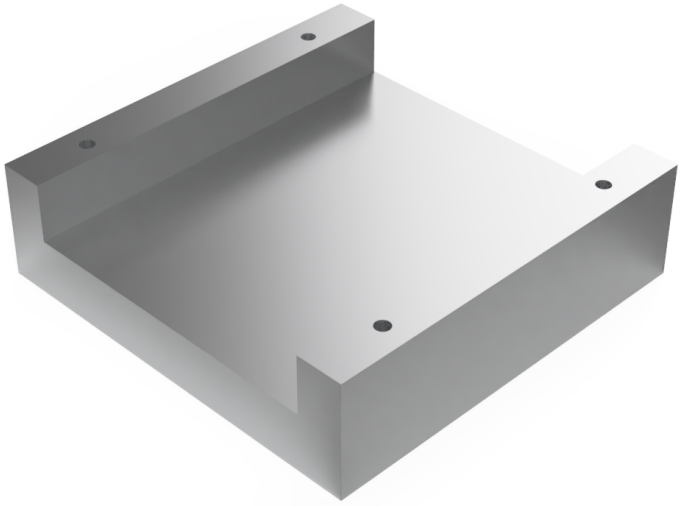


Figure 3.6: *Aluminum block utilized for the cooling of the detector board.*

3.1.2 ASIC Board

The ASIC board is shown in fig.3.7, with a dimension of 35 mm x 120 mm. The ETTORE ASIC is shown in detail in fig.3.8, bonded to 56 pads on the PCB. The body of ETTORE is fixed to the board thanks to an epoxy resin thermally cured. To avoid the accidental damage of the bonding wires during the handling, the ASIC was covered with a special squared metallic case. The voltages necessary for the operation of the ASIC (the power supplies, the static bits and the reset signal) come from the bias board, where they are filtered by RC networks. Also the voltages for the detectors are provided by the bias board: they pass through the ASIC board, where they are properly filtered, and continue to the detector board. The outputs of the ASIC are sent to the bias board. ETTORE is a chip able to sustain 12 channels at the same time, so with our detector having 12 pixels, all the channels were used.

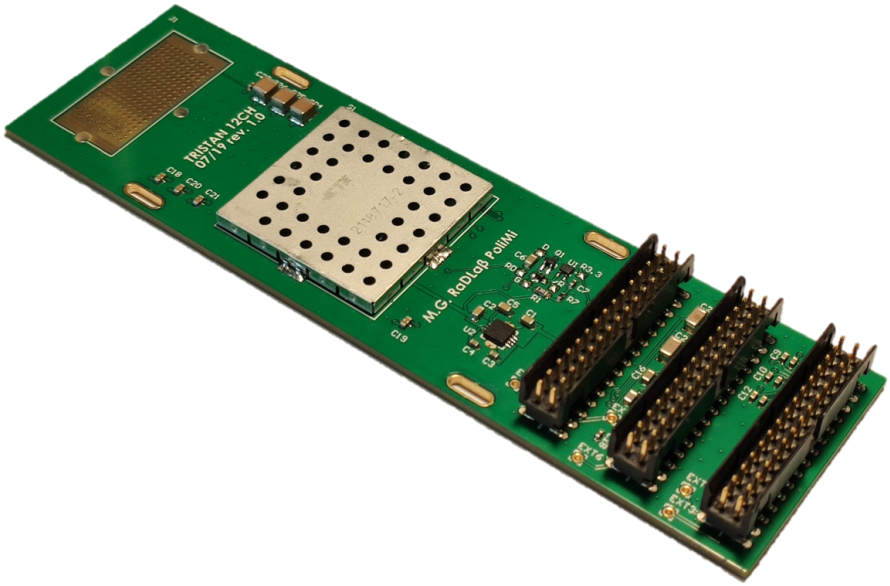


Figure 3.7: *12 pixels ASIC board.*

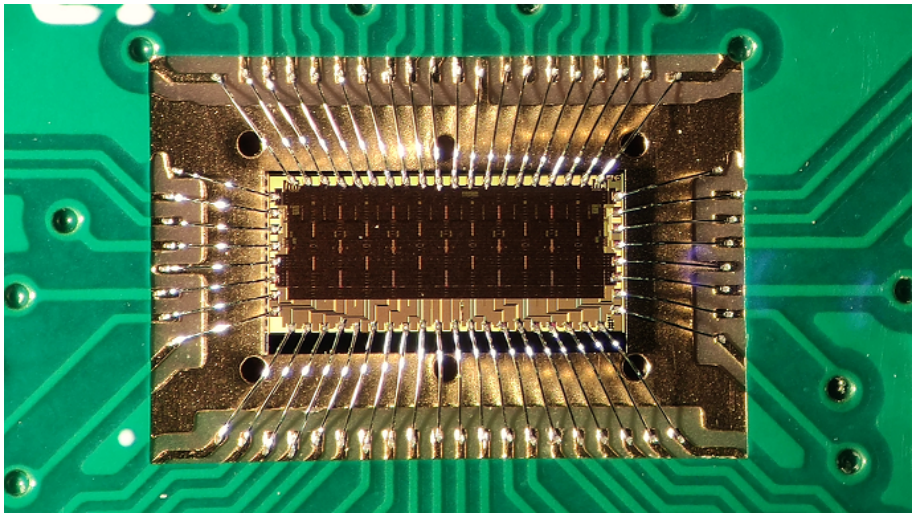


Figure 3.8: *ETTORE bonded on the 12-ch ASIC board.*

To avoid as much as possible the capacitive coupling, all the routing of different signals are divided by ground planes and pours, present in every layer of this PCB.

In fig.3.9 is reported a simplified schematics of the routing of the signals between the ASIC board and the connectors to the other PCBs. Only the significant signals are here represented, which are IN, CF and OUT.

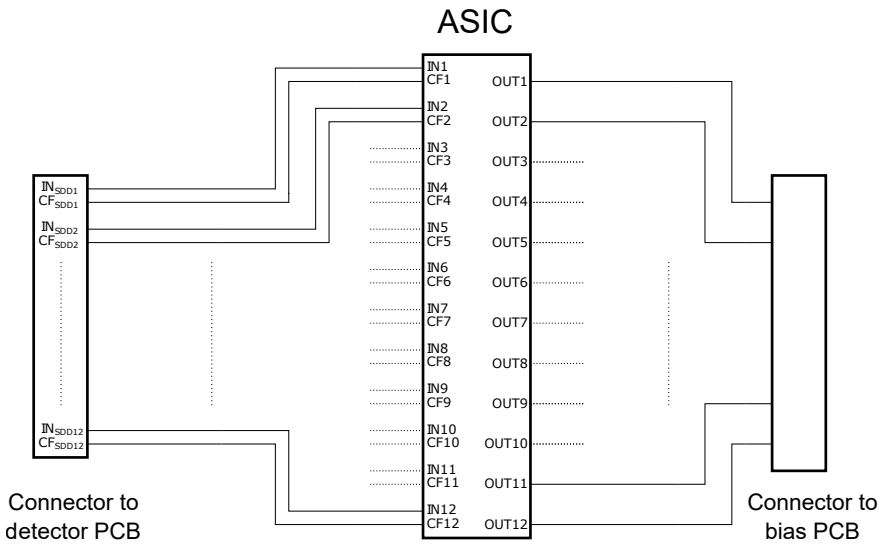


Figure 3.9: *Routing of significant signal tracks in the 12 channels ASIC board.*

There are present four screw holes to allow the connection with a plastic holder printed in our laboratory, for mechanical support. In addition a voltage regulator 3.3 V 600 mA for the ASIC and a switched reset filter, for the filtering of the reset signal going to the SDD, are on the board. While the former is used for the correct functionality of the ETTORE chip, the latter filters the reset signal, using a capacitor, during the working phase of the detector.

The ASIC board, as anticipated, is connected to the detector board through a commercial connector, made by Samtec. It was chosen thanks to its features of compactness, reliability and adequate number of pins. In addition it allowed the swap of different detectors in the setup, since it offered both the backward compatibility with older pixels (simply using fewer channels of the ASIC and a different detector board) and the forward one with the 47-channel detector, resulting in nearly no additional work on the setup. We can see it's 3D model in fig.3.10. The connections to the bias system are made through a three 30-pin flat cables, mating exactly to the connectors of the bias board, with a 1:1 correspondence on each signal.

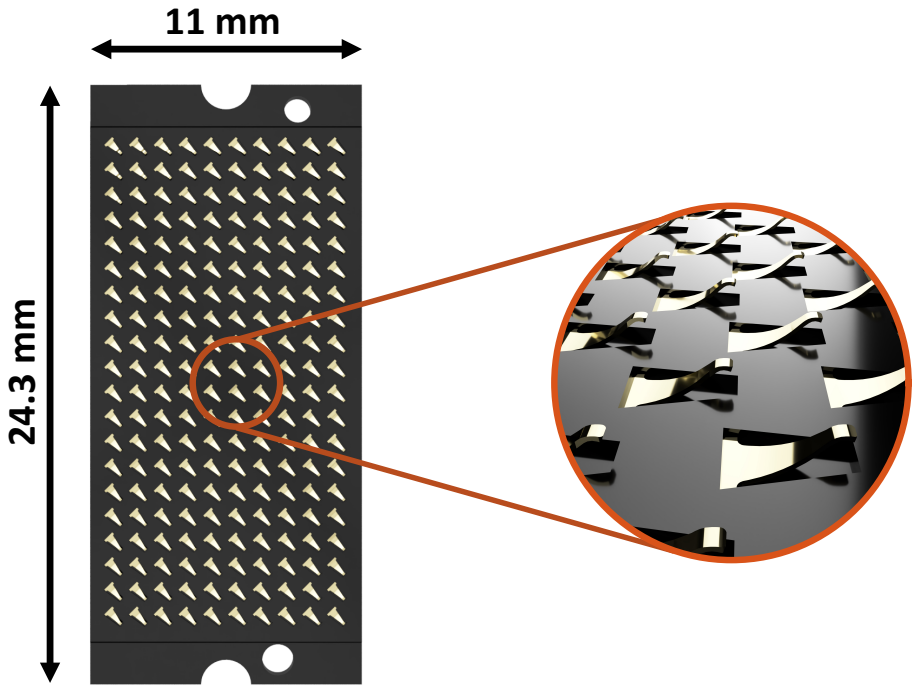


Figure 3.10: *Samtec connector.*

3.1.3 Bias Board

Fig.3.11 shows the bias board, which is designed in collaboration with XGLab. As anticipated its main functions are to provide the bias voltages and reset signals to the SDDs and the ETTORE ASICs. The power supply used for this board is a 24 V bench top power supply, and thanks to its internal DC/DC converters it generates all the voltages needed for the biasing of the detector, $HV, B_F, B_C, V_{SSS}, V_D, IGR, R_1, R_X$ and the ones needed by the ASICs boards. Moreover, it is possible to make a manual adjustment of these voltages by using the resistive trimmers on the bias board.

In regard to the generation of the reset inputs on the detector and on the ASIC, there are three different sources that can be used:

Reset given by the ASIC

As it is described in chapter II, when one channel of ETTORE reach its saturation point (V_{TH}) it is generated a positive pulse, that reaches the bias board. After that, the bias board generates two different reset signals, one for the ASIC and one for

the SDD. These two signals are synchronized and their length is adjustable thanks to resistive trimmers. The voltages for the reset pulse of the detector are trimmable between $-15\,\mathrm{V}$ and $5\,\mathrm{V}$;

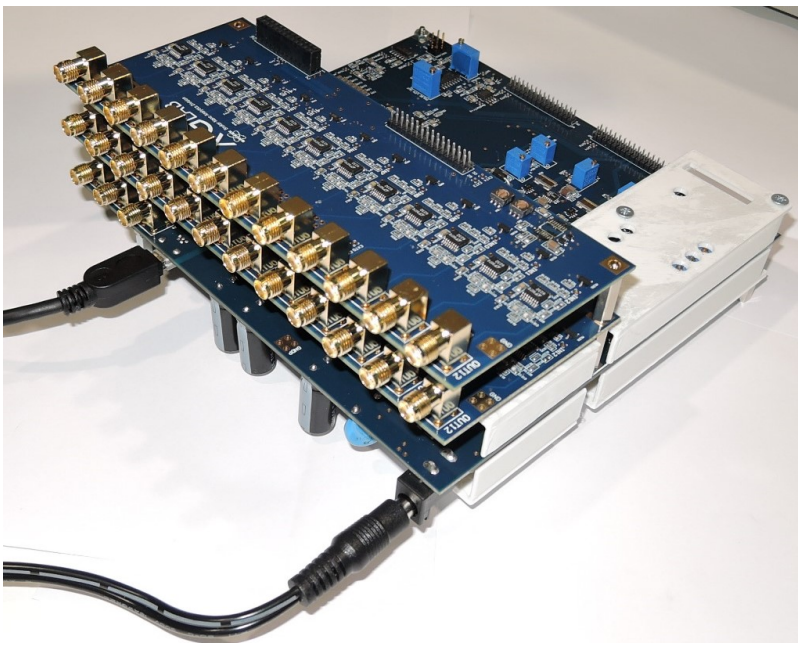


Figure 3.11: *Bias Board developed by XGLab.*

Periodic Reset

On the bias board is present an oscillator that gives the possibility to have a periodic reset. Its frequency depends on the values of resistance and capacitance of the components connected on the astable circuit of the oscillator it is set with a default period of $2\,\mathrm{ms}$. To deactivate or activate this periodic reset (that is the default one active on this board) a jumper have to be connected/disconnected;

External Reset

Thanks to an SMA connector, it is possible to provide an external reset signal using a signal generator. For the following measurements this is the reset mode that has been used.

Using a custom software GUI is is possible to check and adjust additional parameters without acting on the hardware:

- Activate or deactivate the High Voltage part of the Circuit (HV), and all the detector voltages derived from that;
- Check the temperature of the system thanks to a temperature monitor;
- Activate or kill specific ETTORE channels;
- Set the ASIC references voltages and static bits;
- Monitor the SDD's JFET current.

On the bias board all the ETTORE output signals are amplified by a factor of 2 to make negligible the noise introduced by the following circuits. We can see the model of the amplifying stage on fig.3.12.

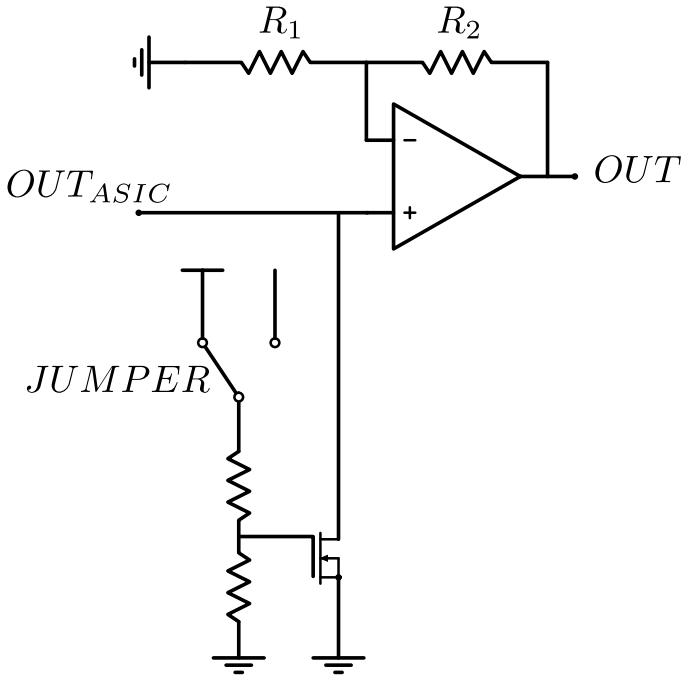


Figure 3.12: *Amplifying stage and channel killing mechanism used for each channel on the bias system.*

It's the classical non-inverting amplifier with the typical transfer function:

$$\frac{OUT}{OUT_{ASIC}} = 1 + \frac{R_2}{R_1} = 2$$

To set the baseline of the voltage OUT to adapt the dynamic of the signal with the one at the input of the DAQ, it is used the voltage OFFSET, that is adjustable using the GUI, thanks to a DAC. This is transferred at the OUTPUT with the following gain:

$$\frac{OUT}{OFFSET} = -\frac{R_2}{R_1} = -1$$

So we find at the output:

$$OUT = OUT_{ASIC} \cdot (1 + \frac{R_2}{R_1}) - OFFSET \cdot \frac{R_2}{R_1}$$

After being amplified, the signals are sent, using SMA connectors, to the DAQ system (DANTE) or KERBEROS.

3.1.4 DANTE DPP

The data acquisition system which has been used is named DANTE. It is a Digital Pulse Processor (DPP) produced by XGLab. Being the commercial system capable of reading 8 channels, for the following measurements a couple of them were used in a modular fashion. A photo of a single unit is shown in fig.3.13.

Figure 3.13: *8-channel DANTE DPP developed by XGLab.*

This acquisition system performs a 16-bit sampling and 125 MHz of the incoming waveform and, by means of a trapezoidal shape digital filtering, it allows to acquire the energy spectrum from the detector signals. DANTE is connected to the PC through USB connection: with a dedicated GUI, it is possible to set the filter parameters and acquire spectra or save raw waveforms. All the technical details and specifications can be found here.

For what regards the software usage, we can see a screenshot of it in fig.3.14. The measurement that we have conducted uses two modalities:

- **Waveform**, in which we can see the output voltages of the Ettore channels in the time domain, in practice as an oscilloscope;
- **Sweep**, in which the energy resolutions (FWHM) of all the channels are measured at specific peaktimes of the energy filter of DANTE, and then plotted. In this way it is possible to check the FWHM trend of all the channels and the best result obtainable.

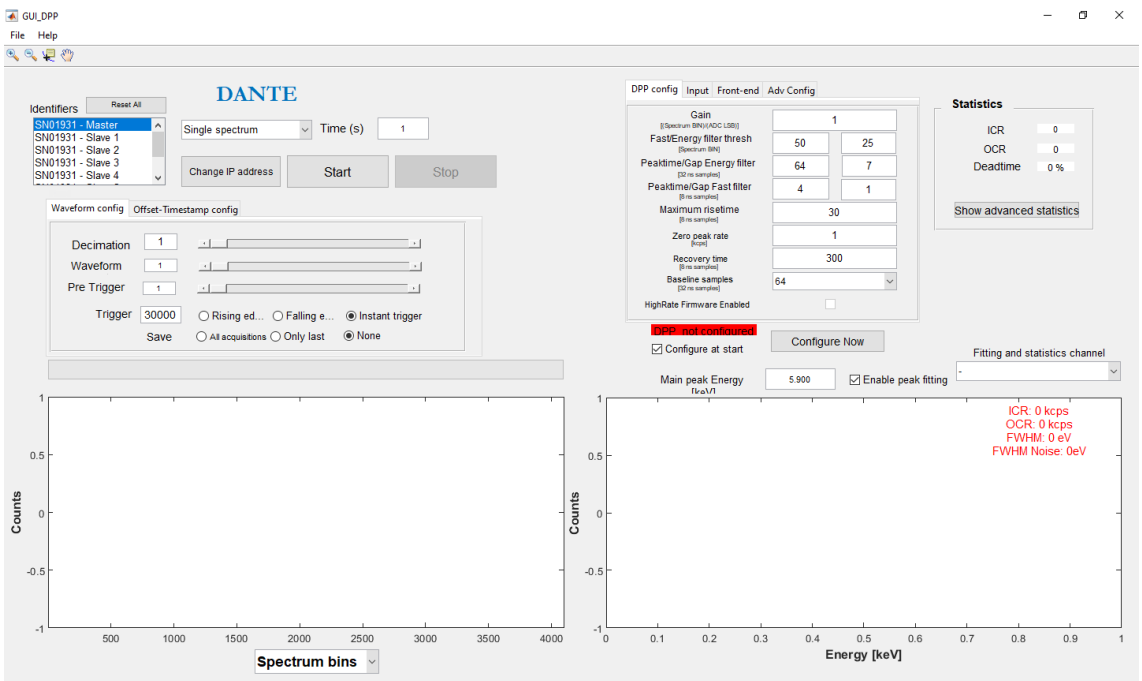


Figure 3.14: *Software GUI of DANTE DPP developed by XGLab.*

3.2 Overview of the 47-pixel setup

The full setup is basically an extension of the 12 pixels one, with a new detector board, new ASIC board and an upgrade of the bias system. These new boards, however, have the exact same dimensions as the old ones, meaning that the switch from the 12 pixels setup to the 47 one does not require mechanical redesign. On top of that, having more channels means having even more DANTEs systems to be used (6 in total) or a single 48-channel KERBEROS platform.

For what regards the detector board, the main difference is to have more pads to be bonded, having exactly 35 more channels in it. Since each channel has two connections with the corresponding ones of ETTORE, IN and CF, we have exactly 70 more connections and lines to the Samtec connector. This connector is sized for 83 channels, half the ones required for the final system, so it has no problem with any detector with a smaller number of channels.

The ASIC board maintains all the characteristics of the old one, apart from the fact of having a total of 4 ETTORE bonded on it. The number of layers has been increased from 4 to 8 in order to keep an adequate shielding against capacitive crosstalk with the now increased number of channels. A representation of the new ASIC board can be seen in fig.3.15. The connections to the bias board, however are different, due to the amount of additional signals that this board have to transmit to the chain. It was decided to use two 100-pin FPC (Flexible Printed Circuit) SMD Hirose connectors together with two flex cables of 100 pins each, one carrying the signals, the other one carrying the bias and control voltages.

All these signals however can not go directly to the bias system, for the simple fact that the bias board is equipped with 2 mm pitch header connectors. Two additional interface boards have been designed and constructed to create a bridge between the new ASIC board flex cables and the existing bias system. They simply receive the signals coming from the ASIC board and bring it to the bias one. A representation of both of them is present in fig.3.16. The board that carriers the bias signals has as additional feature: the inhibit of the switched reset filter on the ASIC board. This allows to temporarily disable the filter, allowing to electrically pulse the SDD pixels trough the capacitive coupling between the anode and the reset diode, using a signal coupled to the RD line thanks to a dedicated SMA on the bias board.

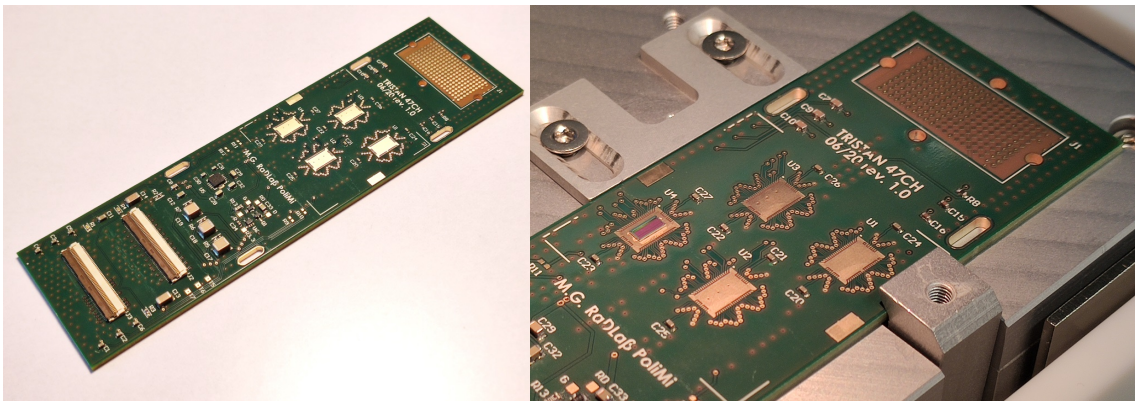


Figure 3.15: *ASIC board for the 47-channel setup. To the right, a zoom after the bonding of the first ETTORE chip.*

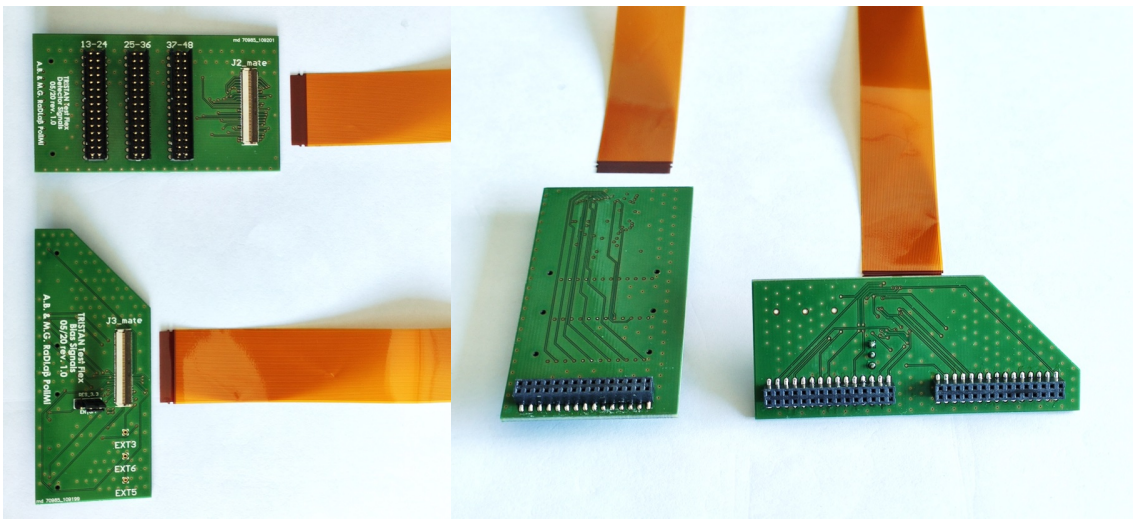


Figure 3.16: *Interface boards, bias one and signals one.*

Lastly, the bias board, maintains its characteristics unchanged. The only difference is regarding the additional number of amplifiers needed (36 channels). These are implemented similar to the modularity of the DANTEs systems, piling up three additional 12-channel buffer boards. These signals are brought from the ASIC board using the signal interface board mentioned before. The stack can be seen in fig.3.17.

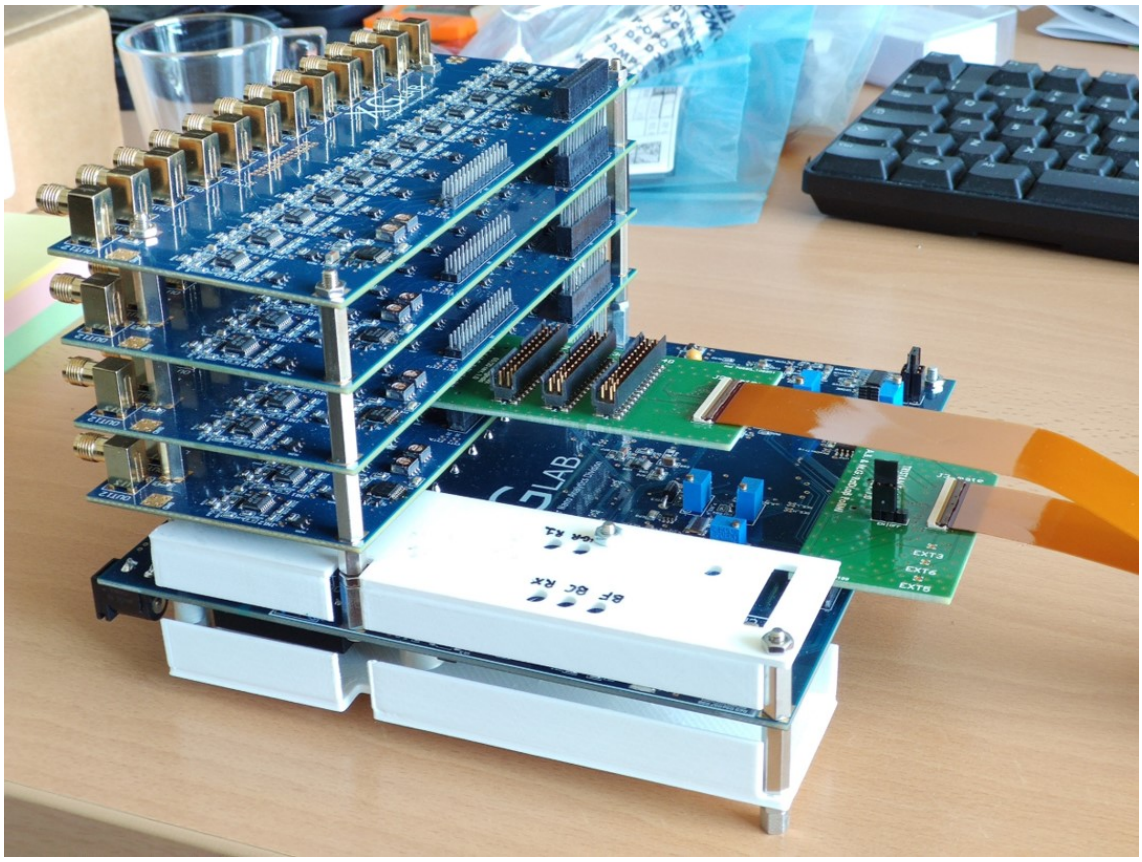


Figure 3.17: *Bias board for the 47 channels setup.*

3.3 Experimental results

3.3.1 12-pixel setup

First of all a complete design of the new two PCBs, the ASIC board and the detector one, has been done in Politecnico di Milano. The detector and the ETTORE ASIC were already available, so as soon as the PCBs were produced, they were bonded on the corresponding boards. The process was straightforward thanks to the fact of the presence of a bonding machine in our laboratory, and thanks to a skillful staff. The bias board was already tested and ready to be used too. Then all the system was assembled, as seen in fig.3.1 on page 54. The detector board is in a metal box because the detector itself is sensible to light, and this would have affected the measurements, adding a source of noise and an additional leakage current. Moreover, to reduce the

leakage current, the detector needs to be cooled below the water freezing point and the metal box permits to create an maintain a low-humidity environment. However, the cable in which the signals travel needs a hole to enter and exit from the box; to avoid the passage of the light and moisture a combination of plastic materials and adhesive tape have been employed.

In this setup, as already discussed, there were the possibility to conduct measurements both in ambient temperature and in a chilled one (around $-38\,°C$). This was possible thanks to the Peltier cell in contact to the metal "heatpipe" of the detector and to the possibility to inject dry nitrogen in the box using a tube. The Peltier cell works in a way that, with a polarization current of around $3\,A$, it creates a temperature difference and an heat flow between its two plates. To reach our desired temperature of $-38\,°C$, the warmer plate had to reach a temperature of around $5\,°C$ and this was possible thanks to a water chiller that cooled down the copper block. In fig.3.18 and fig.3.19 we can see the Peltier module used and the cooling components blocks.

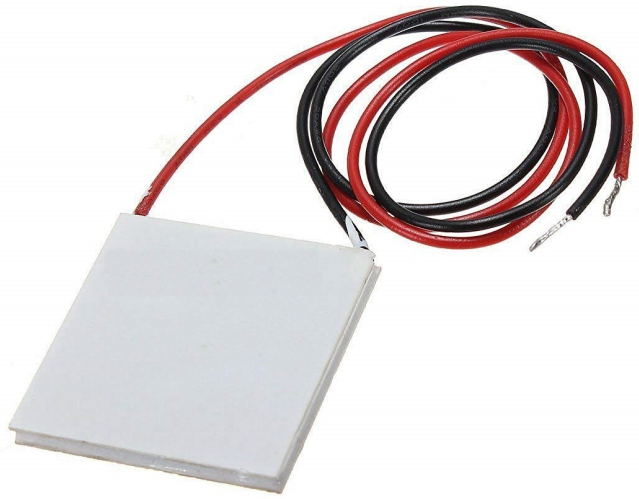


Figure 3.18: *Peltier module.*

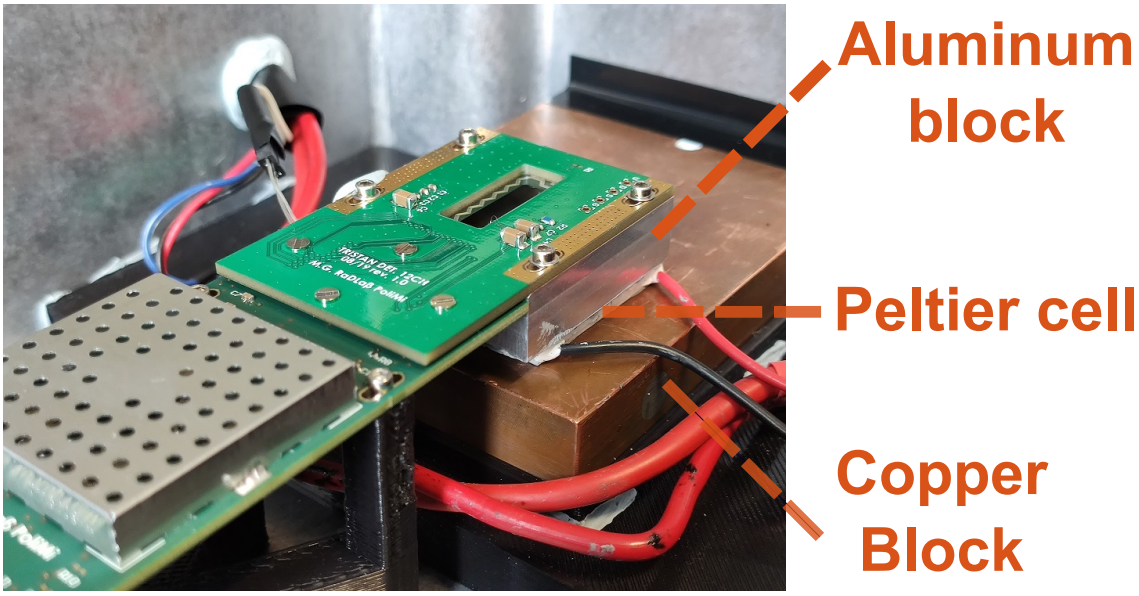


Figure 3.19: *Cooling components used in the 12 pixels setup.*

To check the temperature reached by the detector during the measurements at ambient temperature and at the chilled one, a simple resistance temperature detector (RTD) was used. In particular a PT100 is the type of sensor used and it is soldered on the Detector Board. It's resistance is susceptible to the external temperature, so using a tester it is possible to derive the actual temperature. Tables with known values are easily found, like the one in fig.3.20. We have used also a thermographic camera to check the temperature of the chip and calibrate the PT100 sensor witch is affected by parasitic resistance due to the interconnections. The thermographic measurement is only possible with the setup box opened. For humidity reason this was not feasible with the cooling system in operation. A further addition was the hygroscopic salts, which could be used as an alternative to nitrogen, to maintain the humidity of the system inside the box under a certain value, which was always checked thanks to an external humidity sensor. As a matter of fact, when the temperature goes down a certain value, the humidity as to be low enough to avoid water condensation and ice formation on the surface of the detector, which would damage it.

Temp	0	-1	-2	-3	-4	-5	-6	-7	-8	-9
-200	18.520									
-190	22.826	22.397	21.967	21.538	21.108	20.677	20.247	19.815	19.384	18.952
-180	27.096	26.671	26.245	25.819	25.392	24.965	24.538	24.110	23.682	23.254
-170	31.335	30.913	30.490	30.067	29.643	29.220	28.796	28.371	27.947	27.522
-160	35.543	35.124	34.704	34.284	33.864	33.443	33.022	32.601	32.179	31.757
-150	39.723	39.306	38.889	38.472	38.055	37.637	37.219	36.800	36.382	35.963
-140	43.876	43.462	43.048	42.633	42.218	41.803	41.388	40.972	40.556	40.140
-130	48.005	47.593	47.181	46.769	46.356	45.944	45.531	45.118	44.704	44.290
-120	52.110	51.700	51.291	50.881	50.471	50.060	49.650	49.239	48.828	48.416
-110	56.193	55.786	55.378	54.970	54.562	54.154	53.746	53.337	52.928	52.519
-100	60.256	59.850	59.445	59.039	58.633	58.227	57.821	57.414	57.007	56.600
-90	64.300	63.896	63.492	63.088	62.684	62.280	61.876	61.471	61.066	60.661
-80	68.325	67.924	67.522	67.120	66.717	66.315	65.912	65.509	65.106	64.703
-70	72.335	71.934	71.534	71.134	70.733	70.332	69.931	69.530	69.129	68.727
-60	76.328	75.929	75.530	75.132	74.732	74.333	73.934	73.534	73.134	72.735
-50	80.306	79.909	79.512	79.114	78.717	78.319	77.921	77.523	77.125	76.726
-40	84.271	83.875	83.479	83.083	82.687	82.290	81.894	81.497	81.100	80.703
-30	88.222	87.827	87.433	87.038	86.643	86.248	85.853	85.457	85.062	84.666
-20	92.160	91.767	91.373	90.980	90.586	90.192	89.799	89.404	89.010	88.616
-10	96.086	95.694	95.302	94.909	94.517	94.124	93.732	93.339	92.946	92.553
0	100.000	99.609	99.218	98.827	98.436	98.044	97.653	97.261	96.870	96.478
Temp	0	1	2	3	4	5	6	7	8	9
0	100.000	100.391	100.781	101.172	101.562	101.953	102.343	102.733	103.123	103.513
10	103.903	104.292	104.682	105.071	105.460	105.849	106.238	106.627	107.016	107.405
20	107.794	108.182	108.570	108.959	109.347	109.735	110.123	110.510	110.898	111.286
30	111.673	112.060	112.447	112.835	113.221	113.608	113.995	114.382	114.768	115.155
40	115.541	115.927	116.313	116.699	117.085	117.470	117.856	118.241	118.627	119.012

Figure 3.20: *PT 100 resistance table.*

At the first power up of all the circuits, the correct operation of the detector was inspected: as anticipated, the characteristic voltage ramp with the superimposed spikes due to the events were clearly visible both with an oscilloscope and the DANTE DPP. As a source of X-rays we used a ^{55}Fe source outside the box, exactly at the top of the detector. To avoid the contamination with light and to allow a fast positioning of the source, it was made a window with a graphite layer which is transparent to X-rays produced by the source.

In fig.3.21 we can see the waveforms of the 12 channels at room temperature with a ^{55}Fe source. This result was very promising, because as we can see:

- All the channels were currently working;
- The leakage was very homogeneous;
- The ramps were clean from additional noises and we can see the step signals correlated to the absorption of X-ways from the source.

After that, a measurement at $-34\,°\mathrm{C}$ was done. Using a peaking time of $6\,\mu\mathrm{s}$ and the suggested bias voltages from MPG-HLL, the resulting spectrum for one channel is visible in fig.3.22. Being the k_α and the k_β peaks really well visible, the energy resolution (FWHM) was around 150 eV at 5.9 keV. All this results were made without optimizations of any sort (grounding, voltages) so we expected a lot of room for improvements.

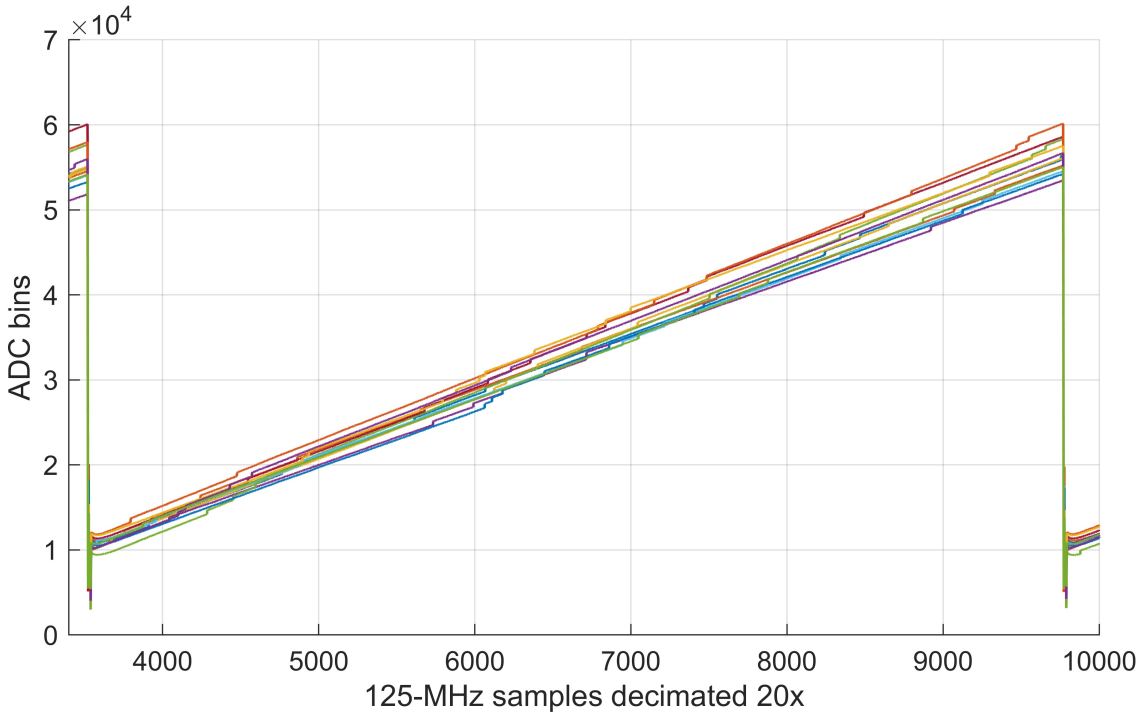


Figure 3.21: *Waveforms of the 12 channels at room temperature with a ^{55}Fe source.*

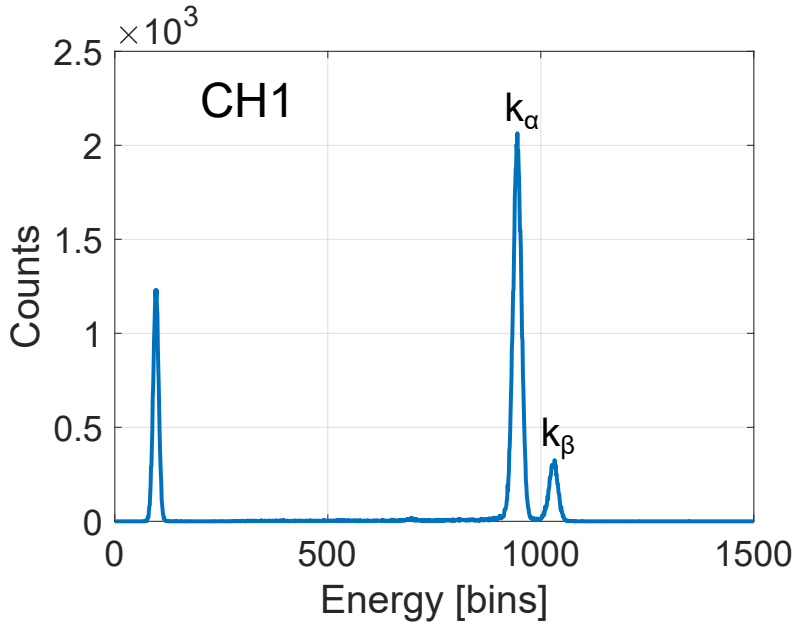


Figure 3.22: *First significant spectrum at $-34\,°C$ in the 12-pixel setup.*

The leakage of each pixel was calculated thanks to an oscilloscope and the formula:

$$I_{leak} = C_{fb} \cdot \frac{dV_{outCSA}}{dt}$$

In tab.3.1 we can see a table with all the leakages. At the chilled temperature all this values are in the order of 200 fA each, that it is indeed a really low value, in line with the specifications.

Table 3.1: Leakage matrix of the 12-pixel detector.

CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	CH9	CH10	CH11	CH12
12.6 pA	12.5 pA	15.6 pA	12.9 pA	14 pA	12.8 pA	14.1 pA	13.3 pA	12.8 pA	13.1 pA	13.1 pA	12.1 pA

The optimizations of the voltages then started, using and empirical method. The relevant parameters and their value are all listed in tab.3.2.

Table 3.2: First optimized voltages in the 12-pixel setup.

V_{drain}	8.5 V
V_{sss}	−6.5 V
Reset diode H	5.75 V
Reset diode L	−10 V
R_1	−15 V
IGR	−22.5 V
R_X	−120 V
BC	−100 V
BF	−110 V

The results of these polarization can be seen in fig.3.23 as a peaking time sweep measurement of all the channels. The best resolution that has been observed is around 144 eV, with an improvement on the previous measurement of around 10 eV. It can be noticed that all the channels had practically the same results. However, this results were not possible using the setup without modifications. The 24 V power supply unit provided by XGLab caused an injection of noise in all the bias voltages, leading in a direct effect on the polarization of the detector.

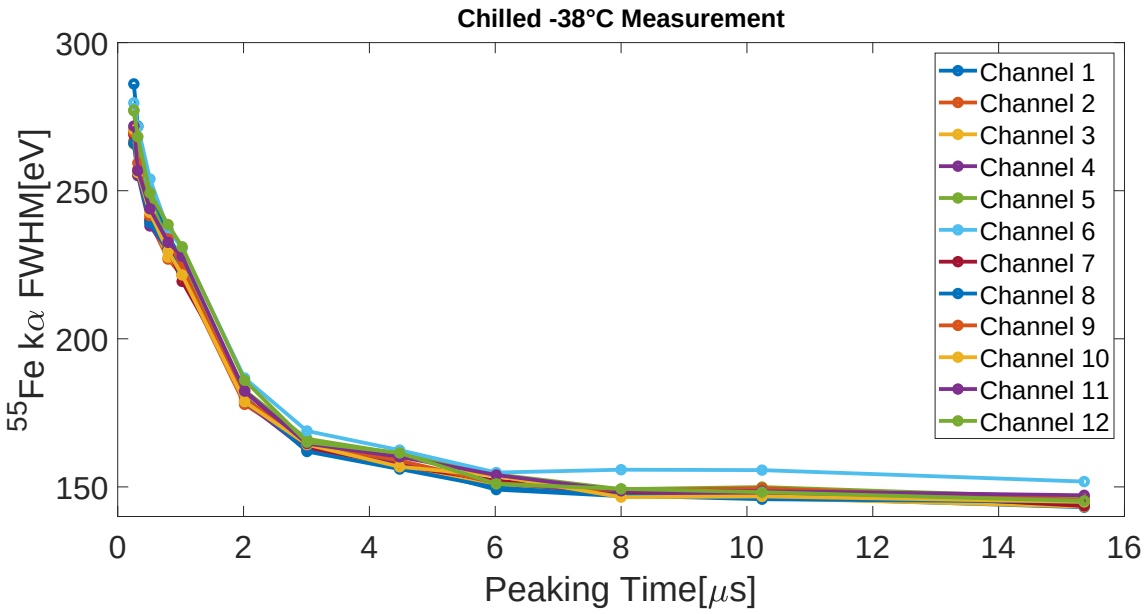


Figure 3.23: *Sweep of all the 12 channels, at* $-38\,°\mathrm{C}$.

This caused a worsening of the energy resolution for short filter peaking times, generating incorrect measurement. In general, DC-DC regulators allow more compactness and efficiency, at the cost of an higher ElectroMagnetic Induction (EMI). Even if it is a challenge to find a proper trade-off, there is the possibility to create switching power supplies [16]. To fix this issue, an external benchtop power supply was used, bypassing the default PSU and providing the 24 V necessary for the board. As comparison, in fig.3.24 we can see the difference between using the default PSU and the external one. The reader can see very well that this noise affected only the low peaking times of the energy filter. Even using the external PSU, a noticeable systematic noise was found on all the bias voltages, thanks to the use of an oscilloscope. An investigation on the electromagnetic interference of this bias board was necessary. For this kind of measurement a RF spectrum analyzer, along with a magnetic field RF probe, were used. The working principle of the probe can be seen in fig.3.25.

A magnetic field passing through the probe loop generates a voltage according to the Faraday's law, which states that the induced voltage is proportional to the rate of change of magnetic flux through a circuit loop. At very low frequencies a voltage would be induced directly in the internal loop conductor, but the copper

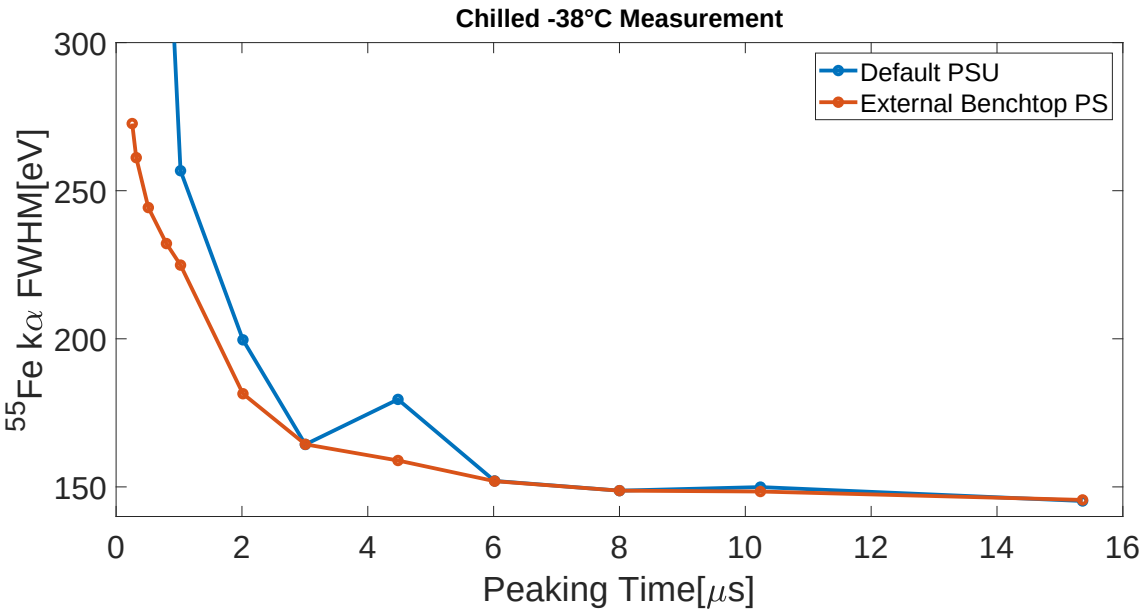


Figure 3.24: *Average of the sweep of the 12 channels, with default and benchtop power supply.*

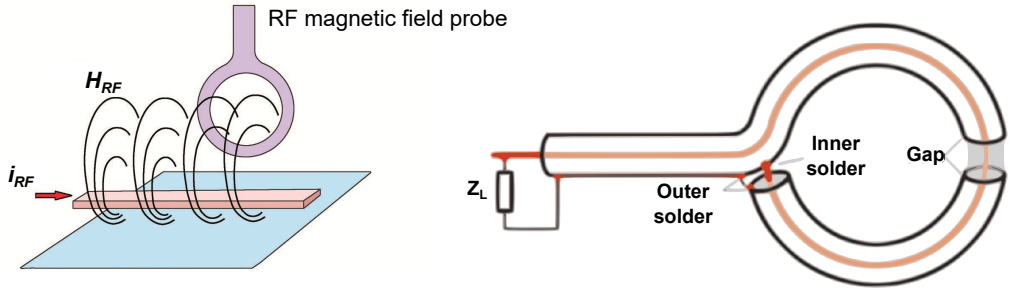
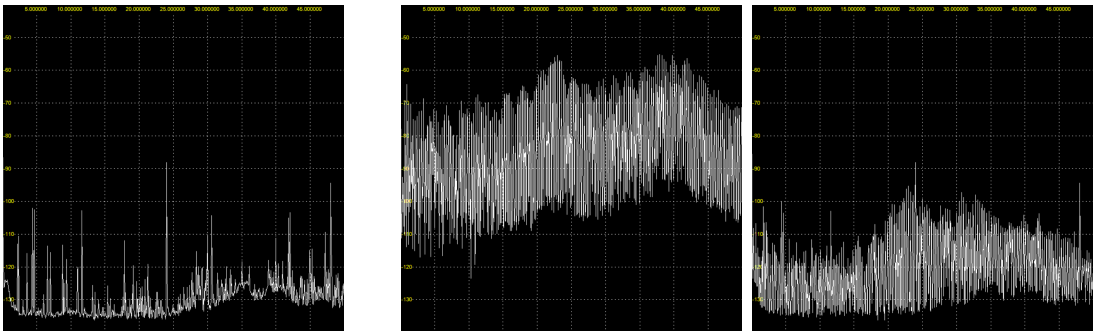


Figure 3.25: *RF magnetic field probe mode of operation.*

sheath is quite a good shield to magnetic fields at frequencies exceeding the low kHz range. So at high frequency, a voltage is then induced preferentially in the outer sheath loop, and this appears across the gap. The metal sheath thickness is enough depth to prevent direct interaction between currents on the external surface and internal surfaces of the shield. The 250 Ω transmission line, formed by the inner surface of the sheath and the inner conductor, is then driven by this voltage and is terminated by the 50 Ω of the measurement system. The results obtained by RF spectrum analyzer, in fig.3.26, highlighted the necessity to apply a shield between

the DC-DC converters and the signal buffer boards, where the signals are amplified and processed. All these measurement have an y-axis from −40 dB to −140 dB and an x-axis that spans from 0 Hz to 50 MHz.



(a) With the bias system off (External noise).

(b) Below the DC-DCs converters.

(c) Above the buffers.

Figure 3.26: *Measurements of EMI on the bias board.*

3.3.2 Optimizations strategies

All the measurements on the 12-pixel SDD matrix have a noticeable higher FWHM than what we were expecting, especially at the shorter peaking times. As comparison, the previous production MPG-HLL 1-pixel detector, installed in the new 12-pixel setup, gave a resolution of 130 eV as its best result, and a lower noise trend overall. To find the source of this noise, several roads were explored.

Collimator

In the higher peaking times, charge sharing and crosstalk effects may worsen the FWHM resolution. To exclude this, only one of the pixels should be active at time, with the others that do not bring any significant signals. A collimator was thus used. It is a device that narrows a beam of particles to a precise point, avoiding the spread of them in the space. A PolyLactic Acid (PLA) cover, made with a 3D printer with holes corresponding to the centre of the pixels, was designed to act as shield for the other channels. With this on top of the detector along with 3 collimator disks (piled up as seen in fig.3.27), a measure of a single channel was performed. Unfortunately,

the sweep gave basically the same results, excluding the cross-talk of the channels as a source of noise for long peaking times.

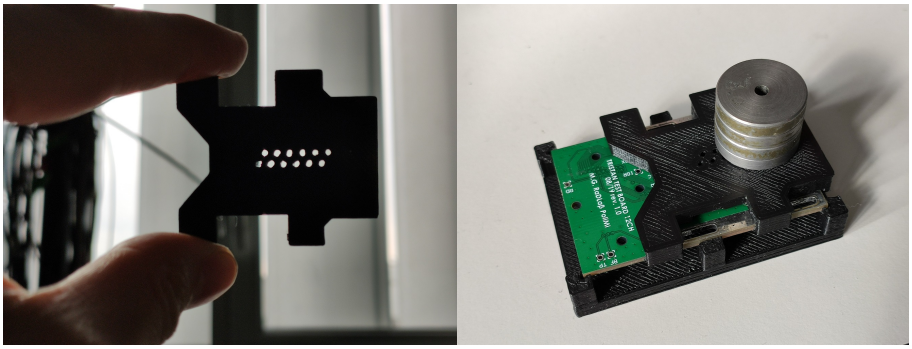


Figure 3.27: *Collimator's usage.*

ETTORE second stage

This additional source of noise could be caused by the coupling of noises after the preamplifier outputs. Using the ETTORE second stage, already discussed in chapter II, we could apply a gain of around 10 on the signals. Introducing this gain early in the signal chain, we could reduce the impact of all the additional noise contributions present after the amplification. In fact, having as G the usual gain of the stage and G_{IN} the gain added at the input:

$$V_{OUT} = V_{IN} * G + V_{noise} * G$$

$$V_{OUT} = V_{IN} * G_{IN} * G + V_{noise} * G$$

In the second case of course the V_{noise} contribution is practically negligible. However, even this method did not give appreciable results.

Voltages optimizations

As additional test to improve the FWHM, a further optimization of the polarization voltages was done reconsidering the circuit schematics in fig.3.28.

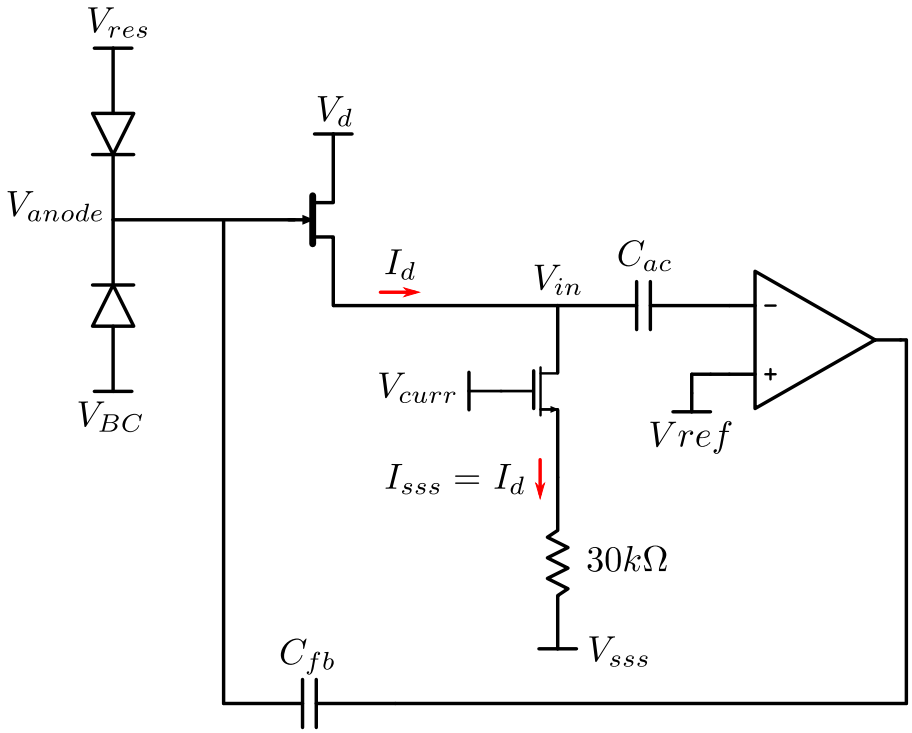


Figure 3.28: *Integrated JFET and connections with ETTORE ASIC schematics.*

Knowing that:

- V_{ref} and V_{curr} are equal to 2.7 V as ETTORE default values,
- the polarization current I_{sss} was chosen equal to 220 µA,
- the reset diode has a threshold voltage of around 0.7 V,
- $V_{in} \geq V_{curr} - 0.5\,\text{V}$ to avoid ohmic mode,
- $V_{ds} \approx 5\,\text{V}$ for the JFET,

we find the polarization voltages in tab3.3.

Even if the noise problematics were not solved, we had a way less delicate bias point, giving stable results with different polarization values. Since this degradation seemed a problem of the 1/f and series noise of the integrated JFET, the design of a noise setup was the subsequent step, in order to exclude possible errors in the design or the production process of the detector. All this can be found in the chapter IV.

Table 3.3: Further optimized voltages in the 12-pixel setup.

V_{drain}	7.3 V
V_{sss}	−4.7 V
Reset diode H	4 V
Reset diode L	−10 V
R_1	−8 V
IGR	−15 V
R_X	−120 V
BC	−100 V
BF	−110 V

3.3.3 47 pixels

The steps used for the composition of this setup followed the one of the 12-pixel. A redesign of the ASIC board and the detector one was done. Having decided to maintain the same dimensions of the 12-pixel ones, their realization was challenging: in the same space containing 1 ETTORE a total of 3 additional ones have to fit, and they were added 35 additional signals overall. This brought to the decision of increasing the layer number of both the boards, specifically from 4 to 8 for the ASIC one and from 4 to 6 for the detector one. On top of that the tracks and the vias had way less freedom regarding their position. In this first part of testing it was reused the old 12 pixels detector board to test that all the new parts were correctly working, like the new piled-up buffers of the bias board or the interface boards. Being a 47 channels setup, all the remaining 35 ones were not used. As consequence only one of the 4 ETTORE chips were needed, so at the start of these testing only one of them was bonded. In the end the full chain can be seen in fig.3.29.

This setup shares the same characteristics of the old one, like:

- The metal box used to stop the light and other unwanted sources of signal;
- The ability to be cooled down thanks to a Peltier cell and a water chiller;
- The presence of the humidity sensor.

Figure 3.29: *47-channel setup with the old 12 pixels board.*

The first resulting FWHMs are basically the same compared to the one of the 12-pixel setup, so all the boards, including the new interfaces, are correctly working. Right now the 47 pixels detector is under characterization, after having been bonded to its board and having activated all the 47 channels.

4 | Noise Test Setup

In this chapter we present the study and the realization of a noise test setup, used to check the noise performances of the integrated JFET SDDs. After presenting the working principle, a study of its feasibility is done. After that, the choice of the components and the working points are setted. At the end, we have the measurements of the real setup and the findings achieved.

4.1 JFET Noises

The main player in the readout of SDDs is the integrated JFET, that transforms the charge collected to the anode in an amplified current. Therefore, in our detector, each pixel has its corresponding integrated JFET. The waveforms obtained after the characterization of the SDDs in the 12 and 47-pixel setups suggest that an additional contribution in the noise of the JFETs is probably altering the measurements. Since a worse than expected energy resolution has been found basically at all peaking times of the energy filter, the guilty noise should have an impact at low frequencies, like an 1/f noise, or have an higher power spectral density than the expected one. Actually, JFETs have indeed two main contributions: a so called white noise, that has a constant power spectral density at different frequencies, and the 1/f noise, that concentrates its power in the low decades. This two noises can be modelized as a single voltage generator (or an equivalent current one), as we can see in fig.4.1. In the case of the JFET we would have:

$$\overline{S}_{vin}^2 = \frac{4kT\gamma}{gm_{JFET}} + \frac{A_f}{f}$$

considering the two sources of noise uncorrelated. The measurements of this two contributions would give us additional informations regarding the kind of noise that affects our measure. In order to correctly find the noise produced by each integrated JFET in our detectors, the design of a custom circuit, to measure and calculate the

input referred noise, was necessary.

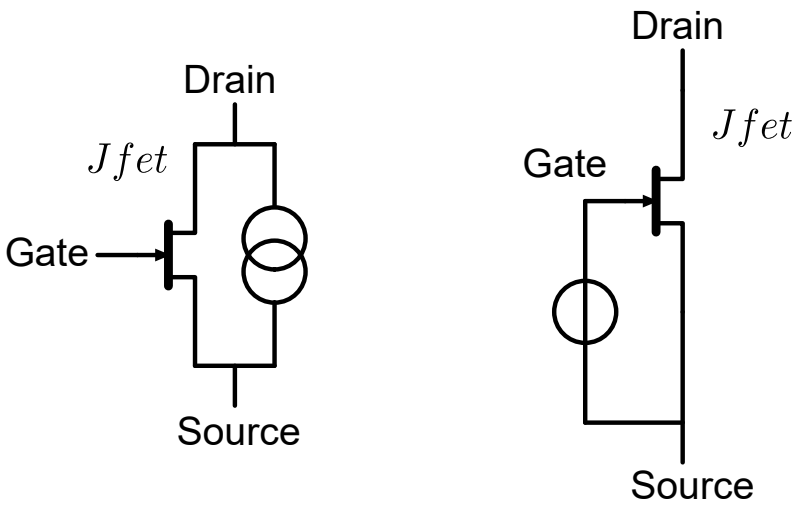


Figure 4.1: *JFET's noise model. To the left the model using current generators, to the right its equivalent circuit with voltage generators.*

4.2 Overview of the circuit

To find the value of the input noise it has been decided to exploit the relation between output noise, Transfer Function (TF) and input referred noise generator. Each system has a certain noise at its output, being a statistical quantity and induced by the many random fluctuations that are present during the motion of the free carriers, for example the electrons. This fluctuations can be modeled as voltage and current generators, as we did at the start of this chapter for the JFET, for every noisy component. Each one of this generators gives at the output a certain noise, depending on the transfer function that they have from their source to the output. Their TFs depend on the position in the circuit and in the type of source which is considered. The input referred noise generator is an equivalent source at the input that would give at the output the same noise generated from all the different generators, but considering a noiseless circuit. We can write:

$$\overline{S}^2_{OUT} = |T(s)|^2 \cdot \overline{S}^2_{IN}$$

with S^2_{IN} our input referred noise generator. To make it clear, fig.4.2 represents the two situations. Both the input generators present on the right of the figure can be contained by a single equivalent voltage generator.

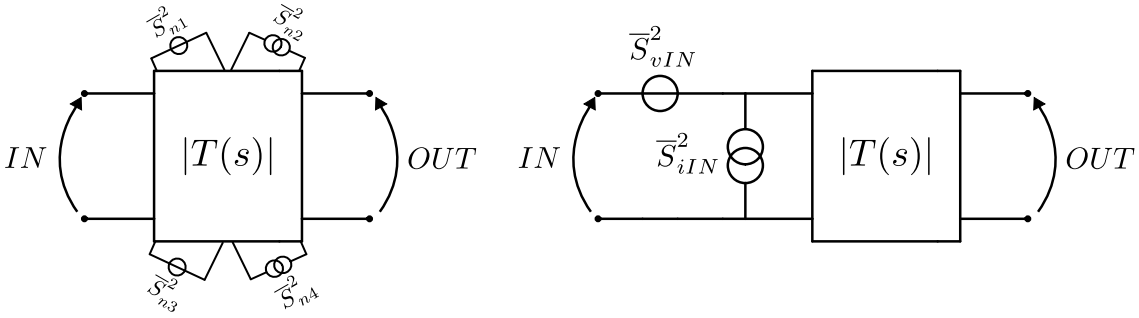


Figure 4.2: *Network with noise sources. In the left we have a noisy system, in the right a noiseless one.*

Being able to modelize all the sources with their input noise generator, in our circuit their contributions should be way less than the JFET's one, since it is the quantity that we want to measure. In the end, the steps followed are:

1. Measure the output noise at the output of the circuit, minimizing all the contributions of the noisy elements in regards to the one at the input of the target FET (or the target component desired);

2. Calculate the transfer function of the circuit using a Spectrum Analyzer (SA) in our range of frequency of interest (between 10 Hz and ≈20 MHz);

3. Divide the output noise with the (modulus) square of the transfer function to finally have the correct value of the input noise, thanks to the known formula here reported.

$$\overline{E}^2_{nOUT} = |H(f)|^2 \cdot \overline{E}^2_{nJfet}$$

The measurements of the TF and the output noise can be performed by the network/spectrum analyzer. The one that has been used is the 4195A by HP. To calculate the transfer function of a circuit, it applies a sinusoidal signal with variable frequency at the input of the setup and reads the resulting waveform at the output of it. Dividing this two known quantities, the transfer function of this network is easily found. This mode of operation is known as "NETWORK".

Figure 4.3: *Spectrum Analyzer 4195A by Hewlett Packard.*

The SA can even perform the calculation of the output noise of a circuit (as an oscilloscope), simply providing at one of its inputs the desired voltage to measure. At fig.4.3 we can see the instrument. A simplified representation of the measurement circuit is shown in fig.4.4. It is composed by:

- **Input filter and polarization.** Here we have an initial high pass filtering and the electronics to polarize the JFET.
- **Source follower and amplification.** The signal is brought at the input of an OPAMP thanks to a buffer made by a source follower, to be amplified and make the noise contribution of the Spectrum Analyzer negligible.

A more detailed schematics of the circuit to bias the JFET is presented in fig.4.5. Here we can see the two switches S_2 and S_3, that are fixed to the A or B position depending on the type (n-type or p-type) of FET that has to be measured. In a similar manner V_p can be trimmered between positive and negative voltages. C_{gx}

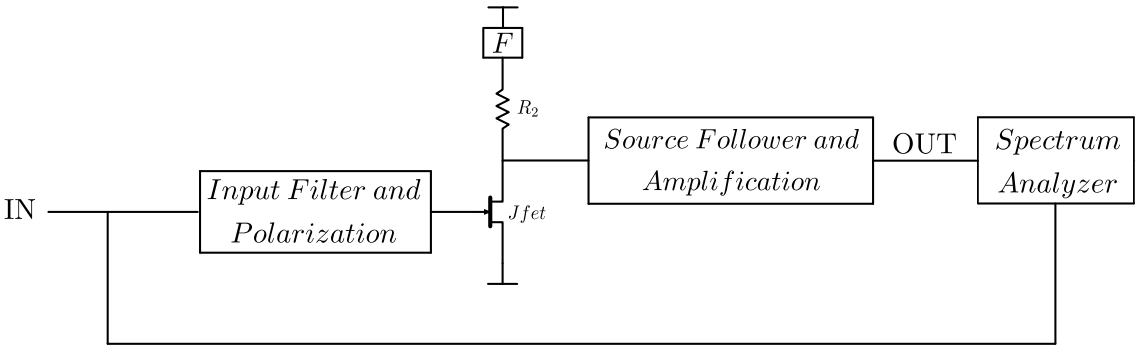


Figure 4.4: *General representation of the circuit used.*

is not always present in the circuit: during the calculation of the transfer function it is removed by the circuit by a jumper, instead during the noise calculation it is present to filter all the noises arising from the left part of the circuit, leaving the contribution due to the JFET thermal noise alone. The role of R_1 and C_{tot} is to act as a filter for the disturbances of the power supplies. In the following sections we will consider the particular case of the n-JFET, since our detector uses this kind of device.

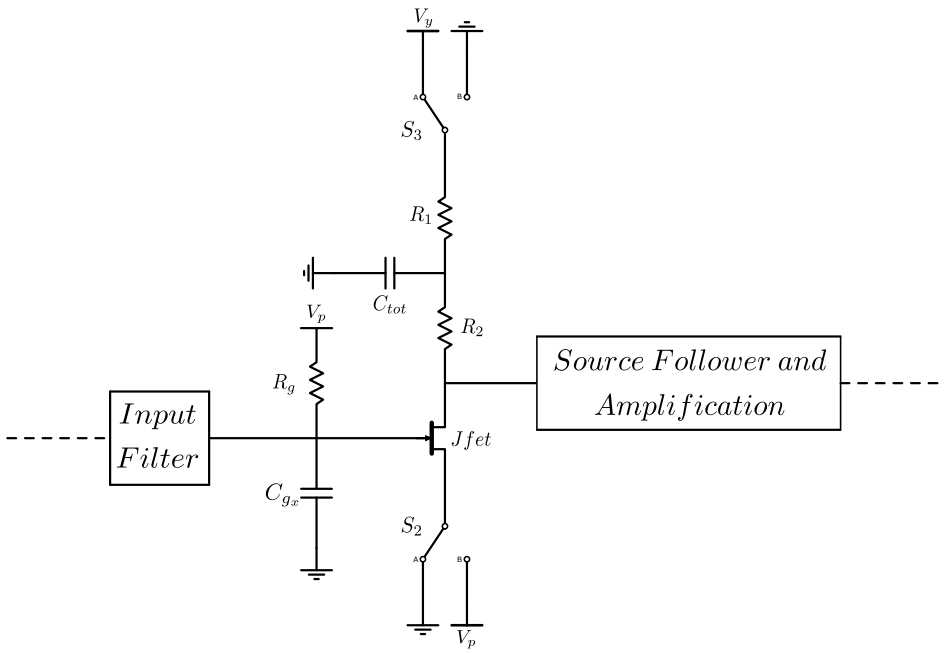


Figure 4.5: *General purpose (n and p-JFET) circuit, thanks to switches.*

In fig.4.6 we can see a complete representation of the circuit used for the calculation of the transfer function. The values of C_{g1}, C_{g2} and R_g depends on the value of the input pole that the user want to implement. As anticipated before, thanks to the function of "NETWORK" of the Spectrum Analyzer, a complete automatic calculation of the transfer function of the circuit is made. Even if it is not represented, there is an output high pass filter given by the requirements of the SA.

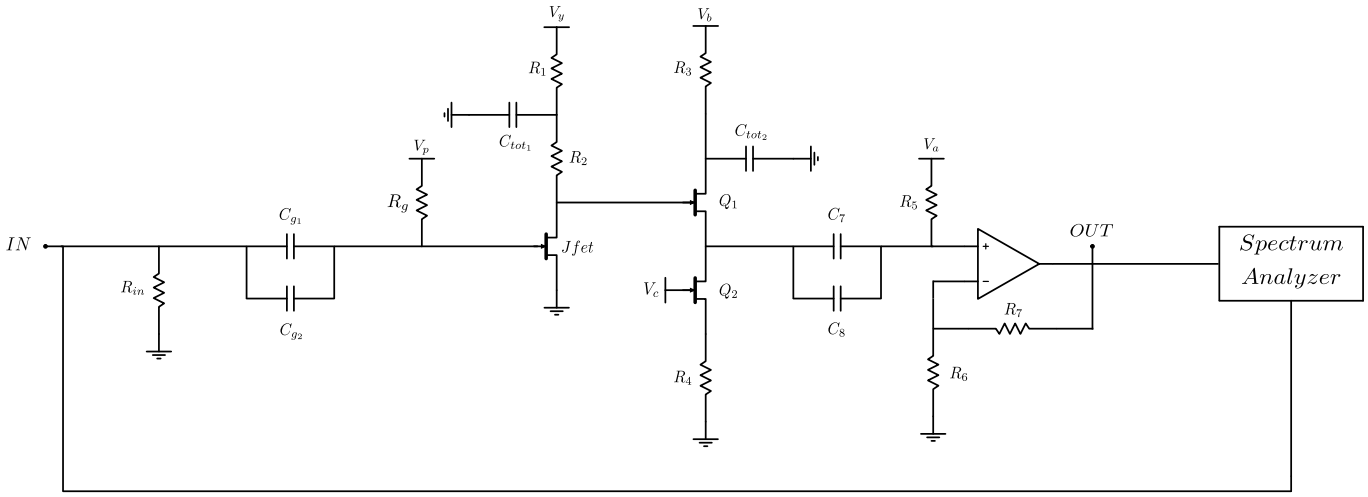


Figure 4.6: Representation of the noise test circuit with the SA connections for the measure of the transfer function.

4.3 Equivalent noises calculations

In order to have at the input of the chain only the contribution due to the JFET's noise, all the other noise components have to be sized to give a small contribution on the output noise compared to the JFET's one. To calculate the output noise of our circuit the input filter and the SA are disconnected. The resulting circuit, along with a representation of all its noise generators, is in fig.4.7. In the following there is the list of noise contributions in addition to the one at the input of the JFET. The equivalent generators are all reported at the input to be compared with the noise of our transistor.

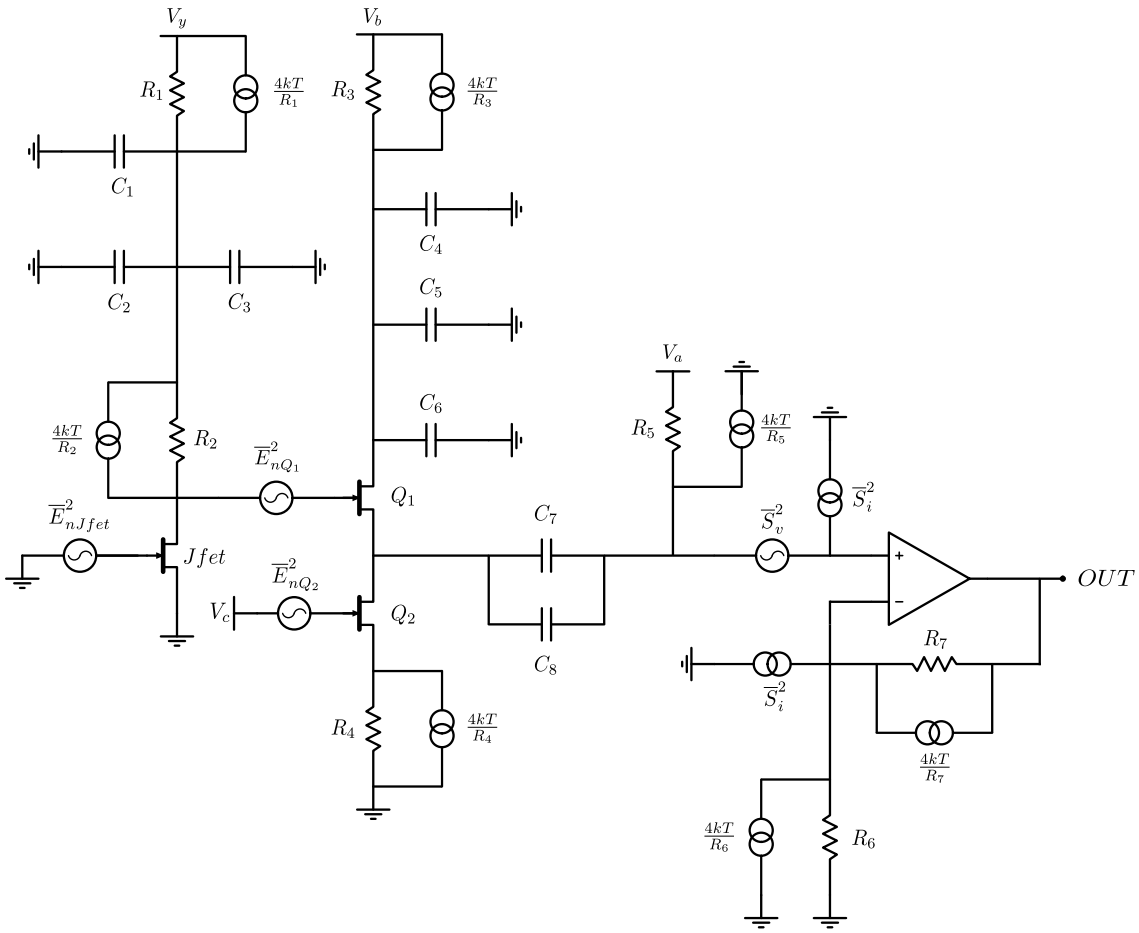


Figure 4.7: *Representation of the circuit used for the calculation of the noise contributions, highlighted by their equivalent noise generators.*

- R_1

  The contribution of R_1 is modeled as a current generator with a value of $\frac{4kT}{R_1}$. However, this type of noise is completely discharged in the capacitors C_1, C_2 and C_3 in our range of frequencies of interest.

$$\overline{E}^2_{nR_1eq} = 0$$

- R_2

  As before, the current noise of R_2 is $\frac{4kT}{R_2}$. This noise can be compared to the

one of the JFET, so we can model it at the input as a voltage generator:

$$\overline{E}^2_{nR_2eq} = \frac{4kT}{R_2 gm^2_{JFET}}$$

- Q_1
  Remembering the gain of the JFET, namely $G = gm_{JFET} \cdot (R_2 // r_0)$, the model of the voltage noise at the input of Q1 is $\overline{E}^2_{nQ_1} = \overline{E}^2_{nQ_1eq} \cdot G^2$. As a consequence, the noise at the input will be:

$$\overline{E}^2_{nQ_1eq} = \frac{\overline{E}^2_{nQ_1}}{(gm_{JFET} \cdot (R_2 // r_0))^2}$$

- Q_2
  In this case, finding the current that flows in the FET Q_2, the calculation of the equivalent noise generator at the input is straightforward. This current is equal to $\overline{E}^2_{nQ_2} \cdot (\frac{1}{\frac{1}{gm_{Q_2}} + R_4})^2$. Being a resistance of around $\frac{1}{gm_{Q_1}}$ at the source of the FET Q_1, a voltage noise of $\overline{E}^2_{nQ_2} \cdot (\frac{1}{\frac{1}{gm_{Q_2}} + R_4} \cdot \frac{1}{gm_{Q_1}})^2$ is present at the source of the FET Q_1. As a result at the input we have:

$$\overline{E}^2_{nQ_2eq} = \overline{E}^2_{nQ_2} \cdot (\frac{1}{\frac{1}{gm_{Q_2}} + R_4} \cdot \frac{1}{gm_{Q_1} G})^2$$

  with $G = gm_{JFET} \cdot (R_2 // r_0)$.

- R_3
  This case is the same as the one of R_1, except that the capacitors are named C_4, C_5 and C_6.

$$\overline{E}^2_{nR_3eq} = 0$$

- R_4
  As Q_2, but with a current divider between R_4 and $\frac{1}{gm_{Q_2}}$. So:

$$\overline{E}^2_{nR_4eq} = \frac{4kT}{R_4} \cdot (\frac{R_4}{\frac{1}{gm_{Q_2}} + R_4} \cdot \frac{1}{gm_{Q_1} G})^2$$

- R_5
  Due to a zero at the DC frequency, it is better to carefully calculate this contribute in term of Laplace transform. The current that enters in the source of Q_1 is equal to $\frac{4kT}{R_5} \cdot (\frac{sR_5(C_7+C_8)}{1+s(C_7+C_8)(R_5+\frac{1}{gm_{Q_1}})})^2$ so we can report at the input as:

$$\overline{E}^2_{nR_5eq} = \frac{4kT}{R_5} \cdot (\frac{sR_5(C_7+C_8)}{1+s(C_7+C_8)(R_5+\frac{1}{gm_{Q_1}})} \cdot \frac{1}{gm_{Q_1}G})^2$$

- *Voltage noise of the Amplifier*
  We can simply reuse the calculation of R_5, converting it as a current generator. So the value of the current is $I^2_{eq} = \frac{\overline{S}^2_v}{(R_5//\frac{1}{gm_{Q_1}})^2}$. At this point it follows the same transfer function of the resistor R_5:

$$\overline{E}^2_{nS_veq} = \frac{\overline{S}^2_v}{(R_5//\frac{1}{gm_{Q_1}})^2} \cdot (\frac{sR_5(C_7+C_8)}{1+s(C_7+C_8)(R_5+\frac{1}{gm_{Q_1}})} \cdot \frac{1}{gm_{Q_1}G})^2$$

- *Current noise of the Amplifier*
  The one at the plus input follows the exact same pattern of R_5:

$$\overline{E}^2_{nS_ieq} = \overline{S}^2_i \cdot (\frac{sR_5(C_7+C_8)}{1+s(C_7+C_8)(R_5+\frac{1}{gm_{Q_1}})} \cdot \frac{1}{gm_{Q_1}G})^2$$

In the end the total equivalent noise at the input of the Jfet is:

$$\overline{E}^2_{ntot} = \overline{E}^2_{nR_2eq} + \overline{E}^2_{nQ_1eq} + \overline{E}^2_{nQ_2eq} + \overline{E}^2_{nR_4eq} + \overline{E}^2_{nR_5eq} + \overline{E}^2_{nS_veq} + \overline{E}^2_{nS_ieq}$$

with, respectively, considering $s \longrightarrow \infty$:

$$\overline{E}^2_{nR_2eq} = \frac{4kT}{R_2 gm^2_{JFET}}$$

$$\overline{E}^2_{nQ_1eq} = \frac{\overline{E}^2_{nQ_1}}{(gm_{JFET} \cdot (R_2//r_0))^2}$$

$$\overline{E}^2_{nQ_2eq} = \overline{E}^2_{nQ_2} \cdot (\frac{1}{\frac{1}{gm_{Q_2}} + R_4} \cdot \frac{1}{gm_{Q_1}G})^2$$

$$\overline{E}^2_{nR_4eq} = \frac{4kT}{R_4} \cdot (\frac{R_4}{\frac{1}{gm_{Q_2}} + R_4} \cdot \frac{1}{gm_{Q_1}G})^2$$

$$\overline{E}^2_{nR_5eq} = \frac{4kT}{R_5} \cdot (\frac{R_5}{R_5 + \frac{1}{gm_{Q_1}}} \cdot \frac{1}{gm_{Q_1}G})^2$$

$$\overline{E}^2_{nS_veq} = \frac{\overline{S}^2_v}{(R_5 // \frac{1}{gm_{Q_1}})^2} \cdot (\frac{R_5}{R_5 + \frac{1}{gm_{Q_1}}} \cdot \frac{1}{gm_{Q_1}G})^2$$

$$\overline{E}^2_{nS_ieq} = \overline{S}^2_i \cdot (\frac{R_5}{R_5 + \frac{1}{gm_{Q_1}}} \cdot \frac{1}{gm_{Q_1}G})^2$$

4.4 Biasing and choice of components

V_{ds}	$4.3\,\mathrm{V}$
V_{gs}	$-0.33\,\mathrm{V}$
I_{Jfet}	$220\,\mu\mathrm{A}$

Table 4.1: *Desired Biasing Values of the 12-channel device.*

The JFET is biased as when it is functioning in the detector with values reported in tab.4.1, given by the characterization results in the chapter III. Following the table , the values of major importance are the V_{ds} voltage of the JFET, which is directly controlled by the values of R_1, R_2 and the JFET current I_{jfet}. R_2 is chosen to be way higher than the $\frac{1}{gm_{JFET}}$ to have a negligible contribution with respect to the white noise of the JFET. In fact:

$$\frac{4kT}{R_2} << 4kT\gamma gm_{JFET} \longrightarrow R_2 >> \frac{1}{gm_{JFET}}$$

Being $\frac{1}{gm_{JFET}} \approx 3.3\,\mathrm{k\Omega}$, the value for R_2 should be at least of $33\,\mathrm{k\Omega}$. In the end:

$$R_2 = 50\,\mathrm{k\Omega}$$

Selecting a R_1 of around $1\,\mathrm{k\Omega}$, the value of V_y can be easily found with this formula:

$$V_{dJFET} = V_y - I_{JFET} \cdot (R_1 + R_2) \longrightarrow V_y \approx 15\,\mathrm{V}$$

Then, we have to consider the polarization of the gate of the FETs Q_1 and Q_2. Their model is the 2SK932 JFET transistor. For this component we want a transconductance way higher than the one of the input JFET, to have a low contribution of the noise, so we impose a high value for the current. Choosing a current of around 1 mA, imposing a V_{gsQ_2} of 0 V and using a resistance $R_4 = 4.3\,\text{k}\Omega$ we find:

$$I_{dQ_2} = \frac{V_{sQ_2}}{R_4} = 1\,\text{mA} \longrightarrow V_{sQ_2} = 4.3\,\text{V}$$

And as a consequence:

$$V_{gQ_2} = V_c \approx 4.3\,\text{V}$$

The V_{ds} of this kind of JFET is really low to have the possibility to bring 1 mA, less then 0.1 V. For what regards the value of R_3, it is chosen to have a low noise contribution (even if the most part of it is filtered out), like 1 kΩ. In the end:

$$V_b = I_d \cdot (R_3 + R_4) + V_{dsQ_1} + V_{dsQ_2} = 9.5\,\text{V}$$

But just to be in a safe zone V_b is at a slightly higher voltage, such as 10 V. For what regard R_5, following the steps of the other resistances to have low noise,

$$R_5 = 10\,\text{k}\Omega$$

The OPAMP should be low noise and with wide enough band. The amplifier chosen is the AD8038 that has a $R_{in} = 10\,\text{M}\Omega$, $\overline{S}_v \approx 8\,\frac{\text{nV}}{\sqrt{\text{Hz}}}$ and $\overline{S}_i \approx 600\,\frac{\text{fA}}{\sqrt{\text{Hz}}}$. For what regards the biasing of this OPAMP, we just select a single-rail voltage of 10 V. To bring it at half of its dynamics to be able to use the full swing of it, a gain $G = 5$ is chosen:

$$V_a = 1\,\text{V} \longrightarrow V_{OUT} = 5\,\text{V}$$

Approximating gm_{Q_1} and $gm_{Q_2} = 5\,\text{mS}$, at first approximation all the noises are equal to:

$$G = gm_{JFET} \cdot (R_2 // r_0) \approx 15$$

$$\overline{E}^2_{nR_2eq} = \frac{4kT}{R_2 gm^2_{JFET}} = 3.68 \times 10^{-18}\,\frac{\text{V}^2}{\text{Hz}}$$

assuming $10\,\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$ as the noise of the JFET 2SK932 (overestimating it):

$$\overline{E}^2_{nQ_1eq} = \frac{\overline{E}^2_{nQ_1}}{G^2} = \frac{\overline{E}^2_{nQ_1}}{225} = 4.44 \times 10^{-19}\,\frac{\mathrm{V}^2}{\mathrm{Hz}}$$

$$\overline{E}^2_{nQ_2eq} = \overline{E}^2_{nQ_2} \cdot (\frac{1}{\frac{1}{gm_{Q_2}} + R_4} \cdot \frac{1}{gm_{Q_1}G})^2 = \overline{E}^2_{nQ_2} \cdot 2.34 \times 10^{-6} = 8.78 \times 10^{-22}\,\frac{\mathrm{V}^2}{\mathrm{Hz}}$$

$$\overline{E}^2_{nR_4eq} = \frac{4kT}{R_4} \cdot (\frac{R_4}{\frac{1}{gm_{Q_2}} + R_4} \cdot \frac{1}{gm_{Q_1}G})^2 = 6.25 \times 10^{-22}\,\frac{\mathrm{V}^2}{\mathrm{Hz}}$$

$$\overline{E}^2_{nR_5eq} = \frac{4kT}{R_5} \cdot (\frac{R_5}{R_5 + \frac{1}{gm_{Q_1}}} \cdot \frac{1}{gm_{Q_1}G})^2 = 2.94 \times 10^{-22}\,\frac{\mathrm{V}^2}{\mathrm{Hz}}$$

$$\overline{E}^2_{nS_veq} = \frac{\overline{S}^2_v}{(R_5 // \frac{1}{gm_{Q_1}})^2} \cdot (\frac{R_5}{R_5 + \frac{1}{gm_{Q_1}}} \cdot \frac{1}{gm_{Q_1}G})^2 = 0.28 \times 10^{-18}\,\frac{\mathrm{V}^2}{\mathrm{Hz}}$$

$$\overline{E}^2_{nS_ieq} = \overline{S}^2_i \cdot (\frac{R_5}{R_5 + \frac{1}{gm_{Q_1}}} \cdot \frac{1}{gm_{Q_1}G})^2 = 64 \times 10^{-24}\,\frac{\mathrm{V}^2}{\mathrm{Hz}}$$

The input noise that we want to calculate is in the order of:

$$\overline{E}^2_{nJfet} = \frac{4kT\gamma}{gm_{JFET}} = 36.8 \times 10^{-18}\,\frac{\mathrm{V}^2}{\mathrm{Hz}}$$

Looking at these value, the target noise is way higher than all the others, so the requirements are meet. A representation of the bias point obtained with these values is in fig.4.8.

4.5 Measurement Setup

A photo of the real setup can be seen in fig.4.9. It is composed by two boards, connected thanks to two rectangular connectors, male and female, in a modular fashion. They are:

- **Carrier board**, in which the detector that should be examined is wire bonded;
- **Noise board**, composed by the analog parts, as the source follower and the OPAMP.

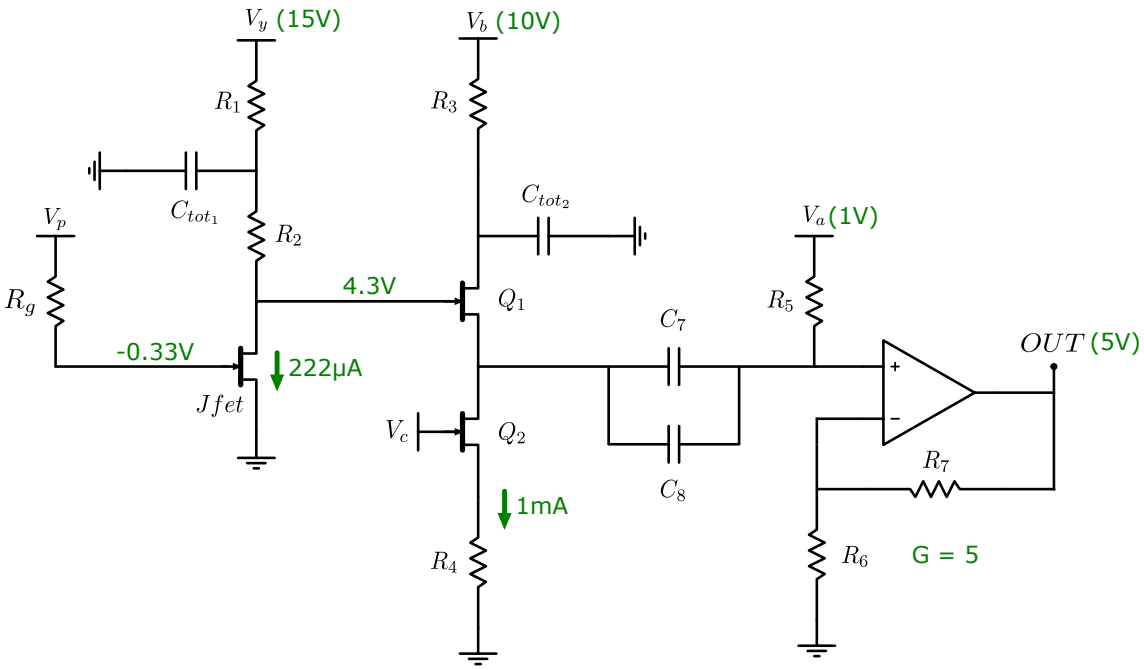


Figure 4.8: *Noise setup biasing value.*

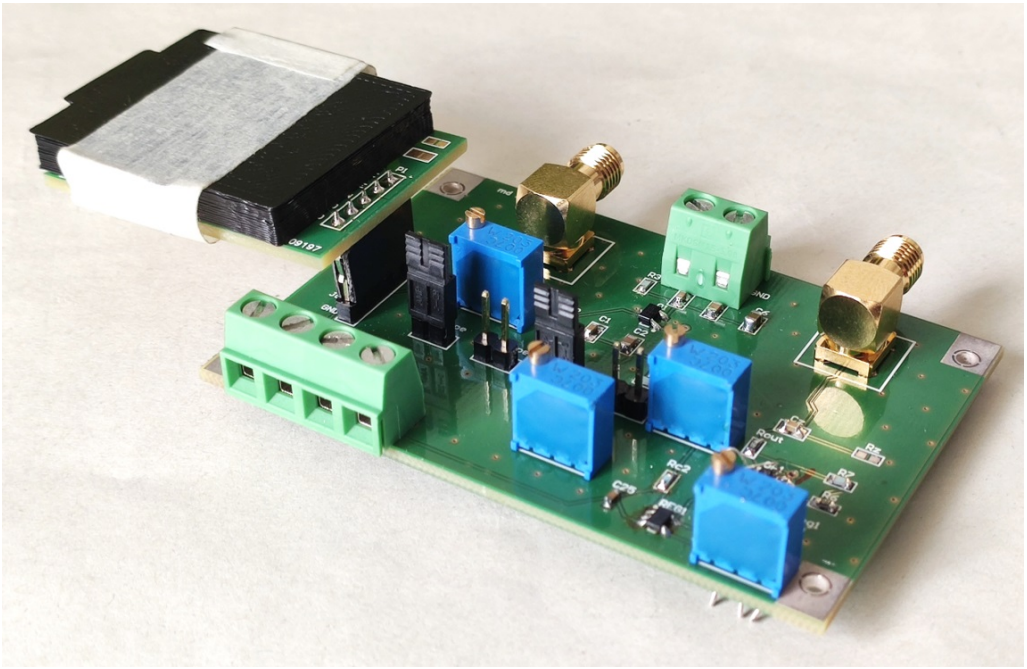


Figure 4.9: *Image of the noise setup, without external generators and SA.*

Since the space for the bondings on the detector side is quite limited, it can not be used an already bonded detector for this kind of measurements. The bonding wire would simply not connect to the corresponding pad. Detaching an already bonded detector for this noise test would mean to lose it for further testing. For this reason all the following measurement are made using a single pixel detector made with the same process technology of the 12 pixels one, of which spares ones were available.

On the detectors it is present an additional JFET, for test purposes, in addition to the ones integrated in the SDD pixels. This additional JFET has the exact same properties of the integrated ones. Unfortunately additional test JFET couldn't be used in this work, because an unoptimized process made it unusable, so the integrated JFET has been directly tested with the following strategy:

- **Drain**: the contact is easily accessible;
- **Source**: as the drain, the access of it is straightforward;
- **Gate**: the contact is reached from the anode, through the undepleted substrate.

As we can see in fig.4.10 the carrier board has the space for the test of even bigger detectors, having the detector slot as big as the 47-pixel detector. The detector is glued on the board using an adhesive foil, allowing it to be reused if necessary. C_{gx}, the capacitance that enables the calculation of the transfer function or the calculation of the output noise, is placed in this board, in order to have it as close to the JFET as possible. In fig.4.10 are present the fundamentals bias voltages for the JFET, namely DRAIN, GATE, SOURCE and the inner guard ring IGR. The JFET would still work with a floating IGR, with the only difference of presenting an higher bias current, so, it has been decided to bias the IGR contact to the value which is normally used for the SDD operation. For what regards the noise setup board, we can see a photo of it in fig.4.11, with dimensions of 50 mm x 75 mm. There are present jumpers made to enable the n-FET or the p-FET configurations. In addition, the four trimmers allow to change the polarization of several part of the circuit: TRIM1 changes the gate voltage of the testing JFET, TRIM2 the gate voltage of transistor Q2, TRIM3 changes the positive power supply of the OPAMP,

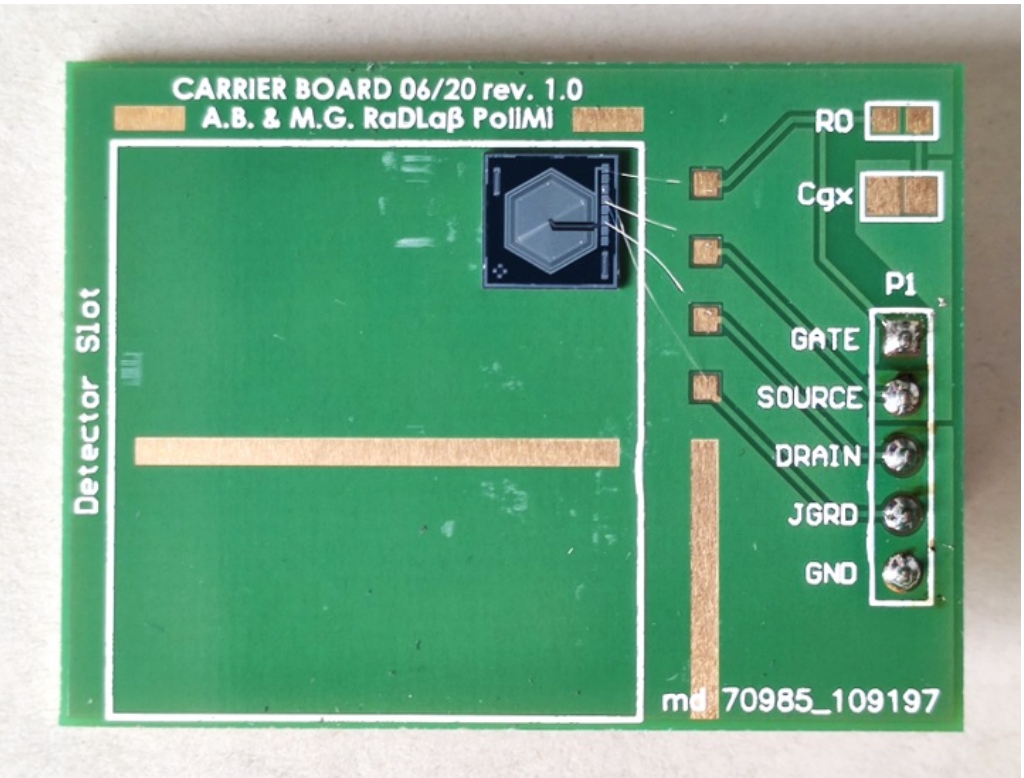


Figure 4.10: *Zoom on the carrier board of the noise setup. Its dimensions are* 30 mm × 40 mm.

TRIM4 the bias voltage at the positive input of the OPAMP. All the supply voltages have a low-pass filter at around 16 Hz. At the output we have a decoupling capacitor to make an high-pass filter of always 16 Hz, in order to match the specifications of the SA. All the supply voltages are provided using two benchtop power supply, using some Phoenix Contact connectors. Instead, the signals IN and and OUT are brought to the SA using two SMA connectors.

4.6 Measurements

The biasing points needed for the following measurements were already defined, as we have discussed in chapter III. To make a further check, we have used an Keysight B1500A Semiconductor Parameter Analyzer, an all in one analyzer supporting current-voltage (I-V), to plot the integrated JFET characteristics.

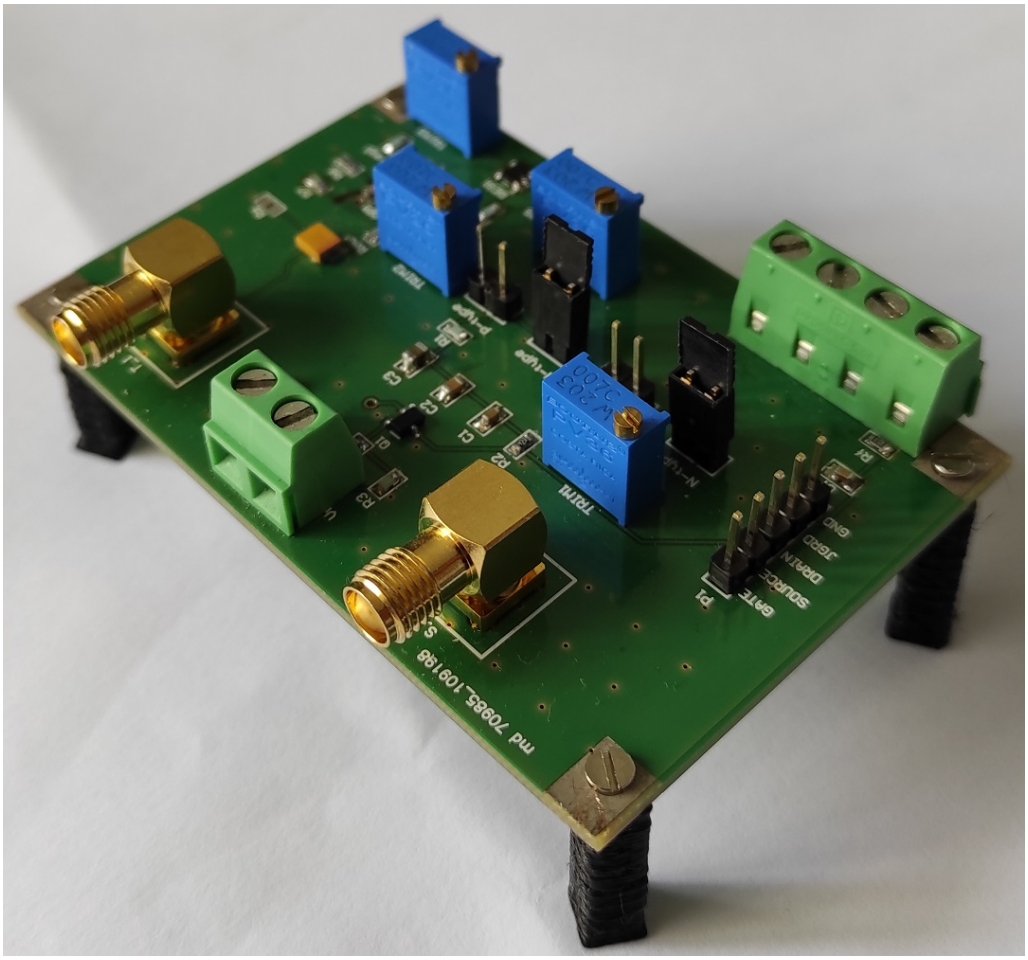


Figure 4.11: *Noise board of the noise setup.*

Using this, it has been assured that the integrated JFET was working correctly. The resulting measures were in line with the expected results and a correct behaviour for different V_{gs} of the JFET as been found (fig.4.12). After that, the successive steps are pretty straightforward.

The calculation of the transfer function is done by the SA. The main parameters used for it are:

- $f_{start} = 10\,\text{Hz}$
- $f_{stop} = 20\,\text{MHz}$
- Resolution Bandwith Width $RBW = 10\,\text{Hz}$

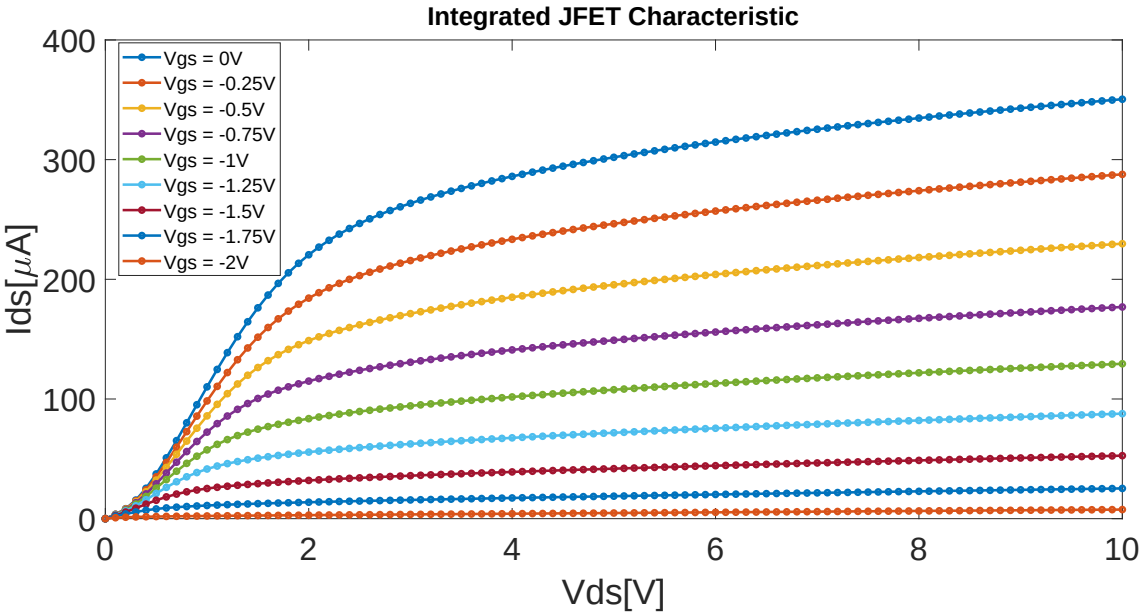


Figure 4.12: *Integrated JFET's characteristics.*

The data are all sent to a PC using a combination of a custom connector (HP-IB, a type of 8-bit interface) and a MATLAB program, that allows to setup all the parameters of the SA without acting physically on it. The resulting TF for a single pixel made with the same process as the TRISTAN ones is represented in fig.4.13.

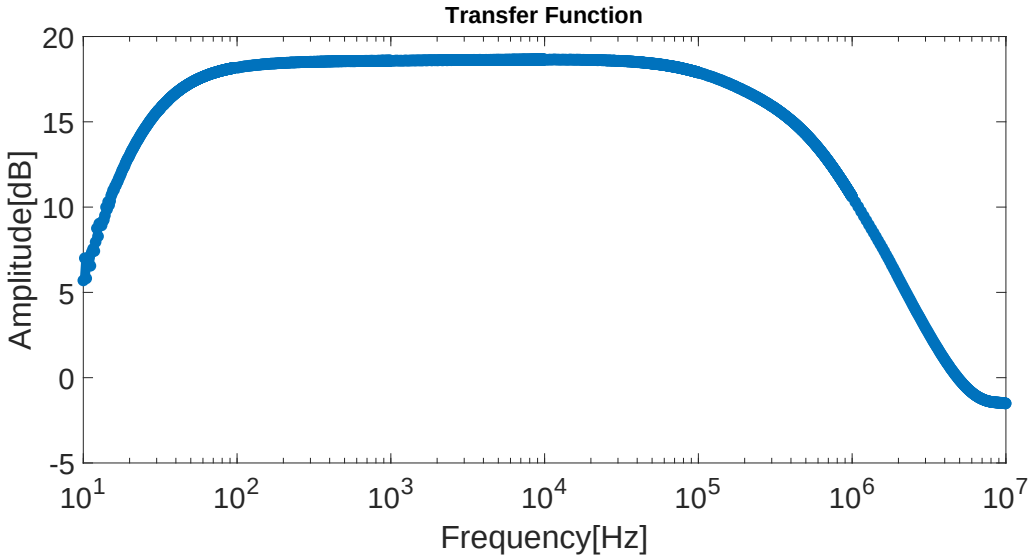


Figure 4.13: *Transfer function plot of a single pixel detector, TRISTAN like.*

For what regards the phase following the TF assessment, the measurement of the output noise, unfortunately the SA showed a Noise Floor (NF) higher than our noise of interest. The usage of an additional oscilloscope with a lower internal noise was forced. The parameters used in it are equal to the ones of the SA. The image in fig.4.14 shows the Fast Fourier Transform (FFT) of the output noise of the setup, after an average on the histogram to have a smoother waveform.

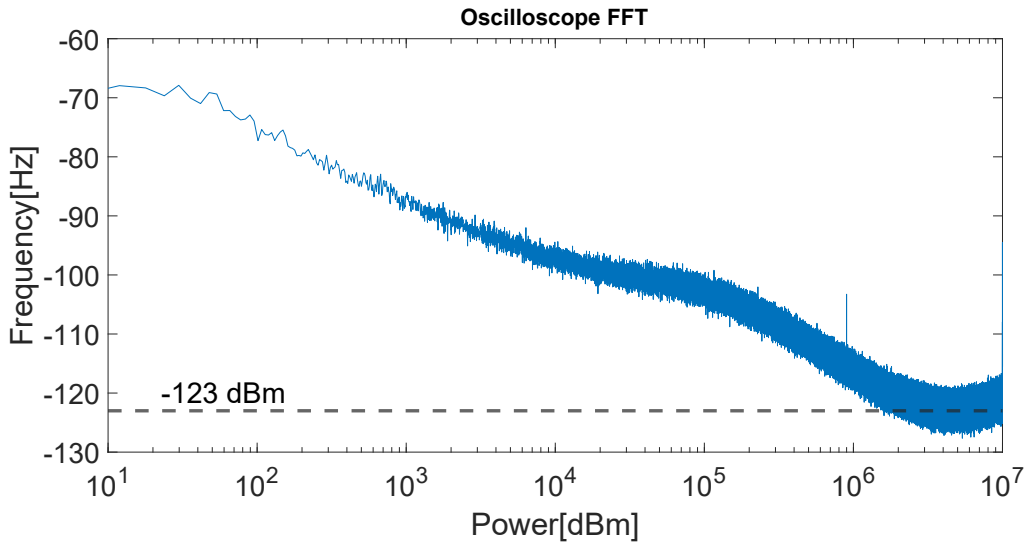


Figure 4.14: *Oscilloscope's Output Noise FFT, averaged.*

The oscilloscope gave the FFT of the noise in power and not in voltage amplitude. For this reason we need to convert this quantity in a more reasonable one, considering the fact that it is all normalized with respect to a power of 1 mW and a matching impedance of 50 Ω. The noise that we expect is in the order of $6\,\frac{\text{nV}}{\sqrt{\text{Hz}}}$ and the converting process follow this steps:

$$S_{out} = \sqrt{G^2 \cdot \frac{4kT\gamma}{g_m}} = \sqrt{G^2 \cdot white\ noise}\left[\frac{V}{\sqrt{Hz}}\right]$$

with G the gain of the total circuit,

$$S_{out} = \sqrt{\frac{1\,\text{mW} \cdot 50\,\Omega \cdot 10^{\frac{x_{dBm}}{10}}}{RBW}}\left[\frac{V}{\sqrt{Hz}}\right]$$

Equaling the two expressions we find:

$$x_{dBm} = 10 \cdot log \frac{white\ noise \cdot RBW \cdot G^2}{1\,\mathrm{mW} \cdot 50\,\Omega} \approx -123\,\mathrm{dBm}$$

This is the level of the theoretical noise that we expect in the ideal case. Of course the following plots, that are in $\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$, are converted using the inverse of the above formula, so:

$$noise^2 = \frac{1\,\mathrm{mW} \cdot 50\,\Omega \cdot 10^{\frac{x_{dBm}}{10}}}{G^2 \cdot RBW} \left[\frac{V^2}{Hz}\right]$$

The resulting real noise plot, along with the curves made from the theoretical ones, white and 1/f noise, can be seen in fig.4.15.

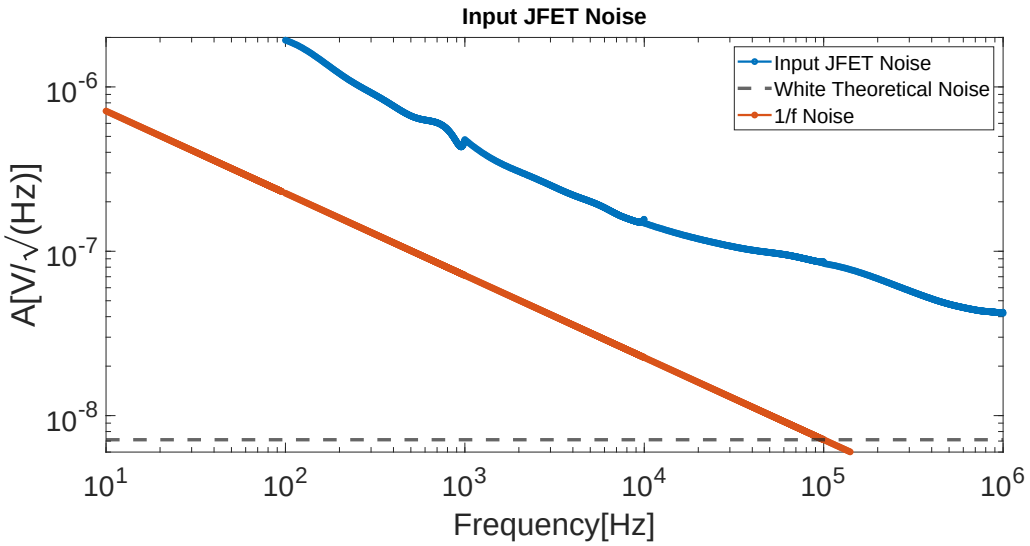


Figure 4.15: *JFET's input noise.*

The higher-than-expected noise is confirmed by other SDD setups in the TRISTAN collaboration. The colleagues of MPG-HLL have done similar testing in order to check if the problem was caused at a device level. Their results highlighted the presence of a contact resistance between the silicon structure and the contact metal higher than what it should be ($\approx \Omega$), in the order of 10 kΩ. On top of that it behaves as a non-linear one, giving a non white noise contribution in terms of power spectral density.

A model of its presence in our system can be seen in fig.4.16 even if it is a simplified one, since the resistance is considered linear and they are considered only the white noises.

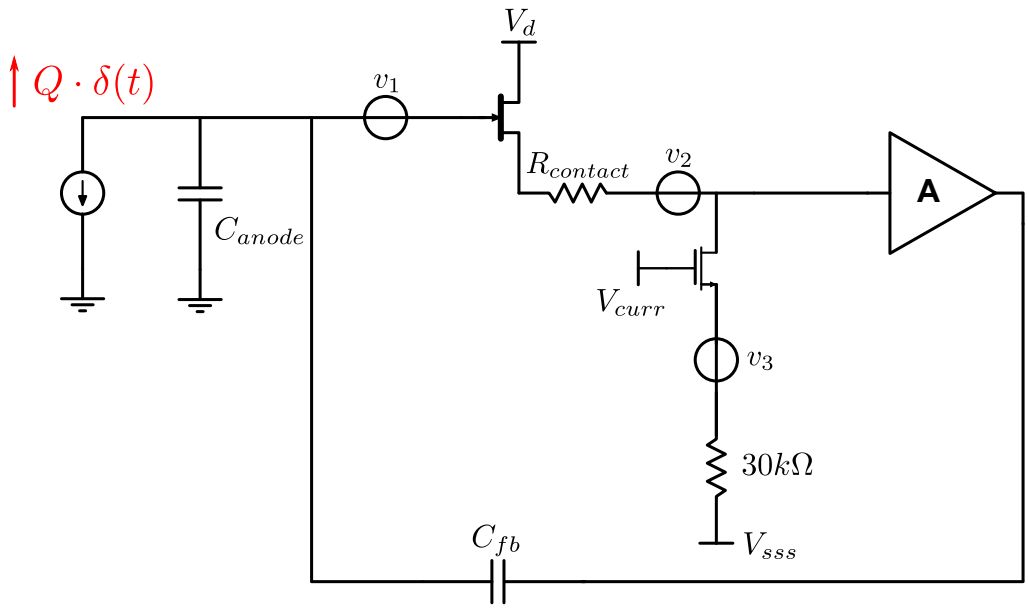


Figure 4.16: *Contribution of noise of the additional contact resistance in the JFET.*

At the input of the JFET we have:

$$v_{1eq} = \frac{4kT\gamma}{g_m}$$

$$v_{2eq} = \frac{4kT}{g_m^2 \cdot R_S}$$

$$v_{3eq} = 4kTR_{contact}$$

and calculating the contributions, we find a total white noise doubled with respect to the expected one.

The possible reasons for this problem could be:

- An incomplete sintering of the metal;
- An incomplete etching of the contacts, creating an insulating layer between metal and silicon.

For what regards the first problem, an additional thermal treatment may fix the sintering of the metal, however there are limits on the temperature tolerance of the passivation. Testing a temperature of 350 °C for 3 hours and later one of 450 °C for 3 hours gave no significant results.

The second one have a possible brute-force repair, the breaking of the insulator layer. This could be achieved using high values of currents or voltages, like blowing a fuse. Even if it is not a fancy method, it appears to work in a very simple test structure which was present on the wafer together with the SDDs, as we can see in fig.4.17.

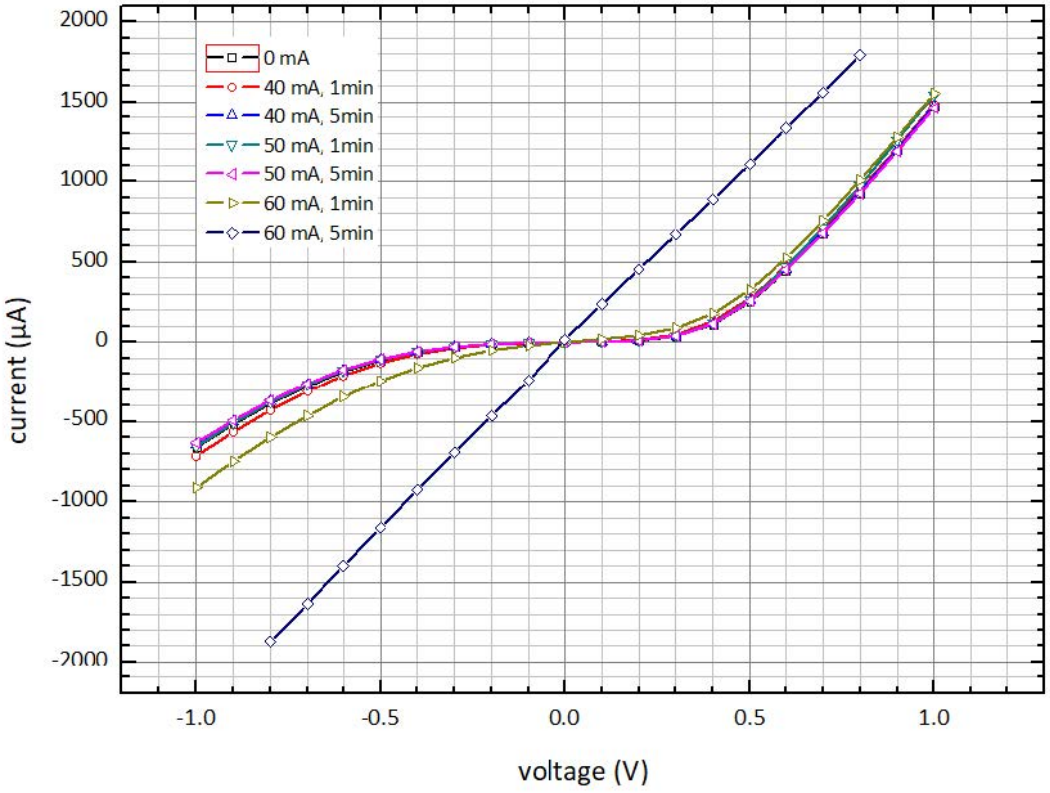


Figure 4.17: *Currents and voltages of the test contact after the cure using high current.*

However, it presents some drawbacks:

- It depends on the currents and voltages application times.
- It is dangerous, very close to the destruction limit of the contact.
- It is probably not applicable for multi-cell devices or, in general, in an SDD without causing any permanent damage.

It is clear that a lot of additional work is required, at manufacturing level, in order to fix this problem.

5 | Test Board 47 channels

This chapter is focused on the description of the test board made for the 47-channels ASIC board. First of all there is a description of why it is needed, and the tests which it can perform. Then a description of the schematics and the components used are given. Finally it can be seen the prototype board, with screenshot taken from its measurements.

5.1 Overview

Given the complexity of the TRISTAN detector, the large number of components and interconnects, the high density that requires non-standard fabrication and assembly procedures, it is important to provide test solutions for individual components across the whole assembly process. Here we present a board that allows testing the ASIC board in the absence of the detector. Two main aspects need to be checked: the correct polarization voltages for the SDDs and the correct behaviour of the ETTORE ASICs on the preamplifier board.

The testboard presented in the following does exactly that. For what regards the polarization voltages, it is able to display on screen to the user, on a custom program, the values set by the bias board and by ETTORE. For what regards the functionalities of ETTORE to be tested, they are mainly three, and a series of multiplexers (MUXs) allow to choose the desired channel to observe:

Input current generators test

This is a test on the current generators of each channels of ETTORE. Having a wrong current brought down by these generators would lead to problems on the polarization current of the detector, completely changing its working points. As we can see in fig.5.1, this is mainly done looking at the voltage drop on a test resistor, and converting this value in a current that the user can immediately see.

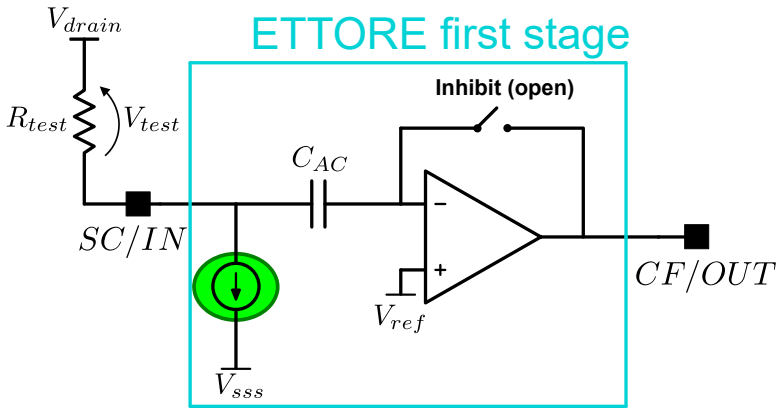


Figure 5.1: *Input current generators test applied by the testboard.*

Inhibit test

To check if the outputs of the ASICs are correctly bonded and that the amplifier is alive, the inhibit test is performed. Basically, applying a periodic inhibit signal to all the channels the output should saturate to 3 V when the inhibit is not active, and be equal to 800 mV when the inhibit is activated and the loop is closed. The periodic inhibit signal is generated in the microcontroller of our board and sent to the ETTORE ASIC through an SMA connector placed on the bias board. In fig.5.2 a simplified schematic of this test is shown.

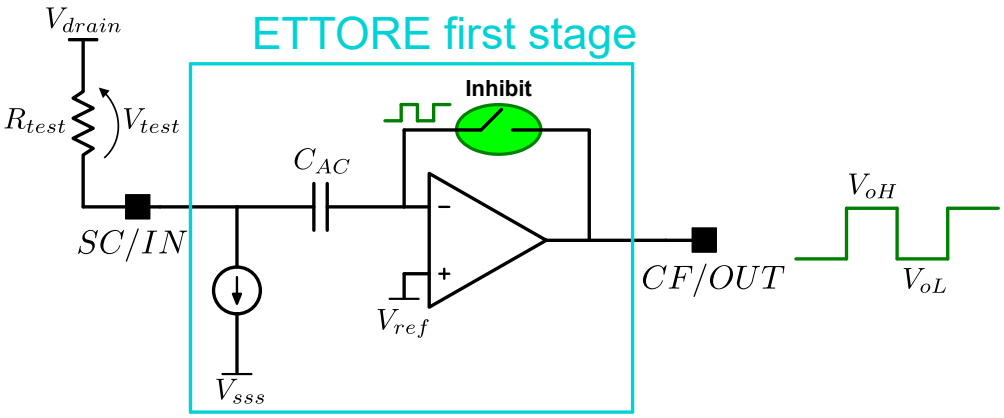


Figure 5.2: *Inhibit test applied by the testboard.*

Injection test

To examine the behaviour of different channels individually, the injection test is performed. Having an external capacitor C_{test} connected to each input, a square wave is injected ($V_{iH} = 250\,\text{mV}$ and $V_{iL} = 0\,\text{V}$), and the first stage of ETTORE, being in an open-loop configuration, acts as a comparator. When the square wave is applied we expect a square wave with opposite slopes at the output, saturating at 3 V and 0 V. In fig.5.3 the usual representation. In principle from this test it can be studied also the crosstalk between close channels, by stimulating one channel with the square wave and checking the output of the other ones.

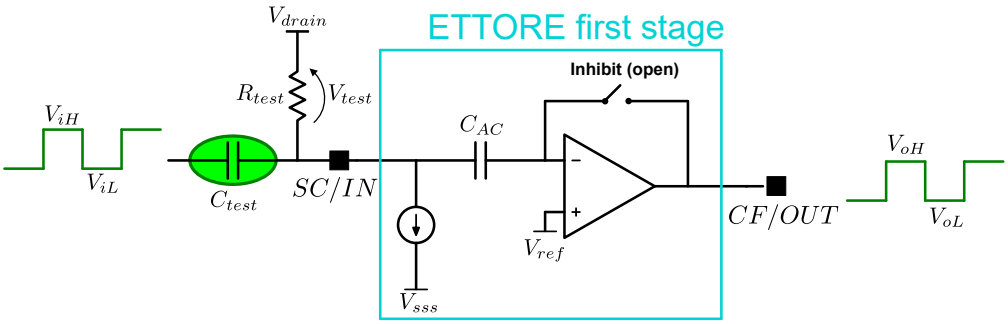


Figure 5.3: *Injection test applied by the testboard.*

5.2 Circuit Design

The main protagonist of this board is the microcontroller. It is a STM32F401RBT6, developed by STMicroelectronics. The main features used in this microcontroller are:

- It can operate with power supplies from 1.7 V to 3.6 V;
- The clock frequency can go up to 84 MHz (using an external oscillator);
- It features a 12-bit ADC with 16 multiplexed channels;
- It contains an USB 2.0 OTG full speed (FS) interface, with speeds up to 12 Mbit/s.

Along with several programmable pins, from the total number of 64. A full image with all the pins used and their functionalities is shown in fig.5.4. Of course they are used even the programmable pins, SWDIO, SWCLK and NRST, along with all the power supply voltages. The microcontroller has an analog part biased to 3.3 V used mainly for the ADC, and a digital one, also biased to 3.3 V. There are three pins used for debugging purposes that drive three LEDs of three different colors, that can be programmed to be switched on and off at any desired time.

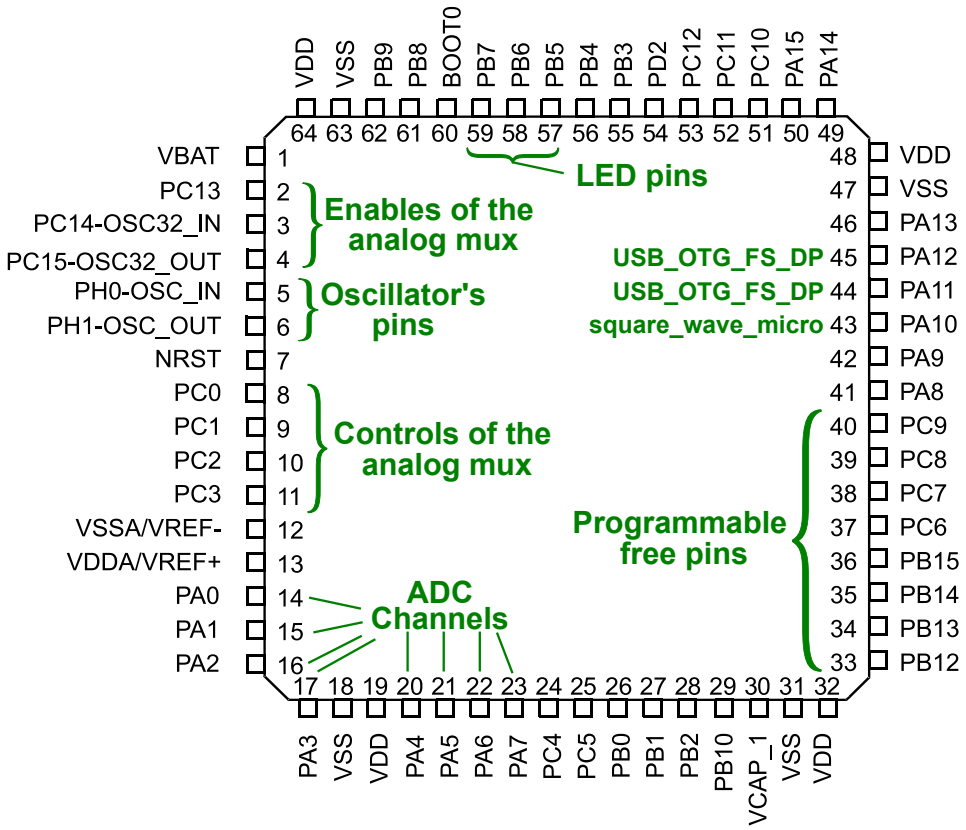


Figure 5.4: *Pin-out of the microcontroller used in the test board 47 channels, with marked pins and their specific function.*

As already anticipated, the connections on all the channels of ETTORE are mainly two: the IN contact and the CF contact. The first one is directly connected to the source of the testing JFET, the other one is responsible for the feedback signal of the circuit, making it a negative looped one.

To recall this concept, a representation of the ETTORE circuitry in correspondence of this two pads can be seen in fig.5.5.

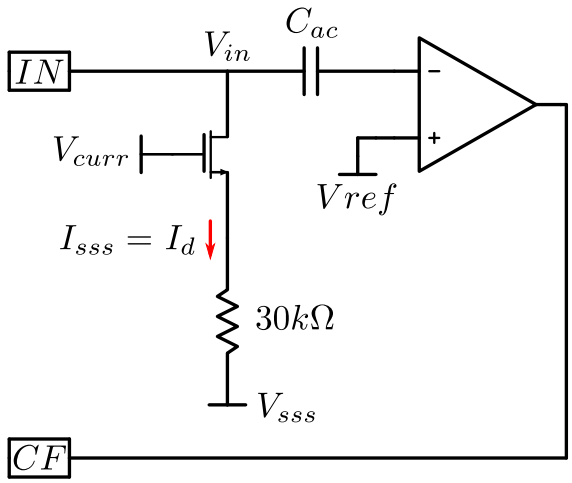


Figure 5.5: *IN and CF contacts on the ETTORE ASIC of a single channel.*

These two pads are the ones that allow to check all the correct functioning of all the channels. To be able to check a single channel per time, a pair of analog multiplexers 16:1, developed by Analog Devices Inc., was used. The control bits of this multiplexer are setted thanks to the microcontroller on the board, programmed using the custom QT interface. The signals that control the MUX are basically 5: one is the Enable bit, the other ones select the channel using a bit code on three pins, A3, A2, A1, A0 (e.g. 1000 is the 9th channel, being 0000 the first one). In this way the user can select the desired channel for the testing in a easy way. The MUX schematic is in fig.5.6. Both the multiplexers have the same enable bits and control ones. Since the MUXs have only 16 channels, three pair of them have to be used, to reach the 47 channels needed (one of them is left unconnected). The current I_{sss} of all the channels is measured simply converting the potential difference on the R_{test} to a current using a correction factor, all this is processed by the microcontroller.

For what regards the polarization voltages, they are all read by the microcontroller using the internal ADC. Since the ADC of the microcontroller is biased between 0 V and 3.3 V, it has a Full Scale Range(FSR) corresponding to that range and at its input it allows only signal of that magnitude. Most of the signals are well beyond that limit (the highest is ≈ -120 V), so a resistive divider is needed

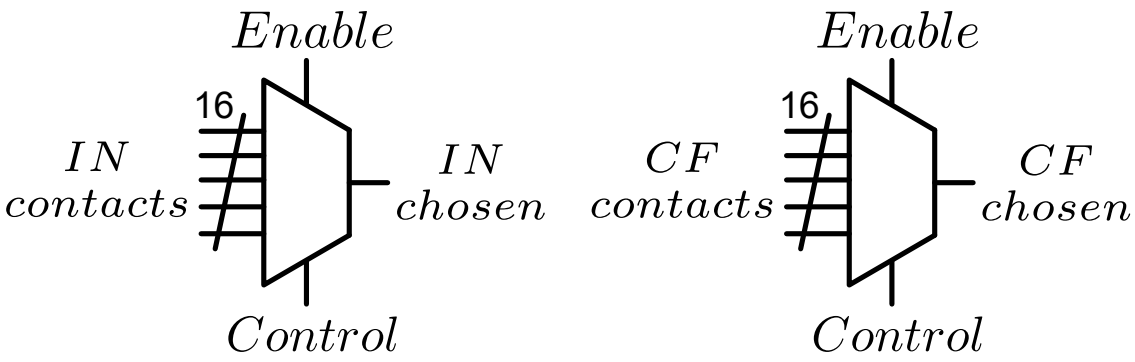


Figure 5.6: *MUX of the IN and CF contacts for the ETTORE ASIC.*

to rescale the voltage to the FSR of the ADC. Of course, the positive voltages, like V_{drain} are all read using an OPAMP in a non-inverting configuration, and the negative ones are read using an inverting configuration. On top of that, protection diodes are present in all the OPAMPs to avoid any possible damage due to uncontrollable voltage spikes. As example for this readout, we have the schematics both for positive and negative SDD bias signals in fig.5.7.

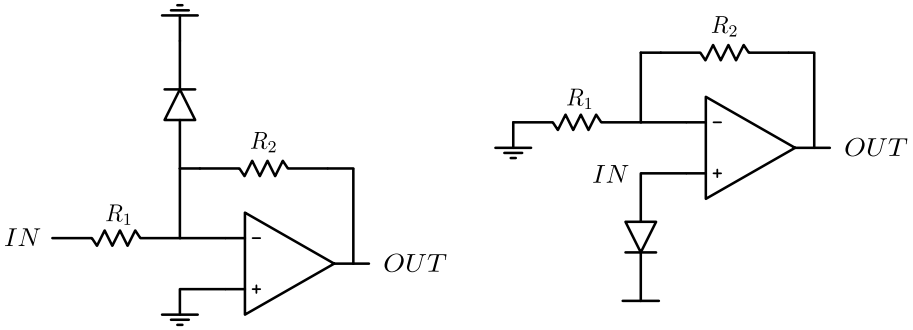


Figure 5.7: *Readout of the polarization signals to the microcontroller. In the left for negative ones, in the right for the positives.*

The programming of the board is done using an external discovery board (STM32F4DISCOVERY) which integrates a programmer interface. To correctly program the board two things are absolutely necessary: the pins SWCLK, SWDIO, NRST and GND have to be connected between both the boards, and a correct firmware to be deployed with the STM32CubeIDE software. The discovery board is not the only board that can be used to program the microcontroller, the only requisite is to have an ST-LINK/V2, which is a debugger and programmer for the

STM8 and STM32 microcontroller families. The pins used in the discovery board can be seen in tab.5.1 and in fig.5.8.

Pin	CN2	Designation
1	VDD_TARGET	VDD from application
2	SWCLCK	SWD clock
3	GND	Ground
4	SWDIO	SWD data input/output
5	NRST	Reset of target STM32
6	SWO	Reserved

Table 5.1: Debug connector CN2 pins.

All the electronics in this board is powered thanks to a simple micro usb connector. This connector has a basically two functions. One of them is that, connected to every PC, this kind of connector is able to provide 5 V and 500 mA, which are more than what it is required by the board. The other one is the exchange of the data with the PC, through Data - and Data + pins, that are respectively the contacts USB_OTG_FS_DM and USB_OTG_FS_DP in fig.5.4 on page 106. The pins of a micro usb port are listed in tab.5.2.

Pin	Name	Description
1	VDD	+5 V DC
2	D-	Data -
3	D+	Data+
4	ID	Mode detect
5	GND	Ground

Table 5.2: Micro USB pins.

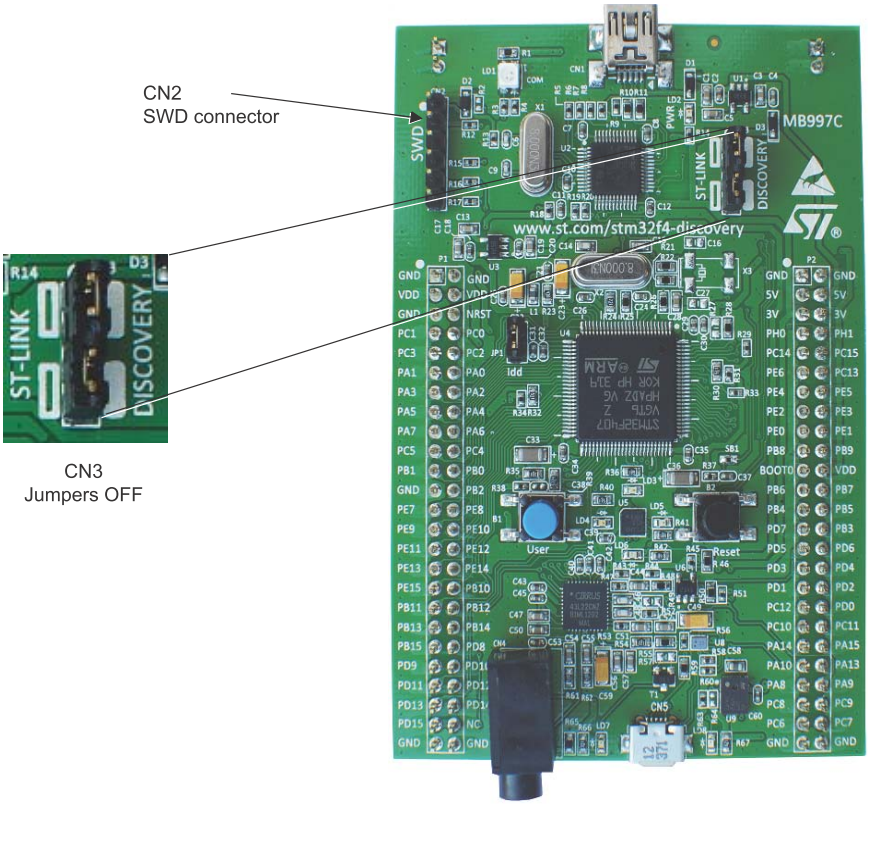


Figure 5.8: *STM32F4DISCOVERY connections used for programming.*

To be able to pilot correctly the data of the USB, the microcontroller requires an external oscillator. For this specific case it was decided to use an ECS crystal oscillator of 8 MHz. Using a Phase Locked Loop implemented directly in the microcontroller, there is the possibility to use frequencies up to 84 MHz.

The connector to the ASIC board is always the same Samtec connector, in order to simulate as close as possible the presence of a real detector board.

5.3 Fabrication and test

In the end the real board, bonded and connected to the setup, can be seen in fig.5.9.

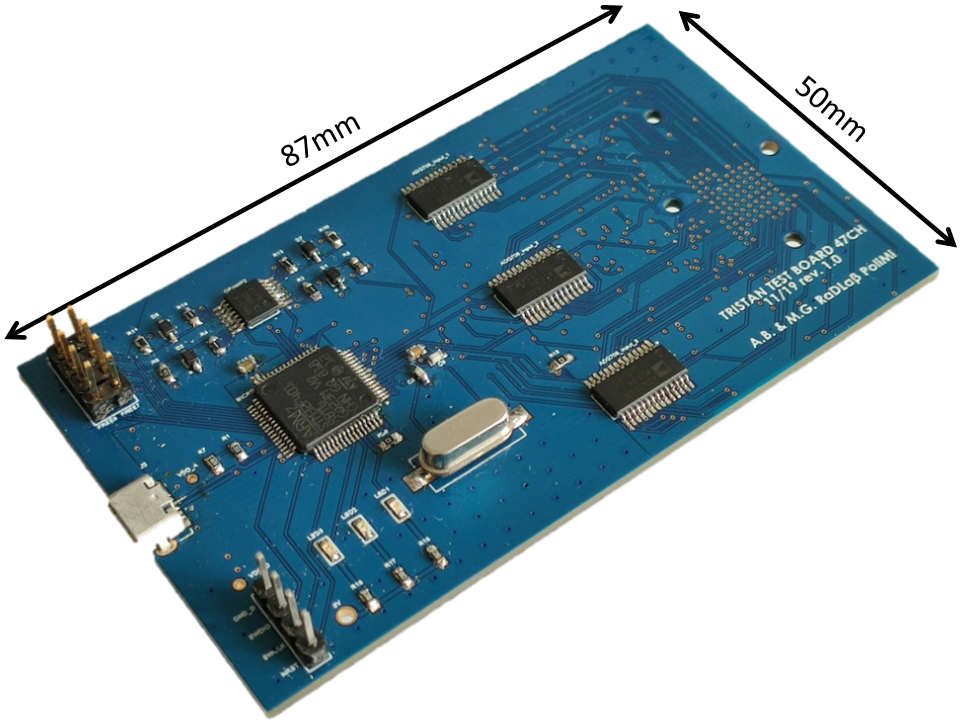


Figure 5.9: *Test board for the 47 channels setup, with highlighted dimensions.*

The connection to the ASIC board is really simple. From an already existing 47 channels setup the only action required is the replacement of the 47 channels detector board with the test one. In this way the testing time and the recovery of a measurement setup are greatly reduced. All the tests carried by this board are processed within an ambient temperature, so there is no need to use an hermetic box to conduct the measures. The only additional space is due to the micro usb connector, needful for the correct operation. A zoom of the 47 channels setup with the test board can be seen in fig.5.10. As anticipated, all the data is processed by the micro, and sent to the PC using the USB FS interface.

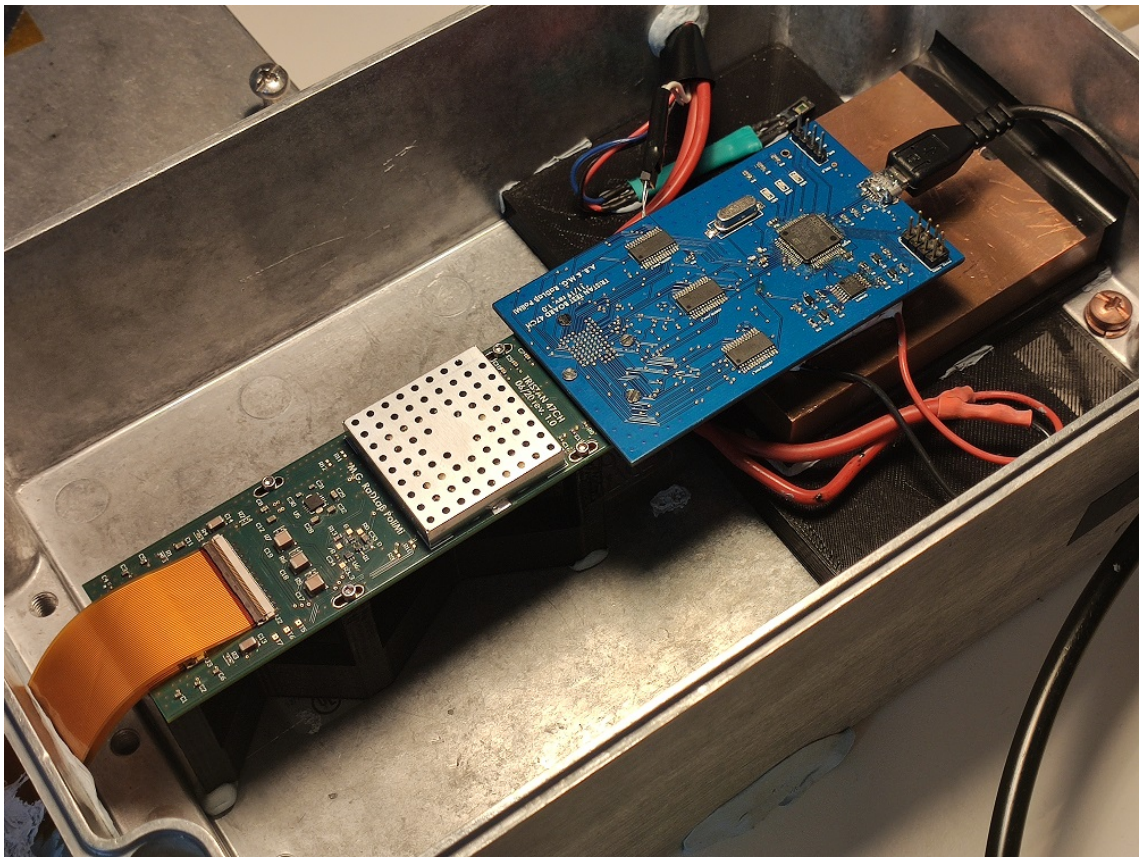


Figure 5.10: *Test board connected in a real, fully working 47 channels setup.*

The program that receive this data is developed using QT, a free and open-source widget toolkit, mainly used for creating Graphical User Interfaces(GUIs) in a simple way. All the software can be compiled in C++ and using custom commands unique for QT. The graphical interface developed is self explanatory to be as user friendly as possible. The combination of the two programming Integrated Development Environment(IDE), namely STM32CubeIDE and QT creator, with a common interface based on sending and receiving "char" data, allowed some advanced functionalities, such as the reprogramming of the microcontroller software. As an example, the injection test discussed before needs a faster ADC configuration compared to the one used for the measurements of the DC bias. The latter can be slower, for obvious reasons, while the former has to correctly acquire square-wave signals, which are way faster. For this task a reprogram of the internal ADC of the microcontroller is needed, hence it is a very useful feature. A screenshot of the QT interface is shown

in fig.5.11.

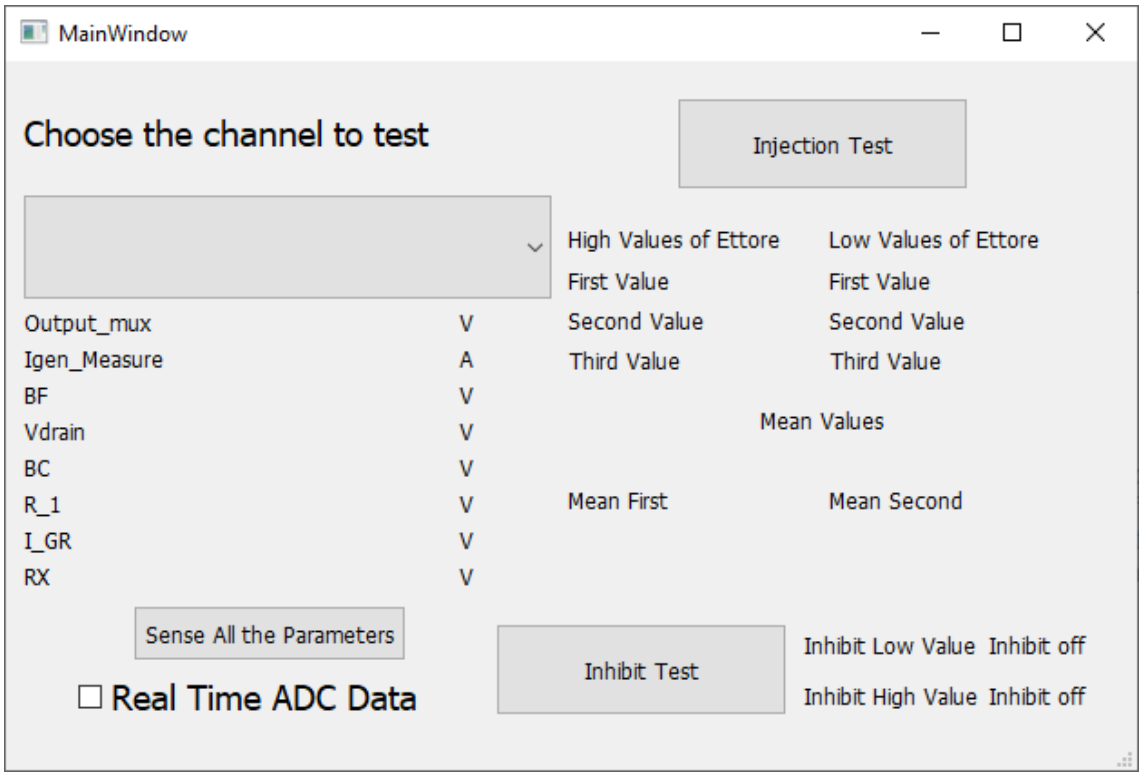


Figure 5.11: *Screenshot of the QT interface.*

As additional feature, this board can be used for the reset pulsing on the bias board, in order to correctly check the correct behaviour of the ETTORE ASIC to this working function. This test board was being developed having in mind the 47 channels setup, but nothing prevents its use to test the 12 pixels, the 7 pixels and even a single pixel setup.

6 | Conclusions and Future Developments

This thesis is carried out in the context of the TRISTAN project, an international collaboration which aims at discovering a new type of particle, the sterile neutrino. Its existence would explain several astrophysical phenomena, and would give new informations regarding the composition of the dark matter. The study of the tritium β-decay spectrum is done using a particular kind of detector, the SDD. Right now the working prototypes are the 12-pixel and the 47-pixel ones. The work of this thesis is basically focused on three main tasks: the experimental characterization of these two experimental setups, to investigate the unexpected noise components which has been observed, and the creation of a 47 channels ASIC test board.

Concerning the experimental setup of the 12 pixels, it was noticed that it is fully working, having however a contribution of the series and 1/f noise higher than what theoretically expected. Further investigations are currently in progress, to check the reason of this behaviour, from the device level to the electronics readout. The 47 pixels setup has been tested with the 12-pixel detector and gives results similar to the previous one. This means that it is ready for the characterization with the new 47-pixel SDD matrix. The 47-pixel detector is now wire bonded on its detector board, and the tests on this setup are ongoing right now. The noise test board allows to check the unexpected noise of the integrated JFET of our detector. Thanks to that, we were been able to identify that one of the noise problems is at device level, being it probably caused by an unfortunate production issue. However, being the complete system really complex and with a lot of novel electronic components, investigations of the main sources of this noise are currently in progress by the whole collaboration. The 47 channels ASIC test board performs three different tests: input current generators test, inhibit test and injection test, along with checking the correctness of the bias voltages for the SDDs. The main feature is that it allows to test the functionality of the ASIC preamplifiers, mounted on the TRISTAN modules, without the need for detectors, which is useful considering the limited number chips

that are present in the TRISTAN collaboration. It is able to test even setup with less pixels, like the single one. The board is fully functional and ready to be shipped to the rest of the collaboration.

The future development of TRISTAN continues having as main objective the realization of the 166-pixel SDD detector. Since the final system will have 21 modules, one close to each other, a 2D design as the one of the 12 pixels and 47 pixels presented in this thesis will not be feasible. A 3D design, where the SDD matrix is perpendicular to the preamplifier boards, requires special rigid-flex PCBs which have already been designed and are in manufacturing phase. A rendering of what the system will be like (in its 3D 47 pixels version and the final 166 pixels one) is represented in fig.6.1. The final 166 SDDs detector will use two rigid flex PCBs and a pair of ASIC boards, as opposed to the 47 channels that needs only one of each.

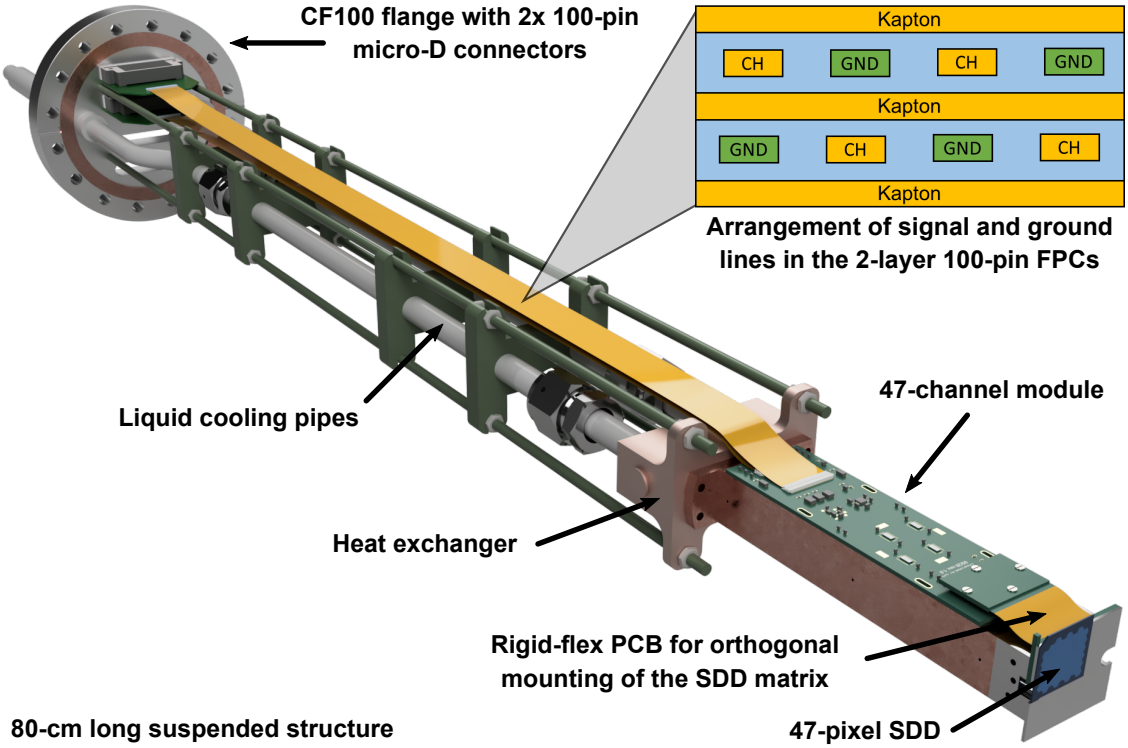


Figure 6.1: *3D design for the 47 pixels module.*

A CF100 flange, which separates the detector's vacuum to the air-side electronics, will have a total of 4 micro-D Airborn connectors, each with 100 pins.

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