POLITECNICO
MILANO 1863

SCUOLA DI INGEGNERIA INDUSTRIALE
E DELL'INFORMAZIONE

Executive Summary of the Thesis

Nanofabrication and characterization of spin-orbit logic devices

Laurea Magistrale in Engineering Physics - Ingegneria Fisica

Author: Giovanni Gandini

Advisor: Prof. Christian Rinaldi

Co-advisor: Federico Fagiani

Academic year: 2021-2022

1. Introduction

From the advent of the complementary metal oxide semiconductor (CMOS) based transistors, electronics has been able to cope with the demanding trend of Moore's law through improvements in the fabrication processes and architectures, while the core of the technology has not changed. However, CMOS devices are currently facing the so-called Boltzmann's tyranny, which dictates an upcoming limit on the scaling of logic devices. An alternative solution to go well-beyond the CMOS paradigm is therefore necessary. Among many technologies at study, one of the most promising paths is the *magneto electric spin-orbit* (MESO) logic, proposed by Intel in 2019 [1]. MESO logic owes much of its success to the combination of ultra-low energy state switching and integrabilitiy in the CMOS fabrication process. Furthermore, the use of the collective switch of ferroelectricity and ferromagnetism grants the non-volatility of information, allowing to combine memory and logic functionalities within the very same physical space [2].
The working principle of a MESO device relies on the presence of a nanomagnet to store information and *spin to charge conversion* (SCC) effects in materials with strong spin-orbit-coupling (SOC) to read-out such information. While the realization of the complete structure has never been achieved so far, MESO read-out stage was demonstrated by V.T.Pham *et al.* in 2020 [3] taking advantage of a bilayer device made of a spin-orbit material structure on whom a magnetic injector was deposited. The aim of this thesis is to implement a similar process for the fabrication of the read-out stage, with the long-term goal of incorporating novel materials to increase the efficiency of the device. The first section of this summary will explain the working principle of the MESO logic and the read-out unit, motivating the approach of this thesis towards spintronics-based beyond-CMOS technologies. Then we will present the fabrication process developed at PoliFab, the micro and nanofabrication facility of Politecnico di Milano. Finally the properties of the read-out stage will be studied through the electrical characterization of devices built with different materials combinations and techniques.

2. MESO technology and read-out stage

The MESO device, being an electronic switch, can be divided in two functional units, one used to *write* the information state and one able to generate an output which is a function of that

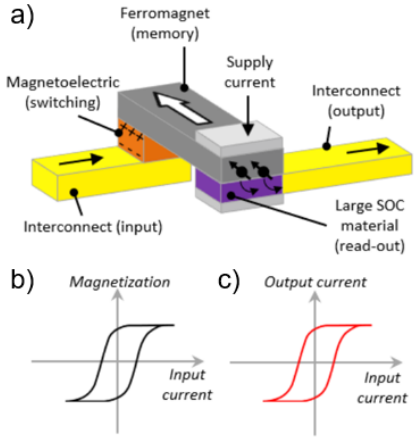

Figure 1: *a)* Structure of a MESO device as conceived by Intel, divided in the writing (*rear*) and read-out (*front*) functional units. *b)* Relation between the input current and the magnetization of the FM layer through the writing unit. *c)* Relation between input and output current showing how, through the read-out stack, it is possible to affect the output current.

state, thus allowing for information processing or *read-out*. The structure of the MESO device, shown in Fig. 1, reflects the presence of the two functional units as two different stacks connected by a ferromagnetic (FM) layer, used to store information.
The *writing* stack is built by a ferroelectric (FE) and a ferromagnetic (FM) layer, coupled via magneto-electric effect as to contemporaneously switch the polarization and magnetization states. The working principle of this unit is based on the use of an input current, able to generate a voltage drop sufficient to switch the polarization of the FE layer and allow to *write* information through the simultaneous 180° switch of the nanomagnets' magnetization. The read-out stack is instead formed by the FM and a strong spin-orbit coupling material. The working principle of this unit is based on the use of the nanomagnet to inject a spin-polarized current (I_{in}) into the spin-orbit material, where it is converted to a transversal charge current (I_{out}) via spin-to-charge conversion effects (e.g. spin Hall effect [4], Edelstein-Rashba effect [5], ecc.). The sign and magnitude of the output current will be therefore dependent on the direction and degree of spin polarization of the current injected in the SOC layer. Thus, this

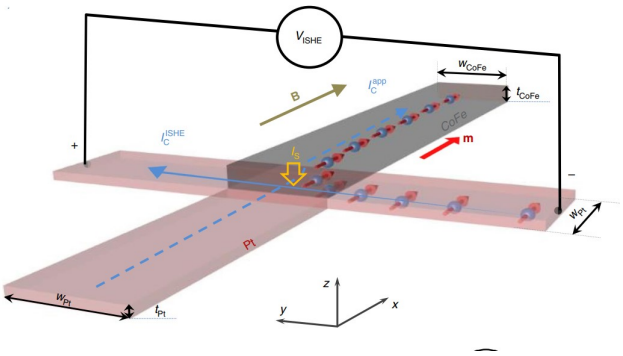

Figure 2: Representation of a bilayer device for the measure of read-out efficiency. Overall the complete device will be shaped as a cross, one of the two branches will be only built by a SOC material (along y in the image), whereas the other branch (along x) will be built by aligning a ferromagnetic (FM) material with the remaining SOC channel. Adapted from ref. [3].

transistor can produce an output current with sign and magnitude depending on the magnetization state of the nanomagnet in which the information is stored. The read-out process was studied by V.T.Pham *et al.* using platinum-based devices in which the same working principle is applied to an open circuit configuration, in which the equivalent current is translated into a charge accumulation, i.e. in a voltage difference (V_{ISHE}), as shown in Fig. 2.
One of the main benefits claimed by Intel about the MESO logic concerns the efficiency of the read-out process, which shows an almost unlimited gain scaling the device's dimensions, unlike what happens with CMOS, for whom this trend is limited below 50 nm. The read-out efficiency can indeed be defined as [3]:

$$\eta = \frac{I_{out}}{I_{in}} = T * \frac{\lambda_{eff}}{w_{FM}} \tag{1}$$

where T takes into account the spin injection efficiency from the FM the the SOC material, w_{FM} is the width of the ferromagnetic injector and λ_{eff} is an equivalent length that describes the efficiency of the spin-to-charge conversion process. This thesis will focus on materials in which the spin-to-charge conversion is provided by Inverse Spin Hall Effect (ISHE) [4], so that λ_{eff} is given by the product of the spin diffusion length (λ_s) and the spin Hall angle (θ_{SH}), a parameter used to quantify the conversion of

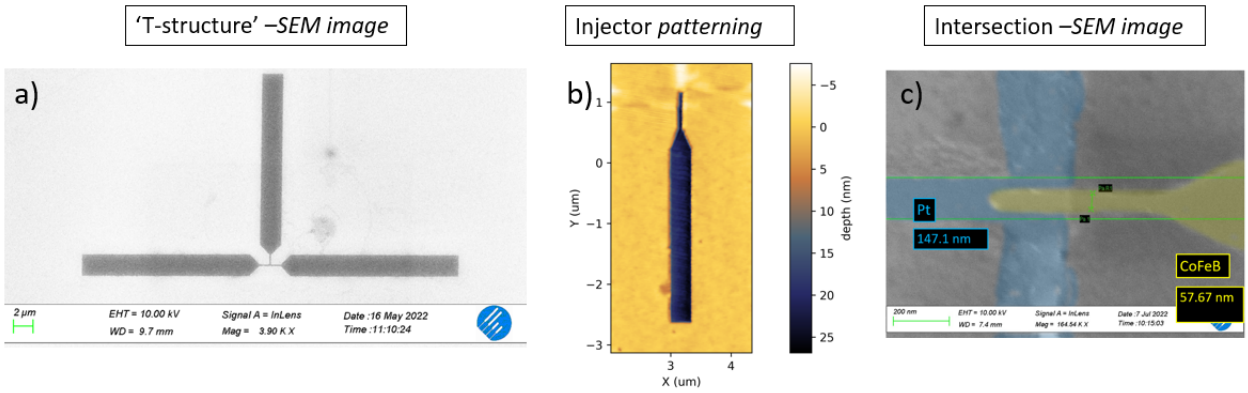

Figure 3: *a*) Electron microscopy image showing the deposited 'T-structure'; *b*) AFM image showing the patterning of the magnetic injector at the intersection of the horizontal and vertical branches of the 'T-structure'; *c*) SEM image showing the result of the first and second step for a Pt-CoFeB heterostructure, a width below 60 nm was achieved for the deposited magnetic injector thanks to optimized t-SPL.

a charge current ($\boldsymbol{J_c}$) into a spin current ($\boldsymbol{J_s}$) by ISHE as:

$$\boldsymbol{J_c} = \theta_{SH} \boldsymbol{J_s} \times \boldsymbol{\sigma} \tag{2}$$

where $\boldsymbol{\sigma}$ is the direction of the spin polarization. In an open circuit configuration (as shown in Fig. 2), the figure of merit used to quantify the read-out efficiency is instead the difference in $R_{ISHE} = \frac{V_{ISHE}}{I_{in}}$ measured with opposite magnetizations of the nanomagnet [3]:

$$\Delta R_{ISHE} = \frac{\lambda_{eff}}{\left(\frac{t_{FM}}{\rho_{FM}} + \frac{t_{NM}}{\rho_{NM}}\right) w_{NM}} \tag{3}$$

where t is the thickness, ρ is the resistivity and w is the width of the interconnections. Eq. (3) can be related through a geometrical factor to the read-out efficiency of the MESO logic shown in eq. (1). According to Intel [2], the ideal value of η to achieve atto-joule energy per reading is in the range $90 - 100$ %. In [3] however, using a Pt-CoFe heterostructure, the authors were able to retrieve a value of $\eta = 0.1$ %, with a width of the magnetic interconnection of about 50 nm.
To achieve an higher read-out efficiency and be able to take full advantage of MESO's scaling law, materials with $\lambda_{eff} > 20 - 50$ nm are auspicable. The extremely low figure found for standard materials as Pt ($\lambda_{eff} \approx 0.05$ nm), Ta ($\lambda_{eff} \approx 0.1$ nm) and W ($\lambda_{eff} \approx 0.15$ nm) [2] calls for the study of novel promising materials with higher spin-to-charge conversion efficiency, as for example GeTe ($\lambda_{eff} \approx 1$nm) [6], SnTe ($\lambda_{eff} \approx 5 - 10$ nm), Bi_2Se_3 ($\lambda_{eff} \approx 10$ nm) [7] or $LaAlO_3/SrTiO_3$ ($\lambda_{eff} \approx 10$ nm) [8].
In this thesis we aimed at developing a suitable fabrication process for the read-out devices. In particular our efforts were focused on the study of *thermally assisted scanning probe lithography* (t-SPL) [9] for the patterning of the magnetic injector. T-SPL's working principle, based on using an heated tip to sublimate the uppermost layer of a resist stack, also allows for an AFM (atomic force microscopy) scan of the sample surface, thus providing a simple and effective method to align the desired pattern with pre-existing structures. Furthermore, this technique offers the highest resolution available at Polifab, allowing to verify the scaling of the read-out efficiency. Finally, thanks to its imaging capabilities and the non-destructive nature of the patterning process, t-SPL is considered particularly promising for the lithography of 2D materials [10] and ferroelectric Rashba semiconductors (FERSC) [11], which are among the most interesting solutions to increase λ_{eff}.

3. Nanofabrication

Here the three step process employed for the nanofabrication of the read-out devices will be presented. A combination of *electron beam lithography* (EBL), *thermally assisted scanning probe lithography* (t-SPL) and standard *optical lithography* was used for the three subsequent lithographic steps.
SOC layer: The first step of the nanofabrica-

tion process was the patterning and deposition of the material responsible for spin-to-charge conversion (SOC layer). SiO_2/Si substrates were spin-coated with a PMMA (*polymethyl-metacrylate*) resist, patterned via electron beam lithography (EBL) and developed in a *methyl isobutyl kethone*(MBIK):*isopropanol* (IPA) solution. About $6-7$ nm of tantalum or platinum were deposited using either evaporation or sputtering deposition as to vary the material's resistivity and thus the spin-to-charge conversion efficiency, as well as to understand the adhesion to the substrate offered by different techniques. The remaining resist was then removed in a *lift-off* process. A proper optimization of the resist thickness, the current dose and the development time allowed to reach the resolution limit of the available system (*LEO 1525 SEM/EDX/EBL* by *Raith* and *Zeiss* [12]). A critical size of $80-90$ nm was achieved for SOC interconnects.

FM injector: The second step is the patterning and deposition of the magnetic 'finger' used for the injection of spin polarized currents in the T-shaped structure by thermally assisted scanning probe lithography (t-SPL) using the *Nanofrazor Explore* by *Heidelberg-Swiss Litho* [13] and a *Polyphthalaldehyde* (PPA)/PMMA bilayer resist [14]. As shown in Fig. 3b the uppermost layer of the resist stack (PPA) was used as a positive thermal resist, sublimating in contact with the hot tip and allowing to write the desired pattern. The developement in a 1:20 H_2O in IPA solution allowed to transfer the pattern to the second layer (PMMA), used to thermally isolate the sample and facilitate the lift-off process. The magnetic material was then deposited using either sputtering (CoFeB/Ru) or evaporation (NiFe/Ti). The use of a sputtering machine also allowed for an in-situ *soft-sputter etch* of the contact surface between the SOC and FM layers. A proper capping layer (either Ru or Ti) was used to protect the nanomagnet against oxidation from the solvents used in the subsequent lithographic step. An example of the final device after the liftoff is shown in as shown in Fig. 3c .
To overcome the $100-120$ nm resolution limit declared by *Heidelberg*, our work focused on the optimization of both the tip writing parameters

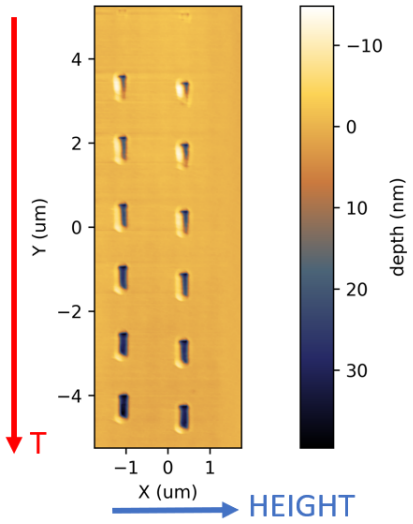

Figure 4: The optimization of the high-resolution patterning in t-SPL was achieved by writing matrix of features of critical size varying the writing parameters. This process was possible thanks to ad-hoc Python scripts developed during the thesis work,allowing to identify the optimal set of parameter for a specific t-SPL tip. Here the temperature and height of the tip vary respectively from top (700°C) to bottom (880°C) and from left to right ($240-250$ nm).

and the resist thickness. The optimization of the tip parameters was done controlling the instrumentation in a python-coding environment and writing *optimization matrices* to understand the role of different parameters in achieving the best resolution. An example of such matrices is reported in Fig. 4. This process showed the necessity of a compromise between the patterning depth and its resolution, respectively directly and inversely proportional to the tip's temperature. As a result, the PPA was therefore diluted to a 1 % solution in anisole, reducing the film's thickness from 30 to 20 nm to allow for a shallower and higher resolution patterning. Also the PMMA was diluted in a 1:2 solution in PGME, reducing the thickness of the second layer (from 110 to $60-70$ nm) and shortening the development time and the consequent undercut profile. Overall the optimization process allowed to increase the resolution of a factor 2 i.e. reaching a critical feature size of about 60 nm, better than that of our EBL (80 nm). However, the

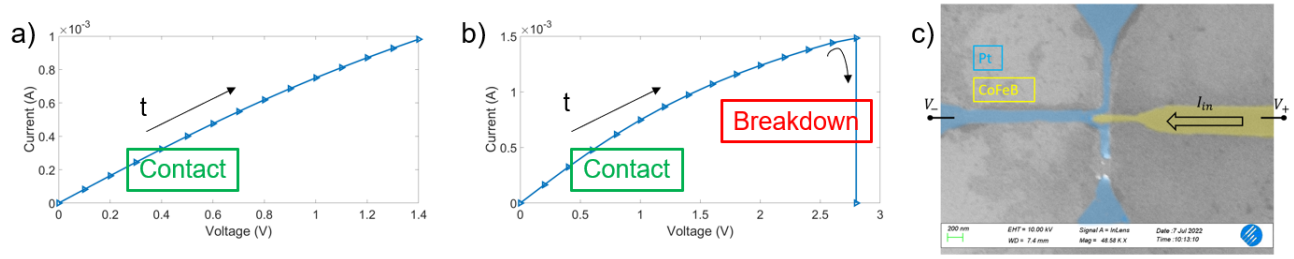

Figure 5: Current vs voltage (I-V) curves measured along a Pt-CoFeB path. The channel shows an almost linear behaviour below 0.8 V (a), while a breakdown is reached at current densities of about $2 * 10^8$ A/cm^2 corresponding in this case to 2.8 V (b). A SEM image of the device is shown in panel c).

much lower throughput of the writing process with respect to EBL and a lower yield in the lift-off process must be considered.

Electrical pads for measurements: The final step of the fabrication process was devoted to the contact pads used to allow the electrical connection of the nanostructure with the measurements setup. Given the micrometric size of the necessary features, optical lithography was chosen for this step. After patterning, the contacts were deposited evaporating a Cr(5nm)/Cu(150 nm)/Au(25 nm) stack, where the Cr film is an adhesive layer, while Au is used to prevent the oxidation of Cu.

4. Device Characterization

Through the process previously described it was possible to successfully fabricate the read-out devices, which were then studied to retrieve some relevant information on the electrical behaviour of the heterostructures and the deposited materials.

Breakdown Current: Given the low efficiency of the read-out mechanism, high input currents are necessary to obtain a significant output signal, requiring the study of the maximum injectable currents. This value was retrieved using a sourcemeter, which allowed to measure the IV characteristic of each channel until breakdown, as shown in Fig. 5 for the case of a Pt-CoFeB channel. A SEM analysis allowed to relate the breakdown to an opening of the channel in the region where the design would narrow to 60−100 nm and the resulting boost in the dissipated power would burn the channel. The maximum operating voltages were found in the order of

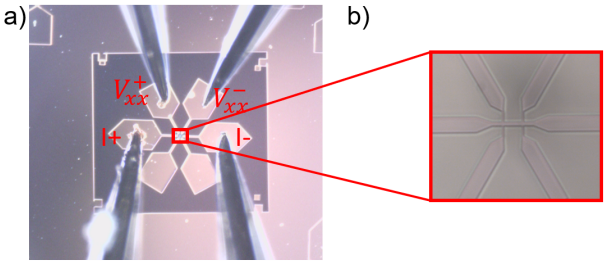

Figure 6: a) Microscope image of the Hall Bar and the micro-probes' configuration used to measure the resistivity. b) Structure of the Hall bars used for the measurement.

1.5 − 3 V for Pt and 15 − 20 V for Ta, with resistances in the order of 10^3 Ω and 10^5 Ω, respectively. The corresponding current densities were found in the order of 10^8 A/cm^2 for Pt based heterostructures and 10^{6-7} A/cm^2 for Ta based heterostructures, thus showing how our devices can be safely operated in the range (10^6 A/cm^2) commonly used for spin-to-charge conversion [3]. Remarkably, some of the devices have shown sensitivity to even small static charges breaking during measurements.

Resistivity: We then focused on the study of the resisitivity of the deposited metals, critical to estimate the output signal (eq.(3)). The first studies were done using Pt Hall bars realized with a combination of e-beam lithography and sputtering deposition. Using a four-contact configuration (as shown in Fig. 6) we were able to estimate the resistivity of the deposited platinum as $\rho_{SOC} = 29.12 \pm 0.54\ \mu\Omega cm$.

The values of resistivity found using the Hall bars resulted comparable with those calculated from a 2-probes measurement on the actual devices. The values found for the resistivity of

different materials are summarized in table 1. If compared with the results in [3], our Pt shows low resistivity whereas our Ta seems to be slightly more resistive. The particular results obtained for Ta can be either ascribed to the partial oxidation of the channel, reducing the effective conductive section, or to the different deposition technique (evaporation instead of sputtering) used. From the results found in [15], relating θ_{SH} and λ_s of Pt (at 10°K) to its resistivity, and considering $w_{Pt} = 100$ nm, we can calculate the expected output signal from eq.(3) as $\Delta R_{ISHE} \approx 40m\Omega$.

Material	$\bar{\rho} \pm \sigma_\rho$ [$\mu\Omega cm$]
Pt	40 ± 10
Ta	7900 ± 4700
CoFeB	165 ± 55
NiFe	160 ± 10

Table 1: Effective resistivity of metallic thin films as measured in nanosized devices fabricated in this thesis work. For the case of NiFe, given the small number of data available the range was used instead of the standard deviation.

Read-out. To measure the efficiency of the state read-out mechanism the value of $R_{ISHE} = V_{ISHE}/I_{app}$ was finally measured versus a sweeping external magnetic field, trying to identify the presence of an hysteresis loop, as expected from magnetization-dependent spin-to-charge conversion (see Fig. 1c). The measurements were performed using a four probes station and using a magnetic field up to 0.2 T. Fig. 7, shows an example of such measurement versus field on a Ta/CoFeB device. So far, we haven't been able to measure a clear hysteresis loop in the resistance at room temperature on such range of magnetic field, despite a bistable state is sometimes detected in the scans. Further work is needed to achieve such a goal, fabricating a larger number of devices with the optimized recipe and investigating the spin-to-charge conversion in these system versus temperature, with higher magnetic fields and exploring several couple of ferromagnets and SOC layers.

5. Conclusions

The work behind this thesis allowed for the complete fabrication of the read-out unit of the MESO logic. From the fabrication perspective, the optimization of the resist stack and the writing parameters of t-SPL allowed to increase the declared writing resolution of almost a factor of 2, up to the limit of 60 nm. Moreover, a semi-automatic system was devised for the identification of the optimal writing parameters for a given resist, allowing to further push this limit in the future. The electrical characterization of the devices allowed to understand their operational limits (maximum current densities and operating voltages) and to retrieve relevant parameters to estimate the efficiency of the read-out process. Further work is however needed to improve the yield of the fabrication process (t-SPL lift-off in particular) and the robustness of the nanostructures (annealing of the samples to achieve strain relaxation and enhanced layer-to-substrate adhesion). Overall, the know-how acquired in both the fabrication and characterization of the spin-orbit devices, is a fundamental step in view of the investigation of spin-to-charge conversion mechanisms with innovative material platforms such as 2D materials or FERSC thin layers.

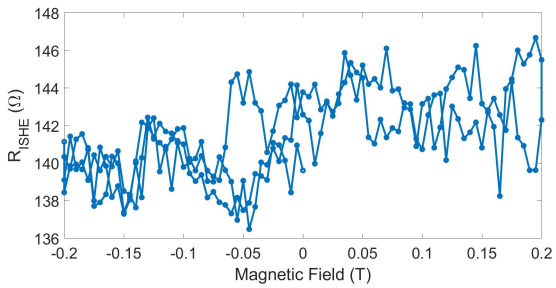

Figure 7: Equivalent output resistance versus magnetic field measured on a spin-orbit device up to 0.2 T at the four-probe station.

6. Acknowledgements

I want to thank Christian Rinaldi, Federico Fagiani, Luca Nessi, Matteo Cantoni and all the people that helped me at PoliFab. A special mention must be also given to my family and friends who always supported and endured me in these years.

References

[1] Sasikanth Manipatruni, Dmitri E Nikonov, Chia-Ching Lin, Tanay A Gosavi, Huichu

Liu, Bhagwati Prasad, Yen-Lin Huang, Everton Bonturim, Ramamoorthy Ramesh, and Ian A Young. Scalable energy-efficient magnetoelectric spin–orbit logic. *Nature*, 565(7737):35–42, 2019.

[2] Sasikanth Manipatruni, Dmitri E Nikonov, and Ian A Young. Beyond cmos computing with spin and polarization. *Nature Physics*, 14(4):338–343, 2018.

[3] Van Tuong Pham, Inge Groen, Sasikanth Manipatruni, Won Young Choi, Dmitri E Nikonov, Edurne Sagasta, Chia-Ching Lin, Tanay A Gosavi, Alain Marty, Luis E Hueso, et al. Spin–orbit magnetic state readout in scaled ferromagnetic/heavy metal nanostructures. *Nature Electronics*, 3(6):309–315, 2020.

[4] Jairo Sinova, Sergio O Valenzuela, Jörg Wunderlich, CH Back, and T Jungwirth. Spin hall effects. *Reviews of Modern Physics*, 87(4):1213, 2015.

[5] Aurelien Manchon, Hyun Cheol Koo, Junsaku Nitta, SM Frolov, and RA Duine. New perspectives for rashba spin–orbit coupling. *Nature materials*, 14(9):871–882, 2015.

[6] Christian Rinaldi, JC Rojas-Sánchez, RN Wang, Y Fu, S Oyarzun, L Vila, Stefano Bertoli, Marco Asa, Lorenzo Baldrati, Matteo Cantoni, et al. Evidence for spin to charge conversion in gete (111). *APL Materials*, 4(3):032501, 2016.

[7] AR Mellnik, JS Lee, A Richardella, JL Grab, PJ Mintun, Mark H Fischer, Abolhassan Vaezi, Aurelien Manchon, E-A Kim, Nitin Samarth, et al. Spin-transfer torque generated by a topological insulator. *Nature*, 511(7510):449–451, 2014.

[8] Edouard Lesne, Yu Fu, S Oyarzun, JC Rojas-Sánchez, DC Vaz, H Naganuma, Giuseppe Sicoli, J-P Attané, Matthieu Jamet, E Jacquet, et al. Highly efficient and tunable spin-to-charge conversion through rashba coupling at oxide interfaces. *Nature materials*, 15(12):1261–1266, 2016.

[9] Edoardo Albisetti, Annalisa Calò, Alessandra Zanut, Xiaorui Zheng, Giuseppe Maria de Peppo, and Elisa Riedo. Thermal scanning probe lithography. *Nature Reviews Methods Primers*, 2(1):1–21, 2022.

[10] Xiaorui Zheng, Annalisa Calò, Edoardo Albisetti, Xiangyu Liu, Abdullah Sanad M Alharbi, Ghidewon Arefe, Xiaochi Liu, Martin Spieser, Won Jong Yoo, Takashi Taniguchi, et al. Patterning metal contacts on monolayer mos2 with vanishing schottky barriers using thermal nanolithography. *Nature Electronics*, 2(1):17–25, 2019.

[11] Sara Varotto, Luca Nessi, Stefano Cecchi, Jagoda Slawinska, Paul Noël, Simone Petrò, Federico Fagiani, Alessandro Novati, Matteo Cantoni, Daniela Petti, Edoardo Albisetti, Marcio Costa, Raffaella Calarco, Marco Nardelli, Manuel Bibes, Silvia Picozzi, Jean-Philippe Attané, Laurent Vila, Riccardo Bertacco, and Christian Rinaldi. Room-temperature ferroelectric switching of spin-to-charge conversion in germanium telluride. *Nature Electronics*, 4:1–8, 10 2021.

[12] PoliFab. Sem with edx and ebl system – leo 1525 / raith elphy plus. `https://www.polifab.polimi.it/equipments/sem-ebl/`.

[13] PoliFab. Nanofrazor explore. `https://www.polifab.polimi.it/equipments/nanofrazor-explore/`.

[14] Nanofrazor recipe book. Technical Report v.1, Heideberg Instruments, 2020.

[15] Edurne Sagasta, Yasutomo Omori, Miren Isasa, Martin Gradhand, Luis E. Hueso, Yasuhiro Niimi, YoshiChika Otani, and Fèlix Casanova. Tuning the spin hall effect of pt from the moderately dirty to the superclean regime. *Phys. Rev. B*, 94:060412, Aug 2016.