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VERY LOW CONTACT RESISTANCE FOR GRAPHENE HIGH-FREQUENCY DEVICES

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Very low contact resistance for graphene high-frequency devices

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Abstract

Just one atom thick with newest and extraordinary properties, graphene is emerging as a fascinating material for many kind of applications. Thanks to its high carrier mobility at room temperature as well as to its saturation velocity, it reveals a great potential for high speed applications. Moreover it possess the largest heat transfer coefficient which allows better power dissipation. The 2D nature of graphene makes it a good candidate in substituting silicon, for which scaling is becoming problematic due to its intrinsic physical limitations. Because of the lack of a band gap, graphene field effect transistors (GFETs) are actually suitable for radio frequency (RF) applications, where a high power consumption can be acceptable in order to reach larger operational speeds. Despite its unusual properties, the route to large scale production is still long. The more studies on the material are done, the more problems have to be overcome to exploit its real potential. So far several integrated circuits (ICs) based on graphene transistors have been fabricated, but only few of them are able to perform operation at frequencies over 1 GHz. Increase of efficiency could be possible by scaling the dimensions of the IC components. However, once the sizes are reduced to the nanometric scale, the RF performances are deteriorated by the very high resistance of the metal-graphene contacts. Here it is reported a systematic study on the contact resistance including a novel methods for its reduction. This made possible to obtain the smallest value of the contact resistance so far reported in literature which are comparable with that of III-V High Electron Mobility Transistors. This result can open alternative ways to reach higher operational frequencies in graphene devices which today are seriously affected by the poor contact performance.

Estratto

A cosa serve il Grafene? "Non lo so. É come presentare un pezzo di plastica a un uomo di un secolo fa e chiedergli cosa ci si può fare. Un po' di tutto, penso" Andre Geim premio Nobel per la Fisica 2010.

Sono passati dieci anni dal momento in cui Andre Geim e Kostya Novoselov, riuscirono nell'impresa di isolare il primo materiale bidimensionale della storia: il grafene. Da quel momento una vera e propria corsa all'oro si è sviluppata intorno a quello che è stato definito come "il materiale delle meravigle". Spesso solamente un atomo, il grafene risulta allo stesso tempo flessibile e più resistente dell'acciaio, è otticamente trasparente e possiede una conducibilità termica superiore a qualsiasi altro materiale conosciuto. Ciò che ha portato questo materiale alla ribalta, sono le sue proprietà elettroniche che ne fanno un conduttore migliore del rame. Gli elettroni all'interno del reticolo bidimensionale del grafene si comportano come fermioni di Dirac, ovvero particelle prive di massa. Questo, oltre a permettere mobilità estremamente elevate anche a temperatura ambiente, fa sì che la loro velocità di saturazione sia solamente 300 volte inferiore a quella della luce. Il grafene presenta inoltre un marcato "effetto di campo" necessario per la realizzazione del componente base dell'elettronica moderna: il transistor. Oggigiorno non è facile per un materiale entrare nel mercato dell'elettronica integrata, attualmente dominato dal silicio. D'altro canto la continua riduzione delle dimensioni dei dispositivi sta generando diversi problemi, alcuni dei quali presentano delle barriere fisiche apparentemente insormontabili. Da qualche anno si stanno testando svariati materiali nella speranza di trovare una soluzione al problema della "scalabilità" dei dispositivi. La natura bidimensionale del grafene può spingere l'elettronica oltre questi limiti e quindi cospicui investimenti nella ricerca sono stati fatti anche da aziende leader nell'industria del silicio.

Benché le premesse siano molto incoraggianti, anche il grafene presenta alcuni problemi. Esso è infatti un semimetallo, ovvero non possiede un gap energetico che separa la banda di valenza da quella di conduzione, aspetto fondamentale per assicurare una buona distinzione tra gli stati di "on" e "off" di un transistor. Questo influenza la sua applicazione nel campo dell'elettronica digitale dove molti transistor vengono combinati per la realizzazione

di reti logiche. É invece il campo dell'elettronica analogica in cui il grafene può portare diversi vantaggi. Grazie all'altissima mobilità dei suoi elettroni è teoricamente possibile la creazione di dispositivi con frequenze operative oltre 1 THz . Diversi circuiti analogici più o meno complessi come moltiplicatori di segnale, amplificatori, e oscillatori ad anello sono stati prodotti con transistor in grafene. Tuttavia la loro massima frequenza operativa non supera i pochi GHz. Per poter raggiungere valori più alti una riduzione delle dimensioni caratteristiche dei dispositivi è necessaria. Tuttavia, come per il silicio, effetti cosiddetti "parassitici" pesano sempre di più sul bilancio globale delle prestazioni mano a mano che i transistor vengono scalati. Attualmente la maggior problematica per quanto riguarda i dispositivi in grafene risiede nella difficoltà di "iniezione" ed "estrazione" di cariche attraverso un contatto metallico. All'interfaccia tra i due materiali si genera una cospicua resistenza che limita la massima frequenza raggiungibile dal dispositivo stesso.

Questo lavoro di tesi si è proposto di analizzare l'interazione metallo-grafene tramite l'estrazione della cosiddetta "resistenza di contatto" (R_c). Come primo step si è definito un processo produttivo standard per le strutture da analizzare, consistenti in un una serie di transistor con differenti lunghezze di canale depositati su una striscia rettangolare di grafene su un substrato rigido di SiO_2/Si. Campioni contenenti contatti di metalli differenti sono stati prodotti e testati tramite l'uso del Transfer Length Method (TLM) che consente l'estrazione dei valori di resistenza di contatto. In questo step sono stati ottenuti valori di R_c molto bassi per elettrodi in oro puro. Successivamente tramite semplici trattamenti di etching, la zona di grafene sottostante il metallo è stata "patternata" permettendo un incremento del bordo di contatto tra gli elettrodi ed il grafene stesso. Questo ha provocato un'ulteriore diminuzione della resistenza di contatto fino ad un valore intorno ai $90\,\Omega$ µm che all'oggi risulta essere il più basso mai registrato.

Questo lavoro apre quindi una strada alternativa per la creazione di nuovi dispositivi basati su grafene in grado di operare a frequenze sempre più alte.

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1 Graphene

This chapter provide an overview on graphene as the building block for a new technological areas. Section 1.1 introduce graphene and its properties; section 1.2 gives a brief description of the band structure and carrier transport in graphene; section 1.3 go deeply exploring the new "exotic" *properties of this 2D material. The principal production methods, with drawbacks and advantages, are finally described in section 1.4.*

1.1 Introduction

In the early 60's Hanns-Peter Boehm were studying single-layer carbon atoms which, stacked one above another result in graphite, giving it the name of *"graphene"* [16]. Although the existence of this kind of material were known from years, only in 2004 A.K Geim and K.S. Novoselov, researchers of the center for Mesoscopic and Nanotechnology at the University of Manchester, were able to isolate and study a single layer of graphene [17] [5]. From that time, graphene has attracted the attention of a large part of the world's science community. Less then 4 Angstroms (Å) thick, it is composed by a set of carbon atoms with a sp^2 hybridization, packed in an hexagonal honeycomb lattice structure. The very high ratio between its flakes size and thickness, makes graphene the firs stable 2-dimensional crystal ever observed in nature. It can be considered as the building block for all the carbon-based systems (Figure 1.1): graphite is an ordered stack of graphene layers with an interplanar distance of about $3,34\,\text{Å}$, carbon nanotubes are rolled-up sheets of carbon atoms, and fullerenes, also known as *"buckyballs"*, are spherical shape nanostructures obtained wrapping-up graphene.

Since it re-discovery graphene caught the attention of many scientists because of its remarkable properties which promise future improvements in numerous technological areas. The possibility to make faster and smaller electronic devices, thanks to the very high carriers mobility [1] [18] and its stability even at room temperature [19], have been leaded to the rise of many new research groups which are currently building the scaffold for the develop of graphene-based devices. Other possible applications come from properties such as an extraordinary strength and flexibility [20], a very high thermal conductivity [21] and low interfacial thermal resistance [22], an optical transparency of about 98% of visible light [23], which make graphene suitable for purposes like optoelectronics [24], molecular sensors, energy storage systems [25], and many else.

Many eyes are focused on this new material and many critics have been

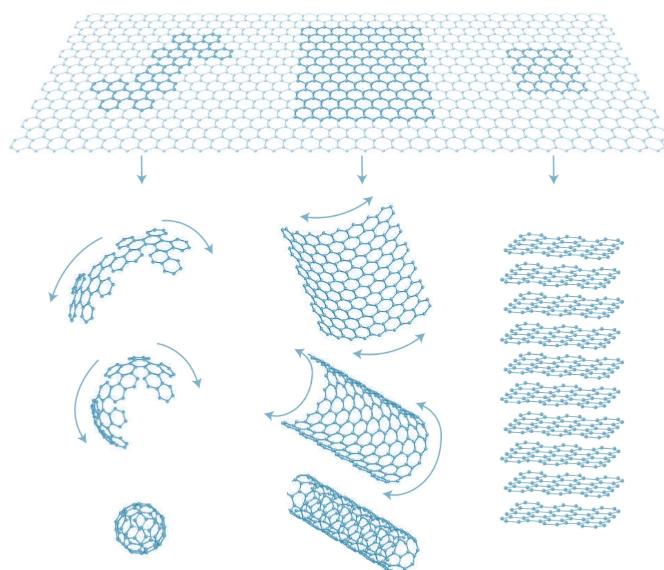

Figure 1.1: *Mother of all graphitic forms graphene is the 2D building block for carbon based materials of all other dimensionalities. It can be wrapped up into a 0D buckyballs, rolled into 1D nanotubes or stacked into 3D graphite.*
Picture adapted from [1].

made on it, however in 2013 Europe financed a research project for one billion euros which involves a lot of groups and companies for ten years, with the aim to explore and develop graphene technology, making it competitive and ready for a large scale production[1].

1.2 Electronic properties

Carbon is the fourth most abundant chemical element in the universe by mass, and can present itself under several forms showing particular characteristics as a result of the different interaction of the electron clouds. In the base form it has six protons and six electrons; two of them are strongly bonded to the nucleus occupying the $1s$ orbital thus they are irrelevant for chemical reactions, whereas the remaining four, placed in the $2s$ and $2p$ orbitals, are available for covalent bonds. The comparable energies of this latter orbitals lead to the possibility of mixing them forming new *hybrid* orbitals which result from the linear combination of the electron wave functions. Depending of how many p orbitals are involved in this process it is possible to speak about sp^1, sp^2, or sp^3 hybridization. The $2D$ nature of graphene is related to the creation of three sp^2 hybrid orbitals which laid in a plane orthogonal to that of the remaining p orbital enabling the formation of three

[1]http://graphene-flagship.eu

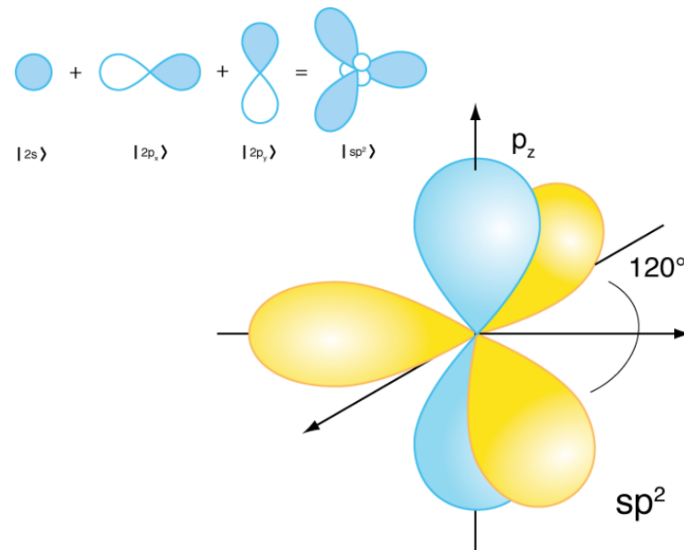

Figure 1.2: *sp^2 utilizes the $2s$ orbital and two of the $2p$ orbitals in order to form three hybrid orbitals and an unchanged p_z orbital. The new set of formed hybrid orbitals creates trigonal structures, leading to a molecular geometry of $120°$. When bonded to other carbon atoms, the remaining p_z orbital give rise to a delocalized π bond, responsible of the electrical conduction.*

σ bonds (Figure 1.2). The last p orbital, when the carbon atoms are put close in contact, forms a delocalized π bond which is the responsible of the electron mobility through the graphene sheet.

The graphene honeycomb lattice for definition is not a Bravais lattice since it is not possible to find a translation vector which can reach all the nodes with an integer combination of two base vectors, however it can be viewed as the interpenetration of two triangular sublattices (A and B in figure 1.3). Therefore the construction of a Bravais lattice can be made taking into account only one triangular lattice with a primitive cell base formed by two atoms separated by a distance $a_{C-C} = 0.142$ nm. The right part of Figure 1.3 show an illustration of the firs Brillouin zone (BZ) based on the construction of the reciprocal lattice; it represents a set of nonequivalent points in the reciprocal space, i.e. points which may not be connected to one another by a reciprocal lattice vector. In the BZ it is possible to distinguish some high symmetry points: the K and K' points are placed at the six corners of the BZ, whereas the Γ and the M points are situated respectively at the center of the BZ and in the middle of the edges [26] [27].

It is proved that charged particles in graphene are well described by the Dirac relativistic equation in which the particles approach a speed lower than that of light called Fermi velocity. The band structure o monolayer

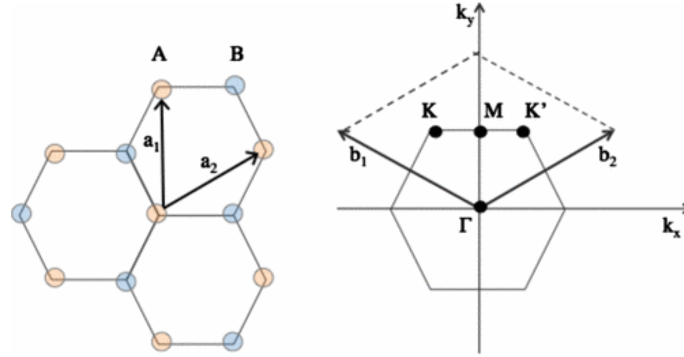

Figure 1.3: *Left: the lattice structure of graphene is composed by two interpenetrating triangular lattices A and B with lattice unit vectors* $\mathbf{a_1}$ *and* $\mathbf{a_2}$*.*
Right: hexagonal Brillouin zone representation in which $\mathbf{b_1}$ *and* $\mathbf{b_2}$ *are the reciprocal lattice vectors; in the* K *and* K' *points, also called Dirac points, the conduction and the valence bands touch each other [2].*

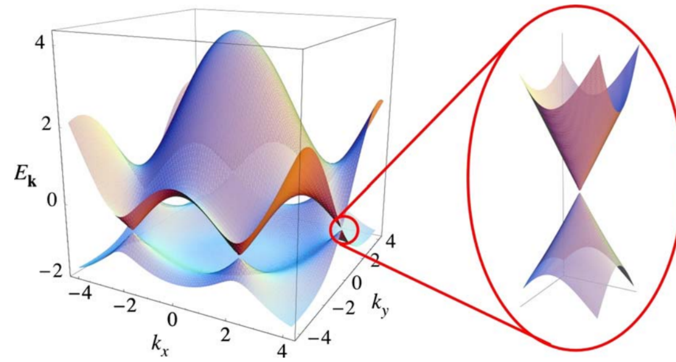

Figure 1.4: *Electron band structure in the honeycomb lattice of graphene. In the right side the conical shape is shown, therefore near* K *and* K' *the dispersion relation is relativistic with an effective mass being zero. Picture taken from [3]*

graphene is accurately extracted using a tight-binding approach considering only nearest-neighbor hooping and a single π electron per carbon atom [3] [28] [29]. As shown by the previously cited articles the resultant dispersion relation can be written as

$$E^{\pm}(k_x, k_y) = \pm\gamma_0\sqrt{1 + 4\cos\frac{\sqrt{3}k_x a}{2}\cos\frac{k_y a}{2} + 4\cos^2\frac{k_y a}{2}} \tag{1.1}$$

where $a = \sqrt{3}a_{C-C}$ is the lattice constant whereas γ_0 is the nearest-neighbor overlap integral which, accordingly with Reich et al. [29], takes a value between 2.5 and 3 eV. Figure 1.4 represent the band structure of graphene calculated using the equation 1.1. The conduction ad the valence band meet at the high symmetry K and K' points also known as the *Dirac* or charge

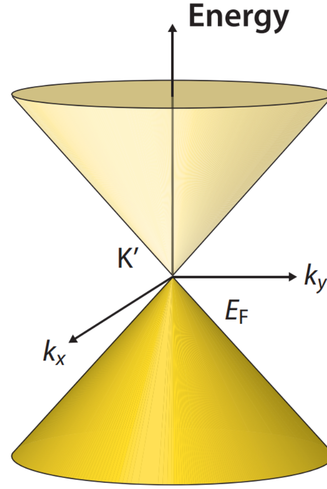

Figure 1.5: *Graphene band structure zoomed in the proximity of the Dirac point. It is clearly visible its conical shape, which is responsible of the massless Dirac fermions behavior of the electrons.*
Picture adapted from [4].

neutrality points. This two points in reciprocal space can be directly related to real space graphene sublattices: K originate from electrons on sublattice A whereas K' from electrons on sublattice B. Graphene, defined as both a semi-metal and a zero-gap semiconductor, has the Fermi level (E_F), in its pristine (undoped) state, situated precisely at the energy where the conduction and valence bands meet, living the valence band completely filled and the conduction band empty.The expansion of the equation 1.1 close to the Dirac point (K or K')[2] result in the well known linear dispersion relation between energy and momentum:

$$E^{\pm}(\kappa) = \pm\hbar v_F|\kappa| \tag{1.2}$$

where $\kappa = k - K\,(K')$ is the wave vector measured from $K\,(K')$ and v_F is the Fermi velocity for the electron in graphene defined as:

$$v_F = \sqrt{3}\gamma_0 a/2\hbar \approx 1 \times 10^6\,\mathrm{m\,s^{-1}}$$

Equation 1.2 is a good approximation as long as the momentum does not deviate so far from the $K\,(K')$ point. As shown in figure 1.5 the effect is the creation of two conic shape bands touching at the Dirac point. Furthermore graphene possesses an additional quantum number called *pseudo-spin*, which originates from the two equivalent A and B sublattices. Carriers with opposite momentum have also opposite pseudo-spin and their wave functions are orthogonal without overlap. As a consequence the $180°$ backscattering is forbidden in graphene.

[2]Due to the equivalence between the three K and K' points it is possible to restrict the consideration on the dispersion relation to just two of them.

Considering the definition of effective mass

$$m^* = \frac{\hbar^2}{\frac{\partial^2 E(k)}{\partial k^2}}$$

it easy to see that this expression for the carriers in graphene takes no sense, in fact a linear dispersion relation is characteristic of massless particle like photons. It is therefore convenient the use of the relativistic expression

$$E = \sqrt{(m_0 c^2)^2 + p^2 c^2}$$

as a way for relating mass with energy. Substituting it in the equation 1.2, with crystal momentum defined as $p = \hbar k$, a unique solution is found setting the rest mass m_0 equal to zero and considering that the Fermi velocity v_F plays the role of the speed of light in graphene.

Summarizing, close to the Dirac point, the graphene dispersion relation is well described by the relativistic Dirac equation. In this description electron and holes are considered as massless Dirac Fermions traveling with a group velocity defined by the Fermi velocity v_F. This makes graphene a bridge between condensed matter physics and quantum electrodynamics (QED) [30], providing an easy way to investigate many QED phenomena.

To conclude the review about the graphene electronic properties a consideration on the density of the states (DOS) (Figure 1.6) is noteworthy as it influence the performance of the graphene based devices. Limiting the discussion around the Dirac point the density of the states can be written as:

$$D(E) = \frac{4|E|}{\pi \hbar^2 v_F^2} = \frac{4\sqrt{\pi n}}{\pi \hbar v_F} \tag{1.3}$$

Thus it increase linearly with energy and is proportional to the square root of the carrier density (n) vanishing at the Dirac point. This DOS lead to a carrier concentration in graphene of about 10^{11} cm^{-2}/10^{13} cm^{-2} with respect to that of a metal that is around 10^{22} cm^{-3}. This difference will be important in the analysis of the metal-graphene contacts since it influences the contact resistance in graphene devices. Despite zero carrier density near the Dirac point, a *quantum conductance* at integer multiples of $2e^2/h$ is observed [31] [5], which is strictly related to the later explained *quantum hall effect* shown by graphene under the application of a magnetic field.

1.3 "Exotic" behaviours of graphene

It is proved that the carrier mobility in graphene could reach the highest value already known. From the technological point of view this is mainly the

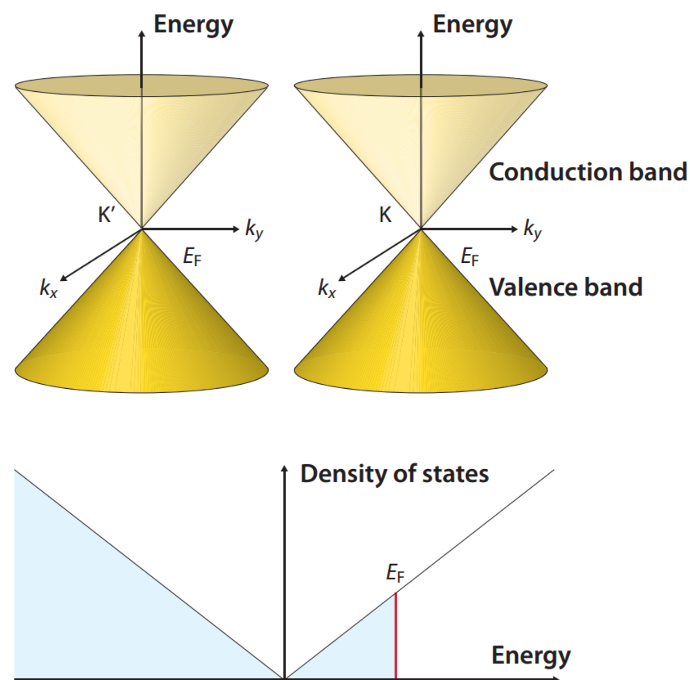

Figure 1.6: *Graphene Density of the States (DOS) calculated starting from the linear dispersion relation in the proximity of the Dirac point. At the energy where the conduction and the valence bands meet, the DOS have a vanishing point.*
Picture adapted from [4].

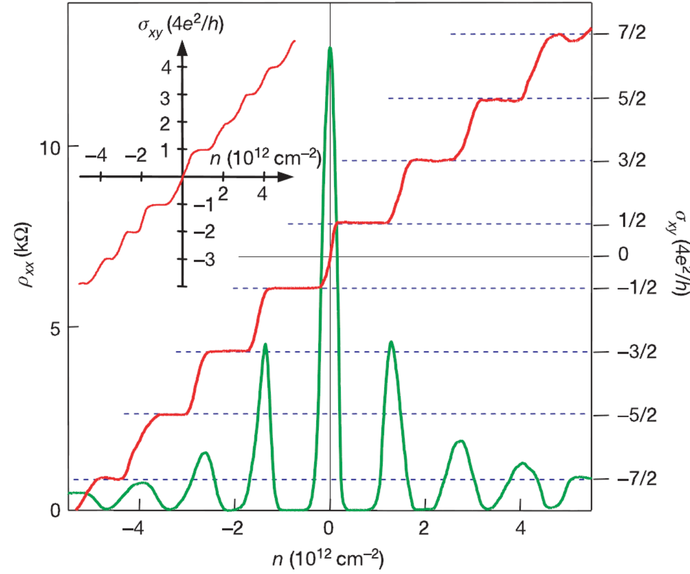

Figure 1.7: *Hall conductivity σ_{xy} and longitudinal resistivity ρ_{xx} of graphene as a function of their concentration at $B = 14$ T and $T = 4$ K. The value of $\sigma_{xy} = (4e^2/h)$ is calculated from the measured dependences of $\rho_{xy}(V_G)$ and $\rho_{xx}(V_G)$. The inset show σ_{xy} in "two-layer graphene" where the quantization sequence is normal and occurs at integer values.*
Picture taken from [5].

reason for the great interest in the design and fabrication of graphene-based devices. Although a value of $1\,000\,000$ cm^{2}V^{-1}s^{-1} is reached in graphene at liquid Helium temperature [32], at room temperature the acoustic phonon interaction limits the mobility value at $200\,000$ cm^{2}V^{-1}s^{-1} [33]. In conventional semiconductor materials such as silicon and gallium arsenide, optical phonon scattering dominates at room temperature, causing a sharp decrease of the electron mobility with increasing temperature. The very high energy of optical phonons in graphene prevents their interaction with the electrons, causing a negligible loss in mobility [34] [35]. Although in some semiconductors like InSb a mobility of $78\,000$ cm^{2}V^{-1}s^{-1} is observed [36], these values are quoted for undoped bulk semiconductors. Conversely in graphene mobility has a weak dependence on n, remaining high even at high carrier concentration. Moreover, the symmetrical behavior of the conduction and valence band around the Dirac point, indicates that electrons and holes should have equal *mobility* unlike the typical semiconductors where two different values are observed, with holes mobility begin particularly low. Since the transport properties in graphene are governed by impurity and defect scattering, ballistic transport should be easy reachable at the submicrometer scale. Room temperature ballistic transport on micrometer scale, predicted by Bolotin et al. [37] and Du et al. [38], has been confirmed in 2011 by Mayorov et al. [39].

1.3.1 Quantum Hall Effect

In the presence of a strong perpendicular magnetic field B, charges confined in two dimensions are constrained to move in close cyclotron orbits with a characteristic cyclotron frequency ω_C. Treating this orbitals quantum mechanically they result quantized leading to the formation of discrete Landau levels (LLs) in the energy spectrum. In other words electrons occupy discrete Landau energy level as a result of their quantized orbits. This is known as *Quantum Hall Effect* (QHE) and in graphene, unlike the conventional 2D systems, it reveals also at room temperature [40]. Roughly speaking the quantum hall effect is a quantization of resistance that is defines by the electron fundamental charge q and the Plank constant h. This quantum behavior shows up as a plateau in the conductance measured transverse to the current flow (σ_{xy} in Figure 1.7). As one LL fills up, the conductance is flat, showing no increase with carrier density until the next LL is nearly filled. Due to the massless Dirac like nature of carriers in graphene, the eigenenergies of the LLs are given by [41] [42]:

$$E_n = \sqrt{2eB\hbar v_F^2 |l|} \qquad l = 0, \pm 1, \pm 2, \ldots$$

instead of that of the conventional 2D systems:

$$E_n = \hbar\omega_C \left(l + \frac{1}{2} \right)$$

This implies the existence of an anomalous LL at zero energy (indicated by the peak at $n = 0$ of ρ_{xx} in Figure 1.7) [5] [43]. Furthermore in graphene the rule for quantization of σ_{xy} takes the form

$$\sigma_{xy} = g \left(l + \frac{1}{2} \right) \frac{e^2}{h}$$

where g is the total degeneracy spin and valley degeneracy. This expression, compared to that of conventional 2D systems

$$\sigma_{xy} = gl\frac{e^2}{h}$$

shows an additional $1/2$ that is an hallmark of the chiral nature of the Dirac fermions in graphene.

1.3.2 Klein tunneling

In classical mechanics, a potential barrier whose height is greater than the energy of a particle will confine that particle. In quantum mechanics, the notion of quantum tunneling describes the process whereby the wawefuncion

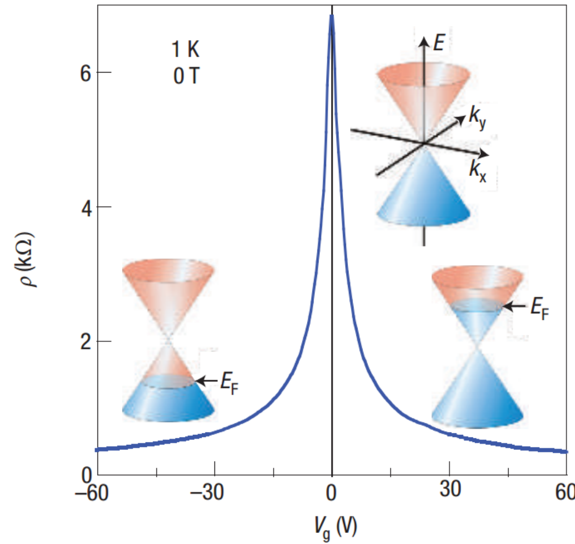

Figure 1.8: *Ambipolar electric field effect in single-layer graphene. The insets show its conical low-energy spectrum $E(k)$, indicating changes in the position of the Fermi energy E_F with changing gate voltage V_G. Picture taken from [1].*

of a non-relativistic particle can leak out into the classically forbidden region. However, the transmission through such a potential barrier decreases exponentially with both barrier height and width. In the case of Dirac relativistic particles, the situation is quite different as demonstrated years ago by the noble prize winner Oskar Klein [44]. When a Dirac electron is incident on a potential barrier it will traverse it as a hole, emerging on the other side as an electron once again. The transmission probability of such a particle increase with increasing barrier height, approaching unity for an infinite wall. This kind of effect, known as Klein tunneling, has been successfully demonstrated for the first time in graphene by Katsnelson et al. [45]. On one hand, the difficulty in confining electrons, represent a real barrier in the develop of short channel graphene-based transistors, but, on the other hand, new ways for take advantage from the Klein tunneling effect are currently being exploring.

Nowadays what makes graphene so interesting for next-future applications is the so called *ambipolar electric field effect* [19]. Despite the classical semiconductors the electrical conduction in graphene can be dominated by either positive (holes) or negative (electrons) charges depending on the sign of the applied electric field modulated by an external bias. This result in a "V-shape" of the drain current - gate voltage (Id/Vg) characteristic for a graphene field effect transistor (GFET). Figure 1.8 represent a resistivity - gate voltage curve of a GFET; at negative gate voltage the conduction is supported by holes whereas at positive gate voltage electrons conduction takes

place. As presented in Section 2.3 this kind of behavior makes graphene a perfect candidate for CMOS applications, since the construction of p-type and n-type transistors could be done on the same piece of material instead of the complex operations required for classical semiconductors.

1.4 Production methods

As already said 2D crystals like graphene were expected not to exist in a stable form. This is principally due to the thermal fluctuations (phonons) taking place at the growth temperature, which force the material into a 3D stable structure. To overcome this obstacle many tricks have been found such as growth graphene on top of a 3D crystal removing the bulk at sufficiently low temperatures to avoid undesirable thermal flacutations. Once Geim and Novoselov found the easiest way to obtain graphene [5], as known as *"scotch tape method"*, many production processes have been exploited. The compromise between reaching a large-scale production and keeping the acceptable quality for applications which graphene is intended for, are the two major criterion for the choice of the fabrication technique.

1.4.1 Micromechanical exfoliation

Scotch tape method consist in the mechanical exfoliation of *Highly Oriented Pyrolytic Graphite* (HOPG) using adhesive tape to extract thin layers of graphene and then transferring them to a silicon substrate. For this reason the technique is referred as "micromechanical exfoliation", which so far provides the best quality graphene in terms of structural integrity and carriers mobility. Even though Blake et al. [23] found an easily way to see graphene with a standard optical microscope, the difficulty in location and the small size of the obtained flakes, limit the use of graphene obtained in such a way for fundamental studies.

The need of large scale manufacturing methods leaded to three principal production techniques named *chemical exfoliation*, *epitaxial growth* and *chemical vapor deposition growth*.

1.4.2 Liquid Phase Exfoliation

Liquid phase exfoliation is obtained starting from a dispersion of graphite in a solvent using ultrasounds to separate the layers. As final step the solution has to be centrifuged in order to separate the mono layer graphene to the thicker flakes [46]. In 2014 a method of producing industrial quantities of high-quality graphene, starting from liquid phase, has been developed by Trinity College (Dublin) researchers [47]. The quality of the obtained graphene

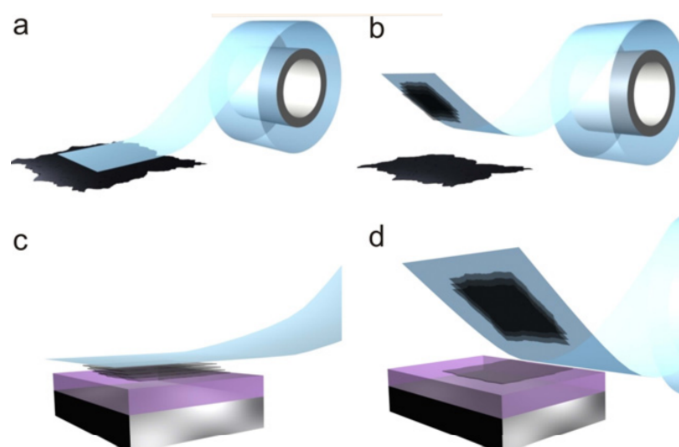

Figure 1.9: *Micromechanical exfoliation of 2D crystals. (a) Adhesive tape is pressed against a 2D crystal so that the top few layers are attached to the tape (b). (c) The tape with crystals of layered material is pressed against a surface of choice. (d) Upon peeling off, the bottom layer is left on the substrate.*
Picture taken from [6].

flakes in addition to the low complexity of production, makes such graphene a good candidate for bulk application such as composite materials [48] as well as coating [49]. However, its use in electronic applications is still not possible due to the very small size of the flakes and the low control of the process.

1.4.3 Epitaxial growth

Structurally perfect, macroscopically large graphene sheet with uniform thickness, should be the starting point for an active device fabrication. In that way the preparation of single-layer graphene by the thermal decomposition of silicon carbide (SiC) has been proposed as a viable route for the synthesis of uniform, large-size graphene layers [50]. Heating a SiC(0001) crystal above 1600 °C in an inert gas atmosphere [51] lead to Si sublimation leaving on the surface single layers and multi-layers carbon domains. As Si evaporates, even though there is a very large lattice mismatch between SiC (3.073 Å) and graphene (2.46 Å), the carbon atoms rearrange itself in a hexagonal structure. This kind of process, known as *"epitaxial growth"*, is limited at present by the lack of continuity and uniformity of the grown film, that makes its quality not as good as that of exfoliated graphene, except if graphene would be grown on a perfect single crystal. A considerable advantage of this method is that insulating SiC substrates can be directly used for device fabrication thus transfer to another substrate is not required.

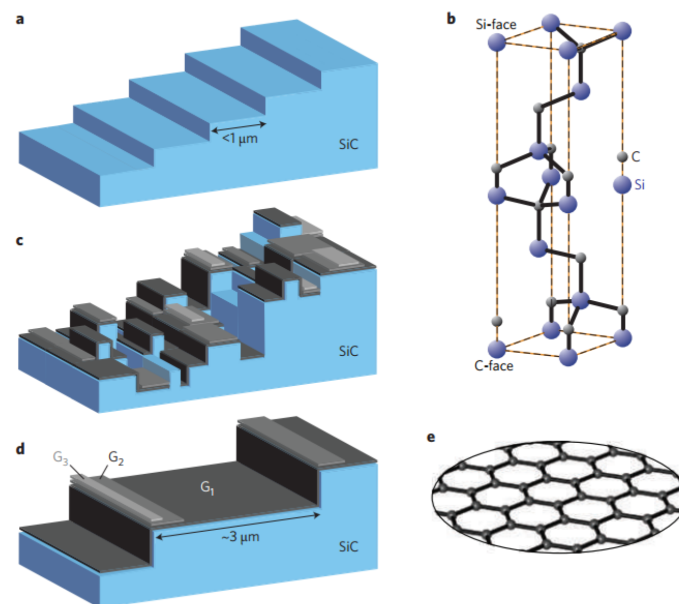

Figure 1.10: *(a) SiC starting surface with a staircase of flat terraces and atomic steps. (b) Unit cell of 6H-SiC. (c) Schematic morphology of vacuum-graphitized SiC. (d) Morphology obtained in high-pressure argon here the surface termination is predominantly monolayer graphene (G1), with narrow stripes of bilayer (G2) and trilayer (G3) graphene near the upper edge of the substrate steps.*
Picture taken from [7].

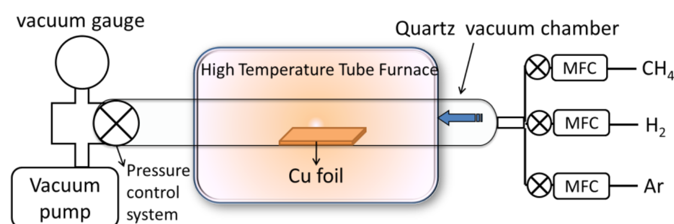

Figure 1.11: *Schematic of a common setup for chemical vapor deposition of graphene.*
Picture reproduced from [8].

1.4.4 Chemical Vapor Deposition (CVD)

Chemical vapor deposition is a well known process involving the decomposition of a precursor on a substrate, forming a thin crystalline film. It has been known for some time that graphene growth from carbon containing gases like methane, can be catalyzed by various transition metal substrates. Since the amount of carbon that can be dissolved in most metals is up to a few atomic percents, for eliminate the competition between forming a carbide and the graphene growth, the use of non-carbide forming metals, e.g. Cu, Ni, Pt, is preferred [52]. Although nickel substrates are cheap, it was found that thermal catalytic decomposition of methane on a copper foil, of a well defined thickness, result in a self limited process, showing the 95% of the substrate surface covered by single layer graphene [53]. Bae et al. [54] achieved a CVD grown poly-crystalline graphene of about 30 inch in the diagonal direction with grain size ranging from 20 μm to 500 μm. As depicted in Figure 1.12 depositing a polymer on the surface of CVD graphene and dissolving the metal layer in acidic solution, it is possible to easily transfer the grown graphene to a new substrate like the standard SiO_2. For this reason, as well as for the simplicity of the growth process, this technique arises as the most promising for electronic applications. However neither CVD growth, produce graphene with quality comparable to that obtained by micromechanical cleavage, reaching so far mobility values of about $25,000\,\mathrm{cm^2V^{-1}s^{-1}}$ at room temperature [55].

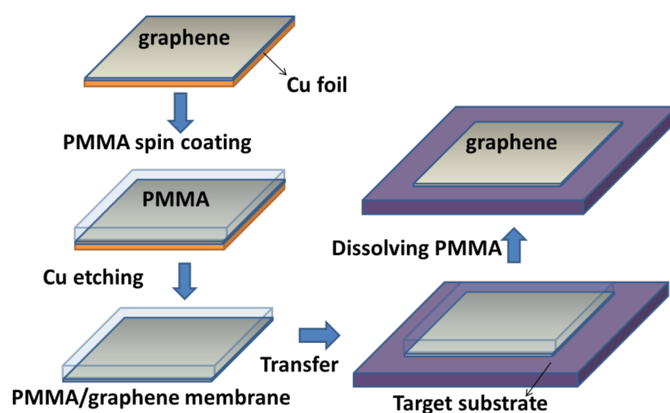

Figure 1.12: *Schematic representation of a standard transfer process of graphene grown on Cu foil onto a target substrate.*
Picture reproduced from [8].

2 High Frequency Electronics

This chapter makes a review on the high frequency electronics panorama which graphene base technologies are promising for. In section 2.1 is explained the fundamental physics of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Section 2.2 describes the principal figures of merit used to classify high frequency devices. An introduction on Graphene-based Field Effect Transistors (GFETs) and the state of the art of their performances is done in section 2.3; finally section 2.4 gives an overview on the limiting factors for high frequency operation of graphene based devices fabricated on silicon-compatible substrates.

The evolution in communications and digital applications have been led to a continuous decrease in size and elaboration time of the electronic devices. As predicted by Gordon Moore after the commercialization of the first microprocessor produced by Intel Corporation in 1971, processor speeds, or overall processing power for chip have been doubling every two years [56][1]. The transistor is the fundamental building block of modern analog or digital devices, so far principally produced using silicon as a semiconductor material. Is not a coincidence that United States semiconductor industry sales for 2013 reached a record of 305.6 billion of dollars[2]. A transistor is a three ports electrical component which can be used both as an amplifier or a switch. This makes it a perfect candidate for the treatment of analog signal, since they need amplification in order to reduce distortions and losses, as well as the elaboration of digital information which are treated as binary data. Many kind of transistors are currently placed on market but only *Field Effect Transistors* will be described in this review since nowadays they are the most diffuse type of transistors.

2.1 Metal Oxide Semiconductor FETs

A Metal Oxide Semiconductor Field Effect Transistor (MOSFET) consist in a three ports device which is able to modulate the current density flowing through two of this terminals namely, *source* and *drain*, by the application of a voltage (V_G) on the remaining *gate* port [57]. Through the years silicon has establish as the best semiconductor for such a kind of device. The structure of a classical silicon nMOSFET is shown in Figure 2.1(a); the two highly doped regions of source and drain are separated by a zone placed under the oxide layer known as channel region. Applying a gate potential

[1]This is known as "Moore's Law" since he predict this trend in 1965.

[2]Data taken by www.semiconductors.org

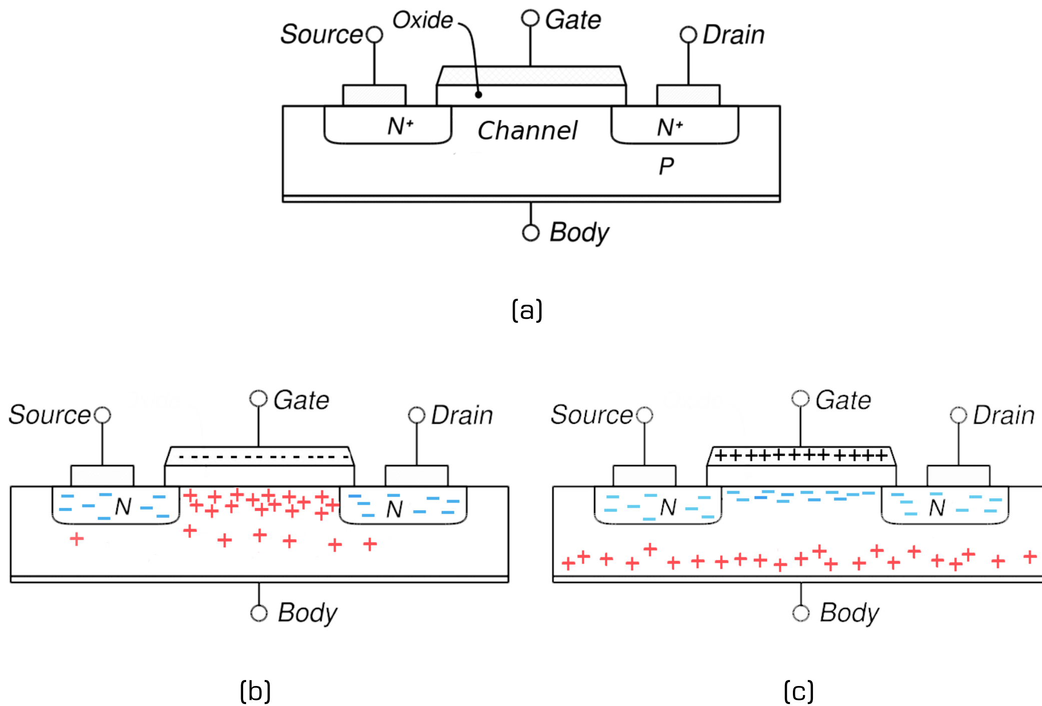

Figure 2.1: *(a): Sketch of an n-type MOSFET device, based on a p-type substrate. The gate stack is formed by an insulator sandwiched between the substrate and the gate metal electrode. Two highly n-doped regions are implanted at the edges of the channel corresponding to the source and drain electrodes. (b): In the off-state of the MOSFET a negative V_G induces in the channel an high concentration of holes; the n-p-n double junction prevents the onset of a current. (c): When $V_G > V_{th}$ in the channel, previously depleted by holes, negative carriers are attracted thus conduction is allowed.*

the Metal Oxide Semiconductor structure behave like a capacitor attracting carriers from the silicon bulk toward the channel, here electrons and holes are placed in an electric field, generated through the application of a voltage between source and drain (V_{DS}), which force them moving in a direction parallel the the channel. The key point for the control of the device is that the bulk and the source/drain regions are doped in an opposite manner: thus for a p-type doped substrate two n-type doped zones are implanted. Hence, whenever a V_G less then a well defined threshold voltage (V_{th}) is applied, the formed n-p-n double junction don't allow the current flow, thus the MOSFET is in an "off" state (Figure 2.1(b)). When V_G approaches V_{th} a depletion zone under the gate stack is created, forcing the holes to go away from this region. Once V_{th} is reached, an high concentration of electrons are attracted in the channel allowing carriers flow, therefore the MOSFET switch into its "on" state (Figure 2.1(c)). The heavily doped source/drain regions,

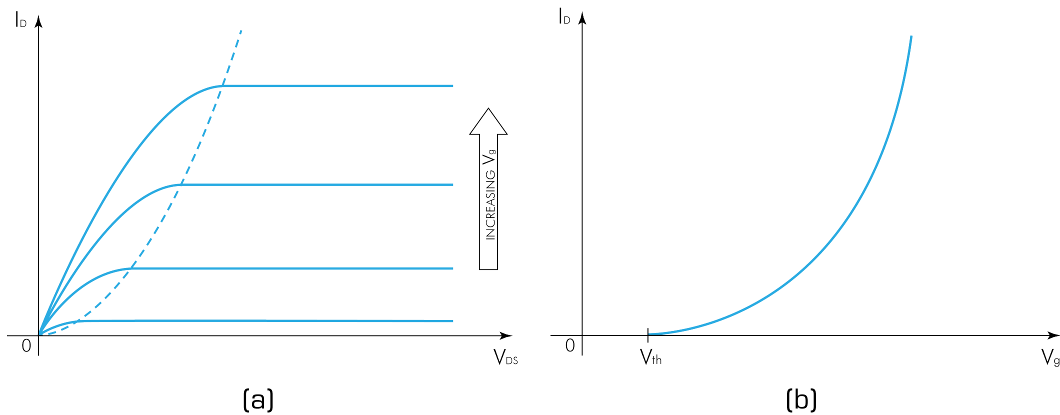

Figure 2.2: *(a): Typical I_D/V_{DS} characteristic for n-channel metal oxide semiconductor field effect transistor at constant gate voltages. Two region are distinguishable, for low V_{DS} the current growth is linear, therefore the MOSFET is said to be in the "ohmic" zone. When V_{DS} goes beyond the threshold value, the channel pinch-off takes place and the current starts saturate.*
(b): I_D/V_G transcharacteristic for a n-channel MOSFET. If $V_G < V_{th}$ no current can flow through the channel, but once V_G approaches V_{th} the drain current starts growing following a shape that depends on V_{DS}.

shown in Figure 2.1, are used to make "ohmic" contact to the conductive channel, so that a voltage difference between the source and the drain will result in current flow from the positive voltage at the drain terminal to the negative voltage at the source(I_D). In the "on" state the drain current is a function of both V_G and V_{DS}. The larger the gate voltage, the larger will be the density of electrons in the conduction channel and the larger will be the device drain current. However I_D can not grow infinitely therefore, as soon as V_{DS} reaches a specific value, it tends to saturate (Figure 2.2(a)). This is a very important feature for a transistor since, as later explained, the maximum frequency at which it can operate is strictly related to the saturation current. The ability to pilot a current in a MOSFET is a function of some physical parameters. Dimensions, like the channel length (L) as well as the oxide thickness (t_{ox}), and the carriers mobility μ, influence in a direct way I_D. In a very rough description the drain current is proportional to μ and $1/L$. Moreover the gate capacitance per unit area of the MOS structure defined as:[3]

$$C_g = \frac{\varepsilon_{ox}}{t_{ox}}$$

determines the ability of the gate to modulate the charges in the channel therefore, the grater the C_{ox} the less the V_G required to reach an high current density thus a reduced on-off switching time. Smaller MOSFETs are

[3] ε_{ox} is defined as the *dielectric constant* of the oxide. It is an intrinsic characteristic of any insulator material.

then desirable for several reasons. First of all making smaller transistors allow to pack more and more devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Moreover the frequency at which a MOSFET can operate, as explained in section 2.2, is strongly dependent on the time constant RC. When dimensions are scaled down by an equal factor, the transistor channel resistance does not change, while gate capacitance is cut by that factor. Despite the outcomes, the continuous MOSFETs dimensions reduction have been led to many relevant problems concerning parasitic effects such as *gate-current leakage*, due to the tunneling effect through the oxide layer, carriers velocity saturation, generated by the very high electric field in the channel, and many others. Trying to attenuate this effects the attempt to increase C_{ox} through the use of insulators with high dielectric constant has been done, but the integration of such materials is not easy with the currently silicon technology [58].

2.2 FETs RF performance parameters

The requirement of different characteristic for analog and digital electronics have been led to the develop of two different kind of semiconductor devices: those applied for logic circuits and those used in the radiofrequency (RF) field. Digital electronics is based on highly integrated silicon CMOS technology. The incredible resources invested on it in the last five decades, result in a big barrier for the develop of any other competitive technology. Analog electronic circuits, on the other hand, are not as highly integrated, and thus are more open to newest materials and devices. In analog high-speed applications, FETs should respond quickly to a variation in the gate voltage; this require short gates and fast carriers in the channel. In high frequency applications, transistors are operating in the "on" state and the RF signals to be amplified are superimposed onto the DC gate bias. To discuss the frequency performance of a FET its equivalent circuit, represented in Figure 2.3(a), is analyzed under the assumption imposed by the small signal model. This type of analysis allows the determination of two important metrics namely the *cut-off frequency* (f_T) and the *maximum frequency of oscillation* ($f_{\max}$). In the equivalent circuit the intrinsic *transconductance* defined as

$$g_m = \frac{\Delta I_{out}}{\Delta V_{in}} = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_{DS}=constant} \quad (2.1)$$

quantifies the strength of the gating effect on the channel, while the *output conductance*

$$g_0 = \frac{1}{r_0} = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_G=constant} \quad (2.2)$$

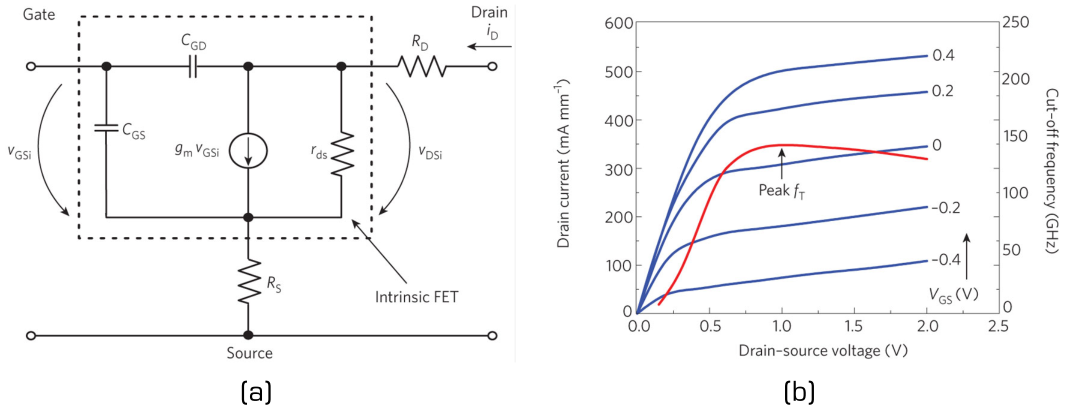

Figure 2.3: *(a): Small-signal equivalent FET circuit. Here C_{GS} and C_{GD} are respectively the gate-source and the gate-drain capacitance. The intrinsic transconductance, g_m, is related to the internal small-signal gate–source and drain–source voltages, whereas the output transconductance, g_0 , is related to the applied gate–source and drain–source voltages.*
(b): The dependence of the cut-off frequency (f_T) on the controlling parameter shows a peak in the region where both the transconductance g_m and the output resistance (r_0) are high. Pictures taken from [9]

quantifies the drain current variation under a drain-source voltage changing. R_D and R_S are parasitic components and they will become important in the discussion of the impact of the contact resistance on the FET performances. The cut-off frequency, f_T, is the frequency at which the magnitude of the small-signal current gain becomes unity, and is indicative of the highest frequency at which the transistor can operate. Considering only the intrinsic FET equivalent circuit in Figure 2.3(a) it can be ideally calculated as:

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})}$$

Introducing the parasitic effect, namely resistances and capacitance, the real dependence of f_T becomes:

$$f_T = \frac{g_m}{2\pi} \frac{1}{(C_{GS} + C_{GD})[g_0(R_S + R_D)] + C_{GD} g_m (R_S + R_D)} \tag{2.3}$$

As shown in Figure 2.3(b), f_T peaks deep in the saturation region where the transconductance reaches it maximum whereas the output conductance is at its minimum. The maximum oscillation frequency, $f_{\max}$, is the frequency at which the maximum power gain equals unity under optimum matching conditions for the input and output impedance.

$$f_{\max} \approx \sqrt{\frac{f_T}{2\pi R_G C_{GD}}} \tag{2.4}$$

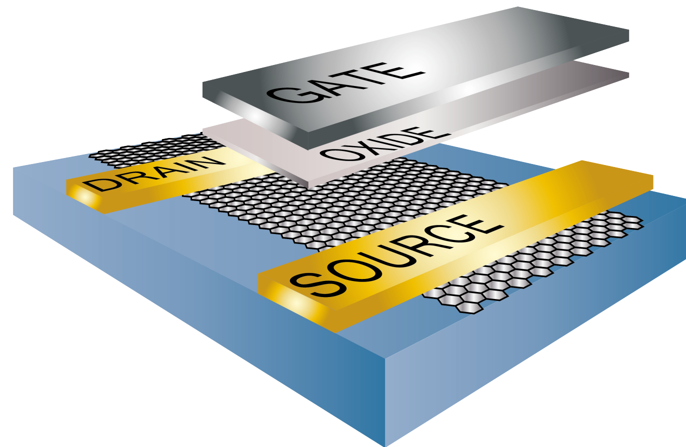

Figure 2.4: *Structure of a classical GFET. Graphene is first transferred on a substrate chosen for the application which the device is intended for. A thin layer of insulating material is deposited over the channel, then the evaporation of the metal electrodes is performed.*

where R_G is the input (gate) resistance. Since f_T and $f_{\max}$ are calculated from the ideal conditions of zero load impedance and best impedance matching networks, another parameter need to be introduced in order to better define the high frequency behavior of a device. The open-circuit voltage gain A_{vo} is directly proportional to the intrinsic gain $G_{int} = g_m/g_0$. This became an important figure of merit for that transistors which don't show a saturation current. Roughly a high frequency performances increment could be obtained through the scaling of the transistors dimensions but, the continued miniaturization of the silicon MOSFETs, have been led to adverse "short channel effects" [59] [60]. Some of these can be partially mitigated by using high mobility constituents, such as III-V semiconductors, that would also result in improved device transconductance. For this reason many new materials, including graphene, are currently being studied in order to overcome some problems reaching higher frequency of operation.

2.3 Graphene FETs

With silicon-based electronics tending towards its scaling limits, the semiconductor industry is looking for new materials which can replace the silicon FETs. Graphene with its very high mobility and Fermi velocities of electrons offers many advantages as a channel material. Since the observation of a 2D field effect in graphene made by Novoselov et al. [19], the challenge in making powerful graphene based transistors (GFETs) have been opening. Due to the lack of a band-gap in the graphene electronic structure and hence the impossibility to completely switch-off the device, the efforts move towards high frequency devices production. Because of its 2D geometry, is less

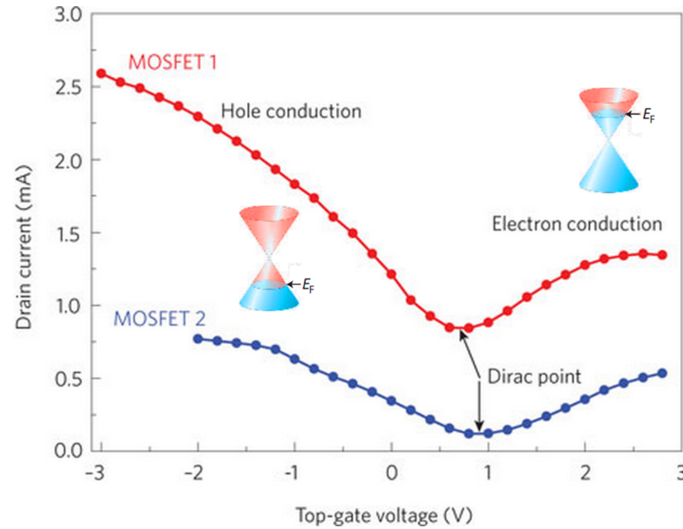

Figure 2.5: *Typical transfer characteristic for two GFETs with large area graphene channels. It is clearly visible the ambipolar conduction: when V_G is less then the Dirac point, E_F goes in the valence band and the conduction is performed by holes. Once V_G goes beyond the Dirac point, E_F falls in the conduction band and electrons transport is promoted. Picture taken from [9]*

likely to suffer from performances degradation due to scaling with respect to devices made using III-V semiconductors. The fabrication of a standard GFET, such as the one depicted in Figure 2.4, involves several generic steps including:

- Preparation of the substrate with graphene on top;
- Deposition of a dielectric material;
- Deposition of the metal electrodes (Gate, Source and Drain);

Graphene electronic properties are really sensitive to interfaces quality both of the substrate and the electrodes; therefore many tricks have been proposed for the execution of all the previous cited steps. Although the realization of back-gated transistors is allowed, this kind of configuration is good for fundamental investigation but not useful for real application. Top-gated graphene FETs, first demonstrated in 2007 [61], represent the preferred option for practical applications.

As pointed out in section 2.1 applying a voltage V_{DS} between source and drain, the potential varies along the channel, generating an electric field that is responsible of the carriers motion.4 As in classical FETs a

4The electric field ξ can be expressed as

$$\xi = -\nabla\Phi$$

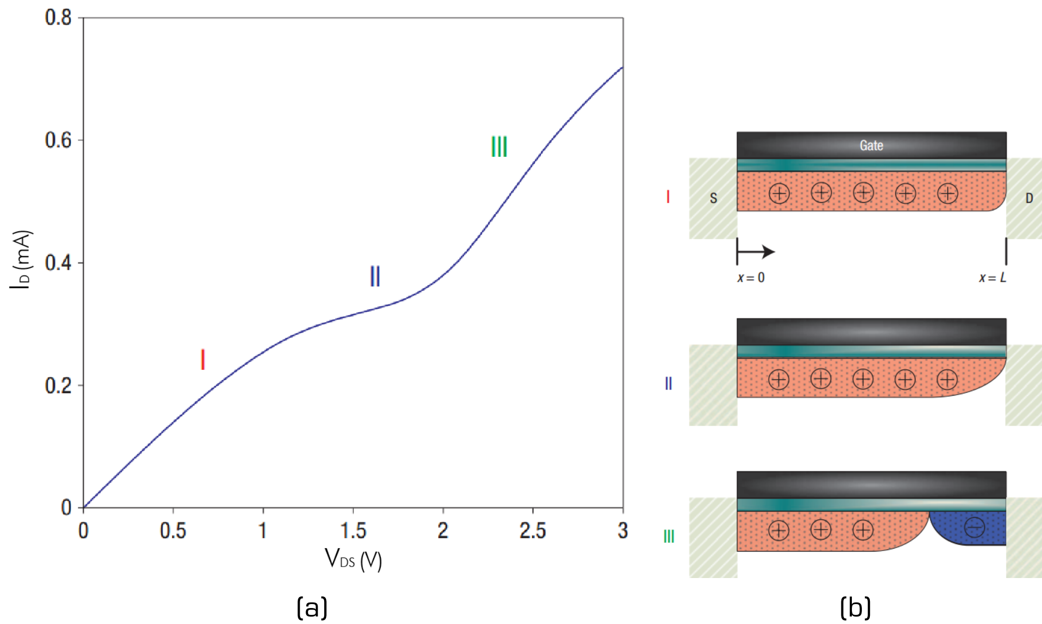

Figure 2.6: *(a): GFET characteristic with a sort of saturation like behavior placed between two regions in which current increase linearly with respect to drain voltage.*
(b): Schematic representation of the carrier concentration under the top-gated region. In point I the channel is entirely p-type and the GFET operate in the linear region. In zone II the drain side of the channel changes carrier type, promoting the recombination between electrons and holes and therefore saturating the current. In zone III the Dirac point, moving toward the source side, promotes the conduction of electron and the current starts growing again. Pictures taken from [10]

variation in the gate voltage V_G, lead to a modulation of the Fermi level (E_F) through the channel under the gate stack. By contrast, unlike the other semiconductors, graphene present an ambipolar field effect, therefore the type of carriers responsible for the conduction depends on the gate voltage. Under the ideally condition of undoped graphene at $V_G = 0$, the Fermi level is pinned at the Dirac point, hence there are a few of either carrier type and the conductivity of graphene is minimized. For positive V_G, E_F falls in the conduction band generating a large quantity of electrons that are accelerated by the electric field (Figure 2.5). When a negative V_G is applied, E_F shifts to the valence band allowing the conduction of holes. Despite conduction and valence bands are symmetric in graphene, an asymmetry in the transfer characteristic is clearly visible. As will be explain later this effect is attributed to the formation of p-n junctions between the channel and the source/drain regions due to the metal contacts.

where Φ is the electric potential that is define as a scalar field.

For high frequency operation a very high r_0 is required. It is not simple to obtain this kind of behavior in graphene FETs because, unlike silicon transistors, they don't reach a pinch-off point and therefore current should be limited only by the velocity saturation of the carriers, obtained only for very high voltages. Despite this some graphene FETs, as depicted in Figure 2.6(a), present an unusual saturation like behavior interposed between two linear regions [10] [62]. For small values of $|V_{DS}|$ the channel is entirely p-type and the transistor operate in the first linear region. Increasing $|V_{DS}|$ around a critical point the potential condition at the drain side correspond to the Dirac point promoting the recombination of the carriers and leading to a sort of saturation behavior (zone II).5 Further increasing the potential the Dirac point shift toward the source, switching the conduction type in the channel from p to n (region III). Although reaching a saturation current in graphene transistors is difficult, the very high mobility lead to an high transconductance g_m. As seen before this is a very important figure of merit for high frequency devices. Due to the V-shape of the transfer curve (Figure 2.5), g_m peaks near the Dirac point where the slope of the curve is bigger then elsewhere.

The first experimental demonstration of RF GFET was a 500 nm channel length top-gated FET fabricated using exfoliated graphene and showing a cut-off frequency of about 14.7 GHz [63]. Progress have been achieved in a short period leading actually to GFET with f_T comparable with the best other RF technologies. Remarkable is the work done by IBM researchers that pushes device performance forward from a cut-off frequency of 26 GHz in 2009 [64], 100 GHz in 2010 [65], 155 GHz in 2011 [66] and finally reaching 300 GHz in 2012 [67]. The actual record of 427 GHz have been reported by Cheng et al. [68] in 2012. So far, despite this very promising results regarding the cut-off frequency, graphene RF transistors have been suffered of a low maximum oscillation frequency that limited the performances of high frequency GFETs-based devices. Recently a 100 nm gate length transistor with an extraordinary high value of $f_{\max}$ (105 GHz) have been published by Feng et al. [69].

As reported by Sordan and Ferrari [70], beside single graphene transistors, different kinds of integrated circuits have already been realized using GFET. From the less complex 6 mixers [71], passing through more complicated voltage amplifiers [72] going to ring oscillators [11] with 12 GFETs inside. Recently IBM researchers demonstrate the powerful of graphene, fabricating a radio frequency receiver performing signal amplification, filter-

5Remember that since graphene is a gapeless material recombination can occurs without the emission of any photons, i.e. no energy is involved in this operation.

6For an integrated circuit the complexity is defined, as a first order approximation, by the number of transistors from which it is composed.

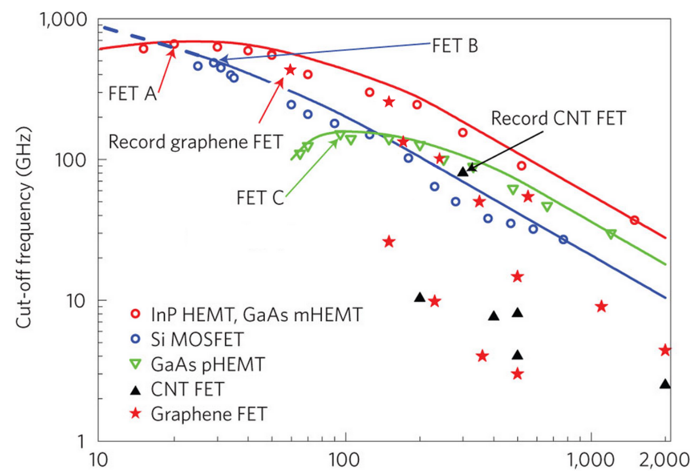

Figure 2.7: *Cut-off frequency versus gate length for graphene FETs, nanotube FETs and three types of radiofrequency FET; the symbols are experimental data points and the lines are a guide to the eye for type A (InP HEMT and GaAs mHEMT), B (Si MOSFET) and C (GaAs pHEMT) devices. The FET A with the highest cut-off frequency of* 660 GHz *is a GaAs metamorphic HEMT (mHEMT) with a* 20 nm *gate. The FET B with the highest cut-off frequency of* 485 GHz *is a Si MOSFET with a* 29 nm *gate. The FET C with the highest cut-off frequency of* 152 GHz *is a GaAs pseudomorphic HEMT (pHEMT) with a* 100 nm *gate. The fastest nanotube device (CNT FET) has* $f_T = 80$ GHz *and* $L = 300$ nm, *and the fastest reported graphene MOSFET has* $f_T = 426$ GHz *and* $L = 64$ nm. *Picture taken from [9]*

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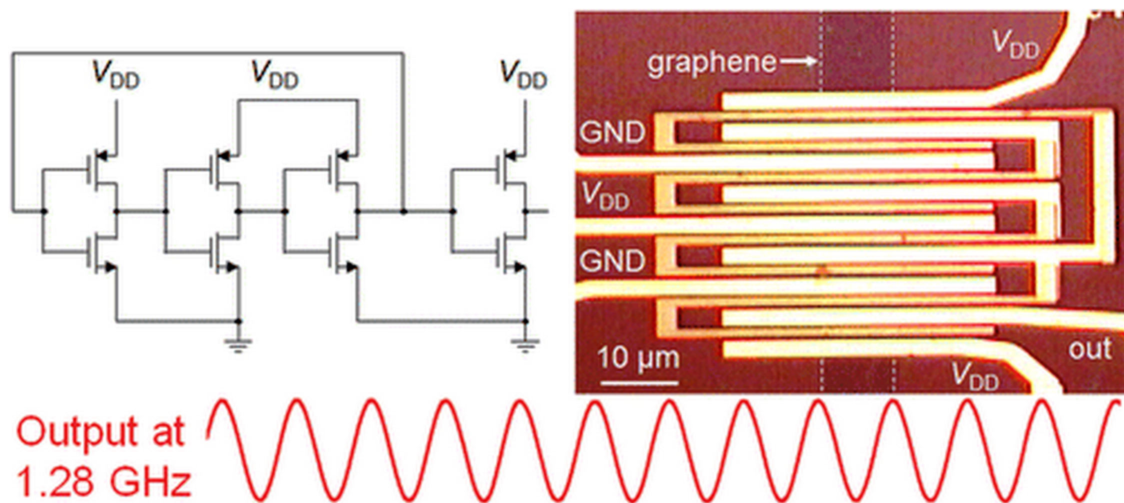
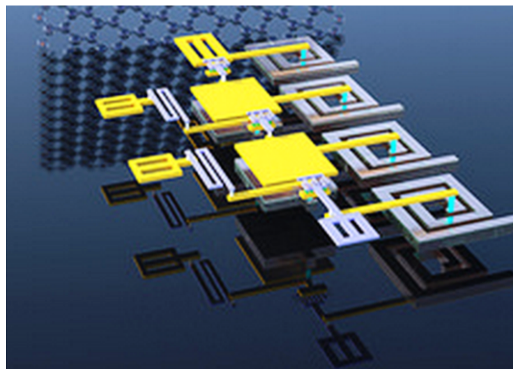


(a)



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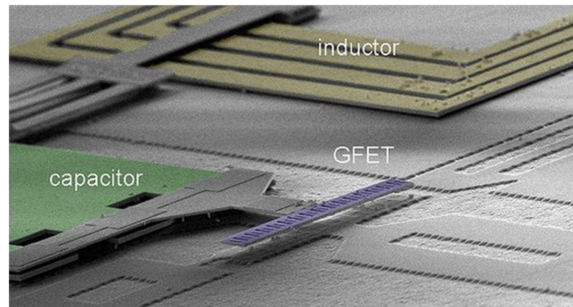


(c)

Figure 2.8: *(a): Ring oscillator produced by Guerriero et al. [11] at the L-NESS laboratories. It is composed by 8 integrated graphene transistors and the maximum frequency of operation goes beyond the GHz barrier.*
(b) and (c): Images taken from [12] representing the new graphene based integrated circuit (by IBM) working with on a wireless network band of 4.3 GHz*; the device was able to receive and restoring a text message without distortions.*

ing and downconversion mixing [12]. They were able to receiving and restoring digital text transmitted on a 4.3 GHz carrier signal.

2.4 Graphene high frequency limiting factors

There exist some factors that crucial influence the high frequency performance of any FET based device. Commonly they are defined as "parasitic elements", namely capacitance and resistances, resulting from both the physical properties of the materials composing the transistor ("intrinsic" elements), and the interaction between different materials ("extrinsic" elements). As already said the two major figure of merits for evaluate the RF performances of a transistor are the cut off frequency and the maximum oscillation frequency. Many intrinsic and extrinsic elements impact on this two parameters. Since the high interest in integrate graphene base devices in silicon technology, here a discussion on factors that influence high frequency operation for GFETs on silicon-compatible substrates is performed. Particularly this points will be outlined:

- Graphene-substrate interface effects limiting carrier mobility;
- Gate stack planning and fabrication;
- Metal contacts deposition;

2.4.1 Mobility

For radio frequency operations an high value of transconductance is desirable. g_m strongly depends of two factors: one, described by the C_g parameter, is the capability of the gate to modulate the charges in the channel, whereas the other one, namely the mobility μ, specifies the ability of carriers to freely move in graphene. Graphene is famous for reaching the highest mobility values already known, in the order of $1\,000\,000$ cm^{2}V^{-1}s^{-1} on "suspended" samples, however when used in real application it result in mobility two orders of magnitude lower. This difference could be explained in principal with two reasons: one is related to the production and transfer of graphene, whereas the other one comes from the physical interaction between the substrate and the graphene itself.

The electrical transport in graphene is really sensitive to charged impurity scattering [73]; moisture and other species drastically impact on its mobility [74] [75]. Although graphene grown by chemical vapor deposition (CVD) provides a promising pathway for the fabrication of GFETs on a large scale, during the transfer procedure many problems appear, influencing its final quality. A common method for graphene transfer uses a polymer layer of

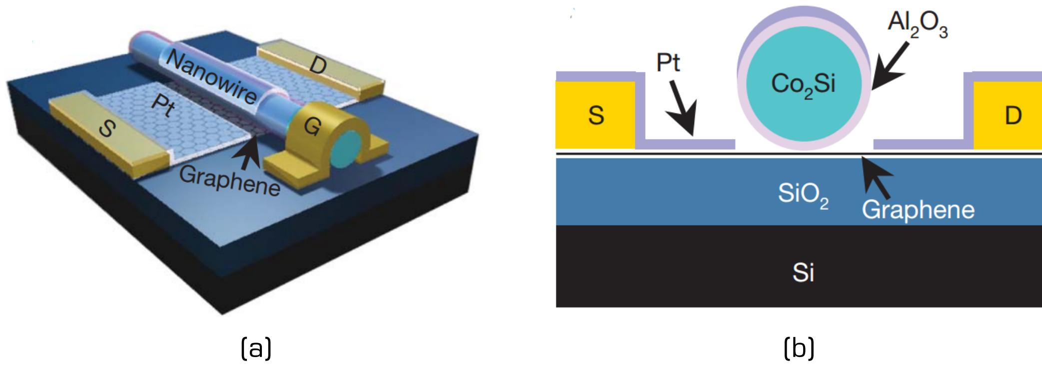
poly(methylmethacrylate) (PMMA) to support the graphene, while the metal substrate is etched away. Furthermore the transfer process is made in a "wet" environment, therefore some water molecules could be trapped under graphene at the interface with the substrate. Removal of both PMMA residues and moisture is quite problematic even annealing the samples in vacuum or inert gas environment. The presence of this "slags", which act as centers of scattering, drastically reduces the carriers mobility [76]. Another effect that dramatically impact on μ is the extrinsic scattering by surface phonons at the graphene-substrate interface [33]. This intrinsically depends on the choice of the substrate [77], limiting the mobility of graphene on conventional, and silicon compatible, SiO_2 around $40\,000\,\mathrm{cm^2V^{-1}s^{-1}}$.

2.4.2 Gate Stack

The capability of the gate to modulate the carrier concentration along the channel, and thus its ability to faster switch the transistor from one state to another, is proportional to C_g namely the gate capacitance per unit area defined as:

$$C_g = \frac{\varepsilon_{ox}}{t_{ox}}$$

where ε_{ox} and t_{ox} are respectively the dielectric constant and the thickness of the oxide. The choice of the dielectric layer is therefore a crucial aspect in the fabrication of high frequency GFETs because small insulator thicknesses require wider energy gap dielectric materials in order to avoid leakage current through the gate. In standard silicon MOSFETs the limits in scaling the SiO_2 insulator thickness have been reached time ago. A solution for the problem have been given from the so called "high-k" dielectric materials, which exhibit grater ε_{ox} which allows to maintain high values of C_g while using grater t_{ox}. The use of this kind of insulators for GFETs gate stacks seems to be the most powerful way to push their high frequency performances. However the deposition of a uniform dielectric layer is difficult and in many cases imply the creation of defects in the graphene below, negatively impacting on the carriers mobility. An easy way to obtain a good oxide layer, concerning the capability of aluminum to spontaneously form a very thin ($\approx 4\,\mathrm{nm}$) layer of AlO_x at the graphene interface, have been found a few years ago [78] [79]. However, further increase in C_g requires the introduction of other insulating materials with higher dielectric constant as well as new structures for the gate stacks. T-shaped gates have been recently proposed [80]. This architecture possesses several advantages over conventional top gate structures, including low gate resistance and low parasitic capacitance. Thus, in accordance with equation 2.4, it allows higher $f_{\max}$. Another aspect to take into consideration during the fabrication process is the formation of not-gateable parts of the channel which originate from the difficulty of aligning the metal electrodes with the gate stack. These regions,between electrodes



(a) (b)

Figure 2.9: *Self-aligned structure with a Co_2Si/Al_2O_3 core–shell nanowire used as the gate, the source and drain electrodes are defined through a self-alignment process whereas the channel length is characterized by the nanowire diameter. The physical assembly of the nanowire gate preserves the high carrier mobility in graphene. Images taken from [13]*

and gate, cause the formation of parasitic effects defined as *access resistances* which impact on both f_T and $f_{\max}$ especially scaling the dimensions of the GFET. Some different strategies are currently under study including the so called self-aligned gate technology (Figures 2.9(a) and 2.9(b)) [13].

2.4.3 Contact Resistance

When two pieces of material are putted in intimate contact, the chemical potential of the system, represented by the Fermi level, tends to equilibrate, modifying the band structure in the proximity of the junction. Typically a charge transfer from one component to the other takes place, leading in some cases to additional series resistances, which are detrimental for the high frequency performances of a device. As shown in Figure 2.10 usually metal-semiconductor junctions form a Schottky barrier while metal-metal contacts, due to their very low screening length, 7 have no potential barrier and the vacuum level changes abruptly at the interface. Many metals used as contacts in graphene devices have a work function, defined as the difference in energy between the vacuum level and the Fermi energy, grater than that of graphene itself; therefore, as shown in Figure 2.10, when they are putted into contact the electrons tends to flow from the graphene to the metal in order to equilibrate the Fermi level. Due to the narrow density of the states (DOS) in the proximity of the Dirac point, the screening length is quite large and a very small amount of electron transfer shift E_F significantly. As a result a long charge transfer region takes place at the graphene-metal

7The screening length $\lambda \propto (DOS(E_F))^{-1/2}$, therefore for metals, which have a large density of the states near the Fermi level, the screening length is very low, conversely for graphene, due to its narrow DOS, λ is much higher.

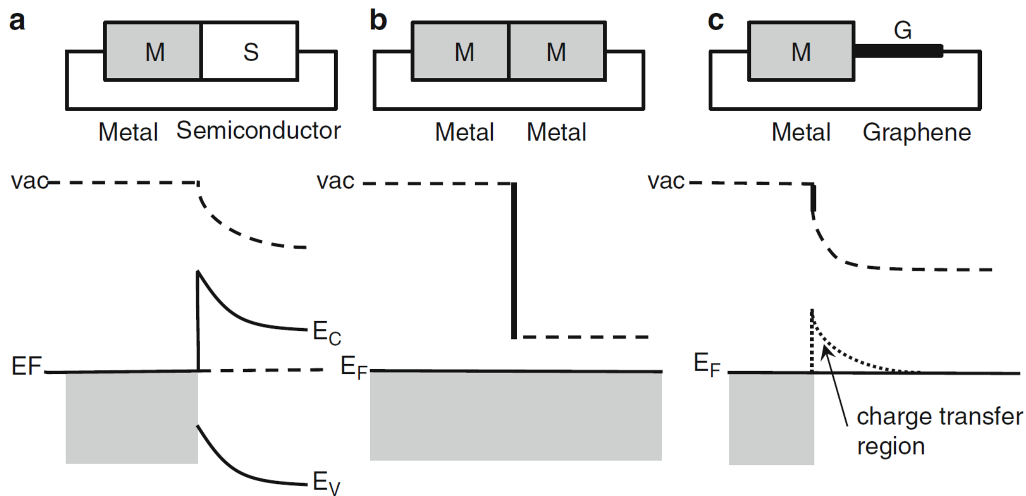


Figure 2.10: *Different type of junctions. (a): A metal-semiconductor junction is characterized by the onset of a energy barrier at the interface, i.e. Schottky Barrier. (b): Due to the very high DOS, which lead to a low screening length, In a metal-metal junction the initial difference in the Fermi level does not involve any energy step. (c) Graphene-metal junction show an increased screening length caused by the low DOS in the proximity of the Dirac point; therefore a charge transfer region forms at the interface. Picture adapted from [14]*

interface that causes the formation of a "p-doped" zone near the electrode. The application of a positive gate potential, forms a p-n junction which is the responsible of an increasing in the contact resistance. Therefore, as depicted in Figure 2.11(b), it lead to an asymmetry in the transfer curve because under positive V_G the formation of a p-n-p junction increase the resistance, whereas with negative V_G a p-p-p junction takes place and the additional series resistance is negligible. Nagashio and Toriumi [14] reveal another important aspect regarding metal-graphene interaction. Using a standard four probes method8 they found that the resistance depends only on the width (W) of the contact instead of the entire area [81]. This indicates that the "current crowding" takes place, therefore the charges flow mainly through the edges of the metal-graphene contacts. This effect occurs in the limit that the contact length is grater than the *transfer length* (d_T), which is defined by the section of the electrodes that contribute to the injection of carriers in graphene. Otherwise a transition from edge-conduction to area-conduction will occur. Even though the dependence of the contact resistance on the metal work function seems to be proved, the physical interaction between the graphene and the metal itself plays a role that have not been fully understood yet. Song et al. [82] proved that the graphene "bare"

8The methods commonly used in determination of the contact resistance, such as the Transfer Length Method and the four probes measurement, will be explain in detail in section **???**.

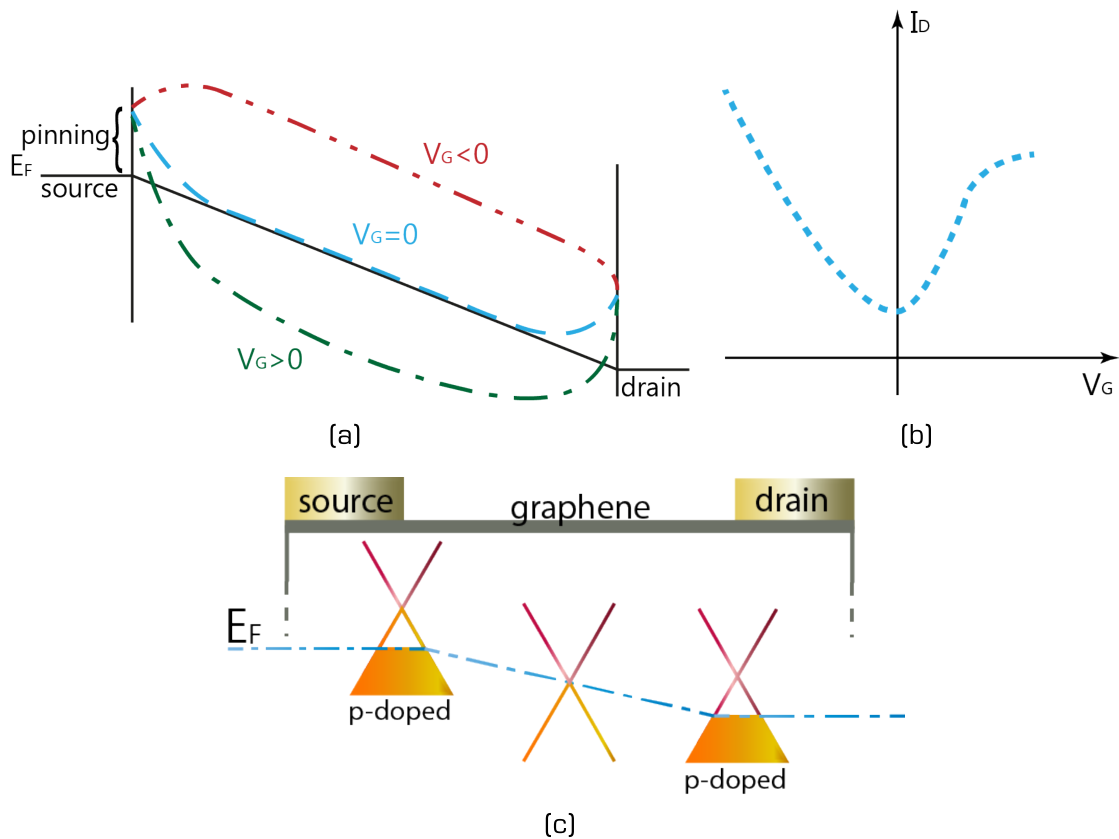


Figure 2.11: *(a): Schematic of the band diagram through the GFET section. The different tracks represent the "position" of the Dirac point for different applied voltages. Picture adapted from [14]*
(c): Transfer curve which shows the asymmetric behavior of the carrier flow due to the p-n junctions.
(b): Representation of the graphene "doping" state in the FET. Once $V_G > 0$ the Fermi level shift upwards leading to the formation of a p-n-p junction.

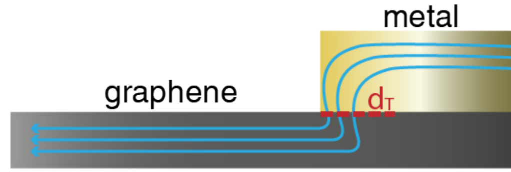


Figure 2.12: *Current crowding effect representation. The charges are not injected by the entire area beneath the electrode, conversely they tends to flow from the zone near the edges.*

Metal/Graphene	Contact Resistance	Reference
Ti Pd Au	$500\,\Omega$ µm	[85]
Ni	$500\,\Omega$ µm	[81]
Pd Au	$600\,\Omega$ µm	[86]
Pd	$900\,\Omega$ µm	[87]
Ti	$800\,\Omega$ µm	[88]

Table 2.1: *Contact resistance values reported for different metals taken at the Dirac point voltage.*

work function is not preserved when it is putted in contact with a metal. Furthermore it is also verified that contact resistance in GFET depends on the back-gate voltage (V_{BG}) showing a peak close to the Dirac point and decreasing elsewhere [83].

A commonly used method to determine the resistance present at an interface between two different materials is based on measuring the two-probe R/V curves in devices where different contact separation is performed. This known as Transfer Length Method (TLM) have been used to evaluate the contact resistance in this work and will be discussed later on.

So far many effort have been made to reduce this kind of parasitic effects in graphene devices, since they drastically kill the high frequency performances. However, till now, the values of contact resistance obtained for GFETs are not comparable with respect to other technologies like the $50\,\Omega$ µm of InAs/AlSb High Electron Mobility Transistors (HEMTs) [84]. Table 2.1 present the state of the art of contact resistances for different metals measured at the Dirac point voltage.

3 Contact Resistance Test Devices Fabrication

In this chapter an overview on the steps and facilities involving the fabrication of the tested sample is given. First of all in section 3.1 is performed a detailed description of the SiO_2/Si substrate preparation with graphene on top. Section 3.2 presents a panoramic view over all the fabrication techniques involved in the production of a contact resistance test structure. Lastly, a step by step procedure explanation for the fabrication of a standard TLM structure, is given in section 3.3.

In order to investigate the resistance which establish when a metal and graphene are brought into contact, i.e. the contact resistance, several type of structures have been fabricated. All of them have been designed in order to perform Transfer Length Measurement (TLM). Generally speaking they consist in a set of metal electrodes deposited on graphene at different distances one another. Here the entire set of steps from the substrate preparation to the metal contacts evaporation are explained.

3.1 Sample Preparation

Before starting the process of design and implementation of devices with graphene as "active" layer, the substrate supporting these components has to be prepared. This include the choice of the appropriate material, the evaluation of whether or not a back gate predisposition is needed as well as of the graphene type to be transferred on top. Lastly the evaluation of the final quality of the graphene is needed since high frequency devices required a defect-free GFET channel.

3.1.1 Substrate

In this work a highly doped silicon substrate with 300 nm of thermally grown oxide have been used as support for the graphene structures. Starting from a degenerate 4 inch As-doped (n^+ type) silicon wafer, a 300 nm tick layer of SiO_2 is grown on both the surfaces through thermal oxidation. This technique forces an oxidizing agent to diffuse into the wafer at temperature usually beyond 1000 °C where it react with silicon forming an highly ordered and dense layer of $SiO2$. A protective coating is then deposited on one surface ensuring the oxide protection in the next etching step. With the aim to both reach a good metal adhesion and provide the best charge modulation ability, the silicon dioxide is etched from the not-protected face. This is done

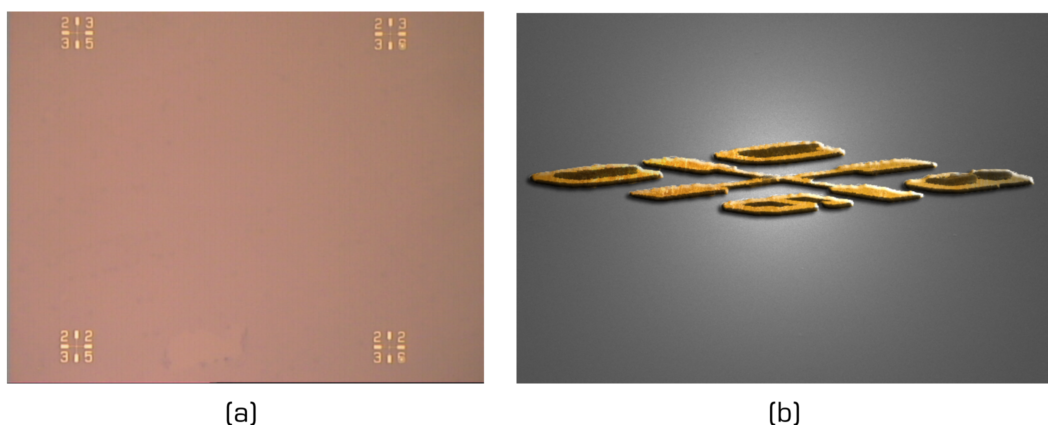
with a hydrogen fluoride acid solution. The etching procedure temporarily inhibits the formation of the natural oxide on the surface when it is exposed to the atmosphere. A metal deposition step, which will serves as a backgate, is then performed through electron beam evaporation. In order to reach a good grip between the oxide-free silicon surface and the silver (Ag) backgate, two thin adhesion layers of chromium (Cr) and antimony (Sb) are deposited before. Exactly the metal evaporation consist in 3 nm of Cr followed by 5.5 nm of Sb and then by 200 nm of Ag. The protective coating is then removed by a bath in highly pure acetone followed by a rinse in isopropanol.

In order to facilitate the positioning for the subsequent devices fabrication steps, a metal grid is "printed" on the top face of the wafer. An electron sensitive film (resist) of Poly(methyl methacrylate) (PMMA) is first coated on the surface and then exposed through the use of an electron beam which draw the required shape on the resist. This technique, also called Electron Beam Lithography (EBL), will be explained in detail in section 3.2.1. Once the process is completed, a bath in a develop solution is performed in order to remove the exposed PMMA. In this way a "mask" is created and the subsequent deposited metal will cover only the resist-free parts. 20 nm of titanium (Ti) followed by 100 nm of gold (Au) are evaporated and an acetone bath is then performed to completely remove the resist and the excess metal. The markers are cross-shaped separated by a distance of 80 µm both in horizontal and vertical direction (Figure 3.1). The so obtained grid constitute a coordinate system which allows a precisely positioning of the structures during the next fabrication steps making more easily the focusing procedure during EBL.

Before transferring graphene a final step needs to be realized. First a protective layer is coated on the upper surface in order to avoid undesirable scratches. Later the wafer is diced in a series of 3.8 mm $\times$ 3.8 mm smaller chips through the use of a dedicated laser cutter. The so obtained samples are finally washed to get rid of the protective coating making them ready for the subsequent graphene transfer.

3.1.2 Graphene Transfer

In order to promote large scale production all the samples studied here for contact resistance tests are based on CVD grown graphene (Section 1.4). As explained before this technique involves the usage of a transition metal thin film (copper Cu in this case) substrate. This is used for catalytic purposes and is typically unwanted after the synthesis is complete, thus the removal of the metal is the logical step after the growth. A thick carrier layer of PMMA is firstly spin coated onto one of the copper-graphene surfaces. The accessible graphene-copper face is then etched by the immersion in a



(a) (b)

Figure 3.1: *(a): Area of* $80\,\mu m \times 80\,\mu m$ *delimited by four* Ti/Au *markers. The standard chip used in this work comprise a matrix of* 40×40 *of them. (b): SEM image of a single marker (false color).*

solution of Ferric Chloride ($FeCl_3$) leaving a free-standing PMMA/graphene membrane. Due to its flexibility it can be comfortably handled, making the deposition on the target substrate quite simple. Once the membrane approaches the SiO_2 surface, dry the interface becomes of great importance since water molecules trapped under graphene will not be able to escape later, therefore decreasing the final performances of the fabricated devices. After that PMMA removal is performed both leaving the sample in an acetone bath and then annealing it beyond $200\,°C$ to ensure the elimination of almost all the polymer residues [89] [90].

3.1.3 Quality assessment

There is a wide range of techniques which are useful to understand and characterize graphene properties and quality, but particularly one stands out. Raman spectroscopy is a technique, based on inelastic scattering of a monochromatic light emitted by a laser source. The incident photons are absorbed and then re-emitted, yielding a characteristic excitation energy to the sample. This inelastic scattering process lead to a change in the frequency of the outcoming light spectrum compered to that of the incident wave, known as "Raman shift". These characteristic shifts provide valuable information about vibrational, rotational and other low frequency changes in the samples [91]. As for all carbon based systems the graphene Raman spectra contain only a few significant peaks in the spectral region $1000 \div 3000\,cm^{-1}$ [92]. Graphite and graphene spectra looks very similar, however careful observation reveals small characteristic shifts in the Raman lines, going from single-layer graphene to multiple layers (Figure 3.3) Ferrari et al. [15]. In single layer graphene some characteristic peaks are clearly visible at $1580\,cm^{-1}$ (the "G" mode) and around $2700\,cm^{-1}$ (the "2D" mode). The

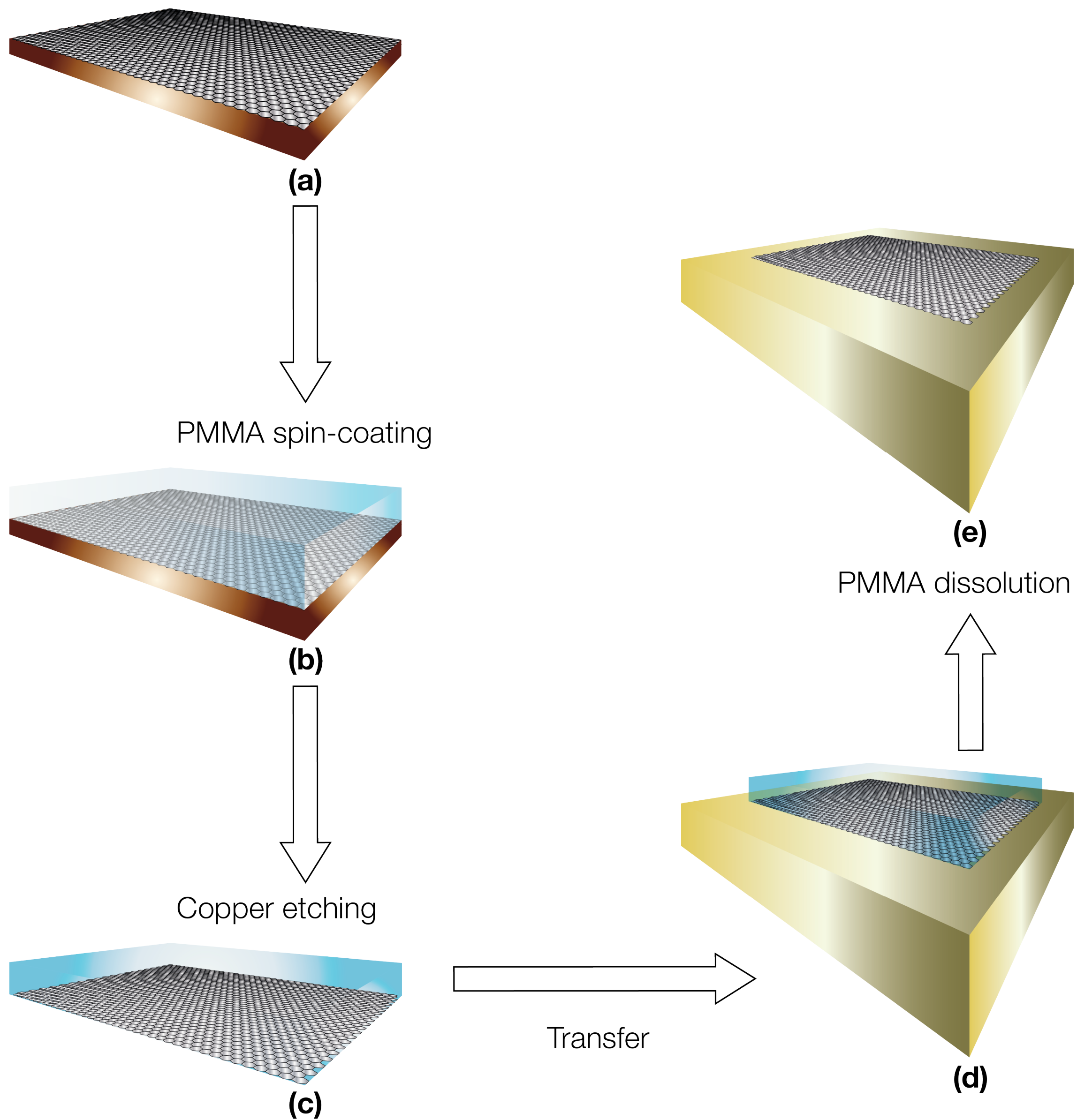


Figure 3.2: *Scheme of a standard transfer procedure for graphene grown by CVD on a copper substrate (a). A film of PMMA is coated on the surface (b) then the copper foil is etched (c) leaving the graphene stuck to the polymer. Once the stack is then transferred to the target substrate (d), the polymer is dissolved leaving the graphene surface free (e).*

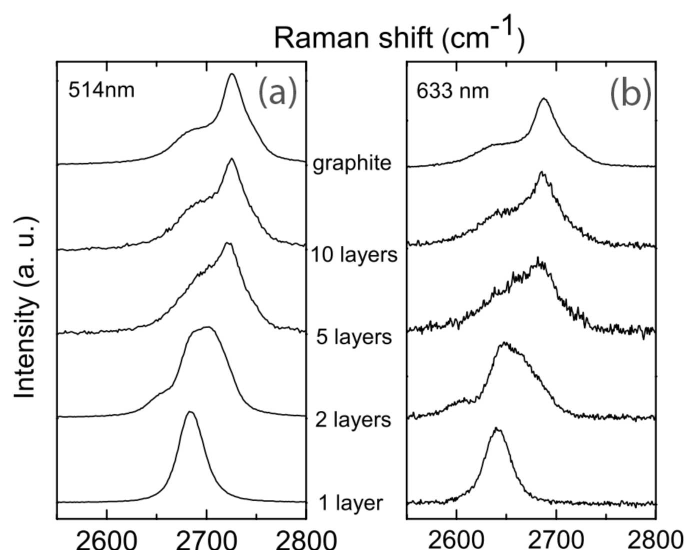


Figure 3.3: *Evolution of the Raman spectra under a* 514 nm *(a) and* 633 nm *(b) laser source with the number of layers. Picture taken from Ferrari et al. [15]*

latter arises from phonons near the K point in the Brillouin zone where conduction and valence bands touches. The presence of "dopants", such as PMMA residues, in graphene induces a shifting in this characteristic peaks [93] providing an easy and non-destructive way to determine whether or not the transferred graphene is of a good quality.

3.2 Fabrication Techniques

Once the substrate is produced, the real fabrication of the planned device takes place. It consist in several steps each of which involves the usage of a dedicated facility.

3.2.1 Electron Beam Lithography (EBL)

With its ability to form arbitrary two-dimensional patterns down to the nanometer scale, electron beam lithography (EBL) is one of the most important techniques in microfabrication. Briefly the substrate is coated with a thin layer of polymer resist, which undergoes to a chemical change when it is placed under the electron beam. Hence the exposed areas can be easily dissolved in a specific organic solvent. Since the final pattern is obtained by an electron beam draw, the time involved in the lithography operation is quite large. However this technique allows to an easily modification of the pattern making this flexibility its strength. Despite the high resolution (less then a nanometers) obtainable with a dedicated EBL system, many research groups use

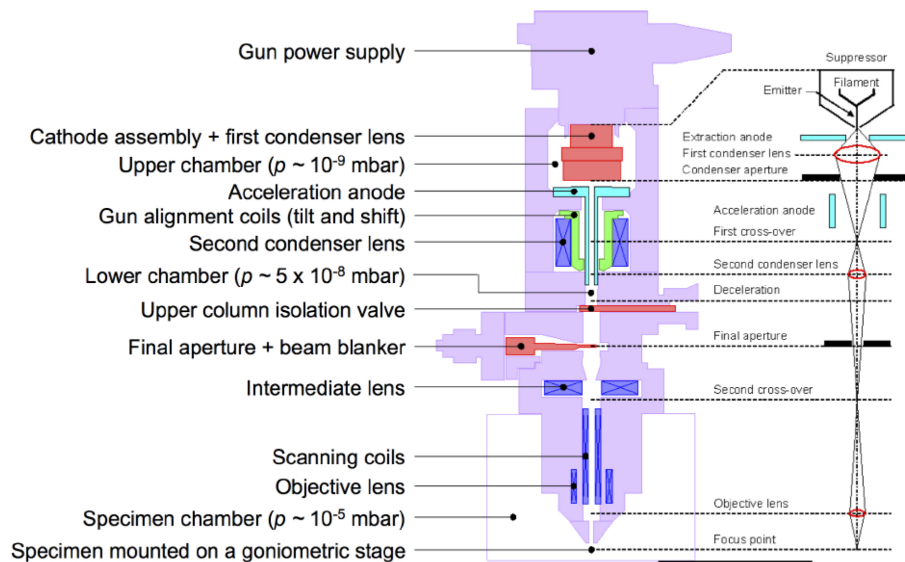


Figure 3.4: *EBL system scheme. For study purpose SEM machine can be adapted for lithography simply adding a beam blanker system and modifying the gun alignment coils. This result in a cheaper but less precise instrument with respect to that dedicated to EBL.*

an adapted scanning electron microscope (SEM) at which a pattern generator and a beam blanker have been added. It have a maximum resolution of about $20\,$nm but result more cheaper with respect to a dedicated system.

The EBL resolution depends on several factors including the electron optics, the used resist, and the substrate. from the first one depends the quality of the spot generated by the thermal field emission gun. It is necessary to have high positional accuracy with limited astigmatism and small spot size. Once the electrons penetrate the polymer layer, they experience many small angle scattering events (forward scattering), each of which deflect the electron slightly. This effect bring to broadens the beam by an amount that increases with the resist thickness. Commonly, the majority of the electrons do not stop in the resist but penetrate deeply into the substrate. A fraction of these electrons experience wide angle elastic scattering and can exit from the surface some distance far from the incident beam. At high energies, these backscattered electrons (BSE) may cause the exposure of the resist causing pattern distortion and overexposure. This phenomenon is known as *proximity effect* and limits the minimum feature size in ordinary SEM adapted systems [94] [95].

The EBL system used in this work is a Philips™XL30 SFEG SEM with a Raith™Elphy Quantum™lithography support and a Scanservice™beam blanker. As shown in the scheme (Figure 3.4) at the top of the column a Field Emission Gun (FEG) in installed. It consist in a very sharp (around $100\,$nm) piece

of tungsten which, under very high electric field, is able to emit electrons. For high performance and high spatial resolution, the electron source should have the following ideal parameters:

- Small tip size;
- Low energy spread of the field-emitted electrons;
- High brightness of the beam (defined as the current density per unit solid angle);

Once the beam is generated it passes through two condenser lenses, with the aim to focus it drastically reducing the spot size. After that the collimated beam is guided through pairs of scanning coils governed by the software system, which are able to deflect the electrons allowing the drawing of the desired pattern on the target. The column, which is divided in an upper and a lower part, is under high vacuum in order to reduce the gas scattering of the beam.

An electron beam lithography operation usually involves several steps. Firstly an alignment procedure is needed to coupling the reference points the CAD design with that of the sample. This is performed through the help of a marking grid previously evaporated on the substrate. The second step consist in the focus of the beam that is a function of the target distance. It is achieved by the "contamination dot" procedure which consist in manually adjust the focus on the edges of a marker and then exposing a dot in order to verify the accuracy of the entire operation. Once this two steps are concluded the automatic exposure can start. To reach the better compromise between the exposure time and the precision of the features, the operator can act on different parameters. The beam current (I_B), quantified by the number of electrons per unit time, is strongly related to the *spot size* d, the lower the dimension the smaller the current value. The *dose* D, defined in unit of μC/cm^{-2}, depends essentially on both the substrate type and the resist, and specify the amount of charge transferred from the primary electrons of the beam to the polymer. Since different features require distinct doses, the controller software allows the use of a scale factor f for D. The last parameter, namely the *step size* s, fix the distance between two subsequent positions of the beam. With this variables the calculation of the dwell time, defined as the time needed to transfer the planned amount of charge to the target, becomes:

$$\tau = \frac{Ds^2}{I_B}$$

therefore the total time needed to expose an area A of resist is obtained by:

$$t = \frac{A\tau}{s^2}$$

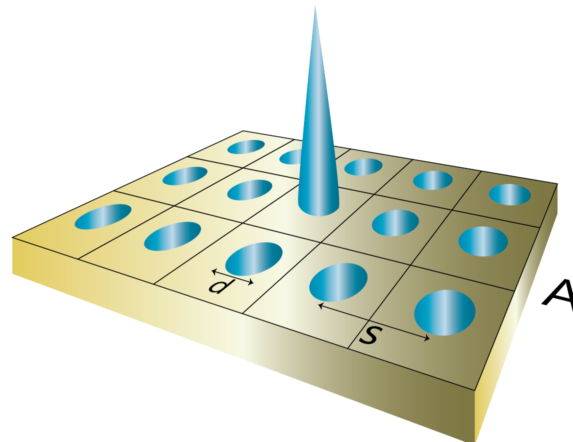


Figure 3.5: *Scheme of some EBL controlling parameters; the spot size (d) and the step size (s) are very important in the definition of the exposure time for an area (A).*

Structures Design

The possibility to fabricate sub-micrometer structures of almost any shape is allowed by the use of Elecron Beam Lithograpy. Raith™ELPHY Quantum™is a lithography system which makes it possible through electron beam writing in connection with a Scanning Electron Microscopy (SEM) setup. It provides a simple CAD software, namely "Raith ELPHY Quantum GDSII Editor", which allows the modification of the structure design and the setting of the controlling parameters.

Different layers are built in order to differentiate the device design. Firstly a graphene stripe is defined at the center of a 1000×1000 µm area, then electrodes of different shape and size are drawn on it, and finally the external connections are performed. To any of these layers different e-beam controlling parameters, such as the spot size and the dose factor, are set.

Resist and Developer

According to the purpose which the devices is fabricated for, different kind of resists can be chosen for the EBL process. The main difference from one to another is whether they become less (negative resist) or more (positive resist) soluble when hit by an electron beam. In this work PMMA with different density and molecular weight have been used as a positive resist. It consist in a colorless thermoplastic polymer which is diluted in a solvent like chlorobenzene for EBL purpose. This solution is deposited on the top surface of the substrate, which is then rotated at high speed in order to spread the coating material by centrifugal force. This procedure, namely *spin coating technique*, creates a very uniform layer of material. After the

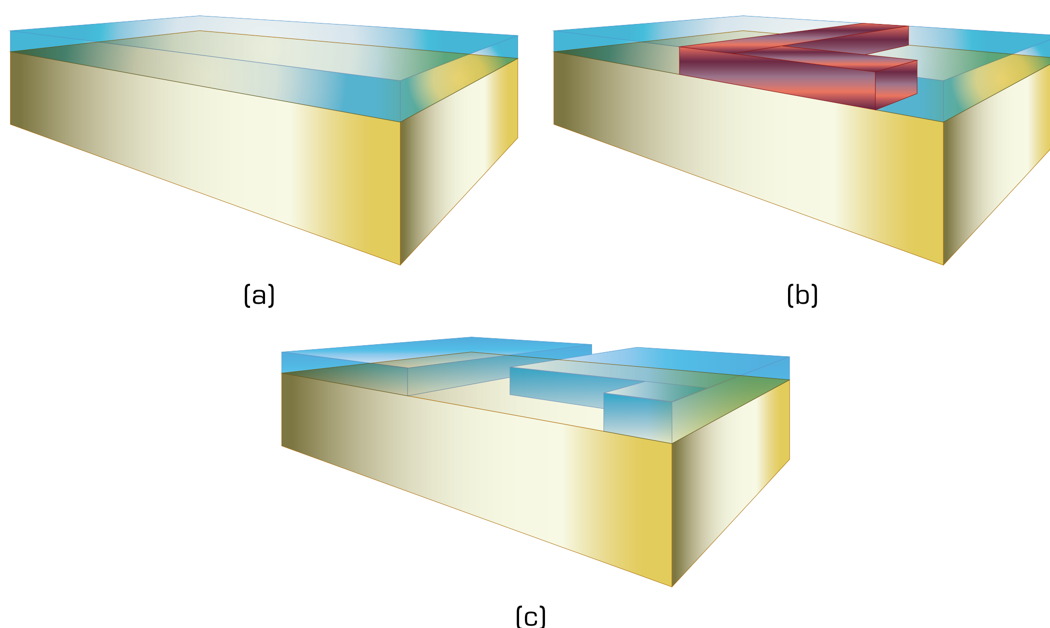


Figure 3.6: *Scheme of a lithography process: firstly a layer of resist is deposited on the top surface (a); the desired mask is patterned drawing with an electron beam (b) and finally the exposed polymer is dissolved by a develop solution (c).*

evaporation of the solvent by baking, a dense polymer film remains on the substrate. The rotational speed, the density of the polymer and the geometry of the sample influence the final layer thickness. In this work multiple layers have been deposited during any step of lithography all of them at a speed of 8000 rpm. The number of coat, as well as the PMMA molecular weight, depend on which steps of the fabrication come after the EBL.

Once the lithography step has been concluded, the sample is washed in a solution of organic solvents which is able to selectively remove the exposed polymer leaving a patterned mask on the surface. Here a solution of isopropanol and 4-methyl-2-pentanone (3:1) has been employed in order to "develop" the samples.

3.2.2 Reactive Ion Etching

In CMOS technology for Ultra High Scale Integration, many etching methods have been introduced so far. Most of them use complicated and expensive equipment. The etching of graphene, instead, requires a simple low pressure oxygen plasma.This kind of technique, classified as a *dry etching*, is used for its high anisotropy and selectivity, which allow to obtain well defined etched areas. Once the resist mask is performed during the first step of lithography, a *Reactive Ion Etching* (RIE) procedure is executed. Firstly

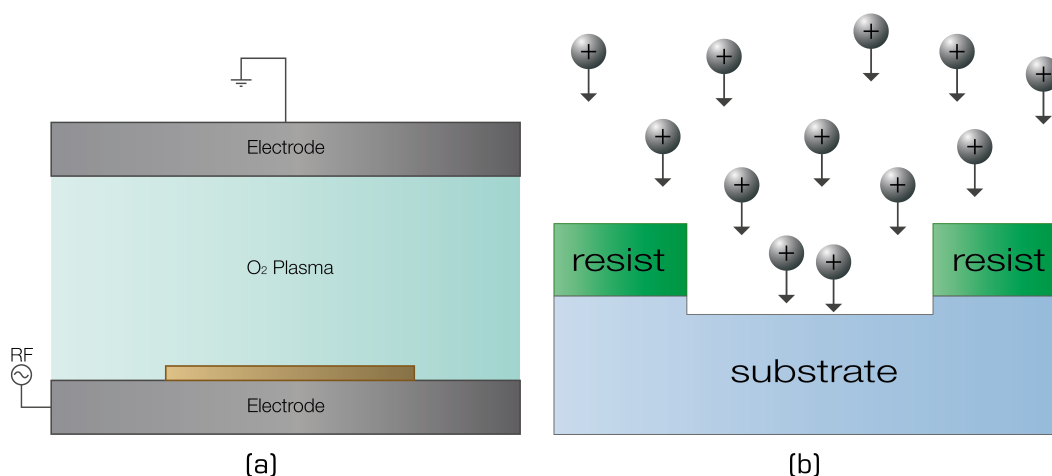


Figure 3.7: *RIE process. (a): schematic of the inner part of a RIE system. The plasma forms between the two electrodes under a radio frequency electric field.*
(b): The "heavy" ions are accelerated towards the surface where the part to be etched is uncovered by the resist mask.

the chip is mounted on the lower of two parallel conductive plates; after the creation of vacuum in the chamber, used for pumping impurities away, a controlled flux of oxygen is introduced. Between the two electrodes, a strong radio frequency[1] field is applied, ionizing the gas molecules by stripping them of electrons. After a transient time the plasma stop grows, then the electrons contribute in charging the lower plate, generating a strong electric field directed towards it. Because of this the positive ions start moving against the sample. Here two different etching "strategies" takes place one chemical and one physical. The former is due to the high reactivity of the oxygen radicals, the latter consist in the sputtering of materials due to a kinetic energy exchange between the ions and the surface. To control the etching rate three parameters are important: the power under which the RF field is generated, the oxygen flux, measured in standard cm^{3}min^{-1} (sccm), and the pressure of the chamber.

In this work a Plasma Technology™plasma etcher have been used to define the active graphene areas in the chip. The machine generate a plasma under an electric field oscillating at a frequency of 13.56 MHz. The oxygen flux and the chamber pressure were set at 500 sccm and 100 mTorr.

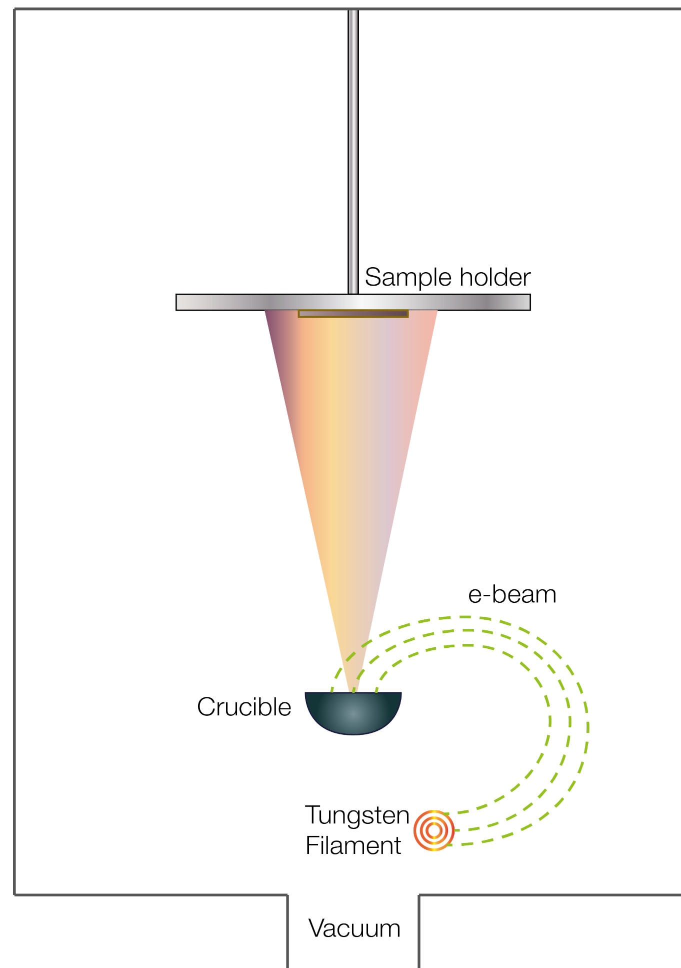


Figure 3.8: *Scheme of an electron beam evaporation system. The sample is hold face down exactly over the source crucible. Once the electron beam hit the metal it evaporate depositing on the cold surface of the chip.*

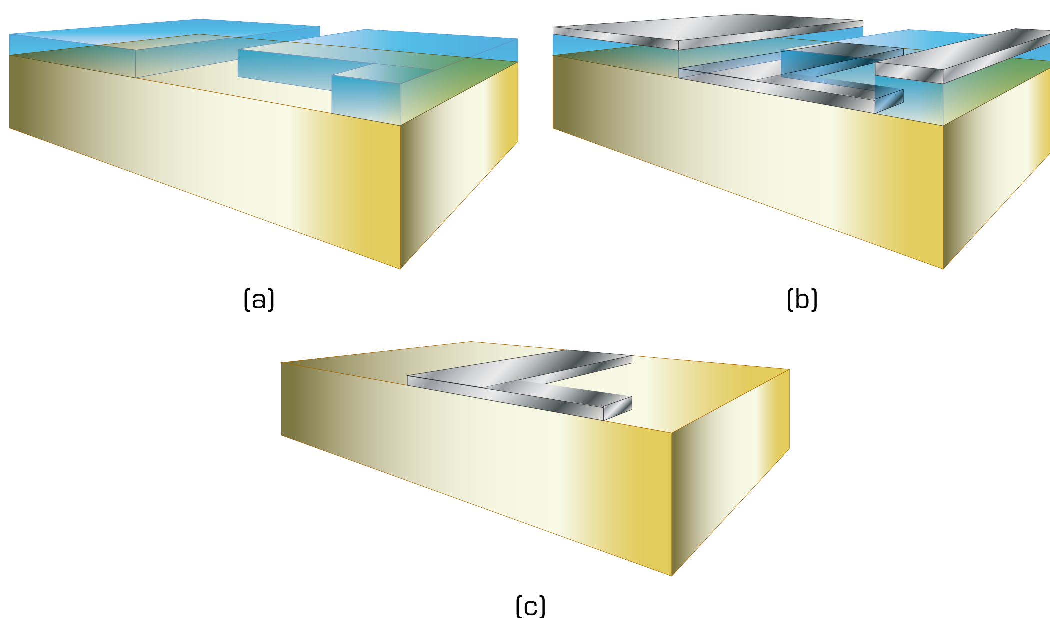
3.2.3 Electron Beam Evaporation

Once a mask is patterned on the substrate surface by EBL, the metal contacts can be evaporated by means of the *Electron Beam Vapor Deposition* (EBVD) technique. As shown in Figure 3.8, the sample is stuck on an holder placed exactly above the metal source in an high vacuum (10^{-6} mbar) chamber. Electrons are generated by thermionic emission[2] from a tungsten filament located under the crucibles zone. Hence the beam passes through a deflection system, generated by a magnetic field, which direct the ray towards the evaporation material. As soon as the electrons strike the metal, they lose their kinetic energy very rapidly, causing the heating of the target, bringing it to melt or to sublimate. Particles, which are in a vapor state, can thus sublimate on the cold surface of the sample. The rate of deposition is evaluated by a quartz crystal microbalance (QCM), which is able to measures a mass per unit area by accordingly to the change in frequency of a quartz crystal resonator. In this work a Leybold™LH 560 e-beam evaporator have been used; besides the possibility to load up to four different crucibles, it provide two sample-holding positions. When the substrate is mounted near the crucibles zone, namely *lower position*, the growth rate is ten times faster then when it is hold in the standard *upper position*. For reaching a good metal film quality, the deposition rate should be slow and very controlled. In order to allow this, some parameters have to be checked; first of all the vacuum pressure is really important to ensure a good quality of the electron beam as well as to limit the scattering of the evaporated particles which can lead to not-homogeneous film deposition. The rate of evaporation is directly controlled by both the power of the beam, i.e. the kinetic energy of the electrons, and its spot size, which allows to spread the energy on a smaller or a bigger area.

After the evaporation took place, over all the surface a thin film of material is present (Figure 3.9). The procedure of removing the polymer mask is called *lift-off*. It simply consist in a bath in organic solvent followed by a gentle jet of acetone to remove the residues and then a rinse with isopropanol. This is a very delicate operation during fabrication since it is easily to damage the structure.

[1]High frequency variation of the electric field is needed in order to create a stable plasma. The "light" electrons are accelerated up and down from the RF signal, moving faster between the walls, whereas "heavy" ions remains almost stationary.

[2]Heating the filament over a threshold value, the electrons acquire enough energy to overcome the potential barrier, i.e. the *work function* of the metal, passing from a binding to a free state.



(a) (b)

(c)

Figure 3.9: *Scheme of the evaporation process.*
Once the EBL mask is ready (a), the evaporation process takes place, depositing a metal layer over the entire surface (b); during the lift-off procedure the resist is dissolved in a solvent and only the patterned metallization remains on the substrate(c).

3.3 Step by step TLM structures fabrication

During this work several chips for contact resistance test with distinct specification have been processed. Their fabrication involved different steps each of which starting with a lithography procedure. Here the method for the fabrication of standard TLM structures is described, starting from a sample with $300\,\mu m$ of thermally grown SiO_2 on top of a degenerate-doped silicon substrate, metallized on the back. Some differences exist between the various fabricated structures, however, since they involve only small variations in the initial design step, their description is given in section 4.3.

The choice to make TLM structures for measuring contact resistance has been taken due to the fact that it is a very powerful tool which, with one configuration, allows the analysis of different parameters in the circuit. It simply consists in a set of back-gated transistors, which are deposited on the same piece of graphene, separated by progressively smaller distances.

3.3.1 Design

The first step consists of the planning of the entire production process. Each chip contains several structures fabricated in a squared area[3] of 1000×1000µm^2. Since the fabrication involves many steps of EBL, the design is divided in multiple layers concerning the different parts of the structures. First of all the graphene channel, which is common for all GFETs, is defined. It consists of a 5×100µm *stripe* of unexposed resist at the center of the $WF = 1000$. The electrodes are then defined in a $WF = 300$ or a $WF = 100$ depending whether the exposure type should be "blind". Finally the external connections are made by patterning rectangular pads in a $WF = 1000$.

All the EBL controlling parameter can be chosen during the design step (see section 3.2.1). For each WF both the beam spot size and the step size are defined. However the use of different WFs introduces possible misalignments in the exposures. Therefore during the design step it should be taken in consideration to overlap the features edges at the boundaries of different WFs. Finally, the dose, set as a common parameter, can be scaled by a factor (less or greater then 1) specific for any part of the structure.

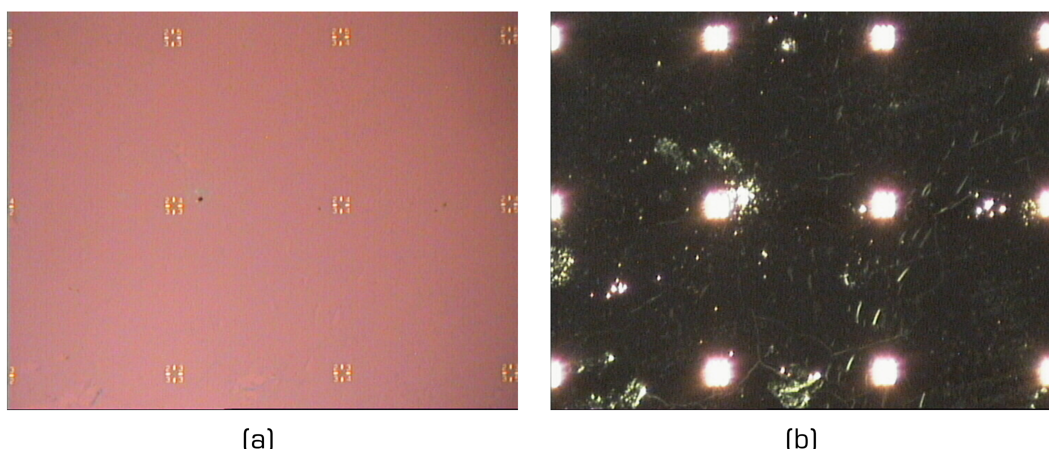
3.3.2 Sample Selection

After the design step is completed a sample with a good quality graphene is needed in order to ensure the most reliable results. The selection is simply made by checking it under a standard optical microscope in both bright and dark field (Figure 3.10). The latter is used for its ability to enhance the contrast, showing cracks and borders in graphene as well as relatively big defects in the oxide layer below.

3.3.3 Graphene Etching

Before starting the graphene stripes exposure, three layers of PMMA with an average molecular weight (M_w) of 950 K are deposited on the sample. Each layer is spincoated at 8000 rpm for 30 seconds and then baked at 160 °C for one hour in order to ensure the complete evaporation of the solvent. The final resist thickness is around 400 nm to ensure enough protection during the etching process. After the PMMA deposition, the standard e-beam exposure step is performed followed by a 90 s bath in the developer solution and one minute rinse in isopropanol. Once the mask is formed, 25 s of RIE are needed to ensure the complete elimination of excess graphene in the

[3]During the EBL the entire area of exposure is divided in smaller portions called *Writing Fields* (WFs). Here three different WFs have been used: the $WF = 1000$ define the area for an entire structure, the $WF = 300$ characterize the electrodes *"blind"* exposure, whereas the $WF = 100$ determine the area for a "manually" aligned lithography.



(a) (b)

Figure 3.10: *Graphene pictures taken by the optical microscope in (a) bright and (b) dark field. Using the dark field it is easy to recognize the bigger defects on the surface.*

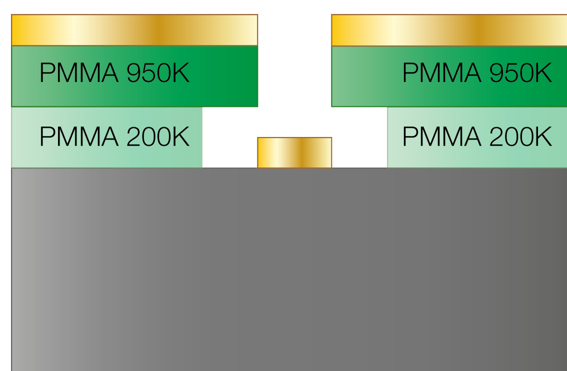


Figure 3.11: *The use of different molecular weight resists allows the formation of an undercut which makes easier the subsequent lift-off procedure.*

developed parts. Lastly the residual PMMA resist is dissolved after two hours of acetone bath.

3.3.4 Electrodes and External Connection

Another EBL step is required for patterning the electrodes. Here two layers of different PMMA are coated. The bottom one has an average molecular weight of 200 K whereas the top one has $M_w = 950$ K. The lower molecular weight of the former allows the formation of the so called *undercut* resist profile (Figure 3.11) which helps in the dissolution of the resist once the metal is deposited on the surface. After the EBL, the sample, with the patterned mask on top, is ready for the next step of metallization. The evaporator is loaded with the chip mounted on the holder with the top face looking to the crucibles zone and the vacuum pumps are turned on. Once

the pressure is in the order of 10^{-6} mbar the e-beam is generated rising gradually its power. Then the shutter over the crucible is opened and the metal starts to deposit on the surface. Usually an evaporation rate in the order of ≈ 10 Ås^{-1} is used. Finally the lift-off procedure takes place. The sample is put in a cold acetone bath for at least 4 hours. Then by the use of a gentle acetone jet, the excess metal is pulled off leaving the chip ready to be measured.

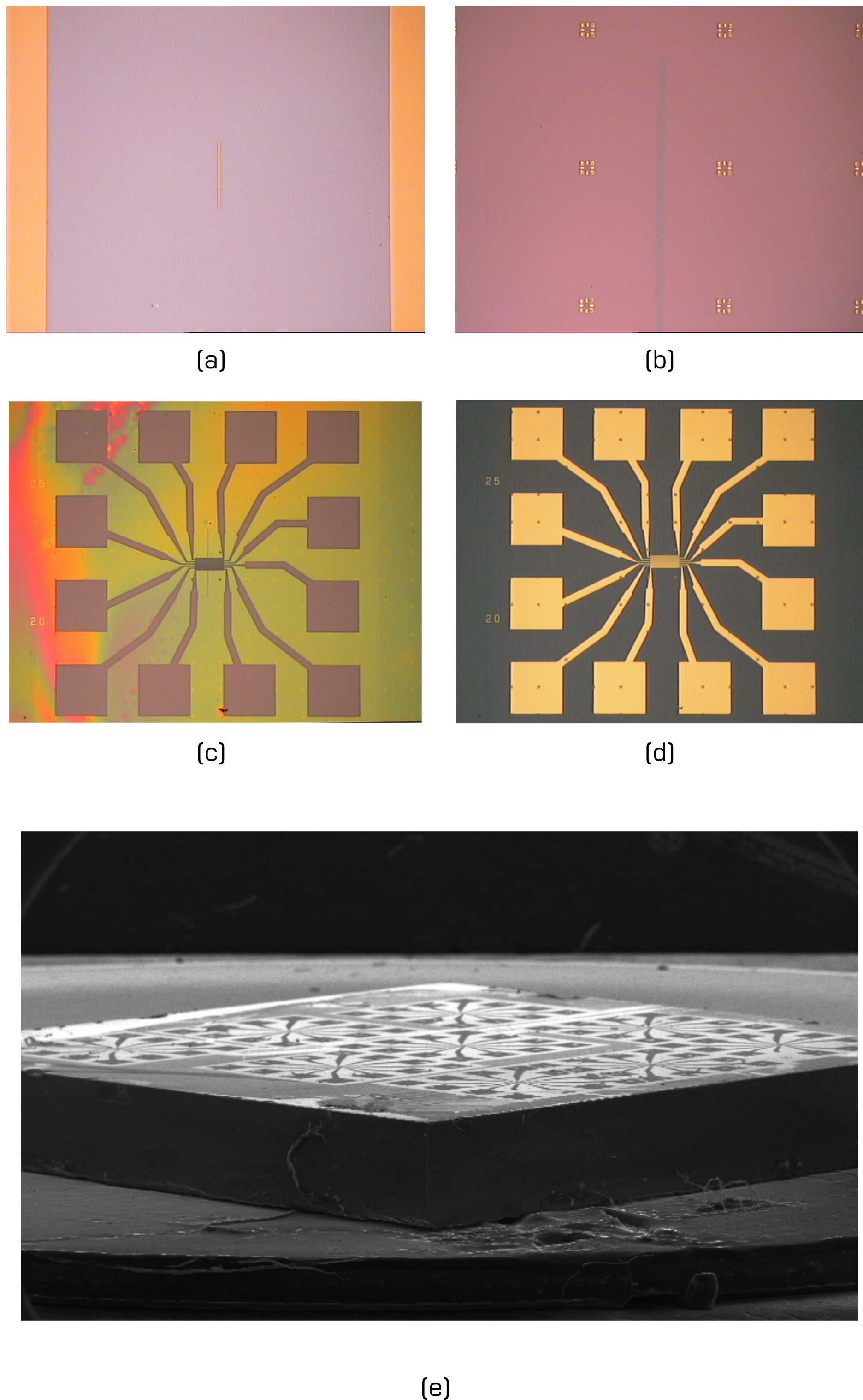


Figure 3.12: *Representation of the entire fabrication process. (a): an area of* $1000 \times 1000 \mu\text{m}^2$ *is completely exposed except of the stripe at the center. After the subsequent etching procedure only a* $5\,\mu\text{m}$ *width of graphene remains (b). The electrodes and the external connections are then patterned (c) and evaporated (d). The final result is showed in (e) through the use of a SEM. The entire chip is composed by nine different structures fabricated at the same time.*

4 Results

This chapter provides a detailed description of the contact resistance tests made during this work. In section 4.1 the Transfer Length Method, which is used to measure contact resistance, is fully explained. Section 4.2 presents a first analysis on the graphene-metal contact determining which kind of material provides the best performance in terms of carrier injection. Once the choice of the optimum metal has been done, in section 4.3 structure with different contact features will be analyzed with the aim of lowering the resistance under the limit of a plain metal contact.

Once a sample has been fabricated, a set of electrical tests were performed in a custom-built probe station. The set-up consists of two source measurement units (SMU), provided by Kithley™, which are capable of both sourcing and measuring at the same time. One of them supplies the voltage at the back gate which is linked by a conductive plate. The other one, which is connected to the electrodes through several needle probes, provides the voltage V_{DS} at the tested transistor, whereas at the same time it measures the current flowing toward the terminals. To avoid adsorption of contaminants and the deposition of external particles on the chip during the measurements, a constant flux of nitrogen is blown toward the surface. The results are then acquired through the use of a custom-built LabView™software, which allows to control the SMUs and collect the data.

4.1 Transfer Length Method

In section 2.4.3 the role of graphene-metal contacts in the increase of the series resistances of GFET based devices have been discussed. Since the bandwidth in a high frequency device is limited by the time constant $\tau = RC$, it is crucial to understand and quantify the contact resistance in order to move forward in graphene electronics. Several parameters have been introduced in the investigation of contact resistance during the years and many of them took different names in the literature. Here contact resistance, measured in ohms (Ω), is referred as R_c, the graphene sheet resistance, which is a 2D resistivity, is denoted with R_{sh} and have dimensions of "ohms per square" ($\Omega/\square$), and finally the *specific contact resistivity* $\rho_c^{\square}$, which quantifies the interfacial resistance of the graphene-metal contact to the current flow, is in Ωcm^2. Furthermore, to make contact resistance independent from the geometric factors, it is common the use of the so called "contact resistivity" simply given by $\rho_c = R_c W$, expressed in unit of $\Omega\,\mu\text{m}$.

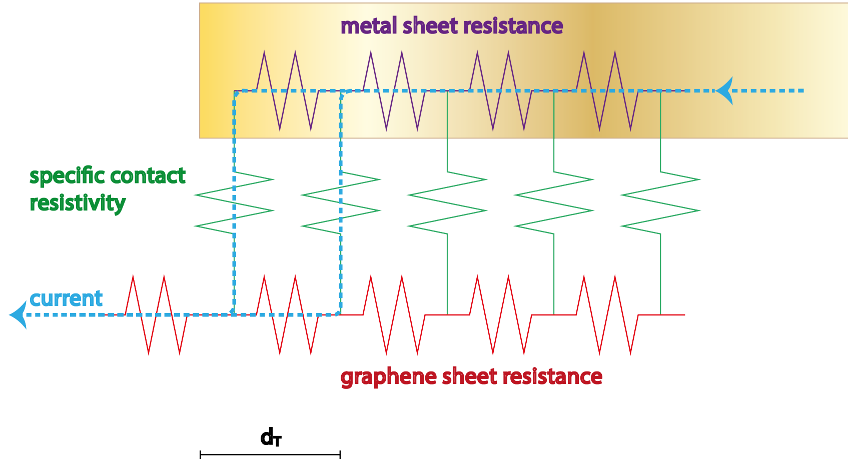


Figure 4.1: *Model of a metal-graphene contact. During its path the charges experience different resistive "forces" coming from the metal sheet resistance, the specific contact resistivity at the contact interface, and the graphene sheet resistance. Here it is also shown the "current crowding" effect, which involves the current flowing preferentially through the contact edges; precisely, the most of the charge transfer takes place in a distance* d_T *from the contact boundary corresponding to the transfer length.*

If the current flow can be considered uniform under the contact area, R_c becomes simply equal to $\rho_c^{\square}/(W \cdot D)$ where W and D refer respectively to the contact width and length. As demonstrated by Nagashio and Toriumi [14] this is not the case for graphene where, conversely, the "current crowding" effect takes place leading the current to flow preferentially through the edges (Figure 4.1). Hence it is possible to define a transfer length d_T as the average distance over which the most of the charge exchange between metal and graphene occurs. In this case the expression for the contact resistance should consider the "effective contact area" $W \cdot d_T$ becoming:

$$R_c = \frac{\rho_c^{\square}}{W d_T} = R_{sh} \frac{d_T}{W}$$

with d_T defined as:

$$d_T = \sqrt{\frac{\rho_c^{\square}}{R_{sh}}} \tag{4.1}$$

A common approach in determining the contact resistance is the use of the Transfer Length Method (TLM). It consists of an array of equal area contacts deposited on a rectangular stripe of graphene placed at different distances from one another. Two test probes are placed on a pair of neighboring contacts which become the source and drain of a graphene transistor. Once a voltage is applied the GFET turns on, and the resistance

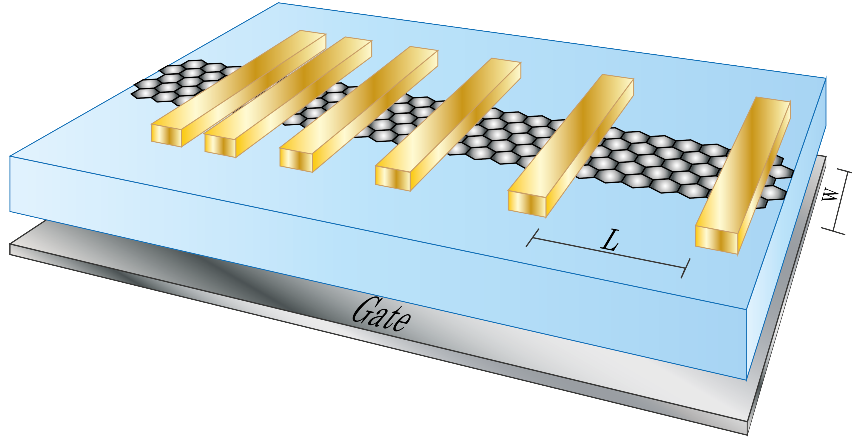


Figure 4.2: *Transfer Length Method based on the measurement of the resistance in the flow of charges between two neighboring electrodes. Here* W *and* L *identify respectively the width and the length of the channel.*

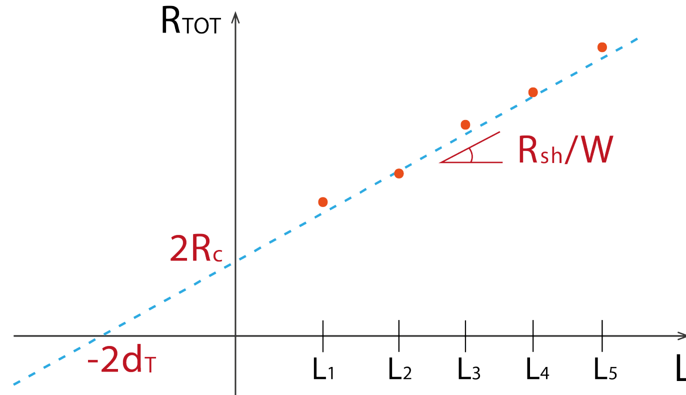


Figure 4.3: R_{TOT} *versus* L *plot. The red points represent the experimental values taken by the resistance measurements. A linear fit is made in order to find the complete set of parameters which characterize the contact resistance and the graphene sheet resistance.*

is calculated by measuring the current flow which is modulated through the use of a back gate voltage (V_{BG}). In this way a classical $R - V_{BG}$ transfer curve is obtained, which reaches a maximum at the Dirac point. This value is then plotted against the channel length L in order to extract the contact resistance (Figure 4.3).

As shown in Figure 4.1 different values contribute to the measured total resistance. The first contribution comes from the sheet resistance of the metal which is negligible since it shows a very low value with respect to other. The second contribution arises from the graphene-metal junction and is denoted by the contact resistance; since it is supposed that the circuit is comprised of two equal contacts the impact on the total resistance is doubled ($2R_c$). The last one stems from the flow of charges in the GFET

channel, namely *channel resistance* (R_{ch}), and is a function of the graphene sheet resistance and geometrical factors. Therefore the total measured resistance as a function of the spacing L becomes:

$$R_{TOT}(L) = R_{ch}(L) + 2R_c = \frac{R_{sh}}{W}(L + 2d_T) \quad (4.2)$$

As shown in Figure 4.3, this result in a linear plot of R_{TOT} versus L which allows the extrapolation of many parameters. In the limit of $L = 0$ the channel resistance is equal to zero and the unique contribution to R_{TOT} is given by $2R_c$. The slope of the curve, i.e. dR_{TOT}/dL, gives the value of the sheet resistance normalized to the channel width (R_{sh}/W) whereas the point where the line intercepts the L axes, identifies the value of $-2d_T$.

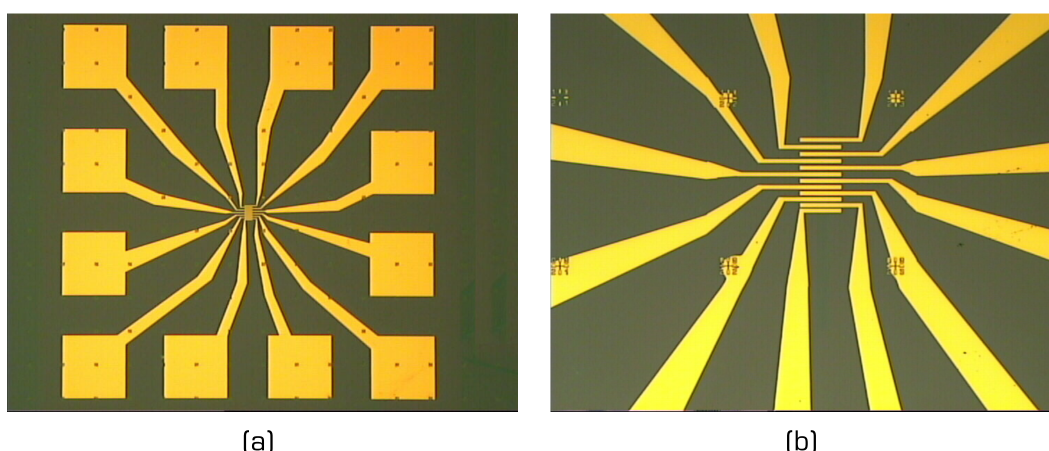
4.1.1 TLM structure specifications

The first objective of the performed experiments was to make the results reproducible and as reliable as possible. In order to ensure this, in this work a detailed analysis on the electrodes separation has been performed. Contacts spread over a very long stripe of graphene, make the local quality of the GFET channel to have a large impact on the final results. On the other hand a too short separation of the electrodes makes difficult to control the error in the linear fits of the obtained resistance points. Here TLM structures with contacts gaps ranging from 700 nm to 1450 nm have been fabricated. Shorter distances have been avoided due to the high proximity effects which takes place during the lithography procedure, leading to a broadening of the contact area.

4.2 Ab initio analysis of metal-graphene interaction

Graphene is a quite-new material and because of this the impact of the fabrication steps on the final device performances have not been fully understood yet. Different transfer methods, as well as the use of various types of resists and solvents, combined to the specific fabrication process, bring to substantial mismatch in the results of a test. In order to avoid this unwanted effects, the here reported analysis has been made on chips fabricated following the standard procedure described in section 3.3.

In literature it is possible to find a few works on the graphene-metal contact resistance, and some of them, even working with the same contact material, show different values of R_c. In Table 2.1 a collection of the best results so far obtained is presented.



(a) (b)

Figure 4.4: *(a): Image taken at the optical microscope of an entire TLM structure. The test probes are placed on the squared metal pads which allows the connection with the inner active part.*
(b): 100x zoom of (a). In the middle of the electrodes the stripe of graphene is barely visible.

As a preliminary step in this work the fabrication and test of TLM structures with different metal contacts have been performed. Chips with nickel-gold, palladium-gold and pure gold electrodes have been analyzed and the contact resistances at the Dirac point extracted. The results are collected in the plot in Figure 4.5. Nickel provides the highest contact resistance, whereas Pd-Au and Au show better result. In particular pure gold stabilize around $250\,\Omega$ µm. The fact that Au contacts provide the lowest values of R_c is also supported by the evidence that in the case of Pd-Au, the less the thickness of the palladium layer the lower the contact resistance is (Figure 4.5).

4.3 Au-graphene contacts

Once was gold selected as the best performing material, different electrode configurations have been fabricated, with the aim to analyze the impact of their particular features on the contact resistance. As mentioned previously, graphene exhibits the "current crowding" effect which involves the current flow preferentially from the edges of the contacts. Ideally the longer the metal-graphene boundaries the lower should be R_c. In this work two different methods have been adopted in order to reach this target:

- increasing the contact perimeter patterning the metal boundaries in a zig-zag fashion;
- increasing the edges etching the graphene underneath the electrodes;

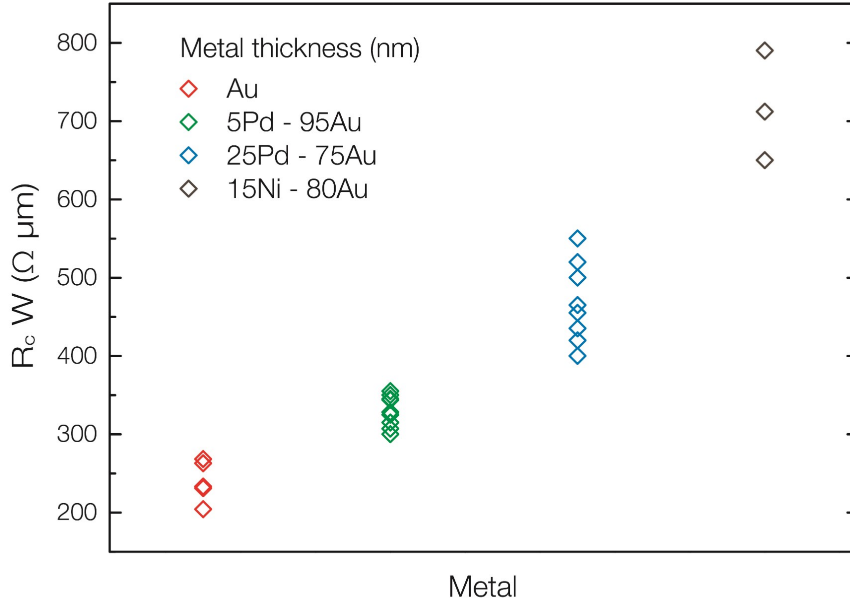
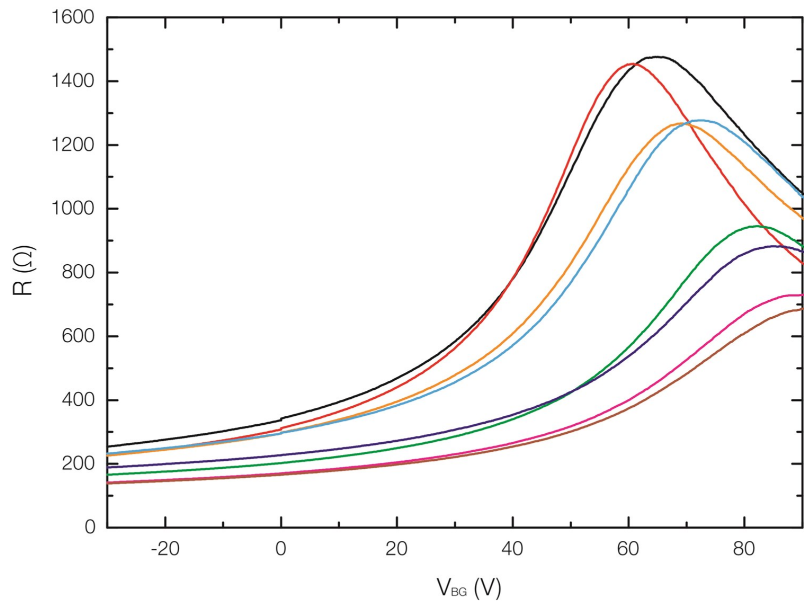


Figure 4.5: *Contact resistance measured for different metal-graphene contacts. Gold shows the best result with an avarage value of R_c in the order of* $250\,\Omega\,\mu\text{m}$.

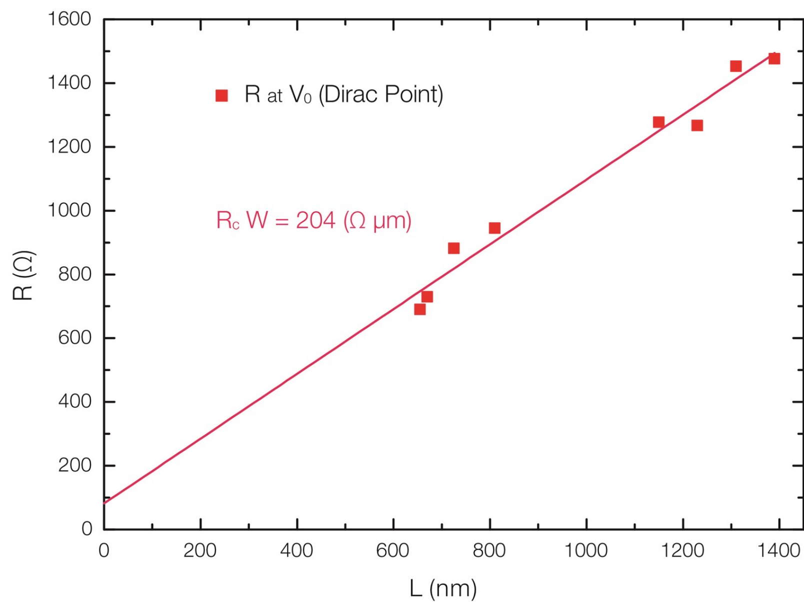
The first configuration (Figure 4.7) have been obtained by patterning the contact boundaries in a zig-zag shape, increasing the metal-graphene perimeter of about the 40%. This has been made during the second EBL step, before the evaporation of gold. The second configuration (Figure 4.8) consists of a matrix of holes etched in the region where the contacts will be evaporated. In this way the contact perimeter is almost tripled, leading to a theoretically better carrier injection. Since the exposed holes need to be etched in graphene this process is performed during the first step of lithography. It is noteworthy that both methods do not introduce any new steps in the fabrication process. This makes the comparison of the TLM test results of these newest structures with that of standard gold electrodes more reliable.

4.3.1 Data comparison

Comparing the results obtained on standard TLM structures (shown in Figure 4.6(a)) with that of the first proposed pattern (Figure 4.9), it is possible to notice that almost no change in the contact resistance occurs. Moreover looking at the $R - V_{BG}$ curves the bell shape remains approximately the same, confirming that the contact behavior is unchanged. This is probably due to the fact that while the increase in the contact boundaries theoretically lead to a W parameter 40% greater than that of standard structures, practically there is no impact on the carrier injection because the geometrical size of

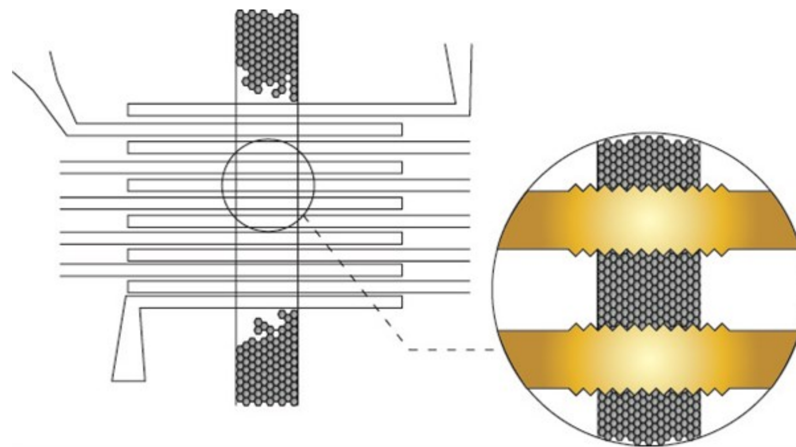


(a)

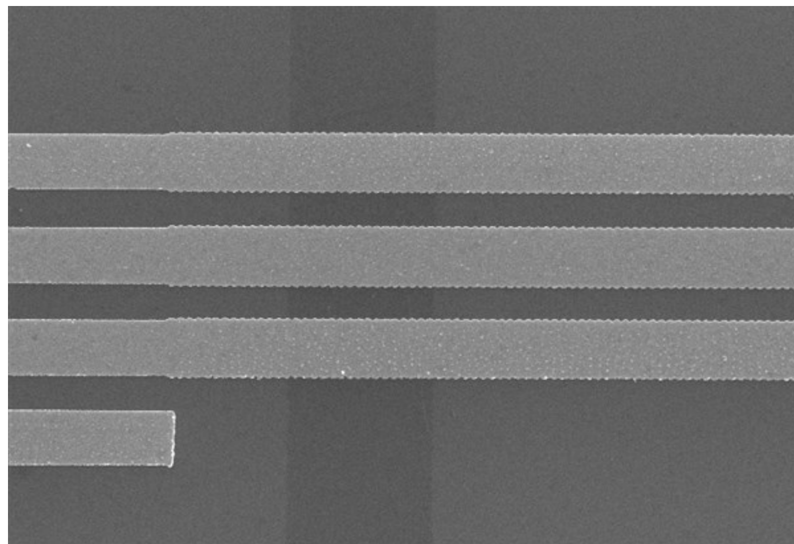


(b)

Figure 4.6: *Standard gold electrode plots. (a): collection of* $R{-}V_{BG}$ *curves taken between electrodes at different distances.(b): The R data of (a) are taken at the Dirac point and fitted by a straight line. The intercept gives the value of* $2Rc$.

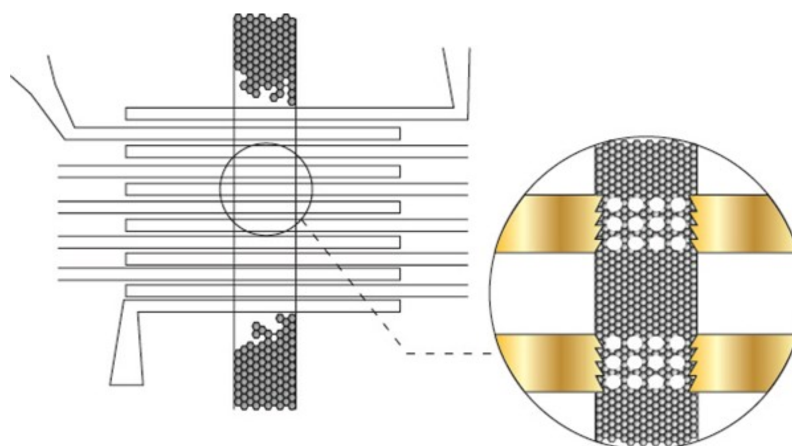


(a)

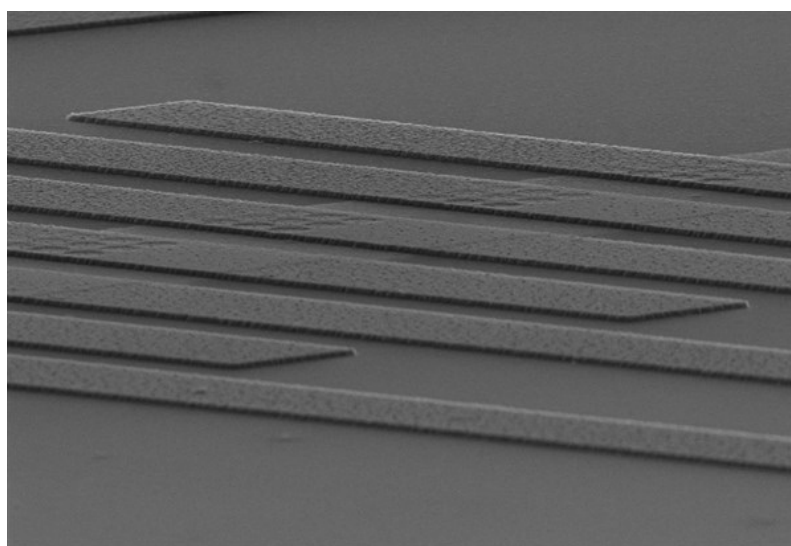


(b)

Figure 4.7: *(a): design sketch of a "zig-zag" patterned TLM structure. (b): SEM image of the same structure after the electrodes deposition. Graphene is clearly visible in the center of the structure (dark stripe).*

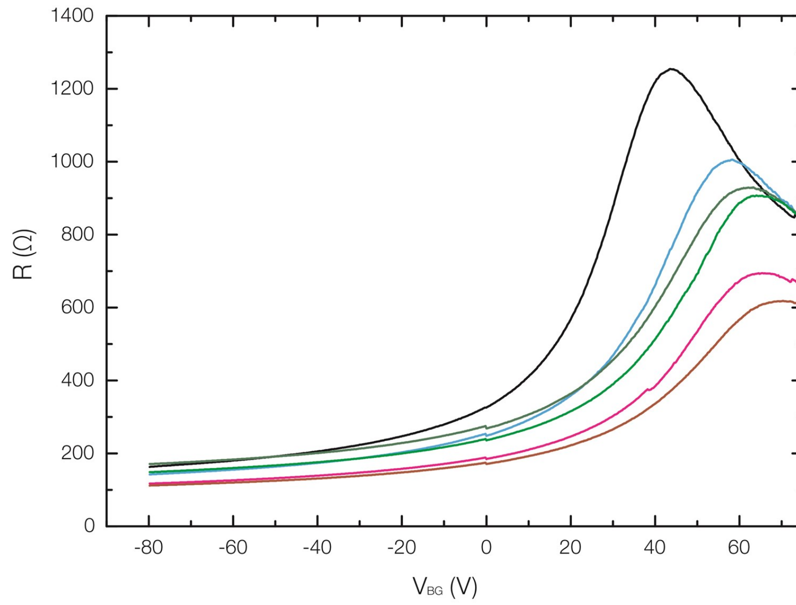


(a)

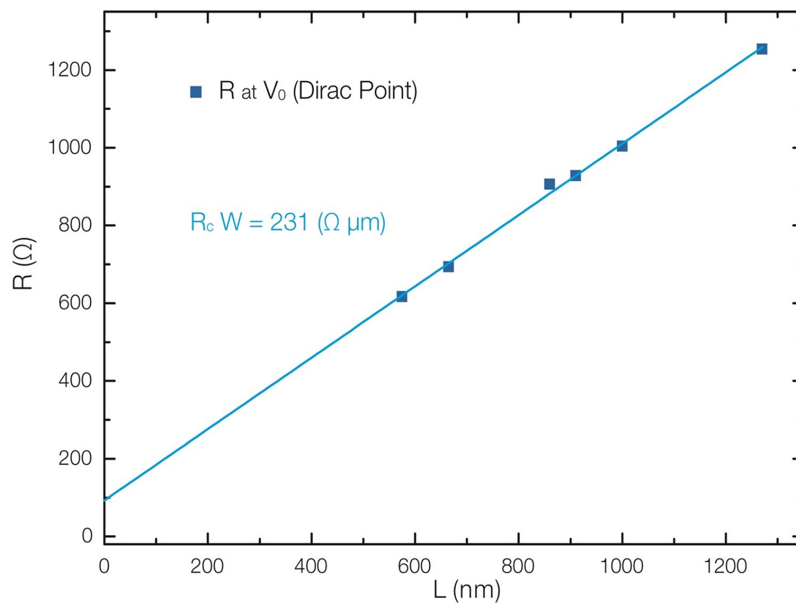


(b)

Figure 4.8: *(a): design sketch of a TLM structure with etched holes in the graphene underneath the electrodes. (b): SEM image of gold contacts deposited on a graphene stripe. The holes matrix beneath the metal is clearly visible.*



(a)



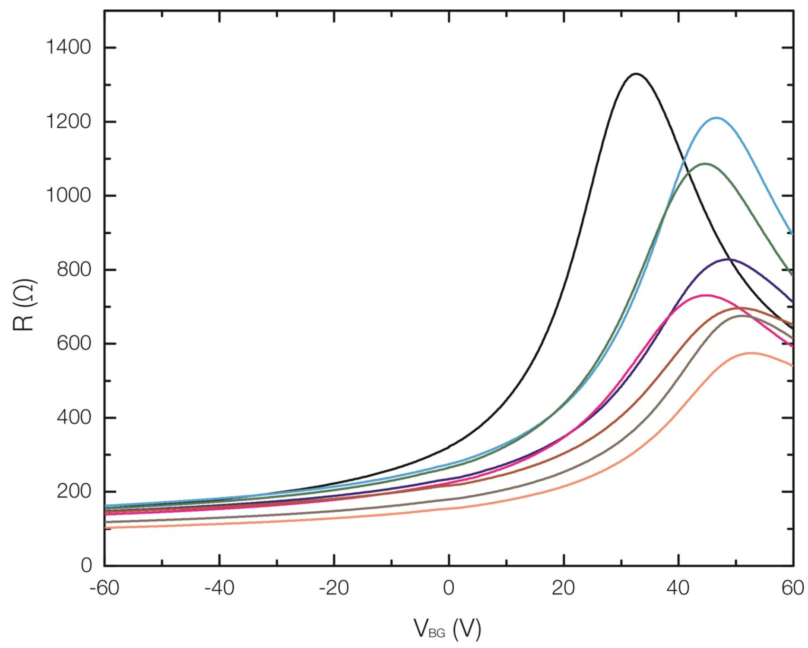
(b)

Figure 4.9: *$R - V_{BG}$ plot and a TLM linear fit for a "zig zag" structure.*

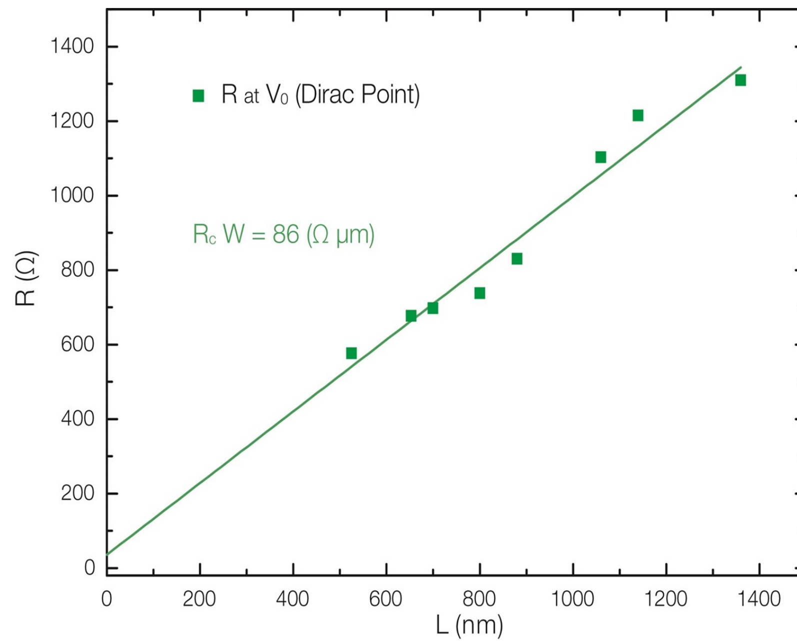
the pattern is smaller than the transfer length d_T.

In the case of the etched matrix of holes a large improvement in contact resistance is obtained. Values around $90\,\Omega\,\mu$m have been reached which so far are the best ever reported in literature (Figure 4.10). This confirms that an increase in the edges length, lead to a better carrier injection and therefore a lower contact resistance.

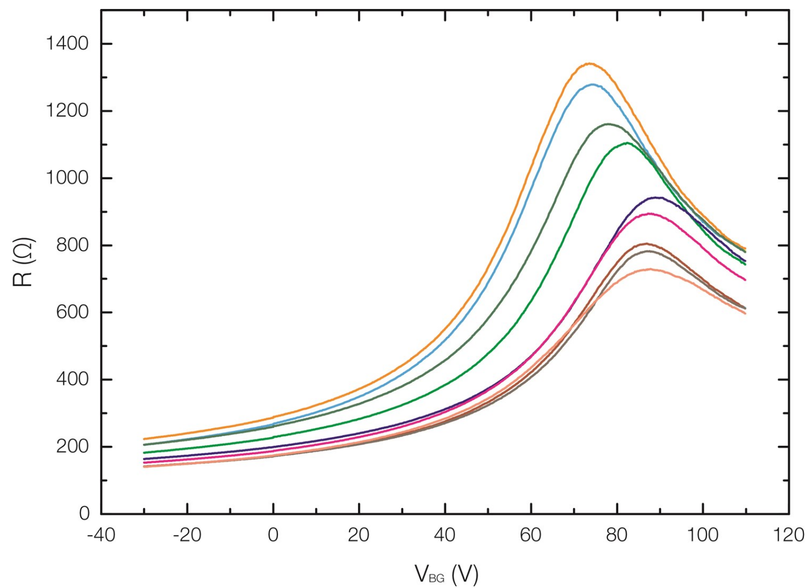
A quite high value of the sheet resistance have been extracted from the plots both for standard electrodes as well as those investigated here. From the fitted linear curves, values of R_{sh} around $5\,\mathrm{K}\Omega/\square$ are obtained. This leads to a substantial difference in the transfer length for the two types of contacts: in the case of zig-zag electrodes d_T ranges from $40 \div 70$ nm whereas is less then a half in the case of etched holes ($16 \div 20$nm). From equation 4.1 it is possible to calculate the specific contact resistivities which in case of standard electrodes are around $10^{-7}\,\Omega\mathrm{cm}^2$ reaching extraordinary low values of $\rho_c^{\square} = 1.3 \times 10^{-8}\,\Omega\mathrm{cm}^2$ in that with holes. Furthermore a comparison between the characteristic $I_D - V_{BG}$ curves (Figure 4.12), shows a steeper rise of the current with respect to the back gate voltage for the etched structures and therefore a higher transconductance. This is a promising result for application in radio frequency devices since, as explained before, in order to reach very high operational frequency, a large value of g_m of a GFET is required.



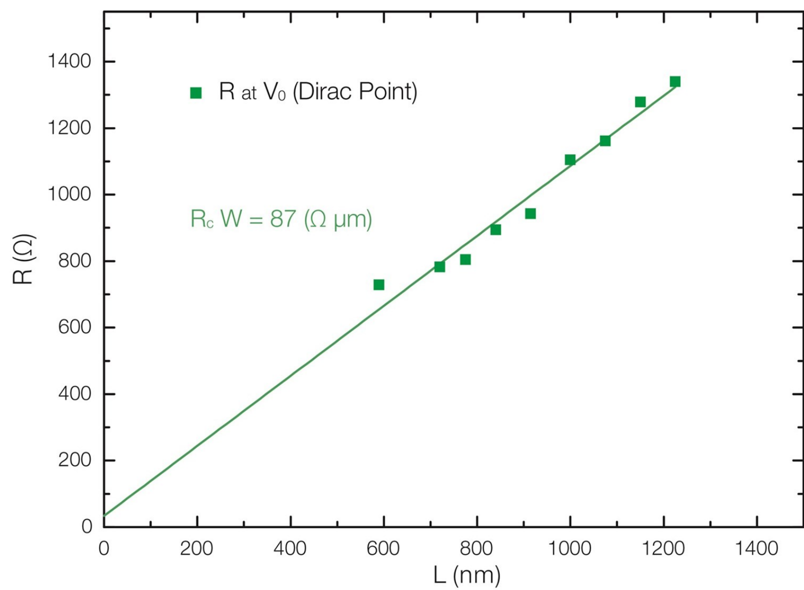
(a)



(b)



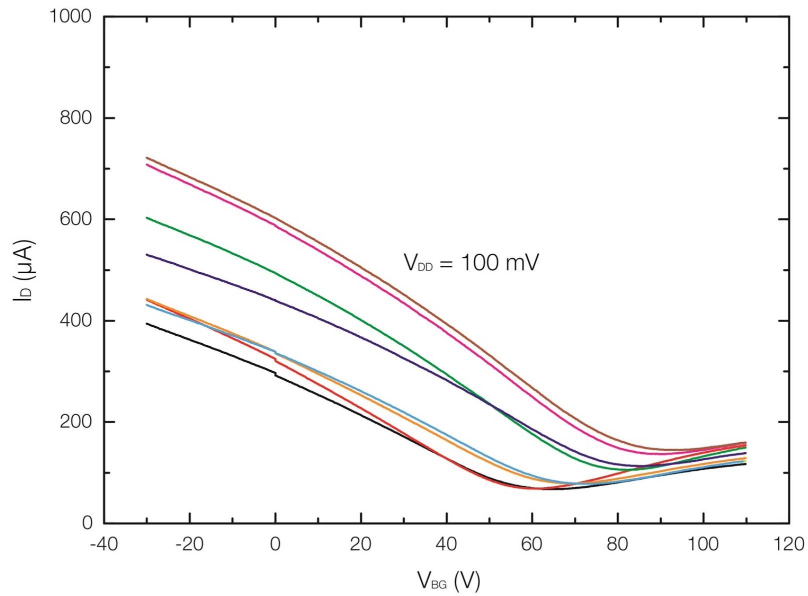
(c)



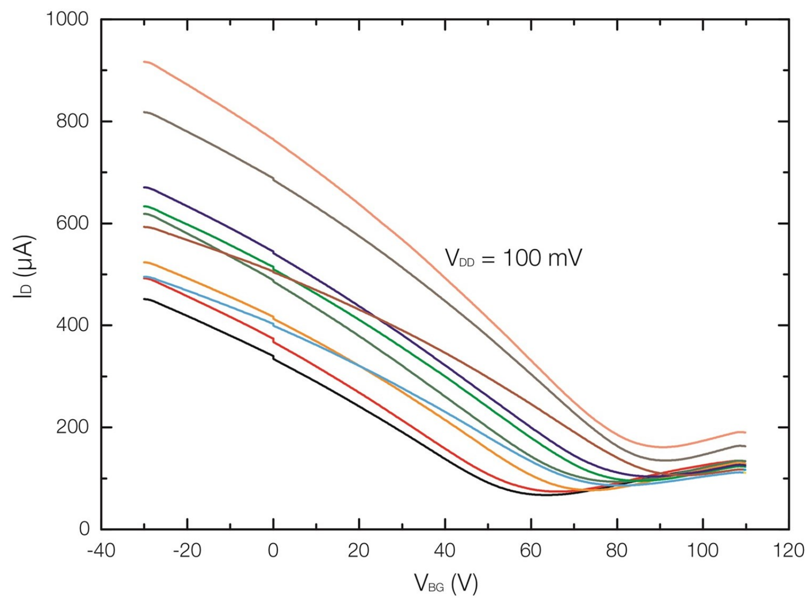
(d)

Figure 4.10: *$R - V_{BG}$ and TLM linear fit for the two "etched" structures which gave the best results in terms of contact resistance. As reported in the plots R_c of $86\,\Omega\,\mu m$ and $87\,\Omega\,\mu m$ have been obtained which so far are the lowest ever obtained for graphene contacts.*

Figure 4.11: *Contact resistance measured in case of standard gold electrodes compared to etched contacts.*



(a)



(b)

Figure 4.12: *Characteristic curves for the series of transistors which compose the TLM test structure. (a): The set of $I_D - V_{BG}$ curves measured in a standard structure. (b): The same measurements performed in etched structures.*

5 Conclusions and Future Work

In the scaling of the graphene devices the contact resistance (R_c) is the performance killer for high frequency operation. With the aim to lower R_c this work proposes both the use of pure gold electrodes, and the increase of the connection edges by etching holes in graphene below the contacts. Some remarkable results have been obtained and are summarized here:

- ⋆ A very low value of contact resistance for standard gold electrodes have been reached through the analysis and the implementation of a reliable fabrication procedure. This avoids the use of particular solvents which were able to penetrate the graphene/gold interface deteriorating the final performances of the devices. The contact resistance of gold stabilize around $250\,\Omega\,\mu m$ which is the lowest value found in literature in the case of standard contacts.

- ⋆ Through the patterning of the graphene underneath the electrodes an increase in the carrier injection is promoted. This brings the contact resistance measured at the Dirac voltage at values in the order of $90\,\Omega\,\mu m$, which are so far the lowest ever obtained for graphene-metal junctions. It is also noteworthy that the introduction of this kind of devices does not increase the complexity of the fabrication process.

While this thesis has demonstrated a very high reduction in graphene-metal contact resistance, a lot of work should be done in order to reach values of R_c comparable with (and better of) the current silicon technology. Moving toward this direction, in the next future a very interesting prospect will be the investigation of the impact of different kind of patterns etched under the electrodes with respect to that proposed here. This concerns the implementation of holes of different dimensions as well as newest shape for the etched graphene parts, which needs to be analyzed both in DC and AC.

Associated to a lowering of contact resistance, in the etched structures an increase of transconductance was found. Even though this should bring to higher operational frequency of graphene based devices, the preliminary tests reveal a negative impact on the performances of ring oscillators. Therefore it should be investigated whether this effect is related to the presence of holes in the graphene beneath the electrodes. Hence as a next step, a performance tests in real devices should be done in order to understand whether this way of decreasing the contact resistance is compatible with a technological application.

Another important aspect regards the discussed dependence of the contact resistance on the back-gate voltage. With the classical TLM the extrapolation of R_c is done through the use of the GFET total resistance taken

at the Dirac point because it represents physically the same (i.e. reference) state for all transistors. The investigation of the contact resistance behavior at different voltages is quite complicated especially for V_{BG} not far from the Dirac point where the transconductance reaches approximately its maximum value. Furthermore, in real devices a top gate configuration is preferred to a back gated one, but the interaction of the surrounding gate stack with the metal contact zone has not been taken in consideration so far.

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