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Fabrication and characterization of WSe_2 PN junctions

TESI DI LAUREA MAGISTRALE IN "NANOPHYSICS AND NANOTECHNOLOGY"

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Abstract

Transistors are the key components of microelectronic and integrated circuit (IC) technology. Their implementation as switches is the basis of digital technology. The microprocessors are the most complex ICs. The processing capability of the processors depends on the number of transistors that can be fit in the surface of the processor. For years, the main drive for lithography technology advancements has been increase in resolution. This increase in resolution allowed to pattern smaller devices, filling the area of the processors with smaller and smaller circuits. This in turn increased the processing capabilities of processors. A switch of focus for lithography based technologies is needed since transistors channels are approaching sizes for which quantum effects have become non negligible. These so called short-channel effects affect the material mainly used in electronics: silicon. To overcome quantum effects, a more radical steer away from silicon based technologies is needed.

This work focuses on the adoption of two-dimensional (2D) materials, mainly tungsten diselenide (WSe_2), a transition metal dichalcogenide (TMDC), to circumvent these effects. Being a 2D material, WSe_2 is immune to short-channel effects. WSe_2 shows important nanoelectronics properties, with the most notable one being thickness-dependent polarity of majority carriers. This property is exploited to achieve early stepping stones into verifying the possibility of employing WSe_2 as a key material for electronics. The first point of this work was fabrication of field effect transistors (FETs), to demonstrate the type of majority carriers in flakes of different thicknesses. Such devices were also useful to study Schottky barriers for different thicknesses of the material and to have an early study of current densities for both electrons and holes in WSe_2.

The flakes of WSe_2 have been subjected to polymethyl methacrylate (PMMA) spin-coating, SF_6 reactive ion etching (RIE) and metal contact deposition through patterning of PMMA masks with electron beam lithography (EBL) and deposition of metals with physical vapour deposition (PVD). The second device, and the one this work mainly focuses on, is the fabrication of PN junctions through contacting two flakes of different thickness. This contact is achieved through hot-pickup and deposition of n-type flakes on top of p-type ones. The last step which was tried, was the fabrication of a bipolar junction transistor (BJT) with the same principle of the

PN junction: hot-pickup and deposition of n-type flakes on top of p-type ones, to achieve an NPN configuration.

Key-words: WSe_2, Lithography, FET, PN, Junction, ambipolarity.

Abstract in italiano

I transistor sono il componente chiave per la microelettronica e per la tecnologia basata sui circuiti integrati. Il loro utilizzo come interruttori è alla base della tecnologia digitale. I microprocessori sono i più complessi circuiti integrati (ICs). La capacità di elaborazione dei processori dipende dal numero di transistor che riescono ad essere installati sulla superficie del processore. Per anni l'obiettivo principale degli avanzamenti nella tecnologia litografica è stato il miglioramento della risoluzione. Questo aumento della risoluzione ha permesso di stampare dispositivi di dimensioni sempre minori, permettendo l'aumento del numero dei circuiti possibili sulle superfici dei processori. Questo miglioramento ha a sua volta migliorato le capacità di elaborazione dei processori. Un cambiamento di direzione per le tecnologie basate sulla litografia si è reso necessario, perché i canali realizzabili per i transistor stanno raggiungendo dimensioni per le quali effetti quantistici non sono più trascurabili. Questi effetti definiti di corto canale, influenzano il materiale largamente utilizzato per l'elettronica: il silicio. Per superare questi effetti quantistici un allontanamento radicale dalle tecnologie a base di silicio è necessario.

Questo lavoro si concentra sulla possibilità di adottare materiali bi-dimensionali (2D), principalmente diselenato di tungsteno (WSe_2), un dicalcogenato di metallo di transizione (TMDC), per evitare questi effetti. Essendo bidimensionale, WSe_2 è immune a effetti di corto canale. WSe_2 mostra importanti proprietà per la nanoelettronica, con la più interessante che è polarità dei portatori maggioritari dipendente dallo spessore del materiale. Questa proprietà è stata sfruttata per tracciare i primi passi verso la verifica della possibilità di utilizzare WSe_2 come materiale per l'elettronica di consumo. Il primo punto di questo lavoro è la fabbricazione di transistor a effetto di campo (FET) per dimostrare la concentrazione di portatori maggioritari a diversi spessori del materiale. Questo primo dispositivo è stato utile anche per studiare l'andamento delle barriere Schottky per diversi spessori del materiale e per studiare le densità di corrente per elettroni e lacune nel WSe_2.

Il materiale è stato soggetto a spin-coating di polimetilmetacrilato (PMMA), attacco con ioni reattivi (RIE) di SF_6 e deposizione di contatti di metallo tramite stampa di pattern sulle maschere di PMMA con litografia a fascio di elettroni (EBL) e

deposizione di metalli con deposizione fisica da vapore (PVD). Il secondo dispositivo, quello su cui questo lavoro si concentra, è la fabbricazione di giunzioni PN attraverso la messa in contatto di due flake di spessore diverso. Questo contatto è raggiunto tramite hot-pickup e deposizione di flake di tipo n su flake di tipo p. L'ultimo passo in avanti tentato è la fabbricazione di un transistor a giunzione ambipolare (BJT), basandosi sullo stesso principio delle giunzioni PN: hot-pickup e deposizione di flake di tipo n su flake di tipo p, per raggiungere una configurazione NPN

Parole chiave: WSe_2, Litografia, FET, PN, giunzione, ambipolarità.

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Introduction

Transistors, mainly MOSFET, BJTs and J-FETs, have been the key component of microelectronics and integrated circuits (ICs) for years now. Their main implementations are to be used both as amplifiers and as switches. The easiest example of the last function is the formation of the depleted channel in a MOSFET: by changing the gate voltage, it is possible to let current flow between source and drain (ON state when current is flowing, while OFF if it is not). In figure i.1 the first working "point contact" transistor.

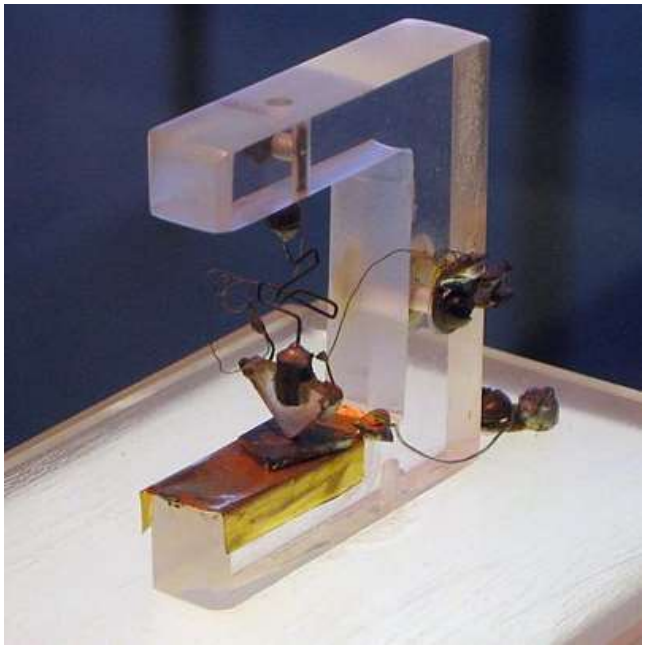


Figure i.1: First working 'point contact' transistor, 1947. Image taken from https://www.electronicsweekly.com/

Achievements in the field of fabrication technologies managed to shrink the sizes of printed patterns. This was especially useful for transistors, since, by reducing their size, it was made possible to fit more transistors in the same surface area, thus increasing processing capabilities for unit of surface area.

Transistor size reduction (which can be translated as increased processing capabilities) increased almost monotonically with the years spent on research. This behaviour was theorized into the Moore's law (which can be seen in Figure i.2), which states that the number of transistors in an IC doubles every two years. Unbelievably, it showed precise prediction of sizes of transistors that have been achieved throughout the years. Nowadays following Moore's law has proven to be difficult since dimensions of channels for devices reached the size for which quantum effects are not negligible anymore. Just focusing on improving resolution of fabrication steps to be able to print smaller patterns for devices is not a suitable strategy anymore.

This present work aspires to supply an early step toward a possible solution to overcome the so called short-channel effects.

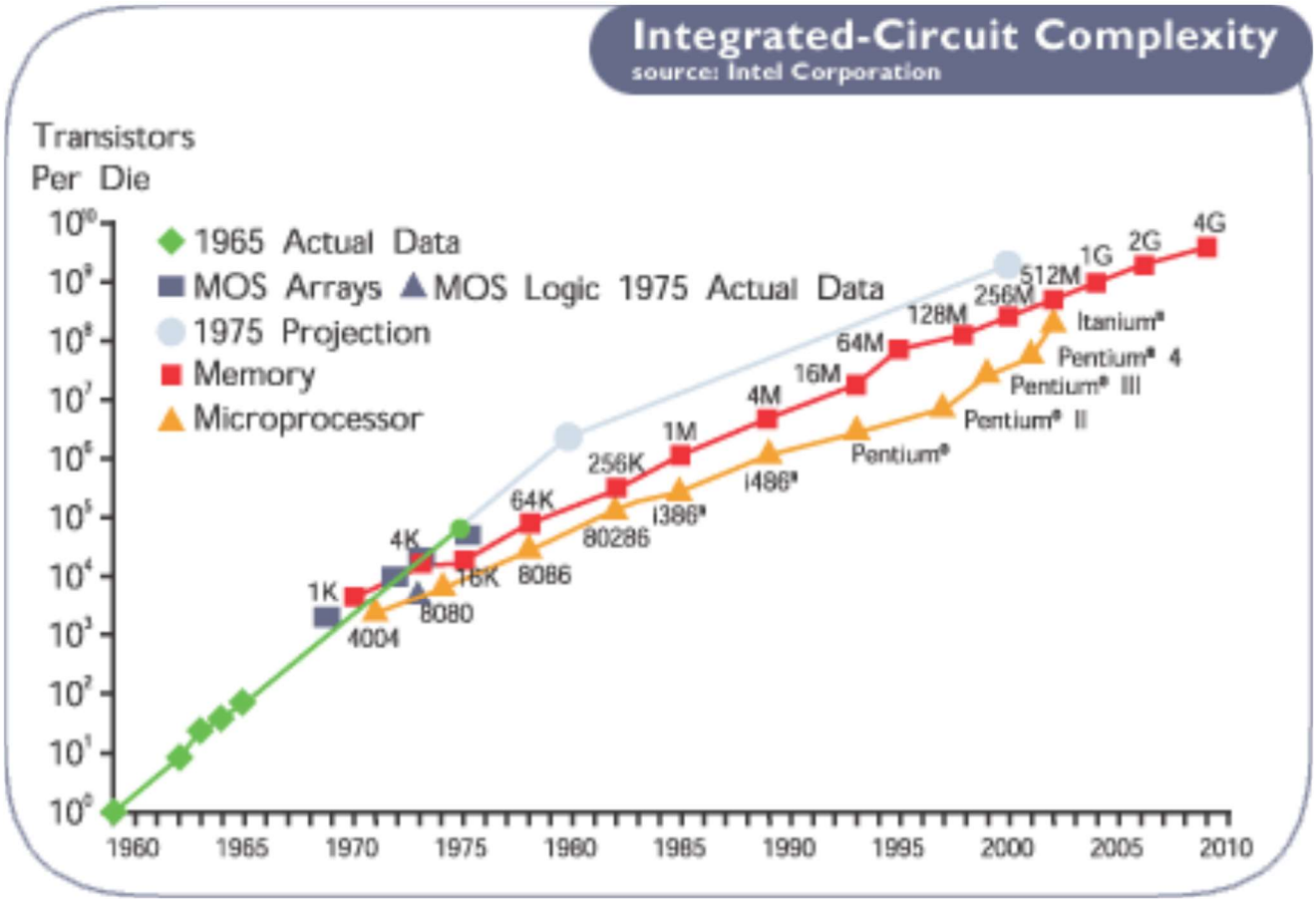


Figure i.2: Moore's law. Image taken from [12]

1 Integrated circuits overview

A small overview of state-of-the-art technologies will be given to let the reader better understand the problematic of "short-channel effects" and to give useful information to understand the direction that has been taken to overcome them.

1.1. State of the art lithography

Silicon (Si) is the mainstream material when it comes to electronic applications. The main reason is that Si is a semiconductor, which means that can act both as a conductor or as an insulator (depending on the application). Si is very abundant in nature (about 27% of the earth crust) and good quality metallurgical grade Si (98% pure) can be easily obtained by heating quartzite (sand, SiO_2) at 2000°C.[12]. A typical procedure can be seen in figure 1.1 (b). SI is also widely used in ICs because it makes an excellent oxide with nearly defect free interface.

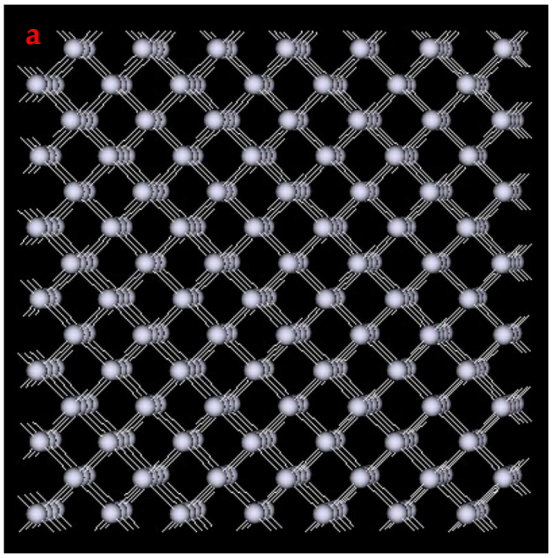
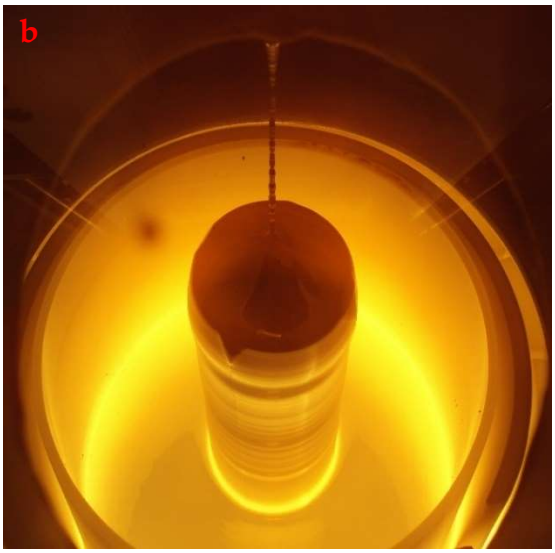


Figure 1.1 (a): Close-up view of Si <100> orientation. Image taken from [12]



(b): Metallurgical grade Si obtained by Czochralski process. Image taken from https://www.sil-tronix-st.com/

Si oxidizes in air at room temperature, but oxidation takes place at Si/SiO_2 interface. At room T, O_2 atoms do not have enough energy to diffuse through the oxide layer and continue the oxidation process after oxidizing only a small layer of Si. Native oxide is thus only 4 nm thick at room T, which is a useful property because it is self-limiting.[12] The interface between Si and SiO_2 behaves like an ideal semiconductor-insulator interface. Si electrical properties are easily altered by introducing doping. Most common ways to introduce doping are ion implantation and introduction of dopant concentration in the melt during growth methods.

The most widely used transistor, built from Si, is the MOSFET.

1.2. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

MOSFETs are widely implemented in modern technology and are a prime example of why Si is the mainstream material for integrated circuits technology. Explanation assumes NPN MOSFET. Same discussion can be performed for PNP MOSFET by reversing polarities.

An NPN MOSFET is composed of two n-type regions (Si appropriately doped with P, or any atom from group V for example) embedded in a p-type substrate (Si grown with B, or any group III atom impurities). For Si, <100> (orientation shown in Figure 1.1 (a)) p-type substrates are widely implemented because of their high resistivity (25-50 Ω/cm^{-3}) and because <100> directions have lower density of crystalline defects and have better SiO_2 properties.[12] At the interfaces between the n-type regions and the substrate there will be PN junctions (functioning of PN junction will be discussed more in detail in the 3.2 chapter) due to the different carrier concentrations and polarities in the regions. The junctions will extend mostly in the p-type region, since usually the n-type regions are more heavily doped than the p-type one.

A Metal-Oxide combination is placed on top of the p-type substrate, in between the two n-type regions. Together they act as a Metal-Oxide-Semiconductor (MOS) capacitor. The metal contact will be called “gate”, while the two n-type regions, each contacted by a metal interconnection, will be called “source”, and “drain”. The p-type substrate also is contacted and its pin will be referred to as “body”, as shown in Figure 1.2.

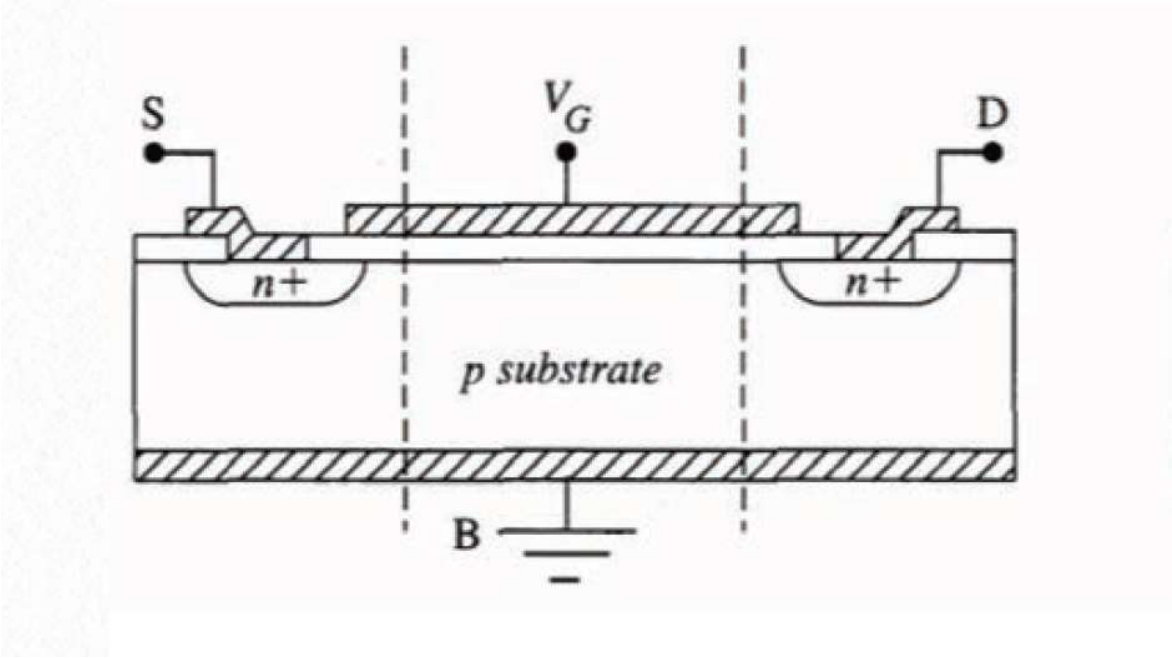


Figure 1.2: NPN MOSFET geometry. Image taken from [28]

Applying a negative potential between gate and body, the gate will be charged negatively. This negative charge will attract free holes of the p-type region, that, since they cannot overcome the oxide region, will accumulate at the oxide-semiconductor interface. This operation mode is called "accumulation regime". Charge transfer between source and drain cannot be achieved since, in between the two n-type regions, no current can flow in the p-polarized substrate. That's why MOSFETs are, usually, employed in "inversion" regime, achieved by biasing the gate with a positive potential.

Applying a positive potential the gate will charge itself with positive charge. This positive charge will repel holes from the oxide-semiconductor interface, creating a depleted region, filled only with fixed negative ionic charges. This condition is referred to as "depleted" regime of the MOS capacitor. When V_{GB} raises above a certain threshold level, free negative charges start to appear close to the oxide-semiconductor interface: below the oxide an n-type channel, where a current can flow, is created. Considering the band diagram for Si, an accumulation of positive charge on the gate creates a positive electric field from the gate metal to the semiconductor. This electric field bends downward the energetic levels of the p-type Si, so, in proximity of the oxide, they will be lower than their bulk values.

For increasing electric fields, the conduction band minimum might be bent below the Fermi level of the material, and so at room T, there will be a non negligible

electron concentration. In bulk p-type semiconductors the density of minority carriers is low and this electron channel is improbable considering only this small density of n-type carriers. Another source of n-type carriers is needed to explain the formation of this n-type channel. the source is found on thermal agitation in the semiconductor: thermal agitation breaks electron-hole couples in the semiconductor. Usually diffusion length of these carriers is small and recombination effects occur in small time windows, restoring concentrations to their bulk values. But, in presence of the gate voltage, close to the oxide-semiconductor interface, holes are repelled by the positive charge of the gate contact, so there will be no recombination with thermally generated electrons. Electron density in the channel increases exponentially with the gate voltage applied, up to a voltage value, referred to as "threshold voltage", above which the MOS enters the "inversion regime". In this regime, the density of n-type carriers close to the oxide-semiconductor interface will be comparable with the density of p-type carriers in the bulk, effectively behaving, in the channel region, as an n-type semiconductor. Schematic of the channel can be seen in Figure 1.3

The density of n-type carriers in the region is usually not as high as in the source and drain regions, which are usually identified as n+ regions.

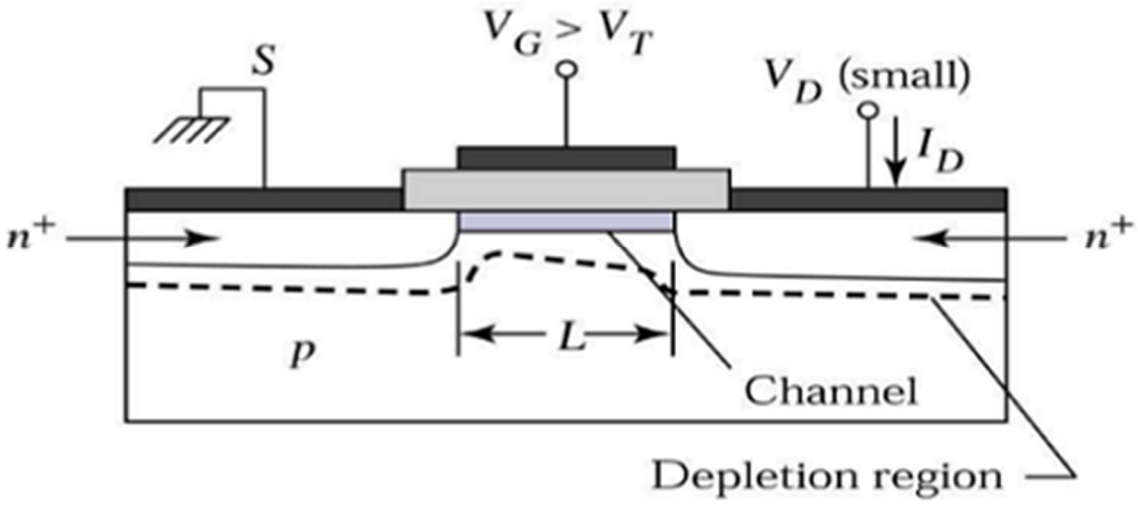


Figure 1.3: MOSFET in depletion regime with depleted regions underlined by dashed lines. Image taken from https://www.tutorialspoint.com/vlsi_design/

To summarize, for negative voltages, the MOS will enter the "accumulation" regime. On the other hand, for positive voltages lower than the threshold one, the MOS capacitor will be in the "depleted" regime, while for higher ones, it will enter the "inversion" regime.

Usually, source and body are connected and they behave as a single contact. This is the "3 terminal configuration". Its symbol is shown in figure 1.4

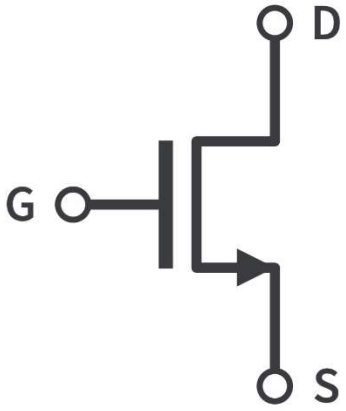


Figure 1.4: Typical symbol for 3 terminal transistor configuration.
Image taken from https://www.circuitbread.com/

If no voltage, or a negative voltage (accumulation regime), is applied to the gate, there will be no current flowing from source to drain, even if a voltage is applied between drain and source. This is due to the fact that the two junctions have opposite polarity: even though the one between source and substrate is directly polarized and current would want to flow through it, it cannot since the junction between substrate and drain is inversely polarized and so it stops the flow of current.

Applying a positive voltage to the gate pin (depletion regime), a depleted region will be formed beneath the oxide, but if this voltage is not bigger than the threshold voltage, there will be not enough n-type charge to permit flow of current between the two n-type regions. Only if the voltage between gate and source is bigger than the threshold voltage (inversion regime), a free electron channel close to the oxide-semiconductor interface will be formed. If this channel laps both n-type regions, applying a voltage between drain and source, a current will flow.

This could be easily implemented by self-aligning the implantation of P atoms to the gate oxide during fabrication. Gate voltage acts as a knob to the flow of current up to a saturation flow.

1.3. Silicon limitations

In modern technology, the possibility of scaling down dimensions is what has driven the increase in processing capabilities.

State of the art Si transistors have inversion channels of 14 nm (2014 intel). Further reducing inversion channel length, it is easy to incur into short-channel effects, which would deteriorate threshold voltage of the device.[12] If Drain-Source voltage in a transistor is too high, depletion regions for both drain and source regions grow to the point of occupying the whole channel length (as shown in Figure 1.5). Gate voltage would not be able to modulate the current flowing from drain to source since now the whole channel length would be depleted even when no gate voltage is applied permitting the current flow for any gate voltage applied.

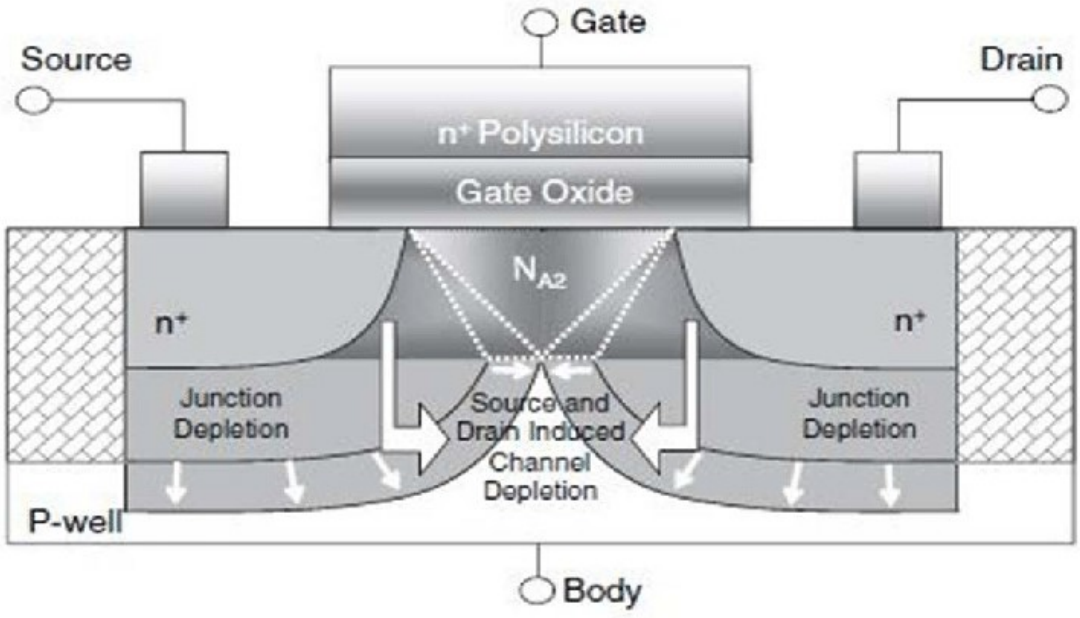


Figure 1.5: Representation of short-channel effects. Image taken from [29]

Needless to say, the lower the channel length, the smaller the amount of drain-source tension needed to reach this effect. For channel lengths smaller than 5 nm, transistor technology completely fails due to tunnelling of carriers from drain to source region. Tunnelling is incentivized by energy of the carriers, therefore heat dissipation also becomes an issue, further increasing the possible transistor channel limit length.

To further reduce transistor dimension, a more abrupt step has to be taken. The direction this work decided to take is to set its eyes upon a different material, less prone to short-channel effects. 2D materials seemed to be the most effective choice.

2 Transition Metal Dichalcogenides (TMDCs)

In 2004 Andre Geim and Konstantin Novoselov demonstrated the possibility of building Field-Effect Transistors (FETs) from flakes of graphite. Some of these FETs, which were achieved on flakes of graphite peeled off through adhesive tape, were built on single-carbon-atom thick flakes, referred to as graphene.

In 2010 they have been awarded the Nobel Prize in Physics "*for groundbreaking experiments regarding the two-dimensional material graphene*".

These experiments on a two-dimensional material drew attention to this class of materials.

However, pure graphene is conductive (as shown in Figure 2.1) and bandgaps are required for many applications in electronics.

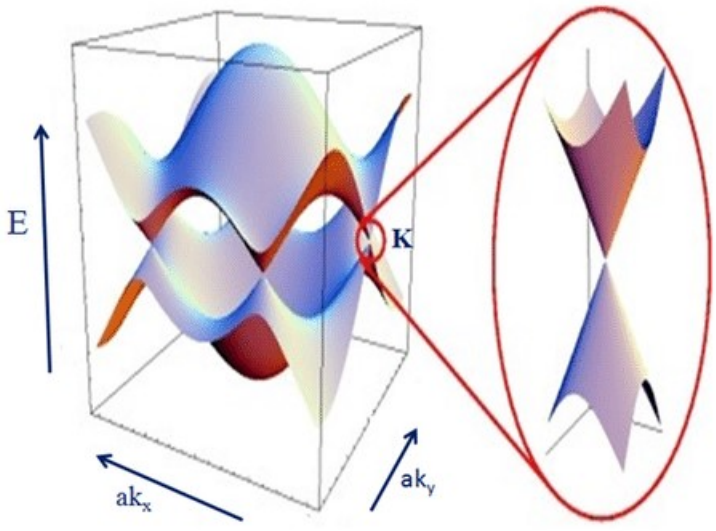


Figure 2.1: Graphene bands in reciprocal space, underlining how at K points graphene is conductive. Image taken from [13]

The ones who received most attention for their nano-electronic properties are semiconducting TMDCs.

2.1. Structure and properties of TMDCs

Transition metal dichalcogenides (TMDCs) are a group of materials formed by a six-fold coordinated transition metal M and a chalcogen X which instead is three-fold coordinated. They collect in compounds of the shape MX_2. TMDCs show a layered configuration in which single layers, of thickness of 6-7 Å, are connected through Van der Waals forces up to bulk crystal shape.[1] Van der Waals forces are weak forces that make it possible for these materials to be easily exfoliated mechanically.

A single layer of a TMDC is made up of a hexagonally packed plane of metal atoms sandwiched in between 2 planes of chalcogen atoms covalently bound to the metal itself as can be seen in Figure 2.2.

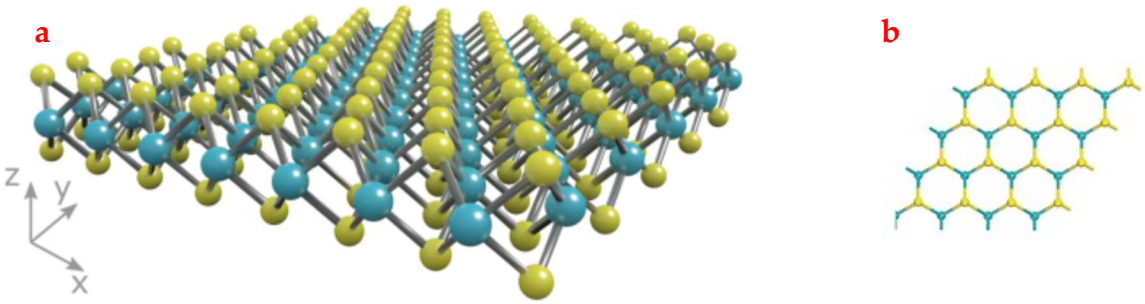


Figure 2.2 (a): 3D view of monolayer of TMDCs. Image taken from [1]

(b): Top view of monolayer TMDCs. Image taken from [1]

The most interesting TMDCs, for their nano-electronic properties, are the semiconducting ones made from W and Mo. TMDCs of these materials (MoS_2, WSe_2…) have been known since early in 20th century. For example, the structure of MoS_2 has been known since 1923, and similarly to graphite, it was used as a lubricant. Some minor "electronic" applications were already implemented in those

years: MoS_2 was used as anode for lithium-ion batteries. Needless to say, MoS_2 was not exploited to its full possibilities.

In the last twenty years, after the discovery of Graphene, a new opportunity was given to these materials. TMDCs were proven to be fully exploitable due to their wide range of properties: semiconducting monolayer TMDCs show the presence of a direct bandgap, bandgap position can be controlled by application of external stimuli (i.e strain), Strong quantum confinement brings high binding energy of excitons (which can be exploited for devices) and the breaking of spatial inversion symmetry in monolayers shows interesting applications in valley-tronics due to a strong spin-valley coupling.

The more interesting properties and the ones this work tried to focus on are: high conductivity, thickness of a single layer smaller than 1 nm (0.75 nm for WSe_2), thickness-dependent band diagram and stable layer surfaces because semiconducting TMDCs do not present dangling bonds.[2] Also, the possibility to control the number of layers in structures, through different fabrication steps, gives an additional degree of freedom in modifying the electronic properties of the material. These properties are sought after in electronic devices since they are needed to have high on/off current ratios in transistors and high ON-to-OFF current ratios in PN junctions (the two types of devices mainly fabricated in this work). Another interesting reason why TMDCs are studied throughout the last 20 years is that lithography process needed for these materials build on the same experience-base as Si. This meant that little to no further research on fabrication technology was needed. Differently from Si though, these materials are immune to "short channel" effects that undermine state of the art Si technology: the atomic thickness smaller than 1 nm suppresses the short-channel effect and renders these materials effectively immune to them. The power consumption is also reduced, which is a step in the right direction to extend the validity of Moore's Law. This property, combined with bond-free surfaces, makes the 2D group VIB TMDCs promising candidates for fabrication of high-performance FETs with reduced channel length. The reduced thickness in TMDCs confines electrons in the plane of the material. In-plane mobility, one of the key aspects to study, can be expressed as

$$\mu = \frac{e\tau}{m^*}. \tag{2.1}$$

Mobility in TMDCs depends on acoustic and optical phonon scattering. These two mechanisms have different contribution weights at different band structures, thicknesses and temperatures. At low temperatures (T < 100 K)[1], acoustic phonon scattering dominates, but at high temperatures optical phonon scattering is the key mechanism.

Theoretical values for mobilities of TMDCs are comparable to those of mainstream electronics semiconductors: Si, Ge and GaAs have theoretical electron mobilities of 1200, 3900 and 9400 ($cm^2 V^{-1} s^{-1}$), while for TMDCs electron mobilities, as calculated assuming limited by acoustic phonon scattering, are 1833, 3579, 1247/1045, 2316 ($cm^2 V^{-1} s^{-1}$) for, HfS_2, $HfSe_2$, ZrS_2, $ZrSe_2$, respectively.[1] Theoretically, TMDCs seem a good replacement to further develop Moore's law. The experimental mobility is, however, lower than the theoretical one. Carrier mobility in TMDCs is lowered by various other scattering mechanisms. Other scattering mechanisms that reduce charged carriers mobility are Coulomb scattering, which is due to charge impurities within or on top of the 2D surface of the material, and surface roughness scattering. Coulomb scattering is the main mechanism that limits carrier mobility below room temperature. Increase in the dielectric constant, of either the surrounding environment or the 2D materials, reduces the Coulombic effect. These last two mechanisms are more or less intrinsic to the material and cannot be externally influenced after fabrication.

Electrical devices, usually, need ratios between on and off currents in the range of 10^4–10^7 for transistor applications. High on/off ratios require high conductance, which is obtained through high carrier density. Usually, high carrier densities are obtained through doping; however, doping can result in a scattering component that hinders carrier mobility: carriers scatter against the ionised impurities, resulting in a decrease in the mobility. At high carrier densities, scattering is typically dominated by ionised impurities.

2.2. Tungsten Di-selenide (WSe_2)

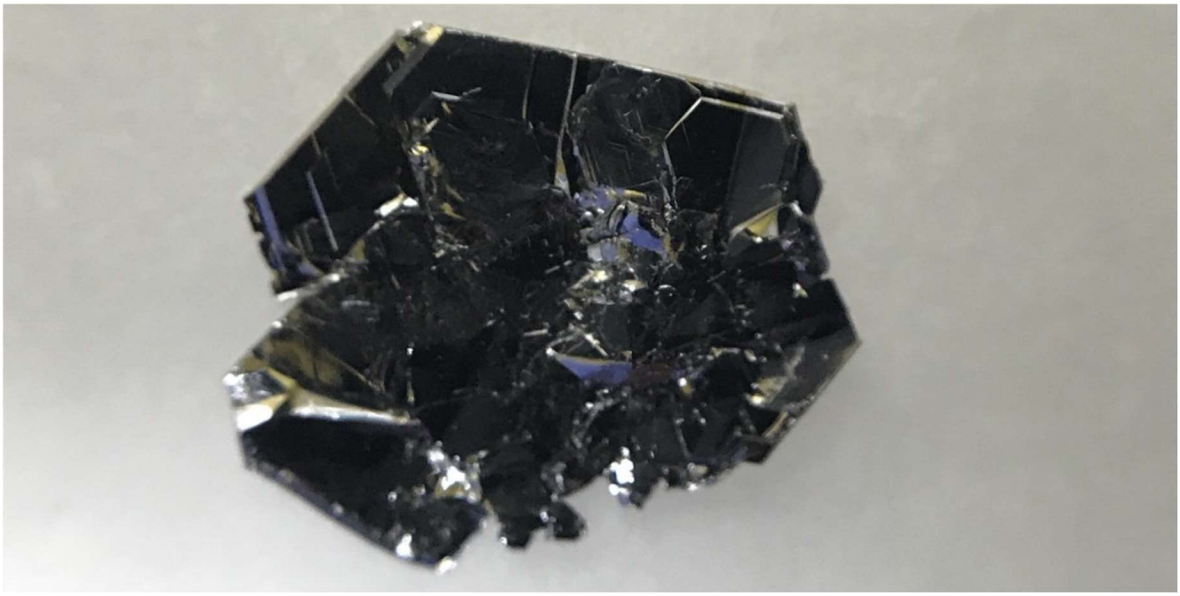


Figure 2.3: WSe_2 Crystal. Image taken from https://www.2dsemiconductors.com/

WSe_2 is a semiconducting TMDC made of two atoms of a non-metal (Se) and one metal atom (W) of the VI group presenting a trigonal prismatic geometry. The configuration is a layered one and each layer is made up of a W metal plane sandwiched in between two Se planes, to which each metal is covalently bound. Thickness of a single layer is 7,5 Å.[1]

Metal-chalcogen bond has a length of 2,526 Å, while the distance between close selenium atoms is 3,34 Å. W-W length is 3,28 Å. Neither W atoms nor Se atoms are bonded with another atom of the same class.[2]

W forms four covalent bonds with Se and, Moreover, two electron pairs, which form a dative bond, can be accepted by the metal. Since chalcogens present a sp^3 hybridization, one electron lone-pair is left on the surface.

However, this lone-pair is not involved in covalent bonds and leaves no dangling bonds on the edges of the surfaces, making the surfaces non-reactive and chemically stable. Therefore, WSe_2 shows one of the key properties that would make it a good TMDC for electronic applications.

The second key property needed for this work is high in plane mobility. WSe_2 shows lower effective electron and hole masses than other semiconducting TMDCs,

making it prime material of choice for this kind of applications. Hole mobility can theoretically reach values up to 500 $cm^2\ V^{-1}\ s^{-1}$.[1]

The last interesting property for electronic applications is thickness dependent band diagram. Bulk WSe_2 presents an indirect optical band gap of 1.35 eV, while monolayer WSe_2 transitions to a direct band gap of energy 1.62 eV.[9] Both can be seen in Figure 2.4.

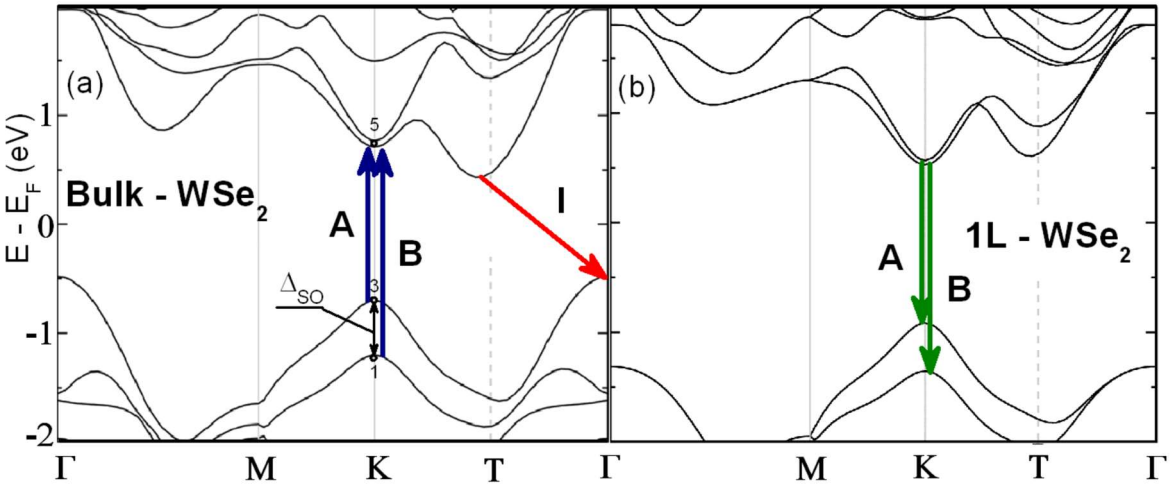


Figure 2.4: Band diagram of WSe_2 for both Bulk and monolayer configuration. Blue and Green arrows indicate direct transitions, while the red one indicates the indirect one for bulk configuration. Image taken from [9]

The conduction band minimum for bulk WSe_2 is situated at the T point, while the valence band maximum will be at Γ point. For monolayer WSe_2 both minimum of conduction band and maximum of valence band will be situated at the K point. The previous minimum and maximum points of conduction band and valence band are found at energies further away from the Fermi level of the metal when a single layer configuration is studied.

What is interesting for WSe_2 is that this material shows not only band diagram changes as a function of thickness, but also polarity has been shown to be dependent on the number of layers. Below 4 nm of thickness, WSe_2 shows majority of carriers to be holes, while for thicknesses larger than 7 nm conduction is carried out predominantly by electrons. Optical and Atomic Force Microscopy images of the flakes for both polarities can be seen in Figure 2.5. Figure 2.6 shows AFM measurement of thickness for these flakes.

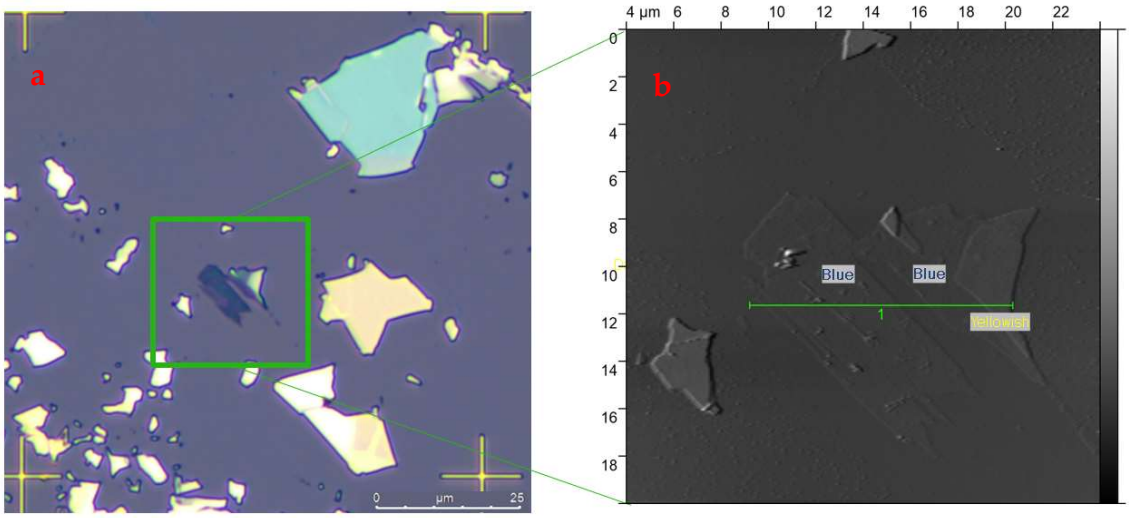


Figure 2.5 (a): Optical image of thin flake obtained by exfoliation. (b): AFM map of the same flake.

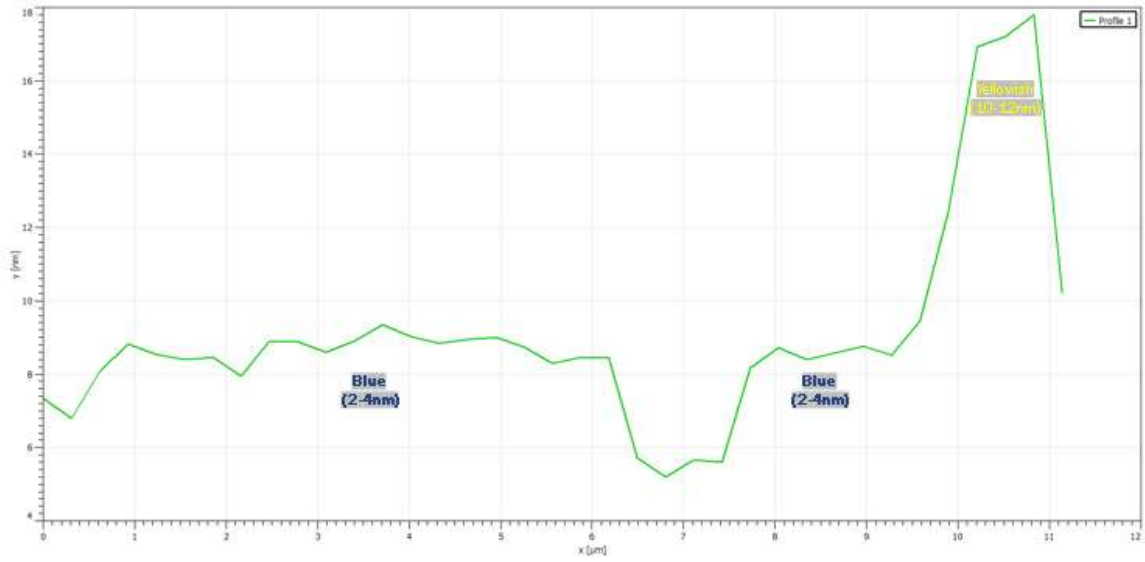


Figure 2.6: Thickness measurement performed by AFM of p-type flakes (left peaks), and a n-type one (right peak).

The region of thicknesses in between these two critical ones shows ambipolarity of carriers.

This thicknesses dependent polarization is what this work focuses on, since it opens up the possibility of building complex devices without the need of implementing heterostructures or to resort to doping by ion implantation, which would hinder the continuity of the layers of material, which would in turn hinder its conduction capabilities.

The theoretical reason behind the peculiar thickness-dependent polarity change is still under debate. three hypotheses seem to explain this phenomenon:

1. The first hypothesis focuses on the p-type carrier density for thin TMDCs materials. The p-type polarity is proposed to be due to charge transfer at the substrate/flake interface, which cannot be fully screened by an atomically thick layer of material. This charge transfer will result in electron depletion in WSe_2, resulting in a p-doping from the substrate to monolayer (or even few-layers) material.
   The reason why this p-type charge injection from the substrate does not play a relevant role in multilayer configurations is because the increasing number of layers yields an increasing interlayer coupling interaction, effectively screening the charge transfer at the interface between WSe_2 and substrate.
   This theory was formulated by Hao, Kou et Al. in "*Electrostatic properties of two-dimensional WSe_2 nanostructures*".[3]
   To demonstrate their claims, the effective surface potential difference has been measured of WSe_2 flakes of increasing thicknesses. The measurements have been performed employing Kelvin probe force microscopy.
   The measurements show how surface potential difference decreases with increasing thicknesses, which indicates that screening effect is higher for thicker flakes. The surface potential for monolayer flakes was measured to approximately 35 mV. Surface potential difference is an effective measuring parameter since it shows strong contrast between layers of different thicknesses: Tri-layer of WSe_2 show surface potential 40 mV higher than monolayer flake. Surface potential behaviour for different thicknesses can be measured and thickness-dependence can be obtained.
   For WSe_2 surface potential increases monotonically with thickness and approaches bulk values for 7 or more layers of WSe_2. Thickness dependence is shown in Figure 2.7
   Contributions deriving from defects or charge impurities can be neglected since surface potential measurements show high uniformity over the WSe_2 surfaces, especially for monolayer ones, where values ranged in an interval of 10 mV.

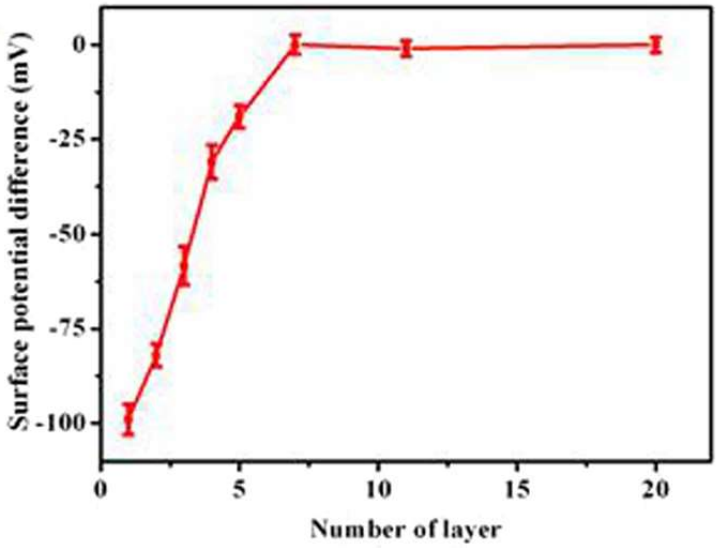


Figure 2.7: Surface potential difference measurement as a function of the thickness of the material performed by Hao, Kou et Al. Image taken from [3]

A model that further verifies this theory was proposed by Wang, Li et Al. and exposed in "*The ambipolar transport behaviour of WSe_2 transistors and its analogue circuits*".[4]

During their work, they measured electric field screening from WSe_2 flakes for thicknesses ranging from 1 to 40 layers through electrostatic force microscopy and the results have been interpreted with Thomas-Fermi theory to model the thickness behaviour of the screening field. two different models have been implemented. In the first model, referred to as "2D model", interlayer coupling interaction is excluded, while for the second model, called "3D model", it is taken into account.

According to their models and fittings, screening effect measurements follow 2D model fitting for thicknesses smaller than 3 layers of WSe_2. For thicknesses higher than those, the 3D model is more suited, as can be seen in Figure 2.8.

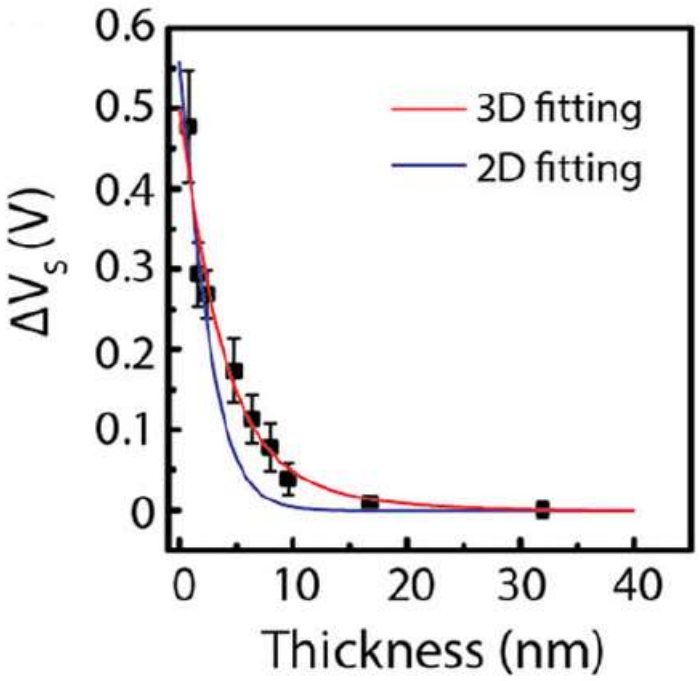


Figure 2.8: Surface potential dependence on thickness of material with 2D and 3D fittings using non-linear Thomas-Fermi theory. Results achieved by Wang, Li et Al. Image taken from [4]

These models suggest that a weak interlayer coupling interaction occurs at lower thicknesses, while it becomes strong for thicknesses higher than critical ambipolar ones.

2. A second theory correlates the carrier density difference, measured between flakes of different thicknesses, to the evolution of electronic mobility as a function of thickness.
   This theory has been demonstrated by Ji Heon Kim, Tae Ho Kim, Hyunjea Lee, et al. in their paper "*Thickness-dependent electron mobility of single and few-layer MoS_2 thin-film transistors*".[5] In their work, carried out on MoS_2 and generalized to semiconducting TMDCs, bottom-gate MoS_2 transistors were fabricated on flakes of different thicknesses. The channel length has been kept constant not to influence carrier mobility.
   MoS_2 shows n-type polarity even for monolayer configurations and Au contacts were fabricated to measure it.

Au is metal that shows ambipolar behaviour when measuring current flows (Schottky barrier with MoS_2 and WSe_2 are not detrimental for both n-type and p-type conduction).
From I-V transfer curves, the effective mobility can be calculated (assuming this device configuration equivalent to the MOSFET standard model).
For average values of calculated mobilities, it can be seen that μ_{eff} increases with the number of layers of MoS_2 constituting the channel. This behaviour is shown in Figure 2.9.

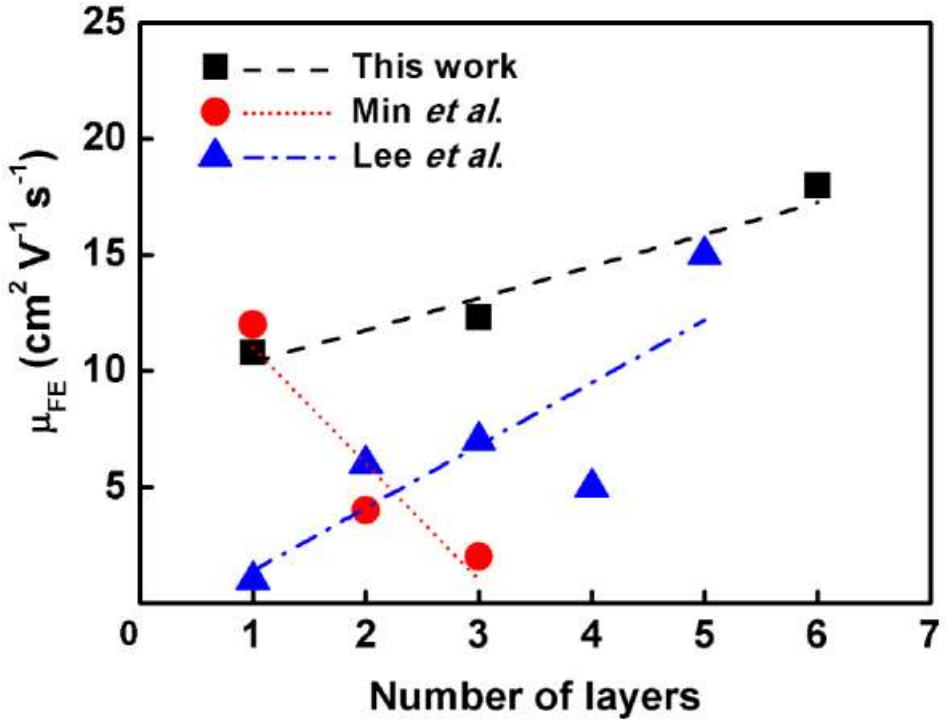


Figure 2.9: Field-effect effective mobility as a function of number of layers of MoS_2, as obtained by Ji Heon Kim, Tae Ho Kim, Hyunjea Lee, et al. The red curve is explained by increased inter-layer scattering of electrons with increasing thickness. Image taken from [5]

The increase of mobility with thickness was correlated to a decrease of contact resistance measured for thicker MoS_2 flakes. This is due to a decrease of charge screening and Coulomb impurity scattering mechanisms and can be demonstrated through simulations: mobility increases regardless of metal contacts.

This decrease of scattering mechanism events is usually associated to deposition of high-k dielectrics due to the so-called "dielectric capping effect". In MoS_2 a similar effect occurs: if subthreshold swings are measured, without modifying any other experimental parameter, they can be related to the dielectric constant of the semiconductor.
Subthreshold swings are given by:

$$SS = \ln(10)\left(\frac{k_B T}{q}\right)\left\{1 + \frac{d_{ox}\left[\left(\frac{q\epsilon_s N}{2\Phi_s}\right)^{\frac{1}{2}} + qD_{it}\right]}{\epsilon_{ox}}\right\}, \qquad (2.2)$$

Where k_B, T, q, d_{ox}, ϵ_s, N, Φ_s, D_{it} and ϵ_{ox} are respectively, Boltzmann constant, Temperature, charge, thickness of gate dielectric, dielectric constant of semiconductor, doping density, band bending, interface trap density and dielectric constant of the oxide insulator.
Subthreshold swings increase with material thickness, which means that the dielectric constant of MoS_2 does too.
These combined 2 effects (reduced contact resistance and increase dielectric constant of MoS_2 due to dielectric capping effect of additional MoS_2 layers) result in the increased electron mobility for thicker flakes of TMDCs.
In this experimental demonstrations MoS_2 has been employed instead of WSe_2, but the discussion can be generalized considering that MoS_2 monolayers have n-type polarity. If also hole mobility increased with thickness, remembering that Au contacts permit ambipolar current flow, a p-type contribution should be seen in transfer curves. Since it is not the case, hole mobility can be assumed to change in a neglectable way with flake thickness.

3. The third theory was proposed by Rani, Dicamillo et Al. in "*Tuning the Polarity of $MoTe_2$ FETs by Varying the Channel Thickness for Gas-Sensing Applications*".[6]
   The key point of their work was correlating the switching of polarity, by thinning TMDC FETs, to an increase of the importance of surface states. These surface state can be thought influencing carrier density in thin layers by modulating the Schottky barrier height at the metal-semiconductor interface.

This modulation increases contact resistance for n-type conduction for known n-type metals, thus forcing a p-type favoured current flow. This characteristic can be further underlined by employing high work function metals like Pt, for which p-type carrier will feel a lower contact resistance.
P-type polarity is thus measured only because high work function metals are the only ones for which significant currents can be measured.

3 Device theory

Theory behind the devices this work focused on will be given to help the reader understand process flow, measurements characterization and results. First a Field Effect Transistor in accumulation regime will be explained. Secondly the theory behind the PN junctions will be given. Lastly the theory of the Bipolar Junction Transistor will be explained.

3.1. Accumulation Field effect transistor (FET)

The key property of WSe_2, onto which this work is focused, is the thickness-dependent carrier concentration. To demonstrate density of carriers for samples both of thickness bigger and smaller of the ambipolarity region, Accumulation Field Effect Transistors (FETs) geometry is implemented. Assuming a back-gating configuration, the semiconducting material is deposited onto an insulating substrate (typically an oxide such as SiO_2), which is gated by a metal contact beneath it, to implement an MOS structure. Metal contacts are then deposited onto the material (it being either n or p-type) that will be referred to as "source" and "drain" (equivalently since the structure is symmetric). A schematic of the FET configuration can be seen in figure 3.1.

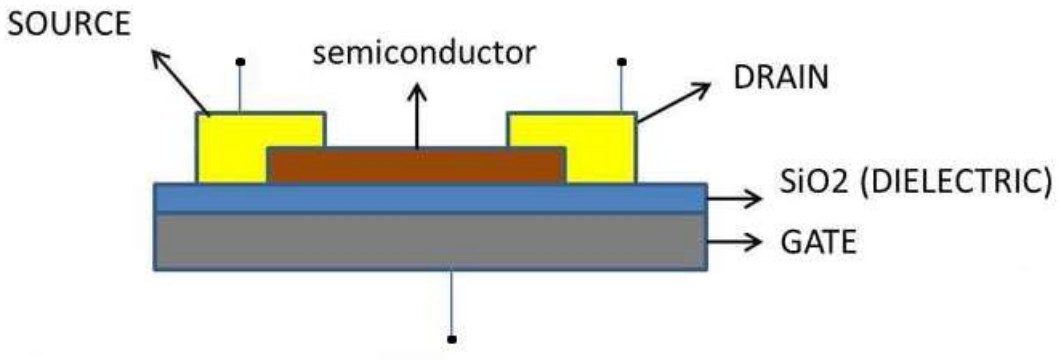


Figure 3.1: Schematic of FET configuration. Image taken from https://www.physicsforums.com/

To measure n-type (p-type) conduction a voltage is applied between gate and source. If the voltage is positive (negative), conduction (valence) band is bent downward (upward) by this positive (negative) potential.

If the applied voltage is enough to have the conduction (valence) band cross the Fermi level, which is closer to the conduction (valence) band, due to the density of carriers in the material, an excess of electrons (holes) will be present attracted by the gate positive (negative) voltage. This voltage is referred to as "threshold" voltage of the FET. This excess of majority carriers comes from thermal agitation which breaks electron-hole couples. Excess electrons (holes), from thermal agitation, will be attracted by the gating voltage, while excess holes (electrons) will be repelled by it, thus no recombination occurs. This excess of charge makes the conduction band semi filled and the semiconducting material starts to behave as a conductor. If now positive (negative) potential is applied between the drain and source contacts, a current will flow. This configuration is useful to demonstrate if the material has high ratio of majority over minority carrier concentration, since, plotting I_{DS} as a function of V_{GS}, in only one of the quadrants the current will be significantly different from negligible noise contribution. If the current is different from negligible in more than one quadrant, then the material will be ambipolar. Both n, p and ambipolar conditions can be experimentally proven for WSe_2 since all three conditions are achieved with different thicknesses of the material, without the need for doping. An example of ambipolare transfer curve can be seen in Figure 3.2.

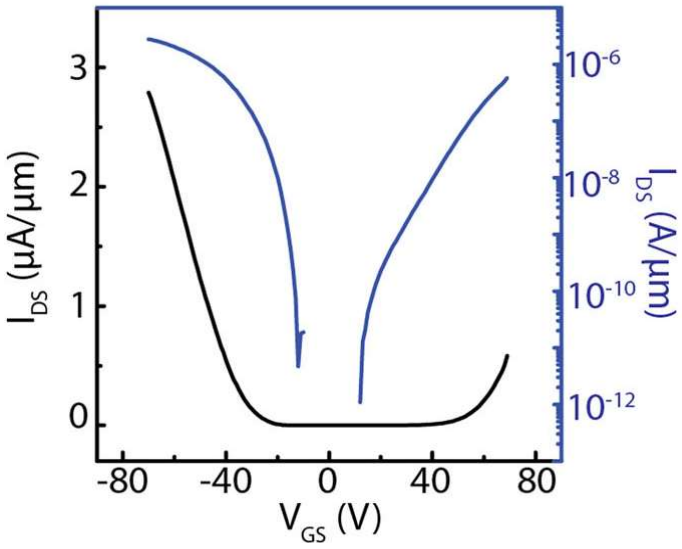


Figure 3.2: Example of ambipolar transfer curve. Current is significantly different from noise contribution for $V_{GS} < 0$ (indicating presence of p-type carriers) and for $V_{GS} > 0$ (indicating presence of n-type carriers). In blue the same curve is expressed in a logarithmic time scale to better understand threshold voltages for n and p-type conduction (where the curve shows vertical tangent). Image taken from [4]

3.2. PN junction

The PN junction is a device obtained by putting in contact a semiconducting region with majority of p-type carriers with one with majority of n-type ones. At the interface between the n-type and the p-type there would be a region where, as soon as they are put in contact, the difference in concentration of carriers in the two regions (excess of p-type carriers in the p-type region and vice versa) would give rise to diffusion currents: Excess electrons majority carriers would diffuse toward the region where they are minority carriers instead (holes toward n-type and electrons toward p-type). Fixed ions will be left at the interface regions by the moving free carriers.

An equivalent way of viewing the diffusion of majority carriers into regions of opposite polarity is that at the interface fermi level of the two materials would be unbalanced. This unbalance, called "built-in" potential, is resolved through motion of intrinsic carriers from one region to the other: excess electrons would move from the n-type to the p-type and vice versa for holes. These diffusing carriers would then recombine in the opposite semiconductor with opposite charges. Due to the charge unbalance of fixed ions in the p-type region and in the n-type region (negatively charged and positively charged respectfully) an electric field builds up that opposes the free charge diffusion through the junction. The region throughout which the electric field is present is called depletion layer or space charge region, since free carriers will not be present anymore. A schematic of depleted region, charge build up at the junction, electric field opposing diffusion and built in potential can be seen in Figure 3.3.

Applying an external positive bias to the p-type contact, free carriers in both regions would be pushed toward the junction, neutralizing the depletion layer, thus reducing its width. The total potential between p and n side decreases or can even change its own sign. Increasing the forward-bias voltage, the space charge zone can become so thin that the electric field in it cannot counter act the free carrier diffusion across the junction, thus resulting in a lower electrical resistance. The voltage for which this low resistance is achieved is called "threshold" voltage of the junction. The number of carriers diffusing up to the neutral zones determines the current that can flow through the diode. Current in a PN junction is thus given by:

$$i = I_S\left(e^{\frac{v}{V_t}} - 1\right), \tag{3.1}$$

With V_t called thermal voltage, I_s inverse saturation current and v, the applied voltage (positive from n to p region).

Free carriers, after having crossed the junction, become minority carriers, which means that they cannot continue to travel through macroscopic semiconductor regions, because it is energetically favourable for them to recombine with majority carriers. The average diffusion length is of the order of few micrometers.

If a reverse bias is applied instead, obtained by connecting the p-type pin to ground and applying a positive potential to the n-type one, very little current flows through

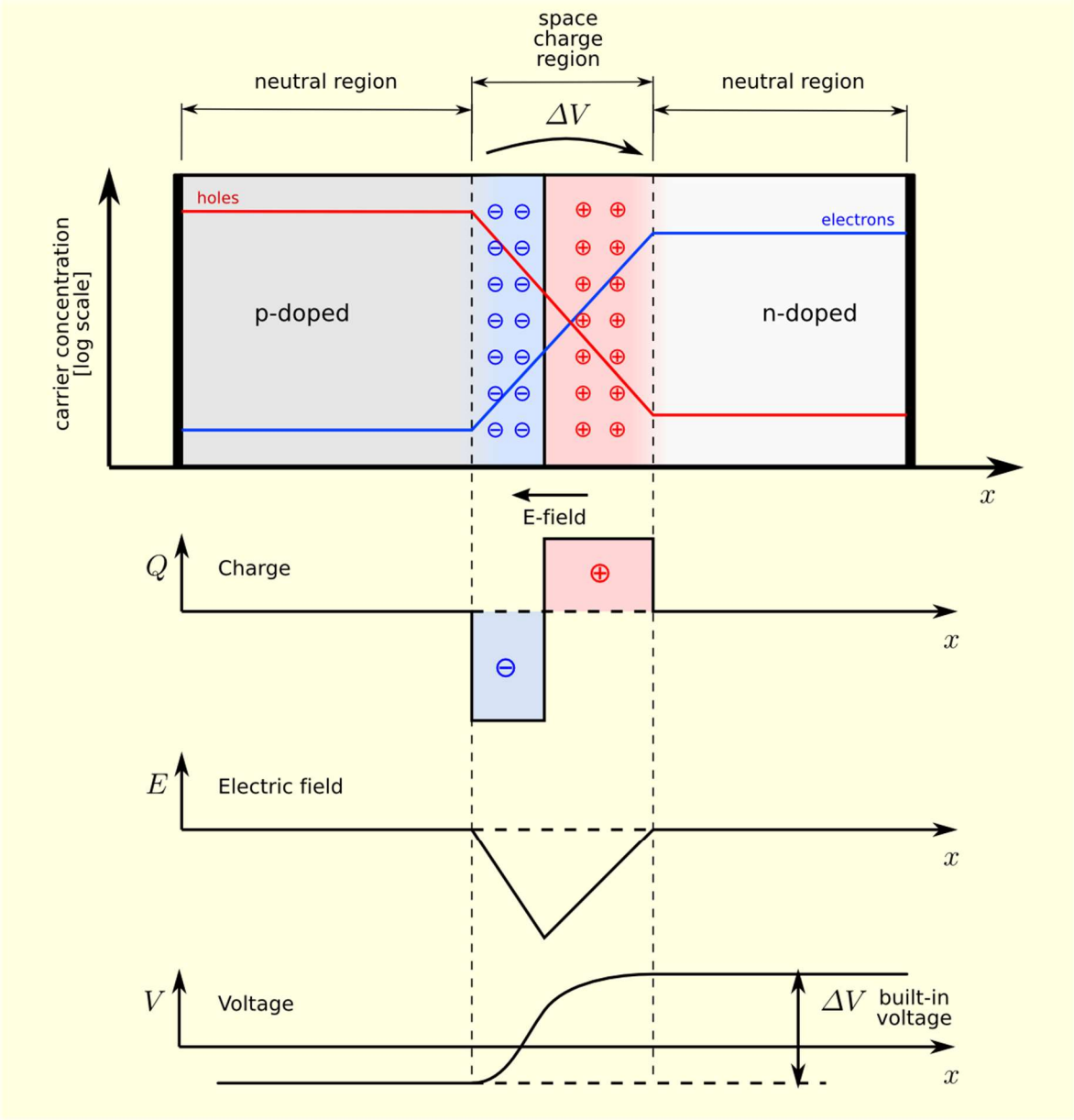


Figure 3.3: Schematic of PN junction, with focus on fixed ion charge, electric field build-up due to counter diffusion and built-in voltage between the two semiconductor regions. Image taken from https://en.wikipedia.org/

the junction. This is due to the fact that in this configuration free carriers are attracted away from the junction region toward the contacts.

Still fixed ions remain in the junction region and a depleted zone is not only present, but it increases in width since more free carriers are pulled away from the junction region. A higher voltage barrier is therefore present at the interface between the two semiconductors and thus the electrical resistance will be higher. The increase in resistance across the junction results in a much lower current through the junction and the interface behaves as an insulator.

Once the voltage across the junction reaches critical levels, the PN junction depletion zone breaks down and current begins to flow, usually by tunnelling through the high voltage barrier or avalanche mechanisms which give rise to high density of carriers to overcome the barrier. Current in forward bias, reverse bias and breakdown regions can be seen inFigure 3.4.

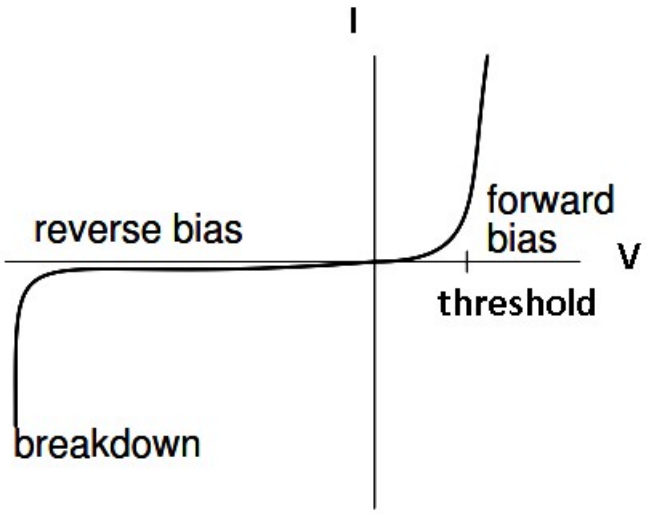


Figure 3.4: Output characteristic of a PN junction, underlining direct current, reverse current and breakdown region. Image taken from https://www.allaboutcircuits.com/

3.3. Bipolar Junction Transistor (BJT)

The Bipolar Junction Transistor is an ambitious further step that was tried during the last months of fabrication, to validate the research on junctions for transistor applications. This is however still a work in progress and not many results were reached during this thesis work.

3.3.1. Operating regimes of the BJT

A BJT consists of three differently doped semiconductor regions: the emitter region, the base region and the collector region. These regions are, respectively, p-type, n-type and p-type in a PNP transistor, and n-type, p-type and n-type in an NPN transistor (the focus of this work).

The first n-type region is contacted to a terminal known as emitter (E), the p-type one is referred to as base (B) and the last n-type region is called collector (C). In the most common applications, a current flows from collector to emitter and it is modulated by the voltage between base and emitter. A BJT is essentially composed by two PN junctions with the p-type region in common. Junctions highlighted in Figure 3.5 for clarity.

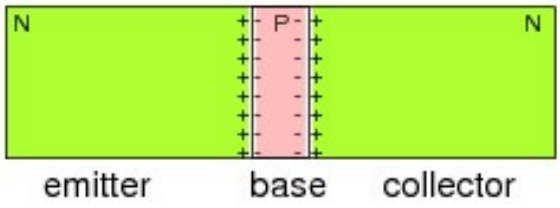


Figure 3.5: BJT schematic underlining PN junctions formation. Image taken from http://transistorcircuits.blogspot.com/

Each junction can be both directly or inversely polarized; four operating regimes can be defined in a BJT:

1. **Forward-active**: junction between base and emitter is directly polarized ($V_{BE} > V_{th}$), while the junction between base and collector is inversely polarized ($V_{BC} < V_{th}$). (Current flowing into collector, into base and from the emitter will be defined positive as an assumption).
   Since the BC junction is inversely polarized, while the BE is directly polarized, current flowing into the base will only flow toward the emitter. Also, a direct current I_t (transport current) could flow from the collector toward the emitter, through the base. Electrons injected from emitter to the base (junction directly polarized), which will be minority charges in the base (p-type region), will be pushed toward the collector n-type region by the electric field in the inversely polarized junction.
   Due to this inversely polarized junction all electrons will reach the collector region, thus leaving no electron concentration at the interface between the base region and the depleted zone between base and emitter.

The transport current I_t will be due to the gradient of these minority carriers throughout the base.
The base current is not the whole current density flowing through the directly polarized junction because some electrons from the emitter will recombine with majority carriers in the base region. This recombination current is compensated by thermal generation of electron-hole couples near the base terminal (electron will be pushed toward the metal contact by the negative charge of the base and the holes will feel attracted by it, compensating the holes lost to recombination mechanisms). This effect can be equivalently thought of as some electrons from the I_t would be collected at the base terminal, instead of reaching the collector contact. This way we can connect the collector current (I_t) and the base current (I_b) through a linear reaction that shows a gain β_F, which depends directly on the diffusion length of electrons in the base (quadratically) and it is inversely proportional to the base length W.

2. **Reverse-active**: opposite of the previous regime; BE junction polarized inversely and BC directly polarized. For symmetry considerations, it is reasonable to imagine that the behaviour of this regime will be the same as the previous one, but with current flowing from Emitter to Collector. The gain β_R will be different from β_F due to the different dopings of the 2 regions (emitter region is usually fabricated to be more doped than the collector one). Usually $\beta_R < \beta_F$. For this reason, BJTs are seldom used in reverse-active regime.
3. **Cut-Off**: both junctions are inversely polarized, so no current flows through either of the junctions. Therefore, no current will be present in the base. This configuration corresponds to a logical "OFF", or an open switch.
4. **Saturation**: both junctions are directly polarized, and current flowing is facilitated from the collector toward the emitter. This configuration corresponds to a logical "ON", or a closed switch.

3.3.2. Output characteristic of a BJT

The collector current I_C measured as a function of the potential V_{CE} is normally referred to as "output characteristic of a BJT". For small values of V_{CE}, the BJT will be in saturation regime and the current I_C will increase rapidly with increasing values of V_{CE}. The BJT will move to the forward-active regime for higher values of V_{CE} and I_C will then reach a stable point at a certain value of V_{CE} and then the current will remain constant if V_{CE} is increased. The voltage at which there is the switch from saturation to forward-active regime is not always the same and depends on the value of the current for which there is stabilization. Usually, the higher this

value of current, the higher the voltage for which there is the switch to forward-active regime. Collector current In the 4 regimes is highlighted infigure 3.6.

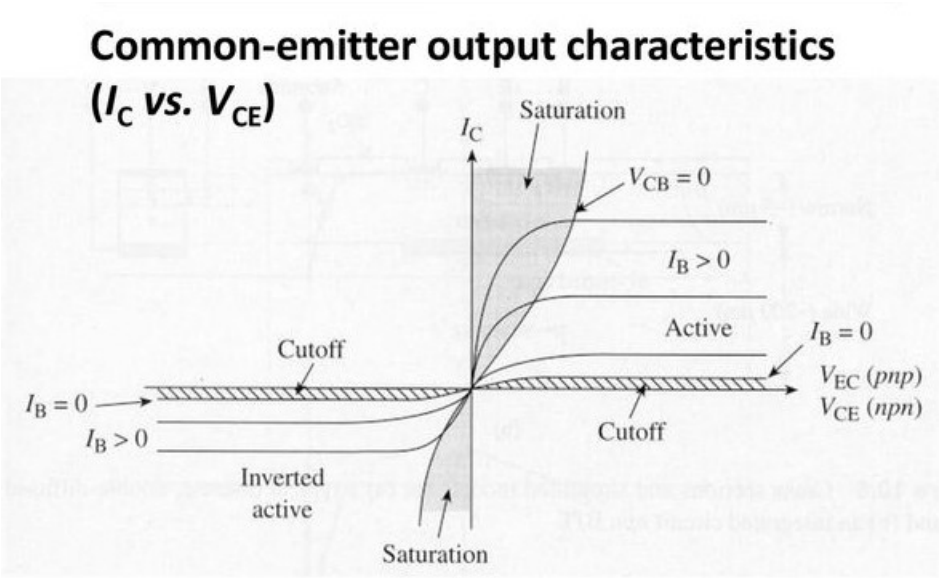


Figure 3.6: Output characteristic of a BJT, with highlighted operating regions. Image taken from https://inst.eecs.berkeley.edu/

4 Process flow of devices

Process flow of devices to give the reader an understanding of how similar devices are fabricated.

4.1. WSe_2 FET process flow

Material is exfoliated from the crystal in two different ways:

1. to achieve higher yield of thick flakes (thickness above 7 nm), a blue tape exfoliation is implemented. In this exfoliation a portion of adhesive tape is deposited onto crystal flake, shaving off a portion of it, by simply stripping away the tape. This portion is exfoliated further to achieve a thickness of 9-10 nm (normally the exfoliation process is repeated 10-15 times to achieve this desired thickness). This thickness is sought after since it showed a higher density of n-type carriers (which was identified by measuring a higher density of n-type current). Example of n-type flake achieved with blue tape exfoliation is present in Figure 4.1.

2. To obtain large thin flakes (areas of 0.5 μm^2), Au exfoliation is needed. During this process, after exfoliating with blue tape 9-14 times, a further exfoliation is implemented by evaporating on the flakes a thin layer of gold (PVD deposition). Gold lamination is essential to achieve thinner flakes since the strength of bonds between Au atoms and WSe_2 flakes makes it so that the attraction is strong enough to exfoliate only 1-3 layers (total thickness below 4 nm) and it is also uniform up to the point of not applying enough stress to cause cracks in the material. The result is large and continuous p-type flakes. The gold layer is then removed through rinsing in Au etchant for a minute and washing the sample in water and isopropanol afterwards (to remove Au etchant residues). Au etchant is completely harmless toward flakes, and so it is necessary since Au atoms might dope the material in an unwanted way.

Example of p-type flake achieved with Au lamination is presented in Figure 4.2.

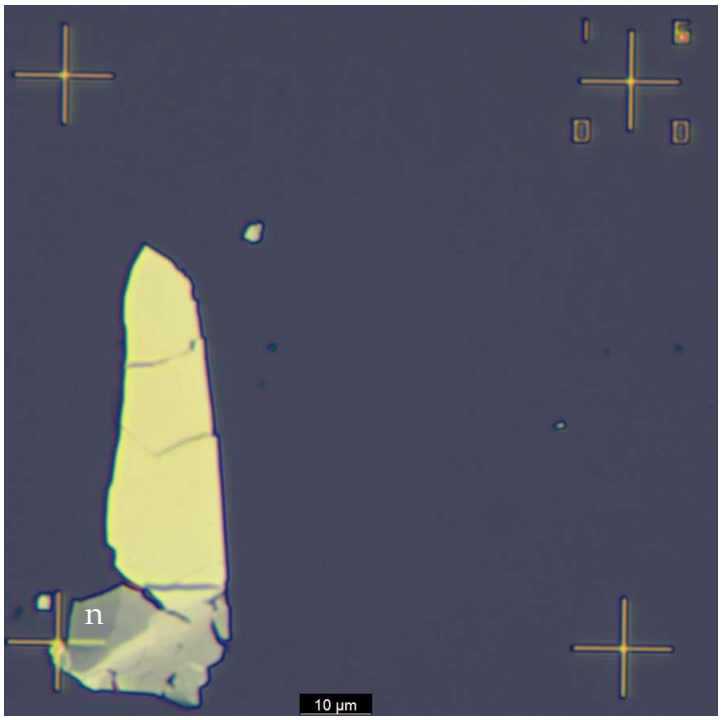


Figure 4.1: Example of n-type flake obtained through blue tape exfoliation. Grey contrast flake showed strong n-type behaviour. AFM measurements showed thickness around 10 nm.

two layers of polymer are then spin-coated onto the sample (LO1 and LO2 usually for one minute each at 6500 [explained better in the appendix]), and the sample is baked to strengthen the bonds in the polymer (one baking for each coating) and make it strong enough to act as a mask for subsequent physical processes (like etching or evaporations). Contacts are patterned through electron beam lithography and developed in a solution of 4-Methil-2-Pentanone and isopropanol (1:3) for a minute and a half. Developing is stopped by rinsing the sample in pure isopropanol for one minute (to avoid over developing the structures). This solution develops only the parts of the resist that reacted with electrons, leaving unexposed portions of the resist intact.

A marking grid is then evaporated (5 nm of Ti that act as adhesion layer followed by 45 nm of Au). Marking grids are useful to navigate around the sample and to easily locate the suitable flakes and not to have to search them every time. After having found the desired flakes, two layers of etching polymer are spin-coated to print and develop patterns to etch undesired flakes. This step is useful to remove

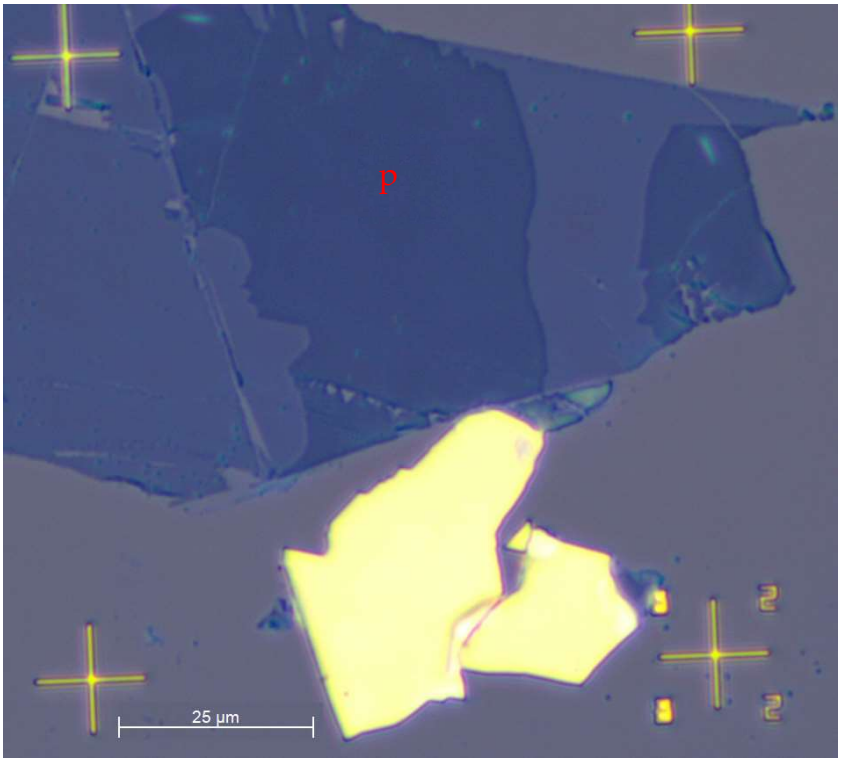


Figure 4.2: Example of thin flake obtained with Au exfoliation. Blue contrast showed p-type behaviour. Through AFM this contrast was measured to be around 1-3 nm.

flakes that could short-circuit contacts that will be printed (p-type flake after etching is showed in Figure 4.3.).The final exposure step is to pattern contacts. The chosen polymer mask consists of two layers, one of LO1 and one of LO2. Contacts, usually of 100 nm width, are exposed, developed and deposited onto the sample.

One of the key properties that were needed for TMDCs was that the surfaces of the layer had to be non-reactive and stable. When it comes to metal contacts, this property is detrimental since there will be no chemical reaction between the metal and the semiconductor. This is the reason behind the high Schottky barriers between metal and semiconductor that bring a low injection of current from the contacts to the material. These characteristics are summarized in the contact resistance contribution. High contact resistance in TMDCs is the limiting factor in TMDCs-based devices.

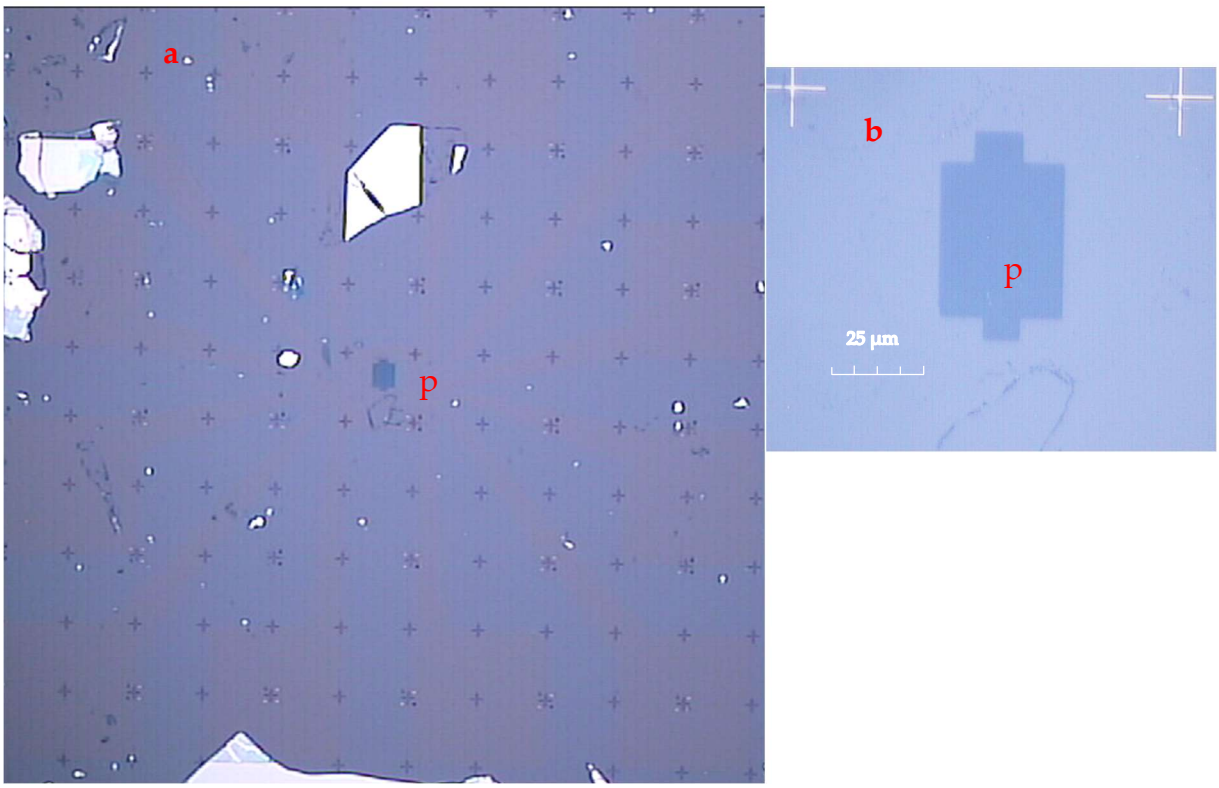


Figure 4.3(a): Through RIE undesired flakes are removed in the regions where the contacts will be patterned. In the same step the sample will be shaped to behave as designed. Etch dopes p-type region, increasing p-type density of carriers.

(b): Close-up-view of the thin flake after etching.

Interfacial Schottky barrier is reduced by choosing different metals for contacts to connect each region (n-type and p-type). P-type materials show a reduction of contact resistance when they are contacted with high work function metals. Vice versa, for n-type flakes, low work function metals show lower contact resistance. For p-type contacts Pt has been chosen, while for n-type flakes Au has been the metal of choice. Au shows low doping of this materials and it has ambipolar connection, making it not too detrimental for both n-type and p-type flakes. Pt, due to its high work-function ($\Phi_M \approx 6.0$ eV), places its Fermi level below the valence band of WSe_2 ($\chi_{WSe_2} \approx 5.5$ eV). This band alignment is expected to result in an ohmic p-type contact.

For n-type flakes the best metal to achieve low contact resistance would have been Ag, but, as experimentally demonstrated, Ag oxidizes quickly, and its oxide is not

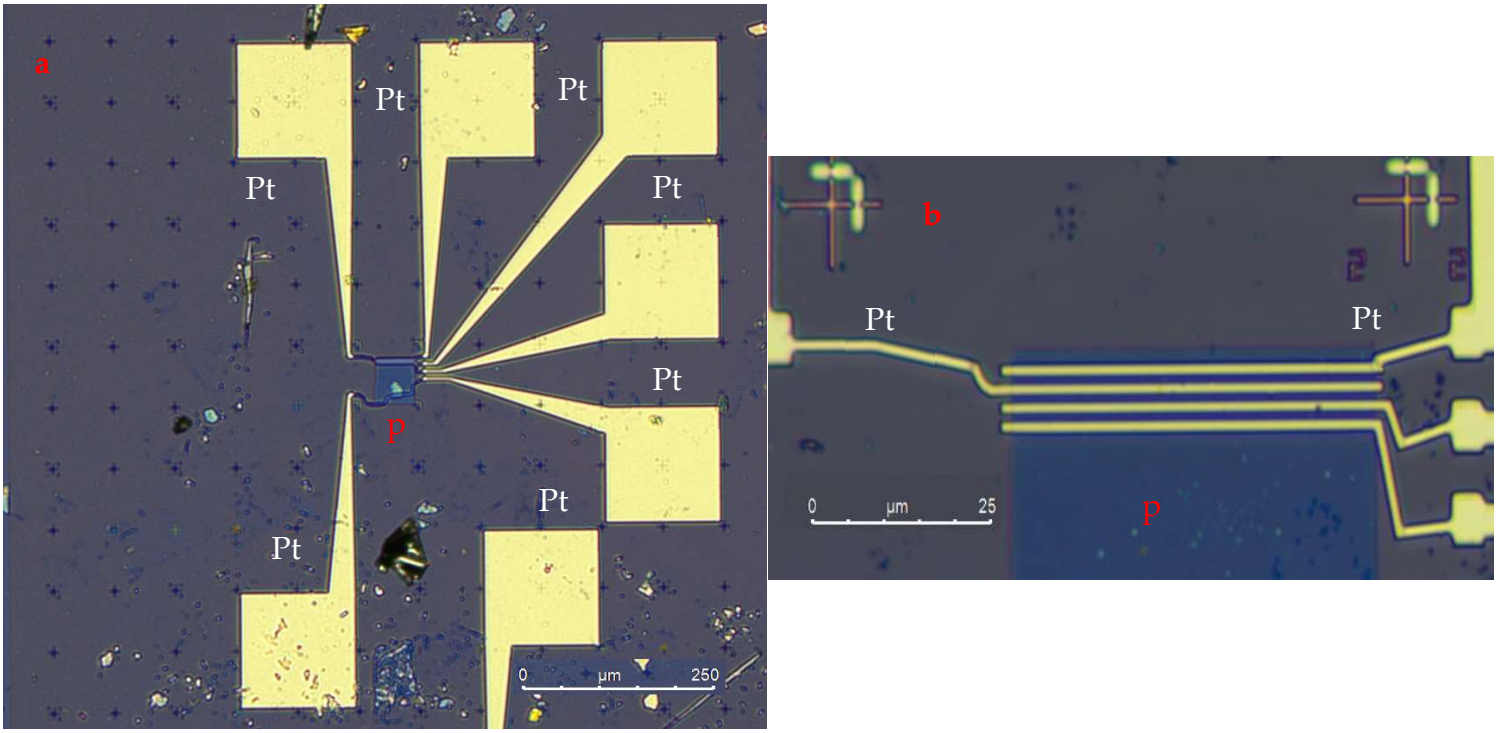


Figure 4.4(a): Pt contacts on a thin flake. 25 nm of Pt were deposited onto an adhesion layer of Ti and were capped by 15 nm of Au to avoid cracks.

(b): Close-up view of the Pt contacts. Contacts span across the whole sample length to avoid non regular conduction across the flake.

self-limiting (as it is for Pt), so Ag contacts have good metallic behaviour only for a small window of time after being exposed to air. So, Au is the material of choice for n-type contacts since other low work function metal contacts are not suitable for the process steps implemented. The sample in which both contacts are printed and tested is shown in Figure 4.5.

For p-type flakes Pt contacts are evaporated (luckily the process step to deposit Pt contact is similar to Au contacts). Pt does not adhere to SiO_2 substrates, and it is frail up to the point that for contacts of 25 nm thickness, cracks are present through the contact, hindering conduction. To avoid the first problem, an adhesion layer can be deposited before the Pt contact deposition. The choice for the material to act as adhesion layer falls on Ti since Ti adheres well with both materials and oxidizes fast enough not to have to worry about conduction of current through the Ti layer. For the second problem, 15 nm of Au can be deposited right on top of the 25 nm of Pt, to avoid cracks in Pt. Contacts evaporated with this method are shown in Figure 4.4.

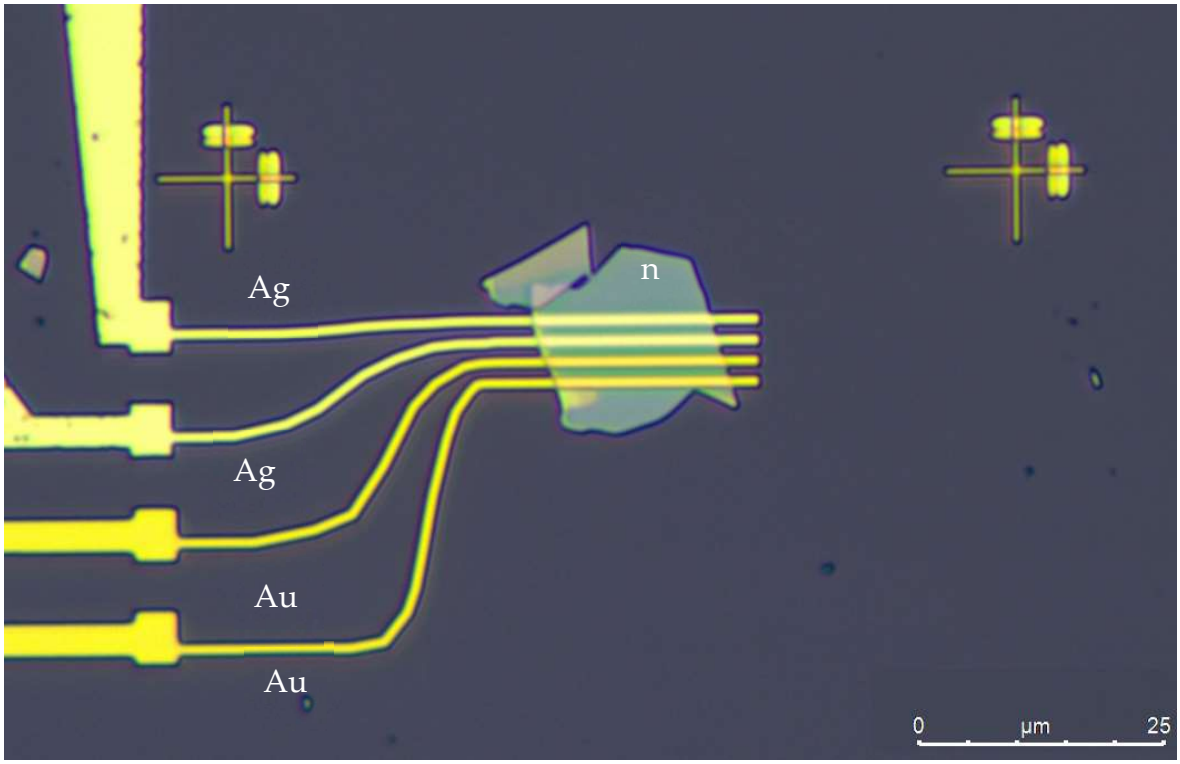


Figure 4.5: Close-up view of Ag contacts (top two, lighter) and Au contacts (lower two, darker) on a 35 nm flake (slightly less strong n-type behaviour).

To apply a gate voltage beneath the substrate (back-gate contact), a copper sheet is connected through silver paste at the back of the substrate, carefully avoiding silver paste slipping from beneath the sample toward the metal contacts on top of flakes to avoid short-circuiting gate and source-drain interconnections. Schematic of back-gatng configuration is seen in Figure 4.6.

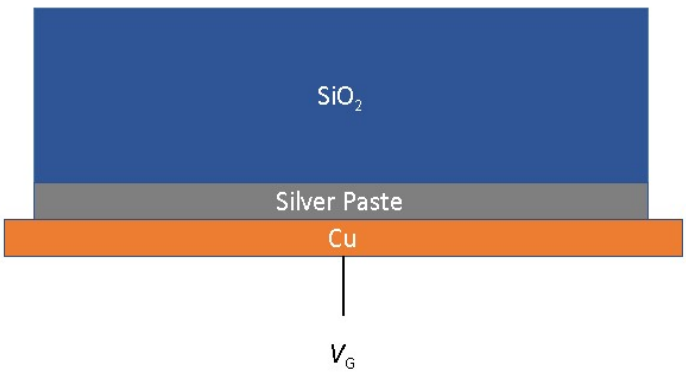


Figure 4.6: Schematic of cross section of back-gate configuration

The sample is now ready to be measured.

4.2. WSe_2 PN junction process flow

After Au exfoliation, p-type sample is coated in two layers of etching polymer and spun. It is exposed and it undergoes RIE. RIE patterns thin flakes by etching away any other flake in the 80x80 micron square. This step is needed because usually thin flakes are connected to thicker ones, and this could cause problems when contacting since avoiding thicker flakes is not always trivial. Furthermore, SF_6 RIE has been proven to implant F atoms, which act as p-dopants for WSe_2, furtherly increasing thin flakes p-type conduction. This increase of p-type carriers should result in a threshold voltage for the FET that is easier to reach. If for both the p-type and the n-type FET threshold voltage is low enough, in absolute value, PN junction behaviour can be expected. To achieve a PN junction, n-type flakes (deliberately not etched to avoid p-type doping) need to be put in contact with p-type ones. Through the hot-pickup technique[21], n-type flakes are stripped away from their sample and gently deposited onto the p-type ones. The sample is gently rinsed in acetone to remove any polymer residues and baking is then needed to strengthen bonds between the newly contacted flakes. 80°C baking for five minutes is usually enough. Contacts are deposited afterwards (Pt contacts for p-type regions with Ti adhesion layer and Au contacts for n-type regions). Pt contacts are deposited as always, while for n-type contacts, 80 nm of Au are needed to ensure continuity over thicker parts of the flakes. After lift-off of contacts and Cu gating through silver paste, measurements can be performed.

Junction formation through deposition of n-type flake onto p-type one was already an established procedure in literature: vertical homo-junctions, as obtained by depositing flakes one on top of another, result in Van der Waals (VdW) interactions keeping the homojunction together. Therefore at the interface the transport has to go through a VdW gap in the homo-junction. The two flakes of WSe_2 have different band diagrams due to their different thickness. This difference in energy levels gives rise to a band offset. A rectifying behaviour can be reached and rectification is due to tunnelling-mediated interlinear recombination.[30] From this knowledge junctions were fabricated as shown in Figure 4.7, with the schematic proposed in Figure 4.8.

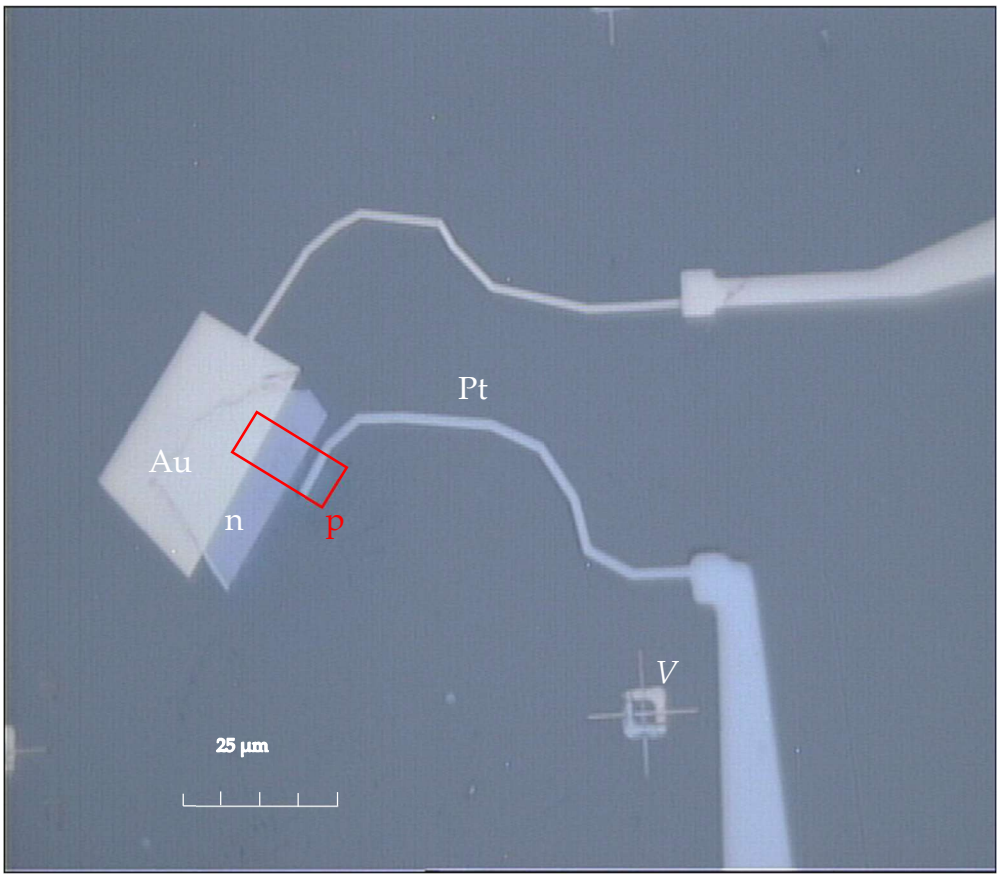


Figure 4.7: Close-up view of PN junction after deposition. Upper contact is Au contact onto thick n-type flake. Lower contact is Pt contact onto thin p-type flake. The red rectangle outlines the thin p-type flake

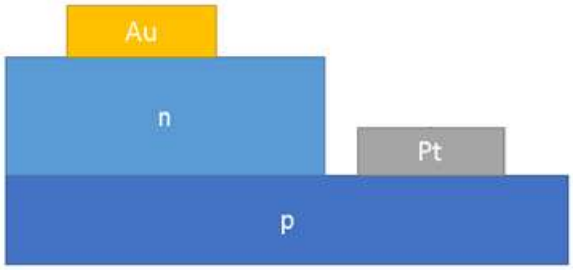


Figure 4.8: schematic of cross section of PN junction after deposition of contacts

4.3. WSe_2 BJT process flow

two procedures have been implemented:

1. the first one consisted in etching a small gap (<100 nm) in the middle of a n-type flake. This was done in order to pick up the whole flake, now divided in two, and deposit onto the p-type one (previously etched). Assuming that the junction between n-type and p-type is present at the edge of the n-type flake, rather than at the surface of interface between the n-type and p-type flakes, the base of the BJT would have been as small as the gap etched in the n-type flake (100 nm, neglecting movement of the flakes while trapped in the polymer and the expansion and contraction of the polymer as the temperature changed). The reuslt of this procedure can be seen in Figure 4.9.

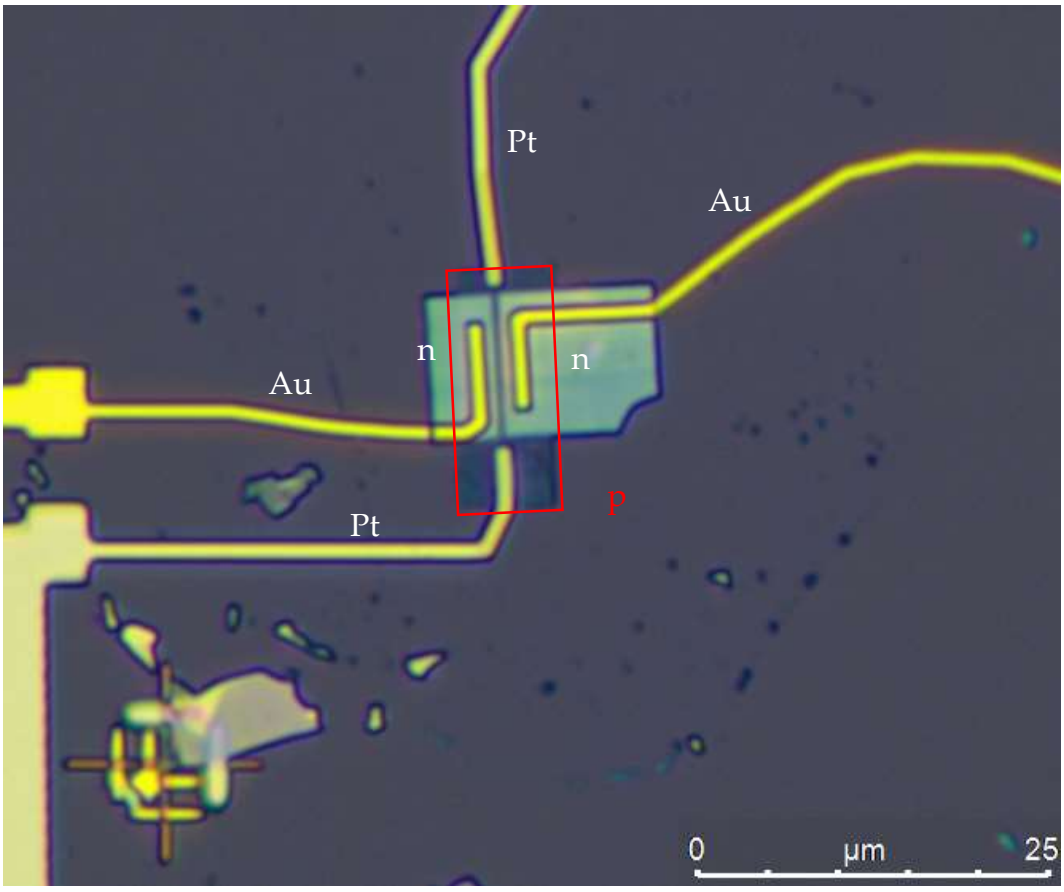


Figure 4.9: NPN BJT view after deposition of thick flake, 100 nm gap previously etched, and after Au and Pt contacts deposition. The red rectangle outlines the thin p-type flake

This procedure was abandoned when the p-doping of SF_6 etching was discovered. The doping in this configuration would have caused a non abrupt junction, which would have hindered the performance of the BJT, not clearly distinguishing between the operating regimes.

2. The second procedure, mainly devised to avoid p-doping was to simply pick up and deposit two different n-type flakes onto the previously etched p-type one. The control on the dimension of the base is now manual and larger bases result in lower probability of achieving BJT behaviour.

After the usual rinse in acetone and baking to strengthen the adhesion between the newly deposited n-type flakes and the p-type base, contacts are patterned and deposited. Cu gating is performed through silver paste and the sample is ready to be measured. A sample obtained with the second procedure is shown in Figure 4.10.

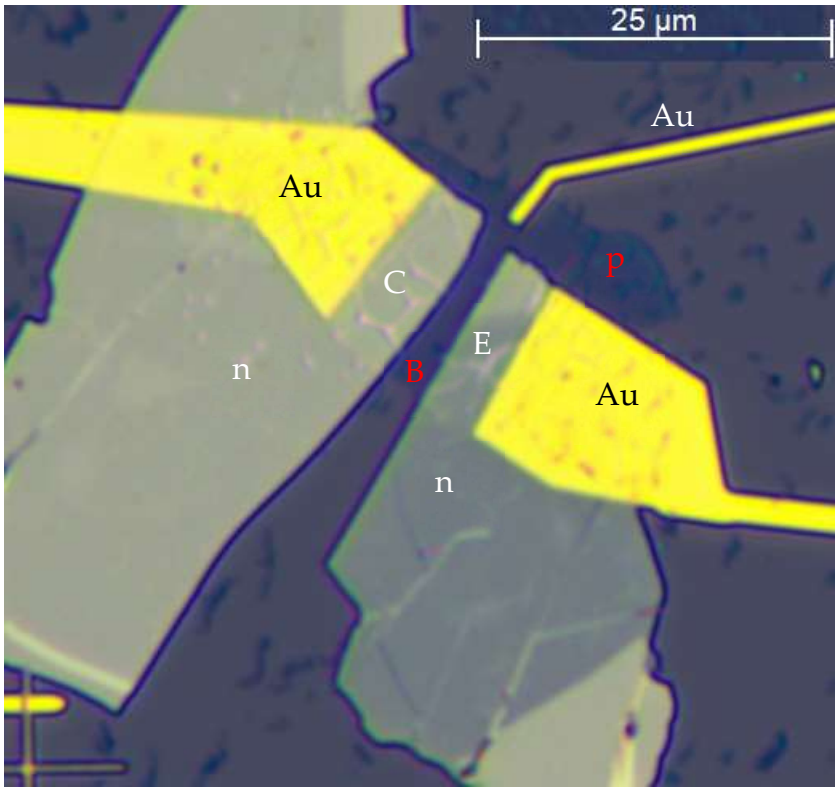


Figure 4.10: NPN BJT fabricated without etching any n-type flake. Base is larger than the other fabrication process, but no doping was implemented that would hinder mobility in the flakes.

both configurations were fabricated to obtain the schematic shown in Figure 4.11

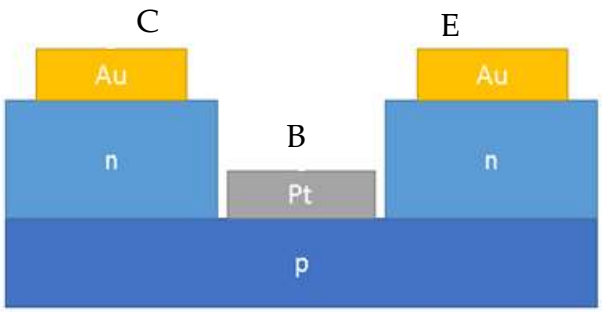


Figure 4.11: Schematic of side view configuration of BJT after deposition of contacts

5 Measurements

In this section measurement procedures are explained, and major results are shown and explained.

5.1. FET

First performed measurements are, usually, transfer curves. Transfer curves are performed by sweeping the gate-source voltage, while a fixed drain-source voltage is applied. The current between source and drain is measured. This measurement is useful to understand the polarity of the material chosen to fabricate.

For n-type materials as the one shown in Figure 5.1, current would flow through the flake only if the conduction band is bent downward up to non-negligible presence of electrons in the conduction band at room T. Therefore, no current would be measured when $V_{GS} < V_{th}$. When $V_{GS} > V_{th,}$ on the other hand, electron presence in the conduction band makes the material conductive. Therefore, when $V_{DS} > 0$ is applied, a current is measured between drain and source. For higher values of V_{GS}, a higher density of electrons will be present in the conduction band, therefore a higher current would be measured for the same V_{DS}. Also, for higher values of V_{DS}, keeping V_{GS} constant, a higher current would be measured since more electrons will be attracted by the positive potential difference between source and drain, up to saturation of currents.

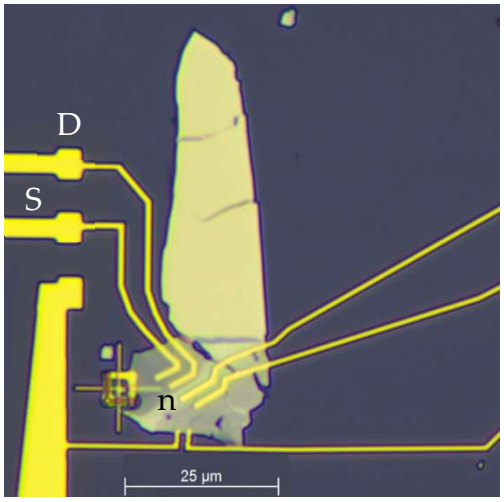


Figure 5.1: n-type flake of which measurements have been performed. Au contacts can be seen deposited on top of it

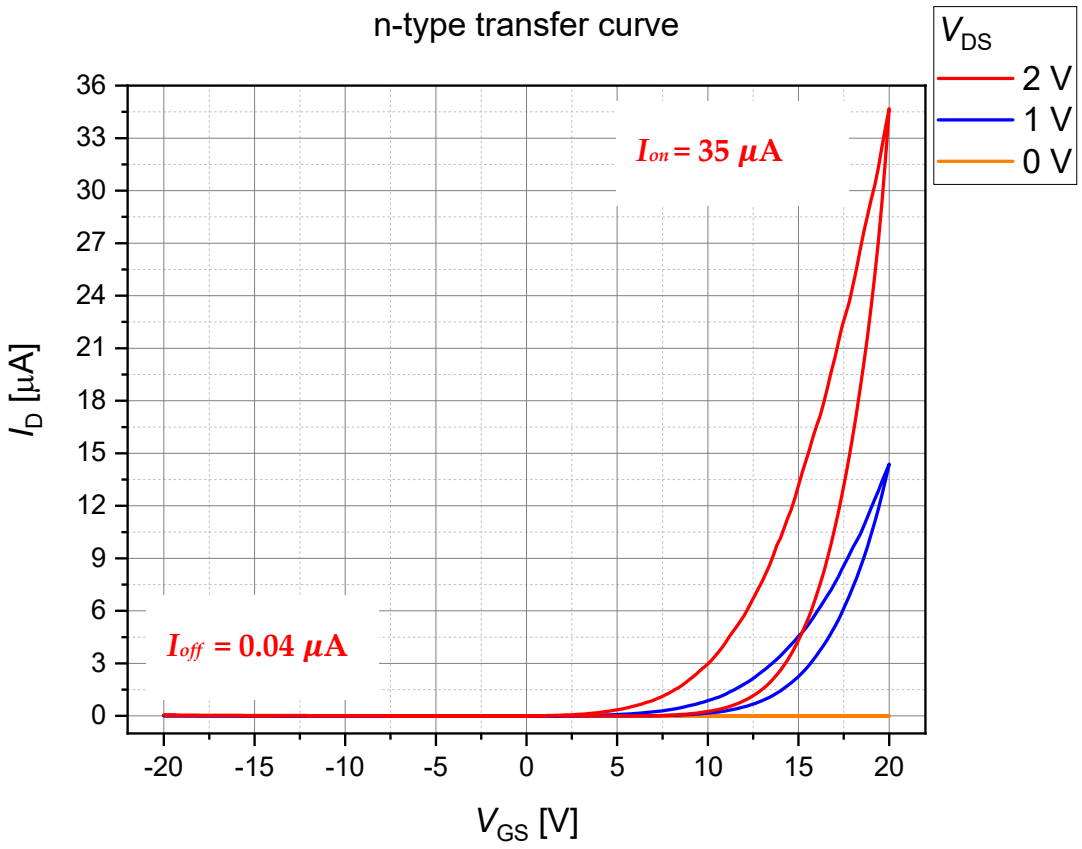


Figure 5.2: Transfer curve of n-type flake measured between -20 V< V_{GS} < 20 V, for V_{DS} values of 0 V, 1 V and 2 V.

This transfer curve for the sample of Figure 5.1 is shown in Figure 5.2. It is measured for V_{GS} sweeping from -20 V to 20 V, for constant values of V_{DS} equal to 0 V, 1 V, 2 V.

It can clearly be seen that for $V_{GS} < 0$, no current flows through the flake even for 2 V of V_{DS}, behaviour which is in agreement with the idea of this flake being a n-type one. No ambipolarity whatsoever is present. Also, current increases with higher values of V_{GS} and of V_{DS}, so the configuration behaves as a FET. Assuming the channel to be as wide as the entire flake (20 μm), we obtain a value of 1.73 A/m. This measurement shows an on/off current ratio of 867.

Threshold voltage of this material is in the range of -5 V - 5 V. To find the correct value more precisely, the current can be expressed in logarithmic scale. The threshold voltage is more visible as it represents the point in which the curve shows a vertical tangent.

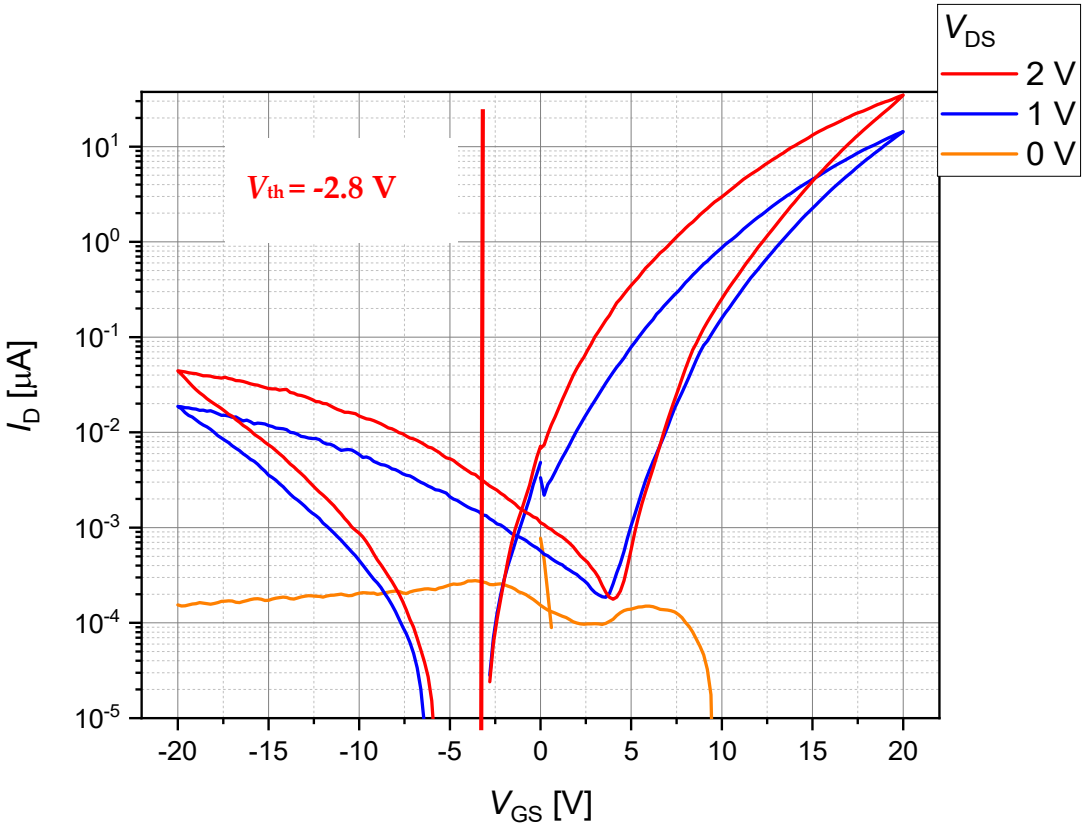


Figure 5.3: Transfer curve of n-type flake measured between -20 V< V_{GS} < 20 V, for V_{DS} values of 0 V, 1 V and 2 V. Current is expressed in logarithmic scale

Expressing the transfer curve in logarithmic scale, as it is done in Figure 5.3, shows interesting properties of the material. V_{th} can be more clearly identified, and it shows a value of -2.8 V. Also, for negative values of V_{GS} the current is not constantly negligible, but a small p-type behaviour is present. N-type behaviour is 4 orders of magnitude stronger than p-type one, and that is why in the graph of Figure 5.2, no p-type curve was seen.

For a p-type flake, like the one shown in Figure 5.4, current would flow through the material only if the valence band is bent upward up to the point of showing non negligible presence of holes in the valence band at room T, thus making the sample conductive. Thus, current would only flow for $V_{GS} < |V\text{th}|$, and increase for lower values of V_{DS}. The transfer curve for the sample of Figure 5.4 is shown in Figure 5.5.

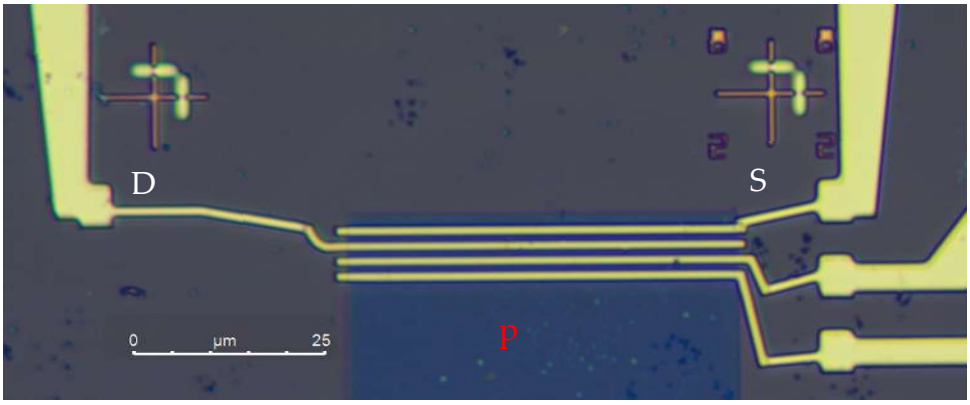


Figure 5.4: p-type flake of which measurements have been performed. Pt contacts can be seen deposited on top of it

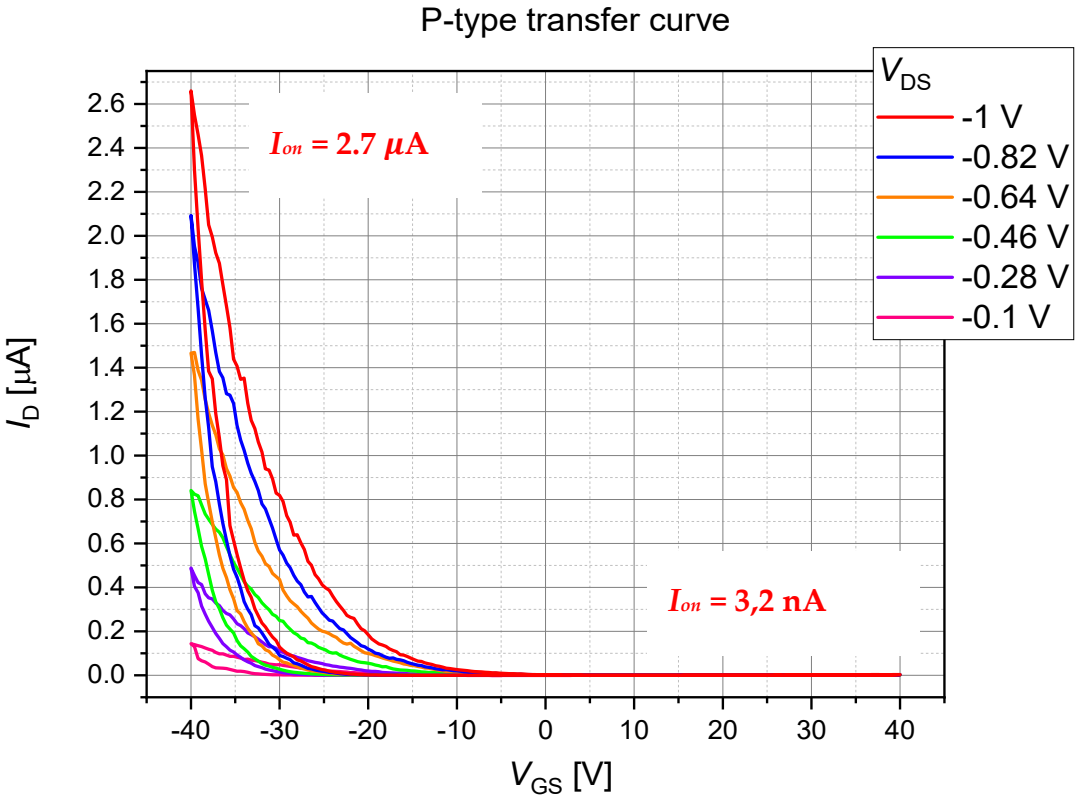


Figure 5.5: Transfer curve of p-type flake measured between -40 V< V_{GS} < 40 V, for V_{DS} values of -0.1 V, -0.28 V, -0.46 V, -0.64 V, -0.82 V and -1 V.

In the transfer curve there is a negligible n-type behaviour, while p-type current is increasing with both V_{GS} and V_{DS} decreasing. Considering the channel length being 45 μm, we obtain a value of 0.05908 A/m. This measurement shows an on/off current ratio of 841. From the logarithmic scale curve, threshold voltage can be identified being 4.8 V.

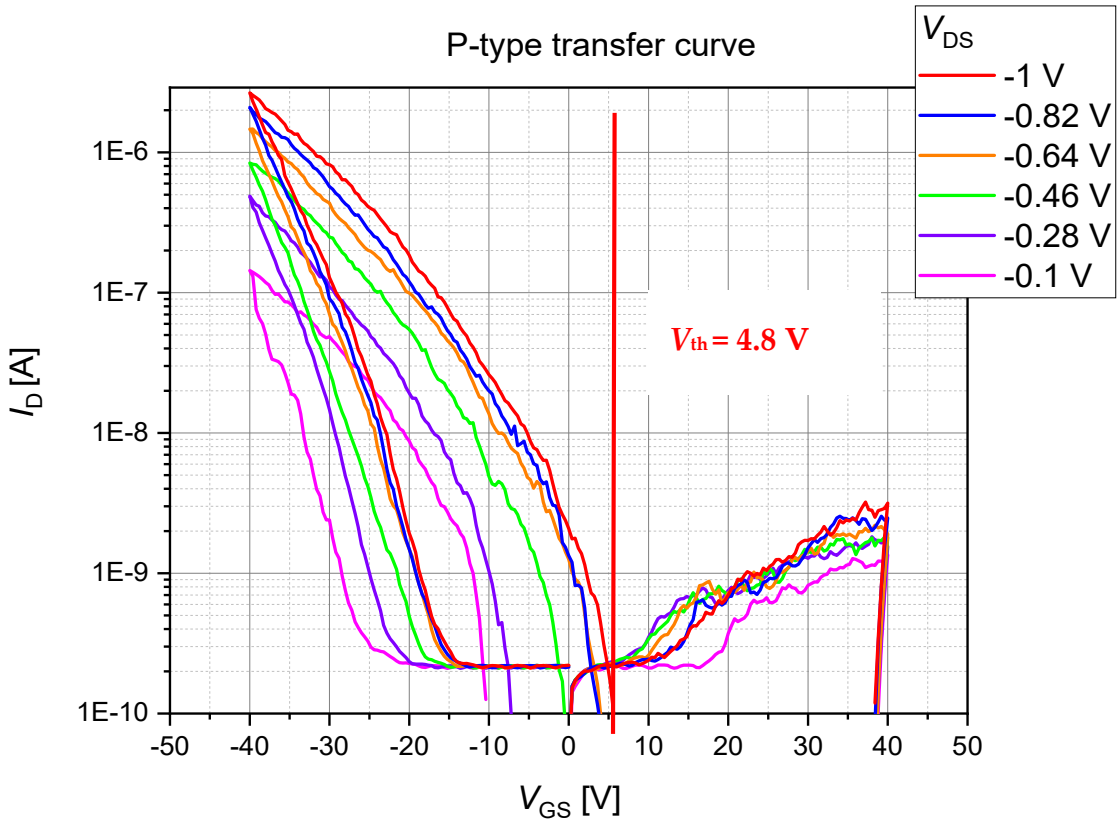


Figure 5.6: Transfer curve of p-type flake measured between -40 V< V_{GS} < 40 V, for V_{DS} values of -0.1 V, -0.28 V, -0.46 V, -0.64 V, -0.82 V and -1 V. Current is expressed in logarithmic scale.

5.3. PN junction

After having established the possibility of tuning the polarity of materials by exfoliation, PN junctions seemed the next obvious step. For PN junctions output measurements are performed. For output measurements a voltage is applied between the p-type region and the n-type one, while the gate voltage is kept constant. Considering the n-type region grounded, for positive voltages applied at the p-type pin, the junction will be directly polarized. In direct polarization, if the voltage is higher than a threshold voltage, current will flow through the junction and increase exponentially with the voltage applied at the p-type pin. On the other hand, if the voltage applied at the p-type pin is lower than the voltage at the n-type region, the junction will be reversely polarized, and only a negligible current will flow through the junction.

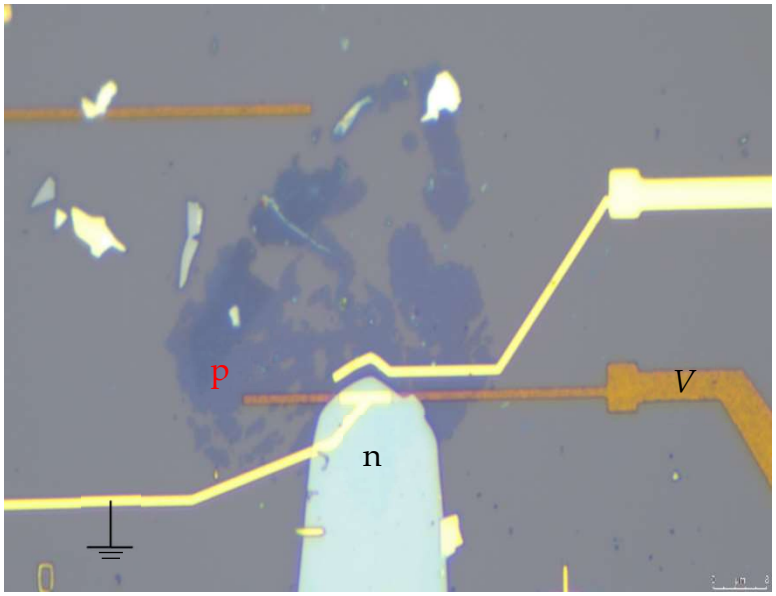


Figure 5.7: PN junction achieved by picking up first an n-type flake and depositing it onto a pre-deposited flake. Afterwards a n-type flake is deposited onto the p-type one. Contacts are then deposited onto both the n and p-type flakes.

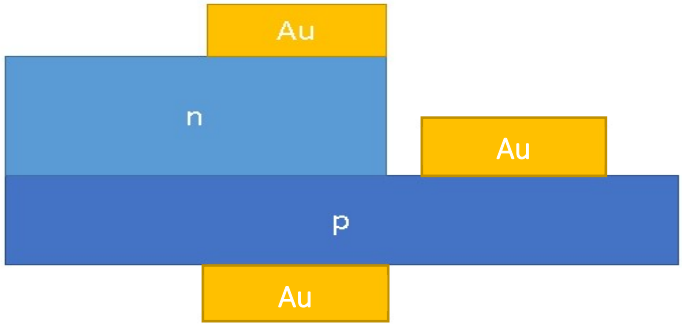


Figure 5.8: simplified schematic cross section of figure 5.7

The interface between deposited n-type flake and the p-type one present below it is not trivial to study. WSe_2 has a layered configuration. Deposition of different flakes on top of the other would make the whole structure behave as a single flake?

If the deposited structure behaves as a single flake, then the junction is present only at the edge of the deposited n-type flake. In the other case, the interface between the p-type region and the deposited n-type flake, will be the region over which the junction extends. A first sample designed to study this behaviour is the one present in figure 5.7, whose schematic is shown in Figure 5.8. This sample is achieved by picking up first an n-type flake and depositing it onto a pre-deposited flake. Afterwards a n-type flake is deposited onto the p-type one. Contacts are then deposited onto both the n and p-type flakes. This configuration allows two measurements to be performed:

1. The first measurement consists in applying a positive voltage at the p-type flake through the contact deposited on top of the flake. In this measuring configuration, both if the junction is at the edge of the n-type region or at the vertical interface between p-type and newly deposited n-type, the current will flow through the junction and a junction behaviour will show in the output curve. Figure 5.9 shows the flow of current and the possible junctions in the material in this measurement.
2. The second measurement is carried out by applying a positive potential to the lower contact (the one onto which the p-type sample is placed). In this configuration, the junction behaviour will be present only if the junction is present at the vertical interface between p and n-type flakes. Figure 5.10 shows flow of current in this configuration and the possible junction in the measurement.

To implement the first measurement configuration, a voltage is applied to the p-type pin of the PN junction. The voltage applied in this configuration is from -0.5 V to 0.5 V. for V > 0 V, the junction is forward biased and current flows. This current increases exponentially with the applied voltage. Considering figure 5.7 voltage is applied at the *V* pin, while the n-type pin is grounded. Current will flow from *V* to ground. If the output curve represents an junction output curve, then the interface between the p-type and deposited n-type, does not behave as a single flake.

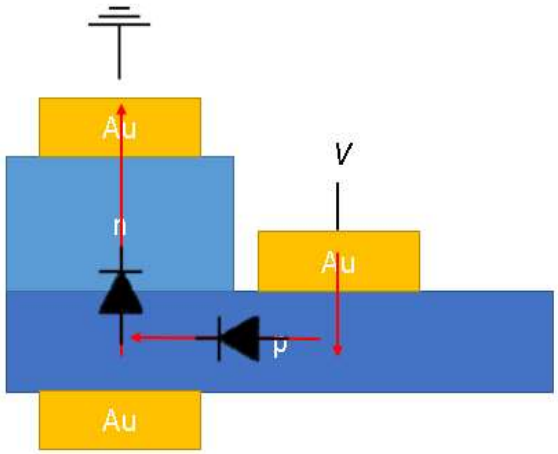


Figure 5.9: schematic of cross section configuration of output measurement of PN junction in the first configuration

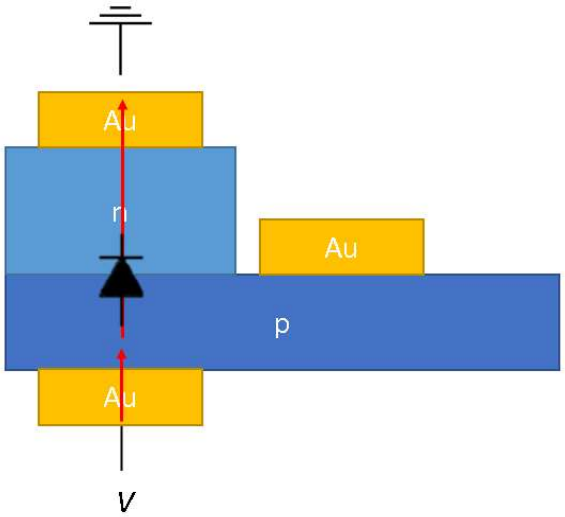


Figure 5.10: schematic of cross section configuration of output measurement of PN junction in the second configuration

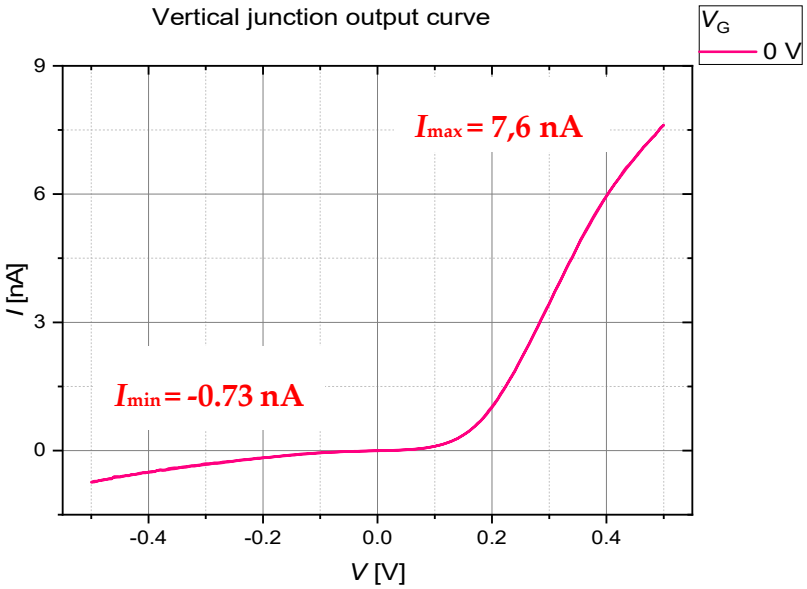


Figure 5.11: For the p-type region Pt contacts have been deposited, while Au contacts are the choice for n-type regions

Measurement carried out for the second configuration, with voltage applied as in the schematic 5.10, is shown in Figure 5.11. Recalling the theoretical output curve of a junction, the junction behaviour is clear. For this measurement, the ON-to-OFF ratio has a value of 10.42.

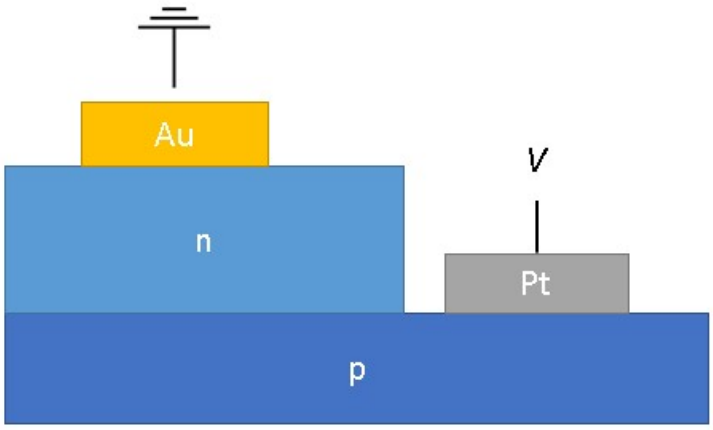


Figure 5.12: schematic of cross section configuration of output measurement of PN junction with both Au and Pt contacts.

Considering now Figure 5.13, the measurement, obtained by the device shown in Figure 4.7, is carried out in the first configuration, the schematic of which is shown in Figure 5.8. In this measurement a negative back-gate voltage was needed to bend upward the valence band of the material. For the n-type flake, this would result in a lower concentration of free electrons, while for the p-type region, this voltage would result in an increase of free holes (just like in the FET configuration). Given that n-type conduction has always shown higher current than p-type one, the negative applied voltage favors p-type carrier concentration hindering the n-type concentration, effectively equaling them. Thus, a better conduction through the junction is achieved. In this measurement the voltage is applied at the *V* pin, while the n-type contact is grounded. Current flows from the *V* pin to ground. For –20 V of V_G, the ON-to-OFF ratio achieved is 16.89.

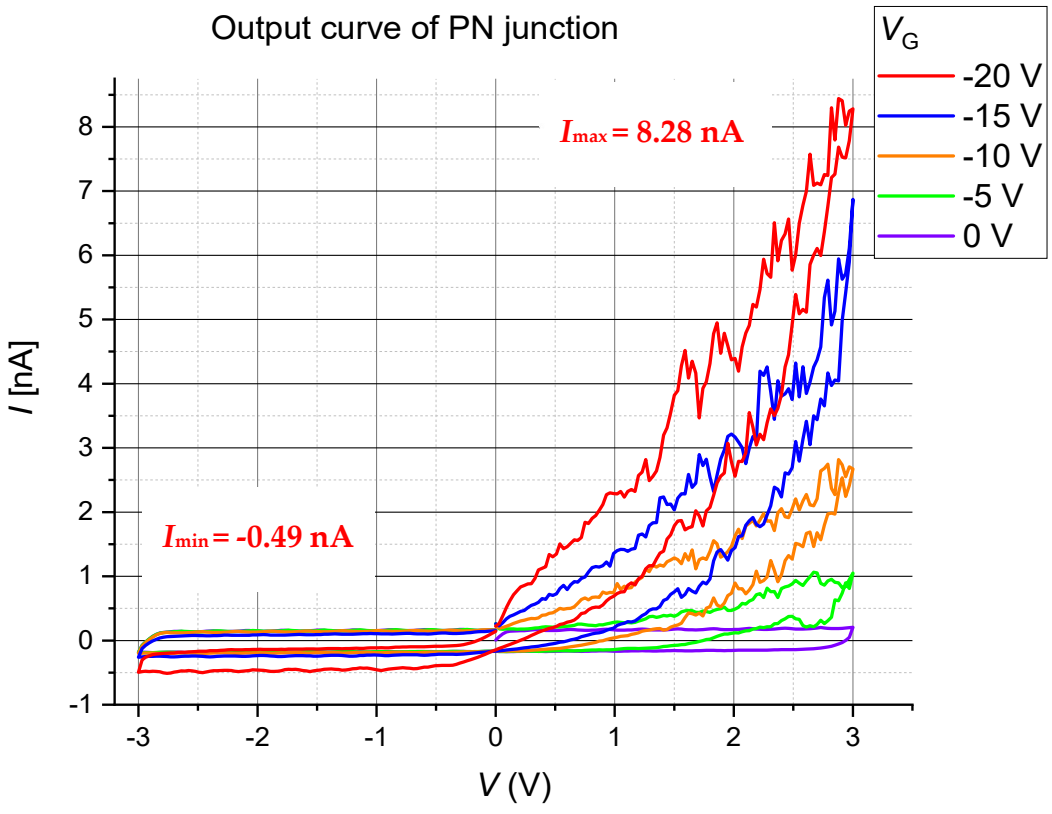


Figure 5.13: output curve of PN junction measured between -3 V and 3 V applied to the p-type pin and grounded n-type region. The gate voltage is varied in steps from 0 V to -20 V

Junctions achieved in the second configuration show no breakdown current for measured voltages V up to -7 V. This characteristic, combined with the possibility of achieving strong rectifying behaviour if the p-type current density is improved show interesting applications for WSe_2 PN Junctions.

To achieve better p-type currents less intrusive fabrication steps might be needed. In p-type flakes obtained without Au lamination, current densities on the same order of magnitude as n-type current densities were achieved, showing how engineering fabrications could open up new possibilities for this material.

Lastly for Figure 5.11 it can be seen how the reverse biased junction exhibits non negligible current. This current also decreases for decreasing values of V_{DS}. Looking for a possible solution in literature, a possible hypothesis that brings a similar result was found in considering ohmic conduction of p-type carriers through both flakes. When a negative back-gate voltage is applied. This negative voltage pushes the Fermi level of both the n-type and p-type flake into the valence band, effectively making both flakes p-type conductors. This behaviour results in the reverse current for negative V_{DS}, which, since conduction is carried out by two p-type flakes, is only an ohmic conduction without any junction behaviour.[31] Getting back to the measurement if Figure 5.11, measured with the junction shown in Figure 5.7, the n-type flakes shows contrast for flakes of measured thickness of 30-40 nm. Flakes of this thickness, when measured, did not show strong n-type behaviour but, while still showing majority of n-type carriers, showed an ambipolar behaviour, despite their thickness being way above the critical thickness for ambipolarity. For 0 V of back gate, as it is in our measurement, the reverse current can be hypothesized by considering an ohmic flow of p-type carriers through the junction. The same behaviour is not seen for the measurement in Figure 5.13, because the n-type flake employed in this device is 10 nm thick, with the grey optical contrast. The application of a positive back gate voltage would result in a raising of the band diagram of both the p-type and n-type flakes. This raising of the bands would lower the p-type minority carrier density in the n-type flake, thus avoiding this ohmic curve. The measurement with applied positive voltage to the back gate can be seen in Figure 5.14

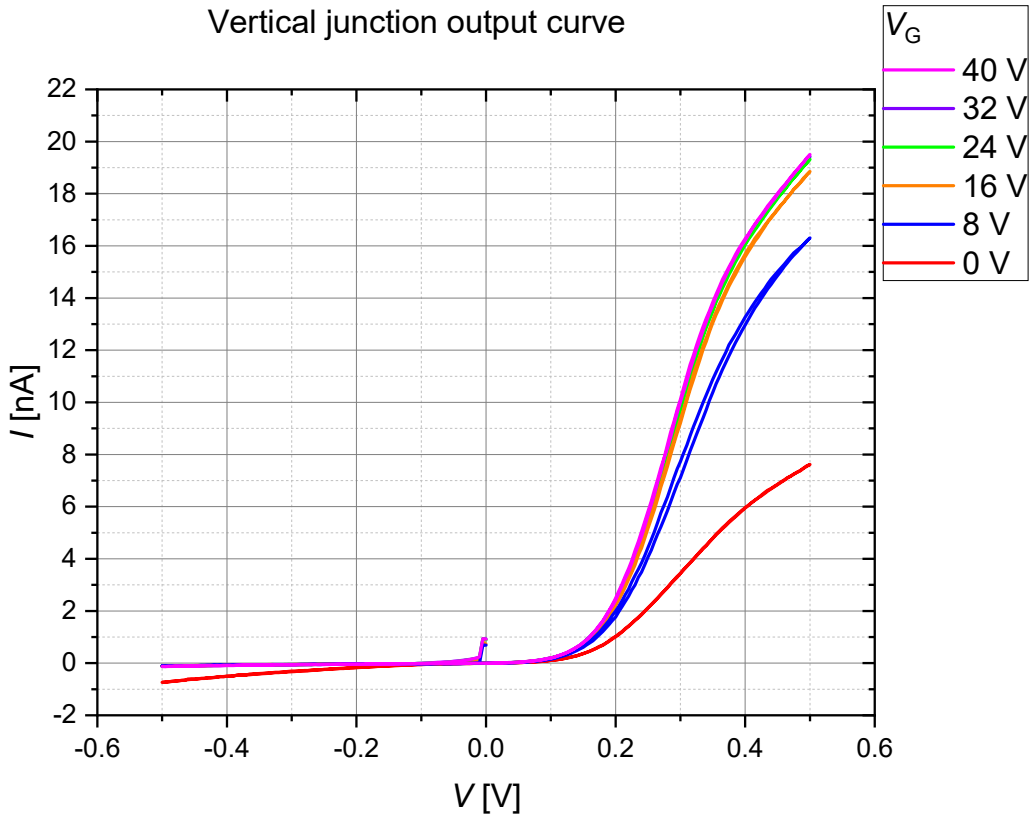


Figure 5.14: Output measurement for the PN junction of Figure 5.7. The positive back-gate measurements support the hypothesis of ambipolarity of the n-type flake.

The measurement is carried out on the device of Figure 5.7 in the configuration shown in Figure 5.10. It can be seen how the ohmic current is present only in the 0 V case for V_G.

5.4. BJT

BJT fabrication steps were proven to ask for a strong toll on the material. Of the devices tried, only a few survived fabrication. Of these few, only one showed what seemed to be control of the collector current by tuning the base voltage. An image of this device is shown in Figure 5.14. Emitter was grounded throughout the measurements. Schematic of the measurement configuration is shown in Figure 5.16.

In the measurement, shown in figure 5.15, even though currents are extremely low, modulation of I_C for different values of V_B can be seen. This behaviour, which looks extremely similar to an output curve of a BJT, shows decrease of current with higher values of V_B. Intuitively this behaviour should be reversed because for higher values of V_B, the base-emitter junction should be more biased, thus, more current should flow in the base-emitter junction. This decrease in the collector current can be explained through considering how thin the base is (< 4 nm). This thin base, combined with the frailty of the p-type flakes, could show deterioration for each sweep of the current, thus explaining how the current lowers for each sweep, since the measurements were performed in order of increasing values of V_B.

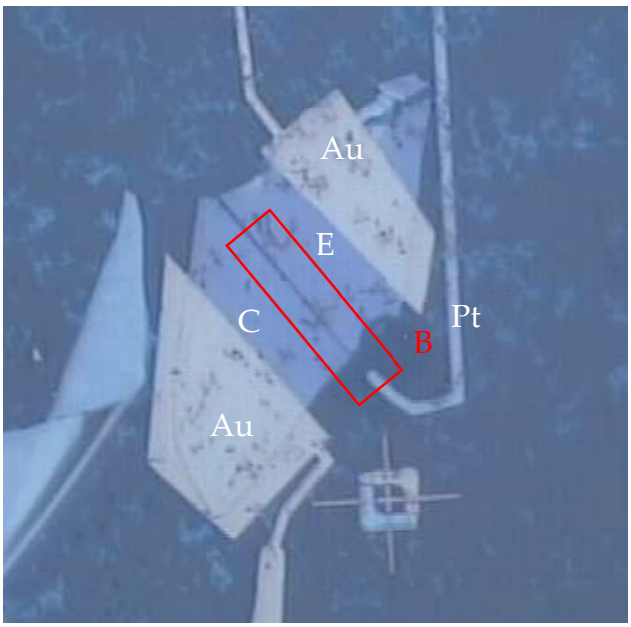


Figure 5.15: NPN BJT fabricated through "hot-pickup" technique. The red rectangle outlines the etched p-type flake below the 2 n-type regions

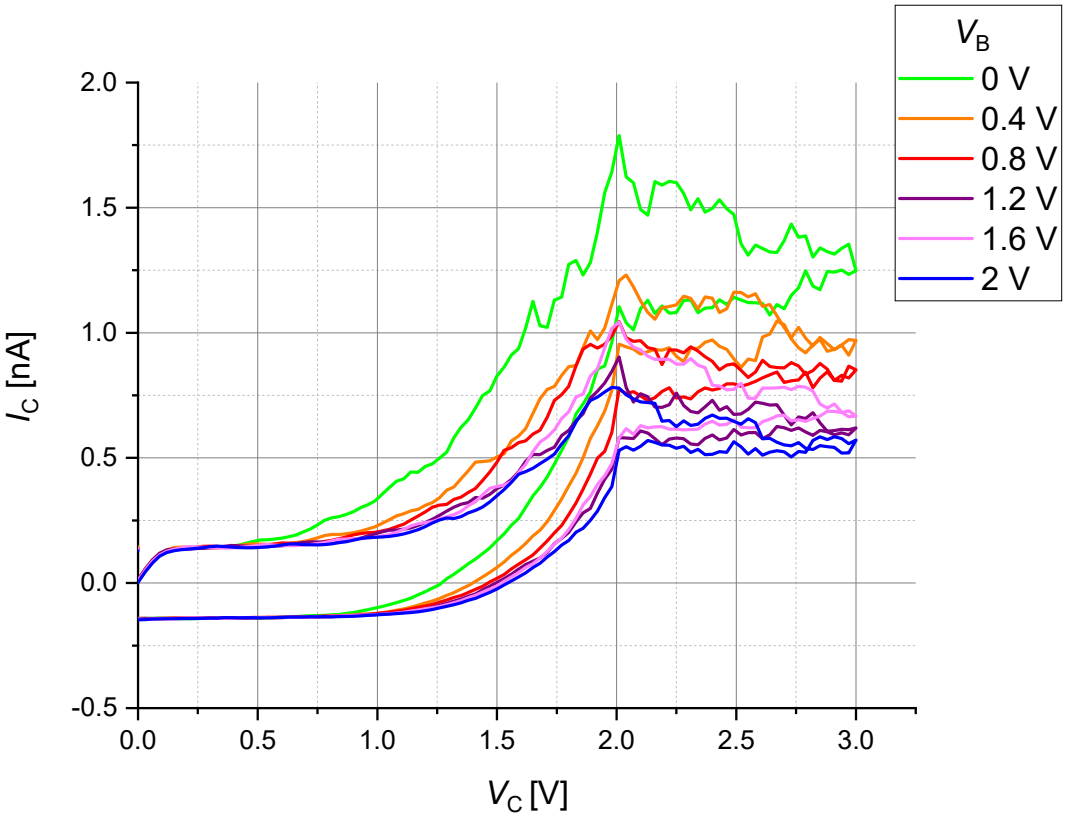


Figure 5.16: output curve of BJT measured from 0 V to 3 V of V_C, for different values of V_B. Emitter is grounded in this configuration.

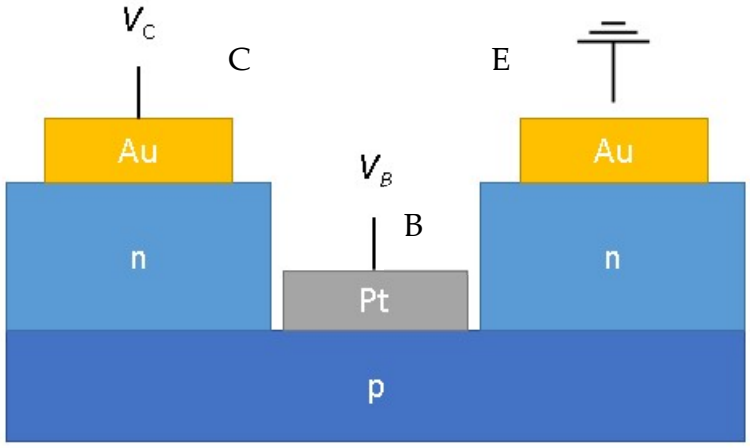


Figure 5.17: schematic of side view configuration of measurements of output curve of a NPN BJT. Au contacts are present on n-type emitter and collector regions, while Pt is deposited onto base p-type region.

6 Conclusions and further applications

In conclusion, thickness-dependent polarity has been demonstrated, with Au and Pt contacts for n-type and p-type regions. The measured currents are not as high as theoretical ones, and this might be due to scattering mechanisms playing a major role in p-type conduction in thin flakes. Doping through other sources could be tried to avoid implantation damage on the thin p-type regions. Another possibility that would result in better mobility through the p-type region could be to pre-evaporate contacts and then strip them and deposit them rigidly on the p-type flake. This would avoid intercalation of the contact material inside the flake during evaporation, thus reducing scattering probability with ionised impurities.

The PN junctions show good ON-to-OFF ratios, but most junctions show good results only for applied gate voltages. To achieve junctions for gates left floating, doping would be needed to move the threshold of both n and p-type flakes so that they would both be active at floating values.

For the BJT configuration a less damaging and more repeatable method needs to be engineered: mechanical pickup and deposition of flakes is a low yield procedure for p-type flakes and the stress applied to the material, both during pickup and deposition, cracks the flakes. The cracks happen both on the deposited flake and the ones around it, including the p-type region that we are depositing onto.

A major difference can be seen between the measurement in Figure 5.11 and the ones in Figures 5.13 and 5.15. The last measurements show hysteresis behaviour between the first current flow and the second one, for the same voltages. The main explanation behind hysteresis is that there are charges at the interface between SiO_2, present below the devices, and the semiconductor. These charges, probably related to incompletely oxidized Si or dangling bonds, can act as trap levels near the conduction or valence bands for the semiconductor. During sweeps, interface charges are filled and emptied with different relaxation times, resulting in the hysteresis behaviour. The hysteresis behaviour also explains why negative current (-200 pA at max) can be measured for forward biased junctions and for positive values of V_C for the BJT measurement. Averaging the values for a round trip measurement, a total positive voltage is obtained. A different substrate to avoid hysteresis behaviour could be adopted

A possible future design for both junction and BJT fabrication might exploit the doping aspect of SF_6 etching to shift carrier concentration of n-type flake toward a p-type carrier majority. Etching of n-type flakes with SF_6 ions has shown intercalation of F atoms from the exposed edges (the ones that get etched) toward the masked fractions of the sample. This doping from the edge characteristic can be exploited if the penetration length of F atoms in WSe_2 is studied. By etching a flake from two parallel sides at a distance double of this penetration length, the remaining strip can be assumed to be uniformly p-type doped. If the doping is enough to suppress the n-type portion, compared to the p-type one, then junctions can be achieved by etching only portions of a flake with this mechanism. The region between the etched portion of the flake and the not etched one might behave as a junction. If the junction is present, a BJT configuration could be designed by connecting in series two junctions fabricated this way and by leaving a strip of p-type doped flake. Ideally a portion of the flake is patterned so that a strip perpendicular to the channel is left. The strip should be of the same width to guarantee uniform p-type majority of carriers, This contact would act as the base of the BJT and modulate the current flow.

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A Fabrication equipment and methods

A.1. Polymer resists

Polymer that reacts when exposed to electrons is the most common material to use as mask for EBL exposures.

Polymers are dispensed onto the sample and then the sample is spun. Final thickness of the resist mask depends on spin speed and on polymer viscosity. Different thicknesses are required for different applications. Through spin-coating high uniformity of the film can be obtained. Then a pre-exposure baking is performed to enhance the evaporation of the solvent within the resist and to improve adhesion: heating strengthens the bonds between the resist and the substrate.

3 different polymer solutions have been used in this work: LO1, LO2, and etching polymer, which are all positive resists and are all soluble in acetone.

They are especially useful when metallization steps are required since combining the 2 solutions (first 1 layer of LO1 and then 1 layer of LO2) would result in the lower film (LO1), being less sensible to exposure then LO2, being exposed more (larger areas exposed, which means more areas developed). This uneven pattern in the resist results, after evaporation, in a discontinuity of the metal lines, which allows further and faster penetration of acetone below the deposited layer. An easier lift-off is thus achieved.

For etching purposes, a different polymer is used, called “etching polymer”.

Few drops of polymer are placed on the sample which is then spun at different velocities in a vacuum chamber. The spinning velocity and the viscosity of the material determine the final thickness of the resist layer. This process offers great uniformity of the resist layer throughout the whole sample surface.

Typical spinning processes are: 60s at 6500 rounds per minute (RPM) which would leave thicknesses of around 80-100 nm for all three polymers, 60s at 4000 RPM which leaves 120 nm layer and finally 30s at 8000 RPM which was only used for etching purposes to print the gaps in between n-type flakes which would act as base width

for the BJT (patterning control and resolution were proven to be the best achieved with this configuration).

Figure A.1: Working station with spin coater and hot plates, in clean room ambient, where polymers are coated and spun and where bakings occur.

A.2. Electron beam lithography (EBL)

Polymers used for coatings during this work react to electrons. After being exposed to electron beams, polymer becomes soluble in a liquid solution. This liquid solution leaves unexposed parts intact and ready for subsequent processes. Since exposed parts are used both for channels etching and for metallic contacts evaporation, exposure resolution becomes key parameter of the whole lithographic process.

The exposure system employed in this work is called Raith E-line and it is a fully integrated electron beam lithography system with a resolution limit of 7 nm. In this system electrons are generated by an electron gun kept at a pressure of 10^{-10} mbar.

Electrons from the gun are driven by an acceleration voltage, which reaches values up to 30 kV, toward an anode inside the column. Beam focusing is performed by electrostatic lenses up to desired aperture spots and accelerations. Usually used acceleration voltages and aperture sizes are 30 kV 10 μm 10 mm, 10kV 10 μm 10 mm, 10kV 60 μm 10 mm and 10kV 120 μm 10 mm.

The region of polymer that can be reached without moving the electron gun is called Writefield. Only a portion of the Writefield is exposed at a time. After a portion is finished, the beam is deflected to the next portion which is printed afterwards.

The main advantage of electron beam direct writing is that patterning masks are not required and any pattern can be designed and printed by the CPU of the system.

To avoid exposing unwanted areas, beam blankers are needed: blankers are helpful to deflect away the beam from the sample fast enough not to expose it. Blankers are thus useful to expose areas not adjacent to each other and permit complex designs exposure.

Different acceleration voltages are needed because when electron beam reaches the coating, secondary electrons are generated and move in the polymer in stochastic paths. The problem rises when considering that wherever these secondary electrons reach, polymer becomes soluble in the developing solution, effectively exposing a larger pattern than the desired one. This process degrades resolution. The perpendicular spreading (with respect to the beam direction) range of the secondary electrons is larger the lower the acceleration energy of the electrons reaching the coating surface since they will have a smaller velocity along the direction parallel to the direction of the beam and will take longer time to reach the bottom of the coating. Higher acceleration voltage exposures achieve better resolution than lower acceleration voltage ones, on the trade off of worse imaging of the sample while the preparation of the exposure is being set up: the e-line system acts also as scanning electron microscope and the image resolution depends on the amount of secondary electrons that are reflected in the direction of the detector. For the same reason as before, more secondary electrons will be generated when lower acceleration voltages are employed.

Figure A.2: Raith e-line exposure system.

A.3. Metal evaporation for marking grids and contacts (PVD)

A source material is heated in a vacuum chamber through exposing it to an electron beam.

The deposition of metals happens as emission from a source (that is approximated point-like) toward a small planar substrate placed directly on top of it at a certain distance. The distribution of atoms from evaporated (initially sublimated) from the crucible toward the sample is uniform (isotropic) in a hemispherical geometry. This deposition is usually referred to as “line of sight” deposition: material evaporates from the source, travels the region between source and sample and deposits on the whole surface of the sample. In the regions of the sample where the mask was removed, the evaporated metal will reach the material beneath it and attach to it, while for the regions covered by polymer, it will deposit on the coating.

To ensure high quality of the material evaporated, a strong increase of the electron power is performed before deposition: this step, called “soak”, ensures evaporation of undesired oxides or by-products that might have formed on top of the source material. Also to avoid reactions of the evaporated material throughout its path toward the sample, the chamber in which the evaporation occurs is kept at a

pressure of 10^{-7} mbar before evaporations, virtually ensuring no contaminants in the chamber.

Desired thickness is ensured by a quartz oscillator that measures the deposition rate of the evaporated material. A desired rate is set up before hand, since, to ensure high quality contacts, low deposition rates are needed (0,5 Å /s – 1 Å /s).

An automatic system reads the deposition rate measured by the quartz oscillator and adjusts the power of the electron beam to reach the desired deposition rate. Once the desired rate is achieved, a shutter opens, allowing deposition of the material onto the sample. From this moment onward the grown thickness is measured (as a simple multiplication of rate*time since shutter opened).

Once the desired thickness is reached, the shutter automatically closes and the beam powers down. Once the crucible is cold, vacuum pumps can be turned off and the chamber can be vented.

When the pressure inside the chamber reaches atmospheric values, the chamber can be opened and the sample can be removed from the chamber.

Bathing the whole sample after evaporation in acetone, the masking polymer which was still present on the sample will dissolve and be removed from the sample and bring with it the metal that was evaporated on top of it. This procedure is called "lift-off" and usually takes long times (4-5 hours of acetone bath of the sample for 80 nm of Au deposition) to completely dissolve the polymer mask before attempting removal of the detached metal. If metal is not completely detached, a re-deposition might occur if the sample is removed from the acetone bath, after which the metal attaches to the sample (either onto flakes or onto the substrate) making it virtually impossible to be removed. If the metal is re-deposited on non-necessary regions, it is not a problem, but if it falls in between 2 metal interconnections, short-circuiting of these contacts is possible, rendering certain measurements impossible to perform.

Figure A.3 (a): Electron beam evaporator

Figure A.3 (b): Close-up view of the evaporation chamber. On the top both the quartz oscillator and the shutter, that prevents deposition until desired parameters are reached, can be seen.

A.4. Reactive ion etching (RIE) and plasma asher

Reactive Ion Etcher (RIE) allows for the vertical anisotropic dry etching of the materials on a sample, for shaping of flakes and removing of unnecessary ones (that might short circuit contacts otherwise).

It consists of a vacuum chamber containing two parallel metal plates between which an RF-powered plasma gives energy to gas phase atoms, ionizing them. Ionized atoms are accelerated, by a self-sustained potential drop, toward the sample. Ions reaching the surface of the sample can both chemically react with surface atoms, creating volatile by-products that are pushed away from the surface from the gas flow or sputter with high energetic ions a further amount of surface atoms.

ion bombardment and chemical etching work in a synergetic way resulting in a etch rate higher than the sum of single etch rates, while also promoting a high anisotropy. The theoretical reason behind this phenomenon is because bonds broken by ion bombardment can leave reactive radicals, thus enhancing chemical reaction rates, while also ion bombardment can remove any inhibitor compound

that might be formed resulting from certain chemical reactions (which would otherwise stop chemical etching in its regions).

Chemical fraction of the etching mechanism is present only if selected gases create ions that can react with sample materials. In some cases, chemical reaction does not occur and ion bombardment is not effective enough to etch layers of the sample material. This is usually referred to as "selective etching": materials are etch only by certain gases.

Selective etching can be exploited by heterostructures of materials which are not etched by the same gases, so that each material can be selectively etched, leaving the other material intact.

Gases present in the RIE at L-NESS in Como are SF_6, CF_4 and O_2.

WSe_2 is etched by SF_6, while polymers are etched by O_2.

When etching of WSe_2 is performed by SF_6, polymer masks are hit by SF_6 ions bombardment, effectively reacting with SF_6 ions. This reaction makes the polymer bonds stronger and makes the polymer masks harder to remove. For this reason, a quick O_2 etch can be performed to remove the harder portion of the mask.

Figure A.4: Parallel-plate Reactive Ion Etcher. On top the vacuum chamber can be seen. On the bottom, all experimental parameters (gas flux, chamber pressure, Plasma power…) can be adjusted.

Plasma asher acts on the same principle, except that no acceleration voltage is applied. It results on an isotropic etching of the whole surface. In plasma asher etching is performed with O_2 or Ar gases. These gases are useful to remove residues before exfoliations or polymer residues after masking, but in the latter case precautions need to be taken: the other materials need not to be etched or doped by these gases, since without an acceleration voltage, no anisotropy can be achieved and no control is had over which parts are subjected to this etch and which parts are not.

Figure A.5: Plasma asher chamber on the left. Monitor to keep under control experimental parameters on the right.

A.5. Micromanipulator and "hot pickup" technique

For the manipulation of n-type flakes which were deposited on p-type ones, a micromanipulator has been adopted. Onto the micromanipulator a glass slide can be connected. This slide is put in contact with the sample and mechanically exfoliates the flakes from the sample by vertically stripping them off the substrate.

The glass slide used to pick up and deposit the flakes is composed by a polydimethylsiloxane (PDMS) portion, covered with a spin-coated polypropylene carbonate (PPC) film. After spin-coating of the PPC, the slides are baked in hot plate

at 110°C to completely melt the PPC removing impurities and wrinkles in the material (thus making it easier to see through).

The micromanipulator structure, placed below the optical microscope (since movements of tens of nm are hard to acknowledge with the naked eye) has several degrees of freedom which allow the correct alignment needed to precisely place the n-type flake of material to be deposited. Moreover, temperature control is achieved through a hot plate (onto which any sample is placed and that also provides a vacuum nozzle to keep the sample in place). This temperature control is helpful since it can prove useful for the case of pickup to raise the temperature: the PPC film, at around 90°C, starts melting. This characteristic is exploited right after coming in contact with the desired flake, since by raising the hot plate temperature to 90°C, the PPC would melt around the flake, evenly covering it. Simply lowering the temperature afterwards, would result on the PPC hardening around the desired flake, making it easier to pick it up. For deposition it is also helpful to raise the temperature, since, because at 90-100°C the PPC softens: a weaker action from the PPC to the flake would result on the flake being easier to be left where it has been deposited.

A typical pick-up procedure goes as follows: The sample is placed on the micromanipulator, which is at room T. The glass slide is clamped in the structure and slowly lowered to the sample level, till PPC comes in contact with the substrate but not with the flake. Flake is covered with PPC by both slowly lowering the slide and by simultaneously raising the temperature to 60°C. This combined effort lowers the possibility of trapping air bubbles between PPC and flake, while also ensuring a larger area of the PPC in contact with the flake (which reduces the probability of not picking up the flake). To ensure a better probability of picking up the n-type flake, the temperature is slowly lowered to about 40°C, which stiffens the PPC, consolidating the position of the flake inside of the polymer. The slide is then rose abruptly to strip the flake away from its sample and keep it inside the slide. Then, the sample is either moved to the position of the desired thin flake to deposit the newly picked up thick flake, if it is in the same sample, or, when the p-type flake is in another sample, the second sample is now placed on the micromanipulator, instead of the first one. For the deposition, the procedure is almost the same, since after having risen the temperature, there is no need to lower it up to 40°C because we want to leave the flake where we put it. To further reduce the strength of bonds between PPC and the n-type flake, often a further temperature rising up to 100°C is implemented, and, in critical situations, also completely melting the PPC slide around the flake is a viable option, but it would damage the slide beyond repair. Luckily slides are easy to make and expendable.

After the deposition a gentle acetone rinsing is performed to remove PPC residues and then the sample is baked to strengthen the bonds between the newly contacted flakes.

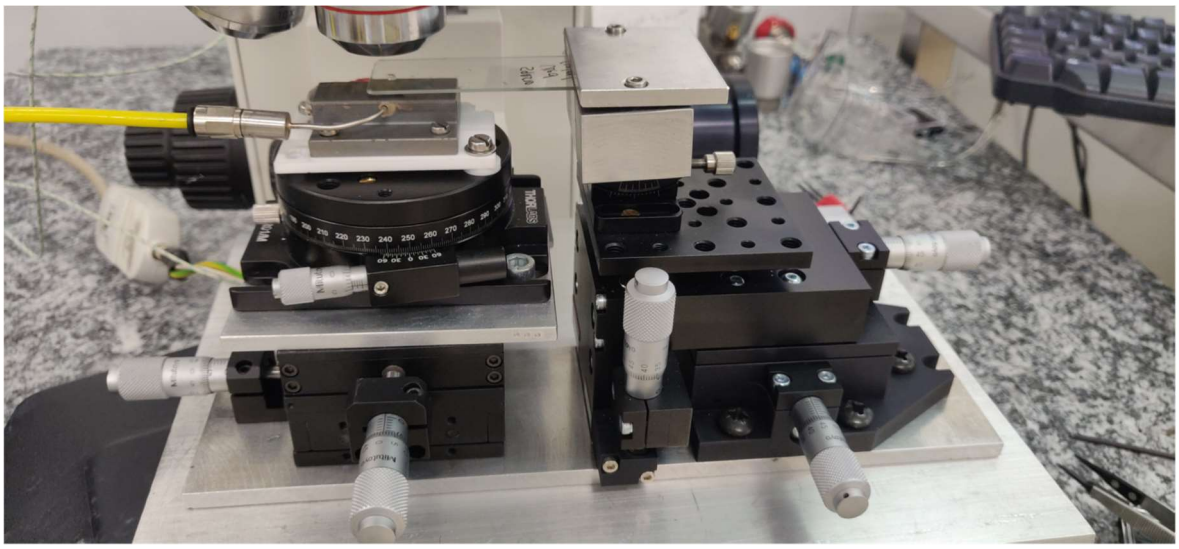

Figure A.6: Micromanipulation station. The glass slide can be clearly seen. The yellow cable transports vacuum to the nozzle placed inside the metal plate, which can be heated to achieve temperature control.

A.6. Probe station

The probe station is composed by 12 tungsten rods through which it is possible to inject signals from 3 different source-meters into our devices and measure the results. During this work, voltage signals have been used as sources and current signals as results.

For Accumulation FETs, voltages were applied by 2 different source-meters: one applied to the back gate, swept from -20 V to +20 V, while the second one was applied to one of the terminals of our device and kept at a constant voltage throughout the back gate voltage sweep. Between each sweep, the constant voltage at the terminal of our device, was switched to a different value. This measurement method is used to plot what are called “transfer curves”.

For PN junctions the measurement consisted in imposing a sweeping voltage at the p-type pin of the device, while the back gate was either floating (no constant voltage

applied to it), or a constant voltage was applied to it. These measurements are called "output measurements".

For BJT measurements three distinct source meters were used: the first one applied a sweeping voltage to the collector pin of our device, the second was needed to apply constant voltages at the base pin of the BJT (the p-type region pin). The base voltage was changed in between the collector sweeps. These measurements represent the "output curve of the BJT".

The last source-meter was used to apply constant back gate voltages in between the measurements of the output curve of the BJT, to improve the flow of current in the 2 junctions constituting the BJT.

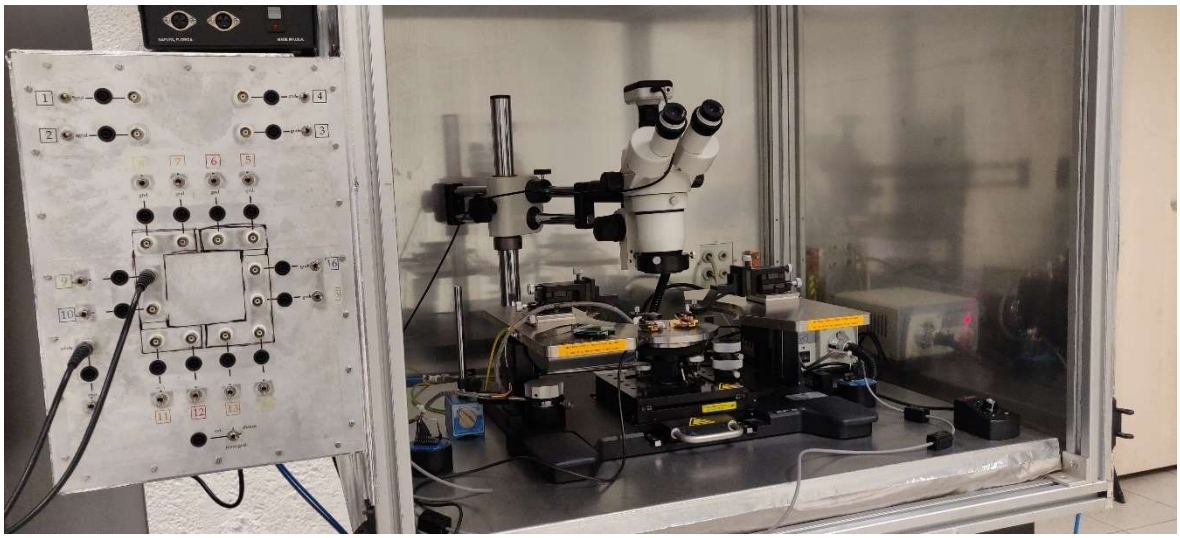

Figure A.7: Probe station.

A.7. Atomic force microscopy

One of the very widely employed techniques for small scale microscopy. A reference force is measured between the tip of a flexible cantilever and the surface of the sample. The force bends the cantilever. The bending is measured through a laser beam sent onto the cantilever, which acts as a reflector. Depending on the bending, portions of the reflected beam will reach the photodetector.

The force acting on the cantilever is approximated by a Lennard-Jones potential: far from the surface, no interaction will bend the cantilever. Closing the gap, the

cantilever will first feel an attractive Van der Waals force, but at a certain distance, it will start to fell the onset of the repulsive regime, that is when electronic charges start to overlap.

The mode in which the device is applied to capture the image is called "tapping mode": an oscillating external force is applied to the cantilever, which will result in an intermittent contact between the surface and the cantilever, which feels a varying force. This operating regime allows for good resolution, while still being non-destructive for the sample studied.

AFM is widely used also because, with respect to Scanning Tunnelling Microscopy (STM), it does not require a conducting sample: any kind of low dimensional system can be studied through AFM.

List of Figures

List of symbols

Variable	Description	SI unit
$\boldsymbol{\mu}$	Mobility	$m^2\ V^{-1}\ s^{-1}$
$\boldsymbol{e}$	Electron charge	C
$\boldsymbol{\tau}$	Scattering rate	s
$\boldsymbol{m^*}$	Effective mass	Kg
SS	Subthreshold swings	V
$\boldsymbol{k_B}$	Boltzmann constant	$m^2\ kg\ s^{-2}\ K^{-1}$
$\boldsymbol{T}$	Temperature	K
$\boldsymbol{d_{ox}}$	Thickness of gate dielectric	m
$\boldsymbol{\epsilon_s}$	Dielectric constant of semiconductor	[/]
$\boldsymbol{N}$	Doping density	m^{-3}
$\boldsymbol{\Phi_s}$	Band bending	V
$\boldsymbol{D_{it}}$	Interface trap density	m^{-3}
$\boldsymbol{\epsilon_{ox}}$	Dielectric constant of the oxide insulator	[/]
$\boldsymbol{I_S}$	Inverse saturation current	A
$\boldsymbol{V_t}$	Thermal voltage	V

$\boldsymbol{\beta_F}$	Forward-active current gain	[/]
$\boldsymbol{\beta_R}$	Reverse-active current gain	[/]

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EXECUTIVE SUMMARY OF THE THESIS

FABRICATION AND CHARACTERIZATION OF WSe_2 PN JUNCTIONS

TESI MAGISTRALE IN PHYSICS ENGINEERING – INGEGNERIA FISICA

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ACADEMIC YEAR: 2021-2022

1. Introduction

Most electronics of our time is based on integrated circuits technology. Over the course of the years lithography improvements resulted in the possibility of patterning smaller integrated circuits components. Smaller dimensions made it so that surface areas of processors shrank while also achieving higher processing capability. This direction drove research into pursuing better resolution for pattern printing. Nowadays Silicon-based technology, the most widely used for electronic purposes, reached dimensions for which quantum effects are no longer negligible. Short-channel effects in transistors must be addressed in order to progress with Moore's law.

This work focuses on employing tungsten diselenide (WSe_2), a two-dimensional semiconducting material, to circumvent this problematic and to set a starting point for transition metal dichalcogenide (TMDC) based electronic technology, by proving how WSe_2 PN junctions are achievable.

2. Fabrication

WSe_2 has been chosen since, by being a TMDC, it is immune to short-channel effects. Also, TMDCs build on the same lithographic experience base of Si. Theoretical carrier mobility in TMDCs is as high as Si. I.e., Si has theoretical mobility of 1200 ($cm^2 V^{-1} s^{-1}$), WSe_2 shows theoretical hole mobility of 500($cm^2 V^{-1} s^{-1}$).[2]

TMDCs show no reactive surfaces due to the absence of dangling bonds in between layers and their band diagram is thickness dependent.[1]

WSe_2 also has the peculiar characteristic of having thickness-dependent polarization. This property has been exploited in this work to achieve elementary electronic device without the need for heterostructures and external doping of carriers.[3]

Below 4 nm of thickness, WSe_2 shows p-type polarization, while n-type polarization is present when thickness is above 7 nm. In between 4 and 7 nm ambipolar carrier density can be measured.[2]

Thicknesses are measured through atomic force microscopy (AFM).

Figure 1 shows optical microscope image and AFM of WSe_2 flake with highlighted interesting thicknesses. Figure 2 shows AFM measurement of thickness for the flake shown in Figure 1.

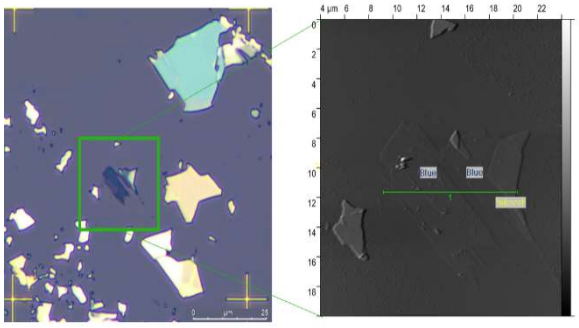

Figure 1: Optical microscope and AFM image of flake of desired thicknesses

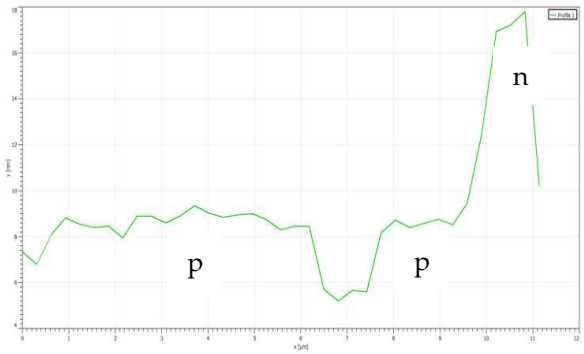

Figure 2: AFM measurement of thickness of flake of Figure 1

To measure transfer curves and demonstrate different polarity of carrier densities the accumulation field effect transistor (FET) configuration has been employed.[6]
WSe_2 crystal is exfoliated to obtain samples of thicknesses needed for the two polarities. Exfoliated material is deposited onto a SiO_2 substrate. Gating is achieved through a back-gating configuration.[5]
Contacts are deposited onto exfoliated samples through Evaporation. To reduce contact resistance different metals were chosen for flakes of different polarity. For p-type flakes Pt contacts were evaporated, while for n-type ones Au contacts were deposited.[7] Patterning of the contacts was achieved through electron beam lithography (EBL).[8]
Contacts are deposited in FET configuration and transfer curves can be measured. Schematic of FET is shown in Figure 3.

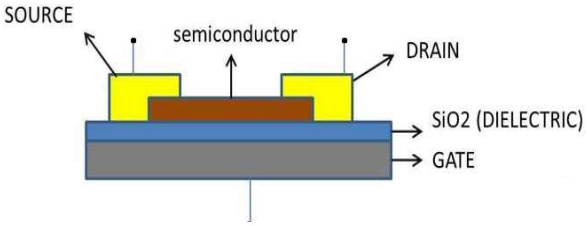

Figure 3: schematic side view of FET configuration

After having demonstrated p-type and n-type polarity in the chosen thicknesses, with neglectable ambipolarity, PN junctions can be fabricated. PN junctions are achieved through contacting p-type and n-type flakes. Flakes of different polarity are put in contact through the hot-pickup technique:
A glass slide, coated with polydimethylsiloxane (PDMS) and polypropylene carbonate (PPC), is lowered, through a micromanipulator, in contact with a desired n-type flake. Through temperature control, PPC is melted around the flake. After melting, temperature is lowered, solidifying the PCC around the flake. Mechanically moving away the glass slide from the sample will result in mechanically stripping the n-type flake from the substrate. The flake can be deposited on top of the p-type flake, by gently lowering the glass slide. Release of the n-type flake from the PPC is favored by melting PPC once again.
After deposition PPC residues are dissolved by rinsing the sample in acetone and baking is employed to strengthen the bonds between the two newly contacted flakes.[9] Contacts are afterwards evaporated the same way they were deposited for the FET device, with Pt contacts for p-type region and Au contacts for n-type region. The PN junction is achieved. Sample is ready for measurement. Scheme of junction is presented in Figure 4.

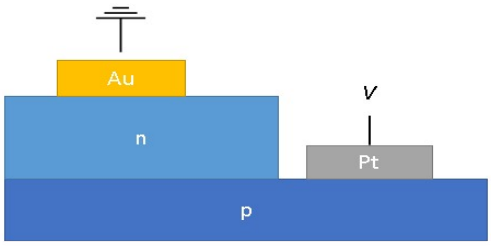

Figure 4: Schematic side view of PN junction configuration

3. Measurements

First n-type and p-type polarity measurements are carried out on the FETs samples.
Optical microscope images of the chosen flakes with evaporated contacts are shown in Figure 5 and Figure 6.

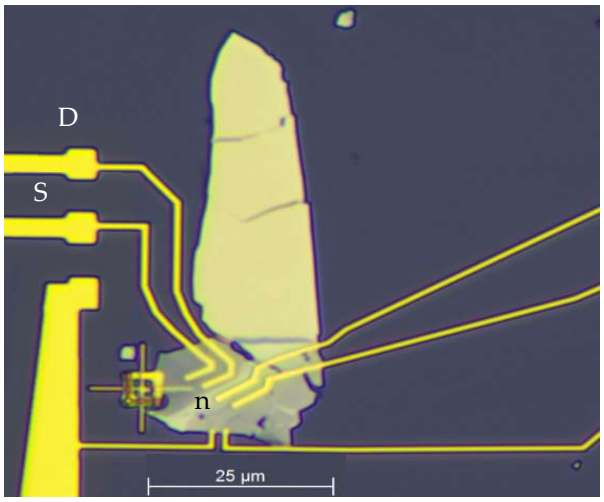

Figure 5: Optical microscope image of n-type flake after Au contacts deposition

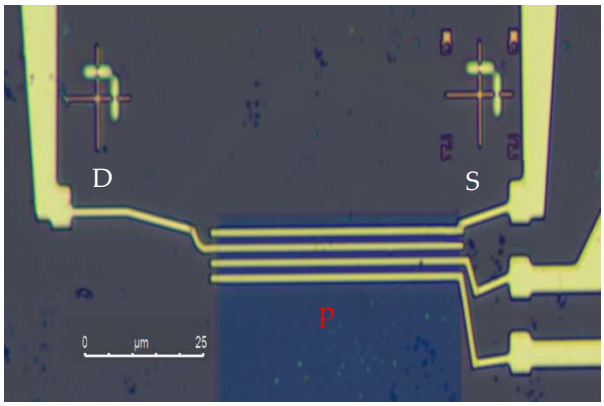

Figure 6: Optical microscope image of p-type flake after Pt contacts deposition

Source (S in the Figure) is grounded and voltage is applied at the drain contact (D in the Figure).

The First measurement performed was the transfer curve for the n-type flake presented in Figure 5.
Transfer curve has been measured by sweeping the gate-source voltage (V_{GS}) from -20 V to 20 V for three different values of drain-source voltage (V_{DS}): 0 V, 1 V and 2 V. Results can be seen in linear scale in Figure 7.

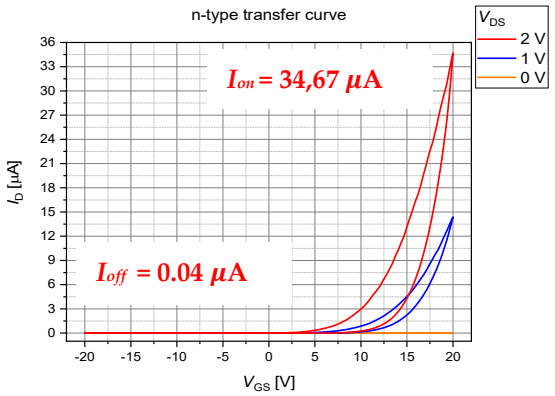

Figure 7: Transfer curve of n-type flake shown in figure 6.

Measurements show strong n-type polarity and an on/off current ratio of 866,75. Considering the width of the flake to be 20 µm, we obtain a current density of 1.73 A/m.
For V_{DS} = 0 there is no current, as expected, and current increases with higher values of V_{GS}. This behaviour proves that the flake behaves as a FET.
To better recognize the threshold voltage of the FET, the current is expressed in logarithmic scale in Figure 8.

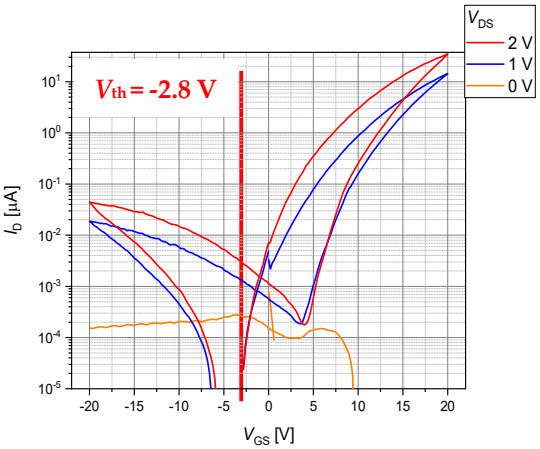

Figure 8: Transfer curve of n-type flake with current expressed in logarithmic scale

Threshold voltage is easily identified having a value of -2.8 V.

Similar measurements have been carried out on the p-type sample of Figure 6.
Transfer curve has been measured by sweeping the V_{GS} from -40 V to 40 V for six different values of V_{DS}: -0.1 V, -0.28 V, -0.46 V, -0.64 V, -0.82 V and -1 V. Results can be seen in linear scale in Figure 9.

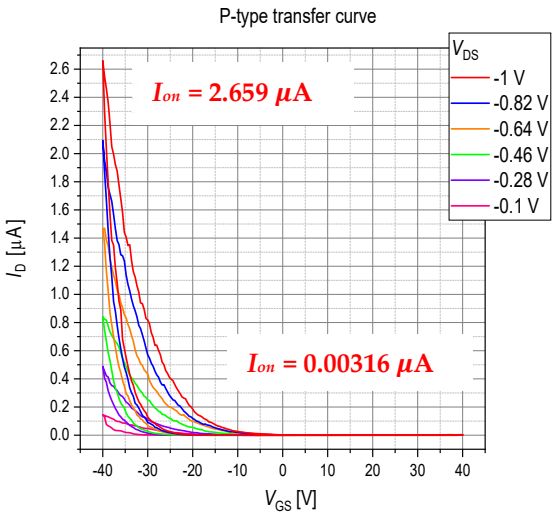

Figure 9: transfer curve on p-type flake shown in figure 7.

Negligible n-type contribution and on/off current ratio of 841,455. Flake presents channel width of 45 μm, thus showing a current density of 0.05908 A/m. Transfer curve with current expressed in logarithmic scale can be seen in Figure 10.

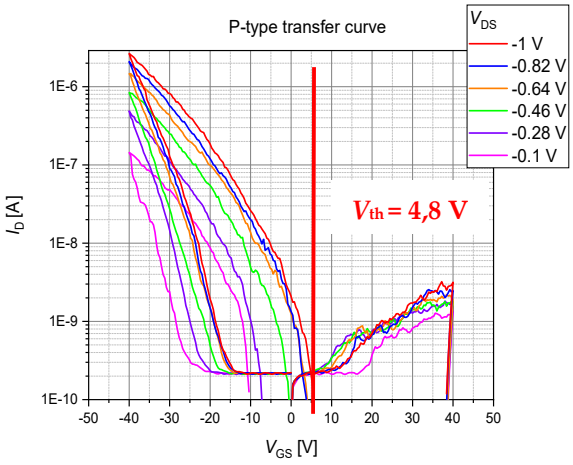

Figure 10: Transfer curve of p-type flake with current expressed in logarithmic scale.

From the transfer curve expressed in logarithmic scale the threshold voltage is identified with a value of 4.8 V.
P-type current density is lower than most common semiconductor used for electronic purposes. To improve p-type conduction doping can be implemented. SF_6 reactive ion etching (RIE), was employed to completely etch not needed flakes, that could short circuit contacts. SF_6 RIE was proven to also introduce F doping on WSe_2. Remembering the layered configuration of WSe_2, F doping would act only by substitution of W atoms with F atoms. Due to the Se layers, both on top and below the W plane, this substitution can only act on the edges of the flakes. Etching of a p-type flake results in intercalation of F atoms from the edges of the flakes, resulting in a higher p-type carrier density in the flake. Unfortunately, F doping was not enough to achieve p-type current density as high as most common semiconductors. The main reason why high current densities are not achieved even with F doping might be that it caused an increase of scattering events in the few layers of material. This scattering component happens in the presence of charge impurities (F atoms) and degrades the mobility of holes and electrons.

For PN junction measurements, voltage is applied to the p-type pin, while the n-type pin is grounded. In this configuration positive applied potentials V polarize the junction directly and, therefore, non-negligible current should flow through the junction. When V is negative, the junction is inversely polarized and only the inverse saturation current should flow through the junction. A top view of the junction, after deposition of both n-type and p-type flake on top of Au contacts, can be seen in Figure 11. Figure 12 shows only a schematic of this peculiar configuration.

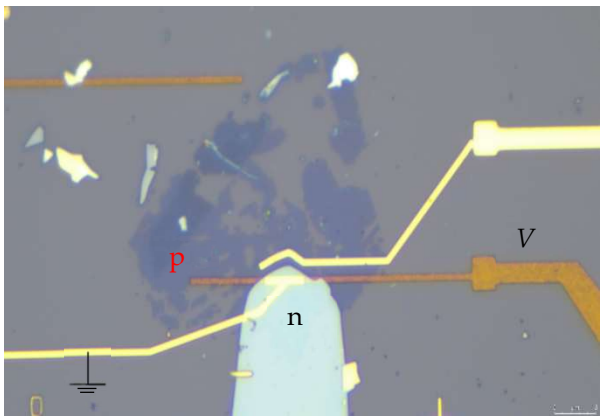

Figure 11: Top view of PN junction, achieved with "hot-pickup" technique, and contacts deposition.

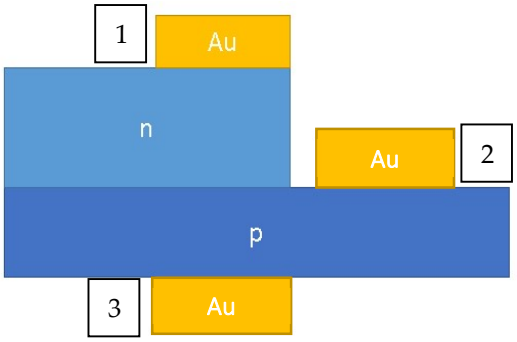

Figure 12: Schematic of side view configuration of vertical PN junction.

With the configuration presented in Figure 12, vertical junction between n-type and p-type flakes can be studied.
This configuration is useful to understand the behaviour of deposited n-type flake on top of the p-type one. Due to the layered configuration of WSe_2, two behaviours can be expected:

1. The p-type layers will form Van Der Waals (VdW) forces with the n-type layers. This will result in the n-type flake and the p-type portion underneath the n-type flake behaving as a single n-type flake, due to the high thickness. It will result in a PN junction measured only between contacts 1 and 2.
2. The second expected behaviour is a junction present vertically between the n-type flake and the p-type flake. This junction could be measured by biasing the contact 3 and grounding contact 1.

Even though Pt contacts showed better conduction of p-type carriers, Au contacts have been employed in this device even for p-type flakes. The first reason behind this choice is that Au contacts show good conduction of both holes and electrons.[7]
The second reason is that different metals for contacts could result in a Schottky barrier due to the different Fermi levels of the contacts.
This barrier could cause diode behaviour and, since the measurement affects what is thought to be a PN junction, this effect could affect the significance of the measurement.

The second configuration is the one studied first.
Output curve of vertical PN junction is presented in Figure 13.

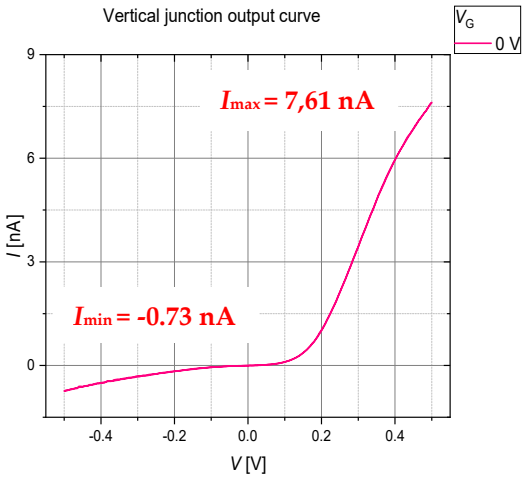

Figure 13: Output curve of vertical junction measured for *V* in between -0.5 V and 0.5 V

This curve shows junction behaviour, suggesting that the n and p-type flake, after being deposited one on top of the other, still behave as different flakes.
ON-to-OFF current ratio has a value of 10.42.
"Hot pickup" of p-type flakes has shown low success rate, so a different approach has been implemented. P-type flakes are not stripped away and re-deposited on contacts, but n-type flakes are deposited on top of p-type flakes and then contacts are evaporated to connect both regions. This configuration is the one showed in Figure 4 and the one mainly employed during this work.
An example of a junction obtained with this method can be seen in Figure 14.

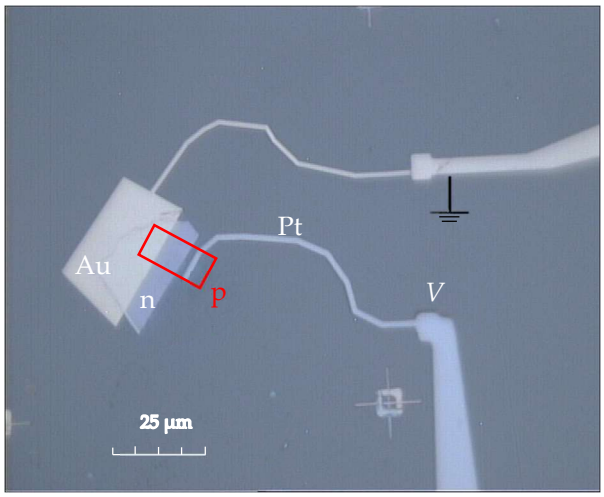

Figure 14: Top view of PN junction, achieved with "hot-pickup" technique, and contacts deposition. P-type flake is highlighted with a red outline due to low outline contrast

Output curve for this configuration is presented in Figure 15.

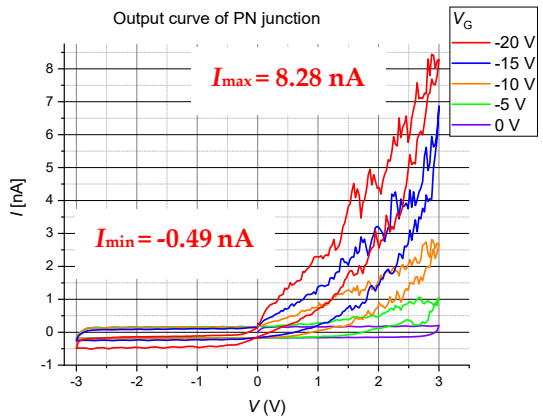

Figure 15: Output curve of PN junction achieved in most employed configuration

This last measurement has been carried out with V ranging from -3 V to 3 V. the application of a gate voltage V_G was made necessary to introduce more p-type carriers since p-type flakes showed poor mobility of holes. This poor conduction might be due to the intrusive fabrication steps, which hinder the continuity of the material. RIE and "hot pick-up", on WSe_2 easily result on cracks, due to the frailty of the material.

A negative gate voltage results in both the p-type band and the n-type band to be pushed upwards, increasing the concentration of holes in the p-type region. This voltage should also hinder the n-type carrier concentration, but n-type carrier density was high enough to retain its n-type behaviour. This can be seen by the junction behaviour. If also the n-type region showed majority of p-type carriers, an ohmic curve would have been present.

A major difference can be seen between this last measurement and the previous one. This last measurement shows hysteresis behaviour between the first current flow and the second one, for the same voltages. The main explanation behind hysteresis is that SiO_2 substrate, present below the junction, shows presence of charges at the interface between SiO_2 and the semiconductor. These charges, probably related to incompletely oxidized Si or dangling bonds, can act as trap levels near the conduction or valence bands for the semiconductor. During sweeps, interface charges are filled and emptied with different relaxation times, resulting in the hysteresis behaviour.

ON-to-OFF current ratio has a value of 16,89.

4. Conclusions

Thickness dependent carrier mobility has been demonstrated. The current densities do not show values as high as most common semiconductors.

To improve current densities, new fabrication mechanisms, less intrusive, could be devised. This would prove extremely useful since flakes, especially thin p-type ones, are frail and easily cracked. For PN junctions, gating was proven necessary in these measurements, due to the poor p-type conduction measured.

This problem could be avoided by doping WSe_2 with acceptors. The choice of the doping material needs to be weighted since F doping was tried and, even though carrier density increased, current density was still in the order of tens of mA/m.

Further testing is needed to develop new fabrication approaches to obtain hole conductivity as high as other experimental results previously achieved.

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