Power Optimization Strategies for the Electronic Control of Photonic Integrated Circuits

Tesi di Laurea Magistrale in
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Abstract

In the last years, integrated photonics has emerged as a promising solution for the transmission and processing of optical signals. In particular, Silicon Photonics technological platform represents a significant option in this direction, since it exploits the traditional microfabrication processes of the CMOS technology to implement photonic integrated circuits with low cost and area occupation. However, the main drawback of Silicon as optical material is its high sensitivity to geometrical fabrication mismatches and temperature variations, that hinder the possibility of open-loop photonic operations. Indeed, the working point of each photonic device needs to be precisely controlled and stabilized to ensure that the overall optical functionality matches the design specifications. To this end, a real-time electronic closed-loop control has to be implemented, by reading on-chip sensors and driving integrated actuators with a suitable feedback law.

The maturity reached by Silicon Photonics has boosted its adoption in the telecommunication commercial field, leading to the realization of increasingly complex photonics systems. The electronic control thus has to address an increasing number of photonic devices on the same chip. A multichannel FPGA-based electronic system, called Helios 3, has been specifically designed in order to handle up to 144 photodetectors and actuators, allowing to control complex photonic structures. The new electronic platform has been designed with a flexible modular architecture, made of a motherboard that is completed by plugin modules that can be reconfigured to change the number and type of sensors and actuators operated on the photonic chip.

Considering the abundant number of channels that need to be driven/acquired, power efficiency becomes a critical aspect. The power supply of the system has thus been realized with an optimized module. The employment of DC/DC converters, with respect to less efficient linear regulators, permitted to avoid the use of bulky benchtop power supplies and efficiently deliver to the system up to 90W from a PC charger. The supply module is connected to the Helios 3 motherboard with vertical connectors, protecting the whole electronic system by EMI generated by the switching regulators. The circuit has been thoroughly tested and validated, verifying its correct design and operation.

Furthermore, a new version of the actuation module has been designed and verified. This pluggable board features 16 actuation channels that can be connected to two types of actuators, i.e. thermal phase shifters specifically targeting the Silicon Nitride platform and the innovative MEMS actuators, that promise to solve the power consumption bottleneck afflicting thermal actuators. The two kind of devices share the need of high operating voltages, therefore a circuit able to correctly drive them has been designed by employing a local high-voltage DC/DC converter. The module has been completely validated, including the VHDL firmare required to operate it with the FPGA.

The complete Helios 3 instrument is now ready to be employed in actual experiments and control cutting-edge photonic structures of relevant complexity, performing advanced optical functionalities.

Keywords: electronic system, integrated photonics, MEMS, Silicon Nitride, modular architecture, FPGA, power electronics.

Abstract in lingua italiana

Negli ultimi anni, la fotonica integrata è emersa come una soluzione promettente per la trasmissione e l'elaborazione di segnali ottici. In particolare, la piattaforma tecnologica Silicon Photonics rappresenta un'opzione significativa in questa direzione, poiché sfrutta i tradizionali processi di microfabbricazione della tecnologia CMOS per implementare circuiti integrati fotonici a basso costo e a bassa occupazione di area. Tuttavia, il principale svantaggio del silicio come materiale ottico è la sua elevata sensibilità agli errori di fabbricazione geometrica e alle variazioni di temperatura, che ostacolano la possibilità di operazioni fotoniche ad anello aperto. Infatti, il punto di lavoro di ogni dispositivo fotonico deve essere controllato e stabilizzato con precisione per garantire che la funzionalità ottica complessiva corrisponda alle specifiche di progetto. A tal fine, è necessario implementare un controllo elettronico ad anello chiuso in tempo reale, leggendo i sensori on-chip e pilotando gli attuatori integrati con un'adeguata legge di retroazione.

La maturità raggiunta dalla fotonica del silicio ne ha favorito l'adozione nel settore commerciale delle telecomunicazioni, portando alla realizzazione di sistemi fotonici sempre più complessi. Il controllo elettronico deve quindi gestire un numero crescente di dispositivi fotonici sullo stesso chip. Un sistema elettronico multicanale basato su FPGA, chiamato Helios 3, è stato appositamente progettato per gestire fino a 144 fotorivelatori e attuatori, consentendo di controllare strutture fotoniche complesse. La nuova piattaforma elettronica è stata progettata con un'architettura modulare flessibile, costituita da una scheda madre che è completata da moduli plug-in che possono essere riconfigurati per cambiare il numero e il tipo di sensori e attuatori operanti sul chip fotonico.

Considerando l'elevato numero di canali da pilotare/acquisire, l'efficienza energetica diventa un aspetto critico. L'alimentazione del sistema è stata quindi realizzata con un modulo ottimizzato. L'impiego di convertitori DC/DC, rispetto ai regolatori lineari meno efficienti, ha permesso di evitare l'uso di ingombranti alimentatori da banco e di fornire al sistema in modo efficiente fino a 90W da un caricatore per PC. Il modulo di alimentazione è collegato alla scheda madre Helios 3 con connettori verticali, proteggendo l'intero sistema elettronico dalle EMI generate dai regolatori switching. Il circuito è stato accuratamente testato e validato, verificandone la corretta progettazione e il funzionamento.

Inoltre, è stata progettata e verificata una nuova versione del modulo di attuazione. Questa scheda collegabile dispone di 16 canali di attuazione che possono essere collegati a due tipi di attuatori, ovvero gli sfasatori termici specificamente destinati alla piattaforma di nitruro di silicio e gli innovativi attuatori MEMS, che promettono di risolvere il collo di bottiglia del consumo di energia che affligge gli attuatori termici. I due tipi di dispositivi condividono la necessità di alte tensioni operative, pertanto è stato progettato un circuito in grado di pilotarli correttamente impiegando un convertitore DC/DC locale ad alta tensione. Il modulo è stato completamente validato, compreso il firmare VHDL necessario per farlo funzionare con l'FPGA.

Lo strumento Helios 3 completo è ora pronto per essere impiegato in esperimenti reali e controllare strutture fotoniche all'avanguardia di notevole complessità, eseguendo funzionalità ottiche avanzate.

Parole chiave: sistema elettronico, fotonica integrata, MEMS, Nitruro di Silicio, architettura modulare, FPGA, elettronica di potenza.

Contents

1 | Introduction

Over the last 70 years, the fabrication process of electronic circuits has been constantly improved, resulting in ever increasing complexity, density, and speed of integrated circuits (IC). As more devices are squeezed into the same silicon area, a problem with metal connections arise: while the transistors on a chip become quicker as the technical dimension reduces, the wires cannot keep the same pace, since their intrinsic resistance and capacitance limit the signal bandwidth. Indeed, aspect ratio of metal lines limits the maximum communication speed, since it can be demonstrated that bit-rate capacitance of a metallic line of cross section A and length L is proportional to A/L^2 [1]. Furthermore, because the operating frequency rises with scaling, total chip power dissipation is almost entirely accounted for by the power required to drive the metallic interconnections.

Using optical links and all-optical signal processors is a good way to bypass these restrictions [2]. In fact, they can operate at greater data rate while using less power than traditional electronics. In addition, photonic devices are less vulnerable to electromagnetic field interference, which may be a concern in electronic communication systems. While photonics has already been employed for long range telecommunications, where fiber optics have completely superseded coaxial cables, the adoption of this technology for short distance interconnections requires the integration of optical devices in compact chips, possibly exploiting currently existing manufacturing process, to reduce cost and size and become attractive over the more traditional electronic components.

Because optical qualities are as important as electrical ones, many integrated solutions, each with advantages and disadvantages, have been proposed, including Silicon Nitride, Indium Phosphide, Lithium Niobate, and, of course, Silicon. Over the last decade, Silicon Photonics (SiP) has become one of the most important technological platforms for photonic integrated circuits (PICs) [3]. Primarily, it owes its success to competitive optical properties obtained with a CMOS-compatible fabrication process. However, these features come at the price of a high sensitivity of silicon photonic devices to temperature variations and fabrication geometrical mismatches, that can impair stand-alone PIC functioning.

In the last years, the realization of closed-loop electronic systems, able to compensate the structural defects and stabilize each device in different thermal conditions, has enabled the operation and control of complex Silicon Photonics structures. As a result, the scale of photonic circuits has increased, requiring improved control mechanisms to fully leverage the capabilities of Silicon Photonics.

1.1.   Silicon Photonics

In addition to CMOS compatibility, Silicon presents significant optical properties: Silicon transparency window extends in the Infrared spectrum region, from 1000 nm to 7000 nm, including typical optical telecommunication bands, i.e. O-band ($\lambda = 1300nm$) and C-band ($\lambda = 1550nm$). Today, Silicon Photonics products are built on Silicon-on-Insulator (SOI) wafers: because of the high refractive index contrast ($\Delta = \frac{n_{Si}-n_{SiO_2}}{n_{Si}} \simeq 0.6$) produced by the combination of Silicon (n_{Si}=3.45) and Silicon Dioxide (n_{SiO_2}=1.45), it is possible to design waveguides with a very tiny footprint and a short bending radius.

1.1.1.   Waveguides

Waveguides are the fundamental structures that transmit light around a photonic chip. SOI waveguides are typically built with a slightly p-doped Silicon core surrounded by SiO_2 cladding, allowing to exploit total reflection and entrap the light inside them with low loss (around $2 \sim 3db/cm$). Different waveguide designs are employed depending on their applications: the buried format (Fig. 1.1aa) is utilized for optical routing, while the rib shape (Fig. 1.1ab) with lateral Si slabs allows for the deposition of metal electrodes, employed in electro-optic devices. Inside this optical structure, travelling modes could be attenuated by scattering losses associated with sidewall roughness and local defects. Indeed, it is possible to describe the propagated electric field inside a waveguide of length L with the following expression:

$$E = E_0 \cdot e^{-j \cdot \Delta\phi} = E_0 \cdot e^{-j\frac{2\pi \cdot L_{opt}}{\lambda}} \cdot e^{-\alpha \cdot L} \tag{1.1}$$

where $\Delta\phi$ represents the phase accumulated by the light after an optical path L_{opt} defined as:

$$L_{opt} = L \cdot n_{si} \tag{1.2}$$

and λ is the wavelength, α the absorption coefficient of the waveguide, n_{si} the refraction coefficient of silicon.
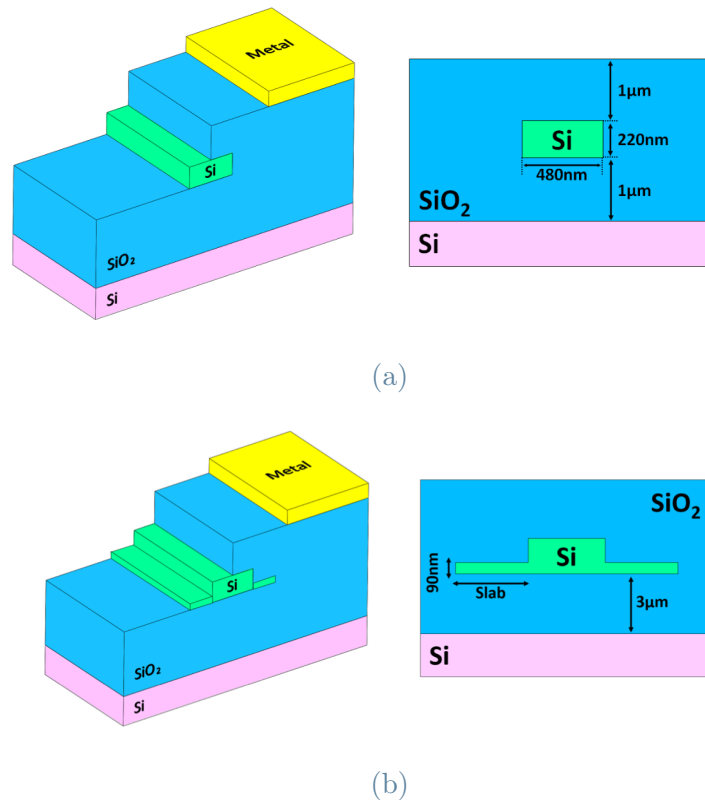
(a)

(b)

Figure 1.1: 3D view and cross-section of buried (a) and rib (b) waveguides with typical geometrical specs

1.1.2. Directional Coupler

The ability to split or combine two or more guided optical fields is a necessary prerequisite for creating components with more sophisticated functionalities than waveguides. In integrated optics, the directional coupler is the basic component to perform this operation. As indicated in Fig. 1.2, the directional coupler has four ports and it is constituted by two waveguides, completely decoupled in proximity of the inputs and the outputs, that are coupled in the central region of length L_c. Power coupling between the two waveguides is possible thanks to the interaction with the evanescent field of the propagating signals, so that light pulses can be transferred from one waveguide to the other.
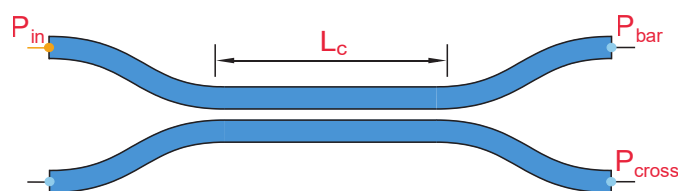

Figure 1.2: Schematic view of a directional coupler.

If the two waveguides are perfectly identical, i.e. they support the same fundamental mode, the directional coupler is *synchronous* and the relation between P_{bar} (power that comes out of the same waveguide of the input) and P_{cross} (power exiting from the coupled waveguide) can be described as:

$$P_{bar} = sin^2(k \cdot L_c) \tag{1.3}$$

$$P_{cross} = cos^2(k \cdot L_c) \tag{1.4}$$

where k is the *coupling coefficient* of the device. This parameter depends on component design choices, i.e. the gap between the waveguides or their shape. As equations (1.3) and (1.4) highlight, the transfers function are periodic and the complete power transfer is possible for $kL_c = \frac{\pi}{2} + N\pi$. The most common directional coupler used in integrated optics is the *-3db coupler* which allows to equally split the input light power to the output waveguides ($kL_c = \frac{\pi}{4}$).

1.1.3.   Mach-Zehnder Interferometer

The Mach-Zehnder interferometer (MZI) is the most basic filter that can be constructed in integrated optics [4]. It features a sinusoidal transfer function, which is not ideal for filtering WDM (*Wavelength Division Multiplexing*) channels, but it provides the basis for creating amplitude and phase filters with good spectral properties. This filter is implemented by two -3db directional couplers, linked by two waveguides with different optical path L_{opt}: the phase shift $\Delta\phi$ introduced in this region determines the interference at the output directional coupler and therefore the power ratio at the two outputs. As depicted by Fig. 1.3 and 1.4, the phase shift $\Delta\phi_{MZ} = \phi_1 - \phi_2 = \frac{2\pi}{\lambda} \cdot \Delta L_{opt}$ can be obtained by waveguides of different length ($\Delta L_{opt} = n \cdot \Delta L$) or waveguides of same length and different refractive index ($\Delta L_{opt} = \Delta n \cdot L$).

Employing the same terminology of the directional coupler, the two output powers can be described by:

$$P_{bar} = sin^2\left(\frac{\Delta\phi_{MZ}}{2}\right) \tag{1.5}$$

$$P_{cross} = cos^2\left(\frac{\Delta\phi_{MZ}}{2}\right) \tag{1.6}$$

As made evident by the two equations, the transfer function of a MZI is really similar to that of a directional coupler, however, while for the latter the periodicity is proportional to the kL_c, for a MZI it is proportional to ΔL_{opt}. This relation makes MZI more robust and controllable than a directional coupler: indeed, MZI can be considered a photonic tunable device since it's possible to modify the optical path unbalance, thus changing the
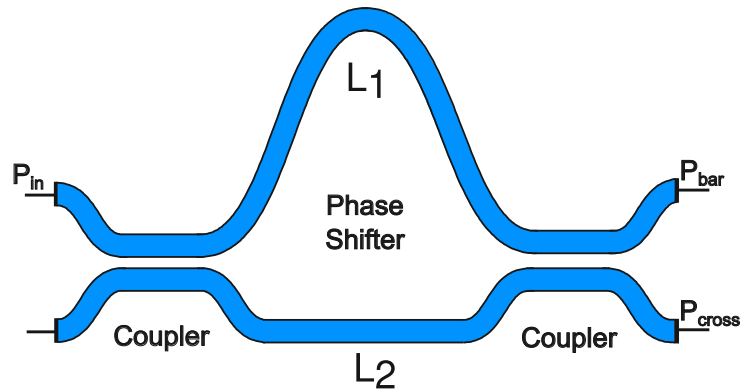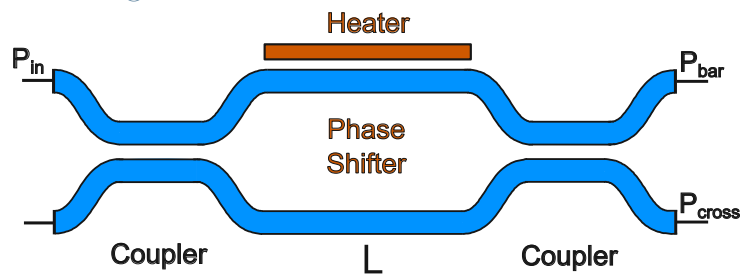
Figure 1.3: Geometrical unbalanced MZI

Figure 1.4: Tunable MZI with thermo-optic actuation mechanism

filter transfer function, by acting with some type of actuation mechanism.

1.1.4. Ring Resonator

Ring Resonator (RR) is another typology of integrated photonic device that implements a Infinite Impulse Response (*IIR*) filter. As shown in Fig. 1.5a, the ring is built with a circular waveguide and two directional couplers, that allow the coupling with the input and output waveguides. The four ports of the device are *In*, *Add*, *Through* and *Drop*. The functioning principle is pretty straightforward: if the input signal wavelength is an integer sub-multiple of the ring circumference (resonance condition), the light couples to the ring and exits from the *Drop* port, otherwise it propagates towards the *Through* port. The *Add* port can be used to add another signal to the *Through* port, always respecting the condition of resonance: with this configuration, the ring resonator acts as *Optical Add Drop Multiplexer* (*OADM*) [5]. If the Drop waveguide is not present (Fig. 1.5b), the ring resonator performs a notch filtering: in this case, the resonating signal is entrapped inside the ring and dissipated by its losses, due to the tight bending radius of the ring.

The optical response of the device is periodic since the resonating condition occurs when the input wavelength is an integer sub-multiple of the ring optical path. Therefore, figures of merit to describe the performance of this filter are the *Free Spectral Range* (*FSR*), i.e.

the distance between two consecutive resonating frequencies, and the *Finesse* (F), i.e. the ratio between *FSR* and bandwidth of the filter, which gives measure of the filter selectivity.

As with the MZI, actuation mechanisms can make the ring resonant frequency tunable and enable advanced operations, such as tunable delay lines [6] (Fig. 1.6): signals can be delayed by a chain of ring resonator since they have to complete multiple roundtrips before reaching the output waveguide. The more the rings are locked on one resonating frequencies, the more the delay adds up.
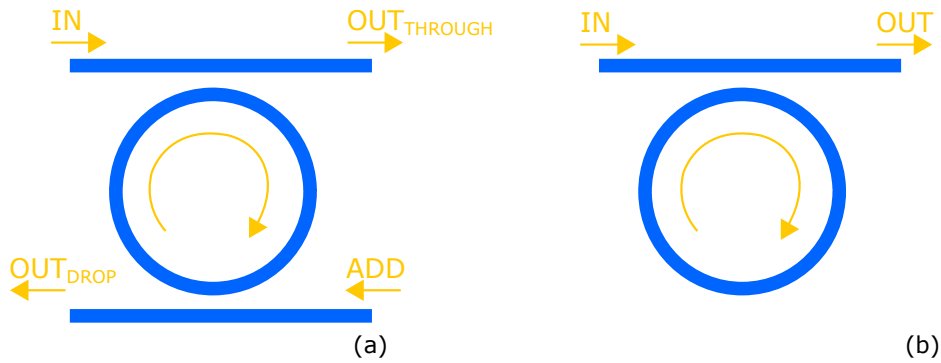

(a)   (b)

Figure 1.5: Ring resonator as a) OADM and b) Notch filter
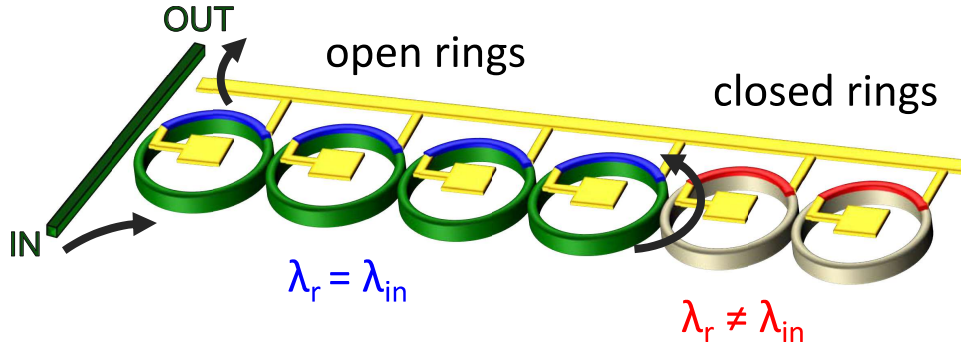

Figure 1.6: Tunable delay lines with 4 locked rings.

1.2.   Electronic control of PICs

As pointed out before, Silicon Photonics devices have to be tuned in order to accomplish their theoretical purpose or to modify their functionality at run-time [7]. Fabrication imperfections and thermal instabilities can cause shifts of spectral response, if centered around $\lambda = 1550nm$, in the order of 1 nm for 1 nm geometrical mismatch or 10 K temperature change [8]. In order to assess the behaviour of a certain PIC during its operation,

sensors need to be placed in the most suitable parts of the chip. The information acquired in this way can then be used to perform a closed-loop control action, by properly driving on-chip actuators so that the chip behaviour matches a certain set-point [9]. The simplified scheme of the control loop is illustrated in Fig. 1.7.
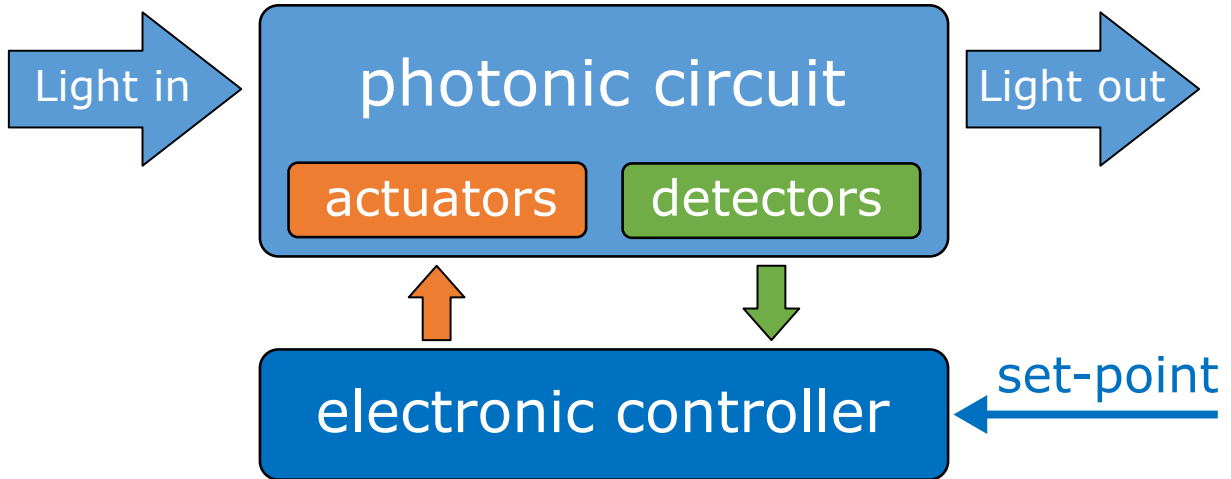

Figure 1.7: Schematic view of the closed-loop control

The electronic control layer can be exploited to:

- Stabilize the photonic components in temperature-varying working environments.

- Tune the device in order to compensate fabrication geometrical defects.

- Completely reconfigure the interferometric devices (*MZI, RR*), to dynamically change the functionality of a photonic chip.

The most common sensors, actuators and control techniques are described in the following sections.

1.2.1.   Sensors

Because of their simple integration with SOI technology process, Germanium photodiodes are the most common on-chip sensors, capable of extracting the information of the working state of photonic devices with good sensitivity [10]. Germanium is a really good candidate for implementing sensors in Silicon Photonics since it's a good absorber along the C-band: the small energy gap of this material translates in fact into a responsivity around $1A/W$ at 1550 nm, that leads to the generation of large electrical signals easy to be detected.

Obviously, the number and placement of photodiodes in a PIC have to be tailored to the specific application, since each detector absorbs part of the travelling optical power. In this

sense, the sensors are conveniently positioned on the unused branch of the interferometric components, in order to not extract too much light from the photonic circuit. Similarly, the amount of employed photodiodes has to be limited to the minimum needed to correctly monitor the state of the PIC.

1.2.2.   Thermal actuators

As mentioned before, the main photonic devices are interferometric, therefore the desired optical response is obtained by controlling the relative phase difference accumulated by two light beams that are travelling on different branches. In Silicon, this phase difference $\Delta\phi$ is directly dependent on the temperature at which the device is operating, since the Silicon refractive index is highly temperature sensitive [11], as shown by the expression of the thermo-optic coefficient (TOC):

$$TOC = \frac{\partial n}{\partial T} = 1.86 \cdot 10^{-4} \quad [1/K] \tag{1.7}$$

This could be considered a drawback because an external control mechanism is required to steady the device. At the same time, this property is exploited to actively manage the operating point of MZIs or RRs, using a closed-loop electrical system, opening the possibility to realize tunable and reconfigurable PICs.

Thermal actuators, typically called *heaters*, are therefore integrated close to the waveguides to define the behaviour of photonic devices. They are usually titanium resistors, with a typical resistance of hundreds of Ohm ($200 \simeq 400\Omega$), deposited at a distance of around 700 nm from the core, to minimize the interaction between the metal and the evanescent field of light. Due to the Joule effect, these actuators heat up when driven by a voltage, locally altering the refractive index and thus regulating the phase shift of the travelling modes. To thermally isolate a piece of the circuit and increase heater efficiency while reducing thermal cross-talk, several foundries currently provide the option of excavating deep trenches in the SiO_2 cladding.

This approach, although being straightforward, has some of problems. The most obvious one is that a single heater uses a significant amount of power (a few mW to tens of mW) to run. Hence, the promised power-efficient solution for short link communications cannot be achieved with photonic circuits that rely on heaters. A lot of research is being put into the investigation of new actuation mechanism to get around the criticalities mentioned. Fig. 1.8 depicts a visual comparison of available tuning methods in terms of feasibility for use in large-scale PICs, showing that optical efficiency of power-hungry heaters could be also mimicked by other type of actuators, such as MEMS actuators.
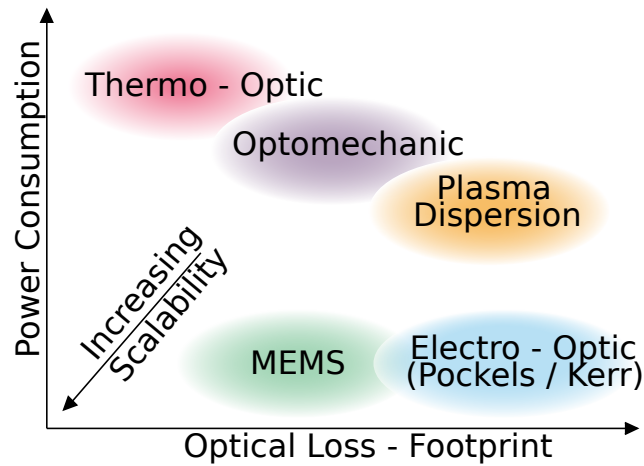
Figure 1.8: Tuning mechanism comparison from a scalability perspective

1.2.3. MEMS actuators

Optical micro electro-mechanical systems (MEMS) are a potential category of devices that could solve the aforementioned problem of power dissipation of thermal actuators. MEMS rely on electromechanical actuation to cause a change in the optical characteristics of a waveguide, with low power dissipation [12]. Recalling equation 1.1, the propagation of a guided mode can be modified by acting on the refractive index of the waveguide or on the absorption of the optical material. In this sense, MEMS actuators perform a modification of these two parameters with the following mechanisms:

- Because compressive and tensile strain affect both parameters, a tunable phase shifter may be realized using a single waveguide subject to mechanical forces [13].

- Displacement or approach of a piece of waveguide to the one where light is travelling can also induce a modification of refractive index, and it is therefore the most common way to realize tunable directional couplers [14].

Generally, the displacements induced by MEMS actuators are in the order of tens of nanometers to tens of micrometers, obtained with *electrostatic* or *piezoelectric* mechanisms [15]. Both the actuator types are driven by an electric field applied to two electrodes, without consuming of any static power.

The most popular MEMS actuators are electrostatic actuators. They exploit the attractive force between charged plates of a capacitor, where at least one plate is free to move to achieve displacement. This attractive force is counterbalanced by a mechanical spring force, so that in equilibrium conditions a fixed displacement dependent on the potential difference is obtained. As depicted in Fig.1.9, the two most prevalent capacitor shapes
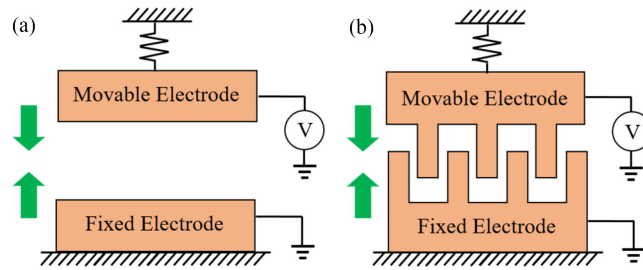
Figure 1.9: Electrostatic actuators schematic view: a) Parallel plate and b) Comb drive electrodes
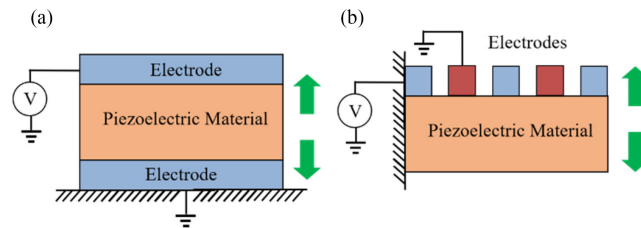

Figure 1.10: Piezoeletric actuators schematic view: a) Sandwiched electrodes and b) Coplanar electrodes

are *parallel plate* and *comb drive* configurations.

Piezoelectric actuators rely instead on the piezoelectric effect, which occurs when a voltage is applied across a piezoelectric material causing strain: in both the electrodes geometries shown in Fig. 1.10, the strain is generated in the horizontal direction, but, since the materials are laterally confined, they stretch vertically.

The adoption of these two types of actuation requires to face some challenges. Regarding the electrostatic actuators, the fabrication of high-aspect ratio structures in SOI is difficult to obtain, making it hard to use comb-drive electrodes without employing complex manufacturing processes. On the other hand, the integration of piezoelectric material in the SOI stack is difficult since complex fabrication steps are required. Furthermore, both architectures require high voltages to obtain relevant phase shifting properties: couplers and switches have a wide range of actuation voltages, from 5 V for devices based on cavities to the more popular range of 30 to 50 V for large waveguide structures. Such high voltages need specialized electronics to be handled. Luckily, the very low current needed to drive the actuators simplifies the electronic design.

1.2.4. Dithering Technique

The sensors and actuators described in the previous paragraph are the interface between electronic and photonic domain. To close the control loop, the information acquired with

the sensors needs to be translated into an operating voltage for the actuators. There are several approaches that can be used for this purpose, one of the most commonly used being the dithering technique.

The dithering technique is a control algorithm that permits to simultaneously tune and stabilize complex photonic systems [16]. It exploits a small modulation of the actuators voltage to retrieve the information of first derivative of a photonic device transfer function. This quantity can be advantageously used to lock an optical component in the stationary points (maximum or minimum) of its transfer function without the need of prior calibration procedures, a relevant advantage when the optical complexity scales up. Indeed, the power at the output of any device can be maximized or minimized by driving to zero the dithering information, regardless of the absolute amount of light in the system.
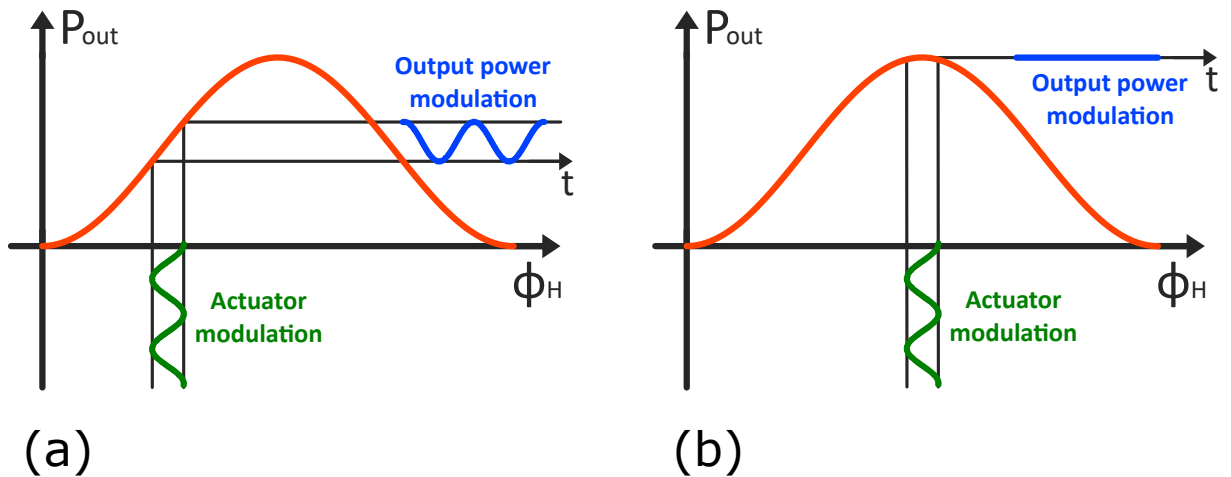

Figure 1.11: Theory of operation of the dithering approach. A modulation of the actuator signal causes an oscillation in the output power whose amplitude depends on the derivative of the transfer function of the device under investigation. The output power modulation depth is maximum on the device slope (a) and zero in stationary points (b).

Principle of operation

The dithering technique is accomplished by adding a small and slow sinusoidal signal (usually in the kHz range) to the actuation voltage delivered to the actuators. As shown by Figure 1.11, a modulation of the phase shift applied to a photonic interferometric device translates into a modulated output optical power. The modulation depth depends on both the amplitude of the sinusoidal signal and on the slope of the transfer function around its bias point. Indeed, the output power can be written as:

$$P_{OUT} = P_{OUT}(\Phi_{H,BIAS}) + P_{dith} sin(2\pi f_{dith} t) \tag{1.8}$$

where

$$P_{dith} = \Phi_{dith} \cdot \left. \frac{\partial P_{OUT}}{\partial \Phi_H} \right|_{\Phi_H = \Phi_{H,BIAS}} \tag{1.9}$$

and Φ_H is the phase shift induced by the actuator, $\Phi_{H,BIAS}$ is the initial bias phase shift, Φ_{dith} and f_{dith} are the amplitude and frequency of the dithering signal, respectively.

The output power is then sensed with a photodetector and the modulated information is extracted with the lock-in technique, by demodulating the acquired signal with a reference at f_{dith}. This information is then used to modify the actuator bias point until P_{dith} is zeroed, thus reaching the desired stationary point. Maxima and minima can be both targeted simply by inverting the sign of the acquired dithering signal, since the lock-in readout maintains the sign of the derivative information.

1.3.   Other photonic technologies: Silicon Nitride

While Silicon Photonics has become the main technology platform for PICs, potential alternative compounds that meet the same essential requirements as the SOI stack, i.e., high index contrast and CMOS integration, are being investigated with growing interest [17]. There are a number of reasons why SOI may not always be the ideal choice for device functioning and performance, one of the main being the need to operate in spectral regions where silicon or silicon oxide are absorbers.

Silicon Nitride (Si_3N_4, SiN) is a significant option in this regard since it features a moderate index contrast ($\Delta \simeq 2$) and it can be manufactured with CMOS-compatible processes [18]. In addition, as depicted in Fig. 1.12, this material is transparent throughout the majority of the visible spectrum up to the mid infrared (2.3 μm), thus extending the range of wavelengths that can be employed as compared to Silicon Photonics. Moreover, SiN can be grown on silicon wafers that are cheaper than the SOI ones, making the material more cost-effective for some photonic applications.

The medium-high refractive index contrast is also an excellent compromise between PIC design compactness and power loss due to scattering effects and absorption. Indeed, the medium refractive index contrast of SiN reflects into waveguides with larger bend radius ($\sim 75\mu m$) and width ($\sim 1.2\mu m$) as compared to SOI waveguides, that usually
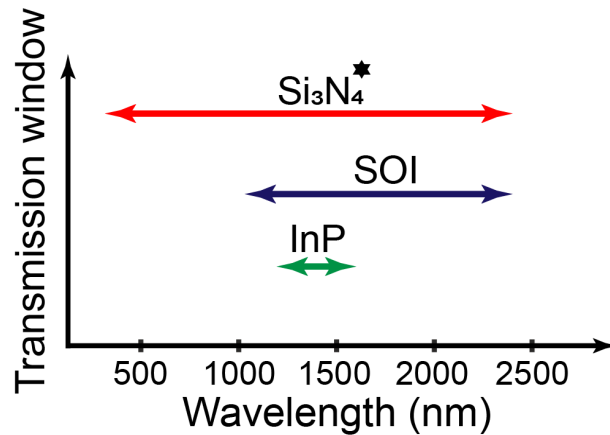
Figure 1.12: Transparency window for typical photonics technologies

feature $\sim 5\mu m$ radius and $\sim 450nm$ width. On the other hand, power losses are directly proportional to $\Delta n^2 = \Delta n_{core}^2 - \Delta n_{cladding}^2$, making SiN an excellent low-loss material $(\alpha_{dB} \simeq 1db/cm)$ [19].

Silicon Nitride waveguides also feature a TOC roughly one order of magnitude smaller than Silicon Photonics. This property is exploited to manufacture photonic chips that are less sensitive to thermal variations and therefore require simpler electronic control. However, when the chip functionality needs to be tuned by means of thermal actuators, a larger current budget is needed to effectively change the refractive index. Indeed, the same refractive index change is obtained with a $\sqrt{10}$ times larger current than in Silicon Photonics, thus requiring to carefully design the driving electronics. In the next chapters, an actuation module for SiN heaters and MEMS actuators is proposed, taking into account the current requirements of SiN and the high driving voltages of MEMS devices.

2 | Hardware control system

As previously stated, photonic chips don't operate as stand-alone devices: an electronic system has to be used to implement a closed-loop control and to stabilize the functioning of each photonic component. Indeed, shifts in the frequency response, caused by temperature variations and fabrication defects, have to be monitored and compensated in real-time.

In this chapter, the overall electronic system, which main goal is to monitor the optical circuitry and tune it into the specific operating regime, is described. It is possible to summarize the complete architecture with the following scheme:

- **Electronic front-end**: it is implemented on a interface board in order to ease the connection between photonic chips and electronic system. It provides a first amplification of the photodetector signals and the electrical connections to the chip.

- **Read-out chain**: the signals coming from the analog front-end are further amplified by Programmable Gain Amplifiers, filtered and digitally acquired by ADCs.

- **Digital signal processing**: an FPGA is the digital core responsible for implementing the closed-loop control law. It realizes the filtering and processing of the acquired information and generates the control signals to minimize the functionality errors of the photonic components. Furthermore, it handles the communication between user (personal computer) and electronic system.

- **Actuation chain**: it handles the driving of the different actuators, principally *heaters* and MEMS structures. This chain translates the digital command given from the FPGA into driving voltage waveforms (DC or modulated signals) through the use of DACs, while the driving voltage dynamics is adjusted by fixed-gain amplification stage.

- **Power supply**: a part of the system is dedicated to supplying the platform and the FPGA. It has both to manage the powering of all the system components and to provide enough current to correctly drive the thermal actuators.

In the next section, the third version of the electronic system, called Helios 3, is presented

(Sec. 2.1). Helios 3 enhances the functionalities and corrects faults of the previous versions, coping in particular with the increasing number of photonic devices that need to be controlled. In order to make the system more flexible to different applications and measurements, a modular structure has been conceived and the different module architectures are introduced in the last section (Sec 2.2) of the chapter.

2.1.   Helios 3 architecture

As already mentioned before, a modular structure has been designed in order to guarantee easy electrical and optical accessibility to the photonic chip. Indeed, placing the photonic chips directly onto the main electronic control board is unpractical. First, the coupling of light with optical fibers and the wire-bonding needed to provide electrical access to the chip are hard to implement if the size of the electronics increases. In addition, gluing the photonic chip directly on the main electronic board makes it hard to test different chips designed for different experiments. The proposed solution is the adoption of an interface board, which permits the optical fiber coupling and guarantees the connection between electronic system and photonic chips.

2.1.1.   Host PCB

Mantis, as colloquially called, is the dedicated host board, employed to interface the electronic circuitry with the optical setup. The module hosts the photonic chip and an analog front-end which reads and pre-amplies the signals coming from the photodetectors. The analog front-end is positioned as close as possible to photonic chips in order to minimize the impact of stray capacitances and retrieve an accurate measurement of the incoming signals. Furthermore, the tiny dimensions of the board ease the coupling with the optical fibers that interacts with the optical circuitry.

The host PCB allows also to add a Peltier cell beneath the chip to manage the overall temperature of the system. In order to analyze temperature of the chips as precisely as possible, a commercial thermistor is put immediately next to it. The board is then mounted atop a metal holder, which serves as both a mechanical support and a heat sink. The other electronic components are housed on a separate and bigger motherboard that is linked to the host board through shielded connections.
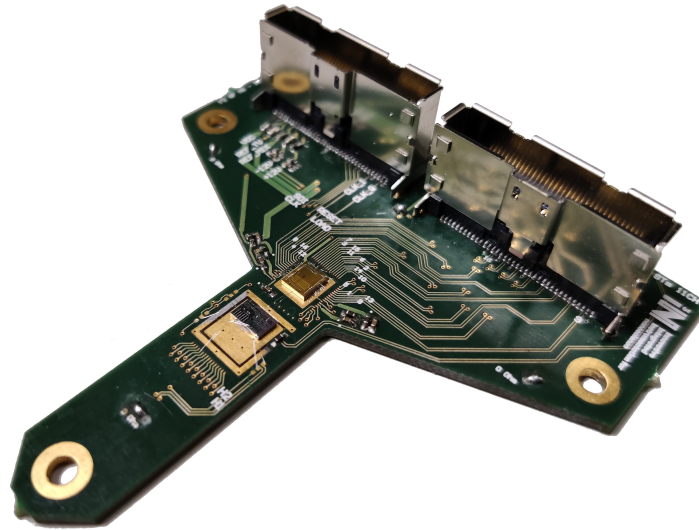
Figure 2.1: Photograph of the interface board Mantis

Photodiodes Front-end

Commercial TransImpedance Amplifiers (TIA) usually accomplish the pre-amplification of signals from photodiodes. As mentioned in the previous chapter, Germanium detectors feature an high sensitivity to the telecommunication wavelengths, hence an high current signal is produced. A resistive-feedback TIA is normally employed in order to translate the photodiode generated current, which it can be a DC value or modulated at few kHz, into a voltage.

2.1.2. Motherboard

In previous versions of the Helios system, all the electronic sections explained in the introduction have been implemented into the same board. An intrinsic limitation to the number of acquisition and actuation channels was posed due to the PCB area required by these different sections. Hence, the increasing complexity of the photonic chips, requiring an increase amount of acquired and driven signals, has brought to reinterpretation of the whole electronic system: a modular architecture has been adopted in order to fit a larger number of channels, with the possibility of reconfiguring the electronic control to address several applications.

The new Helios 3 motherboard is represented in Fig. 2.2 and it accommodates:

- the FPGA, on the right, mounted on a commercial module; it programs the components of the system and is in charge of the Digital Signal Processing (DSP) required to control photonic devices.

- six PCI Express connectors for the plug-in expansion modules.

- the connectors which interface with the optical setup; in particular, on the left, the connectors towards the host board and, on the upper and lower sides, auxiliary SMAs.

- some specific acquisition circuitry for the read-out of bench-top photodiodes.

The specific read-out circuitry present onto the motherboard requires 24 out of 144 digital pins available on the FPGA to be handled. The remaining amount of digital pins is dedicated to the control of the external modules. The central part of the top layer is thus dedicated to the routing of the digital links from the FPGA to the expansion connectors: impedance-matching techniques have been adopted in the layout of these tracks, since high frequency clock signals need to be routed correctly without reflections and interference.

Figure 2.2: Photograph of the Helios 3 motherboard

The left side of the board features a set of six 64-position PCI Express connectors into

which the various functional modules of the system are plugged vertically. Each slots provides 24 analog pins, 16 digital pins, 4 power supplies and several ground pins to prevent crosstalk between the signal lines. Furthermore, analog lines and digital lines are well isolated since they are located on opposite layers. A total amount of 144 analog channels interface with the host board, while 96 digital pins exploit the full capability of FPGA.

The expansion modules have been designed in order to satisfy different requirements of the whole electronic system. So far, two pluggable module have already been realized:

- an acquisition module for the read-out of the signals coming from the host-board front-end circuitry. The incoming signals are further amplified and filtered on the module in order to match the voltage dynamics of the ADCs, which then digitize the sensor information.

- an actuation module able to drive SiP thermo-optic actuators.

To further expand the capability of the platform, Chapter 4 describes the design of an additional actuation module, able to drive SiN thermo-optic actuators and MEMS actuators which require different current and voltage dynamics with respect to the standard SiP heaters.

Power supply circuitry is not included onto the motherboard. Instead, an external module has been implemented in order to power up the whole electronic system. A deep analysis of this module is carried out in Chapter 3, describing the generation of the different supply voltages required by the motherboard and external modules circuitry. This reference voltages are $\pm 6.5\,\text{V}$ and $\pm 13\,\text{V}$, which are delivered to the components on the motherboard and the pluggable modules via power planes present on two different motherboard layers. The power planes have two replicas, which feed the upper/lower parts of the motherboard and the three upper/lower external modules. A few Low DropOut (LDO) regulators are also used filter and provide stable power supplies to the dedicated circuitry implemented directly on the motherboard.

2.1.3. FPGA

A *Field Programmable Gate Array* (FPGA) is the digital core of the electronic system. This component has been chosen in order to efficiently control the large amount of mixed-signal devices on both the motherboard and the expansion modules and to provide re-configurability to the whole system. Indeed, an FPGA provides the required versatility to handle different configurations/sets of pluggable modules employed to address various

applications, measurements and experiments.

The FPGA was not directly embedded into the motherboard in order to ease the layout phase and to facilitate the connection with a computer. The commercial platform Opal Kelly XEM7310 was selected. It presents the following features:

- Xilinx Artix-7 FPGA.

- Bootable serial flash memories (2 x 16MB) to store device firmware and configuration settings.

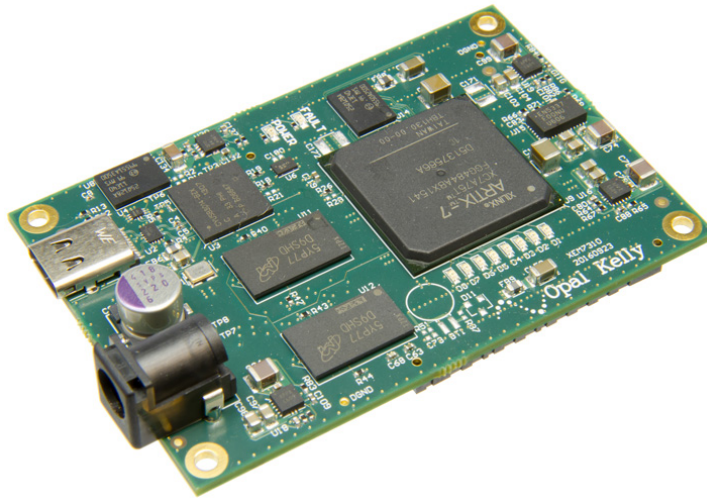- USB 3.0 interface that permits the communication with a computer.

Figure 2.3: Opal Kelly XEM7310

2.2.   Pluggable modules

As already mentioned in the previous section, specific expansion modules can be plugged into the motherboard to expand its functionalities and adapt the system to several photonic circuit configurations. In the following sections, the two modules already developed are introduced, while the power supply and another pluggable module are deeply explained in the last two chapters of this thesis.

2.2.1.   Photodiodes acquisition module

The acquisition module has been designed for the read-out of Germanium photodiodes. The module receives from the host board 16 signals in parallel, that need to be further amplified, filtered and digitized. If the motherboard slots are occupied by only these

modules, Helios 3 can be used to acquire up to 96 incoming signals, even though without the possibility of driving any actuator.

As already mentioned before, a front-end transimpedance amplifier is placed on the interface board, to collect the current generated by the sensors, which is proportional to the light intensity, and convert it into voltage. This operation could be done directly on the acquisition module, however placing the front-end as close as possible to the sensors allows to maximise the measurement resolution by reducing the effect of parasitics caused by connections between photonic chip and electronics. The acquisition module thus has to process the voltage signal generated by the TIAs.

Three main considerations were taken into account during the design of this module:

- The module needs to have a programmable gain, in order to adapt the dynamics of the voltage signals coming from the host board to the dynamics of the analog-to-digital converters responsible for the digitization.

- The signals to be acquired are in a frequency range from DC to 50 kHz, therefore the ADC sampling frequency should be high enough and the antialias filter should not affect the readout.

- Despite 24 analog channels can be routed to the PCIe connector, the number of read-out chains is limited to 16 by the available digital pins, since they have to be employed for the selection of the programmable gain and for the communication between FPGA and ADCs.

The module is thus made of eight 2-channel PGAs and two 8-channel data-acquisition systems (DAS), including both the antialias filter and the ADC. The 3 bits of each PGAs are programmed with six 8-bit shift registers, connected in daisy chain configuration to reduce the number of digital signals required to operate them. The 16 ADCs instead communicate with the FPGA with two data lines, by time-multiplexing the communication among 8 channels each.

2.2.2. SiP actuation module

In order to drive the thermo-optic actuators integrated in Silicon Photonics technologies, a 24-channel actuation module was designed. The purpose of this module is to deliver the correct voltage bias to the heather, with the possibility of superimposing some dithering signals at frequencies of few tens of kHz. If the motherboard was set up with only this kind of module, up to 144 actuation actuators could be driven with Helios 3, with the possibility of acquiring only the signals from the bench-top instruments. In the design
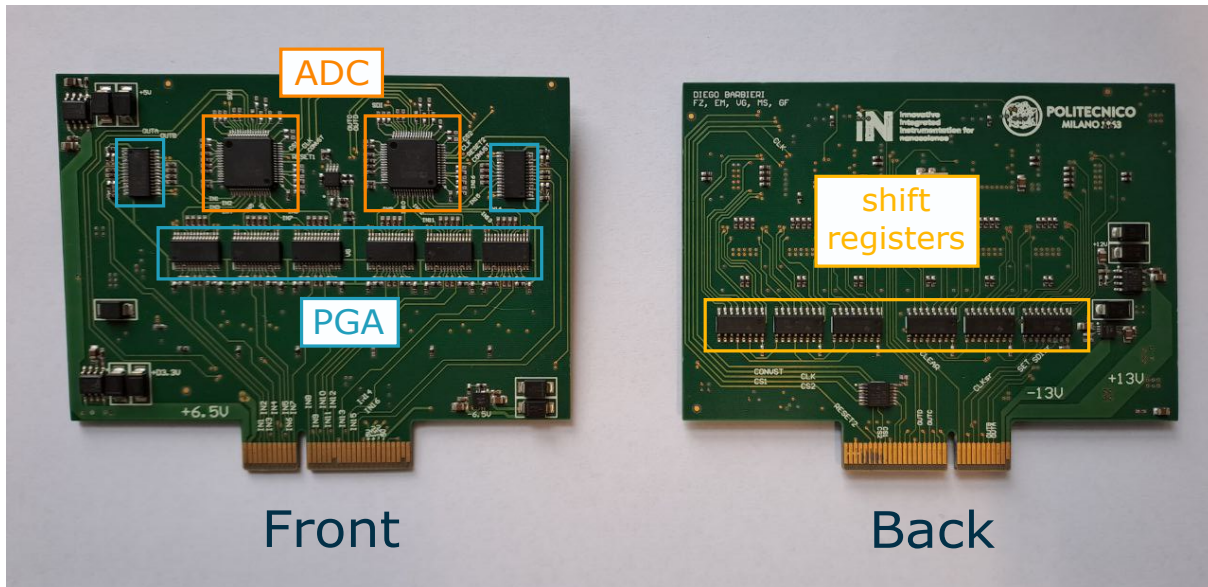
Figure 2.4: Structure of the photodiodes acquisition module.

phase of the power supply module, this particular configuration has been considered as the most power consuming one and the power budget of all the system has been computed taking into account these large current requirements.
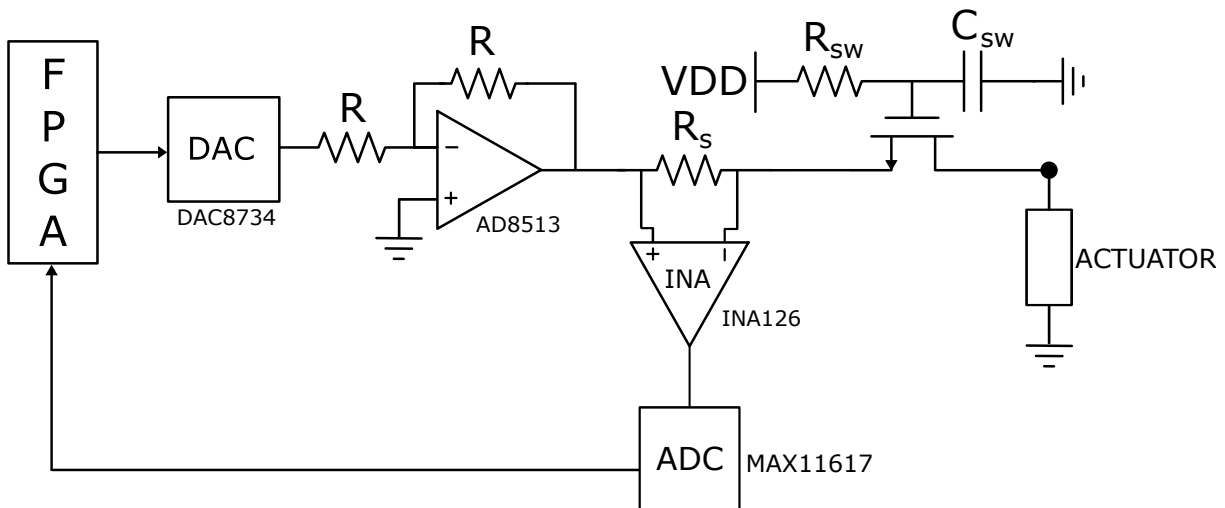

Figure 2.5: Schematic view of the actuation chain for SiP heaters

The module architecture is shown in fig. 2.5. Each chain features a 16-bit DAC able to generate voltage signals with a ±10V bipolar output range, when powered with a ±12V bipolar power supply. A current driver is used in buffer configuration in order to deliver to the heaters the correct amount of current (up to 30 mA), that cannot be provided directly by the DACs. 6 DACs and 6 drivers, both in a 4-channel configuration, are employed to drive 24 channels in total.

A monitoring circuit is placed before the output node in order to sense the current that is flowing towards the SiP heaters. To this aim, the voltage drop across a small shunt resistor in series to the actuators is amplified by an Instrumentation Amplifier (INA) stage and digitized with an ADC. The use of 2 12-channel ADCs allows to monitor the current of all the module channels in parallel.

Finally, a protection switch connects the circuit to the actuator only when the power supply of the module is stable. The transient is handled by an RC network that turns on the switch a few hundreds of ms after the switch-on of the whole instrument.

Taking a cue from the actuation chain of this module, a new version dedicated to generate actuation signals also for SiN heaters and MEMS actuators is proposed in Chapter 4.

3 | Power supply module

3.1. Introduction

This is chapter is dedicated to the hardware description of the power supply module, designed to generate all the voltages required by the motherboard and the several pluggable modules. As already mentioned before, the amount of power needed by the complete instrument has risen in proportion to total number of components and channels. For this reason, the requested power cannot be handled by linear regulators (LDOs) because of their high inefficiency.

It becomes clear that the power supply system has to be managed by DC-DC regulators. The dedicated circuitry has been arranged on a specific module, not directly integrated on the Helios 3 motherboard. Since the switching noise of the regulators could affect the signals controlling the external modules and thus the quality of the control action, it was decided to connect the power supply board right over the Opal Kelly development platform, away from the most sensitive analog signals.

The power supply board is designed to accept a DC input voltage of 19V from an external power supply. This external voltage is generated by an AC adapter without the use of any top bench power supply, making the operation of Helios 3 simple. Finally, DC-DC regulators operate a down conversion in order to generate the voltages required by the system. LDOs are properly placed on the motherboard and modules in order to filter out the switching noise and provide a clean power supply. The simplified supply scheme is depicted in fig. 3.1.

In the following sections, the power requirements of the overall system are assessed and the adoption of switching regulators is explained (Sec 3.2), the power supply board is described (Sec 3.3), and finally the module is validated (Sec 3.4).
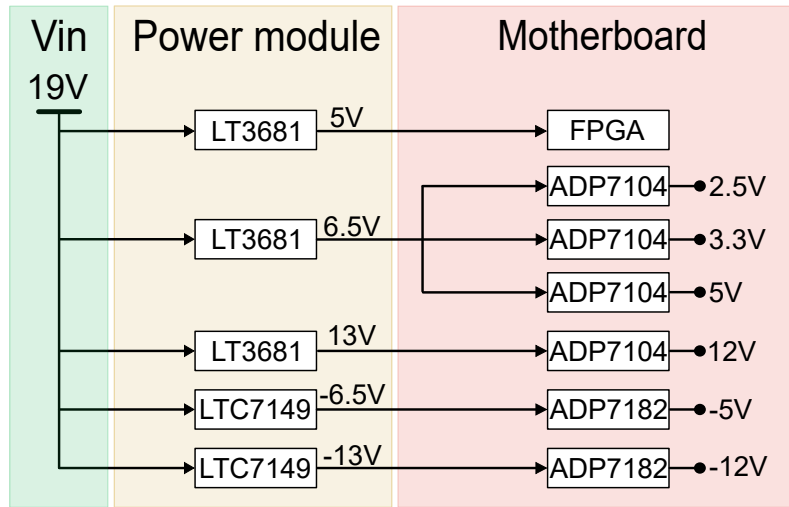
Figure 3.1: Tree diagram of the distributed power supply adopted in Helios 3 platform, from the input voltage of 19V coming from an external power supply (e.g. laptop charger) to the motherboard power supply.

3.2. Design guidelines and power budget

As already stated in Chapter 2, the electronic platform Helios 3 has enhanced the capability of FPGA with the possibility of acquiring and actuating numerous channels. These increment of channels corresponds to an increase of requested power.

The voltage levels that must be created are unavoidably dependent on the different used components, which are unpredictable before the modules development. It was thus decided to generate four fixed voltages on the power supply board, then used by each module to locally create any other necessary level. In particular ±13V and ±6.5V were chosen, since the actual voltages required in the majority of applications are near to these levels. This allows for the operation of both power-hungry components as well as the efficient generation of smaller values, such as those required by digital interfaces or analog voltage references. In addition, the power module also independently generates +5V, that has to be supplied to the Opal Kelly platform.

In order to properly size and design the supply board, the power required to operate the whole system was estimated, obviously considering the worst case scenario in order to guarantee the operation in all possible applications. Considering all the modules, the worst case arrangement is listed as follows:

- **Actuation module**: the actuation module presented in Chapter 2 is able to deliver up to 20mA to the *heaters* implemented in the photonic chip. Since the drivers

employed are working with ± 12V power supply and the number of channels present on the module is 24, if 6 actuation modules are plugged to the motherboard, an estimate of 3A current can be computed, down-scaled to 2A when referred to the 19V input.

- **Opal Kelly platform**: the powering voltage of the FPGA hosting platform is 5V, while the power consumption estimated for the device with a 80% utilization is 3W. Referred to the input, a correct esteem of 0.3A was assessed.

- **Motherboard and acquisition module**: neither the motherboard nor the acquisition module represents the power bottleneck of the overall system.

Considering the previous budget, it was decided to supply the power module with an AC/DC adapter able to deliver up to 5A current, that translates into a maximum available power of 90W.

Component	Supply voltage	Current	Number of devices	Total power dissipation
DAC9734	±12V	12mA	6	1.73W
	+3.3V	25uA		500uW
AD8513	±12V	2mA	6	300mW
INA2126	±12V	200μA	12	60mW
MAX11617	+3.3V	900μA	2	59.4mW
TMUX6212	±12V	35μA	6	84μW
SN74HC125	+3.3V	160μA	1	528μW
Heaters (Load)	±6V	20mA	24	2.88W

Table 3.1: Summary of power dissipation of the actuation module

3.3. Power supply description

Taking into account all the previous considerations, the power supply board generates five voltages, starting from a $V_{in} = 19V$ input which is properly filtered, as follows:

- **Positive voltages**: +5V dedicated to power the FPGA, +6.5V and +13V delivered to the motherboard or to the external modules. These three voltages are generated using three LT3681 Step-Down Switching Regulator, made by Linear Technology, that can deliver up to 2A current with almost 90% efficiency. They operate at 2MHz;

- **Negative voltages**: -6.5V and -13V negative power supply voltages. These two voltages are produced by two LTC7149 Synchronous Step-Down Regulator for In-

verting Outputs, designed by Linear Technology, able to deliver up to 4A current
with 92% efficiency. They operate at 2MHz;

All the five ICs are set to operate at 2MHz: it was decided to center the switching
frequency of the DC-DC converters around MHz region in order not to stay too close
to the frequencies of the signals used to control the optical circuitry. Furthermore, high
switching frequencies decrease the size of components like as inductors, transformers,
resistors and capacitors, as well as the board and case space requirements. However, since
the efficiency of these devices is degraded at too high switching frequencies, the value of
2MHz has been selected as a good compromise.

The two type of ICs (step-down and inverting converter) can work both in Continuous
Current Mode (CCM) and in Burst Mode operation, in order to minimize their power
dissipation in light load condition. Indeed, when the outputs do not require high amounts
of current, the converters charge the output capacitor with single cycle bursts of current,
remaining in sleep mode for almost all the switching period. The light load current is
in fact delivered by the already charged output capacitance. To increase the module
efficiency, the converters have been set to automatically switch from CCM to Burst Mode
when light load is detected.

To take into account future developments of the systems and increase robustness and
reliability of the module, a replica of the five voltages is generated by a second set of DC-
DC converters, leading to the employment of ten devices on the power supply module.

3.3.1. Step-down converter

LT3681 Step-Down Switching Regulator is the DC-DC converter employed for the gen-
eration of the positive power supplies. This type of regulator is a selectable frequency
(300kHz to 2.8MHz) monolithic buck switching regulator that accepts an input up to 34V
and generates an output voltage from 1.265V to 20V. As depicted by fig. 3.2, a high
efficiency $0.18\,\Omega$ NPN transitor (T_1) and a power Schottky diode (D_1) are integrated into
this ICs to minimize the occupied area on the PCB board. A resistor divider between the
output and the FB pin is used to program the output voltage, according to the relation:

$$R_1 = R_2 \cdot \left(\frac{V_{out}}{1.265V} - 1 \right) \tag{3.1}$$

In particular, while $R_1 = 590k\,\Omega$ has been selected for all the three ICs, $R_2 = 63.4\,k\Omega$,
$143\,k\Omega$ and $200\,k\Omega$ are placed to generate 5V, 6.5V and 13V respectively. The resistor
divider voltage is measured by an internal error amplifier to define the output current:

when the error signal grows, more current is given to the output; when it lowers, less current is provided.
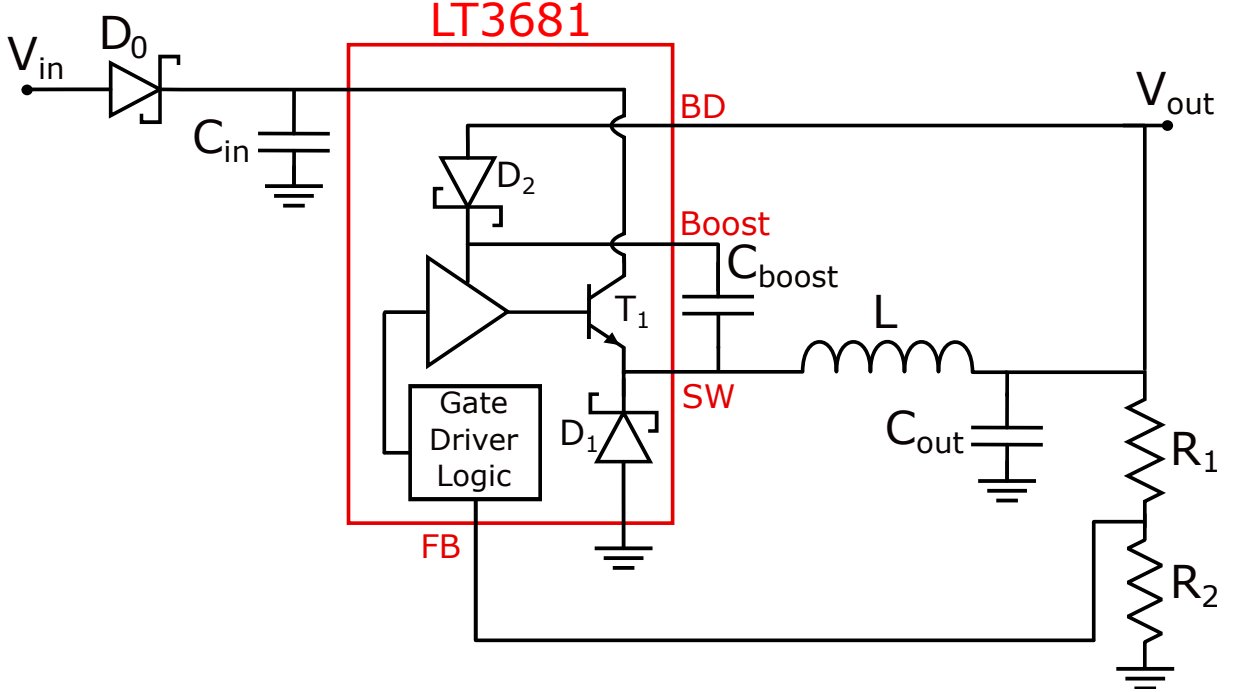

Figure 3.2: LT3681 Step-down converter

The IC is supplied by an embedded regulator, which is generally powered by the regulated output voltage. In order to drive the internal NPN switch, a *bootstrap* circuitry is used, as represented in fig. 3.2. An external capacitor $C_{boost} = 0.47\mu F$ is utilized to create a voltage greater than the input supply of the regulator, i.e. the generated output voltage, at the BOOST pin: in this way, the driver can fully turn on the built-in bipolar power switch.

As already mentioned, the switching frequency of all DC-DC converters was set to 2MHz. This value should be compliant with the maximum operating frequency of the IC, defined as:

$$f_{sw(MAX)} = \frac{V_D + V_{OUT}}{t_{ON(MIN)} \cdot (V_D + V_{IN} - V_{SW})} \tag{3.2}$$

where V_{OUT} is the output voltage, V_{IN} is the input voltage, V_D is the voltage drop across the internal Schottky diode D_1 ($\sim 0.55\,V$), V_{SW} is internal transistor power drop (less than $0.5\,V$) and $t_{ON(MIN)}$ is the minimum switch on time. A 2MHz switching frequency safely accommodates the highest $V_{IN}/V_{OUT} = 19V/5V$.

The sizing of the passive components was started by the selection of the power inductor: indeed, the ripple current is determined by the inductor value and switching frequency

for a particular input and output voltage. Considering a reasonable maximum output current $I_{OUT(MAX)} = 1\,A$ and setting the ripple current at least $\Delta I_L = 0.6 \cdot I_{OUT(MAX)}$ for all three conditions, the main inductor parameters can be assessed:

$$I_{L(RMS)} > I_{OUT(MAX)} \tag{3.3}$$

$$I_{L(SAT)} > 1,3 \cdot I_{OUT(MAX)} \tag{3.4}$$

$$L = \Big(\frac{V_{OUT} + V_D}{f_{sw} \cdot \Delta I_L}\Big)\Big(1 - \frac{V_{OUT} + V_D}{V_{IN}}\Big) \tag{3.5}$$

where $I_{L(RMS)}$ is the inductor RMS current and $I_{L(SAT)}$ is the inductor saturation current, with the other parameters previously introduced.

For all the three step-down circuits, the inductor selected is Bourns SRP4020FA-3R3M shielded power inductor with $L = 3.3\,\mu H$, $I_{L(SAT)} = 2.7\,A$, $I_{L(RMS)} = 4.4\,A$ and low series resistance $DCR = 4.4\,m\Omega$ in order to minimize conductive loss.

The selection of passive components continues with the input capacitor C_{in} and the output capacitor C_{out}. To correctly handle the ripple current and force it into a small loop, the input power supply was bypassed by a X5R ceramic capacitor of $10\,\mu F$. The output ripple is filtered by the same capacitor used for the input bypass, since ceramic capacitors have very low equivalent series resistance (ESR). However, a correct esteem of the ripple is not possible since the output current is not constant and it depends on the different Helios 3 configurations.

Lastly, diode D_0 is placed in series to the input power supply: the main purpose of this component is to protect against a shorted or reversed input.

3.3.2. Step-down converter for Inverting Outputs

LTC7149 Synchronous monolithic regulator is the DC-DC converter employed for the generation of the negative power supplies. This inverting converter can work within a wide input range (3.4V to 60V), generate negative output voltages till -28V and deliver up to 4A. Also in this case, the switching frequency can be externally adjusted in the range from 300kHz to 3MHz, that contains the required 2MHz.

As represented in fig. 3.3, the monolithic regulator integrates both the high-side switch ($110m\,\Omega$ NMOS) and the low-side switch ($50\,m\Omega$ NMOS). The setting of the output voltage is done by the selection of the external resistor R_{set}, connected between I_{SET} pin

and the output node, according to:

$$Vout = -50\mu A \cdot R_{set} \qquad (3.6)$$

where $50\mu A$ is the precise value of the internal current generator on the I_{SET} pin. Hence, to create -6.5V and -13V, $R_{set} = 130\,k\Omega$ and $261\,k\Omega$ are respectively employed.
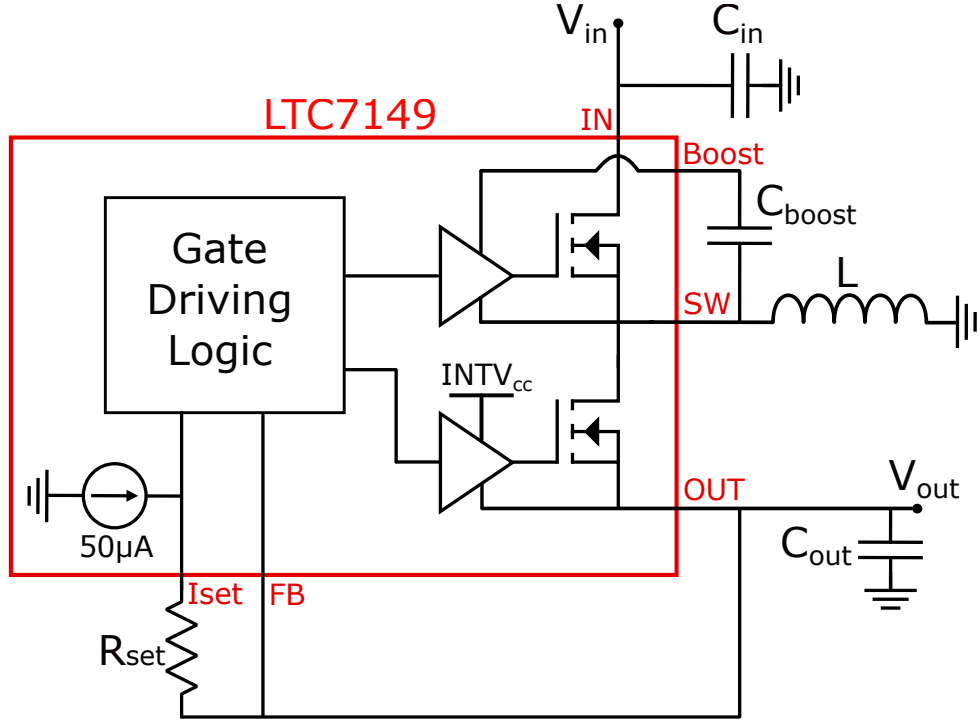

Figure 3.3: LTC7149 Inverting converter

The internal high-side switch is turned on at the start of a clock pulse in normal operation, letting the inductor current ramp up to a certain maximum level. When the level is reached, the top power MOS is deactivated and the low-side MOS is activated until the next clock cycle. The current mode loop is handled by a gate driving controller that, by comparing the voltage values between I_{SET} and F_B pins, adjusts the driving of the switch and matches the current capability requested by the output. As seen with the positive step-down regulator, the presence of the *bootstrap* circuitry ($C_{boost} = 0.1\,\mu F$) permits the efficient driving of the high-side switch.

The design phase followed the same steps of the previous regulator, with only an increase of the output current requirements as allowed by the device. By choosing $I_{OUT(MAX)} = 2\,A$ and by setting the inductor current ripple to 60% of decided maximum current, the same inductor of the previous DC-DC converter has been chosen, since it respects the following

conditions:

$$I_{L(SAT)} > I_{OUT(MAX)} \tag{3.7}$$

$$L = \left(\frac{V_{IN}}{f_{sw} \cdot \Delta I_{L(MAX)}}\right)\left(\frac{|V_{OUT}|}{V_{IN} + |V_{OUT}|}\right) \tag{3.8}$$

where the worst case is the one with $V_{OUT} = -13\,V$, leading to an inductance value $L = 3.3\,\mu F$. Lastly, the input capacitor C_{in} provides the filtering of the square wave current at the drain of high-side switch: several input capacitance were paralleled, reaching a value of $22\,\mu F$, in order to correctly handle the maximum RMS current I_{RMS}. On the other hand, $C_{out} = 50\,\mu F$ was placed at the output node in order to filter the output ripple and provide good stability to the feedback loop.

3.3.3.   EMI Input filtering and Output filtering

An input filter is required to decrease conducted emissions created by a DC/DC converter. As depicted in fig. 3.4, the primary function of the filter is to suppress noise and current surges from the external power supply that may affect the downstream circuits. The filter mitigates interference signals at the input switching frequency and its harmonics, preventing them from injecting noise in the system and interfering with any device [20]. A π network is generally employed: the capacitor C_{f1} provides an rough filtering of the residual AC components of the input power supply, while the following LC network provides of a low-pass action of second order.
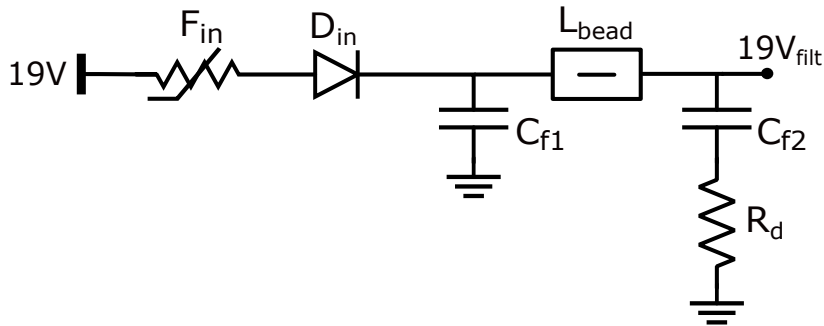
Figure 3.4: Input stage with protection measures and EMI filtering

In the same way, as represented in fig. 3.5, the output of each DC-DC converters is filtered by the same LC network, with the purpose of reducing the output ripple. In the design of the power supply board, each IC presents these filters, with *ferrite beads* instead of a standard inductors in order to reduce the Q factor gain at the filter cutoff frequency, defined as:
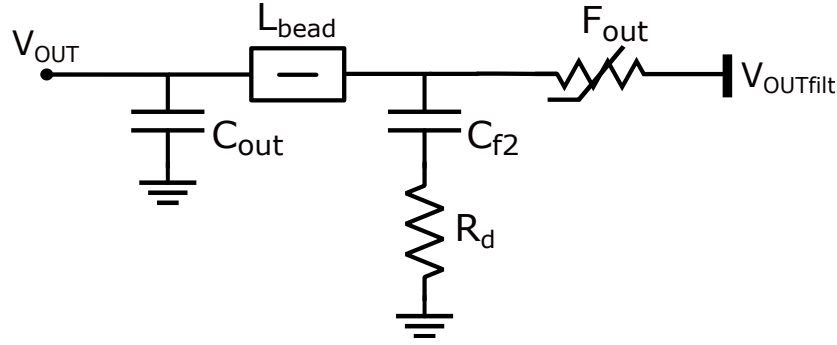
Figure 3.5: Output stage with protection fuse and filtering

$$f_{cut} = \frac{1}{2\pi\sqrt{L_{bead}\,C_{f2}}} \tag{3.9}$$

A ferrite bead is a passive component that absorbs noise energy by turning it into heat. It can be modeled as an inductor in parallel to a resistor, that accounts for the device dissipation. The inductive behaviour is exploited to filter noise on a wide frequency range, while the resistive part of the impedance damps the device resonance without causing any DC voltage drop. Ferrite beads are thus well suited to implement LC filters, however they suffer from saturation due to high load current, that cause the value of inductance to reduce, thus shifting the cutoff toward higher frequencies [21].

The filter cutoff was chosen in order to suppress the 2MHz switching frequencies and its harmonics with an attenuation of at least 40db, hence the filter cutoff was centeread around the 100kHz. This frequency was chosen taking into account that Continuous Current Mode (CCM) is expected to be the normal operating mode of the DC/DC converters of the supply module. A filter able to perform an effective action also for Burst Mode Operations would have required very large inductors and capacitors, not compliant with the available module area. In order to meet the frequency requirements, a ferrite bead with an inductance $L_{bead} = 280\,nH$ and a capacitor $C_{f2} = 10\mu F$ are chosen to build the second order low-pass filter. To increase the smoothing of the transfer function, a damping resistor $R_d = 2\,\Omega$ is added in series to C_{f2}.

3.3.4. Protection measures

Some protection measures were also applied to the power module in order to safeguard its reliability and functionality even in case of malfunctions and unpredicted operating conditions. In particular, the following situations were considered:

- **Input reverse polarity**: to correctly handle the input power supply, a diode D_{in}

is placed in series to the π filter with the purpose of protecting the circuit from reverse polarity. Indeed, if the input voltage has the wrong polarity, the diode turns off and shuts the module down, preventing any damage.

- **Overcurrent protection**: Positive resettable coefficient (PTC) fuses are placed in series to the input and to all the generated output voltages. These components behave as short circuits as long as a small current flows through them, thus not affecting the circuit behaviour. However, when the operating temperature rises due to a large current flow, their resistance increases dramatically, shutting down the downstream circuits. In order to select the correct fuse, the two important parameters to be set are the trip current I_{trip}, i.e. the minimum current required to activate the device transition, and the hold current I_{hold}, i.e. the maximum current that a PTC fuse can handle for extended periods of time without tripping.

The diode RURD620CCS9A (STMicroelectronics) has been chosen as input reverse polarity protection, since it is able to handle currents up to 5A with a negligible voltage drop and has a maximum reverse voltage of 200V, thus perfectly satisfying the requirements of the application. The chosen overcurrent protection fuses are instead 0ZCF0300BF2C (Bel Fuse, 5.2A trip current, 3A hold current) for the overall circuit input and 0ZCF0110AF2A (Bel Fuse, 2.2 A trip current, 1.1 A hold current) at each DC/DC output.

3.3.5. PCB layout

The shape of the power module was conceived similar to an horseshoe (as shown in fig. 3.6), in order to give room to FPGA for dissipating the heat generated during its operation. Indeed, as already mentioned in the introduction, the power board is connected to the motherboard through four vertical headers, right above the Opal Kelly platform. Only two headers are actually used to provide the supply voltages to the motherboard, that distributes them to all the components thanks to several power planes. The other two dummy connectors only ensure mechanical stability and balance when plugging the module. Since the power board can be detached from the motherboard, the disposition and connections of the headers guarantee a correct operation even if the module is inserted with a 180° rotation.

Fig. 3.7 shows the layout of all the DC/DC converters on the top layer, with a simple partitioning of the PCB area. Since the motherboard is much larger than the power module, the layout has been done with no particular requirements in terms of area occupation, allowing to place all the components on the top layer and design a board with only four layers. In this way, no converters have been disposed on the bottom part of the board,

in order to not radiate significant electromagnetic interferences towards the Opal Kelly platform. As already explained in the introduction, the converters are positioned almost symmetrically and connected to the headers on the same side.
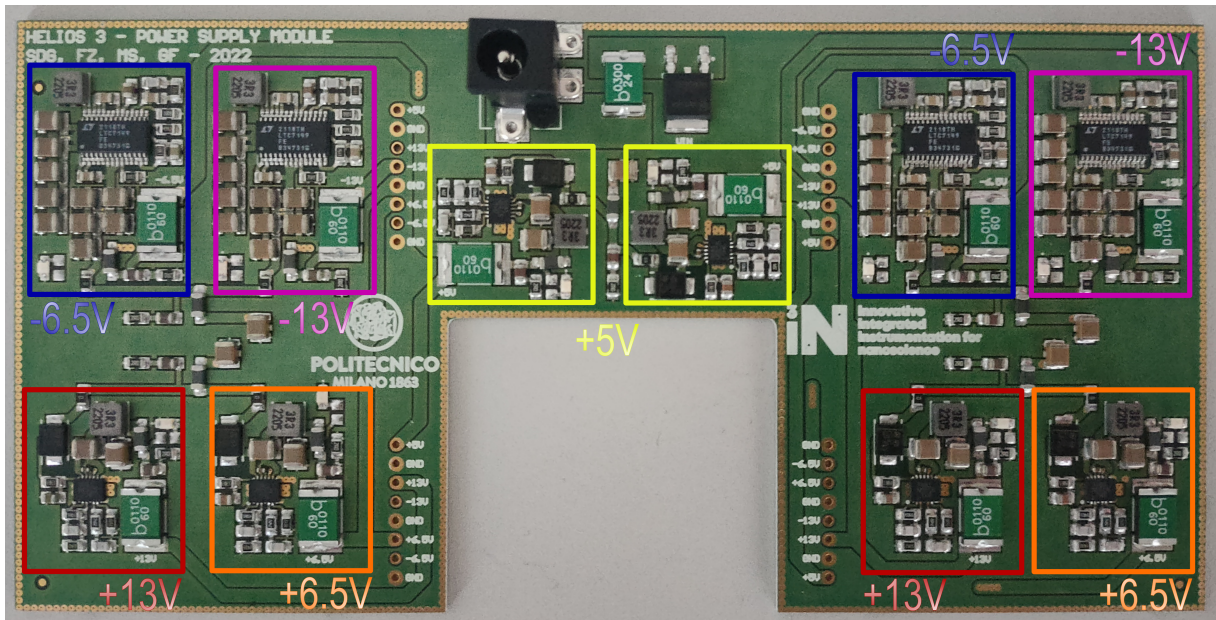
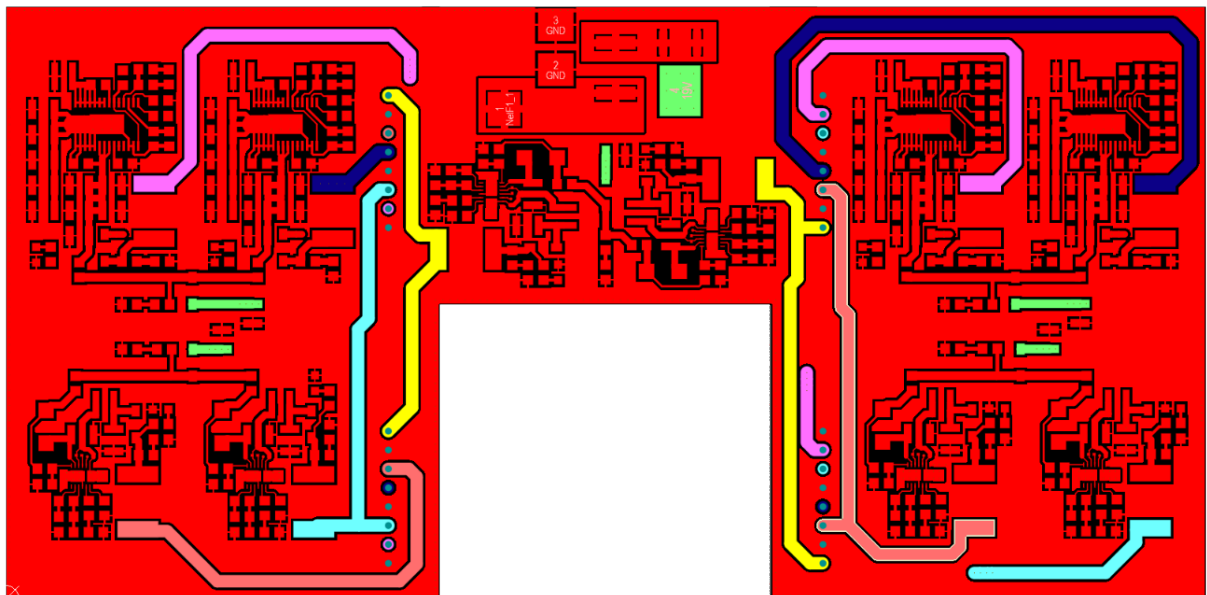Figure 3.6: Power supply board layout with 10 ICs employed
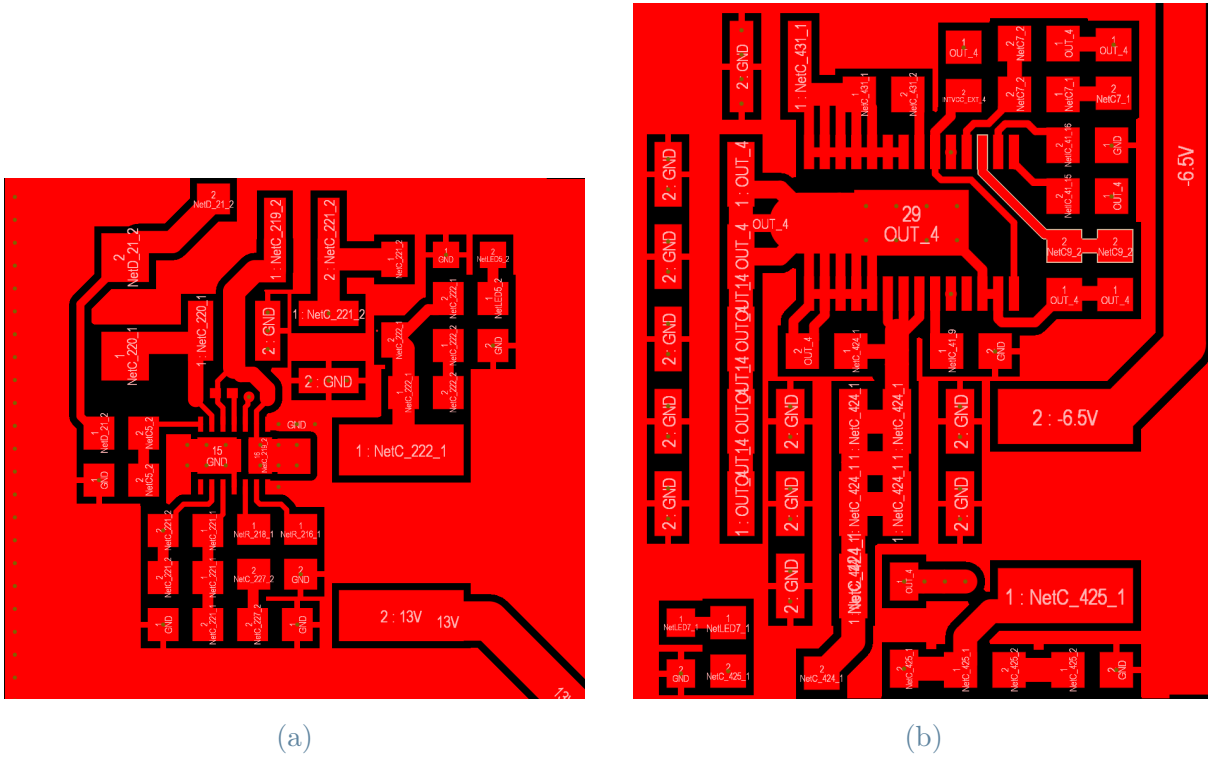

Figure 3.7: Top layer of the power supply board

(a)   (b)

Figure 3.8: Step-down converter layout (a) and Inverting converter layout (b)

For correct operation and EMI minimization, proper care has to be taken during PCB layout. In particular, in order not to generate relevant emitted electromagnetic fields, the current path formed by the two different switching phases has to be as short as possible. As the datasheet of the converters suggests, all the components that take part in the switching mechanisms have to be placed on the same side of the board, as close as possible, and connected on the same layer, while the other components dedicated to the set up of the ICs have to be placed away from the switching pins of the converters. In order to manage the large output currents, traces with large width are implemented. The layout of the two types of converters with the previous listed precautions can be seen in fig. 3.8.

Furthermore, as depicted in fig. 3.9, the inner plane was used to directly connect the input power supply (highlighted in green) to each ICs in order to handle the maximum input available current (5A) and to manage the high switching currents with the creation of power planes directly connected to output node.

Finally, as shown by fig. 3.7, the PCB area surrounding each ICs is covered by copper and connected to ground planes (second and fourth layers) using several vias to keep the operating temperature low.
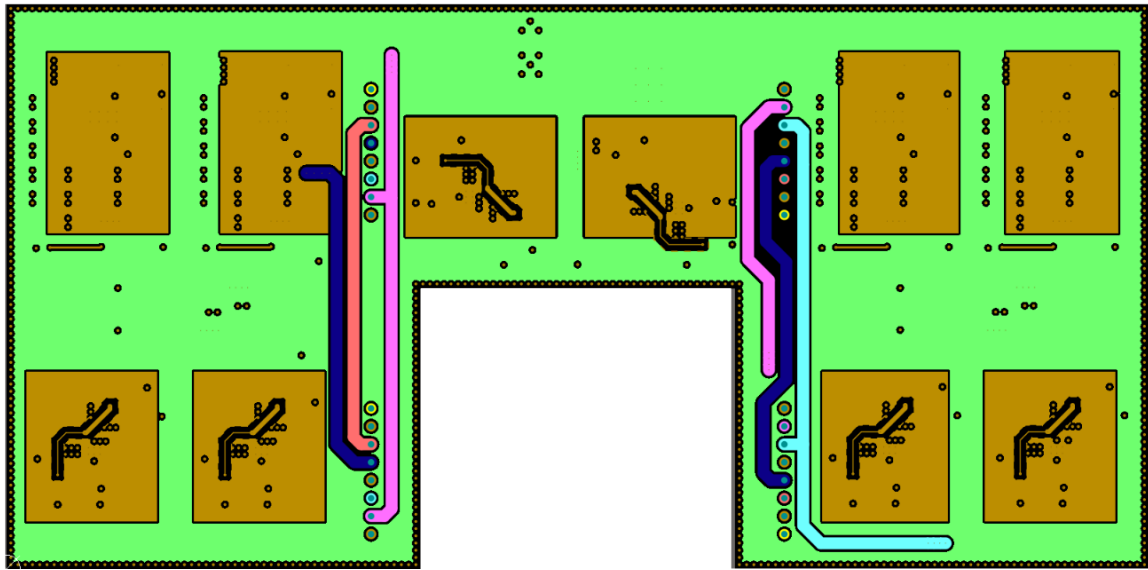
Figure 3.9: Inner layer of the power supply board

3.4. Power module validation

The power supply module was properly designed by selecting the components and validated with simulations. The second step is critical for correctly understanding the behavior of the various components in several circumstances. This method, however, cannot account for all of the non-idealities of each device.

Additionally, as highlighted in the previous section, the PCB layout results to be critical in order to generate really stable power supplies. It is therefore essential to experimentally characterize the manufactured circuits to ensure that they function as predicted. The experimental measurements obtained on the switching regulators are given in this chapter.

3.4.1. Start-up transient

As first validation measurement, the start-up transient of each converter has been estimated. Both the selected switching regulators feature a *soft-start* circuitry in order to properly manage the switch-on.

Soft start solves the problem of high in-rush current which could verify in the start-up condition: indeed, at the start-up, in order to reach the steady state condition all the components of the power circuit are instantly connected to input power supply, requiring an important surge of current to charge the input and output capacitors. Instantaneous spikes of the input current can cause significant overshoots of generated output voltages, leading to a situation that could damage the circuitry connected to the converters. The

soft start circuit is used to control the switch-on of the switching regulator, by limiting the current that flows inside the power switches, so that the charge of all the capacitors is achieved with a clean exponential transient.

In particular, the start-up transient of the generated 5V and -13V voltage is reported in fig. 3.10. The start-up time constants of both converters was set in the order of tens of microseconds, as confirmed by the measurement.
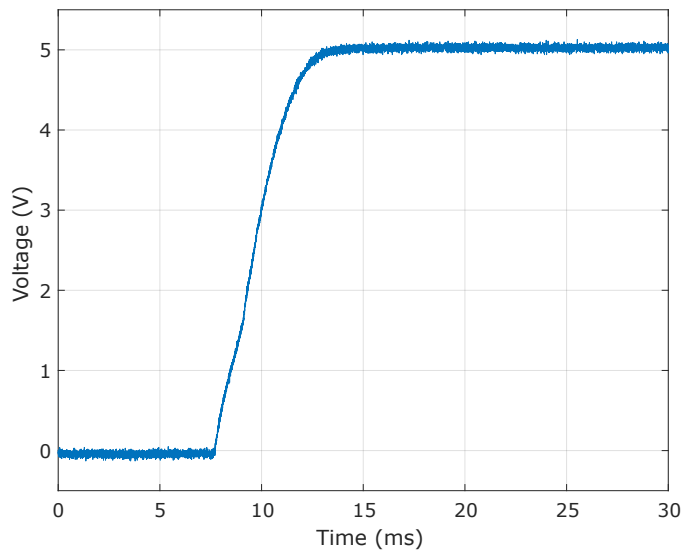
(a)
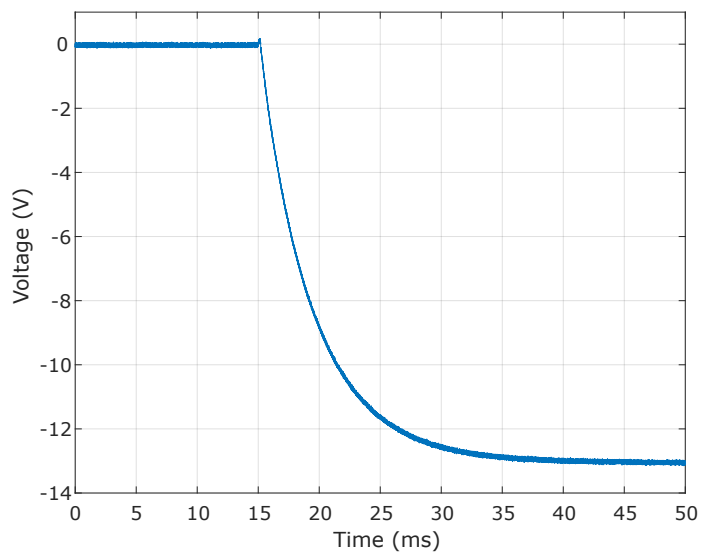
(b)

Figure 3.10: Start-up exponential behavior of the (a) LT3861 and (b) LTC7149.

3.4.2. Output ripple and spectral response

The operating mode of the switching regulators, which depends on the load current required, impacts on the output ripple amplitude and spectral response. Indeed, while in Continuous Current Mode the switching frequency is constant at 2 MHz, in Burst Mode operation, activated at light loads to enhance the converters efficiency, the switching frequency is reduced, leading to an output ripple with higher amplitude. As already mentioned in Sec. 3.3, the Burst Mode operation implies that bursts of current are delivered to the output and the frequency of this bursts, which depends on the load current, is unpredictable a-priori.

All the converters operate in Burst Mode condition when only the motherboard is connected to the power board, since the circuitry implemented in the part of the system does not necessitate of large amount of power. The converters can then switch to CCM operation depending on the number and type of modules plugged into the motherboard to satisfy a certain application.

Figure 3.12 shows the different voltage waveforms generated at the switching node of the buck converter, that change depending on the different load currents. When in CCM, the voltage swings between $V_{in} - V_{out}$ and $-V_{out}$ with a switching period $T_{sw} = 0.5\,\mu s$ and duty cycle $D = 0.68$, as set in the design phase. Instead, in Burst Mode condition the converter enters in sleep mode for a certain time period, in which the output current is provided by the output capacitor, while regaining the established switching frequency in other temporal windows to restore the output capacitor charge. In the waveform reported

(a)   (b)
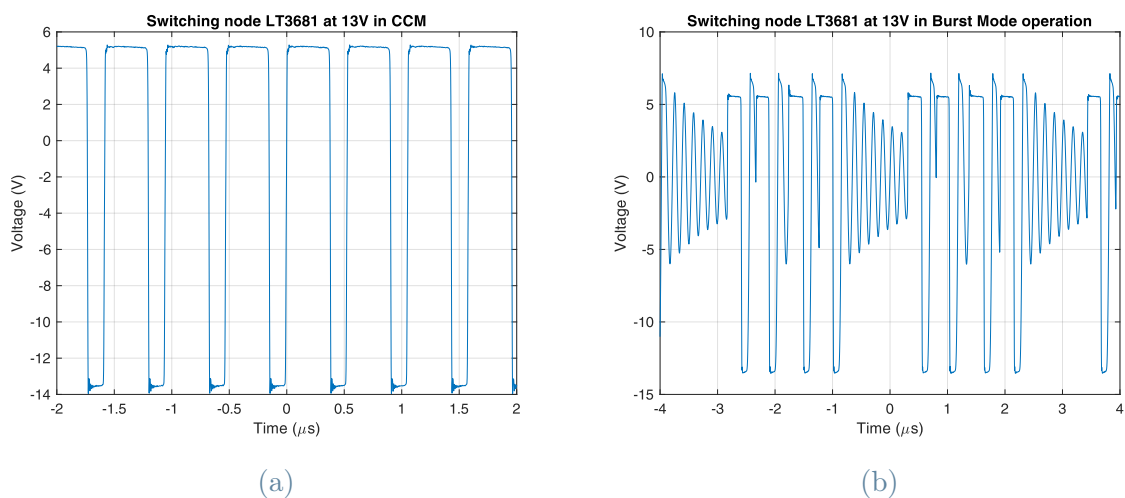
Figure 3.11: Switching node voltage waveform of LT3681 when in (a) Continuous Current Mode and (b) Burst Mode.

in figure, the behaviour in Burst Mode is repeated with a periodicity of almost $2\mu s$.

The same behaviour can be appreciated from Figure 3.11, where LTC7149 operating regimes are displayed. For the inverting converter, the switching node voltage varies between V_{in} and $-V_{out}$ in CCM with a defined duty cycle $D = 0.4$, while single bursts of current are delivered every $3\,\mu s$ in Burst Mode regime.

(a)   (b)
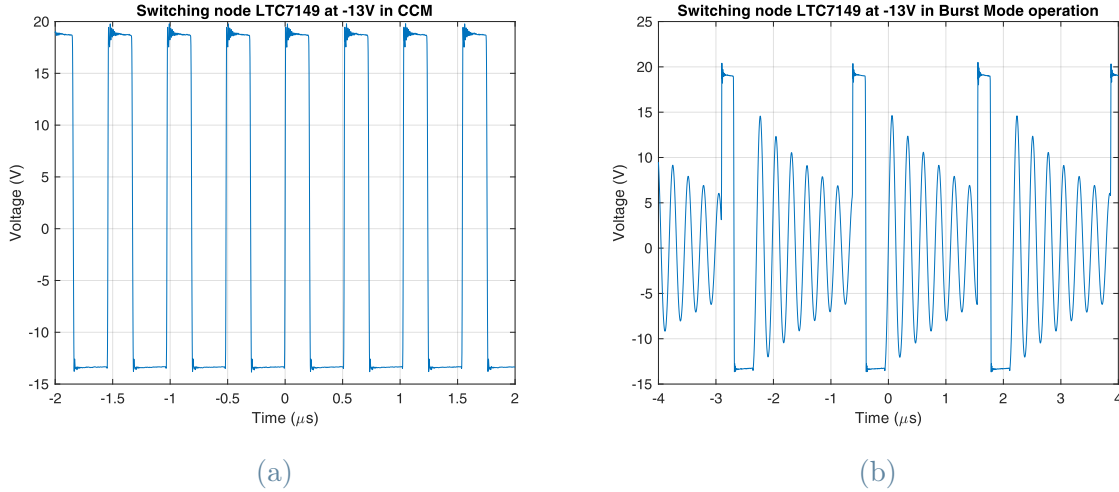
Figure 3.12: Switching node voltage waveform of LTC7149 when in (a) Continuous Current Mode and (b) Burst Mode.

To further explore the effects of Burst Mode operations on the generated voltages, the output of LTC7149 at -6.5V operating at extremely low load current has been acquired with an oscilloscope (HDO6054A-MS, Teledyne Lecroy). Figure 3.13 shows the result. The output ripple has a period of 35 μs, close to the minimum switching frequency allowed by the component, with an amplitude of almost 5 mV. The ripple is significantly larger than what observed in CCM, due to the lower filtering action performed at low frequency by the power module, however, even in this worst case scenario, the generated voltage is sufficiently stable to correctly supply the circuits of Helios 3. The measurement thus confirms the correct operation of the power module in any load conditions.

To quantify the performance of the module in both CCM and Burst Mode, the frequency spectrum of the generated output voltages has been acquired in different load conditions. The measurement was realized with a spectrum analyzer (MXA N9020A, Agilent Technologies) and, in order to correctly acquire the output spectral density while preventing damages, an high pass filter (with a pole at 300 Hz) was connected to the input of the instrument. In figure 3.14, the output spectral response of LTC7149 is compared in the two working conditions. The measurement shows the important difference between the two output signals generated by the converter. In this particular case, the harmonics of
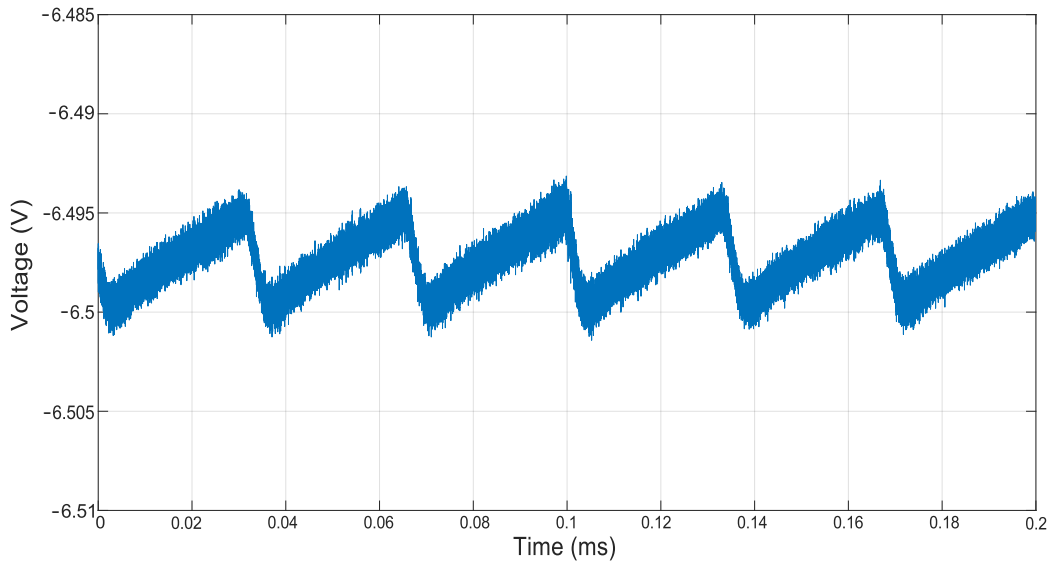
Figure 3.13: Output ripple of -6.5V in Burst Mode Condition

the Burst Mode operation are concentrated around 15 kHz, with a maximum amplitude of $20nV/\sqrt{Hz}$. Instead, in CCM the switching frequency is correctly increased to 2 MHz and the harmonics are significantly attenuated by the LC output filter of the module, whose cutoff has been set around 100 kHz.
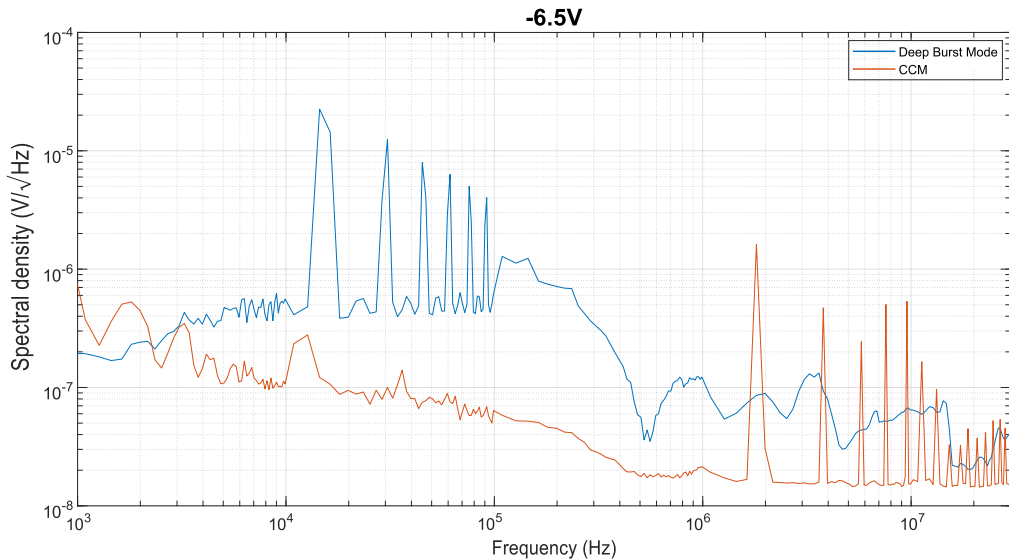
Figure 3.14: Output ripple of -6.5V in Burst Mode Condition (blue) and Continuous Current Mode (CCM)

A similar measurement has been performed to test the positive converters LT3681, as shown in Fig. 3.15. The measurement has been done with the power module supplying just

the motherboard in the first case (blue), while for the second case (orange) one acquisition modules was also operated. It is possible to notice that in the first scenario the device works in deep Burst Mode, with a switching frequency around 50 kHz, indicating a sleep period of the device around $20\mu s$. Instead, in the second curve the converter approaches a switching frequency of 2 MHz but an harmonic at 450 kHz is still visible, suggesting an intermediate working condition between Burst and Continuous Current Mode, usually indicated as Light Burst Mode. Seamless transition between the two working conditions is indeed crucial to maintain a high power efficiency regardless of the load current.
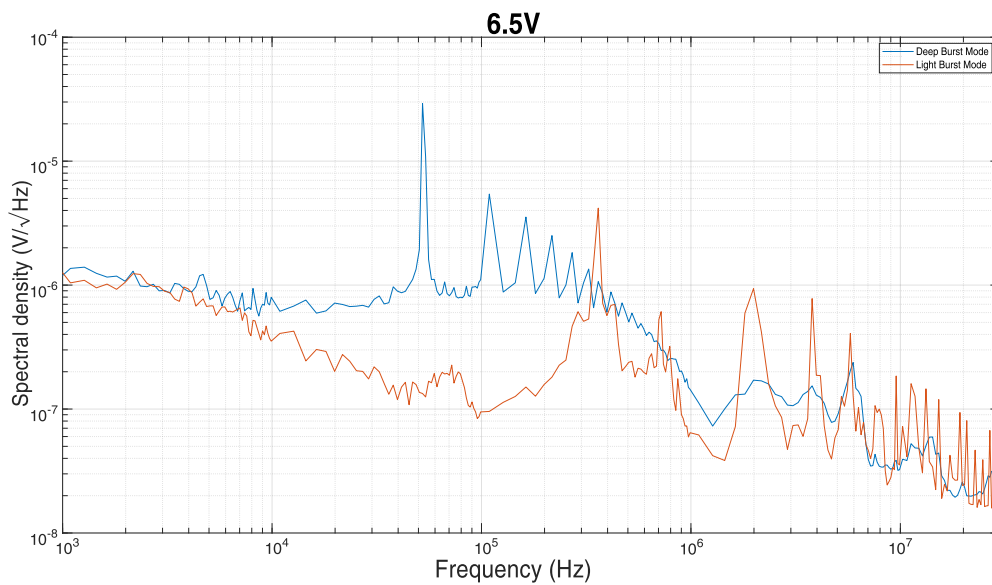
Figure 3.15: Output ripple of 6.5V in Burst Mode with different load current

3.4.3. Filtering measurement

The filtering action of the LC filter at the output of each DC-DC converter and of the LDOs on the motherboard have also been analyzed. As already mentioned in the Sec. 3.3.3, the LC filtering attenuates the output ripple and switching noise of each DC-DC converter. A similar action is performed by the LDOs placed on the motherboard and on the different external modules, thanks to their high power supply rejection ratio (PSRR). To quantify these effects, measurement with the spectrum analyzer have been acquired in three different positions: at the DC-DC converters output, after the LC filter and after the LDOs.

Figure 3.16 and 3.17 depict the output spectral densities of LTC7149 and LT3681, respectively. The filtering process is achieving -20 dB attenuation at 2 MHz switching frequency, confirming the usefulness of the circuit. Simulations of the same filtering network showed

an attenuation of -40 dB, however they did not take into consideration the degradation of the ferrite bead inductance happening at large current loads, which moves the filter cutoff at higher frequencies. Since the filter is designed to attenuate the switching harmonics in CCM, large load currents are expected, making it difficult to predict the attenuation provided by the filter. Ferrite beads with higher saturation current can be considered to improve the filtering action.

Finally, the power spectral density at the output of the LDOs has been acquired. In particular, the LDO placed on the photodiode acquisition module to generate the precise values of ±12V have been analysed. The measurement is useful to characterize the system in a realistic scenario and understand the capability of the LDO in suppressing the switching noise of the power module board. Figure 3.19 and 3.18 show that the LDOs filtering action is able to completely suppress the harmonics due to the switching frequencies (1-10MHz range). The measurement thus certificates that the use of DC-DC converters to supply Helios 3 has no harmful effect on the performance and resolution of the system and certifies the correct design of the overall power supply.
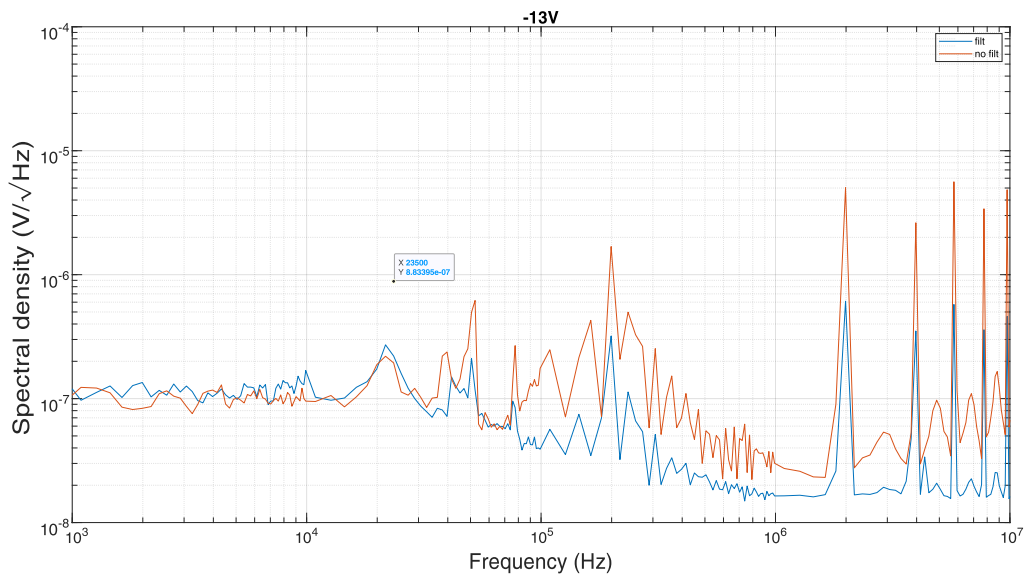
Figure 3.16: Comparison of the output spectral density of LTC7149 before and after the filter
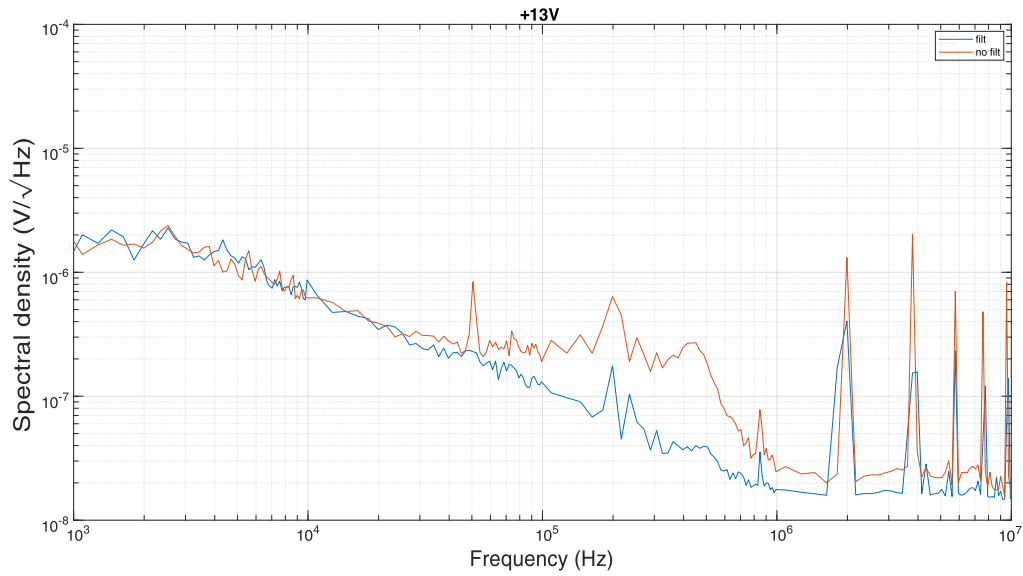
Figure 3.17: Comparison of the output spectral density of LT3681 before and after the filter
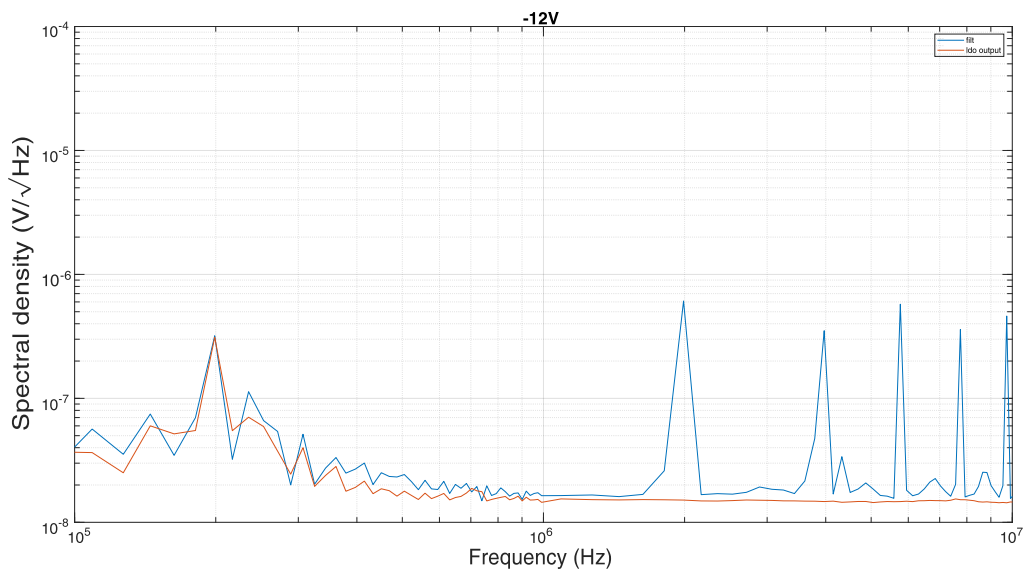
Figure 3.18: Comparison of the output spectral density of LT3681 after the filter and positive LDO output
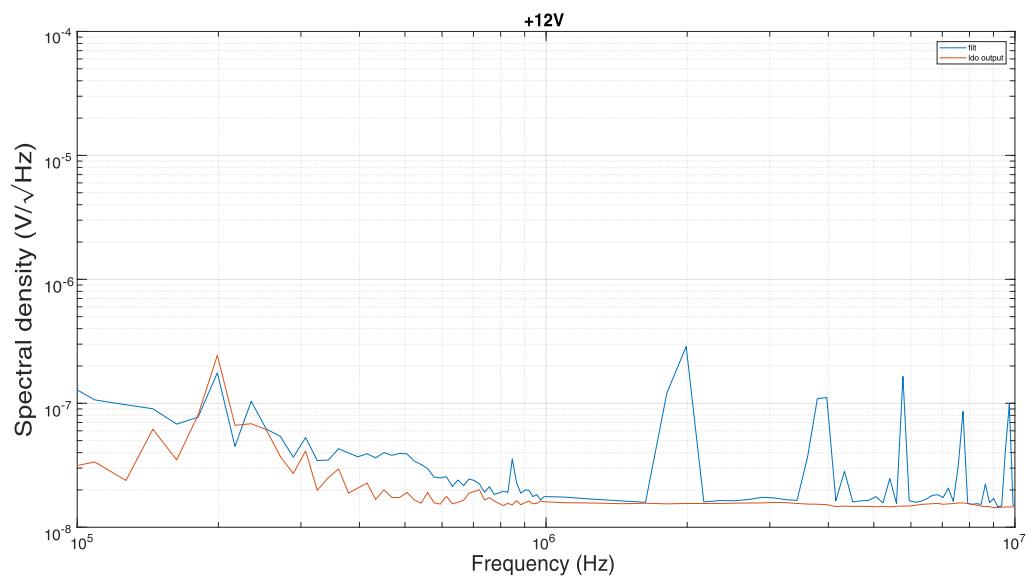
Figure 3.19: Comparison of the output spectral density of LTC7149 after the filter and negative LDO output

4 | High Power - High Voltage actuation module

4.1. Introduction

After the discussion on the Helios 3 platform and its power supply module, an actuation module able to drive both SiN heaters, which requires an important current capability (High Power), and MEMS actuators, which are driven with an extended voltage range (High Voltage), is presented.

As already introduced in Chapter 1, this pluggable module adds another important functionality to the system and increases not only the amount of actuators that Helios 3 can drive, but also the type: while the typical detectors employed for sensing the behaviour of photonic components are Germanium photodiodes, that require only one type of pluggable module, multiple types of modules are required in order to adapt Helios 3 platform to different actuation strategies.

It is important to highlight that the necessity of driving MEMS devices, which require significant voltage levels (up to 30V), was not considered at the beginning of the Helios 3 project. The power supply tree was thus designed in order to correctly drive thermo-optic actuators, so an important aspect of the realization of this module was the re-conception of the power supply needed to drive the novel actuators.

Following what was done in Chapter 3 for the power supply module, this chapter describes this novel actuation module (Sec. 4.2), the power supplies employed in order to correctly drive the actuators (Sec. 4.3) and the complete actuation chain with the selected electronic components and the PCB layout. Lastly, the module has been validated and the measurements are presented.

4.1.1.   Module description and requirements

In this section, the requirements of the previously introduced heaters module are revisited to understand the differences imposed by the new kinds of actuators and design a circuit able to provide the correct control signals.

The frequency range of the voltage signals to be generated is similar to what presented in Chapter 2. Indeed, the same control strategies that are used to drive the heaters in SiP also apply to heaters in SiN and MEMS devices. Therefore, a frequency range from DC to few tens of kHz is considered, to accommodate both DC bias voltages and dithering modulations. A DAC with a sufficiently high update frequency must thus be selected to generate modulated signals with a sufficient number of points per period.

A 20V dynamic range is required to drive heaters in SiN, as a consequence of the lower TOC of this material. In order to provide more power to the thermal actuators, higher driving voltages are indeed required with respect to SiP. Similarly, up to 30V need to be created in order to actuate MEMS devices. It was thus decided to design a module able to work with two different power supplies, i.e. +24V or +36V, according to which type of actuator needs to be driven. To make the module as self-sufficient as possible, a step-up circuitry able to locally generate a stable power supply of +24V or +36V starting from the 13V provided from the PCIe connector has been implemented. This single-supply operation mode was selected in order to limit the PCB area of the step-up circuitry, which needs a dedicated DC-DC converter.

An accuracy around 1 mV is also desired in the generation of the actuation voltages, in order to precisely control photonic devices with narrow and steep transfer functions. This specification defines the number of bits that the employed DACs need to have. In addition, to power SiN heaters, which typically have lower resistance with respect to the ones in SiP, an output current of up to 50 mA is required. Thus, the final stage of the actuation chain necessitates an appropriate current driver. Since the whole module is powered with a single external power supply of +12V, with a limited current capability, the number of actuation chains on the module has been lowered from 24 to 16. No particular current requirements, instead, are required by the MEMS actuators.

Similarly to what implemented in the previous actuation module, a real-time current monitoring circuit needs to be placed at the output of the drivers, so that any actuator failures can be detected. This is particularly important considering the high voltages that can be provided to the devices on the photonic chip. This embedded acquisition chain does not necessitate neither excessive sampling speed nor accuracy. Therefore, slow multichannel ADCs can be utilized.
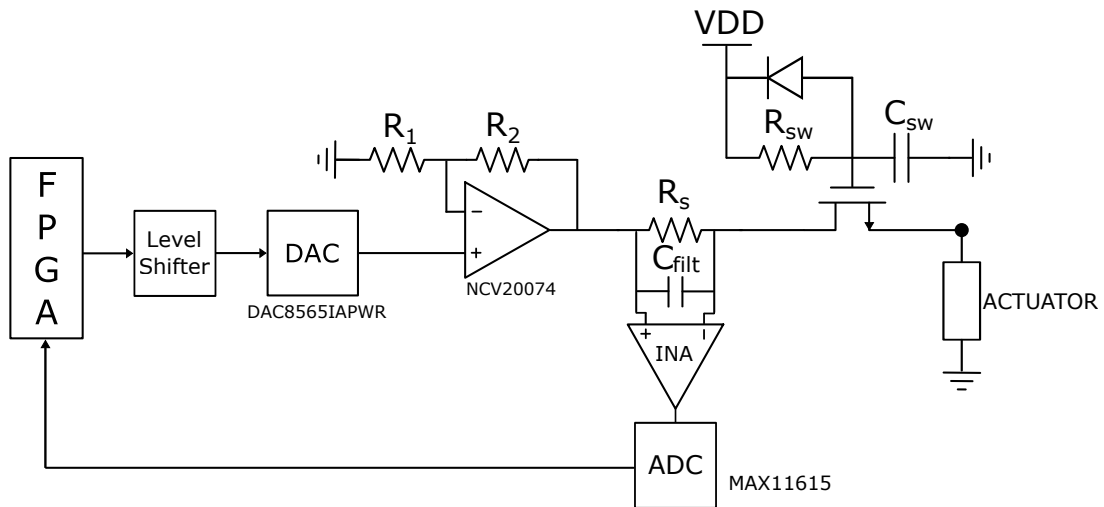
Figure 4.1: Schematic view of the High power - High voltage actuation chain.

Lastly, it is desired to have a protective mechanism at the output of the drivers, since the devices to be driven may be susceptible to short voltage spikes that occur during system startup. This issue was noticed with the prior version of the electronic board, therefore an improved circuit is designed in this module. A safeguard circuit has thus been included at the output of the generation chain, that disconnects the drivers from the actuators until stable supply conditions are achieved.

The final actuation chain is represented in Fig. 4.1 and its structure is described in detail in the next section.

4.2.   Power supply

In this section, the power supply circuitry of the module is presented. As already mentioned, the module is provided with the supplies produced by the power board, i.e. $\pm 6.5\,V$ and $\pm 13\,V$, and it uses these references to generate the voltage necessary to drive the actuators, in addition to the local voltage levels necessary to power up specific components (ADC and DAC) and handle digital signals.

To generate the high-voltage power supply, a boost DC-DC converter is needed to step-up from +13V to the two selected levels, i.e. +24V and +36V, while the other references, i.e. +3.3V and +5V, are produced by linear regulators.
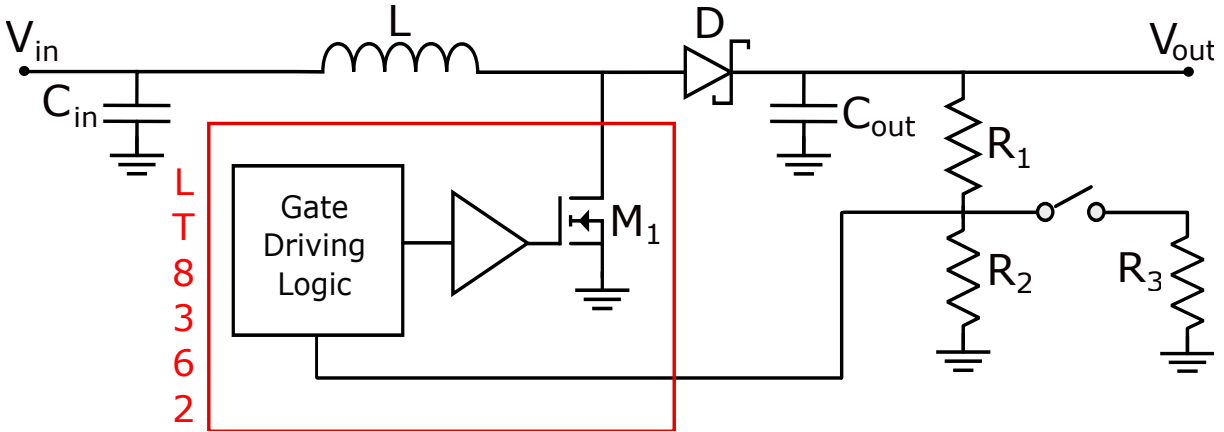
Figure 4.2: Schematic view of LT8362 Step-up regulator.

4.2.1. Boost converter

The LT8362 by Analog Devices is a 2.8V-to-60V-input current mode DC/DC converter including a monolithic 60V, 2A power switch. Its single feedback pin architecture allows it to operate in boost, SEPIC, or inverting modes. In this design, the switching converter is working in a step-up, boost configuration, turning the input positive power supply +13V into two possible voltage levels, i.e. 24V and 36V. The selection of the output voltage is done according to the resistor divider composed of R_1, R_2, applied to IC feedback pin, shown in Figure 4.2.

The output regulated voltage is set by the following relation:

$$V_{OUT} = 1.6 \left(\frac{R_1}{R_2} - 1 \right) \tag{4.1}$$

To allow the generation of two levels depending on the actuators to be used, a dip switch has been added to the feedback network, allowing to easily change the value of the feedback divider by connecting/disconnecting R_3 in parallel to R_2.

The same design choices of the converters used on power supply board are adopted in this case:

- **Switching frequency**: $f_{sw} = 2$ MHz has been selected to operate the DC-DC converter away from the signal frequencies used for the dithering technique.

- **Component selection**: a high performance Schottky diode (VS-10MQ060NTRPbF) with forward voltage drop $V_F = 0.63$ V at maximum average current $I_F = 1$ A has been selected, since the maximum current is limited by the input power supply specs (+13V, $I_{max} = 2$ A). The selected inductor is 74437349068 Wurth Electronic

Shielded Power Inductor with $L = 6.8\,\mu H$ and $DCR = 51.5\,m\Omega$, chosen according to the following formula:

$$L = \frac{V_{IN}}{\Delta I_{sw} \cdot f_{sw}} \cdot D_{max} = \frac{V_{IN}}{\Delta I_{sw} \cdot f_{sw}} \cdot \left(\frac{V_{OUTmax} - V_{IN}}{V_{OUTmax}} \right) \tag{4.2}$$

where $\Delta I_{sw} = 0.6\,A$ is the inductor current ripple suggested by the datasheet, D_{MAX} is the maximum duty cycle of the converter defined by the maximum output voltage $V_{OUTmax} = +36\,V$ and the input power supply $V_{IN} = +13\,V$.

4.2.2. Linear regulators

Low Drop-Out (LDO) regulators are employed for the generation of other voltage levels necessary to correctly operate the module and handle the digital signals coming from the FPGAs. In particular, +3.3V and +5V are generated by two different LDOs, whose +6.5V input comes from the motherboard. This solution was chosen since LDOs occupy less area on the PCB board with respect to switching converters, even though they are less efficient. The current to be supplied by these components is however limited in this application, so the low efficiency is not critical.

To produce the two voltage levels, two LT3045 by Analog Devices have been employed. Similarly to the previous DC-DC converter, the output voltage of this device is selected with a reference resistor, allowing to generate both +3.3V and +5V with the same component. To filter the power supply, a pair of capacitances, one large (10 μF) and one small (100 nF), are connected to the input and output of each LDO.

4.3. Actuation Chain

In this section, the actuation chain is explained in detail. All the components are introduced and their specs are explained to understand the design choices.

4.3.1. Digital-to-Analog Converter

As previously mentioned, the FPGA digitally generates the signals to be sent to the actuators. In order to convert them into analog signals, a Digital-to-Analog Converter is required. The dynamic range of the DAC must be amplified by a driver stage to reach the extended voltage range required by the MEMS actuators, while the number of bits must be high enough to guarantee an LSB at the output of less than 1 mV.

Furthermore, the sampling frequency should be compatible with the frequency require-

ments of the dithering signals. A high sampling frequency results in a higher maximum dithering frequency that can be generated or in modulated signals with more samples per period and hence higher spectral purity.

The component selected to satisfy these requirements is 'DAC8565' by Texas Instruments. It features a 16-bit string resistor architecture with a standard 3-wire SPI interfaces, consisting in clock, serial data in (SDI) and chip select (CS), and four channels are included inside a single package.

The DAC maximum clock frequency is 50 MHz, that can be reached only if the device is powered with a supply of +5V. As a consequence, also the digital signals provided to the component need to have this amplitude. Since the FPGA can only generate 3.3V digital signals, level shifter circuits have been included in the board. Nine digital signals are required overall to operate the module, i.e. four couples of SDI and CS and a shared clock. Their amplitude is translated by three level shifters: in detail, two 'TXU0104' 4-bit level shifter and one 'SN74LV1T34' single-bit level shifter, both by Texas Instruments, are employed.

An input digital word of 24 bits, consisting of 8 bit for the configuration of the device and 16 bit for the actual data, is needed to operate each DAC. Considering that each component includes four converters in the same package, a maximum sample rate of 520 ksps is obtained with a clock frequency of 50 MHz, high enough for the generation of dithering signals up to 50 kHz.

The output voltage range of the DAC is 2.5V, so an amplification of a factor 12 is needed to reach up to 30V at the output of the actuation chain. By using a DAC with 16 bits, the accuracy at the output is thus 460 μV, satisfying the requirement of the application.

To drive all the 16 channels of the module, four independent components are used. All components share the clock line of the SPI interface, while having dedicated SDI and CS lines.

4.3.2.   Driver

In the actuation module for SiP heaters presented in Chapter 2, the role of the output driver was to enhance the current capability of each actuation channel, since the selected DAC could already provide the required voltage dynamics but with a limited current. In this new version, the same function is required to properly drive the SiN heaters. However, the driver has also an amplification function, needed to meet the high voltage span required by MEMS actuators.

On Semiconductor 'NCV20074' 3 MHz 4-channel Operational Amplifier is the driver selected to satisfy these requirements. It can be supplied with a wide range of voltages (3.6V to 36V) and features a rail-to-rail output stage. As highlighted by fig.4.3, the operational amplifier is used in a non inverting configuration with a gain of 12 to match the dynamics of the DAC to the full voltage range required for the MEMS actuators. In addition, a resistor is placed is series to the positive input pin to mitigate the effect of the amplifier bias currents.

Considering the 3 MHz gain-bandwidth product and the selected gain of 12, the bandwidth of the amplifier results to be around 250 kHz, satisfying the frequency requirements for the generation of the dithering signals. The Slew-Rate of 2.4 $V/\mu s$ of the amplifier doesn't affect the dithering modulation waveform. Considering a maximum amplitude of a dithering signals equal to one eighth of voltage dynamic of the driver output, i.e. 3.75V, a full power bandwidth of $f_{max} = 100kHz$ is obtained, higher than the maximum frequency of interest. Furthermore, the output sourcing current of 65mA is high enough to drive SiN heaters. Considering a typical heater resistance of 400 Ω, the circuit can thus provide up to around 170 mW to the actuator, enough to properly tune photonic devices even with the low TOC of SiN.

Since each component features 4 amplifier in a single package, 4 devices are needed to handle the 16 channels.
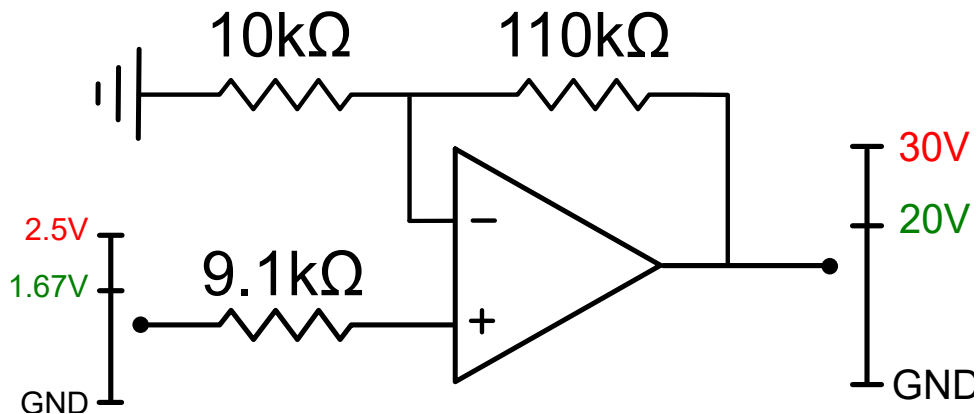
Figure 4.3: Schematic view of the driver stage with the output voltage dynamics referred to SiN heaters (green) and MEMS actuators (red).

4.3.3. Monitoring circuit

A monitoring circuit is included at the driver output to provide a feedback measure of the current delivered to the different actuators. This information is needed to detect

faults in the photonic chip, by highlighting unwanted short-circuits or open-circuits when operating the actuators. These can be due to both device failures and wrong connections when wire-bonding the chip to the control electronics. In particular, SiN heaters are subject to burn-out if they are not properly designed to handle a large power consumption, while MEMS devices can experience pull-in if the driving voltage is too large. Both these conditions can be detected by monitoring the current in the actuation chains.

The current measurement must be performed in a non-invasive way, in order not to affect the behaviour of the actuation chain. This is not a problem in the case of MEMS, since no current is expected to flow in the actuators. Conversely, SiN heaters, that can be modelled as low-value resistors of few hundreds of Ohm, require large amounts of current. The measurement is thus performed by adding a small shunt resistor in series to driver output and by measuring the voltage drop across its terminals. By choosing $R_{SHUNT} << R_{HEATER}$ a negligible impact on the behaviour of the actuation chain is obtained.

The sensed voltage drop, which is in the order of few mVs, can be amplified with an Instrumentation Amplifier (INA). The requirements of input common mode dynamics and small differential signals to be amplified lead to the choice of implementing a custom INA, made by using, as building block, the same amplifiers of the driver stage. The circuit topology, shown in Figure 4.4, is the standard 3-amplifier INA.

Since 48 devices are needed to realize 16 INAs, 12 'NCV20074' are needed to complete the whole monitoring circuitry. In particular, considering four actuation channels, two components have been used to design the input stage while the output buffer is implemented with a further amplifier.

By selecting a resistance R_G of the desired value, the user can adjust the INA gain in accordance with the following formula:

$$G_{INA} = 1 + \left(\frac{2R}{R_G}\right) \tag{4.3}$$

The gain has to be chosen to match the ADC input dynamics, so that the current signal is properly read. Considering a maximum driving voltage of 20V and the maximum output current of 65mA, the minimum acceptable resistance of SiN heater can be estimated to be 300Ω. The shunt resistor has been sized 100 times lower than R_{HEATER} to have a negligible impact, thus defining the INA gain needed to match the 3.3V ADC input dynamics. The voltage drop across $R_{sh} = 2\,\Omega$ is 130mV, leading to a $G_{INA} = 25$ ($R = 12k\,\Omega$ and $R_G = 1k\,\Omega$).
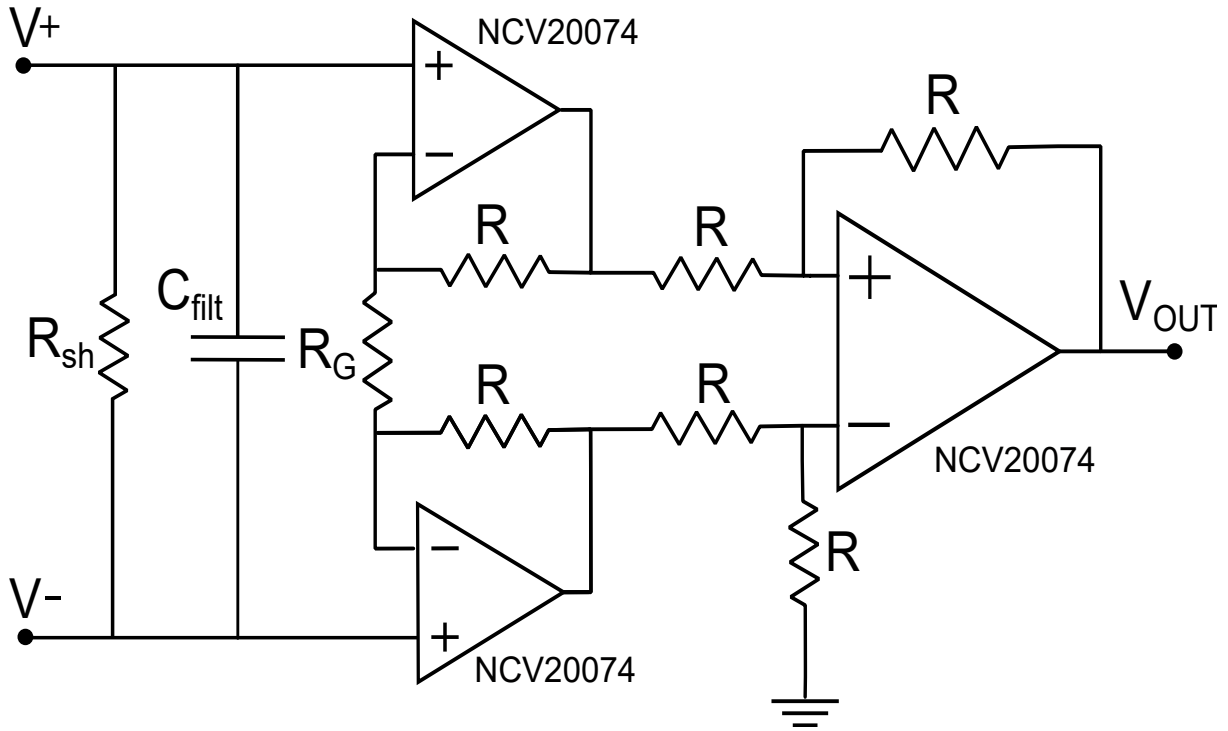
Figure 4.4: Schematic view of the custom INA employing three NCV20074 amplifiers.

Naturally, an ADC is required to acquire the current information after the amplification. Acquisition of these signals does not need to be very precise or rapid because their purpose is only to provide a rough estimate of the current flowing in the actuators. 8-channel ADC 'MAX11615' by Maxim Integrated has been selected. This ADC captures and converts an analog signal to a 12-bit serial digital output using successive-approximation conversion techniques. Considering the maximum current range of 65mA, the minimum current resolution obtained is around 8 μA, well below the requirements of the application.

The device is supplied at +3.3V and the maximum sampling rate is 94 ksps when using a clock of 1.7 MHz. This sampling frequency is too low to detect the dithering sinusoids but high enough to estimate the average current in the actuator. In order to prevent aliasing, a RC filter is created by placing a capacitance $C_{filt} = 2.2 \, \mu F$ in parallel to the shunt resistor, setting the filter frequency f_{cut} is set to 36 kHz. The anti alias filter is effective only when one channel of the ADC is activated, since the maximum sampling frequency is divided by the number of active channels, down to 12 ksps when all are on. The filter frequency has not been set to lower values for debug purposes, but if needed it could be changed by modifying the value of C_{filt}.

Two ICs are placed onto the PCB board in order to scan all the 16 channels of the module and they share the Serial Clock Line employed in I²C protocol.

4.3.4. Protection switches

Lastly, some form of decoupling device between the actuators and the driver output is required to safeguard the actuators during system startup.

For this purpose, the analog switch 'MAX4602' by Maxim Integrated can be a viable option. This device features a low on-resistance of 2.5 Ω, required not to affect the current delivery of the circuit, with a single supply operation range suitable for the application (4.5V to 36V). The component includes in the same package four normally open (NO) switches, that do not conduct until the 'NC' (normally closed) pins receives a high signal.

A simple RC network with a time constant of 0.4 seconds has been inserted between VDD and the 'NC' pin, since the protection is only needed for a brief period of time after the power supply is turned on. With this setup, the switches do not activate until the power supply of the module has stabilized, thus shielding the actuators from sudden voltage changes.

The same consideration can be done at the switch-off of the module, since significant spikes of voltage at the output node can affect the functionality of the actuators employed on the photonic chip. In order to speed up the aperture of the switch by easing the discharge of the RC network, a diode was positioned in parallel to the resistance, drastically decreasing the time constant of the circuit at the system switch-off.

4.3.5. Digital pins distribution

As already mentioned in Chapter 2, 16 digital pins are available for each module, while 24 analog connections can be exploited to read or generate signals. Here, only 16 analog channels are used because of the power supply limitations. Table 4.1 summarizes instead all the digital signals needed by the various components of the module, that fit inside the 16 available.

	Digital signals per components	Number of devices	Total digital signals
DAC8565	2 + one shared clock	4	9
MAX11615	1 + one shared clock	2	3

Table 4.1: Summary of digital pins required by the High Power - High Voltage module.

4.3.6.   Power dissipation

Table 4.2 summarizes all the supplies needed by the components on the module and their power dissipation in quiescent conditions. The table only reports the components powered by the linear regulators, to highlight that they are responsible of a negligible part of the overall power consumption.

Instead, table 4.3 and table 4.4 show the power dissipated by the drivers and INAs for both the configurations of the module, i.e. high voltage (+36V input supply) and high power (+24V input supply) configuration. In the latter case, the power consumption of the load is also shown.

	Supply voltage	Current	Number of devices	Total power dissipation
DAC8565	+5V	1mA	4	20mW
MAX11615	+3.3V	900 μA	2	6mW
TXU0104	+3.3V / +5V	1.5μA	2	10μW / 15μW
SN74LV1T34	+3.3V / +5V	1μA	1	3.3μW / 5μW

Table 4.2: Summary of the module components supplied by LDOs, reporting the required voltage level and power dissipation.

	Supply voltage	Current	Number of devices	Total power dissipation
NCV20074	+36V	1.86 mA	48	3.2W
MAX4602	+36V	0.5 μA	4	720μW

Table 4.3: Summary of the power supply needed for drivers and INAs in the high voltage configuration and their power dissipation.

	Supply voltage	Current	Number of devices	Total power dissipation
NCV20074	+24V	1.86 mA	48	2.14W
MAX4602	+24V	0.5 μA	4	48μW
Load (heaters)	+20V	20mA	16	6.4W

Table 4.4: Summary of the power supply needed for driver and INAs in the high power configuration and their power dissipation.

4.3.7. PCB Layout

After having defined the module architecture, all the components have been placed on the PCB board. For this specific module, a four-layer PCB has been employed, enough to handle the density of connections. The 64-pin PCIE connector described in the Chapter 2 is placed at the bottom side of the board and the position of the signals connected to it is defined by the motherboard architecture. The module size is 7cm x 11cm, standardized for all kinds of modules to always have a comparable occupation of volume regardless of the Helios 3 system configuration.

Both the top and bottom layers have been used for placing the components, to better exploit the available space and shield the sensitive signals from interference. The tracks conveying the output analog signals, the DACs, ADCs and power circuitry have been routed on the top layer, while input digital signals, drivers and INAs were located on the bottom layer (fig. 4.6). The level shifters have been placed as close as possible to the PCIe connector, to regenerate the digital signals before delivering them to the module. Particular care has been taken in designing the DAC digital lines with similar length, in order not to introduce unwanted skews between clock and data. For effective interference protection of all the connections, the second layer of the board has been used as a ground plane. Instead, the third layer is reserved to the power supply planes, handling and distributing the voltages generated by the DC-DC converter and by the two LDOs (fig. 4.7).
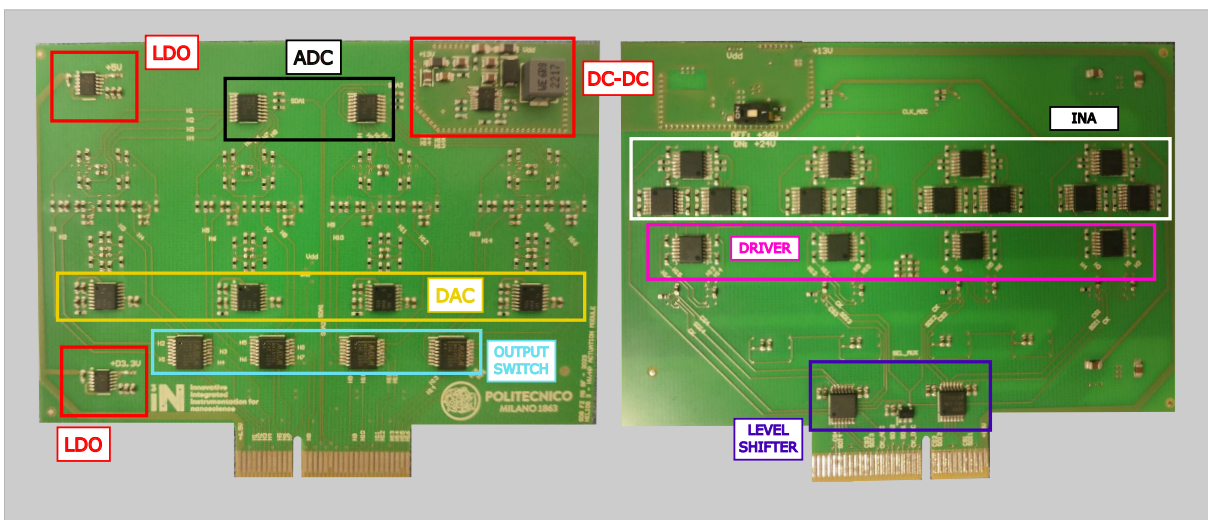
Figure 4.5: Photograph of the High Power-High Voltage module highlighting the different electronic sections.
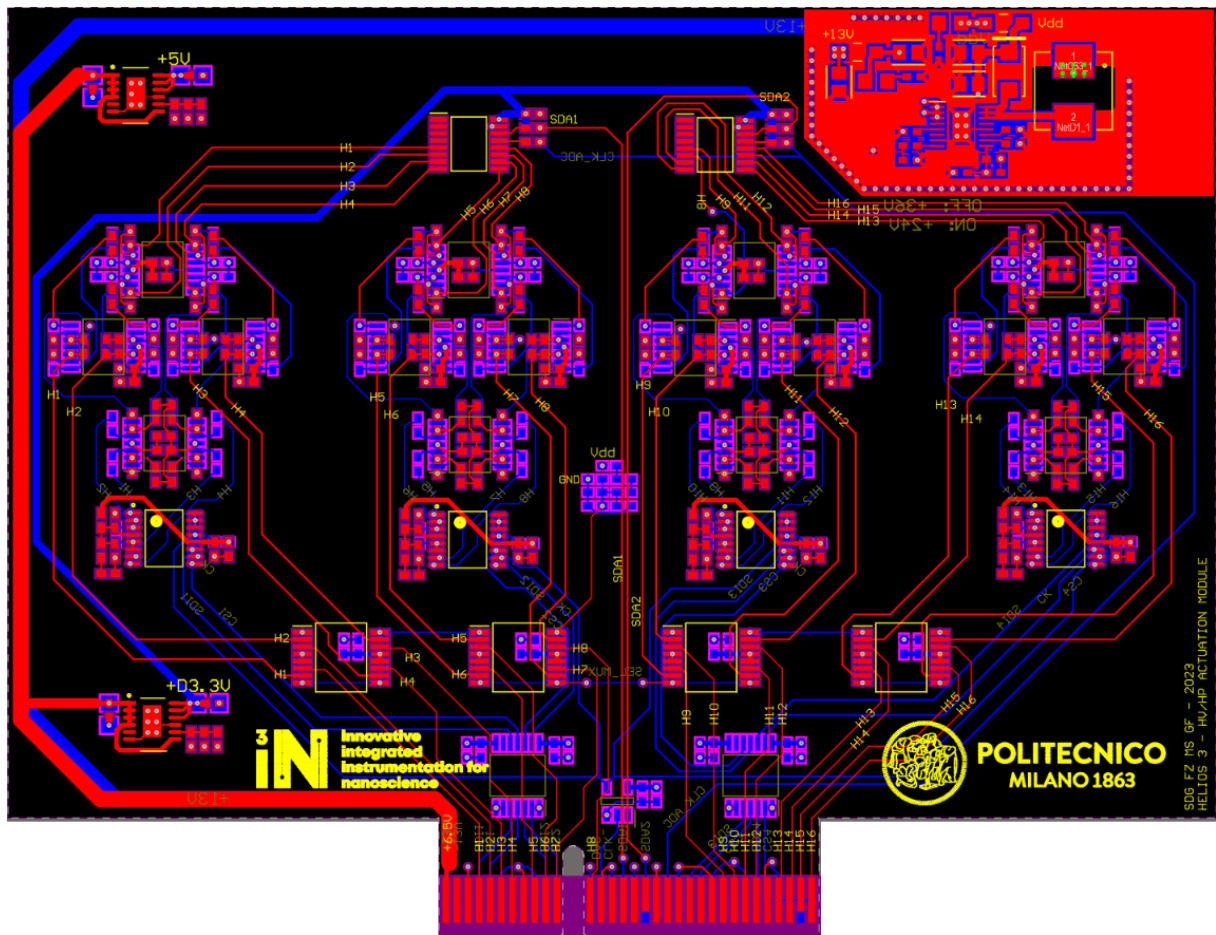
Figure 4.6: 2D view of the layout of the actuation module.

A consistent part of the top layer has been reserved to the layout of the step-up regulator: it has been placed close to the right top angle, far enough from the actuation circuitry not to create interference. The arrangement of the several passive components connected to the boost converter has been done following the same criteria described for the power supply module (fig. 4.8). In order to isolate the module from EMI generated by the converter, all the region employed for its layout has been isolated with several vias, connected to the ground plane. In addition, on each layer the area occupied by the converter has been filled with copper connected to ground. This precaution also helps in dissipating the heat generated by the component.
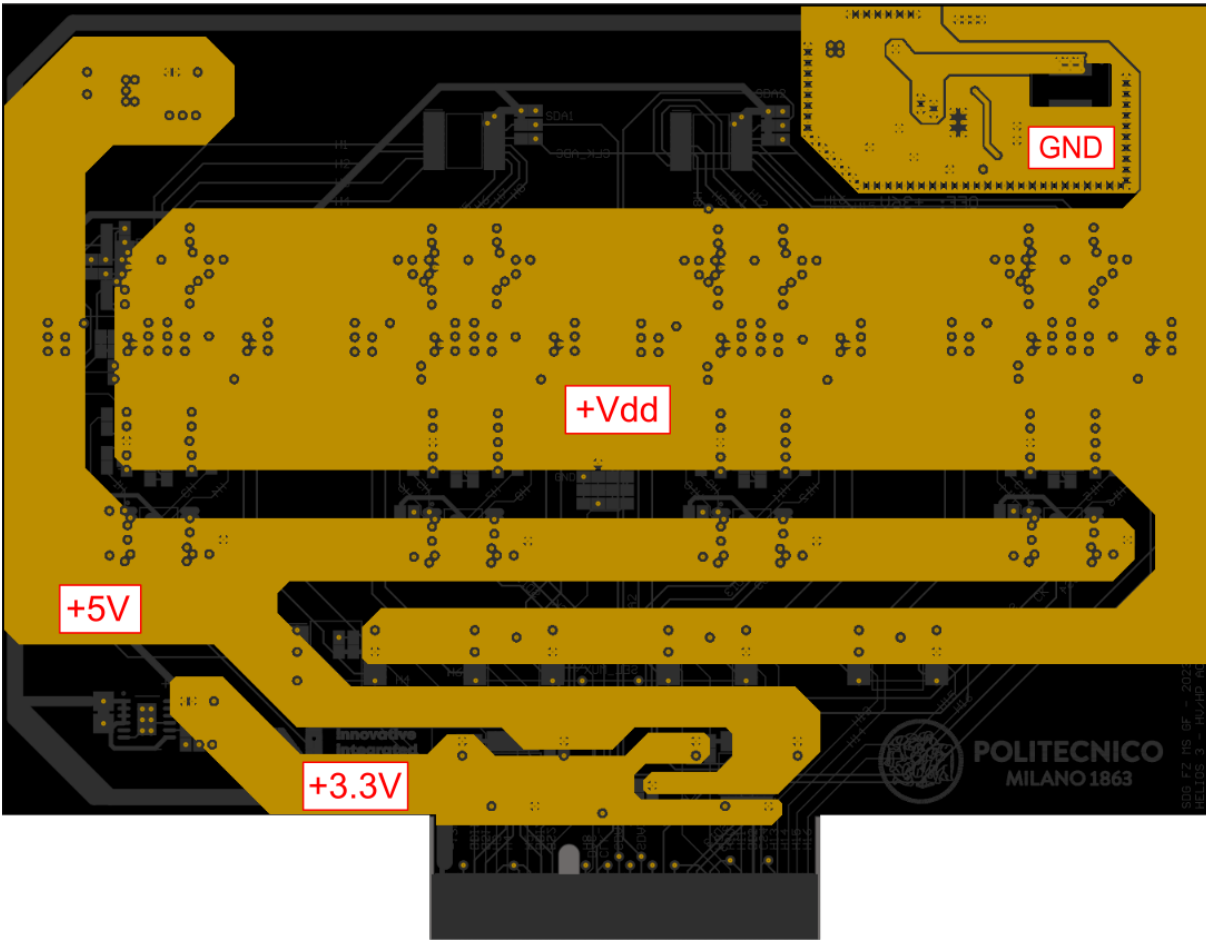
Figure 4.7: 2D view of the inner layer used as power supply layer.
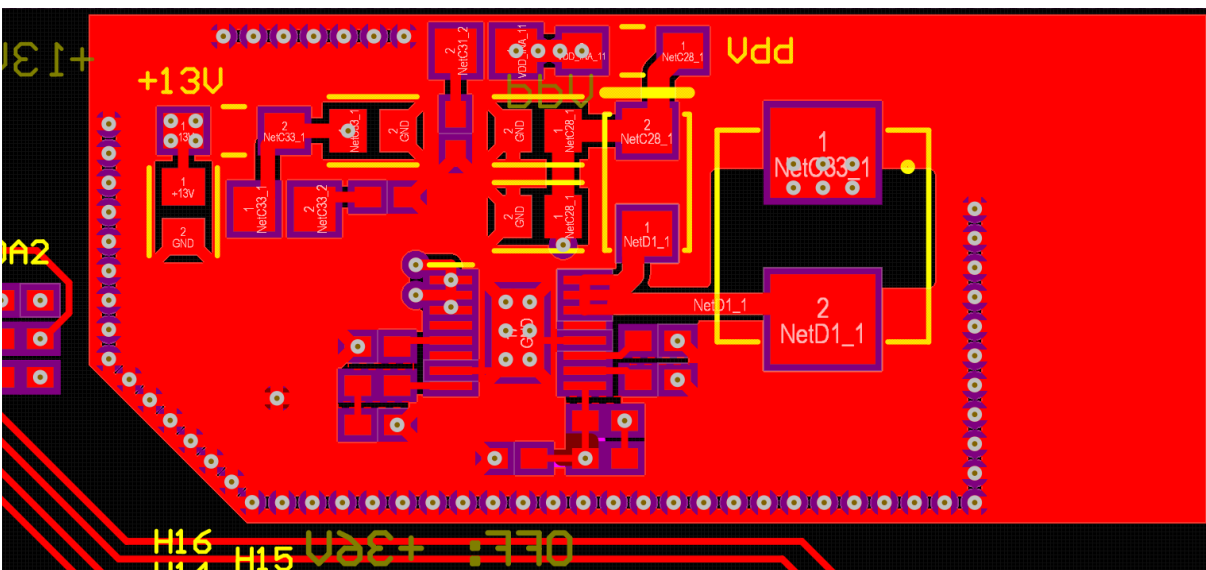
Figure 4.8: Boost converter layout.

4.4. Firmware

The FPGA firmware to control the actuation module has also been implemented. In particular, the FPGA communicates with the DACs and monitors the current delivered to actuators by reading the output of the ADCs. The VHDL firmware is described in the following sections.

4.4.1. DAC

As already mentioned in the previous section, DAC8565 is the component responsible of the generation of the analog signals that drive the actuators. This DAC features a stantard 3-wire SPI interface.

The Serial Peripheral Interface (SPI) is a serial communication protocol which governs the communication between a *master* device and several possible *slave* devices. In this case, the FPGA acts as the master device, controlling the start and the end of the transmission, while the four DACs of the module are the slaves. The SPI communication protocol is *synchronous*, since the data transfer speed and timing is determined by a clock signal. Considering the unidirectional communication between FPGA and DACs, the interface presents only three wires for each device:

- **Serial CLock (SCL)**: the master generates this signal, that controls how the data transfer is timed.

- **Serial Data In (SDI)**: the serial data line used by the master to send the digital words towards the slaves.

- **Chip Select (CS)**: when many peripherals are connected to the same SPI bus, this signal is used to select the receiver. By asserting this signal, the selected slave is notified that the communication is starting, allowing it to receive the transmitted data.

The FPGA executes an SPI write whenever new data must be sent to the DAC. First, the CS signal of the selected DAC is driven low to start the communication. The writing operation is then performed by sending a 24-bit digital word through the SDI line: as anticipated, 8 bits are needed to program the internal configuration register of each component, while the actual data is composed by the following 16 bits.

Table 4.5 shows the content of the DAC configuration register. Since each component features four converters inside the same package, bits D18 and D17 are continuously configured in order to select the actual output to be updated. Instead, bits D21 and D20

are always set to 0 and 1, respectively, indicating that the converters outputs need to be updated with the value stored in the data word.

D23	D22	D21	D20	D19	D18	D17	D16
0	0	LD1	LD0	0	DAC sel 1	DAC sel 0	0

Table 4.5: Structure of the control register in the SPI write protocol of DAC8565.

The firmware implemented to control the DAC consists of a Finite State Machine (FSM) with three states (fig. 4.9). The FSM is normally in the idle state, waiting for the start condition to begin the DAC update process. The signal 'Start DAC' is asserted when one or more of the DAC channels need to be updated, moving the FSM to the next state. Here, the channels to be updated are identified by comparing the new data word with the one previously sent and the corresponding instruction word are prepared. The FSM then moves to the transmission state, by pulling the CS low and by controlling the SDI line. When the transmission is completed, the instruction word of any other channel to be updated is fetched and transmitted, until all the channels that need to be programmed are reconfigured. In this way, an optimal throughput is guaranteed, since DC channels are updated only when the bias is modified and modulated signals are continuously set.
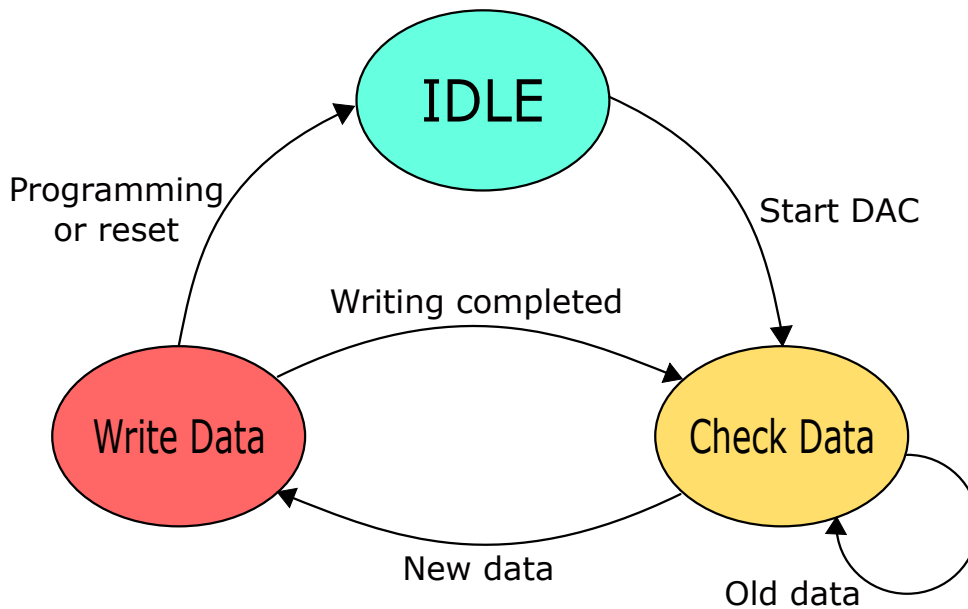
Figure 4.9: Scheme of Finite State Machine that handles the DAC8565 operation.

4.4.2.   ADC

The ADC used to monitor the current delivered to the actuators features 8 converters in the same package and communicates with the FPGA with an Inter Integrated Circuit (I^{2}C) interface.

I^{2}C is another serial communication protocol which uses only two lines:

- **Serial CLock (SCL)**: similar to SPI protocol, the clock signal is generated by the master device and it defines the transmission timing.

- **Serial DAta (SDA)**: this line is employed for the data transfer and it is bidirectional. It can be thus driven by both the master and the slave.

To allow a bidirectional communication using only one SDA line, the link is implemented with open-drain configuration: the master and the slave can only pull the SDA line low or leave it in high impedance state. An external pull-up resistor drives the line high when both master and slave release it. In this way, conflicts are avoided and there is no chance of creating a short circuit between VDD and ground.

A transmission is started by the master (FPGA) with a START condition (S), i.e. a low-to-high transition on SDA while SCL remains high. This command activates the slave. The FPGA then starts sending the clock to the ADCs on the SCL line. At the system startup, the ADCs is first initialized with a write instruction, as reported by fig. 4.10. In particular, the *scan mode* is selected, in order to cyclically convert all the 8 channels inside the component. The FPGA thus transmits an 8-bit write address, which is a string that identifies all MAX11615 devices and specifies that the subsequent operation is a write. The slave sends an acknowledgement bit towards the FPGA if it successfully receives a byte, by forcing the SDA line to a low level when the FPGA releases it. This mechanism is useful to establish if the ADC is available to receive data and if any fault has occurred. After receiving the acknowledgement, the FPGA sends a setup byte to configure the ADC in scan mode and waits for a new acknowledgement to conclude the communication.
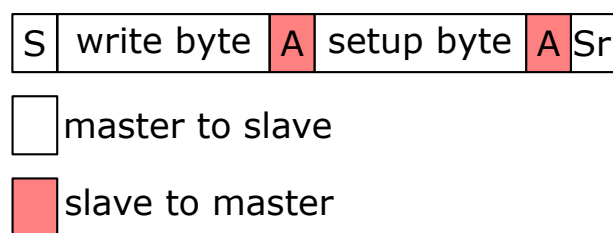
Figure 4.10: I^{2}C write protocol of MAX11615.

Since the configuration of the device is done only at the start-up, a repeated START

(Sr) condition can be generated by the FPGA to immediately start the readout of the ADC conversion without deactivating the bus. A read byte is sent from the FPGA to the ADC (fig. 4.11) to indicate that a read operation is being performed. After the acknowledgement bit, the FPGA reads from the slave the conversion result, which is formed by two bytes, and it sends an acknowledgement if every byte is received correctly. Considering that the ADC only has 12 bits resolution, the first four bits of the MSB byte are always zero. After scanning the eight channels, the master can give an acknowledge bit if it wants to start a new readout cycle or a not-acknowledge condition if it wants to end the communication. The first option is chosen to continuously monitor the eight channels.

| S | read byte | A | MSB byte | A | LSB byte | A |

x 8 channels
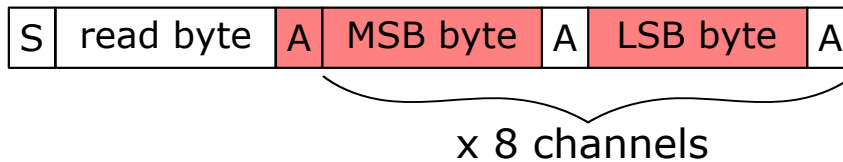
Figure 4.11: I²C read protocol of MAX11615.

4.5. Actuation module validation

The High Power-High Voltage module has been thoroughly validated. Proper interest was dedicated to the validation of the step-up converter, as well as of the whole actuation chain. In addition, the correct functioning of the firmware implemented to handle the operation of DACs, with the generation of DC bias and dithering signals, and ADCs, with the monitoring of the actuation current, has been verified.

4.5.1. Power supply measurement

The validation of the module started from the electrical characterization of the DC/DC converter employed to provide the high-voltage supply.

The start-up of the converter is regulated by a soft start circuitry, already explained in Chapter 2. Figure 4.12 shows the turn-on transient of the generated output voltage, for both cases of +24V and +36V. The two different power supplies reach the voltage regime in around 10ms, as defined by the soft start circuit. In addition, no overshoot is observed with respect to the steady-state voltage.

As already done in Chapter 3, the analysis of the ripple at the converters output (after the LC filter) has also been carried out. The measurement was first done by powering only the components of the module (48 'NCV20074' employed for drivers and INAs), not
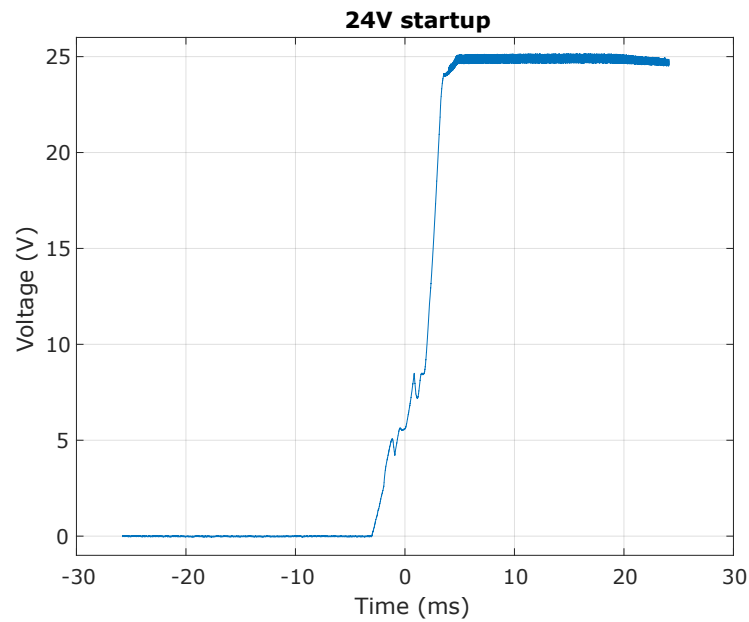
(a)
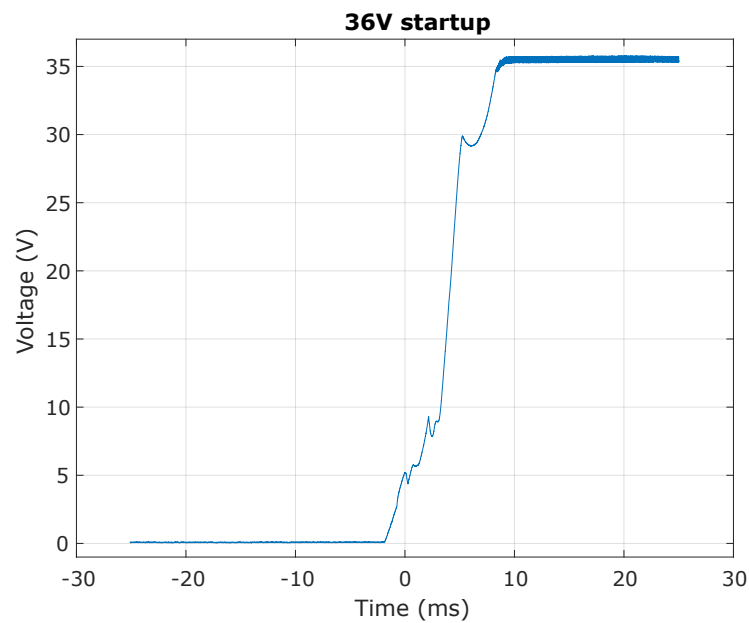
(b)

Figure 4.12: Start-up exponential behavior of the LT8362 when 24V (a) and 36V (b) are respectively generated.

evaluating the performance of the converters in their most power consuming configuration, i.e. the driving of 16 SiN heaters at the same time. The switching node waveforms, i.e. the voltage across the integrated switch of the converter, have first been monitored, as shown in Fig. 4.13 and Fig. 4.14. As expected, the measured voltage varies between 0V for

the on-period and $V_{out} + V_f$ for the off-period (V_f being voltage drop across the Schottky diode). The measurement also allows to assess the operation mode of the converter. At 24V the device works in Light Burst mode condition, with a switching frequency similar to the maximum selected one ($T_{sw} = 600ns$). Instead, at 36V the converter operates in Discontinuous Current Mode, since the switching frequency reaches 2 MHz.
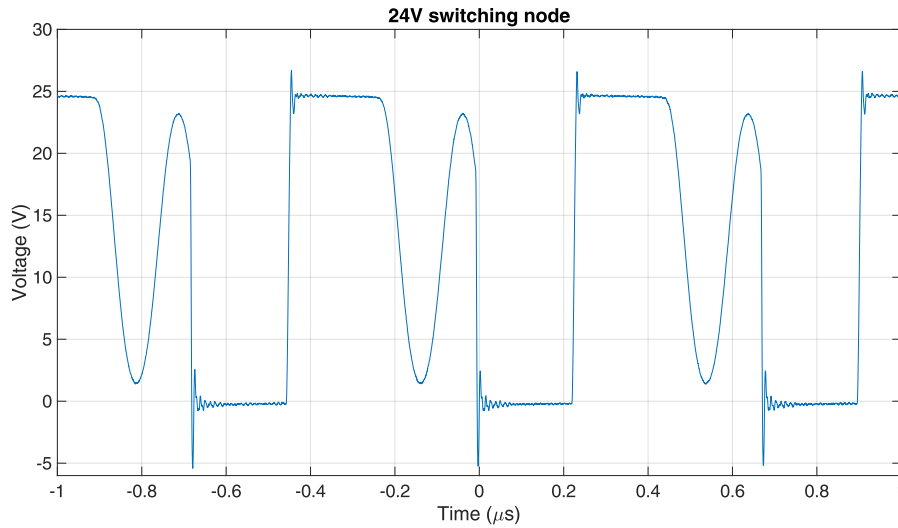
Figure 4.13: 24V waveform of the switching node.
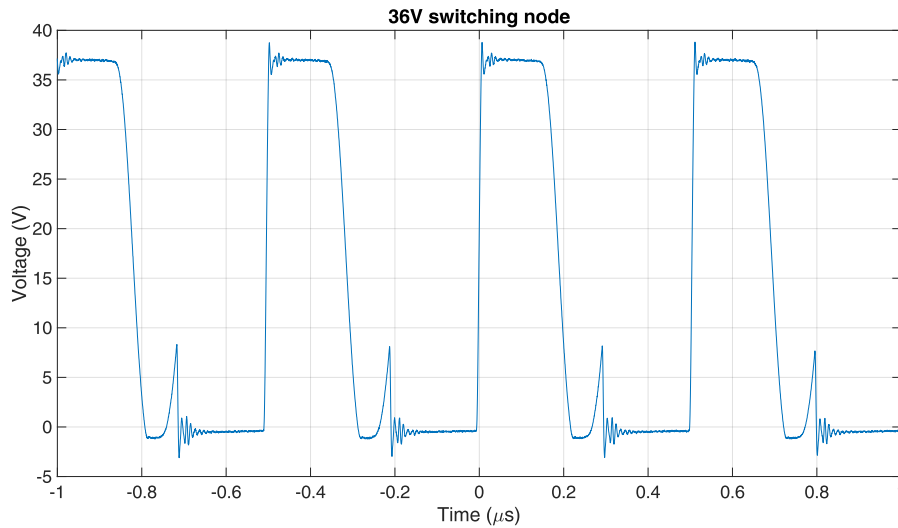
Figure 4.14: 36V waveform of the switching node.

The spectrum of the output waveform has also been acquired with a spectrum analyzer to investigate the ripple of the DC-DC converter, that could not be measured with the oscilloscope because of its really low amplitude. The measurement has been evaluated in CCM working regime for both output voltages, by connecting a load to the actuation chains.

The result is shown in Fig. 4.15 and Fig. 4.16. It is possible to see that the switching harmonics of the regulator, around 2 MHz, are suppressed by the output filter, resulting in a very small amplitude. It is thus possible to conclude that no detrimental effect on the actuation channels resolution is due to the employment of this boost converter.
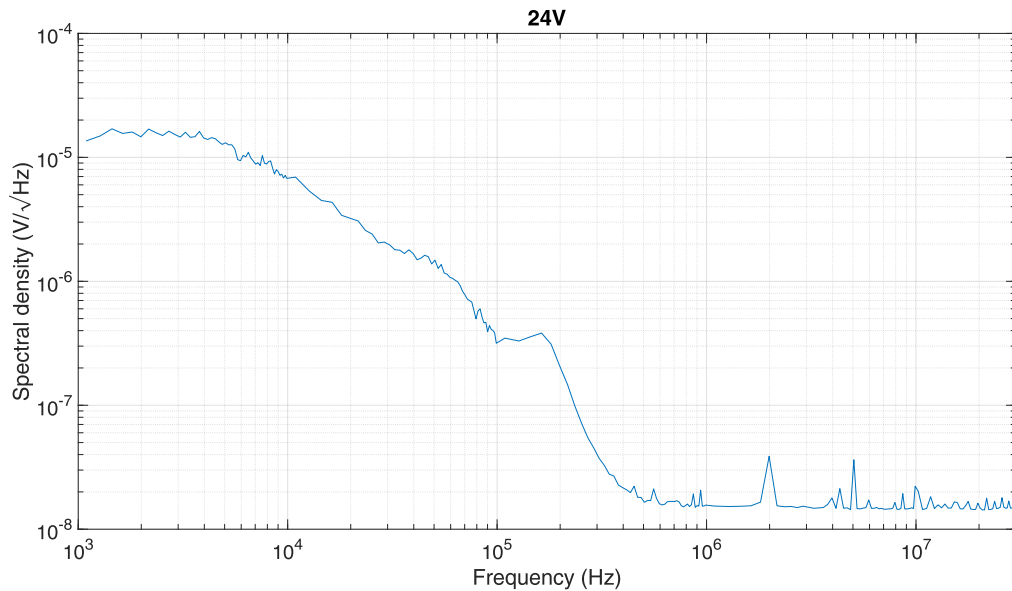
Figure 4.15: 24V power supply output spectral density when the converter is operating in CCM regime.
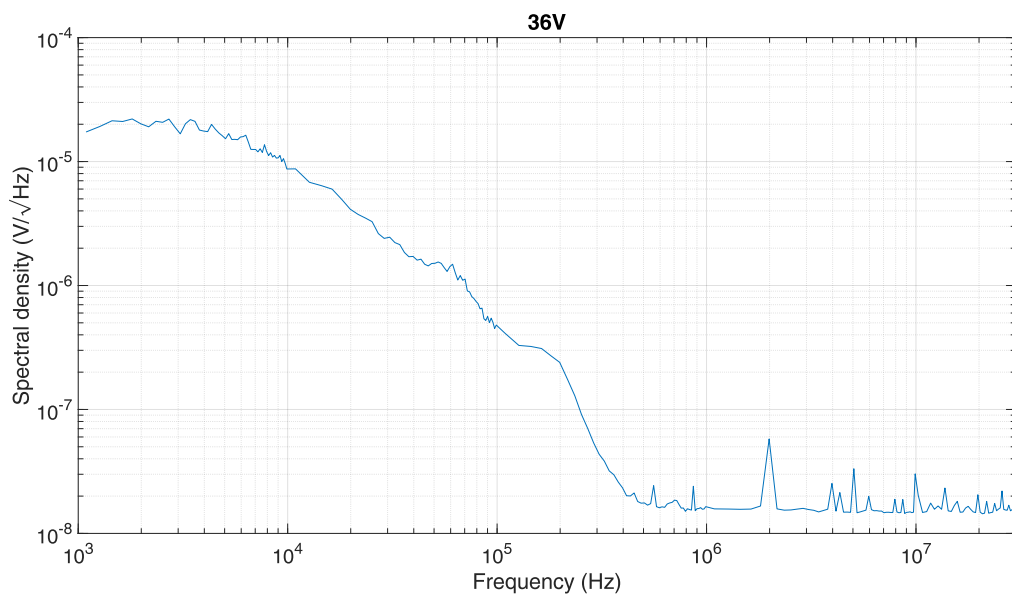
Figure 4.16: 36V power supply output spectral density when the converter is operating in CCM regime.

4.5.2.   Driver transfer function

The transfer function of the driver has been characterized in order to verify if the bandwidth is large enough to amplify the dithering frequencies,in the range of tens of kHz, without any impact on the amplitude and phase of the implemented circuit.

As mentioned, the gain of the stage is 12 to match the dynamics of the DAC to what required from the MEMS actuators (30V). Considering the amplifier GBWP of 3 MHz, the expected bandwidth of the driver is around 250 kHz. For this measurement, a network analyzer (E5061B, Agilent Technologies) has been employed, by injecting a voltage signal at the non-inverting node of the amplifier and detecting the corresponding signal at the output of the circuit.

As portrayed in Fig. 4.17, the transfer function is flat up to 250 kHz, perfectly matched to the system specifications and appropriate for the amplification of the dithering signals. No important variations on amplitude and phase are detected in the frequency range of interest, up to 100 kHz.
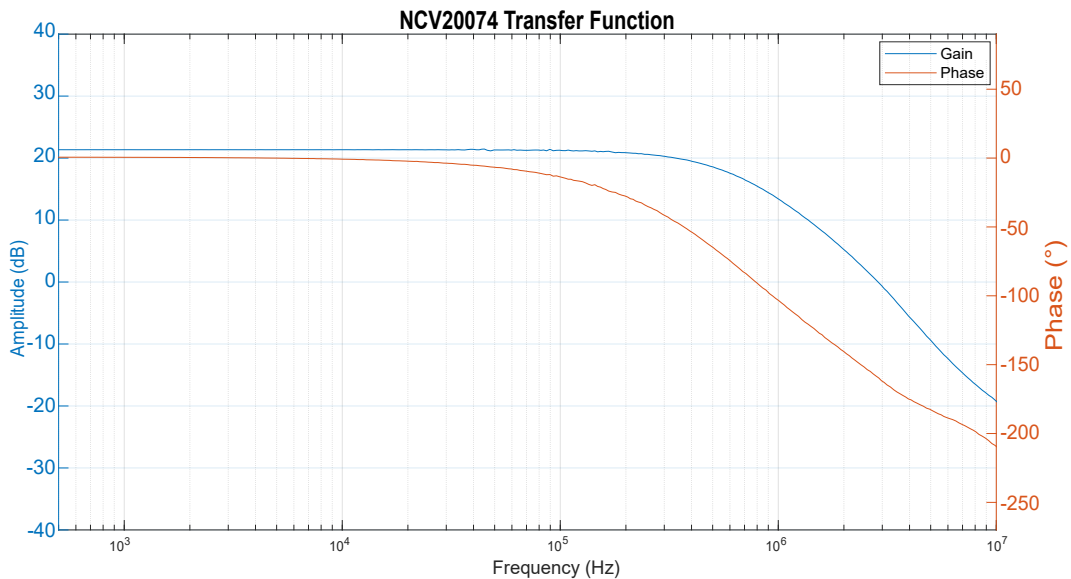
Figure 4.17: Magnitude and phase of the actuation gain circuit transfer function.

4.5.3.   Noise

The noise of the High Power-High Voltage actuation chain has been measured with the spectrum analyzer. In order to correctly evaluate the output spectral density, the DAC was turned on and a DC signal at mid dynamics was generated to drive the amplifier. This precaution was needed to avoid saturation of the driver output to ground, that would

have led to an incorrect measurement. Since the driver in this conditions generates 18V, an high pass filter has been connected in series to the output in order to correctly perform the measurement. Indeed, the spectrum analyzer can accept only small input DC values, up to 5V. The filter pole frequency was set to 100 Hz, setting the minimum valid frequency of the measurement.

According to the datasheet of DAC6585, the output spectral density for midscale code is $120\,nV/\sqrt{Hz}$ at 1 kHz and $100\,nV/\sqrt{Hz}$ at 1 MHz. Instead the driver stage input referred white voltage noise is $30\,nV/\sqrt{Hz}$. Taking into account this two values, which correspond to the most significant noise contributions of the circuit, the ultimate noise performance of the chain is correctly set by the DAC.

Figure 4.18 shows the measurement result over the frequency range of interest. An approximately white noise is observed at low frequency, that starts to decrease from around 250 kHz following the driver transfer function. At 1 kHz, the measured output noise spectral density is $1.5\,\mu V/\sqrt{Hz}$, which can be input referred by dividing it by the gain of the driver. The estimated input referred noise of the circuit results to be equal to the output spectral density of the DAC, confirming that the remaining components of the circuit have a negligible contribution to the overall noise of the actuation chain.
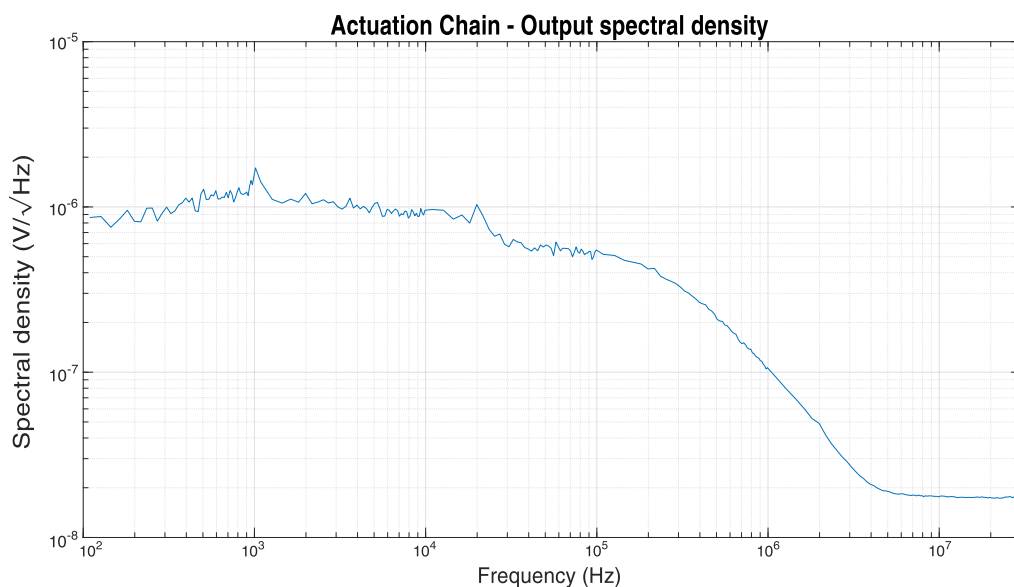
Figure 4.18: Output spectral density of the actuation chain when midscale code is generated by DAC8565.

4.5.4.   Startup output protection circuit

Next, the behaviour of the driver output node at the startup of the module has been investigated. As already introduced in the chapter, the protection switch located before the output node prevents issues related to voltage instabilities of the module components.

The measurement has been realized by connecting the module output to an oscilloscope, both with DC coupling of 50 Ω and DC coupling of 1 MΩ to model the low resistance of SiN heaters and the high impedance of MEMS actuators, respectively. The voltage before and after the protection switch has been simultaneously monitored.
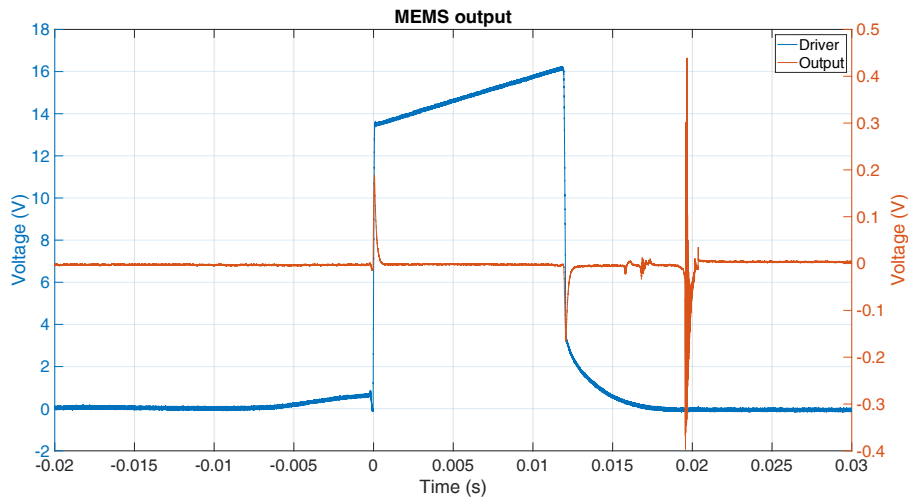
(a)
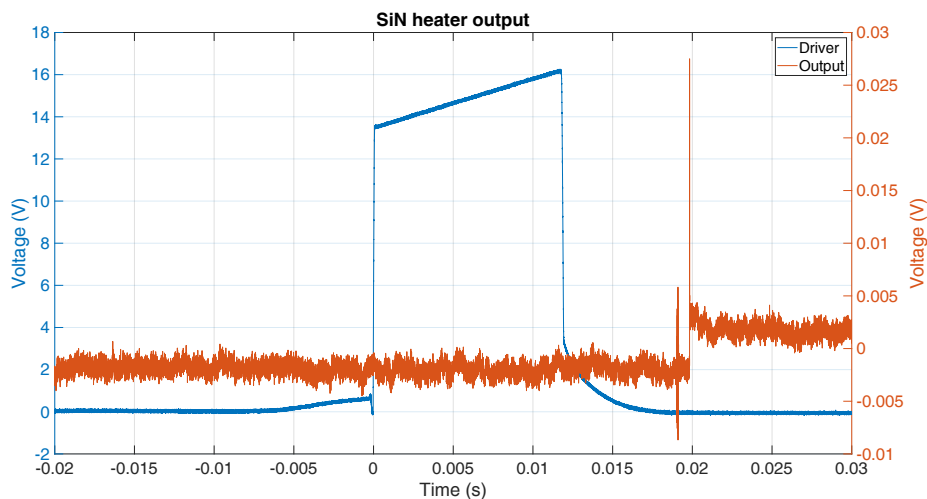
(b)

Figure 4.19: Waveforms before and after the output switch at the startup of the module when MEMS actuators (a) and SiN heaters (b) are used.

Figure 4.19a and 4.19b show the measurement result. Even though the DAC has been set to provide zero-scale output voltage at startup, this condition is reached after an initial transient, as it is possible to see from the figures. As a consequence, the voltage at the driver output reaches up to 16V during the startup, before correctly dropping to zero. This could lead to the damage of the actuators if this condition is not intended in their normal operations. The presence of the protection switch, that has been set to turn on after the initial transient, drastically mitigates this issue, reducing to few hundreds of millivolts the maximum output voltage at startup. Some voltage spikes can still be observed in the output waveform. For the MEMS case, a couple of spikes are visible in correspondence of the edges of the driver transient. They are due to the feed-through capacitance of the switches, that define the output voltage with a capacitive division together with the parasitics of the connections. The low impedance of heaters instead prevents this effect. Some fluctuations are also visible at around 0.2 s, due to residual instabilities of the power supply at the system startup. Even taking into account also these secondary undesired outcomes, the circuit can properly protect the actuators, since no relevant voltage oscillation can reach them.

Similar considerations can be done at the switch-off of the module, since in this phase the voltage at the output node is not properly controlled anymore. For this reason, the switch-off waveform at the output node has also been monitored. As shown in fig. 4.20, it is possible to compare the discharge of the output node of the driver and of the actuator
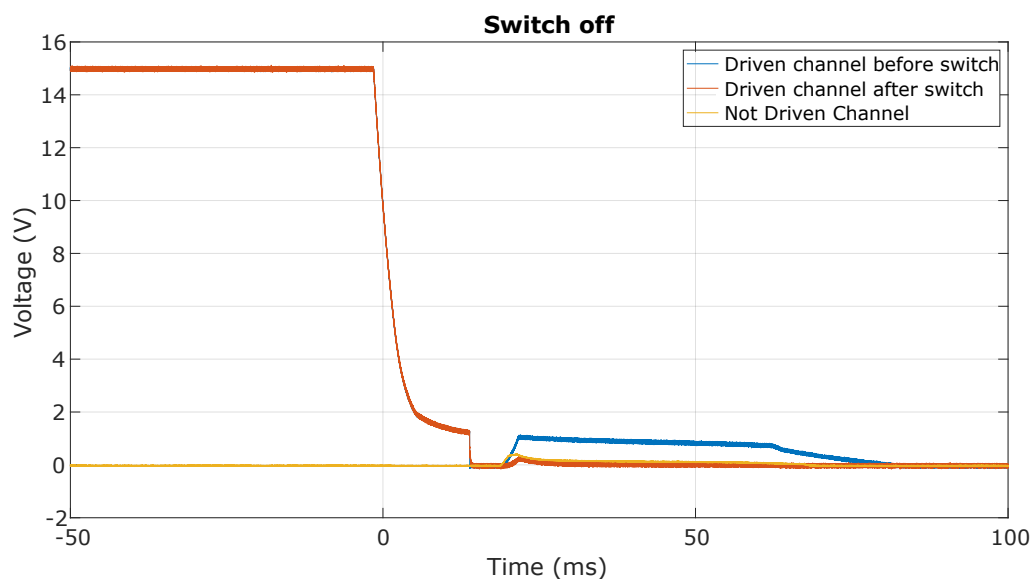
Figure 4.20: Switch off waveforms of the actuation node, before and after the protection switch in the case of active and unselected output channels.

node, both for channels that were actively driven before the switch-off and for unselected ones. As in the startup behaviour, the DAC presents an unwanted transient, that is correctly counteracted by the switch-off of the protection switch, happening 15 ms after the shut down of the power supply.

4.5.5. Generation of actuation signals

The end use of the module is to generate different types of driving signals to be applied to the actuators and perform the closed loop control of the photonic chip. The capability of generating arbitrary waveforms has thus been verified. The measurement has been conducted by reading with the oscilloscope the outputs of the module. To test the circuit in real actuation condition, a low resistance load has been connected to the output in order to assess the driving of SiN heaters, while a DC 1MΩ coupling has been used to check MEMS actuation. The two configurations have been tested with the two different power supplies (24V for heaters, 36V for MEMS).

A graphical user interface was created in order to configure the FPGA with the variables needed to generate all the 16 driving signals. The user can set a DC bias and enable the dithering modulation, adjusting its amplitude, frequency, and phase.

First, the driver capability of generating voltages close to the power supply has been investigated. Fig. 4.21 shows the output waveform with 24V supply when a DC bias of 21.5V is set and a dithering amplitude of 3.75V (one eighth of the voltage range of the
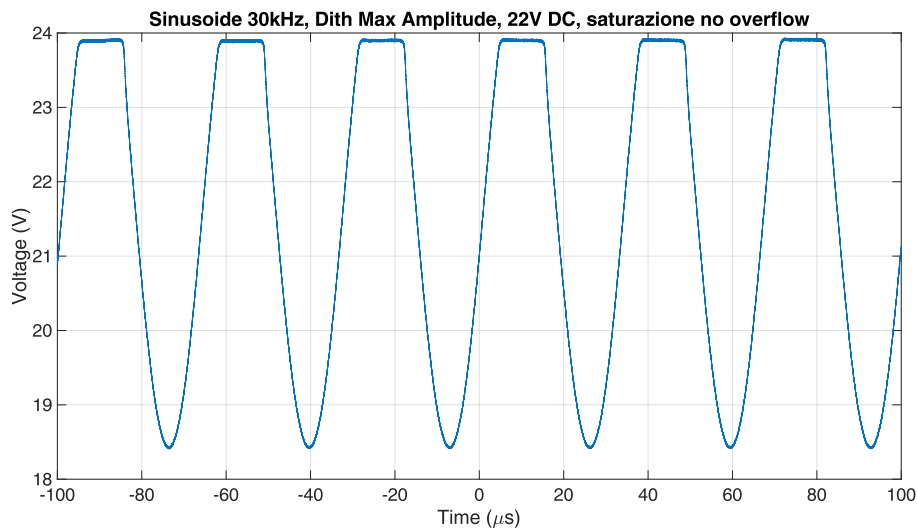
Figure 4.21: Sinusoidal modulation at 30 kHz close to 24V power supply with maximum amplitude dithering modulation and no overflow.
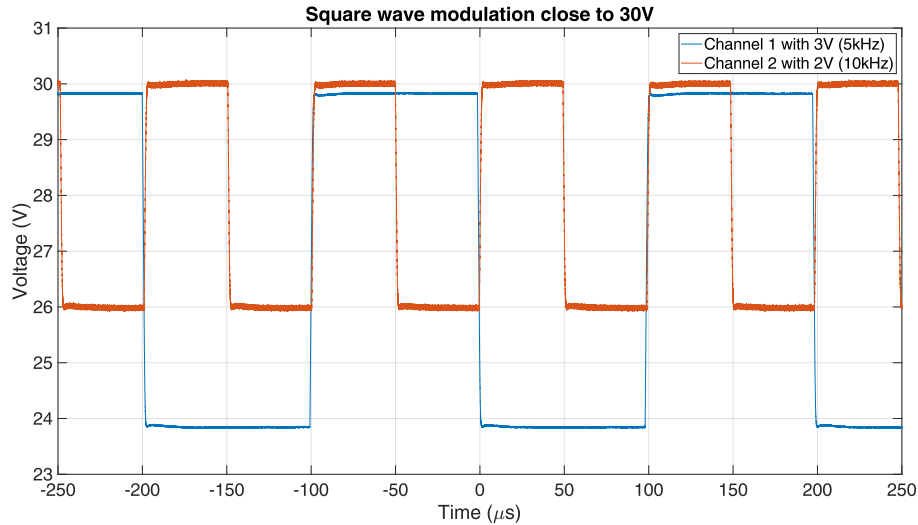
Figure 4.22: Square wave modulation of two channels close to 30V (maximum positive voltage)

driver) is selected. The waveform is correctly generated in the FPGA and provided to the module. Saturation of the circuit happens on the positive lobes of the sinusoid, at a voltage very close to the power supply, confirming the correct operation of the driver.

A similar measurement, shown in Figure 4.22, has been done for the case of MEMS structures. Here, the supply voltage has been increased to 36V and square waves at different amplitudes and frequency have been generated. It is possible to see that the driver is able to correctly generate these signals, with sharp transitions even at high amplitudes, and that up to 30V are correctly provided to the actuators.

4.5.6. Frequency spectrum of the generated signals

The frequency spectrum of the generated signals has been acquired with a spectrum analyzer, to investigate their spectral purity. The noise floor of the measurement, i.e. the statistical white noise generated by the circuit or the measurement device, is ultimately limited by the circuit noise performance, investigated in the previous sections.

Fig. 4.23 shows the spectrum of a sinusoidal wave with 2V amplitude and 10 kHz frequency. The presence of the higher order harmonics is due to the discretization performed by the direct digital synthesizer (DDS) in the FPGA to generate the DAC digital word. DAC8565 provides a conversion rate much larger than the 10 kHz frequency of this sinusoid, therefore the higher order harmonics have a much lower amplitude with respect to the fundamental tone (-66 dB attenuation).

Fig. 4.24 represents the spectrum of the square wave at 5 kHz with 3V amplitude. Ideally, only the odd harmonics should be present in the spectrum, correctly scaled by a factor equal to the harmonic number. Here, small tones are visible around each odd harmonic, due to residual phase noise that appears when generating square waves with digital synthesizers. In addition, small even harmonics appear in the spectrum since the duty cycle of the generated waveform is not precisely 50%. All these second order effects are 60 dB lower than the main tone, therefore they do not have relevant effect.
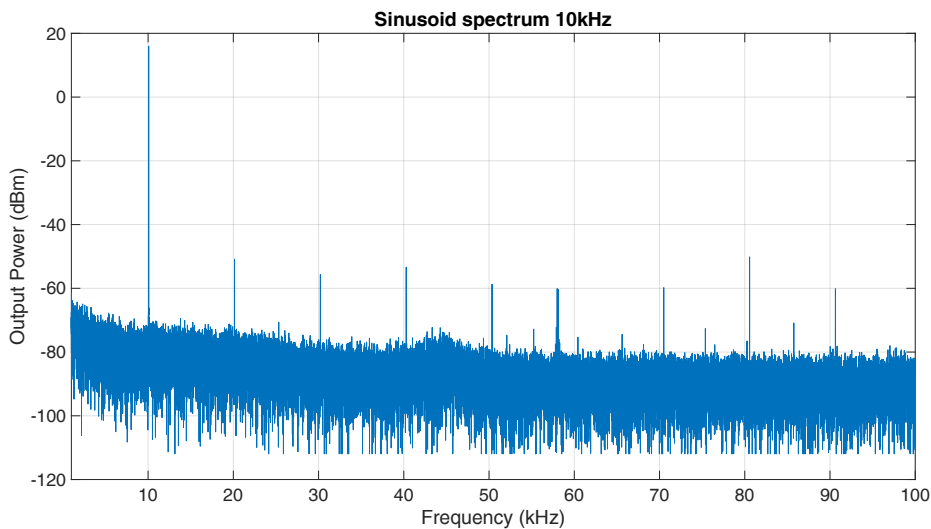
Figure 4.23: Frequency spectrum of a sinusoidal waveform at 10 kHz frequency and 2V amplitude.
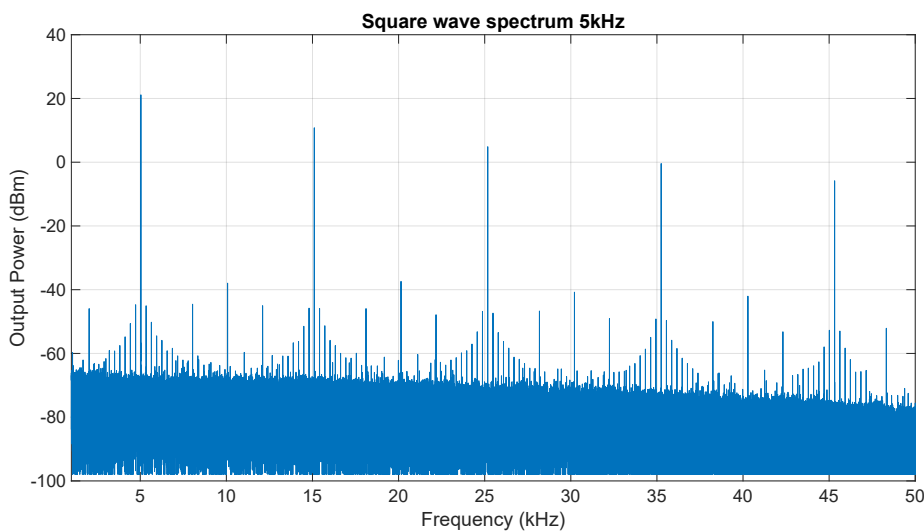
Figure 4.24: Frequency spectrum of a square wave at 5 kHz frequency and 3V amplitude

4.5.7. Current monitoring circuit

Finally, the validation of the current monitoring circuit has been performed. The I²C protocol which allows the communication between FPGA and ADC has first been tested, to ensure proper configuration and readout of the ADC. Then, the readout of the current flowing towards the actuator has been acquired by the FPGA and graphically shown by a custom-designed graphical user interface.

This measurement has been conducted with a power supply of 24V. Indeed, a precise current monitoring with the ADC is particularly relevant when SiN heaters are connected to the instrument, since in the case of MEMS no current is expected to flow and its monitoring is important just to detect faults. In any case, the choice of power supply does not influence the performance of the monitoring circuit.

First, the behaviour of the circuit has been checked by simultaneously probing with an oscilloscope the output of the driver and of the INA. Figure 4.25 shows the obtained result. The blue curve refers to the driver output waveform: in order to test the circuit near the maximum possible driving voltage, a signal with 18V DC level, modulated with an amplitude of 1V at a frequency of 2 kHz, has been generated. The SiN heater has been modeled with a 450Ω resistor connected to the drivers output, respecting the current limit that can be sourced by the circuit. Considering the generated waveform, the current flowing through the load has an average value around 40 mA, with a peak-to-peak mod-
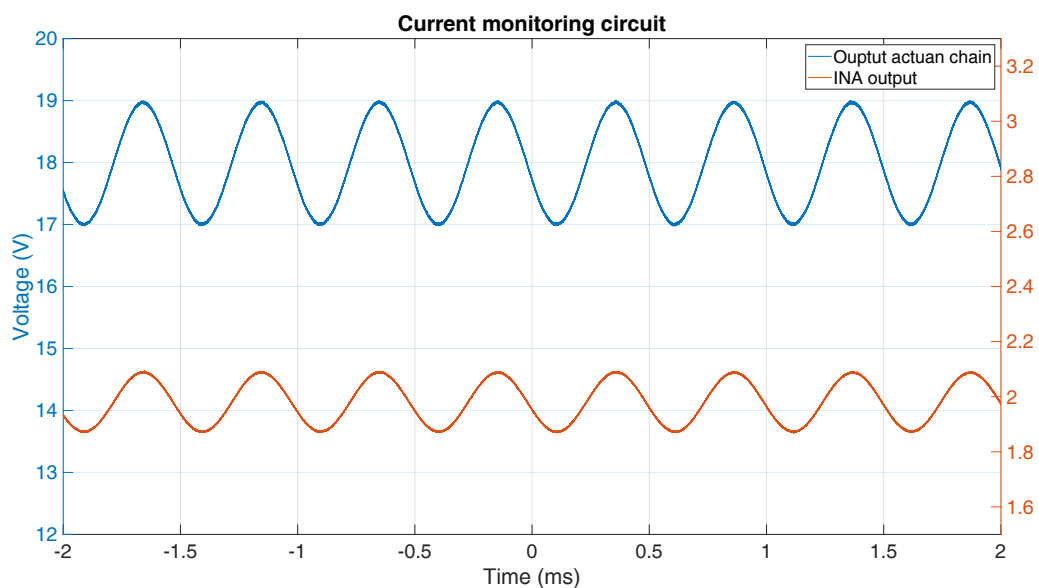
Figure 4.25: Current monitoring circuit: comparison of the output of the actuation chain and the INA output

ulation of 4 mA. The overall gain of the monitoring circuit from actuator current to INA output is 50 Ω, correctly resulting into the orange waveform shown in figure. The correct sizing of the circuit guarantees that the voltage dynamic of this signals always respects the limit imposed by the input range of MAX11615.

Finally, the INA output has been acquired with the ADC, transmitted to the FPGA and shown in the graphical user interface on a personal computer. The user interface has been programmed to convert the ADC input voltage into the actuators current level, conveniently displayed in a real-time graph. The measurement has been repeated in two different operating conditions, by first generating a DC signal and then a modulated one to drive the actuators. This allowed to test the ADC accuracy in both static and dynamic operations.

Figure 4.26 and Figure 4.27 show the sensed currents when two type of signals are generated by the DAC: for the DC waveform, the maximum actuation voltage of 20V has been applied, correctly translating into a current of 44 mA. Instead, the AC waveform has been generated with a 10V DC bias and 1V amplitude modulated at 800 Hz. The measurement confirms that the ADC can correctly measure and convert the INA output, in this case with a sample frequency of 11.6 ksps, and that the communication between the module and the FPGA is successful, thus validating the overall module operation.
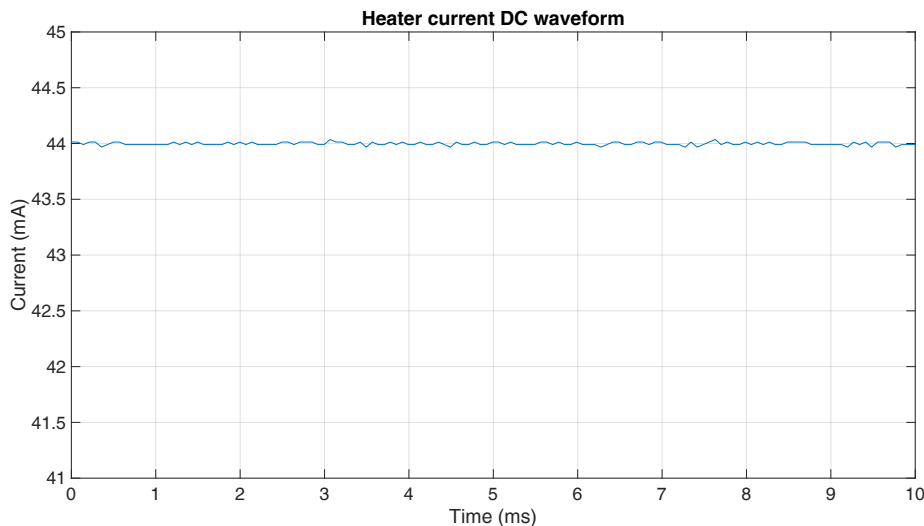
Figure 4.26: UI oscilloscope view of the sensed actuation current when a DC voltage is applied
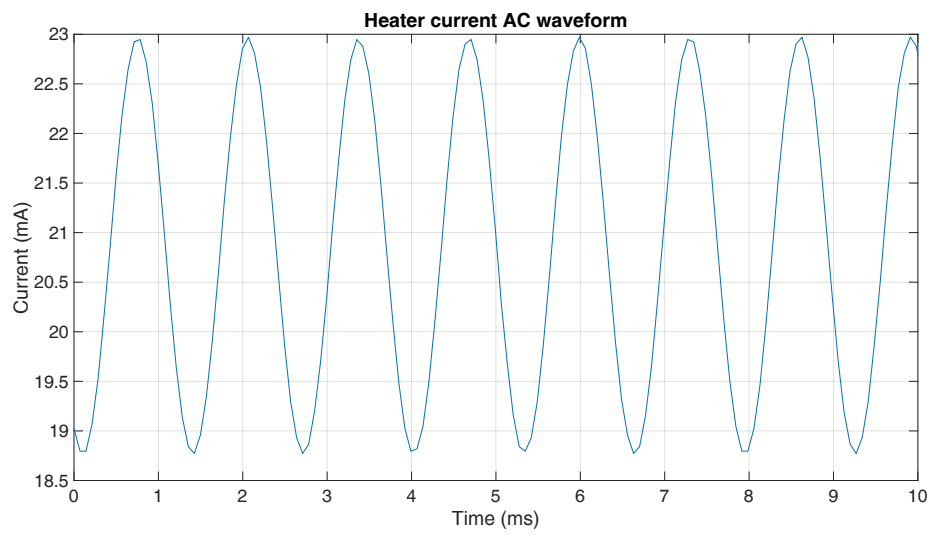
Figure 4.27: UI oscilloscope view of the sensed actuation current when an AC waveform is applied

5 | Conclusions and future developments

The purpose of this thesis was to complete the design of an electronic system able to perform closed-loop stabilization of the working point of multiple photonic devices, integrated in complex solid-state optical circuits. The focus of the activity was on the power optimization of the electronics, in order to efficiently handle large-scale photonic systems.

The real-time control action is implemented by monitoring the optical behaviour with on-chip photodetectors and by driving several integrated actuators, with the most appropriate feedback law. A custom electronic platform, Helios 3, has thus been developed, able to handle the tuning, control and reconfiguration of up to 144 photonic devices. To achieve this goal, a modular architecture, made of a motherboard completed by pluggable modules, has been exploited, enabling a complete reconfiguration of the electronic acquisition or actuation depending on the photonic architecture to be controlled.

Considering the abundant number of channels of the instrument, power optimization strategies have been considered in the electronic design. In particular, in the context of this thesis the power supply module of the whole system, which employs efficient DC/DC converters, has been designed and validated, together with a new pluggable actuation module, able to deliver high power performance and high voltage dynamics to heaters (specifically targeting the Silicon Nitride technological platform) and low-power actuators (as electrostatic or piezoelectric MEMS actuators). The full simulation, design and experimental validation of both circuits has been carried out.

The power supply module, which can accept and efficiently deliver up to 90W towards the whole electronic system, represents a significant improvement with respect to the power supply tree of the previous version, where a bulky benchtop power supply and power inefficient LDOs were employed. In this case, switching regulators are used to generate four different reference voltages, i.e. ± 6.5V and $\pm 13V$, providing stable power supplies to the all the circuitry employed on the motherboard and on the several pluggable modules. A dedicated buck converter also feeds the FPGA with a power supply voltage of 5V.

The design has been carried out taking into account the worst-case scenario in terms of power requirements, i.e. a motherboard equipped with six 24-channel actuation modules for heaters in silicon chips. In addition, dedicated filtering stages at the input and at the output of each switching regulator have been introduced in order to limit the EMI interference of the module and reduce the ripple amplitude of each power supply. Experimental measurements have been carried out, certifying the correct design and operation of the module.

Then, a new High Power-High Voltage actuation module has been designed and validated, able to simultaneously drive up to 16 innovative actuators. The module has been configured to generate single-ended voltages with variable amplitude and frequencies, needed for heaters in silicon nitride platforms or for MEMS phase shifters. In order to extend the voltage dynamics of the previous actuation module, a local boost converter has been employed, with the possibility of choosing two different power supply voltages (24V or 36V). The generation of actuation signals is made by a 2.5V DAC with 16 bit accuracy and 520 ksps sampling frequency, whose output is amplified of a factor 12 by a driving stage to reach up to 30V and simultaneously being able to deliver high amounts of current (up to 50mA). A monitoring circuit is exploited at the driver output to acquire the information of the current flowing towards the actuators: the voltage drop across a shunt resistor in series to the actuators is sensed by an instrumentation amplifier and acquired by 12 bit accuracy ADC. The driver output node is also connected/disconnected to the actuators through a protection switch activated only when the power supply of the module has reached a stable voltage level, preventing unwanted damages.

The complete electronics system is now ready to tune and reconfigure a far larger number of photonic devices than the prior generation, handling the control of really complex photonic circuits. The possibility of reconfiguring the entire system, by changing the number of channels dedicated to the readout and to the actuation depending on the different needs of the user, and of expanding its functionality by designing new pluggable modules, to handle new innovative types of sensors and actuators, are by far the most important features of the designed electronic system. In Fig. 5.1, the Helios 3 instrument, complete with the pluggable and the power supply modules, is shown.

Figure 5.1: Photograph of Helios 3 complete electronic system

5.0.1.   Future developments

Even though the whole electronic system has been electrically validated and it is showing its significant potentialities, the closed-loop control action has still to be analyzed and authenticated in actual photonic experiments. Helios 3 will be thus employed in challenging scientific experiments, enabling large-scale photonic systems to be tuned and controlled in a robust and reliable manner. This will require a complete synergy between the low-level hardware, the FPGA firmware and the user interface, in a multilevel framework. When fully operative, the instrument is expected to help in accelerating the adoption of photonic integrated technologies, from laboratory activities to commercial applications.

All the main building blocks of the system have been designed and the instrument is ready to be used, however its development can be further continued thanks to the modular structure. Other pluggable modules can be implemented, to acquire signals from other types of sensors or to drive different types of actuators, whenever required by particular applications or user needs.

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