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Executive Summary of the Thesis

Fabrication of spin-orbit logic devices by thermal nanolithography

Laurea Magistrale in Physics Engineering - Ingegneria Fisica

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1. Introduction

The energy consumption for information and communication technology infrastructures is constantly increasing and is predicted to reach 20% of the global energy consumption by 2030 [1]. This is due to the worldwide digitalization and the rise of technologies such as the Internet of Things (IoT), that drastically increase the volume of stored and processed data. The miniaturization of traditional silicon-based transistors is approaching its physical scaling limit, as the leakage currents become an issue as the channel length and the thickness of the gate dielectric is reduced to a few nanometers [2]. These trends call for architectures beyond the well-established CMOS platform, whose design and scaling to tens of nanometres is beneficial in terms of energy efficiency. A lot can also be done in terms of architectures: a well-know source of power dissipation is caused by the enormous data shuttling between the information processing units (*e.g.* CPU) and memory in standard configurations, where the two are physically separated. This known as the the 'von Neumann bottleneck' for computing that significantly affects the energy efficiency, besides limiting the overall speed. It is nowadays accepted that a new generation of nanosized devices must intrinsically address this point with non-volatility, and the processing and memory must coexist in the same physical space in order to overcome the von Neumann scheme and ensure reduced power consumption. To allow for non-volatile, interconnected devices, four important ingredients are needed: state switching, state retention,

Figure 1: Beyond-CMOS "Wheel of technologies" for state retention, state sensing, state switching and interconnects.

state sensing and interconnects. Fig. 1 summarizes the wide variety of promising possibilities that are being investigated for beyond CMOS architectures in laboratories worldwide, spanning from photonics to exotic quasi-particles. Information storing in a material's order parameter, such as ferromagnetism or ferroelectricity, could be solution for replacing or enhancing existing CMOS transistor, as suggested in 2018 by Intel [3]. In 2019, they also proposed a concept for a novel logic element called magneto-electric spin-orbit (MESO) device [4]. In order to meet the scaling requirements, ideally around and below 10 nm, for atto-joule class logic gates the thesis explored the nanofabrication of devices with an innovative lithographic technique: thermal scanning probe lithography (t-SPL). At the core of this innovative method of doing lithography there is an ultra-sharp heatable tip (similarly to that of an atomic force microscope) which is used for writing and simultaneously inspecting complex nanostructures. This approach, offers unique *in situ* imaging and nanoscale patterning without ultra high vacuum in contrast to the more standard electron beam lithography (EBL). Moreover, the heat stimulus can be used to directly induce chemical (*e.g.* temperature-induced topological phase transition) and physical modifications (*e.g.* magnetic/ferroelectric domain manipulation) locally at the nanoscale which could open a new array of possibilities when working with novel materials.
To reach 10 nm resolution capability, very complex processes including hard masks depositions and etchings are required. Instead, in the easier resist-based approach the resolution is typically limited to an ultimate 100-120 nm and above. Here I want to push forward the resolution achievable with a standard resist-based approach by engineering the thickness of the resist to reach a minimum feature size down to 50 nm or below, while keeping the fabrication process relatively simple and non-invasive.

2. Motivation: beyond CMOS with spin and polarization

The MESO device proposed by Intel (sketched in Fig. 2) includes a magnetoelectric switching capacitor, a ferromagnet and a spin-to-charge conversion module. The state retention is provided by a nanomagnet (FM), that can be switched

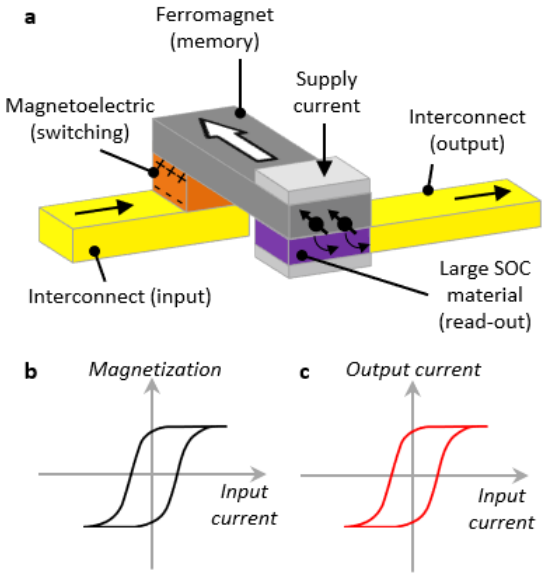


Figure 2: **(a)** MESO device formed with a magnetoelectric capacitor and a high SOC material stacked with a nanomagnet for state retention. **(b)** The magnetoelectric transfer function can change the magnetization direction of the ferromagnet. **(c)** The spin orbit module performs the conversion of spin to charge output.

by a magneto-electric (ME) capacitor. A suitable large spin-orbit coupling (SOC) material is used to transduce an injected spin current into an electrical one, allowing for readout of the magnetization state by inverse spin-Hall effect (ISHE) [5] and the inverse Rashba-Edelstein effect (IREE) [6]. Techniques for sensing magnetic states in spintronics usually rely on measurements of magnetoresistances but they do not generate an electromotive force (*i.e.* a voltage) or a current that can be used to drive other circuit elements connected to them in cascade. The MESO device exploits instead spin-to-charge conversion to allow communication with other electronic devices through charge and/or voltages. The efficiency of such process, being the current gain of the device, can be written as [7]:

$$G = \frac{I_{out}}{I_{in}} = \frac{\lambda_{eff}}{W_{FM}} \tag{1}$$

where λ_{eff} is an effective length that depends on the specific effect involved in the conversion, and W_{FM} is the width of the ferromagnetic injector (as sketched in fig.3). If the SCC mechanism is the spin Hall effect $\lambda_{eff} = \theta_{SH}\lambda_S$ where θ_{SH} is the spin Hall angle and λ_S is the spin dif-

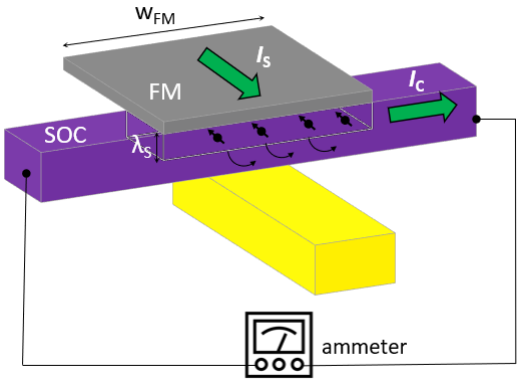


Figure 3: A ferromagnet injects a spin polarized current I_s into a high SOC material. The spin current is transformed in a transversal charge current I_c.

fusion length [8]. On the other hand, in the case of the Rashba-Edelstein effect $\lambda_{eff} = \alpha_R \tau/\hbar$ where α_R is the Rasha coefficient and τ is the mean scattering time [9]. These effects can happen in a large variety of large SOC materials, such as: heavy metals with λ_{eff} typically smaller then 1 nm [5], Bi_2Se_3 $\lambda_{eff} \sim 10$ nm [10], graphene/MoS_2 $\lambda_{eff} \sim 10$ nm [11], $LaAlO_3/SrTiO_3$ $\lambda_{eff} \sim 6$ nm [12] and ferroelectric Rashba semiconductors such as GeTe [13]($\lambda_{eff} \sim 1$ nm) and SnTe ($\lambda_{eff} \sim 5 - 10$ nm).

In order to make spin-orbit based devices such as the MESO logic, and according to the gain G reported in Eq. 1, two strategies are available: (1) the downscaling the FM nanostructure (W_{FM}) and (2) the exploitation of materials with sizeable λ_{eff}. *It turns out that such devices are advantageous whenever realized with materials owning λ_{eff} comparable with W_{FM}, the gain can become greater than unit and further increase with the down scaling of the device dimensions.*

To reach such goal, I employed the commercial *Nanofrazor Explorer* t-SPL system commercialized by *Heidelberg Instruments* (link: Heidelberg NanoFrazor) [14]. Being the *Nanofrazor* still in its infancy, the initial objective of this work was to fabricate proof of concept devices based on magnet/heavy metal bilayers [7], in order to optimize and push the Nanofrazor's process to reach the target minimum feature size for spin-orbit based devices.

3. Methodology

(a) (b)

Figure 4: **(a)** The Heidelberg NanoFrazor Explore is the first commercial t-SPL tool, with an hybrid direct laser sublimation and t-SPL patterning capability in a single tool. **(b)** Closed loop lithography concept.

The Polifab cleanroom hosts a *NanoFrazor Explore* (see Fig.4). This machine was employed to pattern the core of the device as it offers a series of key advantages in contrast with other lithographic techniques, as summarized below [15]:

1. *Heat* is an universal stimulus that can induce functional modifications to a wide range of materials without strict physical boundaries on the limit resolution. The landscape of possibilities is summarized in fig. 5.
2. The *absence of any high energy particle bombardment or extreme UV exposure* avoids the unwanted creation or scission of covalent bonds, lattice defects, vacancies or trapped charges. These damages are more evident when working with atomically-thin 2D materials, t-SPL can readily produce residual- and damage-free surfaces that lead to dramatic enhancements in device performance [16].
3. The t-SPL tip can perform surface imaging topography before, after and during patterning, similarly to what happens in standard atomic force microscopy (AFM).
4. The *in situ* reading capability allows straightforward marker-less alignment above existing structures or 2D material flakes (*e.g.* SnTe, MoS_2)
5. The whole system is compatible with am-

bient environments which means that an UHV chamber is not necessary.

6. The Nanofrazor offers an integrated optical tool in addition to its thermal tip, which can be employed to drastically increase the throughput when patterning optically feasible features.

t-SPL is compatible with standard etching procedures and could potentially be pushed to single-digit-nm spatial resolution, and, by multiplexing with thermal nanoprobe arrays, to higher throughput.

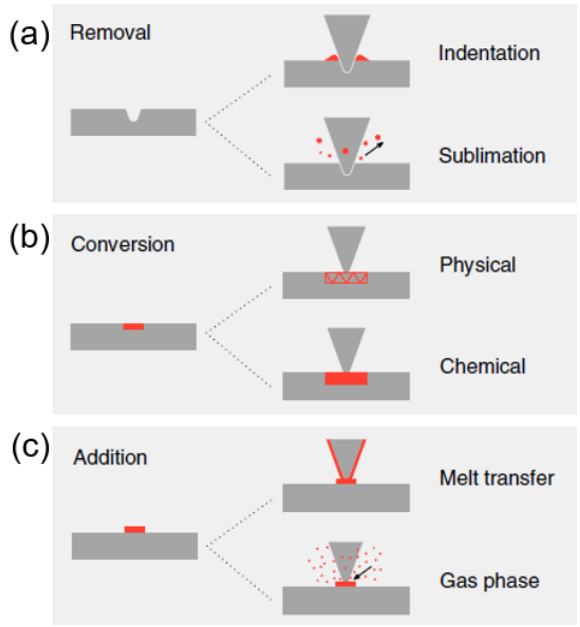


Figure 5: Applications of t-SPL, namely: **(a)** removal of material by thermomechanical indentation or sublimation of a sample material; **(b)** conversion of a sample by local modification of its physical properties such as the crystallinity or magnetic/ferroelectric dipole orientation, or chemical conversion; **(c)** addition of a functional material by melt transfer from a heated tip to the substrate or from a gas phase such as chemical vapor deposition of a precursor material

3.1. The bilayer lift-off process

The Nanofrazor was employed in the so called "bilayer lift-off process", which features a double polymer resist stack. Each step can be summarized as follows:

Writing. The Nanofrazor's hot tip or laser sublimate a thin thermal resist, *e.g.* PPA, on top of a lift-off resist layer, *e.g.* PMMA/MA (see Fig. 6a). The achievable resolution of the written

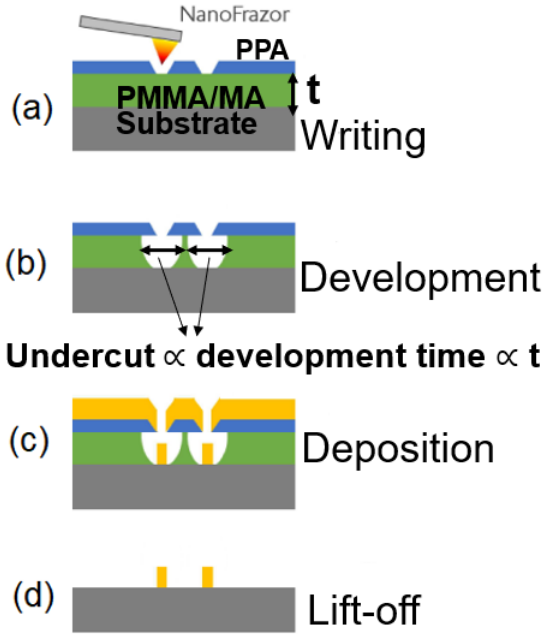


Figure 6: The bilayer lift-off process. **(a)** The NanoFrazor imprints a pattern on PPA. **(b)** The sample is developed in a solution and the pattern is transferred in the lift-off resist layer PMMA; wet isotropic processes lead to the so called "undercut". **(c)** A metallic thin film is deposited. **(d)** the sample is immersed in a polar solvent which removes the residual resist layers on the unwanted parts of the substrate.

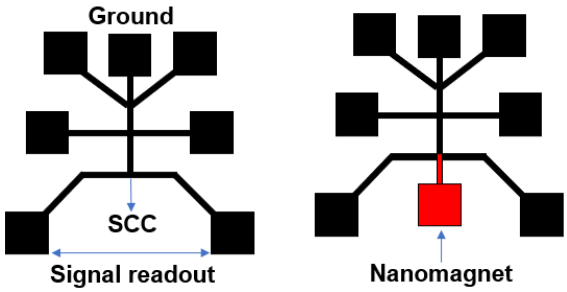
pattern mainly depends on the PPA thickness. This is because a thinner PPA allows to write at lower tip temperatures, limiting the heat diffusion. Furthermore, the conical shape of the tip leads to larger patterns for thicker PPA.

Development. After patterning the PPA with the Nanofrazor, the exposed PMMA/MA is dissolved in a wet mixture of deionized water and IPA. The development rate in this solution is estimated to be between 1 and 1.2 nm/s for exposed PMMA/MA. Being the etch isotropic, an undercut of the PMMA/MA develops under the PPA (see Fig.6b). *Undercut formation is the main factor limiting the resolution of this process*: the resulting metal lines will be wider and the minimum spacing between nearby features is restricted. *The thickness of the PMMA/MA determines the development time, hence reducing this parameter leads to a better resolution.*

Deposition. An additive or subtractive process is carried out (see Fig. 6c). It turns out that large undercuts might lead to a collapse of the

resist stack in some critical points of the structures during deposition.
Lift-off. Both the resist layers are stripped in a polar solvent such as acetone (see Fig. 6d). The pattern is finally transferred to the target material.
This process is claimed to be limited to a resolution of 100-120 nm and above by *Heidelberg*, but we noticed that it's not straightforward to reach 100 nm with a certain degree of reproducibility. The optimization approach that we followed in this thesis is the thinning of the PMMA/MA layer by properly diluting it with a solvent, leading to a smaller undercut (see Fig.6b). This allowed to push the resolution below 100 nm and improve reproducibility by avoiding mechanical instability of the resist stack during deposition.

4. Fabrication and results

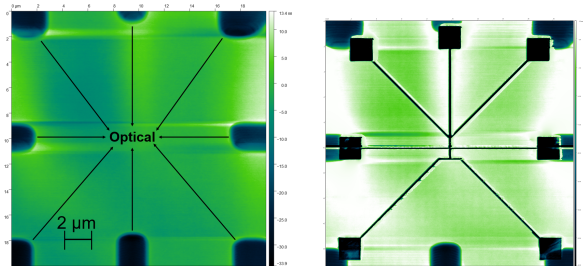


(a) (b)

Figure 7: **(a)** Heavy metal nanostructure, the spin-Hall signal is sensed at the bottom while the top pads can be used for resistive measurements; **(b)** Nanomagnet aligned on top for spin current injection.

A sketch of the devices fabricated in this thesis is shown in Fig. 7. The core of these devices (Fig. 7a) consists of an heavy metal (*e.g.* Pt or Ta) nanostructure which comprises a main channel grounded on one side, contacted with transversal Hall-bars for signal readout and longitudinal resistivity measurements. The longitudinal resistivity measurements are useful in the estimation of the expected spin-Hall signal. A nanomagnet (CoFeB or NiFe) has then to be patterned on top of the existing heavy metal structure (Fig. 7b). Realizing such a design by a bilayer lift-off process below 100 nm was not straightforward. The process was optimized to achieve a reasonable reproducibility with the following steps:

Writing and alignment. The Nanofrazor explorer is a closed loop lithography system that can adjust the hot tip writing parameters after each write line to get closer to the target sublimation depth in PPA. However, there are many parameters controllable by the user which can drastically impact the quality and accuracy of the resulting pattern (*e.g.* writing height, writing temperature). In order to achieve the desired geometries we had to fine tune each of these parameters. The *in-situ* imaging capabil-



(a) (b)

Figure 8: **(a)** *In situ* Nanofrazor reading of the laser pattern; **(b)** the t-SPL writing is then perfectly aligned because the reader and the writer circuits are integrated in the same cantilever.

ity of the Nanofrazor provides flawless overlay alignment with nanometric precision between t-SPL features. This was essential to pattern the nanomagnet exactly in the right position above the heavy metal nanostructure. The difficulties aroused when we tried to align optical features on the existing t-SPL patterns: the NanoFrazor allows to assign each section (called "fields") of the layout to either t-SPL or laser, this gives the advantage of increased throughput and prevents unnecessary tip wear out for optically feasible features. This characteristic was exploited, however the alignment between hybrid fields is far from perfect because the laser is not integrated in the cantilever. Due to the complexity of our design, it was impossible to align the laser features on top of the existing t-SPL ones in a reliable way. This problem was tackled by writing with the laser first and then reading/writing on top with the tip (see fig. 8).
Development and lift-off. When the bilayer lift-off was first applied with a standard PMMA/MA (*AR-P610.03* 3% solid content) 110-120 nm thick, we observed a very low lift-off yield on a lot of samples. Moreover, the ini-

tial resolution was not suitable to achieve the objectives of this thesis, due to the fact that the resulting nanostructures had a feature size of 120 nm and above. To improve with respect to this, we followed a meticulous optimization approach to reduce the critical size by reducing the thickness of the PMMA layer. As explained above, the undercut caused by the isotropic development limits the achievable resolution. The spinning speed was increased to 6000 rpm and this resulted in a thinner PMMA of about 100 nm. Then, the resist was diluted with a solvent (PGME) to reach 1% solid content. The dilution led to a 65 to 70 nm thick PMMA/MA. The reduced undercut led to a better reliability of the process and allowed to obtain 80 nm width lines. The better reliability is given by the fact that large undercuts caused mechanical instability of the resist stack in some critical points, leading to compromised structures after lift-off.
Combining Nanofrazor lithography with the bilayer lift-off process offers a very gentle and simple nanofabrication technique in which sample heating and damage by charged particles is avoided. However, the ultimate achievable resolution is limited by the isotropic etch usually to above 120 nm. Nevertheless, the wet etch gives the advantage of selectivity and the absence of hard masks. We demonstrated that it's possible to push the resolution down to 80 nm while keeping the process simple. In this regard, Fig. 9 shows the successful realization of complete devices with a critical dimension of 80 nm.

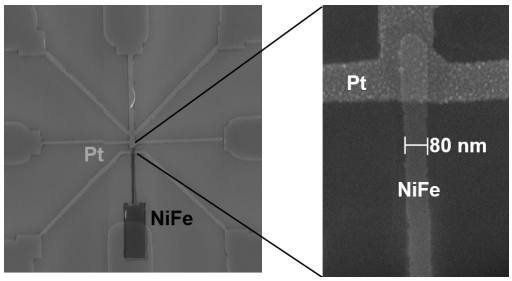


Figure 9: SEM immage of the finalized device.

5. Conclusions

The work behind this thesis was dedicated to achieving a 50 nm resolution with t-SPL and a solely resist-based approach, for future development of spin-orbit transduction devices. While extreme care must be used to avoid issues with this kind of process, we partially succeeded in pushing the resolution closer to 50 nm, overwhelming the 100-120 nm resolution declared as limit for this approach. In perspective, the resolution could be pushed in the 20 to 30 nm range with the bilayer lift-off process, employing a PPA of about 10 nm and a PMMA/MA of about 40 to 50 nm; considering the notable results we obtained by thinning the PMMA/MA only. The acquired knowledge on the practical operation of the machine and the process will be essential in the future in view of the use of 2D materials or thin films of FERSC that could be damaged by more invasive processes.

6. Acknowledgements

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