POLITECNICO
MILANO 1863

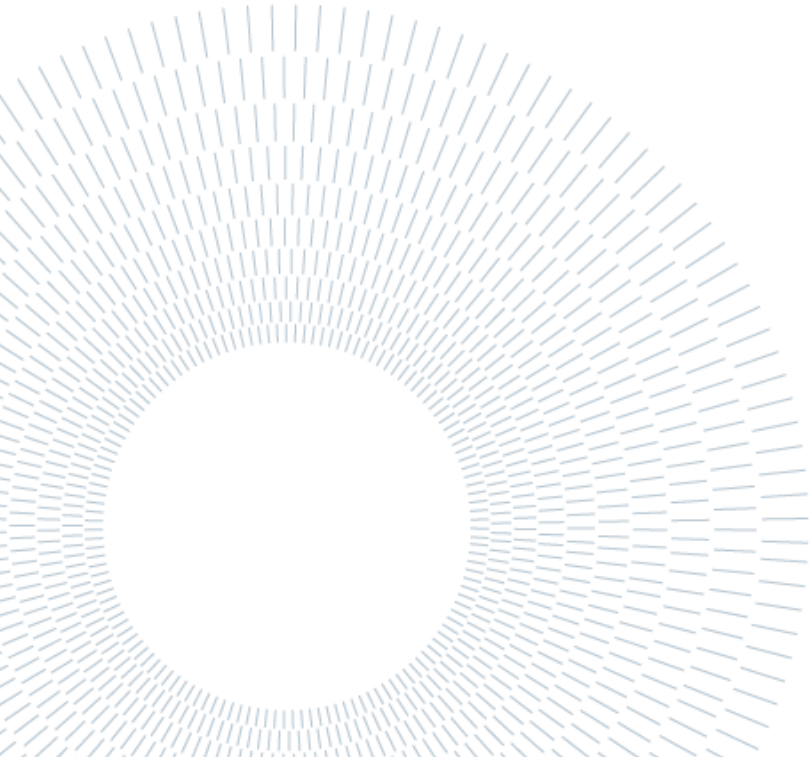
SCUOLA DI INGEGNERIA INDUSTRIALE
E DELL'INFORMAZIONE

Design and Validation of Planar Setups for the Characterization of TRISTAN Detectors

TESI DI LAUREA MAGISTRALE IN
ELECTRONICS ENGINEERING
INGEGNERIA ELETTRONICA

Author: **Alessio Pigliafreddo**

Student ID: 919734
Advisor: Prof. Marco Carminati
Co-advisor: Dr. Matteo Gugiatti
Academic Year: 2021-22



Abstract

The existence of sterile neutrino, a subatomic particle which is not affected by weak interaction but only interacts via gravitational forces, is proposed by many theories outside the Standard Model of particle physics. If its mass was in the keV range, it would be a viable dark matter candidate, which can solve many open questions in cosmology and astroparticle physics. The TRISTAN (Tritium Investigations on Sterile to Active Neutrino mixing) project aims at detecting a sterile neutrino signature by measuring the entire tritium β^- decay spectrum. To measure the imprint of sterile neutrinos, the TRISTAN project will extend the KATRIN (Karlsruhe Tritium Neutrino Experiment) setup with a new multi-pixel Silicon Drift Detector (SDD) system, which will have to be able to handle high signal rates with an excellent energy resolution.

In this context, this thesis focuses on the design and the subsequent validation of in-air and in-vacuum planar setups to characterize the SDD-based TRISTAN detectors. In particular, the first part of this work was devoted to the design, realization and testing of a bias system for the 166-pixel in-air setup. This bias system, called Lifeboard, allowed to perform the first X-ray spectroscopy measurements to characterize the 166-pixel SDD-based detector, which is a relevant milestone in this field. After these preliminary characterization measurements, a long time stability measurement has been performed to test the stability of the system in terms of energy resolution and channels gain as a function of time and temperature variations.

The last part of this thesis explains the reasons why a vacuum testing setup is needed and its main goals, illustrating the already existing in-vacuum 12-pixel setup located in the Department of Physics of Milano-Bicocca University. This part focuses on the importance of modelling the SDD detector response to electrons, which are here generated and accelerated against the detector by a photoelectric based electron gun, and it describes the backscattering mechanism. Understanding these interactions is fundamental for the final TRISTAN experiment to analyse the tritium β^- decay spectrum. The thesis work here regarded the development of a new vacuum-air interconnection system to move from the 12-pixel setup to the 47-pixel one. Finally, a description of all the improvements of the novel 47-pixel vacuum setup is reported alongside with the illustration of the new in-air interconnections and their mapping.

Key-words: neutrino, SDD, bias system, characterization, backscattering, vacuum-air interconnection.

Abstract in lingua italiana

L'esistenza del neutrino sterile, una particella subatomica che non viene influenzata dall'interazione debole ma interagisce solo tramite la forza di gravità, è sostenuta da diverse teorie che vanno oltre il Modello Standard della fisica delle particelle. Se la sua massa risultasse nel range dei keV, il neutrino sterile potrebbe essere un possibile candidato per la materia oscura e ciò potrebbe risolvere molte domande aperte riguardanti la cosmologia e la fisica delle astroparticelle. Il progetto TRISTAN (Tritium Investigations on Sterile to Active Neutrino mixing) mira a rilevare la firma del neutrino sterile misurando l'intero spettro del decadimento β^- del trizio. Per misurare l'effetto del neutrino sterile, il progetto TRISTAN estenderà il setup di KATRIN (Karlsruhe Tritium Neutrino Experiment) con un nuovo sistema multi-pixel di Silicon Drift Detectors (SDD), il quale dovrà essere in grado di gestire alti tassi di conteggio di segnali con un'eccellente risoluzione energetica.

In questo contesto, questa tesi si focalizza sulla progettazione e la successiva verifica dei setup planari in aria e in vuoto per caratterizzare i rilevatori a SDD di TRISTAN. In particolare, la prima parte di questo lavoro è stata dedicata alla progettazione, alla realizzazione ed ai test di un sistema di alimentazione per il setup in aria a 166-pixel. Questo sistema di alimentazione, chiamato Lifeboard, ha permesso di eseguire le prime misure di spettroscopia a raggi X per caratterizzare il rilevatore a 166-pixel basato su SDD, che è un traguardo importante in questo campo. Dopo queste misure preliminari di caratterizzazione, una lunga misura di stabilità è stata effettuata per testare la stabilità del sistema in termini di risoluzione energetica e di guadagno dei canali, in funzione del tempo e delle variazioni di temperatura.

La parte finale di questa tesi spiega le ragioni per cui è necessario un setup di test in vuoto e i suoi principali obiettivi, mostrando il setup in vuoto a 12-pixel già esistente ed ubicato nel Dipartimento di Fisica dell'Università di Milano-Bicocca. Questa parte si focalizza sull'importanza di modellizzare la risposta del rilevatore SDD agli elettroni, che qui sono generati ed accelerati contro il rilevatore da un cannone elettronico basato sull'effetto fotoelettrico, e descrive il meccanismo di backscattering. Comprendere queste interazioni è fondamentale per l'esperimento finale di TRISTAN al fine di analizzare lo spettro del decadimento β^- del trizio. Il lavoro di tesi qui ha

riguardato lo sviluppo di un nuovo sistema di interconnessione vuoto-aria per passare dal setup a 12-pixel a quello a 47-pixel. Infine, viene riportata una descrizione di tutti i miglioramenti del nuovo setup a 47-pixel, assieme all'illustrazione delle nuove interconnessioni in aria e le loro mappature.

Parole chiave: neutrino, SDD, sistema di alimentazione, caratterizzazione, backscattering, interconnessione vuoto-aria.

Contents

1. The TRISTAN Project

In this chapter a brief overview on neutrinos, their physics, and their role in the study of the dark matter will be given. A description of the KATRIN experiment, which is trying to find the active neutrino mass, is then given, showing the beamline components and its main results. Starting from KATRIN results, the TRISTAN project, which aims at detecting a keV-scale sterile neutrino signature, is illustrated giving a detailed description of its SDD based detector, of the readout ASIC and, finally, of the experiment roadmap.

1.1 Neutrino physics and dark matter

Dark matter is a hypothetical form of matter that does not emit electromagnetic radiations, but it only occurs through gravitational forces. This means that a direct observation of it is not possible, and it has been theorized to account for discrepancies between the current laws of physics and the experimental observations. The European Space Agency (ESA) *Planck space mission*, launched in 2009, has released the most accurate and detailed map ever made of the early moments of cosmic history [1]. According to this analysis [2], the estimate of dark matter content in the universe is 26.8%, while the dark energy should be 68.3%. The normal, visible, matter is only 4.9%, as illustrated in Figure 1.1. Up to now, the existence of the dark matter has never been experimentally proved. Nevertheless, many hypotheses on its origin have been proposed by different theories. In particular, since the dark matter almost does not interact with the normal matter and the electromagnetic radiation, a promising candidate, who can account for at least a part of the missing mass, is the neutrino.

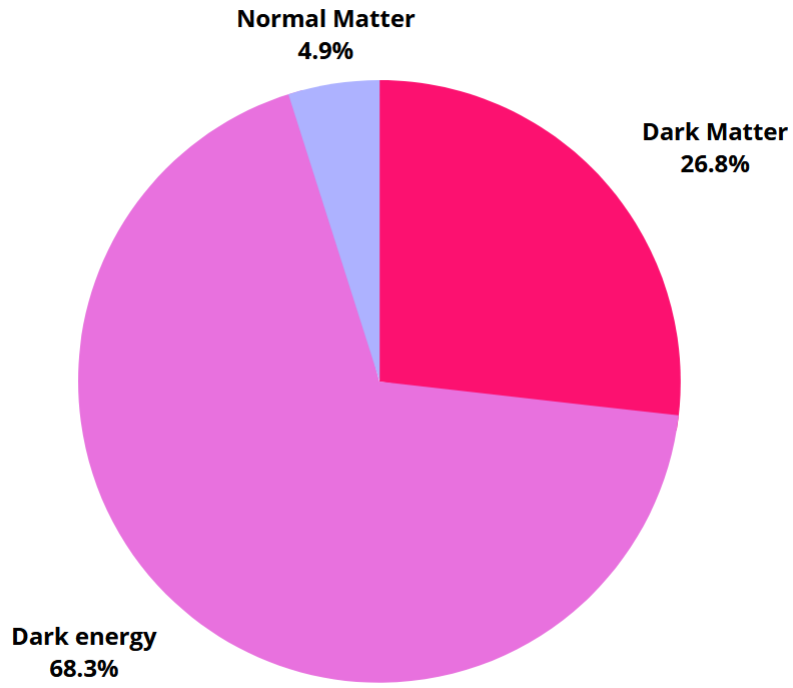


Figure 1.1: *Estimated distribution of mass-energy in the universe.*

Neutrinos are electrically neutral subatomic particles of the Standard Model of particle physics, with a mass at least six orders of magnitude smaller than the mass of an electron [3]. They do not interact with the strong nuclear force and are only weakly affected by the gravitational force and the weak nuclear force. The latter is responsible for the creation of neutrinos, in association with the corresponding charged lepton, in one of the three leptonic flavours: electron neutrinos (ν_e), muon neutrinos (ν_μ) and tau neutrinos (ν_τ) [4]. Each of these three types of neutrino (flavour eigenstates), can be described as a function of the three mass eigenstates (ν_1, ν_2 and ν_3) through the Pontecorvo-Maki-Nakagawa-Sakata (PMNS) unitary matrix [5], illustrated in Eq. (1.1).

$$\begin{bmatrix} \nu_e \\ \nu_\mu \\ \nu_\tau \end{bmatrix} = \begin{bmatrix} U_{e1} & U_{e2} & U_{e3} \\ U_{\mu 1} & U_{\mu 2} & U_{\mu 3} \\ U_{\tau 1} & U_{\tau 2} & U_{\tau 3} \end{bmatrix} \begin{bmatrix} \nu_1 \\ \nu_2 \\ \nu_3 \end{bmatrix} \tag{1.1}$$

Where $U_{\alpha i}$ represent the amplitude of the mass eigenstate to the flavour eigenstate. Despite a unitary three-by-three matrix has nine degrees of freedom, the PMNS matrix is commonly re-parametrised with only four parameters: three mixing angles (θ_{12}, θ_{23} and θ_{13}) and a phase parameter called δ_{CP}. Therefore, each neutrino of a certain flavour is a mixed state of neutrinos with distinct masses. This mass mixture is not constant over time, but it can change. In particular, the neutrino property of changing flavour, called neutrino oscillation, was firstly predicted by Bruno Pontecorvo in 1957. This property was confirmed by the Super-Kamiokande Observatory [6], earning the 2015 Physics Nobel Prize to Takaaki Kajita and Arthur McDonald for it [7]. This discovery made possible to assert that neutrinos are massive: indeed, to have a flavour oscillation, a difference in mass is needed, thus neutrinos must have a mass.

Up to now the neutrino is the only particle of the Standard Model which was observed exclusively with left-handed chirality, due to their interaction with the weak nuclear force. The chirality is an intrinsic quantum property of a particle, which determines whether or not it is subject to weak interaction. The existence of another type of neutrino, with right-handed chirality, has been hypothesised but not experimentally confirmed yet [8]. In opposition to left-handed neutrinos, which are called "active", these right-handed neutrinos are called "sterile neutrinos", since they interact just via gravity and not through any of the Standard Model's fundamental interactions. This new type of neutrinos is predicted to be significantly heavier than the active neutrinos, with which it can interact through oscillations [9]. The different types of neutrinos are summarized in Figure 1.2.

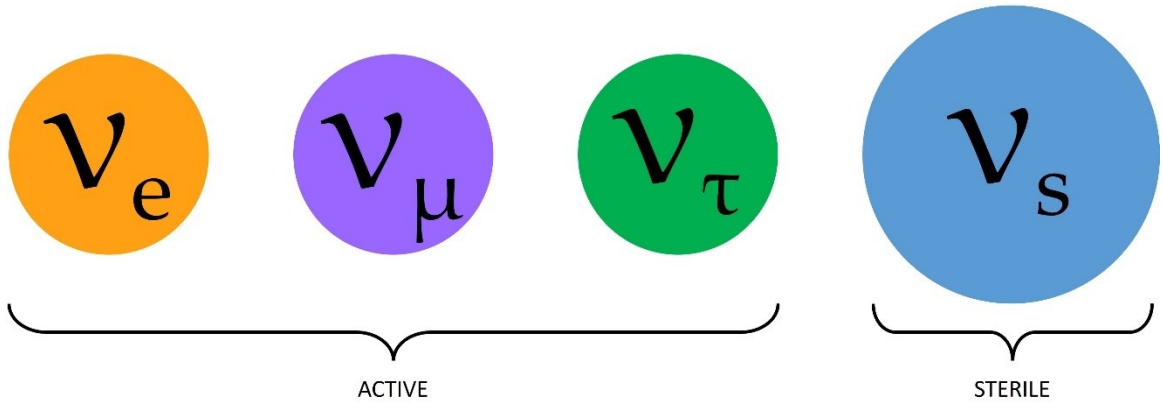


Figure 1.2: *Summary of the different types of neutrino.*

The smallness of active neutrino masses and some questions on their generation, are the main motivations why an extension of Standard Model, aiming to include a heavier neutrino flavour, is advocated by theoretical physicists. In particular, some observed

neutrino oscillation anomalies hint at the existence of sterile neutrinos at the eV scale, while some X-ray astrophysical observations could be due to the radiative decay of keV-scale sterile neutrinos, which may be good candidates for the dark matter [10]. Indeed, a particle that has a non-zero mass and no electromagnetic charge is a good candidate for it, but the active neutrinos have a too small mass to account for all the dark matter. Sterile neutrinos instead are potentially much more massive than the active ones, and so they may have a significant role in the dark matter [11].

1.2 The KATRIN experiment

After that neutrino oscillation experiments proved that neutrinos had a non-zero rest mass, the measure of neutrino absolute mass has become crucial in particle physics and cosmology fields. The KATRIN (KArlsruhe TRItium Neutrino) experiment [12], at the Karlsruhe Institute of Technology (KIT), is trying to measure the effective electron antineutrino mass by searching for a shift of the endpoint of the tritium β^- decay spectrum. The experiment employs molecular tritium gas as a radioactive source, due to its high activity and low endpoint energy of 18.6 keV, combined with an electrostatic high-pass energy filter of the MAC-E type [13]. This same method has already been employed in two previous neutrino mass experiments, Mainz [14] and Troitsk [15], both of which have been able to improve the upper limit of the electron antineutrino mass to $m_{\nu_e} < 2.2\ eV/c^2$. As mentioned before, the measurement principle of the KATRIN experiment is based on the tritium β^- decay. In particular, tritium decays spontaneously into ^3He emitting a fast energetic electron and an electron antineutrino, as shown in Figure 1.3. The energy released by the reaction is distributed between these two emitted particles. Specifically, this energy is divided into kinetic energy of electron and of antineutrino, rest mass of the electron and of the antineutrino.

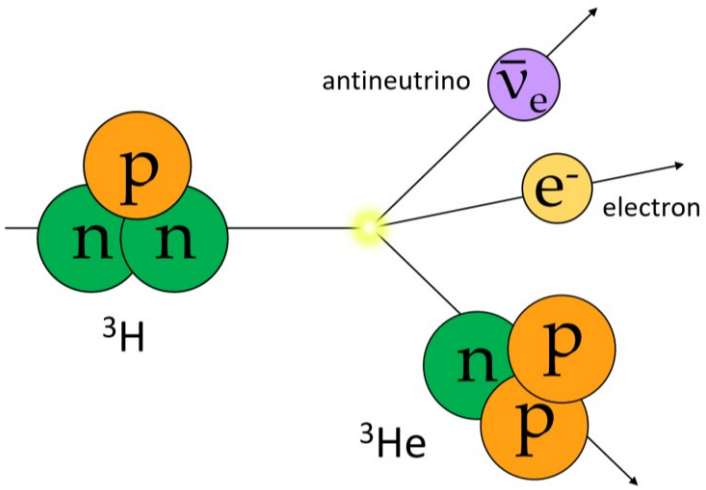


Figure 1.3: *Tritium β^- decay reaction.*

The rest mass of the electron (511 keV) and of the antineutrino are constant values, while the remaining energy is divided between the two particles kinetic energy based on a given statistics. So, through the high precision measurement of the electrons kinetic energy, focusing on the region near to the β^- decay endpoint energy E_0, it is possible to derive the antineutrino mass. The red line in Figure 1.4 represents the tritium β^- spectrum in the case of massless neutrino. In this case the endpoint energy reaches 18.6 keV. Instead, a non-zero neutrino mass decreases the electron endpoint energy and alters the shape of the beta spectrum. The fraction of β^- decays falling in the last 1 eV (grey area in the figure) is equal to 2×10^{-13}. Being a really low number, a huge tritium source luminosity and a very high energy resolution are needed.

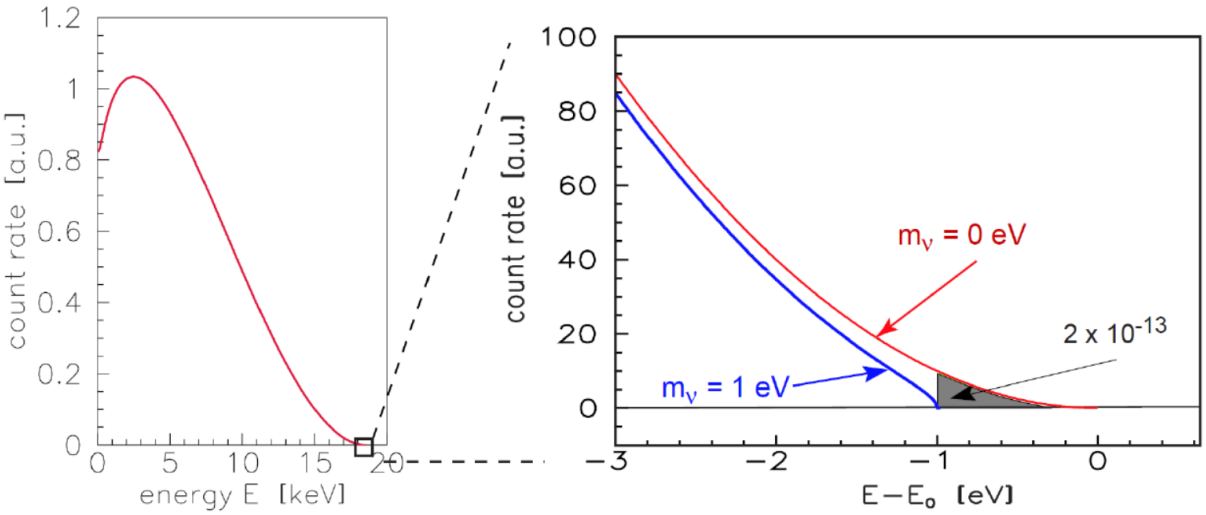


Figure 1.4: *Right plot: full tritium β^- spectrum with endpoint energy E_0 = 18.57 keV. Left plot: close-up view of the endpoint region in the case of m_{ν_e} = 0 eV/c^2 (red line) and m_{ν_e} = 1 eV/c^2 (blue line). Plot taken from Ref. [16].*

Since it is expected to have a sub-eV endpoint shift and the energy resolution of the experiment must be in the same range, a conventional semiconductor detector is not enough to resolve it. In order to solve this problem, a MAC-E filter, that combines electrodes with magnetic adiabatic collimation, have been designed.

As already mentioned, the MAC-E filter, shown in Figure 1.5, acts as a high-pass energy filter for electrons that are generated by the tritium source. This allows to filter them according to their energy, in order to count only the ones with an energy higher than a given threshold. In particular, the electrons emitted from the tritium source are collimated magnetically by the use of superconducting solenoid magnets, while the electrodes create an electrostatic retarding potential. Electrons with insufficient kinetic

energy are reflected back to the source, while those with sufficient energy to pass the filter are transmitted and counted by the detector.

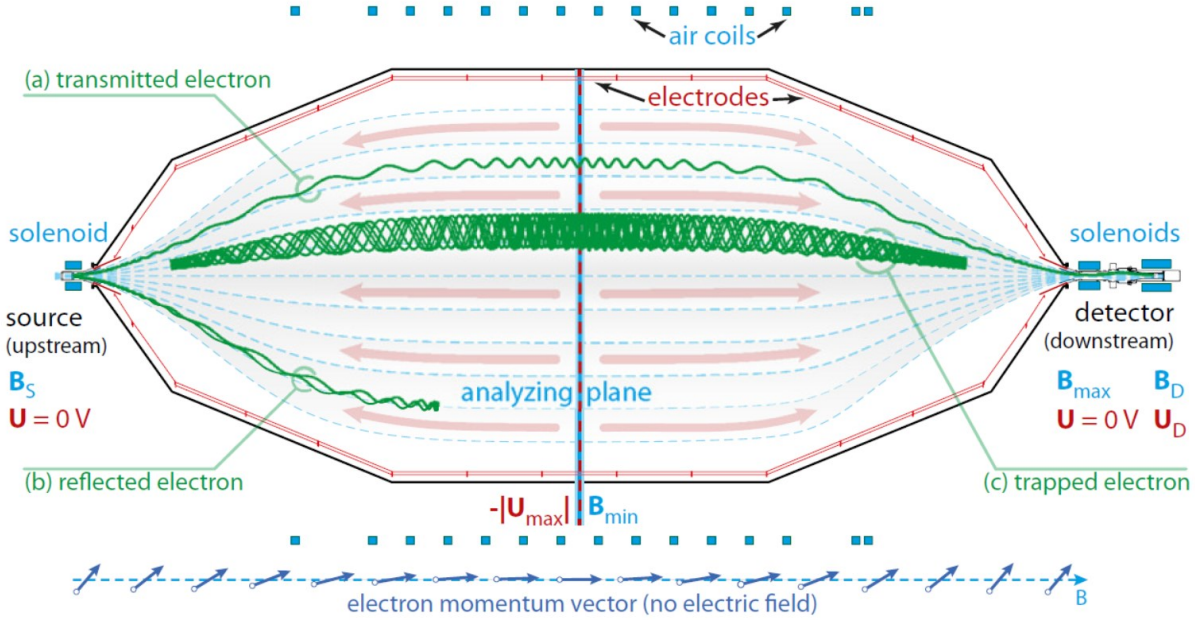


Figure 1.5: *Operation of the MAC-E filter. The electrons emitted from the source are being collimated by the magnets, while the retarding potential slows them down and analyses their kinetic energy. Figure taken from Ref. [17].*

The detector is a 5-inch-wafer monolithic silicon p-i-n diode with 148 pixels organized in a "dartboard" layout that gives spatial information. The detector has an energy resolution of 1.5 keV FWHM at 18.6 keV. A post-acceleration electrode, placed in front of the wafer, can be used to increase the energy of the electrons by up to 30 keV in order to shift the measured spectrum into a region with less background.

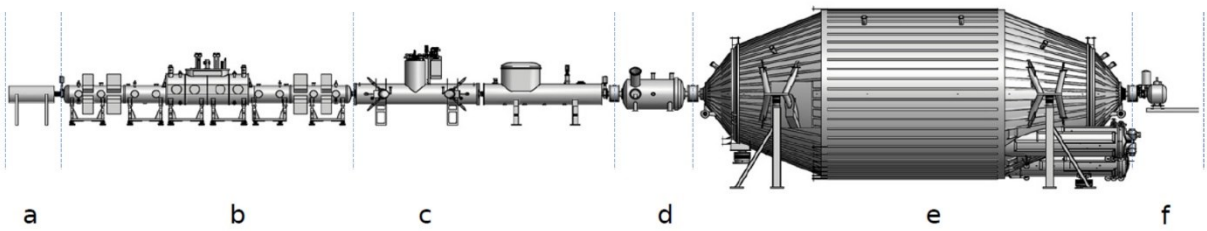


Figure 1.6: *KATRIN experiment beamline: (a) rear section; (b) windowless gaseous tritium source; (c) differential and cryogenic pumping section; (d) pre-spectrometer; (e) main MAC-E spectrometer; (f) focal plane detector. Figure taken from Ref. [18].*

Figure 1.6 illustrates the entire 70 m long KATRIN experiment beamline. Its main sections [19] are:

- **Rear Section:** on the beam line extremity opposite to the detector, it is installed a gold plated disk (called "rear wall") that defines the electrical potential of the gaseous tritium source U_s, with respect to the main spectrometer high voltage U. Gold material has been chosen because it has a lower probability of electron backscattering than stainless steel. In this way, almost all electrons reflected in the spectrometers eventually hit the rear wall where they recombine. The rear section also hosts a calibration e-gun and other diagnostic tools.

- **Windowless Gaseous Tritium Source (WGTS):** this section is a 10-m-long tube where gaseous tritium, with high isotopic purity (> 95%), at a temperature of 27 K is injected into the reactor in the middle of the tube and transported by diffusion for 5 m in both directions before most of the tritium will be pumped out by turbomolecular pumps (TMP). During the diffusion time inside the WGTS, some tritium molecules decay and the resulting β electrons are guided through the beamline. The remaining tritium, that has diffused and has been pumped by the TMPs, is later re-injected after a complex cleaning and purification process managed in closed loop by the Karlsruher Tritium Laboratory (TLK).

- **Transport Section:** this section is used both to drive the β electrons from the source to the spectrometer through a magnetic field generated by superconductive magnets, and to remove the tritium gas molecules through a differential pumping section and a cryogenic pumping section.

- **Pre-spectrometer:** the pre-spectrometer is a smaller MAC-E filter, placed in front of the Main Spectrometer, that acts as a first potential barrier used to reduce the number of electrons entering the main spectrometer. These low energy electrons, which are not useful for the study of the endpoint shift, are discarded, minimizing the measurement background.

- **Main Spectrometer:** the Main Spectrometer is employed to scan the kinetic energy of the β-electrons belonging to the region of interest (around 18.6 keV). It has a 0.93 eV energy resolution and, thanks to a negative electrical potential (*retarding potential*) in the centre of the spectrometer, acts as a high pass filter with an adjustable threshold. The electric field is generated by a system of electrodes, while the magnetic field is generated by superconducting magnets

and it guides the electrons toward the detector side. Both spectrometers work in Extreme High Vacuum conditions, with a pressure lower than 10^{-10} mbar.

- **Focal Plane Detector:** after travelling through the main spectrometer's retarding potential, the β electrons are re-accelerated to their original energy and magnetically directed to the focal plane detector (FPD), which is placed at the end of the beamline. As mentioned before, the detector is a 148-pixel pin-diode array on a monolithic silicon wafer. This detector has a FWHM energy resolution of about 1.4 keV at 18.6 keV. It is used to count the number of electrons that passed the filter and the maximum rate that this pin-based FPD can handle is about 100 kcps for the entire detector (~ 675 cps/px).

In addition to the two described spectrometers, a third one, called *Monitor Spectrometer* (MoS) is connected to the same high voltage of the main spectrometer, and it is used to monitor the voltage stability of the latter. It has an input of mono-energetic electrons coming from a ^{83m}Kr source that allows to measure the oscillation of supply voltage with high precision [20]. Being a replica in miniature of the KATRIN main spectrometer, the MoS has the same working principle and similar structure. Therefore, it is a very good place to test the first TRISTAN detector prototypes, as will be described later on.

Finally, recent studies on the KATRIN measurements resulted in the determination of an upper limit of 1.1 eV (with 90% confidence level) on the absolute mass scale of neutrinos [21].

1.3 The TRISTAN experiment

1.3.1 Sterile neutrino search

The TRISTAN project (TRitium Investigation on STerile to Active Neutrino mixing) is an extension of the KATRIN physics program. The plan is to make use of the KATRIN high-resolution spectrometer and its beamline. The aim of TRISTAN is to search for the signature of sterile neutrinos with masses in the keV range by measuring the entire tritium β^- decay spectrum.

The electron antineutrino generated by the tritium decay is given by the superposition of the three different neutrino mass eigenstates. As discussed before, the existence of another eigenstate in the order of keV, called sterile neutrino, have been suggested by some observations. Looking at the tritium β^- decay spectrum: the active neutrinos produce a distortion close to the endpoint energy E_0 = 18.57 keV; the superposition of this hypothetical sterile neutrino instead would result in the presence of a kink at

$E_{kink} = E_0 - m_s$ in the tritium spectrum, with m_s being the sterile neutrino mass, as shown in Figure 1.7. The distance of the "kink like" signature from the endpoint region is equal to the mass of the sterile neutrino.

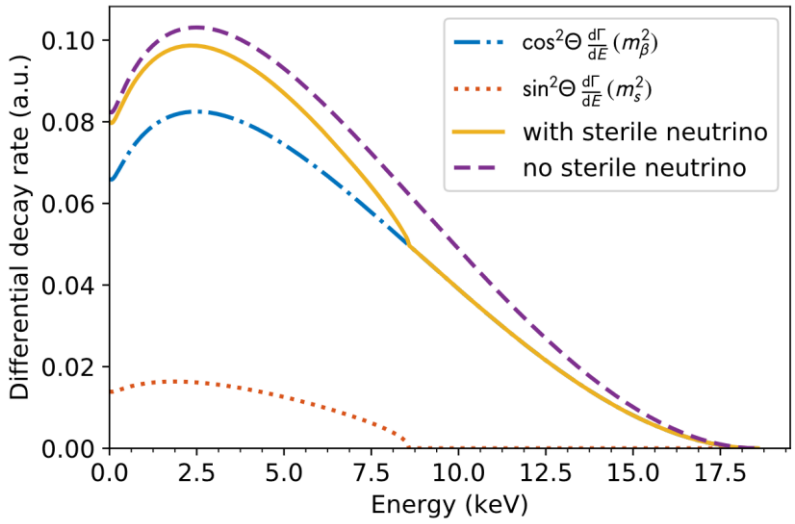


Figure 1.7: *Entire tritium β^- decay spectrum in case of sterile neutrino with m_s = 10 keV and unphysically high mixing angle of $\sin^2(\vartheta)$ = 0.2. The blue dashed-dotted line represents the decay branch into a light active neutrino, while the orange dotted line is the decay branch into a sterile neutrino. The solid yellow line is given by the two spectra superimposed, showing the kink-like distortion. Finally, the purple dashed line represents the spectrum without sterile neutrino. Figure adapted from Ref. [22].*

The two main advantages of the KATRIN setup for the research of the sterile neutrino are the very high β electrons generation rate given by the tritium reaction, which allows to obtain the high statistics necessary for the measurement, and the tritium endpoint energy (E_0 = 18.57 keV), which allows to probe the existence of a keV-scale sterile neutrino up to a mass m_s = 18.57 keV/c^2.

Differently from the KATRIN experiment, to search for the keV-scale sterile neutrinos the spectrum measurement interval must be extended to cover the entire energy range. This requires to set the spectrometer energy threshold to much lower levels than in regular operation [23]. With such a new operation modality, the number of electrons driven to the detector will be several orders of magnitude higher than the standard KATRIN operating mode. The actual focal plane detector, based on pin diodes, is not able of handling such a high count rate. This is the reason why in TRISTAN it is required to design a new detector and readout system capable of detecting very tiny

spectrum distortions and handling a total rate up to 10^8 cps, that will be integrated into KATRIN beamline.

1.3.2 TRISTAN detector

The need of a good energy resolution and of a high count-rate, make the SDD (Silicon Drift Detector) technology a good choice as TRISTAN experiment's detector. Its main benefit is the low value of its output capacitance, allowing SDDs to have measurements with a good energy resolution using short shaping times. Nevertheless, just a single pixel SDD detector was not sufficient for the huge electron rate of the tritium source. Thus, a large detector segmentation was made to reduce the count rate requirement to 100 kcps/pixel, and to minimize pile-up probability. For this reason, the final detector will be composed by a 3486-pixel matrix, divided into 21 modules of 166 monolithic SDDs each.

The TRISTAN detectors are custom-made monolithic SDD matrices designed and fabricated by the semiconductor laboratory of the Max-Plank-Society (MPG-HLL). The detectors are cut out from 6-inch 450-µm-thick wafers with a high-resistivity n-type substrate. Each pixel has a surface of about 7 mm^2 and, to avoid dead area between the different pixels, a honeycomb structure with hexagonal cells is employed. Figure 1.8 illustrates the structure of a single SDD cell. In particular each of them features an integrated n-JFET with an integrated feedback capacitor (C_{FB} = 25 fF) and an integrated reset diode. The latter is necessary to restore the initial condition of C_{FB}, since the devices are designed to work in a pulsed-reset regime.

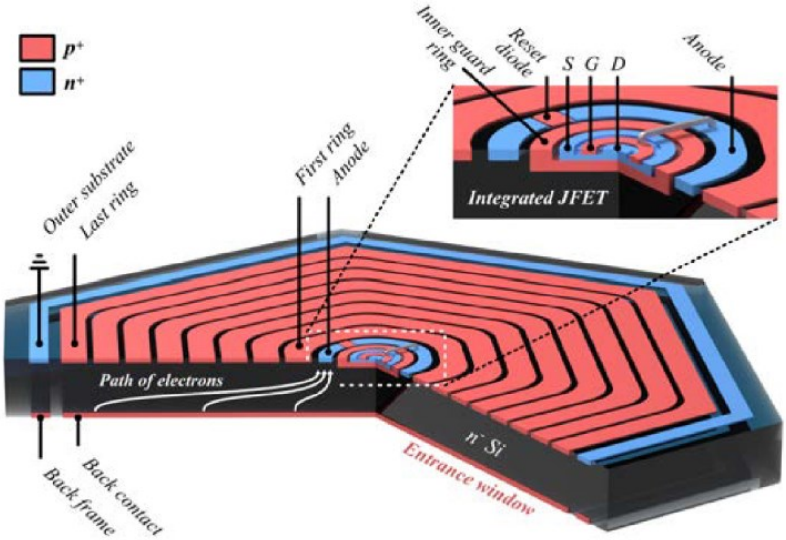


Figure 1.8: *Structure of a single TRISTAN SDD pixel. On the top right, a close view shows the JFET and the anode with the reset diode. Figure taken from Ref. [24].*

The integrated JFET technology instead has been preferred due to mechanical constrains. Indeed, for the pixels in the middle of the matrix, it would have been difficult to keep short wedge bonding contacts. With an integrated JFET instead, the first amplification stage is placed on the same wafer of the detector, reducing the noise issues.

For simplicity, Figure 1.8 shows only eight drift rings; in reality they are twenty and are biased using a resistance partition between the applied V_{R1} (voltage applied at the first ring) and V_{RX} (voltage applied at the last ring). In this way, the current flowing through the resistances of the voltage divider produces voltage drops that guarantee a smooth electric field variation inside the device.

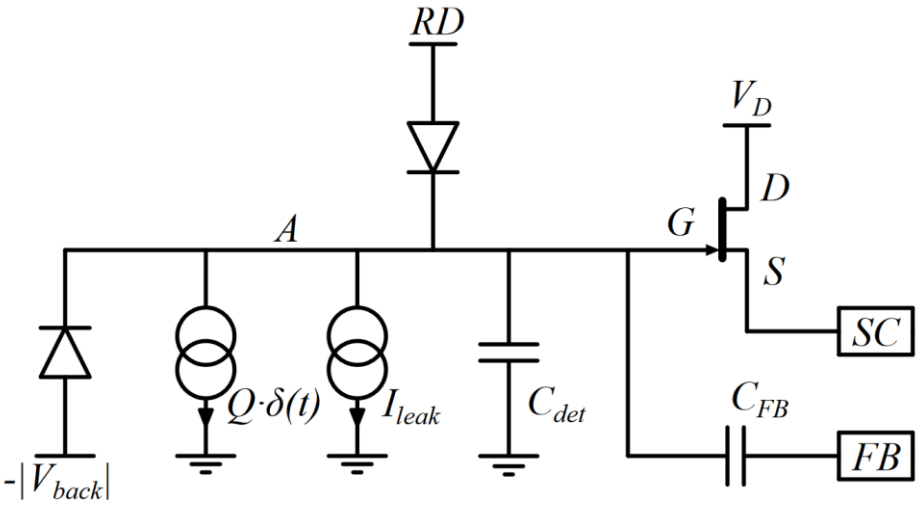


Figure 1.9: *Equivalent circuit of the TRISTAN SDD cell. The SDD is modelled with a delta-like signal current generator, a leakage current generator (I_{leak}), a detector capacitance C_{det}, including both the anode and the JFET gate contributions, and a diode (on the left) representing the inversely biased junction. On the right the integrated n-JFET and the integrated feedback capacitor are shown. The reset diode (on top), driven by the RD signal, is reversely bias for all the time, except during the reset phase.*

The equivalent circuit of the TRISTAN SDD cell is displayed in Figure 1.9. The *SC* and *FB* bond pads are shown on the right: the first corresponds to the source of the JFET, while the second is attached to the integrated feedback capacitor. An external ASIC, not shown in this scheme, closes the loop and completes the CSA circuit (see next section). Following a "step-by-step approach", different sizes of SDD matrices are produced: 1, 7, 12, 47, or 166 pixels. The main TRISTAN detector prototypes, whose matrices structures are shown in Figure 1.10, are the 12, 47 and 166 pixel versions.

The 12-pixel detector and its on-chip metal layout are used as elementary block of the bigger matrices. Indeed, they are built by multiple replicas of this 12-pixel elementary structure, which is called "reset group", since the corresponding 12 reset diodes are connected to a unique *RD* bond pad common to all the 12-pixel group. Each reset group have the possibility to be reset independently but, to reduce the amount of signal lines and the potential crosstalk, it has been chosen to drive the whole matrices with just a single synchronous reset signal. The bond pads are placed at the edges of the device, and they are connected to the pixels through metal line buses to provide all the signals and power supplies required.

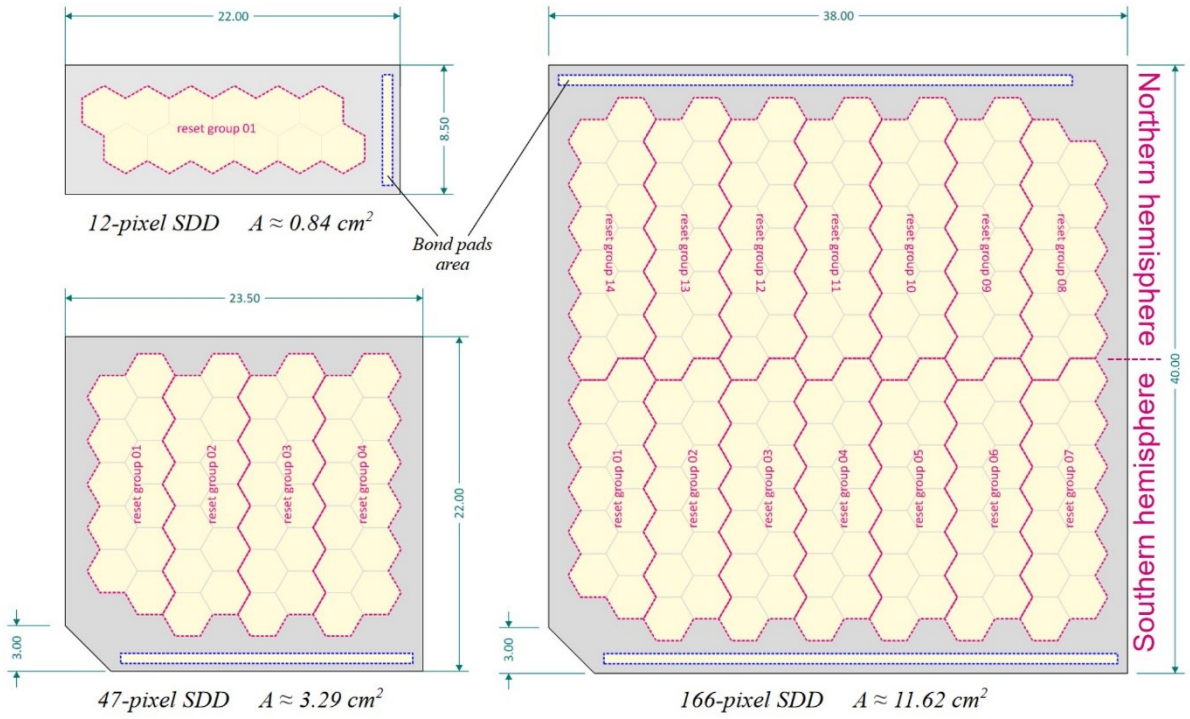


Figure 1.10: *Structures of the 12, 47 and 166 pixels detector. The pixels are organized in replicas of the base 12-pixel group and bond pads areas are used for signals and bias voltages. Only the 166-pixel detector has bond pads along two edges, and it is divided into two hemispheres (North and South).*

Important to notice is the fact that in the 47-pixel matrix there is a "missing pixel" (pixel #1), while in the 166-pixel there are two missing pixels (pixel #1 and #84). The bottom left missing pixel is due to the cut corner for the entrance window bond wires, while the top right one in the 166-pixel matrix is done in order to avoid the presence of a pixel with no neighbouring pixels in four out of six sides in the final structure. In this way the signal lost by charge spreading is minimized.

1.3.3 TRISTAN readout ASIC

To readout the TRISTAN detector pixels, a custom ASIC, called *ETTORE*, has been designed by an external company (XGLab S.r.l.) in collaboration with Politecnico di Milano [25]. ETTORE is a 12-channel ASIC, each of which features a first stage pre-amplifier, a second AC-coupled amplification stage and a comparator, used to detect the pre-amplifier saturation. It's realized in the 0.35 μm AMS CMOS technology and each 12-channel chip is matched with the 12-pixels of a reset group on the detector matrix.

The schematic of a single ETTORE channel connected to a detector pixel is reported in Figure 1.11. The first stage has a Charge Sensitive pre-Amplifier (CSA) architecture: the charge coming from the detector is integrated in the feedback capacitance C_{FB}. In this architecture, the n-JFET is used in source follower configuration with the source connected to the negative input terminal of the operational amplifier, through a decoupling capacitance (C_{AC} = 10 pF), used to cut the DC frequencies.

Thanks to the negative feedback, the voltage of the SDD anode is kept constant and the charge is integrated on C_{FB}. So, the output of the first stage (see Figure 1.12) is given by the superposition of a ramp like signal, due to the continuous integration of the leakage current (I_{leak}), and step like signals, due to the integration of the charge pulses generated by the detected events. The amplitude of each voltage steps is proportional to the energy of the corresponding event.

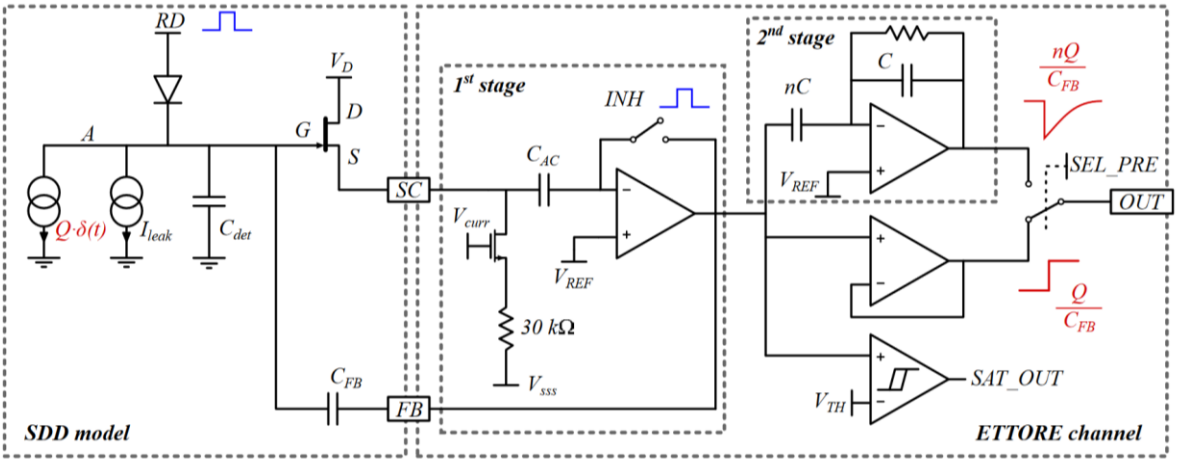


Figure 1.11: *Schematic block diagram of one ETTORE channel coupled to an SDD cell.*

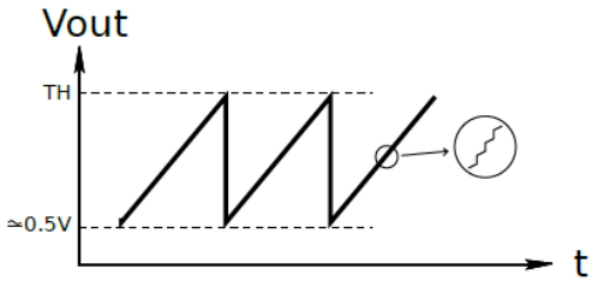


Figure 1.12: *First stage output signal.*

To prevent the saturation of the first stage output, due to the charge accumulated on C_{FB}, when the ramp signal gets close to the supply voltage, overcoming a threshold voltage (V_{TH}) at the input of the comparator, the comparator output (*SAT_OUT* signal) is driven high to inform the external reset logic. Indeed, the reset is managed by external electronics that coordinates the *RD* (SDD Reset Diode) and the *INH* (ASIC inhibit) signals. These two signals are low during the integration of the charge, while they are driven high during the reset phase. In particular: *RD* forward biases the reset diode, by fixing the anode potential (upper side of C_{FB}); *INH* puts the gain block of the first stage in buffer configuration, imposing the V_{REF} voltage at the bottom side of C_{FB}. Therefore, C_{FB} is brought to its starting condition, ready for the next integration phase.

Alternatively to the *SAT_OUT* signal, it is possible to provide an external periodic reset. The external electronics can decide to consider the *SAT_OUT* signal and apply a prompt or delayed reset or ignore it and apply the periodic reset.

The circuitry described until now and the output of the first stage are used in the experimental setup of this thesis. In particular, by setting the bit *SELECT_PRE* to 3.3V, the ramps, with the superimposed step-like signals, are sent at the input of a buffer stage that brings them directly to the bias board. However, ETTORE has also the possibility to add a second gain stage in cascade to the CSA, illustrated in Figure 1.13. In this second stage, whose output is selected by setting *SELECT_PRE* to 0V, the ramp is rejected using an AC-coupling capacitor, whereas the step signal of the first stage becomes a negative exponential signal. This additional gain stage can be used to further amplify the signals, reducing the Integral Non Linearity (*INL*) effect of the ADC used in the DAQ. In fact, if a portion of the signal is covered by more bits of the ADC, the INL effect has a minor impact [27].

The second stage transfer function is basically a high-pass filter, so with a step-like signal we find at the output a negative amplified exponential signal, with its characteristic τ , as shown in Figure 1.14.

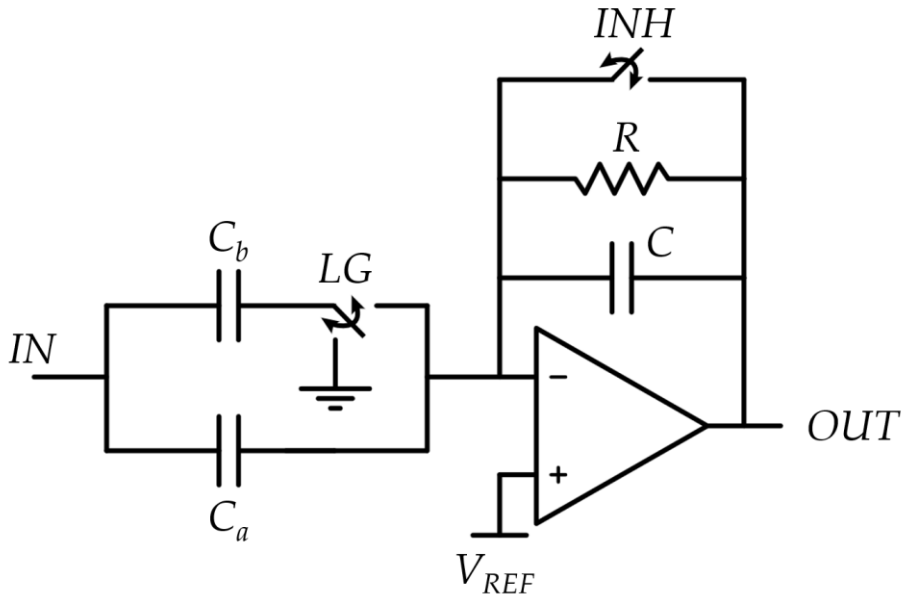


Figure 1.13: *Schematics of ETTORE second stage. The LG bit is used to change the gain "n" of the stage to optimise the dynamics, adding or not an additional capacitance C_b in parallel to C_a.*

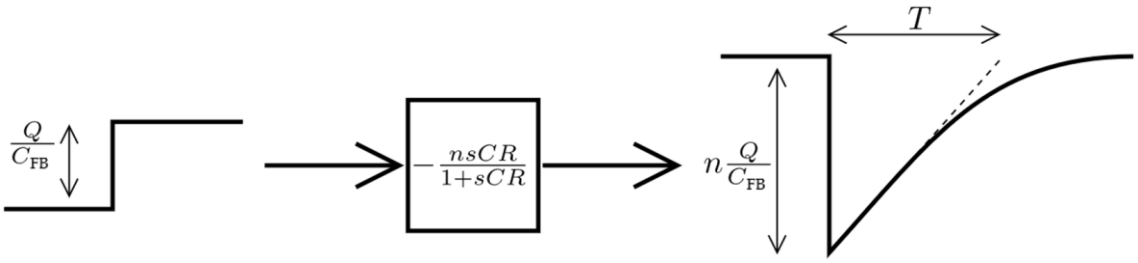


Figure 1.14: *ETTORE second stage filtering effect and transfer function with $nC = C_a + C_b$. In particular the gain factor n can be equal to 5 or 10 depending on the LG value.*

To give a complete overview of the ETTORE chip and to understand all the signal functionalities, a list of each bond pad is reported in Figure 1.15 and in the following list:

OUTxx: outputs of the ASIC channels. These lines feature a 50-Ω impedance and are connected to the back end electronics for signal processing.

INxx: inputs of the ASIC channels. They are linked to the source of the integrated JFETs (*SC* bond pads).

CFxx: outputs of the first stage of each channel. They must be connected to the integrated feedback capacitor C_{FB} (*FB* bond pads).

GNDA1: ground reference for the first stages.

VDDA1: 3.3 V power supply for the first stages.

GNDA2: ground reference for the second stages and auxiliary logic.

VDDA2: 3.3 V power supply for the second stages and auxiliary logic.

V_{SSS}, V_{CURR}: they are used to control the current generator, embedded in each channel, that sets the JFET bias current. The V_{SSS} line carries the JFET source currents, and its voltage sets the desired bias current value (see Figure 2.7 in the next chapter). V_{CURR} is internally set at 2.7 V by an integrated voltage divider, but can be changed externally to tune the gate voltage of the current generator FET.

V_{BW}: reference voltage used to tune a variable nulling resistor used for the compensation of the first stage OTA. It is internally set to 1 V, but it can be modified externally.

V_{REF}: reference voltage for the first and second stage operational amplifiers. It is internally set to 2.7 V but can be modified externally.

V_{TH}: threshold voltage at the negative input of the comparators, that detects the saturation of the first stage outputs. It is internally set to 2.7 V, but, similarly to the previous analog reference voltages, can be changed externally.

SAT_OUT, SAT_IN: saturation output and input. *SAT_OUT* is the logic OR between the twelve comparators inside the same ASIC and the *SAT_IN* signal. In normal conditions, the *SAT_OUT* = 0 V. If it's high, it means that at least one channel has overcome the threshold voltage. *SAT_IN* is a digital input signal used to propagate the saturation information when more than one ASIC is used. ASICs can be connected in a daisy chain, with the first ASIC having *SAT_IN* tied to ground, and the last ASIC providing the global *SAT_OUT* signal, which goes high as soon as any channel in the series of ASICs overcomes the threshold.

INH: inhibit digital input (0 ÷ 3.3 V). When is driven high, the amplifier becomes a buffer and, in conjunction to the activation of the reset diode, the detector is reset.

LG: "low gain". Static bit setting the gain n of the second stage: if LG = 0 V then n = 10; if LG = 3.3 V then n = 5.

SEL_PRE: "select preamplifier". Static bit controlling the output multiplexers that select either the buffered first stage output or the second stage output to be sent to the OUTxx lines. *SEL_PRE* = 0 V selects the second stage output; *SEL_PRE* = 3.3 V selects the first stage output.

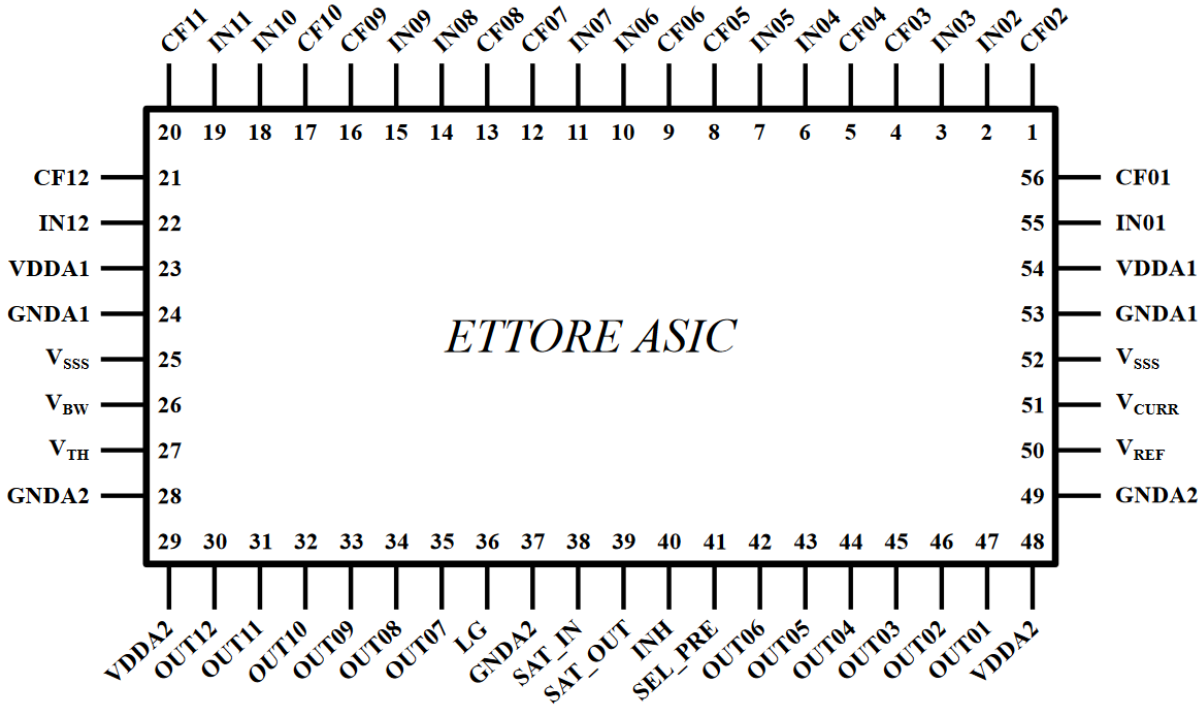


Figure 1.15: *Contacts names and pad numbering of the ETTORE ASIC.*

Finally, Figure 1.16 illustrates the acquisition chain developed for the readout of the TRISTAN detectors. The SDD is coupled to ETTORE preamplifier and read by a data acquisition system. In particular, it's composed by:

- a **bias board**, used to provide the supplies both to the ASICs and to the detector. The bias systems designed by XGLab includes a buffer board to provide an additional gain (G = +2) and selectable DC offset; instead, in the bias system developed in this thesis, it has been avoided in order to have a more compact system, since it is not a limitation in the laboratory setup.

- a **Digital Acquisition (DAQ) system** (called "**Athena system**") composed by four 48-channel Kerberos analog pulse processors and a digital data aggregator (Athena itself), presented in Section 3.2.1.

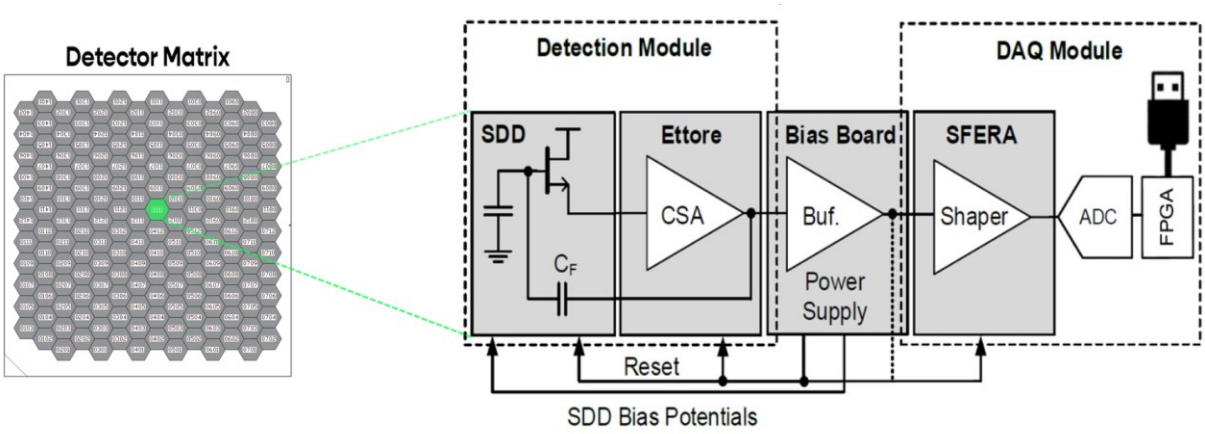


Figure 1.16: *Schematic view of the electronic acquisition chain.*

1.3.4 Experiment roadmap

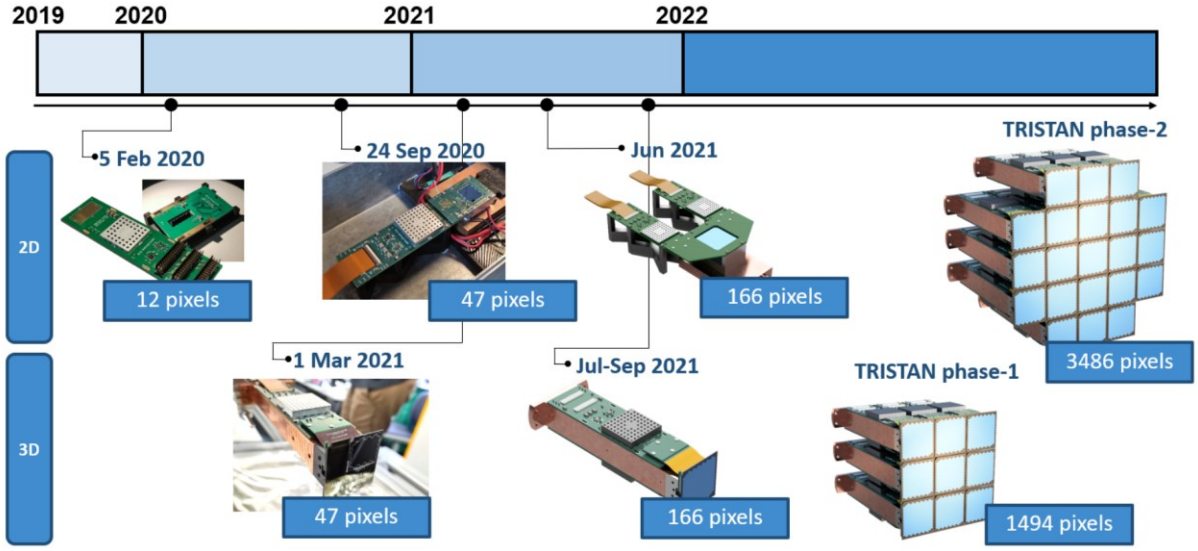


Figure 1.17: *TRISTAN project roadmap from 2019 and future plans.*

Figure 1.17 illustrates the evolution in the front end electronics setup of TRISTAN from 2019 and the future phases of the project. The detector electronics was divided into 2D and 3D setups and each detector version was first tested in the planar (2D) version to

control the electrical interconnections and functionality of the matrix, before moving to the 3D version. As mentioned before, the main TRISTAN detector prototypes are the 12, 47 and 166 pixels versions. Thus, in parallel to them, for the readout, three different versions of *detector board* and *ASIC board* were implemented for the 12, 47 and 166 pixel planar setups. In particular: the 12-channel ASIC board (for more information refer to Ref. [28]) hosts only a single ETTORE chip and, on one side, it's linked to the detector board hosting the 12-pixel detector, on the other side, it's connected to the 12-pixel XGLab bias system; the 47-channel ASIC board (refer to Ref. [29]) hosts four ETTORE chips and it's linked to the detector board hosting the 47-pixel detector on one side, while on the other side, it's connected to the 47-pixel XGLab bias system; for the 166-pixel setup, two 83-channel ASIC boards (refer to Ref. [30]), placed one next to the other, host 14 ETTORE chips (seven chips in each ASIC board) and are linked to the same detector board hosting the 166-pixel detector on one side, while on the other side, it's connected to the 166 bias system developed during this thesis.

A summary of all the different planar setups is displayed in Figure 1.18.

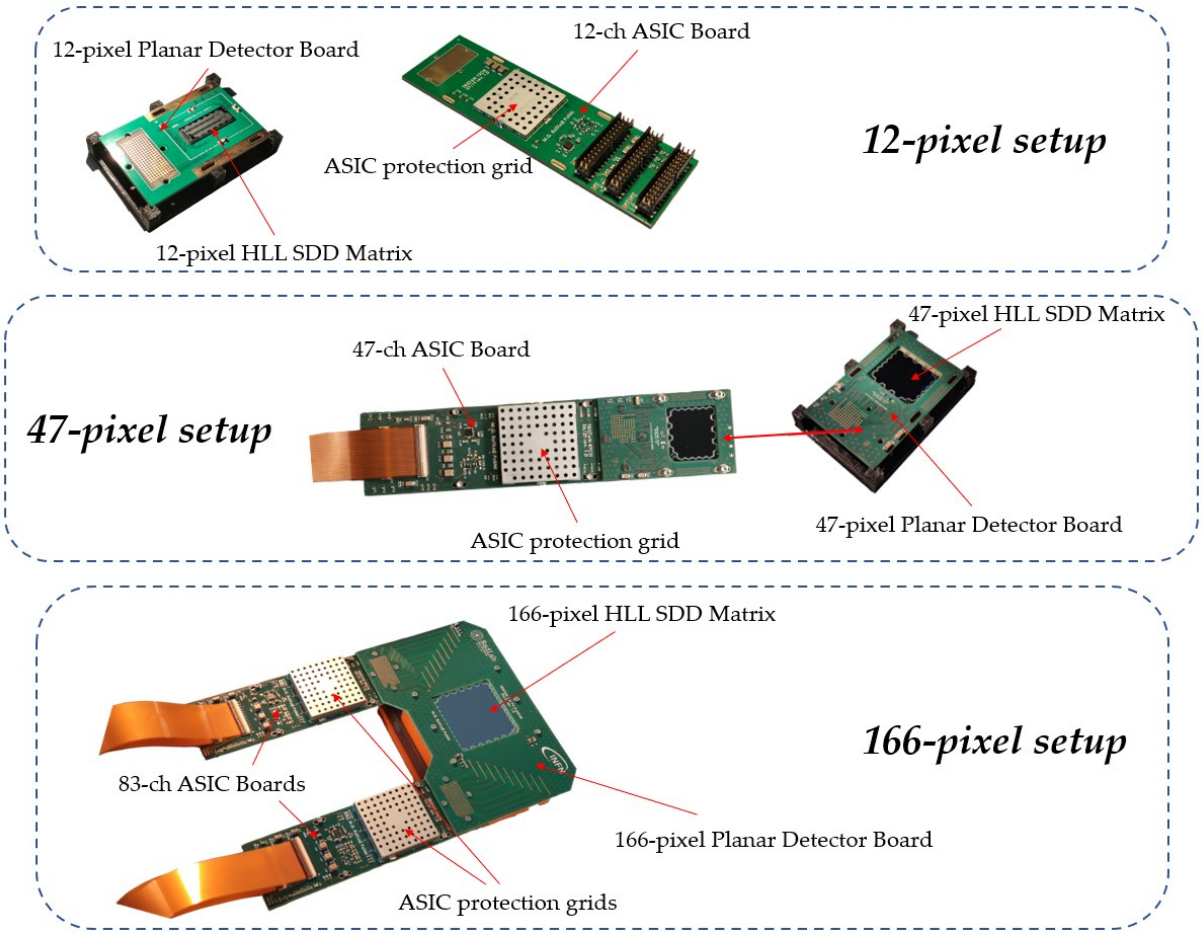


Figure 1.18: *12, 47 and 166 pixels planar setups.*

The 3D setups, more faithful to the final TRISTAN experiment layout, are more mechanically challenging. Indeed, since the detector matrix is orthogonal to the holding structure where the ASIC boards are fixed, the design and the development of complex rigid-flex-rigid detector boards was required (see Figure 1.19).

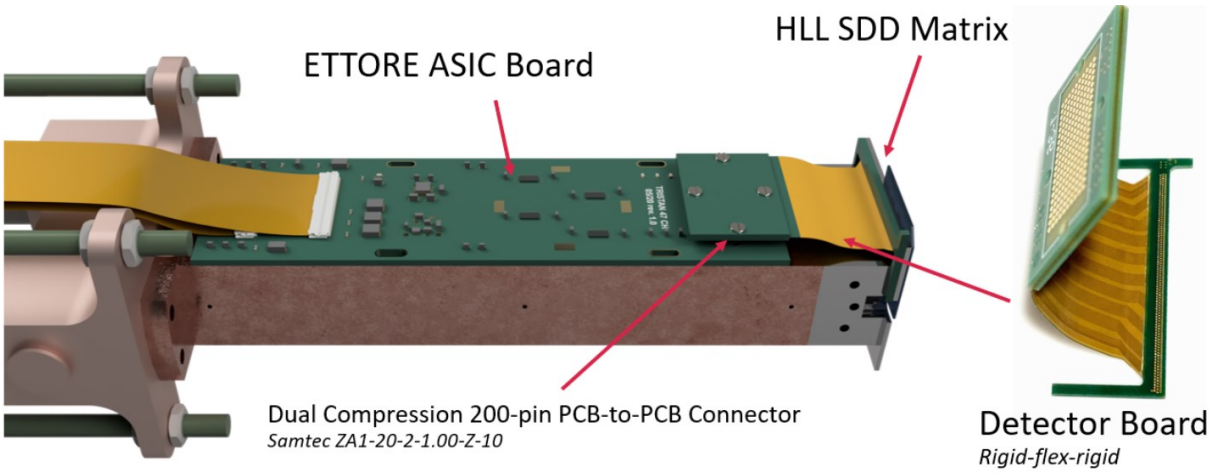


Figure 1.19: *3D design setup showing the rigid-flex-rigid detector board used to connect the ASIC boards to the detector matrix placed perpendicularly.*

The first rigid part of the PCB is glued to the detector and holds the pads for the wedge bonding to the detector. This is followed by a Kapton flex PCB that is used to mechanically shift the signals from the vertical to the horizontal plane, and it finishes with an additional rigid part, which is then connected to the boards that host the ETTORE ASICs by the use of a "SAMTEC ZA1-20-2-1.00-Z-10" 1-mm-pitch low-profile 200-pin dual-compression interposer.

The TRISTAN project roadmap is divided into three main phases:

- **Phase 0:** the first main milestone of the project will be reached with the insertion of a full 166 pixel TRISTAN module inside the KATRIN *Monitor Spectrometer* to test the first TRISTAN detector prototype, as shown in Figure 1.20.

- **Phase 1:** integration of nine 166-pixel modules inside the KATRIN *Main Spectrometer*. The KATRIN detector (FPD) will be removed, and about 1500 TRISTAN SDD pixels will be inserted into the experiment main beamline. From the scientific point of view, the phase 1 will allow measurements in the standard neutrino mass mode giving significantly better signal to background ratio, higher position resolution and higher allowed data rates with respect to the previous KATRIN measurements.

- **Phase 2:** the last main step requires the integration of all the 21 detector modules, for a total of 3486 pixels. An important redesign of the detector section is required to allocate the complete TRISTAN detector and all its electronics.

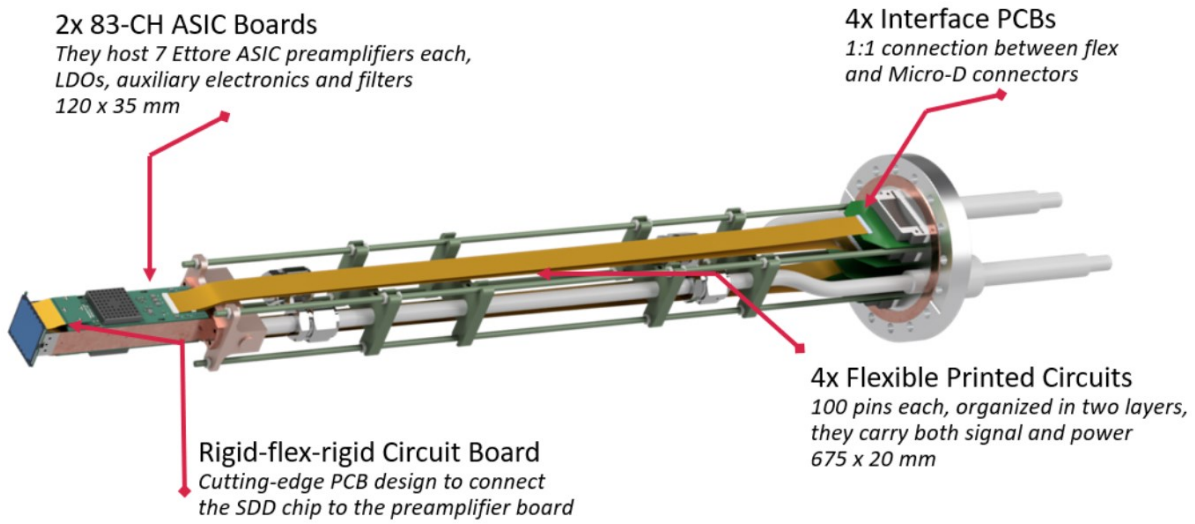
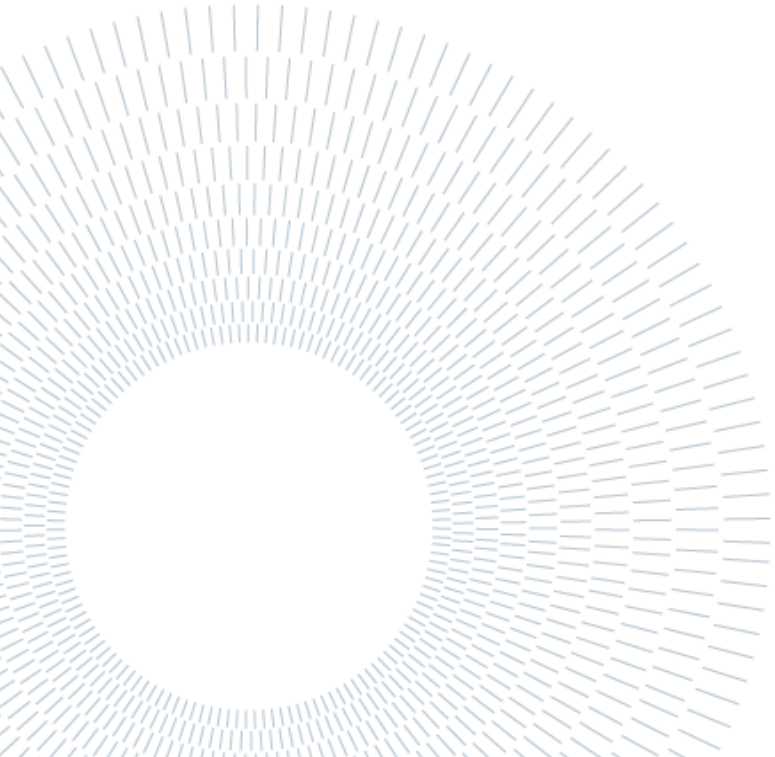


Figure 1.20: *CAD model of the 166-pixel 3D module inside the MoS. A single complete TRISTAN module (166-pixel SDD, 14 ETTORE ASICs hosted by two ASIC boards, cooling and supporting mechanics) will be inserted at the end of phase 0.*



2. 166-pixel Bias System

This Chapter presents the design of the 166-pixel bias system called "Lifeboard", which is a core part of the work of this thesis. Initially a general overview of the system is given, followed by the technical specifications and the layout choices; finally, the improvements made to the Lifeboard are discussed in detail.

2.1 Overview

During the development of the TRISTAN project, to move from the 47-pixel to the 166-pixel planar setup, it was required a new bias system, able to provide the supply to the new 166-pixel detector and the two 83-channels ASIC boards, to manage the ASIC control signals and the SDD reset and to interconnect the 166 ASIC boards outputs with the DAQ inputs.

A commercial bias system, also including a Graphical User Interface (GUI) to monitor the bias voltages, a buffer board for the 166 outputs and a digitalized control of various sections was under development by XGLab company and will be employed for the Monitor Spectrometer installation of the 166-pixel prototype. Anyway, more compact system was required to perform preliminary tests with the new 166-pixel detector and to characterize the full setup.

In particular our system has been simplified by removing the buffers and the GUI. This is not an issue since in our laboratory setup the interconnections between ASIC boards and bias board and from this last to the Athena DAQ are shorter (less than 1m) with respect to the final setup in the Monitor Spectrometer, so the ETTORE chip can drive the cables and the high impedance inputs of the SFERA ASICs (see Section 3.2.1) without the necessity of using a buffer stage.

The Lifeboard is composed by three boards: a main bias board and two identical 83-channel connection boards placed over it, as represented in Figure 2.1.

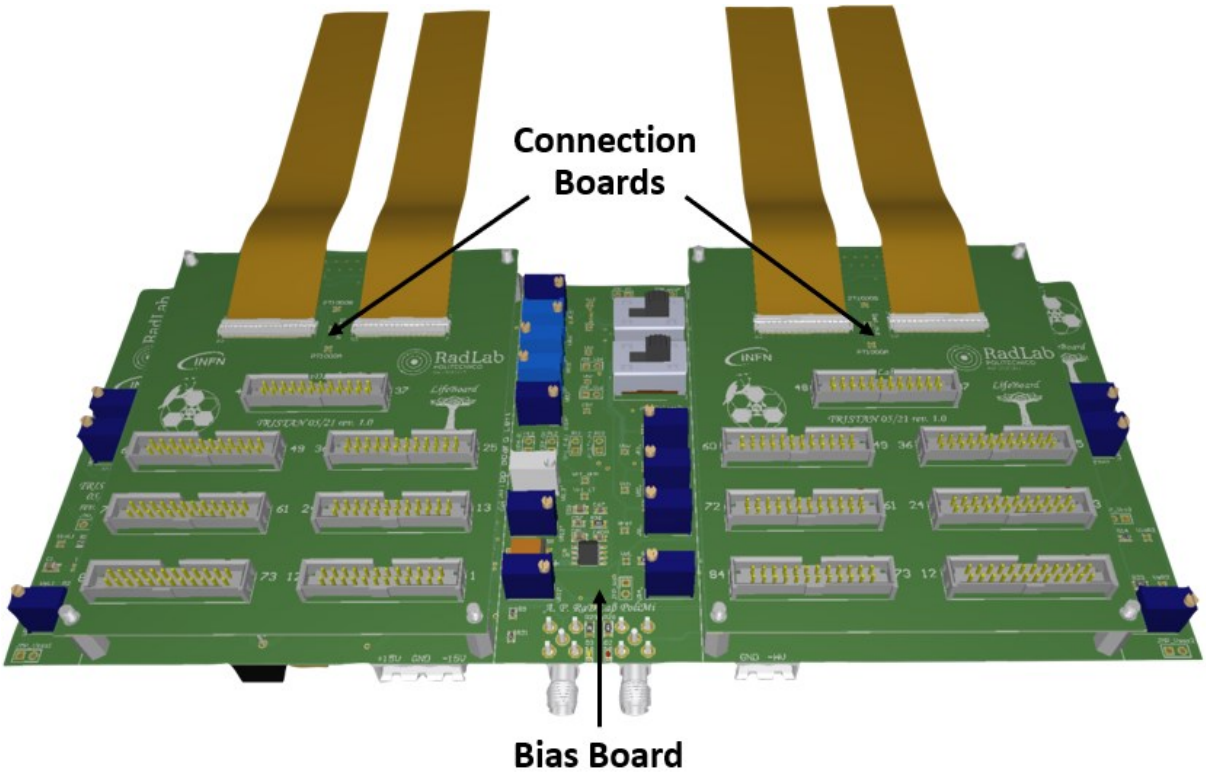


Figure 2.1: *3D CAD model of the Lifeboard.*

The bias board generates the bias voltages (adjustable with trimmers) and the control signals both for the SDD matrix and for ETTORE ASICs. Instead, the purpose of the connection boards is to send the ETTORE outputs to the DAQ.

The voltage and current requirements of the 166-pixel setup that this bias system have to satisfy are shown in Table 2.1. In particular this table specifies if the voltages have fixed values (*fixed*) or can be adjusted with trimmers (*adj.*) and which voltages are sent independently (*hemisphere*) or in parallel (*global*) to the two ASIC boards.

Feature	Voltage	Max. current	Type
ASIC board supply (V_{IO})	4.1 V	700 mA	Fixed, hemisphere
ASIC ref. (V_{REF}, V_{TH}, V_{BW})	0÷3.3 V	1 mA	Adj. global
JFET drain (V_D)	1.22÷13.42 V	50 mA	Adj. global
JFET bias generator (V_{SSS})	-1.22÷-13.42 V	-50 mA	Adj. hemisphere
SDD reset diode high (V_{RES_H})	0÷10 V	200 µA	Adj. hemisphere
SDD reset diode low (V_{RES_L})	0÷-15 V	-200 µA	Adj. hemisphere
SDD inner guard ring (V_{IGR})	0÷-26.3 V	-10 µA	Adj. global
SDD first ring (V_{R1})	-1.58÷-13.78 V	10 mA	Adj. global
SDD last ring (V_{RX})	-95÷-145 V	-10 mA	Adj. global
SDD back frame (V_{BF})	0÷-150 V	-10 µA	Adj. global
SDD back contact (V_{BC})	0÷-150 V	-10 µA	Adj. global

Table 2.1: *List of bias voltages and corresponding currents in the Lifeboard bias system.*

2.2 Bias Board

2.2.1 Front side

The front side of the bias board is divided in 5 main sections (Figure 2.2):

- The **positive and negative low voltages section**, that provides the ASIC board supply (V_{IO}), split in V_{IO1} (for the Northern hemisphere) and V_{IO2} (for the Southern hemisphere); the JFET drain voltage (V_D); the JFET bias generator voltage (V_{SSS}), split in V_{SSS1} and V_{SSS2}; the ASIC reference voltage (V_{ASIC}), used to generate the reference signals for the ETTORE ASICs. This section also includes two LEDs, red and yellow, switching on respectively when the positive power supply (+15 V) or the negative power supply (-15 V) are switched on.

- The **reference voltages section**, that provides the V_{REF}, the V_{TH}, the V_{BW} and the *SEL_PRE* signal (called *select_pre* on the bias system).

- The **reset section**, driven by an external reset (*RES_EXT*) taken from an external pulse generator by an SMA connector. The *RES_EXT* is used to drive the circuit that provides the reset signal to the SDDs and the one that provides the inhibit

signal to the ASIC. Those two signals are sent to the ASIC board through the connection boards.

- The **detector bias section**, providing both the high voltages (V_{BC}, V_{BF} and V_{RX}) and the low voltages (V_{IGR} and V_{R1}) for the 166-pixel SDD detector. The inner guard ring (*IGR*) is turned on/off by switching on/off the lower switch (*SW_LV*), while V_{BC}, V_{BF} and V_{RX} are turned on/off by switching on/off the upper one (*SW_HV*). V_{R1} is instead set independently. This section features a diode protection mechanism to prevent damages when switching off the *SW_LV* without having completely discharged the V_{BC}, V_{BF} and V_{RX} voltages (this protection mechanism will be explained in Section 2.4.4).

- The **interconnection section**, which features two 40-pin board-to-board "SAMTEC-TFM-120-32-X-D-A" connectors to provide the signals and the bias voltages from the bias board to the connection boards.

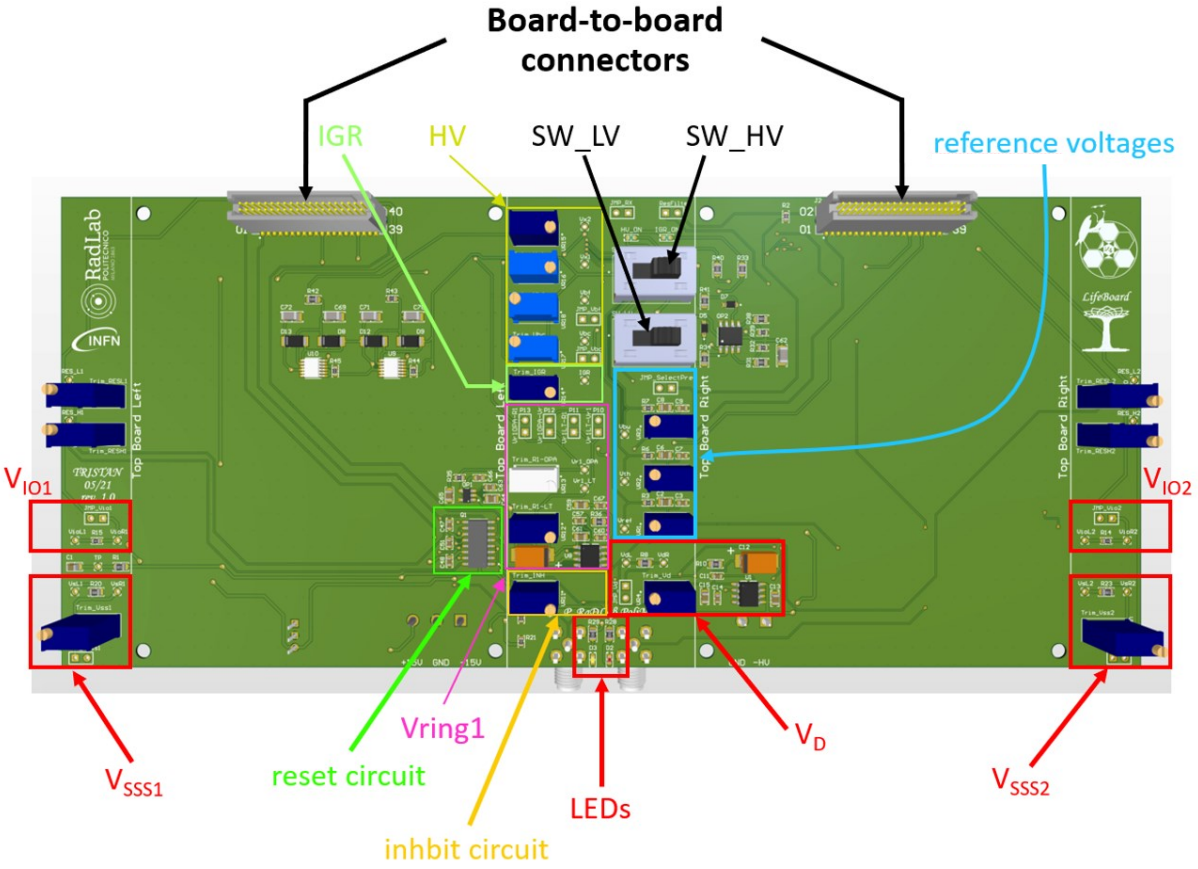


Figure 2.2: *Graphical representation of the different sections.*

2.2.2 Back side

In the back side of the bias board the different sections are highlighted using silkscreen printing on the bottom overlay layer (Figure 2.3). This gives a snap visual overview of the entire PCB useful to identify immediately the components during the soldering procedure and during testing.

In the bottom side (highlighted in red in Figure 2.3) there are two SMA connectors for the *RES_EXT* signal, the HV (-150 V) connector and the ±15 V connector. The HV and the ±15V connectors are linked to two external voltage generators providing respectively the high voltages (HV = -150 V) and the low voltages (LV = ±15 V) to the system.

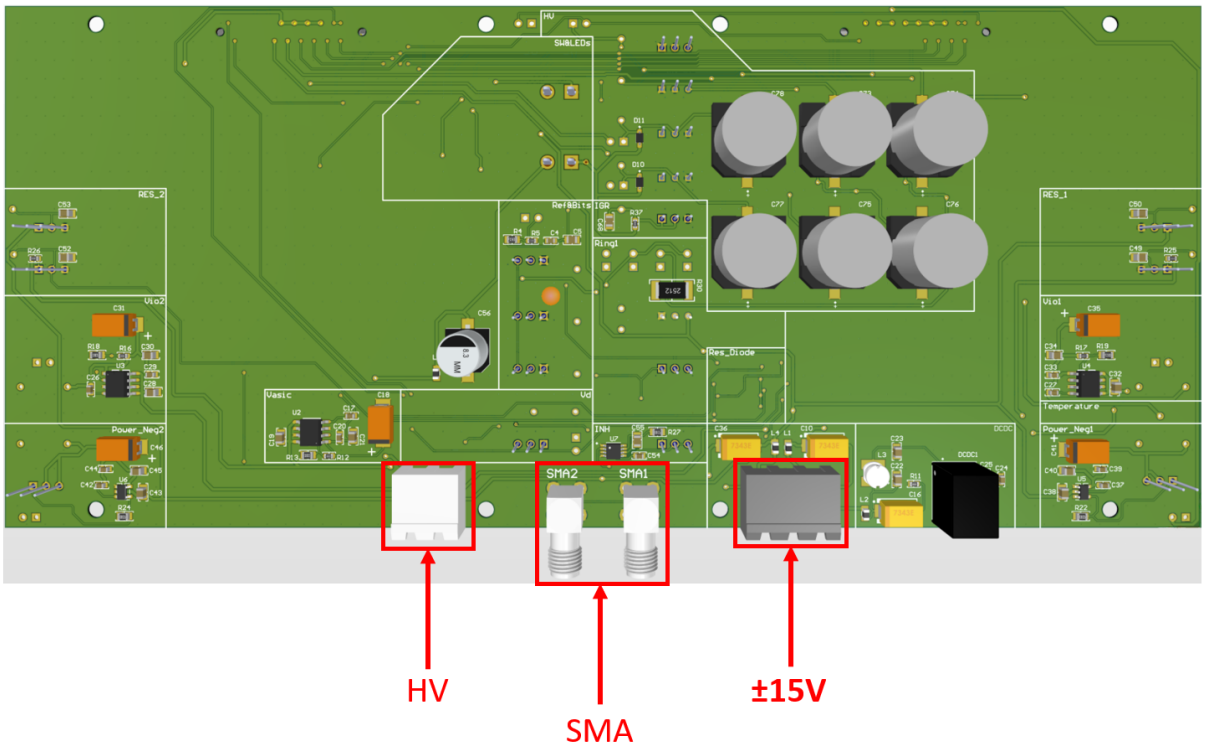


Figure 2.3: *Back side view of the bias board.*

2.3 Connection Board

2.3.1 Front side

The front side of the connection board (Figure 2.4) is composed by:

- **7** "STMM-112-02-L-D" 24-pin **connectors to Kerberos** analog pulse processors (described in Section 3.2.1). In each connector: the 12-pins upward are outputs, the 12-pins on the bottom are GND. The first pin of the first connector is not connected to a pixel of the SDD matrix (it corresponds to the detector missing pixel), so this channel is left floating in the detector board.

- **2 test points** to measure the voltage across the **PT1000 sensor** present in the ASIC board (to monitor its temperature during the system operation).

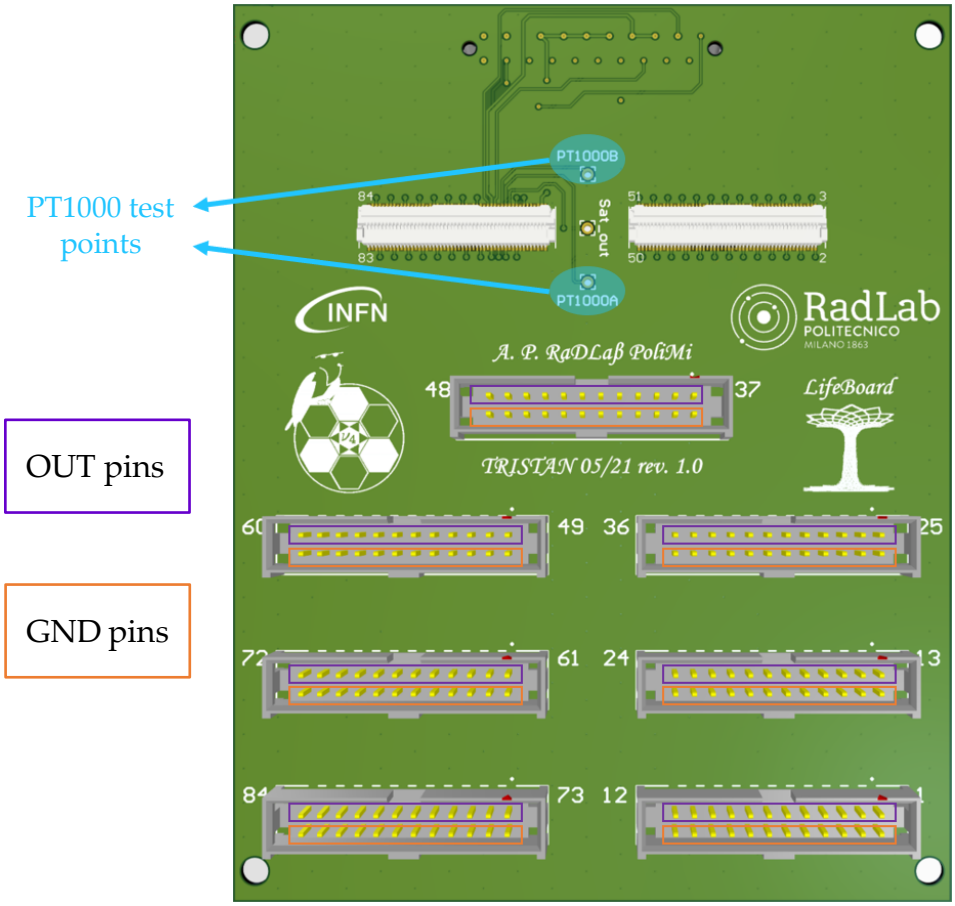


Figure 2.4: *Front side view of the connection board.*

- **2** "Hirose FH29B-100S-0.2SHW" **100-pin flexible printed circuits (FPC) connectors** to connect the connection board to the ASIC board through two dual-layer flexible printed circuits (FPC) cables. These connectors have both the 83 output pins and the bias voltages pins, arranged as in the schematic view of Figure 2.5.

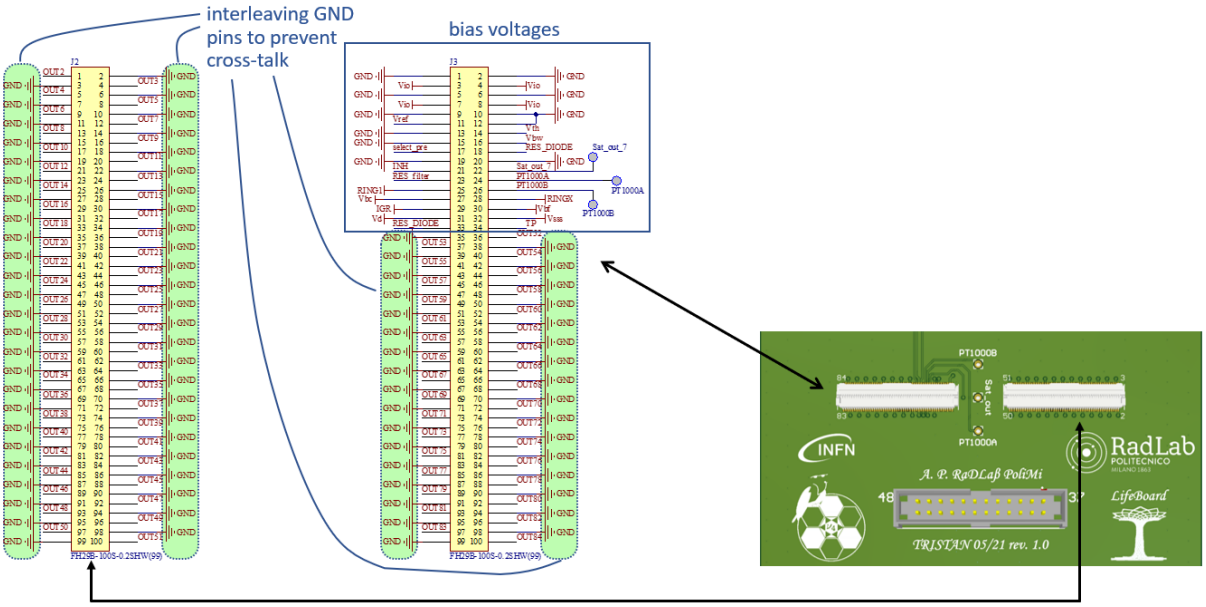


Figure 2.5: *Schematic view of the 100-pin connectors shown on the right.*

2.3.2 Back side

In the back side of the connection board is present a 40-pin **board-to-board** "SAMTEC-SFM-120-02-X-D-A" **connector** (Figure 2.6) that electrically connects the bias board to the connection board bringing the power supplies and complementary signals in the appropriate lines.

On the four corners of the connection board are present 4 alignment holes (3 mm diameter) to mount it on the bias board, using 25 mm standoffs.

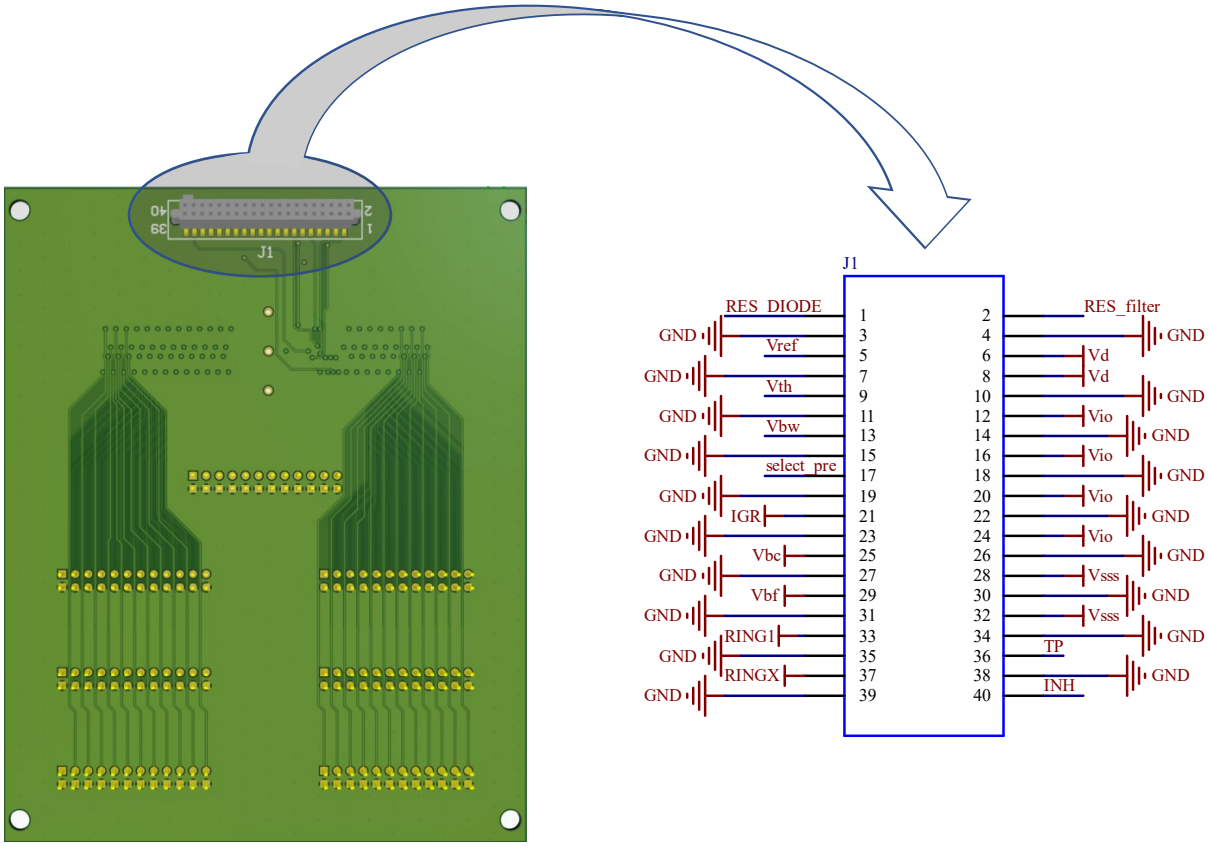


Figure 2.6: *Back side view of the connection board and schematic view of the connector.*

2.4 Technical specifications

This section presents the key technical specifications of the bias system, explaining how the different signals are generated, the design choices and the protection mechanisms to prevent damages during the setup operation.

2.4.1 Positive and negative LV power

Both the positive low voltage (+15 V) and the negative low voltage (-15 V) are taken from an external voltage generator and filtered by an 2nd order LC low pass filter to attenuate the disturbances, providing respectively the filtered V_{POS} and V_{NEG} voltages.

- V_{NEG} is used as input of two low-dropout (LDO) negative voltage regulators (LT1964) placed in parallel to generate two V_{SSS} (called V_{SSS1} and V_{SSS2}), independently adjustable in the -1.22 ÷ -13.42 V range. V_{SSS1} is sent to the 7 ASICs of the Northern hemisphere, through the left connection board, while V_{SSS2} is sent to the 7 ASICs of the Southern hemisphere, through the right connection board. Exploiting this parallel configuration, each regulator absorbs only half of the JFET bias current (I_{SSS} = 50 mA) resulting in a maximum power dissipation given by Eq. (2.1):

$$P_{max} = I_{max} \times (V_{in} - V_{out}) = 25\ mA \times (15\ V - 1.22\ V) = 0.3445\ W \qquad (2.1)$$

The LT1964 datasheet [31] reports a worst case thermal resistance junction-to-case of $R_{\theta JC}$ = 150 °C/W (for SOT-23 package) and a maximum rated junction temperature of T_{Jmax} = 125 °C. Therefore, the maximum allowed ambient temperature of operation is:

$$T_A = T_{jmax} - P_{max} \times R_{\theta JC} = 125\ °C - 0.3445\ W \times 150\ °C/W = 73.325\ °C \qquad (2.2)$$

This value is more than enough to operate safely the setup.
In series with the output pin of the LT1964 regulator there is a 1Ω resistance and two test points at its terminals used to measure the actual current I_{SSS}. This current is proportional to the V_{SSS}, as reported in the Cadence simulation of Figure 2.7 referred to a single pixel of the detector (the total I_{SSS} required from the bias system is obtained just by summing the current of each of the 166 pixels).

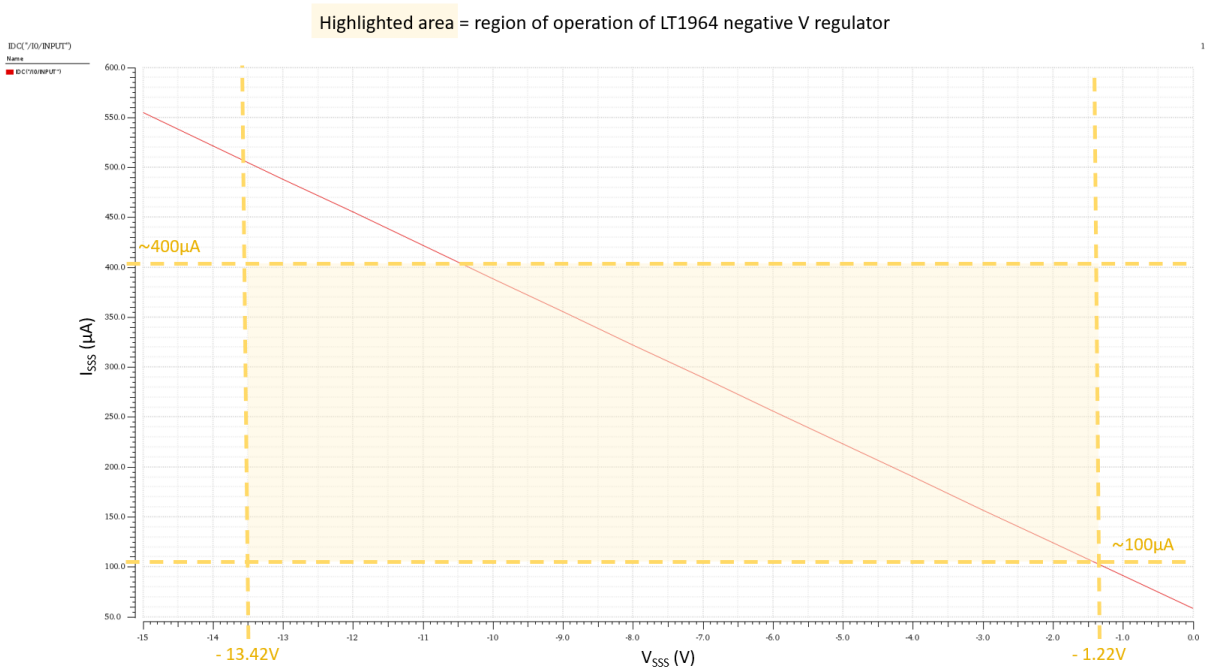


Figure 2.7: *Cadence simulation of Isss vs Vsss in a single SDD pixel.*

- V_{POS} is used as input of two low-dropout positive voltage regulators (LT1763) . One of them is used to generate the JFET drain voltage (V_D) and features a manually adjustable trimmer to set the V_D in the 1.22 ÷ 13.42 V range; the second regulator provides the ASIC reference voltage (V_{ASIC}), fixed at 3.3V by properly setting the resistances connected to the regulator.
  The current required by the V_{ASIC} is negligible, so there's no need of performing a thermal analysis. Instead, the maximum drain current (I_D) is 50 mA, which is not negligible, resulting in a maximum power dissipation given by:

$$P_{max} = I_{max} \times (V_{in} - V_{out}) = 50\ mA \times (15\ V - 1.22\ V) = 0.689\ W \qquad (2.3)$$

  The LT1763 datasheet [32] reports a worst case thermal resistance junction-to-case of $R_{\theta JC}$ = 86 °C/W (for S8 package) and a maximum rated junction temperature of T_{Jmax} = 125 °C. Therefore, the maximum allowed ambient temperature of operation is:

$$T_A = T_{jmax} - P_{max} \times R_{\theta JC} = 125\ °C - 0.689\ W \times 86\ °C/W = 65.746\ °C \qquad (2.4)$$

  This value is more than enough to operate safely the setup.
  In series with the output pin of the LT1964 regulator there is a 1 Ω resistance and two test points at its terminals used to measure the actual current I_D.

- The positive low voltage (+15 V) is also sent to the input of a DC-DC converter, "R-78C5.0-1.0" [33], after being filtered by a different 2nd order LC low pass filter (Figure 2.8). Having two separated filters is important to attenuate the harmonic disturbances injected by the DC-DC converter. In fact, if the input of the DC-DC converter would be connected to the same input of the LDO regulators (V_{POS}), the disturbances would be directly propagated to the regulators. In addition to it, an EMC filter is placed at the input side of the converter (as suggested in the datasheet by the manufacturer).
  The DC-DC converter output (V_{DCDC} = 5 V) feeds the input of two low-dropout positive voltage regulators (LT1763) placed in parallel to generate two V_{IO} (called V_{IO1} and V_{IO2}), with fixed value of 4.1 V. V_{IO1} is sent to the 7 ASICs of the Northern hemisphere, through the left connection board, while V_{IO2} is sent to the 7 ASICs of the Southern hemisphere, through the right connection board. Exploiting this parallel configuration, each regulator absorbs only half of the ASIC bias current, which was initially estimated to be I_{IO} = 700 mA (see Table 2.1), resulting in a maximum power dissipation of each regulator given by:

$$P_{max} = I_{max} \times (V_{in} - V_{out}) = 350\ mA \times (5\ V - 4.1\ V) = 0.315\ W \qquad (2.5)$$

  The LT1763 has a worst case thermal resistance junction-to-case of $R_{\theta JC}$ = 86 °C/W (for S8 package) and a maximum rated junction temperature of T_{Jmax} = 125 °C, so the maximum allowed ambient temperature of operation is:

$$T_A = T_{jmax} - P_{max} \times R_{\theta JC} = 125\ °C - 0.315\ W \times 86\ °C/W = 97.91\ °C \qquad (2.6)$$

  This value is very high thanks to the employment of the DC-DC converter, that converts the +15 V input voltage in a +5 V voltage used as input of the LDO regulators, allowing to reduce their dropout voltage and so the power dissipation.
  In series to the output pin of the LT1763 regulator there is a 100 mΩ resistance and two test points at its terminals used to measure the actual current I_{IO}.

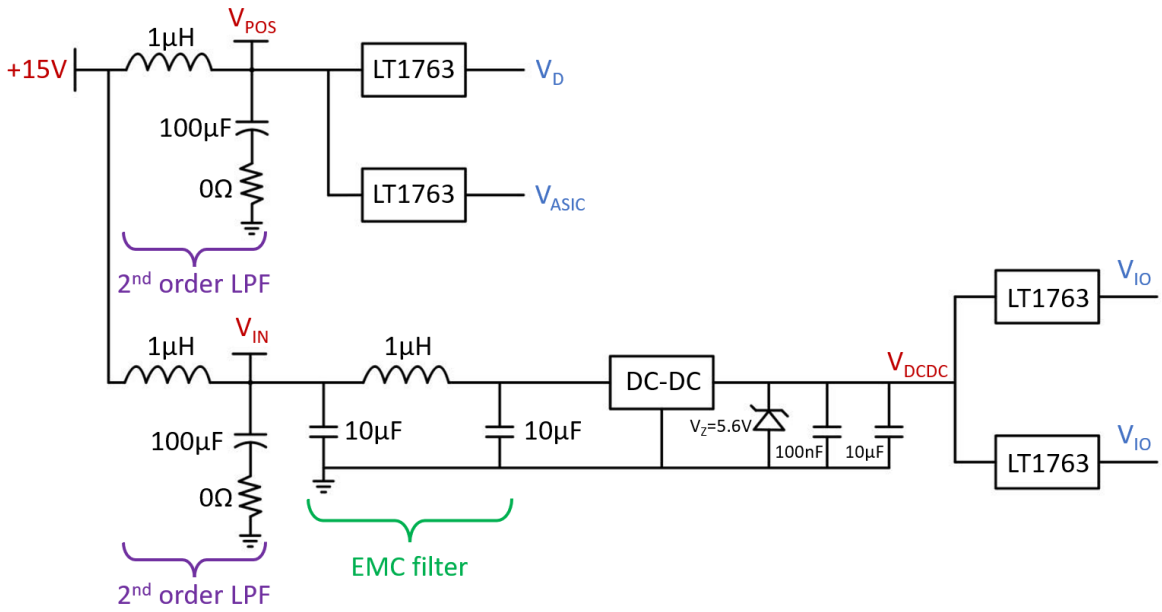


Figure 2.8: *Schematic view of the positive power circuitry.*

To clearly indicate the V_{NEG} and V_{POS} status, two LED are placed in the circuit as reported in Figure 2.9.

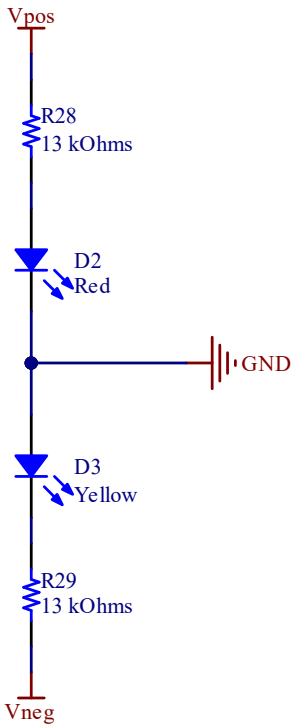


Figure 2.9: *Schematic view of the V_{NEG} and V_{POS} LED status indicators.*

As soon as the ±15 V external generator provides the voltage to the system: a current starts to flow from the V_{POS} node, down to the red LED, switching it on and indicating that the positive supply is correctly reaching the system; an equal current (same resistor, same voltage drop and same LEDs are used) flows from the ground pin to the V_{NEG} node, passing through the yellow LED, switching it on and indicating that the negative supply voltage is correctly reaching the system.

2.4.2 Reference voltages and static bit

The V_{ASIC} is internally used to generate the *select_pre* static bit and the reference voltages for the ETTORE ASICs.

The reference voltages can be tuned by a trimmer in the 0÷3.3 V range, while the *select_pre* signal can be either 0 V or 3.3 V by means of a 2-pin header that can be open (*select_pre* = 0 V) or closed (*select_pre* = 3.3 V) using a jumper, as shown in Figure 2.10. Specifically, the *select_pre* signal is the output of a pull-down network, so it's normally low and driven high when the header is closed.

For each reference voltage it has been placed a test point to probe the voltages during the testing phase of the bias system.

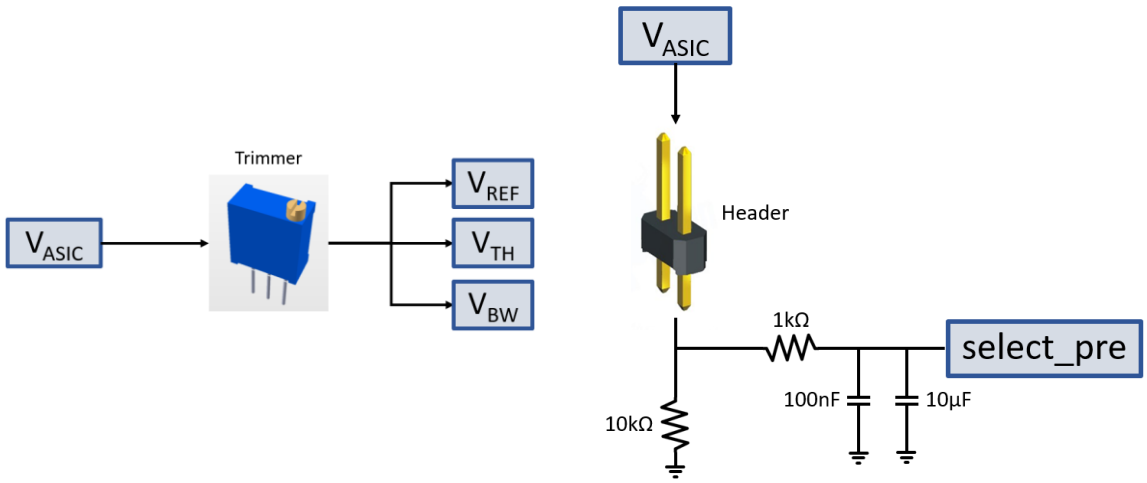


Figure 2.10: *Simplified block diagram of reference voltages (a) and select_pre (b) driving circuits.*

2.4.3 Reset

Figure 2.11 shows the reset scheme used to forward bias the diode integrated on the SDD and, simultaneously, to drive the inhibit signal to reset the detector.

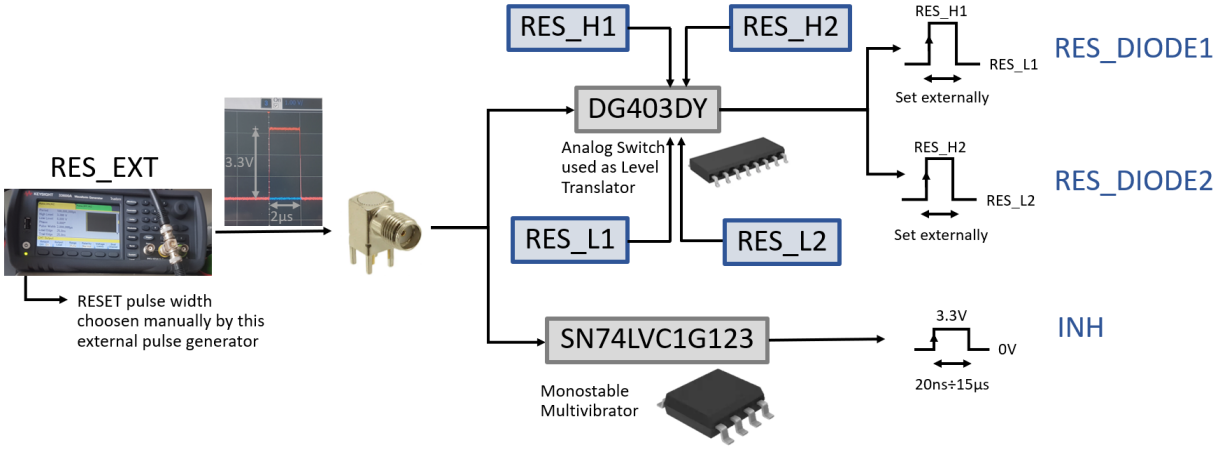


Figure 2.11: *Bias board reset scheme.*

In particular the reset signal (*RES_EXT*) is taken from an external pulse waveform generator (connected through a coaxial cable to one of the two SMA connectors) choosing a pulse amplitude of 3.3 V and a time width of 2 µs. This signal is used to drive a high-speed analog switch and a monostable multivibrator:

- The **high-speed analog switch** (*Vishay DG403DY*) is used as level translator to move the 3.3 V to *RES_H* level and the 0 V to *RES_L* level to generate the SDD diode reset signal. The two reset voltage values are generated from the ±15 V power supplies and each one is split in two independently regulated signals, resulting in: *RES_H1* and *RES_H2* for the high-level voltage; *RES_L1* and *RES_L2* for the low-level voltage. The voltage values can be adjusted by tuning the corresponding trimmer (Figure 2.12). *RES_H* can be set in the 0÷10 V range, while *RES_L* can be set in the -15÷0 V.

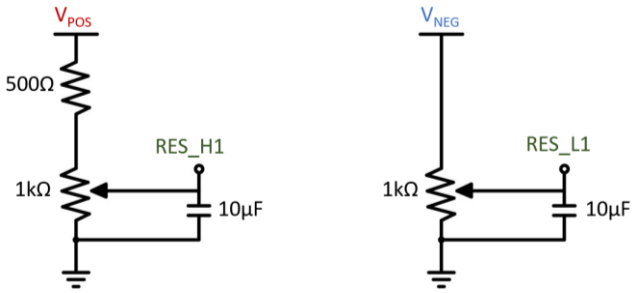
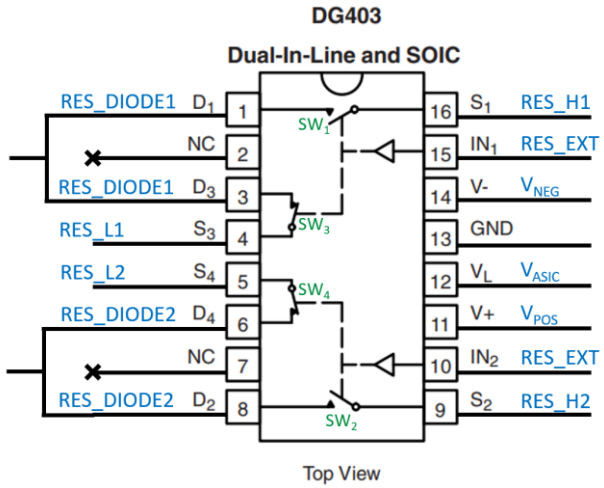


Figure 2.12: *Driving circuit of the reset voltage levels (the same for RES_H2 and RES_L2).*



(a) Schematic view of the analog switch

Two SPDT Switches per Package

TRUTH TABLE		
Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

(b) Truth table of the two SPDT switches

Figure 2.13: *Functional schematic and pin configuration reported in the datasheet [34].*

Figure 2.13 (a) reports a schematic view of the DG403DY analog switch. In blue are highlighted the different signals connected to the pins. Figure 2.13 (b) shows the truth table of the four *SPDT* switches: when *RES_EXT* is low (Logic = 0) the SW_1 and SW_2 are OFF, while SW_3 and SW_4 are ON, thus *RES_DIODE1=RES_L1* and *RES_DIODE2=RES_L2*; vice versa when *RES_EXT* is high (Logic = 1) the SW_1 and SW_2 are ON, while SW_3 and SW_4 are OFF, providing the *RES_H* level to the *RES_DIODE1* and *RES_DIODE2* out signals. The resulting output signals are two-level pulse voltage waveforms switching between *RES_H* and *RES_L* levels, with pulses duration equal to the *RES_EXT* pulse width set by the external waveform generator. The *RES_DIODE1* signal drives the 7 reset groups of the Northern hemisphere, via the left connection board, while the *RES_DIODE2* drives the 7 reset groups of the Southern hemisphere, through the right connection board.

The advantage of using this configuration, where all the signals are split, is that the switch on-resistance is halved ($R_{DS}(on)$ = 30 Ω) compared to a standard configuration using single *RES_H* and *RES_L* signals to generate a single *RES_DIODE* driving the entire SDD matrix (the requirement was to have $R_{DS}(on) \leq 45$ Ω).

- The "SN74LVC1G123" **monostable multivibrator** [35] is used to generate the inhibit signal for the ETTORE ASICs. It's supplied by V_{ASIC} and the output pulse duration is programmed by selecting external resistance and capacitance values. The capacitance must be connected between C_{ext} and R_{ext}/C_{ext} pins, while the external resistor between R_{ext}/C_{ext} and Vcc (= V_{ASIC}) pins. To obtain a variable pulse duration an external trimmer has been added in series to the resistance, as shown in Figure 2.14.

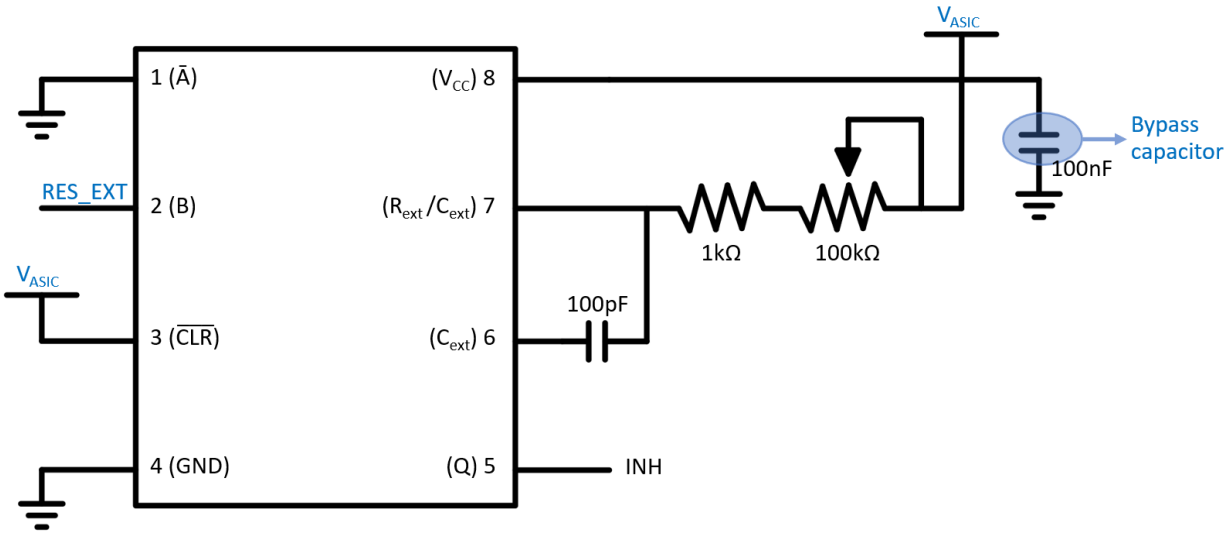


Figure 2.14: *Pin configuration and schematic circuit of the monostable multivibrator.*

RES_EXT signal is sent to the (B) pin, which is a *rising edge sensitive input* that requires (Ā) to be kept low and $\overline{CLR}$ high, accordingly to the datasheet indications. The 100 nF capacitor from *Vcc* pin to ground, placed as closed as possible to the device, is used as bypass capacitor to reduce the effect of voltage spikes on the power supply line due to the integrated circuit (IC) commutations.

The sizing of the remaining components is performed by looking at the application curve present on the datasheet and reported in Figure 2.15. Choosing a *Cext* of 100 pF, a resistance of 1 kΩ and a trigger of 100 kΩ, the *INH* pulse duration can range from about 20 ns to 15 μs by regulating the trigger value.

A second SMA connector is used to provide the same *RES_EXT* signal to the Athena DAQ (the two SMA connectors are connected to the same reset line on the PCB).

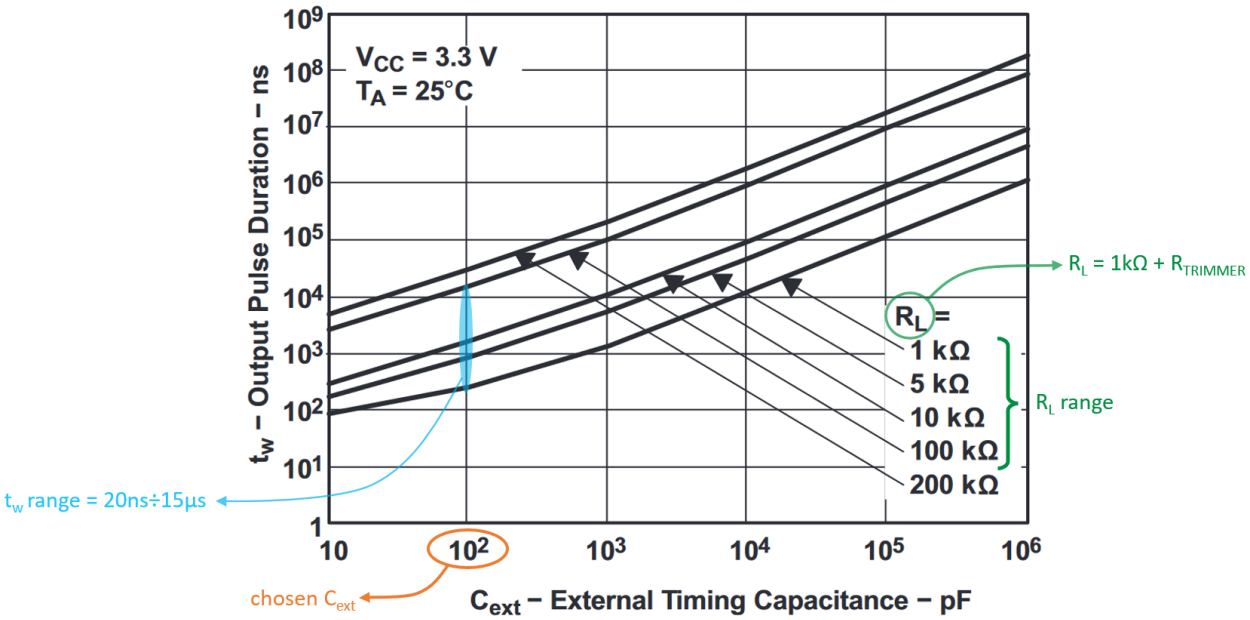
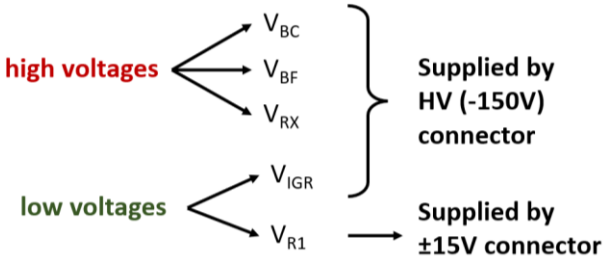


Figure 2.15: *Output pulse duration vs external timing capacitance for different R_L values.*

2.4.4 Detector bias voltages

Figure 2.16 gives a quick view of all the voltages needed to bias the detector. They can be divided in: "high voltages", provided by an external HV generator; "low voltages", driven by the same ±15 V external generator used for the positive and negative low voltages previously described. The only exception is V_{IGR}, driven by the HV generator, but adjustable in a relatively low-voltage range.



Name	Minimum V	Maximum V	Adjustable	Type
V_{IGR}	0V	-26.3V	Trimmer	Global
V_{R1}	-1.58V	-13.78V	Trimmer	Global
V_{RX}	-95V	-145V	2xTrimmer	Global
V_{BC}	0V	-150V	Trimmer	Global
V_{BF}	0V	-150V	Trimmer	Global

Figure 2.16: *Detector bias voltages.*

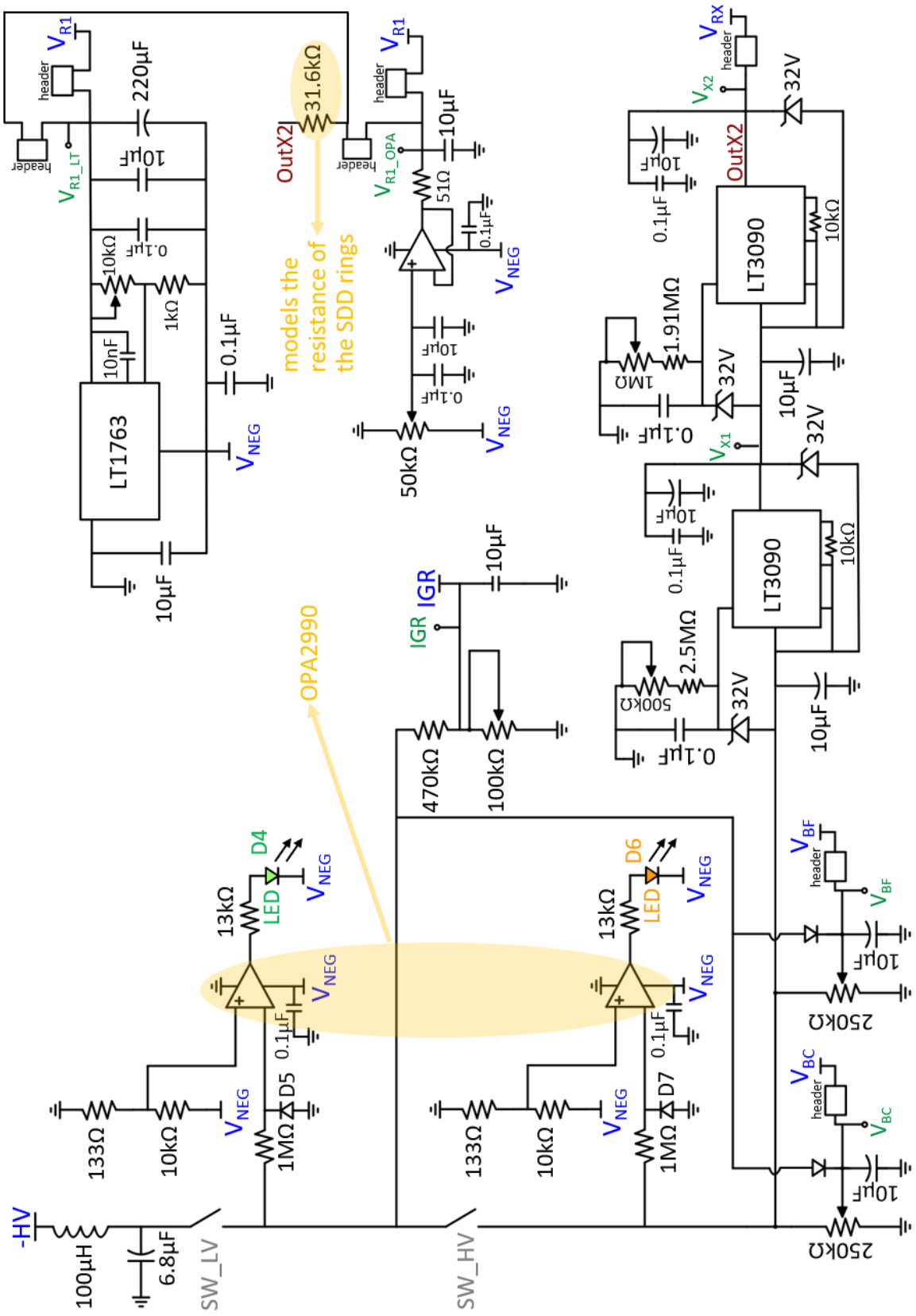


Figure 2.17: *Detailed detector bias schematic.*

The detailed detector bias schematic is shown in Figure 2.17:

- The low voltages switch (*SW_LV*) is used to connect the *-HV* (= -150 V) to the circuit. When it closes, the inner guard ring is activated and its voltage (V_{IGR}) is set by the trimmer in the 0÷26.3 V range. To make sure that *IGR* switches on, a green LED has been added to the circuit (Figure 2.18). The LED is driven by an OPAMP ("OPA2990", dual low-power operational amplifier [36]) biased between GND and V_{NEG}: when the *SW_LV* is open, the negative pin of the OPAMP is grounded and the output voltage of the OPAMP is V_{OUT} = -15 V so no current flows in the LED (*D4*) and it's switched off; when the *SW_LV* is closed, the negative pin of the OPAMP decreases until it's clamped by the diode at minus its forward voltage ($V^- = -V_F \approx$ -0.5 V), so the output voltage of the OPAMP rises up to 0 V providing a current flowing inside the LED which starts emitting a green light. In this way, since the LED and the *IGR* switches on at the same time, the *IGR* status can be easily seen by looking at the LED light.

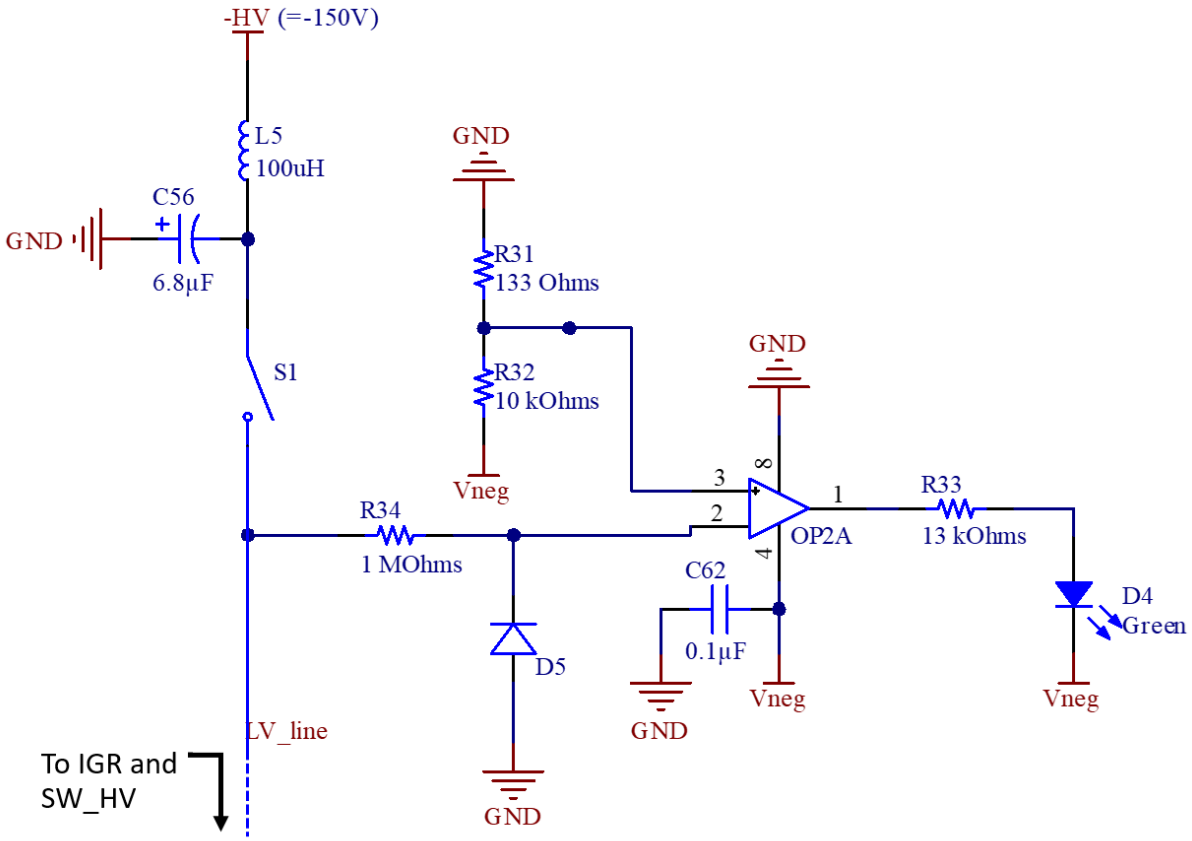


Figure 2.18: *LED driving circuit: S1 corresponds to SW_LV and OP2A is the OPAMP driving the LED.*

- The high voltages switch (*SW_HV*) is used to connect the lower side of the *SW_LV* to the V_{BC}, V_{BF} and V_{RX} biasing network. V_{BC} and V_{BF} are generated by using 250 kΩ trimmers, providing voltages adjustable over the entire 0÷150 V range. V_{RX} instead is generated by using a cascade of two LT3090 low-dropout voltage regulators. The internal schematic of the LT3090, provided by the manufacturer [37], is shown in Figure 2.19. In the Lifeboard, to generate an adjustable V_{RX}, the 1 MΩ resistance is substituted by a series of a fixed value resistance and a trimmer (as shown in Figure 2.17) and the 4.7 μF capacitances (minimum value required for stability) are replaced by 10 μF capacitances. The LT3090 features a 50 μA reference current source that flows into the *SET* pin, which is the inverting input of the error amplifier. This current, flowing through the series of the fixed resistor and the trimmer, generates a voltage at the negative input of the amplifier that, thanks to the negative feedback of the amplifier, is replicated at the positive input and so at the output pin of the regulator. The *SET* pin, and therefore also the *OUT* pin, can be up to 36 V above the *IN* pin. To take some margin, 32V Zener diodes have been chosen in place of the 36 V ones (fixing the maximum voltage drop between *SET* and *IN* to 32 V) and the series between the resistor and the trimmer has been sized to provide a voltage in the -150 ÷ -125 V range at the output of the first LT3090 and in the -145.5 ÷ -95.5 V range at the output of the following LT3090 (providing the V_{RX}). V_{BC}, V_{BF} and V_{RX} pins present a 2-pin header at their output, used to disconnect a particular voltage during test phase if needed.

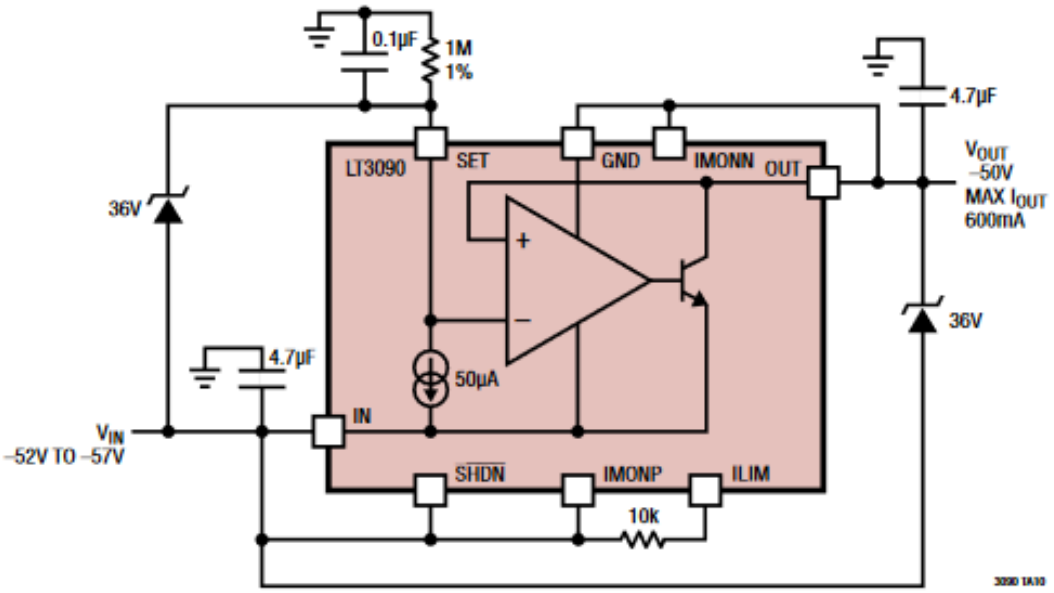


Figure 2.19: *LT3090 schematic circuit.*

To monitor the high voltages status, an orange LED has been connected to the bottom side of the high voltages switch (*SW_HV*). The driving circuit topology of the orange LED is the same used for the green LED discussed before and shown in Figure 2.18: the only difference is that now *S1* correspond to *SW_HV*, while the OPAMP used is the same OPA2990, being a dual operational amplifies featuring two identical OPAMPs in the same chip. This LED is important mainly during the switch off, since it visually indicates when the high voltages discharge completely (after opening the *SW_HV*) and so the *IGR* can be safely switched off by opening the *SW_LV*, as will be discussed later.

- Differently from the previous SDD biasing voltages, the V_{R1} is supplied by the ±15 V external generator. This voltage can be driven by two different networks by closing the corresponding 2-pin header (as shown in Figure 2.17):

    - The first network features a LT1763 voltage regulator powered between V_{NEG} and ground, able to provide a V_{R1} adjustable in the -1.58 ÷ -13.78 V range. The adoption of this solution is required by the outward going current needed at the V_{R1} pin to bias the SDD rings, not achievable by using a negative voltage regulator like the LT1964, which is only able to provide a negative current at its output.

    - The alternative network features an OPA990 in buffer configuration. This OPAMP is used to buffer at the output the voltage at the positive input generated by a trimmer in the 0 ÷ -15 V range. Like the previous, also this network is able to provide an outward going current to correctly bias the SDD rings.

- A 31.6 kΩ resistor, connected to the *OutX2 line*, can be used to simulate the SDD rings during the testing phase of the Lifeboard since this resistance value is equal to the overall ring resistance of the entire detector. This resistor can be easily connected to one of the two V_{R1} networks by closing the corresponding header and opening the header connecting the real detector (opening the one connected to the blue V_{R1} label in Figure 2.17). This "simulated SDD" allows closing the circuit with the same resistive load and so having a more realistic model to be used during the test of the system, before connecting the real detector to avoid damages.

- The detector bias network features a **detector protection system** to protect the detector during the switching off phase. Specifically, if the circuit is switched off by opening the *SW_LV* before the *SW_HV*, it may happen that the V_{IGR} drops down while V_{BC} and V_{BF} are still at high absolute values. This situation may damage the detector, so two diodes have been added between the bottom of the *SW_LV* and the V_{BC} and V_{BF} lines. Before opening the *SW_LV* the two diodes are in reverse bias; switching off the *SW_LV*, the upper side becomes more positive until the diodes switch on pushing current toward V_{BC} and V_{BF} making them increase toward 0V in a faster way and slowing down the $|V_{IGR}|$ decreasing. In this way the high voltages discharge before than the V_{IGR}, preventing any damages to the detector caused by high electron fluxes reaching the JFET due to the low V_{IGR}.
  Figure 2.20 shows the real discharging curves, measured with the oscilloscope during testing phase, with and without the diode protection mechanism: the first and the second plots show the discharge of the V_{IGR} and the V_{BC} highlighting the longer discharge time of the back contact with respect to the inner guard ring if the protection system is not acting; the third plot instead shows the precise moment when the diode mechanism enters into place slowing down the discharge of V_{IGR} and speeding up the V_{BC} discharge.

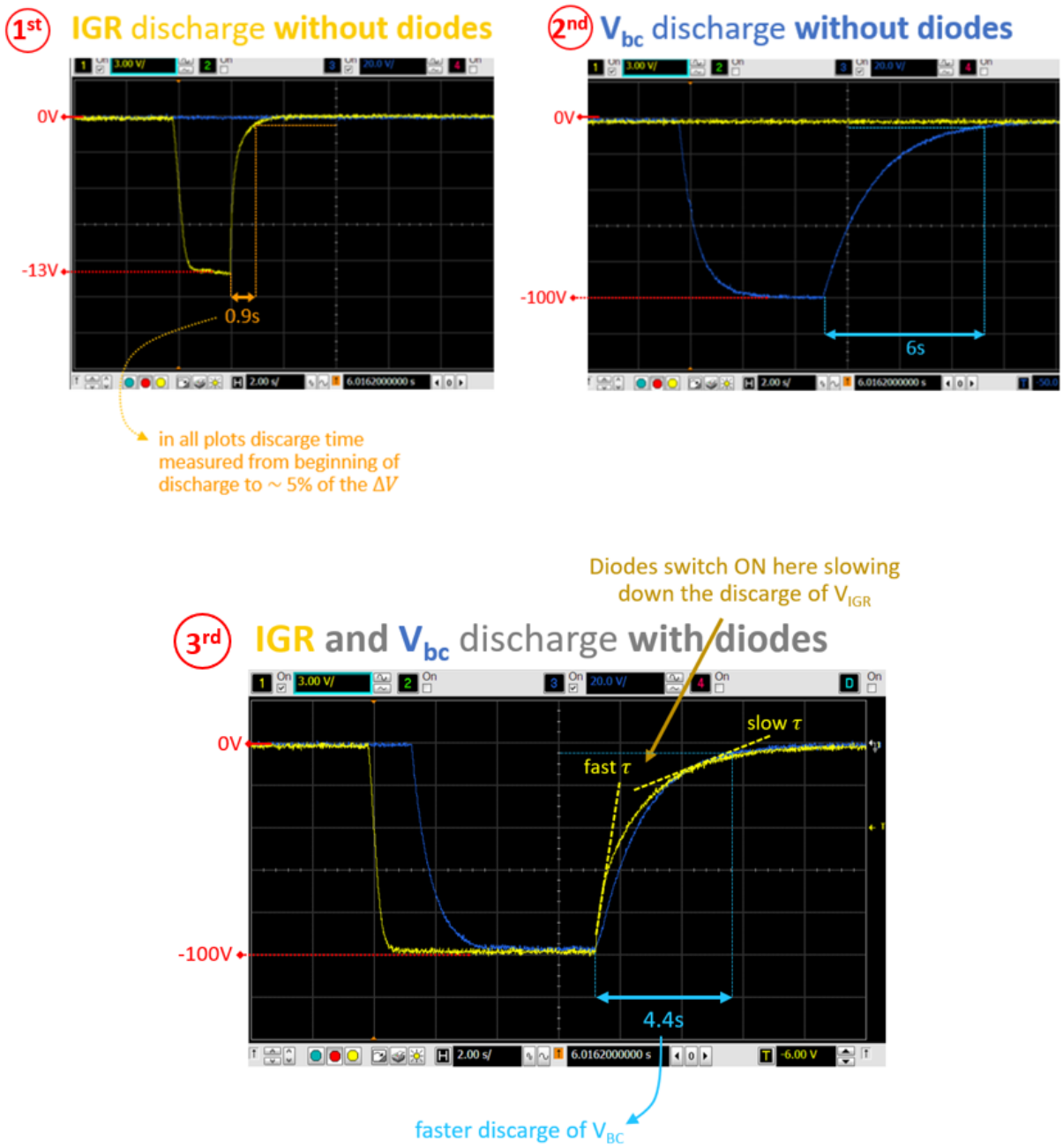


Figure 2.20: *Real discharging curves with and without the diode protection mechanism.*

2.4.5 Layout choices

During the design of the bias system, various layout choices has been taken to avoid or limit possible issues.

- To limit the maximum current flowing in each pin of the two board-to-board "SAMTEC-SFM-120-02-X-D-A" connectors (illustrated in Figure 2.21), the following choices has been done:

  - V_{IO1}/V_{IO2} is shared between 4 different pins, resulting in an expected current per pin of:

$$I_{PIN} = \frac{I_{ASIC}}{N_{pins} \times N_{connectors}} = \frac{700\ mA}{4 \times 2} = 87.5\ mA \tag{2.7}$$

  - V_D is shared between 2 different pins, resulting in an expected current per pin of:

$$I_{PIN} = \frac{I_D}{N_{pins} \times N_{connectors}} = \frac{50\ mA}{2 \times 2} = 12.5\ mA \tag{2.8}$$

  - V_{SSS1}/V_{SSS2} is shared between 2 different pins, resulting in an expected current per pin of:

$$I_{PIN} = \frac{I_{SSS}}{N_{pins} \times N_{connectors}} = \frac{50\ mA}{2 \times 2} = 12.5\ mA \tag{2.9}$$

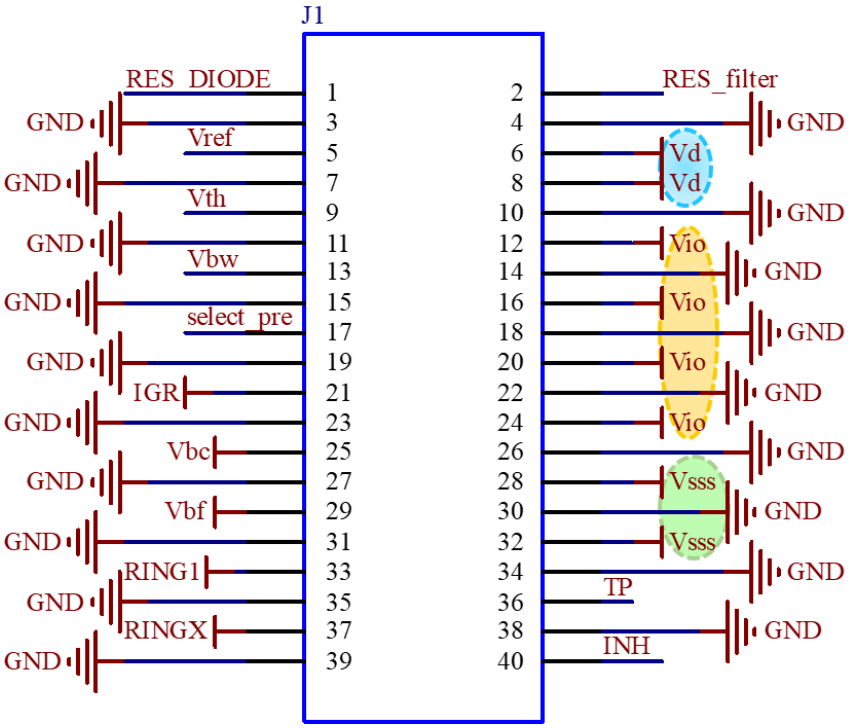


Figure 2.21: *Schematic view of the connector with shared pins highlighted with same colour.*

In addition to that, not to reach critical temperatures due to large current flowing in too small tracks, during the PCB routing it has been decided to use larger tracks for these voltage lines compared to the other signal lines (as shown in Figure 2.22).

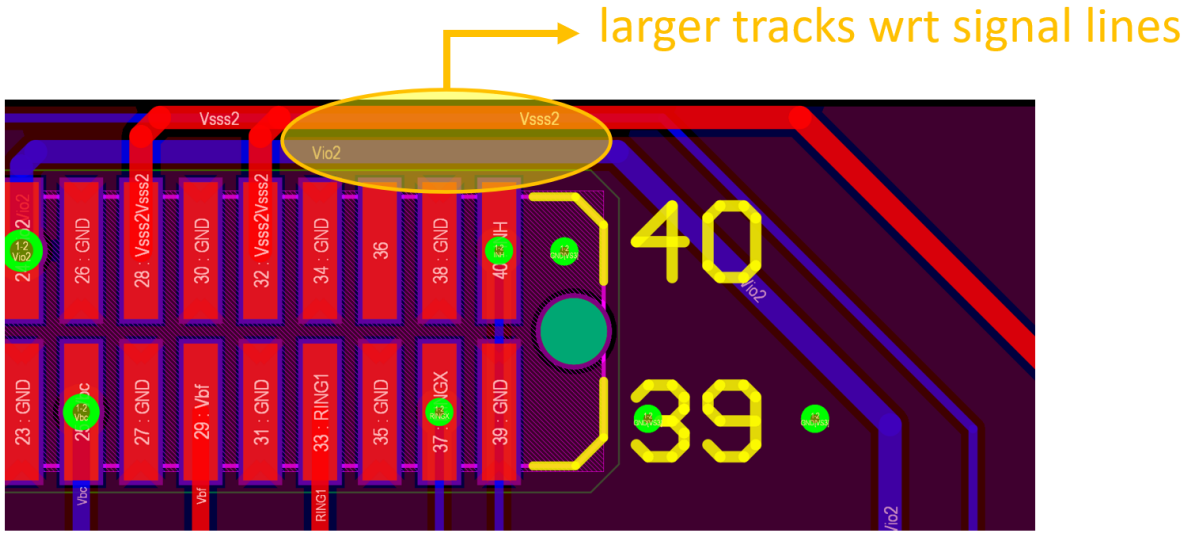


Figure 2.22: *Detail of the V_{IO2} and V_{SSS2} lines in the PCB layout view.*

- To reduce crosstalk or any other kind of inter-track disturbances, two main strategies has been adopted:
    - Avoid long tracks with fast signals running in parallel near to each other, keeping them as far as possible on the same layer, or making them run on different layers reducing as much as possible the regions where they are placed in parallel.
    - Use interleaving ground pins both in the board-to-board SAMTEC connectors (Figure 2.21) and in the 100-pin connectors (Figure 2.5).

2.5 Problems and Solutions

During the testing phase of the Lifeboard bias system, the following problems arose:

- The DC-DC converter and the LT1963 voltage regulators, used to provide the V_{IO}, featured a too small output current.
- The high voltage switch (*SW_HV*) produced a spark when switched on.
- The high voltage and low voltage status LEDs did not work correctly when the Lifeboard was connected to the entire system.
- There was an unexpected power consumption increase when the external reset signal (*RES_EXT*) was provided to the system.

2.5.1 Voltage regulator and DC-DC converter

The estimated ETTORE ASIC power consumption, provided by the manufacturer, is about 15 mW for each channel. The supply voltage is 3.3 V, so:

$$I_{channel} = \frac{P_{channel}}{V_{ASIC}} = \frac{15\ \text{mW/ch}}{3.3\ \text{V}} = 4.55\text{m A/ch} \tag{2.10}$$

Every ASIC board features 7 ASICs, each of them with 12 channels. Therefore, the total current required by each ASIC board is:

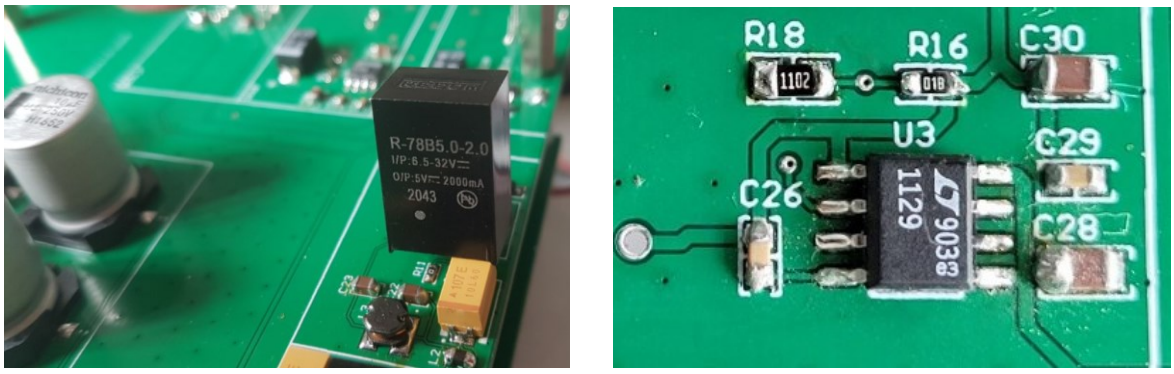
$$I_{ASIC\_board} = I_{channel} \times N_{ASIC} \times N_{channels} = 4.55\ \text{mA/ch} \times 7 \times 12 = 382.2\ \text{mA} \tag{2.11}$$

However, during the testing phase of the system, a larger current consumption has been measured, equal to 550 mA (= I_{ASIC_M}) for each ASIC board. This value corresponds to a larger power consumption for each channel compared to the nominal one, as computed in Eq. (2.13):

$$I_{channel} = \frac{I_{ASIC\_M}}{N_{ASIC} \times N_{channels}} = \frac{550\ \text{mA}}{7 \times 12} = 6.55\ \text{mA/ch} \tag{2.12}$$

$$P_{channel} = I_{channel} \times V_{ASIC} = \ 6.55\ \text{mA/ch} \times 3.3\text{V} \ = 21.6\ \text{mW/ch} \tag{2.13}$$

Each of the two LT1763, used to provide the V_{IO} to the ASICs, can supply up to 500 mA to its output (V_{IO1} or V_{IO2}). This value is not enough due to this unexpected increase of the ASIC current consumption. To fix this issue, the LT1763 voltage regulator has been replaced by the LT1129, whose maximum output current is 700 mA [38]. As discussed in previous section, the two voltage regulators are driven by a DC-DC converter. Specifically, the "R-78C5.0-1.0" DC-DC converter has a maximum output current of 1 A [33], which is not enough to supply the ASICs. This led to the choice of a new DC-DC converter ("R-78B5.0-2.0"), featuring a maximum output current of 2 A [39]. The new components have been soldered on the bias board in place of the old ones, as illustrated in Figure 2.23.



(a) (b)

Figure 2.23: *Detail of the new components soldered on the bias board. (a) The "R-78B5.0-2.0" DC-DC converter. (b) The LT1129 voltage regulator.*

The two replacements are summarized in Figure 2.24 and the new positive power network is shown in Figure 2.25.

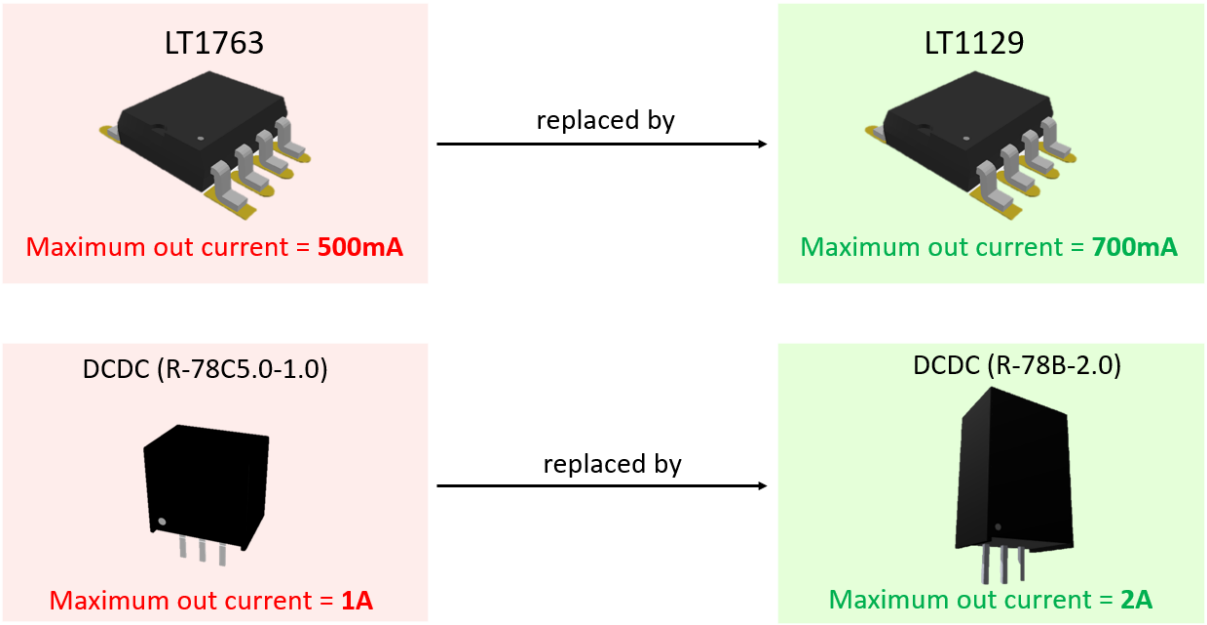


Figure 2.24: *Old (in red) and new (in green) DC-DC converter and voltage regulators.*

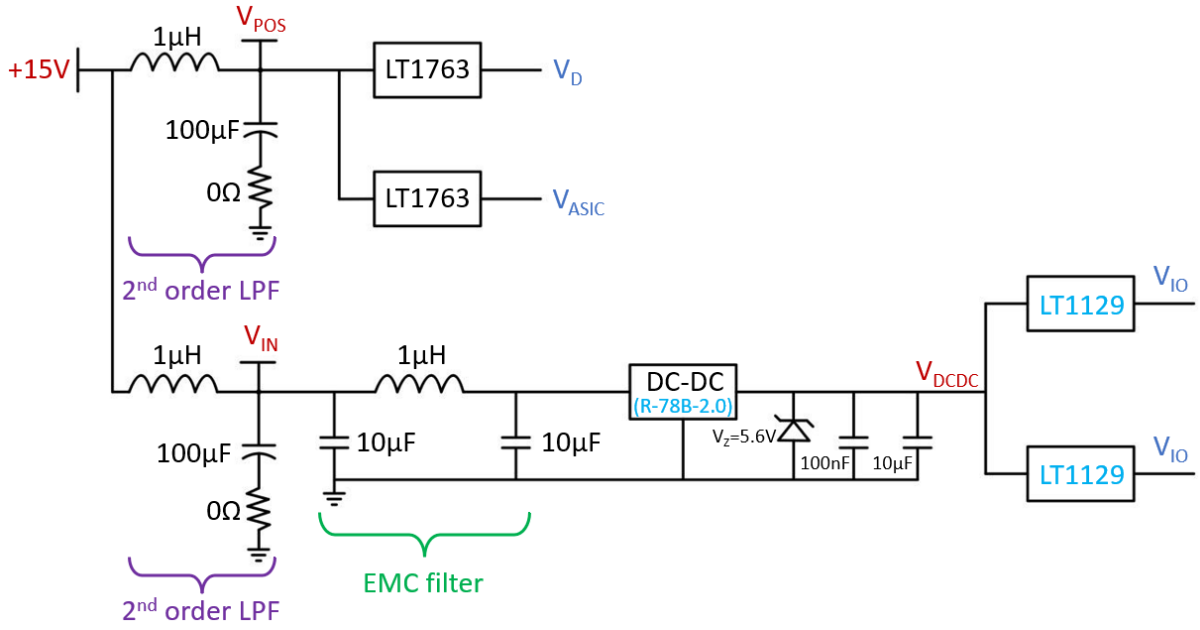


Figure 2.25: *Schematic view of the positive power network after the replacements.*

Each LT1129 regulator absorbs an ASIC bias current of 550 mA, resulting in a maximum power dissipation given by:

$$P_{max} = I_{max} \times (V_{in} - V_{out}) = 550\ \text{mA} \times (5\ \text{V} - 4.1\ \text{V}) = 0.495\ \text{W} \quad (2.14)$$

The LT1129 has a worst case thermal resistance junction-to-case of $R_{\theta JC}$ = 69 °C/W (for S8 package) and a maximum rated junction temperature of T_{Jmax} = 125 °C, so the maximum allowed ambient temperature of operation is:

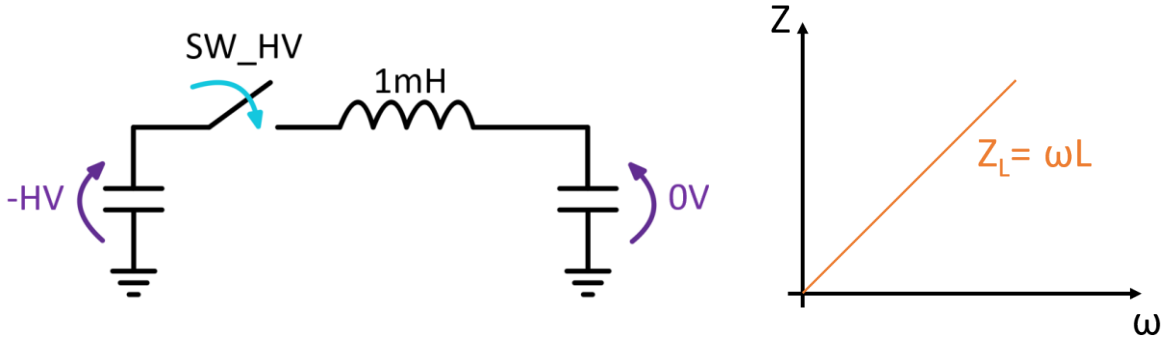
$$T_A = T_{jmax} - P_{max} \times R_{\theta JC} = 125\ °\text{C} - 0.495\ \text{W} \times 69\ °\text{C/W} = 90.85\ °\text{C} \quad (2.15)$$

This value is more than enough to safely work also in presence of near components that may locally increase the ambient temperature.

2.5.2 Sparkling high voltage switch

The high voltage switch (*SW_HV*), used to connect the *-HV* generator (through the SW_LV) to the V_{BC}, V_{BF} and V_{RX} biasing network, showed a spark during the switching on. This is due to the high transient current flowing in the line as soon as the switch is closed, caused by the charging of LT3090 input capacitor (initially discharged at 0 V) instantaneously put in parallel to the already charged capacitor (the 6.8 µF filter capacitor charged at *-HV*).

To solve this problem, a 1 mH inductor has been placed in series to the *SW_HV* to avoid this instantaneous huge current flowing in the line (Figure 2.26). Indeed, the inductor has an impedance $Z_L=\omega L$, behaving as a high impedance when the switch suddenly switches on. Thus, the instantaneous current flowing through the switch keeps low, solving the spark issue.



(a) (b)

Figure 2.26: *(a) Schematic view of the SW_HV circuit solution to avoid sparks. (b) Z_L vs ω graph.*

2.5.3 Status LED indicators

Figure 2.27 illustrates a simplified view of the detector bias network, including the SDD that connect the V_{RX} biasing circuit to the V_{R1} biasing circuit. In particular, when the V_{R1} switches on, it is connected to V_{RX} through the SDD rings resistance.

Setting V_{R1}= -8 V, the measured voltage on the line connected to the bottom side of *SW_HW* decreases to -5.4 V, while the voltage on the line between the two switches goes down to -3.2 V even if both *SW_LV* and *SW_HV* are open. These two negative voltages, that were expected to be zero, turn on respectively the orange LED and the green LED as soon as the ±15 V external generator powers on the V_{R1} biasing network. This behaviour is wrong, since the green LED should switch on when the *SW_LV* gets closed and then the orange LED should switch on when the *SW_HV* gets closed.

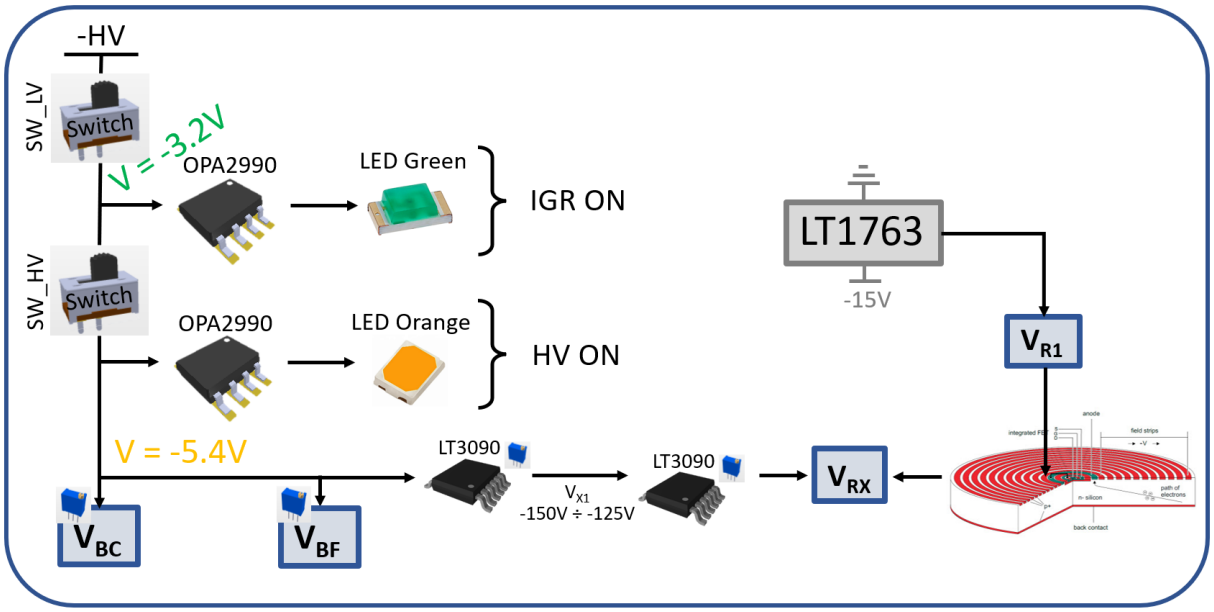


Figure 2.27: *Simplified view of the detector bias network.*

Looking more in detail the two LED driving circuits (see Figure 2.28), this unexpected behaviour is due to the more negative voltage present at the negative input of the two operational amplifiers (V^- = -0.33 V or -0.36 V) compared to the voltage at the positive pin (V^+ = -0.197 V) that brings the OPAMP's output nodes to ground. The current flows through the LEDs, switching them on even if the two mechanical switches are open. In this way there is no difference in having the switches on or off, the effect is the same.

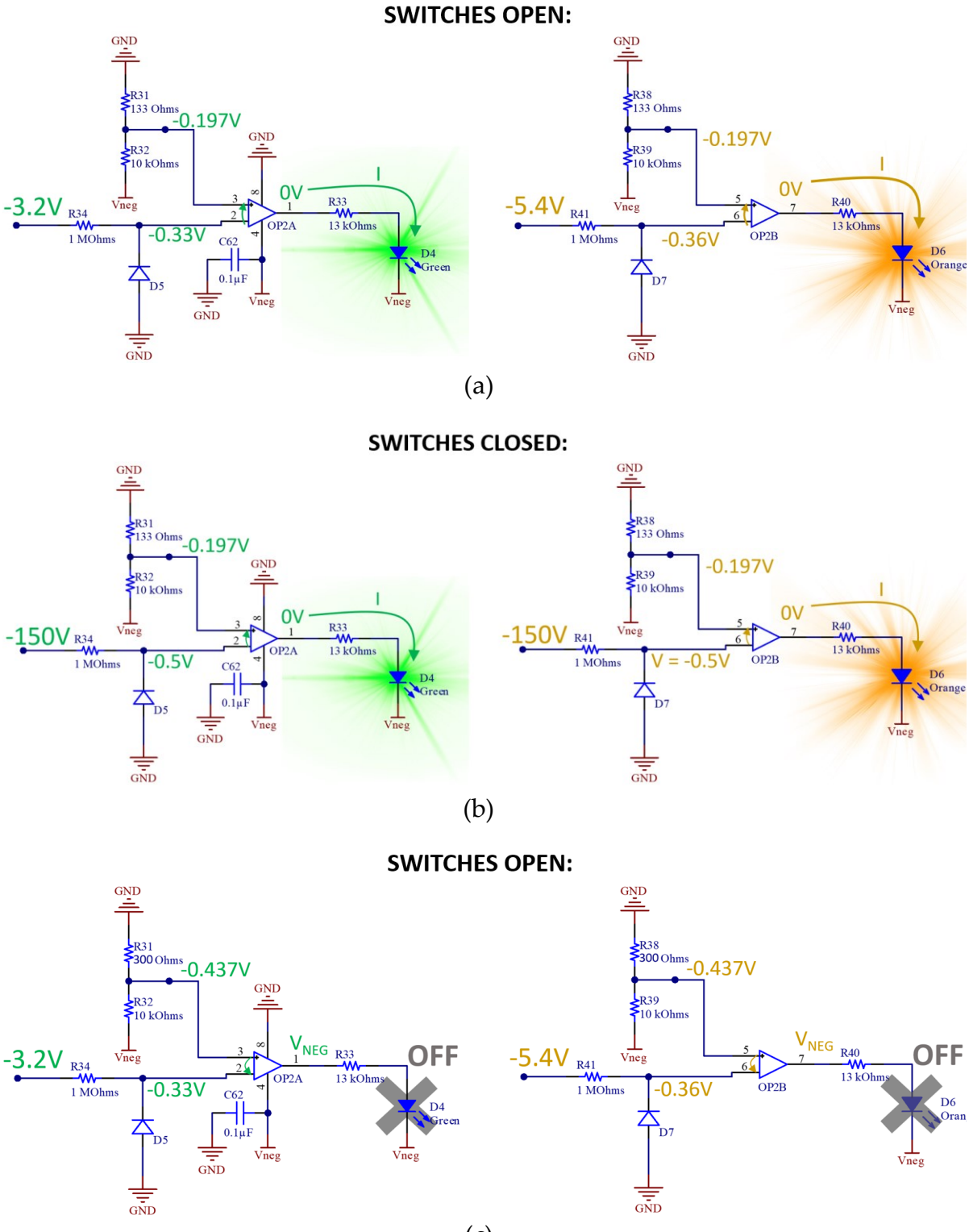


Figure 2.28: *LED driving networks. (a)LEDs don't switch off even if the switches are open. (b) LEDs on when switches are closed. (c) Issue solved: LEDs correctly switched off when the switches are open.*

To solve this problem, it has been changed the resistive partition in such a way that:

- when the **switches** are **open,** the positive input voltage (V^+) results more negative than the voltage measured at the negative input (V^- = -0.33 V or V^- = -0.36 V) so the output voltage is V_{NEG} = -15 V and the LEDs are switched off.

- when the **switches** are **closed**, the positive input voltage (V^+) results more positive than V^- = -0.5 V, so the output voltage is 0 V and the LEDs switch on.

Choosing a R = 300 Ω (in place of the previous R = 133 Ω), the positive pin voltage becomes V^+ = -0.437 V, inside the range between the minimum voltage drop across the diode (V^- = -0.33 V or V^- = -0.36 V) and the maximum one (V^- = -0.5 V)[1].

The final LEDs correct behaviour is shown in Figure 2.29.

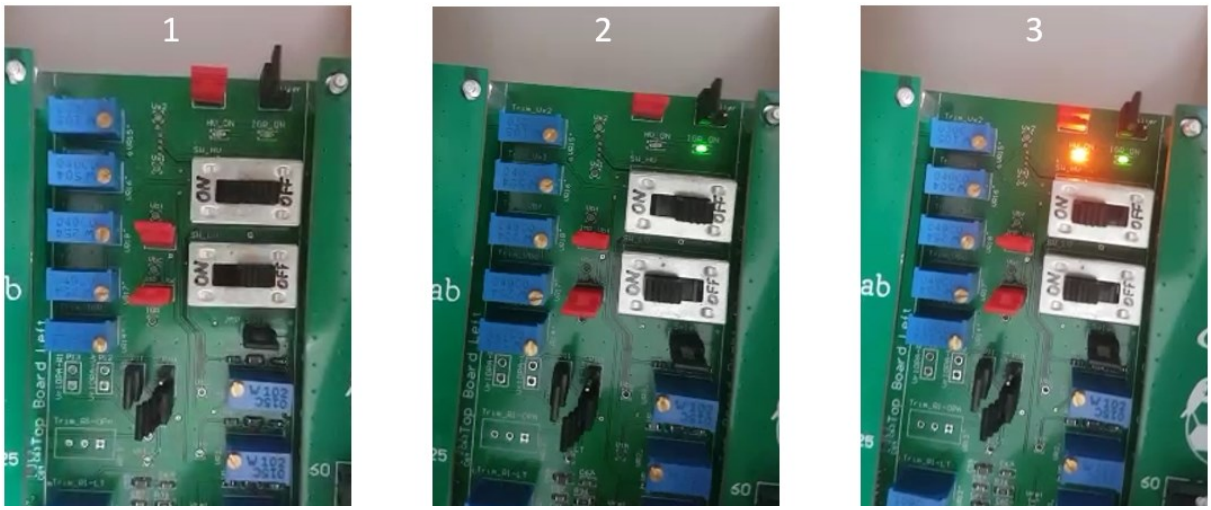


Figure 2.29: *Correct diode behaviour during SDD high voltage switching on procedure.*

[1] *the forward voltage drop across the diode (D5 or D7) increases increasing the current flowing through it (so the voltage drop across R = 1 MΩ): it's minimum when the switches are open (-3.2 V or -5.4 V on the input line); maximum when the switches are closed (-150 V on the input line).*

2.5.4 Power consumption increase

During the testing phase, an unexpected power consumption increase was measured when the external reset signal (*RES_EXT*) was provided to the bias board, bringing the setup in a high-current consumption condition (limited by the 1.4 A external generator limitation set to protect the system from overcurrent conditions).

Specifically, the setup switched on and started working fine, but then, after few minutes of operation, this high-current condition was reached. This caused the V_{IO} supply voltage to drop from the nominal 4.1 V and some of the ASICs stopped working correctly. Switching off and restarting the system solved temporarily the problem, but after some minutes the high-power consumption condition was reached again.

When the system was working for some time, this effect became more frequent (when the *RES_EXT* signal was provided, the high-current condition was reached in a shorter time). A possible reason for this behaviour was initially supposed to be a temperature dependence but, measuring the temperature with a thermographic camera, nothing on the ASIC board region got too hot (see Figure 2.30).

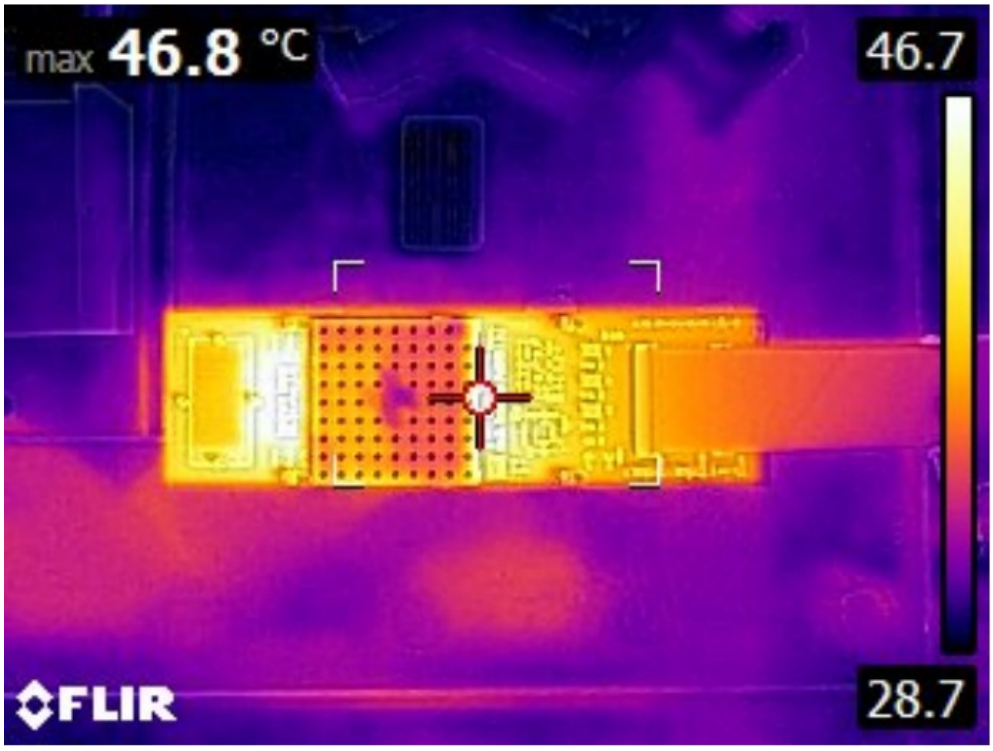


Figure 2.30: *Thermographic camera view showing the ASIC board temperature during operation.*

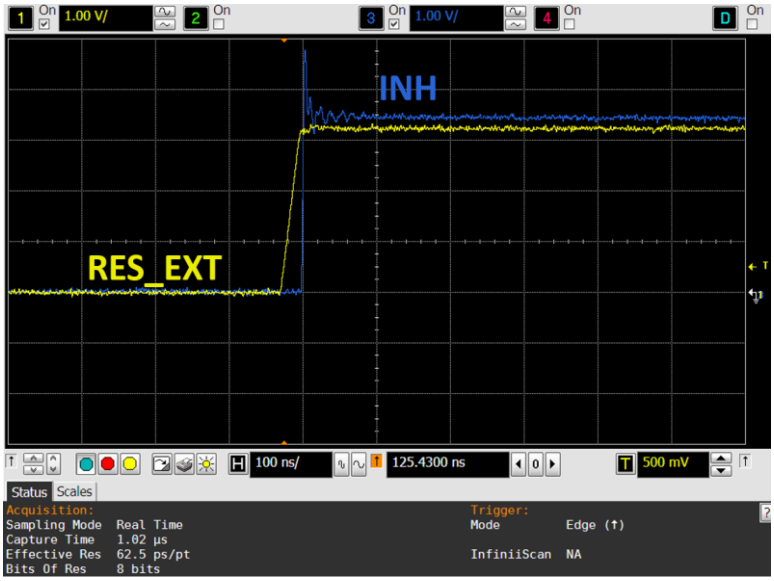
An important observation is that when only an ASIC board was connected, the high-current condition occurred instantaneously. Connecting only one ASIC board means having about half the output impedance load. This last statement is the key point to understand this issue and to find the solution to fix it. This problem is related to the external reset signal, and the first attempt was to set to 0 V both *RES_H* and *RES_L* to stop the SDD reset, but the issue was still present. Thus, the only remaining candidate to cause this high-current condition was the inhibit signal. Looking at its waveform with the oscilloscope, an overshoot was clearly visible as soon as the *RES_EXT* signal was provided and it had different amplitude if none, one or both the ASIC boards were connected. This brought us to the conclusion that the overshoot depended on the load attached to the inhibit line and, since some ASICs are sensitive to it, a sort of latch-up condition was observed. A test performed with a single pulse waveform generator, used to provide the *RES_EXT* signal, showed that just a single inhibit signal with overshoot is sufficient to observe the phenomenon. In particular:

- Figure 2.31(a) illustrates the behaviour with no ASIC boards attached to the bias system, where the inhibit signal has an overshoot synchronously to the *RES_EXT* rising edge (as described before). A slightly attenuated inhibit shape was observed with one ASIC board connected, instantaneously bringing the ASICs into latch-up condition. Instead, with both ASIC boards connected, the overshoot was enough attenuated not to bring the ASICs into latch-up condition, but still enough high to bring them if a periodic reset was provided at the input.

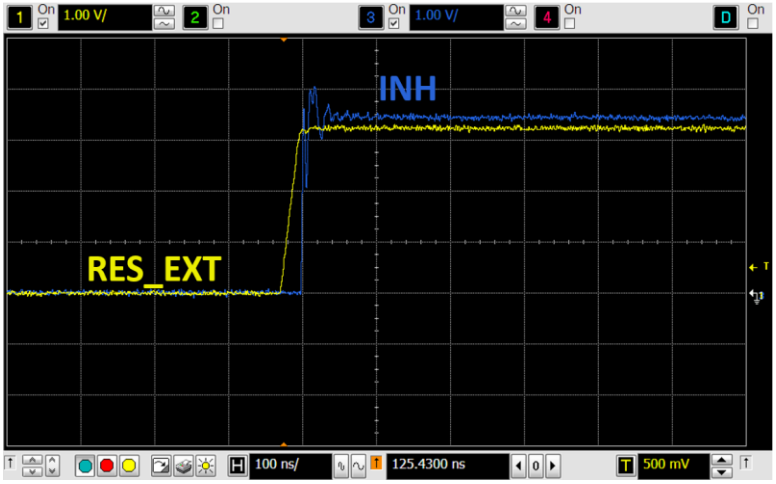
- Figure 2.31(b) shows what happens adding a 100 pF capacitance toward ground to the inhibit line, with no ASIC boards attached to the bias system. It is clearly visible that the overshoot is damped a lot.

- Figure 2.31(c) displays what happens connecting both the 100 pF capacitance and the two ASIC boards. The overshoot is further reduced, since now the load attached to the inhibit line is higher. In this configuration the latch-up condition was no more observed, even providing a periodic reset.

(a)



(b)



(c)

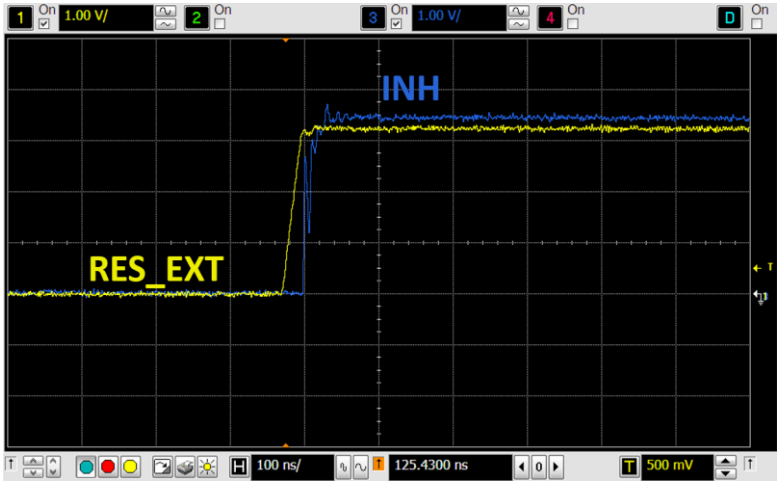
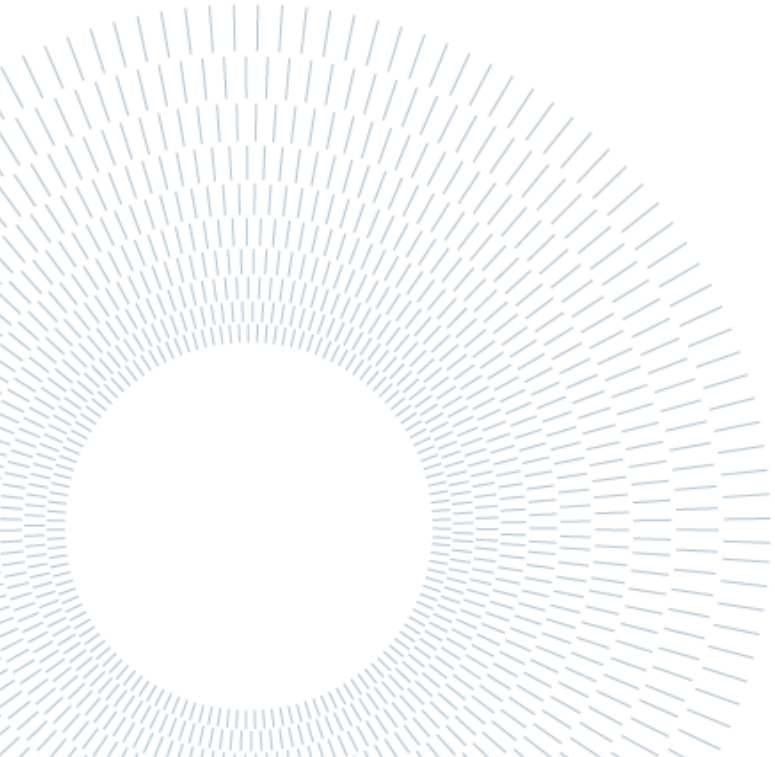


Figure 2.31: *Single pulse external reset and inhibit waveforms measured with oscilloscope.*



3. In air 166-pixel module characterization

This Chapter presents the characterization of the 166-pixel module. It stars from the preliminary tests made on the Lifeboard bias system to verify the correct behaviour and optimize the performances before connecting the detector and the ^{55}Fe radioactive source.

The 166-pixel measurement setup is then described, giving an overview of the detector box and of the 192-channel Athena system (DAQ) that, alongside the bias system, represent the main components of the planar setup.

In the following, all the preliminary characterization measurements performed using the ^{55}Fe radioactive source are described, including energy spectra, resolution, gain and count rate calculations.

Finally, a long-time stability measurement of the setup is described, and the results are shown at the end of this Chapter.

3.1 Lifeboard test and optimization

3.1.1 Testing and soldering

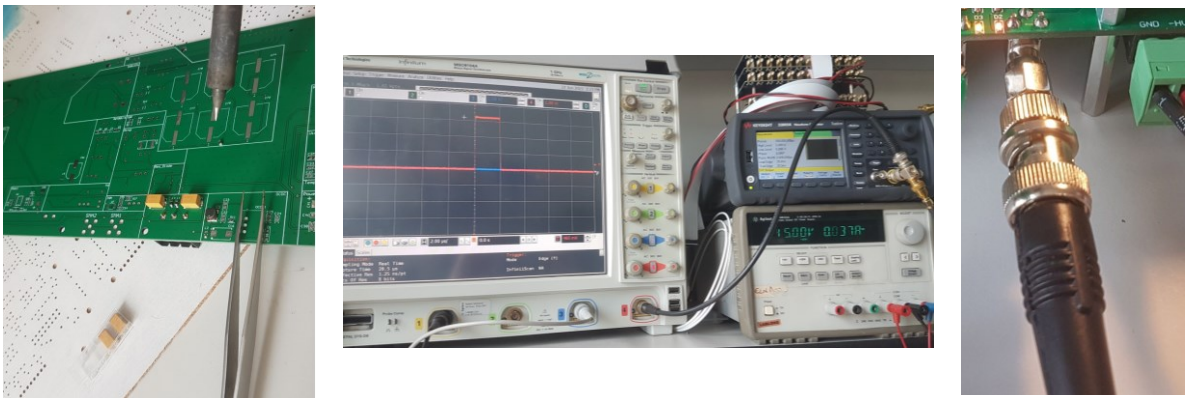
During the soldering phase of the Lifeboard bias system, each section has been tested with a step-by-step approach:

- The positive and negative low voltage section was the first to be soldered and V_{IO}, V_D, V_{ASIC} and V_{SSS} were correctly working in the right voltage ranges.

- Then the reset signal section has been soldered and tested connecting one of the two SMA connectors to the external pulse generator using a coaxial cable, while

probing the inhibit and the reset diode signals with the oscilloscope (see Figure 3.1).

- After that, the reference voltages section and the detector bias section have been soldered and tested. For the detector bias voltage an additional external voltage generator is required to provide the *-HV* = -150 V to supply V_{BC}, V_{BF}, V_{RX} and V_{IGR}. A picture of the completed bias board with all the components is shown in Figure 3.2, displaying also the 25 mm standoffs used to mount the two connection boards on top of the bias board. 12 mm standoffs are instead placed on the bottom side of the bias board to lift it up in order to allow to plug in the external connectors and not to press the bottom side components.



(a) (b) (c)

Figure 3.1: *Soldering and testing phases. (a) Soldering of the first components over the bias board. (b) Test of the reset section probing the inhibit signal with the oscilloscope. (c) Detail of the coaxial cable connected to the SMA to provide the RES_EXT to the system.*

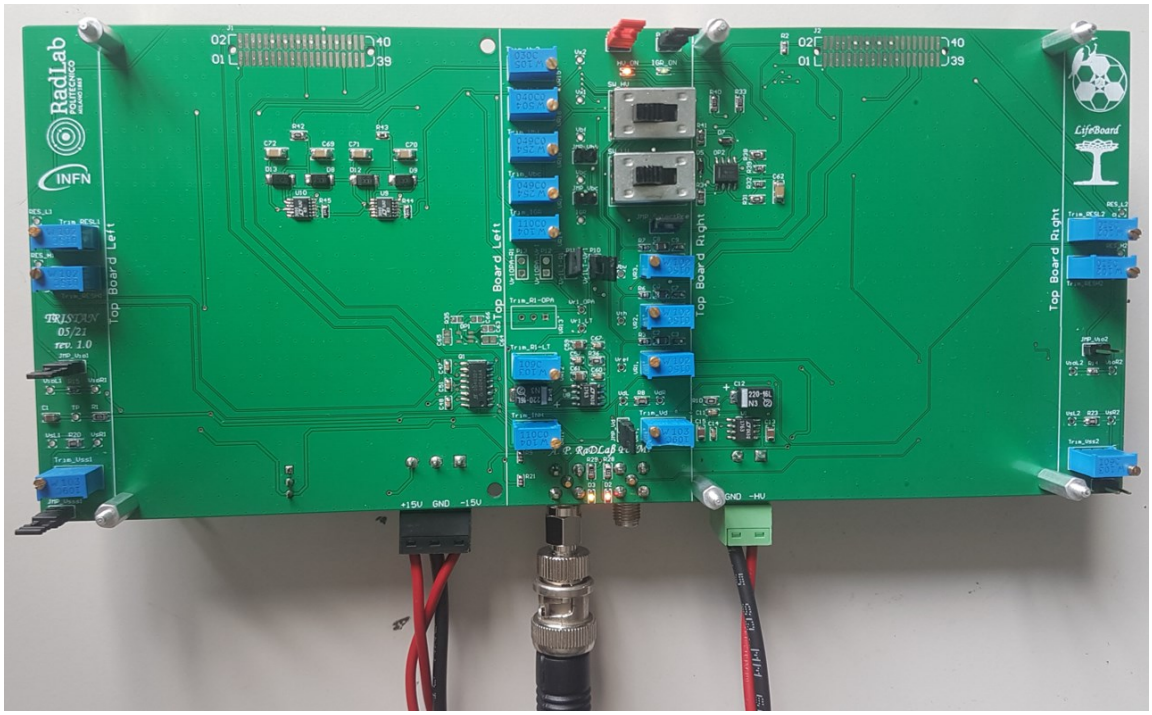
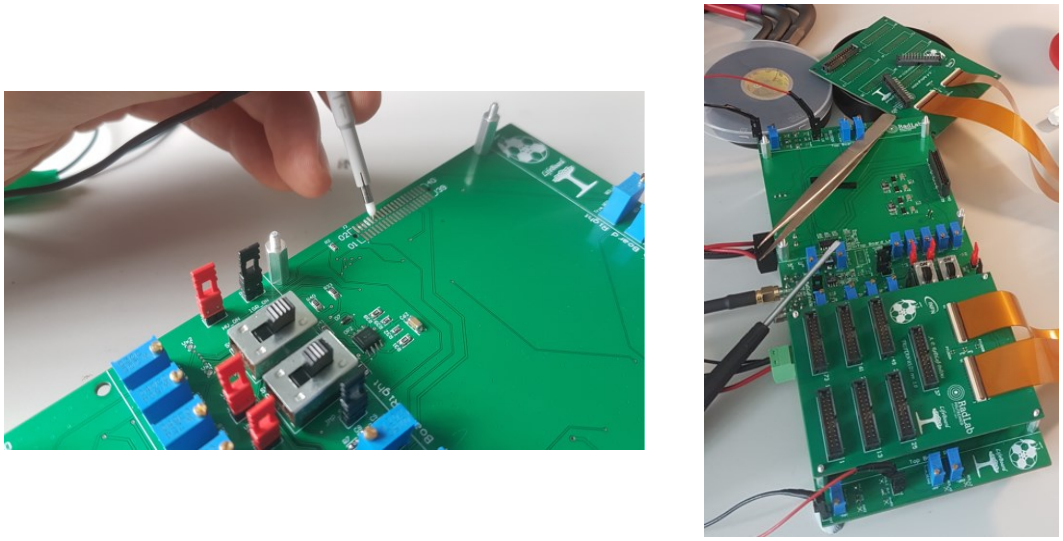


Figure 3.2: *Top view of the fully soldered bias board.*

- Before soldering the 40-pin board-to-board SAMTEC connectors, all the PCB pads have been carefully probed to verify their operation, as shown in Figure 3.3(a).



(a) (b)

Figure 3.3: *(a) PCB pads probing. (b) Soldering of the 24-pin connectors.*

- Finally, the seven 24-pin and the two 100-pin connectors have been soldered to the two connection boards attaching also the FPC cables, as illustrated in Figure 3.3(b). The connection boards are then mounted on the 25 mm standoffs, fixing them with bolts (see Figure 3.4).

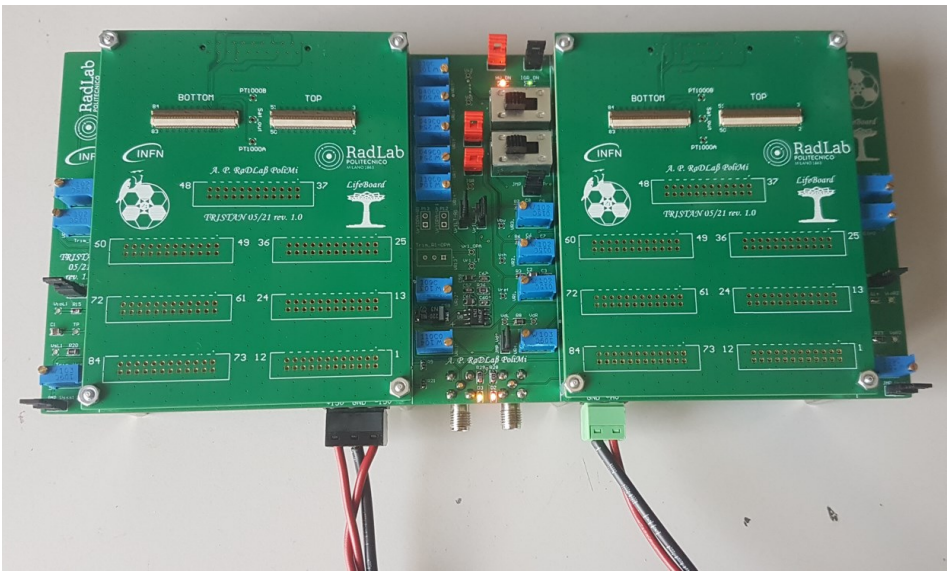
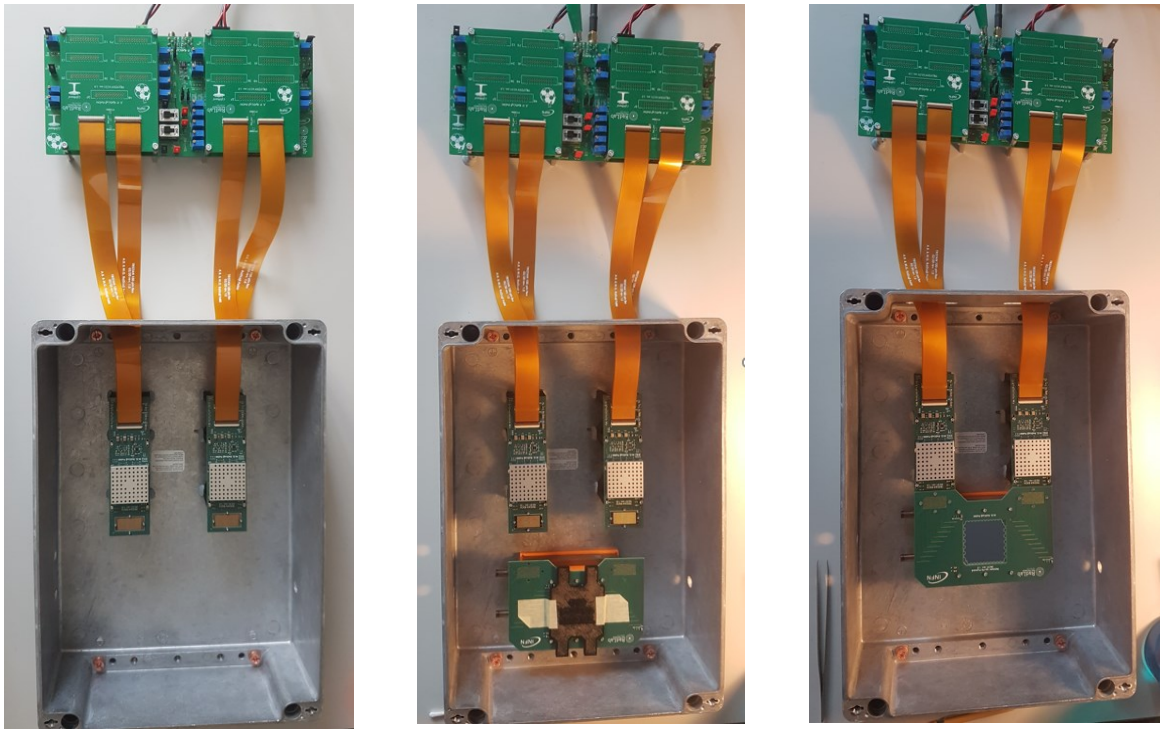


Figure 3.4: *Fully mounted Lifeboard bias system.*

A preliminary measurement, closing the biasing loop using the 31.6 kΩ resistor to reproduce the SDD rings resistance, has been performed. All the DC voltages were correctly set and adjustable in the designed ranges. At this point the biasing system has been connected to the ASIC board using the FPC cables so that the detector, wire bounded on the detector board (connected to the ASIC board), is now ready to be tested (see Figure 3.5 and Section 3.2.1).

As a first test, a simply output probe using the oscilloscope at room temperature has been performed: all the channels were perfectly functional, showing output ramps (due to the leakage current integrated on the feedback capacitance C_{FB} = 25 fF), as displayed in Figure 3.6.



(a) (b) (c)

Figure 3.5: *Boards connections steps. (a) Lifeboard connected to the two ASIC boards. (b) Detector board added inside the box, with a black protection case for the detector. (c) Detector board connected to the two ASIC boards.*

Figure 3.6: *Output ramps measured with the oscilloscope.*

3.1.2 DC-DC vs external voltage generator

In the bias board there are two different ways to provide the V_{IO} biasing voltage:

- Using an external voltage generator.
- Using the LT1129 voltage regulators driven by the DC-DC converter.

The selection is done using two headers, one for V_{IO1}, the other for V_{IO2}, as displayed in Figure 3.7.

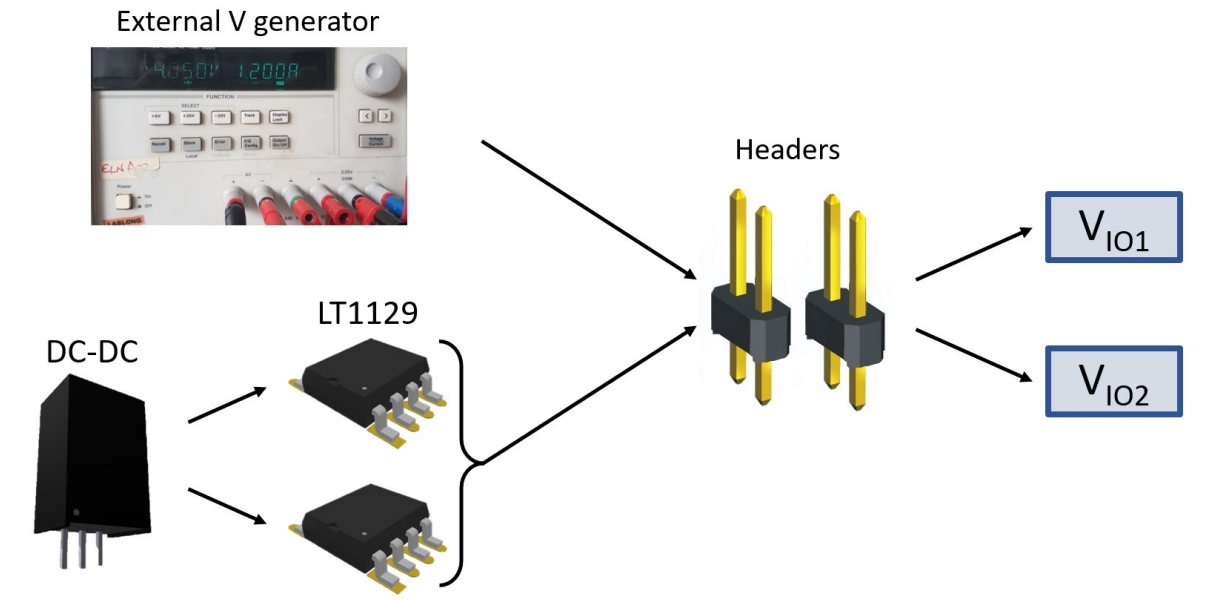
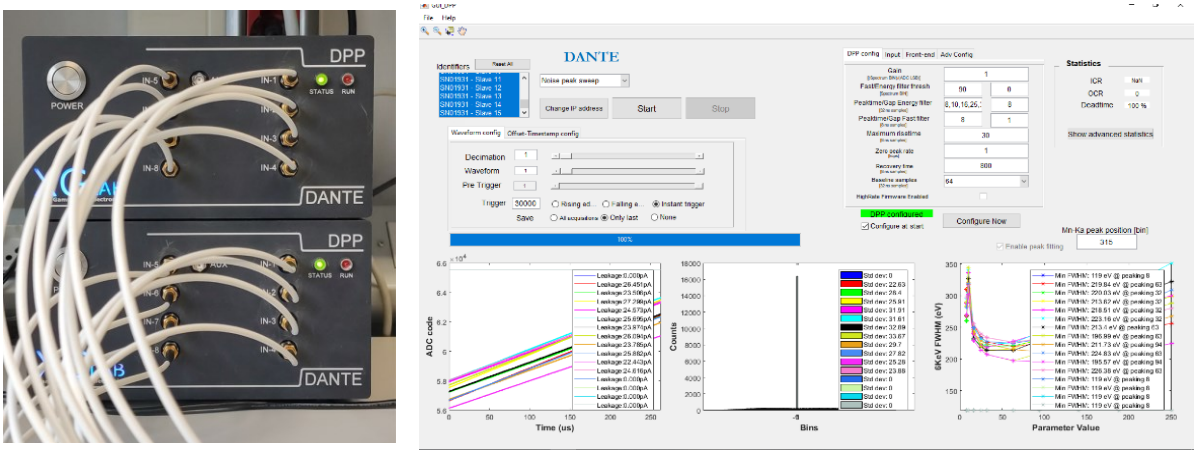


Figure 3.7: *Two different V_{IO} driving circuits.*

For the sake of compactness and to avoid too many external supplies, the DC-DC driving network is the preferred choice, but it may have worst performances compared to the external generator alternative. To compare the two options, a noise peak sweep has been performed using first the external generator driving circuit and then connecting the DC-DC one. This measurement has been performed at ambient temperature without the ^{55}Fe radioactive source, sampling the output ramps and the superimposed noise, and sweeping the time duration of the DAQ filter.

The DAQ used to acquire the noise features the DANTE processor [40], a commercial DPP (Digital Pulse Processor), implementing a trapezoidal shaping filter and able to acquire up to 8 channels through coaxial cables (see Figure 3.8).



(a) (b)

Figure 3.8: *Dante DPP. (a) Front view of the two DPPs. (b) Noise peak sweep GUI interface.*

The GUI interface, displayed in Figure 3.8(b), enables to have a real time view of both the leakage current ramps (on the left box), the standard deviation (central box) and the 5.898 keV FWHM vs peaking time (time duration of the filter). In particular, the first DPP channel is the one connected to the first output of the northern hemisphere, which is not attached to any pixel, so DANTE computes an intrinsic FWHM, just due to Fano factor "F" [41].

$$F = \frac{\sigma^2}{\mu} \tag{3.1}$$

With σ^2 the variance and μ the mean value of an observable event (in this case the number of generated charges). For a Poisson distribution, the factor is defined as $F = 1$, while in a semiconductor the factor results $F < 1$. This means that, compared to a purely statistical process ($F = 1$), the process inside semiconductors results in improved energy resolution. The Fano factor is dependent on temperature and on the type of material: for Si, at room temperature, $F = 0.115$ [42].

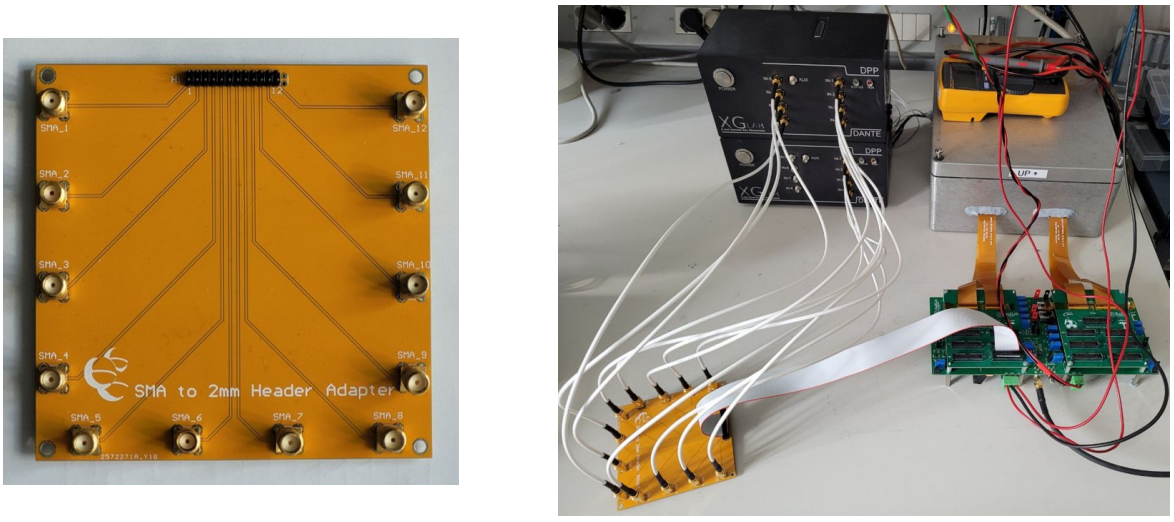
The FWHM contribution due to Fano factor can be expressed as in Eq. (3.2).

$$FWHM_{eV} = 2.355 \times \sqrt{\mathrm{wFE}_0} \tag{3.2}$$

In Si at room temperature, with w = 3.65 eV, E_0 = 5898 eV (Mn-Kα line) and F = 0.115, the intrinsic broadening in eV is $\mathrm{FWHM}_{eV} \approx 119$ eV at 5.898keV, known as the "Fano limit". This is a physical limit for any Si-based detector. Thus, for the first channel DANTE computes a $\mathrm{FWHM}_{eV} \approx 119$ eV. For all the other channels instead, the intrinsic

119 eV broadening is summed up quadratically to the broadening due to the filtered electronic noise, giving the total FWHM at 5.898 keV as a function of peaking time (computing the same value measured if a ^{55}Fe radioactive source is used).

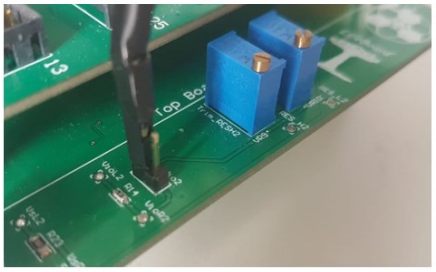
A 12-channel interconnection board (Figure 3.9) is used to adapt the 24-pin connector, present on the Lifeboard, to 12 SMA connectors, attached to the coaxial cables entering in the DPP. Since a single DPP have only 8 channels, two of them have been run in parallel to acquire all the 12 interconnection board outputs.

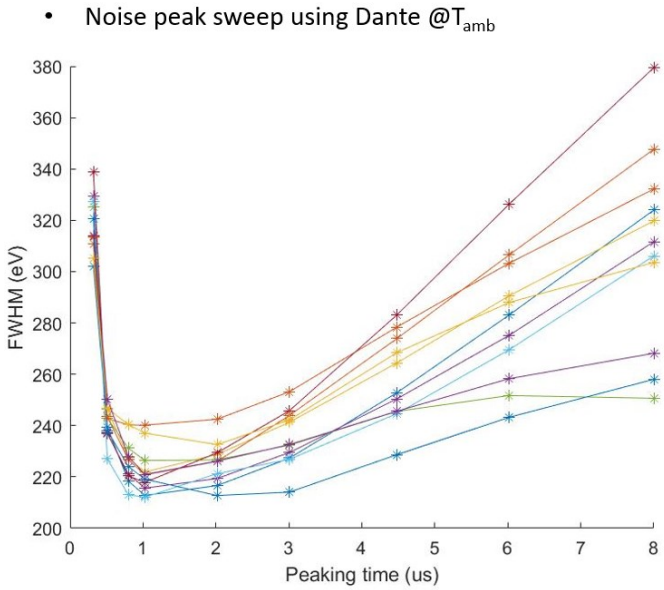


(a) (b)

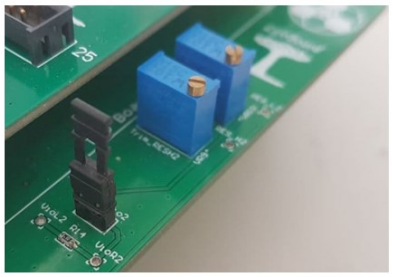
Figure 3.9: *(a) 12-channel interconnection board. (b) Full view of the measurement setup showing the interconnection board connected to the Lifeboard bias system and the DANTE DPP. The detector box is also present, connected to the bias system thorough the 4 FPCs.*

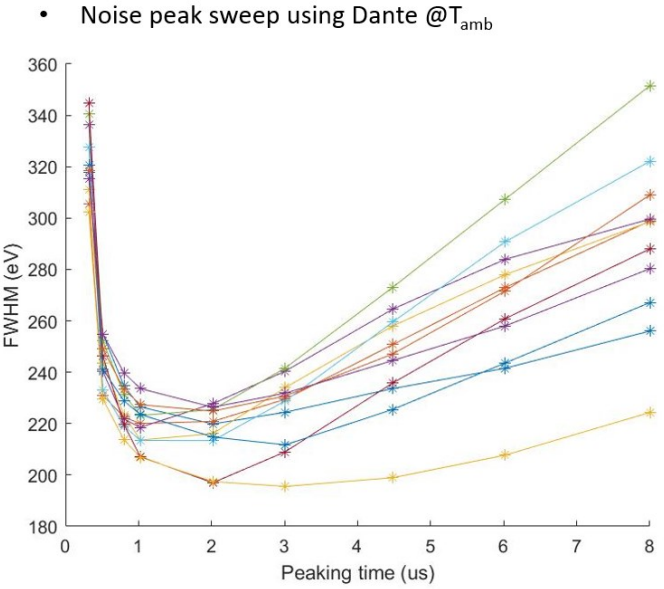
The experimental results, reported in Figure 3.10, show a similar dependence of the FWHM from the peaking time and, on average, comparable values. So, the DC-DC choice has no negative impact on the performances and can be used for the 166-pixel characterization.





(a)





(b)

Figure 3.10: *Experimental results using the external voltage regulator (a) or the DC-DC (b) driving circuit, acquired with DANTE DPP @T_{amb}. Each colour in the graph correspond to a different channel.*

3.2 Preliminary characterization measurements

3.2.1 Laboratory experimental setup

Figure 3.11 illustrates the experimental setup employed for the laboratory characterization of the 166-pixel planar module with a ^{55}Fe radioactive source.

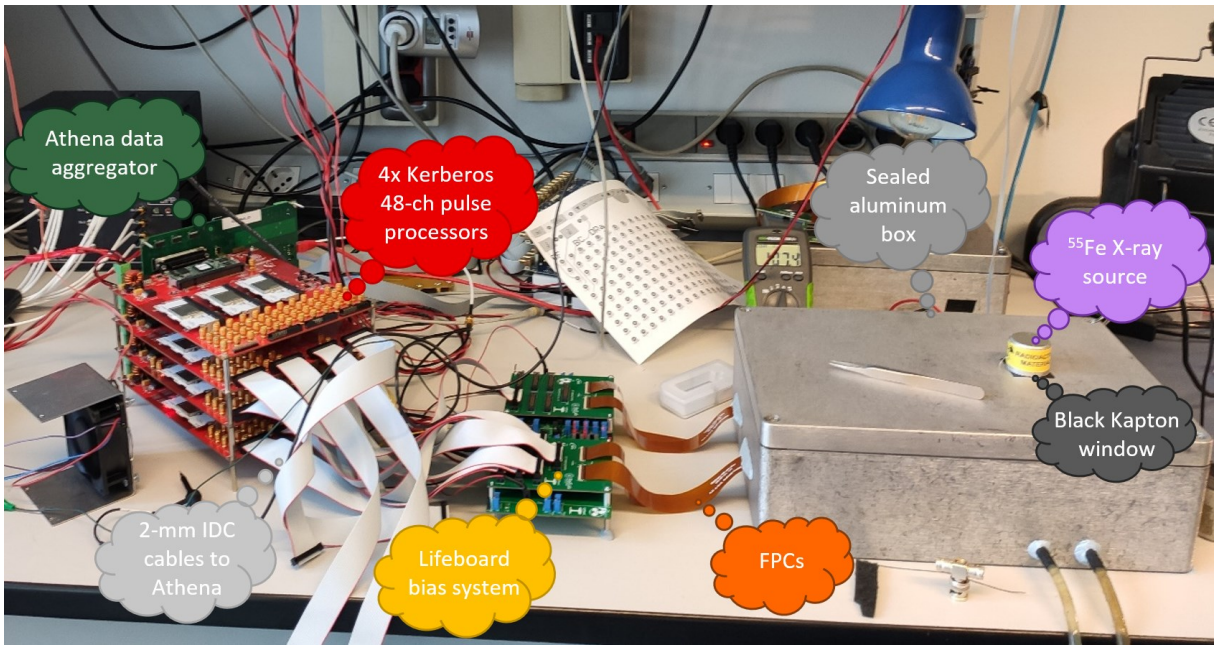
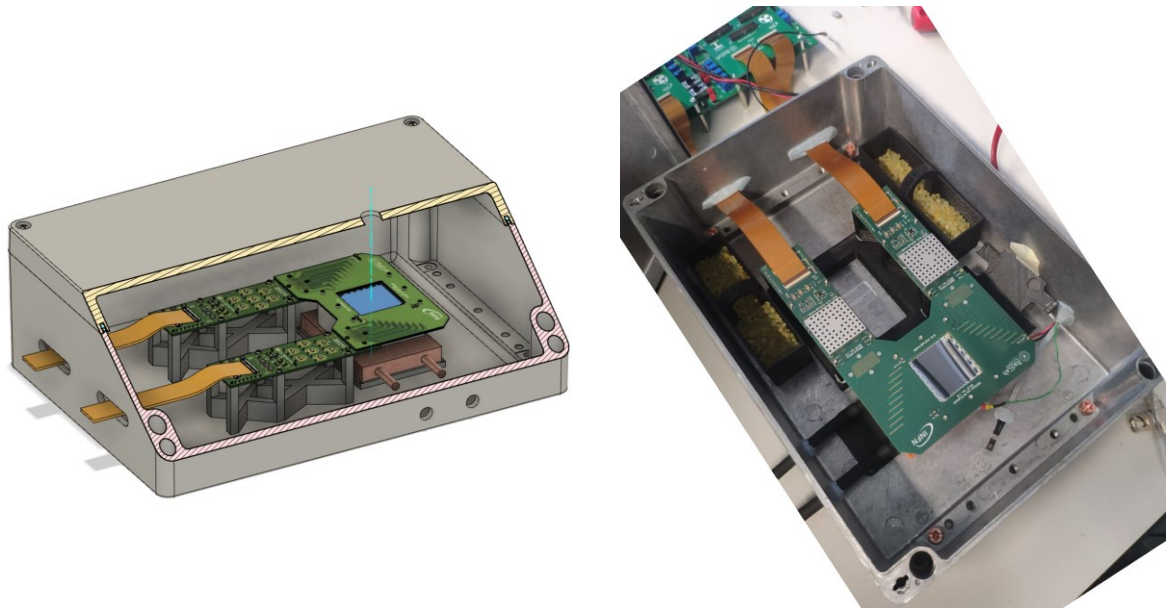


Figure 3.11: *Overview of the 166-pixel experimental setup.*

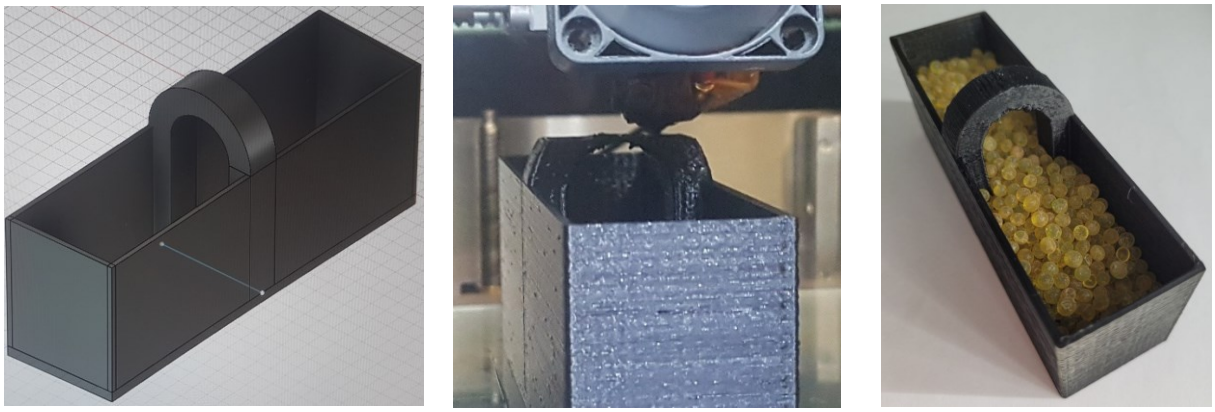
The detection module [30] is contained in a **sealed aluminum box** (see Figure 3.12). It features a liquid cooling solution based on a chiller refrigerating water (typically set at 5 °C) and circulating it in a heat exchanger to extract the heat produced by the Peltier device that cools the detector. The combination of chiller and Peltier cell can cool down the detector up to −40 °C. At this temperature, the parallel noise contribution, associated with the thermal leakage shot noise, becomes negligible. The sealing of the box is necessary for two reasons: to protect the inner environment from humidity, which is dangerous when the detector is cooled down due to the risk of water condensation and ice formation on the surfaces; and to shield the SDD from ambient light, that would strongly increase the current leakage. The relative humidity is kept below 10% fluxing dry nitrogen in the box or employing silica gel as a desiccant, put in a custom designed 3D printed case (Figure 3.13). The temperature and the humidity parameters are monitored with sensors to ensure the safe operation of the detector.

The ^{55}Fe X-ray source can reach the detector thanks to a black Kapton window opened on the top side of the box, that provides a good X-ray transmittance.



(a) (b)

Figure 3.12: *Aluminum box. (a) CAD 3D model seen along an oblique section showing the inside of the box. (b) Front view of the opened setup box.*



(a) (b) (c)

Figure 3.13: *(a) 3D model of the silica gel case. (b) Detail of the 3D printing of the case. (c) Silica gel put inside the case.*

As shown in Figure 3.12, attached to the detector board there are also the two 83-channel ASIC boards with 7 ETTORE chips each. The chips are covered by a

protection grid to protect them against accidental touch. The two ASIC boards are connected via four 100-pin FPC cables to the Lifeboard bias system.

The Lifeboard is then connected, through the 24-pin connectors, to the **Digital Acquisition (DAQ) system** (called "**Athena system**"), which is composed by four 48-channel Kerberos analog pulse processors [43] and a digital data aggregator (Athena itself) [44], as shown in Figure 3.14. The interconnections between the bias system and the DAQ use ribbon cables with 2-mm insulation-displacement contact (IDC) connectors. The Kerberos boards, equipped with three 16-channel SFERA ASICs [45] and a Xilinx Artix-7 FPGA, can operate in parallel to acquire up to 192 channels simultaneously thanks to the data aggregator. Athena features a Zynq UltraScale+ MPSoC (Multiprocessor System on Chip) running a Linux distribution that communicates to the four Xilinx Artix-7 FPGAs present on the Kerberos boards [46], on one side, and to a remote PC via the GbE (Gigabit Ethernet) link, on the other side. The data, coming from the four Kerberos boards, are collected by Athena which coordinates the inter-Kerberos triggering. Each time any channel registers and event, all Kerberos boards are read out concurrently, producing a 192-channel frame. Only 166-channels are used in this setup, so the remaining channels are not connected.

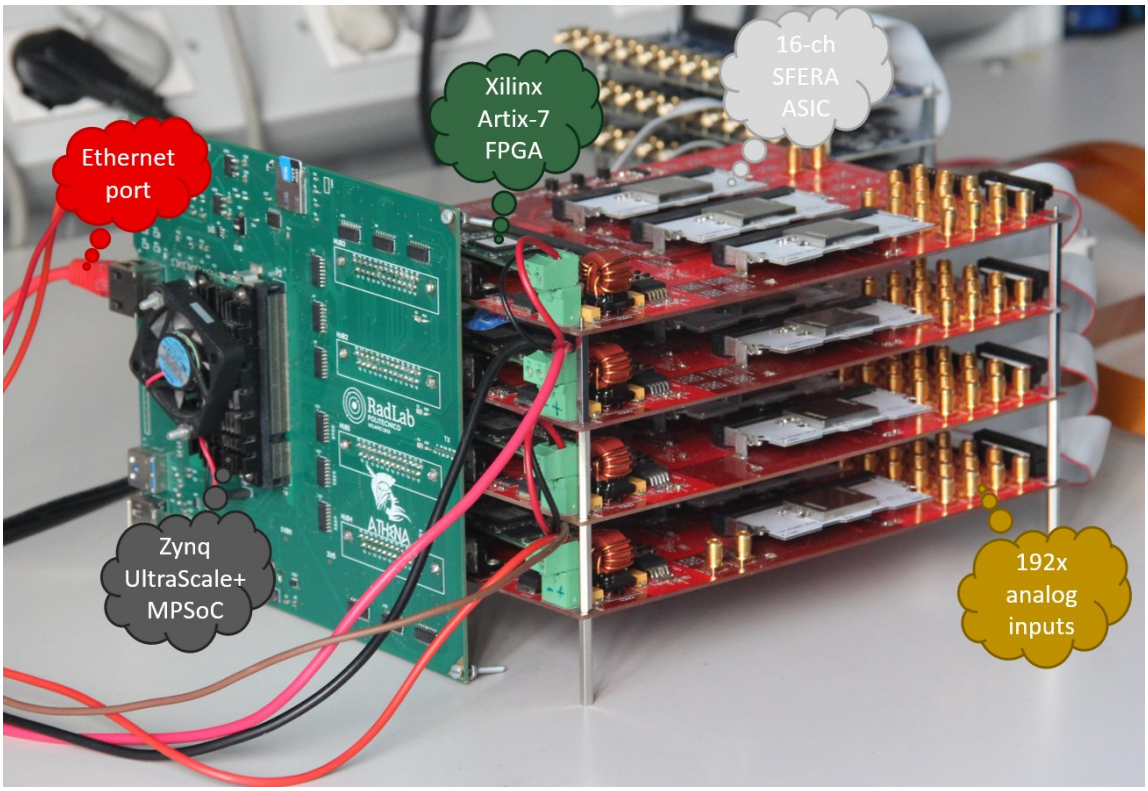


Figure 3.14: *Athena Digital Acquisition System.*

The Kerberos boards are supplied by an external voltage generator providing two independently regulated 6 V DC supplies, each of them feeding two Kerberos boards. The total power consumption is about 33.6 W (175 mW/ch), so the total current drawn from the generator is 5.6 A (2.8 A from each generator).

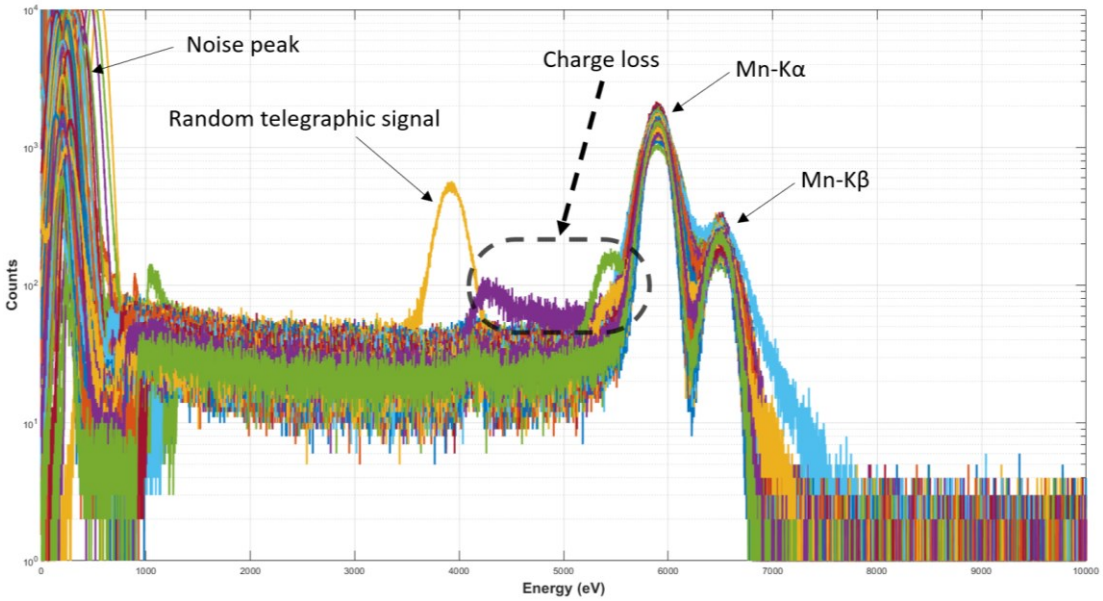
3.2.2 ^{55}Fe source measurements

The X-ray spectroscopy measurements have been performed using a ^{55}Fe radioactive source and setting the SFERA ASICs to their longest shaping time of 6 μs. The SDD detector has been cooled down to 0 °C by using the chiller refrigerating system combined with the Peltier cell. The bias parameters have been set as illustrated in Table 3.1 and the measurement lasted 300 s (acquisition time t_{ACQ} = 300 s).

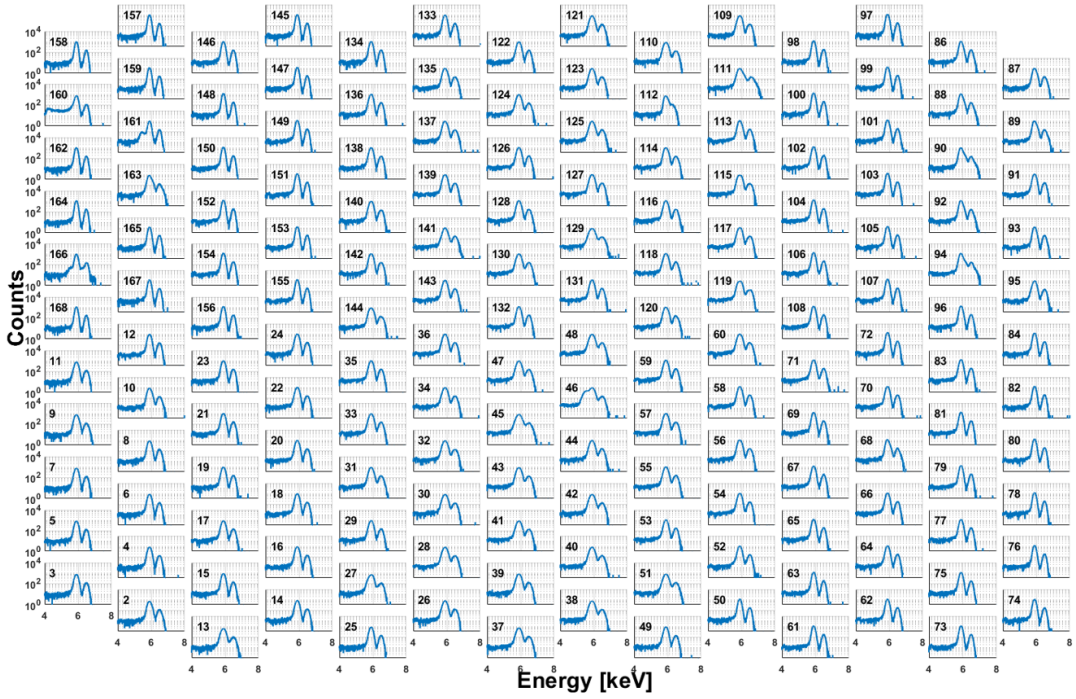
JFET and Detector Voltages-Currents	SDD 33.2 W.01 – B.06
I_{SSS}	≈125μA
V_D	8.0 V
V_{SSS}	-2.0 V
V_{RES_H}	3.8 V
V_{RES_L}	-10 V
V_{R1}	-8 V
V_{IGR}	-15 V
V_{RX}	-120 V
V_{BC}	-100 V
V_{BF}	-110 V

Table 3.1: *JFET and Detector bias parameters used for ^{55}Fe characterization measurements.*

Figure 3.15 shows the **166 spectra** acquired with the setup and calibrated using MATLAB software. In most of them the Mn-Kα and Mn-Kβ lines are well visible, while some pixels present distortions in the spectrum shape. These distortions are caused either by charge loss mechanisms in the device or by random telegraphic signals (RTS), as displayed in Figure 3.15(a).



(a)



(b)

Figure 3.15: *Calibrated 166-channel spectra. (a) Superimposed in a single plot with different colours. (b) Displayed singularly with a disposition that mimics the real pixel arrangement on the SDD matrix.*

Due to contaminations during the fabrication process, the detector has an unexpected not negligible drain line resistance. This made critical the correct biasing of all the pixels simultaneously, so a compromise has been made trying to minimize the pixels affected by spectrum distortions. The best results have been obtained using the parameters already shown in Table 3.1.

To test the homogeneity of the SSD matrix, the **event rate** of each pixel has been evaluated from the same set of data. The result is obtained by computing the integral of the counts with energy > 5 keV and dividing it by the acquisition time. The colourmap, shown in Figure 3.16, displays a continuous and regular gradient toward the source position, located over the blue region where the counts are higher. Thus, the system has homogeneous sensitivity in all pixels and DAQ channels.

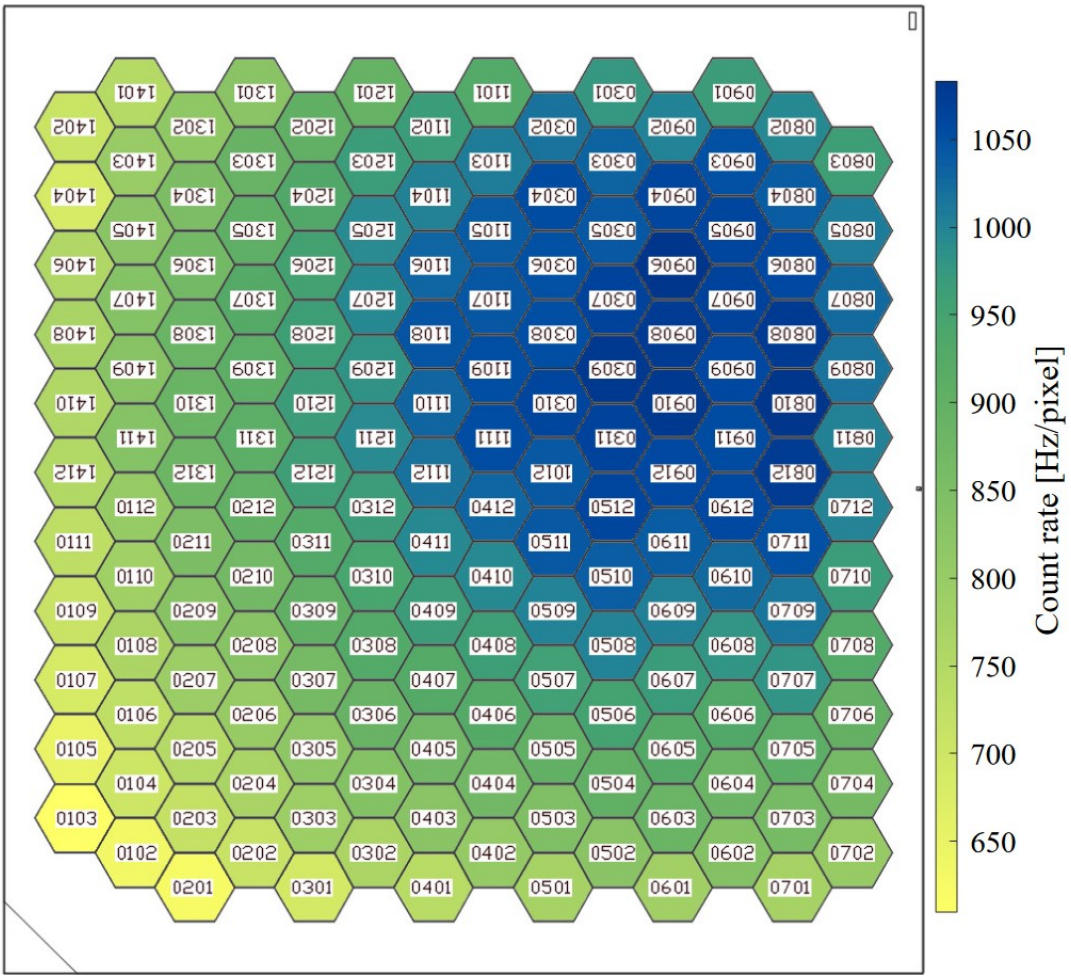


Figure 3.16: *Count rate colourmap.*

The next characterization step is the calculation of the **gain** of each channel and the **energy resolution**. Figure 3.17 shows the **model** used to fit the spectrum of each pixel, which includes:

- Two Gaussian functions, used to fit the Mn-Kα and Mn-Kβ lines, each one with centroid, height and sigma as free parameters.

- Two constant functions with a variable endpoint, to account for the background events, caused by incomplete charge collection and charge sharing between neighbouring pixels. Each of them has the height and the centroid as free parameters.

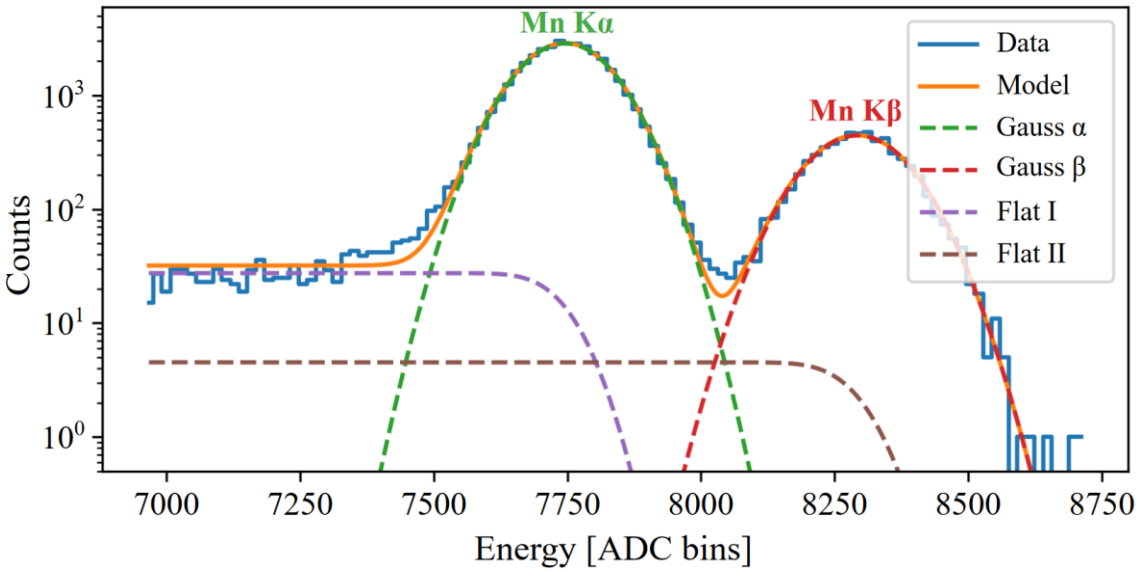


Figure 3.17: *Model exploited to fit the ^{55}Fe spectra. Courtesy of K. Urban.*

Figure 3.18 displays the gain of each channel, which is extremely uniform across the entire SDD matrix, with only a few outliers. Those few gain differences are both due to fabrication variations in the feedback capacitance C_{FB} and to small mismatches in the DAQ channels (e.g. ADC reference voltage or SFERA gain). To compute the gain, the energy difference between the Mn-Kα and the Mn-Kβ lines is divided by the distance, in ADC LSBs (or "bins"), between the centroids of the two X-ray lines fitted with the model previously described.

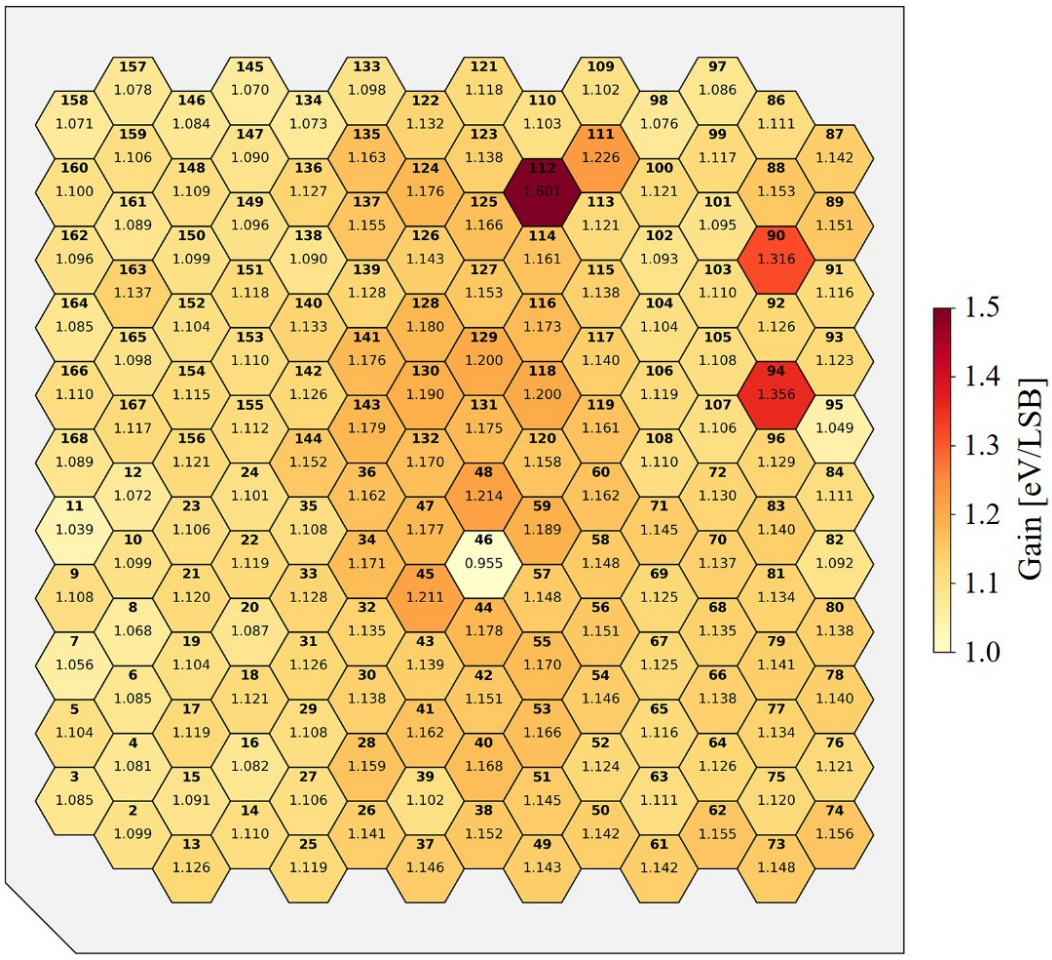


Figure 3.18: *Gain in eV over ADC LSB (least significant bit). Courtesy of K. Urban.*

The energy resolution ("FWHM") at the 5.898 keV Mn-Kα X-ray line of the 166-pixel detector is shown in Figure 3.19. On average, the FWHM is quite good, even if there're some outliers showing resolution higher than 400 eV. This result can be enhanced by cooling the detector below 0° C, finding a new optimal biasing of the detector. Nevertheless, the main issue, as already mentioned, is the resistance in the drain voltage lines that affects the pixel columns in the central region of the detector since the drain contacts are placed on the corners, as illustrated in Figure 3.20. This situation cannot be improved significantly without a new SDD production able to reduce the drain lines resistance.

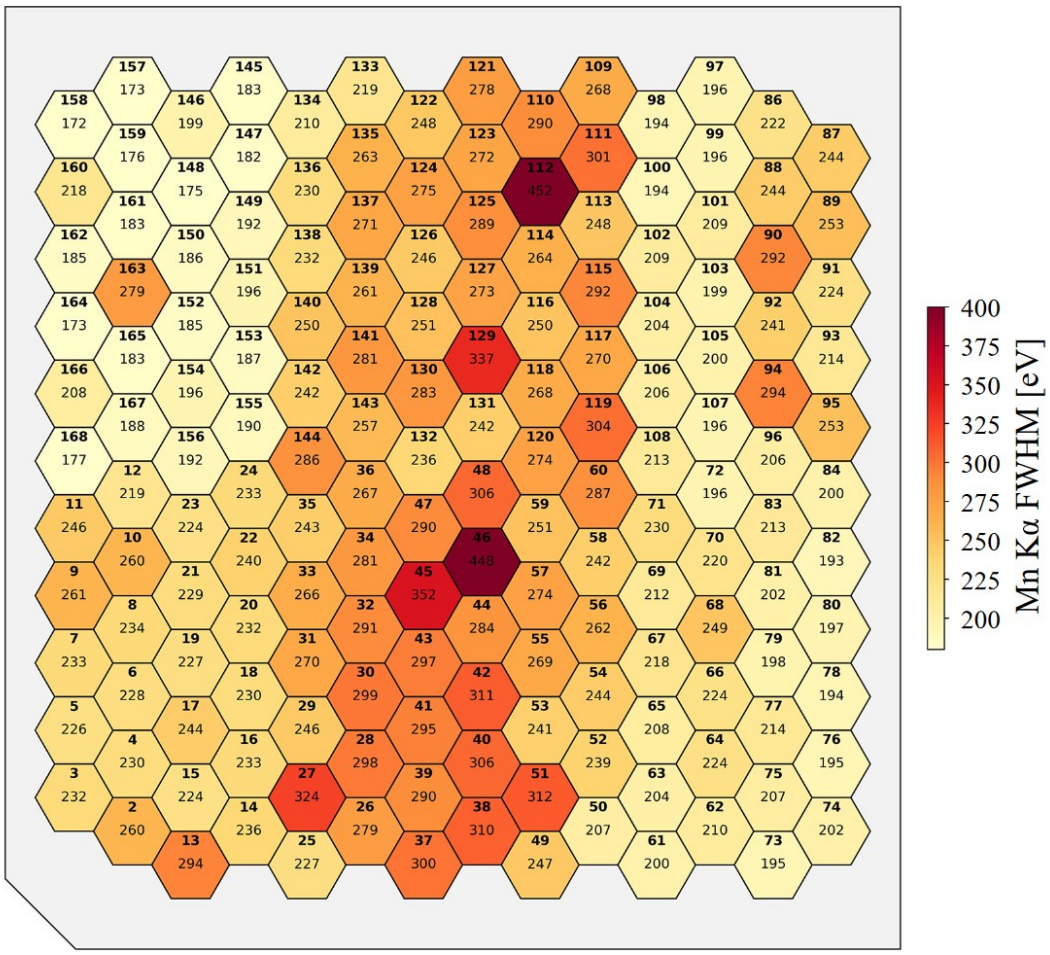


Figure 3.19: *Energy resolution (FWHM) in eV at the Mn-Kα X-ray line. Courtesy of K. Urban.*

The 166-pixel detector of the new SDD production is going to be tested by our colleagues in MPP ("Max Planck Institute For Physics"). In our preliminary and forerunning characterization instead, to mitigate the problem, the 166-pixel detector has been operated with reduced JFET bias current (~125 μA). This made possible to improve the energy response and the FWHM homogeneity, thus obtaining good results and acquiring the know how to obtain even better results with the new production. Another factor of improvement is the cooling of the detector. Given its large size, the temperature in the planar setup has been limited to 0 °C, since the mechanical structure of the SDD matrix is subjected to stress due to the mismatches in the thermal expansion coefficients of the PCB material and the silicon. In the final 3D configuration, the detector will be glued to a CeSiC block, which has a thermal expansion coefficient very similar to the one of the SDD detector (2.3×10^{-6} K^{-1} and 2.6×10^{-6} K^{-1}, respectively), allowing to further decrease the temperature without creating stress forces on the mechanical structure.

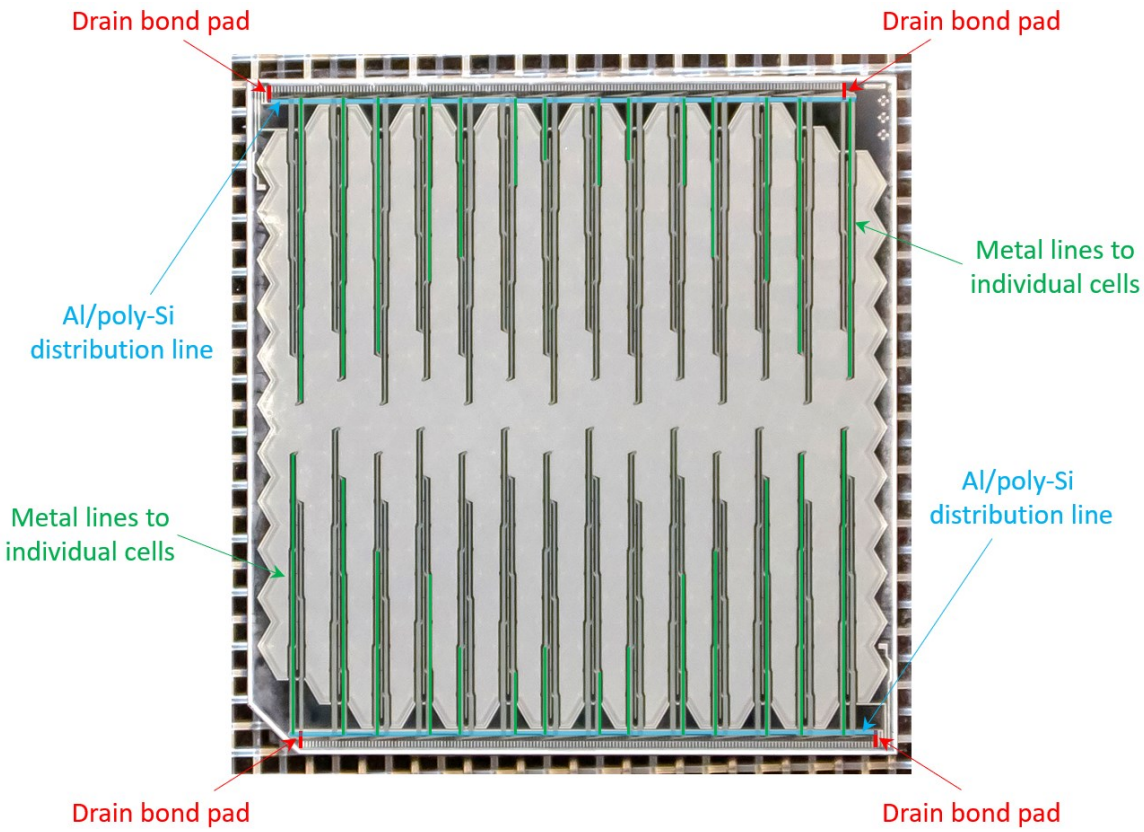


Figure 3.20: *166-pixel detector layout. The drain voltage is set through the bond pads (contacts), but the voltage drop across the resistance of the poly-Si lines makes the central columns pixels working with a suboptimal drain bias voltage.*

3.3 Long-time stability measurement

Another important parameter of the system is the stability over a long time measurement. The previous 300 s measurements give an overview of the system performances, but they may vary over time giving different results every time a test is performed. Also the temperature variation over time may change the system performances. Therefore, a long time measurement, also monitoring the temperature of the setup (in particular of the ASIC board and of Kerberos), is required to have a clearer understanding of the system behaviour over time and temperature variations.

This section presents a 53-hour measurement, performed by interleaving 300 s (5 minutes) measurements and 55 minutes of stops (stand-by operation) for a total of 53 data acquisitions, as shown in Figure 3.21. This repeated sequence can be programmed thanks to a functionality present on the Athena GUI, in which both the measurement duration, the stop duration and the number of them can be freely set.

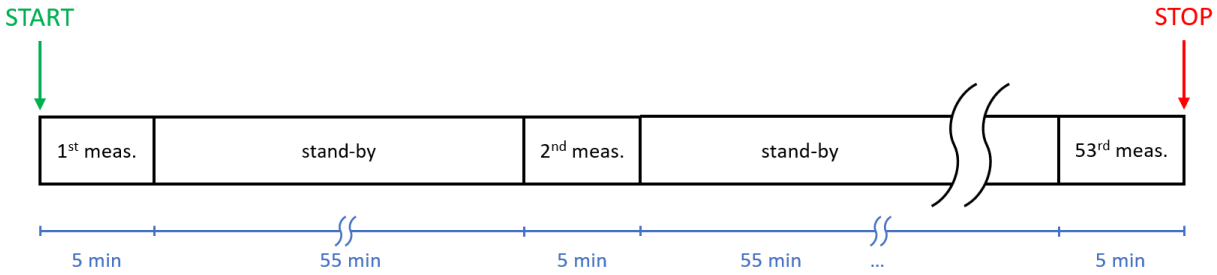


Figure 3.21: *Long time measurement timeline. 5 minutes measurements and 55 minutes stops (stand-by) are alternated until reaching the 53rd measurement, overall performing 52 hours and 5 minutes of measurement.*

3.3.1 Stability measurement setup

Figure 3.22 illustrates the setup employed for the long time stability measurement. The sealed aluminum box, the Lifeboard bias system and the Athena DAQ system are the same already described in Section 3.2.1. The two additional blocks in the 53 h measurement setup are: the *Texas Instruments Analog System Lab Kit (TI ASLK) Pro* [47] and the *Moku:Go M1 data logger* [48].

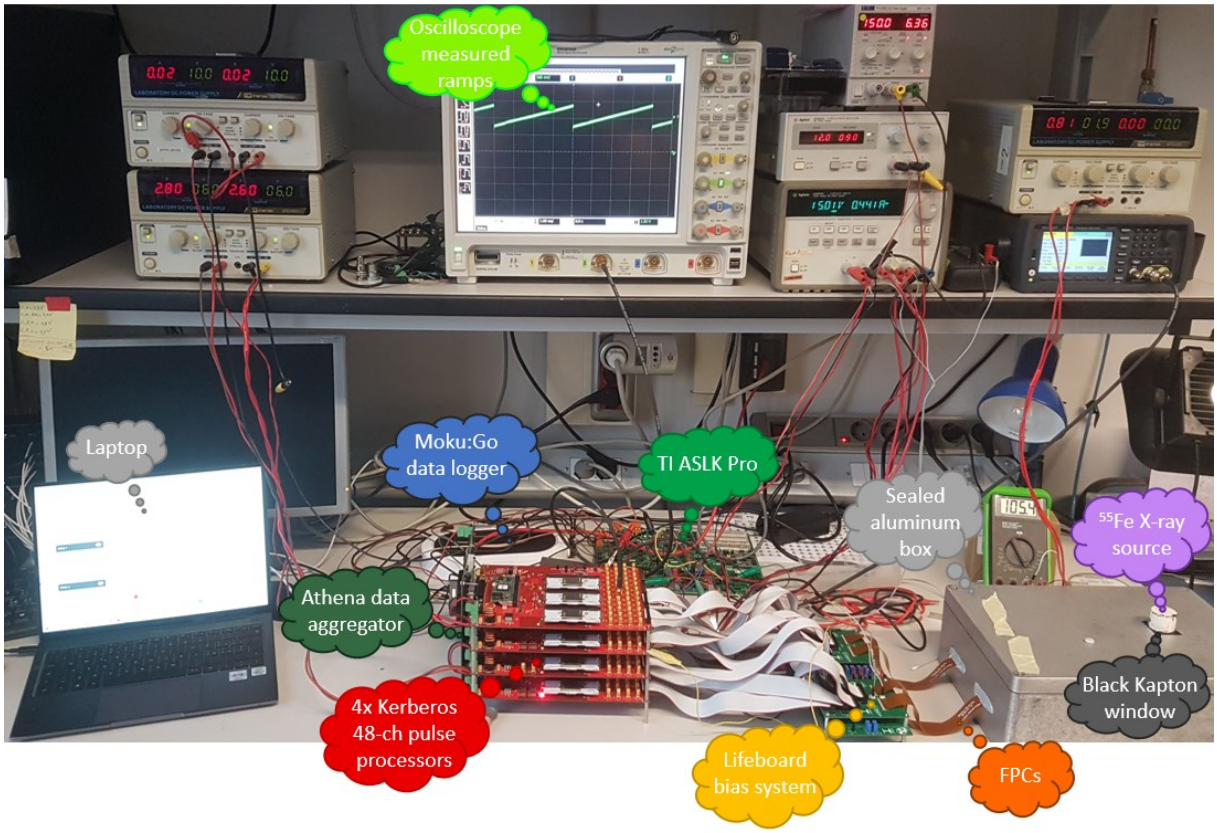


Figure 3.22: *Overview of the long-time stability measurement setup.*

The **Texas Instruments Analog System Lab Kit (TI ASLK) Pro** is a board featuring multiple basic analog components with already drawn interconnections and customizable networks (see Figure 3.23). The component of our interest is the TL082 OP-Amp in the "OPAMP TYPE II FULL" section used to build a read out circuit needed to amplify the PT1000 signal that is proportional to the temperature. Specifically, there are 3 different PT1000 temperature sensors in the setup: two of them are present in the ASIC boards and they're accessed by two test points on the Lifeboard, as shown in Figure 3.24(a); the third one has been added to the setup and soldered on a wire placed near to the Kerberos boards. The PT1000 temperature sensor is basically a platinum temperature varying resistance, whose value is 1000 Ω at 0 °C with an increment of 3.9 Ω/°C. Its biasing network is shown in Figure 3.24(b). By choosing a supply voltage V_{DD}=12 V and a series resistance R=39 kΩ, the corresponding current flowing in the biasing network at 0 °C is:

$$I_{@0°C} = \frac{V_{DD}}{(\mathrm{R} + \mathrm{PT1000}_{@0\,°C})} = \frac{12\ \mathrm{V}}{39\ \mathrm{k\Omega}\ +\ 1000\ \Omega} = 300\ \mu\mathrm{A} \tag{3.3}$$

The voltage across the PT1000 sensor (V_{OUT}) function of the temperature T is:

$$V_{OUT} = \frac{V_{DD} \times (PT1000_{@0\,°C} + 3.9\,\Omega \times T)}{R + (PT1000_{@0\,°C} + 3.9\,\Omega \times T)} \tag{3.4}$$

Thus, the voltage variation given by a temperature variation (ΔT) of 1 °C results:

$$\Delta V_{OUTmin} = \frac{V_{DD} \times (3.9\,\Omega \times \Delta T)}{R + (3.9\,\Omega \times \Delta T)} = \frac{12\,V \times (3.9\,\Omega \times 1\,°C)}{39\,k\Omega + (3.9\,\Omega \times 1\,°C)} \approx 1.2\,mV \tag{3.5}$$

This variation is too small, since the Moku:Go data logger features a 12-bit ADC and a 10 V peak-to-peak input range, giving an LSB=2.44 mV, so higher than the minimum voltage variation (as explained in the following discussion). In order to have a higher precision when measuring the temperature variation, an amplification stage is needed so that, at its output, the ΔV_{OUTmin} can span over more than one LSB.

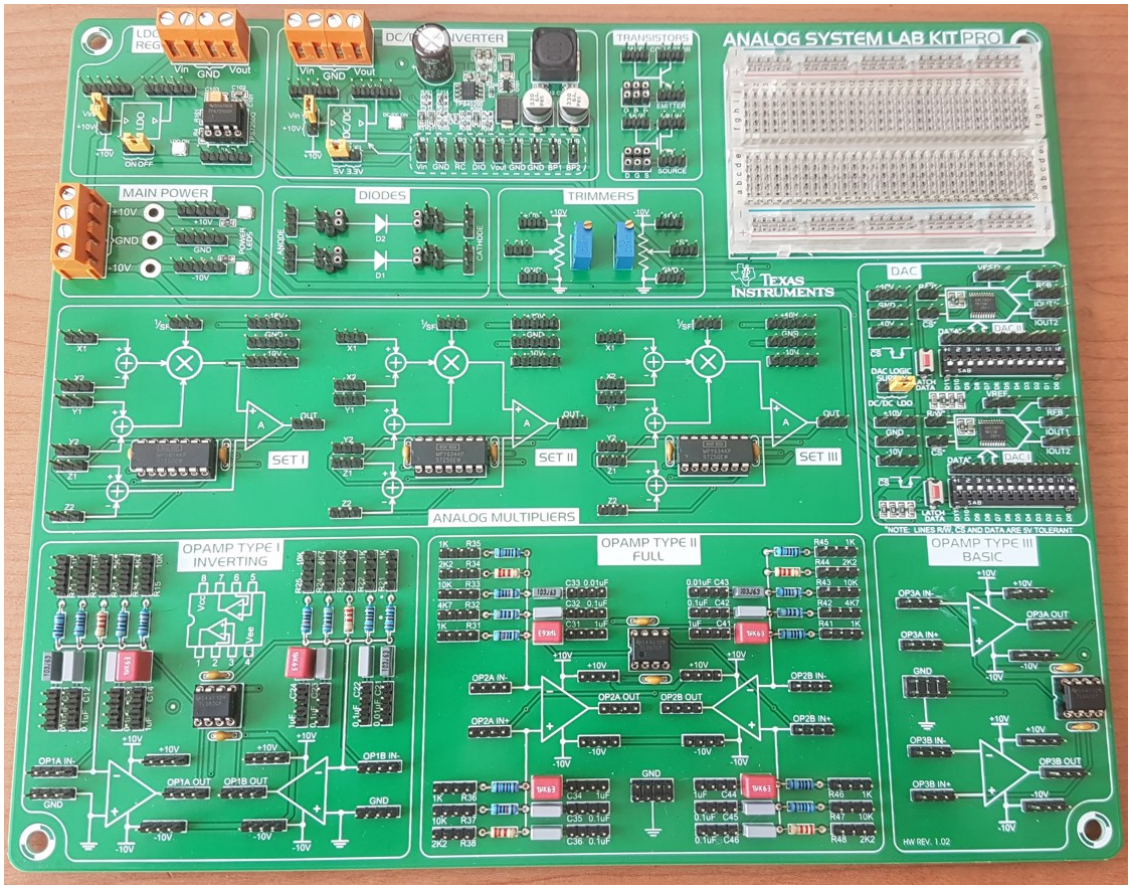
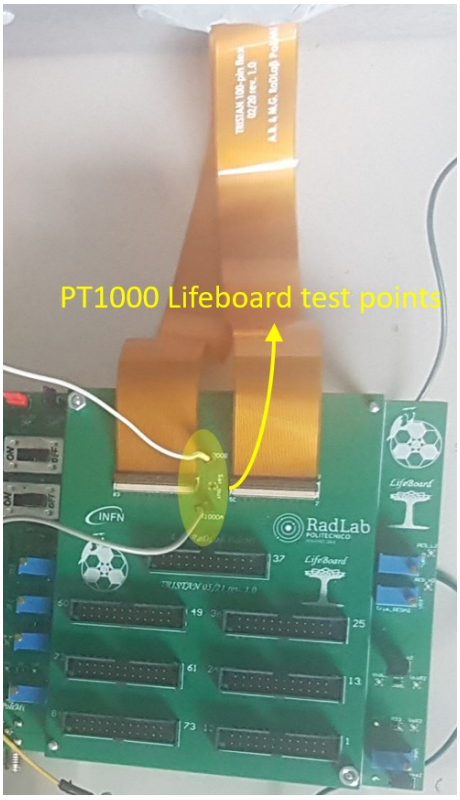
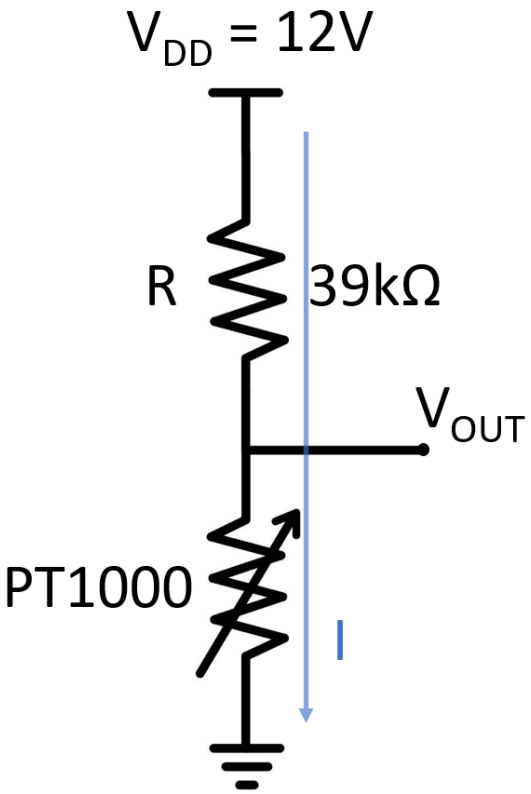


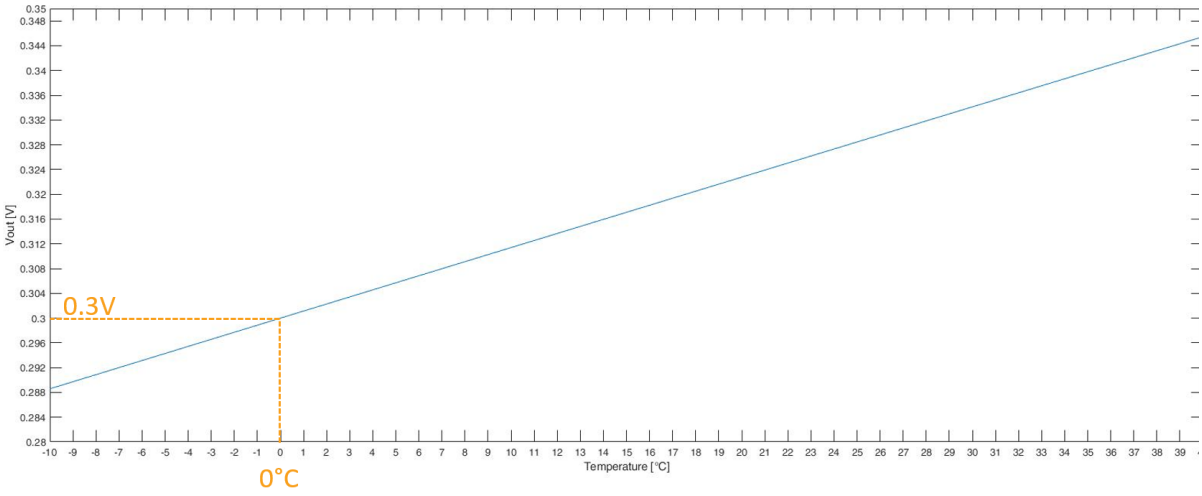
Figure 3.23: *Texas Instruments Analog System Lab Kit Pro front view.*



(a)



(b)



(c)

Figure 3.24: *(a) PT1000 Lifeboard test points. (b) PT1000 biasing network. (c) VOUT vs temperature plot.*

As mentioned before, the readout circuit features a TL082 OP-Amp [49]: an IC made by two integrated amplifiers, that can be used to build two non-inverting configurations to amplify the voltage signals across the two PT1000 temperature sensors (the one placed near the Kerberos board and one of the two PT1000 present on the ASIC boards). Figure 3.25 illustrates the readout circuit, which is supplied by the V_{DD} = 12 V provided by one of the two Moku:Go outputs, while the other one is used to give the reference ground to the network.

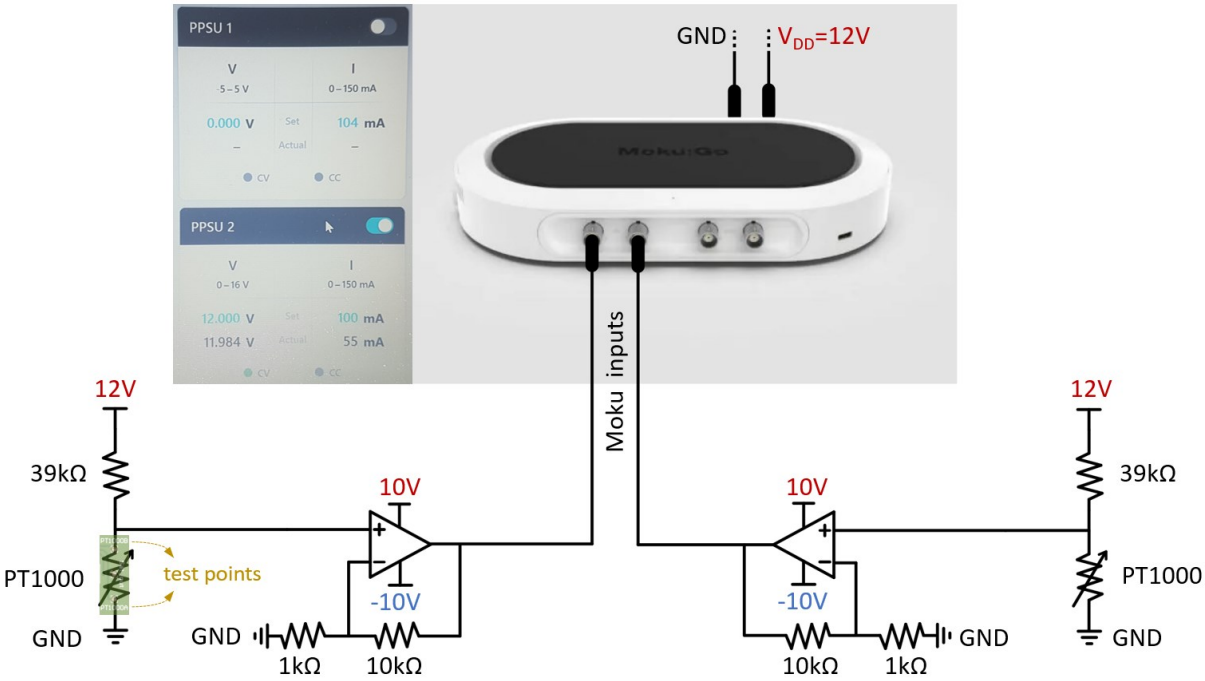


Figure 3.25: *Schematic view of the readout circuit used to amplify the PT1000 signal. On the top side, the Moku:Go M1 case and the GUI programmable power supplies interface are shown.*

The two non-inverting configurations provide a voltage gain of:

$$G = 1 + \frac{R_F}{R_G} = 1 + \frac{10\ \text{k}\Omega}{1\ \text{k}\Omega} = 11 \tag{3.6}$$

Where the R_F =10 kΩ are the feedback resistances, while the R_G =1 kΩ are the resistances toward ground. The outputs of the two OP-Amps are the two inputs of the Moku:Go data logger. Thanks to this amplification, the minimum voltage variation at the input of Moku, given by a temperature variation (ΔT) of 1 °C, results:

$$\Delta V_{OUTmin} = \mathrm{G} \times \frac{\mathrm{V}_{DD} \times (3.9\ \Omega \times \Delta\mathrm{T})}{\mathrm{R} + (3.9\ \Omega \times \Delta\mathrm{T})} = 11 \times \frac{12\ \mathrm{V} \times (3.9\ \Omega \times 1\ °\mathrm{C})}{39\ \mathrm{k}\Omega + (3.9\ \Omega \times 1\ °\mathrm{C})} \approx\ 13.2\ \mathrm{mV} \qquad (3.7)$$

Which is enough large, compared to the LSB, to have an accurate monitoring of the temperature during the stability measurement, as illustrated by the V_{OUT} vs T plot of Figure 3.26, where V_{OUT} now is the amplified voltage at the output of the two operational amplifiers. These two amplifiers outputs are the input signals of Moku.

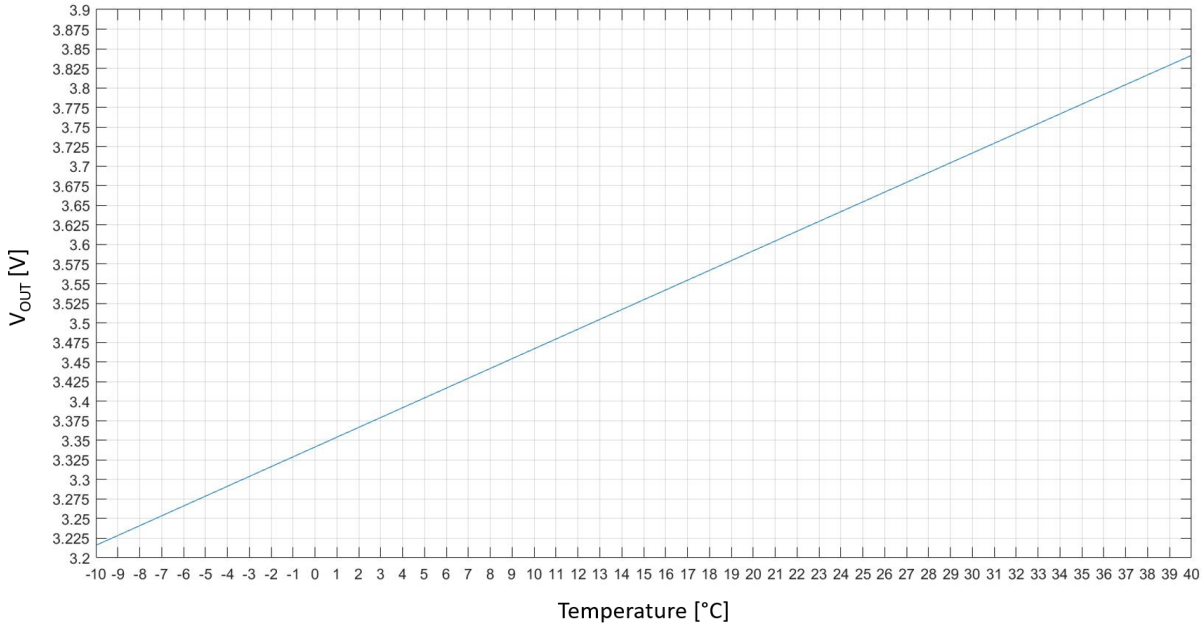


Figure 3.26: *Amplified V_{OUT} vs T plot.*

The **Moku:Go M1** [48] is a multi-instrument laboratory tool programmable using a custom user interface provided by the manufacturer and running on Windows or MacOS environment. The connection to the computer is made through a USB Type-C port or using WiFi Hotspot connection. The Moku:Go (M1 version) features two programmable output power supplies: a -5÷5 V and a 0÷16 V, providing a current up to 150 mA, in constant voltage or constant current mode with auto overvoltage and overcurrent protection (see fig Figure 3.25). In particular, in the long time measurement setup, the 0÷16 V output supply is used to provide the 12 V to the PT1000 readout circuit.

The Moku:Go also have two 12-bit analog input channels with 1 MΩ input impedance, AC or DC coupled. In particular, to monitor the actual temperature values, the outputs of the two Op-Amps have been DC coupled to the two Moku:Go inputs. The input range can be set to 10 V or 50 V peak-to-peak (±5 V or ±25 V respectively). To have higher resolution, the 10 V option has been preferred, thus giving an LSB value of:

$$LSB = \frac{Vpp}{2^n} = \frac{10\ \mathrm{V}}{2^{12}} = 2.44\ \mathrm{mV} \tag{3.8}$$

Where *Vpp* is the peak-to-peak input voltage range and *n* is the number of bits of the ADC.

The ±5 V input range is satisfactory since, as already mentioned, it gives an enough small LSB and also the system doesn't run the risk of overcoming the input range, because, if the temperature varies in the -10÷40 °C range, the amplified V_{OUT} ranges within the 3.20÷3.85 V interval, as illustrated in the plot of Figure 3.26. More in detail, this plot considers also the offset (V_{OFFSET} = 41.5 mV) measured at the input of Moku:Go when the 12 V supply is switched off. Thus, the final V_{OUT} equation is:

$$V_{OUT} = \mathrm{G} \times \frac{\mathrm{V}_{DD} \times (\mathrm{PT1000}_{@0\,^\circ C} + 3.9\ \Omega \times \mathrm{T})}{\mathrm{R} + (\mathrm{PT1000}_{@0\,^\circ C} + 3.9\ \Omega \times \mathrm{T})} + \mathrm{V}_{OFFSET} \tag{3.9}$$

The temperature monitoring has been performed by selecting the "Data Logger" function from the GUI. This functionality enables to log data directly to the Moku:Go internal memory with a sampling rate configurable up to 1 MSa/s if only one channel is used, while up to 500 kSa/s if both the inputs are enabled. Since the temperature variations are slow in time and not to have a too large output file, the minimum sampling rate, corresponding to 10 samples/s, has been chosen for the measurement. Another functionality of the data logger is the possibility to program the duration of the measurement, that, for the stability measurement, has been set to 52 hours and 5 minutes, to perform all the 53 measurements (of 5 minutes each, interleaved by the 55 minutes stops).

At the end of the measurement, the binary log file has been converted into .csv format by a built-in conversion tool, transferred to the PC and imported into MATLAB to analyse the temperature variations alongside the 166-pixels ^{55}Fe measurements, as discussed in the next section.

Figure 3.27 illustrates the temperature monitoring (on the Moku:Go GUI running on the laptop) together with the X-ray spectroscopy measurements (on the tablet screen, remotely connected with another PC running the Athena GUI).

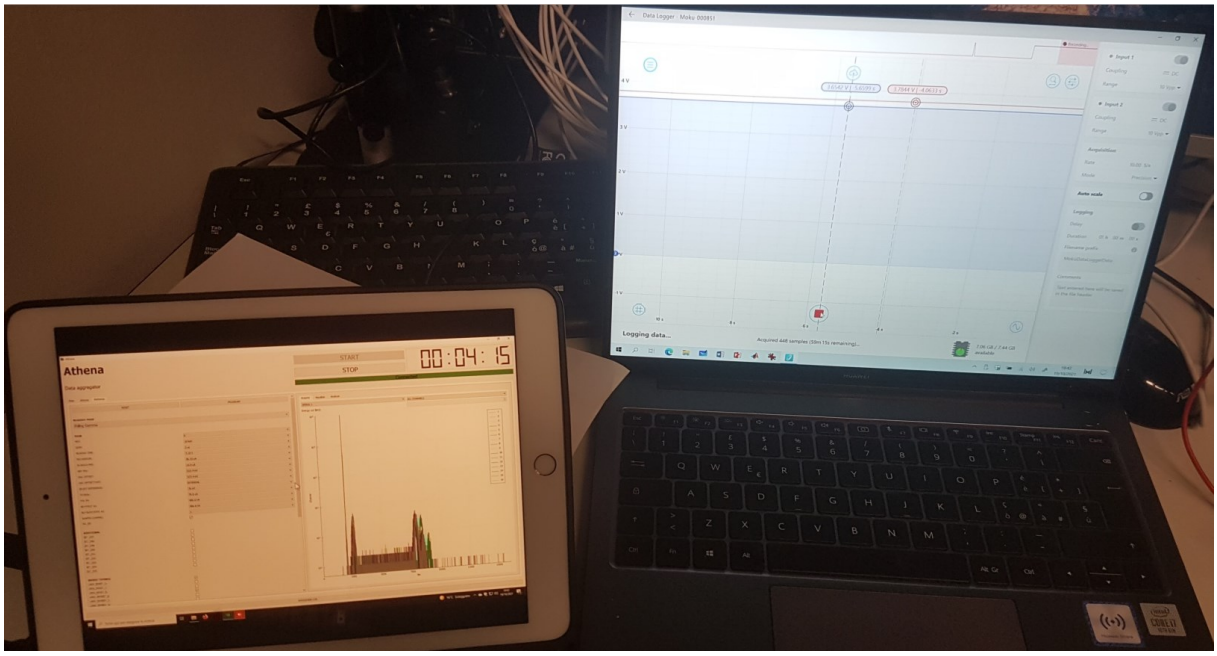


Figure 3.27: *On the left screen: live spectra view on the Athena GUI during one of the ^{55}Fe spectroscopy measurements. On the right screen: live temperature monitoring on the Moku:Go GUI.*

3.3.2 Experimental results

The experimental results, obtained by performing a sequence of 53 X-ray spectroscopy measurements using ^{55}Fe radioactive source and lasting 5 minutes each, monitoring also the temperature using the Moku data logger, are shown in this section.

Before that, an important observation has to be made. Since many data have been acquired, a **simplified model** has been employed to perform the fitting of the 166×53 spectra (see Figure 3.28). It includes only the two gaussian functions, used to fit the Mn-Kα and Mn-Kβ lines, and then, in the MATLAB script, the following spectra controls are introduced:

- Acceptable range of computed FWHM, discharging the spectra with not physical values.
- Check on the positions of the peaks, discharging the wrong spectra with only one peak (or none) correctly fit.
- Discharge the spectra having a wrong Kα vs Kβ relative intensity.

These verifications are necessary to compute, for each of the 53 acquisitions, a reliable FWHM and gain (G) averaged over all the correctly fitted spectra. On the contrary, if all the spectra are considered and there are some outliers, they would produce a corrupted value for the averaged FWHM and gain.

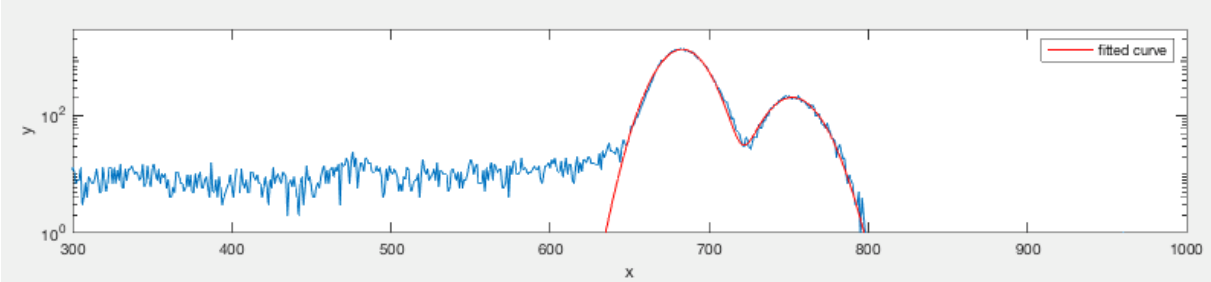


Figure 3.28: *Simplified fitting model for the long time stability measurement.*

As for the previous characterization measurements, the detector has been cooled down to 0 °C using the combination of the Peltier cell and the chiller refrigerating system.

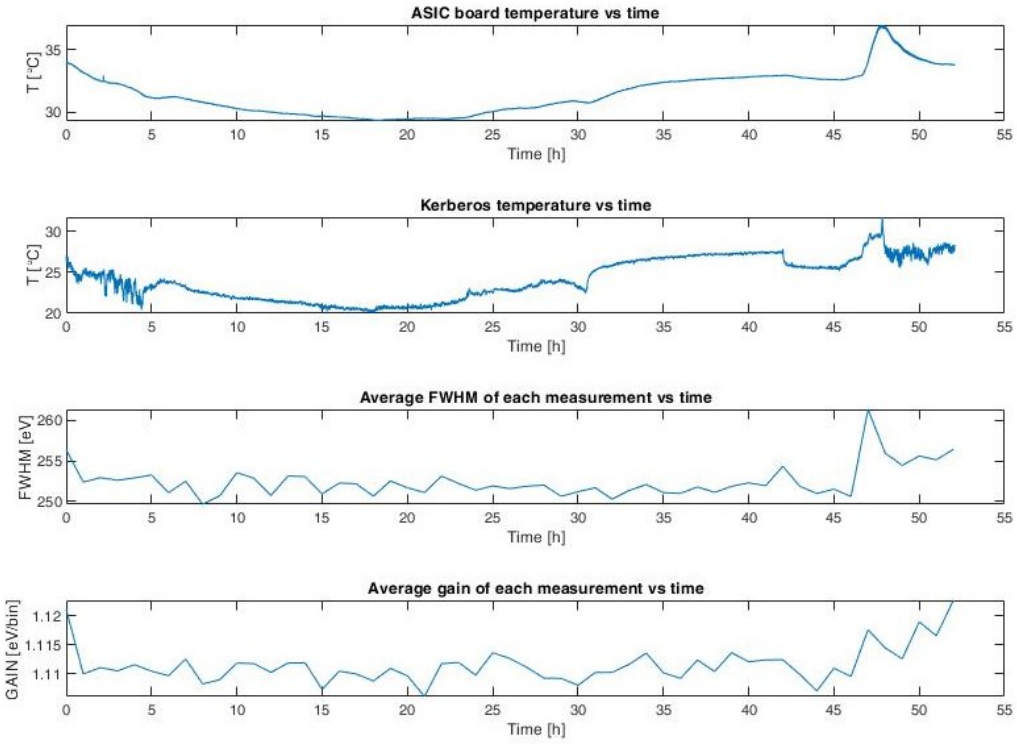


Figure 3.29: *Time plots of: (a) ASIC board temperature; (b) Kerberos temperature; (c) Average FWHM of the measurement; (d) Average gain of the measurement.*

Figure 3.29 shows the time plots of the data acquired with the setup:

- The first plot represents the ASIC board temperature variation over time. It spans over the 29÷37 °C range, decreasing during the first night, while keeping quite constant in the following hours. A temperature peak is observed at the end, due to the fact that the sun was shining directly on the setup. These variations are possible since the detector is directly placed over the Peltier cell and kept to 0°C, while the ASIC board is connected to the detector through the detector board PCB, thus having a limited thermal conductance.

- The second plot shows the Kerberos boards temperature variation over time. It spans over the 20÷30 °C range, following the ambient temperature variations as the previous plot, but with more fast variations since there is no a cooling system that keeps stable the ambient temperature like inside the sealed box.

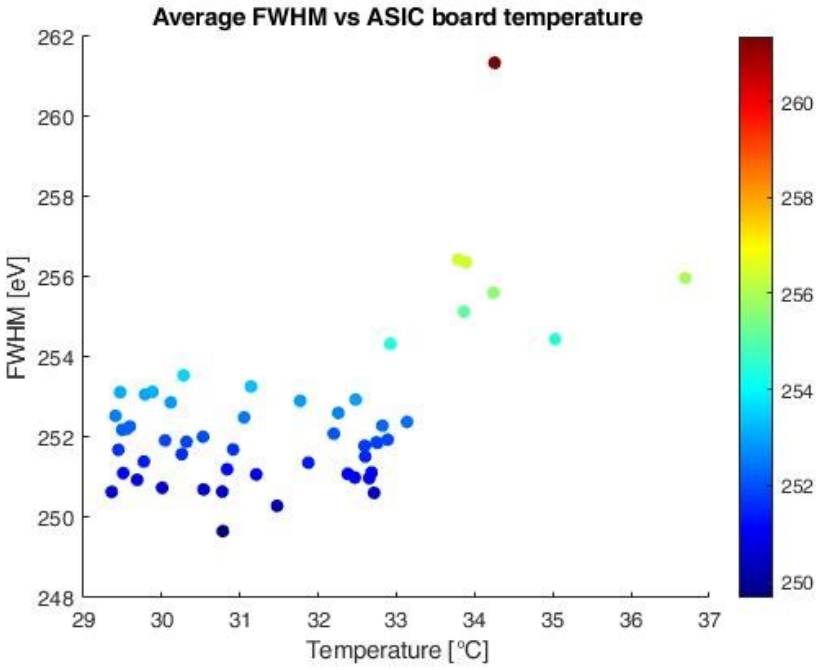
- The third plot displays the average FWHM of each measurement as a function of time. It ranges in the 250÷260 eV and, except in correspondence of the temperature peak, it is quite stable over time. The values are similar to the average FWHM measured in the preliminary characterization measurements shown in the previous section.

- The last plot shows the average gain of each measurement as a function of time. It ranges in the 1.11÷1.12 eV/bin, showing a good stability and values in agreement with the preliminary characterization measurements.

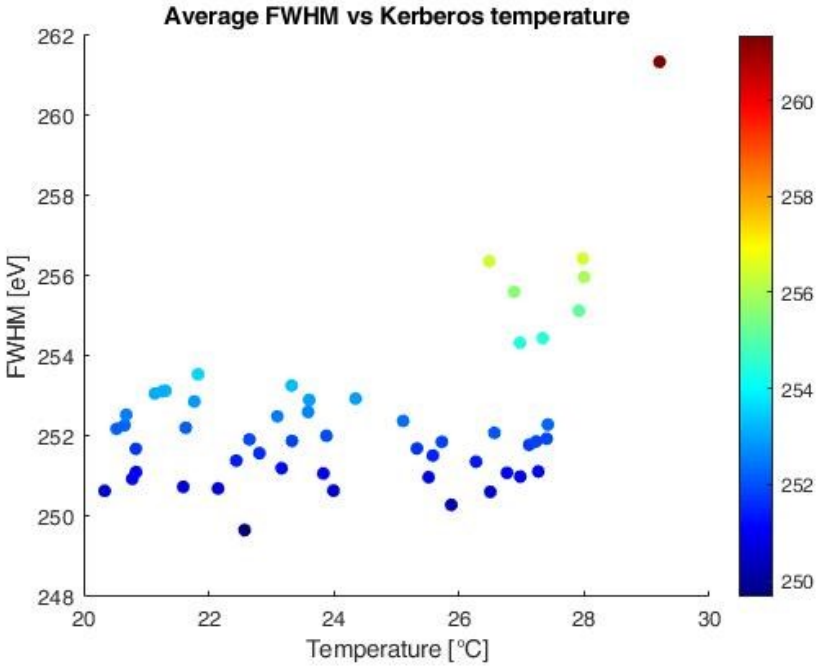
To displays the FWHM and the *G* variations as a function of the temperature, the average ASIC board temperature and the average Kerberos temperature, during each 5 minutes measurement, have been computed from the temperature data.

Figure 3.30(a) shows the average FWHM of each measurement as a function of the ASIC board temperature (averaged as described before). The FWHM appears almost independent on the temperature up to about 33 °C; after this value it shows a small increase, but only few measurements were acquired with this higher temperature, so there are too small statistics. The majority of the measurements features an average temperature lower than 33 °C.

A similar situation occurs in Figure 3.30(b), showing the average FWHM of each measurement as a function of the temperature near to the Kerberos boards. The FWHM is approximately independent on the temperature up to about 27 °C; after this value it increases slightly, but there are only few measurements with an average temperature higher than that value.



(a)



(b)

Figure 3.30: *Plot of the average FWHM as a function of (a) the ASIC board temperature, (b) the Kerberos boards temperature.*

The average FWHM, over all the 53 acquisitions, is about 252 eV.

Figure 3.31(a) displays the average gain of each measurement as a function of the ASIC board temperature. The average gain increases with temperature. Indeed, fitting the scatter plot with a line that minimizes the square distances, it is possible to compute an increase of:

$$\frac{\Delta G}{\Delta T} = 9.9 \times 10^{-4} \ \frac{eV}{bin \times °C} \tag{3.10}$$

It corresponds to a peak shift of 0.99‰ for each degree of temperature increase. Thus, for a variation of 1 °C, the measured value of the Mn-Kα line will change of about:

$$\Delta E = 9.9 \times 10^{-4} \ \frac{eV}{bin} \times ADC_{K\alpha bin} \tag{3.11}$$

Where $ADC_{K\alpha bin}$ is the bin of the Kerberos ADCs corresponding to the Mn-Kα peak. This result is useful to perform spectra calibration with varying temperature.

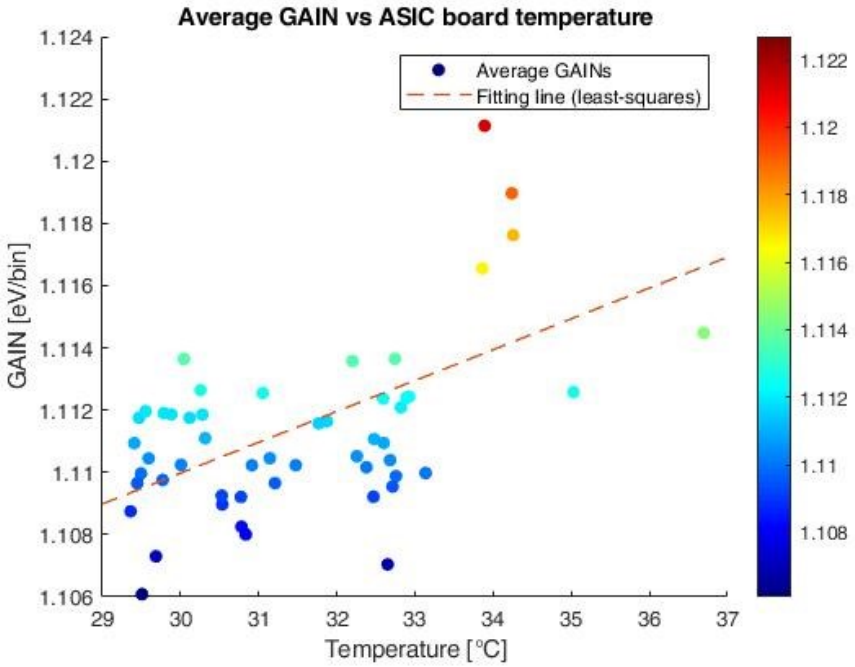
Similar behaviour is shown in Figure 3.31(b) by plotting the average gain of each measurement as a function of the temperature near to the Kerberos boards. Even in this case the average gain increases with temperature and, performing the same least-squares line fitting, it is possible to compute an increase of:

$$\frac{\Delta G}{\Delta T} = 6.1 \times 10^{-4} \ \frac{eV}{bin \times °C} \tag{3.12}$$

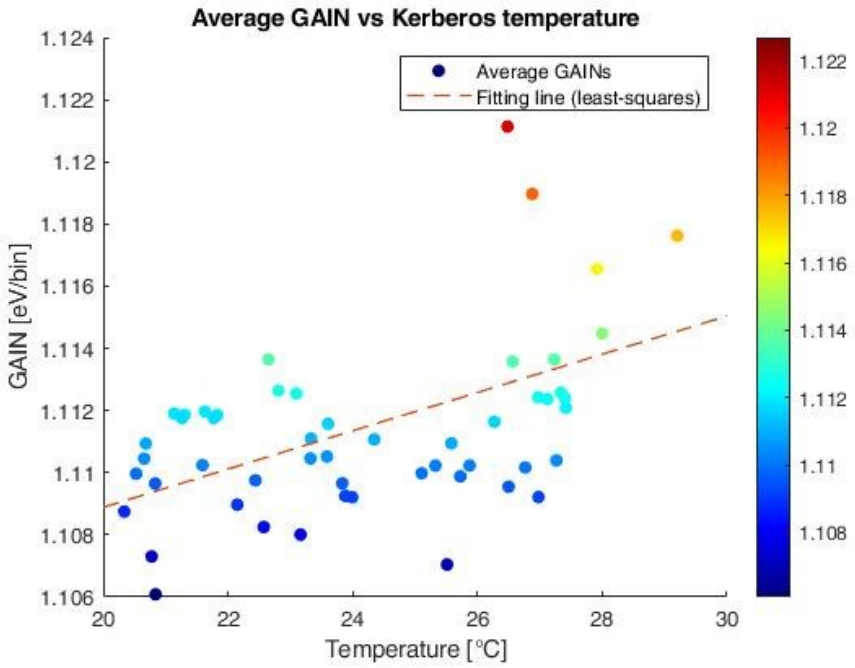
It corresponds to a peak shift of 0.61‰ for each degree of temperature increase. Thus, for a variation of 1 °C, the measured value of the Mn-Kα line will change of about:

$$\Delta E = 6.1 \times 10^{-4} \ \frac{eV}{bin} \times ADC_{K\alpha bin} \tag{3.13}$$

Summing up the results: the FWHM does not show a clear dependence with temperature over the long time stability measurement; the gain instead shows a small increase with temperature, both due to the temperature variations of the ASIC board gain (front end gain) and of the Kerberos gain (variations in the gain of SFERA ASICs, of the buffers and of Kerberos ADCs). Overall, the stability is good and the small gain variation is tolerable since in the final 3D vacuum setup the temperature will be better controlled.



(a)



(b)

Figure 3.31: *Plot of the average GAIN as a function of (a) the ASIC board temperature, (b) the Kerberos boards temperature.*

4. In vacuum 47-pixel module

This Chapter describes the design and the physical implementation of the "in vacuum 47-pixel module". It starts from an overview of the reasons why a vacuum testing setup is needed and its main goals. The discussion continues with an introduction to the in vacuum 12-pixel setup already present in the Department of Physics of Milano-Bicocca University.

The extension of this setup from 12 to 47-pixel is then described, focusing on the vacuum-air flange and on the interconnection board, called "Luna", which have been design and physically assembled during this thesis.

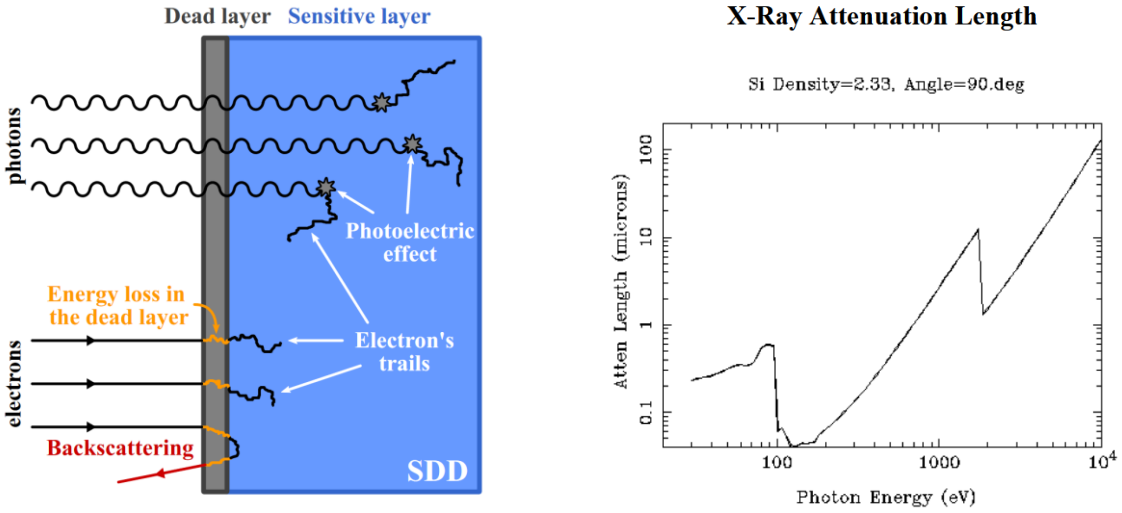
The last part of this chapter will focus on the in-air interconnections and will give a schematic description on how the in-vacuum components will be interconnected with the bias system in the final 47-pixel setup.

4.1 Overview

The main reasons to build a vacuum setup are to be able to test the SDD detectors (planar and 3D configurations) with different sources (X-rays, electrons, etc…) and using ancillary detectors to collect more information (e.g. backscattering).

This setup gives the possibility of doing different kinds of measurements. Alongside the typical X-ray characterization of the SDD detectors (e.g. the ones reported in Ref. [50] and in Ref. [51]), electron spectroscopy measurements are also possible. The detector response to electrons is much different and more complex than the response to X-ray photons. This originates from the incomplete charge collection happening in the partially sensitive entrance window region of the detector and also from the fact that electrons can backscatter. Since in TRISTAN experiment the detectors are hit by electrons generated from the tritium β^- decay, a deep understanding and modelling of the detector response is needed to take advantage of the high-resolution and high-rate capabilities of the SDDs to measure an unknown electron spectrum. In literature, only few articles address the response of SDDs and other Si-based detectors to impinging electrons. For the KATRIN project, a characterization with 20 keV and 30 keV has been

performed on the current FPD [52]. The interaction with Internal Conversion Electrons (ICEs), using ^{131m}Xe and ^{137}Cs sources is investigated in Ref. [53]. Another research focuses on the response to ICEs generated by ^{109}Cd, ^{133}Ba and ^{133}Xe sources [54]. Nevertheless, it is important to do a complete study of the SDD detector used in the TRISTAN project in order to build a precise model of the detector response to electrons.



(a) (b)

Figure 4.1: *(a) Simplified view showing the comparison between the absorption of photons and electrons in a silicon detector. (b) X-ray attenuation length in Silicon with 90° impinging angle [55].*

Figure 4.1(a) shows a comparison between the behaviour of a beam of photons and of a beam of electrons when they impinge on a silicon target. The photons, in the X-ray energy range, are absorbed mainly by photoelectric effect generating electron-hole pairs deeply inside the silicon sensitive layer. This because the energy of the X-ray lines (e.g. the Mn-Kα and the Mn-Kβ lines) is enough to provide an absorption length in silicon much higher than the dead layer thickness (< 100 nm in TRISTAN detector [56]), as shown in Figure 4.1(b). Therefore, the energy spectrum produced by a ^{55}Fe radioactive source, neglecting some marginal charge losses in the detector, can be well approximated with a Gaussian function, as shown in Figure 4.2.

The electrons, instead, undergo multiple interactions inside the detector. They start to interact in the superficial dead layer before releasing their energy into the active layer and, eventually, stop their path. This is the reason why, with electrons, the entrance windows effects are always observed, regardless of their energy, and a fraction of the initial electron energy is always released in the dead layer. This fraction of energy is lost, cannot be detected by the SDD. Moreover, some electrons may release a portion of their energy in the active layer , then backscatter and leave the detector still having a consistent fraction of the initial kinetic energy [57]. In the red energy response of Figure 4.2 the effect of backscattering and of the dead layer are clearly visible. The backscattering produces a low-energy continuum in the spectrum, while the interactions in the dead layer determine a shift to lower energies and an asymmetry in the electron peak.

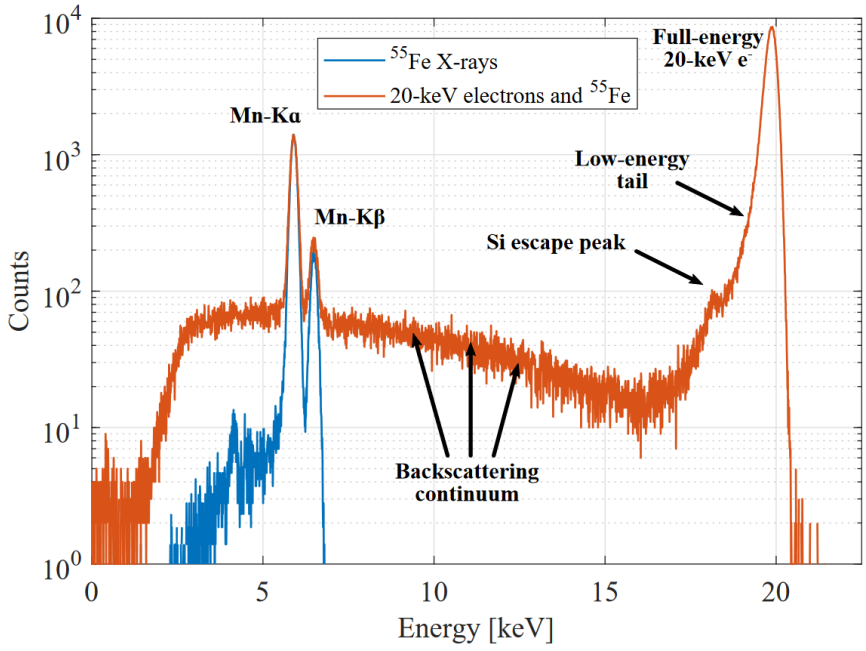
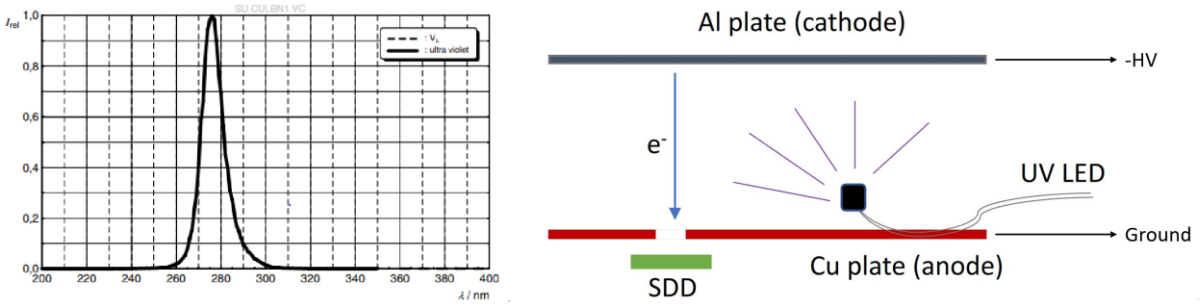


Figure 4.2: *Comparison between the energy response measured using only a ^{55}Fe X-ray source (in blue) and adding a mono-energetic 20 keV electrons source with normal incidence to the SDD surface (in red).*

In order to study the detector response to electrons accelerated with different energies, a photoelectric based electron gun has been implemented. It consists of an UV LED with peak photon emission at 275 nm wavelength, corresponding to an energy of 4.52 eV, as displayed in Figure 4.3(a). These photons are impinging on an aluminium

(*Al*) plate, used as cathode, and they are able to cause photoelectric emission, since the aluminium material has a work function of about 4.25 eV [58]. The emitted electrons are accelerated from the Al cathode plate toward a copper (*Cu*) plate, used as anode, by means of a potential difference. Indeed, the cathode plate is biased at a high negative voltage (*-HV*) provided by an external high voltage generator, while the anode plate is connected to ground. The SDD detector is placed underneath the anode and the electrons can impinge on it thanks to a little hole (1 mm) made on the copper plate and acting as a collimator for the electron beam. The working principle of the electron gun is summarized in Figure 4.3(b).



(a) (b)

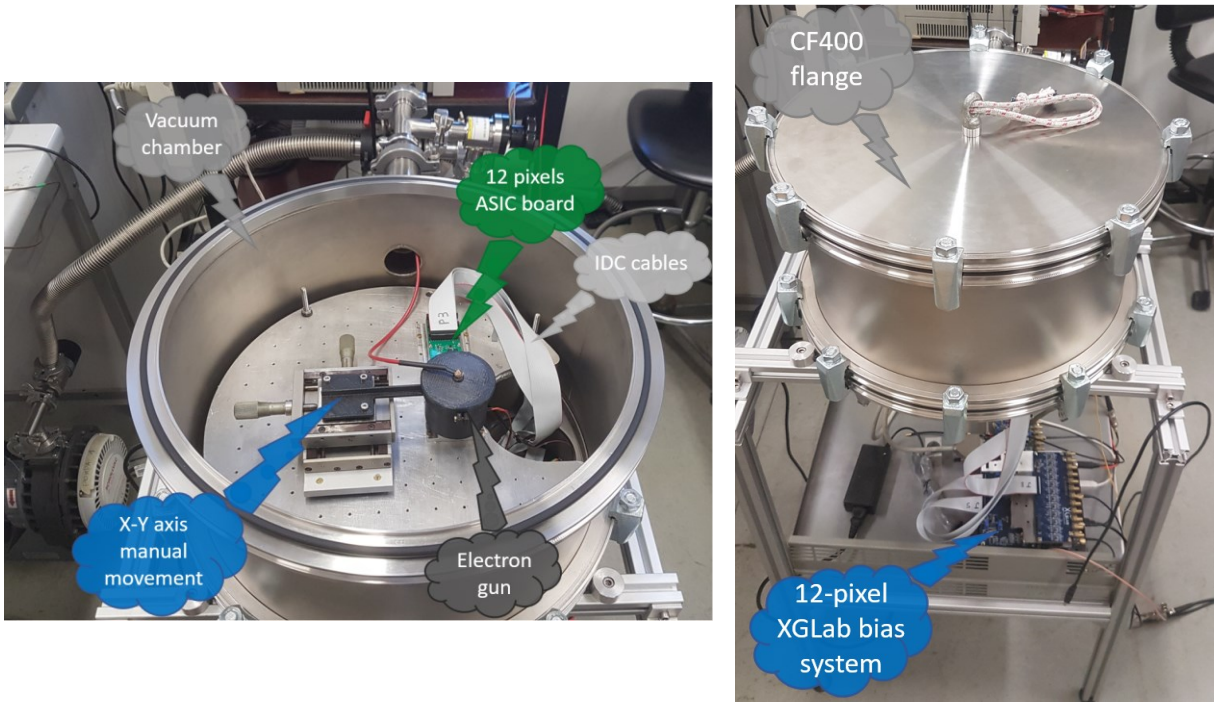
Figure 4.3: *(a) UV LED photon emission relative intensity vs wavelength. (b) Photoelectric based electron gun structure. Courtesy of A. Nava.*

The electron gun has been inserted in an insulator box, rigidly connected to an X-Y axis movement, as showed in the next section. This makes possible to study the charge sharing mechanism in the SDD detector. The charge sharing effect happens when the charge produced by an electron is generated at the border between two or more pixels and so it may be divided and collected by more than one pixel. Having a movable collimated beam allows us to precisely scan a given pixel of the detector matrix, moving the beam from the central region to the outer region of the pixel, and looking how the signals vary in the adjacent pixels.

4.2 12-pixel setup

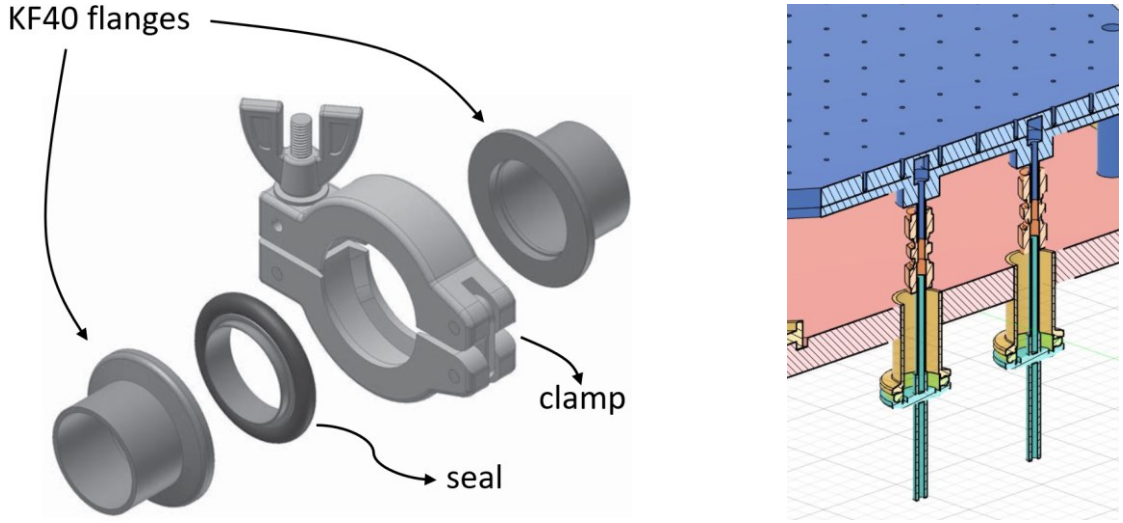
This section presents the experimental setup employed for the laboratory characterization of the 12-pixel detector with the electron gun source in vacuum environment.

Figure 4.4 illustrates the overview of the 12-pixel vacuum setup. The vacuum environment is provided by a vacuum chamber consisting of a lateral shielding and two CF400 flanges: the bottom one features feed-throughs and mechanical connections; the top one instead is blind. The chamber features a sophisticated cooling system based on a platform with a matrix of threaded holes with 26 mm pitch. A cooling fluid (can be either liquid nitrogen or chilled fluid) flows inside the platform thanks to two KF40 flange based sealing systems [59] connected to two Swagelok fittings [60], as shown in Figure 4.5. In particular, both sealing systems are composed by a seal placed between two flanges, where the seal consists of a centering ring and an O-ring stretched upon. The flanges are held together by a clamp having a modelled interior surface adequate to rigidly lock the conical shaped flanges.



(a) (b)

Figure 4.4: *Overview of the 12-pixel vacuum setup. (a) Internal view of the chamber. (b) External view of the chamber.*



(a) (b)

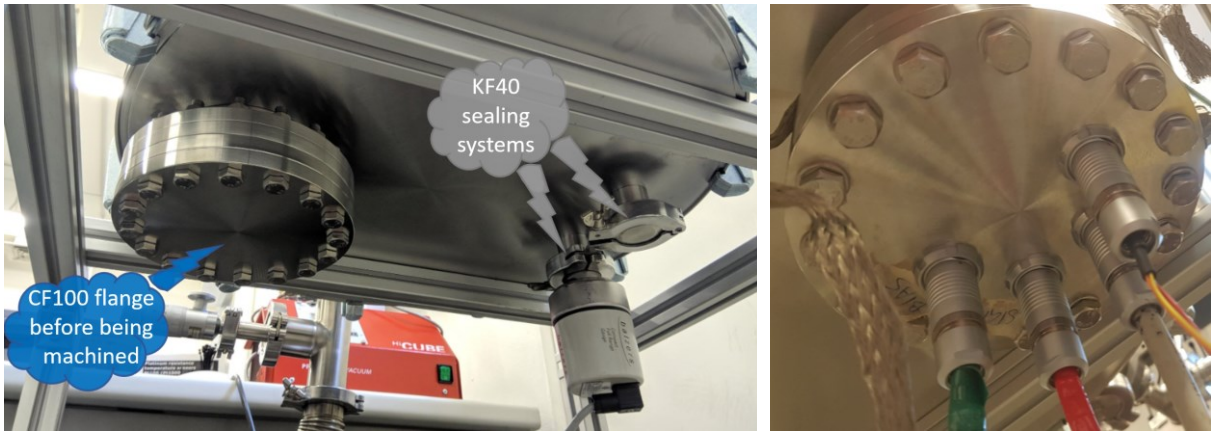
Figure 4.5: *(a) 3D illustration of the KF40 flange based sealing systems. (b) 3D model cross section showing the sealing systems connected to the Swagelok fittings reaching the cooling platform (Courtesy of A. Nava & M. Biassoni).*

Next to the KF40 systems there is a Vacom CF100 flange hosting four 27-pin Fischer connectors (described in the next section) employed to connect all the electrical signals inside the vacuum chamber, as shown in Figure 4.6. Specifically, they are configured in this way:

- Two 27-pin connectors are used for the 12-pixel module. One provides the detector and the ASIC biasing voltages, the other brings the 12-channel ASIC outputs outside the chamber. In vacuum side these two connectors are attached to the ASIC board connectors through 2-mm IDC cables soldered directly on the Fischer connector; in air side instead, they're connected to the 12-pixel XGLab bias system through 2-mm IDC cables soldered on a complementary connector (described in Section 4.4) plugged inside the Fischer connector.

- A 27-pin connector is partially used to bias the UV LED.

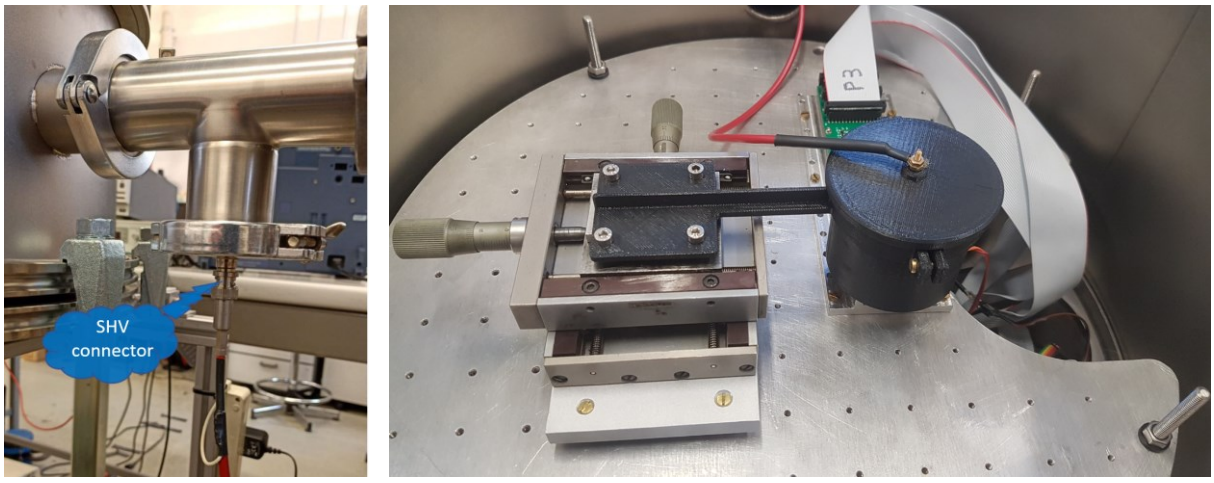
- A 27-pin connector hosts the biasing voltage lines and the readout lines of the single pixel detector.



(a) (b)

Figure 4.6: *(a) Bottom view of the chamber showing the KF40 sealing systems and the CF100 flange before being machines (Courtesy of A. Nava & M. Biassoni). (b) Close view of the CF100 flange after being machined and connected to the cables.*

As illustrated in Figure 4.7(a), an additional hole has been done in the lateral face of the chamber connecting other cavities to provide the high voltage to the electron gun (using a SHV connector linked to an external high-voltage generator) and to create a vacuum ambient of about 1e-4 mbar during measurements (using a vacuum pump).



(a) (b)

Figure 4.7: *(a) SHV connector (Courtesy of A. Nava & M. Biassoni). (b) Electron gun mechanically connected to the X-Y axis manual movement and placed over the 12-pixel module.*

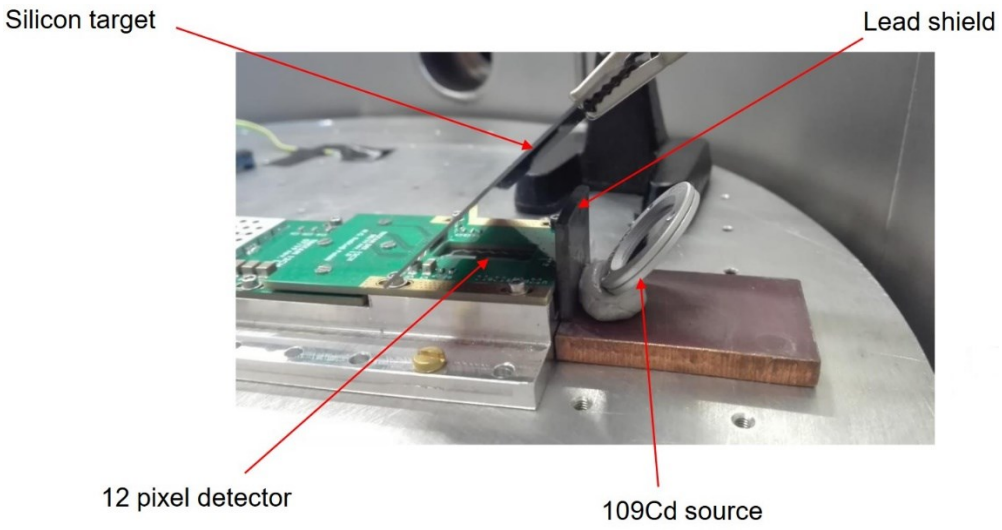
Figure 4.7(b) gives a close view of the components inside the chamber. The already mentioned electron gun is placed above the 12-pixel detector, which is bonded to the detector board that, in turn, it is attached to the ASIC board. The electron gun can be moved along X and Y axis by a manually regulated mechanical movement system. This is useful to perform charge sharing measurements by moving the electron gun across the pixel matrix, as described in the previous section.

A drawback of this configuration is that every time the electron gun needs to be moved, the chamber have to be opened to manually adjust the movement system, losing the vacuum generated inside and requiring a quite long time to recreate it. This is why, in the following 47-pixel setup, this manual movement will be substituted by an automatic movement (described in the next section).

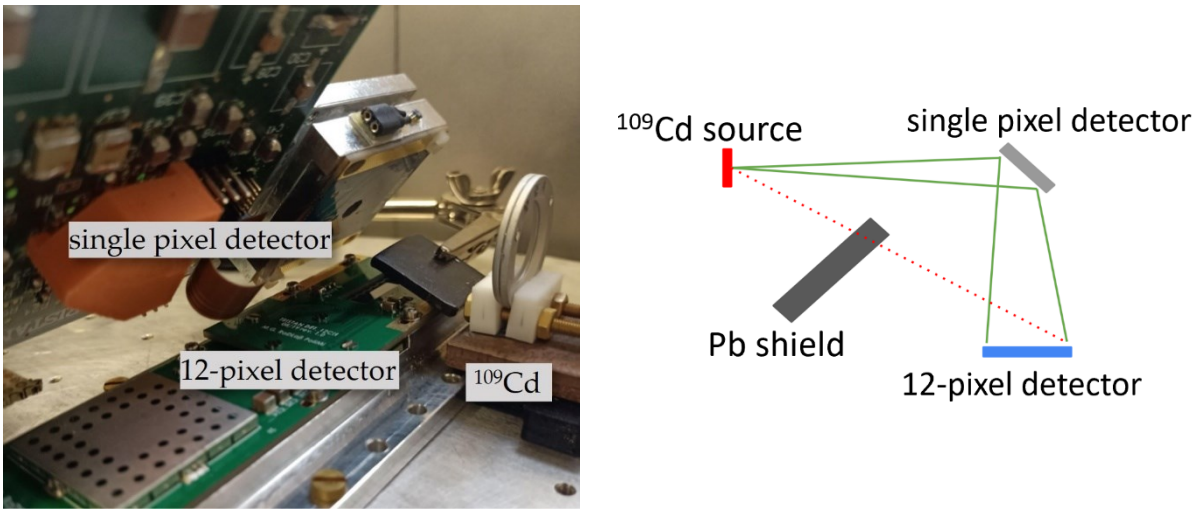
This vacuum setup is able also to perform backscattering measurements. In particular, a ^{109}Cd radioactive source, which emits mainly two X-ray (22 and 25 keV) and two internal conversion electrons (62.5 and 84 keV), is used to hit a passive Si target (a simple block of silicon) or an active Si target (the single pixel detector) and the backscattered electrons are measured with the 12-pixel detector. To protect the 12-pixel detector by direct irradiation of the Cd source and measuring only the backscattering effect, a lead shield has been inserted between the detector and the source, as illustrated in Figure 4.8.

Outside the chamber, in air, the 12-pixel XGLab bias system provides power supply and control signals for the ASIC and for the SDD matrix. This system also contains a buffer board that provides single-ended outputs for each pixel signal with a gain factor $G = +2$, and selectable DC offset to adapt these outputs to different DAQ solutions.

Specifically, in the 12-channel setup, two different DAQ solutions have been adopted: a single channel version of the already mentioned DANTE DPP and the CAEN DT5743 8-channel digitizer [61]. Therefore, with the 12-pixel setup is not possible to observe all the 12-pixel outputs simultaneously.



(a)



(b)

Figure 4.8: *Backscattering measurement setup using: (a) a passive Si target; (b) an active Si target. Courtesy of A. Nava & M. Biassoni.*

4.3 47-pixel setup

This section presents the changes and the upgrades done in the previous setup to avoid the drawbacks highlighted in the previous section and to be suited for the laboratory characterization of the 47-pixel detector, performed with the electron gun source in vacuum environment.

4.3.1 47-pixel flange

The vacuum chamber structure, with its cooling system and the lateral cavities, was already compatible with the 47-pixel module, so no changes have been introduced. Concerning the vacuum-air interconnections, the main difference between the 12-pixel setup and the 47-pixel setup is due to the number of output channels present in the ASIC board. Indeed, since the supply voltages of the new detector and of the 47-channel ASIC board are the same as the 12-pixel module, an equal pinout connector can be adopted. The 4×12-channel outputs ETTORE ASICs instead require a complete redesign of the CF100 flange. The new flange, shown in Figure 4.9, hosts six 27-pin "DBPE 105_A102-130" Fischer connectors and it's configured in this way:

- A 27-pin connector is used to provide the control and biasing voltages both to the detector and to the ASIC board.

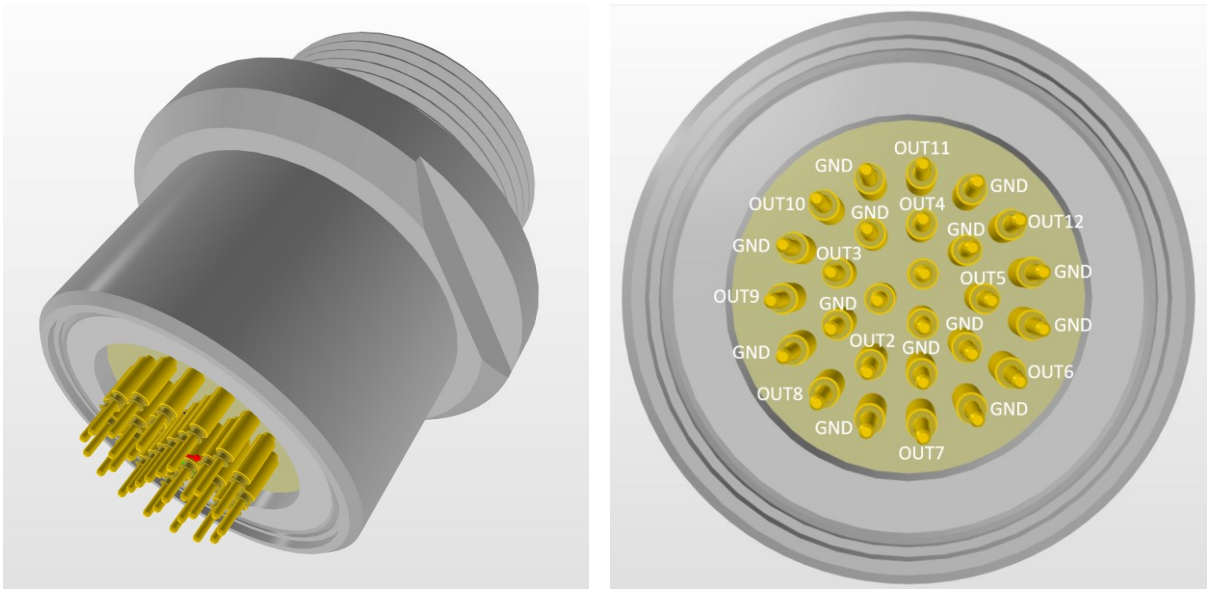
- Four 27-pin connectors are employed to brings the ASICs outputs outside the chamber. In particular each of them has 12 pins connected to the 12 outputs of a different ASIC, alternated with 12 pins connected to ground, while the three central pins are left floating. The connector which is carrying the first 1-to-12 channels of the ASIC board has the first output pin connected to ground, since the first channel of the 47-pixel board is not connected to any pixels. The pinout of this connector is shown in Figure 4.10.

- A 27-pin connector is used to bias the UV LED and the new vacuum compatible stepper motors used to move the electron gun.

On top of the flange, soldered to the connectors, has been placed an interconnection board to adapt the 100-pin connectors, present on the ASIC board, to the 27-pin connectors. This board, designed and realised during this thesis together with the flange, is described later.

(a) (b)

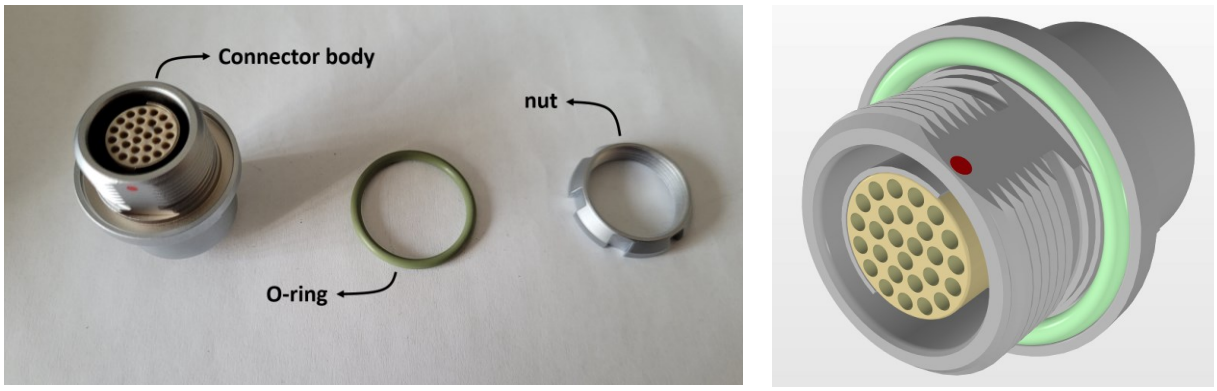
Figure 4.9: *(a) Front view of the flange (vacuum side). (b) Back view (air side) of the 3D model of the flange. The red dot indicates the flat side of the connector.*



(a) (b)

Figure 4.10: (*a) Lateral view of the 3D Fischer connector model. (b) Front view of the 3D connector model showing the pinout used for the first 2-to-12 ASIC outputs.*

As already mentioned, the connectors used in the flange are the *27-pin Fischer DBPE 105_A102-130* [62]. They are made up of a main body hosting the 27 pins, an O-ring used to get the vacuum seal and a nut, as illustrated in Figure 4.11(a). The main body is placed in the vacuum side of the flange, with the O-ring interposed between the shrinkage of the flange and the connector body. The nut is placed in the opposite side and screwed to the connector thread. The connectors present a flat side indicated with a red dot, visible in Figure 4.11(b).



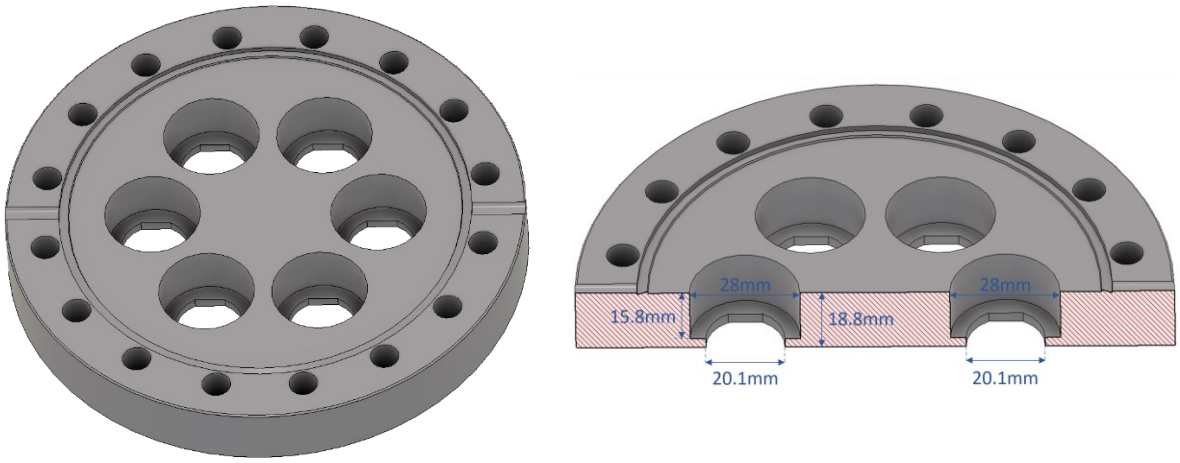
(a) (b)

Figure 4.11: *(a) Connector components. (b) 3D model of the connector showing the green O-ring and the flat side indicated with a red dot.*

Figure 4.12 displays two important details of the flange holes design:

- In order to avoid a too high torque on the soldered pins during the screwing of the connectors, a flat side on the flange holes, aligned to the one of the connectors, has been performed.

- In order to get a good vacuum seal, the O-ring must adhere properly. This is obtained by properly sizing two different diameters of the holes: 28 mm in the vacuum side, 20.1 mm in the air side.



(a) (b)

Figure 4.12: *(a) 3D model of the flange showing the flat side of the holes. (b) Annotated cross-section of the 3D model displaying the holes geometry.*

4.3.2 Luna Board

Moving from the 12-pixel setup to the 47-pixel one, the 47-channel ASIC board has been adopted to readout the detector. Differently from the 12-channel version, this board features two *Hirose FH29B-100S-0.2SHW* 100-pin FPC connectors used for the output signals and for ASIC and SDD power supply. The FPC connectors are attached to FPC cables to link the ASIC board to an interconnection board, since these cables cannot be directly soldered to the 27-pin Fischer connectors (as happens for the IDC cables used for the 12-channel board). This interconnection board, used to connect the ASIC board to the Fischer connectors, is called *Luna board* and is shown in Figure 4.13. On the front side, the FPC connectors are placed in the central region, with the corresponding labels realized with silkscreen printing. The same technique is used to indicate the signals of the connectors pads. Specifically, they're arranged at five vertices of a hexagon, while the sixth vertex has been cut out because it corresponds to the connector used to bias the UV LED and the stepper motors. Indeed, the previous five connectors are linked, through the Luna board, to the two FPC connectors, instead the last connector is mounted on the flange and directly soldered to the UV LED and the stepper motors wires.

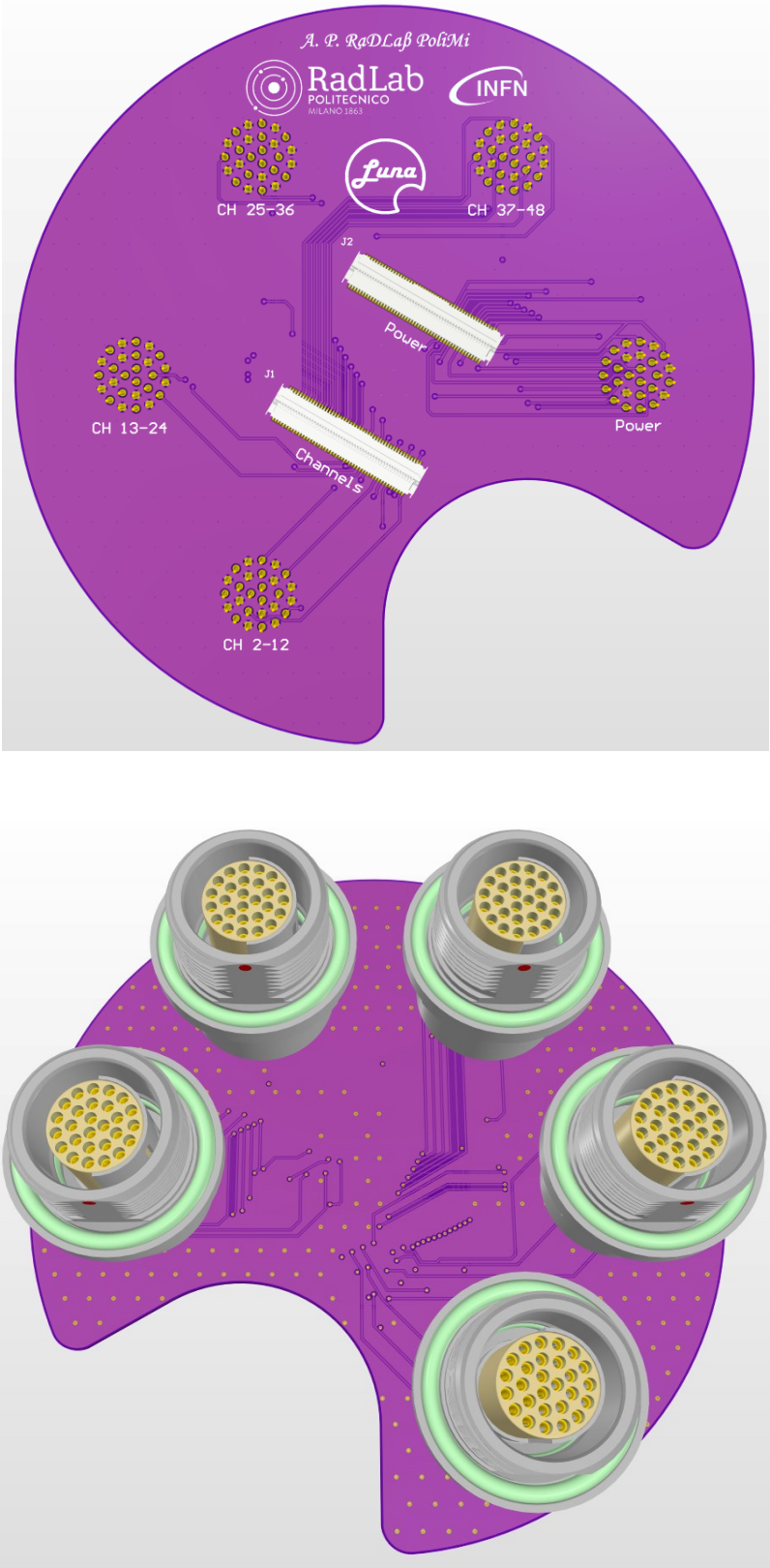


Figure 4.13: *Front side (top) and back side (bottom) of the 3D model Luna board.*

The routing of Luna board has required a 4-layers PCB, due to the high density of tracks near to the FPC connectors used for the output signals, as displayed in Figure 4.14. The hexagonal placement of the connectors pads, around the central FPC connectors, allows to have not only enough space between parallel running tracks, so minimizing the crosstalk effects, but also a not too sharp angle of the FPC cables, which may cause damages or even break the cables .

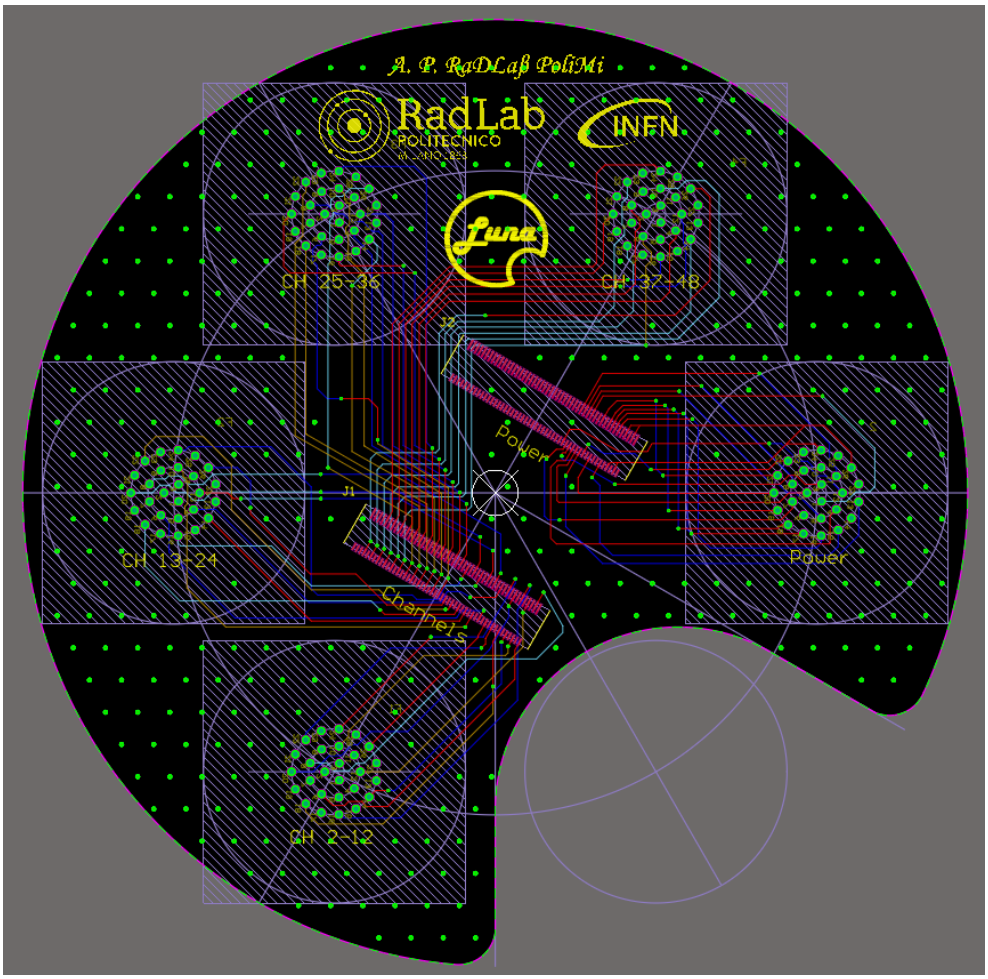


Figure 4.14: *2D layout view of Luna board.*

Figure 4.15 shows the soldering of the Luna board to the 27-pin Fischer connectors performed in the laboratory. The final structure, ready to be inserted in the vacuum setup, is displayed in Figure 4.16. It's composed by the Luna board, the two FPC connectors, the five Fischer connector soldered to the board, the connector for the LED and motors and the vacuum-air CF100 flange.

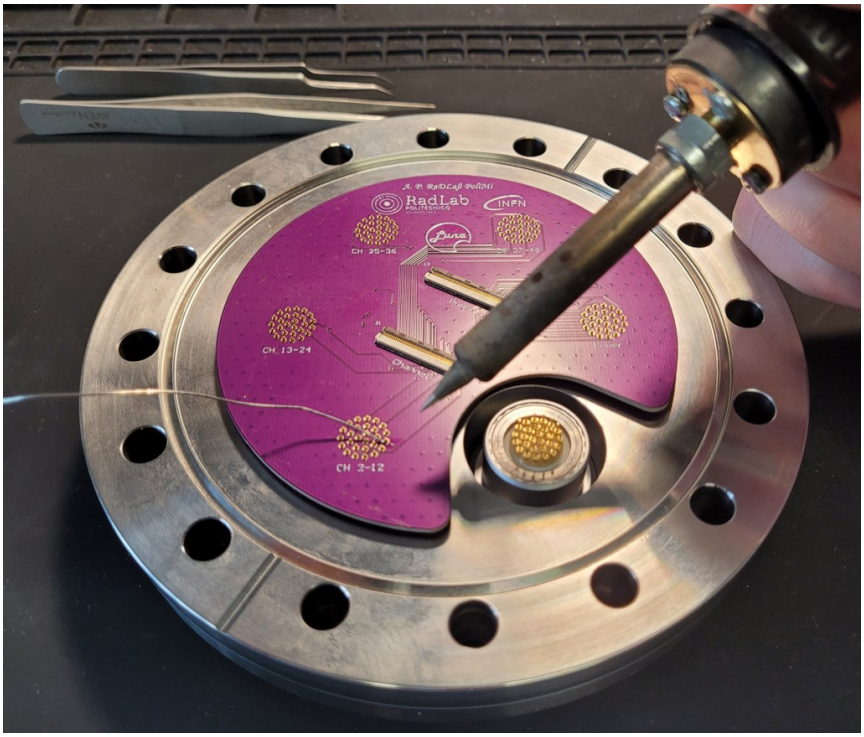


Figure 4.15: *Soldering of Luna board to the five 27-pin Fischer connectors*

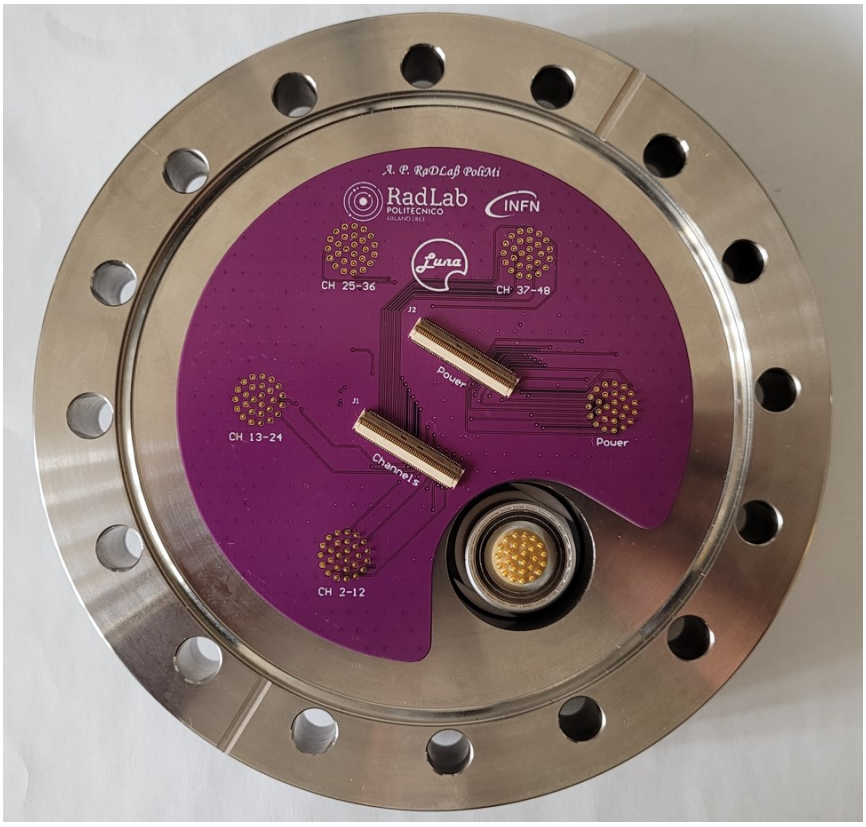


Figure 4.16: *Vacuum-air interconnection system for the 47-pixel vacuum setup.*

4.3.3 Kerberos TAC

For the 47-pixel setup, a new DAQ has been designed, in parallel, in another Master Thesis project at Politecnico di Milano. It's called *Kerberos TAC* (Time to Amplitude Converter) and is an evolution of Kerberos.

In particular, Kerberos TAC (Figure 4.17) is able not only to acquire the energy information, but also to acquire the time information of the triggering event on the pixel. Therefore, not only the energy spectrum, but also the arrival time can be measured, allowing to detect charge sharing events by looking at neighbouring pixels showing a given charge simultaneously.

Figure 4.17: *Kerberos TAC.*

4.3.4 Automatic movement system

Finally, to move the electron gun without opening the chamber, a vacuum compatible stepper motors based movement system is under development by the Milano-Bicocca University team (Figure 4.18).

This movement system will allow not only to move along X-Y directions, but also to change the electron gun and target angles when backscattering measurements are carried out. In this way, measurements at different energies, different angles (both of incidence and reflection) and with different target materials can be performed.

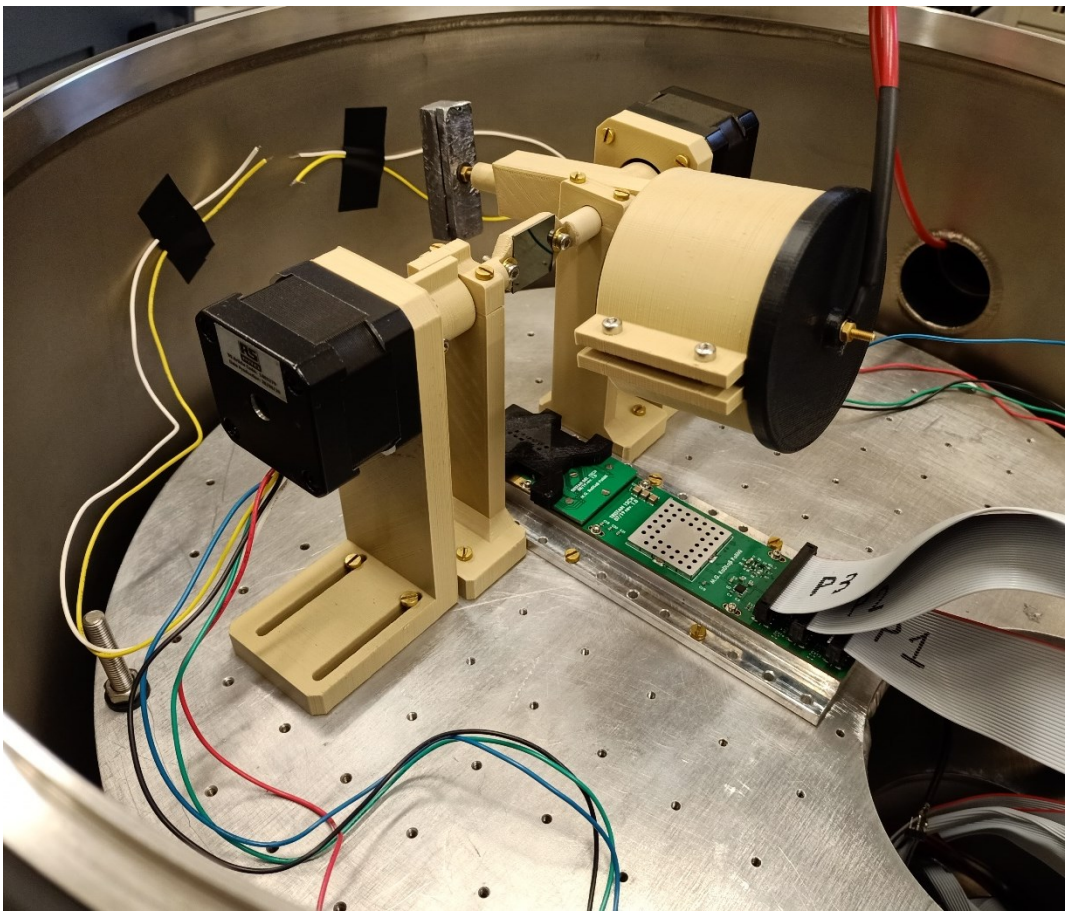


Figure 4.18: *Vacuum compatible stepper motors movement system during testing phase in the old 12-pixel setup. Only the automatic angular movement is shown in this picture, the automatic X-Y movement will be implemented in the future. Courtesy of A. Nava & M. Biassoni.*

4.4 In-air interconnections

This section describes the interconnections between the in-vacuum components and the external bias system. In particular, since the vacuum side interconnections have already been described, it will focus on the in-air interconnections between the 27-pin connectors and the bias system, to give a complete view of the interconnection scheme.

Both in the 12-channel and 47-channel XGLab bias system, the detector biasing and the ASIC biasing are provided by two 2-mm IDC connectors having the same pinout in both the setups. These connectors are located on the left side of the bias board, as shown in Figure 4.19, and are linked to the same 27-pin Fischer connector through IDC ribbon cables. The cables have been crimped to the IDC connectors, on the board side, while, on the other side, they have been frayed and soldered to a complementary connector, plugged inside the vacuum-air Fischer connector (see Figure 4.20).

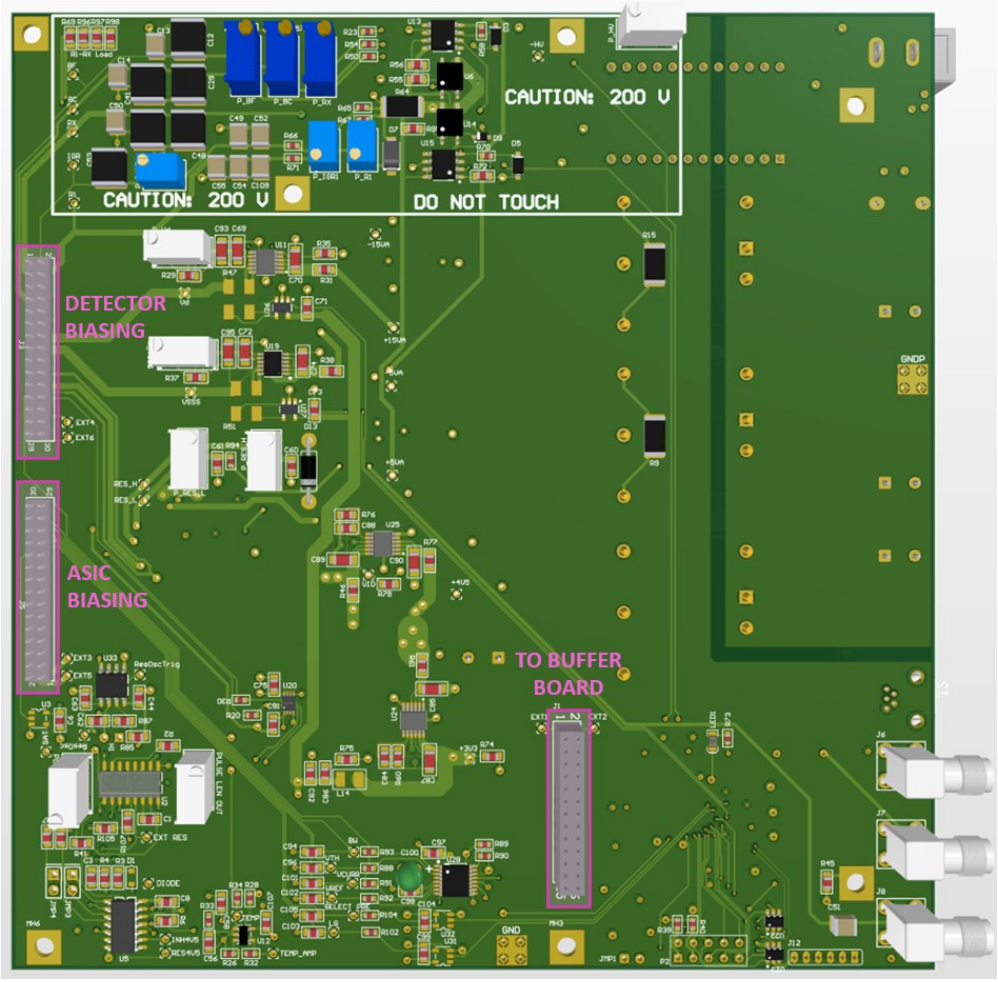


Figure 4.19: *3D model of the bias board showing the two IDC connectors and the board-to-board connector.*

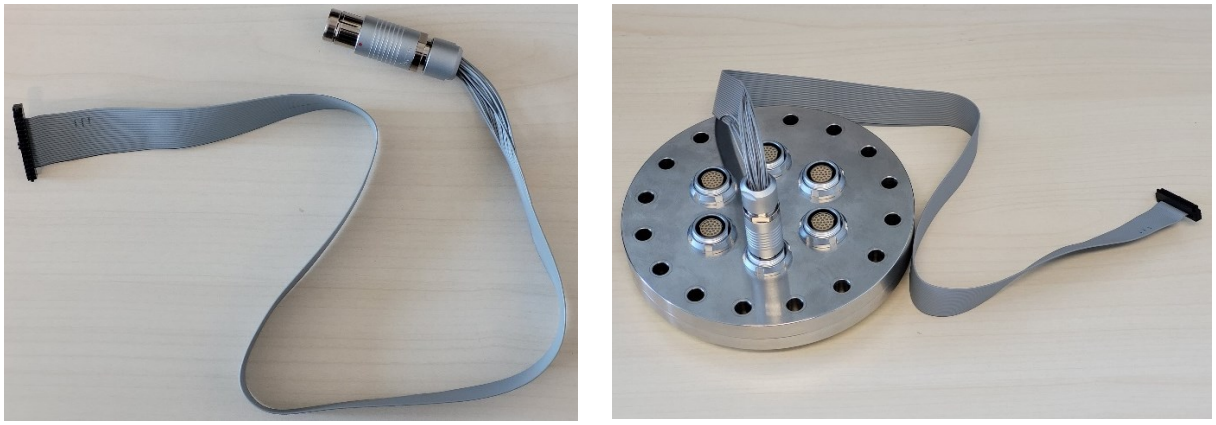


Figure 4.20: *On the left: ribbon cable crimped to the IDC connector, on one side, and attached to the complementary connector, on the other side. On the right: connector plugged inside the vacuum-air Fischer connector.*

This complementary connector, show in Figure 4.21, is the *Fischer S 105 A102-130+* [63]. On one side it has 27 pins that are connected to the air side of the *Fischer DBPE 105_A102-130* connector, as visible in Figure 4.21(b). On the other side it presents a conical disposition of the pins that helps the soldering of the frayed IDC cables, as illustrated in Figure 4.21(c). The same interconnection strategy, using the same type of complementary connectors, is adopted for the other vacuum-air connectors present inside the CF100 flange.

(a) (b) (c)

Figure 4.21: *Fischer "S 105 A102-130+" connector: (a) before being assembled; (b) front side view; (c) back side view.*

Each IDC connector have 30 pins, but many of them bring redundant/optional signals or additional ground lines, not necessary for the vacuum setup. Thus, in order to adapt them to the 27 pins of the Fischer connector, a mapping of the pins has been done, as shown in Figure 4.22. The pins highlighted in green are the ones that are soldered to the Fischer connector, while the pins highlighted in red are left floating. The *EXT4* and *EXT6* pins are additional lines implemented in the bias system to drive some extra sensors that are not used in this setup.

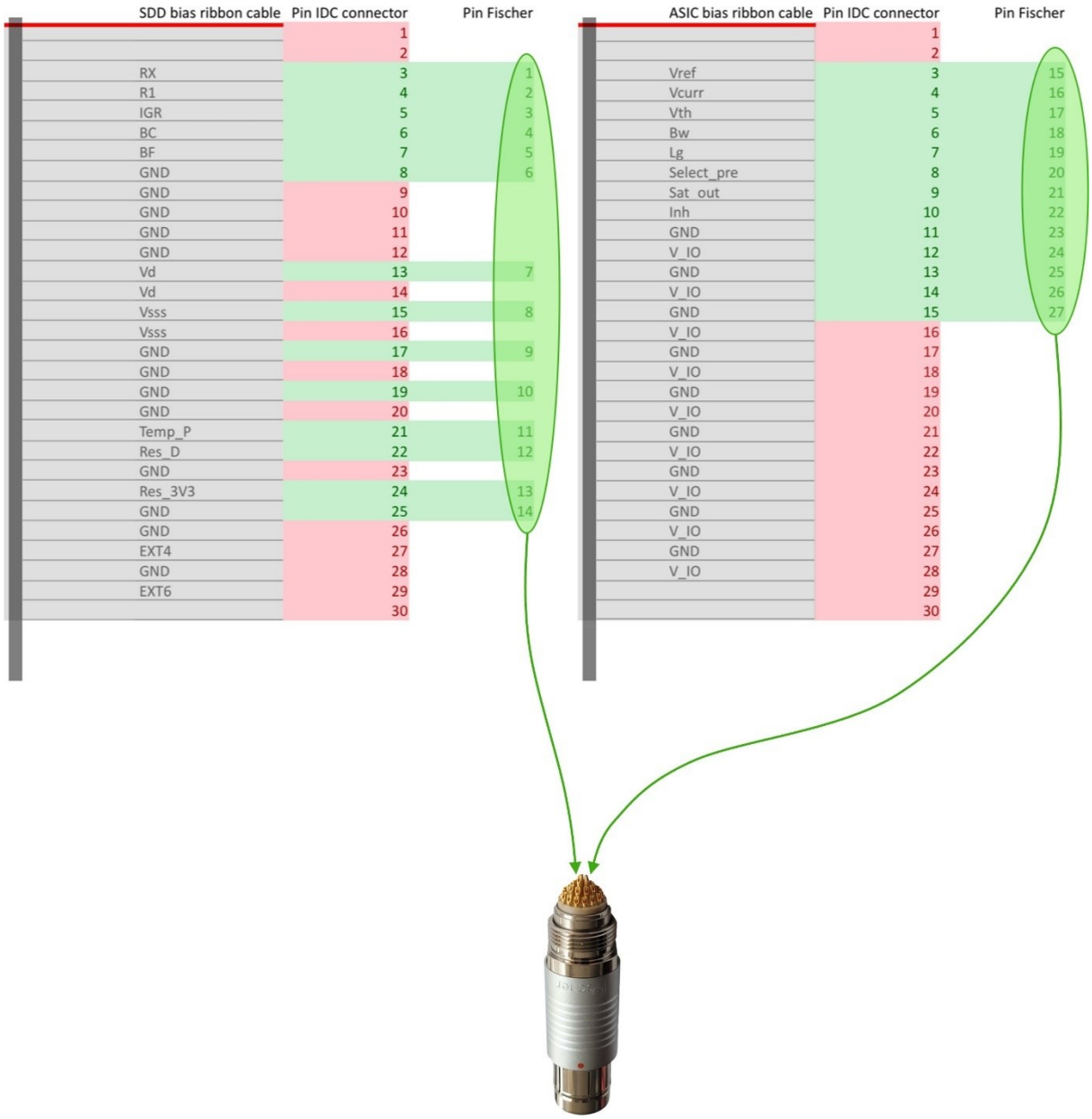
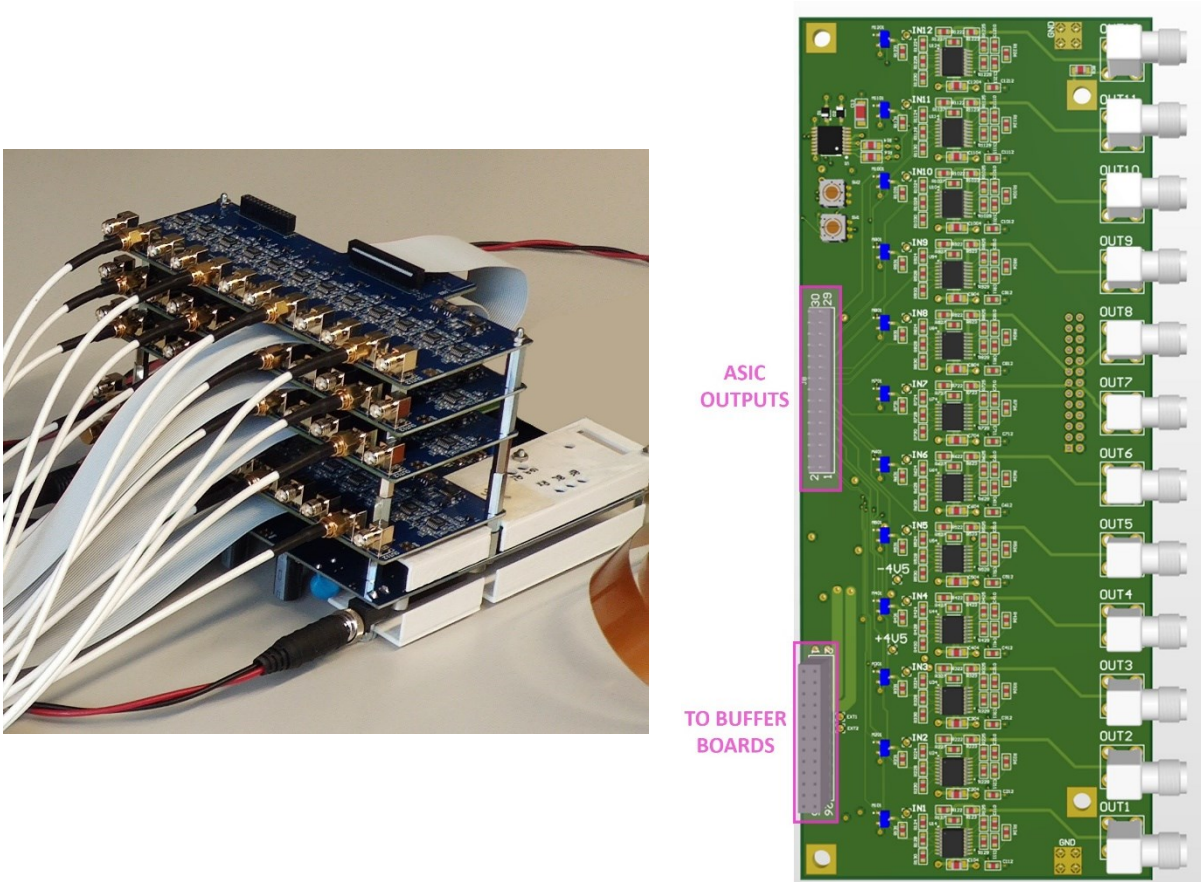


Figure 4.22: *Pinout mapping scheme of the Fischer connector bringing the detector and ASIC bias and control signals.*

The board-to-board connector, visible in Figure 4.19, is used to attach the bias board to the buffer board. In the 47-channel version, displayed in Figure 4.23(a), the bias system contains four replicas of the 12-channel buffer board, described at the end of Section 4.2. These four buffer boards are arranged one on top of the other, linked through board-to-board connectors, and each of them is connected to a different Fischer connector, in order to buffer 12 outputs coming from a different ETTORE ASIC.

This connection is made through IDC ribbon cables linking each IDC connector, present on the buffer boards, to the corresponding *S 105 A102-130+* Fischer connector, following the interconnection strategy already described for the detector and ASIC biasing connector. The 3D model of the buffer board is illustrated in Figure 4.23(b).



(a) (b)

Figure 4.23: *(a) 47-channel XGLab bias system. (b) 3D model of the buffer board showing the IDC connector (for the ASIC outputs) and the board-to-board connector.*

Even in this case, a mapping of the pins, equal for all the four buffer boards, is needed to adapt the 30 positions IDC connectors to the 27-pin Fischer connectors. Each ribbon cable carries 12 output signals, except for the output #1 of the first connector, which is attached to the missing pixel and thus it's connected to ground on the Luna board. These output lines are interleaved with ground lines to reduce the crosstalk between different output channels. The remaining lines are not used, so they're left floating. The schematic view of the mapping is illustrated in Figure 4.24, where the pins highlighted in red are the ones left floating.

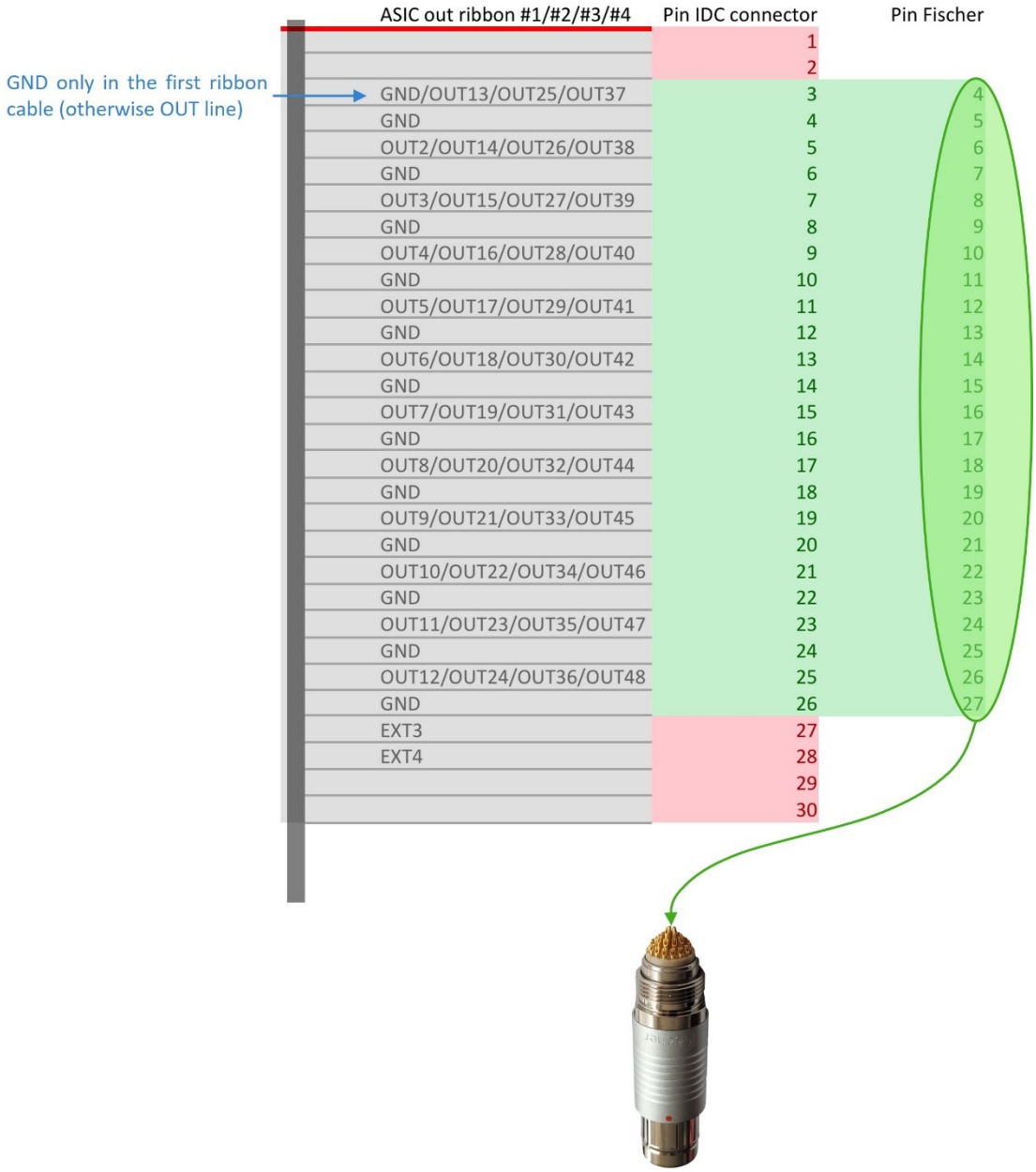
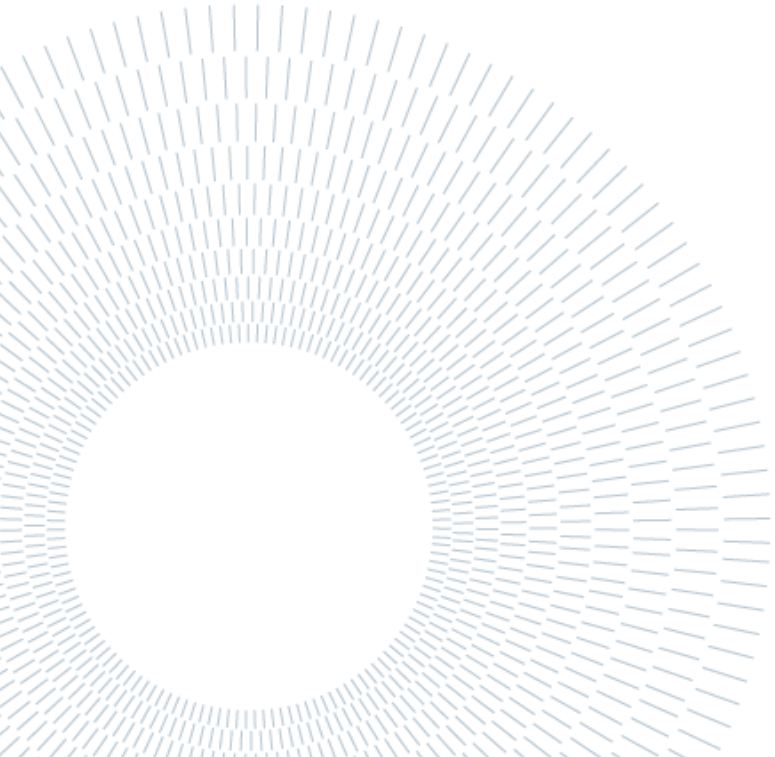


Figure 4.24: *Pinout mapping scheme of the Fischer connectors bringing the ASICs outputs.*



5. Conclusion and future development

This thesis work is carried out in the context of the TRISTAN project, an international collaboration that aims to probe the existence of a new type of elementary particle: the sterile neutrino. In particular, it takes place at the end of *Phase 0* of the project, whose purpose is to develop the first 3D 166-pixel monolithic detection module that will be installed and tested inside the KATRIN MoS (Monitor Spectrometer).

The first objective of the thesis was the realization of a more compact bias system for the planar 166-pixel TRISTAN module to perform the preliminary in-air characterization of the new 166-pixel SDD detector and to test the 83-channel ASIC boards, each of them equipped with 7 ETTORE chips. This bias system, called "Lifeboard", is able to provide all the supply voltages required by the SDD detector and by the ASIC boards, to give the global SDD reset and the ETTORE inhibit signal, and to set the control signals of the ASICs. The only missing components are the buffers, used to give a further amplification to the output signals (G = +2) and selectable DC offset, which is not a limitation in the laboratory setup.

The Lifeboard has been used to perform spectroscopy measurements to characterize the 166-pixel detector. The operation of a monolithic SDD array of this size represents a relevant milestone in this field. All the measurements were performed using a ^{55}Fe radioactive source. The count rate of each pixel, the gain of each channel and the energy resolution of each spectrum have been computed from the data acquired with these measurements, showing a quite good FWHM but not optimal due to an unexpected not negligible drain line resistance that made critical the correct biasing of all the pixel simultaneously. In the next months, the 166-pixel detectors of the new wafer production, implementing design modifications to mitigate this issue, are going to be tested in MPP.

Another important measurement performed during this thesis with the in-air 166-pixel planar setup is the long-time stability measurement. It was a 53-hours measurement aiming at studying the system performance stability over time and with temperature variations. The monitoring of the temperature was done by designing a simple

amplifying circuit to readout two PT1000 sensors and by using the data logger functionality of the Moku:Go tool. The results of this measurement showed a not clear dependence of the FWHM with temperature, while the gain revealed a small increase with temperature which is tolerable for the final 3D vacuum setup.

The final part of this thesis work was the development of the new vacuum-air interconnection system to move from the 12-pixel vacuum setup (already present in the Department of Physics of Milano-Bicocca University) to the 47-pixel one. This vacuum setup is important to study and model the SDD detector response to electrons, which are here generated and accelerated against the detector by a photoelectric based electron gun, and to analyse the backscattering phenomena. Understanding the interaction of the SDD detector with electrons is fundamental since, in the final TRISTAN experiment, the detectors will be hit by electrons generated from the tritium β^- decay and accelerated by magnetic fields. The new 47-pixel vacuum setup will be fully tested in the next months to acquire the first 47-pixel detector energy spectra using the electron gun accelerating electrons with different energies. New backscattering measurements will be also done, to understand the behaviour of this larger detector. In particular, the stepper motors based movement system will allow to measure the backscattering due to electrons impinging at different angles.

As illustrated in Figure 5.1, the TRISTAN project phase 0 will ends with the realization and subsequent installation of the 166-pixel module inside the MoS, that will be the first *tile* of the final detector for the sterile neutrino search. The following developments of the TRISTAN project will consist in the duplication of this first 166-pixel module in order to obtain nine tiles (1494 pixels), at the end of phase 1, and twenty-one tiles (3486 pixels), at the end of phase 2, that will be installed in the Main Spectrometer of the current KATRIN experiment.

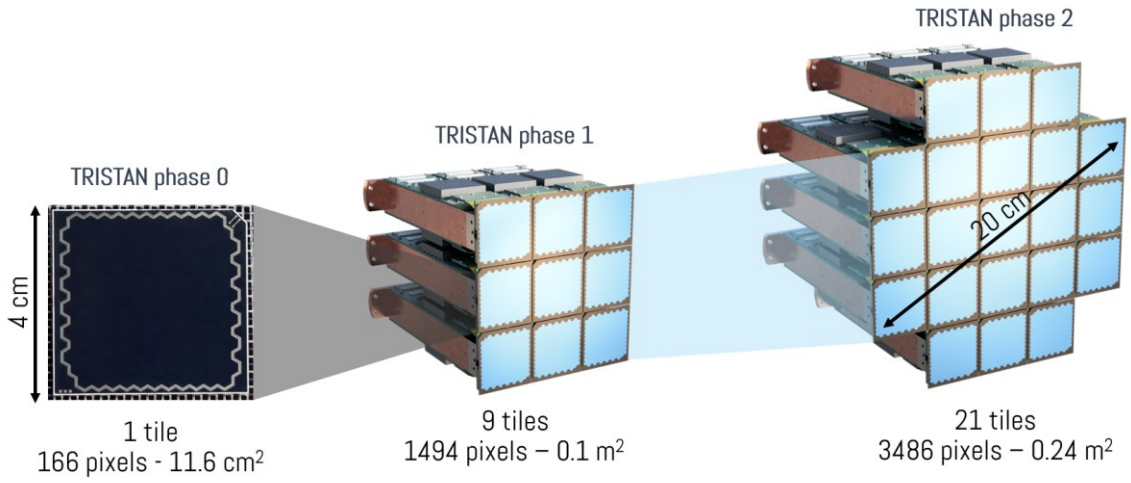


Figure 5.1: *TRISTAN detector development phases.*

Bibliography

[1] T. Greicius, 'Planck: Exploring the Birth of Our Universe', *NASA*, Jul. 05, 2018. http://www.nasa.gov/mission_pages/planck/overview.html (accessed Mar. 28, 2022).

[2] T. Greicius, 'Planck Mission Brings Universe Into Sharp Focus', *NASA*, Jun. 07, 2013. http://www.nasa.gov/mission_pages/planck/news/planck20130321.html (accessed Mar. 28, 2022).

[3] S. Mertens, 'Direct Neutrino Mass Experiments', *J. Phys. Conf. Ser.*, vol. 718, p. 022013, May 2016, doi: 10.1088/1742-6596/718/2/022013.

[4] Nakamura, K et al. "Neutrino mixing 1 13. NEUTRINO MASS , MIXING , AND OSCILLATIONS." (2014).

[5] M. Tanabashi, K. Hagiwara, K. Hikasa, K. Nakamura, Y. Sumino, F. Takahashi, J. Tanaka, K. Agashe, G. Aielli, C. Amsler, et al., "Review of particle physics", Physical Review D, vol. 98, no. 3, p. 030 001, 2018.

[6] Y. Fukuda, T. Hayakawa, E. Ichihara, K. Inoue, K. Ishihara, H. Ishino, Y. Itow, T. Kajita, J. Kameda, S. Kasuga, et al., "Evidence for oscillation of atmospheric neutrinos", Physical Review Letters, vol. 81, no. 8, p. 1562, 1998.

[7] T. Kajita, "Discovery of atmospheric neutrino oscillations", Nobel Lecture, 2015.

[8] L. Canetti, M. Drewes, and M. Shaposhnikov, "Sterile neutrinos as the origin of dark and baryonic matter", Physical review letters, vol. 110, no. 6, p. 061 801, 2013.

[9] T. Thakore, M. M. Devi, S. K. Agarwalla, and A. Dighe, 'Active-sterile neutrino oscillations at INO-ICAL over a wide mass-squared range', J. High Energy Phys., vol. 2018, no. 8, p. 22, Aug. 2018, doi: 10.1007/JHEP08(2018)022.

[10] C. Giunti and T. Lasserre, "Ev-scale sterile neutrinos", Annual Review of Nuclear and Particle Science, vol. 69, pp. 163–190, 2019.

[11] R. Adhikari, M. Agostini, N. A. Ky, T. Araki, M. Archidiacono, M. Bahr, J. Baur, J. Behrens, F. Bezrukov, P. B. Dev, et al., "A white paper on keV sterile neutrino dark matter", *Journal of cosmology and astroparticle physics*, vol. 2017, no. 01, p. 025, 2017.

[12] G. Drexlin, K. Collaboration, et al., "Katrin-direct measurement of a sub-ev neutrino mass", Nuclear Physics B-Proceedings Supplements, vol. 145, pp. 263–267, 2005.

[13] A. Picard et al. *A solenoid retarding spectrometer with high resolution and transmission for keV electrons. Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, 63(3):345–358, 1992.

[14] C. Kraus et al. *Final results from phase II of the Mainz neutrino mass search in tritium beta decay. The European Physical Journal C-Particles and Fields*, 40(4):447–468, 2005.

[15] V. N. Aseev et al. *Upper limit on the electron antineutrino mass from the Troitsk experiment.* Phys. Rev. D, 84:112003, Dec 2011.

[16] K. Collaboration, "Katrin design report 2004", Wissenschaftliche Berichte FZKA, vol. 7090, 2005.

[17] M. Aker, K. Altenmüller, J. Amsbaugh, M. Arenz, M. Babutzka, J. Bast, S. Bauer, H. Bechtler, M. Beck, A. Beglarian, et al., "The design, construction, and commissioning of the katrin experiment", Journal of Instrumentation, vol. 16, no. 08, T08015, 2021.

[18] S. Mertens, K. collaboration, et al., "Status of the katrin experiment and prospects to search for kev-mass sterile neutrinos in tritium beta-decay", Physics Procedia, vol. 61, pp. 267–273, 2015.

[19] M. Aker et al. *The design, construction, and commissioning of the KATRIN experiment. Journal of Instrumentation*, 16(08):T08015, 2021.

[20] M. Zbořil et al. *Ultra-stable implanted 83Rb/83mKr electron sources for the energy scale monitoring in the KATRIN experiment. Journal of Instrumentation*, 8(03):P03009–P03009, 2013.

[21] M. Aker, K. Altenmüller, M. Arenz, M. Babutzka, J. Barrett, S. Bauer, M. Beck, A. Beglarian, J. Behrens, T. Bergmann, et al., "Improved upper limit on the neutrino mass from a direct kinematic method by KATRIN", Physical review letters, vol. 123, no. 22, p. 221 802, 2019.

[22] S. Mertens et al. *A novel detector system for KATRIN to search for keV-scale sterile neutrinos. Journal of Physics G: Nuclear and Particle Physics*, 46(6):065203, 2019.

[23] S. Mertens et al. *Sensitivity of next-generation tritium beta-decay experiments for keV-scale sterile neutrinos. Journal of Cosmology and Astroparticle Physics*, 2015(02):020–020, 2015.

[24] M. Gugiatti et al. *Characterisation of a silicon drift detector for high-resolution electron spectroscopy. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 979:164474, 2020.

[25] P. Trigilio, L. Bombelli, M. Carminati, R. Bisognin, A. Grande, M. Gugiatti, C. Fiorini, P. Lechner, T. Brunst, and S. Mertens, *ETTORE: a 12-Channel Front-End ASIC for SDDs with Integrated JFET, in 2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC), IEEE*, 2018, pp. 1–4.

[26] P. Trigilio et al. *ETTORE: a 12-Channel Front-End ASIC for SDDs with Integrated JFET. In 2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC)*, pages 1–4, 2018.

[27] Kai Dolde et al. "Impact of ADC non-linearities on the sensitivity to sterile keV neutrinos with a KATRIN-like experiment". In: Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 848 (2017), pp. 127–136 (cit. on pp. 6, 39).

[28] A. Brunero. *Experimental characterization of an SDD-based monolithic multichannel detection module for the TRISTAN project.* Master's thesis, Politecnico di Milano, 2020. http://hdl.handle.net/10589/166352.

[29] M. Gugiatti et al. *Towards the TRISTAN detector: Characterization of a 47-pixel monolithic SDD array. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 1025:166102, 2022.

[30] M. Gugiatti, "Development of a Large-matrix SDD-based Radiation Detector for Beta-decay Spectroscopy in Neutrino Physics", Ph.D. dissertation, Politecnico di Milano, 2021.

[31] 'LT1964 Datasheet and Product Info | Analog Devices'. https://www.analog.com/en/products/lt1964.html.

[32] 'LT1763 Datasheet and Product Info | Analog Devices'. https://www.analog.com/en/products/lt1763.html.

[33] 'R-78C-1.0 Series - DC/DC, Single Output, THT | RECOM'. https://recom-power.com/en/products/switching-regulators/switching-regulators-sip/rec-s-R-78C-1.0.html?4.

[34] 'DG401, DG403, DG405 Low-Power, High-Speed CMOS Analog Switches | Vishay'. https://www.vishay.com/ppg?70049.

[35] 'SN74LVC1G123 data sheet, product information and support | TI.com'. https://www.ti.com/product/SN74LVC1G123.

[36] 'OPA2990 data sheet, product information and support | TI.com'. https://www.ti.com/product/OPA2990.

[37] 'LT3090 Datasheet and Product Info | Analog Devices'. https://www.analog.com/en/products/lt3090.html.

[38] 'LT1129 Datasheet and Product Info | Analog Devices'. https://www.analog.com/en/products/lt1129.html.

[39] 'R-78B-2.0 Series - DC/DC, Single Output, THT | RECOM'. https://recom-power.com/en/products/switching-regulators/switching-regulators-sip/rec-s-R-78B-2.0.html?4.

[40] GLab S.r.l. *XGLab DANTE: The Digital Pulse Processor for X-Ray Spectroscopy*. https://www.xglab.it/products/dante/.

[41] U. Fano. *Yield of Radiations. II. The Fluctuations of the Number of Ions. Phys. Rev.*, 72:26–29, 1947.

[42] R. C. Alig, S. Bloom, and C. W. Struck. *Scattering by ionization and phonon emission in semiconductors. Phys. Rev. B*, 22:5565–5582, 1980.

[43] P. King, G. Torrisi, M. Gugiatti, M. Carminati, S. Mertens, and C. Fiorini. *Kerberos: a 48-Channel Analog Processing Platform for Scalable Readout of Large SDD Arrays. In 2019 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, pages 1–3, 2019.

[44] P. King, "Development of a multi-channel analog pulse processing and data acquisition system for the TRISTAN detector", Politecnico di Milano, 2021.

[45] F. Schembari, R. Quaglia, G. Bellotti, and C. Fiorini. SFERA: *An Integrated Circuit for the Readout of X and γ-Ray Detectors. IEEE Transactions on Nuclear Science*, 63(3):1797–1807, 2016.

[46] P. King, M. Gugiatti, et al. *Design and characterization of Kerberos: a 48-channel analog pulse processing and data acquisition platform. Journal of Instrumentation*, 16(07):T07007, 2021.

[47] 'Analog System Lab Kit Pro'. https://university.ti.com/en/faculty/teaching-materials-and-classroom-resources/ti-based-teaching-kits-for-analog-and-power-design/analog-system-lab-kit-pro.

[48] 'Moku:Go', Liquid Instruments. https://www.liquidinstruments.com/products/hardware-platforms/mokugo/ (accessed Mar. 15, 2022).

[49] 'TL082 datasheet | TI.com'. https://www.ti.com/document-viewer/TL082/datasheet/GUID-EC824372-78D6-4A89-9886-C946D053EE50#TITLE-SLOS081SLOS0812026 (accessed Mar. 15, 2022).

[50] G. Bertuccio et al. *X-Ray Silicon Drift Detector-CMOS Front-End System with High Energy Resolution at Room Temperature. IEEE Transactions on Nuclear Science*, 63:400–406, 2016.

[51] G. Utica et al. ARDESIA-16: *a 16-channel SDD-based spectrometer for energy dispersive X-ray fluorescence spectroscopy. Journal of Instrumentation*, 16(07):P07057, 2021.

[52] S. Wüstling, T. Armbrust, M. Steidl, and S. Zadorozhny. *A large, 64-pixel PIN-diode detector for low-energy beta-electrons. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 568(1):382–387, 2006.

[53] H. Zhang et al. *Application of a silicon drift detector to measuring internal conversion electrons and analysis of their spectra. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 950:162941, 2020.

[54] C. E. Cox, S. J. Asztalos, W. Hennig, and W. K. Warburton. *Electron response in windowless Si(Li), SDD and PIN diode photodetectors. In 2011 IEEE Nuclear Science Symposium Conference Record*, pages 2074–2080, 2011

[55] 'X-Ray Attenuation Length'. https://henke.lbl.gov/optical_constants/atten2.html (accessed Mar. 24, 2022).

[56] T. Brunst. *First generation prototype detectors for the TRISTAN project*. Dissertation, Technische Universitat Munchen, 2020.

[57] R. F. Dashen, "Theory of electron backscattering", Physical Review, vol. 134, no. 4A, A1025, 1964.

[58] E. W. J. Mitchell, J. W. Mitchell, and N. F. Mott, 'The work functions of copper, silver and aluminium', *Proc. R. Soc. Lond. Ser. Math. Phys. Sci.*, vol. 210, no. 1100, pp. 70–84, Dec. 1951, doi: 10.1098/rspa.1951.0231.

[59] 'KF Components'. https://www.vacom.net/en/products/standard-components/kf-components.html (accessed Mar. 25, 2022).

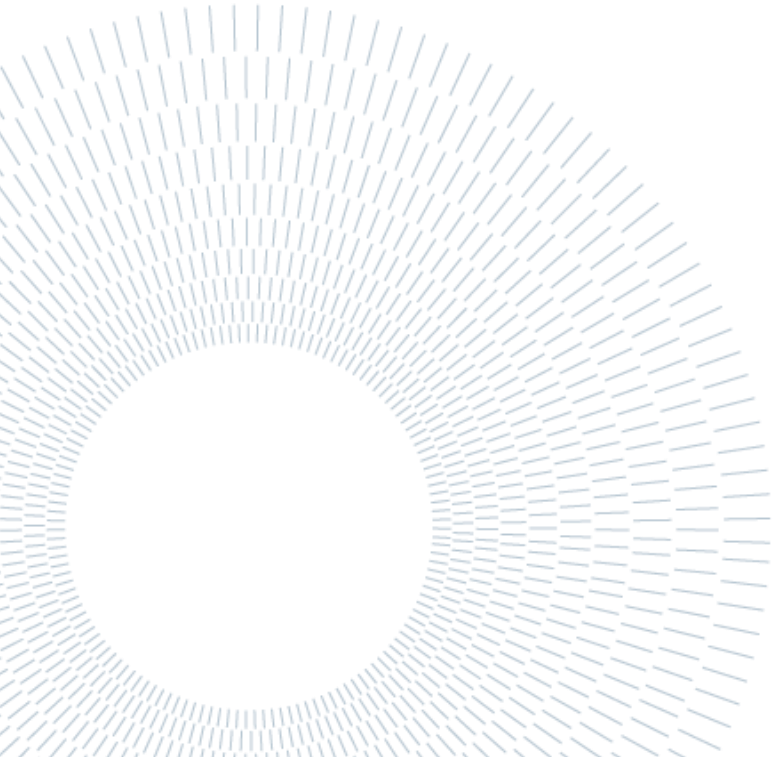
[60] 'Fittings | Swagelok'. https://products.swagelok.com/fittings/c/100?clp=true (accessed Mar. 25, 2022).

[61] 'DT5743 - 8 Channel 12bit 3.2 GS/s Switched Capacitor Digitizer', *CAEN - Tools for Discovery*. https://www.caen.it/products/dt5743/ (accessed Mar. 25, 2022).

[62] 'Fischer Connectors - Product Finder - DBPE 105 A102-130'. https://my.fischerconnectors.com/products/104503 (accessed Mar. 25, 2022).

[63] 'Fischer Connectors - Product Finder - S 105 A102-130+'. https://my.fischerconnectors.com/products/104457 (accessed Mar. 25, 2022).

List of Figures



List of Tables