EXECUTIVE SUMMARY OF THE THESIS
Parallel connected inverters' Common-mode Voltage Reduction for applications in energy storage systems

TESI MAGISTRALE IN Electrical ENGINEERING – INGEGNERIA Elettrica

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1. Introduction

Conventional two-level and three-level voltage source inverters (VSI) are widely used in power applications such as renewable energy sources, uninterrupted power supplies (UPS), variable speed drives etc. Two level NPC inverters are common mainly for low voltage applications and three-level inverter more for medium and high voltage applications. The prevalence of these topologies is due to their simplicity, low cost, and high flexibility. They are also mainly used in parallel connection of the inverters to improve the performance of the system as parallel connected inverters provides more stability over a single centralized inverter. However, parallel connection gives rise to many problems such zero sequence circulating currents, poor CMV, parasitic capacitance etc. In [1], it is discussed that CMV is a source of excitation for ZSCC and by reducing the latter, it is possible to decrease the former. Traditionally, hardware solutions have shown effectiveness in terms of CMV and ZSCC like use of common mode inductances [2]. However, as the power increases these solutions become less effective. Ever since, the use of software solutions to target the problems has become dominant like modified PWM techniques and appropriate control systems.

PWM techniques has been widely used to achieve variable voltage and variable frequency in DC/AC and AC/DC converters and different applications such as variable speed drives, uninterrupted power supplies etc. Traditionally, PWM techniques can be classified into space vector PWM and Sinusoidal PWM. As the main goal of any modulation is to obtain a variable output with the maximum fundamental component with minimum harmonics, the SVPWM technique is preferred for higher efficiencies.

Although SVPWM, provides satisfactory results in terms of desired outputs/inputs, poor CMV characteristics are generated. In general, CMV is defined as the potential between the star point of the load and the ground and can be written as v_{cm}

= (va+ vb+ vc)/3. The CMV ranges from $\pm$Vdc/6 to $\pm V$dc/2. This causes CMV with sharp edges that can result in leakage currents. In this thesis, different SVPWM techniques has been used to reduce the CMV in both two-level and three-level inverters and the effect on the ZSCC and the percentage of the reduction and at last the THD is analyzed in case of parallel connected inverters and the results are compared with the traditional SVPWM for each topology. For each modified SVPWM method, the tests with different frequencies and different connections of the DC bus (different DC bus, same DC bus) and different frequencies between the two parallel inverters are carried out and, in each condition, the effectiveness of the method is verified.

2.   Two-level inverter

The conventional two-level SVPWM, Figure 1, of the three-phase VSI utilizes two neighboring active space vectors in each sector with the conjunction of the zero vectors to obtain the reference vector, $\bar{\bar{V}}^* = Me^{j\vartheta}$. For example, if $\bar{V}^*$ is in sector A1, then the vectors $\bar{V}1$ and $\bar{V}2$ are utilized as shown in the Figure 2:
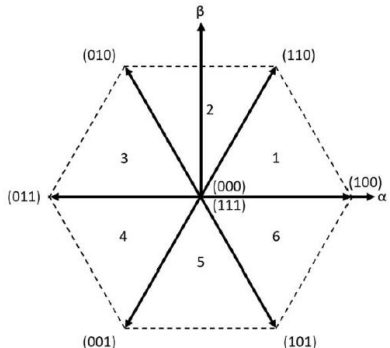

Figure 1-SVPWM,2L inverter

The reference vector is synthesized with the vectors as:

$V_{ref} = V_1 t_1 + V_2 t_2 + V_z t_z$ (2-1)

$T_c = t_1 + t_2 + t_z$ (2-2)

And Tc is the period of PWM which is divided between the zero vectors (000) and (111).
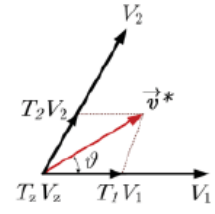

Figure 2- reference voltage in the sector 1

The common mode voltage on the output of the inverter depends on the switching state of the inverter. If a basic schematic of two-level inverter is considered in Figure 3, the corresponding CMV for each switching state is summarized in the Table 1.
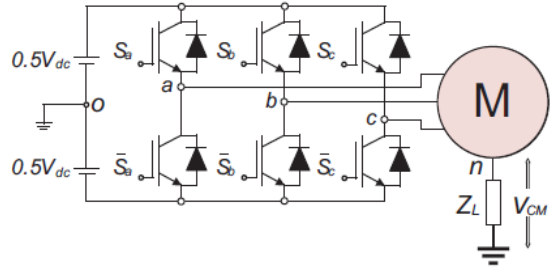

Figure 3-Basic schematic of 2L inverter

Table 1.Inverter switching states and related CMV magnitude

Switching state			Phase Voltage			CMV
A	B	C	Van	VBn	VCn	
0	0	0	1/2Vdc	1/2Vdc	1/2Vdc	1/2Vdc
1	0	0	1/2Vdc	1/2Vdc	1/2Vdc	-1/6Vdc
1	1	0	1/2Vdc	1/2Vdc	1/2Vdc	1/6Vdc
0	1	0	1/2Vdc	1/2Vdc	1/2Vdc	1/6Vdc
0	1	1	1/2Vdc	1/2Vdc	1/2Vdc	1/6Vdc
0	0	1	1/2Vdc	1/2Vdc	1/2Vdc	1/6Vdc
1	0	1	1/2Vdc	1/2Vdc	1/2Vdc	1/6Vdc
1	1	1	1/2Vdc	1/2Vdc	1/2Vdc	+1/2Vdc

According to the Table.1, the highest peak of the CMV corresponds to the zero vectors. Therefore, by modifying the way the reference voltage is synthesized in the SVPWM, the CMV can be reduced. The method that is explored is called Active Zero State PWM (AZSPWM) [3]. In this method, the two zero vector are replaced by the opposite active vectors with equal times of

applications [3]. The selected sectors instead of V_0 and V_7 are V_3 and V_6 as illustrated in Figure 4.
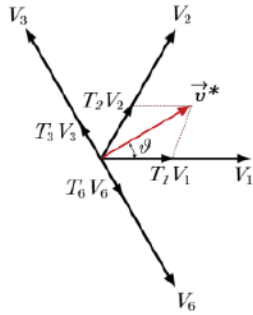

Figure 4-AZSPWM vector selection, sector 1

Therefore, the reference voltage can be written as:

$$V_{ref} = V_1 t_1 + V_2 t_2 + V_3 t_3 + V_6 t_6 \quad (2\text{-}3)$$

$$T_c = t_1 + t_2 + t_z \quad (2\text{-}4)$$

$$T_z = t_3 + t_6 \quad (2\text{-}5)$$

It has been observed that by this method the peak of CMV is reduced by $\pm V_{dc}/6$ in Figure 5. In the Figure 5, two inverters are connected in parallel, the bottom one with modulated with the conventional SVPWM and the top one with AZSPWM and as it is shown the inverter with AZSPWM produces lower CMV compared to the conventional one.
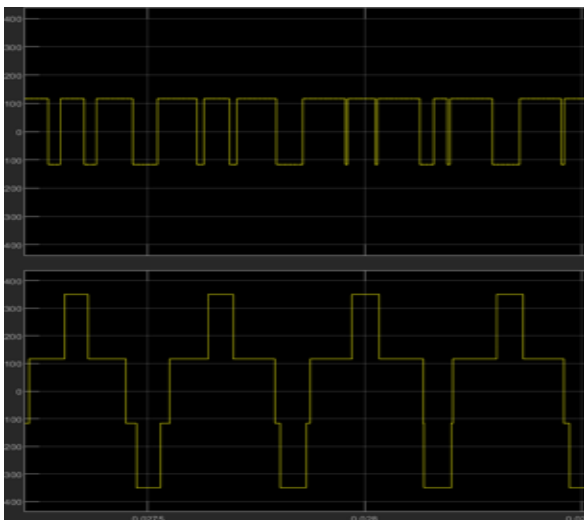

Figure 5-CMV comparison between AZSPWM and conventional SVPWM

It has been observed that the PI controllers were still able to track the desired set point and the current delivered to the grid is the sum of the currents of two inverters.
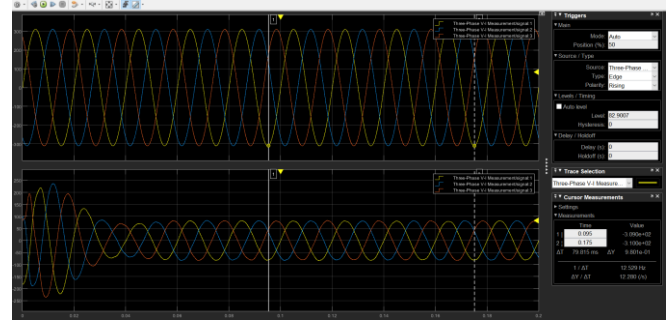

Figure 6-voltage and currents on the grid side

The THD measured in this method is slightly higher than the conventional method but still complies with the grid requirements.

Table 2.THD comparison between AZSPWM and conventional SVPWM

Objective	Condition	THD of Current delivered to the grid
Conventional PWM method	Different DC Bus	1.26%
AZSPWM method		2.11%

As stated before, the CMV is a source of excitation for the ZSCC. The ZSCC is measured in through the parasitic capacitance connected to the negative poles of the DC bus towards the ground and a decrease in the average of the ZSCC is observed which is summarized in the Table.3.

Table 3.ZSCC comparison between AZSPWM and Conventional SVPWM

Objective	Condition	ZSCC
Conventional PWM method	Different DC Bus	<10
AZSPWM method		<8

The method has been tested different situations with different frequencies and same/different DC buses and the effectiveness is verified.

3. Three-level inverter

The conventional three-level SVPWM has 4 switches per leg and two free-wheeling diode per leg. This results in the division of each sector into 4 regions as shown in the Figure 7.
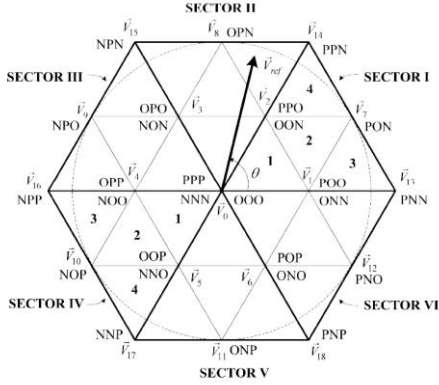

Figure 7-SVPWM,3L inverter

At any given time, the reference voltage is synthesized with the three nearest vectors. If the sector 1 and region 3 is considered, the reference is synthesized with three nearest vectors, which are $\bar{V}_1$, $\bar{V}_2$ and $\bar{V}_7$:
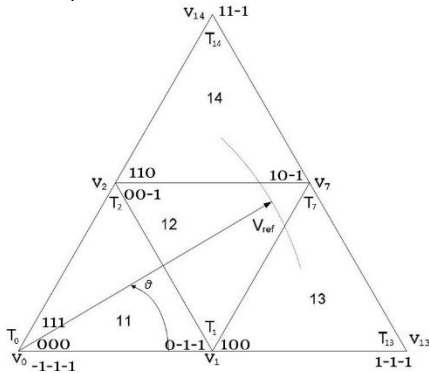

Figure 8-SVPWM vector selection for sector 1, region3

$$\bar{V}_{ref} \cdot T_s = \bar{V}_1 \cdot T_1 + \bar{V}_2 \cdot T_2 + \bar{V}_7 \cdot T_7 \text{(3-1)}$$

$$Tc = T_1 + T_2 + T_7 \text{ (3-2)}$$

In the three-level SVPWM, the vectors can be categorized into zero, small, medium, and large vectors and their related CMV magnitudes are shown in the table below:

Table 4-3L inverter vectors and their corresponding magnitude

Vectors	Switching states	CMV
Zero vectors	OOO	0
	PPP	Vdc/2
	NNN	-Vdc/2
Small vectors	POO, OOP, OPO	Vdc/6
	PPO, POP, OPP	Vdc/3
	ONN, NNO, NON	-Vdc/3
	OON, ONO, NOO	-Vdc/6
Medium vectors	PON, OPN, NPO	0
	NOP, ONP, PNO	
Large vectors	PPN, NPP, PNP	Vdc/6
	PNN, NPN, NNP	-Vdc/6

It can be seen that CMV corresponding to the zero vector (OOO) and medium vectors is zero.
To reduce the CMV and consequently ZSCC, proper combination of the vectors can be utilized. In this thesis, two possible solutions are explored.

3.1. MV3

As previously stated in the Table.4, the CMV corresponding to the medium vectors is zero. In this method, which is called MV3[4], three nearest vectors are used to synthesize the reference voltage as shown in the Figure below for sector 1:
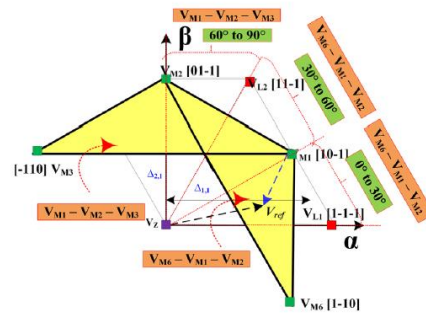

Figure 9- MV3, sector 1 vector selection

The reference voltage then can be written using $\bar{V}_{12}$, $\bar{V}_7$, $\bar{V}_8$:

$$\bar{V}_{ref} \cdot T_s = \bar{V}_{12} \cdot T_{12} + \bar{V}_7 \cdot T_7 + \bar{V}_8 \cdot T_8 \text{ (3-3)}$$

$$T_c = t_{12} + t_7 + t_8 \text{ (3-4)}$$

The effectiveness of this model is verified by Simulink. The measured CMV by this method is approximately zero as shown in the Figure 10. The two inverters are connected in parallel. The upper waveforms show the CMV of the inverter with conventional method and the lower waveform shows the CMV of the second inverter using MV3 method.
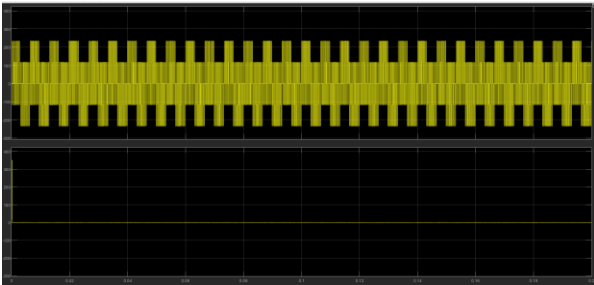

Figure 10- CMV output between two parallel connected inverters, one using the conventional SVPWM the other with MV3

The THD is measured for the current delivered to the grid which is the sum of the currents of two inverters. As it is shown in the Table.5 and the Figure 11, THD still satisfies the grid requirements but still higher compared with the conventional method.
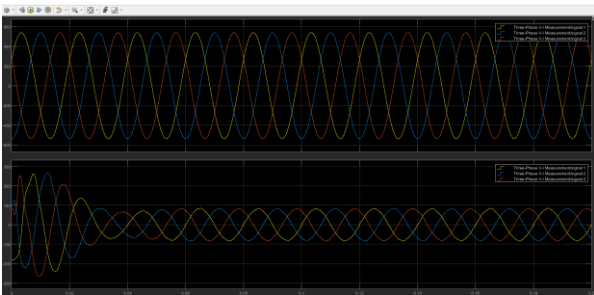
Figure 11-Output voltage and currents on the grid side

Table 5-THD comparison between MV3 method and conventional method,3L inverters

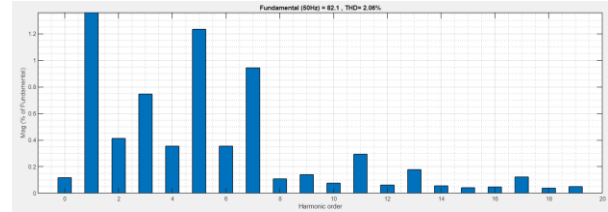| Objective	Condition	Current delivered to the grid
THD of Conventional PWM method	Different DC Bus	1.77%
THD of MV3 PWM method		2.06%

Figure 12-FFT analysis of grid currents using MV3 method

As stated before, CMV is a source of excitation for ZSCC. A difference between frequencies is imposed to cause ZSCC and measured it through the parasitic capacitance.

Table 6- ZSCC comparison between two parallel inverters using conventional and MV3 method,3L inverter

Objective	Condition	ZSCC
Conventional PWM method	Different Frequency	<4
MV3 PWM method	Different DC Bus	<0.02

It is observed that the ZSCC is reduced drastically since the CMV reduction was dramatic.

The effectiveness of this model is tested in different situations using the same DC bus and frequency conditions and verified.

3.2 LMZV

Since in the previous method the modulation range is only limited to the medium vectors, a huge part of hexagon is lost. To reduce the CMV but not to sacrifice much of the modulation ratio, LMZV method can be used [5]. In this method, the hexagon is divided into 12 sectors instead of 6 and the reference voltage is synthesized with the nearest medium, large and zero vector (OOO).
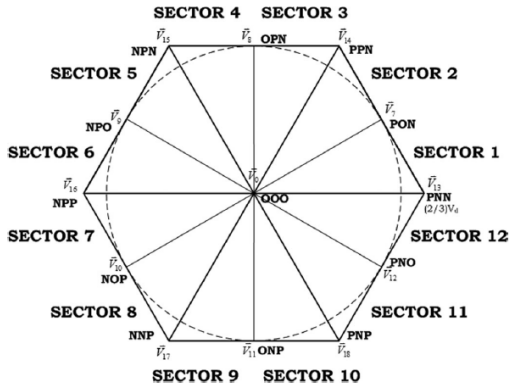
Figure 13-LMZV PWM

The reference voltage in sector 1 is synthesized with the vectors $\bar{V}_{13}$, $\bar{V}_7$, $\bar{V}_0$ and the reference voltage can be written as:

$$\bar{V}_{ref} \cdot T_s = \bar{V}_{13} \cdot T_{13} + \bar{V}_0 \cdot T_0 + \bar{V}_7 \cdot T_7 \quad (3\text{-}5)$$
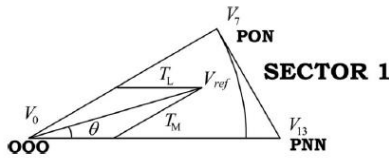
$$T_c = t_{13} + t_7 + t_z \quad (3\text{-}6)$$

Figure 14- Vector selection for LMZV

The effectiveness of this model is verified by Simulink. The measured CMV by this method is approximately half of the conventional SVPWM as shown in the Figure 14. The two inverters are connected in parallel. The upper waveforms show the CMV of the inverter with conventional method and the lower waveform shows the CMV of the second inverter using LMZV method.
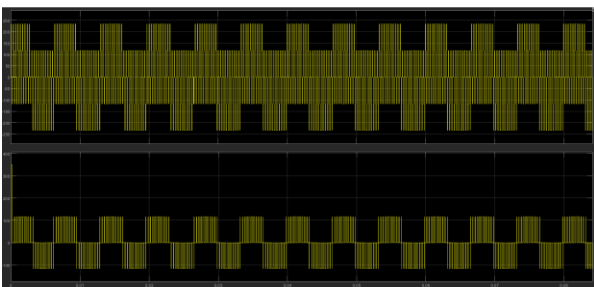

Figure 15-Output CMV of two parallel inverters using the conventional and LMZV PWM

The THD is measured for the current delivered to the grid which is the sum of the currents of two inverters. As it is shown in the Table.7 and the Figure 11, THD still satisfies the grid requirements but still higher compared with the conventional method.
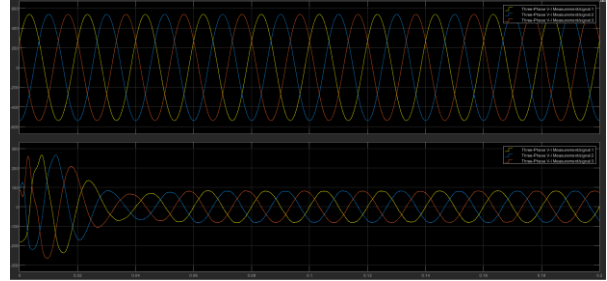

Figure 16-Output voltage and currents on the grid side

Table 7-THD comparison between conventional SVPWM and LMZV method

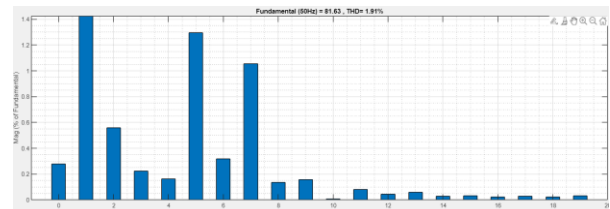| Objective	Condition	Current delivered to the grid
THD of Conventional PWM method	Different DC Bus	1.77%
THD of LMZV PWM method		1.91%

Figure 17-FFT analysis of grid currents of two parallel connected inverters with LMZV

It is observed that the THD of parallel connected inverters in case of using the LMZV method is slightly higher compared to the conventional method but still satisfies grid codes.

The ZSCC as previous chapters is measured through the parasitic capacitance. The ZSCC is

slightly reduced but not as much as using MV3 method.

Objective	Condition	ZSCC
Conventional PWM method	Different DC Bus	<4
LMZV PWM method		<3

All the measurements are repeated with differences in the frequency and same DC buses and the effectiveness is verified.

4. Equivalent zero sequence model of two parallel connected inverters

In this chapter, the procedure taken to model the zero-sequence model of the two parallel inverters is explained for the two-level inverter.
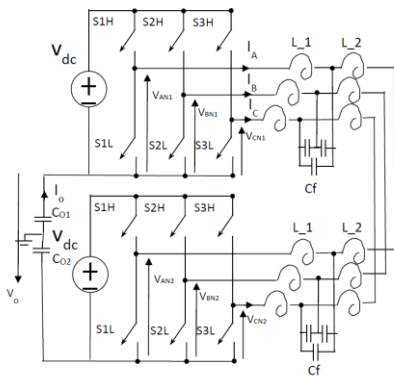
Figure 18-Two inverters in parallel

From the homopolar point of view the capacitance C_f does not appear. So that the LCL filter equivalence would be L_1 and L_2 in series with each other, L_{tot} the total inductance of a phase is: L_1+L_2+L_2+L-1 = 2*(L_1+L_2). The KVL can be applied to each phase and sum of them would be:

$$V_{AN1} + V_{BN1} + V_{CN1} - L_{tot}\frac{d(I_A+I_B+I_C)}{dt} - V_{AN2} - V_{BN2} - V_{CN2} - 3V_O = 0 \,(4\text{-}1)$$

And if the homopolar current is identified as: I_o = I_A+ I_B+ I_C and taking into the consideration the CMV definition using equation (4-1):

$$3V_{O1} - 3V_{O2} = L_{tot}C_O \frac{d^2V_O}{dt^2} + 3V_O (4\text{-}2)$$

Where V_{O1} and V_{O2} are CMV of the inverter 1&2.

If you consider $L_{eq}=L_{tot}/3$

$$V_{O1} - V_{O2} = L_{eq}C_O \frac{d^2V_O}{dt^2} + V_O (4\text{-}3)$$

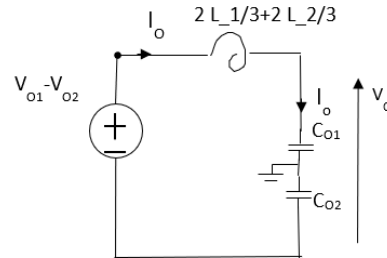the dynamic equation (4-3) is the same as the following circuit:

Figure 19- Equivalent zero sequence model of two parallel connected inverters

The same procedure can be done for three-level inverters.

5. Conclusions

Parallel connection of inverters comes with problems such as poor CMV and ZSCC. Traditional methods of PWM are not able to reduce these phenomena and modifications have been to SVPWM to reduce CMV and followingly ZSCC both for two and three level inverters. The CMV corresponding to each switching state is obtained and actions has taken place accordingly. For two level inverters, AZSPW is used and the CMV is reduced by half. A decrease in ZSCC is also seen. For three-level inverter, two methods have been used. First, MV3 method which reduces the CMV to zero and drastically reduces ZSCC as well. Second, LMVZ method is explored which has a higher modulation range compared to MV3 and reduces CMV by half. A slight decrease is also seen in the ZSCC.

In all the methods mentioned, the current injected to the grid by two parallelly-connected inverters has an acceptable THD which complies with the grid codes but still higher than the traditional method in both two and three level topologies. All the methods were tested with different frequencies and DC bus connections and the results have been verified.

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PARALLEL CONNECTED INVERTERS' COMMON-MODE VOLTAGE REDCUTION FOR APPLICATIONS IN ENERGY STORAGE SYSTEMS

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$$\underline{N\,H\,\Omega\,A}$$

ABSTRACT

This thesis deals with the problems that arise by parallel connection of inverters with the focus mainly on the reduction of the common mode voltage. It has been observed that common mode voltage is a source of excitation for the zero sequence circulating currents as well. The thesis is developed first with single grid connected two-level and three-level inverter using conventional SVPWM and then as the next step two scenarios are considered: 1) two inverters directly connected on the AC side and separated on the DC bus. 2) inverters are directly connected both on AC and DC side.

As the easiest solutions to reduce the common mode voltage is using passive filters and transformers to reduce the zero sequence circulating currents can be numbered. However, these hardware solutions are cost intensive and requires lots of space as the power rating increases.

In this thesis, different software approaches regarding the reducing the common mode voltage has been taken. Depending on the objective, proper combination of the vectors can reduce the CMV. Modified SVPWMs comes with more degrees of freedom to implement as the level of inverters increases but the computational burden increases as well.

In this thesis, the modification of the vectors was so that the vectors contributing the most to the producing the common mode voltage were replaced by the proper neighboring vectors and the effect of the latter has been studied on the common mode voltage and the also circulating currents. During each technique, the output currents delivered to the grid and the level of its THD is monitored to verify the grid requirements. The ZSCC is measured through the parasitic capacitance caused by the PV systems and the proper LCL filter and control systems have been designed according to the objective.

key words: common-mode voltage, zero sequence circulating currents, parallel connection, SVPWM

ABSTRACT IN LINGUA ITALIANA

Questa tesi affronta i problemi che sorgono dal collegamento in parallelo di inverter con particolare attenzione alla riduzione della tensione di modo comune. È stato osservato che la tensione di modo comune è una fonte di eccitazione anche per le correnti circolanti di sequenza zero. La tesi viene sviluppata prima con inverter a due livelli e tre livelli collegati alla rete singola utilizzando SVPWM convenzionale e quindi come passaggio successivo vengono considerati due scenari: 1) due inverter collegati direttamente sul lato AC e separati sul bus DC. 2) gli inverter sono collegati direttamente sia sul lato AC che DC.

Poiché la soluzione più semplice per ridurre la tensione di modo comune consiste nell'utilizzare filtri passivi e trasformatori per ridurre la sequenza zero, le correnti circolanti possono essere numerate. Tuttavia, queste soluzioni hardware sono costose e richiedono molto spazio all'aumentare della potenza nominale.

In questa tesi sono stati adottati diversi approcci software per quanto riguarda la riduzione della tensione di modo comune. A seconda dell'obiettivo, una corretta combinazione dei vettori può ridurre il CMV. Gli SVPWM modificati offrono più gradi di libertà da implementare all'aumentare del livello degli inverter, ma aumenta anche il carico di calcolo.

in questa tesi, la modifica dei vettori è stata tale che i vettori che contribuiscono maggiormente alla produzione della tensione di modo comune sono stati sostituiti dai vettori propri vicini ed è stato studiato l'effetto di questi ultimi sulla tensione di modo comune e anche le correnti circolanti. Durante ciascuna tecnica, le correnti di uscita immesse in rete e il livello del suo THD vengono monitorati per verificare i requisiti di rete. Lo ZSCC viene misurato attraverso la capacità parassita causata dai sistemi fotovoltaici e il filtro LCL e i sistemi di controllo adeguati sono stati progettati in base all'obiettivo.

Parole chiave: tensione di modo comune, correnti circolanti a sequenza zero, collegamento in parallelo, SVPWM

CONTENTS

1 INTRODUCTION:

Energy is the forcing drive to move forward to the future. As the fossil fuels become scarcer and the human society become more conscious with its footprint, new policies are being adopted to reduce the GHG emissions.

Factors impacting these considerations are a) energy demand in both developing and developed countries b) large CAPEX for building new centralized power plants c) insufficient power generation in some regions d) and the last but not the least, climate change. Therefore, the renewable energy sources like solar energy, wind turbines, biogas etc., are the part of the prospective of the future power generation. [1-2]

The new trend is developing towards distributed power generation (DG), which means that energy conversion plants are close to the consumer. For the consumer, it reduces the cost, higher service reliability, high power quality, increase the efficiency and energy Independence are all great Importance in all sectors [3].

In most of the sources mentioned, there should be a way to alternate direct current to AC as the power generated Is DC [4].

So, inverters are an essential component at the grid side due to a wide range of applications they have. Besides alternating the current from DC/AC or vice versa, they provide support also to the grid from peak shaving to handling the electricity variations caused by generators variation and loads.[5]

Inverters are often paralleled to construct power systems to improve performance or to achieve a high system rating. Parallel operation of inverters offers also higher reliability over a single centralized source because in case one inverter fails the remained (n−1) modules can deliver the needed power to the load. This is as well driven by the increase of renewable energy sources such as photovoltaic and wind.

There are many control techniques to parallel inverters which are already suggested in the literature, they can be categorized to the following main approaches:

- master/slave control techniques, current/

- power sharing control techniques and frequency and voltage

- droop control techniques.

PWM techniques has been widely used to achieve variable voltage and variable frequency in DC/AC and AC/DC converters and different applications such as variable speed drives, uninterrupted power supplies etc.

The classical square wave inverter used in low or medium power applications suffers from a serious disadvantage such as lower order harmonics in the output voltage. One of the solutions to enhance the harmonic free environment in high power converters is to use PWM control techniques. The objective of PWM techniques was to fabricate a sinusoidal AC output whose magnitude and frequency could both be restricted.

Traditionally, PWM techniques can be classified into space vector PWM and Sinusoidal PWM. SVPWM shows advantages over SPWM as it utilizes the DC bus voltage more and provide lesser THD. As the main goal of any modulation is to obtain a variable output with the maximum fundamental component with minimum harmonics, the SVPWM is explored in this thesis work to maximize the capacity of the delivered power from the renewable source or the battery storage systems for higher efficiency and lower emissions while connecting the inverters in parallel to each other. Modified methods of SVPWM have been explored to target the problems arise by the parallel connection of inverters such as AZSPWM, MV3, LMZV to minimize the effects of parallelization of inverters.

2   LITERATURE REVIEW

Parallel connection of inverters provides many economical and technical benefits for both the DS as well as the consumer.

When connecting inverters in parallel, the systems reliability and capacity will increase. Comparing the central inverters to the string inverters in case of solar farms, central inverters have one single failure point which decrease the reliability of the system and in case of fault, there would be the outage of the whole system which causes a huge economic burden. On the other hand, the string inverters are more reliable as one faulty inverter doesn't result in the outage of the whole system.

2.1   Principle of parallel operation:

For the stable operation, the balance between the active power (P) and reactive power (Q) is essential. The real and reactive power flow is described as following [6] and figure (1):
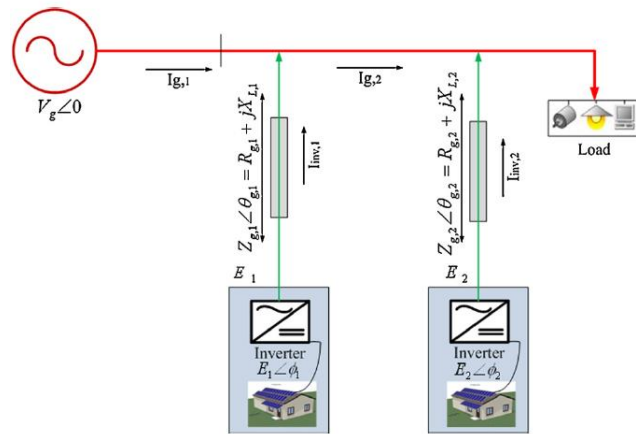
Figure 1-Equivalent circuit of power inverters connected to the grid

$$P_1 = [(\frac{E_1 V_g \cos \phi_1}{Z_{g,1}} - \frac{V_g^2}{Z_{g,1}}) \cos \theta_{g,1} + \frac{E_1 V_g}{Z_{g,1}} sin\phi_1 sin\theta_{g,1}] \qquad (2\text{-}1)$$

$$Q_1 = [(\frac{E_1 V_g \cos \phi_1}{Z_{g,1}} - \frac{V_g^2}{Z_{g,1}}) \sin \theta_{g,1} + \frac{E_1 V_g}{Z_{g,1}} sin\phi_1 sin\theta_{g,1}] \qquad (2\text{-}2)$$

Since the output impedance of the inverter is very low, any change in Φ_1 (the phase difference between the inverter and the grid) could result in a very large output imbalance. Therefore, it is strictly important for the inverters connected in parallel to be in phase with the grid. E_1 and V_g represent the inverter output voltage and grid voltage.

An inverter has an overload capacity of only 150-200 percent, and if the output current exceeds this limit, even for a fraction of a cycle, this will result in a commutation failure or in damage of the valve devices.

There are many different configurations of an inverter circuit with various operating principles and each characteristics has its own pros and cons. [7]

However, there are some constraints on parallel connections of the inverters:

1. Circulating currents

2. parasitic capacitance

3. common mode voltage

In this section, each problem will be discussed in detail.

2.2   Circulating currents

Ideally, each inverter has the same magnitude, frequency, and phase in the output but in real world it is not possible to achieve this situation. In real world applications, there would be a mismatch in each inverter output due to inaccuracy of each. This would result in the circulating currents flowing between parallel inverters [8].

In [9], even without uniform modulation there would be circulating currents flowing between parallel inverters.

In [10], the circulating currents are considered as the negative of the difference between the average currents in the system and outputs of the inverters considering two inverters in parallel.

In the figure (2), equivalent circuit of a parallel inverter is shown. I_1 and I_2 are defined as the output currents of the inverters.
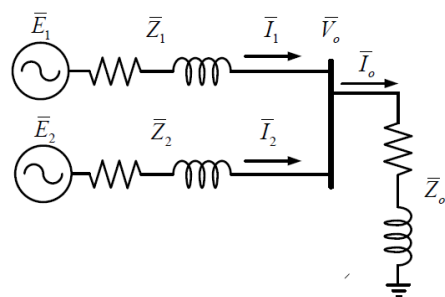

Figure 2-Two parallel inverters

$$\bar{I}_1 = \frac{\bar{E}_1 - \bar{V}_0}{\bar{Z}_1} = \frac{\bar{U}_{\Delta 1}}{\bar{Z}_1} \qquad (2\text{-}3)$$

$$\bar{I}_2 = \frac{\bar{E}_2 - \bar{V}_0}{\bar{Z}_2} = \frac{\bar{U}_{\Delta 2}}{\bar{Z}_2} \qquad (2\text{-}4)$$

The calculation can be done based on which way the circulating currents are seen. The circulating current seen by inverters 1 and 2 are given by:

$$\bar{I}_{H1} = \frac{\bar{I}_1 - \bar{I}_2}{2} \qquad (2\text{-}5)$$

$$\bar{I}_{H2} = \frac{\bar{I}_2 - \bar{I}_1}{2} \qquad (2\text{-}6)$$

The average output current is:

$$\bar{I}_{avg} = \frac{\bar{I}_1 + \bar{I}_2}{2} \qquad (2\text{-}7)$$

The difference between the output current of each inverter and the average current is the circulating currents.

$$\bar{I}_1 - \bar{I}_{avg} = \frac{2\bar{I}_1 - \bar{I}_2 - \bar{I}_1}{2} = \frac{\bar{I}_1 - \bar{I}_2}{2} = \bar{I}_{H1} \quad (2\text{-}8)$$

$$\bar{I}_2 - \bar{I}_{avg} = \frac{2\bar{I}_2 - \bar{I}_1 - \bar{I}_2}{2} = \frac{\bar{I}_2 - \bar{I}_1}{2} = \bar{I}_{H2} \quad (2\text{-}9)$$

In [6], the circulating currents is given for N parallel-connected inverters.

$$\bar{I}_k = \frac{\bar{E}_k - \bar{V}_0}{\bar{Z}_k} = \frac{\bar{U}_{\Delta k}}{\bar{Z}_k} \ (k = 1,2,\dots,N) \quad (2\text{-}10)$$

where I_k, E_k and Z_k are the output current, output voltage and system Impedance of the Kth inverter. The average output current is given by:

$$\bar{I}_{avg} = \frac{\sum_j^N \bar{I}_j}{N} \quad (2\text{-}11)$$

The circulating current seen by each inverter therefore is given by:

$$\bar{I}_{Hk} = \bar{I}_k - \bar{I}_{avg} = \frac{N\bar{I}_k - \sum_j^N \bar{I}_j}{N} \ (k = 1,2,\dots,N) \ (\ 2\text{-}12)$$

In [6] also the behavior of the inverters is studied under different conditions. It can be concluded that:

- Circulating currents can arise due to the differences between in output voltage amplitude, phase, and frequency of parallel connected inverters.

- Circulating current is a current superimposed on normal power currents and is used as a tool to describe imbalance between inverters.

- Circulating current exists regardless of the load.

- At low load condition or no-load condition, circulating current can cause power exchange among parallel connected inverters. This can affect the overall control and even damage the inverter. At high load condition there would be no net power flow among the inverters. In this case, the circulating currents determines the power sharing ratio of parallel connected inverters.

To reduce the circulating currents hardware and software solutions can be taken. As in [11], the common mode inductances are used to suppress the circulating currents, but this method results in the core losses and requires bigger space and higher cost.
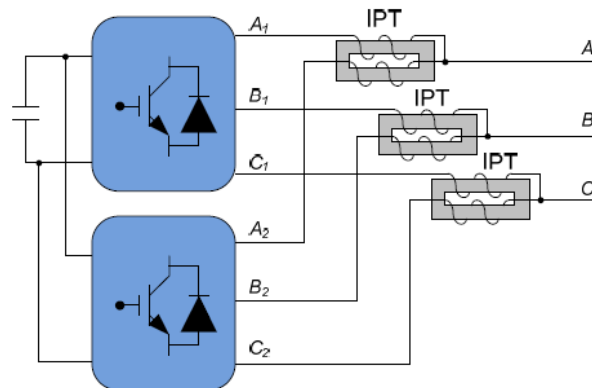
Figure 3-common mode inductance to suppress the circulating currents

For the cost and space reasons, software solutions are often preferable specially in high power applications. In [12], the difference between CMVs and NPPs are considered the source of excitation for the circulating currents. Therefore, by reducing the source of excitation through SW solutions such as PWM techniques, circulating currents will decrease as well.

2.3   Parasitic capacitance

The advantages of the PV systems are not of question for nobody. The economic and environmental impacts that they have is undeniable, however, the negative effect of the additional leakage current Is widely recognized.

As shown in the picture 3, the potential difference caused by different switching states injects leakage currents on both DC and AC sides.
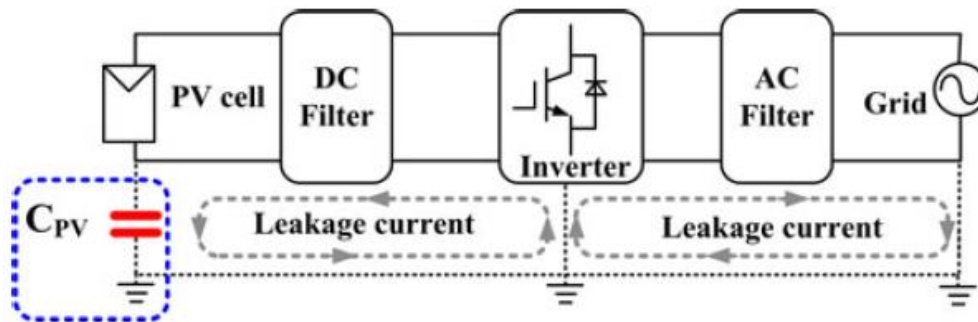

Figure 4-Simplified common mode leakage current coupling model in PV

The negative effects caused by these leakage currents are such as: electromagnetic Interference (EMI), grid current distortions, additional losses in the PV systems, harmonics injected into the grid and unsafe conditions for work. Therefore, parasitic capacitance between the PV panel and the ground is an important parameter for the estimation of the likelihood of occurrence of leakage currents during the design of a new PV generation system [13].

Over the past years there has been extensive research on the parameters of the parasitic capacitance. In [14] the PV panels is modeled as a capacitance towards the earth due to the large area of the module itself. It has been observed in [15] the occurrence of the high frequency leakage currents depends strongly on the value of the parasitic capacitance.

In [16], a detailed analysis of the Issue is given:

1. that PV panel grounding capacitance should be divided into cell to-frame capacitance, cell-ton capacitance, and cell to ground capacitance.
2. The dependence of parasitic capacitances on physical parameters such as panel frame thickness, width and length, cell to frame spacing, and solar cell tilt angle is studied.

3. A pi-shape equivalent circuit is derived to calculate the value of leakage current in the PV system. The derived mathematical expressions are relatively simple.

Therefore, parasitic capacitance in the PV systems is divided into three parts as shown in the picture 4:

1. C_{cf} : cell to the frame capacitance. Although the effective area of this capacitance is small but can't be neglected as the distance between the capacitor plates is so small.
2. C_{cr} : cell to rack capacitance. since there are many different types of the rack the value of this capacitance changes by the size and shapes of the racks.
3. C_{cg} : cell to the ground capacitor. It is believed to be the main parasitic capacitance in the PV systems since the effective surface area of this capacitance is larger than the others.
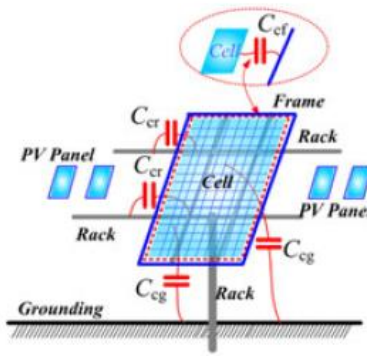
Figure 5-Capacitance modelling in PV systems

So, the total capacitance of a single PV panels can be calculated as:

$$C_{tot} = C_{cf} + C_{cr} + C_{cg} \quad (2\text{-}13)$$

Another aspect [17] that can be considered is the parasitic capacitance due to switching devices. In this aspect, Parasitic capacitance is a capacitor like phenomenon between emitter (source), drain (collector), and grid (gate) electrodes in power devices owing to packaging and electrical wiring. Grid-drain (gate-collector) and grid-source (gate-emitter) parasitic capacitances are the input capacitances of the inverter. During the turn-on and turn-off processes of the switch, gate current will charge and discharge the input capacitances, which influence the rising and falling processes of grid-source (gate-emitter) voltage, thus influencing the turn-on and turn-off delays.

2.4   Common-mode Voltage

NPC multi-level inverters are widely used in the industry and to obtain a variable voltage with variable frequencies space vector PWM (SVPWM) is widely used as the standard modulation technique. Although SVPWM provides a satisfactory operation of the input and output requirements, poor CMV is generated. CMV voltage has many down effects on the operation of the system such as leakage currents, the radiation of the electromagnetic interference noise, a faulty activation of the current detection circuit [18].

To reduce the common mode voltage, hardware and software solutions can be taken. As for the hardware approaches, one solution can be using an extra leg or passive filters [19]. However, software solutions are widely used due to lower cost and no need for the space. For two level inverters in [20], it is observed that the peak of the common mode voltage corresponds to the zero voltage so instead of synthesizing the reference voltage with the two nearest vectors and one zero vector as in conventional method, the zero vectors are neglected and instead the two neighboring vectors are used to synthesize the reference voltage (APPENDIX 7.3).
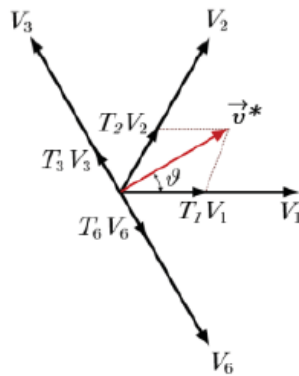
Figure 6-Reference voltage combination, AZSPWM

For three-level inverters, there are more solutions with respect to the two-level inverters as there are more switching states and more degree of freedom. The vectors can be divided into zero, small, medium, and large vectors. In [21], it is explained that CMV produced by the medium vectors is zero. So instead of using three nearest vectors to synthesize the reference voltage, three nearest medium vectors are used. In this way, the common mode voltage is zero and it affects the circulating currents also as the CMV plays as the source of excitation for the circulating currents (APPENDIX 7.5)
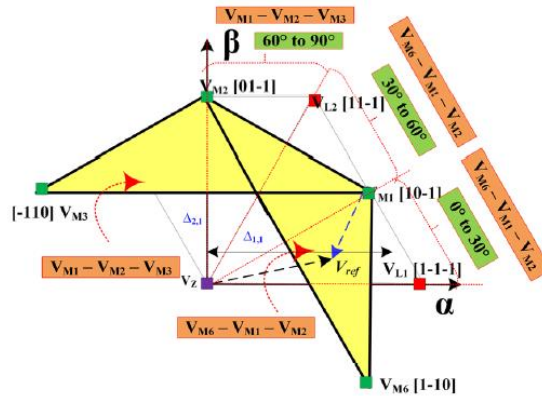
Figure 7-MV3 reference voltage combination, MV3

Another consideration that can be discussed is the switching sequence. The switching sequence is important as one switching should be executed at a time so that leakage currents reduce. In [22], the hexagon is divided into 12 sectors instead of six sectors and the reference voltage is synthesized by the nearest zero vector (OOO), large, medium vectors. The common mode voltage is reduced by half and the circulating currents are slightly decreased (APPENDIX 7.6)
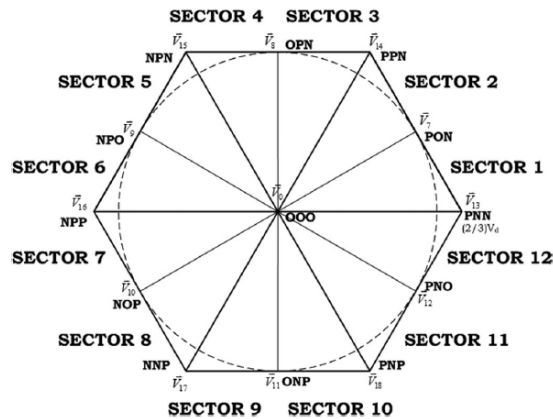

Figure 8-Reference voltage combination, LMZV

2.5   LCL Filter

Due to the harmonic content of output currents, the passive and active filters are used to reduce the ripple and higher harmonics. By means of the filter, one can smooth out the output current.

The design of the filter depends on the space available, cost, weight, volume, and total harmonics. The cost mainly depends on the number of components used for example the magnetic material used for the core of the inductance. It is important for the filter to be able to operate with some degrees of freedom from the grid parameters.

 Higher order filters can have better harmonic attenuation at lower switching frequency.

As proposed in [23], has the following four pole configuration:
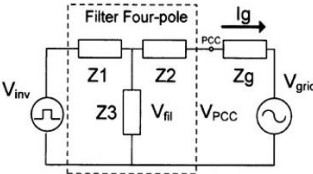
Figure 9-Generic diagram of three element filter

Based on above topology, three possible combinations are available [24]:

A. L filter: this filter only consists of an inductance used at the output of the inverter. Although the cost is low due to lesser number of components, the system dynamic is poor due to the voltage drop across the inductance.

Figure 10-L filter

B. LC filter: this filter is the result of association of the inductance and capacitance. With higher values of capacitance, inductance size can be reduced and so too the cost. However, higher values of capacitance may result in inrush currents.
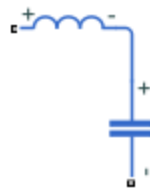
Figure 11-LC filter

C. LCL filter: LCL filter provides better decoupling between the grid and filter, reducing the dependance on the grid impedance and lower ripple current stress across the grid inductance. It has also the same advantage and disadvantage of LC filter, by increasing the capacitance, the inductance value can be reduced but may result in inrush currents.

It may cost more than the other filter types, but its small dependance on the grid impedance is of great importance.

And furthers, it provides better attenuation than other filters.
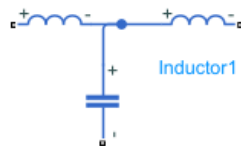
Figure 12-LCL filter

In [25], the case of LCL filter in terms of parallel-connected inverters is investigated. The resonance frequency of the parallel-connected inverters may get affected by the number of inverters in parallel due to the impact of grid impedance and it may deteriorate the performance of active damping method aimed at fixed resonance frequency.
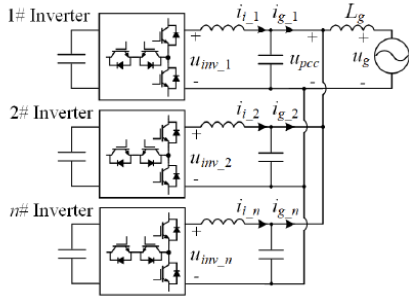
Figure 13-Simplified single-phase model

For the j_{th} Inverter the grid side current is composed of circulating current and current flowing to the grid.

Therefore, the grid side current I_{g_j} is expressed as:

$$i_{g\_1} = \underbrace{\frac{1}{n}G_{mutal}\left(u_{inv\_1} - u_{inv\_2}\right) + ... + \frac{1}{n}G_{mutal}\left(u_{inv\_1} - u_{inv\_n}\right)}_{Circulating\ current\ among\ inverters}$$

$$\underbrace{+\frac{1}{n}G_{common}\left(u_{inv\_1} + ... + u_{inv\_n}\right)}_{Common\ current}.$$

(2-14)

In order to avoid the resonance to be affected by the number of inverters in parallel, a common capacitor is used at the PCC to adjust the resonance frequency.
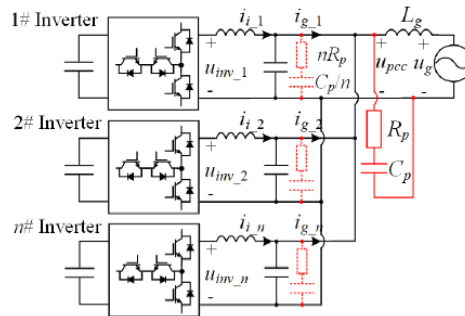
Figure 14-multi-Parallel grid connected inverters with common RC branch

$$G_{mutual}(s) = \frac{1}{SL} \ (\ 2\text{-}15)$$

$$G_{common}(s) = \frac{1}{S^3*Li*Lg*(Cp+n*Cf)+S(Li+nLg)} \ (\ 2\text{-}16)$$

The resonance frequency can be obtained as:

$$\omega_{res} = \sqrt{\frac{nL_g + L_i}{L_g L_i (C_p + nC_f)}} \quad (\text{2-17})$$

And based on above formula, it can assume that the resonance frequency is kept constant.

while designing the filter several characteristics should be considered such as current ripple, filter size, and switching ripple attenuation.

The following parameters should be considered for the filter design:

Un, line to line RMS voltage (inverter output), Uwx-phase voltage (inverter output),Pn -rated active power, Vdc-DC link voltage, fn-grid frequency, fsw-switching frequency, fres-resonance frequency.

The filter's values are referred to in a percentage of the base values:

$$Z_b = U_n{}^2/S_n; C_b \; (\text{2-18})$$

Design of LCL filter parameters:

The LCL filter sizing procedure is as follows [26]:

The first step is the design of the Inverter's side inductance. It can limit the output current ripple by up to 10% of the nominal amplitude.

$$Li = \frac{Udc}{16 * fs * \Delta IL\_MAX} \quad (\text{2-19})$$

ΔIL_{Max} is the 10% of the current ripple specified by:

$$\Delta IL_{Max} = \frac{P_n * \sqrt{2}}{U_n} * 0.01 \; (\text{2-20})$$

The next step is designing the capacitance and the constraints come from the fact that maximum power factor variation acceptable by the grid Is 5 %.

Cf = 0.05 * Cb (2-21)

The grid side inductance Lg can be calculated as:

Lg = r *Li (2-22)
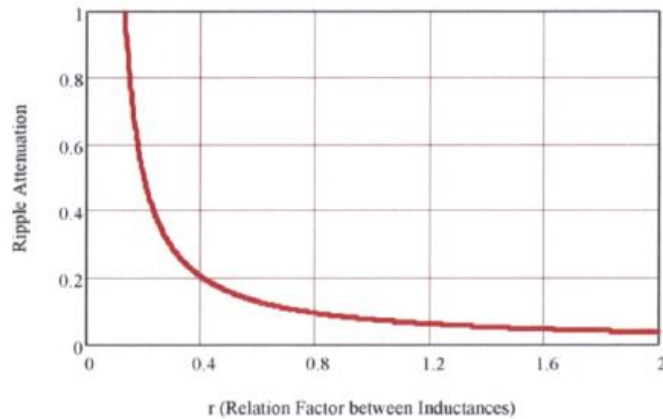
Figure 15- Factor r and the relationship with Ripple Attenuation

In order to verify the design, the resonance frequency should be in the range of 10*fn < fres < fsw

$$\text{Fres} = \frac{1}{2\pi} * \sqrt{\frac{L_i + L_g}{L_i * L_g * C_f}} \quad (2\text{-}23)$$

To reduce the resonance and the unstable states of the filter, the capacitance should be added with an in series connected resistor. This solution is often called as the passive damping. As the drawbacks of this method Increase in the heat losses and consequently decrease in the efficiency of the filter but on the other hand it is a simple and reliable method. The damping resistor is obtained as follows:

$$R_{sd} = \frac{1}{3 * \omega_{res} * C_f} \quad (2\text{-}24)$$

2.6   Market Analysis

2.6.1   The General trend

Power electronics are facing the limits of hardware performance due to the maturity of the topologies and advances of the semiconductor devices and now PE is at the crossroad of shifting the goals to more flexibility, integration and commonality as identified in the 2015 workshop of **US Naval Research** rather than the hardware performance merits such as weight, smaller size, and lower cost [27].

One of the main emerging usages of the power electronics Is the electric grid facing a high penetration of the power electronics from the transmission backbone to grid edges as Illustrated In the figure (13):
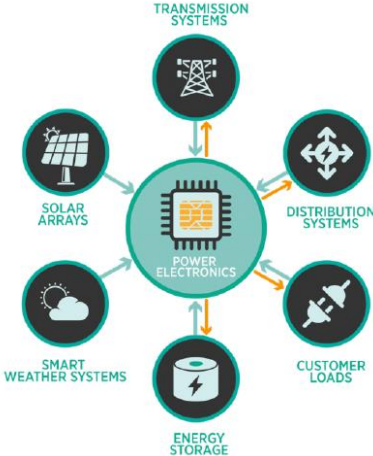
Figure 16-Power electronics applications in electric grid. (Source: U.S.)

2.6.2   General solution Trend

The development of power electronics has been driven by internal semiconductor technology and converter circuit topology, approaching the limits of its internally set metrics, e.g., efficiency. Although the original driving philosophy indicating internal maturity, the external constituent technologies of packaging, manufacturing, electromagnetic and physical impact, and converter control technology still present remarkable opportunities for development [28].
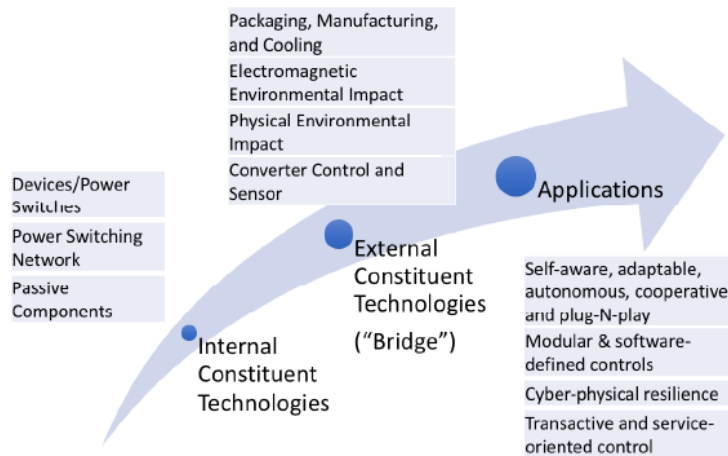
Figure 17-Power Electronics General Trend

In 2011, US Department of Energy (DOE), identified six attributes for a modernized grid which include reliability, security, affordability, flexibility, sustainability, and resilience. This has resulted in tremendous opportunities for power electronics to be expand the utilized space and moves from high voltage to medium and low voltage applications.

The deployment of the small-scale Inverter-based distributed generations, has brought the concerns to maintain the frequency stability and voltage level as well as issues due to reverse power flow etc. All had resulted in the system operators to demand the active participation of the inverters. The concept of the smart inverters was Introduced in [29] and [30].

2.6.3   The global string inverter market size and growth

According to Mordor's Intelligence, the global string inverter market is estimated around $ 3.8 billion in 2021 and is expected to grow up to $ 4.6 billion by 2027. With targets to decrease the carbon footprint and reduce the GHG emissions and RES coupled with storage systems which create opportunities to for the string inverter market to grow.

Study Period:	2016 - 2026
Base Year:	2020
Fastest Growing Market:	Asia Pacific
Largest Market:	Asia Pacific
CAGR:	>15 %

Figure 18-Market Size

2.6.4 The global string Market Regional Analysis

Asia-pacific is the dominating region with the highest installed capacity of the string inverters. Asia-pacific region has 47.6% of the global market.

China, Japan, and India have the highest share in the market. China is the leading at the country level.

These regions are among the most populated regions in the globe and have established themselves as the industrial and technological centers which yields in higher demand for electricity and subsequently this impacts the inverter markets.

Figure 19-String Inverter by Region
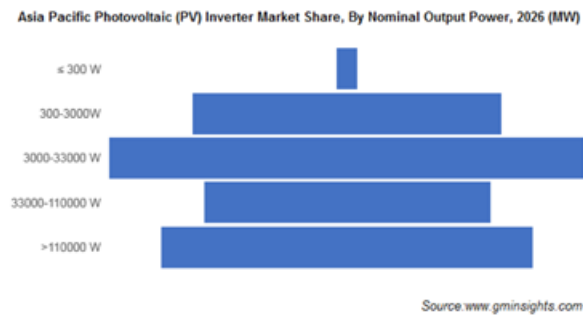
Figure 20-Asia Pacific Inverter Market

According to GTM Research, the European inverter market is led by three companies (SMA, Fronius and ABB) that are also in a favorable position in the world market. SMA Solar (Germany) is the world's highest ranked company about R&D investment in the PV sector.

Manufacturers supplying three phase string inverters for sub 1MW systems – namely SMA, ABB, Huawei, SolarEdge Technologies, Fronius and Ginlong Solis, who together are estimated to account for 67% of the shipped capacity for these types of products in 2017x.
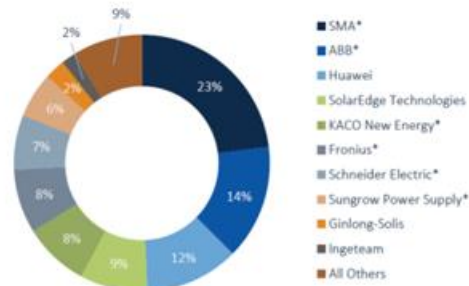
Source: GTM Research (2017) *estimates

Figure 21-Manufactures

In terms of module level power electronics, SolarEdge, Tigo Energy and Maxim Integrated can be identified as the leading manufactures of DC power optimizers for use in combination with transformer-less string inverters. Manufacturers currently offering inverter level power electronics that support battery integration include SolarEdge, Huawei and SMA.

Projected annual sales growth rates for inverters

Inverter type	2016	2017E	2018E	2019E	2020E	2021E	2022E
Microinverter	81%	58%	11%	17%	13%	6%	10%
Single-Phase String	-24%	28%	17%	6%	7%	-1%	10%
Three-Phase String	103%	4%	38%	12%	-1%	19%	13%
Central Standalone	-62%	4%	10%	61%	-6%	32%	-10%
Central Solution	-41%	21%	11%	103%	-35%	97%	-2%
Total	-4%	9%	27%	24%	-4%	24%	7%

Source: calculated from data provided by GTM Research (2017)

Figure 22-Projected annual growth rate for Inverters

In figure, European Inverter shipments by technology in the year of 2016 Is shown. As it can be seen, three-phase string Inverters have the highest share of the market. Utility segment string inverters are primarily three-phase, have a power rating of more than 80kW, and have unique properties to withstand extreme climatic conditions.
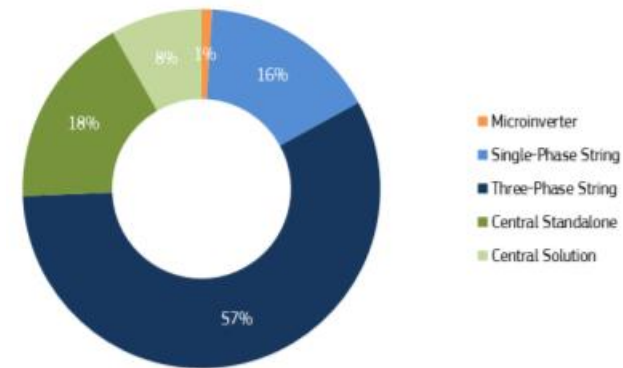
European inverter shipments by technology (2016)

Source: GTM Research (2017)

Figure 23-Shipment by technology

In terms of performance improvement, the most significant trend projected as taking place in 2018 is the potential introduction into the market of inverter designs with silicon carbide (SiC) and gallium nitride (GaN) switching components (transistors). It is claimed their introduction support increased power densities whilst reducing cooling requirements, thereby reducing the bill of materials, a large part (70%) of which is accounted for by mechanical and electromechanical components such as metal heat sinks 24. This can be achieved by so-called 'hot core' architectures that require heat sinks to be made of composite materials with greater thermal conductivity.

2.6.5 The global string market drivers

Many installations require a mean of alternating direct current to alternating one. The increasing demand for the continuous and reliable power along with easy installation are the main drivers of the market. String inverters are used in residential, commercial, and utility scale and ever-increasing consumption of the solar energy is the main driver of the string inverter market which provide long-term efficiency and decrease the utility bills in the residential sector. Further, the integration of the latter in large-scale is the main driver in the utility scale. Effective feed-in-tariffs and cost reduction of batteries are expected to benefit the string inverter market.

2.6.6 The global string inverter market segmentation

- **Based on the end-user**: string inverters are used in residential, commercial, and industrial sections and among all, the utility segment is the largest one.
- **Based on system**: the market is divided into on-grid and off-grid. In the review period, the on-grid inverters are dominating, however, the off-grid type is expected to grow in a faster rate in the future. In terms of number of phases, the three-phase are mostly used in the forecasted period.
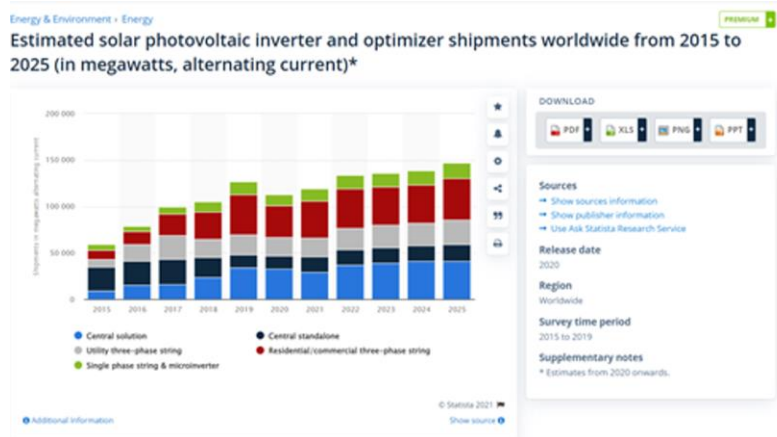
Figure 24-
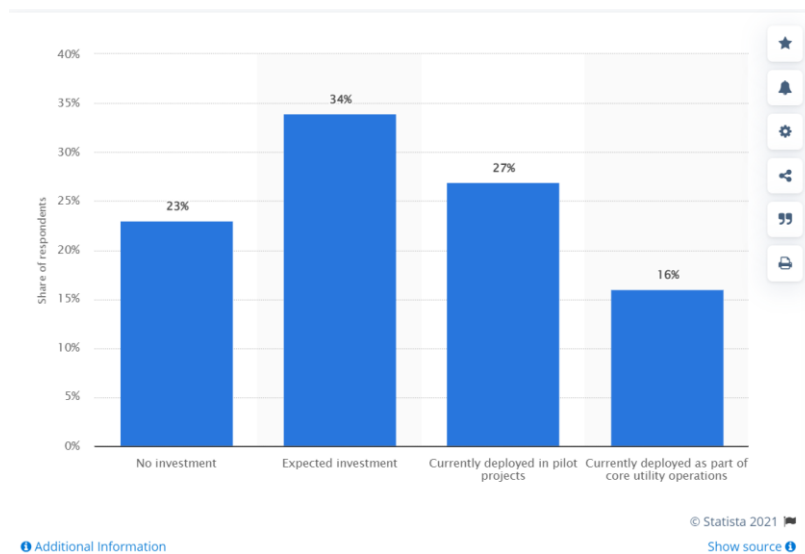
Figure 25-Level of investment in smart inverters and grid communication technologies in the US and Canada in 2017

- **Based on power rating:** the largest segment of global string inverters is between 41kW-80kW due to their compact size and light weight.

2.6.7 Comparison between Central and string inverter

There is no single answer to which technology is the best since it depends on the situation. Concepts

based on central inverters or string inverters are characterized by low specific system costs, and a high level of efficiency. String inverters also have benefits regarding installation and serviceability. Particularly in industrial and commercial plants [31],[32].

Microinverters have their place in installations of 1kW or less. They shift a lot of electronic components to the modules. But this has the disadvantage of difficult servicing or replacement. The number of electronic components which can fail is much larger for a microinverter, and they are also exposed to high temperatures [PV Magazine].

2.6.8   String inverters in a snapshot

As in [33] String inverters offer easier scalability for future upgrades and have shorter DC wires. They also monitor the installation at the string level rather than a central one.

String inverters offer also higher reliability. Since the power is converted through fewer strings, if part of the system fails, the whole power is not lost.

The cost reductions are driven by the continuous development of technology. Maintenance of the string inverters is also easier as the replacement is easier in case of fault, this result in lower cost [34].

2.6.9   Central inverter in a snapshot

 As stated in [35],[36] The individual solar panels/batteries are connected in series and the DC power from these panels is converted by the central inverter.

The main advantage of the central inverters over the other types is the low cost.

However, the drawbacks are hindering the growth of its market:

1. **Single point of failure**: the failure even in one single panel can result in the down performance of the whole system.
2. **Higher risk factors:** the high DC power produced, needs to be transformed to the central inverter for a long distance which can result in threats both for the installer and owners.
3. **Higher costs:** the failure of one single panel can result in the halt of the whole production and consequently, greater economic loss.

3   SIMULATION AND MODEL DESIGN

The thesis work started with the understanding the fundamental principles of three-phase Inverters, control systems and the modulation techniques. As for the first step, the simulation of a single three-phase grid connected inverter with the line-to-line RMS voltage of 380V is carried out. Then a model of two parallel inverters on the AC side with different DC buses and a delay In the PWM modulation waveforms is developed. Thirdly, the model is tested with the same DC bus to observe the effect of the latter.

Since Simulink world requires some specific blocks to make simulations work, in this case powergui block must be used to make electrical/power system blocks run. In addition, this block allows to perform THD analysis of the signals and other functionalities.
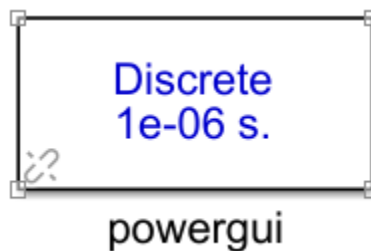
Figure 26-Powergui

3.1   General structure

3.1.1   Two-level inverter

Two level three phase NPC Inverters consists of 6 switches, 2 per each leg and from the middle point of each leg, phase A, B and C are derived respectively. Each switch receives a signal for functioning.
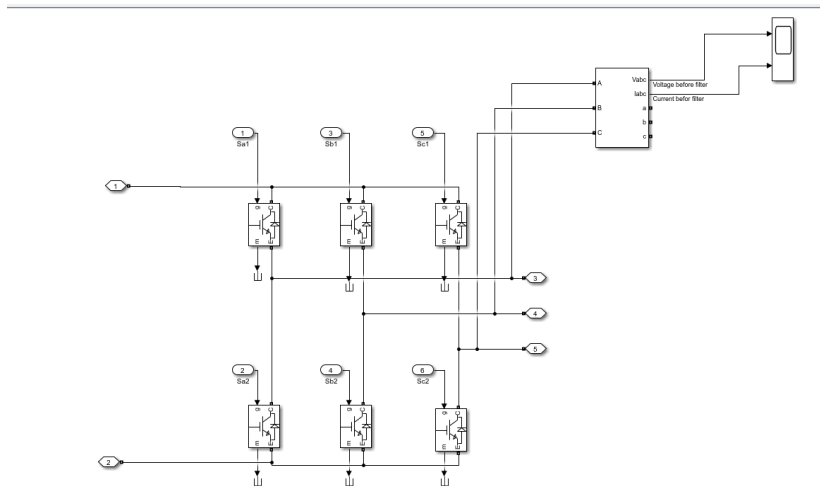
Figure 27- 2level inverter

3.1.2   3-Level inverter

Compared with two level inverters, three level inverters have lower harmonic content, higher voltage range and small du/dt.

Three level three phase NPC inverter consists of 12 switches, 4 per each leg and 2 free-wheeling diodes per leg.

The dc voltage is divided in two by a middle point connected to the free-wheeling diodes.
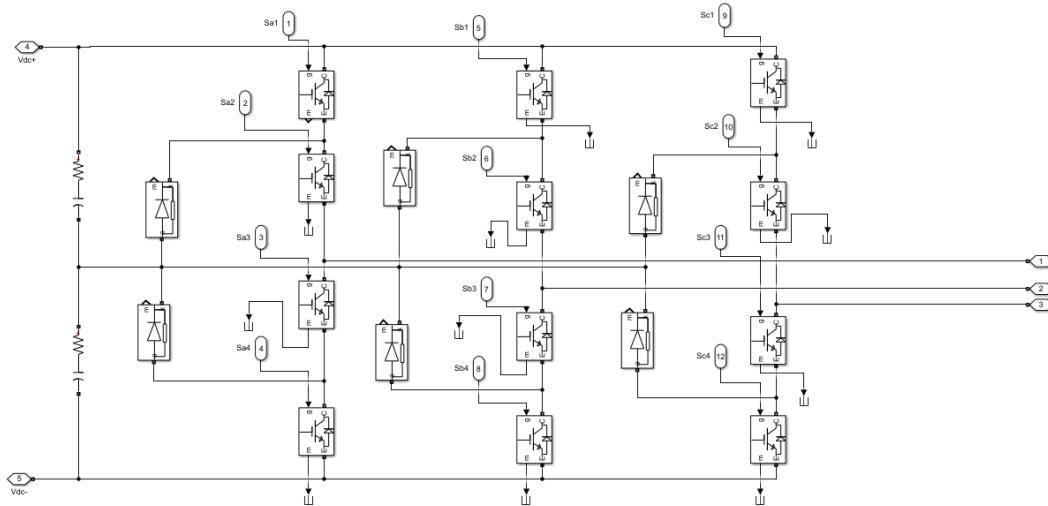
Figure 28-3level inverter

3.1.3   LCL filter

Due to the switching sequence of the inverters, output voltage of the PWM inverters contain higher order harmonics which interference with grid code. Therefore, the output current is smoothed out by means of the filter.

Design of the filter depends on the size, current ripple etc. Therefore, choosing the right parameters is of great Importance. three different configurations can be considered:

L filter: It's a simple Inductive filter. Due to the voltage drop across the Inductance, the system dynamic is too low.

LC filter: the frequency response of this system is strongly dependent on the grid impedance and large values of the capacitance, may result in inrush currents.

LCL filter: this type of the filter, the reduces the dependence on the grid impedance and lower the ripple the most.

In MATLAB Simulink, two inductance and capacitance is used in T shape to form the LCL filter.
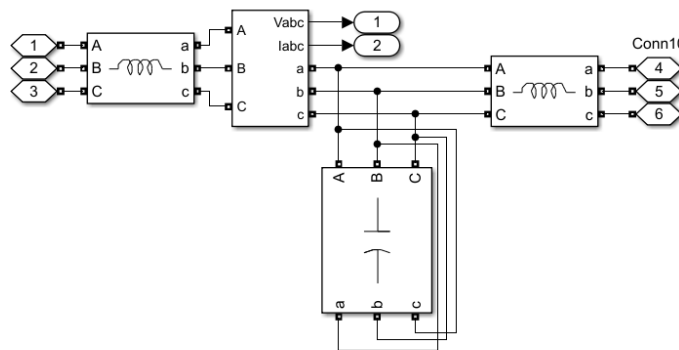
Figure 29-LCL filter

In the figure 25 shows a three phase Inductance on the left called L1 and a three-phase inductance on the right called L2 and a three-phase capacitance is delta connected in the middle.

The last block, a three-phase measurement block, measures phase to phase voltages and line currents.

The LCL filter will be vulnerable to oscillations too and it will magnify frequencies around its cut-off frequency. Therefore, the filter is added with damping. The simplest way is to add damping resistor. In general, there are four possible places where the resistor can be placed series/parallel to the inverter side inductor or

series/parallel to filter capacitor. In this Simulink model, the damping resistance is added in series with the filter's capacitance.

Table 1-LCL Filter values

Parameter	Value
L1	756.21μH
L2	453.726851 μH
C	300 μF
Rf	0.54Ω
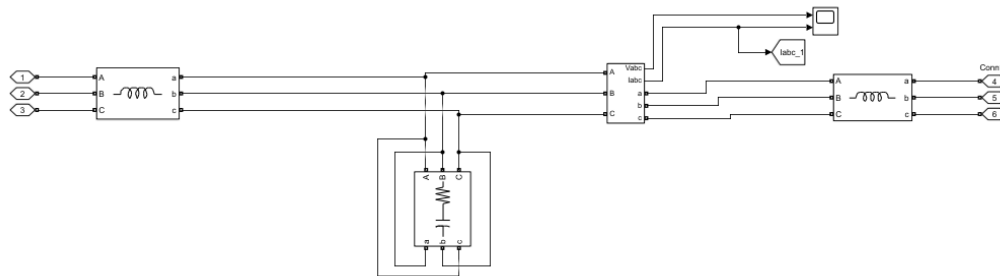
Figure 30-LCL filter with damping resistor

3.1.4   Grid

The grid is simulated using a delta connected three phase sources with: $V_{grid,RMS,ph-ph} = 380\ V$ and $f_{grid} = 50\ Hz$. The variable voltage source is selected to further observe the effect of the harmonics. The Controlled Voltage Source block converts a Simulink® input signal into an equivalent voltage source. The generated voltage is driven by the input signal of the block. The proper design of the Grid is out of scope of this project.
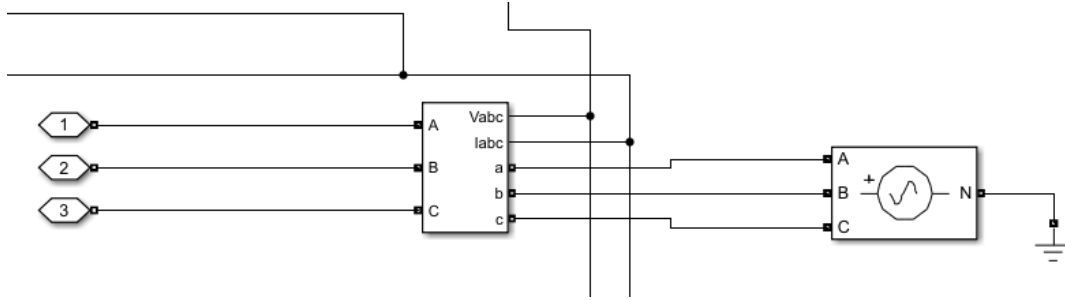
Figure 31-Three-phase source

The phase-locked loop (PLL) block is a feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal. PLLs operate by producing an oscillator frequency to match the frequency of an input signal. In this locked condition, any slight change in the input signal first appears as a change in phase between the input signal and the oscillator frequency. This phase shift then acts as an error signal to change the frequency of the local PLL oscillator to match the input signal. The locking-onto-a-phase relationship between the input signal and the local oscillator accounts for the name phase-locked loop. PLLs are often used in high-speed communication applications.

The MATLAB Simulink PLL block models a Phase Lock Loop (PLL) closed-loop control system, which tracks the frequency and phase of a sinusoidal signal by using an internal frequency oscillator. The control system adjusts the internal oscillator frequency to keep the phases difference to 0. It has as input the vector containing the normalized three-phase signal and as outputs: measured frequency [Hz] and ramp $\omega \cdot t$ varying between 0 and 2π, synchronized on zero crossings of the fundamental (positive-sequence) of phase A.
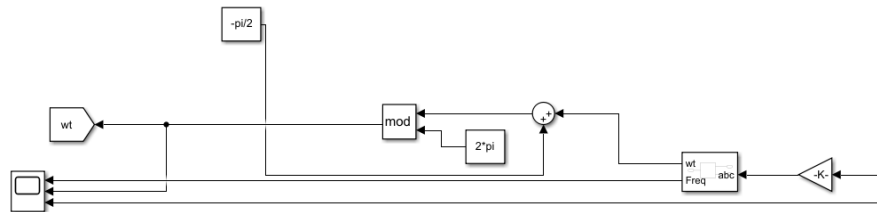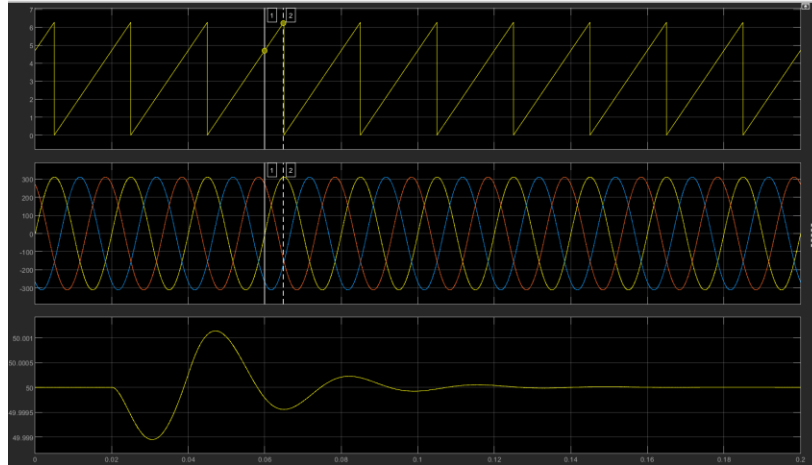
Figure 32-PLL

3.1.5   Current controller

One of the main controllers for regulation of power exchange between the grid and the MMC is grid current controller. There are multiple ways for implementation of this controller scheme such as three dimensional abc-frame, stationary two-dimensional ab-frame, and rotating two dimensional dq-frame. In this thesis, a decoupled dq-frame current control scheme has been employed to ensure that the ac current components, id and iq, are independently controlled and rapidly track their respective reference commands, i_d and i_q .

The Clarke and Park transformations can be carried out both based on the d-axis and q-axis. In this simulation phase a is aligned with the d-axis and all transformations are time Invarient.

```
function y = fcn(ua,ub,uc,wt)

K= sqrt(2/3);

T0 = K*[cos(wt) cos(wt-((2*pi)/3)) cos(wt+((2*pi)/3)); -sin(wt) -sin(wt-((2*pi)/3)) -sin(wt+((2*pi)/3));1/sqrt(2) 1/sqrt(2) 1/sqrt(2)];

T1 = [ua;ub;uc];

y = T0 *T1;
```

Figure 33-abc to dq transfromation

Then, the closed-loop current controllers are obtained based on dq-axis and PI controller Is designed individually for each axis respectively. This generally allows to generate a balanced abc three-phase current if the PI controllers are well regulated. The difference of the two currents, on d-, q- and 0-axis, gives an error

that becomes the input of a PI controller. PI is based on two parameters: k_p and k_i, proportional and integral term respectively.
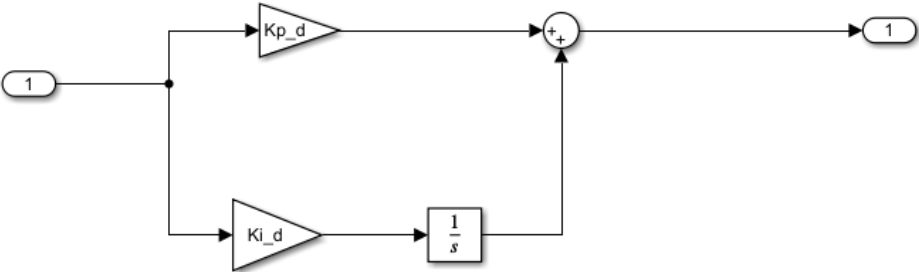
Figure 34-PI controller

Table 2- Controller Coefficients

Parameters	Value
Kp_d	0.2
Ki_d	20
Kp_q	0.2
Ki_q	20
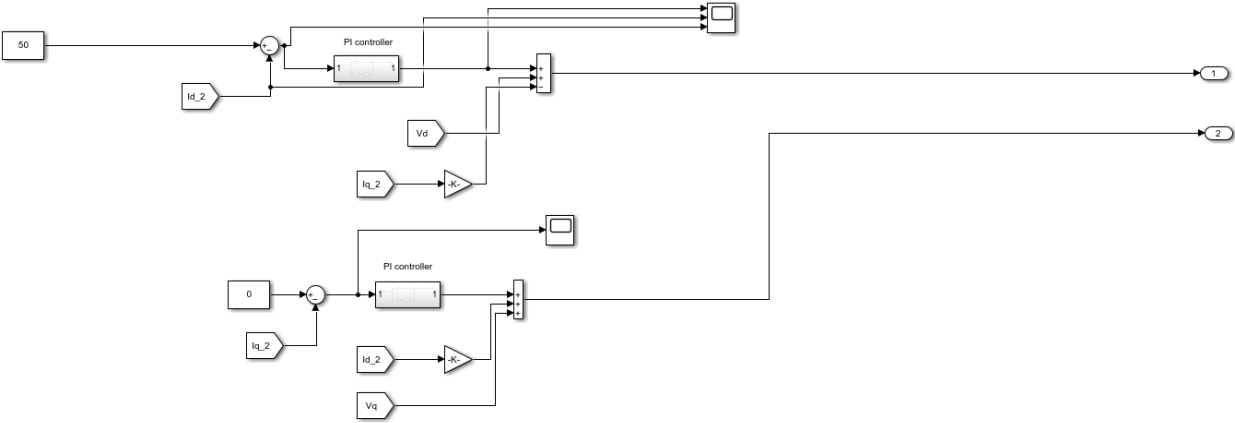
Figure 35-current controller

The measured dq0 currents are compared with the reference ones.

The RMS value of the reference current is obtained according to the power reference.

$$I_{RMS} = \frac{\frac{P}{3}}{\frac{V_{RMS,ph-ph}}{\sqrt{3}}} = \frac{\frac{33000\ W}{3}}{\frac{380\ V}{\sqrt{3}}} = 50$$

$$i_{d_{ref}} = 50\ A$$

$$i_{q_{ref}} = i_{0_{ref}} = 0\ A$$

3.1.6   Inverter Modulation: SVPWM

Once the controller is regulated based on dq-axis, its output Is transferred to alpha_beta reference frame and given to the Inputs of the modulation waveforms. The transformation Is Time-Invariant and phase A Is aligned with d-axis.

```
function y = fcn(ud,uq,u0,wt)

T0 = [cos(wt) -sin(wt) 0; sin(wt) cos(wt) 0; 0 0 1];
T1 = [ud;uq;u0];

y = T0 * T1;
```

3.1.6.1   Sector selection of 2 Level-inverter

Through alpha-beta component the angle and reference voltage of the 2-level inverter Is calculated. The hexagon of 2 level inverter is divided into 6 sectors, each 60 degrees apart. So, the angle is calculated through logical ports and by the Data type converter block the Boolean value is converted into Integer.
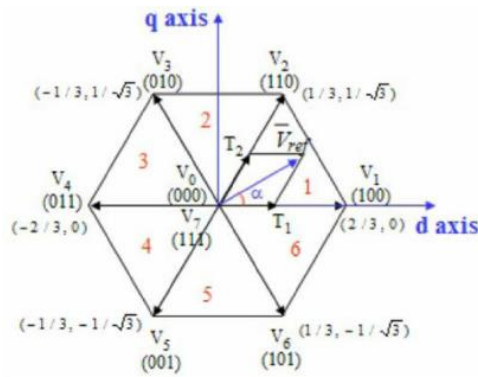
Figure 36-SVM of 2 level inverters
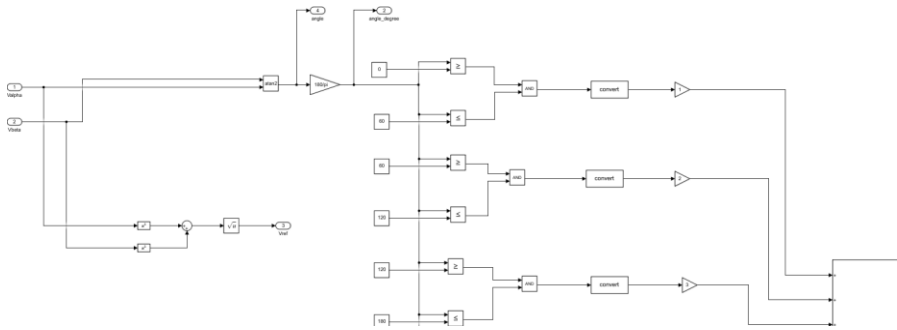
Figure 37-Sector selection of 2 level inverter

3.1.6.2 Dwell times and switching states

Based on the possible combinations of switch states, vector dwell times are calculated.

Table 3-Switching states of two-level Inverter

Switching state			Line to neutral Voltage			Line to Line Voltage		
A	B	C	VAN	VBN	VCN	VAB	VBC	VCA
0	0	0	0	0	0	0	0	0
1	0	0	2/3 Vdc	-1/3 Vdc	-1/3 Vdc	Vdc	0	Vdc
1	1	0	1/3 Vdc	1/3 Vdc	-2/3Vdc	0	Vdc	-Vdc
0	1	0	-1/3 Vdc	2/3 Vdc	-1/3 Vdc	-Vdc	Vdc	0
0	1	1	-2/3Vdc	1/3 Vdc	1/3 Vdc	-Vdc	0	Vdc
0	0	1	-1/3 Vdc	-1/3 Vdc	2/3 Vdc	0	-Vdc	Vdc
1	0	1	1/3 Vdc	-2/3Vdc	1/3 Vdc	Vdc	-Vdc	0
1	1	1	0	0	0	0	0	0

//MATLAB code

function [T1, T2, T0] = fcn(Vref, Tz, Vdc, n, angle)

T1 = ((sqrt(3)*Tz*Vref)/Vdc) * sin((n*pi/3)-angle);

T2 = ((sqrt(3)*Tz*Vref)/Vdc) * sin(angle- ((n-1)*pi/3));

T0 = Tz-(T1+T2);
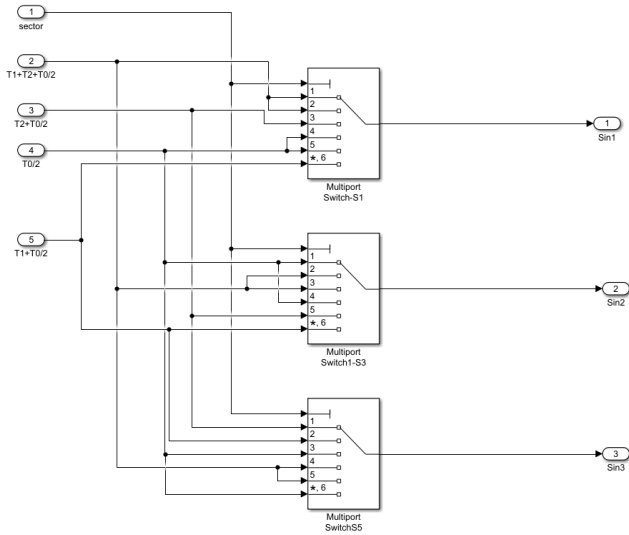
Figure 38-on state of switches

The method mentioned above is easy to implement for two level inverter, however as the level of inverters increase, the process becomes more complex and time consuming.

A general approach has been developed based on the value of the alpha-beta vectors. Reference voltage is synthesized with the three nearest vectors and realized respectively.

A MATLAB-function is used to calculate the modulation waveforms derived from the theory in Appendix. The generation of the modulation signals is based on the same logic both for 2Level and 3Level Inverter.

At last, the modulation waveforms are compared with a triangular waveform whose period is equal to the period of PWM signals and half of the switching period. The amplitude of the triangular waveform is set according to the modulation waveforms respectively. At last, the signals are used to command the IGBT switches.
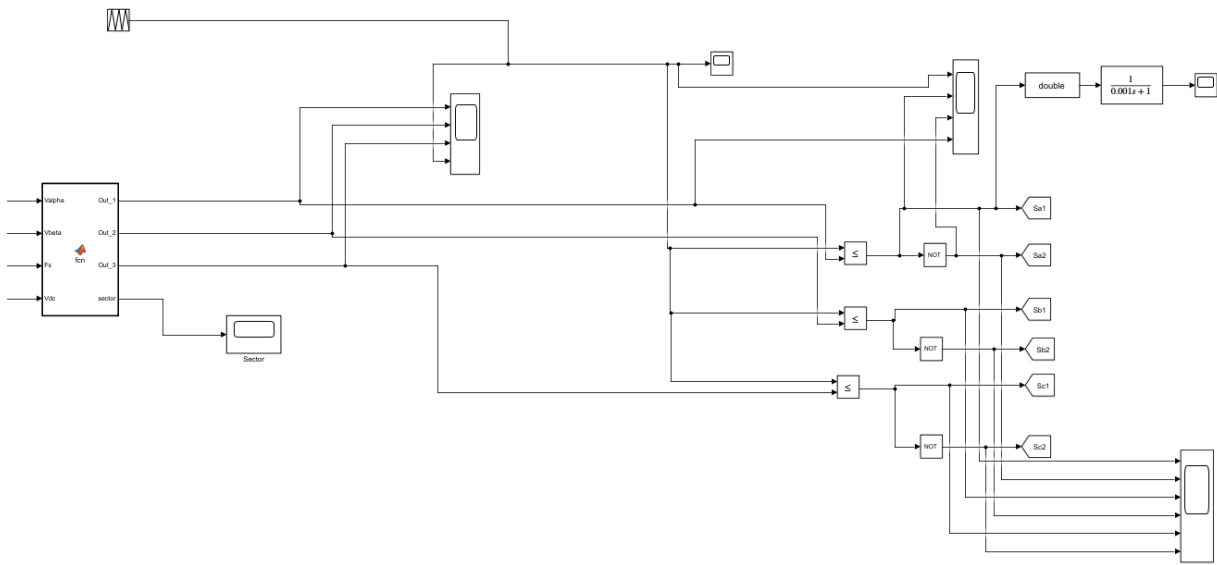
Figure 39-2-Level SVPWM
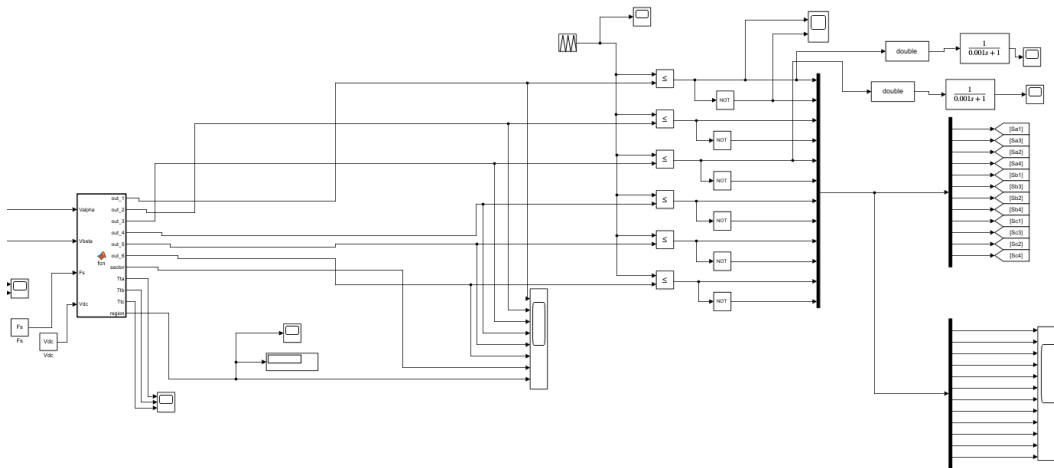
Figure 40-3Level SVPWM

Above the general structure of the simulation is explained. In the next chapter, different SVPWM approaches are put to test to evaluate the impact on the common-mode voltage, ZSCC and the output voltage and

currents both in the single grid-connected inverter and the parallel connections. The theoretical details of the approaches are explained throughout in the APPENDIX.

4 TEST RESULTS

In this chapter, in a sequential manner, all the steps taken to lead to the final results has been taken.

At first, three-phase single grid connected two-level and three-level inverters are simulated and the traditional SVPWM is implemented. Then, for each topology of the inverters, parallel scheme is developed and the effect on the CMV and the ZSCC is studied and lastly, modified SVPWM techniques are implemented to reduce the CMV and consequently ZSCC. For each method, THD is measured and verified with the grid requirements. The details of each modified SVPWM are explored deeply in the appendix.

4.1 SINGLE THREE-PHASE INVERTER CONNECTED TO THE GRID

4.1.1 Two-level inverter

As the foundation of the thesis, first a model of 2Level/3 level grid connected inverter is developed. The theory of the SVPWM is implemented. LCL filter Is designed according to the desired sizing's and current controllers are tuned to regulate the PCC current.
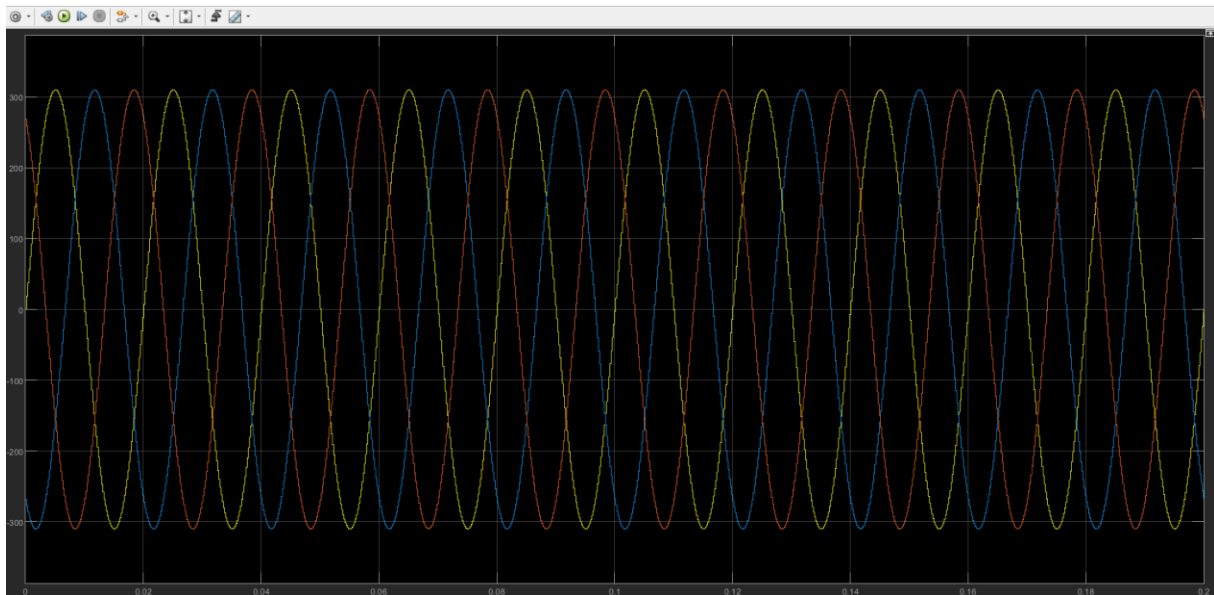
Figure 41-Voltage delivered by the Grid,2L Inverter

The output current:
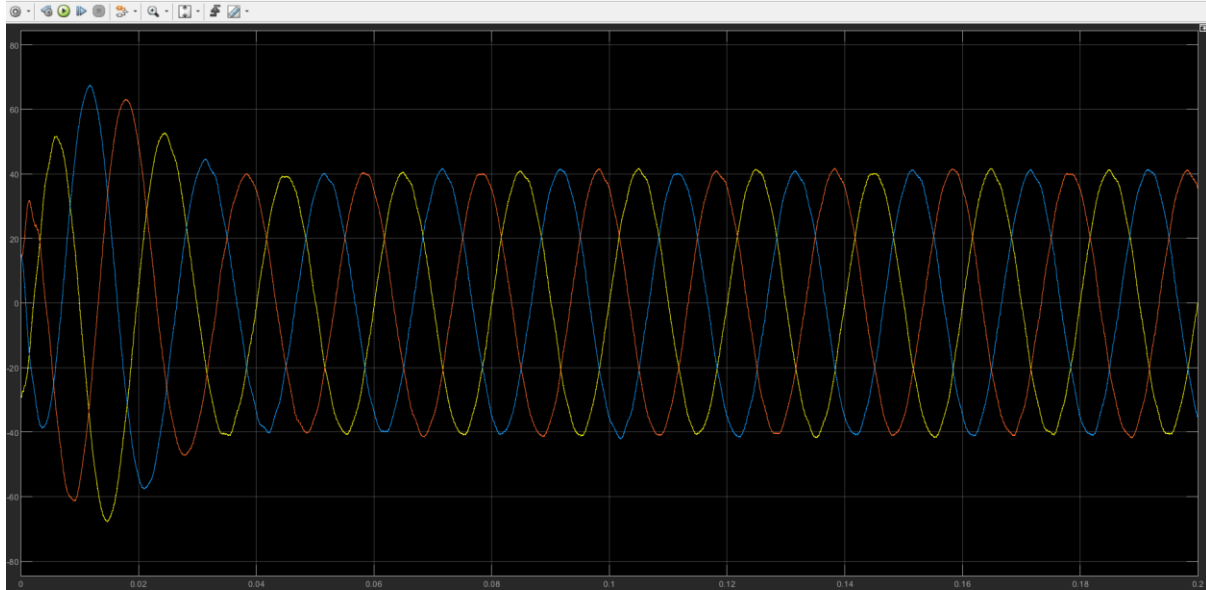
Figure 42-output current of 2 level inverter

As it can be seen In Figure-41 and Figure-42, the voltage and current are in phase with each other.

A power measurement unit is introduced to see the trend of power. The measured active power is according to the desired reference power and reactive power is zero as expected.
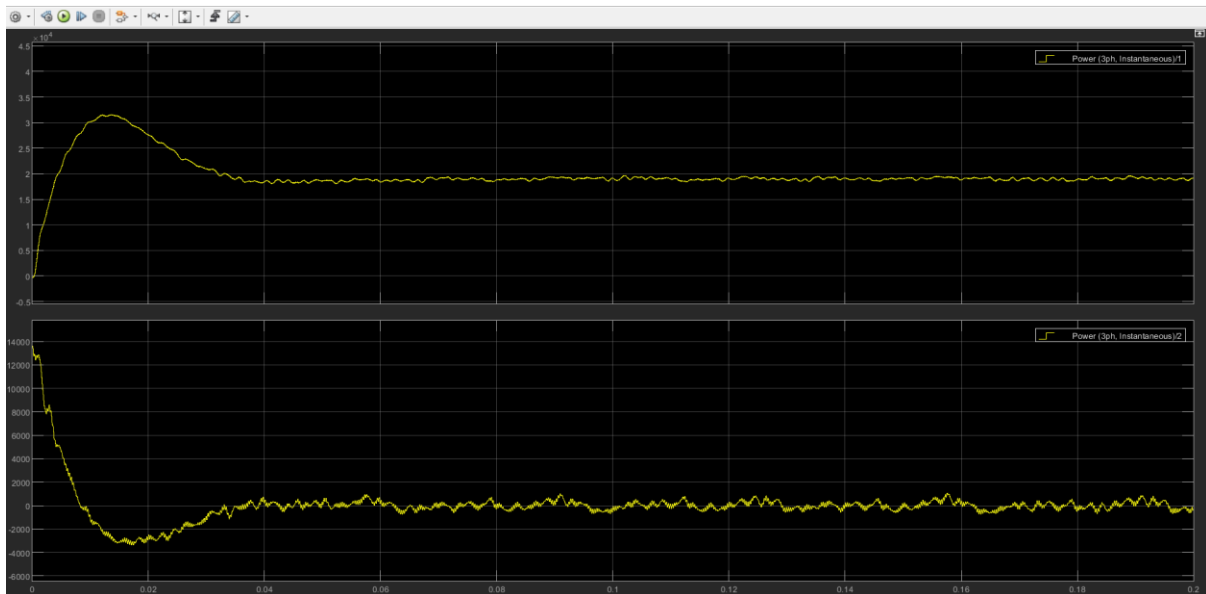

Figure 43-Power measurements

The space vector hexagon is consisting of sectors leading each other by 60 degrees and Figure 44, change of sectors by change of reference voltage and currents is observed.
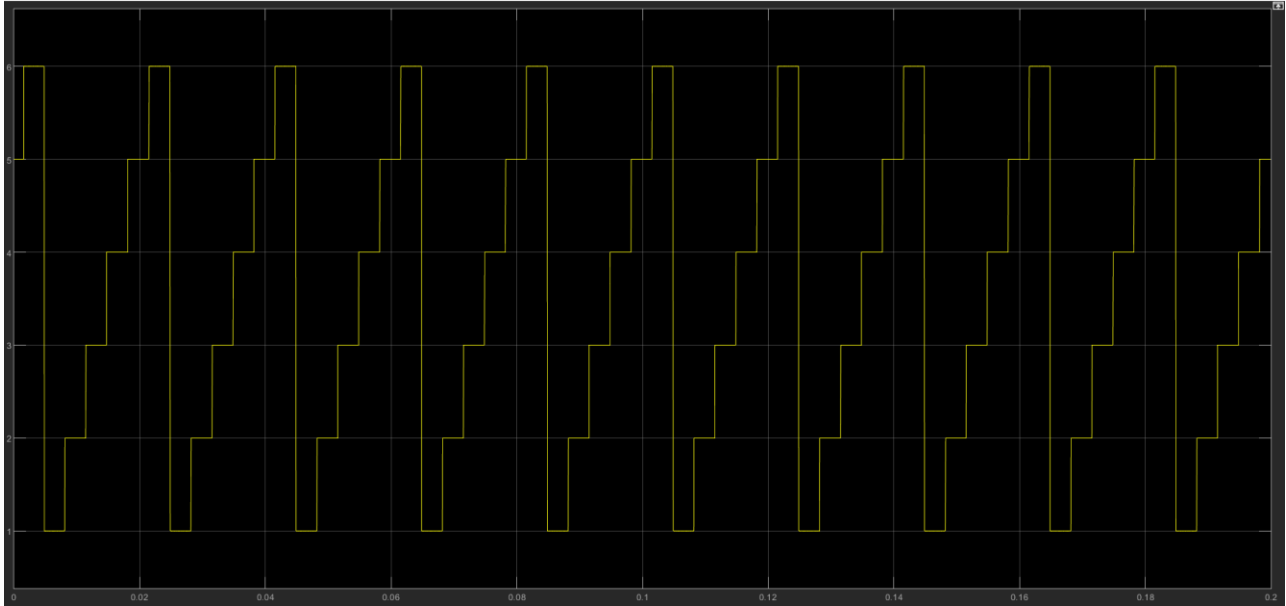
Figure 44-2Level Sector Change

A step-by-step current analysis is taken. This means, we start from transform of current from abc to dq0-axis. Figure below represents dq0-axis currents, errors, and voltage errors after the PI controller respectively.

Figure 45-Inverter dq0-currents
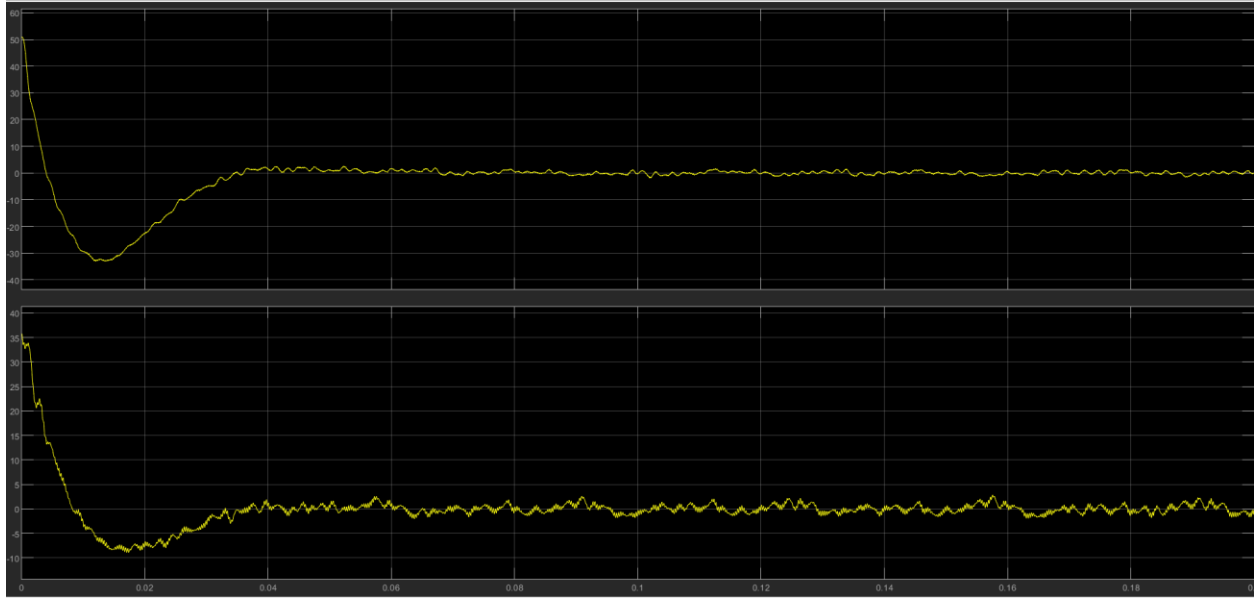
Figure 46-Inverter dq0-errors
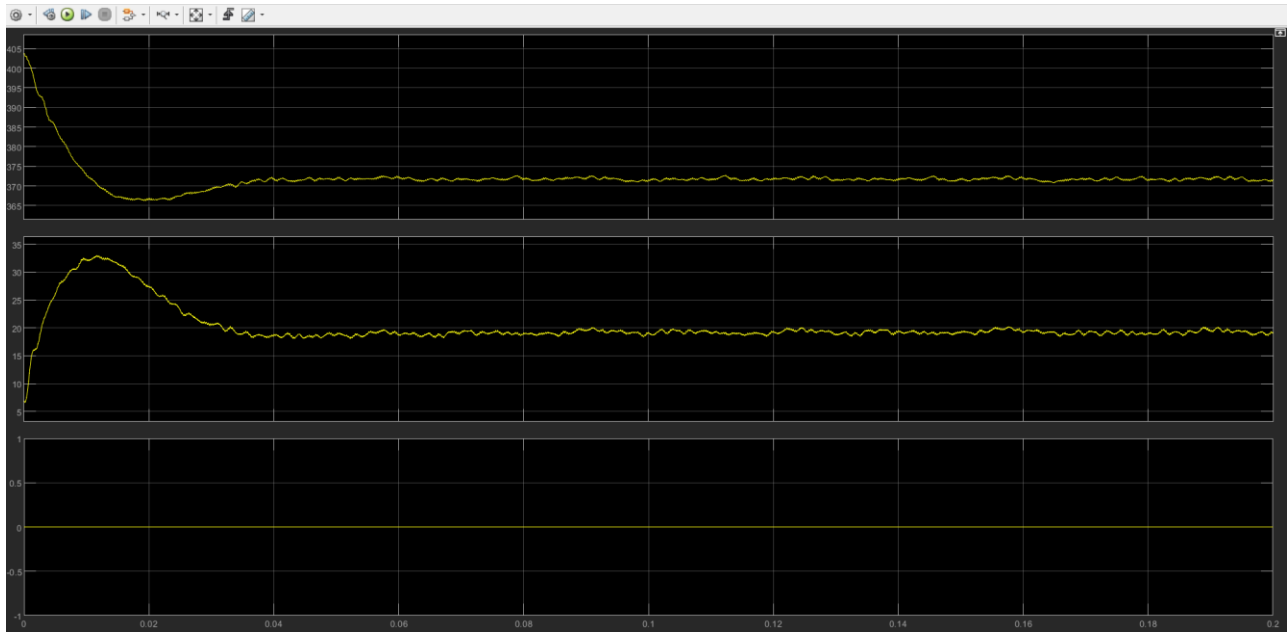
Figure 47-Inverter dq0 Voltage errors

The modulating signals are the IGBTs reference times of each phase, from the MATLAB-function, while the triangular carrier signal varies between 0 and $Ts/2$, where Ts is the switching period.
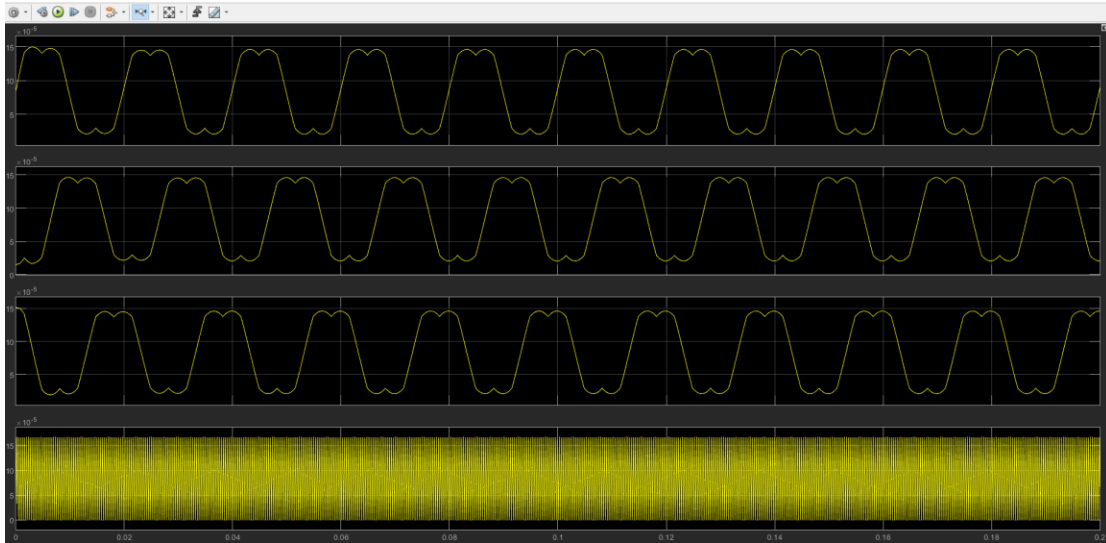
Figure 48-2Level modulation signals with respect to the carrier signal

4.1.2   Three-level Inverter

In this chapter, the same procedure has been done on 3Level Inverter. The theory of the SVPWM is implemented. LCL filter is designed according to the desired sizing's and current controllers are tuned to regulate the PCC current.
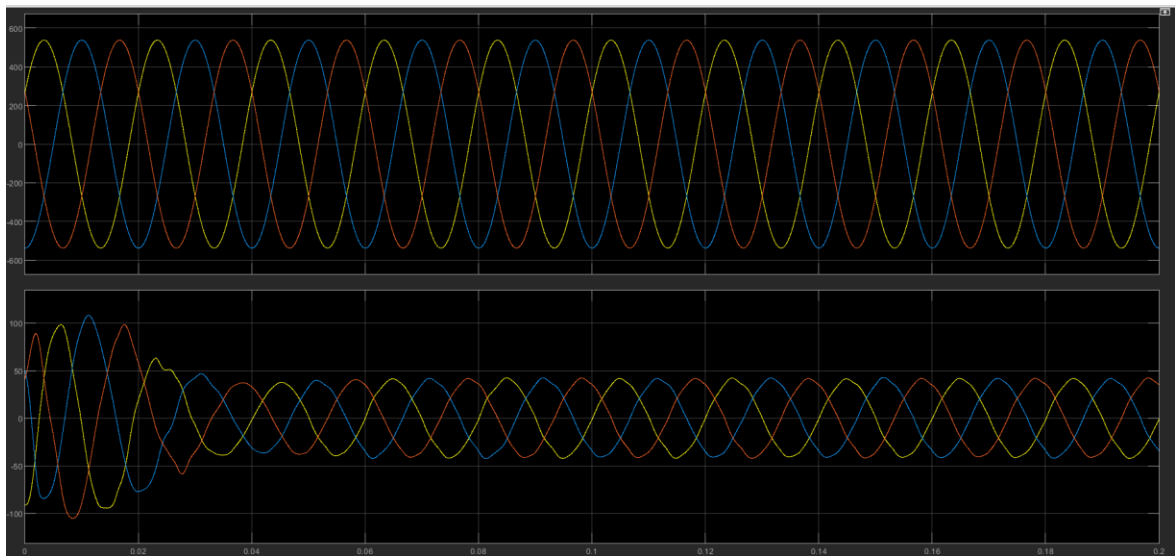
Figure

49-3Level inverter Grid voltage and currents

As it can be seen In Figure 49, the voltage and current are in phase with each other. Due to the nature of 3 - level inverter that has lower harmonic content with respect to 2-level inverter, the filter to be used can be smaller in size but for the sake of comparison the size of the filters and the PI controller coefficients are kept constant throughout the work.

A power measurement unit is introduced to see the trend of power. The measured active power is according to the desired reference power and reactive power is zero as expected.
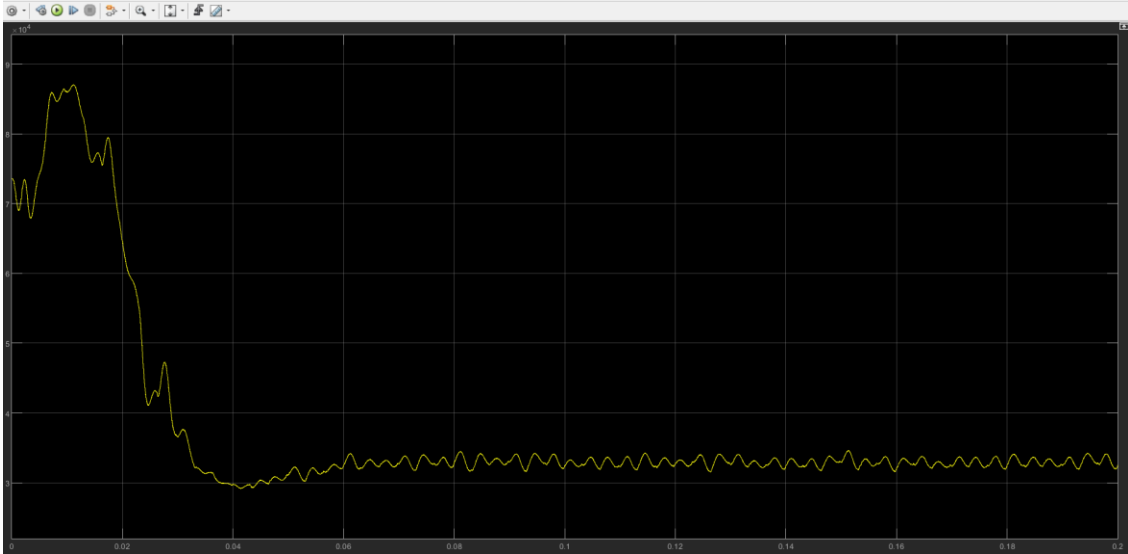
Figure 50-Power output-3Level

A step-by-step current analysis is taken the same as 2-Level inverter. This means, we start from transform of current from abc to dq0-axis. Figure below represents dq0-axis currents, errors, and voltage errors after the PI controller respectively.
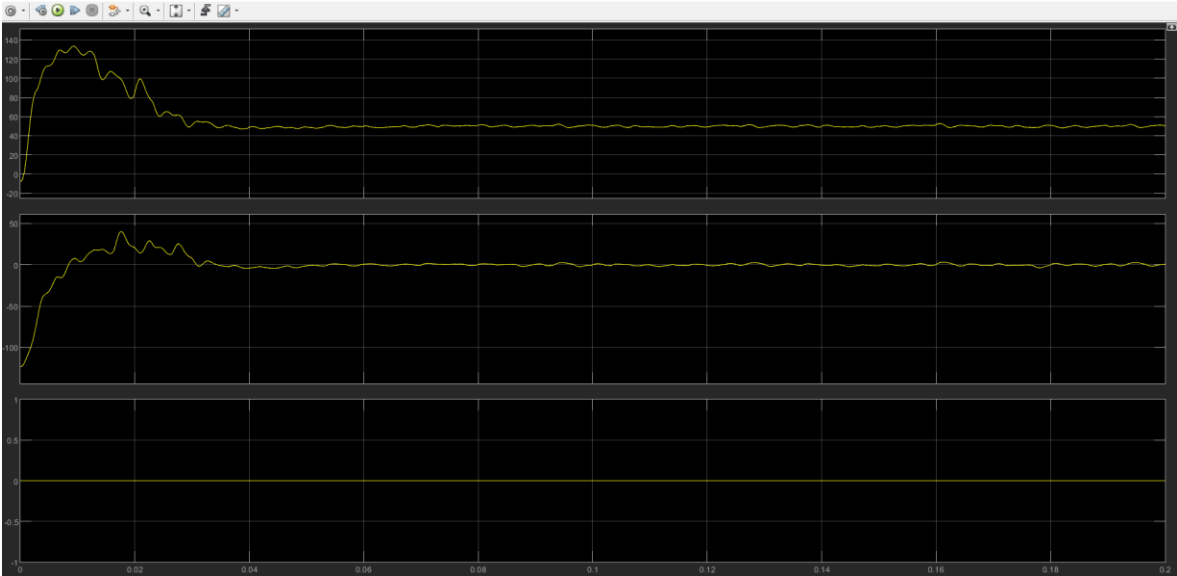

Figure 51-3Level dq0 currents

The modulating signals are the IGBTs reference times of each phase, from the MATLAB-function, while the triangular carrier signal varies between 0 and $Ts/2$, where Ts is the switching period.
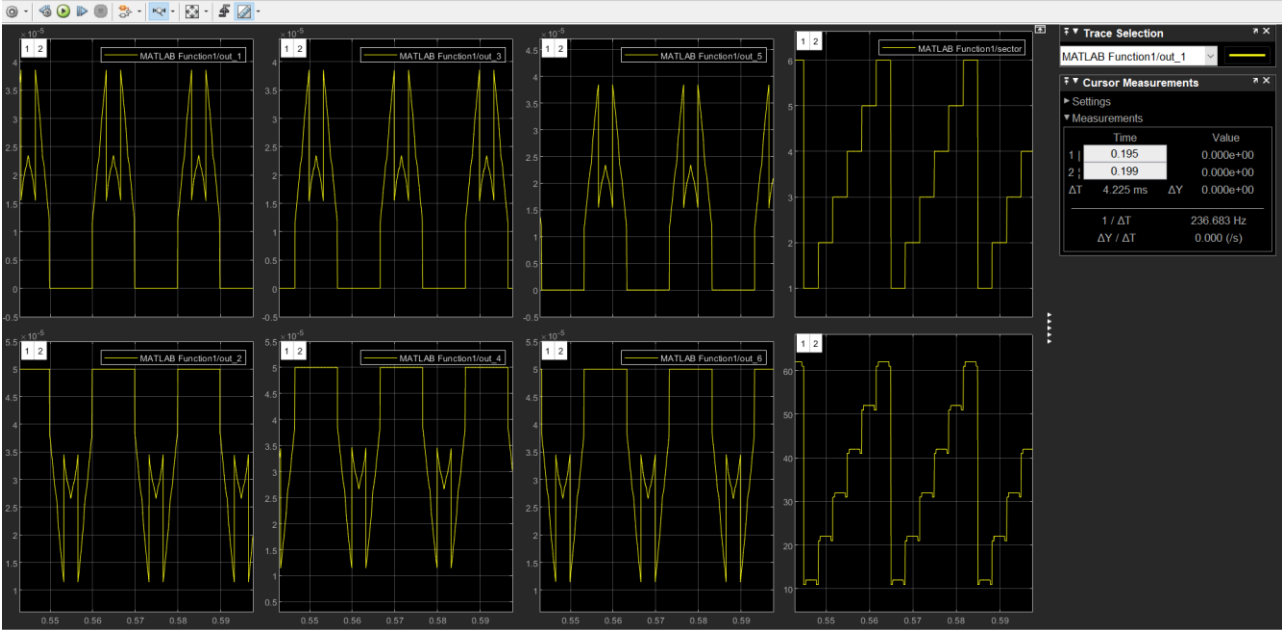
Figure 52-3Level modulation signals with respect to change of sector and region

4.2   Two inverters in parallel

4.2.1   Same frequency, separate DC buses

In this condition, when the two inverters are working with the same frequency and different dc buses, it is observed that the power delivered to the grid is twice the condition of one single Inverter.
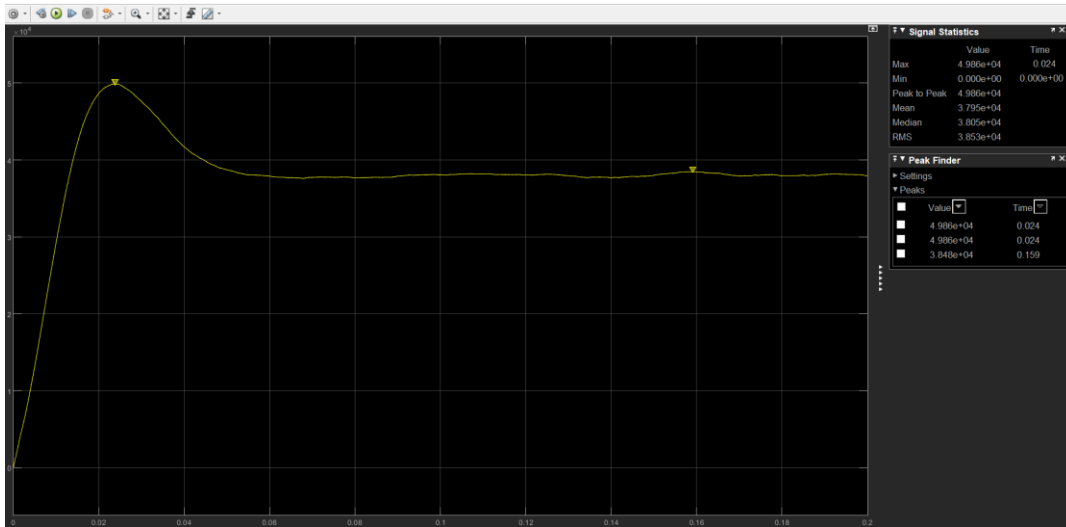
Figure 53-Delivered power in parallel condition

The voltage and currents are still in phase with each other, hence the reactive power measured is zero.

The current delivered to the grid is the sum of currents of two inverters.
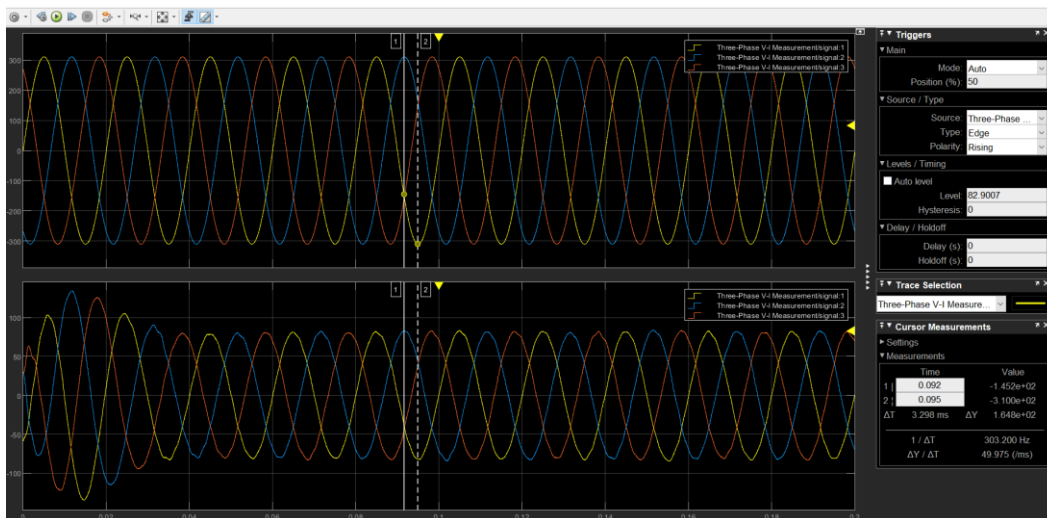
Figure 54-Voltage and currents on grid side

The output voltage and current of each inverter is measured by a three-phase measurement unit after the LCL filter. The results are show in the Figure 55&56:

Figure 55-Inverter 1 output voltage and current
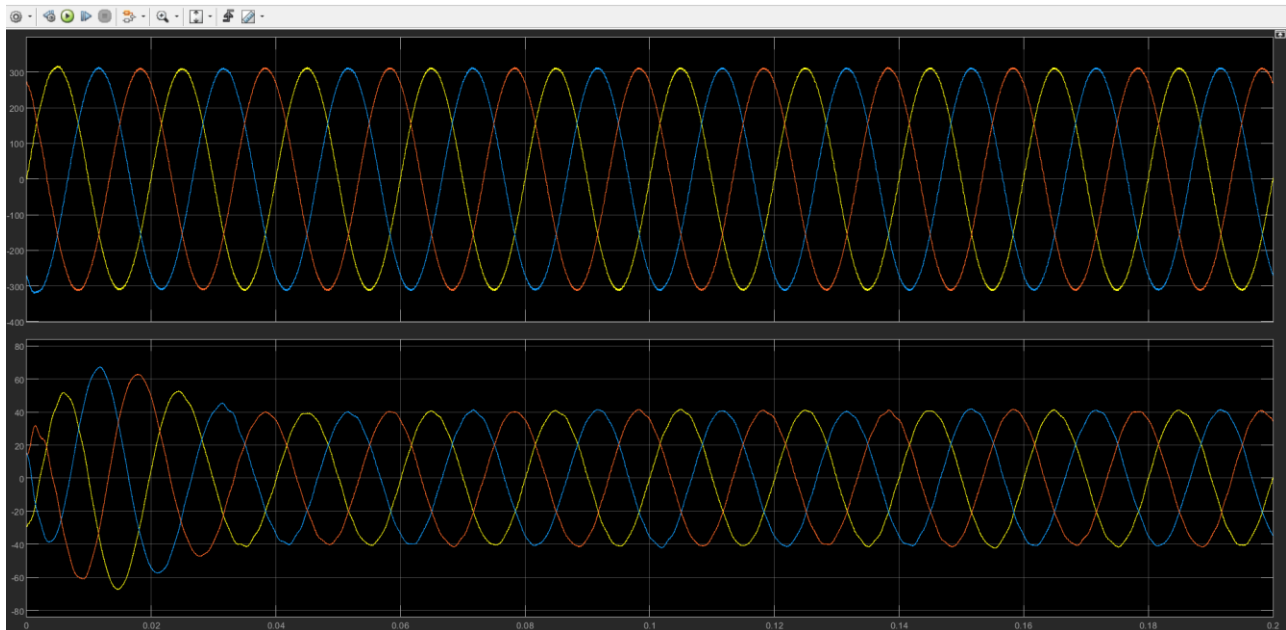
Figure 56-Inverter 2 output voltage and current

As stated in the literature review, circulating currents arise due to differences in frequency, amplitude, phase etc. To measure the circulating currents, a parasitic capacitance is connected in series between the negative poles of the DC buses. In this condition, since all the conditions are the same for both Inverters, the measured ZSCC is zero as expected.

Figure 57-ZSCC

The steps taken for current analysis are the same as one single inverter. This means, we start from transform of current from abc to dq0-axis. Figures below represent dq0-axis currents, errors, and voltage errors after the PI controller respectively.
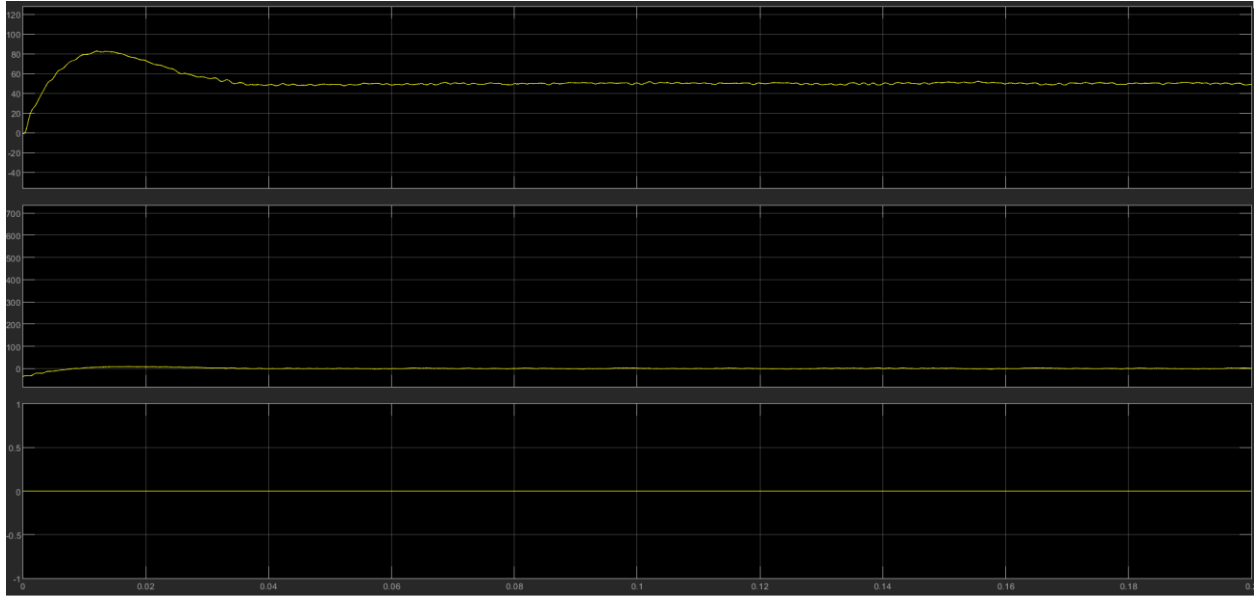
Figure 58-dq0 currents of inverter 1
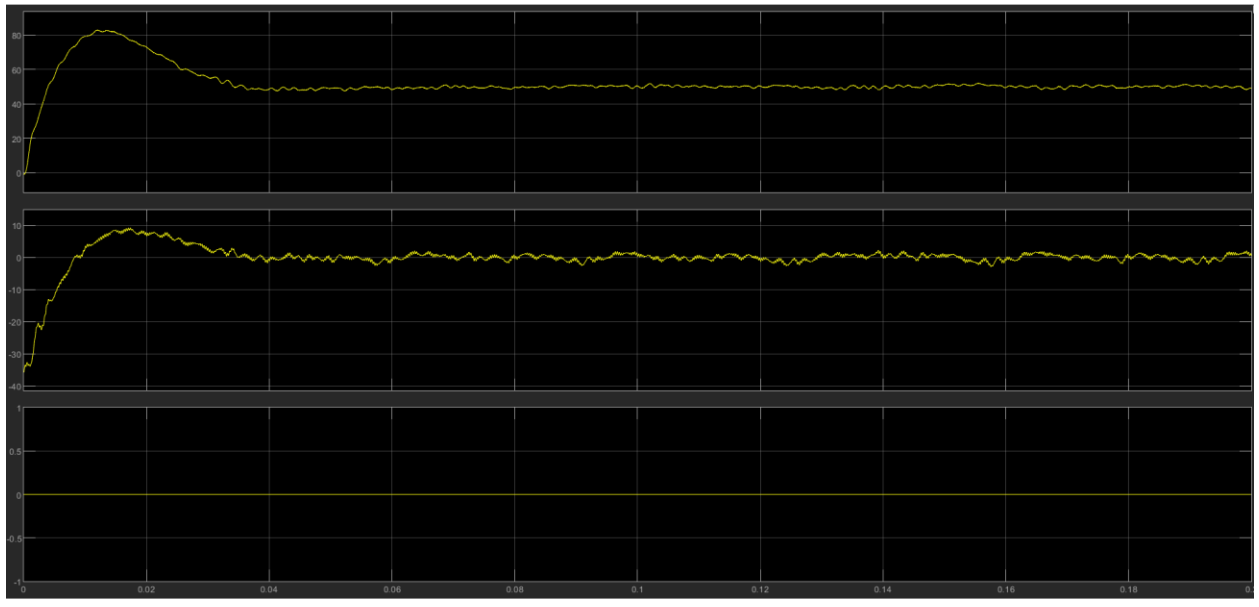
Figure 59-dq0 currents of inverter2
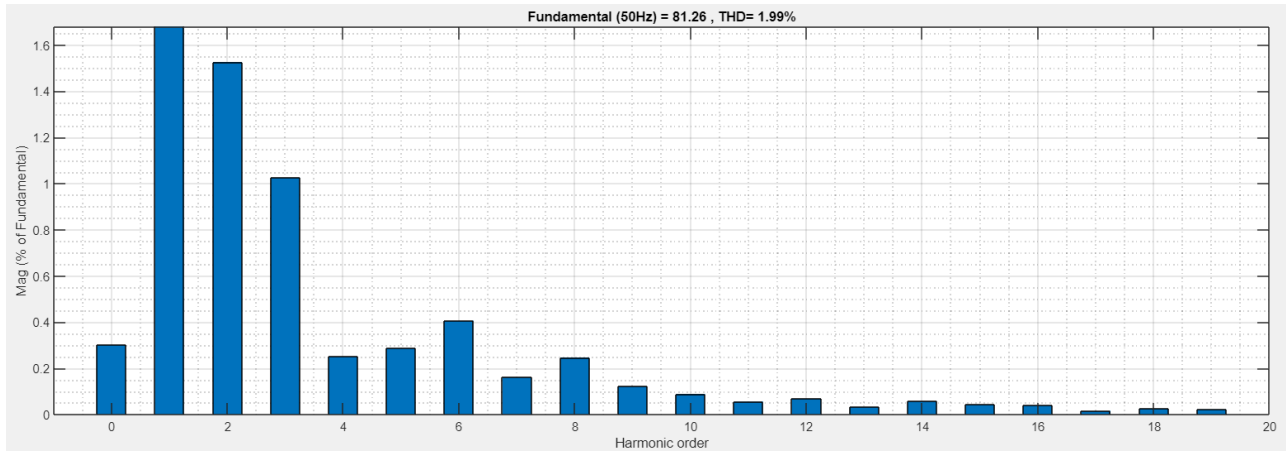
Figure 60-FFT analysis of 2L inverter with same frequencies and different DC buses

4.2.2   Difference in the frequency

In order to simulate a more real situation, a difference of 1Hz is imposed between the frequency of two inverters.

This change in the parameters, results in the ZSCC to circulate between the Inverters.
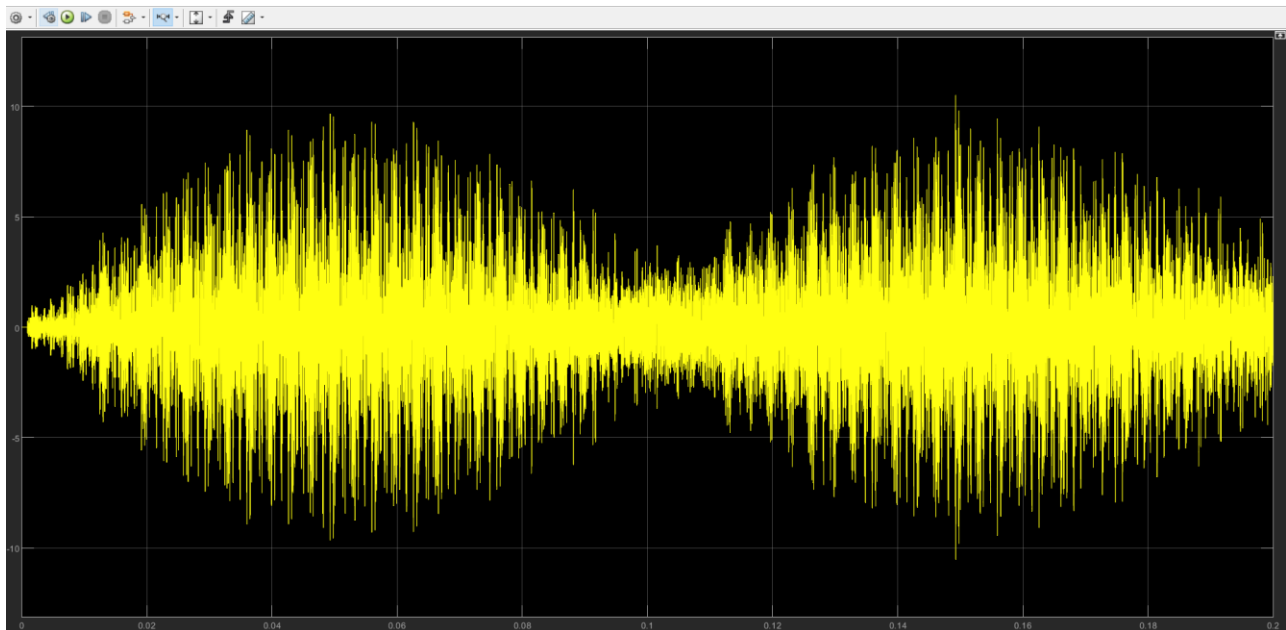
Figure 61-ZSCC with diff-frequency

The dq0 currents are shown the picture below.
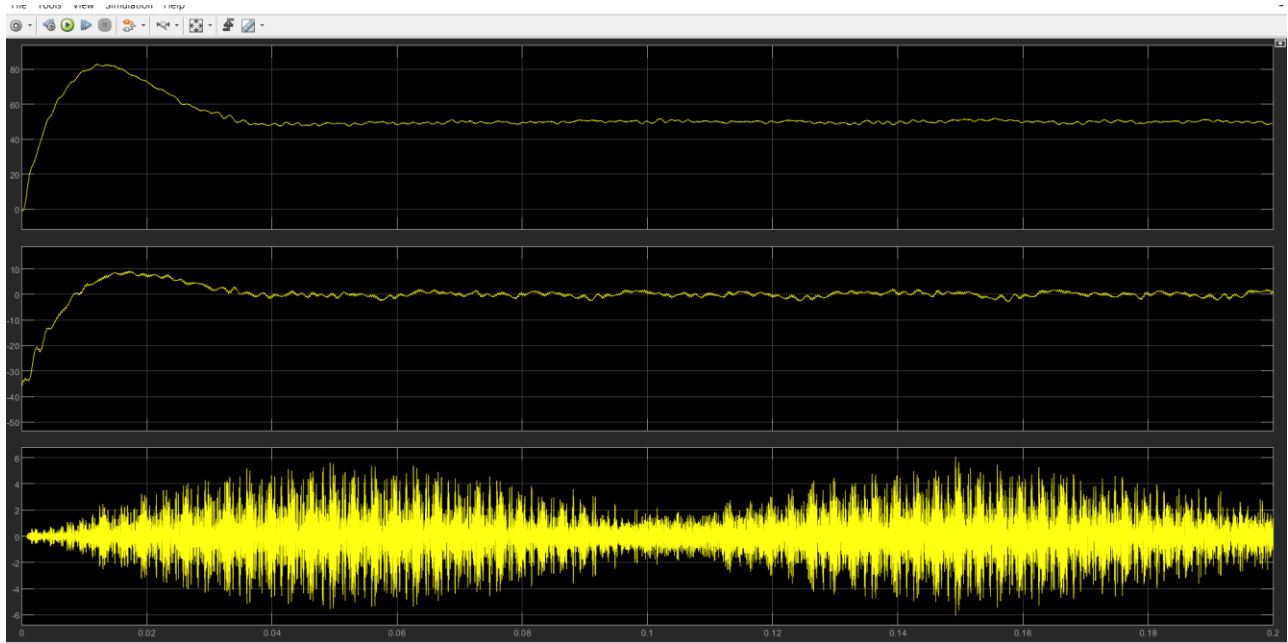
Figure 62-Inverter 1 dq0 currents

The homopolar current is not negligible anymore but due to the presence of the LCL filter and functional PI controllers, the grid side current and voltages aren't distorted.
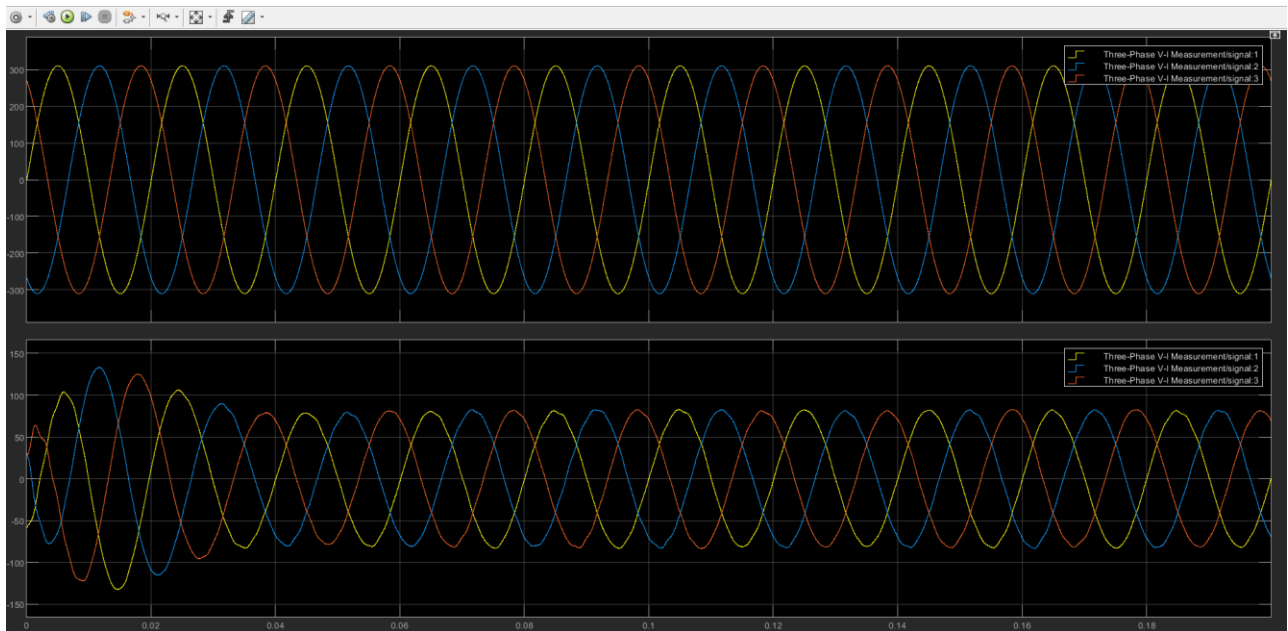
Figure 63-Grid Voltage and current

The dq0 voltage errors are also can be observed:
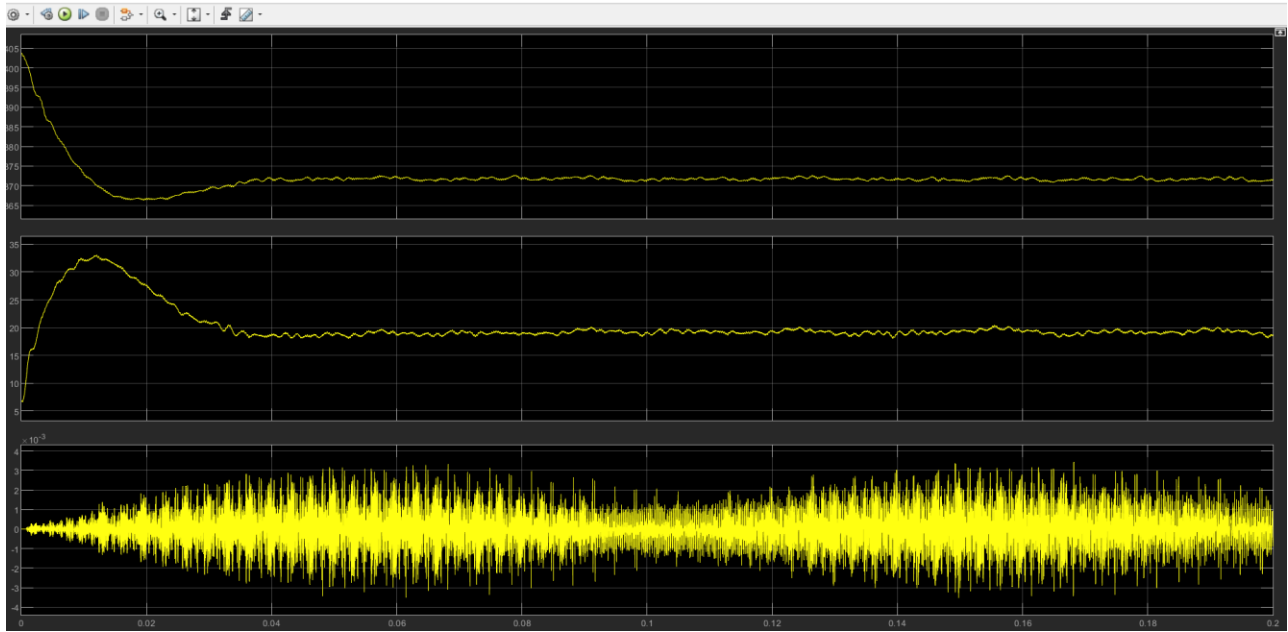
Figure 64-Inverter 1 dq0-voltage errors
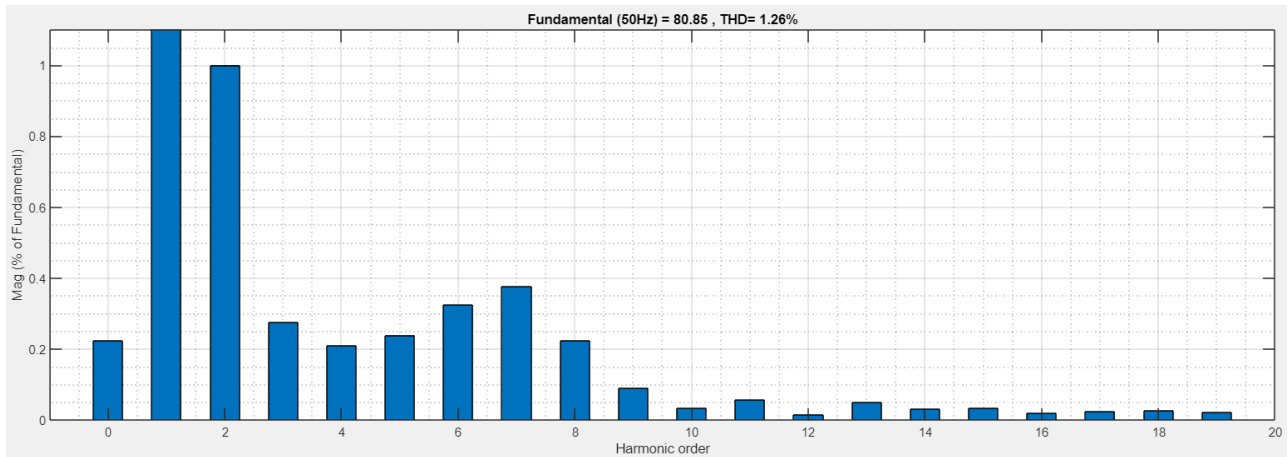
Figure 65-FFT analysis of 2L inverter with different frequencies and different DC buses

4.2.3   The equivalent model of two inverters in parallel

In this section, an equivalent model for two inverters in parallel is developed based on the homopolar point of view. Considering the fact that homopolar current doesn't pass through the capacitance, the capacitance Cf can be neglected in LCL filter.
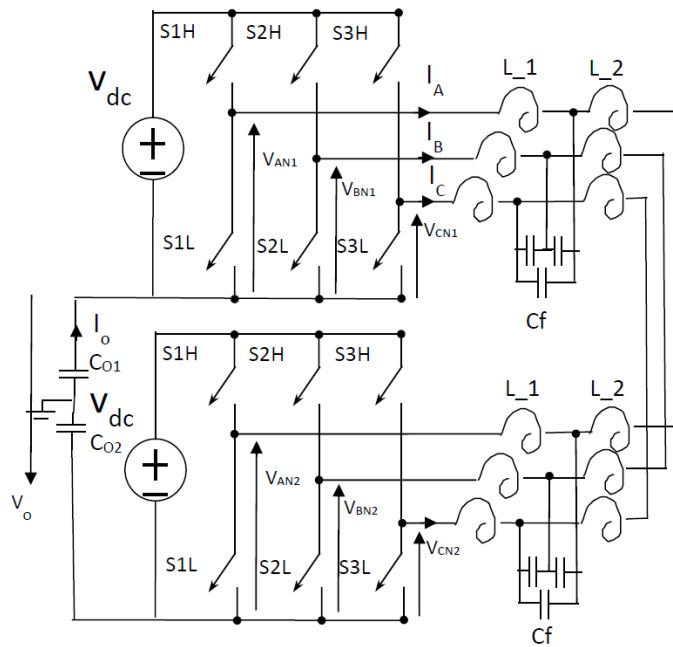
Figure 66-Model of two inverters in parallel

Consider that from homopolar point of view, the capacitances Cf do not appear.

Call Ltot the total inductance of a phase: L_1+L_2+L_2+L_1=2 L_1+2 L_2

Call CO=1/(1/CO1+1/CO2))

The KVL applied to the three phases

$$V_{AN1} - L_{tot}\frac{dI_A}{dt} - V_{AN2} - V_O = 0 \quad (4\text{-}1)$$

$$V_{BN1} - L_{tot}\frac{dI_B}{dt} - V_{BN2} - V_O = 0 \quad (4\text{-}2)$$

$$V_{CN1} - L_{tot}\frac{dI_C}{dt} - V_{CN2} - V_O = 0 \quad (4\text{-}3)$$

While KCL

$$I_O = I_A + I_B + I_C \quad (4\text{-}4)$$

And

$$I_O = C_O\frac{dV_O}{dt} \quad (4\text{-}5)$$

If you sum the three dynamic equations (KVL).

$$V_{AN1} + V_{BN1} + V_{CN1} - L_{tot}\frac{d(I_A+I_B+I_C)}{dt} - V_{AN2} - V_{BN2} - V_{CN2} - 3V_O = 0 \qquad (4\text{-}6)$$

Call

$$\frac{V_{AN1}+V_{BN1}+V_{CN1}}{3} = V_{O1} \qquad (4\text{-}7)$$

And

$$\frac{V_{AN2}+V_{BN2}+V_{CN2}}{3} = V_{O2} \quad (4\text{-}8)$$

Therefore

$$3V_{O1} - L_{tot}\frac{dI_O}{dt} - 3V_{O2} - 3V_O = 0 \quad (4\text{-}9)$$

Using eq (4.3)

$$3V_{O1} - 3V_{O2} = L_{tot}C_O\frac{d^2V_O}{dt^2} + 3V_O \quad (4\text{-}10)$$

If you consider Leq=Ltot/3

$$V_{O1} - V_{O2} = L_{eq}C_O\frac{d^2V_O}{dt^2} + V_O \quad (4\text{-}11)$$

But this dynamic equation is the same of the following circuit:

Figure 67-equivalent model of two-level inverter in parallel and the simulated model in MATLAB
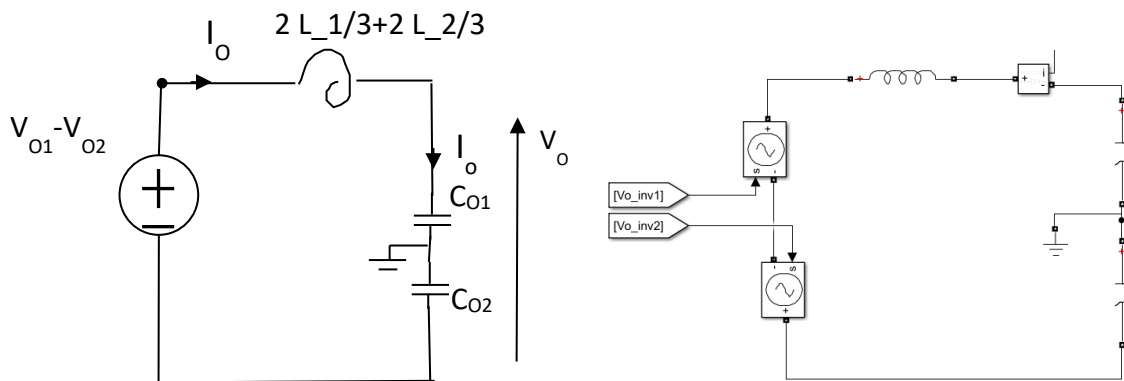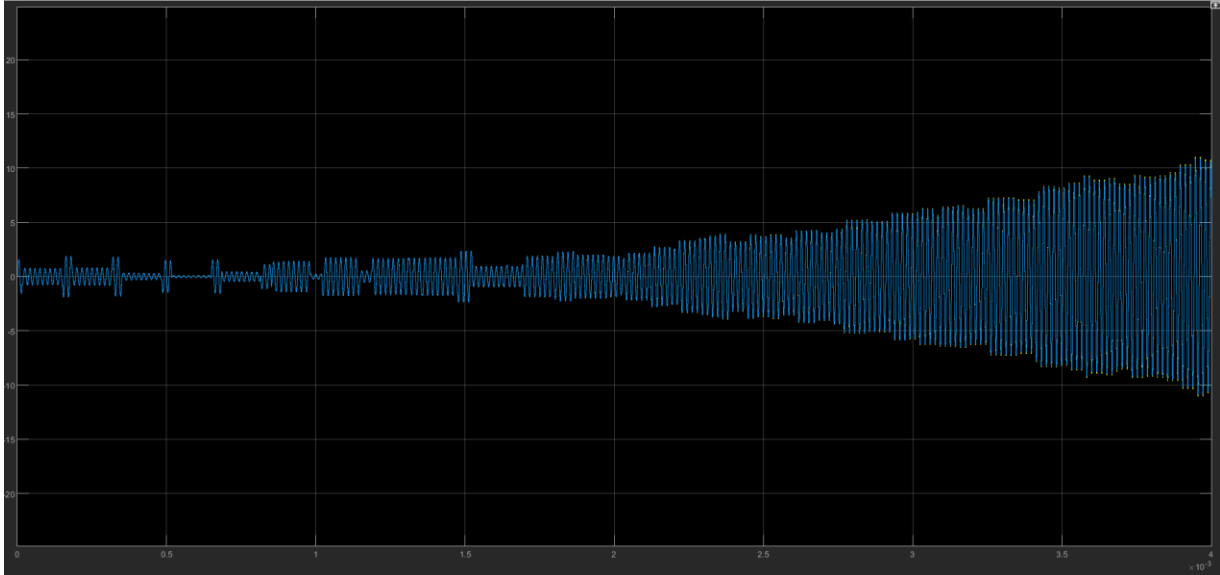
Figure 68a-Homoplar currents measured through the circuit and equivalent model
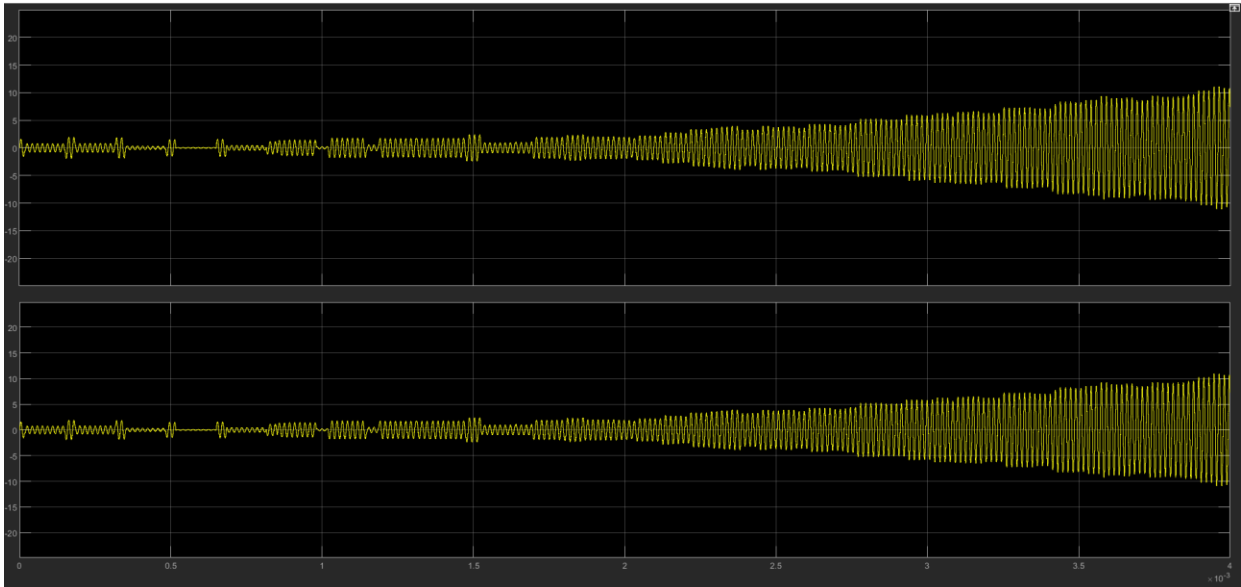
Figure 64b-Homoplar currents measured through the circuit and equivalent model

By running the simulation, it can be observed that the measured homopolar current in the equivalent model equal to the ones measured through parasitic capacitance in the actual circuit.

In the figure 69, the results of the spectrum analyzer are displayed. per expected, the homopolar current consists of both low frequency and high frequency components. Higher frequency components of the signal have a negligible power whereas the low frequency components of the signal have higher power. Consequently, high frequency components of the homopolar current can be neglected. when the homopolar current is passing through the LCL filter, the capacitance reactance is close to infinity and acts as the open

circuit while considering the only the low frequency components. As a result, since there is no current passing through the capacitance, the equivalent of LCL filter can be depicted as the series equivalence of inverter side and grid side inductances.
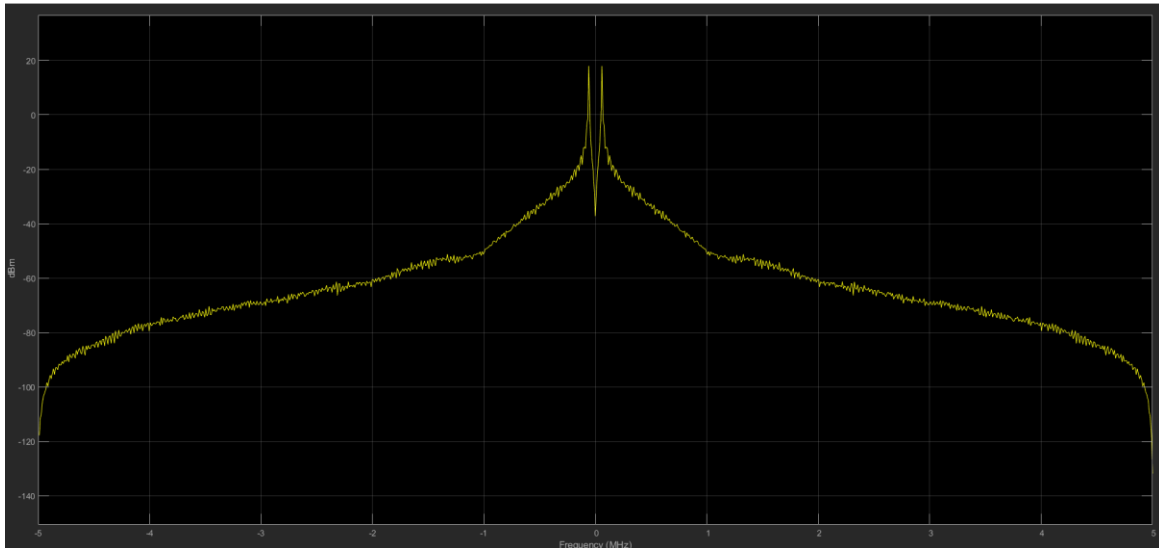
Figure 69-Spectrum analyzer

4.2.4   Two-level inverter in parallel with same DC bus

In this section, the behavior of the system with regards to the same DC bus is observed. Two inverters are connected in parallel with the same DC bus and the same frequency. The power delivered to the grid is twice the single inverter.
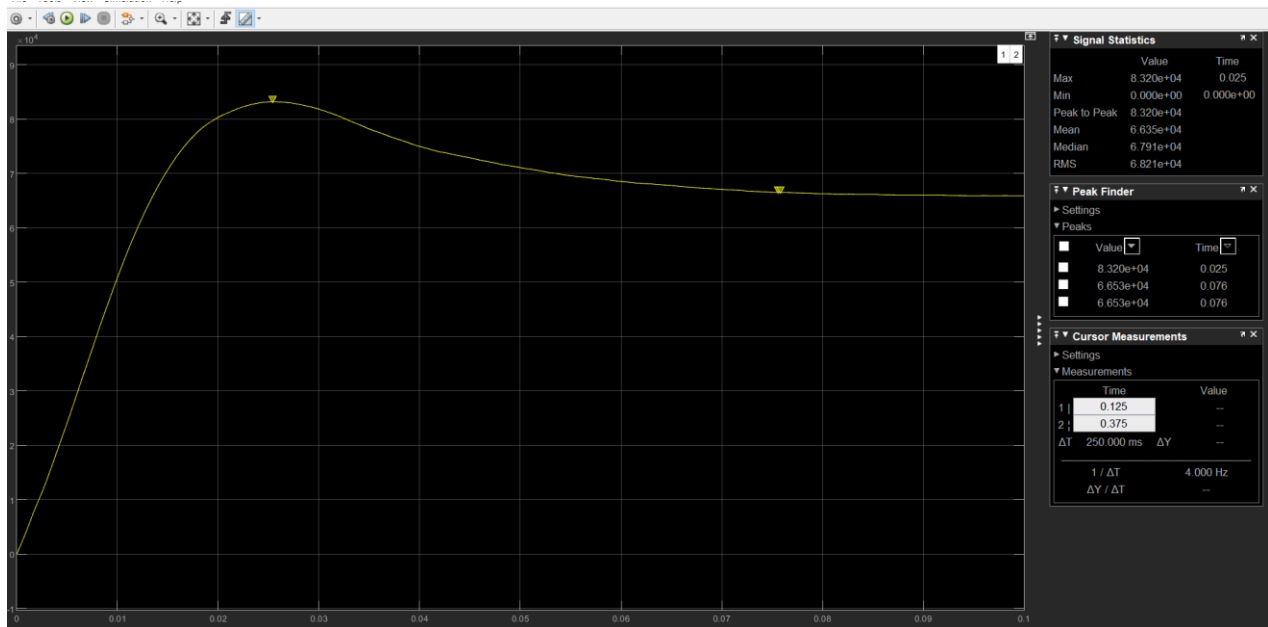
Figure 70-Power Delivered to the grid

The line voltage and currents are measured on the grid side. As expected, the phase current and voltage are in phase to each other, and the current delivered to the grid is the sum of each inverter.
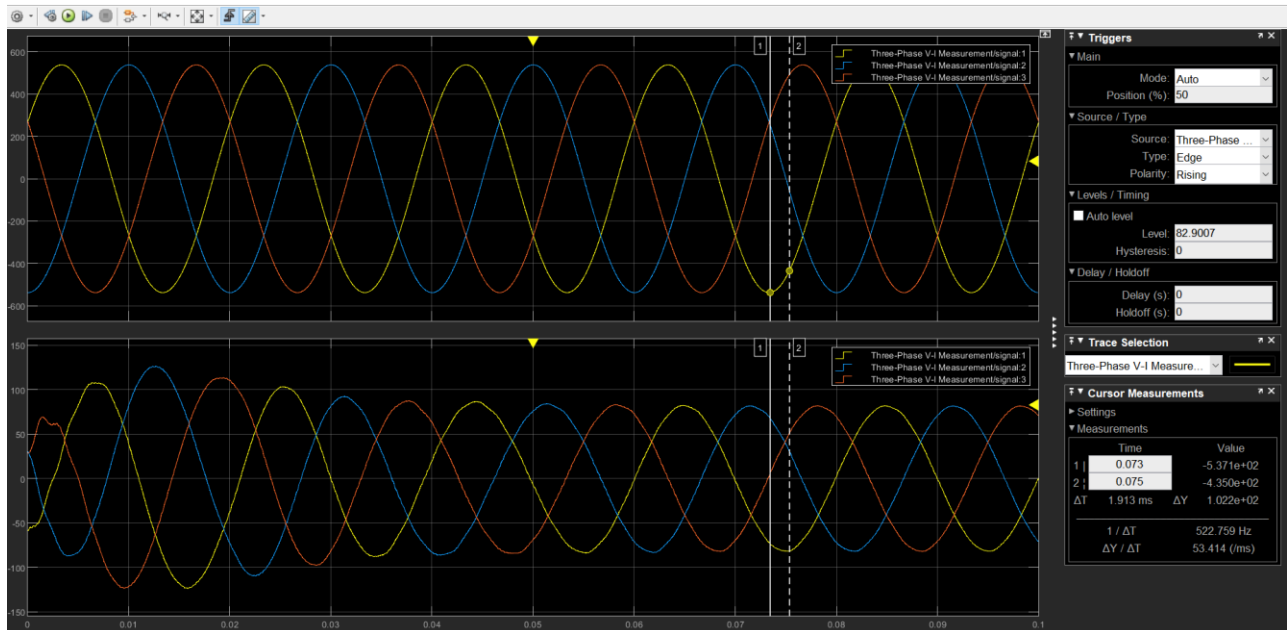
Figure 71-Line Voltage and currents

A step-by-step analysis of the current is given. Current is measured by the three-phase measurement block.
By Clarke transformation, the three phase currents are transformed from abc reference frame to the dq0 axis.
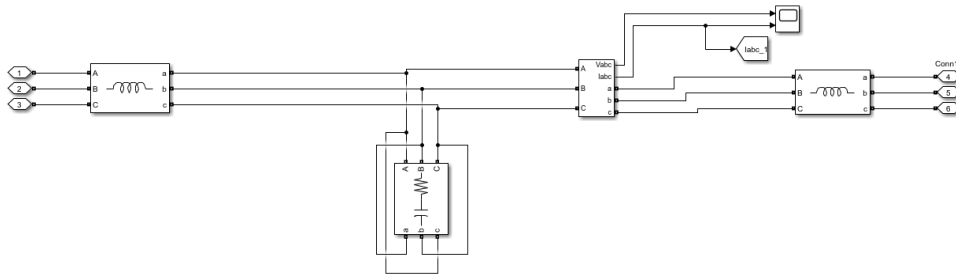
Figure 72-Current measurements

```
function y = fcn(ua,ub,uc,wt)
%%Id = 0;
%%Iq = 0;
%%I0 = 0;

K= sqrt(2/3);

T0 = K*[cos(wt) cos(wt-((2*pi)/3)) cos(wt+((2*pi)/3)); -sin(wt) -sin(wt-((2*pi)/3)) -sin(wt+((2*pi)/3));1/sqrt(2) 1/sqrt(2) 1/sqrt(2)];

T1 = [ua;ub;uc];

y = T0 *T1;
```

Figures below represent dq0-axis currents. There is a transient at the beginning and after a while the waveforms reach the stead state.
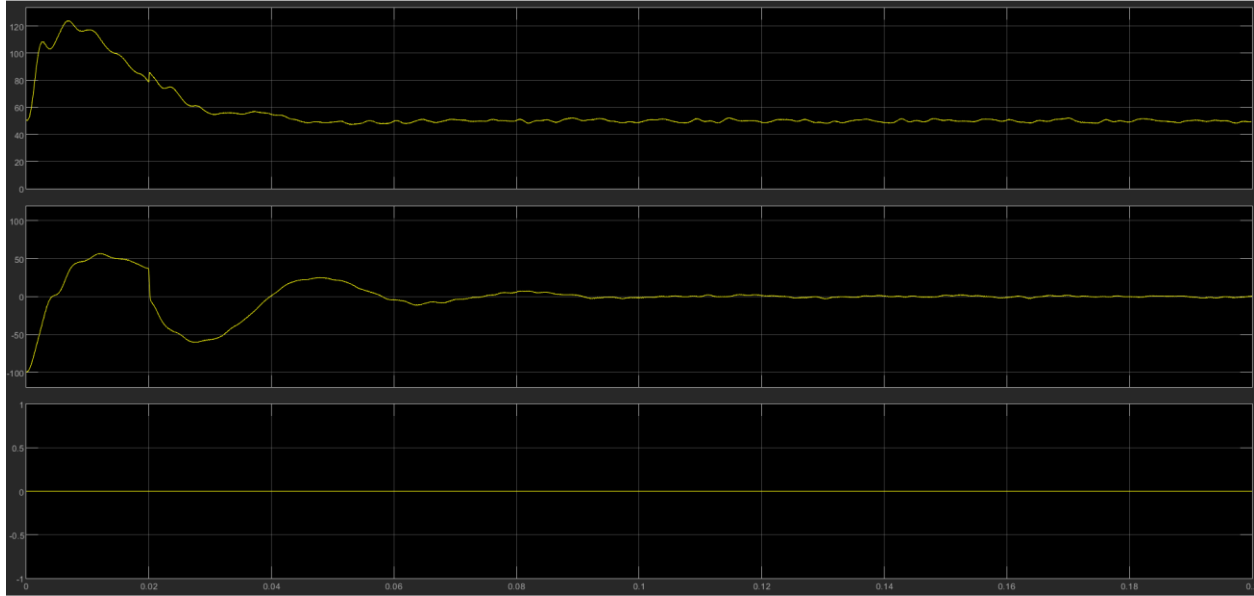
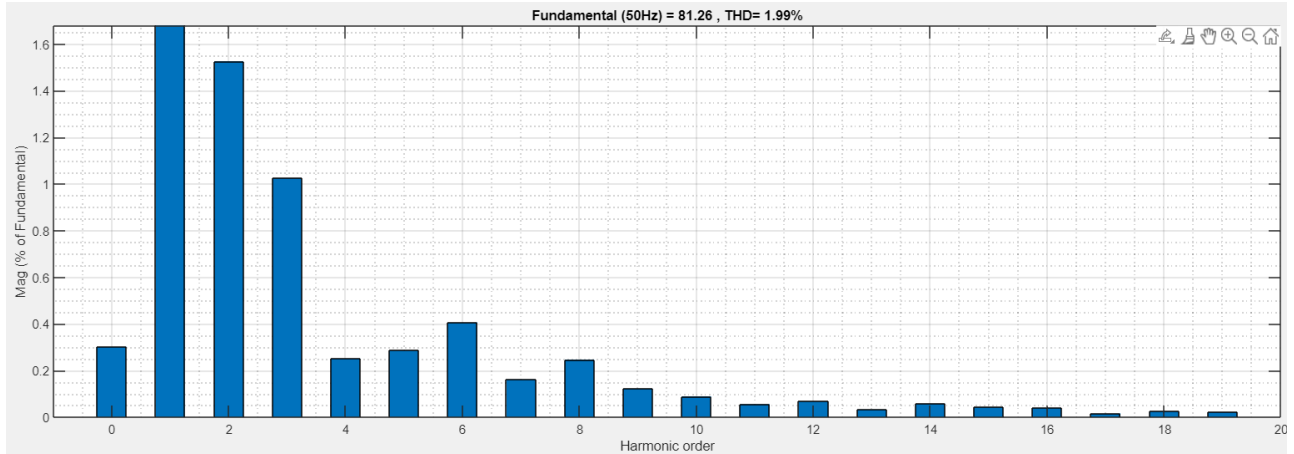Figure 73-dq0 currents of inverter1
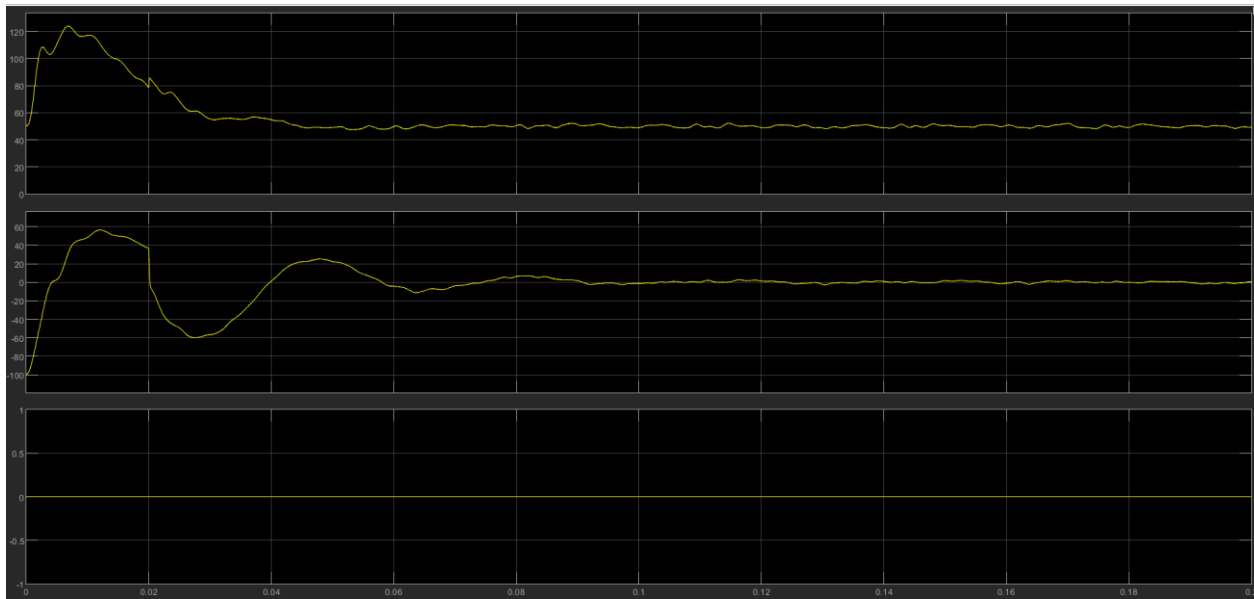
Figure 74-dq0 currents of inverter 2

Figure 75-FFT analysis of 2L inverter with the same DC bus and same frequencies

4.2.5   Two inverters in parallel with the same DC bus and different frequencies

In this section, the effect of the frequency difference between two inverters is studied. For these matters, the frequency of the inverter two is set to 3001Hz.

Following figure shows the grid line voltage and currents. As expected, the phase voltage and currents are in phase which shows the PI controllers are working correctly.
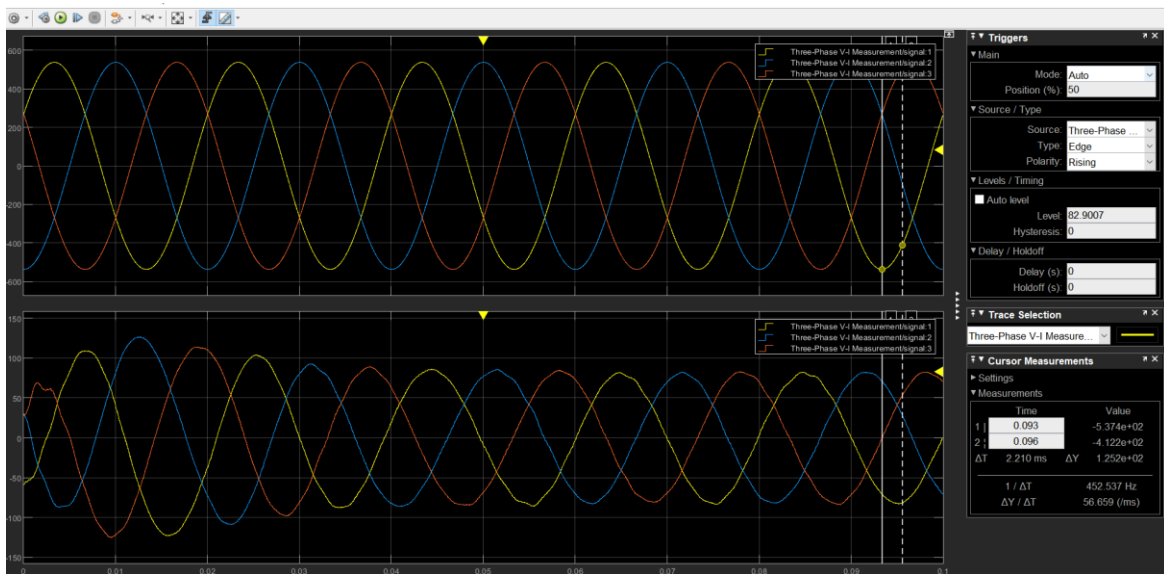
Figure 76-line voltage and currents

The power delivered to the grid is twice the power of one inverter.
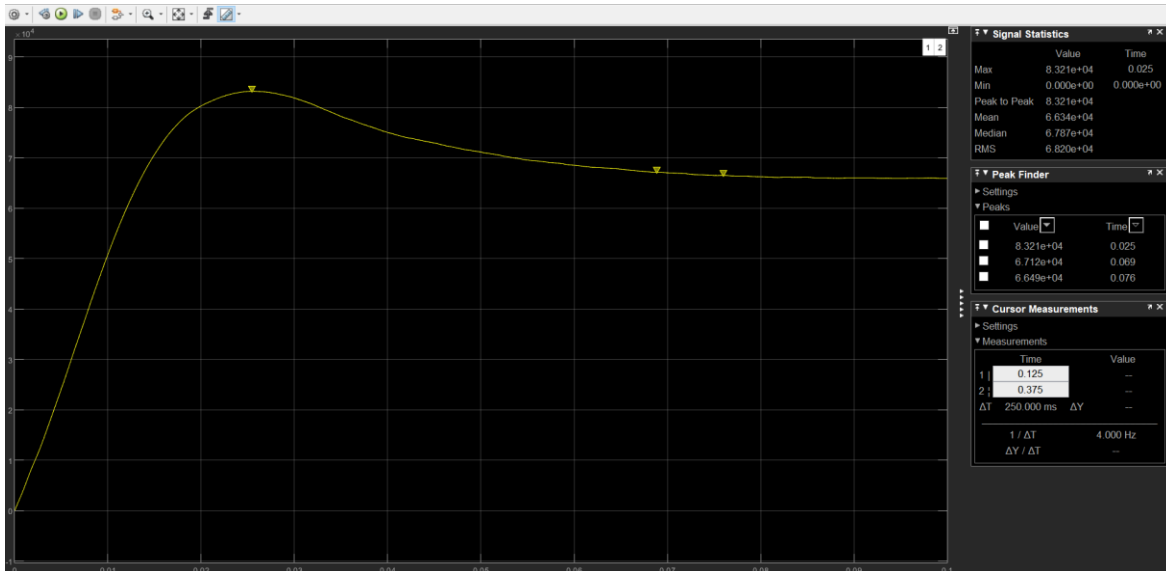
Figure 77-Power delivered to the grid

As an example, the dq0 currents of inverter one is shown. The homopolar current is no longer negligible.

There is a transient at the beginning but after a while dq currents go to stable state.
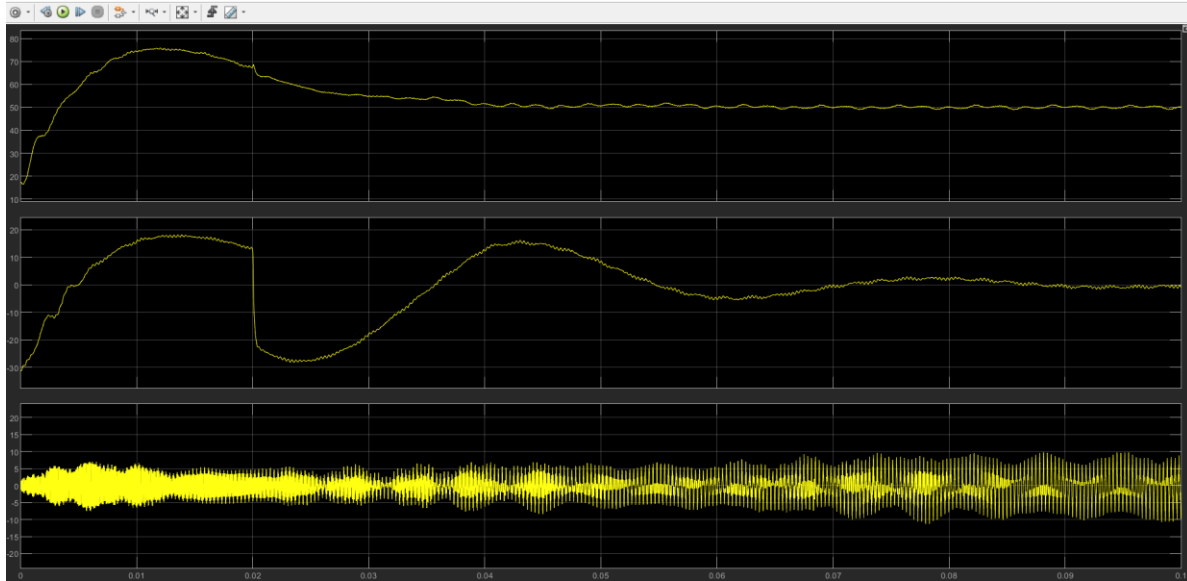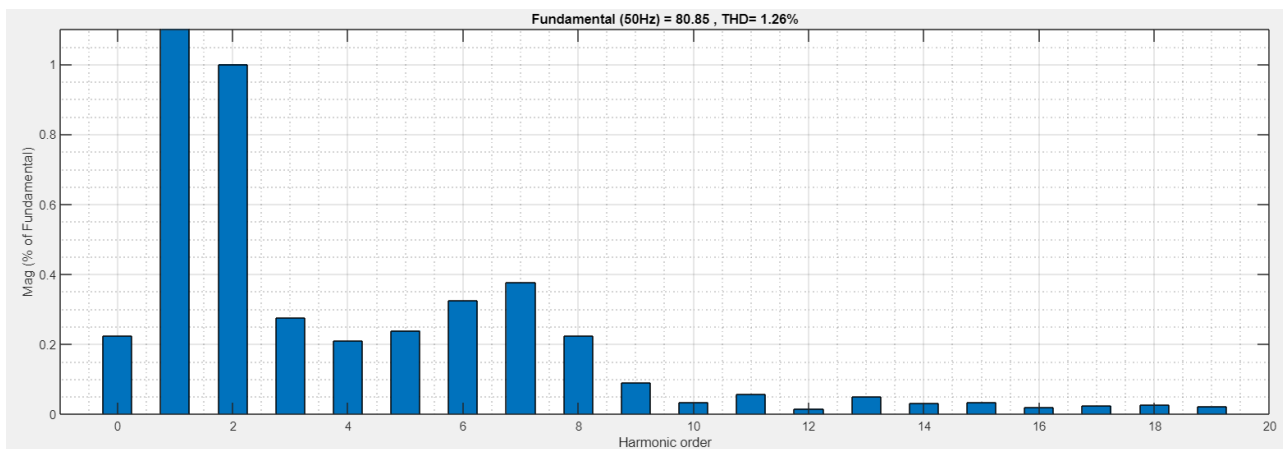
Figure 78-dq0 currents of inverter 1

Figure 79-FFT analysis of 2L inverter with the same DC bus and different frequencies

4.2.6   CMV Reduction Method for two level inverters

As stated before, CMV is defined as the voltage between the star point of the load and supply ground. It can be expressed as Vcm = (Vao+Vbo+Vco)/3. Since VSI cannot provide actual sinusoidal voltages and has pulsed output voltages synthesized from the DC bus voltage Vdc, the CMV is always different from zero and takes the values of +-Vdc/6 or +- Vdc/2 depending on the inverter switch state. This cause CMV with sharp edges that can result in high leakage current.
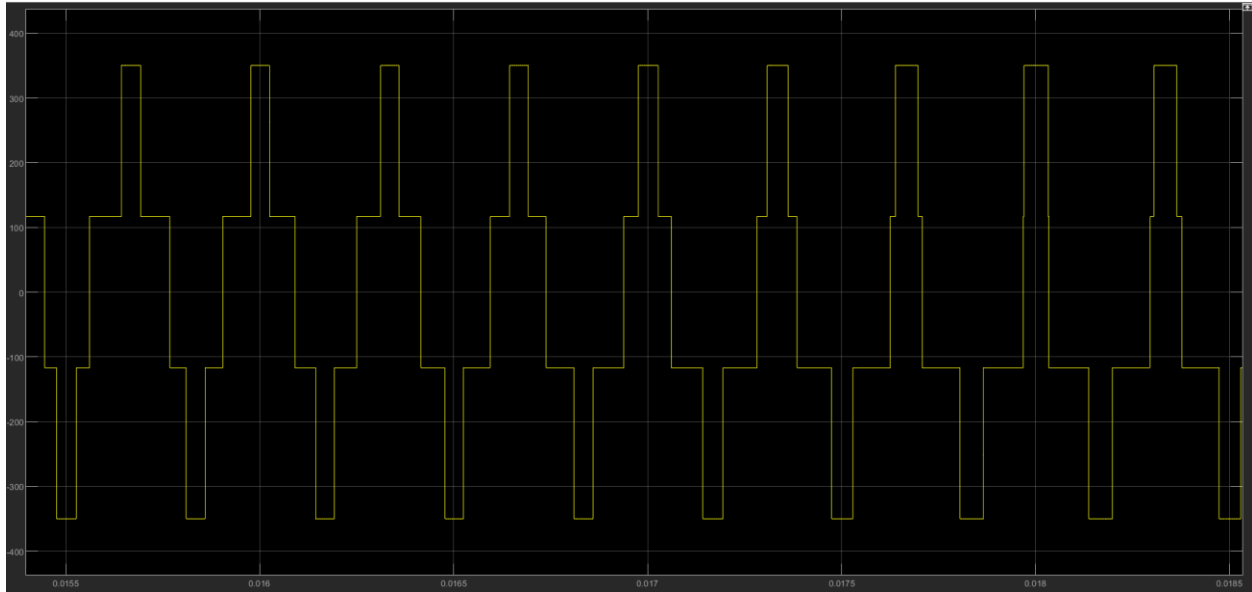
Figure 80-CMV of one inverter

There are many hardware solutions to reduce CMV while as a cost-effective solution, the appropriate design of PWM technique. In this thesis, Active zero state PWM technique which is a modification of the conventional SVPWM has been chosen to minimize CMV which is explained in detail in appendix.

In the Figure 75, the modulation waveforms as the result of AZSPWM in comparison with the change of the sector and the carrier signal is presented. In this method, zero vectors are replaced by the two opposite neighboring vectors. The details are explained in the appendix 7.3.
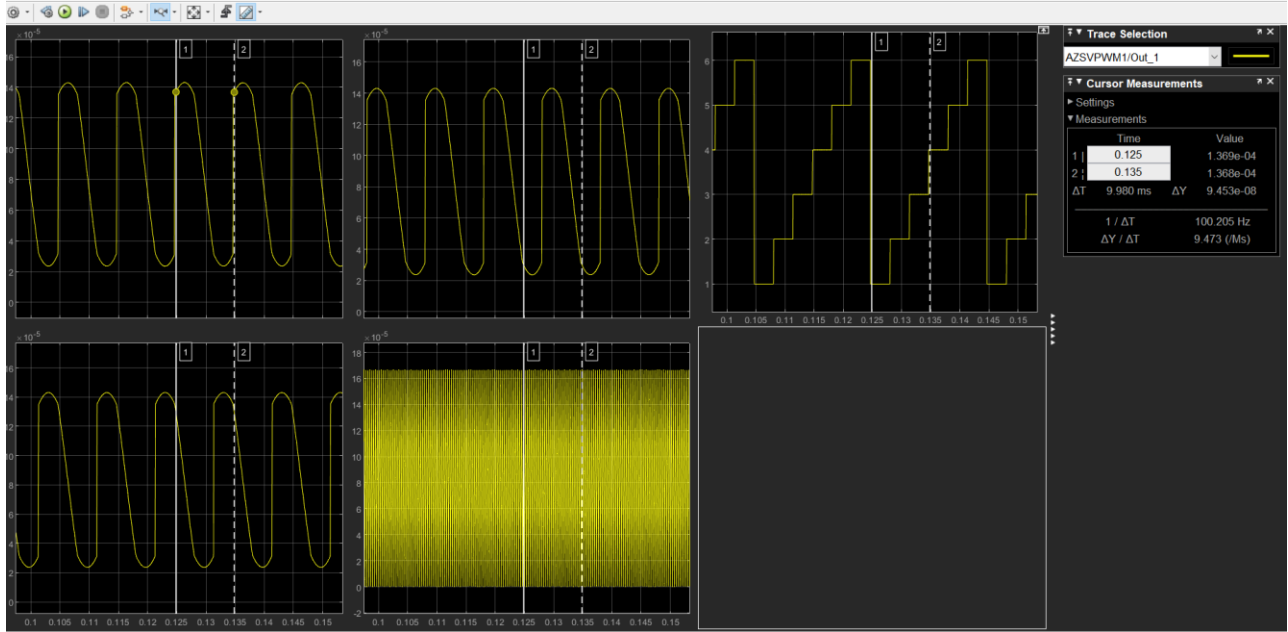
Figure 81-PWM waveforms of AZSPWM

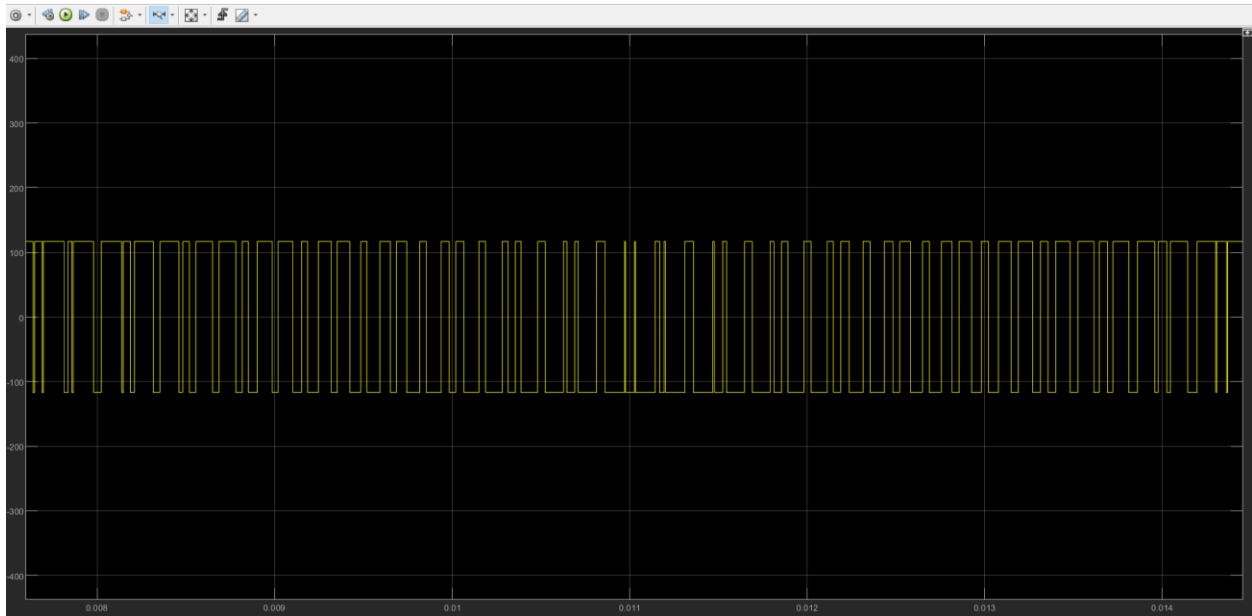As a result of this technique, the CMV has been decreased and the peaks of it is avoided.

Figure 82-CMV reduction using AZSPWM

The line voltage and currents on the grid side is presented in the case of single grid-connected inverter. The is no phase difference between the phase voltage and currents and the PI controllers are still able to function properly.
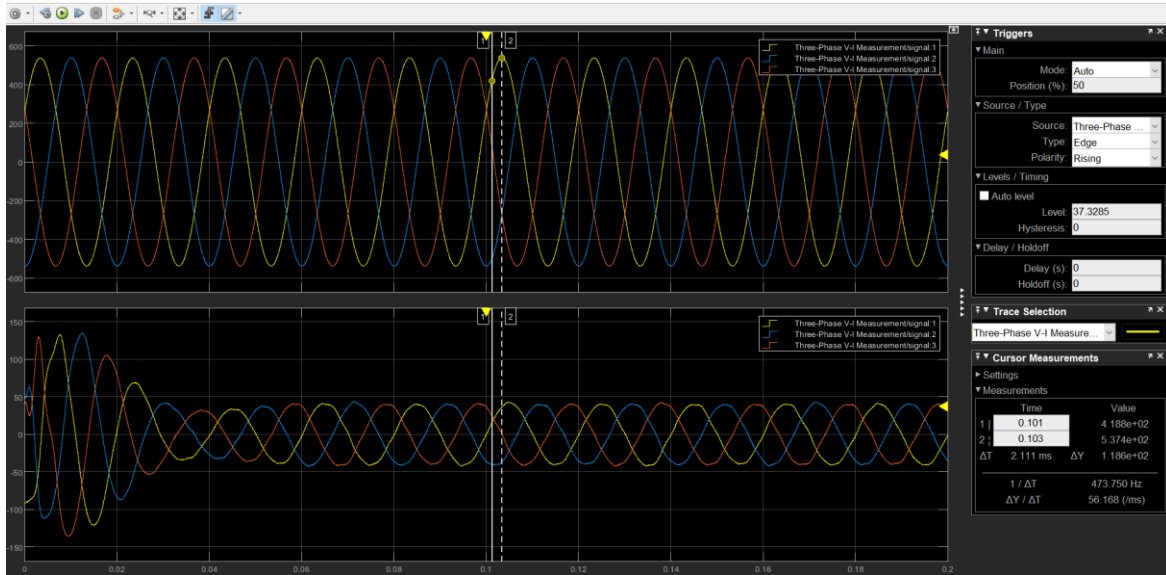
Figure 83-Line voltage and currents with AZSPWM

4.2.6.1   AZSPWM with two inverters in parallel

To proceed with the aim of two inverters in parallel, the first inverter is connected to the grid with conventional PWM technique, and the second inverter is connected using the AZSPWM technique. To simulate a condition closer to the reality, inverter 2 frequency is set a 1 Hz higher than inverter1.

It is observed that compared to inverter 1, the CMV of inverter 2 is reduced and the peaks have been avoided.
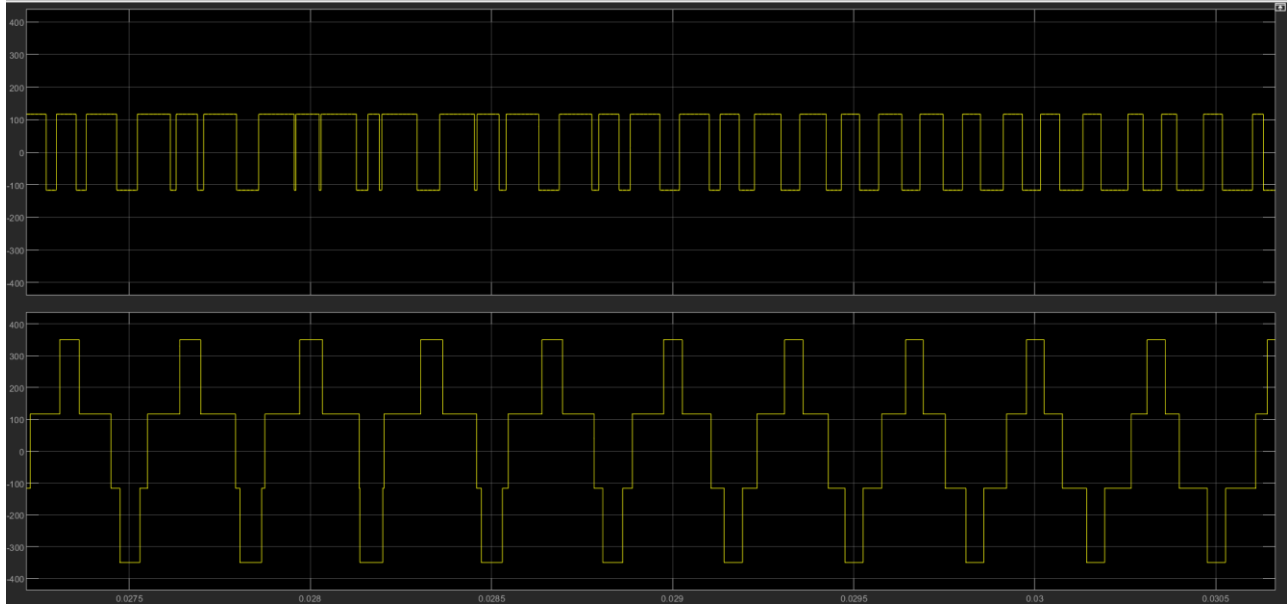
Figure 84-CMV1 compared to CMV2

The PI controllers are still able to follow the current and this results in the three-phase output current to be in phase with each other. Since two inverters are connected in parallel, the current on the grid side is the sum of each inverter.
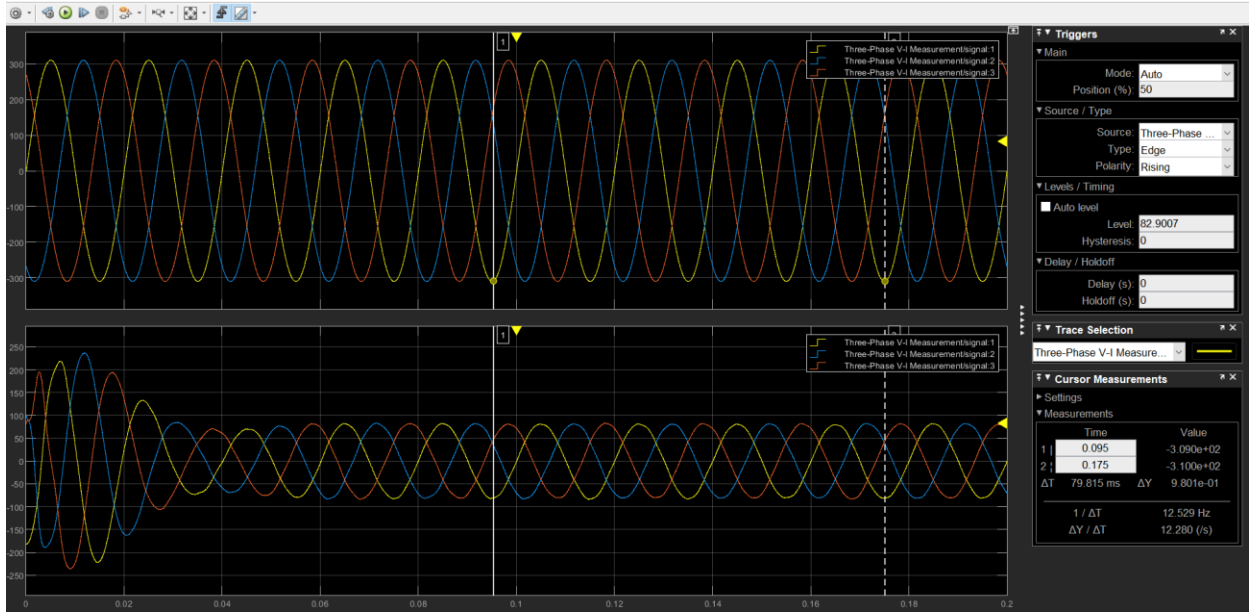
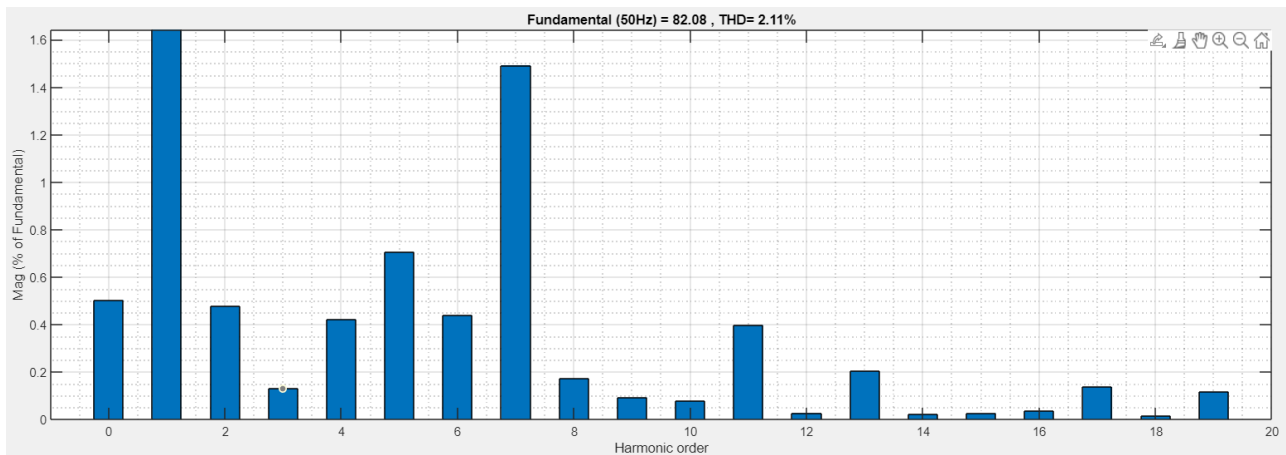Figure 85- Line voltage and currents with AZSPWM

Figure 86-FFT analysis of AZSPWM with different frequencies and different DC buses

Table 4-THD comparison between the conventional method and AZSPWM,2L Inverter

Objective	Condition	Current delivered to the grid
THD of Conventional PWM method	Different DC Bus	1.26%
THD of AZSPWM method		2.11%

The zero circulating currents measured with this method shows a slight reduction compared with the conventional method:
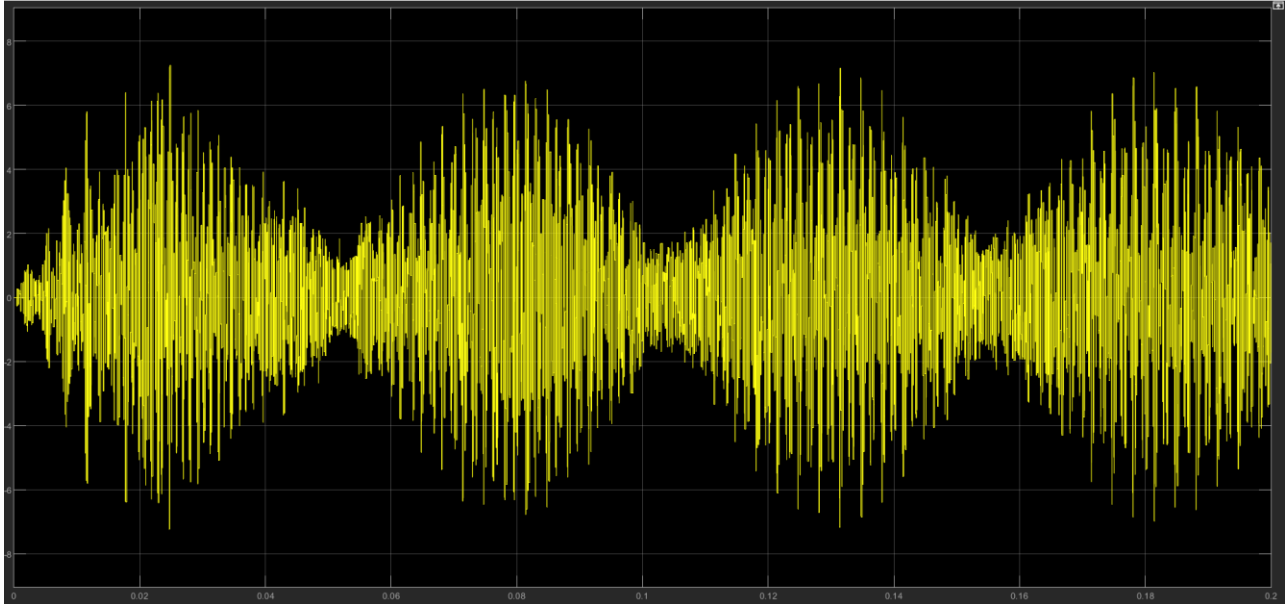
Figure 87-ZSCC of AZPWM

Table 5-ZSCC comparison between the conventional method and AZSPWM,2L Inverter

Objective	Condition	ZSCC
Conventional PWM method	Different Frequency Different DC Bus	<10
AZSPWM method		<8

4.2.6.2   Common DC-bus

In the case where two inverters are in parallel both on AC and DC side, the CMV is again measured, and the success of the method is observed:
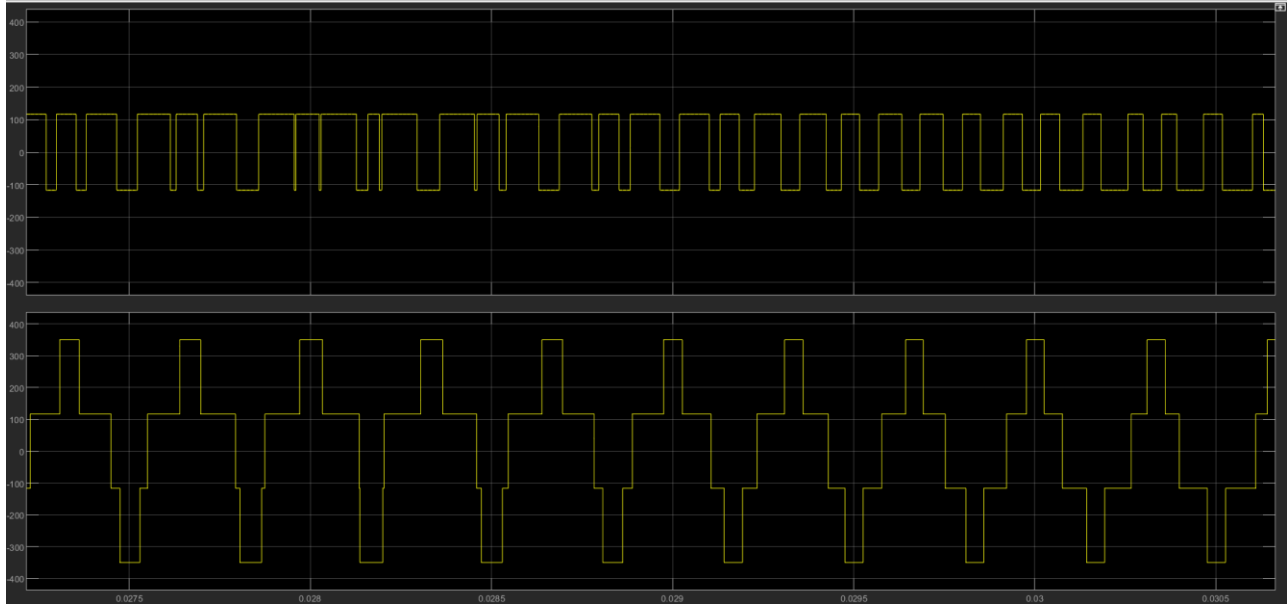
Figure 88-CMV2 and CMV1-same DC bus

The THD is measured for both the case with the same and different frequencies and the measured values are compared with the conventional method:
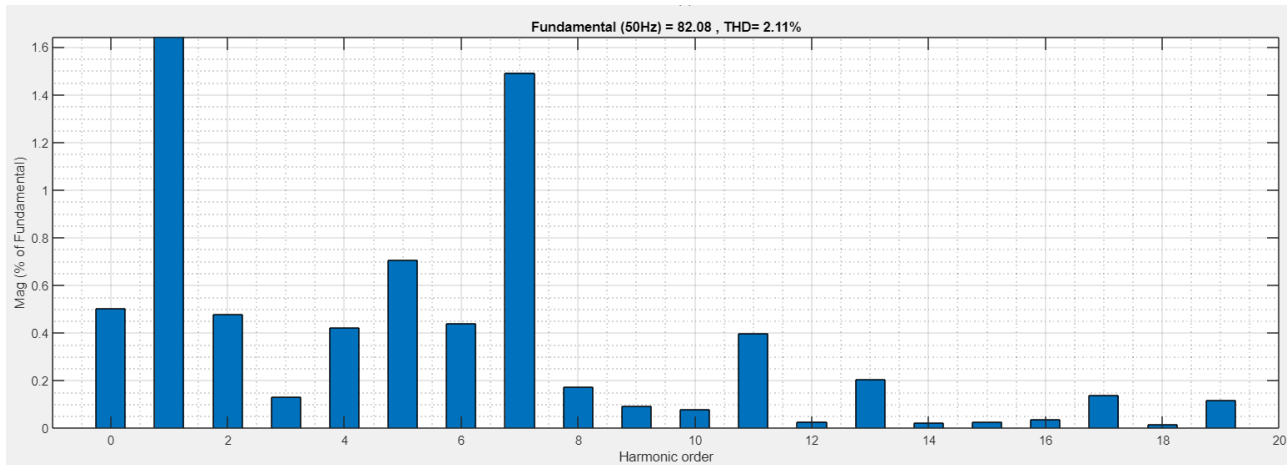

Figure 89-FFT analysis for the same DC bus and different frequencies for AZSPWM

Table 6-THD comparison between AZSPWM and the conventional method for 2L inverters in case of the same DC bus

Objective	Condition	Current delivered to the grid
THD of Conventional PWM method	Different Frequency Same DC Bus	1.99%
THD of AZSPWM method		2.11%

It is observed that the THD in both cases is less than 3% which satisfies the requirements by the grid. As observed in the tables above, this method has a slightly higher THD compared with the conventional method.

In both cases, the PI controllers are able to maintain the currents delivered to the grid to the desired value and phases.
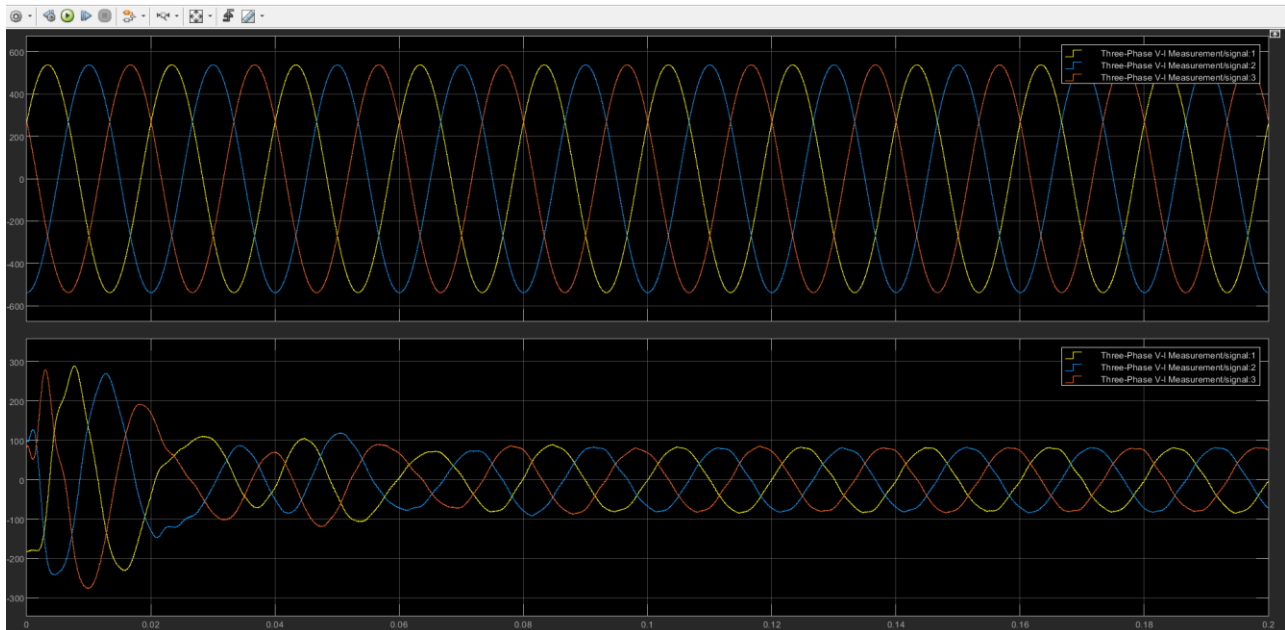

Figure 90-Output currents and voltages with the same DC bus

4.3 Three-level in parallel

The same procedure as for the two-level inverter has been taken to connect two three-level inverters in parallel.

As the first step, the two inverters are connected in parallel with the same AC bus but different DC buses.

The reference current is 50A and the frequency of the two inverters are 3kHz.

The current delivered to the grid is the sum of the two currents of each inverter and the phase voltage and currents are in phase with each other.
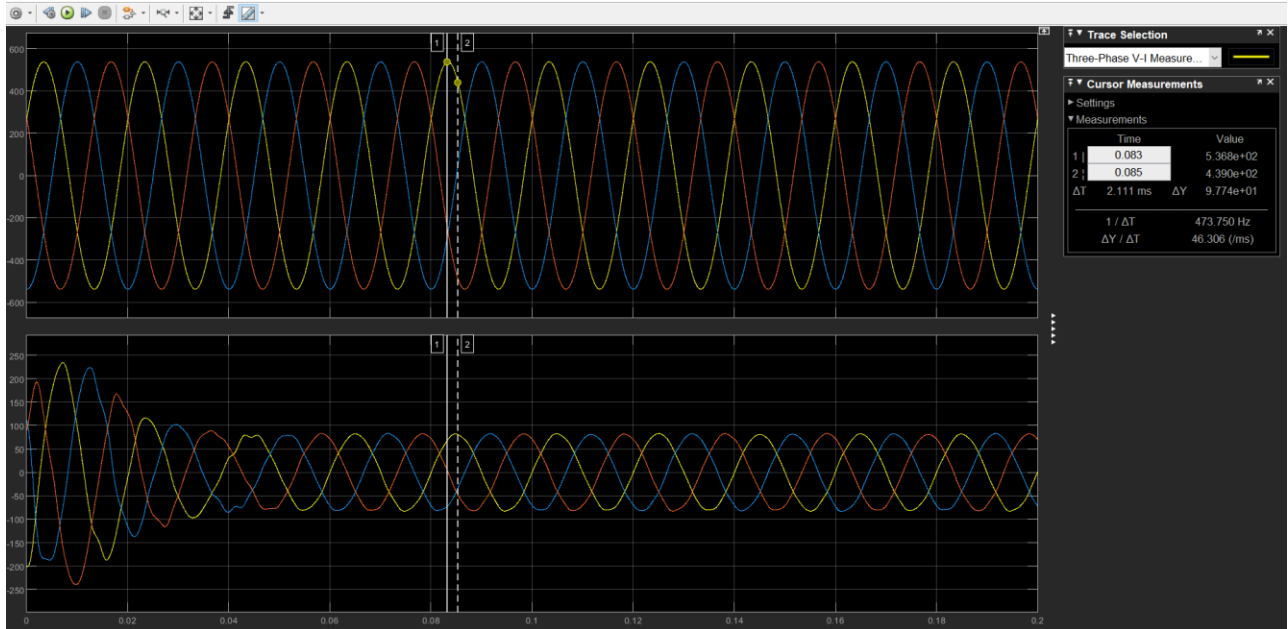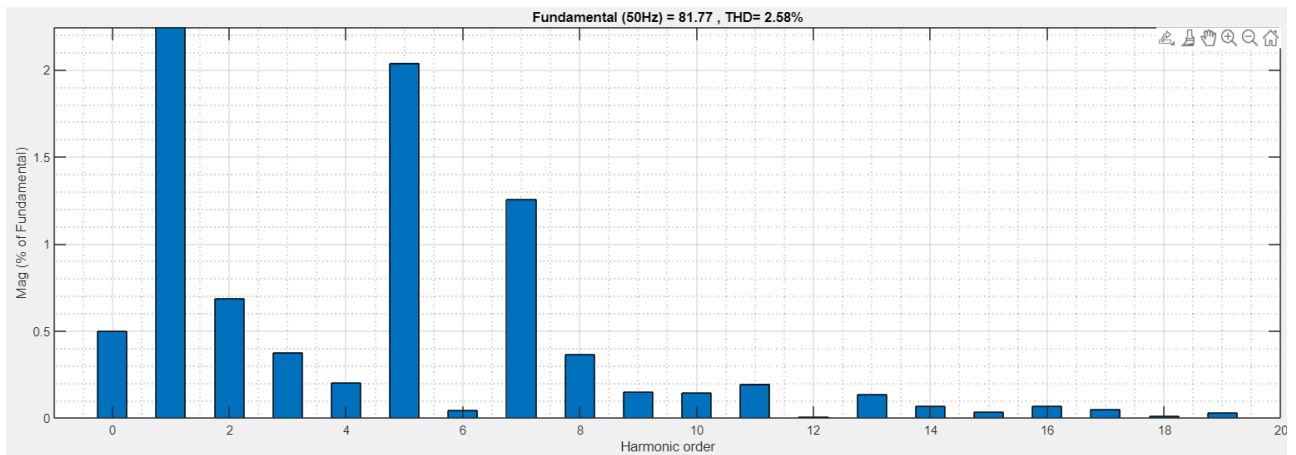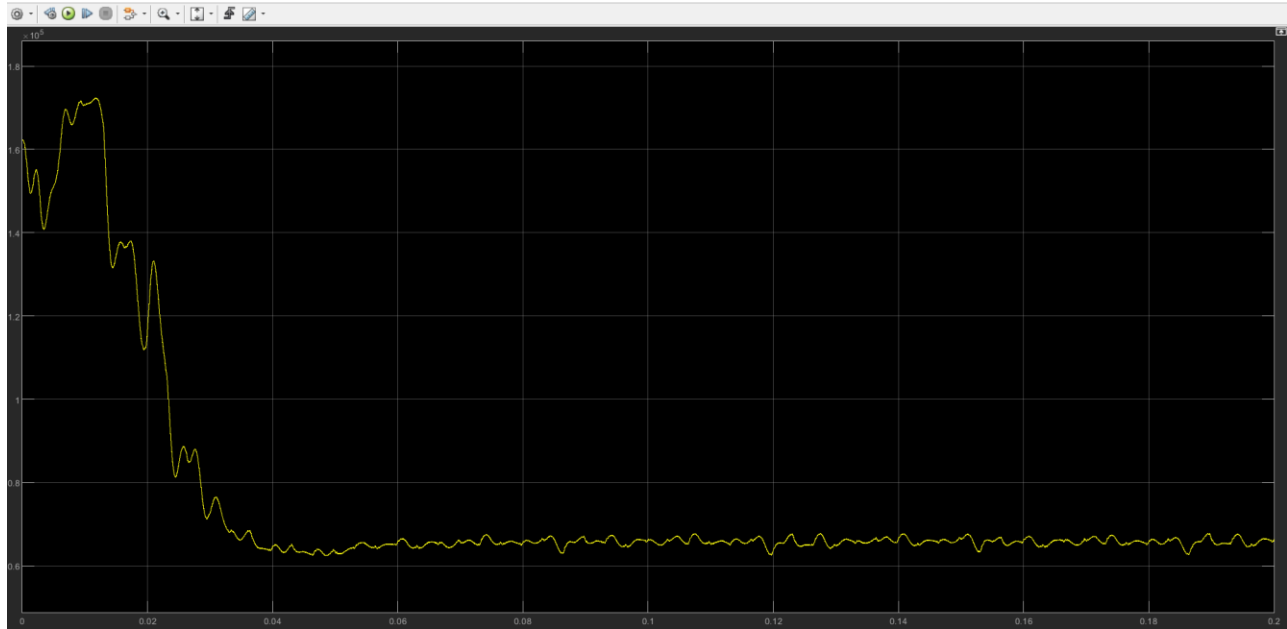
Figure 91-Line voltage and currents

Figure 92-Grid currents FFT analysis

The power delivered to the grid is twice the power in single inverter.

Since the conditions of both inverters are the same, the measured ZSCC current through the parasitic capacitance is zero.

4.3.1 Two-inverters in parallel with different DC bus and different frequency

As the next step, the frequency of the second inverter differs by 1 Hz from the first inverter. Since the conditions of the two inverters don't match each other anymore, zero sequence circulating currents will flow between the two inverters and it's measured through the parasitic capacitance connected to the negative terminals of the DC buses.
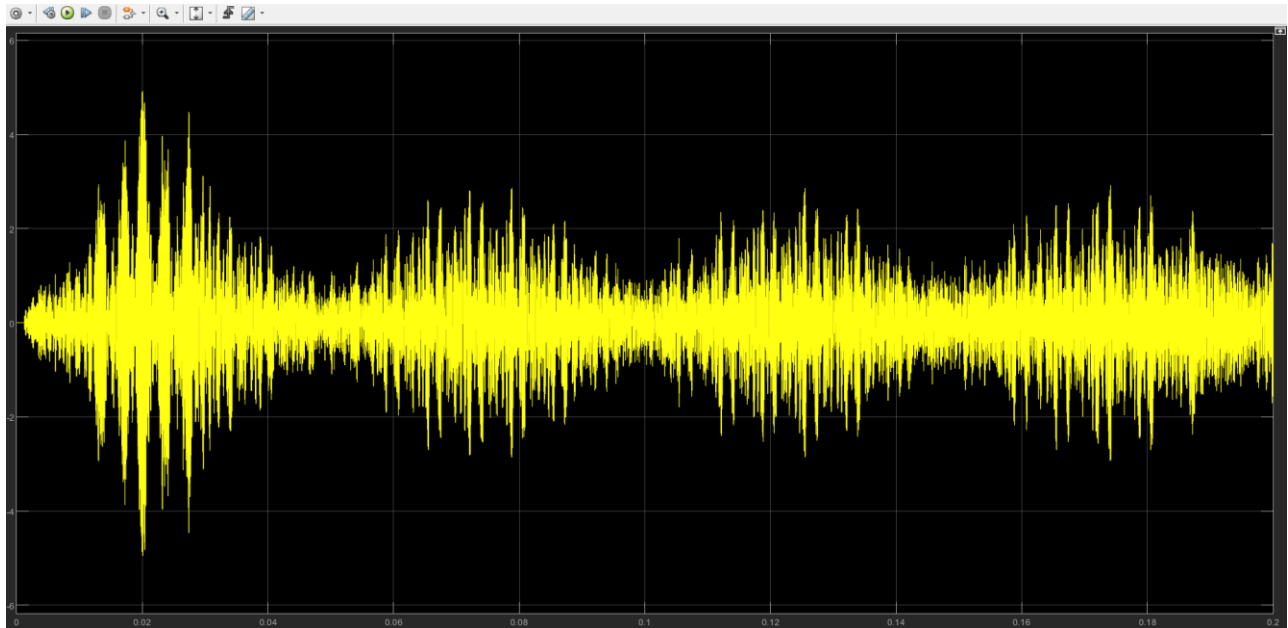
Figure 93-ZSCC with frequency difference

The controller is still able to function properly as the phase voltage and currents are in phase with each other although the frequency differs from one inverter to another.
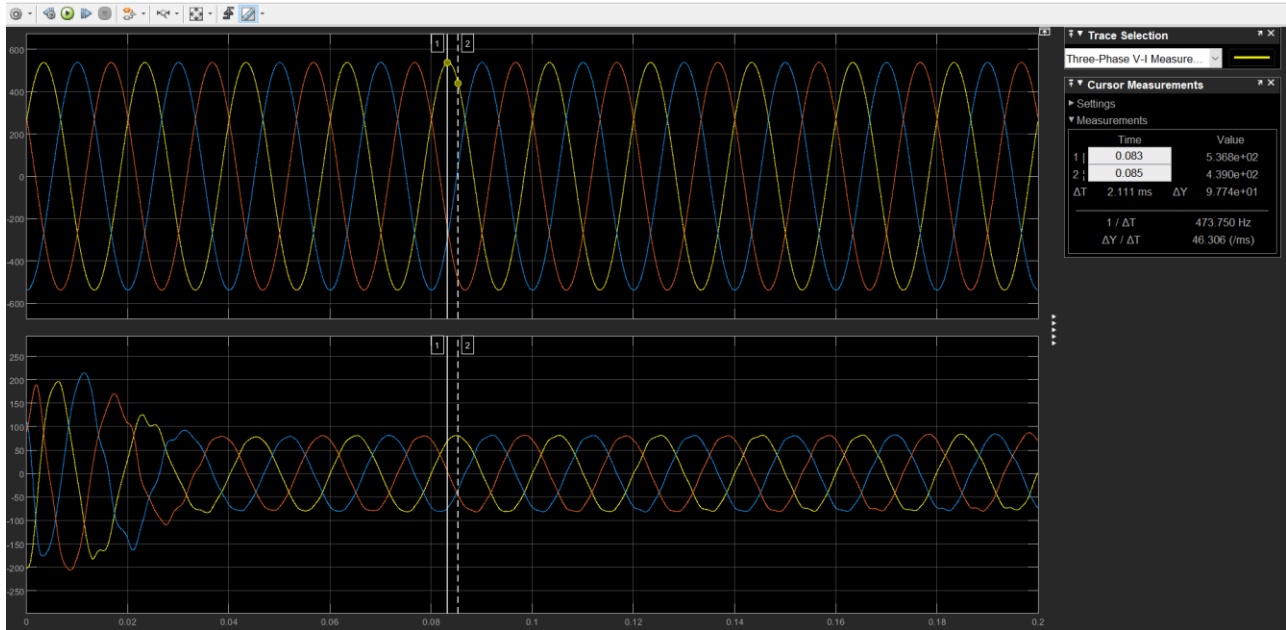
Figure 94-line voltage and currents
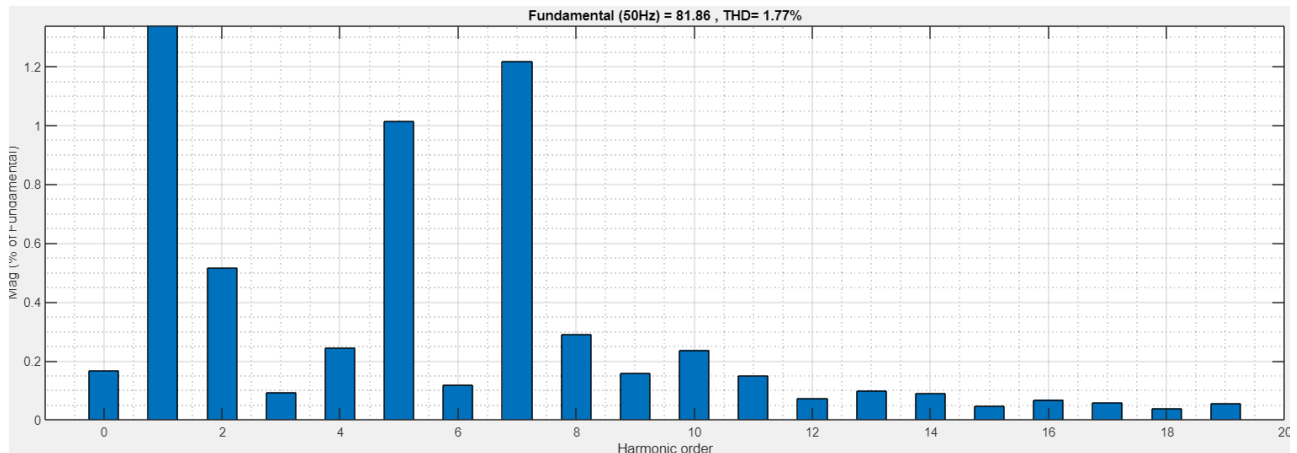
Figure 95-FFT analysis of 3L inverter conventional method, different frequencies, and different DC buses

4.3.2   Equivalent model of the three-level inverter

The same concepts and the procedures as of two-level inverter has been taken to find the equivalent model of the two three-level parallel connected inverters.

Considering the fact that homopolar current doesn't pass through the capacitance, the capacitance Cf can be neglected in LCL filter, and all the formulas applied to the three-level inverter in the same fashion which resulted in the same equivalent model as of two-level inverter.
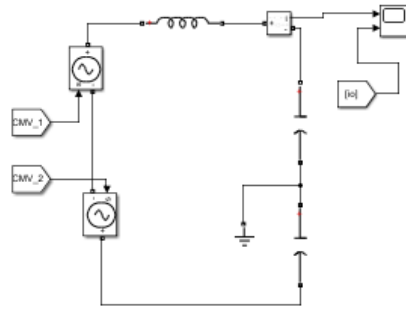
Figure 96-equivalent model

The ZSCC measured through the parasitic capacitances and the current measured by the equivalent model are exactly equal. Therefore, this model can be verified as the equivalent model.
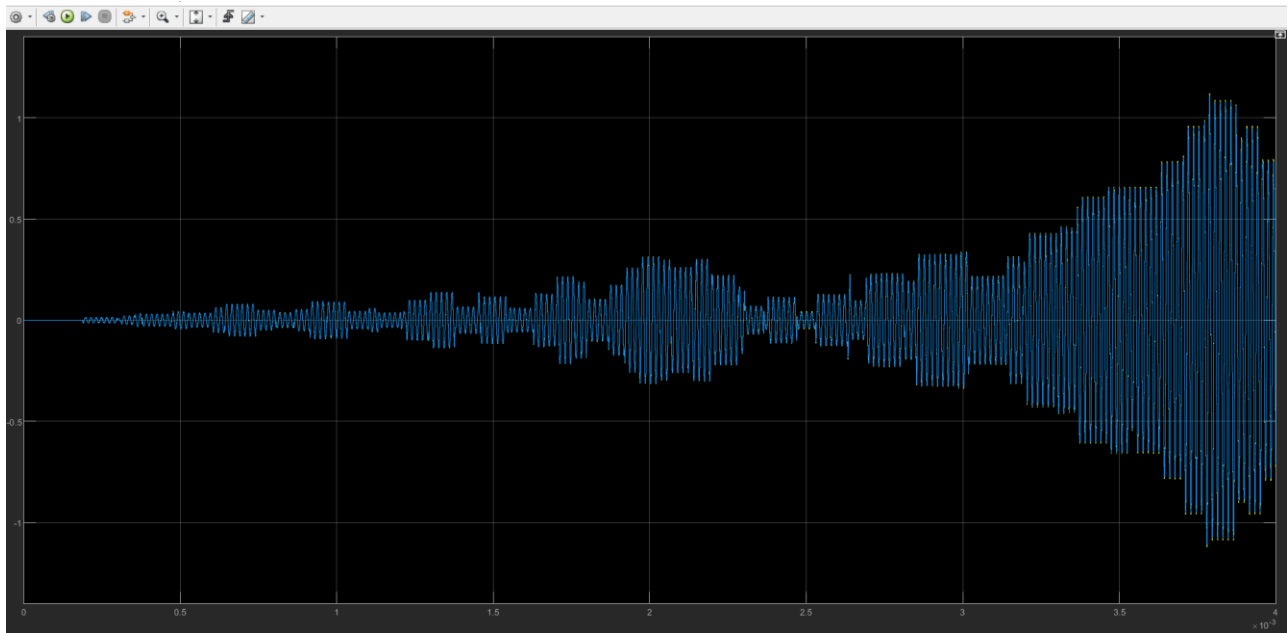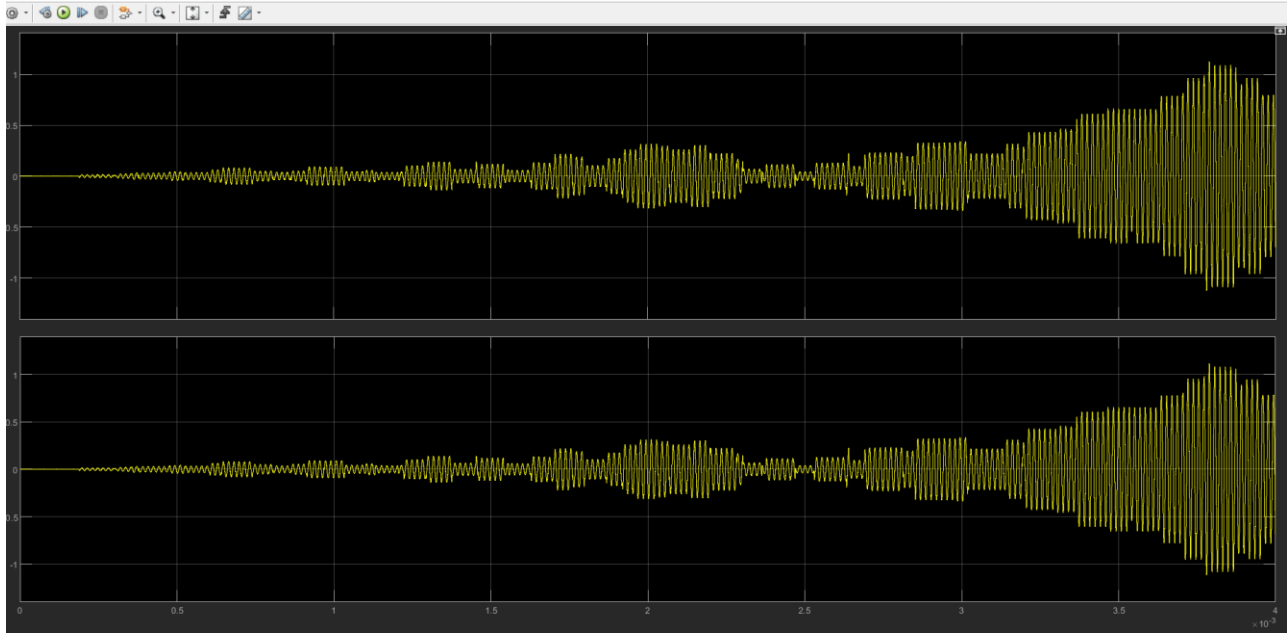
Figure 97-Measured ZSCC current of two three-level parallel connected inverters

4.3.3 Three-level inverters in parallel with the same DC bus

In this condition, the two inverters are connected in parallel both in DC and AC buses.
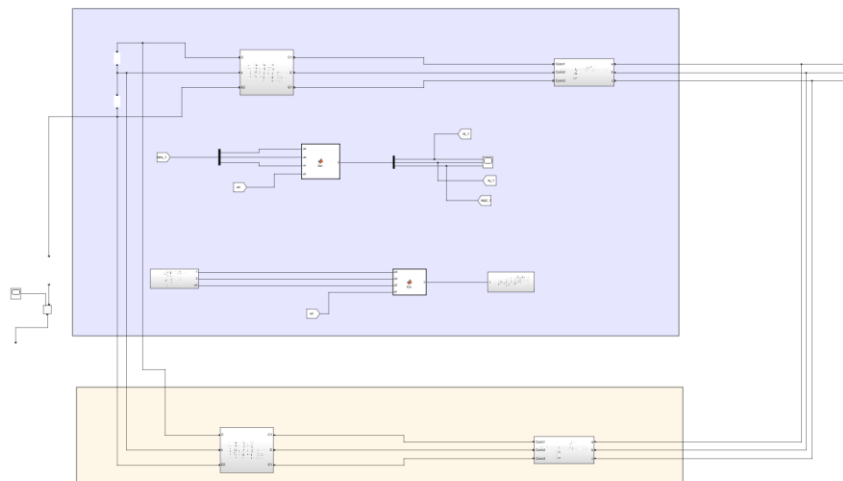
Figure 98-DC/AC bus connected

Since the two inverters have the same parameters, the homopolar component of the current in both inverters are negligible.
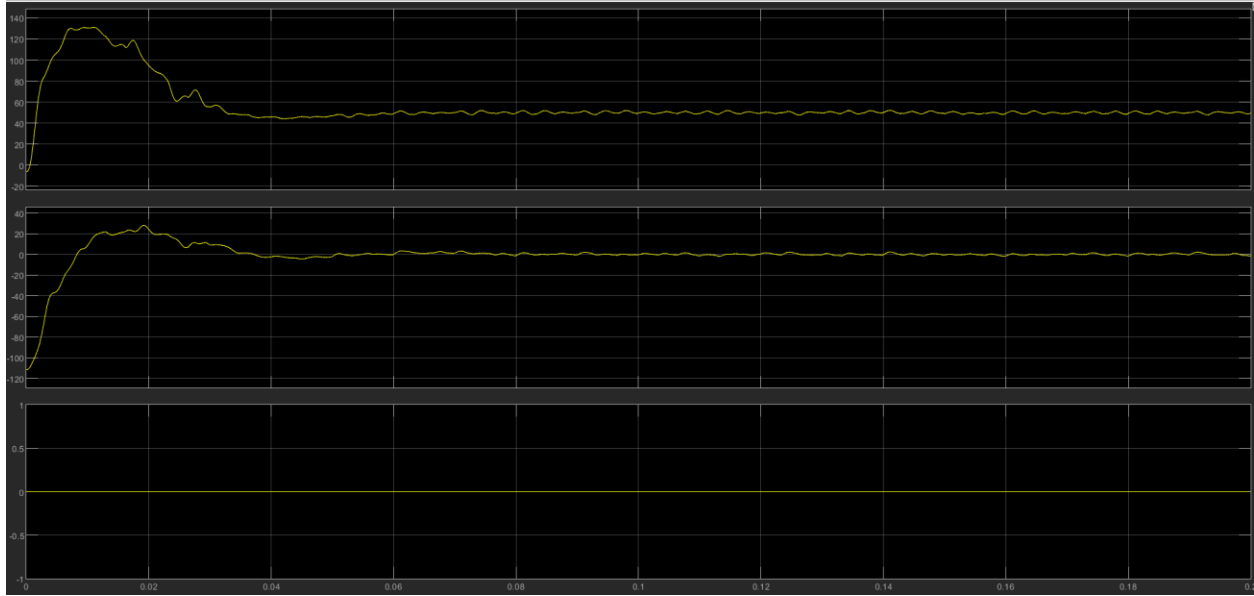
Figure 99-dq0 current of the inverter 2

If a frequency difference is introduced in between the two inverters, the homopolar component of the current is no longer negligible.
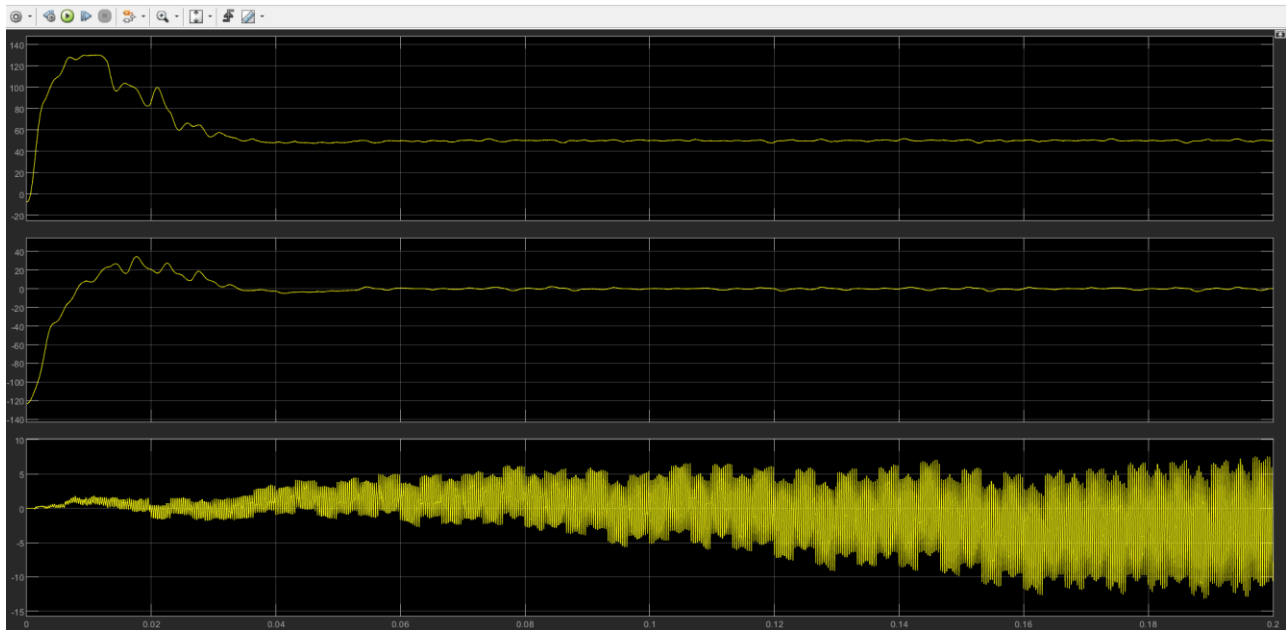
Figure 100-dq0 component of inverter 1

The current controllers are still able to follow the references, therefore the grid side voltage and currents are as desired.
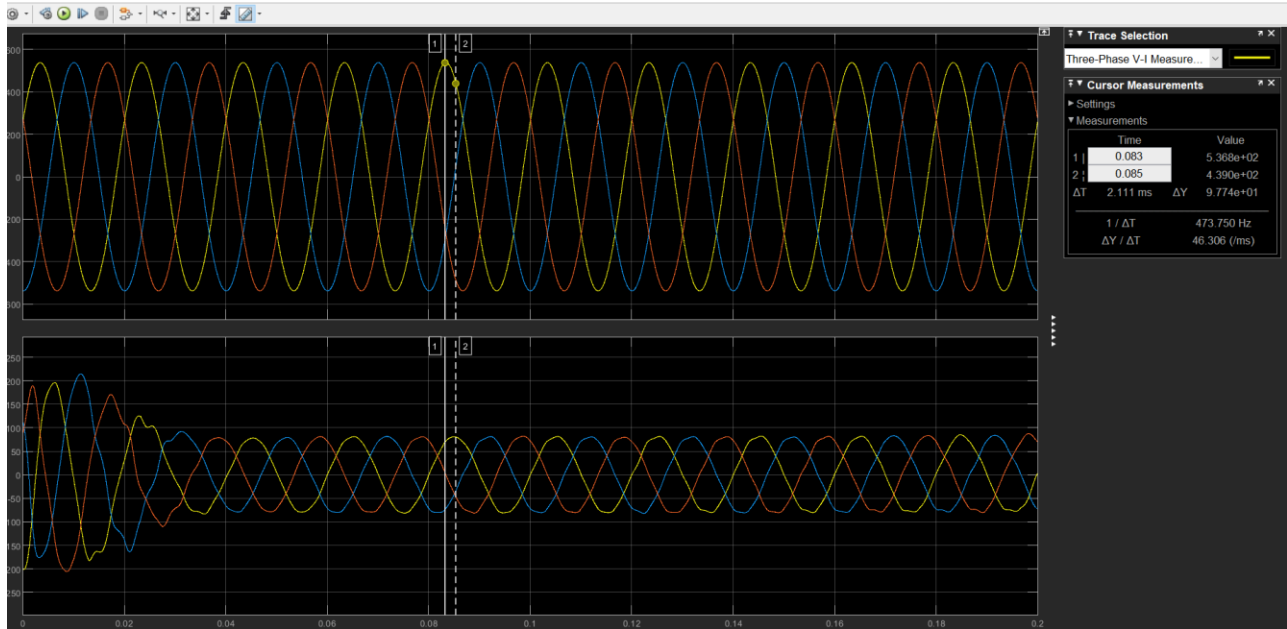
Figure 101-grid line voltage and currents
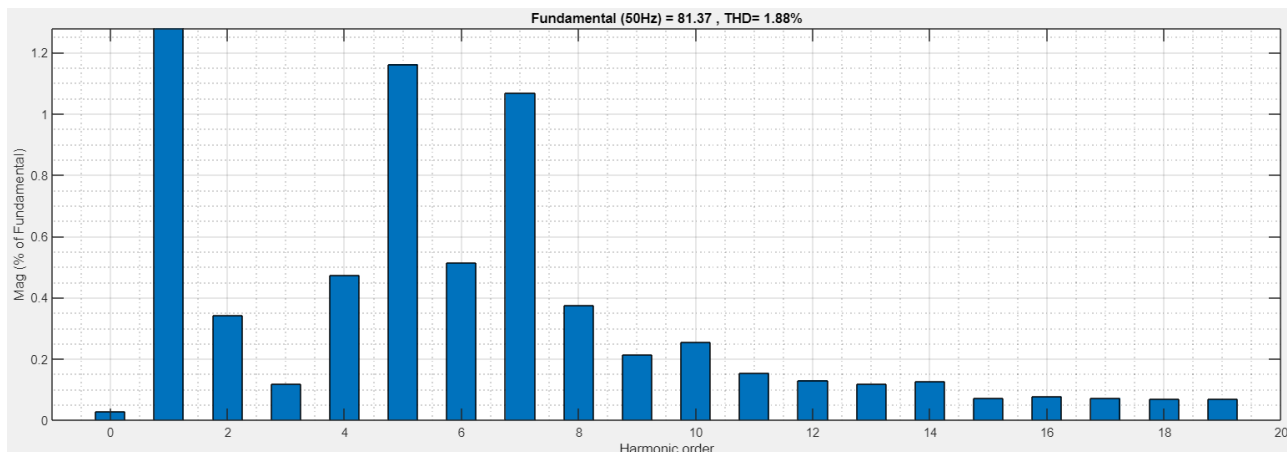
Figure 102-FFT analysis-Grid currents in conventional method,3L inverter, same DC bus and different frequencies

4.3.4   CMV reduction of parallel connected three-level inverters

4.3.4.1   MV3

The first method that has been implemented to reduce the CMV in three level parallel inverters is MV3 which uses the three nearest medium voltages to synthesize the reference voltage since the corresponding common mode voltage to the medium vectors is zero. This method is explained in the details in appendix 7.5.

As the first step like previous tests, the method is tested in different conditions in parallel connected mode with different frequencies and DC bus conditions.

As explained in the appendix, this method reduces the common mode voltage to zero. The statement is verified by MATLAB simulation. The common mode voltage measured by this method is shown:
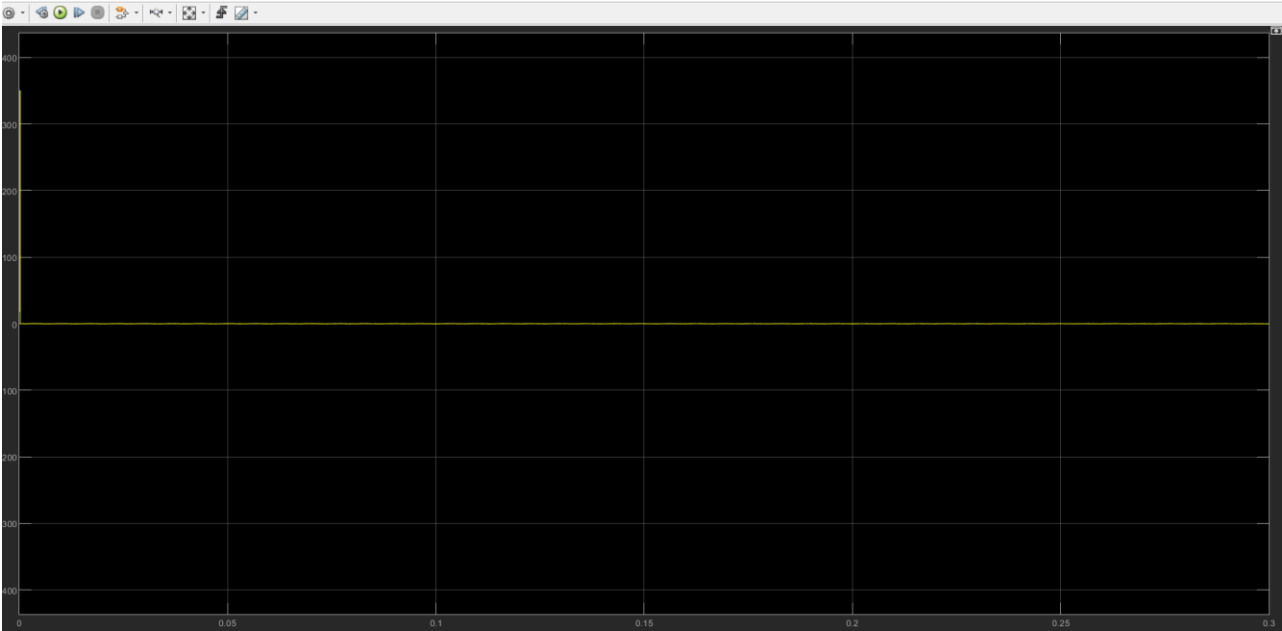
Figure 103-CMV-MV3 method
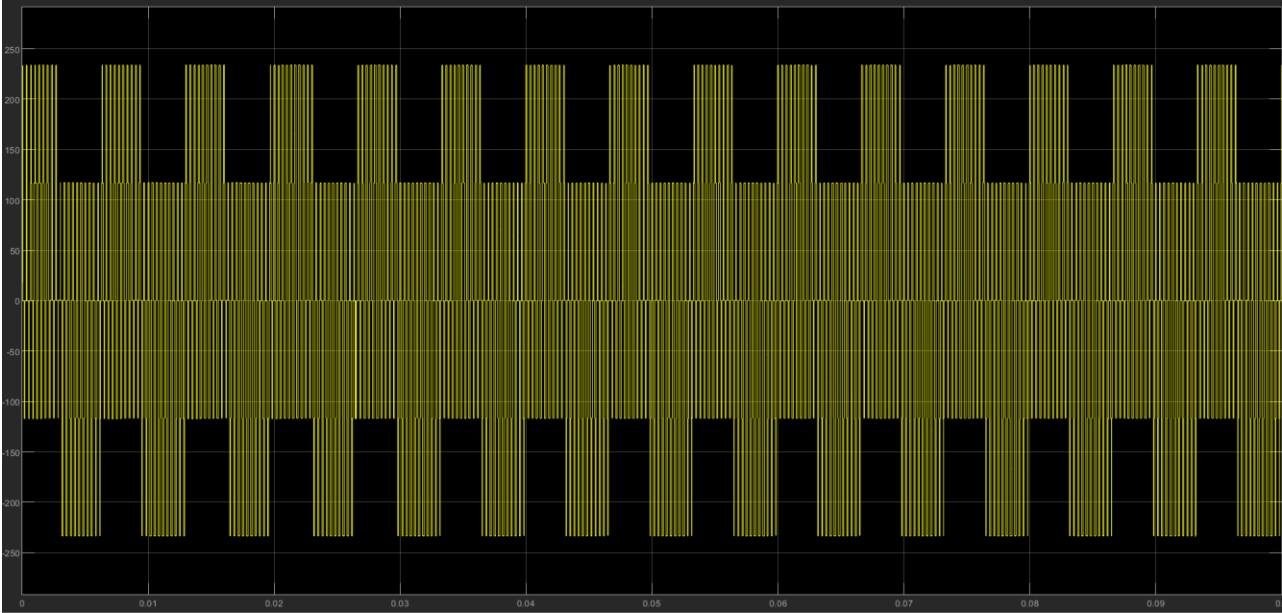
Figure 104-CMV-Conventional method

The controller successfully maintains the output voltage and currents to the desired value.

Figure 105-output Voltage and currents-MV3

As in parallel connection, the frequency of the second inverter is changed to 3001kHz, different from the first one by 1 Hz. And this effect is studied on the output voltage and currents, circulating currents and CMV.

The CMV is maintained to zero as it can be observed in the picture below:
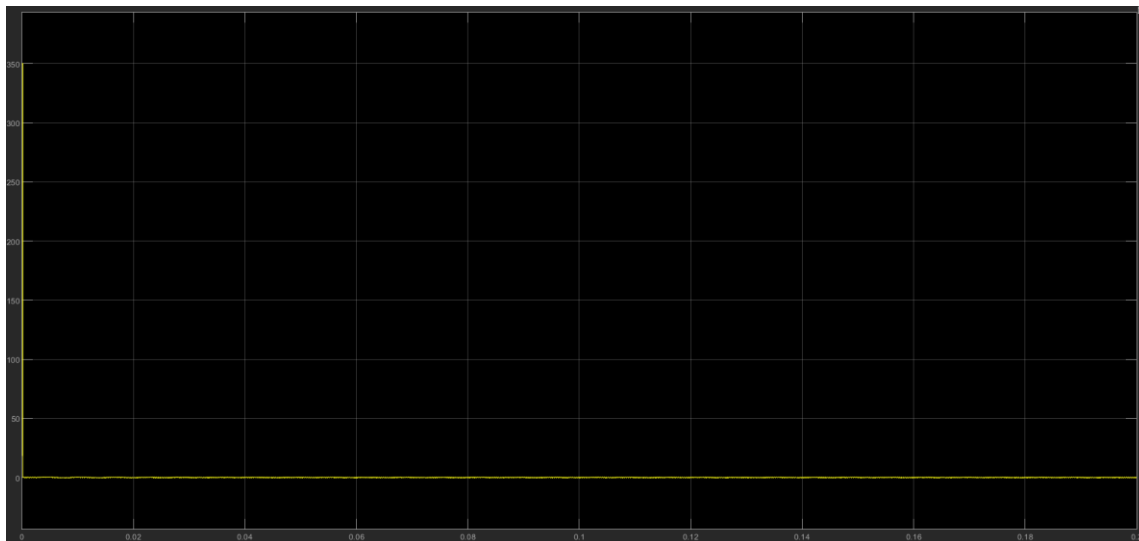
Figure 106-CMV-MV3 method with Frequency difference

The zero-sequence circulating current measured through parasitic capacitance is depicted In the Figure below. The method shows the benefit of reduction of circulating currents as well as CMV.
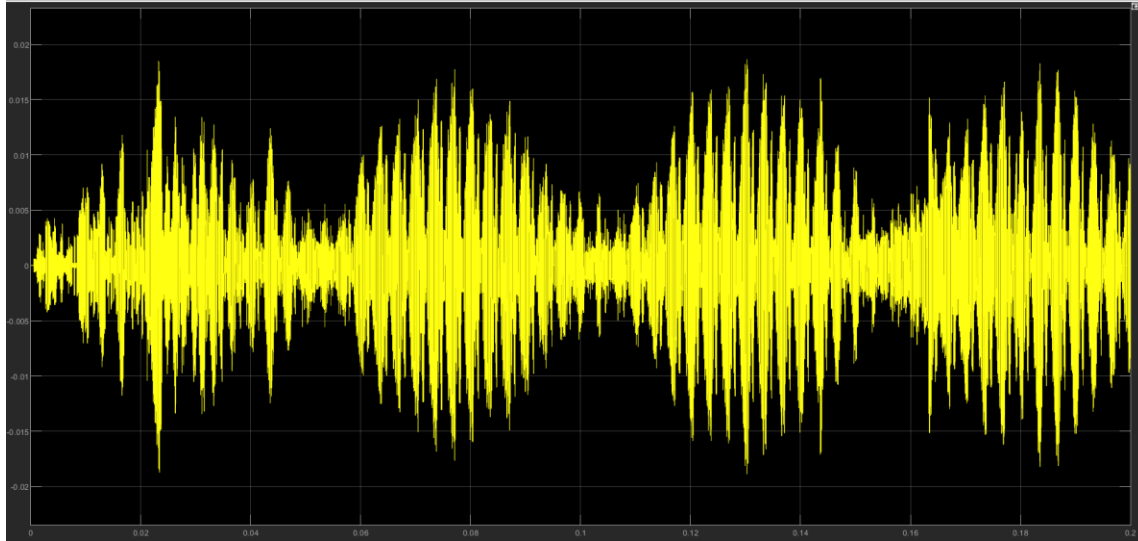
Figure 107-ZSCC-MV3
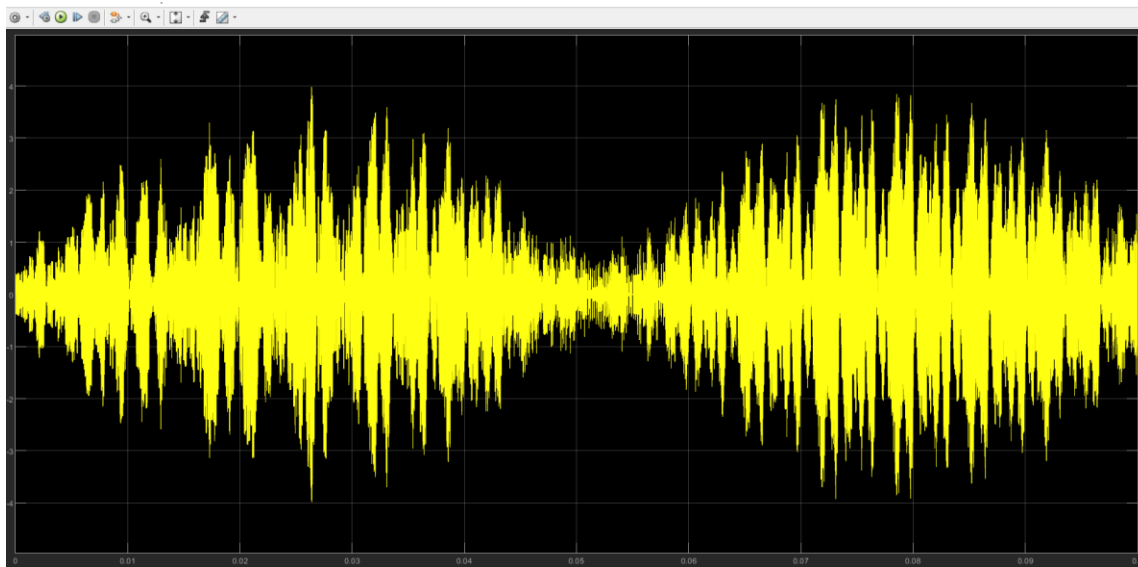
Figure 108-ZSCC-conventional method

Table 7-ZSCC comparison between the conventional method and MV3 method,3L inverter

Objective	Condition	ZSCC
Conventional PWM method	Different DC Bus	<4
MV3 PWM method		<0.02

The controllers successfully are able to maintain the grid side voltage and currents:
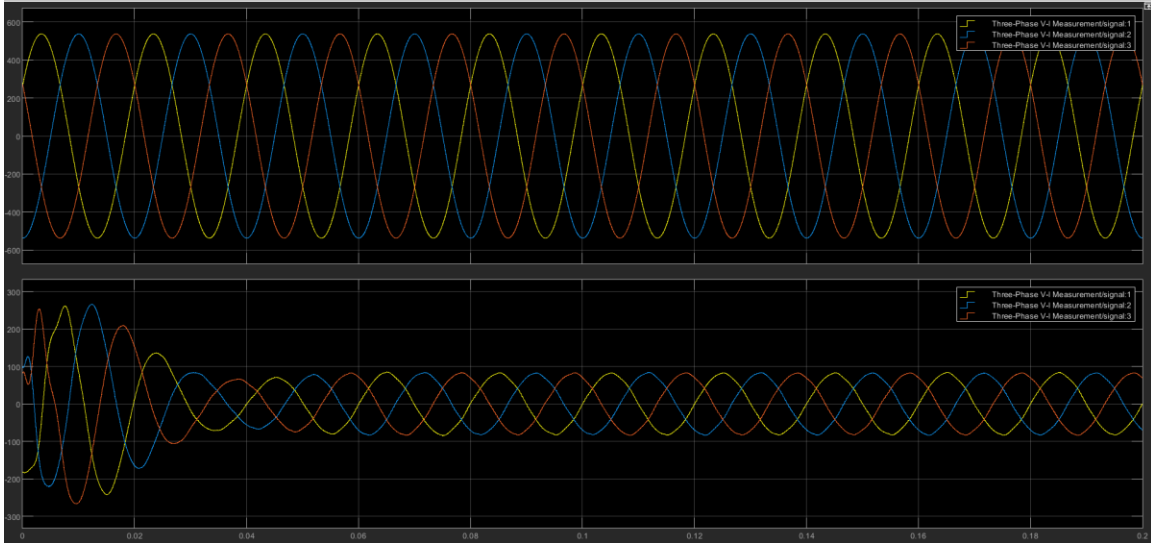
Figure 109-output voltage and currents in MV3 method with frequency difference
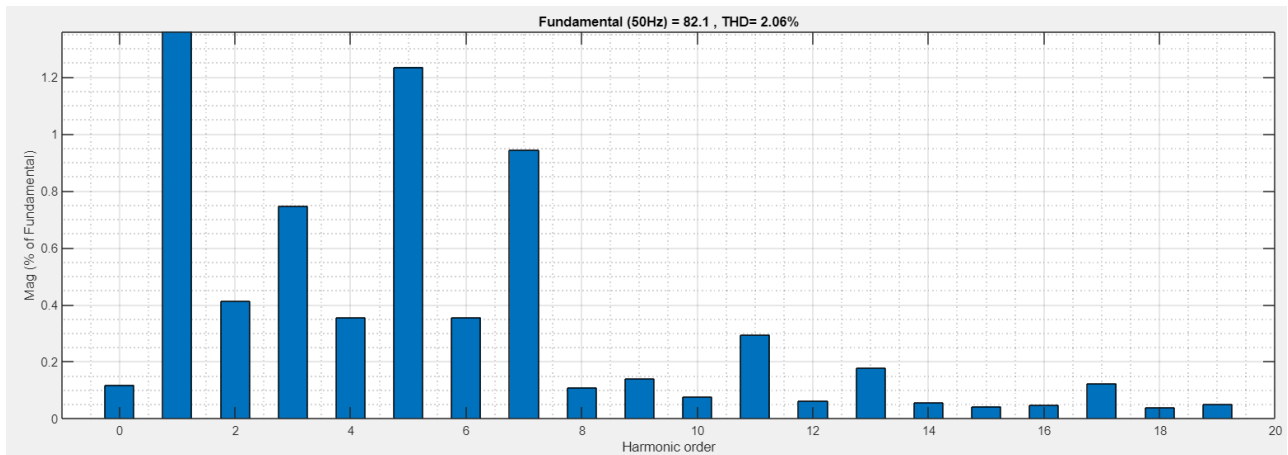
Figure 110-FFT analysis of the MV3 method with different DC buses and different frequencies

Table 8-THD comparison between the MV3 method and the conventional method with different frequencies,3L inverter

Objective	Condition	Current delivered to the grid
THD of Conventional PWM method	Different Frequencies Different DC Bus	1.77%
THD of MV3 PWM method		2.06%

4.3.4.2   MV3 with the same DC bus

Above considerations are applied with the condition of the same DC bus and the results are compared with the conventional method.

It is verified that this method is still able to reduce the CMV to zero with the condition of the same DC buses and same frequencies:
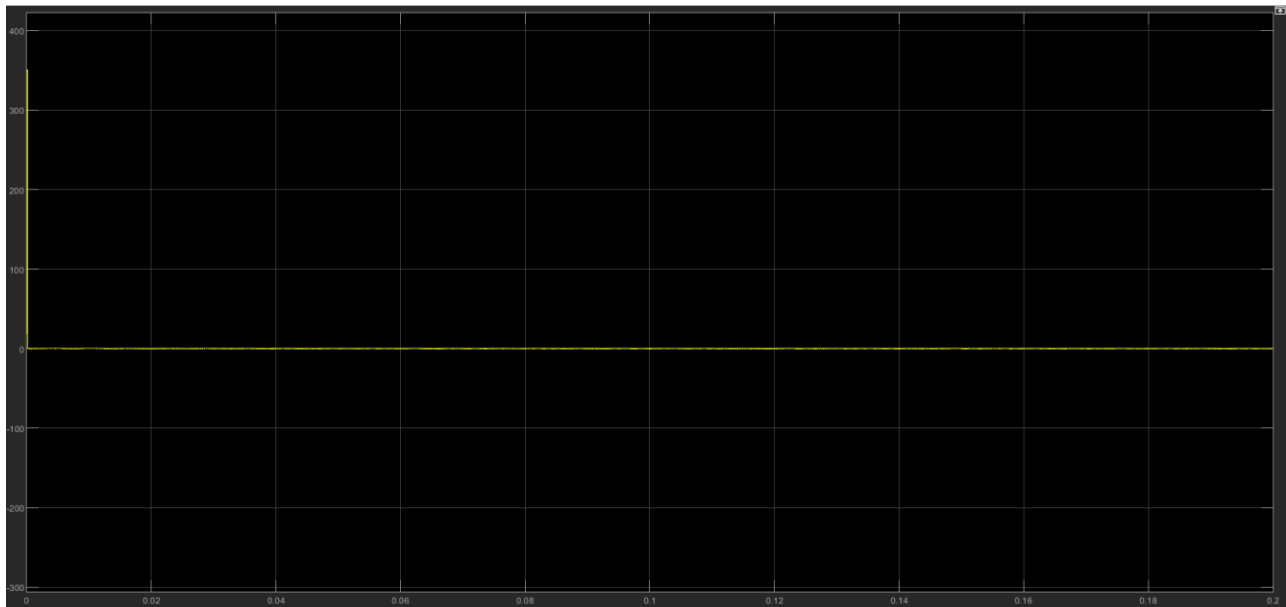
Figure 111-CMV in MV3 method with the same DC bus and same Frequencies
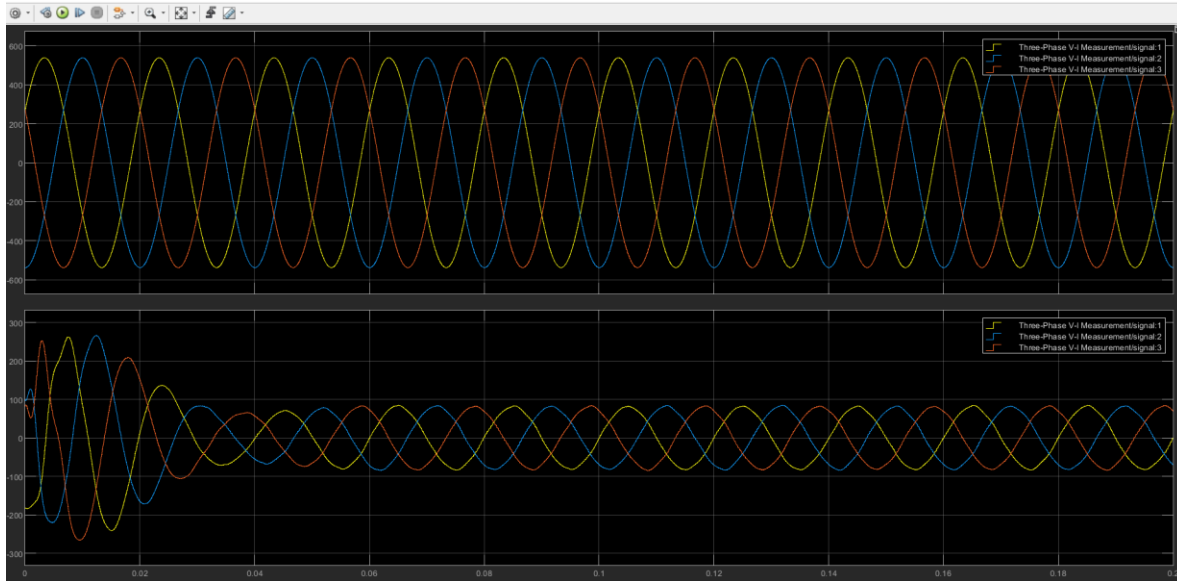
As in parallel connection, the frequency of the second Inverter is changed to 3001Hz, different from the first one by 1 Hz. And this effect is studied on the output voltage and currents, circulating currents and CMV.

The CMV is maintained to zero as it can be observed in the picture below:
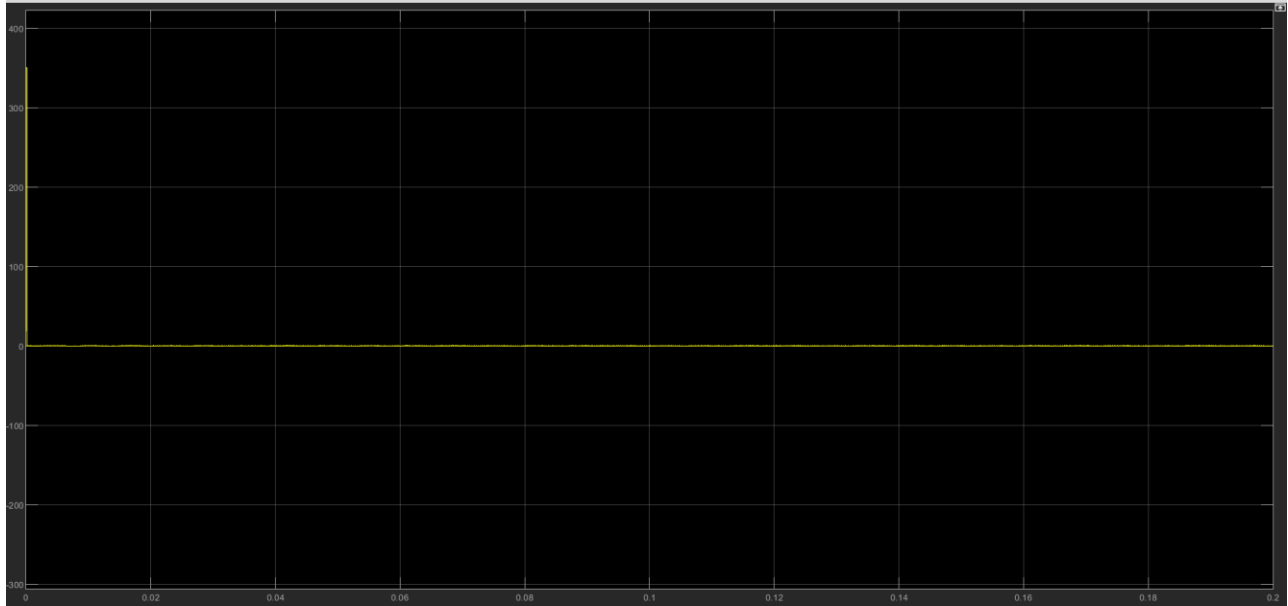
Figure 112-CMV of MV3 method with the same DC bus and different frequencies

The THD analysis has been executed for two parallel inverters connected in parallel with the same DC buses and different frequencies and the results are compared with the conventional method and the MV3 method. The THD of MV3 method is less than 3% which satisfies the grid requirements.
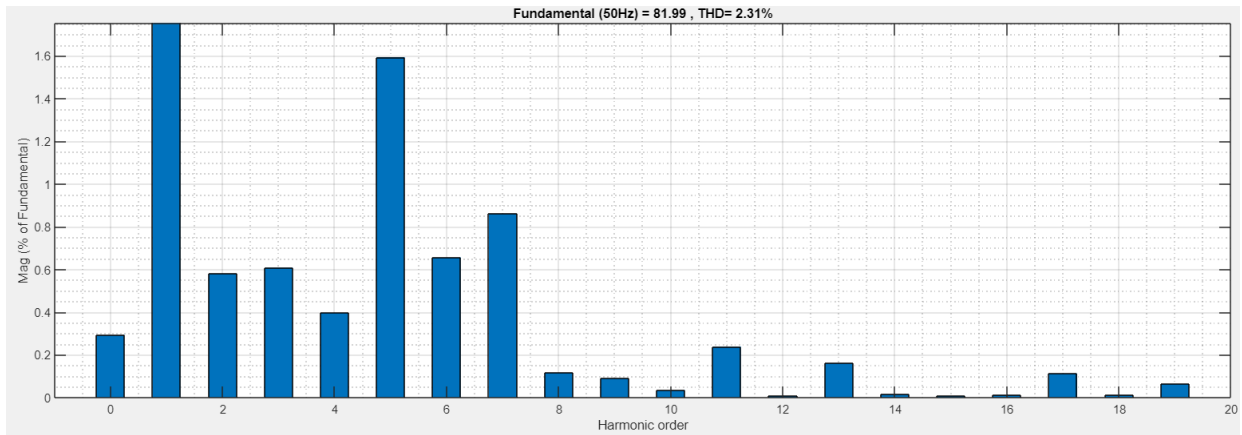
Figure 113-FFT analysis of Grid currents with the same DC buses and different frequencies for MV3 method

Table 9-THD comparison between the MV3 method and the conventional method,3L inverter in case of same DC bus and different frequencies

Objective	Condition	Current delivered to the grid
THD of Conventional PWM method	Different Frequency Same DC Bus	1.88%
THD of MV3 PWM method		2.31%

In both conditions the PI controllers are able to maintain the current delivered to the grid at the desired value and phase.
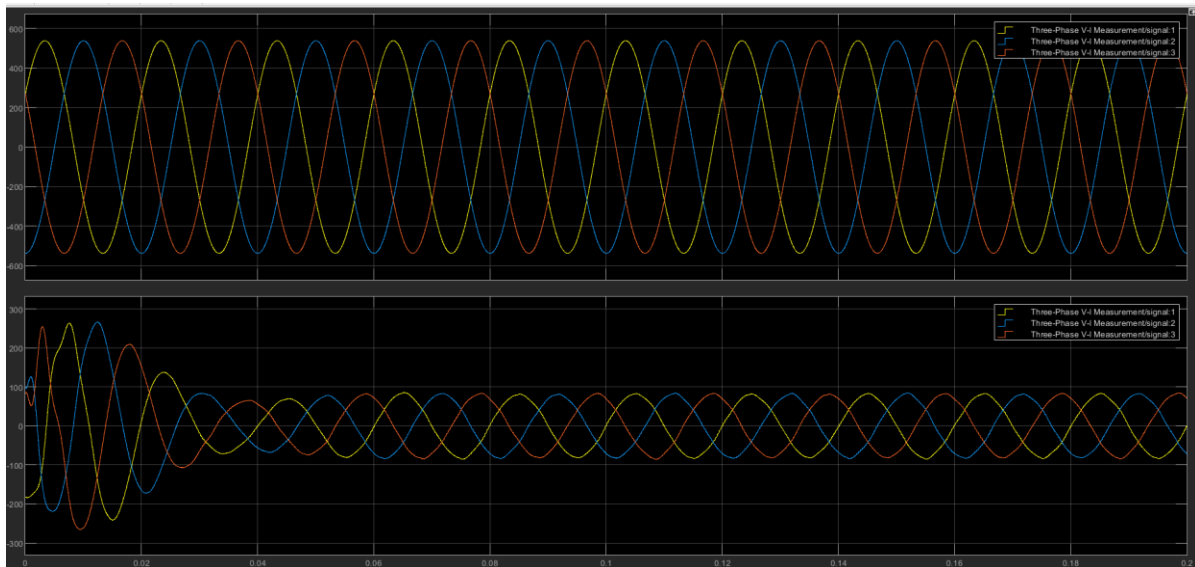
Figure 114-grid currents and voltages in MV3 method with the same DC bus

4.3.4.3   LMZV method

In this method as it is explained in detail in appendix 7.6, the hexagon of space vector PWM is divided into 12 sectors instead of 6 sectors and the reference voltage is synthesized with the nearest large, medium and zero vector (OOO) to avoid the peak of CMV as the other zero vectors and small vectors contribute to higher CMV. This method is able to reduce the common mode voltage to the half of conventional methods.

The method is tested with different parameters and conditions and the effects are compared with of conventional method. As it can be observed in the figure below, the CMV is reduced compared with the conventional method:
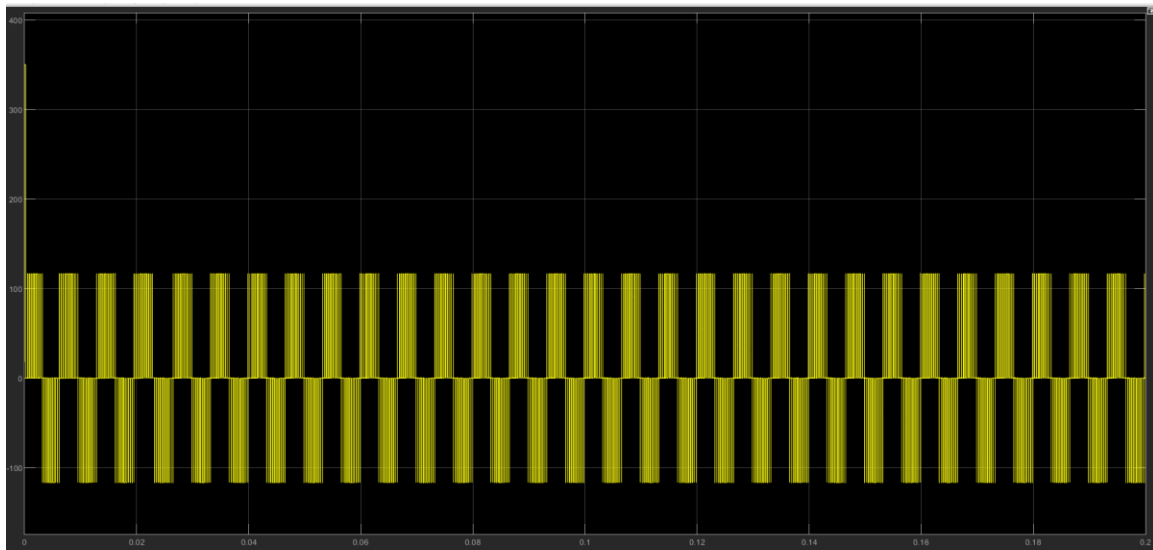
Figure 115-CMV of LMZV same frequency and different DC buses

Then the effect of frequency difference is observed for this condition and method and zero sequence circulating.

It is verified that the method is still able to reduce the CMV and in both conditions the PI controllers are able to maintain the currents to the desired value and phase.
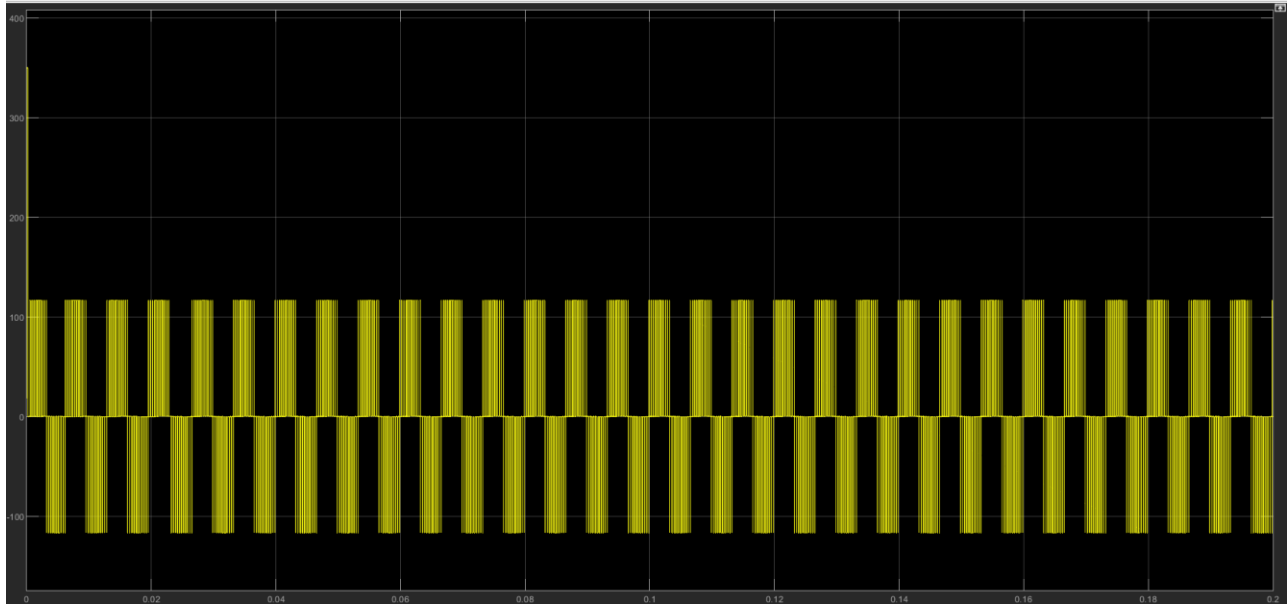
Figure 116-CMV of LMZV with Different frequencies and different DC buses
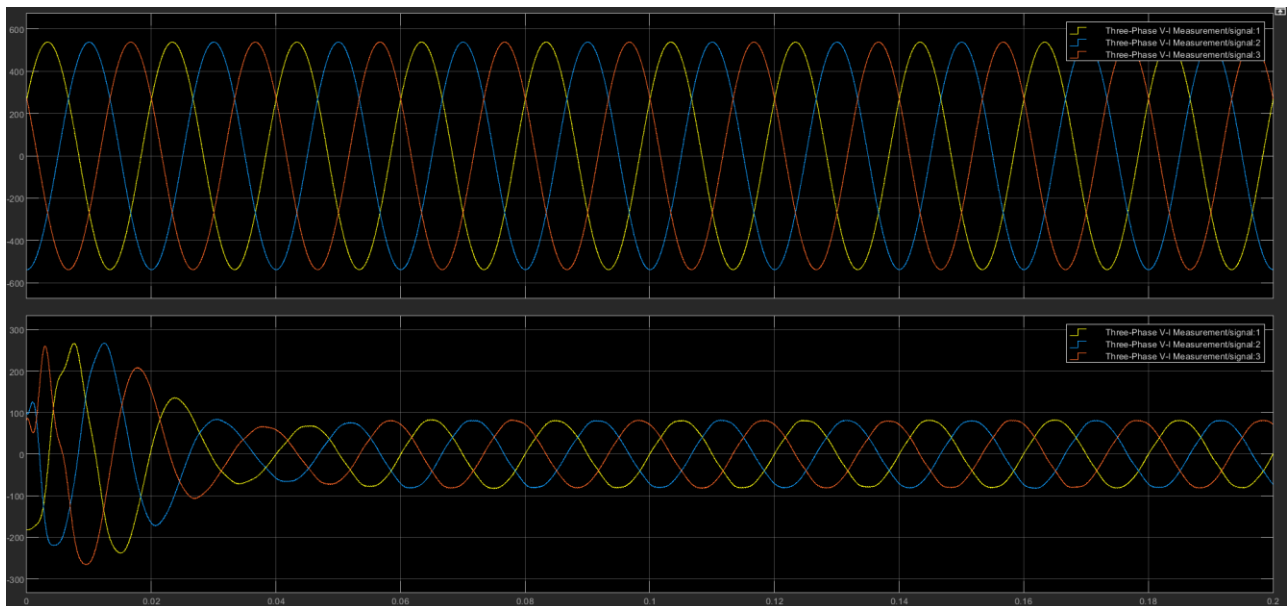
Figure 117-Grid voltage and output currents

The zero sequence circulating currents measured through parasitic capacitance is depicted in the picture below. Compared with the MV3 method, the ZSCC is still higher but compared to the conventional method, the ZSCC is slightly reduced.
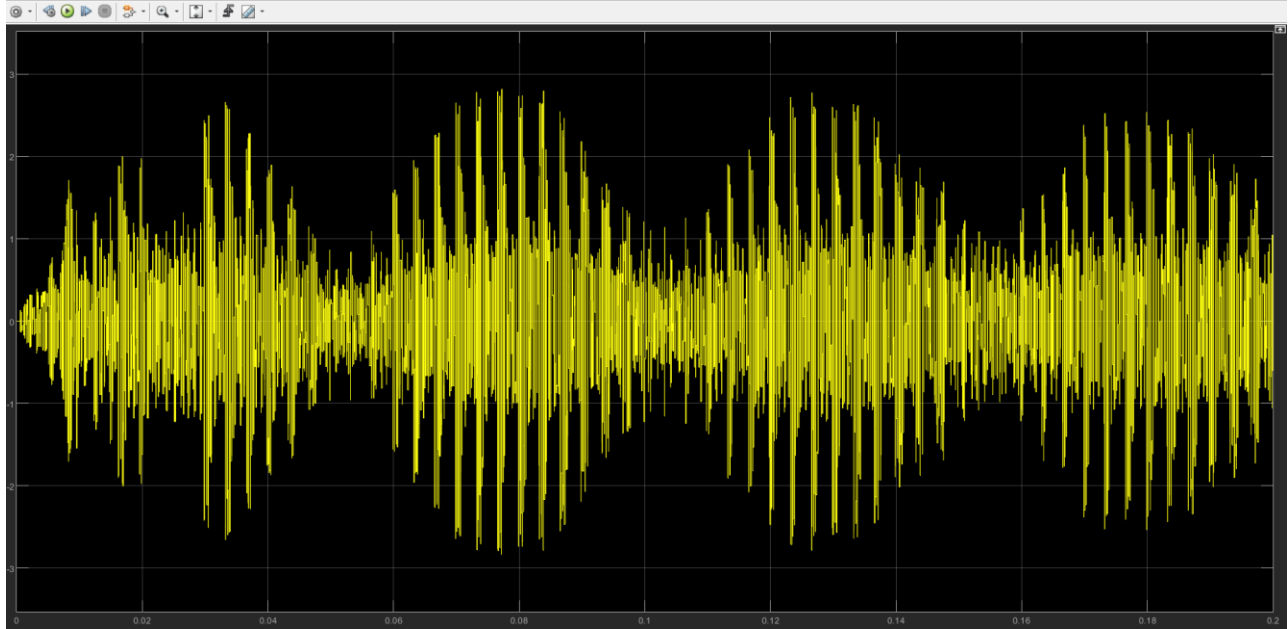
Figure 118-ZSCC of LMZV

Table 10-ZSCC comparison between conventional method and the LMZV method,3L inverters

Objective	Condition	ZSCC
Conventional PWM method	Different Frequencies Different DC Bus	<4
LMZV PWM method		<3

THD is measured for the currents delivered to the grid which is the sum of the currents of two inverters. It is verified that the THD is less than 3 % which satisfies the grid requirements.
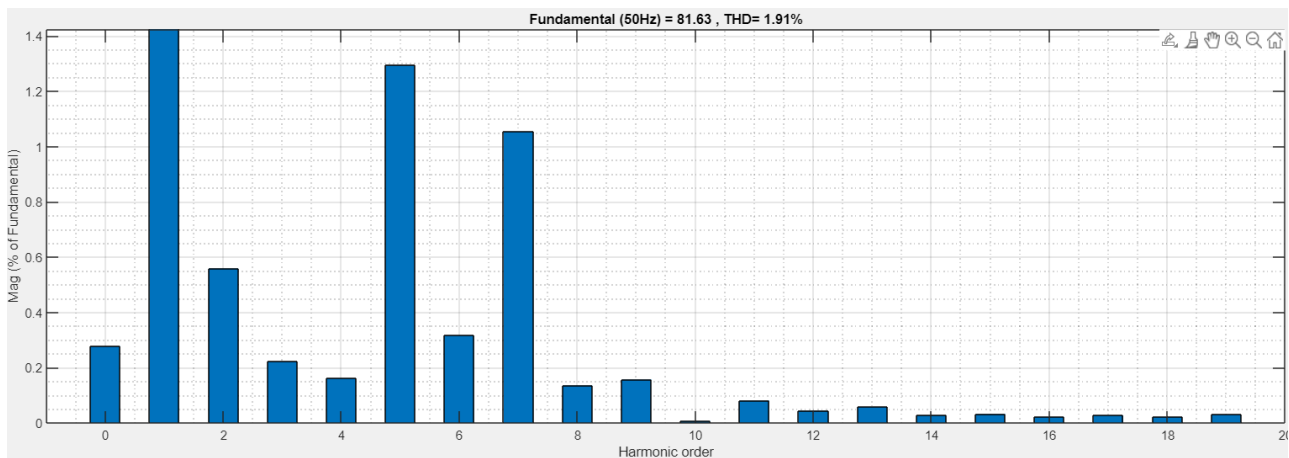
Table 11-THD comparison between the LMZV method and the conventional method,3L inverter, different frequencies

Objective	Condition	Current delivered to the grid
THD of Conventional PWM method	Different frequencies Different DC Bus	1.77%
THD of LMZV PWM method		1.91%

At the last step in this method, the two inverters are connected with the same DC bus.

If the two inverters have the same frequencies, the effect on CMV and the THD is studied.

CMV is reduced to the half as observed in the picture below compared to that of conventional method:
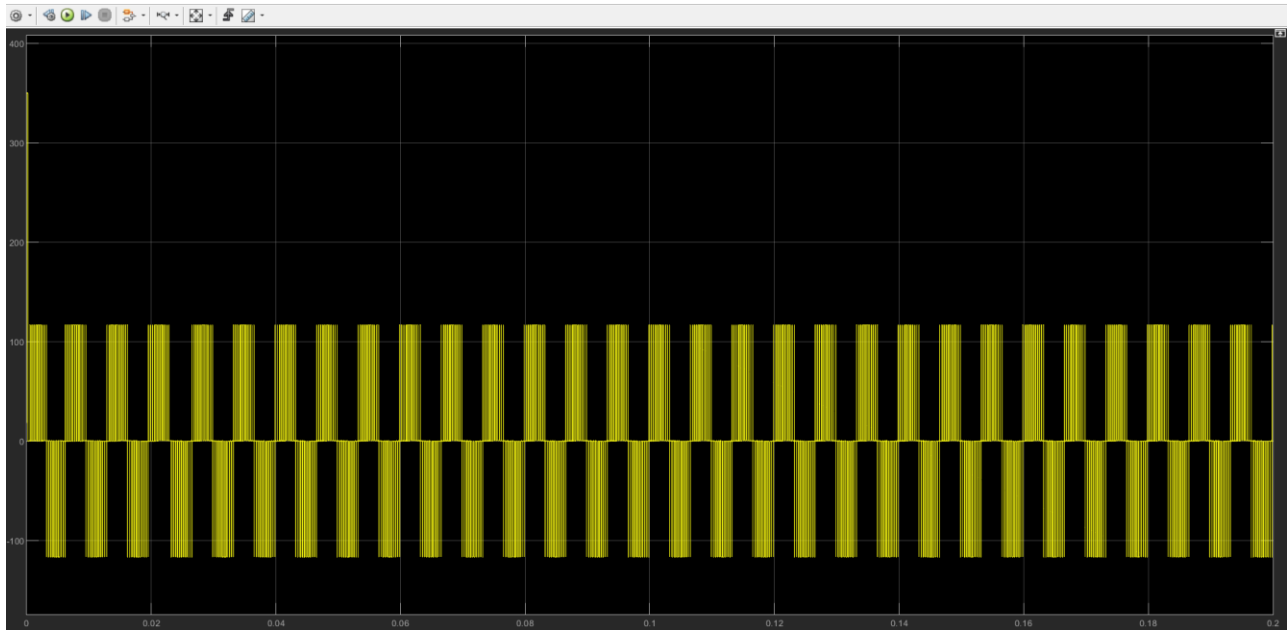
Figure 119-CMV of LMZV with the same Frequency and same DC buses

The FFT analysis is done to observe the magnitude of different harmonics and calculate the THD and compare it with the similar configuration of the conventional method. The THD is still less than 3 percent which satisfies the grid requirements.

And as the last step the frequency of the second inverter is set to a different value of the first inverter.

It is observed that the method is still able to deliver the currents to the grid with a THD of less than 3%.
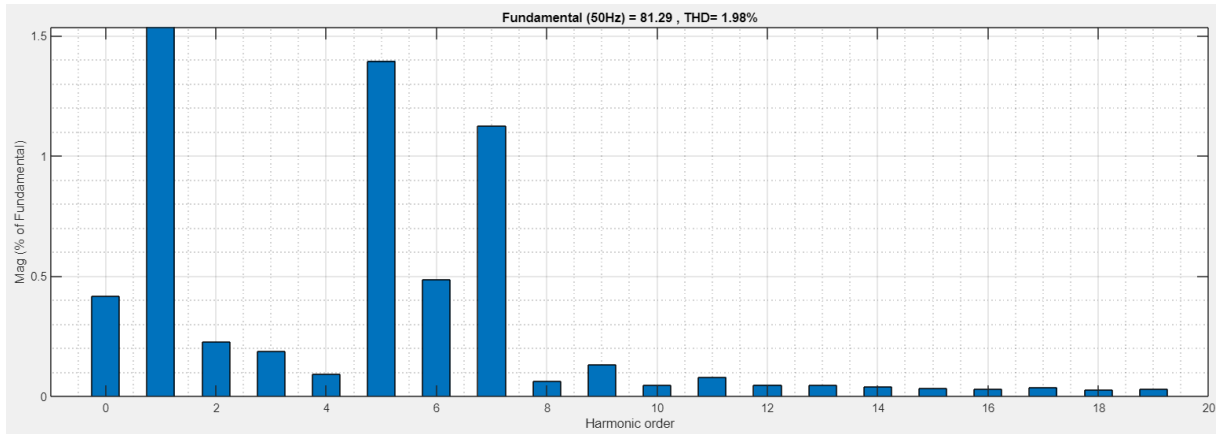
Figure 120-FFT analysis of the LMZV with different frequency and the same DC bus

Table 12-THD comparison between the LMZV method and the conventional method,3L inverter in case of same DC bus and different frequencies

Objective	Condition	Current delivered to the grid
THD of Conventional PWM method	Different frequencies Same DC Bus	1.88%
THD of LMZV PWM method		1.98%

In both cases, the PI controller is able to deliver the currents to the grid with the desired value and phase.
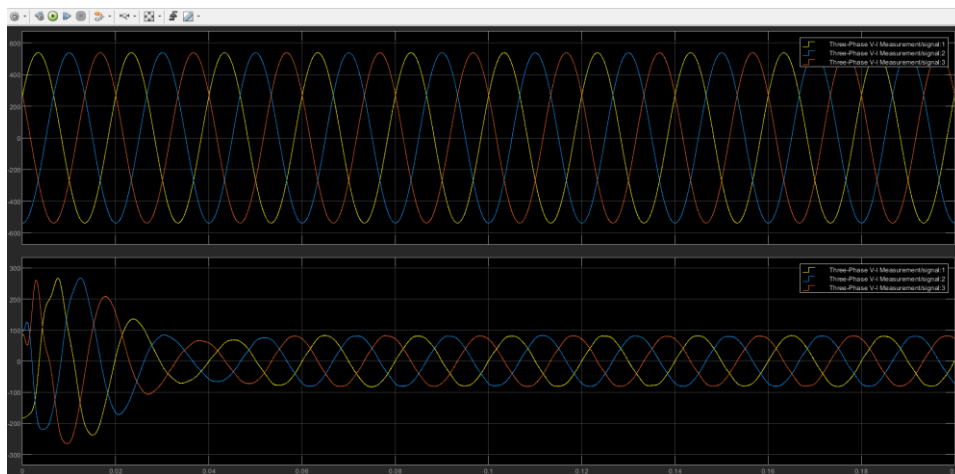
Figure 121-Grid currents and voltages with the same DC bus-LMVZ method

5   CONCLUSIONS

5.1   Conclusion

In this thesis work, two different inverter topologies have been used as to connect two inverters in parallel.

Two level inverter which have two switches per leg

Three-level Inverter which have 4 switches per leg

As the modulation technique, SVPWM has been chosen to turn on/off the IGBT switches in both inverter topologies and PI controllers are set to maintain the current delivered to the grid to the desired value.

The conventional SVPWM has been widely used for both topologies in recent years and are able to meet the grid requirements. Parallel connection of inverters gives rise to many problems such as circulating currents and the common mode voltages which can damage the systems since the real world is not ideal and there are mismatches between modules operating together. While using the conventional SVPWM, it is not possible to address these issues and minimize them. As stated in the literature, common-mode voltage is an excitation source for the zero sequence circulating currents. Therefore, one solution for reducing the ZSCC is to decrease the common-mode voltage.

The vectors in SVPWM can be categorized and the CMV corresponding to each switching state has been considered for both topologies. In some switching states the CMV is the lowest whereas in some the peak is observed. For two level inverters, the highest peak of CMV corresponds to the zero vectors hence by replacing the zero vectors with two neighboring active vectors the common mode voltage can be reduced. This method is called Active Zero State PWM (AZSPWM) which has the same modulation range as the conventional method. However, due to the nature of two-level inverters, the CMV cannot be minimized to zero. A decrease in the level of the ZSCC has been observed after reducing the CMV. For three-level inverters, there are many different modulation techniques to reduce the CMV as three-level inverter has more degree of freedom due to higher number of switches per leg. In this thesis work, two methods have been used to reduce the CMV. Considering that the vectors in three-level inverter can be divided into zero, small, medium, and large vectors and the lowest CMV which is CMV equal to zero corresponds to the medium vectors and zero vector (OOO). In the first method, the three nearest medium vectors are used to synthesize the reference voltage (MV3 method) and it resulted in the CMV of zero. Since the CMV has been decreased drastically, a sharp reduction in the ZSCC is also observed. With this method, the objective of the reduction of CMV and ZSCC are met but at the cost of limiting the modulation ratio since only medium vectors are used and a slight increase in the THD. The second method that is used to reduce CMV for three-level inverter is called LMZV PWM technique which uses the two nearest medium and large vectors plus zero vector (OOO) to reduce the CMV. It is observed that CMV is reduced to the half compared with the traditional method and the ZSCC has been

decreased slightly. In this method, the hexagon of SV is divided into 12 sectors instead of 6 sectors. LMZV PWM's modulation ratio is wider than the MV3 method as the more sections of the hexagon is used. However, the CMV voltage is higher than MV3 but lower than the conventional method. The same comparison applies to the ZSCC. The measured THD with this method is slightly higher than the conventional method and lower than the MV3 method.

Another task that has been covered in this thesis work is obtaining the equivalent zero sequence model of the two parallel inverters. By assuming that the zero-sequence circulating current does not pass through the capacitance of the LCL filter, the filter can be summarized into two inductances in series with each other. For each phase the KVL equations are written between two inverters path considering the parasitic capacitances that are connected to the negative terminals of each inverter to the ground. The equivalent model is obtained from zero sequence point of view and the model is verified by the simulation.

5.2   Future work

In the MATLAB simulation all components and the grid are considered as ideal. However, in the real-world application hardly an ideal component can be found. As the next step, a simulation with real components can be done to measure switching losses and THD in different modulation techniques. Another approach that can be taken as discussed in the introduction, is the different control techniques to find the best solution for multi-parallel inverters.

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7   APPENDIX

7.1   Clarke and Park transformations

Clarke transformation transfer abc reference frame to components in a stationary αβ0 reference frame. In order to preserve the active and reactive powers with the powers of the system in abc reference frame, a time invariant version of the Clarke transformation is implemented in this thesis.

Clarke transformation is a "fixed-axis" transformation at constant coefficients.

The time-invariant transformation matrix results in:

$$\bar{\bar{T}}_o = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\dfrac{1}{2} & -\dfrac{1}{2} \\ 0 & \dfrac{\sqrt{3}}{2} & -\dfrac{\sqrt{3}}{2} \\ \dfrac{1}{\sqrt{2}} & \dfrac{1}{\sqrt{2}} & \dfrac{1}{\sqrt{2}} \end{bmatrix}$$

If the power-variant transformation is needed, the following matrix should be used:

$$\bar{\bar{T}}_o = \frac{2}{3} \begin{bmatrix} 1 & -\dfrac{1}{2} & -\dfrac{1}{2} \\ 0 & \dfrac{\sqrt{3}}{2} & -\dfrac{\sqrt{3}}{2} \\ \dfrac{1}{\sqrt{2}} & \dfrac{1}{\sqrt{2}} & \dfrac{1}{\sqrt{2}} \end{bmatrix}$$

This matrix, applied to three-phase instantaneous quantities $v_a(t)$, $v_b(t)$, $v_c(t)$, gives origin to three Clarke components: α, β and 0, or homopolar.

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \\ v_0(t) \end{bmatrix} = \bar{\bar{T}}_o \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix}$$

Clarke vector, composed by $v_\alpha(t)$ and $v_\beta(t)$, can be defined; it is also known as spatial vector:

$$\bar{v}(t) = v_\alpha(t) + jv_\beta(t)$$

Anyway, Clarke transformation is a particular case of Park one, obtained on rotating axis. Park transformation can be divided into time-variant and time-invariant transformations. Another classification of Park transformation is based on the alignment of the transformation with the dq0 axis.

If the rotating frame is aligned with the phase A, the transformation is based on d-axis and if the rotating frame is 90 degrees behind phase A, the transformation is aligned with q-axis.

Park transformation matrix, time-invariant and aligned with the d-axis, always orthogonal, is as follow.

$$\bar{\bar{T}}(\theta) = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

And a time-variant version of Park transformation aligned with the d-axis:

$$\bar{\bar{T}}(\theta) = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

The time-invariant Park transformation, aligned with the q-axis or sine-based transformation:

$$\bar{\bar{T}}(\theta) = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

And the time-variant version deferrers by a coefficient of $\sqrt{\frac{2}{3}}$.

As Clarke transformation, this matrix, applied to three-phase instantaneous quantities, gives origin to three elements: d, q and 0, or homopolar.

$$\begin{bmatrix} v_d(t) \\ v_q(t) \\ v_0(t) \end{bmatrix} = \bar{\bar{T}}(\theta) \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix}$$

It is also possible to converter the latter reference frames to each other. To convert from αβ0 reference frame to dq0, the following matrix is used which phase A is initially aligned with the q-axis:

$$\bar{\bar{T}}(\theta) = \begin{bmatrix} \sin(\theta) & -\cos(\theta) & 0 \\ \cos(\theta) & \sin(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

And if the phase A is aligned with the d-axis, the following matrix is used:

$$\bar{\bar{T}}(\theta) = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

The matrix is applied to αβ0 quantities to obtain dq0 elements:

$$\begin{bmatrix} v_d(t) \\ v_q(t) \\ v_0(t) \end{bmatrix} = \bar{\bar{T}}(\theta) \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \\ v_0(t) \end{bmatrix}$$

For Park to Clarke transformation, phase A initially aligned with the d-axis, the following matrix Is used:

$$\bar{\bar{T}}(\theta) = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 0 \\ \sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

The matrix is applied to dq0 quantities to obtain αβ0elements:

$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \\ v_0(t) \end{bmatrix} = \bar{\bar{T}}(\theta) \begin{bmatrix} v_d(t) \\ v_q(t) \\ v_0(t) \end{bmatrix}$$

7.2   Two-level conventional SVPWM

The conventional SVPWM of the three-phase VSI utilizes two neighboring active space vectors in each sector with the conjunction of the zero vectors to obtain the reference vector, $\bar{\bar{V}}^* = Me^{j\vartheta}$. For example, if $\bar{V}^*$ is in sector A1, then the vectors $\bar{V}1$ and $\bar{V}2$ are utilized as shown in the figure below.
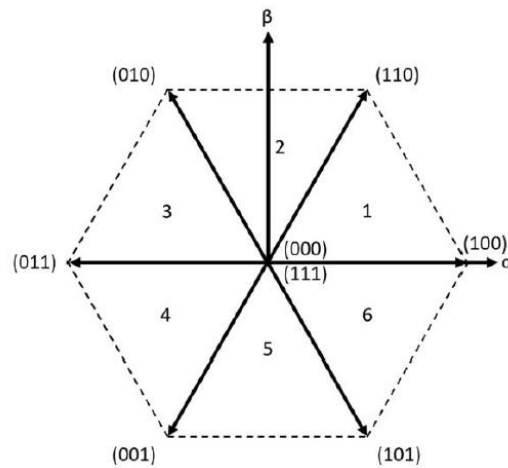

Figure 122-SVPWM two-level inverter

The hexagon Is consisting of 6 sectors leading each other by 60 degrees. there are 8 vectors which 6 vectors are active ones and 2 vectors (000) & (111) are zero vectors. These two vectors represent all upper switches off/on respectively. Using the Park transformation, the reference voltage can be written as:

$$\bar{v} = v_\alpha + jv_\beta = \frac{\sqrt{2}}{\sqrt{3}} \cdot (v_{AO} + \bar{\alpha}v_{BO} + \bar{\alpha}^2 v_{CO})$$

- $\bar{\alpha} = e^{j\frac{2}{3}\pi}$
- $v_{AO} + v_{BO} + v_{CO} = 0$

And from the equation it results:

$$v_\alpha = \frac{\sqrt{3}}{\sqrt{2}} v_{AO}$$

$$v_\beta = \frac{1}{\sqrt{2}} \cdot (v_{BO} - v_{CO}) = \frac{1}{\sqrt{2}} \cdot (2v_{BO} + v_{AO})$$

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And from the equation it results:

$$v_\alpha = \frac{\sqrt{3}}{\sqrt{2}} v_{AO}$$

$$v_\beta = \frac{1}{\sqrt{2}} \cdot (v_{BO} - v_{CO}) = \frac{1}{\sqrt{2}} \cdot (2v_{BO} + v_{AO})$$

The pole voltages can be written with respect to the middle point of the DC bus.

The phase voltages then can be obtained:

$$v_{AO} = \frac{2 \cdot v_{AN} - v_{BN} - v_{CN}}{3}$$

$$v_{BO} = \frac{2 \cdot v_{BN} - v_{AN} - v_{CN}}{3}$$

$$v_{CO} = \frac{2 \cdot v_{CN} - v_{AN} - v_{BN}}{3}$$

In the two-level inverter, the reference voltage is synthesized with the 2 nearest voltage and the zero vectors in the conventional method. In the figure below, the reference for the first sector is demonstrated:
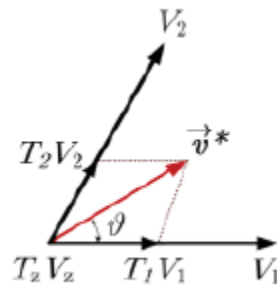

Figure 123-reference voltage in sector 1-two level inverter

As above picture, in sector one, region 3, the reference is synthesized with three nearest vectors, which are $\overline{V}_1, \overline{V}_2$:

$$V_{ref} = V_1 t_1 + V_2 t_2 + V_z t_z$$

$$T_c = t_1 + t_2 + t_z$$

And Tc is the PWM period. Z vectors is divided evenly between zero vectors (000) and (111).

It is now to split the reference voltage vector in real and imaginary part by the means of the Park transformation:

$$v_\alpha = v_{\alpha 1}t_1 + v_{\alpha 2}t_2 + v_{\alpha z}t_z$$
$$v_\beta = v_{\beta 1}t_1 + v_{\beta 2}t_2 + v_{\beta z}t_z$$

The length of each leg Is considered $\sqrt{\frac{2}{3}}V_{DC}$.

$$v_{\alpha 1} = \sqrt{\frac{2}{3}}V_{dc} \; ; \; v_{\beta 1} = 0 \; ; \; v_{\alpha 2} = \frac{1}{\sqrt{6}}V_{dc} \; ; \; v_{\beta 2} = \frac{1}{\sqrt{2}}V_{dc}$$

To simplify previous equations, since they present common terms, it is possible to introduce 2 coefficients:

$$H_1 = \frac{\sqrt{3} \cdot T_s \cdot V_{\alpha_{ref}}}{\sqrt{2} \cdot V_{dc}}$$
$$H_2 = \frac{T_s \cdot V_{\beta_{ref}}}{\sqrt{2} \cdot V_{dc}}$$

Now, it is possible to calculate the value of the real and Imaginary over the switching period:

$$V_\alpha = \frac{1}{T_s} \cdot \left(\sqrt{\frac{2}{3}}t_1 + \frac{1}{\sqrt{6}}t_2 \right) \cdot V_{dc}$$
$$V_\beta = \frac{1}{T_s} \cdot \frac{1}{\sqrt{2}}t_2 \cdot V_{dc}$$

The application times is now can be obtained based on above equations:

$$t_1 = H_1 - H_2$$
$$t_2 = 2 \cdot H_2$$
$$t_0 = T_s - t_1 - t_2$$

The other sector that can be taken as an example is sector 2:

In sector 2, the reference voltage is synthesized with the neighbouring vectors $\overline{V}_2$, $\overline{V}_3$.

$$v_\alpha = v_{\alpha 2} t_2 + v_{\alpha 3} t_3 + v_{\alpha z} t_z$$
$$v_\beta = v_{\beta 2} t_2 + v_{\beta 3} t_3 + v_{\beta z} t_z$$

If the length of the vector is considered $\sqrt{\frac{2}{3}} V_{DC}$:

$$v_{\alpha 2} = \sqrt{\frac{2}{3}} \frac{V_{DC}}{2} \; ; \; v_{\beta 2} = \frac{1}{\sqrt{2}} V_{dc} \; ; \; v_{\alpha 3} = -\sqrt{\frac{2}{3}} \frac{V_{DC}}{2} \; ; \; v_{\beta 3} = \frac{1}{\sqrt{2}} V_{dc}$$

And considering the 2 coefficients H1 and H2, the average value over the switching period is determined:

$$V_\alpha = \frac{1}{T_s} \cdot \left(\sqrt{\frac{2}{3}} t_2 - \sqrt{\frac{2}{3}} t_3 \right) \cdot \frac{V_{DC}}{2}$$

$$V_\beta = \frac{1}{T_s} \cdot \frac{1}{\sqrt{2}} \cdot (t_1 + t_2) \cdot V_{dc}$$

At the end the application times for vectors 2 and 3 are obtained:

$$t_2 = H_1 + H_2$$
$$t_3 = H_2 - H_1$$
$$t_0 = T_s - t_2 - t_3$$

Once the application times are determined, it is possible to find the reference times for each leg. These modulation waveforms are then compared with a triangular waveform with the duration of Ts. The comparator results are then given to the IGBT switches.
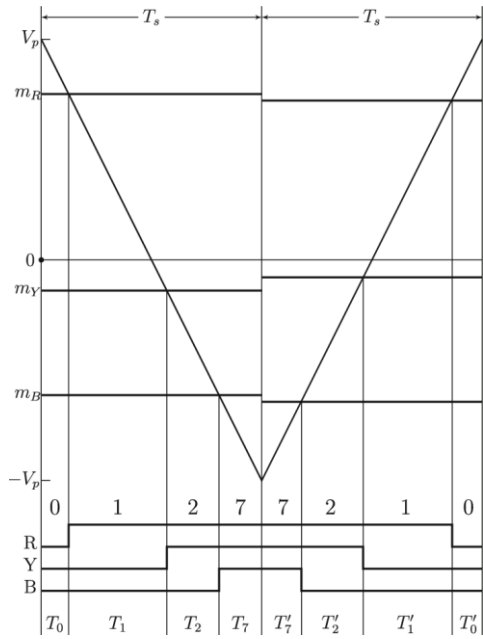
Figure 124-Carrier signal comparison

During the PWM period, the configurations must follow two rules:

1. The sequence must be symmetrical with respect to the central point and always first increasing and then decreasing.
2. when changing from one vector to another, just one leg should change at the time.

As an example, the switching table of the sectors 1 and 2 are given.

Table 13-switching tables for sector 1 & 2, 2L inverter,conventional method

		0	1	2	7	7	2	1	0	
		OOO	POO	PPO	PPP	PPP	PPO	POO	OOO	t_IGBT
sector 1	IGBTa_1		1	1	1	1	1	1		t1+t2+t0/2
	IGBTb_1			1	1	1	1			t0/2+t2
	IGBTc_1				1	1				t0/2

sector 2		0	3	2	7	7	2	3	0	
		OOO	OPO	PPO	PPP	PPP	PPO	OPO	OOO	t_IGBT
	IGBTa_1			1	1	1	1			t2+t0/2
	IGBTb_1		1	1	1	1	1	1		t2+t0/2+t3
	IGBTc_1				1	1				t0/2

This allows us to write the application times:

Table 14-Application times for 2L inverter, conventional method

Sector	Active states	Conditions	Application times
1	POO PPO	H2>0 H1>H2	t1 = H1-H2 t2 = 2H2 t0 = Tc-H1-H2
2	PPO OPO	H2>0 H2>H1	t2 = H1+H2 t3 = H2-H1 t0 = Tc-2H2
3	OPO OPP	H2>0 H2<-H1	Tt3 = 2H2 Tt4 = -H1-H2 Tt0 = Tc+H1-H2
4	OPP OOP	H2<0 H2>H1	t4 = -H1+H2 t5 = -2H2 t0 = Tc+H2+H1
5	OOP POP	H2<0 H2<H1	t5 = -H1-H2 t6 = H1-H2
6	POP POO	H2<0 H2>-H1	t1 = H1+H2 t6 = -2H2 t0 = Tc-H1+H2

Once the application, reference times and the conditions are determined, it is possible to implement the method in a MATLAB Function. The variables of the space vector PWM techniques are v_α, v_β, Fs and Vdc. The output values are the modulation waveforms that then are compared with a triangular waveform.

//MATLAB code

```
Function [Out_1,Out_2,Out_3,sector] = fcn(Valpha,Vbeta,Fs,Vdc)

Ts = 1/Fs;

Tc = Ts/2;

H1 = sqrt(3/2) * Tc * Valpha/Vdc;

H2 = Vbeta * Tc/(sqrt(2)*Vdc);


if H2 >0

if H1 > H2

sector = 1;

Tt1 = H1-H2;

Tt2 = 2*H2;

Tt0 = Tc- Tt1-Tt2;

if (Tt0<0)

b=Tc/(Tt1+Tt2);

Tt1=Tt1*b;

Tt2=Tt2*b;

Tt0=0;

end


Ta = Tt0/2;

Tb = Tt0/2+Tt1;

Tc_1 = Tt0/2+Tt1+Tt2;


elseif H2 < -H1

sector = 3;



else

sector = 2;

    end
```

```matlab
else
    if H2>H1

        sector = 4;


    elseif H2 > -H1
        sector = 6;



    else
        sector = 5;


    end
end



Out_1 = Tc-Ta;
Out_2 = Tc-Tb;
Out_3 = Tc-Tc_1;
```

7.3   AZSPWM

As the common mode voltage is defined in the literature the voltage between the star points of the load and the supply ground. It can also be expressed as the average value of the output three-phase voltage.

A basic schematic of two-level inverter is considered.
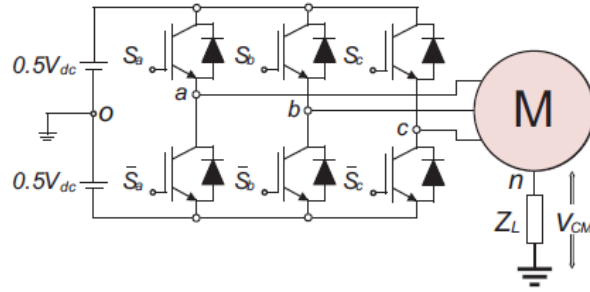
The resulted vectors and corresponding instantaneous CMV magnitude for each switching vectors are summarized in Table below. It can be obvious from Table that, the switching vectors of the VSI can be classified according to the CMV magnitudes to:

- Large CMV (+-Vdc/2) that produced by zero-vectors.
- Small CMV (+-Vdc/6) that produced by the other vectors.

Table 15-Switching states of 2L inverter

Switching state			Phase Voltage			CMV
A	B	C	Van	VBn	VCn	
0	0	0	-1/2Vdc	-1/2Vdc	-1/2Vdc	-1/2Vdc
1	0	0	1/2Vdc	-1/2Vdc	-1/2Vdc	-1/6Vdc
1	1	0	1/2Vdc	1/2Vdc	-1/2Vdc	1/6Vdc
0	1	0	-1/2Vdc	1/2Vdc	-1/2Vdc	-1/6Vdc
0	1	1	-1/2Vdc	1/2Vdc	1/2Vdc	1/6Vdc
0	0	1	-1/2Vdc	-1/2Vdc	1/2Vdc	-1/6Vdc
1	0	1	1/2Vdc	-1/2Vdc	1/2Vdc	1/6Vdc
1	1	1	1/2Vdc	1/2Vdc	1/2Vdc	+1/2Vdc

The largest CMV corresponds to the two zero vectors (000) and (111).

To avoid the peak of the CMV, the AZSPWM technique is used. In this method, the zero vectors are replaced by the opposite active vectors and the zero-vector time is divided evenly between these two opposite vectors.

For the sector 1, the reference voltage is synthesized by the active vectors $\overline{V}_1$, $\overline{V}_2$ as the conventional method and the zero vector is replaced by the two opposite vectors $\overline{V}_3$, $\overline{V}_6$.
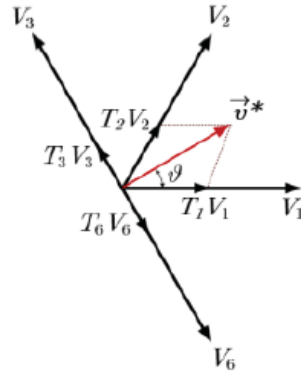
Figure 125-AZSPWM-sector 1

Therefore, the reference voltage can be written as:

$$V_{ref} = V_1 t_1 + V_2 t_2 + V_3 t_3 + V_6 t_6$$

$$T_c = t_1 + t_2 + t_z$$

$$T_z = t_3 + t_6$$

It is now to split the reference voltage vector in real and imaginary part by the means of the Park transformation:

$$v_\alpha = v_{\alpha 1} t_1 + v_{\alpha 2} t_2 + v_{\alpha 3} t_3 + v_{\alpha 6} t_6$$
$$v_\beta = v_{\beta 1} t_1 + v_{\beta 2} t_2 + + v_{\beta 3} t_3 + + v_{\beta 6} t_6$$

The length of each leg is considered $\sqrt{\frac{2}{3}} V_{DC}$.

$$v_{\alpha 1} = \sqrt{\frac{2}{3}} V_{dc} \; ; \; v_{\beta 1} = 0 \; ; \; v_{\alpha 2} = \frac{1}{\sqrt{6}} V_{dc} \; ; \; v_{\beta 2} = \frac{1}{\sqrt{2}} V_{dc}$$

To simplify previous equations, since they present common terms, it is possible to introduce

2 coefficients:

$$H_1 = \frac{\sqrt{3} \cdot T_s \cdot V_{\alpha_{ref}}}{\sqrt{2} \cdot V_{dc}}$$
$$H_2 = \frac{T_s \cdot V_{\beta_{ref}}}{\sqrt{2} \cdot V_{dc}}$$

Now, it is possible to calculate the value of the real and imaginary over the switching period:

$$V_\alpha = \frac{1}{T_s} \cdot \left(\sqrt{\frac{2}{3}} t_1 + \frac{1}{\sqrt{6}} t_2 - \frac{1}{\sqrt{6}} t_3 + \frac{1}{\sqrt{6}} t_6 \right) \cdot V_{dc}$$

Considering that t3 and t6 are equal, the average value can be rewritten:

$$V_\alpha = \frac{1}{T_s} \cdot \left(\sqrt{\frac{2}{3}} t_1 + \frac{1}{\sqrt{6}} t_2 \right) \cdot V_{dc}$$

$$V_\beta = \frac{1}{T_s} \cdot \frac{1}{\sqrt{2}} t_2 \cdot V_{dc}$$

The application times is now can be obtained based on above equations:

$$t_1 = H_1 - H_2$$
$$t_2 = 2 \cdot H_2$$
$$t_3 = t_6 = T_s - t_1 - t_2$$

The result for each sector is provided in the table below:

Table 16-Application times for AZSPWM,2L inverter

Sector	Active states	Conditions	Application times
1	POO PPO OPO POP	H2>0 H1>H2	t1 = H1-H2 t2 = 2H2 t3=t6 = Tc-H1-H2
2	PPO OPO POO OPP	H2>0 H2>H1	t2 = H1+H2 t3 = H2-H1 t4=t1 = Tc-2H2
3	OPO OPP PPO OOP	H2>0 H2<-H1	Tt3 = 2H2 Tt4 = -H1-H2 t2=t5 = Tc+H1-H2
4	OPP OOP OPO POP	H2<0 H2>H1	t4 = -H1+H2 t5 = -2H2 t3=t6 = Tc+H2+H1
5	OOP POP OOP PPO	H2<0 H2<H1	t5 = -H1-H2 t6 = H1-H2 t4=t1= Tc-t5-t6

		POP POO POP OPO	H2<0 H2>-H1	t1 = H1+H2 t6 = -2H2 t2=t5 = Tc- H1+H2
	6			

Once the application and reference times are determined, the switching table can be set up following two rules the same as the conventional method:

1. The sequence must be symmetrical with respect to the central point and always first increasing and then decreasing.
2. when changing from one vector to another, just one leg should change at the time.

Then these modulation waveforms are compared with a triangular waveform with the period equal to Ts to give the commands to the IGBTs.

As an example, the switching table of the sectors 1 and 2 are given.

Table 17-switching tables for sector 1&2 AZSPWM,2L inverters

sector 1		3 OPO	2 PPO	1 POO	6 POP	6 POP	1 POO	2 PPO	3 OPO	t_IGBT
	IGBTa_1		1	1	1	1	1	1		t1+t2+t6/2
	IGBTb_1	1	1					1	1	t2+t3/2
	IGBTc_1				1	1				t6/2

sector 2		4 OPP	3 OPO	2 PPO	1 POO	1 POO	2 PPO	3 OPO	4 OPP	t_IGBT
	IGBTa_1			1	1	1	1			t2+t1/2
	IGBTb_1	1	1	1			1	1	1	t2+t4/2+t3
	IGBTc_1	1							1	t4/2

//MATLAB code

```
function [Out_1,Out_2,Out_3,pol_1,pol_2,pol_3,sector] =
fcn(Valpha,Vbeta,Fs2,Vdc)
```

```matlab
Ts2 = 1/Fs2;
Tc = Ts2/2;
%%b = 0;


H1 = sqrt(3/2) * Tc * Valpha/Vdc;
H2 = Vbeta * Tc/(sqrt(2)*Vdc);


if H2 >0
    if H1 > H2
        sector = 1;
        Tt1 = H1-H2;
        Tt2 = 2*H2;
        Tt6 = Tc- Tt1-Tt2;
        Tt3 = Tt6;




        if Tt6 <0
            b=Tc/(Tt2+Tt1);
            Tt1=Tt1*b;
            Tt2=Tt2*b;
            Tt6=0;
            Tt3=0;
        end


        Ta = Tt1+Tt2+Tt6/2;
        Tb = Tc-(Tt3/2+Tt2);
        Tc_1 = Tt6/2;
        pol_1 = 1;
        pol_2 = 0;
```

```matlab
        pol_3 = 1;


    elseif H2 < -H1
        sector = 3;


        Tt3 = 2*H2;
        Tt4 = -H1-H2;
        Tt2 = Tc-Tt4-Tt3;
        Tt5 = Tt2;



        if Tt2 <0
            b=Tc/(Tt4+Tt3);
            Tt4=Tt4*b;
            Tt3=Tt3*b;
            Tt2=0;
            Tt5=0;
        end



        Ta = Tt2/2;
        Tb = Tt2/2+Tt3+Tt4;
        Tc_1 = Tc-(Tt4+Tt5/2);


        pol_1 = 1;
        pol_2 = 1;
        pol_3 = 0;


    else
sector = 2;
```

```
end


else
if H2>H1
sector = 4;


elseif H2 > -H1
sector = 6;
else
end
end



Out_1 = Ta;
Out_2 = Tb;
Out_3 = Tc_1;
```

7.4   Three-level SVPWM with the three nearest vectors

For three-level inverter, there is 27 states that three of them are zero states and 24 of them are active states.

Table 18-symbols definition for 3L inverter switching states

Switching State	Device Switching Status (Phase A)			
	S_1	S_2	S_3	S_4
P	On	On	Off	Off
O	Off	On	On	Off
N	Off	Off	On	On
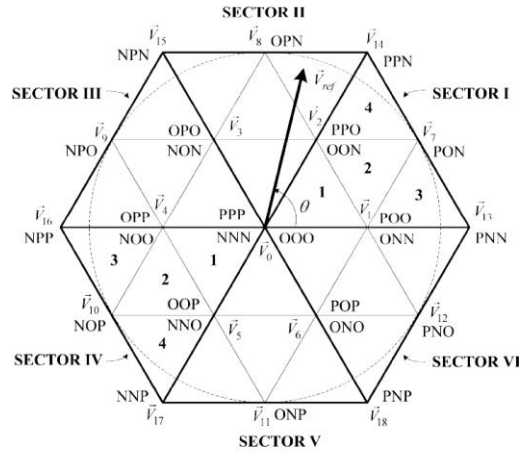
Figure 126-SVM of Three-level inverter

So, at any time instant, at any given moment the concatenated voltage rotating vector can be identified by the time-weighted summation of the three vectors that identify the vertices of the triangle in which it is located at that instant.
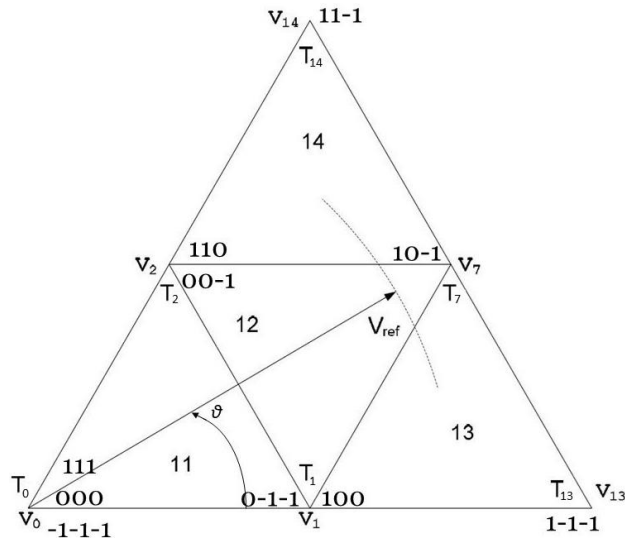
Figure 127-Sector1-Region3 application time

As above picture, in sector one, region 3, the reference is synthesized with three nearest vectors, which are $\bar{V}_1$, $\bar{V}_2$ and $\bar{V}_7$:

$$\bar{V}_{ref} \cdot T_s = \bar{V}_1 \cdot T_1 + \bar{V}_2 \cdot T_2 + \bar{V}_7 \cdot T_7$$

$$\bar{V}_1 = \frac{1}{\sqrt{6}} \cdot V_{dc}; \quad \bar{V}_2 = \frac{1}{\sqrt{6}} \cdot V_{dc} \cdot e^{j\frac{\pi}{3}}; \quad \bar{V}_7 = \frac{1}{\sqrt{2}} \cdot V_{dc} \cdot e^{j\frac{\pi}{6}};$$

$$\bar{V}_{ref} = V_{ref} \cdot e^{j\theta}$$

$$V_{ref} \cdot (\cos\theta + j\sin\theta) \cdot T_s =$$

$$= \frac{1}{\sqrt{6}} \cdot V_{dc} \cdot T_1 + \frac{1}{\sqrt{6}} \cdot V_{dc} \cdot \left(\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}\right) \cdot T_2 + \frac{1}{\sqrt{2}} \cdot V_{dc} \cdot \left(\cos\frac{\pi}{6} + j\sin\frac{\pi}{6}\right) \cdot T_7$$

It is now to split the reference voltage vector in real and imaginary part:

$$\bar{V}_{ref} = V_{\alpha_{ref}} + jV_{\beta_{ref}}$$

$$V_{\alpha_{ref}} \cdot T_s = \frac{1}{\sqrt{6}} \cdot V_{dc} \cdot T_1 + \frac{1}{2\sqrt{6}} \cdot V_{dc} \cdot T_2 + \frac{\sqrt{3}}{2\sqrt{2}} \cdot V_{dc} \cdot T_7$$

$$V_{\beta_{ref}} \cdot T_s = \frac{1}{2\sqrt{2}} \cdot V_{dc} \cdot T_2 + \frac{1}{2\sqrt{2}} \cdot V_{dc} \cdot T_7$$

Remembering that $T_s = T_1 + T_2 + T_7$, it is:

$$T_1 = T_s - \frac{2\sqrt{2} \cdot T_s \cdot V_{\alpha_{ref}}}{V_{dc}}$$

$$T_2 = T_s - \frac{\sqrt{6} \cdot T_s \cdot V_{\alpha_{ref}}}{V_{dc}} + \frac{\sqrt{2} \cdot T_s \cdot V_{\beta_{ref}}}{V_{dc}}$$

$$T_7 = \frac{\sqrt{6} \cdot T_s \cdot V_{\alpha_{ref}}}{V_{dc}} + \frac{\sqrt{2} \cdot T_s \cdot V_{\beta_{ref}}}{V_{dc}} - T_s$$

To simplify previous equations, since they present common terms, it is possible to introduce 2 coefficients:

$$H_1 = \frac{\sqrt{3} \cdot T_s \cdot V_{\alpha_{ref}}}{\sqrt{2} \cdot V_{dc}}$$

$$H_2 = \frac{T_s \cdot V_{\beta_{ref}}}{\sqrt{2} \cdot V_{dc}}$$

This allows to rewrite the application times as:

$$T_1 = T_s - 4H_2$$

$$T_2 = -2H_1 + 2H_2 + T_s$$

$$T_7 = -T_s + 2H_1 + 2H_2$$

In the following, the calculation of the application times and reference ones is carried out.

Table 19-Application times for the conventional SVPWM ,3L inverters

Sector	Region	Active states	Conditions	Application times
1	1	OON ONN OOO	$H2 > 0$ $H2 < H1$ $H2 < -H1 + 1/2$	Tt1 = 2*H1 -2*H2; Tt2 = 4*H2; Tt0 = -2*H1 -2*H2 + Tc;
	2	ONN OON PON	$H2 < 1/4$ $H2 > H1 - 1/2$ $H2 > -H1 + 1/2$	Tt1 = -4*H2 + Tc; Tt2 = -2*H1 + 2*H2 + Tc; Tt7 = 2*H1 +2*H2 - Tc;
	3	ONN PNN PON	$H2 > 0$ $H2 < H1 - 1/2$	Tt1 = -2*H1 -2*H2 + 2*Tc; Tt7 = 4*H2; Tt13= 2*H1 -2*H2 -Tc;
	4	OON PON PPN	$H2 < H1$ $H2 > 1/4$	Tt2 = -2*H1 - 2*H2 +2*Tc; Tt7 = 2*H1 -2*H2; Tt14= 4*H2 -Tc;
2	1	OON OOO OPO	$H2 > H1$ $H2 > -H1$ $H2 < 1/4$	Tt0 = -4*H2 + Tc; Tt2 = 2*H1 + 2*H2; Tt3 = -2*H1 + 2*H2;
	2	OON OPN OPO	$H2 > ¼$ $H2 < H1 + 1/2$ $H2 < -H1 + 1/2$	Tt8 = 4*H2 -Tc; Tt2 = 2*H1 - 2*H2 +Tc; Tt3 = -2*H1 -2*H2 +Tc;
	3	OON OPN PPN	$H2 > H1$ $H2 > -H1 + 1/2$	Tt2 = -4*H2 + 2*Tc; Tt8 = -2*H1 + 2*H2; Tt14= 2*H1 + 2*H2 - Tc;
	4	NON NPN OPN	$H2 > -H1$ $H2 > H1 + 1/2$	Tt3 = -4*H2 + 2*Tc; Tt8 = 2*H1 + 2*H2; Tt15= -2*H1 + 2*H2 - Tc;
3	1	NON NOO OOO	$H2 < -H1$ $H2 > 0$ $H2 < H1 + 1/2$	Tt0 = 2*H1 -2*H2 +Tc; Tt3 = 4*H2; Tt4 = -2*H1 -2*H2;
	2	NOO NON NPO	$H2 < 1/4$ $H2 > -H1 – 1/2$ $H2 > H1 + 1/2$	Tt3 = 2*H1 + 2*H2 + Tc; Tt4 = -4*H2 + Tc; Tt9 = -2*H1 + 2*H2 - Tc;

	3	NON NPN NPO	H2 < - H1 H2 > 1/4	Tt3 = 2*H1 -2*H2 +2*Tc; Tt9 = -2*H1 -2*H2; Tt15= 4*H2 - Tc;
	4	NOO NPO NPP	H2 > 0 H2 < - H1 − 1/2	Tt4 = 2*H1 -2*H2 +2*Tc; Tt9 = 4*H2; Tt16= -2*H1 -2*H2 -Tc;
4	1	NOO OOO OOP	H2 < 0 H2 > - H1 − 1/2 H2 > H1	Tt0 = 2*H1 + 2*H2 +Tc; Tt4 = -2*H1 +2*H2; Tt5 = -4*H2;
	2	NOO NOP OOP	H2 > -1/4 H2 < - H1 − 1/2 H2 < H1 + 1/2	Tt4 = 4*H2 +Tc; Tt5 = 2*H1 -2*H2 +Tc; Tt10= -2*H1 -2*H2 -Tc;
	3	NOO NOP NPP	H2 < 0 H2 > H1 + 1/2	Tt4 = 2*H1 +2*H2 +2*Tc; Tt10= -4*H2; Tt16= -2*H1 +2*H2 -Tc;
	4	NNO NNP NOP	H2 > H1 H2 < - 1/4	Tt5 = 2*H1 +2*H2 +2*Tc; Tt10= -2*H1 +2*H2; Tt17= -4*H2 -Tc;
5	1	NNO ONO OOO	H2 > -1/4 H2 < H1 H2 > - H1	Tt0 = 4*H2 +Tc; Tt5 = -2*H1 -2*H2; Tt6 = 2*H1 -2*H2;
	2	NNO ONO ONP	H2 < -1/4 H2 > H1 − 1/2 H2 > - H1 − 1/2	Tt5 = -2*H1 +2*H2 +Tc; Tt6 = 2*H1 +2*H2 +Tc; Tt11= -4*H2 -Tc;
	3	NNO NNP ONP	H2 < h1 H2 < - H1 − 1/2	Tt5 = 4*H2 +2*Tc; Tt11= 2*H1 -2*H2; Tt17= -2*H1 -2*H2 -Tc;
	4	ONO ONP PNP	H2 < - H1 H2 < H1 − 1/2	Tt6 = 4*H2 + 2*Tc; Tt11= -2*H1 -2*H2; Tt18= 2*H1 -2*H2 -Tc;
6	1	ONO OOO POO	H2 < 0 H2 > - H1 H2 > H1 − 1/2	Tt0 = -2*H1 +2*H2 +Tc; Tt1 = 2*H1 + 2*H2; Tt6 = -4*H2;
	2	ONO PNO POO	H2 > -1/4 H2 < - H1 + 1/2 H2 < H1 − 1/2	Tt1 = 4*H2 +Tc; Tt6 = -2*H1 -2*H2 +Tc; Tt12= 2*H1 -2*H2 -Tc;
	3	ONO PNO PNP	H2 > - H1 H2 < -1/4	Tt6 = -2*H1 +2*H2 +2*Tc; Tt12= 2*H1 +2*H2; Tt18= -4*H2 -Tc;

	4	ONN PNN PNO	H2 < 0 H2 > - H1 + 1/2	Tt1 = -2*H1 + 2*H2 + 2*Tc; Tt12 = -4*H2; Tt13 = 2*H1 +2*H2 -Tc;

Once the application times are determined, the reference times are obtained by comparing the reference times with the triangular carrier signal.

During the PWM period, the configurations must follow two rules:

3. The sequence must be symmetrical with respect to the central point and always first Increasing and then decreasing.
4. when changing from one vector to another, just one leg should change at the time.

The small-vectors (V1 – V6) are each characterized by two different possible configurations but identical to the effects of chained voltages.

Table 20-P&N type vectors for 3L SVPWM

Vector	N-type	P-type
V1	ONN	POO
V2	OON	PPO
V3	NON	OPO
V4	NOO	OPP
V5	NNO	OOP
V6	ONO	POP

In order to obtain the switching table for each region and sector, it is necessary to use both types of small vectors, N-type and P-type, in such a way that the sequence starts with the N-type vector until reaching the P-type vector.

As an example, the switching sequence of region 13 is given.

Table 21-switching table for 3L inverters, conventional method

		1	13	7	1	1	7	13	1
		ONN	PNN	PON	POO	POO	PON	PNN	ONN
Regione 13	IGBTa_1		1	1	1	1	1	1	
	IGBTa_2	1	1	1	1	1	1	1	1
	IGBTb_1								
	IGBTb_2			1	1	1	1		
	IGBTc_1								
	IGBTc_2				1	1			

It starts with the N-type vector (ONN) until it reaches the P-type vector (POO).

In order to obtain the reference time for each IGBT, the on-time of each vector is summed up.

Table 22-obtaining the reference time in 3L inverters, conventional method

		1	13	7	1	1	7	13	1	t_IGBT
		ONN	PNN	PON	POO	POO	PON	PNN	ONN	
Regione 13	IGBTa_1		1	1	1	1	1	1		t1/2+t7+t13
	IGBTa_2	1	1	1	1	1	1	1	1	Tc
	IGBTb_1									0
	IGBTb_2			1	1	1	1			t1/2+t7
	IGBTc_1									0
	IGBTc_2				1	1				t1/2

Region 1 and region 2 are of interest as each have 2 small-vectors at their vertices. For this reason, these regions are divided into two sub-regions (a and b). The two sub-regions will exploit sequences of different configurations in order to make greater use of small-vectors closest to the rotating vector.
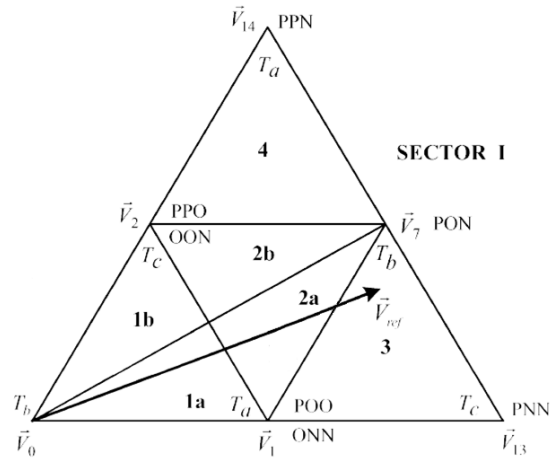
Figure 128-Region1&2 division

As an example, the sequence of the first region Is provided in the tables below

Table 23-sub regions in sector 1, 3L inverter

		1	2	0	1	1	0	2	1	
		ONN	OON	OOO	POO	POO	OOO	OON	ONN	t_IGBT
	IGBTa_1				1	1				t1/2
	IGBTa_2	1	1	1	1	1	1	1	1	Tc
Regione 11a	IGBTb_1									0
	IGBTb_2		1	1	1	1	1	1		t1/2+t0+t2
	IGBTc_1									0
	IGBTc_2			1	1	1	1			t1/2+t0

		2	0	1	2	2	1	0	2	
		OON	OOO	POO	PPO	PPO	POO	OOO	OON	t_IGBT
	IGBTa_1			1	1	1	1			t2/2+t1
	IGBTa_2	1	1	1	1	1	1	1	1	Tc
Regione 11b	IGBTb_1				1	1				t2/2
	IGBTb_2	1	1	1	1	1	1	1	1	Tc
	IGBTc_1									0
	IGBTc_2		1	1	1	1	1	1		t2/2+t1+t0

To realize which region and sector the reference voltage resides in, some conditions are imposed based on alpha-beta values. Through park transformation, the reference voltages are transformed to alpha-beta values. These two values are always tangential to each other. If the hexagon is divided into six sectors, each sector leads by 60 degrees by another.

Based on alpha-beta values, easily each sector can be realized. To determine the regions, the reference voltage is synthesized with the three nearest vectors and application times are also determined:

Below you can find the MATLAB code for the sector 3. region 3:

```
function region = fcn(sector, Valpha, Vbeta,fs,Vdc)


Ts = 1/fs;

Tc = Ts/2,

region = 0;


H1 = sqrt(2/3)*Tc* Valpha*/Vdc;

H2 = Tc*Vbeta/(sqrt(2)*Vdc);


if H2 > 0

  if H2 < H1

  %%   sector = 1;


    if H2 < -H1+ Tc/2;

      region = 11;

    elseif H2 > Tc/4;

      region = 14;

    elseif H2 < H1 - Tc/2,

      region = 13;

    else

      region = 12;

    end

  end
```

```
    elseif H2 > Tc/4

      %%region = 33;

      Tt3 = 2*H1 -2*H2 +2*Tc;

      Tt9 = -2*H1 -2*H2;

      Tt15= 4*H2 - Tc;


      T_a1 = 0;

      T_a2 = Tt3/2;

      T_b1 = Tt3/2+Tt9+Tt15;

      T_b2 = Tc;

      T_c1 = 0;

      T_c2 = Tt3/2 +Tt9;
```

Hence, this second transformation rotates the dq components by the angle θ, while the homopolar component remains unchanged.

7.5 MV3

As mentioned before, three-phase three-level NPC inverter has 3 legs and, in each leg, there are 4 switches. This gives 27 different states of possible combinations. The vectors can be divided into the categories of zero, small, medium, and large vectors. And each vector corresponds to a certain voltage level and common mode voltage. As previously stated, common mode voltage is the voltage measured between the star point of the load and the ground and can also be expressed as the average output value of the output voltages: Vcm = (VAO + VBO + VCO)/3.

In the table below the vectors and the corresponding common mode voltage is described:

Table 24-3L inverter's vectors division

Vectors	Switching states	CMV
Zero vectors	OOO	0
	PPP	Vdc/2
	NNN	-Vdc/2
Small vectors	POO, OOP, OPO	Vdc/6
	PPO, POP, OPP	Vdc/3
	ONN, NNO, NON	-Vdc/3
	OON, ONO, NOO	-Vdc/6
Medium vectors	PON, OPN, NPO	0
	NOP, ONP, PNO	
Large vectors	PPN, NPP, PNP	Vdc/6
	PNN, NPN, NNP	-Vdc/6
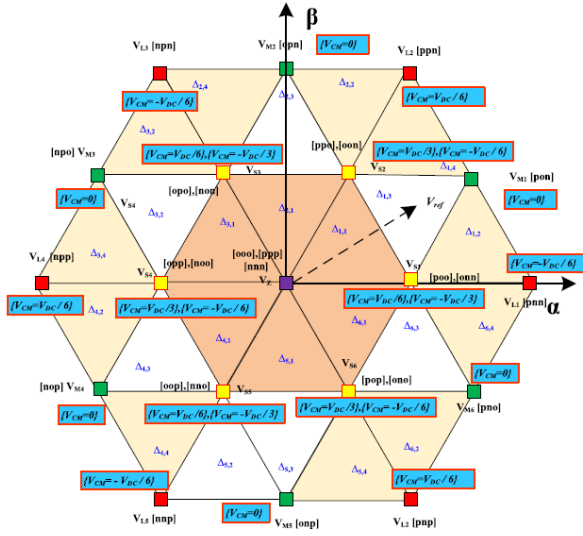
Figure 129-3L SV diagram with CMV calculation

As it is described in the table and the SV diagram, the lowest common mode voltage corresponds to the medium vectors and zero vector (OOO).

One possible solution to minimize CMV is to synthesize the reference voltage with the three nearest medium vectors. This method is called MV3.

As an example, the sector one is explained in detail.
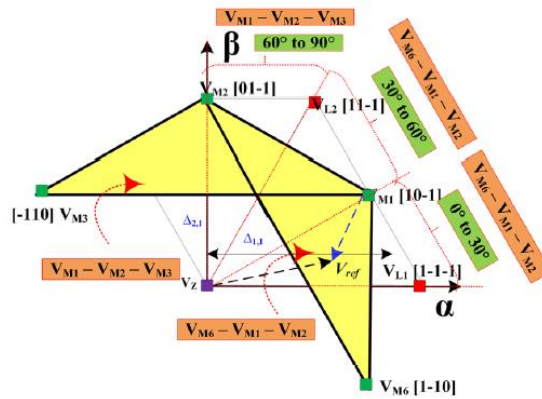
Figure 130-Sector 1,3L inverter, MV3 method

$$\bar{V}_{ref} \cdot T_s = \bar{V}_{12} \cdot T_{12} + \bar{V}_7 \cdot T_7 + \bar{V}_8 \cdot T_8$$

$$T_c = t_{12} + t_7 + t_8$$

It is now to split the reference voltage vector in real and imaginary part by the means of the Park transformation:

$$v_\alpha = v_{\alpha 12}t_{12} + v_{\alpha 7}t_7 + v_{\alpha 8}t_8$$
$$v_\beta = v_{\beta 12}t_{12} + v_{\beta 7}t_7 + + v_{\beta 8}t_8$$

The length of each leg is considered $\sqrt{\frac{2}{3}}V_{DC}$.

$$v_{\alpha 12} = \sqrt{\frac{3}{2}}\frac{V_{DC}}{2} \; ; \; v_{\beta 12} = -\frac{1}{\sqrt{2}}\frac{V_{DC}}{2} \; ; \; v_{\alpha 7} = \sqrt{\frac{3}{2}}\frac{V_{DC}}{2} \; ; \; v_{\beta 7} = \frac{1}{\sqrt{2}}\frac{V_{DC}}{2} \; ; v_{\alpha 8} = 0 \; ; \; v_{\beta 8} = \frac{1}{\sqrt{2}}V_{DC}$$

To simplify previous equations, since they present common terms, it is possible to introduce 2 coefficients:

$$H_1 = \frac{\sqrt{3} \cdot T_s \cdot V_{\alpha_{ref}}}{\sqrt{2} \cdot V_{dc}}$$
$$H_2 = \frac{T_s \cdot V_{\beta_{ref}}}{\sqrt{2} \cdot V_{dc}}$$

Now, it is possible to calculate the value of the real and Imaginary over the switching period:

$$V_\alpha = \frac{1}{T_s} \cdot \left(\sqrt{\frac{3}{2}}t_{12} + \sqrt{\frac{3}{2}}t_7 \right) \cdot \frac{V_{DC}}{2}$$
$$V_\beta = \frac{1}{T_s} \cdot \frac{1}{\sqrt{2}} (t_7 - t_{12} + 2 * t_8) \cdot \frac{V_{DC}}{2}$$

The application times is now can be obtained based on above equations:

$$t_7 = 2 * H1 + 2 * H2 - Tc$$
$$t_{13} = Tc - (4 * H1/3)$$
$$t_{12} = Tc - (2 * H1/3) - 2 * H2$$

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The conditions and reference times for each sector is summarized in the table below:

Table 25-Application times MV3 method,3L inverter

Sector	Active states	Conditions	Application times
1	PNO PON OPN	H2>0 H1>H2	Tt7 =2*H1+2*H2-Tc; Tt13 =Tc-(4*H1/3); Tt12 = Tc-(2*H1/3)-2*H2
2	PON OPN NPO	H2>0 H2>H1	Tt7 = Tc+(2*H1/3)-2*H2; Tt8 = 4*H2-Tc; Tt9 = Tc-2*H2-(2*H1/3);
3	OPN NPO NOP	H2>0 H2<-H1	Tt8 = Tc+(4*H1/3); Tt14 =2*H2-2*H1-Tc; Tt10 =Tc+(2*H1/3)-2*H2;
4	NPO NOP ONP	H2<0 H2>H1	Tt9 = Tc+2*H2+(2*H1/3); Tt10 =-2*H1-2*H2-Tc; Tt11 = Tc+(4*H1/3);
5	NOP ONP PNO	H2<0 H2<H1	Tt12 =Tc+(2*H1/3)+2*H2; Tt11 = -4*H2-Tc; Tt10 = Tc+2*H2-(2*H1/3);
6	ONP PNO PON	H2<0 H2>-H1	Tt11 = Tc- 4*H1/3 Tt12 = 2*H1-2*H2-Tc Tt7 = Tc+2*H2-2*H1/3

Once the application times are determined, the reference time is obtained by setting up the switching tables:

Table 26-switching table for MV3 method,3L inverter

		12	7	8	8	7	12	
		PNO	PON	OPN	OPN	PON	PNO	t_IGBT
sector 1	IGBTa_1	1	1			1	1	Tt12+Tt7
	IGBTa_2	1	1	1	1	1	1	Tc
	IGBTb_1			1	1			Tt8
	IGBTb_2		1	1	1	1		Tt8+Tt7
	IGBTc_1							0
	IGBTc_2	1					1	Tt12

		7	8	9	9	8	7	
		PON	OPN	NPO	NPO	OPN	PON	t_IGBT
sector 2	IGBTa_1	1					1	Tt7
	IGBTa_2	1	1			1	1	Tt7+Tt8
	IGBTb_1		1	1	1	1		Tt9+Tt8
	IGBTb_2	1	1	1	1	1	1	Tc
	IGBTc_1							0
	IGBTc_2			1	1			Tt9

In this method, the application times are not symmetrical around the center as it is shown in the tables above. To obtain the symmetry around the center, the application time of the switches that are not center aligned is subtracted from the switching period Tc and then an indicator is defined to flag out the ones that have a changed polarity. After obtaining the reference times, the modulation waveforms are then compared with a triangular waveform to give the commands to the switches. But before that to obtain the original switching pulses, a switch is placed with the threshold of 0.5 so that if the signal has been changed by Tc, the inverse of it is given to the IGBT switches.

It has been observed that the indicator that marks the change of the polarity is not synched with the carrier signal and this phenomenal results in the appearance of the seventh harmonic.
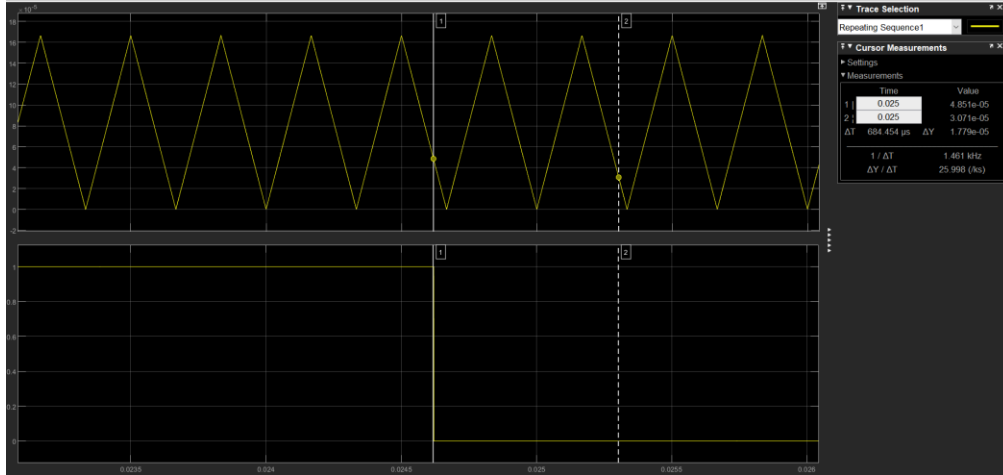
Figure 131- Indicator compared with the carrier signal

The same situation persists for the gate commands to IGBTS:
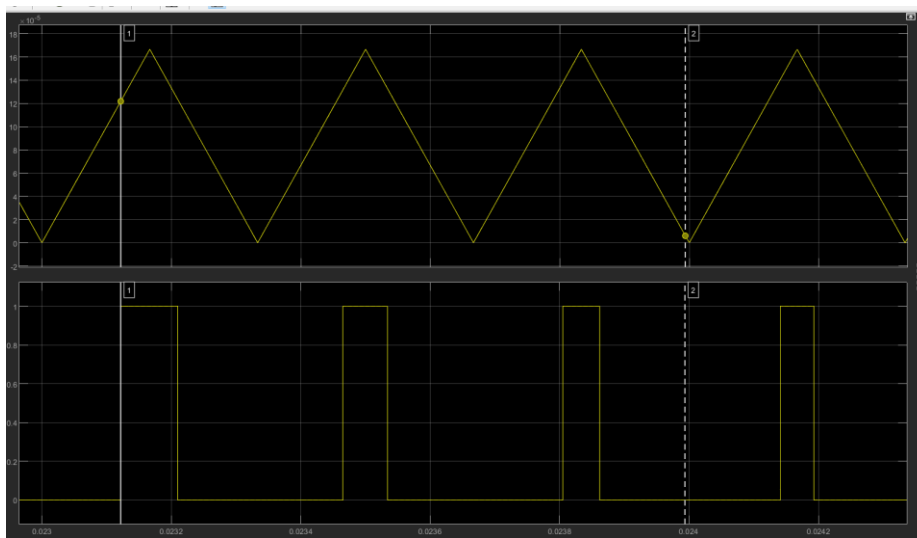
To eliminate the seventh harmonic a trigger is defined so that the polarity and the modulation waveforms are synched with the carrier signal.
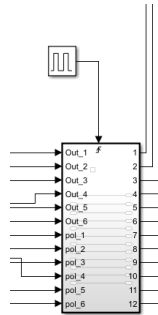
Figure 132-Trigger

The implemented MATLAB code is as below:

```matlab
function[Out_1,Out_2,Out_3,Out_4,Out_5,Out_6,pol_1,pol_2,pol_3,pol_4,pol_5,pol_6,sector]=
fcn(Valpha,Vbeta,Fs,Vdc)

Ts = 1/Fs;
Tc = Ts/2;
%%b = 0;


H1 = sqrt(3/2) * Tc * Valpha/Vdc;
H2 = Vbeta * Tc/(sqrt(2)*Vdc);


if H2 >= 0
    if H1 > H2
        sector = 1;
        Tt7 =2*H1+2*H2-Tc;
        Tt8 = Tc-(4*H1/3);
        Tt12 = Tc-(2*H1/3)-2*H2;



        Ta_1 = Tc-(Tt12+Tt7);
        Ta_2 = Tc;
        Tb_1 = Tt8;
        Tb_2 = Tt8+Tt7;
```

```
        Tc_1 = 0;
        Tc_2 = Tc-Tt12;


        pol_1 = 0;
        pol_2 = 1;
        pol_3 = 1;
        pol_4 = 1;
        pol_5 = 1;
        pol_6 = 0;


    elseif H2 <= -H1
        sector = 3;


    else
        sector = 2;


end


else
if H2 >= H1
sector = 4;


elseif H2 >= -H1
sector = 6;


else
sector = 5;


end
end
```

Out_1 = Ta_1;

Out_2 = Ta_2;

Out_3 = Tb_1;

Out_4 = Tb_2;

Out_5 = Tc_1;

Out_6 = Tc_2;

7.6   LMZV PWM technique

As explained before, the CMV can vary based on the combination of zero, small, medium, and large vectors. Therefore, a SW solution to reduce the common mode voltage is choosing the right sequence of the vectors and consequently reducing the circulating currents.

The proposed solution in this section is using the combination of zero, medium and large vectors and avoid the small vectors hence the CMV is reduced by half. Additionally, only the zero vector (OOO) Is used because the fluctuation is minimized. Therefore, the space vectors diagram is divided into 12 sectors Instead of 6 sectors as shown in the figure below:
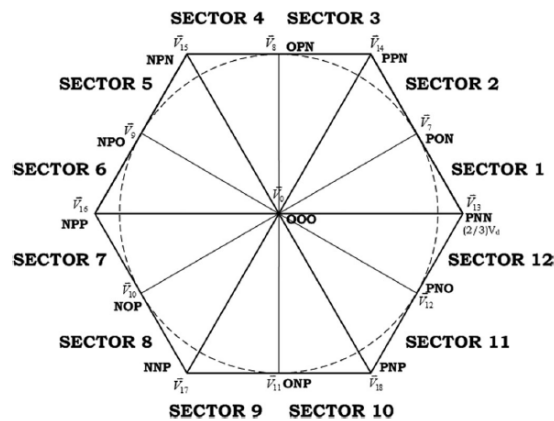
Figure 133-LMZV space vector diagram

If sector one is taken as an example, the reference voltage is synthesized by a medium, large and zero vectors as figure below:

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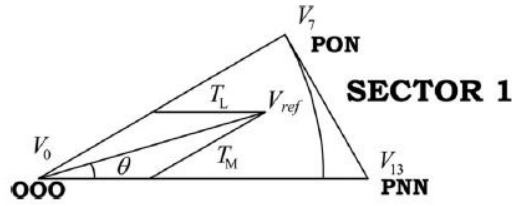
$$\bar{V}_{ref} \cdot T_s = \bar{V}_{13} \cdot T_{13} + \bar{V}_0 \cdot T_0 + \bar{V}_7 \cdot T_7$$

$$T_c = t_{13} + t_7 + t_z$$

It is now to split the reference voltage vector in real and imaginary part by the means of the Park transformation:

$$v_\alpha = v_{\alpha 13} t_{13} + v_{\alpha 7} t_7 + v_{\alpha 0} t_0$$
$$v_\beta = v_{\beta 13} t_{13} + v_{\beta 7} t_7 + + v_{\beta 0} t_0$$

The length of each leg is considered $\sqrt{\frac{2}{3}} V_{DC}$.

$$v_{\alpha 13} = \sqrt{\frac{2}{3}} V_{dc} \; ; \; v_{\beta 13} = 0 \; ; \; v_{\alpha 7} = \sqrt{\frac{3}{2}} \frac{V_{DC}}{2} \; ; \; v_{\beta 7} = \frac{1}{\sqrt{2}} \frac{V_{DC}}{2}$$

To simplify previous equations, since they present common terms, it is possible to introduce 2 coefficients:

$$H_1 = \frac{\sqrt{3} \cdot T_s \cdot V_{\alpha_{ref}}}{\sqrt{2} \cdot V_{dc}}$$

$$H_2 = \frac{T_s \cdot V_{\beta_{ref}}}{\sqrt{2} \cdot V_{dc}}$$

Now, it is possible to calculate the value of the real and imaginary over the switching period:

$$V_\alpha = \frac{1}{T_s} \cdot \left(\sqrt{\frac{2}{3}} t_1 + \frac{1}{\sqrt{6}} t_7 \right) \cdot V_{dc}$$

$$V_\beta = \frac{1}{T_s} \cdot \frac{1}{\sqrt{2}} t_7 \cdot \frac{V_{DC}}{2}$$

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The application times is now can be obtained based on above equations:

$$t_{13} = 4 * H_2$$
$$t_7 = H1 - 3 * H_2$$
$$t_0 = T_s - t_{13} - t_7$$

In the table below, the conditions for all sectors are provided:

Table 27-LMZV application times,3L inverters

Sector	Active states	Application times
1	PNN PON OOO	Tt7 =4*H2 Tt13 = H1-3*H2 Tt0 = Tc-Tt7-Tt13
2	PON PPN OOO	Tt7 = 2*H1-2*H2 Tt14 = -H1+3*H2 Tt0 = Tc-Tt7-Tt14
3	OPN PPN OOO	Tt8 = 2*H2-2*H1 Tt14 = 2*H1 Tt0 = Tc+-Tt8-Tt14
4	OPN NPN OOO	Tt9 = 2*H2+2*H1 Tt10 = -2*H1 Tt0 = Tc-Tt9-Tt10
5	NPO NPN OOO	Tt9 = -2*H1-2*H2 Tt15 = H1+3*H2 Tt0 = Tc-(Tt9+Tt16)
6	NPP NPO OOO	Tt9 = 4*H2 Tt16 =- H1-3*H2 Tt0 = Tc-(Tt9+Tt16)
7	NOP NPP OOO	Tt16 = -4*H2; Tt10 = -H1+3*H2 Tt0 = Tc-(Tt10+Tt16)
8	NNP NOP OOO	Tt10 = 2*H2-2*H1 Tt17 = H1-3*H2 Tt0 = Tc-(Tt10+Tt17)
9	ONP NNP OOO	Tt11 = -2*H2+H1 Tt17 = -2*H1 Tt0 = Tc-(Tt11+Tt17)

10	PNP ONP OOO	Tt11 = -2*H2-2*H1 Tt18 = 2*H1 Tt0 = Tc-(Tt11+Tt18)
11	PNP PNO OOO	Tt12 = 2*H2+2*H1 Tt18 = -H1-3*H2 Tt0 = Tc-(Tt12+Tt18)
12	PNN PNO OOO	Tt12 = -4*H2 Tt13 = H1+3*H2 Tt0 = Tc-(Tt12+Tt13)

The switching table is designed for every sector considering the symmetry constraints so that each sector it finishes with the zero vector. As an example, the switching table of sector 1 & 2 is provided:

Table 28-Switching table for LMZV method,3L inverters

		13 PNN	7 PON	0 OOO	0 OOO	7 PON	13 PNN	t_IGBT
sector 1	IGBTa_1	1	1			1	1	Tt13+Tt7
	IGBTa_2	1	1	1	1	1	1	Tc
	IGBTb_1							0
	IGBTb_2		1	1	1	1		Tt0+Tt7
	IGBTc_1							0
	IGBTc_2			1	1			Tt0

		14 PPN	7 PON	0 OOO	0 OOO	7 PON	14 PPN	t_IGBT
sector 2	IGBTa_1	1	1			1	1	Tt7+Tt14
	IGBTa_2	1	1	1	1	1	1	Tc
	IGBTb_1	1					1	Tt14
	IGBTb_2	1	1	1	1	1	1	Tc
	IGBTc_1							0
	IGBTc_2			1	1			Tt0

In this method similar to MV3, the application times are not symmetrical around the center as it is shown in the tables above. In order to obtain the symmetry around the center, the application time of the switches that are not center aligned is subtracted from the switching period Tc and then an indicator is defined to flag out the ones that has been changed. After obtaining the reference times, the modulation waveforms are then

compared with a triangular waveform to give the commands to the switches. But before that to obtain the original switching pulses, a switch is placed with the threshold of 0.5 so that if the signal has been changed by Tc, the inverse of it is given to the IGBT switches.

```
function [Out_1, Out_2, Out_3, Out_4, Out_5, Out_6, pol_1, pol_2, pol_3,
pol_4, pol_5, pol_6, sector,angle] = fcn(Valpha, Vbeta, Fs, Vdc)


Ts = 1/Fs;

Tc = Ts/2;

H1 = sqrt(3/2) * Tc * Valpha/Vdc;

H2 = Vbeta * Tc/(sqrt(2)*Vdc);

angle = atan2d(Vbeta,Valpha);




if (angle >= 0) && (angle <= 30)

sector = 1;


Tt7 = 4*H2;

Tt13 = H1-3*H2;

Tt0 = Tc-(Tt7+Tt13);




Ta_1 = Tc-(Tt13+Tt7);

Ta_2 = Tc;

Tb_1 = 0;

Tb_2 = Tt0+Tt7;

Tc_1 = 0;

Tc_2 = Tt0;


pol_1 = 0;
```

```
pol_2 = 1;

pol_3 = 1;

pol_4 = 1;

pol_5 = 1;

pol_6 = 1;


elseif (angle >= 30) && (angle <= 60)

sector = 2;

elseif (angle >= 60) && (angle <= 90)

sector = 3;


elseif (angle >= 90) && (angle <= 120)

sector = 4;


elseif (angle >= 120) && (angle <= 150)

sector = 5;


elseif (angle >= 150) && (angle <= 180)

sector = 6;


elseif (angle >= -180) && (angle <= -150)

sector = 7;


elseif (angle >= -150) && (angle <= -120)

sector = 8;


elseif (angle >= -120) && (angle <= -90)

sector = 9;
```

```
elseif (angle >= -90) && (angle <= -60)
sector = 10;


elseif (angle >= -60) && (angle <= -30)
    sector = 11;


else
   sector =12;
end
```

Out_1 = Ta_1;

Out_2 = Ta_2;

Out_3 = Tb_1;

Out_4 = Tb_2;

Out_5 = Tc_1;

Out_6 = Tc_2;

7.7   LCL filter design

 A LCL filter is often used to interconnect an inverter to the utility grid to filter the harmonics produced by the inverter.

 The harmonics caused by the switching of the power conversion devices are the main factor-causing problems to sensitive equipment or the connected loads, especially for applications above several kilowatts, where the price of filters and total harmonics distortion (THD) is also an important consideration in the systems design phase.

 An L filter or LCL filter is usually placed between the inverter and the grid to attenuate the switching frequency harmonics produced by the grid-connected inverter. Compared with L filter, LCL filter has better attenuation capacity of high-order harmonics and better dynamic characteristic.

 However, an LCL filter can cause stability problems due to the undesired resonance caused by zero impedance at certain frequencies. To avoid this resonance from contaminating the system, several damping techniques have been proposed. One way is to incorporate a physical passive element, such as, a resistor in series with the filter capacitor.

As discussed in the literature, the LCL filter Is sized step by step and is implemented in MATLAB.

```matlab
%% system parameters
Pn = 30000; % inverter power
En = 220; % Grid voltage
Vdc = 700; %  DC link voltage
fn = 50; % Grid frequency
wn = 2 *pi*fn;
fsw = 3000; %swicthing frequency
wsw = 2*pi*fsw;


%% Base values
Zb = (En^2)/Pn;
Cb = 1/(wn*Zb);


%% Filter Parameters
delta_Imax = 0.1*((Pn*sqrt(2))/En);
Li = Vdc/(16*fsw*delta_Imax); % inverter side inductance
x = 0.05;
Cf = x*Cb; % Filter capacitance
r = 0.6;
Lg = r*Li; % grid side inductance


%% resonance frequency
wres = sqrt ((Li+Lg)/(Li*Lg*Cf));
fres = wres/(2*pi); % resonance frequency


%% Damping resistance
Rd = 1/(3*wres*Cf);
```

```matlab
%% Transfer function of the filter

numerator = [Cf*Rd,1];

denominator = [Li*Lg*Cf,Cf*Rd*(Li+Lg),(Li+Lg),0];

sys = tf(numerator,denominator);

bode(sys)
```
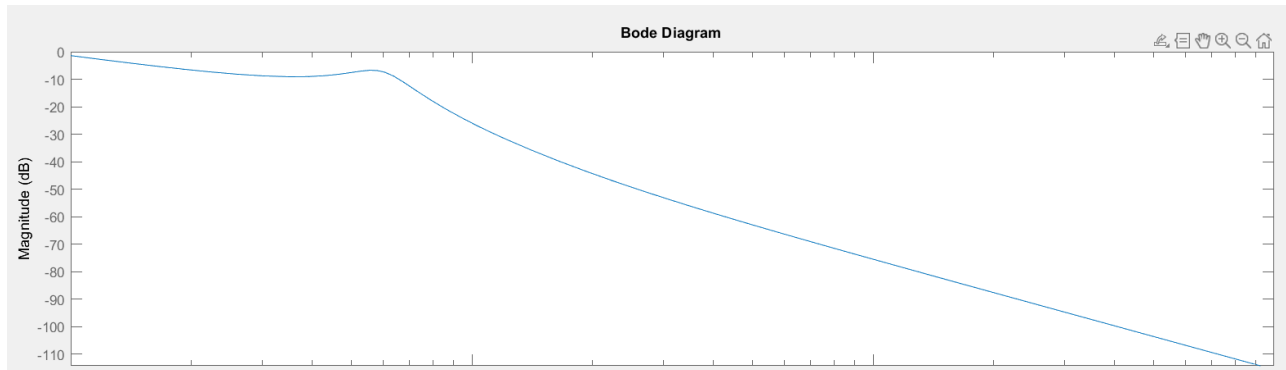

Figure 134-Filters Bode Diagram

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9 LIST OF FIGURES

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