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Design and Synthesis of Digital Circuit for Microelectrode Arrays in 180nm CMOS Technology & Real-Time Stimulation Artifact Removal Algorithm

TESI DI LAUREA MAGISTRALE IN
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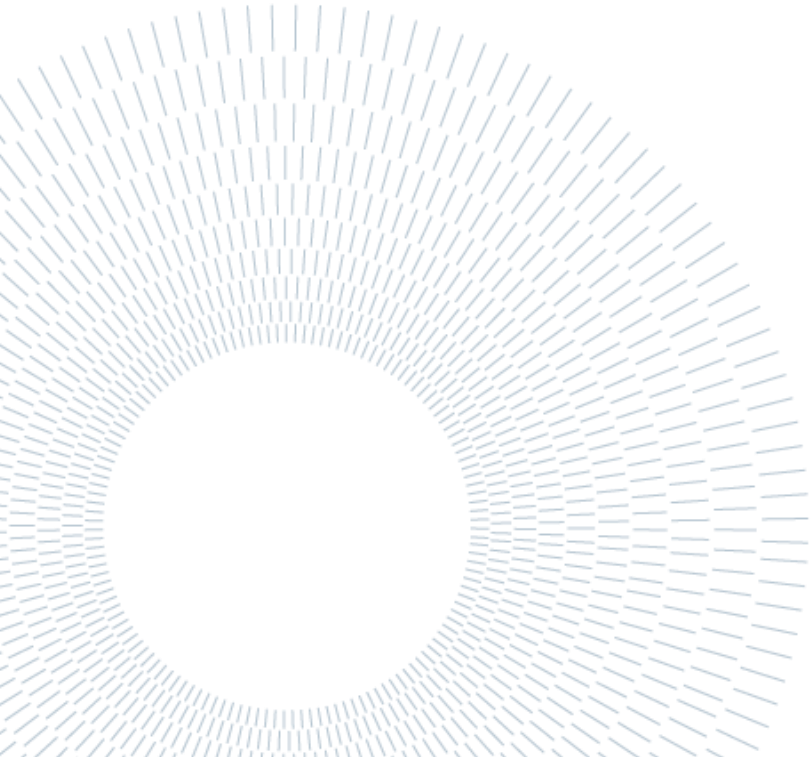


Abstract

By using complementary metal–oxide-semiconductor (CMOS) based integrated circuit (IC), integrating active microarrays for recording and stimulating electrogenic cells *in vitro* in a single chip is feasible. Active array means that circuitry components, such as amplifiers or filter units, are integrated with the digital core and the electrodes on the same substrate. As a result of integration on a single chip, the microelectrodes site close to each other. Neural cells can be cultured on microelectrode arrays (MEAs), which allow simultaneous electrical stimulation and recording of their electrical activity. This enables to study neuronal information process, neurological disorders, and the effects of drugs in electrogenic cells. During recording, all signals are recorded, including stimulation pulse and spike signals. The stimulation pulse has a significant amplitude, which causes the spike signal to be distorted, especially near the electrode where the stimulation pulse is applied.

The purpose of this work is to design and implement the digital core of the MEA integrated circuit (IC), followed by a real-time post-digital signal processing algorithm to remove the artifacts caused by the stimulation pulses. The digital core is designed at register transfer level and implemented in layout level using Modelsim, Design Compiler, and SoC Encounter tools. The real-time artifact removal algorithm is achieved through principal component analysis (PCA), which is based on Singular Value Decomposition (SVD) calculations and implemented on Xilinx Kintex-7 FPGA KC705 Evaluation Kit.

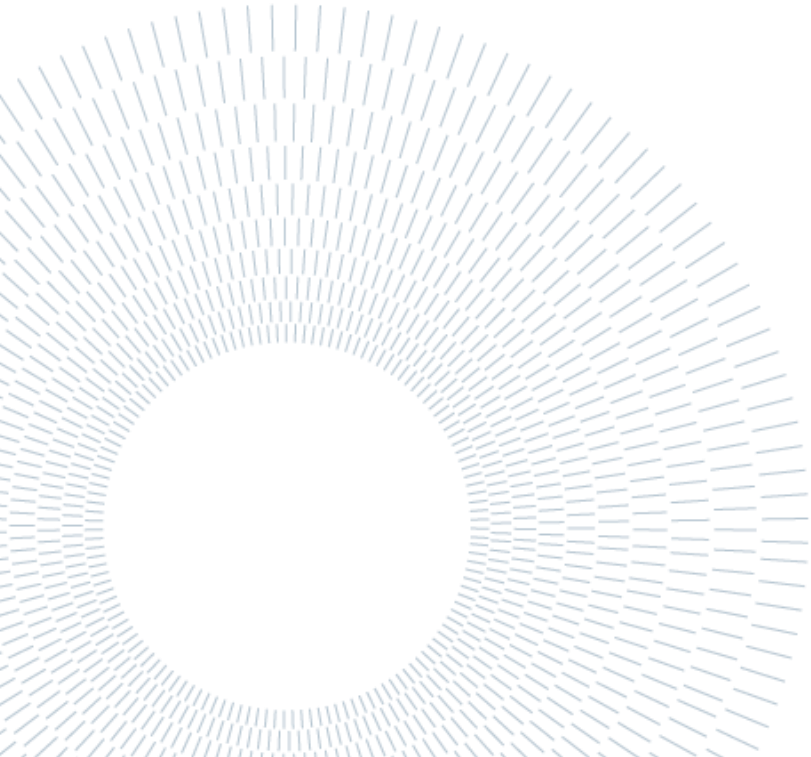
Key-words: Microelectrode arrays, Digital controller, SPI, Layout design, Stimulation artifact, Singular Value Decomposition, High-Level Synthesize.

Abstract in Italiano

Utilizzando un circuito integrato semiconduttori complementari a ossidi metallici (CMOS), è possibile l'integrazione di microarray attivi per la registrazione e la stimolazione di cellule elettrogeniche in vitro in un singolo chip. Array attivo significa che i componenti del circuito, come amplificatori o unità di filtraggio, sono integrati con gli elettrodi e il nucleo digitale sullo stesso substrato. Come risultato dell'integrazione su un singolo chip, i microelettrodi sono vicini l'uno all'altro. Le cellule neurali possono essere coltivate su array di microelettrod (MEA), che consentono simultaneamente la stimolazione elettrica e la registrazione della loro attività elettrica. Ciò consente lo studio elaborazione delle informazioni neuronali, delle malattie mentali e degli effetti dei farmaci nelle cellule elettrogeniche. Durante la registrazione, vengono registrati tutti i segnali, inclusi impulsi di stimolazione e segnali di picco. L'ampiezza dei segnali di stimolazione è molto ampia, il che impedisce di registrare chiaramente il segnale di picco, soprattutto per l'elettrodo vicino alla sorgente dell'impulso di stimolazione.

Lo scopo di questo lavoro è progettare e implementare il core digitale del circuito integrato MEA, seguito da un algoritmo di elaborazione del segnale post-digitale in tempo reale per rimuovere gli artefatti causati dagli impulsi di stimolazione. Il core digitale è progettato a livello di RTL e implementato a livello di layout, utilizzando gli strumenti Modelsim, Design Compiler e SoC Encounter. L'algoritmo di rimozione degli artefatti in tempo reale è ottenuto attraverso l'analisi dei componenti principali (PCA) basata sul calcolo della decomposizione del valore singolare (SVD) e implementata sul kit di valutazione Xilinx Kintex-7 FPGA KC705.

Parole chiave: Array di microelettrodi, controller digitale, SPI, progettazione del layout, artefatto di stimolazione, decomposizione del valore singolare, sintesi di alto livello.



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1 Introduction

1.1. Neuroscience and Electrophysiology

Electrophysiology is a branch of neuroscience devoted to study the electrical properties of biological cells and tissues. Electrophysiology typically involves measuring voltage change or electrical current flow on various scales, ranging from single ion channel proteins to whole tissues [1]. The nervous system consists of an enormous number of neuronal cells that regulate all aspects of body functions (Figure 1. 1). A human brain possesses approximately 10^{12} neurons (nerve cells), and each neuron forms thousands of connections to other neurons, creating an extensive network of electrical connections with massively parallel information processing characteristics.

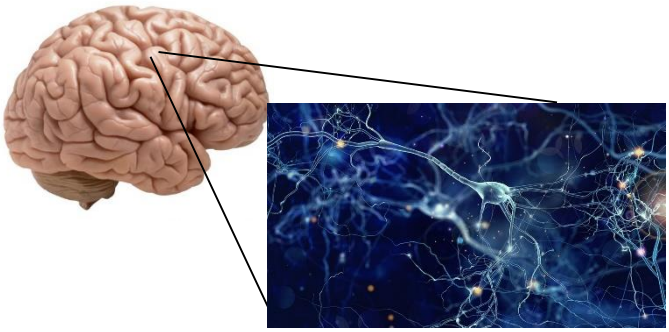

Figure 1. 1. An illustration of the human brain and neuron cells: the human brain contains large number of neurons [2]. The brain's functionality depends on the interplay between a large number of neurons. [3].

Interestingly, the output of a nervous system is impacted by both inputs and circuit properties, i.e., the wiring (synapses) that are established among its neurons and the strength of their interconnections (synapses). The synaptic connections between neurons can be reorganized, a phenomenon known as synaptic plasticity, and is believed to be the mechanism for learning in our brain. Neurons can be classified into different types based on their physiology and function [4], [5]. Neurons are

composed of four distinct regions with different functions: the cell body, the dendrites, the axon, and the axon terminals (Figure 1. 2).

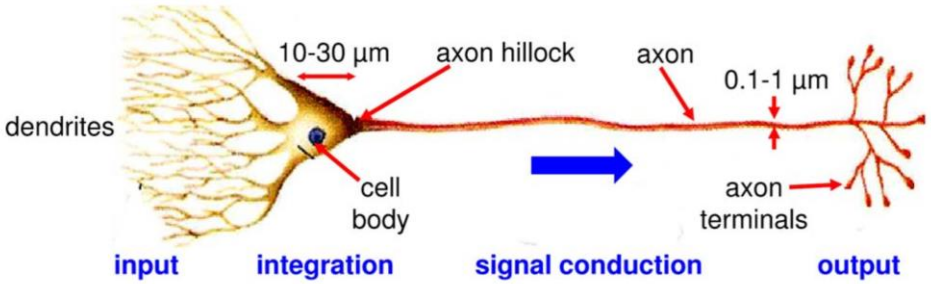

Figure 1. 2. Schematic view of a neuron cell [6]. A neuron's cell body is surrounded by dendrites, which conduct electrical pulses called action potentials away from the cell body to its axon terminals.

The neural cell body, also known as the soma, which has a diameter of 10–30 µm, contains the nucleus, which produces most of the neuronal proteins.

Almost all neurons are composed of a single axon, and their diameters can vary considerably, from micrometers in the human brain to hundreds of millimeters in the giant squid. An axon has the specific function of conducting electrical pulses, called action potentials or spikes, away from the cell body towards the axon terminals (Figure 1. 3). Neurons, in most cases, are polarized: their dendritic ends receive synaptic input and their axon ends produce output through synapses (Figure 1. 2) [4].

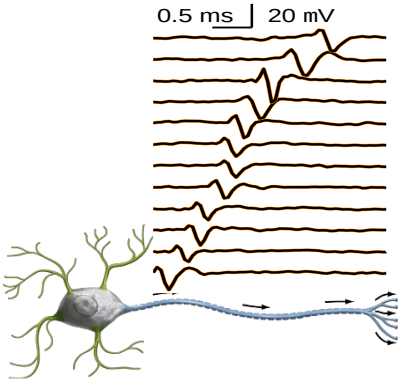

Figure 1. 3. Action potentials (spikes) are transmitted through axons [7]. In extracellular recordings, neural activity may be recorded from different sites along the axon, which may cause recording different spike amplitudes. [8].

1.2. Microelectrode arrays chips

Extracellular recordings can be used to determine the electrical activity of cultured electrogenic cells (like neurons, heart cells, retina cells, or muscle cells), for instance, through external microtransducers [9], [10], [11]. For extracellular recordings, the cells are cultured or placed directly on top of the sensors or electrodes (Figure 1. 4). Ions flow across a cell membrane in milliseconds when electrical activity occurs. Ions in motion induce an electric field that affects the open-gate region of a field-effect transistor (FET) [12], [13], [14], or can be recorded by metal microelectrodes [15]. Recordings carried out extracellularly are noninvasive (no puncture of cell membrane occurring), allowing long-term measurements.

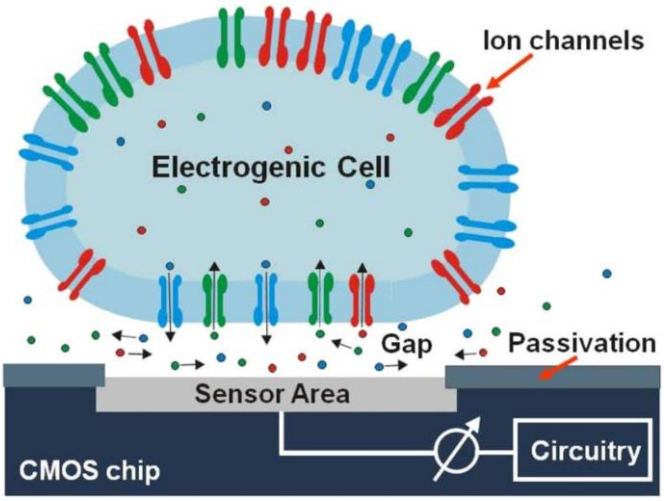

Figure 1. 4. An electrogenic cell is attached to a sensor surface. Cells with ion channels are placed on a microsensor (an open-gate transistor or electrode). Microsensors record the electric field or voltage generated by ions moving near electrodes [6].

The mechanisms of the brain or the cellular responses upon dosing biologically active agents can be elucidated by studying neuronal information processing using substrate-integrated MEAs [16], [17]. Comparing electrogenic cells *in vitro* with cells *in vivo* or in intact organisms provides different experimental conditions: in intact organisms or animals, there are typically a variety of different cell types, while in a culture there can be one specific cell type or an assembly of several different types. Furthermore, experimental parameters, such as the temperature or concentration of a chemical compound, can be more precisely controlled in cell cultures than in living organisms. Nevertheless, inferences from *in vitro* experiments to *in vivo* cell behavior should be experimentally verified. The investigation of acute or organotypic slices, such as brain and other tissue slices, can provide some insight

into the difference between experiments conducted *in vitro* and those conducted *in vivo* [18], [19].

On a single chip, complementary metal-oxide-semiconductor integrated circuits (CMOS) can integrate active microarrays for recording and stimulating electrogenic cells *in vitro*. An active array consists of circuitry components such as amplifiers and filters that are integrated together with the electrodes and the digital core (Figure 1. 5). This application-specific integrated circuit (ASIC) will be focused on *in vitro* applications so that needle arrays carrying electrodes can be utilized [6].

An integrated circuit or CMOS system has three primary advantages, including 1) connectivity; the structure allows a large number of transducers or electrodes to be addressed by on-chip multiplexing architectures; then 2) signal quality; the signal is conditioned right at the electrode by means of dedicated circuitry units (filters, amplifiers); and, finally, 3) straightforward handling and use; robust devices and signals (no Faraday cages, digital signals); various functions can be programmed or automated via user-friendly software and digital interfaces that directly address digital registers and logic or memory units on the chip side. Automation includes the self-identification of the chip, storing calibration parameters, and performing self-test functions. The presence of user-friendly features is an essential aspect to encourage neuroscientists to adopt such systems.

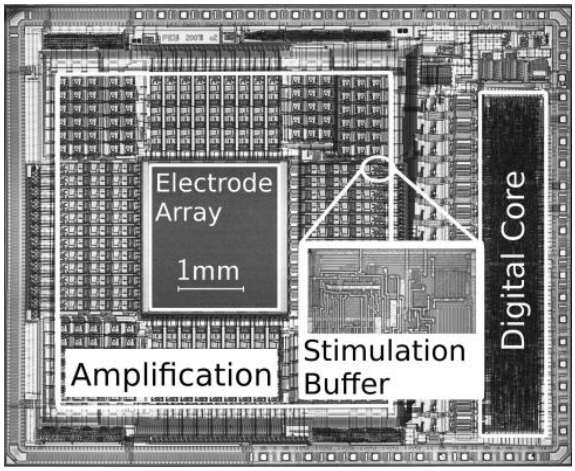

Figure 1. 5. ASIC for neuron signals stimulating and recording [20]. Electrode arrays, recording amplifiers, stimulation buffers, and digital core are integrated into a single CMOS chip.

1.3. Stimulation pulse and its artifacts

The use of electrical stimulation has become an effective tool for the localization of brain activity. Through non-invasive stimulation methods such as transcranial magnetic stimulation and transcranial alternating current stimulation, large-scale network dynamics can be modulated to control behavior [21], [22]. Additionally, both deep brain stimulation (DBS) and direct cortical stimulation (DCS) are invasive techniques that can be used for treating neurological and psychiatric disorders [23], mapping cortical function [24], [25], [26], or modulating memory [27]. Typically, these studies have examined the impact of stimulation on behavior without providing much insight into the effects of stimulation on ongoing brain activity. The impact of stimulation on neuron cells is typically measured via electroencephalography (EEG), magnetoencephalography (MEG), or invasive electroencephalography (iEEG). The electric field and the recording system interact during stimulation, resulting in high amplitude stimulation artifacts. These artifacts obscure the endogenous activity. In the frequency domain, stimulation artifacts are reflected, resulting in a structured spikey pattern when the stimulation follows a periodic pattern (Figure 1. 6). Since the majority of analyses of brain activity occur in the frequency domain, the presence of artifacts invalidates the analysis of stimulation effects on oscillations. Thus, removing these artifacts would provide us with insights into how electrical stimulation interacts with neural activity, and how neural activity interacts with behavior [28].

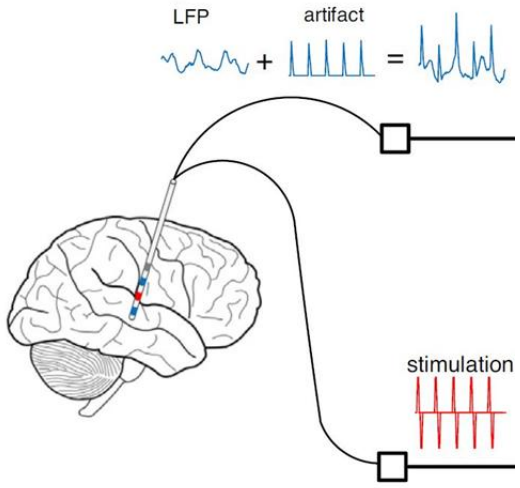

Figure 1. 6. Stimulation artifacts contaminate the recorded signal and prevent robust biomarker detection [29].

1.4. Motivation

The proposed microelectrode array (MEA) chip is composed of microelectrodes, analog components, and a digital core. In the analog part, a variety of functionalities can be implemented, including voltage and current sensing, impedance measurement, stimulation, etc. Digital core modules fall into two categories: on-chip digital controller and digital interface to off-chip PCB. The first part of the project involved designing and implementing the digital core in 180 nm CMOS technology. The work was carried out at the ETH Zurich, Switzerland.

The analog stimulation block generates stimulation pulses that are used to stimulate electrogenic cells, cultured on top of MEA. In order to recover the spikes that occur during stimulation, real-time post-digital signal processing has to be applied. Using this algorithm, recording artifacts will be detected and removed from signals. In the second part of this project, the real-time artifact removal algorithm is implemented on Xilinx Kintex-7 FPGA KC705 Evaluation Kit, by implementing principal component analysis. The work was performed at Imec in Belgium.

2 Design and Synthesize of Digital Circuit for Microelectrode Arrays in 180nm CMOS Technology

2.1. Introduction

In the introduction chapter, we mentioned that an IC is required to record neuron cell signals. The designed IC consists of an array of 50,000 micro-electrodes that are able to detect these kinds of signals. These microelectrode arrays (MEAs) detect extracellular activity signals of neuron cells. Analog circuitry in this IC, including filters, amplifiers, and analog-to-digital converters, also plays a key role. The filters are intended to eliminate out-of-band frequency noise. The operating frequency of these filters can be configured. Amplification of the detected signals is then performed using the amplifier where the gain of the amplifier can be controlled according to input range. Following that, analog-to-digital signal converter circuits are used to convert these recorded analog signals to digital signals. There are 1024 channels for recording neuron cell signals in this IC, which means 1024 filter, amplifier, and ADC units. A variety of options are typically considered among analog functionalities, including voltage sensing, current sensing, impedance measurement, stimulation pulse generation, etc. The final on-chip section is the digital circuitry. From a digital perspective, analog circuits are the register memories that can be altered to determine the desired filter frequency or gain of amplifiers. As a final step, recorded digitized signals are transmitted to the off-chip PCB. In Figure 2. 1, the block diagram of this IC is shown.

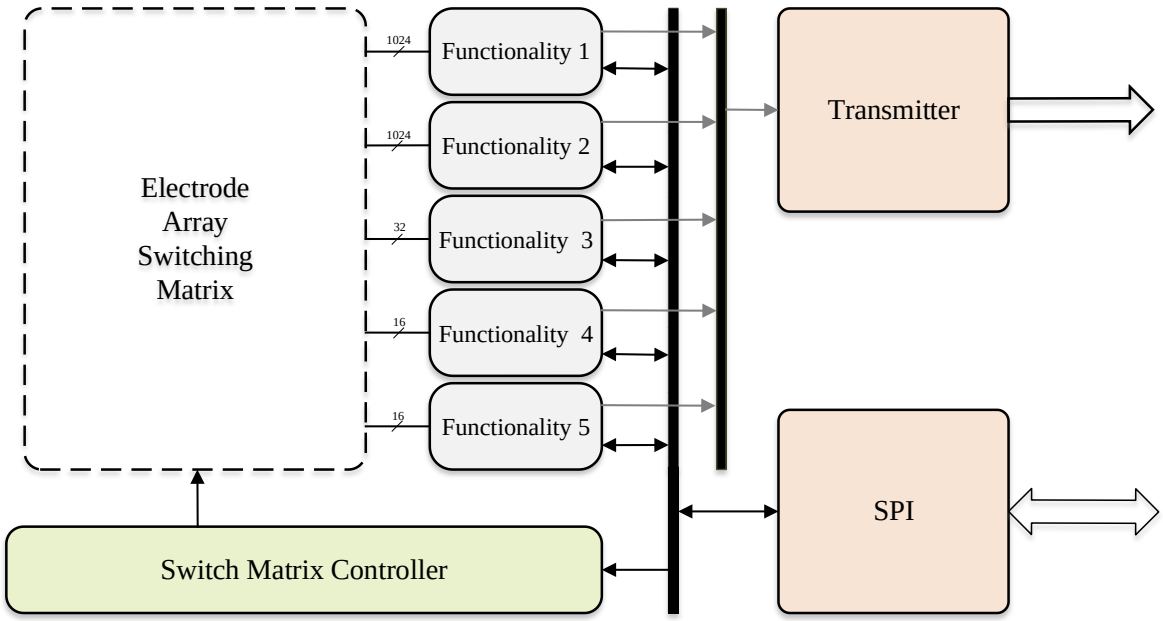

Figure 2. 1. Designed MEA IC block diagram. Configuration data enters through SPI, and recorded data is transmitted through the transmitter block. On-chip analog functions are considered register memories from digital view.

2.2. Previous related work

Over the last few years, several CMOS MEAs have been developed. There is an evolution toward increasing the number of electrodes, number of channels and increasing the versatility, moving towards more modern technology.

A high-density CMOS-based MEA featuring 11,011 metal electrodes and 126 channels, each of which comprises recording and stimulation electronics, for extracellular bidirectional communication with electrogenic cells, was designed and developed [20].

In [30], A 1024-channel CMOS microelectrode array with 26,400 electrodes was developed for recording and stimulating electrogenic cells *in vitro*. Figure 2. 2 shows the fabricated IC.

Figure 2. 2. Microelectrode array packaged IC [30]. On the left side of the chip, power and digital interfaces are visible. Neurons can be cultured on top of the fabricated IC.

A microelectrode array featuring 59,760 electrodes with 2048 channels was developed for recording the extracellular neuron activity [31].

2.3. Digital Core Design

The digital core can be divided into three sub-sections. Serial peripheral interface (SPI) for receiving configuration data, data interface for transmitting the recorded digitized signal to the off-chip PCB, and register memories for configuring analog components. According to Figure 2. 3, Each subsection follows an identical design flow with four main stages.

Step 1. Digital circuit module design at the register transfer level (RTL): Each of these digital circuit modules is designed and simulated at the RTL. This step is accomplished by developing a design file and a test bench file for simulation in Modelsim. As a result of this step, the logical point of that module is verified.

Step 2. Module design at gate level: The designed file is then converted to netlists by the Design Compiler tools. It produces a time constraint file and gate-level netlist. Several reports will be generated, including design area reports, timing reports, and reports regarding resource utilization. Synopsys Design Constraints (SDC) is another file generated by this tool. It is used in the next step. An example Tool Command Language (TCL) file used for this project can be found in appendix A.

Step 3. Layout level design: The final layout is created using the Innovus SoC Encounter tools. This stage involves importing 180nm technology library files. Then the input and output pins for each digital block are determined. This step is also known as the I/O pin configuration. Floor Planning is the next stage, which is the area considered for a specific block. The next step is power planning and routing. Each block's power path (VDD and GND) is explicitly tailored by adding power rings and power stripes. Next, the library gates will be placed. The clock tree is synthesized after the gates are placed. In a design, the clock signal is a critical signal. The arrival of this signal in different parts of the IC imposes restrictions that must be taken into consideration at this point. After the clock tree has been synthesized, the rest of the signals must be routed. This is the final step of the design process. Now it's time to verify the design and check for any violations. The final layout and SDF file are then created.

Step 4. Digital core integration with analog circuits and microelectrode arrays: We can integrate the digital core with analog circuits using the Cadence tool. The final file can be designed to fabricate the IC by using this tool.

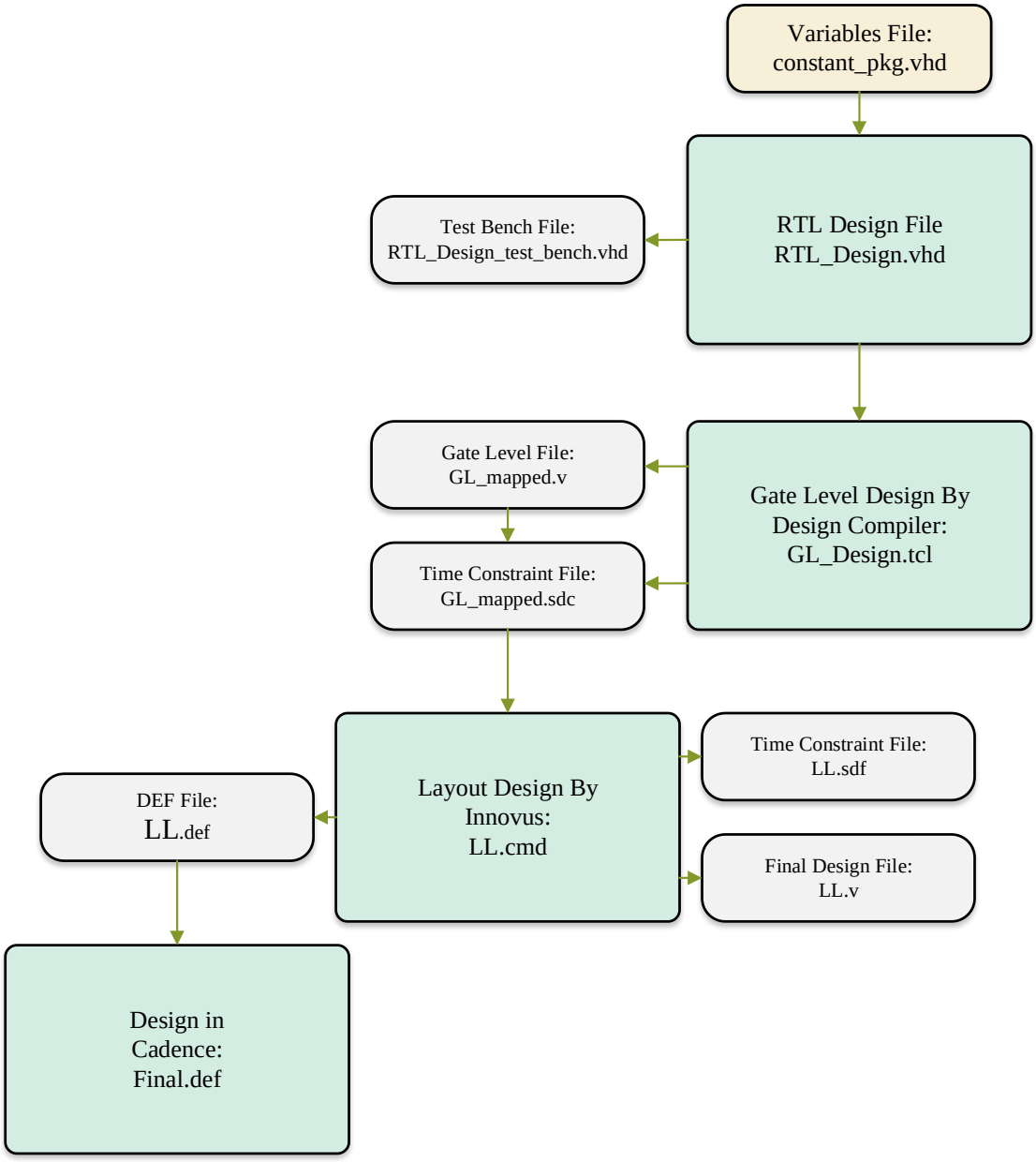

Figure 2. 3. The design flow for an ASIC's digital core involves RTL design, GL design, layout design, and finally, integration with microelectrodes and analog blocks.

2.3.1. Serial Peripheral Interface (SPI)

Five single-bit signals are present on this interface. General *spi_clk* is a clock signal, *spi_rst* is the reset signal, and *ssel* signal for selecting and activating the IC when more than one IC is connected to the main system. The *mosi* (Master Output Slave Input) signal for receiving bit-by-bit command code and the *miso* (Master Input Slave Output) signal, which is the output signal from the IC, indicating that the protocol is bi-directional. Using *miso* signal, each analog block's register memory will be checked to determine if its frequency or gain is at the desired value. The internal ports of this block are the address port *addr* to specify the register's address, the output data port *dout*, which contains the transmitted data. For read and write mode in the register memories, the single-bit signals *rd* and *wrt* are used, respectively. The *din* signal is used to transfer data from the memory to the off-chip PCB, using the *miso* port to check the register values (Figure 2. 4).

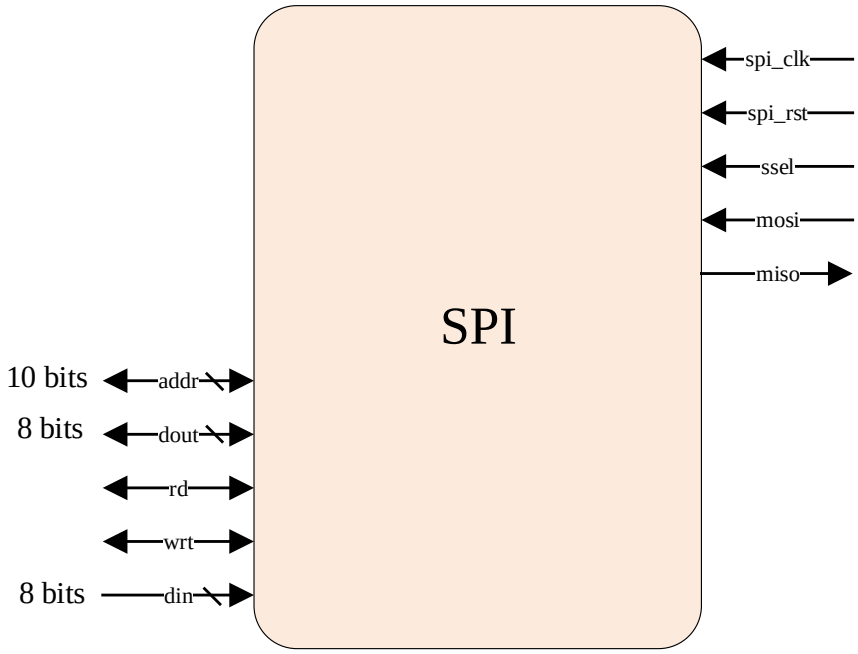

Figure 2. 4. SPI block diagram. The interfaces to the off-chip world can be seen on the right. The internal signals are shown on the left.

2.3.1.1. SPI Functionality

This interface works by entering the input bits of a *mosi* signal one by one into a 12-bit input internal register inside this module (Figure 2. 5). Upon receiving all bits of this internal input register, the last two bits determine the type of operation for this controller according to **TABLE 2.1**. If both bits are zero (00), the first 8 bits of the internal input register receive the received data, which must be in the previously

sent address without changing it. When bits 01 are sent, the first ten bits of the register indicate the address of the memory where the data is going to be stored. If bits 10 are sent, the first eight bits are considered as data and an increment in the value of the address. This auto-increment prevents sending addressing at any time when memory cells are stacked in a row. Lastly, code 11 is used to take the data from an address, which is inserted into an 8-bit register(Figure 2. 6). In each of these cases, the data relate to values that control and configure analog parts.

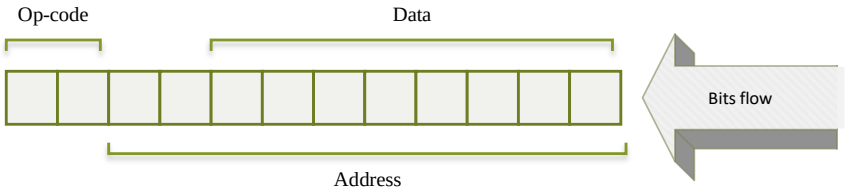

Figure 2. 5. 12 bits internal input SPI register. Depending on the operation requested, the first two bits represent the requested operation, while the remaining bits represent data or address.

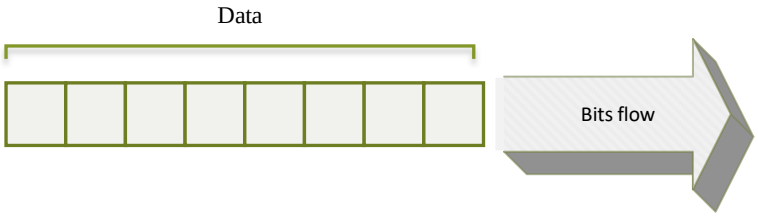

Figure 2. 6. 8 bits internal output SPI register.

TABLE 2.1: SPI op-code is determined by the first two bits the of SPI internal register.

Mode	**Op-Code**
WRITE DATA WITHOUT INCREMENTING ADDRESS	00
WRITE ADDRESS	01
WRITE DATA AND INCREMENT ADDRESS	10
READ ADDRESS	11

The next bits are then streamed and specify the next commands.

2.3.1.2. Register Transfer Level (RTL) Design

This interface protocol was developed at the RTL level in VHDL, and simulated in the Modelsim tools.

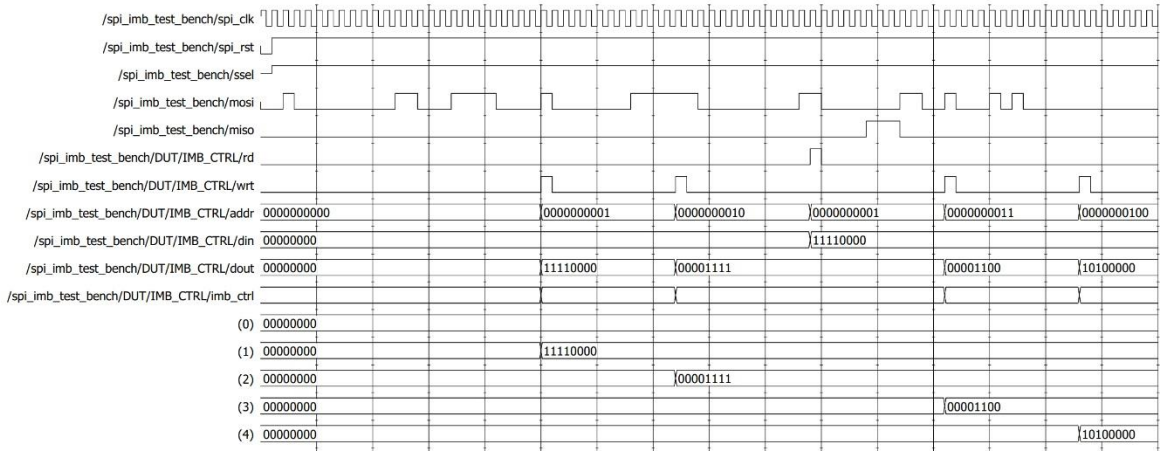

Figure 2. 7. SPI simulation waveform result obtained from Modelsim tools. SPI off-chip interface and internal signals list are shown. The read/write memory with initial content starts receiving data through SPI.

As can be seen in Figure 2. 7, the address bits which correspond to a specified memory are sent one by one through the *mosi* signal. Then, through the same signal, the data related to that address of memory is sent one by one and the *wrt* signal is activated to write in the memory. After writing some data, the operation of reading data in memory is performed and the *rd* signal is activated. And the existing bits are transmitted off-chip via the *miso* signal.

2.3.1.3. Gate Level Design

After RTL-level design and simulation and verification in the Modelsim tools, the design should be converted to netlists in 180nm technology. The Design Compiler tool is used to convert the designed circuit to standard cells.

2.3.1.4. Layout Level Design

As described above, all steps are performed and the desired IC is generated. The SPI interface can be seen in Figure 2. 8. The Interface pins with the off-chip PCB are marked on the left and the internal signals exist on the right.

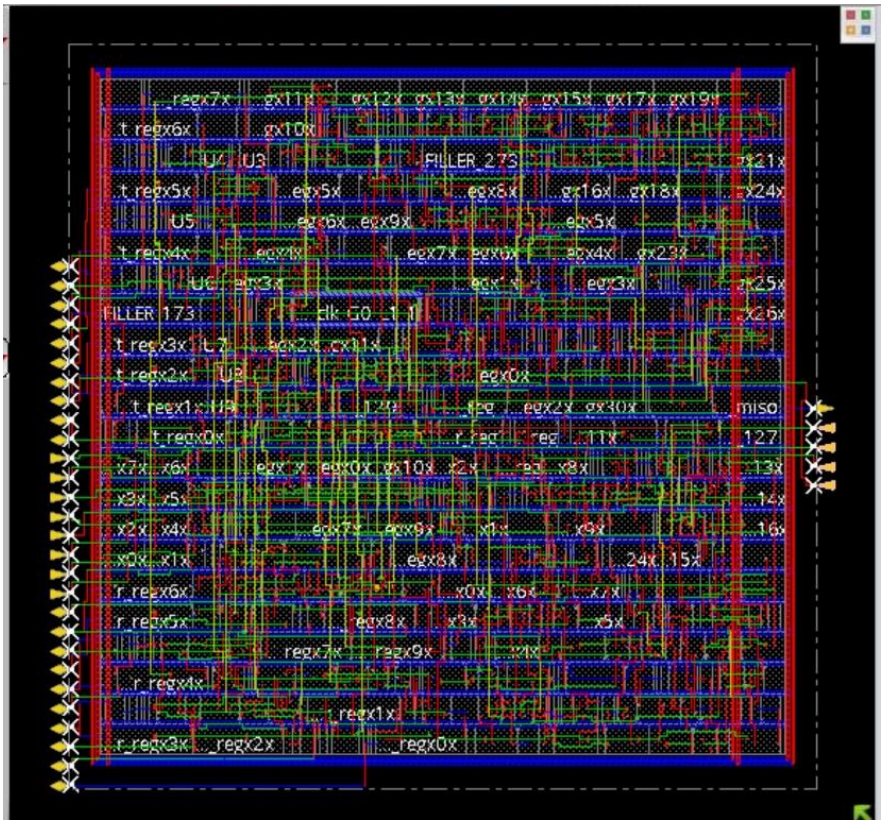

Figure 2. 8. Final layout for SPI. off-chip I/O pins are located in the right and internal signals are shown in the left side of block.

2.3.2. Transmitter Interface of Recorded Data

This module of the digital circuit is used to transmit recorded data to the outside world. Single-bit input signals *tx_clk*, *tx_rst*, and *tx_enbl* are used as a clock, reset, and enabling this section, respectively. The single-bit output signal *tx_frm_sync* is used to display the first word of the transmitted data frame as a synchronous bit. The ten-bit port *tx_data_out* is the output bits of the recorded data. These ports are interface ports to the off-chip PCB. Four 10-bit internal ports *data_bus* are used to receive signal data from analog components. There is also an 11-bit signal counter to indicate which analog block is currently sending the data (Figure 2. 9).

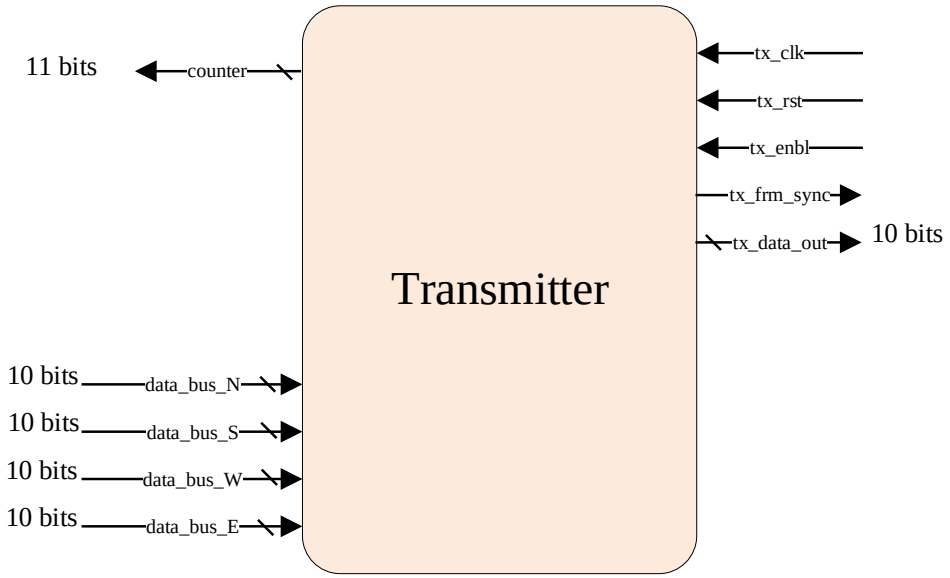

Figure 2. 9. Diagram block of the transmitter module. The interfaces to the off-chip world can be seen on the right. The internal signals are shown on the left.

2.3.2.1. Transmitter Functionality

This section is connected to different analog sections by 4 buses. **TABLE 2.2** summarizes the locations of the various analog components in the IC. For example, there are impedance measurement blocks in the western and eastern parts of the IC. When sending information from this section, even words from 50 to 81 are used to send data from the west and odd words from 50 to 81 are used to send data from the east. This data is placed in a frame similar to Figure 2. 10, in the form of ten-bit words. With the first word sent, the *tx_frm_sync* signal becomes one to indicate that the first word is being sent as a synchronous signal.

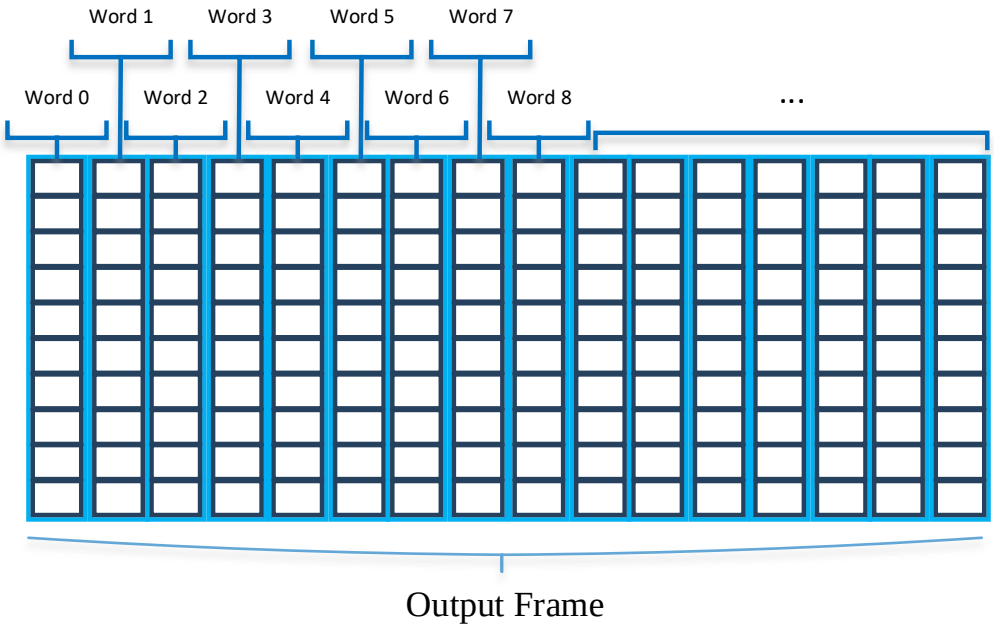

Figure 2. 10. Output data frame. Each word contains 10-bit recorded data.

TABLE 2.2: Analog block location and specification

Unit/Block	On-Chip Bus Location	Frame Number	Setting Frame Number	Data Frame Number
Impedance Measurement Block	West	Even Number	0 – 9	50 – 81
	East	Odd Number	(10)	(32)
Voltage Recording	North	Even Number	10 – 19	82 – 1105
	South	Odd Number	(10)	(1024)
Current Source	North	Even Number	20 – 29	-
	South	Odd Number	(10)	
Voltage Clamp Recording	West	Even Number	30 – 39	1106 – 1169
	East	Odd Number	(10)	(64)
Stimulation Block	West	Even Number	40 – 49	-
	East	Odd Number	(10)	

2.3.2.2. RTL level design

This communication protocol was first developed at the RTL level by Verilog and then VHDL. And implemented in the Modelsim tools environment for verification purpose (Figure 2. 11).

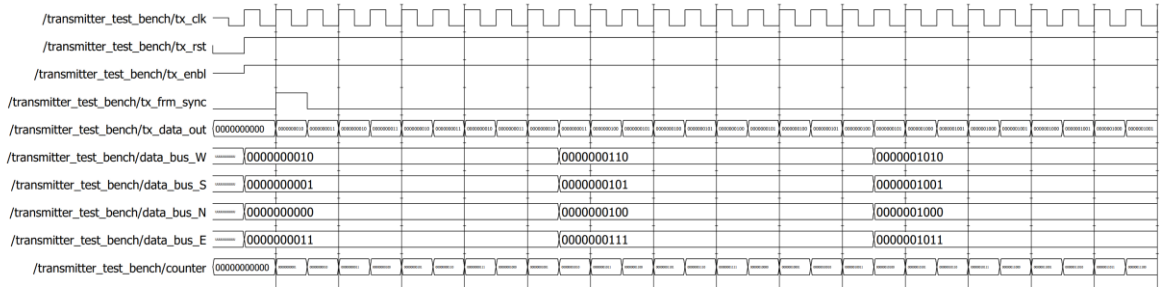

Figure 2. 11. Transmitter simulation result. The *tx_frm_sync* bit is activated when the first word is being transmitted.

As can be seen in the simulation, the *tx_frm_sync* bit is activated when the first word is being sent out of the IC. Then, example recorded data is transmitted out of the IC. During this period, the counter signal also changes to indicate the analog block of the current data.

2.3.2.3. Gate Level Design

After RTL-level design and simulation and verification in the Modelsim tools, the design should be converted to netlist in 180nm technology. The Design Compiler tools is used to convert the designed circuit to standard cells.

2.3.2.4. Layout Level Design

As described above, all steps are performed and the desired IC is generated. In Figure 2. 12, you can see the transmitter of the recorded data layout. The communication pins with the outside world of the IC are marked on the left and the internal signals are positioned on the right.

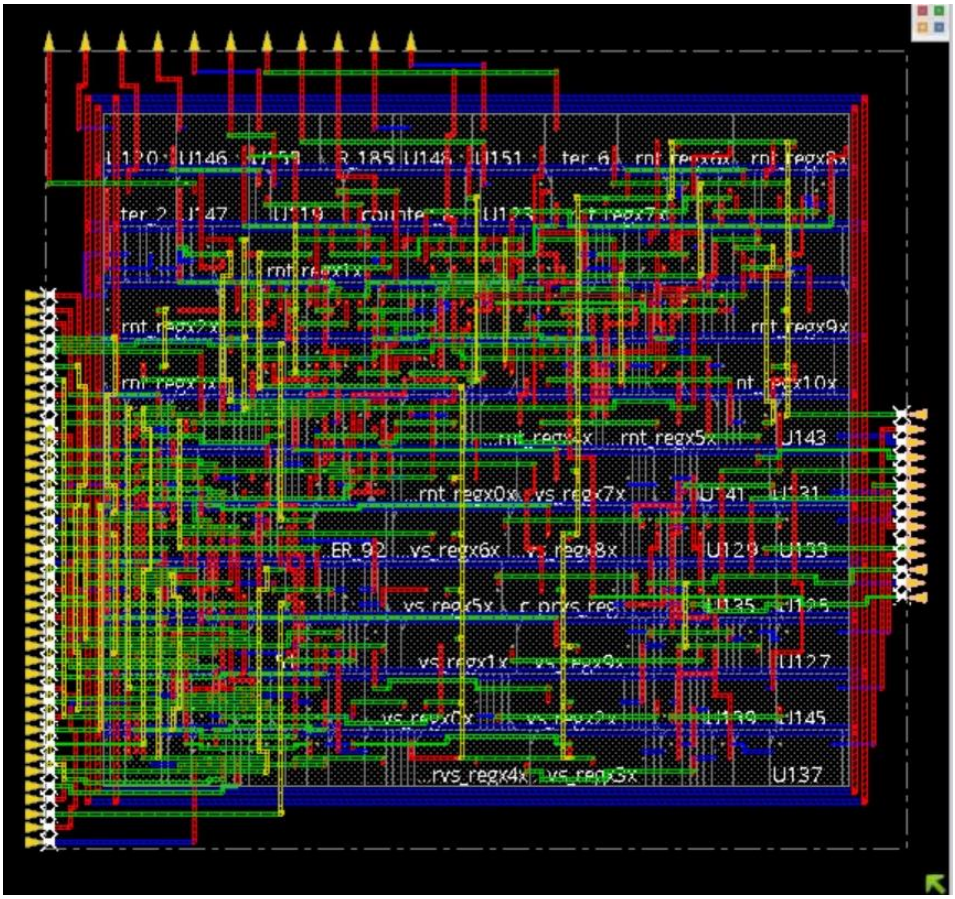

Figure 2. 12. Final layout of transmitter. The interfaces to the off-chip world can be seen on the right. The internal signals are shown on the left and top.

2.3.3. Register Memory

To the digital designer, an analog part is a register memory used to configure the analog part. By changing the data in each register, different values can be set for the operating frequency of the filter or the gain of amplifiers. This memory has 5 internal ports, all of which are connected to each other through a bus. Single-bit input signals *rd* and *wrt* are used to activate read mode and write mode in memory. The ten-bit *addr* port points to the address of the register which is being sent. The 8-bit *dout* ports are for input data from the bus, and the 8-bit *din* port is for reading data and transferring it through the bus (Figure 2. 13).

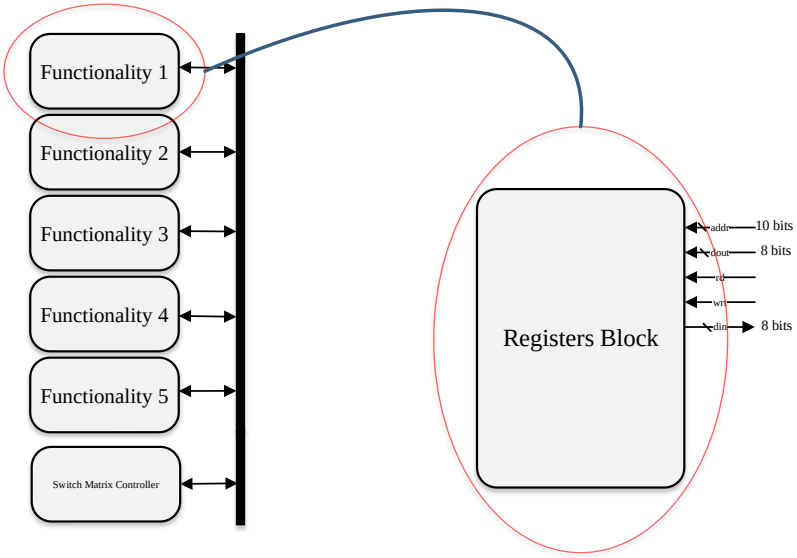

Figure 2. 13. Register memory diagram block. A register memory block can be considered for each analog function.

2.3.3.1. RTL level design

This register memory was first designed at the RTL level by Verilog and then VHDL. And implemented in the Modelsim tools environment. As seen in the SPI section, values were written and read to and from a register memory.

2.3.3.2. Gate Level Design

After RTL-level design and simulation and verification in the Modelsim tools, the design should be converted to netlist in 180nm technology. The Design Compiler tools is used to convert the designed circuit to standard cells.

2.3.3.3. Layout Level Design

As described above, all steps are performed and the desired IC is generated. In the Figure 2. 14 you can see a register memory with SPI interface.

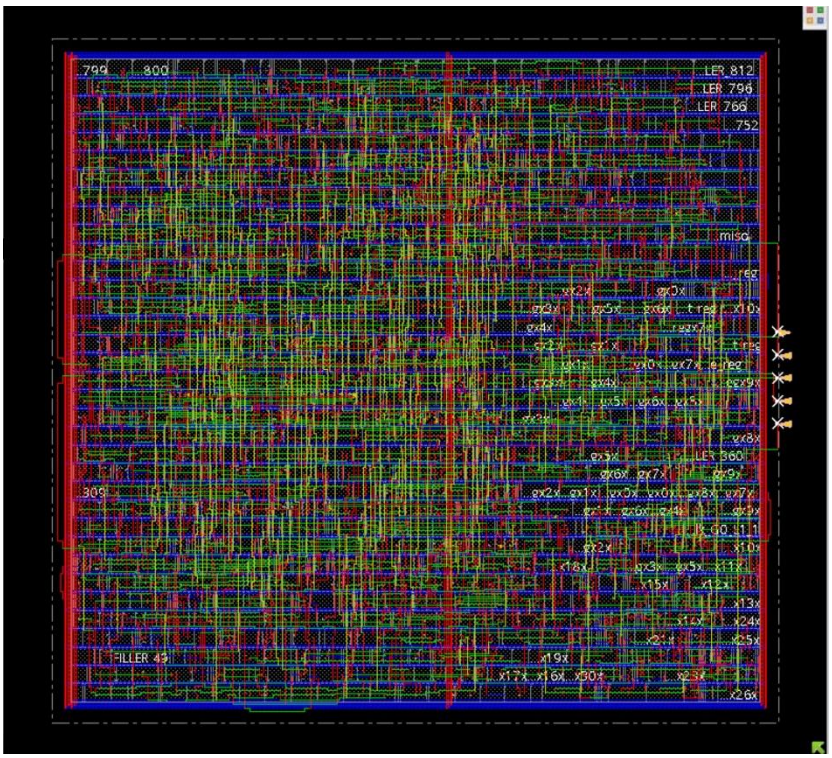

Figure 2. 14. Final layout of a register memory integrated with SPI

2.3.4. Digital Core

All the items designed above are integrated together and the digital core in this IC would be designed.

2.3.4.1. RTL level design

This digital control unit was first designed at the RTL level by Verilog and then VHDL. And implemented in the Modelsim tools environment (Figure 2. 15).

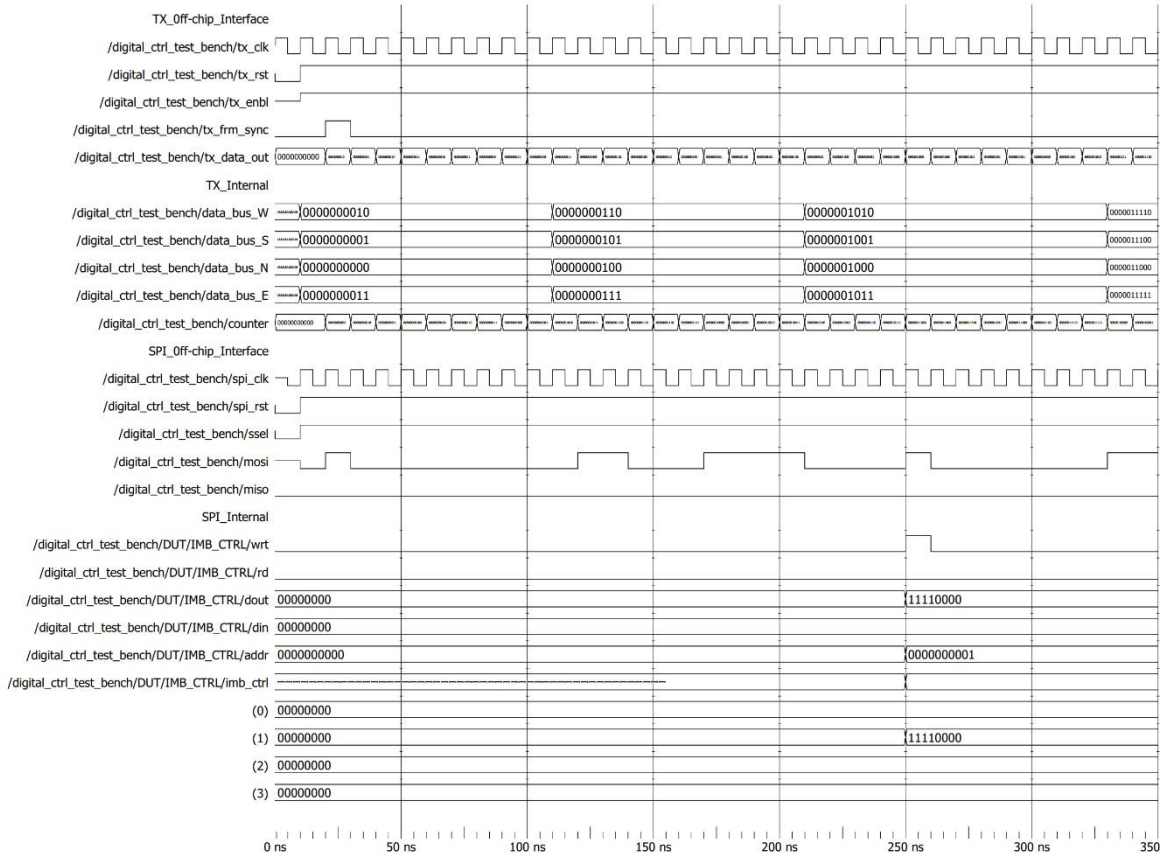

Figure 2. 15. Digital core simulation result. The transmitter and SPI off-chip ports, as well as internal ports, are grouped for ease of reading.

2.3.4.2. Gate Level Design

After RTL-level design and simulation and Verification in the Modelsim tools, the design should be converted to netlist in 180nm technology. The Design Compiler tools is used to convert the designed circuit to standard cells (Figure 2. 16).

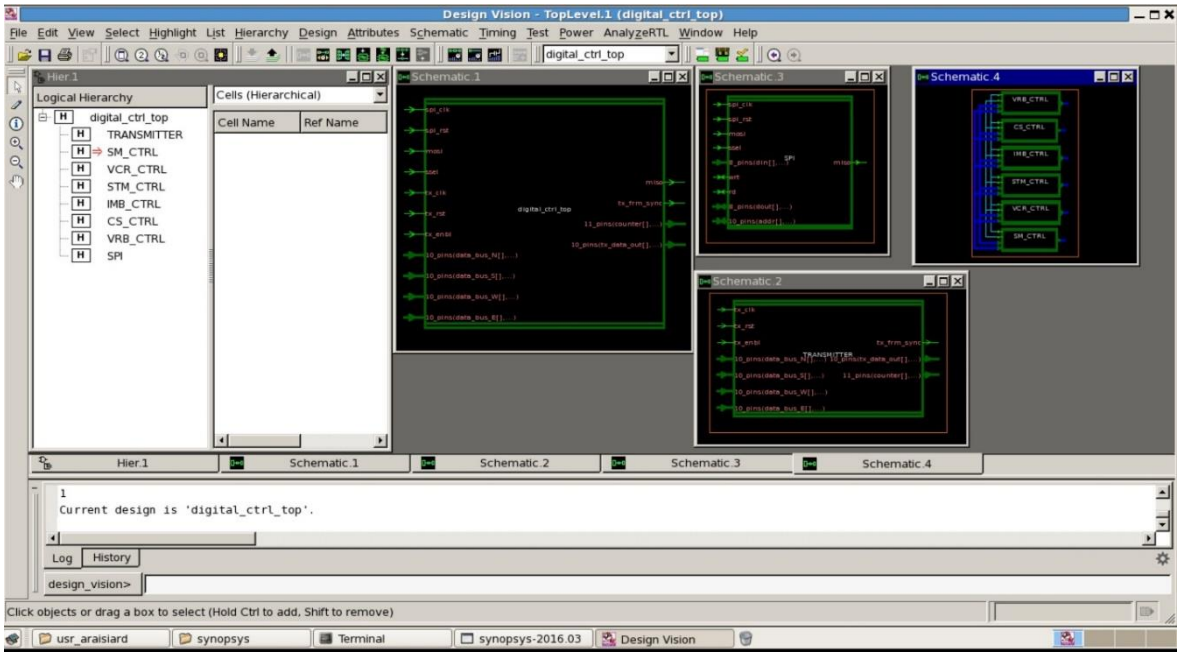

Figure 2. 16. Digital controller netlist of all blocks. Different sub-modules are shown in the separate window.

2.3.4.3. Layout Level Design

As described in the introduction, all steps are performed and the desired IC is generated. In Figure 2. 17, you can see the digital control unit.

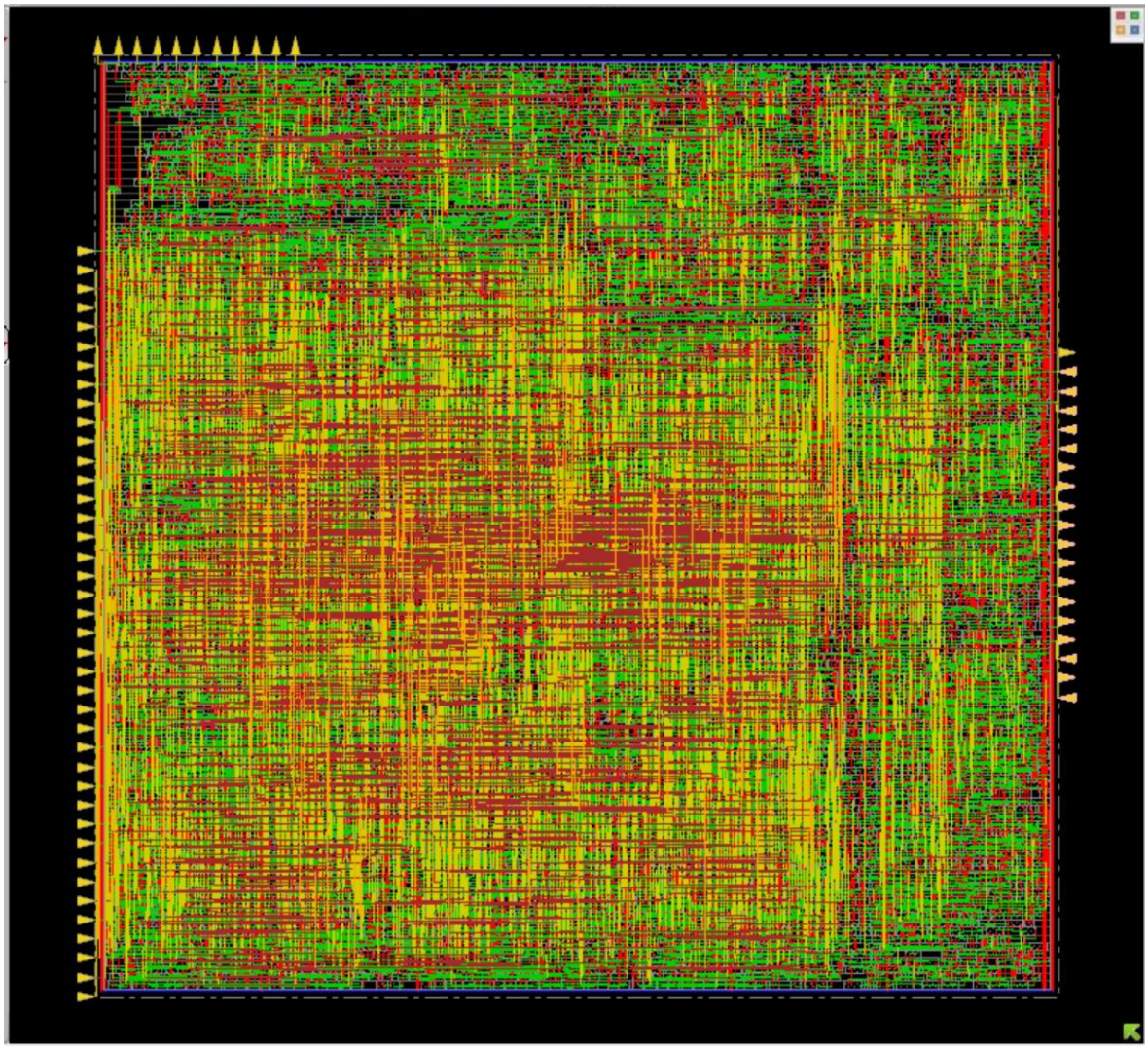

Figure 2. 17. Final layout of the digital controller. On the chip, internal signals are located on the left and top, while off-chip ports are located on the right.

2.4. Integration with analog parts to Fabricate Mixed-signal IC

In order to fabricate the final IC, all the designed components, including digital core, amplifiers, filters, analog-to-digital converters, must be integrated, which is done in the Cadence tools. In the introduction of this chapter, we mentioned that we use the final designed file in the Cadence tool to integrate digital core with other blocks. Figure 2. 18 shows the final design implemented in the Cadence tool.

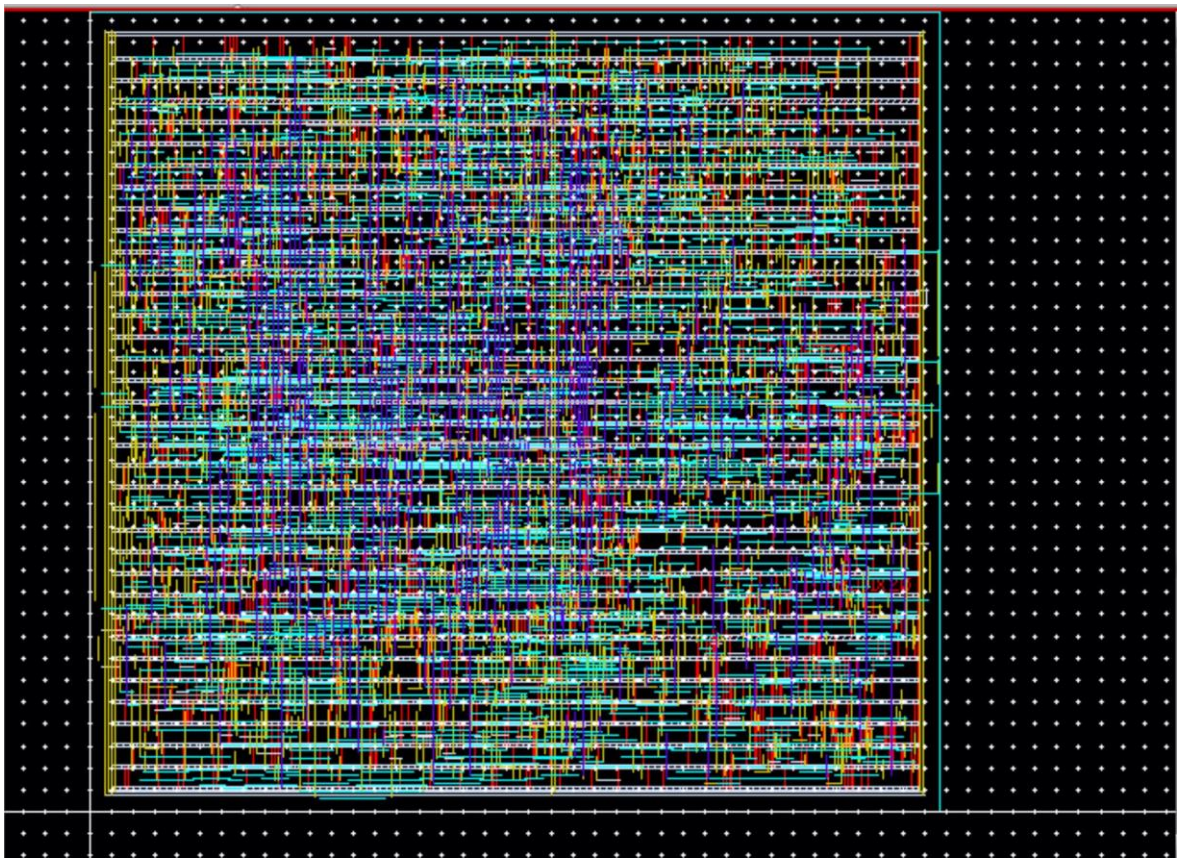

Figure 2. 18. The final layout of the digital controller in Cadence

j

2.5. Conclusion

For this part of the dissertation, a digital controller was designed in 180nm CMOS technology from RTL to Layout, using Modelsim, Design Compiler, and SoC Encounter. In order to achieve this goal, a register memory was designed. Then the SPI protocol and the transmitter interface were developed, and their functionalities were verified through Modelsim simulation tools. Finally, all the digital components were integrated. This IC is in the process of being fabricated and being used to record the extracellular activities of *in vitro* neuron cells.

3 Design and Implement Real-Time Stimulation Artifact Removal Algorithm

3.1. Introduction

As part of the recording phase, all signals are recorded, including spikes and stimulation pulses. Especially near the electrode where the stimulation pulse is applied, the spike signal is distorted due to the large amplitude of the stimulation pulse. As the distance between the recording electrode and the stimulation pulse source increases, this effect diminishes. In this section, we aim to develop a real-time algorithm that can eliminate the effect of stimulation pulses while simultaneously recording the data (Figure 3. 1).

Figure 3. 1. Algorithm functionality scheme. The algorithm receives contaminated signals and generates stimulation-artifact-free signals

The stimulation pulse can generally be removed by two methods [32].

1. Blanking: When stimulation is occurring, the signals are blanked, or the recording blocks are turned off.
2. Template Subtraction: A template format of the stimulation artifact is constructed and subtracted from the raw recorded signal. The advantage of this method is that it preserves spikes during stimulation. In this method, the template is usually constructed by averaging several stimulation pulses, which is a critical step. By finding the general template or shared structure among the channels, the template can be developed for all input channels and clear all channels from this artifact caused by the stimulation signal without losing the spike signal during the stimulation pulse.

The two methods, which have been described, can be implemented in two ways

Online method: Removal of stimulation artifacts requires special hardware. Despite its effectiveness, this method is expensive and challenging to develop, especially when large numbers of recorded signals are present. In addition, it usually requires constant stimulation pulses over time to function well.

Offline method: Only recording raw signals require electronic hardware. Nevertheless, no special hardware is required to remove the artifact generated by the stimulation pulse.

A comparison of all methods, in terms of design complexity and ability to recover spike during stimulation period, is shown in TABLE 3. 1**.**

TABLE 3. 1. Compare the advantages and disadvantages of different methods

	Design Complexity	**Ability to recover spike simultaneously with the stimulation pulse**
Offline Blanking	The simplest	No
Online Blanking	simple	No
Offline Template Subtraction	Complex	Yes
Online Template Subtraction	The most complex	Yes

3.2. Previous related work

As described in [33], the online blanking method is implemented entirely in analog. An artifact-elimination circuit that returns the stimulation electrode to its initial voltage following stimulation. This minimizes interference with recording. In 16 channels, it starts recording after a maximum of 2ms, so it is not possible to record the spike during the stimulation pulse.

A similar situation occurs in [7] for all 2000 recording channels, i.e. there was no recording during the stimulation pulse event.

As part of Stanislav's work [34], which is based on template subtraction, a general template is first designed to evaluate and then subtracted from the signal. This design requires constant time-varying stimulation pulses at each evaluation and only works on one channel.

There are limitations and drawbacks to the online methods mentioned above. A spike can only be recovered after the stimulation pulse, and it cannot be recovered simultaneously with the stimulation pulse. Those methods are only applicable to a single channel.

The algorithm proposed by [35], addresses both of these limitations. A limitation of this approach is that obtaining a spike signal simultaneously with a stimulation pulse requires having an electrical image of the neuron.

3.3. Stimulation Artifact Removal Algorithm

The goal is to create and implement an online algorithm that will be able to recover spikes simultaneously with stimulation pulses. In order to achieve this, we can exploit the similarity and shared structure between stimulation pulses recorded by different recording electrodes (different channels). For all channels, the stimulation pulses arrive almost at the same time. According to this algorithm, the number of stimulation pulses is not specified, so whatever the number is, any artifacts on the recorded data must be eliminated [36].

As shown in Figure 3. 2. spikes affect and can be recorded for a single channel and the adjacent channels, while stimulation pulses affect all channels. Therefore, in order to identify the shared structure of stimulation pulses for a specific channel, the algorithm neglects that specific channel and its neighbors. By subtracting the shared structure from that channel, the spikes remain and can be retrieved. The procedure is applied to every single channel separately.

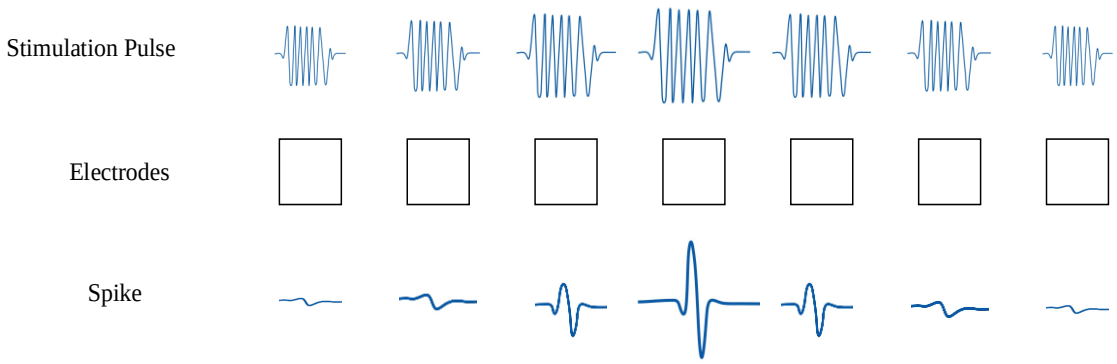

Figure 3. 2. Spikes and stimulation pulses on recording electrodes.

Figure 3. 3 shows the effect of the stimulation pulse, which has less impact on the recorded data as it moves away from the stimulation pulse source. To plot Figure 3. 3, A curve fitting, power model is used.

$$Y = ax^b + c \quad (2.\ 1)$$

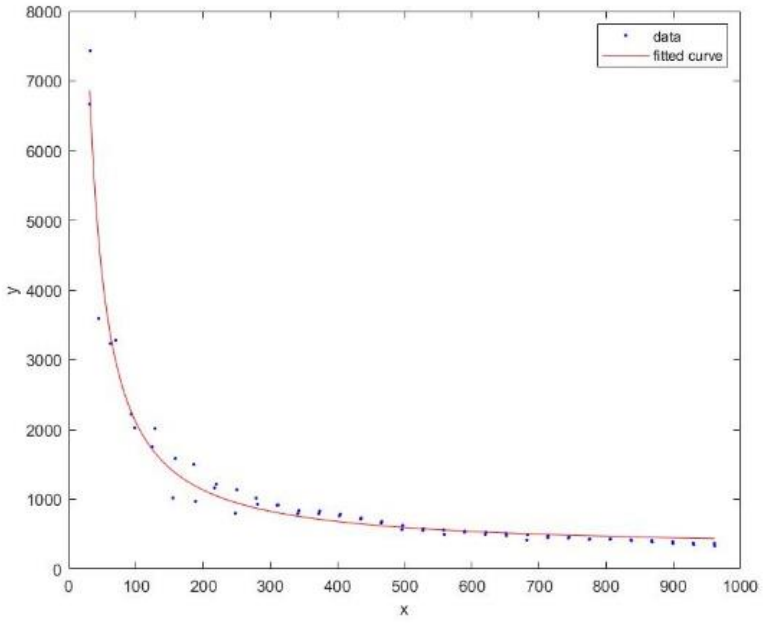

Figure 3. 3. Stimulation pulse power model curve fitting for distance relation

This online algorithm can only be implemented if the algorithm's processing time is less than the interval time it takes for the sample to be stored in memory, so the input data does not overflow. As a result, input data does not exceed the available memory on the FPGA chip.

Since only a limited amount of memory is available on the FPGA chip, a careful selection of samples needs to be made. Besides memory, other resources should not be utilized beyond their availability. Using the designed algorithm, ten channels are processed simultaneously at a sampling rate of 30 kbps. Processes up to 145 samples at a time and then the next 145 enter the processing unit. The processing time should not exceed the data interval time, which is:

$$\frac{samples}{sample\ rate} = \frac{145}{30000} = 4.834\ ms \qquad (2.\ 2)$$

This part of the signal is fed into the algorithm where the stimulation pulses are eliminated and the spikes preserved. As a side note, the object channel and its adjacent channels are not used to calculate the shared structure. This way, if there is a spike in the object channel, it can be recovered. After determining the shared structure, similar to creating a template, this template is removed from that object channel (Figure 3. 4). As a result, the mentioned operation must be carried out independently for each channel, which can be done in parallel. While parallelism can reduce processing time, it requires more resources. This shared structure is created using a machine learning algorithm known as principal component analysis (PCA) [36]. As input data for this algorithm, we select two channels after the adjacent channels. These two channels are used to calculate the shared structure for the object channel.

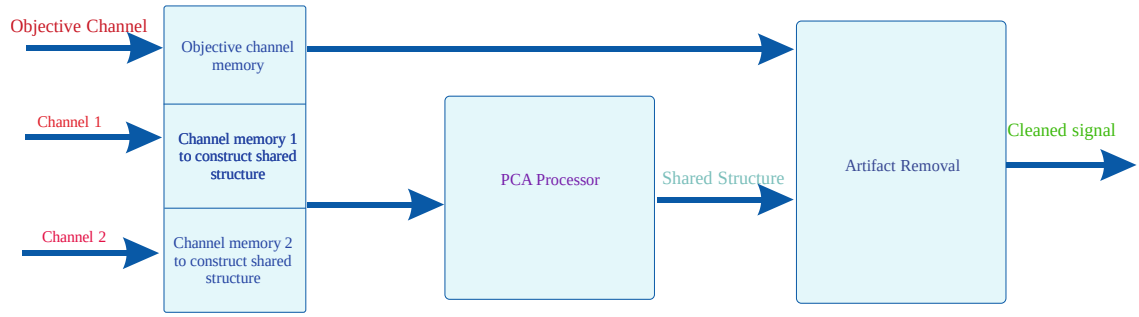

Figure 3. 4. Block diagram of the proposed algorithm

3.3.1. Creating Shared Structure by PCA

A processing unit is used to design the shared structure. The calculations in this processing unit are based on Single Value Decomposition (SVD) and Least Squares Method (LSQR).

3.3.1.1. Singular Value Decomposition (SVD)

PCA analysis involves the computation of eigenvectors and eigenvalues, which are the most challenging parts. Since the input data is a rectangular matrix of 145 by 2, Singular Value Decomposition is used to calculate the eigenvalues and eigenvectors [37].

$$SVD(A) = U\Sigma V^T \quad (2.\ 3)$$

The equation (2. 3) means that each vector can be decomposed by multiplying three matrices (Figure 3. 5). The calculated σ matrix is a matrix of eigenvalues used to reduce the dimensions of the data. And the matrix U is the same as the eigenvector matrix. The output we consider for this function is two matrices U and Σ. Essentially, this is the part of the algorithm that requires mathematical calculations.

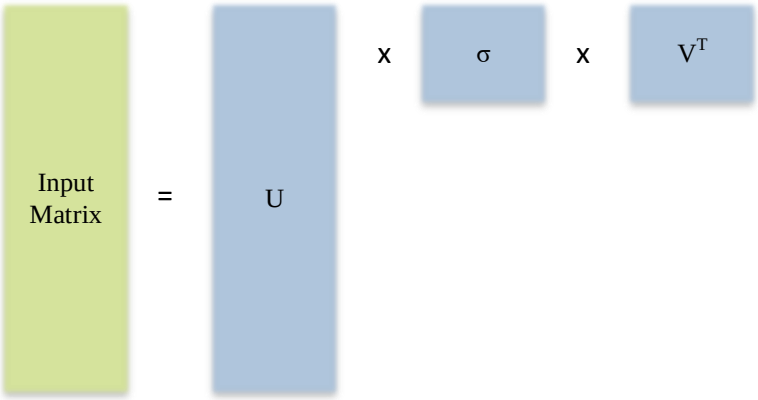

Figure 3. 5. SVD scheme. An input matrix can be decomposed into three matrix

We first use the following equation to decompose each matrix into its SVD values:

$$A^T A = V\Sigma^T \Sigma V^T \quad (2.\ 4)$$

Where Σ is the same as the eigenvalue matrix and V and U are the right eigenvector matrix and the left eigenvector matrix, respectively. A characteristic of the U matrix is that it is an orthonormal matrix, i. e. $U^T.U = I$.

Assume that the matrix A is decomposed into its $U,\ \Sigma,\ V$ components. So we have:

$$A^T A = \ (U\Sigma V^T)^T\ U\Sigma V^T = (V\Sigma^T U^T)\ U\Sigma V^T \quad (2.\ 5)$$

By multiplying the data matrix by its transpose matrix a 2-by-2 matrix is created.

$$Since\ U^T.U = I \ \Rightarrow\ A^TA = V\Sigma^T\Sigma V^T \quad (2.\ 6)$$

To decompose the input matrix, we first compute the matrix of eigenvalues(σ). For this purpose, we perform the following calculation, in which a specific value of λ is calculated for each row.

$$\det|A^TA - \lambda I| = 0 \quad (2.\ 7)$$

Matrix I is the identity matrix, i. e. its diagonal values are one and the other matrix elements are zero. The above value is a quadratic equation, for which, according to its degree, two answers are obtained.

After calculating the roots of the above equation, the eigenvalues(σ), which form the diagonal of the matrix Σ, can be calculated as follows. The other matrix elements of the matrix Σ are zero.

$$\Sigma: \sigma_i^2 = \lambda_i \quad (2.\ 8)$$

Where: $\sigma_1 \geq \sigma_2 \geq \sigma_3 \geq 0$

In this way, the matrix of eigenvalues Σ is calculated and ordered.

To calculate the V matrix, the following equation (2. 10) is used:

$$(A^TA - \lambda_i I) * V = 0 \quad (2.\ 9)$$

Since we have calculated λ_i in previous step, now the only variables are V_i ,and can be calculated.

Finally, from the matrices V and Σ, the matrix U is calculated using the equation (2. 10).

$$AV = U\Sigma \tag{2. 10}$$

We rewrite the data along the axes of the principal components. Each variable in the data is called a dimension or feature. And we are looking for the most effective components, which exists as a shared structure in all data and is caused by the stimulation pulse. In this step we calculated the decomposed matrices. So the values are specified.

$$SVD(A) = U\Sigma V^T = \sigma_1 u_1 v_1^T + \sigma_2 u_2 v_2^T + \sigma_3 u_3 v_3^T \tag{2. 11}$$

Each of these components, $\sigma_i u_i v_i^T$, is a matrix, and due to the order in the eigenvalue matrix, these components are arranged in order. This means that the first component has the greatest impact on the data, which can be used to reconstruct a shared structure in signals. This shred structure is the stimulation pulse in data. With the first two principal components, a shared structure can be created. For this reason, to create this input matrix, we use the data of the first two channels after the adjacent channels.

3.3.1.2. Least Square Method (LSQR)

After calculation of SVD is the part related to calculating the shared structure, which is done through the least square method. The least squares method is a statistical procedure to find the best fit for a set of data points by minimizing the sum of the offsets or residuals of points from the plotted curve. Least squares regression is used to predict the behavior of dependent variables [38], [39].

After calculation of LSQR, the shared structure is created and removed from the input data, to remove the artifact by stimulation pulse.

3.4. Real-time Algorithm Result

The hardware base algorithm was first designed and tested in MATLAB. Then it was synthesized through Vivado HLS tool using C ++ language and the output of high level synthesis was compared with the golden model created by MATLAB and the same result was achieved.

After implementing and synthesizing this algorithm on FPGA, ten channel data was given to the algorithm for one second and a clear signal was received without the artifact by the stimulation pulse, which indicates that this algorithm is working properly. Figure 3. 6 shows the primary recorded 145 data samples for nine channels. The stimulation pulses have a similar structure and effect across all recorded data, while the spike is recorded by channel number 7. Figure 3. 7 shows artifact-free data for all channels using the implemented PCA algorithm. The spike signal is recovered in channel number 7.

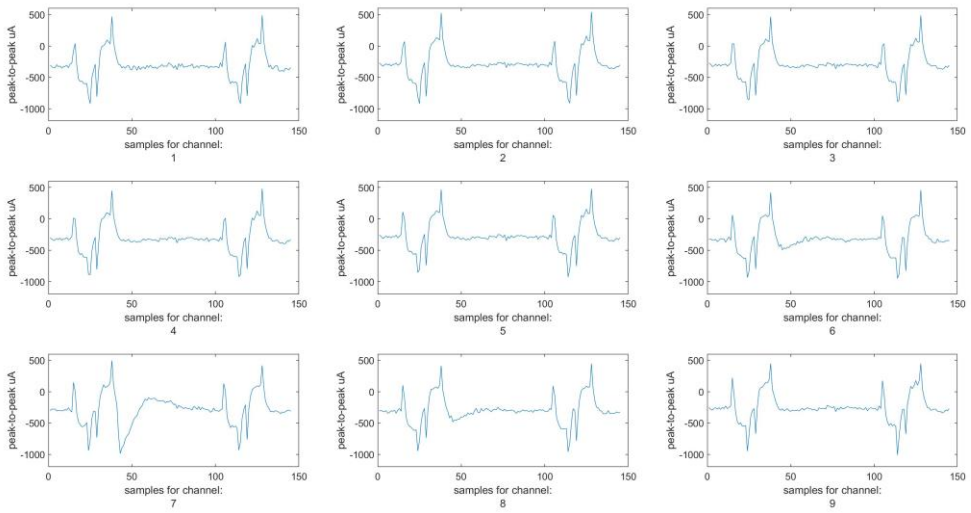

Figure 3. 6. Recorded data contain spike on channel number 7 and stimulation artifacts which has a shared structure on all channels.

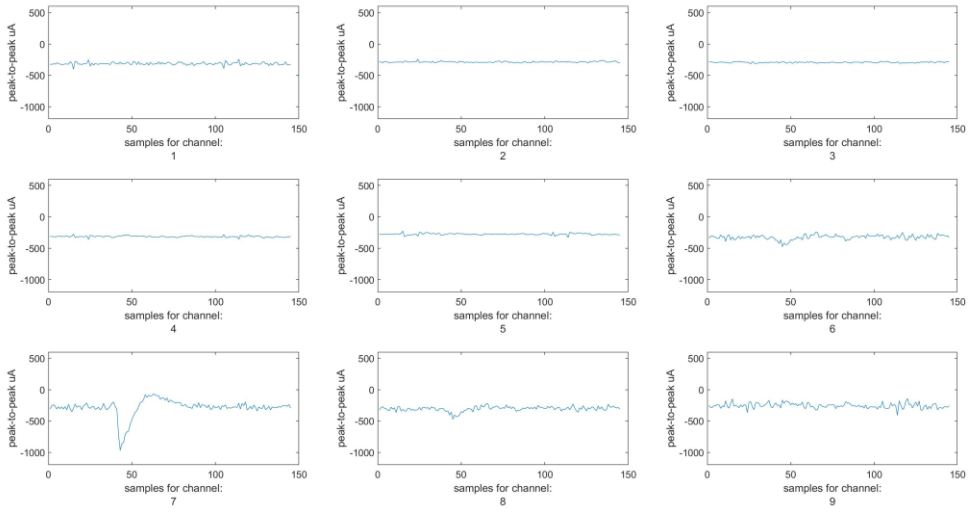

Figure 3. 7. Cleaned data preserving spike on channel number 7

Figure 3. 8 shows the recording data for 9 channels for a recording duration of 0.33 seconds. Each channel recorded the stimulation artifact. There are two spikes recorded in channel number 7, one of them during the stimulation pulse period. Figure 3. 9 shows artifact cleaned data for all channels using the implemented PCA algorithm. The two spikes are recovered in channel number 7.

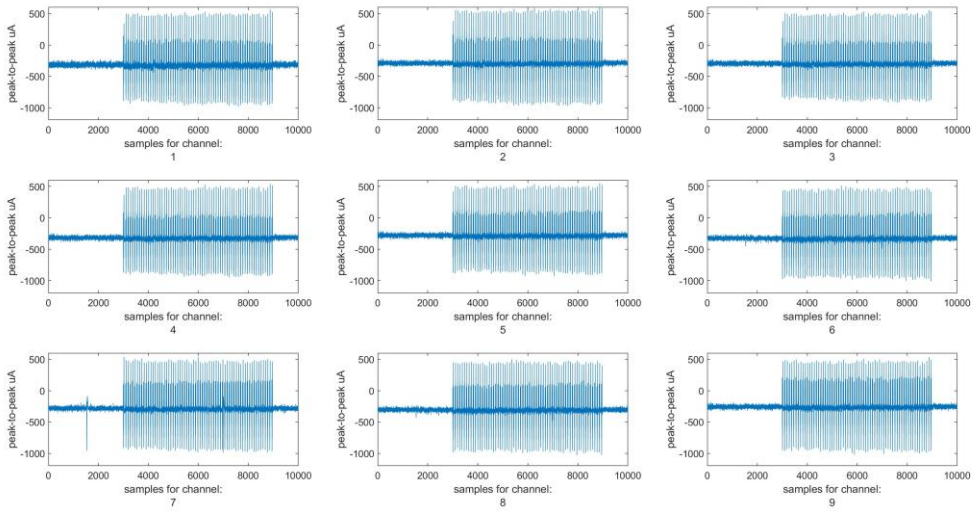

Figure 3. 8. Recorded data for a duration of 0.33 seconds contain two spikes on channel number 7 and stimulation artifacts on all channels.

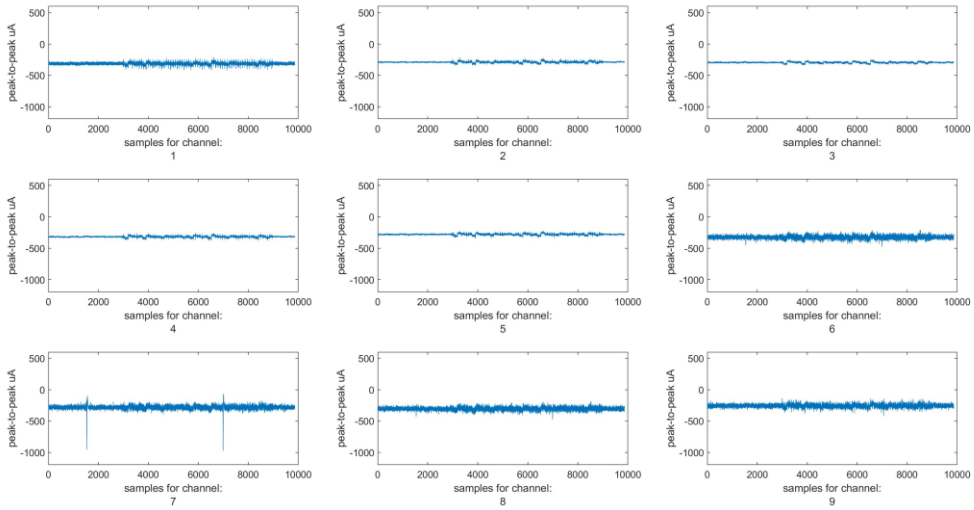

Figure 3. 9. Cleaned data preserving two spikes on channel number 7

The timing reports of the final implementation for the ten channels can be seen in TABLE 3. 2**.** Working frequency of the PCA algorithm is 10MHz. As it turns out, the processing time is equal to:

$$18020 \times 100ns = 1.802\ ms \qquad (2.\ 12)$$

Which is less than calculated interval time(4.834 ms).

TABLE 3. 2: Synthesis timing result

Timing	
Clock Frequency	10 MHz
Clock Period	100 ns
Clock Latency	18020

The resources usage of the final implementation for the ten channels can be seen in TABLE 3. 3**Error! Reference source not found.**. According to the results, there are enough resources for ten channels of data to be cleaned.

TABLE 3. 3: Synthesis resource result

Resource Usage	BRAM_18K	DSP48E	Flip Flop	Look Up Tables
Total Usage	86	401	61637	122753
Available	890	840	407600	203800
Utilization (%)	9	47	15	60

3.5. Conclusion

In this part of the project, first the behavior of the stimulation pulse in saline was analyzed experimentally, and various stimulation pulses were characterized in RHS Stim/Recording controller by Intan Tech. device. Then the hardware base PCA algorithm was implemented on Xilinx Kintex-7 FPGA KC705 Evaluation Kit. To this aim, first hardware base SVD processing unit was design and implemented. Then least square method unit was designed and implemented. At the first stage, the system simulated on Matlab and the result was calculated. Then, algorithm synthesized in Vivado HLS, and the result compared with the golden model by Matlab.

For the future work, optimization can be achieved by optimizing mathematical calculations and implementing them in the lower levels than high-level synthesis. This processing unit can then be integrated within the IC as a biomedical signal processor. In this way, the ASIC output is cleaned recorded data in terms of stimulation pulse artifacts.

4 Conclusion and Future Developments

In this dissertation, the complete flow of digital design from system-level design in MATLAB software, then high-level design simulation using Vivado HLS tool, then implementation in RTL and GL stage and finally implementation in Layout Level was performed. The application of whole design flow was neural signals analysis.

The digital core for the microelectrode array IC was designed and implemented in 180 nm CMOS technology. Digital core modules contain an on-chip digital controller and digital interface to off-chip PCB. This digital controller was designed and developed from RTL to Layout level.

In order to achieve this goal, a register memory was designed. Then the SPI protocol and the transmitter interface were developed, and their functionalities were verified through Modelsim simulation tools. Finally, all the digital components were integrated. This IC is in the process of being fabricated and being used to record the extracellular activities of *in vitro* neuron cells.

In order to recover the spikes that occur during stimulation by analog stimulation block, a real-time post-digital signal processing algorithm is designed and implemented on Xilinx Kintex-7 FPGA KC705 Evaluation Kit using Vivado HLS tool. Using this algorithm, recording artifacts will be detected and removed from signals.

To this aim, first hardware base SVD processing unit was design and implemented. Then least square method unit was designed and implemented. At the first stage, the system simulated on Matlab and the result was calculated. Then, algorithm synthesized in Vivado HLS, and the result compared with the golden model by Matlab.

For the future work, optimization can be achieved by optimizing mathematical calculations and implementing them in the lower levels than high-level synthesis. This processing unit can then be integrated within the IC as a biomedical signal processor. In this way, the MEA ASIC output is cleaned recorded data in terms of stimulation pulse artifacts.

Bibliography

[1] Frank Gibson et al., Minimum Information about a Neuroscience Investigation (MINI): Electrophysiology, Nat Biotechnol, 2008.

[2] A. S., «Focus on glia and disease,» *Nature Neuroscience* , vol. 10, pp. 1349-1349, 2007.

[3] C. Koch, G. Laurent, «Complexity and the nervous system,» *Science,* vol. 284, pp. 96-98, 1999.

[4] H. Lodish, A. Berk, C. A. Kaiser, M. Krieger, Molecular Cell Biology, New York: W. H. Freeman, 2000.

[5] E. R. Kandel, J. H. Schwartz, T. M. Jessell, Principles of Neural Science, New York: McGraw-Hill, 2000.

[6] A. Hierlemann, U. Frey, S. Hafizovic, F. Heer, «Growing Cells Atop Microelectronic Chips: Interfacing Electrogenic Cells In Vitro With CMOS-Based Microelectrode Arrays,» *Proceedings of the IEEE,* vol. 99, n. 2, pp. 252-284, 2011.

[7] J. Müller, B. J. Douglas, and A. Hierlemann, «Sub-millisecond closedloop feedback stimulation between arbitrary sets of individual neurons,» *Frontiers in neural circuits,* n. 6, p. 121, 2012.

[8] D. J. Bakkum,Z. C. Chao ,S. M. Potter, «Long-Term Activity-Dependent Plasticity of Action Potential Propagation Delay and Amplitude in Cortical Networks,» *PLoS ONE,* vol. 3, n. 5, 2008.

[9] P. Fromherz, «Electrical interfacing of nerve cells and semiconductor chips,» *Chemphyschem,* vol. 3, pp. 276-284, 2002.

[10] K. D. Wise, D. J. Anderson, J. F. Hetke, D. R. Kipke, and K. Najafi, «Wireless implantable microsystems: High-density electronic interfaces to the nervous system,» *Proc. IEEE*, vol. 92, n. 1, pp. 76-97, 2004.

[11] R. H. Olsson, III, D. L. Buhl, A. M. Sirota, G. Buzsaki, and K. D. Wise, «Band-tunable and multiplexed integrated circuits for simultaneous recording and stimulation with microelectrode arrays,» *IEEE Trans. Biomed. Eng.,* vol. 52, n. 7, pp. 1303-1311, 2005.

[12] M. Voelker and P. Fromherz, «Signal transmission from individual mammalian nerve cell to field-effect transistor,» *Small,* vol. 1, pp. 206-210, 2005.

[13] M. Jenkner, B. Mu¨ller, and P. Fromherz, «Interfacing a silicon chip to pairs of snail neurons connected by electrical synapses,» *Biol. Cybern.,* vol. 84, pp. 239-249, 2001.

[14] P. Bergveld, «Development of an ion-sensitive solid-state device for neurophysiological measurements,» *IEEE Trans. Biomed. Eng.,* Vol. %1 di %2BME-17, n. 1, pp. 70-71, 1970.

[15] M. P. Maher, J. Pine, J. Wright, and Y.-C. Tai, «The neurochip: A new multielectrode device for stimulating and recording from cultured neurons,» *J. Neurosci. Methods,* vol. 87, pp. 45-56, 1999.

[16] Y. Jimbo, T. Tateno, and H. P. Robinson, «Simultaneous induction of pathway-specific potentiation and depression in networks of cortical neurons,» *Biophys. J.,* vol. 76, pp. 670-987, 1999.

[17] A. Stett, U. Egert, E. Guenther, F. Hofmann, T. Meyer, W. Nisch, and H. Haemmerle, «Biological application of microelectrode arrays in drug discovery and basic research,» *Anal. Bioanal. Chem.,* vol. V377, pp. 486-495, 2003.

[18] U. Egert, D. Heck, and A. Aertsen, «Two-dimensional monitoring of spiking networks in acute brain slices,» *Exp. Brain Res.,* vol. 142, pp. 268-274, 2002.

[19] M. Hutzler, A. Lambacher, B. Eversmann, M. Jenkner, R. Thewes, and P. Fromherz, «High-resolution multitransistor array recording of electrical field potentials in cultured brain slices,» *J. Neurophysiol.,* vol. 96, pp. 1638-1645, 2006.

[20] U. Frey et al., «Switch-Matrix-Based High-Density Microelectrode Array in CMOS Technology,» *IEEE Journal of solid-state circuits,* vol. 45, n. 2, 2010.

[21] F. F., «Endogenous and exogenous electric fields as modifiers of brain activity: rational design of noninvasive brain stimulation with transcranial alternating current stimulation.,» *Dialogues in clinical neuroscience,* vol. 16, pp. 93-102, 2014.

[22] Luber B, Lisanby SH, «Enhancement of human cognitive performance using transcranial magnetic stimulation (TMS),» *NeuroImage,* vol. 85, pp. 961-970, 2014.

[23] Kocabicak E, Temel Y, Hollig A, Falkenburger B, Tan SKH, «Current perspectives on deep brain stimulation for severe neurological and psychiatric disorders,» *Neuropsychiatric disease and treatment,* vol. 11, pp. 1051-1066, 2015.

[24] Borchers S, Himmelbach M, Logothetis N, Karnath HO, «Direct electrical stimulation of human cortex - the gold standard for mapping brain functions,» *Neuroscience,* vol. 13, pp. 63-70, 2012.

[25] Duffau H, Capelle L, Sichez J, Faillot T, Abdennour L, Law Koune JD, Dadoun S, Bitar A, Arthuis F, Van Effenterre R, Fohanno D, «Intra-operative direct electrical stimulations of the central nervous system: the Salpetriere experience with 60 patients,» *Acta neurochirurgica,* vol. 141, pp. 1157-67, 1999.

[26] Matsumoto R, Nair DR, LaPresto E, Najm I, Bingaman W, Shibasaki H, Luders HO, «Functional connectivity in the human language system: a cortico-cortical evoked potential study.,» *Brain : a journal of neurology,* vol. 127, pp. 2316-2130, 2004.

[27] Kucewicz MT, Berry BM, Miller LR, Khadjevand F, Ezzyat Y, Stein JM, Kremen V, Brinkmann BH, Wanda P, Sperling MR, Gorniak R, Davis KA, Jobst BC, Gross RE, Lega B, Van Gompel J, Stead SM, Rizzuto DS, Kahana MJ, Worrell GA. , «Evidence for verbal memory enhancement with electrical brain stimulation in the lateral temporal cortex.,» *Brain : a journal of neurology,* 2018.

[28] S. Alagapan, H. W. Shin, F. Fröhlich, H. Wu, «Diffusion geometry approach to efficiently remove electrical stimulation artifacts in intracranial electroencephalography,» *J Neural Eng,* vol. 16, n. 3, 2019.

[29] A. Zhou, B. C. Johnson, R. Muller, «Toward true closed-loop neuromodulation: artifact-free recording during stimulation,» *Current Opinion in Neurobiology* , vol. 50, pp. 119-127, 2018.

[30] M. Ballini et al., «A 1024-Channel CMOS Microelectrode Array With 26,400 Electrodes for Recording and Stimulation of Electrogenic Cells In Vitro,» *IEEE Journal of solid-state circuits,* vol. 49, n. 11, 2014.

[31] J. Dragas et al., «In Vitro Multi-Functional Microelectrode Array Featuring 59 760 Electrodes, 2048 Electrophysiology Channels, Stimulation, Impedance Measurement, and Neurotransmitter Detection Channels,» *IEEE Journal of Solid-State Circuits,* vol. 52, n. 6, pp. 1576-1590, 2017.

[32] K. Limnuson, H. Lu, H. J. Chiel, and P. Mohseni, «Real-Time Stimulus Artifact Rejection Via Template Subtraction,» *IEEE Transactions on Biomedical Circuits and Systems,* vol. 8, n. 3, pp. 391-400, 2014.

[33] Brown, E A, J D Ross, R A Blum, Y Nam, B C Wheeler, and S P DeWeerth , «Stimulus-Artifact Elimination in a Multi-Electrode System.,» *IEEE transactions on biomedical circuits and systems,* vol. 2, n. 1, pp. 10-21, 2008.

[34] Stanislav Culaclii, Brian Kim, Yi-Kai Lo, and Wentai Liu, «A Hybrid Hardware and Software Approach for Cancelling Stimulus Artifacts During Same-electrode Neural Stimulation and Recording,» *UCLA Journal,* pp. 6190-6193.

[35] Mena, Gonzalo E, Lauren E Grosberg, Pawel Hottowy, Alan Litke, John Cunningham, E J Chichilnisky, and Liam Paninski, «Electrical Stimulus Artifact Cancellation and Neural Spike Detection on Large Multi-Electrode Arrays.,» *Journal of neuroscience,* vol. 141, n. 2, pp. 171-198, 2016.

[36] Daniel J. O'Shea, Krishna V. Shenoy, «ERAASR: an algorithm for removing electrical stimulation artifacts from multielectrode array recordings,» *Journal of Neural Engineering,* vol. 15, 2018.

[37] Michael E. Wall, Andreas Rechtsteiner, Luis M. Rocha, «Singular Value Decomposition and Principal Component Analysis,» *A Practical Approach to Microarray Data Analysis,* pp. 91-109, 2003.

[38] Charnes, A., Frome, E. L.; Yu, P. L., «The Equivalence of Generalized Least Squares and Maximum Likelihood Estimates in the Exponential Family,» *Journal of the American Statistical Association,* vol. 71, n. 353, pp. 169-171, 1976.

[39] Lai, T.L.; Robbins, H.; Wei, C.Z, «Strong consistency of least squares estimates in multiple regression,» *PNAS,* vol. 75, n. 7, pp. 3034-3036, 1978.

A TCL Command for Design Compiler

```
# ****** PROVIDE DATA: ******
# time unit: 1ns
# Set variables and design names
set TOP_DESIGN_NAME spi
set TOP_DESIGN_ARCHITECTURE structural

# Clock signals
set CLK_NAME sck
set CLK_PERIOD 50 #ns (frequency = 20 MHz)

########################################
# Start from fresh state
#Removes the designs or libraries from memory
remove_design -all

# Analyze VHDL sources
#Reads and analyzes the HDL files and stores the intermediate format in the specified design library
analyze -format vhdl {\
        /home/{source_code_directory}/spi.vhd
   }
# Elaborate design#Builds a design from the intermediate format (maps to gtech lib)
elaborate ${TOP_DESIGN_NAME} -architecture ${TOP_DESIGN_ARCHITECTURE} -library work

# Define constraints#Creates a clock object and defines its waveform
create_clock $CLK_NAME -period $CLK_PERIOD
# Displays clock-related information on the current design.
report_clock

#Sets the load attribute of the specified ports
#Set a capacitive load value of 1.5 on all output ports
set_load 1.5 [all_outputs]
# Set output external delay
set_output_delay 20 -max -clock $CLK_NAME [all_outputs]
# Compile design
set compile_top_all_paths true
compile_ultra
#--------------------------# Generate reports#----------------------------------------------------------
if { ! [file exists reports/${TOP_DESIGN_NAME} ] } {file mkdir reports/${TOP_DESIGN_NAME}}
# Constraint Report: List of the constraints on the current design and their cost, weight, and weighted cost.
# Area Report: the required area of the design in "micro-meter^2".
# Register Report: List of sequential elements or pins in a design.
# Timing Report: "slack time" requires to be positive time. In Timing Report,  key word "met" means it met this requirement.
#Resource Report: Displays information about the resource implementation.
#Design Check: Checks the current design for consistency
report_constraint -nosplit -all_violators \
  > reports/${TOP_DESIGN_NAME}/${TOP_DESIGN_NAME}_mapped_allviol.rpt
report_area -hierarchy > reports/${TOP_DESIGN_NAME}/${TOP_DESIGN_NAME}_mapped_area.rpt
report_register -nosplit > reports/${TOP_DESIGN_NAME}/${TOP_DESIGN_NAME}_mapped_registers.rpt
report_timing > reports/${TOP_DESIGN_NAME}/${TOP_DESIGN_NAME}_mapped_timing.rpt
```

```
report_resources -nosplit -hierarchy \
  > reports/${TOP_DESIGN_NAME}/${TOP_DESIGN_NAME}_mapped_resources.rpt
check_design -summary > reports/${TOP_DESIGN_NAME}/${TOP_DESIGN_NAME}_mapped_check_design.rpt
#----------------------Generate VHDL netlist
if { ! [file exists netlists ] } {file mkdir netlists}
change_names -rule vhdl -hierarchy
# Writes a design netlist to a file
write -format vhdl -hierarchy -output netlists/${TOP_DESIGN_NAME}_mapped.vhd

#----------------------Generate Verilog netlist
#The mapped design is reloaded to avoid potential naming problems when using
#the netlist for placement and routing
if { ! [file exists ../encounter/src ] } {file mkdir ../encounter/src}
change_names -rule verilog -hierarchy
# Writes a design netlist to a file
write -format verilog -hierarchy -output netlists/${TOP_DESIGN_NAME}_mapped.v
# verilog netlist preferred to be used for Placing and Routing
write -format verilog -hierarchy -output ../encounter/src/${TOP_DESIGN_NAME}_mapped.v
#-----------------------Generate SDF data
#Delay and constraints data in Standard Delay Format (sdf)
write_sdf -version 2.1 netlists/${TOP_DESIGN_NAME}_mapped.sdf
#-----------------------Generate SDC data
#Synopsys Design Constraints (sdc) file for a third party tool (Place-and-Route tools)
write_sdc -nosplit netlists/${TOP_DESIGN_NAME}_mapped.sdc
write_sdc -nosplit ../encounter/src/${TOP_DESIGN_NAME}_mapped.sdc

echo "-i- Done"
```

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List of symbols

Abbreviations	Description
IC	Integrated Circuit
MEA	Micro Electrod Arrays
PCA	Principal Component Analysis
RTL	Register Transfer Level
SPI	Serial Peripheral Interface
GL	Gate Level
LL	Layout Level
SDC	Synopsys Design Constraints
TCL	Tool Command Language
VDD	Voltage Drain Drain
GND	Ground
SDF	Standard Delay Format
LSM	Least Square Method
PCB	Printed Circuit Board
FPGA	Field Programable Gate Array
SVD	Singular Value Decomposition
LSQR	Least Square Method

ASIC	Application-Specific Integrated Circuit
FET	Field-Effect Transistor

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