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**SCUOLA DI INGEGNERIA INDUSTRIALE
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EXECUTIVE SUMMARY OF THE THESIS

Real-Time Emulation of a Power Converter using Microcontroller-Based Systems

LAUREA MAGISTRALE IN ELECTRONIC ENGINEERING - INGEGNERIA ELETTRONICA

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Introduction

The growing demand for highly efficient power electronic systems has driven the development of increasingly advanced converters, characterized by high switching frequencies, elevated power density, and sophisticated control strategies. In this context, rapid prototyping and validation methodologies have become essential tools to reduce development time and overall design costs. Hardware-in-the-Loop (HIL) has emerged as a powerful approach for the testing and validation of power electronic systems, where part of the physical system is replaced by a high-fidelity digital model interacting in real time with the remaining hardware. **“Why should an emulation-based approach be adopted if the real system is already available?”** The motivation can be summarized in three main aspects: the ability to continue testing even when some components are unavailable, the reduction of risks associated with experimental validation, and the increased flexibility in modifying operating conditions and system parameters.

These advantages are particularly relevant in power electronics applications, where loads and industrial equipment are often costly, inaccessible, or exposed to damage during testing. HIL

platforms therefore provide a safe and portable environment for system validation while reducing the need for dedicated high-power laboratory infrastructure.

This work investigates the development of a low-cost HIL platform for power converter emulation, focusing on the selection of the emulation hardware, the implementation of a computationally efficient converter model, and its experimental validation.

1. Hardware-in-the-Loop (HIL)

“How can a low-power device such as an HIL platform emulate high-power systems rated in the order of tens of kilowatts while maintaining high fidelity?”

The key principle is that the HIL platform does not reproduce the full power flow of the system, but only its external behavior as observed at the electrical interfaces. In fact, it emulates also the sensor signals that connect the subsystem under test to the rest of the system. Although the real application may involve high-power levels, the HIL device operates exclusively with low-voltage signals (typically 0–5 V), meaning that its firmware must accurately model both the dynamic behavior of the subsystem and its sensors

response.

This approach enables safe validation by removing parts of the physical system during early testing. Faults such as overcurrent events can be simulated without risking hardware damage while still providing realistic stimuli for algorithm development.

1.1. FPGA vs Microcontroller emulation boards

Numerous Hardware-in-the-Loop (HIL) platforms are available on the market, which can be distinguished on Field Programmable Gate Arrays (FPGA) or microcontrollers (MCU). Microcontroller-based systems rely on a sequential execution model, where algorithms are implemented in C/C++ or generated from tools such as MATLAB/Simulink. The processing is handled by a CPU, while peripherals such as ADCs, timers, PWM modules ... support the execution. In contrast, FPGAs are configured through Hardware Description Languages (HDLs) such as VHDL or Verilog, allowing the designer to define custom hardware structures composed of logic blocks, registers, and interconnections. This results in a massively parallel architecture with deterministic timing and very low latency, which makes FPGAs particularly well suited for real-time HIL applications that require high fidelity and fast dynamic response. Despite these advantages, FPGA-based solutions present two major drawbacks: high development complexity and elevated cost. The design flow, including synthesis, can require significant computational time even for relatively simple systems. Additionally, FPGA hardware is considerably more expensive compared to microcontroller-based platforms.

Platform	Cost	HW	Timestep
Typhoon HIL604	~120k €	FPGA	20 ns
PLECS RT Box 1	~18k €	FPGA CPU	7.5 ns
Speedgoat Performance	~60k €	FPGA CPU	~100 ns
ST HIL board	~200 €	MCU	~10 μ s

For this reason, microcontrollers represent a competitive alternative in many HIL applications. Although they offer lower accuracy in reproducing very high-frequency dynamics, they provide substantial benefits in terms of cost reduction, simpler development, and faster implementation. From an industrial perspective, this

cost-effectiveness validation tool is crucial, especially for who need real-time emulation technologies and may not have access to expensive FPGA-based solutions. STMicroelectronics offers a microcontroller-based solution with the *STEVAL-HILE1G4K1* kit, specifically designed for real-time HIL applications [3].

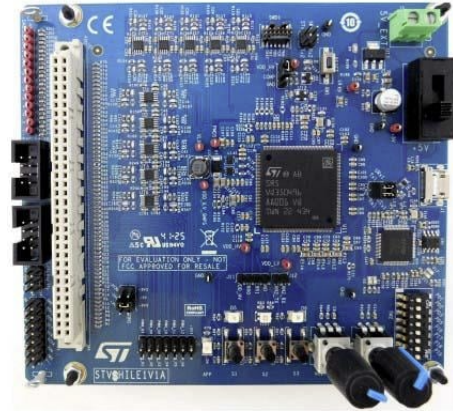


Figure 1: HIL MCU board

The platform targets power electronics emulation, where dominant system dynamics typically lie in the kilohertz range. In this context, the use of a microcontroller operating at a few hundred kilohertz, combined with advanced mathematical models, is sufficient to achieve the required level of fidelity. The system supports a model-based design workflow using MATLAB/Simulink, enabling automatic code generation from graphical models and thereby facilitating rapid prototyping, simplified debugging, and extensive pre-deployment simulation.

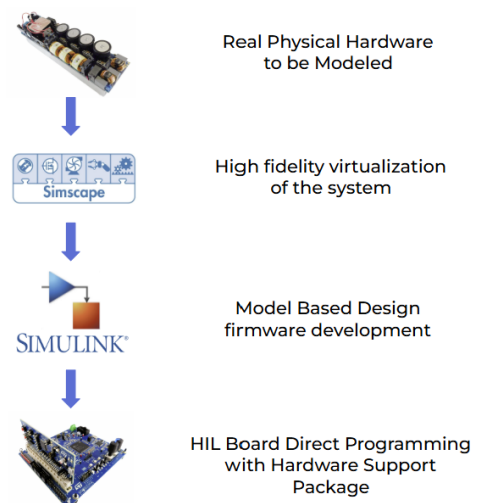


Figure 2: Flow HIL Design

2. Application

Totem-Pole (TP) AC-DC converter is introduced as a representative case study for the analysis of Hardware-in-the-Loop (HIL) emulation in power electronics.

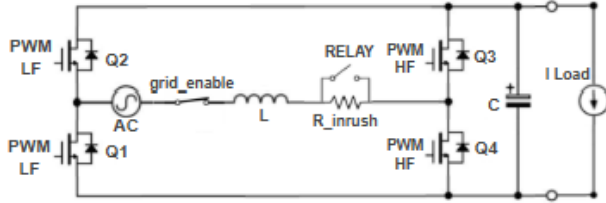


Figure 3: Totem Pole Schematic

The low-frequency switches act as a synchronous rectifier, while the high-frequency switches implement a boost stage that alternately stores and releases energy in the inductor. This allows the output capacitor voltage to exceed the grid peak value while maintaining a controlled sinusoidal input current for a Power Factor Corrector action driving correctly the gates.

The objective of this thesis is to:

1. **develop a mathematical model of the Totem-Pole converter (plant)** that can be performed at frequencies compatible with the working frequency of the HIL board ($\sim 100kHz$);
2. **validate it** through software simulations using Simscape;
3. implement it on the HIL hardware platform;
4. connect the HIL board to a dedicated control board mounted on the STEVAL-7BIDIRCB STMicroelectronics product;
5. verify through hardware testing that the controller responds to and regulates the HIL model as if it were interacting with the real converter;
6. verify that the regulated waveforms match those observed on the complete STEVAL-7BIDIRCB system.

3. Circuit Modeling

Inrush phase

Before reaching steady-state operation, a soft-start procedure is implemented. During the precharge phase, the DC bus capacitor is charged through an inrush resistor while all MOSFETs remain OFF. The current flows only through the body diodes of the power switches,

which temporarily operate as a passive rectifier bridge, limiting the charging current and producing a controlled capacitor voltage rise.

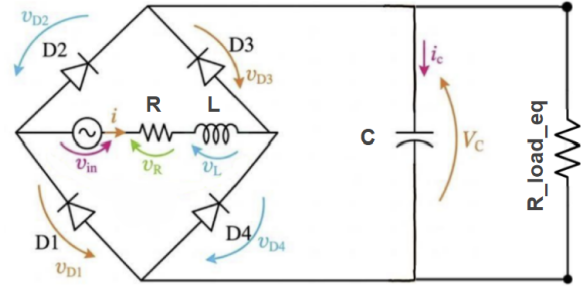


Figure 4: Inrush circuit model

The startup dynamics can be described by a piecewise-linear model characterized by three operating states, corresponding to the possible diode conduction configurations. We will adopt the Backward Euler method, with step size h , to solve the piecewise system of the inrush phase on microcontroller [2].

D1-D3 ON D2-D4 OFF

$$\begin{cases} V_{in,n+1} = Ri_{L,n+1} + L \frac{i_{L,n+1} - i_{L,n}}{h} + 2V_{TH} + v_{c,n+1} \\ C \frac{v_{c,n+1} - v_{c,n}}{h} = i_{L,n+1} - \frac{v_{c,n+1}}{R_{eq_load}} \end{cases}$$

D2-D4 ON D1-D3 OFF

$$\begin{cases} V_{in,n+1} = Ri_{L,n+1} + L \frac{i_{L,n+1} - i_{L,n}}{h} - 2V_{TH} - v_{c,n+1} \\ i_{L,n+1} = -C \frac{v_{c,n+1} - v_{c,n}}{h} - \frac{v_{c,n+1}}{R_{eq_load}} \end{cases}$$

D1-D2-D3-D4 OFF

$$\begin{cases} i_{L,n+1} = 0 \\ -\frac{v_{c,n+1}}{R_{eq_load}} = C \frac{v_{c,n+1} - v_{c,n}}{h} \end{cases}$$

And a state machine capable of determining when to switch between the different sets of equations, by monitoring the voltages to turn-on and the inductor current for the turn-off.

Burst phase

The burst phase completes the soft-start procedure bypassing the R_{inrush} . After a predefined delay, the PWM signals are activated in burst mode, introducing high-frequency switching. Here we need to change model.

“Why is it necessary to introduce a new model instead of using the same one

throughout the entire startup process?”

The answer lies in the computational limitations of the HIL platform, fast switches need to be modeled with mathematical techniques on period to slow down the computation without losing accuracy. The previous model considered only the body diodes, now we need to model the MOSFETs as switches like in PFC mode.

Power Factor Corrector (PFC) phase

The system can therefore be modeled as a piecewise-linear switching system, characterized by four distinct operating modes.

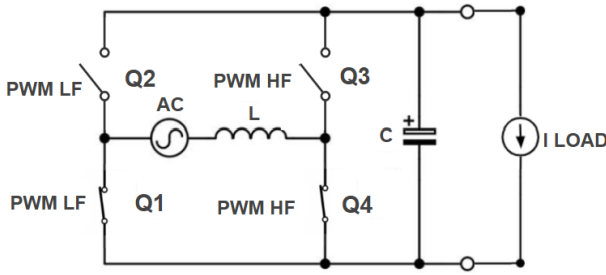


Figure 5: Totem Pole PFC Model

PWM LF DOWN and HF DOWN = ON

$$\begin{cases} L \frac{di_L}{dt} = v_{in}(t) \\ C \frac{dv_c}{dt} = -i_{load} \end{cases}$$

PWM LF DOWN and HF UP = ON

$$\begin{cases} L \frac{di_L}{dt} = v_{in}(t) - v_c \\ C \frac{dv_c}{dt} = i_L - i_{load} \end{cases}$$

PWM LF UP and HF UP = ON

$$\begin{cases} L \frac{di_L}{dt} = v_{in}(t) \\ C \frac{dv_c}{dt} = -i_{load} \end{cases}$$

PWM LF UP and HF DOWN = ON

$$\begin{cases} L \frac{di_L}{dt} = v_{in}(t) + v_c \\ C \frac{dv_c}{dt} = -i_L - i_{load} \end{cases}$$

Solving this equations with Backward Euler is impossible since required a discretization step smaller than the capability of the board. So we need Average Model. The *Average model* is a modeling technique that enables the description of switching power converters by replacing the time-varying dynamics introduced by the switching actions with an equivalent averaged

behavior over a switching period. In this approach, the switching dynamics of the system are substituted by an equivalent continuous-time representation obtained as the weighted average of the state derivatives over the different switching intervals [1].

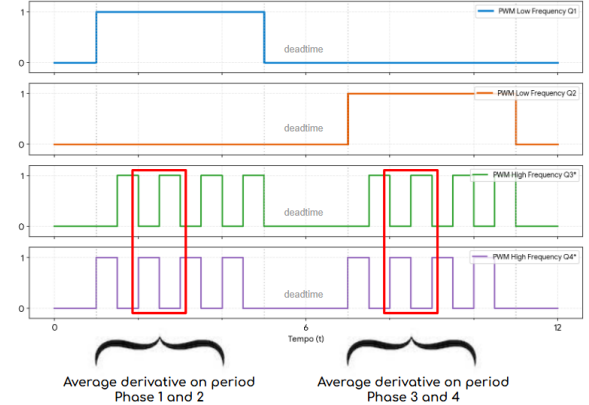


Figure 6: Qualitative PWM in PFC mode

The two average derivatives for the inductor current are

Phase 1 - 2 - Q1 ON

$$\left\langle \frac{di_L}{dt} \right\rangle = \frac{v_{in}(t)}{L} \text{duty}_{Q4}(t) + \frac{v_{in}(t) - v_c}{L} \text{duty}_{Q3}(t)$$

Phase 3 - 4 - Q2 ON

$$\left\langle \frac{di_L}{dt} \right\rangle = \frac{v_{in}(t)}{L} \text{duty}_{Q4}(t) + \frac{v_{in}(t) + v_c}{L} \text{duty}_{Q3}(t)$$

While for the derivative of the capacitor voltage:

Phase 1 - 2 - Q1 ON

$$\left\langle \frac{dv_c}{dt} \right\rangle = -\frac{i_{load}}{C} \text{duty}_{Q4}(t) + \frac{i_L - i_{load}}{C} \text{duty}_{Q3}(t)$$

Phase 3 - 4 - Q2 ON

$$\left\langle \frac{dv_c}{dt} \right\rangle = -\frac{i_{load}}{C} \text{duty}_{Q4}(t) + \frac{-i_L - i_{load}}{C} \text{duty}_{Q3}(t)$$

Once the average state derivatives have been defined, they can be integrated using the Forward Euler method with a time step equal to the switching period

$$i_L(k+1) = i_L(k) + T_s \left\langle \frac{di_L}{dt} \right\rangle_k$$

$$v_c(k+1) = v_c(k) + T_s \left\langle \frac{dv_c}{dt} \right\rangle_k$$

4. Validation

Software Simulation Results

Taking advantage of the Model-Based Design approach, a preliminary software validation is performed by comparing the proposed numerical model, based on the equations derived in the previous sections, with a high-fidelity Simscape simulation. The reference Simscape model is executed without real-time constraints, using a discretization step equal to one hundredth of the timestep adopted for the microcontroller implementation, namely $h = T_{sw} = 15 \mu s$. This allows the Simscape model to be considered as a highly accurate benchmark for evaluating the accuracy of the proposed HIL-oriented model.

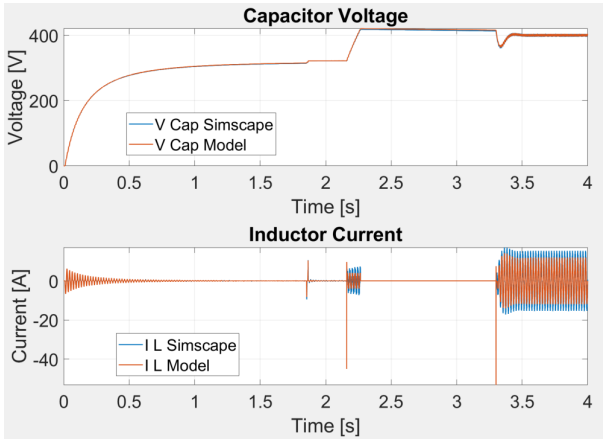


Figure 7: Software Validation

The high-frequency Simscape simulation and the proposed Average Model produce almost identical results. For this software simulation, a simplified control algorithm was implemented to regulate the plant. The same virtual controller was used for the high-fidelity Simscape model and the numerical model, ensuring a consistent basis for comparison between the approaches.

Hardware Validation Results

For the hardware validation, the control firmware originally developed for the *STEVAL-7BIDIRCB* converter was employed. The proposed plant model was deployed onto the HIL board, while the control firmware was executed on a Nucleo board featuring an STM32G474RE microcontroller.

After performing the required firmware porting and determining the appropriate digital gains, the signals exchanged between the controller and

the emulated plant were successfully monitored and analyzed using an oscilloscope.

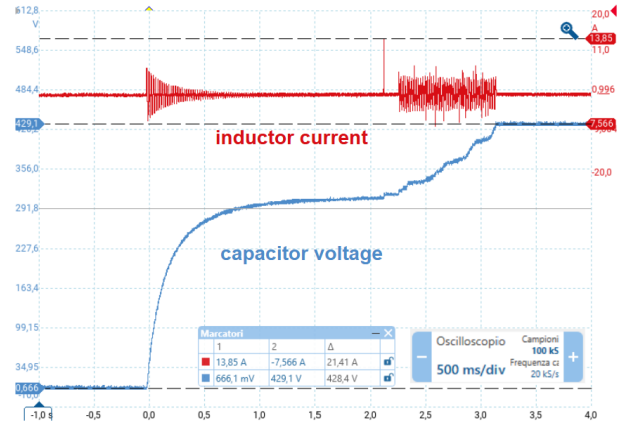


Figure 8: Hardware Validation

5. Conclusion

The objective of developing a computationally efficient and high-fidelity digital model of a power converter, capable of real-time execution on a low-cost microcontroller, has been successfully achieved.

The mitigation of the minor glitches caused by PWM soft-start effects during LF-PWM dead-time would further improve the overall performance; however, this extension is already well structured within the current modeling framework and can be readily implemented by extending in a new phase the existing model.

The adoption of a Model-Based Design workflow significantly simplified the development, testing, and deployment processes, proving to be an effective methodology for both emulation and control-system design.

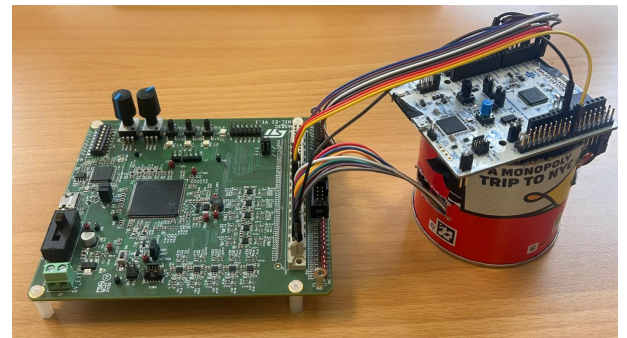


Figure 9: Hardware Setup

References

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- [2] Alfio Quarteroni, Riccardo Sacco, and Fausto Saleri. *Numerical Mathematics*. Springer, 2 edition, 2007.
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