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Executive Summary of the Thesis

Analog-Digital CMOS Controller for Real Time Reconfiguration of Integrated Photonic Circuits

Laurea Magistrale in Electronics Engineering - Ingegneria Elettronica

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1. Introduction

Integrated Photonics is gaining interest in an increasing number of applications where light demonstrated to be an efficient medium for transmitting and processing information. Long range optical communications through optical fibers is a successful example of this trend. The advantages introduced by these optical links with respect to former wires are pushing the adoption of such optical technology in smaller scale systems as well, down to the size of a single integrated chip. One example in this direction is the interconnection and data transfer among servers where optical links seem representing the only viable solution for the power-hungry industry of data centers.

Among many technologies used to create Photonic Integrated Circuits (PICs), Silicon Photonics seems to be one of the most promising. Silicon offers two major advantages: it is almost transparent, on short distances, for Near InfraRed (NIR) wavelengths (1550 and 1300 nm), and it relies on a long-established technology already developed for electronics, thus allowing for a relatively cheap fabrication of complex and densely integrated optical systems. It is hard to find a material that better combines optical and electrical properties.

However, silicon optical properties, particularly the refractive index, are extremely sensitive on temperature variations. No Si-PIC could work open-loop: it is mandatory to implement a control system that guarantees the reliable operation of the photonic circuit. This need has triggered the design of electronic circuits specifically devoted to sensing, steering, setting and locking the working point of a SiP PIC to the desired value. The striking advantage of silicon photonics is clear: the whole system (optics, sensors, control loop and actuators) can be realized onto the same wafer and with common process fabrication steps.

As a step in this direction, this thesis develops a CMOS electronic control system, with comparable size to that of the optical devices to be controlled (so as to be placed next to the photonic chip), able to perform real-time reconfiguration of a PIC consisting in a matrix (*mesh*) of *Mach-Zehnder Interferometers* (MZIs, Fig. 1). The ASIC contains both the analog sections to acquire the signals from the photodiodes integrated into the MZIs and to drive the actuators that modify the working point of the device. In addition to that, the chip is provided with all

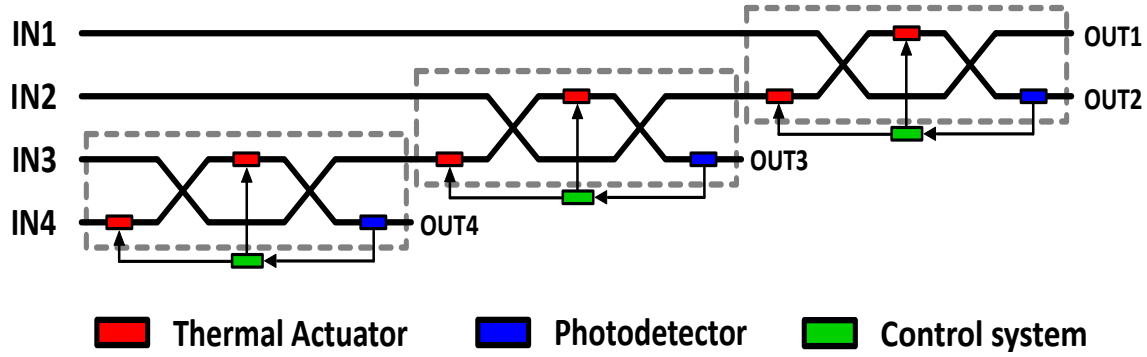

Figure 1: Schematic representation of a mesh of Mach-Zehnder interferometers

the digital sections to perform a full and independent electronic control of the system, with no the need of additional external circuits. With respect to previous fully analog designs [1], the adoption of a mixed analog-digital solution will pave the way for an increase in the integration density and versatility of the electronic system and, as a consequence, in the complexity of the PIC to be controlled. What follows goes into the details of the ASIC architecture and of the design solutions adopted in the work.

2. Control System

In a very simplified description, the output power distribution P_{OUT} of MZIs is determined by the interference between the waves propagating in the two branches, and it is, in general, a sinusoidal function of their relative phase shift. Recalling that a wave propagating in a waveguide for a distance L accumulates a phase $\phi = 2\pi\frac{L_{opt}}{\lambda}$, with $L_{opt} = n_{Si} \cdot L$, it is possible to exploit the dependence of n_{Si} on temperature variation ($\approx 1.8 \cdot 10^{-4}\,K^{-1}$ at 300 K) in order to modify such phase shift and implement a control loop around the device. This is the reason behind the adoption of thermal actuators, called *heaters*, consisting in Ti resistors ($R_H \approx 0.1 - 1\,k\Omega$), driven with a 0-6 V voltage drop, integrated close to the waveguides so as to locally modify n_{Si} and as a consequence the accumulated ϕ_H.
The linearization of $n_{Si}(T)$ around a given temperature allows to state a proportionality between ϕ_H and the heaters' dissipated power P_H:

$$\phi_H = \phi_0 + \Delta\phi_H \frac{P_H}{P_{HMAX}} = \phi_0 + \Delta\phi_H \frac{V_H^2}{V_{HMAX}^2}$$

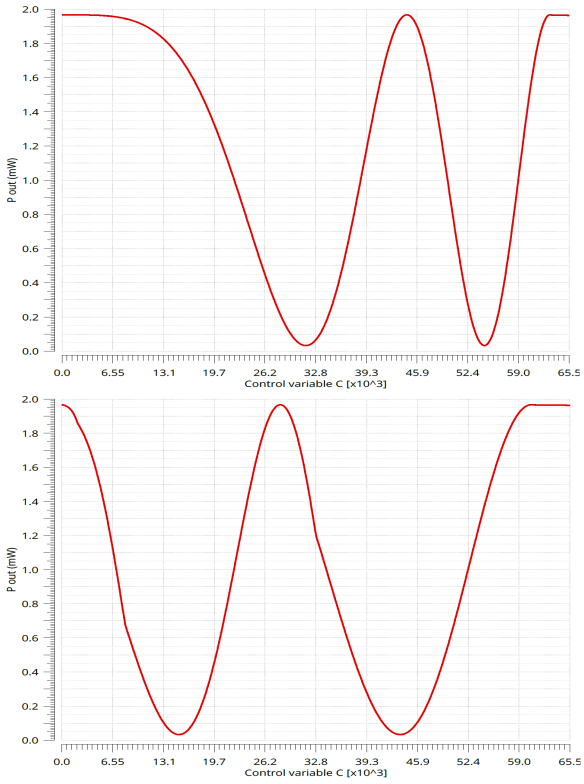

Figure 2: Output power of the MZI as a function of the control variable C without (**a**) and with (**b**) making the square-root. Residual distortion is due to the algorithm that approximates a square root at digital level, but does not exactly match it.

It is evident that a non-linearity has been introduced: the phase shift ϕ_H is proportional to the square of the control variable V_H: it means that whatever small signal v_d superimposed to V_H will modulate ϕ_H with a dependence on the working point of the heater (Fig. 2a). To solve this issue, a possible solution is the introduction, inside the loop, of a block, realized in this project at digital level, that imitates a

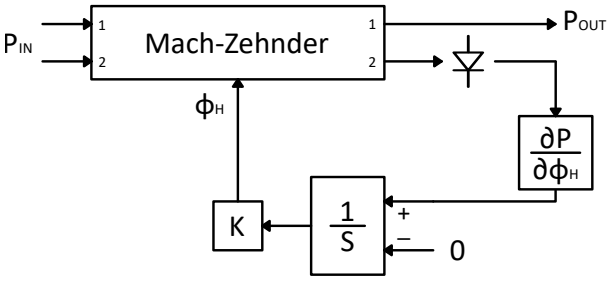

Figure 3: Simplified schematic of a single-variable integral control system

square root operation. The system elaborates a control variable C, which eventually undergoes the square root so as to deliver at the heater $V_H \propto \sqrt{C}$, so that $\phi_H \propto C$: whatever signal superimposed to C will determine a modulation of ϕ_H whose amplitude will be independent from the working point(Fig. 2b).
Most applications requires the MZI to fully steer input power towards one of the two branches, i.e. to make the system work around a maximum/minimum of $P_{OUT}(\phi_H)$. From the standpoint of the control loop, this is equivalent to say that the system has to look for the points where $\frac{\partial P_{OUT}}{\partial \phi_H} = 0$. It is thus necessary to extract the information about the derivative of the MZI transfer function in order to implement an integral controller that always tries to minimize $\frac{\partial P_{OUT}}{\partial \phi_H} = 0$. The sign of the integration determines whether the system points to a maximum or to a minimum.
The operation that allows to extract the information about $\frac{\partial P_{OUT}}{\partial \phi_H} = 0$ goes under the name of *dithering*, which already proved effective in many similar applications [2]. It consists in the application of a small square wave (amplitude v_d, frequency f_d) on top of the working point of the heater, as:

$$V_H(t) = V_{H0} + v_d \cdot sqw(t)|_{f=f_d}$$

This will turn into a modulation of the output optical power, as:

$$P_{OUT} \approx P_{OUT}(V_{H0}) + P_d \cdot sqw(t)|_{f=f_d}$$

If v_d is sufficiently small, the amplitude of the output modulation will be proportional, in the first approximation, to:

$$P_d = v_d \cdot \left.\frac{\partial P_{OUT}}{\partial V_H}\right|_{V_H=V_{H0}}$$

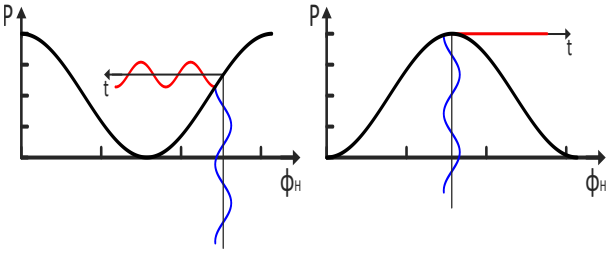

Figure 5: Schematic representation of dithering: blue is the modulation of phase shift applied by the heater, red signal is the resulting modulation at output, which is nil when working close to a maximum or minimum.

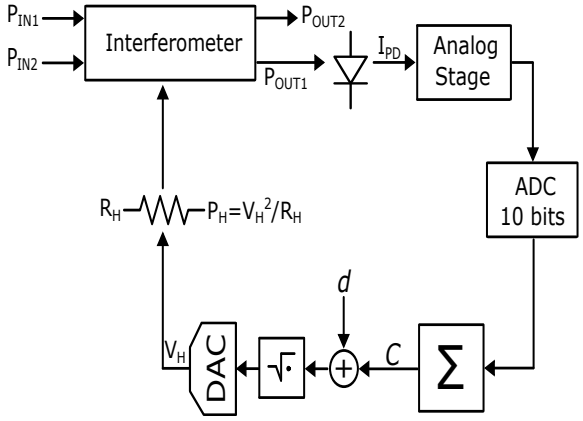

Figure 4: Schematic representation of the control loop. Highlighted in red are all the gains of the blocks.

The technique can be extended to systems with two actuators, as it is the case of the MZI: the output power modulation will be proportional to the sum of the partial derivatives $\frac{\partial P_{OUT}}{\partial V_{H1}}$ and $\frac{\partial P_{OUT}}{\partial V_{H2}}$. In order to be able to discriminate the two dithering signals that will mix up in the photodiode current, it is sufficient that they are in quadrature: the application of a demodulating signal in phase with $v_{d1} \cdot sqw(t)|_{f=f_d}$ will extract $\frac{\partial P_{OUT}}{\partial V_{H1}}$, and at the same time will make nil the integral of the other dithering over one period.
It is interesting to try to evaluate the loop gain around a minimum of the transfer function, which is a typical working point for the device: when no power impinges on the photodiode, it means that all the light is steered towards the "non blocking" output of the MZI. A schematic representation of the control loop is represented if Fig. 4. Particular care should be put in computing the gain of two blocks:

- The optical part. The relevant informa-

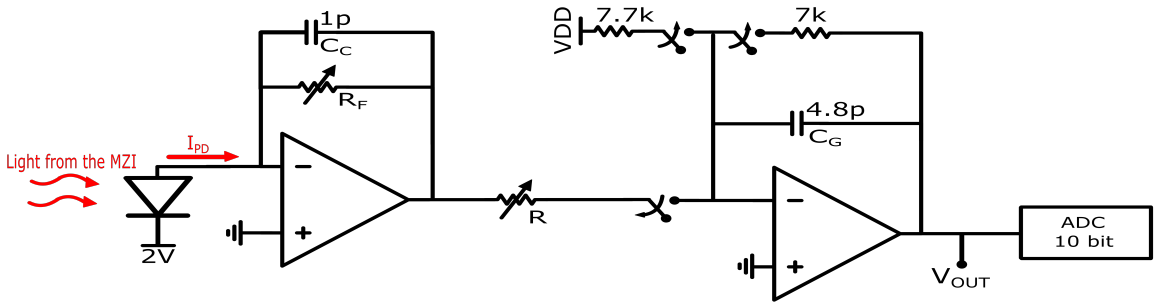

Figure 6: Schematic representation of the input stage

tion consists in the variation of the output dithering amplitude with respect to the variation of the control variable C, i.e. of $\frac{\partial P_d}{\partial C}$. This information can be extracted by measuring $\frac{\partial I_{PD}}{\partial V_H^2}$. Since the system is supposed to be locked in a minimum, where $\frac{\partial I_{PD}}{\partial V_H^2}$=0, the second derivative of the MZI transfer function should be considered, i.e. $\frac{\partial^2 I_{PD}}{\partial V_H^4}$.

- The integrator. It is implemented as a discrete time integrator, working in digital domain. However, it is possible to demonstrate that for signals at a frequency lower than the sampling frequency (set at 100 kHz), the discrete-time integrator can be approximated just as a continuous-time one, described in Laplace domain as $\frac{K}{s}$, K being the sampling frequency f_s.

All these premises being done, and assuming an ideal square root operation, the loop-gain can be written as:

$$\frac{C_0 + \Delta C}{C_0} = \left.\frac{\partial P_d}{\partial C}\right|_{C=C_0} \cdot S_{21} \cdot G_{TIA} \cdot G_{ADC} \cdot \frac{K}{s}$$

Considering a measured $\frac{\partial^2 I_{PD}}{\partial V_H^4} = 7.4\,\frac{\mu A}{V^4}$, f_S=100 kHz, $f_d = \frac{100\,kHz}{12}$ and a dithering amplitude d=2^{10}, the resulting bandwidth is around 1 kHz, well beyond what is needed for most applications: that is why in the digital part the possibility to slow down the bandwidth has been added.

3. Analog Front-End

The very first stage of the acquisition chain is composed by an analog front-end, schematically represented in Fig. 6. The current signal is first amplified by a TIA and then integrated for $T_G \approx 9.55\,\mu s$ (10.5 clock cycles) on C_G, for a resulting

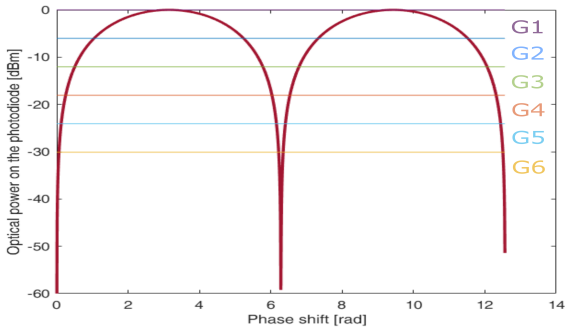

Figure 7: Power on the photodiode (log scale) as a function of the relative phase shift induced in the waveguides of the MZI

voltage gain equal to

$$G_{IN} = \frac{R_F}{R} \cdot \frac{T_G}{C_G}$$

A photodiode is used to sense the optical power at the MZI output. With respect to transparent methods of detection [3] that rely on the very little losses in the waveguide, the photodiode absorbs all the output light, allowing for an improved sensitivity and, as a consequence, a better rejection ratio when steering the MZI. The price to pay is the fact that all the outputs of the *mesh*, except one, will be blocked by the photodiode. Despite this partial limitation, however, meshes with photodiodes are still useful in a number of applications [4].

A problem this stage has to deal with is the very wide range of possible I_{PD} values: the photodiode has a declared radiant sensitivity S_{21}=0.85 $\frac{A}{W}$, meaning that, considering a maximum optical power of P_{OUT}^{MAX}=1 mW (0 dBm), I_{PD} can be as high as 850 μA down to 150 nA (dark current). The limited ADC resolution (10 bits) has to be improved in order to discriminate P_{OUT} variations that can be as small as

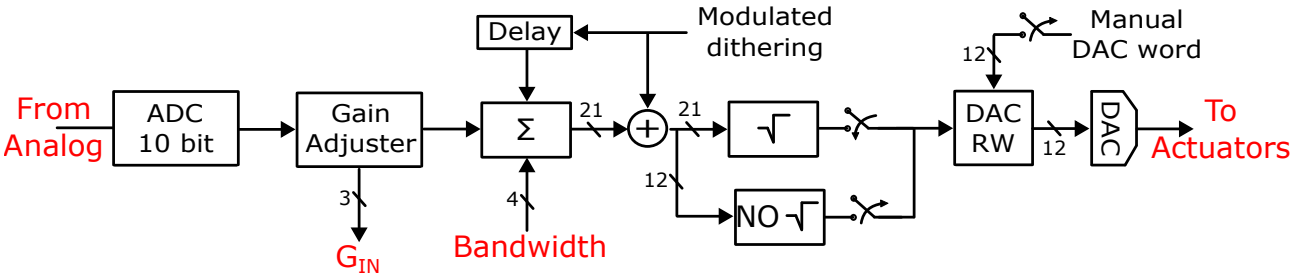

Figure 8: Simplified schematic of the digital chain

-50 dBm. This was done by introducing a variable gain, determined by the values of R_F and R, which are automatically set at digital level. Every time the I_{PD} scales down by a factor 4, G_{IN} is increased by a factor 4 as well, starting from 3.5 kΩ up to 3.58 MΩ, always "mapping" the signal in the [VSS+0.15 V; VDD-0.15 V] range, which corresponds to making a "zoom" on the MZI transfer function. This allowed to improve the resolution from 10 to 20 bits, as it will be shown in sec. 4.

Care was put in sizing the amplifiers, with focus on:

- Noise: the OTAs were designed so as not to add significant noise with respect to the shot noise ($S_I = 2qI_{PD}$) that comes with the signal, for whatever I_{PD}.
- Stability: the system should be stable for whatever values of R_F and R (hence the placement of a compensation capacitance C_C) and for both configurations of the gated integrator (integration and reset).
- Slew rate: the second amplifier bias current should be sufficiently large so as to discharge the output node capacitance (Miller compensation and ADC input) within 0.5 clock cycles (450 ns).

With respect to noise, both input referred voltage noises of the OpAmp are negligible, and the spectral current density injected into C_G is:

$$S_I = \frac{1}{R^2} \cdot (2qI_{PD}R_F^2 + 4kTR_F + 4kTR)$$

In the worst case, accounting also for the switching noise of the reset, the total rms noise on V_{OUT} after each integration is $\sigma_{out} = 475\,\mu V_{rms}$, well below the quantization noise of the ADC.

4. Digital Circuit

Almost all the control system, i.e. the application, extraction and integration of the dithering signal is done at digital level. The main blocks of the system are now reviewed.

First, the 10 bit sample from the ADC is elaborated by a *gain adjuster* that:

- adjusts the gain of the analog stage in case the sample overcomes upper/lower thresholds, externally set.
- adds as many '00' pairs to the left of the sample as the gain of the analog stage: in fact, in order to be coherent with the portion of the MZI transfer function that is represented, a sample should be scaled down by a factor 4 every time G_{IN} is increased by one step. Having a total of 5 transitions (10 additional '0' to be added) from G_1 to G_6, the sample fed to the integrator will be a 20 bit word.

At this point the system splits in two independent and identical paths, each one demodulating the respective dithering signal and driving its own heater. An integrator is the next block, whose functionalities include:

- The demodulation: each dithering signal consists in a square wave which is sampled 12 times. Demodulation and integration happen at the same time: for each sample the information about whether making a sum or a subtraction is also provided, and it is possible to invert this information to change the sign of the feedback and drive the system either towards a minimum or a maximum. It is fundamental that the demodulating signal is properly delayed with respect to the modulating one: that is why a delay block, clocked by the ADC's EoC, is added between the dithering generation and the integrator, where demodulation happens.
- The possibility to reduce the bandwidth. In addition to the 20 bit word determined by the *gain adjuster*, it is possible to shift the

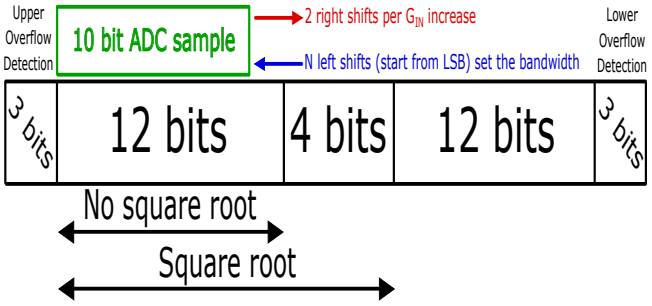

Figure 9: Allocation of the 34-bit digital word elaborated by the integrator

input sample up to an additional 8 bits to the right: the result is a division by a factor 2^N of the weight of the sample and, as a result, of the bandwidth of the system.

- An alternative control algorithm that makes the output of the integrator move whenever no dithering signal is detected and the MZI is not locked to a minimum (i.e. not using G_6), to avoid the system being stuck in a wrong working point.
- A reset mechanism that sets back the working point to a preset value when the integrator gets too close to saturation.

As a consequence, the integrator elaborates a 34 bit wide digital word, that is fed to the following blocks every 12 samples. How each portion of the word is allocated is shown in Fig. 9.
Before reaching the DAC two operations are done:

- Dithering d is superimposed to modulate the working point.
- The 21 bit $C+d$ undergoes the square root operation to produce a 12 bit value to be fed to the DAC. It is also possible to exclude this block and directly feed to the DAC the 12 MSBs of $C+d$.

A number of SIPO and PISO shift registers have also been added respectively to set external parameters (reset thresholds, dithering amplitude, bandwidth...) and to monitor the system (ADC samples, value of G_{IN}, digital word fed to the DAC). Despite being very bulky (one flip-flop per bit is required), most of these parameters are common to all the channels of the chip, making the area occupation more and more irrelevant as the number of channels increases.
As a final option, it is possible, with the *RST* pin, to deactivate the loop and manually set (via the *DAC-RW* block) the voltage of each heater.

5. Conclusions

Scope of the thesis was to design a fully-integrated electronic system for feedback control of a PIC consisting of a mesh of MZIs. This work improves a previous design that already demonstrated the advantages of adopting a CMOS solution with respect to discrete components [5]. The major modification - and improvement - is indeed the massive adoption of digital electronics, that allows to successfully address the ever-growing complexity of PICs, and introduce the largest possible programmability in the control loop: the number of MZIs of the mesh will be increased from 4 to 16, and the closed-loop bandwidth range will be extended and made tunable between few Hz up to 2 kHz.
The following steps will consist in the physical implementation of the chip with the technology AMS C35B4, its characterization, the development of the appropriate control electronics and finally its application in an actual photonic system. It is evident, though, that as the digital approach becomes more and more relevant, the move to a smaller technological node can no longer be postponed: in this chip, >90% of the area is occupied by digital blocks.

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