POLITECNICO DI MILANO

School of Industrial and Information Engineering

Master of Science in Electrical Engineering

Design of a Modular Multilevel Converter Embedded with Battery for Traction Drive Applications

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Abstract

English

The main aim of this thesis is to develop a new kind of converter, a modular multilevel converter (MMC) embedded with batteries, for traction drive applications in order to improve the features of the conventional two-level converter. A small scale prototype of this converter module to power an induction motor is developed. In this converter topology, the battery cells are directly connected to the half-bridge module. Therefore, it is possible to integrate the battery management system , the traction inverter, and the charging power electronics topology within the same converter. In fact, using the state of charge balancing algorithm, each module will converge to the average state of charge of all the batteries, resulting in eliminating battery management system. Depending on the number of modules in an arm, lower voltage and current harmonic distortion are generated. Finally, due to low voltage harmonic distortions and its topology, this converter is able to directly connect to the single phase or three phase AC sockets. Also, it is possible to connect DC charging without any external power electronics.

This report is divided into five main sections.

From the theoretical point of view, the converter working principle and modules balancing algorithms proposed in the literature are discussed in chapter 2. In the next one (chapter 3), the proposed balancing algorithms have been validated using Matlab/Simulink simulations. Also, the effect of real component characteristics on generated load voltages is examined. Furthermore, field oriented control parameters are set to make the motor follow a specific speed profile.

The choice of some main components in the three parts of the PCB design, namely power, measurement, and communication parts, based on the required module board ratings are discussed in chapter 4. The PCB developing process is presented in chapter 5. The power part in the design consists of correctly sending a control signal from the master microcontroller that computes the modules to turn ON to the half-bridge switching components. The measurement part is responsible for measuring the cell voltage and battery voltage and sending this information to the master microcontroller. The communication part responsible for communicating with the modules in the leg is designed. The MMC module PCB schematic and layout are shown.

Finally, in chapter 6, module testing and their troubleshoots have been discussed. The module PCB is able to achieve the maximum current ratings, with power MOSFETs command signals and drain-source voltage ripples safely within the threshold limits. Moreover, the temperatures attained by the PCB devices and tracks are within the datasheet limits. The cell voltages along with battery voltage are read with a maximum error reasonable for the application.

Italian

L'obiettivo principale di questa tesi è quello di sviluppare un nuovo tipo di convertitore, un convertitore modulare multilivello con batterie integrate, per applicazioni di trazione al fine di migliorare le caratteristiche del convertitore convenzionale a due livelli. Viene sviluppato un prototipo su piccola scala di questo modulo di convertitore per alimentare un motore a induzione. In questa topologia del convertitore, le celle della batteria sono direttamente collegate al modulo half-bridge. Pertanto, è possibile integrare il sistema di gestione della batteria (BMS), l'inverter di trazione e la ed il convertitore di ricarica all'interno dello stesso convertitore. Infatti, utilizzando l'algoritmo di bilanciamento dello stato di carica (SoC), ogni modulo convergerà al SoC medio di tutte le batterie, con conseguente eliminazione del BMS. A seconda del numero di moduli in un ramo, si generano tensioni con minore distorsione armonica a parità di valore di prima armonica.. Proprio perché presenta una bassissima distorsione della tensione in uscita, questo convertitore può essere connesso direttamente alle prese CA monofase o trifase. Inoltre, è possibile collegare la ricarica CC senza alcuna elettronica di alimentazione esterna.

La presente tesi è suddivisa in cinque sezioni principali.

Dal punto di vista teorico, il principio di funzionamento del convertitore e gli algoritmi di bilanciamento dello stato di carica proposti in letteratura sono discussi nel capitolo 2. Nel capitolo successivo (capitolo 3), gli algoritmi di bilanciamento proposti sono stati convalidati utilizzando simulazioni Matlab/Simulink. Inoltre, è stato esaminato l'effetto delle caratteristiche dei componenti reali sulle tensioni generate. Inoltre, è stato implementato un algoritmo di controllo ad orientamento di campo (FOC) per far seguire al motore asincrono uno specifico profilo di velocità.

La scelta di alcuni componenti principali nelle tre parti del progetto PCB, vale a dire la potenza, la misurazione e le parti di comunicazione, in base alle valutazioni della scheda MMC richiesta, è discussa nel capitolo 4. Il processo di sviluppo della PCB è presentato nel capitolo 5. La parte di alimentazione nel progetto consiste nell'inviare correttamente un segnale di controllo dal microcontroller master per accendere i componenti dei moduli necessari ad ottnere in uscita il riferimento di tensione. La parte di misura è responsabile della misurazione della tensione delle celle e della tensione della batteria e dell'invio di queste informazioni al microcontrollore

principale. La parte di comunicazione responsabile della comunicazione con i moduli nella gamba è progettata. Vengono visualizzati lo schema e il layout della PCB del modulo MMC.

Infine, nel capitolo 6 sono stati discussi i test dei moduli e i relativi problemi. La PCB del modulo è in grado di condurre la massima correntecontenendo la tensione tra drain e source dei singoli MOSFET entro limiti di sicurezza. Inoltre, le temperature raggiunte dai dispositivi e dalle tracce della PCB rientrano nei limiti della scheda tecnica. Le tensioni delle cell insieme alla tensione della batteria vengono lette con un errore massimo ragionevole per l'applicazione.

1 Introduction

1.1 State of the art

During 20th century, the world population increased from 1.65 billion to 6 billion. The present population is at 7.8 billion (2020), growing at a rate of 1.05% per year and is estimated to be 9.9 billion by the year 2050 [1]. More than half of the global population currently resides in metropolitan areas, and by 2050, it is expected to increase by 75%. So, the number of people driving cars may also increase, with the increase in population in the next 30 years. This implies that the present mobility model is not sustainable even with significant efficiency advancements [2].

In the past few decades, transportation emissions account for more than 24% of global emissions, of which 72% originate from road vehicles. It has been reported in [2] there is an 80% growth in emissions from 1970-2010, which is expected to increase at a faster rate than any other sector. At present, most of the transportation depends on fossil fuel, resulting in two-thirds of the worldwide oil consumption [3]. This demand in oil for transportation is growing at 25% rate every year. Due to inadequate availability of fossil fuels, and lower efficiency of internal combustion engines (ICE) (theoretically between 10-30%), it can be noted that enhancements in ICE are not sufficient to reduce the CO_2 emissions globally. Therefore, the automobile industry started to move gradually from oil-based vehicles to the cleanest, highly efficient, and economic-friendly cars fueled by electricity.

An electric vehicle having higher tank to wheel (TTW) efficiency and less emission of carbon dioxide is capable of reaching 0% emissions if we use renewables for electricity generation. The high TTW efficiency of electric vehicles (EVs) is impacted by the efficiency of the drive train elements. These modern components, such as battery packs, electric motors, and converters used in EV drives, are effective enough to put TTW efficiency at the limit of 60-90%. Higher efficiency is also possible considering the energy from regenerative braking [4]. The critical limitations hindering the electric vehicle’s development are charging complexity, a necessity to have good charging infrastructure, extended battery charging time, and higher costs.

1.2 Trends in electric mobility

A battery driven electric vehicle (EV) power conversion system contains a battery pack supplying a traditional two-level inverter [5], [6]. A large number of low voltage electrochemical cells are connected in series in a battery pack to obtain the voltage requirement of the inverter -link. Despite its simplicity in power electronics applications, this solution has several drawbacks. In this battery pack, the series connection suggests that all battery cells have the same current. Due to the differences in leakage currents, internal impedances, charge storage volumes, and chemical characteristics, voltage imbalance appears between the cells when the battery is charged or discharged several times. This result in gradual damage and premature failure of battery cell [7]. Therefore, to balance the battery cell, a battery management system (BMS) is usually added to the battery pack [7]. However, the added BMS consumes battery energy, decreasing the conversion efficiency and the vehicle range. Furthermore, an additional built-in charger is required to recharge the battery pack.

1.3 Review of BMS

This section reviews the BMS available in the technical studies. The most important parameter required by the BMS is the state of charge (SoC) of the cells, which is a good indicator of the current state of the battery [8]. The two categories of charge equalizing techniques used in BMS are passive BMS and active BMS [9], [10], [11], [12]:

- In passive BMS, external resistors are used to dissipate the excess energy from higher SoC cells until their SoCs match with the lower SoC. The resistors used in this BMS can be either fixed in value [9], [10] or switched values [9]–[13].
- In active BMS, excess energy is transferred from the higher SoC cells to the lower SoC cells. Its topologies use different active elements as a buffer for the energy transfer between the cells, i.e., capacitors, inductors or transformers, as well as different controlled switches or converters [9], [14], [15], [12].

In the next section, a brief description of these BMSs is provided.

1.3.1 Passive BMS

Passive BMS are cheap and simple to implement. They use a smaller number of components with respect to the active BMS. Since all the excess energy is dissipated across the balancing resistors, these BMS have a slow equalization rate and low efficiency. By using bypass shunt

resistors, they dissipate the excess energy from the higher voltage cells connected in parallel to each battery cell. They are divided into fixed shunt resistor (FSR) and switched shunt resistor (SSR) methods, as shown in *Figure 1.1* and *Figure 1.2*. These methods can be used for low power applications with a balancing current smaller than 10mA/Ah as recommended in [11] to limit the energy dissipated across the shunt resistors. The circuits for FSR and SSR are shown below.

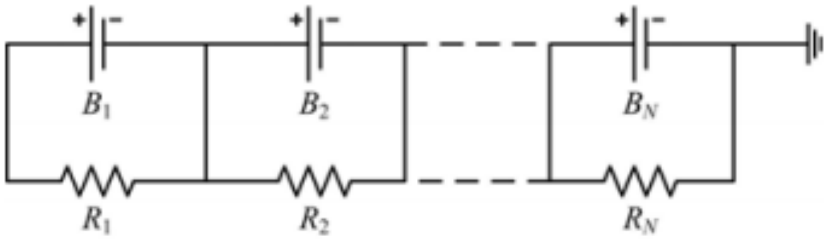

Figure 1.1 Circuit diagram for FSR method

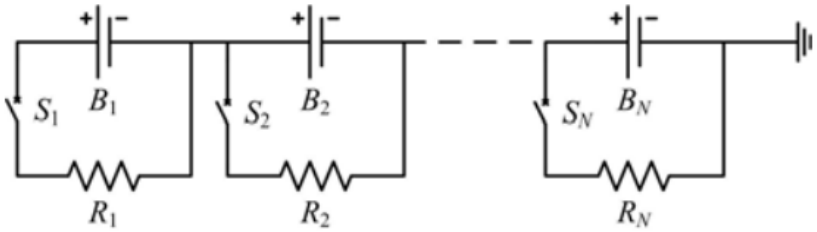

Figure 1.2 Circuit diagram for SSR method

The main drawback of passive BMS is that it requires a thermal management system (TMS) as excess energy is converted into heat. Another disadvantage is that when passive BMSs are applied during the discharge, the battery discharge time is reduced compared to active methods [17].

1.3.2 Active BMS

Active BMS offers a faster balancing rate and a higher efficiency when compared to passive BMS. They are divided into capacitor-based BMS, inductor or transformer-based BMS, and converter-based BMS.

- In capacitor based BMS, capacitors are used as an external storage device to transfer energy among battery cells. They work for both charging and discharging operations.

- In inductor based BMS, inductors or transformers are used to transfer energy from a cell to another cell in order to achieve balancing. A shorter balancing time can be achieved as these methods offer a balancing current higher than that based on capacitors,
- In converter based BMS, power converters are used to balance the cells in a battery. They feature a fully controlled balancing process. However, the resulting BMS has relatively high cost and complexity [11], [16]–[20]

The active BMS drawbacks are the higher cost and losses. Furthermore, this BMS may require high switching frequency operation to reduce the inductor or transformer size. Along with that frequency operation and to achieve fast equalising speed, extra capacitors should be added across each battery cell to filter high frequency current harmonics [9].

1.4 Review of traditional inverter

The most common topology used for traction motors is a two-level inverter. With this inverter, the ac line voltage is pulsed in nature with a magnitude of *+Vdc, 0, -Vdc*, as shown in *Figure 1.6*, resulting in the occurrence of higher harmonics. Therefore, total harmonic distortion (THD) is high, which results in a reduction of motor efficiency and performance. Furthermore, harmonics in current produce torque ripples in the motor. They can be reduced by using a filter which adds extra space and weight to the inverter.

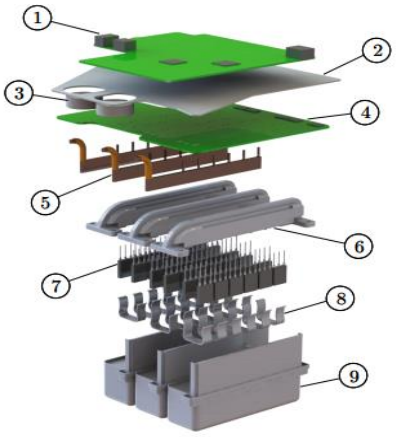

Figure 1.3 Tesla Model S inverter components 1) Control board 2) Aluminum shield 3) Current sensor 4) Gate driver board 5) Busbar 6) Heat sinks 7) IGBT 8) IGBT clips 9) DC-link capacitors

Figure 1.4 Tesla Model S rear drive unit inverter

Taking an example of the tesla model S, which consists of a single inverter with total power ratings of 193 kVA and a power density of 30.1 kVA/L with a specific power of 33.3 kVA/kg.

Tesla model S has a range of 426 km, and its battery pack size is 85kWh, and it has electric motors on both the rear and front wheels. Model S inverter shown in *Figure 1.3* contains, control board is on the top. Below the board, there is the gate driver board. In between these boards, a stamped metal shield containing a plastic cover with silica gel is present. Underneath the gate driver board, there are busbars followed by transistors and the bottom DC-link capacitors. Here hall-effect sensor of soft ferromagnetic rings are kept in phase with the cables so that they sense current. Instead of using power modules, Tesla used parallel discrete package ICs for essential current ratings. Each leg consists of two switches, and each switch consists of 6 parallel IGBTs where a total of 36 IGBTs are welded to the busbar. In addition, these are soldered to reach the gate driver board. Here AC busbars are parallel, and DC busbars are perpendicular to the transistors. A coolant is used to lower the heat in the drive unit. This is split into three different heatsinks in which six transistors are fixed with clips to dissipate the heat of the transistor. Finally, below the transistor stage, the DC-link capacitors are present with a planar terminal connection to the DC busbars [21].

The major drawbacks of a two-level inverter are:

- High harmonic content of the current
- High switching losses
- Necessity of an additional BMS for the battery pack

1.5 Modular Multilevel Converter

Since the standard two-level three-phase inverter has higher harmonic distortion in voltage and current, it will produce torque ripples in the motor that leads to mechanical vibrations and faster wear and tear of the motor. Therefore, a new type of DC-AC converter for electric vehicles has been studied. The modular multilevel converter (MMC) has been proposed by Lesnicar and Marquardt [22] for high power generation and transmission applications, primarily for HVDC applications. At present, it is extended to various applications such as railways, wind power conversion systems, and integrated PV systems. It is also used in motor drive applications because it is able to improve the performance and efficiency of the system.

The load voltage waveforms of two different inverters are reported below in *Figure 1.5* and *Figure 1.6.*

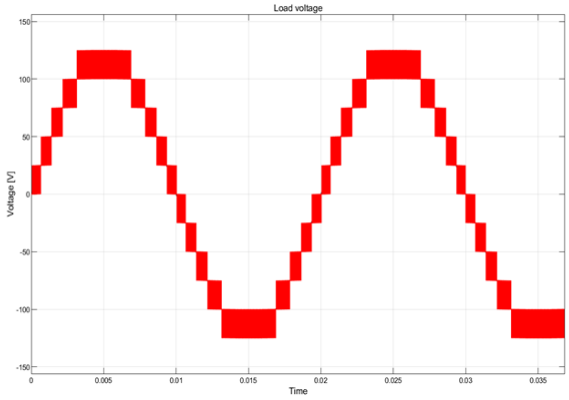

Figure 1.5 Load voltage of MMC with PD-PWM

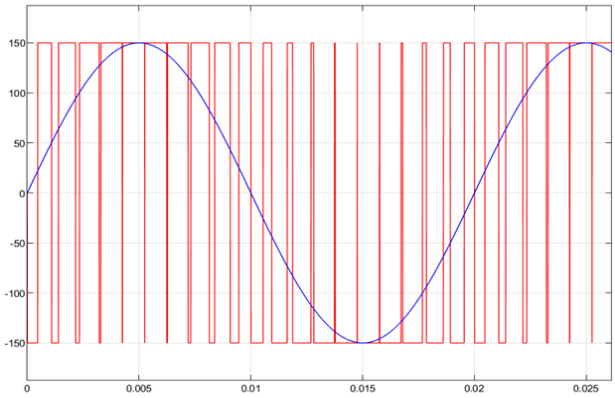

Figure 1.6 Load voltage of 2-Level converter with bipolar SPWM

Referring to *Figure 1.5*, by using modular multilevel converters, the harmonics in current can be reduced and produce the approximate sinusoidal voltage with very low total harmonic distortion, resulting in a reduction of the filter size at output; it is also possible to obtain high pulse width modulation (PWM) frequency output by using low PWM modulation for each staircase voltage [23].

A general view of a converter with double star chopper cell configuration is shown in *Figure 1.7.*

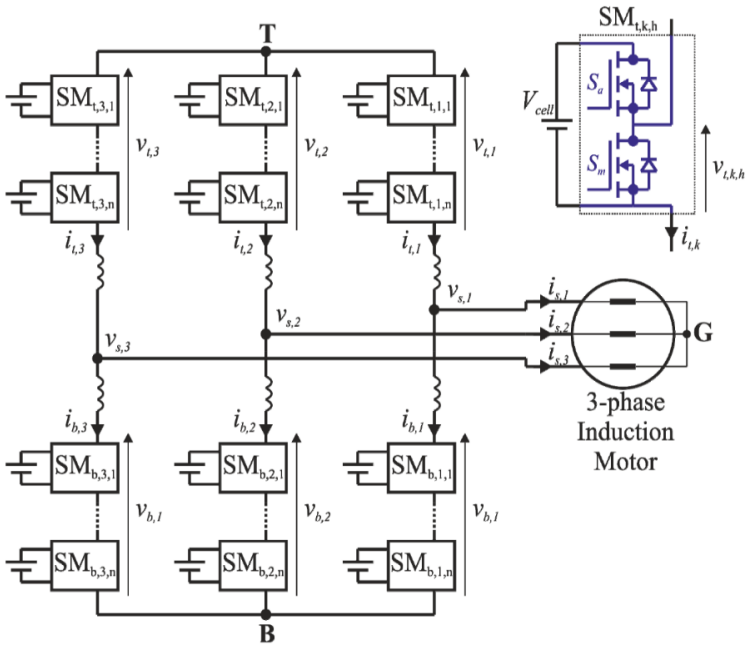

Figure 1.7 Double star chopper cell converter topology

The power converter is created by equal modules, connected in series to reach the desired voltage, and arranged in parallel to obtain the desired number of phases. The battery, intended as the complex of all the cells, is not anymore in a single package (or in few packages), but the cells are spread in the modules of the converter. Every module contains some cells of the battery (e.g., 14 in our prototype) connected in series, while the number of parallel cells depends on the current required by the load.

At present, in the automation industry, all the battery electric vehicles (BEVs) contain several individual converters for onboard charging and inverter to deliver voltage and frequency to the motor drive, as shown in *Figure 1.8*. As we discussed earlier, different cells in the battery pack are connected in series and parallel to obtain desired power rating. Due to the chemical properties of each cell in the battery, these cells will not be identical as they may result in different leakage currents leading to unequal or inhomogeneous distribution of voltages. Therefore, the state of charge and temperature in each cell is different. To sustain the equal state of charge in each cell, a battery management system is required [6].

In the family of modular multilevel converters, a double star chopper cell (DSCC) converter can be used for battery electric vehicles since it can handle the functions of a traction inverter, battery charger, and battery management system shown in *Figure 1.8 and Figure 1.9*. All the multilevel converters, such as single-delta bridge cell (SDBC), single-star bridge cell (SSBC), and the cascaded H-bridge (CHB), will also allow the integration of both traction inverter and battery management system by controlling the power supplied by individual modules. However, the double star chopper cell is selected, which offers higher freedom than SDBC, SSBC, CHB configurations because cell balancing can be completed using direct, inverse, and zero sequences of the circulating current. An additional advantage of using a DSCC is, it can be connected directly to the external DC bus for charging the system [13].

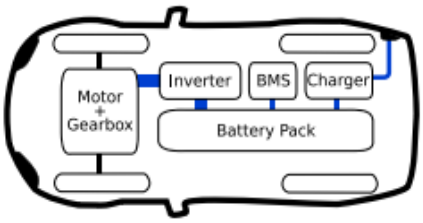

Figure 1.8 Typical battery electric vehicle power train

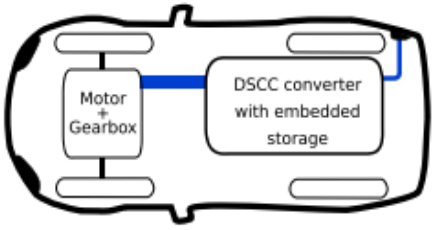

Figure 1.9 Battery electric vehicle with DSCC-MMC

This double star chopper cell converter can be connected directly to three phase or single phase AC sockets without using additional power electronic devices and large filters. Here the converter logic algorithm will adjust to the existing power source with a power factor close to unity. If this converter is used in battery electric vehicles, high overall efficiency is achieved when compared with traditional two-level inverter as this single converter can be used for different tasks like BMS, traction inverter, and battery charging. In addition, rapid charging is permitted without using additional hardware since it can work with rated power even at charging operations. Here cell balance is achieved using load current instead of the energy transfer between the cells. By using new modulation techniques, efficiency can be further increased to reduce THD in current. This THD is a significant concern in the automated industry because when THD increases, losses will also increase, generating torque ripples that may lead to mechanical vibrations in the motor.

Furthermore, the modular multilevel converter has several advantages, such as

i. Modular construction i.e., each arm in MMC contains many identical low voltage rating submodules which can be easily modified to obtain different voltage and power levels.
ii. Multilevel waveform i.e., modules in each arm can be increased to produce output voltage with an approximately sinusoidal waveform.
iii. High reliability i.e., if there is any damage in a module or its components, we can bypass the desired module and continue to operate without much impact on the converter functionality.

1.6 Thesis Overview

The main objective of this thesis is to build a prototype of this converter type to drive an induction motor. The initial part of this report is dedicated to the explanation from theoretical point of view, working principle of the converter, mathematical modeling of the converter, and the SoC balancing algorithms proposed in the literature.

Later, Matlab/Simulink simulations are performed in order to validate the balancing algorithm and to establish the parameters of a field-oriented control (FOC) to make the motor follow a certain speed profile. Here the simulations use a detailed hardware model for the modules. These modules are triggered with a pulse width modulation technique in order to verify the balancing algorithm. When the motor is operating, the FOC parameters are validated with the

SoC balancing. After the simulation's validation, the dimensioning of the main components mounted in the module hardware is discussed.

Then, the module PCB designing process is explained. The design of PCB has divided into three sections: one section is responsible for the power part, which consists of properly sending the PWM signal from the master microcontroller(µC)[1] to the half-bridge, the next one is responsible for the measurement part, which measures the individual cell voltages along with the battery voltage and sends them to the master microcontroller. The last section is the communication part, which is used to communicate with all the modules in a leg using a single measurement controller[2] in order to measure the voltages in a daisy-chain connection. These PCB sections provide electrical insulation between the battery and the master microcontroller to avoid dangerous parasitic currents.

Finally, the module testing and their troubleshoots have been discussed. The module PCB is able to achieve the maximum current rating of 50 A, with power MOSFETs command signals *Vgs* and *Vds* ripples that safely accomplish the limits. Moreover, the temperatures attained by the PCB devices and tracks are within the datasheet limits. The cell voltages along with battery voltage are read with a maximum error reasonable for the application.

[1] From now on, we will refer to the master microcontroller as the one that, after computation of the FOC, and a balancing algorithms, sends the proper ON/OFF signals to the modules.

[2] Measurement controller refers to the one responsible for communicating with battery management chip.

2 Modular Multilevel Converter

2.1 Topology

The schematic shown in *Figure 2.1* is the double star chopper cell in the family of modular multilevel converter for traction drive applications. The drive selected is a three-phase induction motor drive that generates an approximately sinusoidal waveform from the DC source. This converter layout is very similar to the traditional modular multilevel converter except that, the capacitor, usually present in the submodules, is replaced by a battery unit. Managing the power exchanged by each module, this converter is capable, is capable to perform as a battery management system. To generate a three-phase signal, three legs are required, as shown in the color pink in *Figure 2.1*. By looking at the MMC, it is inferred that the N number of submodules, as shown in *Figure 2.1* with green color are connected in series to reach the desired voltage level. These submodules are half-bridge converters and are combined to form a converter arm. Each phase contains two arms, namely upper and lower, as shown in *Figure 2.1* with yellow color. Here the inductor present in each arm is called as an arm inductor. Its main function is to limit the circulating current in each leg, used for module SoC balancing. Instead of a normal inductor, a mutually coupled inductor is used to reduce the converter weight and voltage drop at the output.

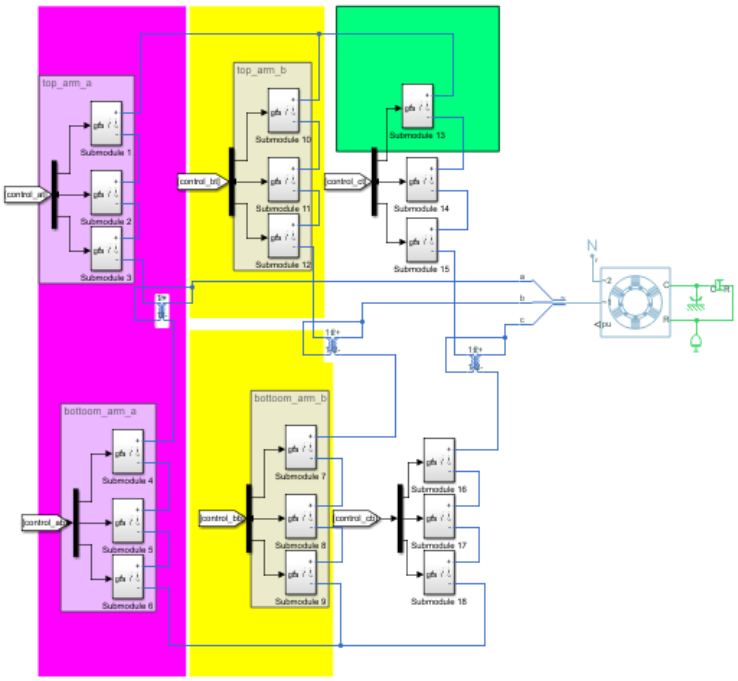

Figure 2.1 MMC topology

Each module consists of a bidirectional half-bridge converter and a battery as shown *Figure 2.2*. Here half-bridge is selected as it contains only two semiconductor switches. In our case, MOSFETs are used to reduce forward voltage drop and switching losses [24]. The latest advancement in MOSFETs show that they have significantly low on-state resistance and gate capacitances. Therefore, they are more suitable than IGBTs when the module voltage is low.

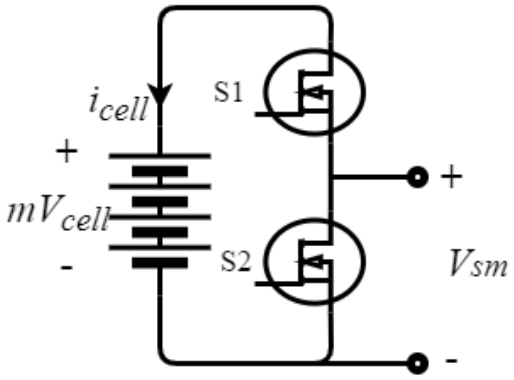

Figure 2.2 Half-bridge submodule topology

Each half-bridge sub module, *Figure 2.2,* includes a battery which is the combination of *m* different independent cells connected in series to reach the desired voltage. The half-bridge sub-module can operate in two modes, namely insertion mode and bypassed mode. When a high command is given to the upper transistor, i.e., *S1=ON* and *S2=OFF*, then the voltage across the submodule is $m * V_{cell}$ (insertion mode). Similarly, when a low command is given to the lower transistor *S2=ON* and *S1=OFF*, then the voltage across the submodule is 0 (bypassed mode). Both these modes will have conduction losses since current flows through one of the transistors.

The required number of modules per arm depends on the needed maximum voltage on a single arm, the nominal voltage of the cells (*Vcell*), and the number of series cells in each module. For example, to have the possibility to generate the nominal phase to phase voltage in a motor, it is necessary to have:

$$Vdc_{bus}{}^{3} \geq 2 * \frac{V_n}{\sqrt{3}} * \sqrt{2} \tag{2.1}$$

where Vdc_{bus} is the voltage between positive and negative busbars and V_n is the motor nominal voltage. Equation (2.1), written in terms of cell voltages, is:

[3] Vdc_{bus} is defined as voltage between positive and negative bus bar.

$$Vdc_{bus} \geq mV_{cell} * N \tag{2.2}$$

where N is the number of submodules per arm. From the above two equations, if we choose a number of modules per arm based on the required harmonic distortion reduction in load voltage and available I/O ports of the microcontroller, then the number of cells required per module are determined.

2.2 Circuit Analysis

To analyze the circuit, half-bridge variant of MMC with a single phase is considered, *Figure 2.3*. Each arm is modelled as a controlled voltage source since the voltage produced by each arm depends on the gate signal provided by the control algorithm. Both the upper and lower arms are controlled in a complementary way so that the voltage across the DC side is constant.

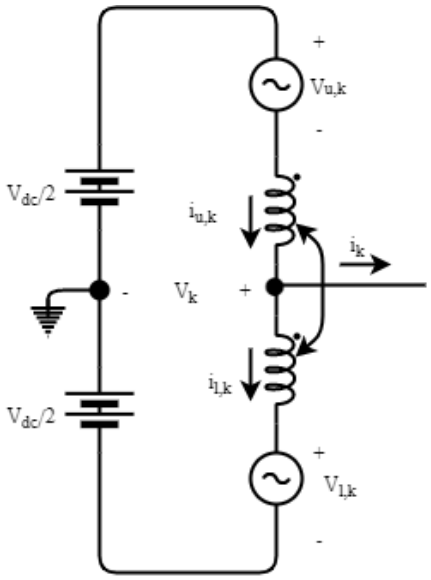

Figure 2.3 Equivalent circuit of the phase

To produce the reference phase voltage, the upper and lower arm references are obtained by applying Kirchhoff's voltage law for *Figure 2.3.*

$$\begin{aligned} V_{u,k} &= \frac{V_{dcbus}}{2} - L\frac{di_{uk}}{dt} - v_k \\ V_{l,k} &= \frac{V_{dcbus}}{2} - L\frac{di_{lk}}{dt} + v_k \end{aligned} \tag{2.3}$$

where $V_{u,k}$ is the upper arm reference, and $V_{l,k}$ is the lower arm reference, and v_k is the reference phase voltage, *k=a, b, c* indicates the generic phase and $i_{uk}, and\ i_{lk}$ are the upper and lower arm currents, respectively.

The upper and lower arm currents in generic leg *k* can be written as:

$$\begin{aligned} i_{uk} &= \frac{i_k}{2} + i_{cir} \\ i_{lk} &= -\frac{i_k}{2} + i_{cir} \end{aligned} \tag{2.4}$$

where i_{cir} is the circulating current, i_k is the generic phase current. If we consider the steady-state condition of the MMC. i.e., after all the modules are converged to the average $\overline{SoC}$, the circulating current flowing between the arms and legs is negligible. Therefore (2.4) can be written as

$$\begin{cases} i_{u,k} = \frac{i_k}{2} \\ i_{l,k} = -\frac{i_k}{2} \end{cases} \tag{2.5}$$

Inserting (2.5) in (2.3) results:

$$\begin{cases} V^*_{u,k} = \frac{Vdc_{bus}}{2} - v_k \\ V^*_{l,k} = \frac{Vdc_{bus}}{2} + v_k \end{cases} \tag{2.6}$$

By adding the upper and lower arm, we will obtain the DC bus voltage:

$$V_{u,k} + V_{l,k} = Vdc_{bus} \tag{2.7}$$

Assuming ac side load current and voltage as sinusoidal, then equations for $phase\ k$ are:

$$v_k = V_k \cos \omega t \tag{2.8}$$

$$i_k = I_k \cos(\omega t + \varphi) \tag{2.9}$$

where φ is phase angle of the current and ω is the fundamental angular frequency.

In traction drive applications, it is necessary to change the voltage for motor control with variable voltage and frequency. To change the output phase voltage v_k, the upper and lower arm reference voltages are altered. Therefore, substituting (2.8) in (2.6), we get:

$$\begin{cases} V^*_{u,k} = \frac{Vdc}{2}(1 - q\cos\omega t) \\ V^*_{l,k} = \frac{Vdc}{2}(1 + q\cos\omega t) \end{cases} \quad 0 \le q \le 1 \tag{2.10}$$

where $q = \frac{V_k}{\frac{Vdc}{2}}$ is the modulation index varying from 0 to 1.

The output load voltage reference can be calculated from (2.6) as:

$$V_k = \frac{V_l^*{}_{,k} - V_u^*{}_{,k}}{2} \tag{2.11}$$

To generate reference voltage for each arm, different modulation techniques can be used.

2.3 Modulation techniques

There are many modulation techniques available for MMC converter. In this section, only two modulation techniques have been discussed. They are nearest level control (NLC) and pulse width modulation techniques. Both the techniques have their own advantages and disadvantages. NLC has low switching losses with more total harmonic distortion, whereas PWM techniques have low THD, but switching losses are high. In the below sections, a detailed description of these techniques is given.

2.3.1 NLC

A modular multilevel converter has N submodules per arm and 2N submodules per phase. Therefore, we require 2N constant carriers for module switching, as shown in *Figure 2.4*. If we consider $\overline{V_b}$ as the average battery voltage of modules, the error in phase voltage is defined as the difference between a reference voltage ($V_{ref,phase,k}$) and actual voltage ($V_{phase,k}$) [25]. From this error (2.12), we can decide to turn ON N^{th} module or $(N-1)^{th}$ module.

$$error_v = V_{ref,phase,k} - V_{phase,k} \tag{2.12}$$

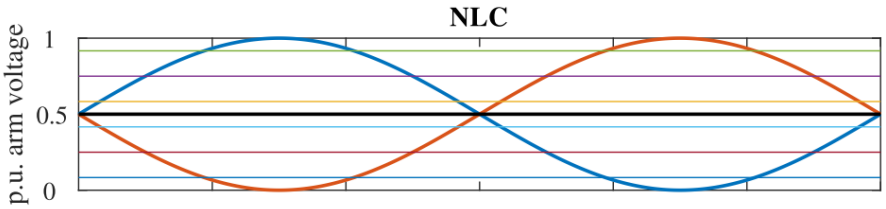

Figure 2.4 Nearest level control

If the error is less than the threshold voltage, $(N-1)^{th}$ module is turned ON, whereas if the error is greater than the threshold voltage, N^{th} module is turned ON. Here the threshold voltage can be calculated as,

$$v_{th}(N) = (N-1) * \overline{V_b} + \frac{1}{2}\overline{V_b} \tag{2.13}$$

The discretizing error generated from the difference in reference and actual value has significant effect on the DC bus, which leads to flow of circulating currents between the arms. Since these currents are limited by arm inductors, they are especially high at low frequencies. Therefore, pulse width modulation technique is preferred.

2.3.2 Pulse width Modulation

In this section, only five PWM techniques are discussed. Namely, phase shifted carrier PWM (PSC-PWM), phase disposition PWM (PD-PWM), phase opposition disposition PWM (POD-PWM), alternating phase opposition disposition PWM (APOD-PWM), and last level PWM (LLPWM)

2.3.2.1 PSC-PWM

It is an extensive version of the typical sinusoidal PWM technique. With this phase shift carrier PWM, semiconductor stresses of all the modules are evenly distributed as all the modules are switched in each carrier period, which can be seen in *Figure 2.5*. This PWM technique can generate N+1 levels of output phase voltages with N submodules per arm [26]–[29].

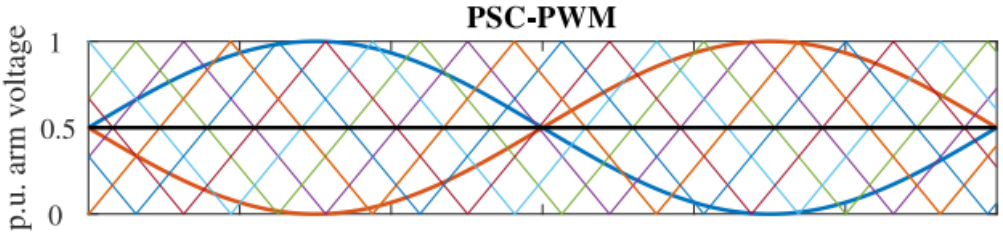

Figure 2.5 Phase shift carrier pulse width modulation

If a modular multilevel converter consists of N submodules per arm to apply phase shift carrier PWM, we need 2N triangular carriers and each carrier is shifted by (2π/N).

Hence the phase angle $\theta_{l(j)}$ of the j^{th} carrier in the lower arm is given by:

$$\theta_{l(j)} = \frac{2\pi}{N} \times (j-1). \tag{2.14}$$

And for the upper j^{th} arm carrier is given by

$$\theta_{u(j)} = \theta + \frac{2\pi}{N} \times (j-1) \tag{2.15}$$

where θ is the phase angle displacement of each carrier signal.

2.3.2.2 PD-PWM

In this modulation technique, as shown in *Figure 2.6,* all the triangular carrier signals are in phase with each other [26]. For each module, there will be one carrier signal whose magnitude is equal to the module voltage. The reference signal for the arms is generated as below.

$$\begin{cases} pwm_l = \frac{V_l^*{}_{,k} - V_{l,k}}{V_{mod,l,k,n}}; \\ pwm_u = \frac{V_u^*{}_{,k} - V_{u,k}}{V_{mod,u,k,n}}; \end{cases} \tag{2.16}$$

where $V_{mod,l,k,n}$ and $V_{mod,u,k,n}$ are the voltages for the selected module. $V_l^*{}_{,k}$ and $V^*{}_{,u,k}$ are the upper and lower arm reference voltages, $V_{l,k}$ and $V_{u,k}$ are the instantaneous upper and lower arm voltages, pwm_l and pwm_u are gate signals which can be either 0 or 1 produced by comparing the actual voltage with a triangular carrier signal.

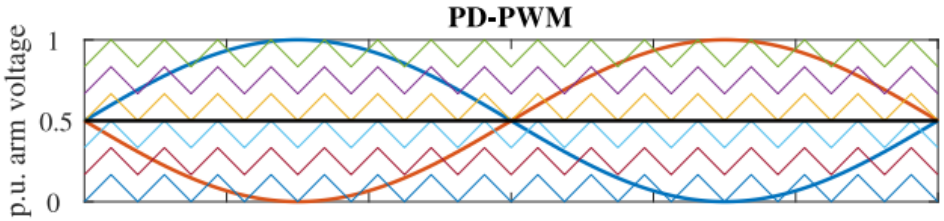

Figure 2.6 Phase disposition pulse width modulation

While using this modulation technique, a sorting algorithm is mandatory since the lower module responsible for lower carrier signals stays in activation mode for a long time. Then it results in fast discharge of the respective module, creating unbalance in their voltages. Using this modulation technique, we can achieve 2N+1 levels on the output phase.

2.3.2.3 POD-PWM

The POD-PWM shown in *Figure 2.7* is based on the same principle of phase disposition pulse width modulation. In this modulation technique, the upper arm carriers are in phase with each other. Similarly, the lower arm carriers are also in phase with each other. But both these carriers are 180 degrees (half period) shifted from each other. Using a sorting algorithm with this technique, circulating currents that flow internally are minimized by generating output phase voltage of N+1 level. With this technique, the total number of active modules are always equal and independent of the modulation index [30].

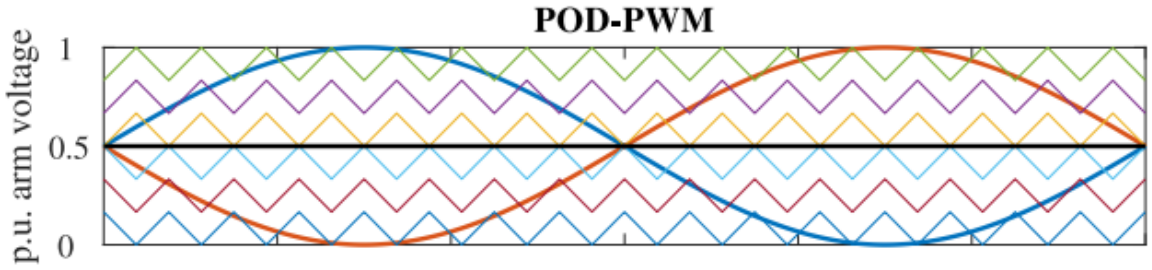

Figure 2.7 Phase opposition disposition pulse width modulation

2.3.2.4 APOD-PWM

As the name suggests, this modulation technique is also based on the same principle of POD-PWM. Here every triangular phase is 180 degrees shifted with the other. With this, voltage ripples across the DC bus are considered negligible. Then N+1 levels of output phase voltage can be achieved [31].

2.3.2.5 LLPWM

The last level modulation technique is to apply modulation only for upper or lower modules representing maximum and minimum values of the phase voltage. The discussed modulation techniques in the previous sections have high commutation losses since each module will have commutation to get the desired voltage. But with the last level modulation technique, the desired output with lower commutation losses without affecting too much output distortion is obtained. This technique is shown in *Figure 2.8.*

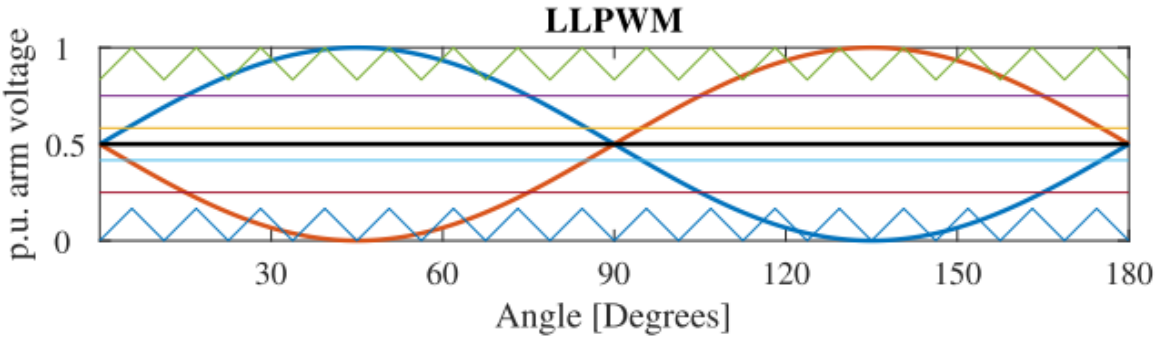

Figure 2.8 Last level pulse width modulation

The reference for upper and lower arms are determined as:

$$\begin{cases} V_{u,k}^{*} = \dfrac{Vdc_{bus}}{2} - V_{phase,k,max} \\ V_{l,k}^{*} = \dfrac{Vdc_{bus}}{2} + V_{phase,k,max} \end{cases} \tag{2.17}$$

where $V_{phase,k,max}$ is the maximum phase voltage of the load that the converter generates. All the other submodules are controlled using nearest level control to reduce the switching losses. The modules responsible for PWM gives the maximum and minimum values of the peaks for the sinusoidal signal [31].

2.4 Balancing Process

The state of charge for each module will not be equal due to an unavoidable difference in leakage currents. This will introduce circulating current flowing in the arm. Also, characteristics of battery like aging, charging rate, and discharging rate of the battery cells are affected, resulting in premature failure of the cells. To prevent this, the battery management system is necessary to keep battery voltage between the modules constant. If we configure MMC with DSCC and a battery in each module, balancing is attained with module sorting algorithm and circulating current without using external BMS. However, balancing inside module cells is not possible by this method [32].

Usually, such MMC integration consists of three balancing processes, namely:

1. Balancing among the modules of each arm (Module balancing).
2. Balancing upper and lower arms of each leg (Arm balancing).
3. Leg balancing.

All these balancing techniques are achieved by using the SoC of each module.

2.4.1 Module balancing

In module balancing, a sorting algorithm is used with reference to the SoC of each module and its current direction. If the arm current is positive (charging the battery), then all the modules in an arm will be activated in ascending order. That implies the module with lower SoC will be activated first for charging and will remain in a charging state for a longer time when compared to other modules of the same arm. Similarly, when the arm current is negative (discharging the battery), the modules in the arm will be activated in descending order i.e., the module with higher SoC will be connected and will remain in discharging state for a longer time. In this way, the SoC of all modules in the upper and lower arms will converge to their average SoC, $\overline{SoC_{u,k}}$ and $\overline{SoC_{l,k}}$, respectively[33].

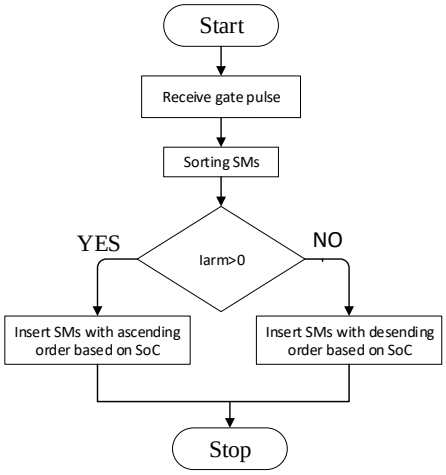

Figure 2.9 Flow chart for sorting algorithm

2.4.2 Arm and leg balancing

For achieving arm and leg balance, we need to control circulating currents flowing through each leg. In modular multilevel converter with double star chopper cell, it is possible to control the flow of currents in modules without affecting the load current.

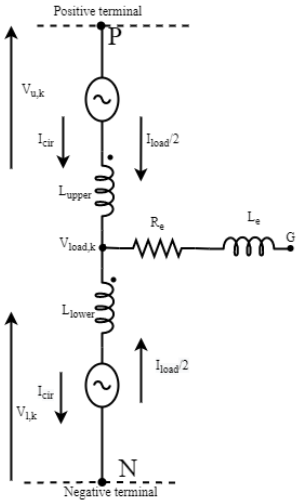

Figure 2.10 Load and circulating currents equivalent circuit.

The upper and lower arm currents of the generic phase *k* can be defined using *Figure 2.10*.

If we consider the current positive when flowing from the positive to negative terminal of the DC bus, it is:

$$\begin{cases} i_{u,k} = i_{cir,k} + \dfrac{i_{load}}{2}; \\ i_{l,k} = i_{cir,k} - \dfrac{i_{load}}{2}; \end{cases} \tag{2.18}$$

From the above equation, the circulating current and load current can be expressed as:

$$\begin{cases} i_{cir,k} = \dfrac{i_{u,k} + i_{l,k}}{2} \\ i_{load,k} = i_{u,k} - i_{l,k} \end{cases} \tag{2.19}$$

The upper and lower arm of the same leg are controlled in a complementary way, so that the number of active submodules in a leg is constant and it is equal to N. Then the instantaneous power of the lower and upper arm can be defined from the product of arm voltage and arm current. It is:

$$\begin{cases} p_{u,k} = v_{u,k}\, i_{u,k} = NQ_{max}V_{mod}\dfrac{d\overline{SoC}_{u,k}}{dt} = \left(\dfrac{NV_{mod}}{2} - v_{load,k} - L\dfrac{di_{u,k}}{dt}\right) i_{u,k} \\ p_{l,k} = v_{l,k}\, i_{l,k} = NQ_{max}V_{mod}\dfrac{d\overline{SoC}_{l,k}}{dt} = \left(\dfrac{NV_{mod}}{2} + v_{load,k} - L\dfrac{di_{l,k}}{dt}\right) i_{l,k} \end{cases} \tag{2.20}$$

Assuming load current and voltage to be sinusoidal, at steady state, circulating current will be low resulting in a negligible voltage drop across the arm inductance. Neglecting the alternating term, the sum and difference of the power can be expressed as

$$\begin{aligned} p_{diff,k} = p_{u,k} - p_{l,k} &= NQ_{max}V_{mod}\frac{d(\overline{SoC}_{u,k} - \overline{SoC}_{l,k})}{dt} \\ &\cong -V_{load,k}\, I_{cir,1,k}\cos\theta_1 \\ p_{sum,k} = p_{u,k} + p_{l,k} &= NQ_{max}V_{mod}\frac{d(\overline{SoC}_{u,k} + \overline{SoC}_{l,k})}{dt} \\ &\cong NV_{mod}I_{cir,dc,k} - V_{load,k}\, I_{load,k}\cos\varphi_1 \end{aligned} \tag{2.21}$$

where $I_{cir,dc,k}$ is the DC component of the circulating currents and $I_{cir,1,k}$ is the fundamental harmonic component of circulating current with phase angle θ_1 with respect to the load voltage phasor, $I_{load,k}$ is the load current with phase angle φ_1 with respect to load voltage phasor, and $V_{load,k}$ is the load voltage.

From the equation (2.21), it is observed that the sum of power can be controlled by using the DC component of the circulating current i.e., each leg SoC can be controlled by generating proper DC component circulating current reference. Also, the power difference between arms can be controlled by using the fundamental component of the circulating current. i.e., arm balancing can be achieved by proper reference of the first harmonic component of circulating current.

Therefore, by producing proper circulating current reference of DC and fundamental components for each leg, battery management system is obtained. A fundamental component of circulating current is produced by controlling SoC in such a way that the difference between

two arm average SoC is zero. i.e., ($\overline{SoC}_{u,k}$-$\overline{SoC}_{l,k}$) =0. While to produce DC component of circulating reference, we will control the average SoC of each leg $\overline{SoC}_k = \overline{SoC}_{u,k} + \overline{SoC}_{l,k}$. This is equal to the average SoC of all legs $\overline{SoC} = \frac{(\overline{SoC}_1+\overline{SoC}_2+\overline{SoC}_3)}{3}$. The resultant three-phase circulating current consists of both direct and inverse sequence components at fundamental frequency since each leg currents depends on their actual SoCs. Here the DC component of the circulating current will be different for each phase [34].

2.4.3 Definitions

The definitions of balancing process to find circulating current reference are discussed.

The sum and difference in voltages of upper and lower arms referring to the generic leg *k* of MMC in above *Figure 2.10* can be defined as

$$\begin{aligned} v_{+,k} &= v_{u,k} + v_{l,k} \\ v_{-,k} &= v_{u,k} - v_{l,k} \end{aligned} \tag{2.22}$$

Similarly, the sum and difference in arm power can be defined as

$$\begin{aligned} P_{+,dc,k} &= P_{dc,u,k} + P_{dc,u,k} = v_{u,k}\, i_{u,k} + v_{l,k}\, i_{l,k} \\ P_{-,dc,k} &= P_{dc,u,k} - P_{dc,l,k} = v_{u,k}\, i_{u,k} - v_{l,k}\, i_{l,k} \end{aligned} \tag{2.23}$$

The generic three-phase quantity x_k's zero sequence and space vector can be defined as

$$\boldsymbol{x} = \frac{2}{3}\left(x_1 + x_2 e^{j\frac{2\pi}{3}} + x_3 e^{j\frac{4\pi}{3}}\right); \quad x_0 = \frac{(x_1 + x_2 + x_3)}{3} \tag{2.24}$$

From the zero-sequence and space vector components of two generic three-phase quantities x_k and y_k , other zero-sequence and space vector components are found by product of these two quantities, hence $z_k = x_k y_k$ defined as

$$z_k = x_k y_k \rightarrow \begin{cases} \boldsymbol{z} = \frac{1}{2}(\hat{\boldsymbol{x}}\hat{\boldsymbol{y}}) + y_0\boldsymbol{x} + x_0\boldsymbol{y} \\ z_0 = \frac{1}{2} Re\{\boldsymbol{x}\hat{\boldsymbol{y}}\} + x_0 y_0 \end{cases} \tag{2.25}$$

where $\boldsymbol{x}$ and $\hat{\boldsymbol{x}}$ represents generic space vector and its complex conjugate.

2.4.4 Voltage balance

With reference to the MMC of *Figure 2.10*[4], the Kirchhoff's voltage laws applied to the generic leg *k* yields:

$$\begin{cases} v_{P,N} = v_{u,k} + v_{l,k} + L\dfrac{di_{u,k}}{dt} + L\dfrac{di_{l,k}}{dt} \\ v_{P,G} + v_{B,G} = v_{u,k} - v_{l,k} + L\dfrac{di_{u,k}}{dt} - L\dfrac{di_{l,k}}{dt} + 2v_{load,k} \end{cases} \tag{2.26}$$

Replacing (2.18) into (2.26) becomes

$$\begin{cases} v_{P,N} = v_{u,k} + v_{l,k} + 2L\dfrac{di_{cir,k}}{dt} \\ v_{P,G} + v_{N,G} = v_{u,k} - v_{l,k} + L\dfrac{di_{load,k}}{dt} + 2v_{load,k} \end{cases} \tag{2.27}$$

Substituting equation (2.27) in (2.22) results in

$$\begin{cases} v_{P,N} = v_{+,k} + 2L\dfrac{di_{cir,k}}{dt} \\ v_{P,G} + v_{N,G} = v_{-,k} + L\dfrac{di_{load,k}}{dt} + 2v_{load,k} \end{cases} \tag{2.28}$$

Equation (2.28) can be rewritten with respect to zero-sequence and space vector components as,

$$\begin{cases} \dfrac{d\boldsymbol{i_{cir}}}{dt} = -\dfrac{\boldsymbol{v_+}}{2L} \\ v_{P,N} = v_{+,0} \\ \boldsymbol{v_{load}} = -\dfrac{\boldsymbol{v_-}}{\mathbf{2}} - \dfrac{L}{2}\dfrac{d\boldsymbol{i_{load}}}{dt} \\ v_{P,G} + v_{B,G} = v_{-,0} + 2v_{load,0} \end{cases} \tag{2.29}$$

The first equations of (2.29) highlights that the space vector of circulating currents can be controlled by the space vector of arm voltages. The second equation of (2.29) is a direct consequence of the converter topology, for which the zero-sequence component of the circulating current is identically zero. The third equation of (2.29) represents the relation between the space vector of load voltages and the space vector of arm difference voltages. The fourth equation of (2.29) represents load neutral point voltage displacement to the zero-sequence component of the load voltage and the arm difference voltage. Since load neutral

[4] In this figure P is the positive busbar terminal, N is the negative busbar terminal, G is the motor neutral point and $L_{upper}=L_{lower}=L$ are the arm inductance.

point is not connected, this equation does not influence any state variables of the system. This states that we have an additional degree of freedom which allows us to arbitrarily fix the value of zero sequence of the arm difference voltage $v_{-,0}$ [34].

2.4.5 Power balance

Based on (2.18) and (2.22), the arms sum and difference power of the generic leg *k* can be defined as

$$\begin{cases} P_{+,k} = v_{+,k}\, i_{cir,k} + \dfrac{1}{2} v_{-,k}\, i_{load,k} \\ P_{-,k} = v_{-,k}\, i_{cir,k} + \dfrac{1}{2} v_{+,k}\, i_{load,k} \end{cases} \tag{2.30}$$

The equation (2.30) can be written in terms of zero-sequence components and space vector components referring (2.25) as,

$$\begin{cases} \boldsymbol{P}_{+} = \dfrac{1}{2}\hat{\boldsymbol{v}}_{+}\hat{\boldsymbol{i}}_{\boldsymbol{cir}} + v_{+,0}\,\boldsymbol{i}_{\boldsymbol{cir}} + \dfrac{1}{4}\hat{\boldsymbol{v}}_{-,}\hat{\boldsymbol{i}}_{\boldsymbol{load}} + \dfrac{1}{2} v_{-,0}\,\boldsymbol{i}_{\boldsymbol{load}} \\ P_{-,0} = \dfrac{1}{2} Re\{\boldsymbol{v}_{+}\hat{\boldsymbol{i}}_{\boldsymbol{cir}}\} + \dfrac{1}{4} Re\{\boldsymbol{v}_{-}\hat{\boldsymbol{i}}_{\boldsymbol{load}}\} \\ \boldsymbol{P}_{-} = \dfrac{1}{2}\hat{\boldsymbol{v}}_{-}\hat{\boldsymbol{i}}_{\boldsymbol{c}} + v_{-,0}\,\boldsymbol{i}_{\boldsymbol{cir}} + \dfrac{1}{4}\hat{\boldsymbol{v}}_{+}\hat{\boldsymbol{i}}_{\boldsymbol{load}} + \dfrac{1}{2} v_{+,0}\,\boldsymbol{i}_{\boldsymbol{load}} \\ P_{-,0} = \dfrac{1}{2} Re\{\boldsymbol{v}_{-}\hat{\boldsymbol{i}}_{\boldsymbol{cir}}\} + \dfrac{1}{4} Re\{\boldsymbol{v}_{+,}\hat{\boldsymbol{i}}_{\boldsymbol{load}}\} \end{cases} \tag{2.31}$$

By replacing first and third in equation (2.29) and (2.31), the equations can be expressed as

$$\begin{cases} \boldsymbol{P}_{+} = -L\hat{\boldsymbol{i}}_{\boldsymbol{cir}}\dfrac{d\hat{\boldsymbol{i}}_{\boldsymbol{cir}}}{dt} - \dfrac{1}{4}L\hat{\boldsymbol{i}}_{\boldsymbol{load}}\dfrac{d\hat{\boldsymbol{i}}_{\boldsymbol{load}}}{dt} + v_{+,0}\,\boldsymbol{i}_{\boldsymbol{cir}} - \dfrac{1}{2}\hat{\boldsymbol{v}}_{\boldsymbol{load}}\hat{\boldsymbol{i}}_{\boldsymbol{load}} + \dfrac{1}{2} v_{-,0}\,\boldsymbol{i}_{\boldsymbol{load}} \\ P_{+,0} = -LRe\left\{\hat{\boldsymbol{i}}_{\boldsymbol{cir}}\dfrac{d\boldsymbol{i}_{\boldsymbol{cir}}}{dt}\right\} - \dfrac{1}{4}LRe\left\{\hat{\boldsymbol{i}}_{\boldsymbol{load}}\dfrac{d\boldsymbol{i}_{\boldsymbol{load}}}{dt}\right\} - \dfrac{1}{2}Re\{\boldsymbol{v}_{\boldsymbol{load}}\hat{\boldsymbol{i}}_{\boldsymbol{load}}\} \\ \boldsymbol{P}_{-} = -\dfrac{1}{2}L\hat{\boldsymbol{i}}_{\boldsymbol{load}}\dfrac{d\hat{\boldsymbol{i}}_{\boldsymbol{cir}}}{dt} - \dfrac{1}{2}L\hat{\boldsymbol{i}}_{\boldsymbol{cir}}\dfrac{d\hat{\boldsymbol{i}}_{\boldsymbol{load}}}{dt} + \dfrac{1}{2} v_{+,0}\,\boldsymbol{i}_{\boldsymbol{load}} - \hat{\boldsymbol{v}}_{\boldsymbol{load}}\hat{\boldsymbol{i}}_{\boldsymbol{cir}} + v_{-,0}\,\boldsymbol{i}_{\boldsymbol{cir}} \\ P_{-,0} = -\dfrac{1}{2}LRe\left\{\hat{\boldsymbol{i}}_{\boldsymbol{load}}\dfrac{d\boldsymbol{i}_{\boldsymbol{cir}}}{dt}\right\} - \dfrac{1}{2}LRe\left\{\hat{\boldsymbol{i}}_{\boldsymbol{cir}}\dfrac{d\boldsymbol{i}_{\boldsymbol{load}}}{dt}\right\} - Re\{\boldsymbol{v}_{\boldsymbol{load}}\hat{\boldsymbol{i}}_{\boldsymbol{cir}}\} \end{cases} \tag{2.32}$$

When the coupling inductors are correctly designed, their power can be neglected. Moreover, second of (2.32) states that the power produced by all the modules is supplied to the load, i.e., it is not linked to the SoC balancing problem. Thus, balancing can be achieved using the reference to the given equations:

$$\begin{cases} \boldsymbol{P}_{+} \cong v_{+,0}\, \boldsymbol{i_{cir}} - \frac{1}{2}\hat{\boldsymbol{v}}_{\boldsymbol{load}}\hat{\boldsymbol{i}}_{\boldsymbol{load}} + \frac{1}{2} v_{-,0}\, \boldsymbol{i_{load}} \\ \boldsymbol{P}_{-} \cong \frac{1}{2} v_{+,0}\, \boldsymbol{i_{load}} - \hat{\boldsymbol{v}}_{\boldsymbol{load}}\hat{\boldsymbol{i}}_{\boldsymbol{cir}} + v_{-,0}\, \boldsymbol{i_{cir}} \\ P_{-,0} \cong -Re\{\boldsymbol{v_{load}}\hat{\boldsymbol{i}}_{\boldsymbol{circ}}\} \end{cases} \quad (2.33)$$

The converter leg balancing can be achieved by the space vector of $\boldsymbol{P}_{+}$, sum of power in arms, (2.33). $\boldsymbol{P}_{+}$ is controlled to bring the common level of average SoCs and obtain $\boldsymbol{SoC}_{+} = 0$.

The balancing of upper and lower arms can be achieved by the quantities $\boldsymbol{P}_{-}$ and $P_{-,0}$ (2.33). The $\boldsymbol{P}_{-}$ is controlled in such a way to ensure that on each leg, there will be same difference between lower arm average SoC and upper arm average SoC to obtain $\boldsymbol{SoC}_{-} = 0$. The $P_{-,0}$ is controlled to ensure in such a way that the SoC sum of three upper arms is equal to the SoC sum of three lower arms to obtain $SoC_{-,0} = 0$. The zero-sequence and space vector components of sum and difference arm SoC are derived by the phase components $SoC_{+,k} = \overline{SoC}_{u,k} + \overline{SoC}_{l,k}$ and $Soc_{-,k} = \overline{SoC}_{u,k} - \overline{SoC}_{l,k}$.

Equation (2.33) is composed by two vector equations and one scalar equation ($\boldsymbol{P}_{+}, \boldsymbol{P}_{-}, P_{-,0}$), with one vector unknown and two scalar unknowns $\boldsymbol{i_{cir}}, v_{+,0}, v_{-,0}$, i.e., three equations for four unknowns. This implies that (2.33) cannot be instantaneously satisfied.

Moreover, the upper and lower arm within the same leg are typically controlled in a complementary way, resulting in $v_{+,0} = NV_{mod}$ and $v_{-,0} = 0$ This approach leaves the space vector of the circulating currents as the only manipulated variable to balance the six arms average SoCs, while the balancing of the cells SoCs within the same arm rely on the sorting technique. Therefore, in order to control the average values of the three power terms in (2.33), the circulating current can be composed by the following three components.

- A DC component of circulating current $\boldsymbol{i}^{*}_{+,\boldsymbol{cir}}$ which interacts with $v_{+,0}$ and control $\boldsymbol{P}_{+}$,
- An inverse component at the fundamental frequency $\boldsymbol{i}^{*}_{-,\boldsymbol{cir}}$ which interacts with $\hat{\boldsymbol{v}}_{\boldsymbol{load}}$ and controls $\boldsymbol{P}_{-}$.
- A direct component at the fundamental frequency $\boldsymbol{i}^{*}_{-,\boldsymbol{cir}}$ which interacts with $\boldsymbol{v_{load}}$ controls $P_{-,0}$.

Then, the unknown variables can be computed as,

$$i^*_{cir} = i^*_{+,cir} + i^*_{-,cir} + i^*_{+,cir,0} \rightarrow \begin{cases} \boldsymbol{i^*_{+,cir}} = \frac{\boldsymbol{P^*_+}}{NV_{mod}} \\ \boldsymbol{i^*_{-,cir}} = -\frac{\boldsymbol{\hat{P}^*_-}}{\boldsymbol{v_{load}}} \\ i^*_{-,cir,0} = -\frac{P^*_{-,0}}{\boldsymbol{\hat{v}_{load}}} \end{cases} \tag{2.34}$$

The equation (2.34) cannot satisfy (2.33) instantaneously, leaving uncompensated power terms, which can be calculated in the hypothesis under steady-state operations:

$$\begin{cases} \boldsymbol{v_{load}} = V_{load} e^{j\omega t} = \varepsilon \frac{NV_{mod}}{2} e^{j\omega t} \\ \boldsymbol{i_{load}} = I_s e^{i(\omega t - \varphi)} \\ \boldsymbol{P_{load}} = \frac{1}{2} \boldsymbol{\hat{v}_{load}} \boldsymbol{\hat{i}_{load}} = \frac{1}{4} \varepsilon NV_{mod} I_{load} e^{-i(2\omega t - \varphi)} \end{cases} \tag{2.35}$$

where ε is the modulation index, V_{load} is the load voltage amplitude, I_{load} is the load current magnitude, φ is the load current phase angle with respect to load voltage phasor angular position, ω is the electrical angular frequency.

Rewriting the eq (2.34) into (2.33) and considering (2.35), the residual power terms can be written as

$$\begin{cases} \widetilde{\boldsymbol{P}}_+ \cong -\frac{1}{4} \varepsilon NV_{mod} I_{load} e^{-j(2\omega t - \varphi)} - \frac{\boldsymbol{2\hat{P}^*_-}}{\varepsilon} e^{-j\omega t} - \frac{2\hat{P}^*_{-,0}}{\varepsilon} e^{j\omega t} \\ \widetilde{\boldsymbol{P}}_- \cong \frac{1}{2} NV_{mod} I_{load} e^{j(\omega t - \gamma)} - \frac{\varepsilon}{2} \boldsymbol{\hat{P}^*_+} e^{-j\omega t} + P^*_{-,0} e^{-j2\omega t} \\ \tilde{P}_{-,0} \cong -Re\left\{ \frac{\varepsilon}{2} \boldsymbol{\hat{P}^*_+} e^{j\omega t} - \boldsymbol{P^*_-} e^{j2\omega t} \right\} \end{cases} \tag{2.36}$$

where $\tilde{P}$ represents not compensated power term. From the above equation (2.36), uncompensated power terms consist of conditions oscillating at $\pm\omega \; and \; \pm 2\omega$, whose magnitude depend on balancing power reference value, operating conditions, and modulation index. The residual power has zero value average for $\omega \neq 0$ and is not expected to influence SoC, since electrochemical cells have slow dynamics. Conversely for $\omega = 0$, the residual powers have steady-state average. This implies, equation (2.33) cannot be decoupled, and the equations cannot be satisfied, not even in terms of average value, using circulating current $\boldsymbol{i_c}$ as a control variable.

The error inputs $(SoC^*_+ - SoC_+), (SoC^*_- - SoC_-) \; and \; \left(SoC^*_{-,0} - SoC_{-,0}\right)$ can be given to the PI regulator to generate reference power values $P^*_+, \hat{P}^*_- \; and \; \hat{P}^*_{-,0}$. But it might cause non-

uniform behavior of residual power for different working conditions due to oscillations of electrochemical cell SoCs. On the other hand, a hysteresis regulator is used to generate circulating current references directly from the estimated SoCs.

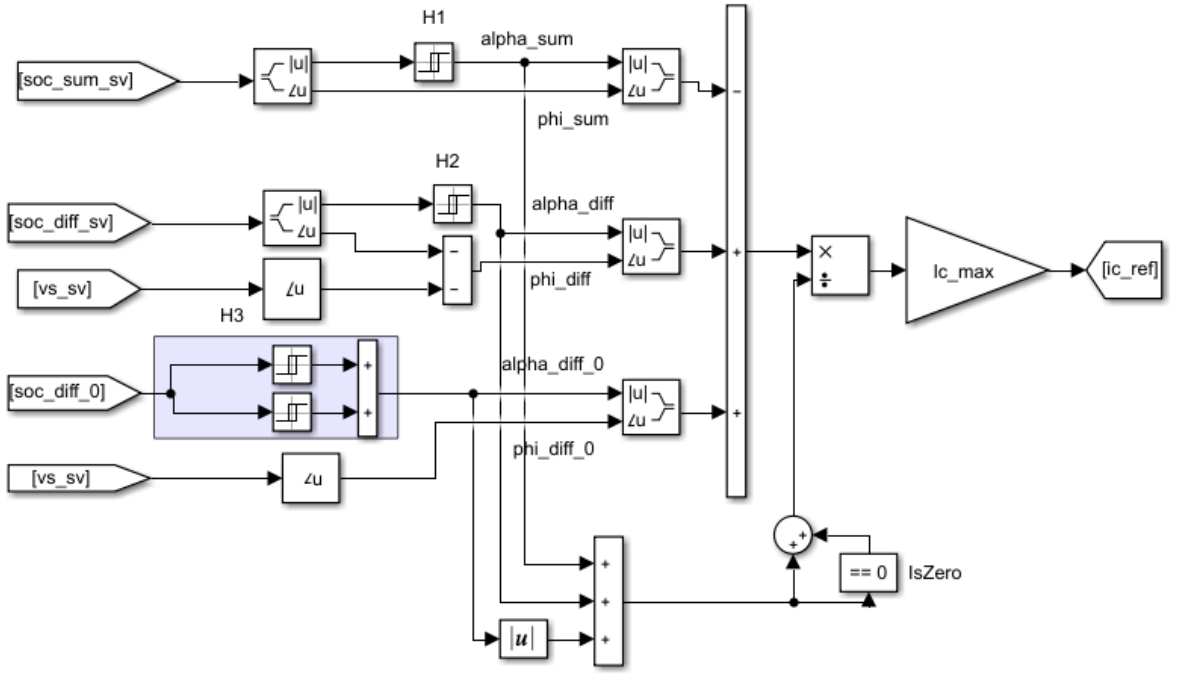

Figure 2.11 Circulating current reference using hysteresis regulator.

When the magnitude of SoC_+ is above the upper hysteresis band (UHB) as shown in *Figure 2.11*, the first term is generated by the hysteresis controller H1 and the magnitude of α_+ becomes 1. To oppose the SoC deviation, the circulating current contribution is computed as $\alpha_+ * e^{\varphi_+}$, where φ_+ is the phase angle of SoC_+. The quantity alpha_sum becomes 0 when magnitude SoC_+ is under the lower hysteresis band (LHB). In the same way, H2 is responsible for producing the variable α_- and its phase angle φ_-; this angle is the difference between the phase angle of V_{load} and SoC_-. The hysteresis band H3 is symmetrical around 0 and the output of $\alpha_{-,0}$ are three values (-1,0,1). The quantity of $\alpha_{-,0}$ is -1 when $SoC_{-,0}$ is below the lower hysteresis band. $\alpha_{-,0}$ and is 1 when $SoC_{-,0}$ is above the upper hysteresis band i.e., it switches from 1 to 0 when $SoC_{-,0}$ reaches from positive value to zero, or from -1 to 0 when $SoC_{-,0}$ reaches zero from negative value. Here the phase angle of $\varphi_{-,0}$ is the same as that of load voltage.

After computing the circulating current reference, it is necessary to modify the supplied voltage of arm in order to slightly change the Vdc_{bus} between the phases to create voltage difference between them.

The arms reference can be written as:

$$\begin{cases} V_{ref,u,k} = \dfrac{V_{dc_{bus}}}{2} - V_{load,k} - V^{*}_{cir,ref,k} \\ V_{ref,l,k} = \dfrac{V_{dc_{bus}}}{2} + V_{load,k} - V^{*}_{cir,ref,k} \end{cases} \tag{2.37}$$

where $V_{cir,ref,k}$ is the circulating currents voltage reference for each phase. This is calculated by proportional regulator with the circulating current errors. The maximum allowed value of $V_{cir,ref,k}$ is 10% of the Vdc_{bus} nominal value.

3 Simulation Modelling and results

In this chapter, the design of modular multilevel converter in Matlab/Simulink library has been discussed. Before designing a converter prototype, the performance of each module, balancing operation, and field-oriented control of the induction machine are discussed. The simulation parameters considered here are similar to the future prototype requirements.

In our modular multilevel converter, each module consists of 14 cells to form a battery, and each arm consists of 6 modules. The initial part of this chapter presents a design of the converter, whereas, in the second part, the speed control of the induction machine has been discussed. The PWM technique used in our modular multilevel converter is phase disposition pulse width modulation and the semiconductors used are N-channel MOSFETs.

3.1 MMC Modelling

In our modular multilevel converter, each module consists of a half-bridge converter composed of two N-channel MOSFETs. To drive this MOSFET, a signal is given from the master microcontroller to the gate driver. Based on the input received from the master microcontroller, the gate driver will turn ON the respective MOSFET. Therefore, at first, the half-bridge converter with the gate driver is selected. The parameters used for the testing module are mentioned below in *Table 3.1*.

Parameters	*Value*
Module battery voltage	*50V*
No. of Modules per arm	*6*
Max DC bus voltage	*300V*
Number of phases	*3*
Arm mutual inductor	*1mH*

Table 3.1 MMC parameters

Simulation parameters

Solver time	*5 µs*
Switching frequency	*10 kHz*
Load resistance	*2.5 Ω*
Load inductance	*3 mH*
Reference voltage frequency	*50Hz*
Reference voltage	*120 V*

Table 3.2 Simulation parameters

3.1.1 Ideal module with gate driver

The input signal of the gate driver of each module is received from the microcontroller that calculates it by comparing the reference voltage with the PWM carrier signal. The compared output, a HIGH signal of 3.3V, and a LOW signal of 0V are selected, which are realistic values of the microcontroller board. For the gate driver, HIGH threshold of 2.5V and LOW threshold of 0.8V are selected. These are the real threshold values of IRS2184 half-bridge gate-driver. Each module consists of dedicated hardware to measure the battery voltage and the temperature. At present, constant battery voltage is considered with the negligible battery internal resistance and negligible MOSFET conduction resistance. The Simulink model of the module is reported below in *Figure 3.1.*

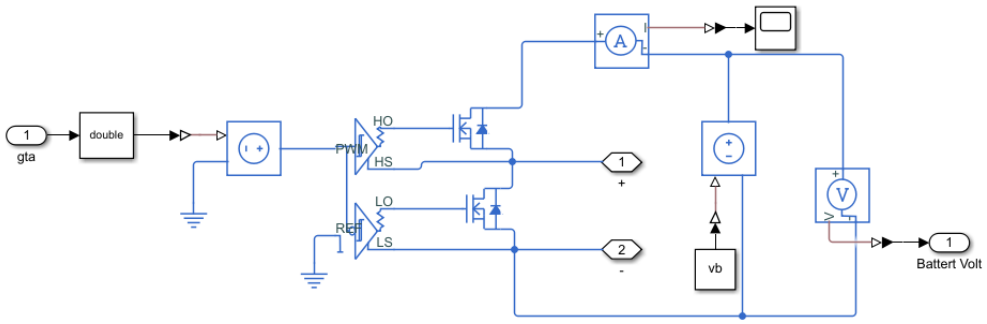

Figure 3.1 Module modeling with half-bridge gate driver

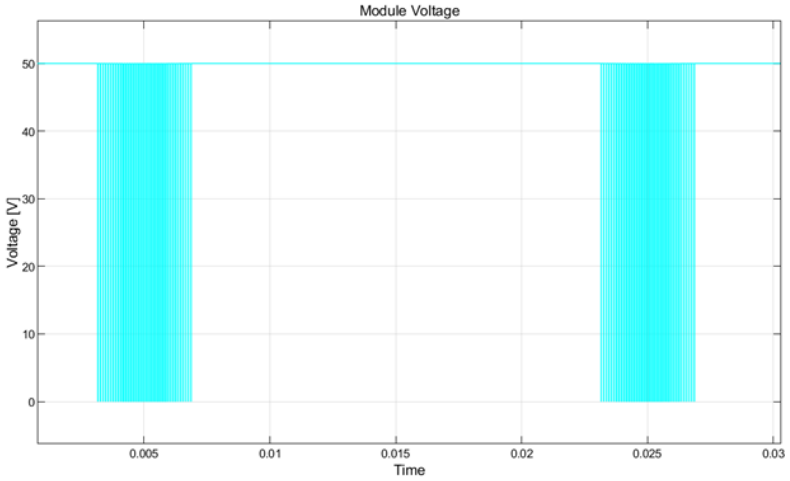

Figure 3.2 Module voltage of MMC

From *Figure 3.2*, it is observed that when the reference voltage is greater than the module voltage, it generates a voltage equal to the battery voltage of 50V. Here the frequency of each module is 10kHz. Therefore, the overall frequency of phase voltage is equal to the product of the number of modules and the frequency of each module. Each arm consists of six modules, and their arm voltages are shown in *Figure 3.3*.

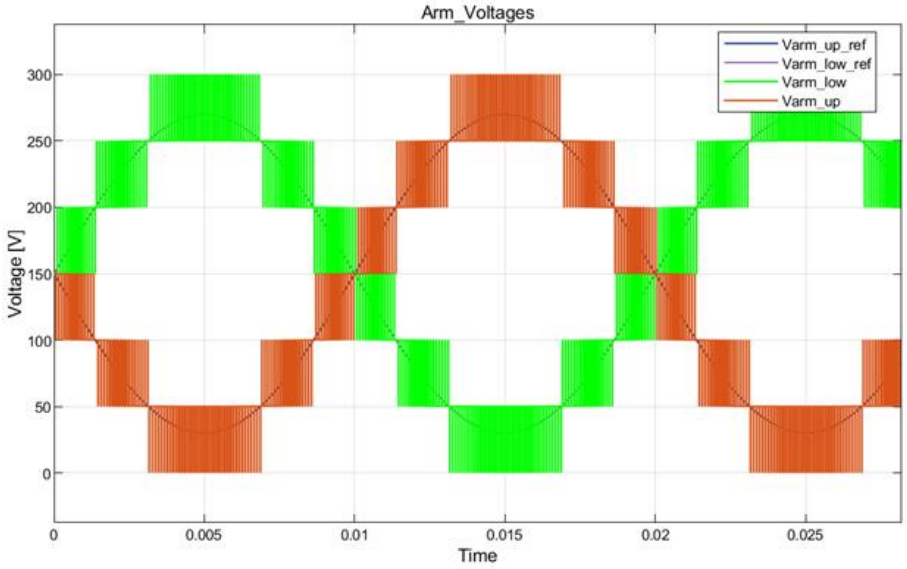

Figure 3.3 Arm voltages of MMC

The arm voltages are following their reference, and there is no voltage drop in the modules as the internal battery resistance, and MOSFETs on-resistance are considered negligible for ideal conditions.

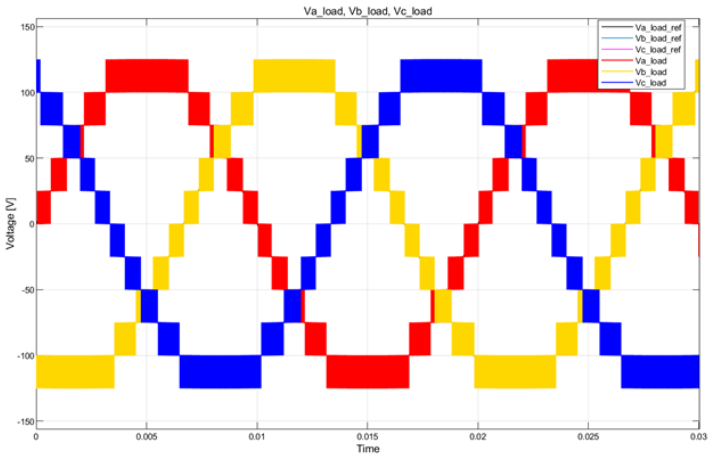

Figure 3.4 Load voltages of MMC

Figure 3.4 and *Figure 3.5* represent the load voltages and load currents with respect to load parameters reported in Table 3.2. It can be observed that the load voltage is almost sinusoidal with total harmonic distortion equal to 29%. This can be further reduced by increasing the number of modules per arm. Then the load current is almost sinusoidal, resulting in torque ripple reduction in traction drive applications. The phase peak value of 120 V with a load resistance of 2.5 Ω results in the current of 50A, as shown in *Figure 3.5*. which is the maximum current the module should handle when implementing hardware.

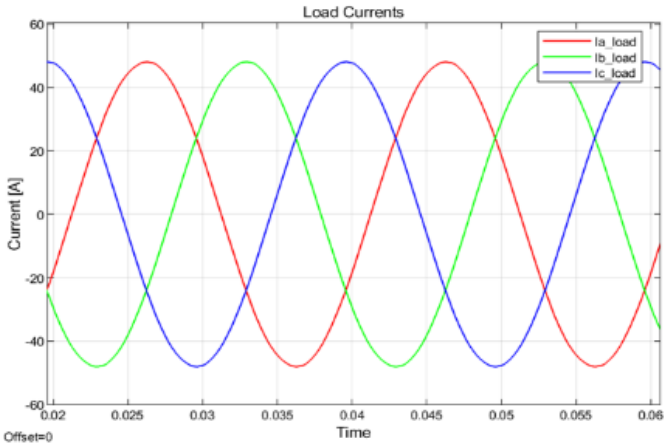

Figure 3.5 Load currents of MMC

3.1.2 Module with battery and MOSFET resistance

In 3.1.1, an ideal module is considered, and their voltage and current waveforms are shown. In practical scenarios, each MOSFET will have drain-source resistance and a battery with internal resistance. Therefore, by looking at the datasheet of IPP041N12N3-G MOSFET selected for

our hardware, on-resistance of 3.8 mΩ and internal battery cell resistance of 3 mΩ per cell are chosen [35]. Then the module is constructed by considering these resistances are shown in *Figure 3.6.*

$$R_{ds,on} = 3.8\ m\Omega$$

$$R_{batt,int} = 42\ m\Omega$$

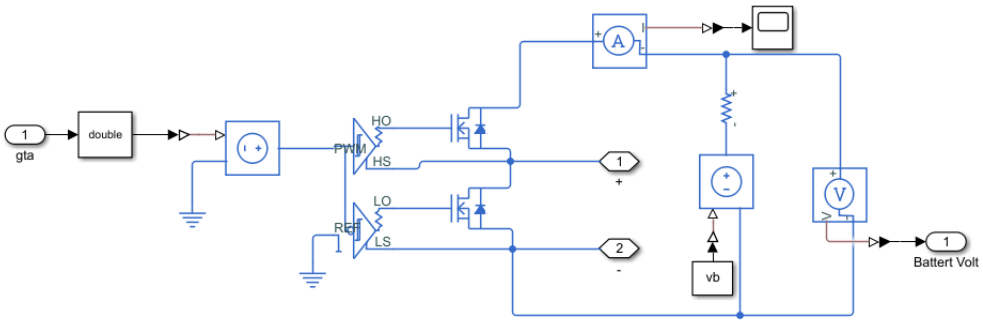

Figure 3.6 Module with resistance drop

The results obtained by adding resistance can be seen in *Figure 3.7.* Here module voltage is not constant anymore as it fluctuates between 48V and 52V depending on the direction of the current. The voltage drop is approximately 2V, i.e., $v_{drop} = 45.8m\Omega * 50 = 2.2V$. Also, the resultant arm voltage with drop is reported in *Figure 3.8.* Due to this resistance drop, the module switching in each leg is not constant anymore but will fluctuate between 6 and 7, resulting in the increase of circulating current to flow between the legs of our MMC.

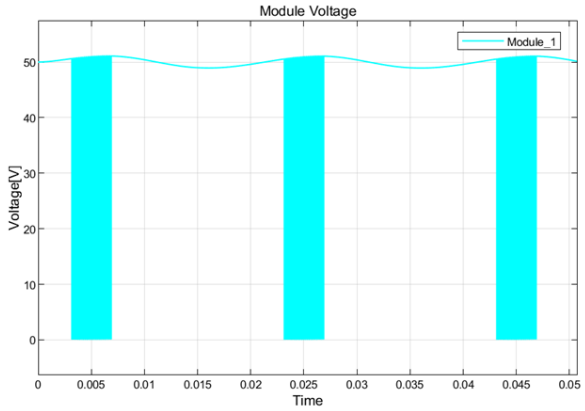

Figure 3.7 Module voltage with resistance drop

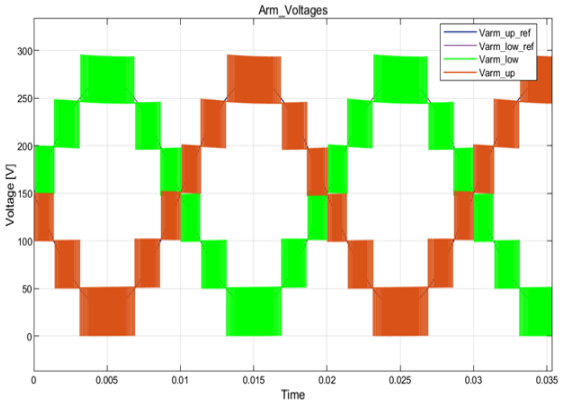

Figure 3.8 Arm voltage with resistance drop

3.1.3 Average model of module

To reduce the simulation time in Matlab without affecting the modules functionality, an ideal module is selected. In this ideal module, N-channel MOSFET is replaced with an ideal semiconductor switch. The average model of the module is represented below in *Figure 3.9*.

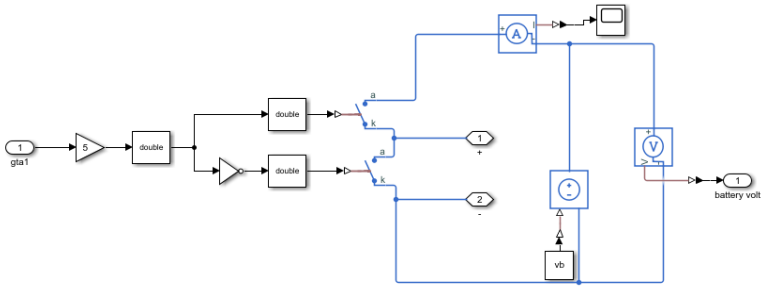

Figure 3.9 Average model of module

This ideal switch has the same function as an N-channel MOSFET, and the gate driver is also removed. Instead, the compared signal (0 or 1) is connected with a gain of 5V to reach the threshold voltage of the ideal semiconductor switch. This signal is sent directly to control the semiconductor. The arm voltages of the average model are compared with the arm voltages of actual model in *Figure 3.3*.

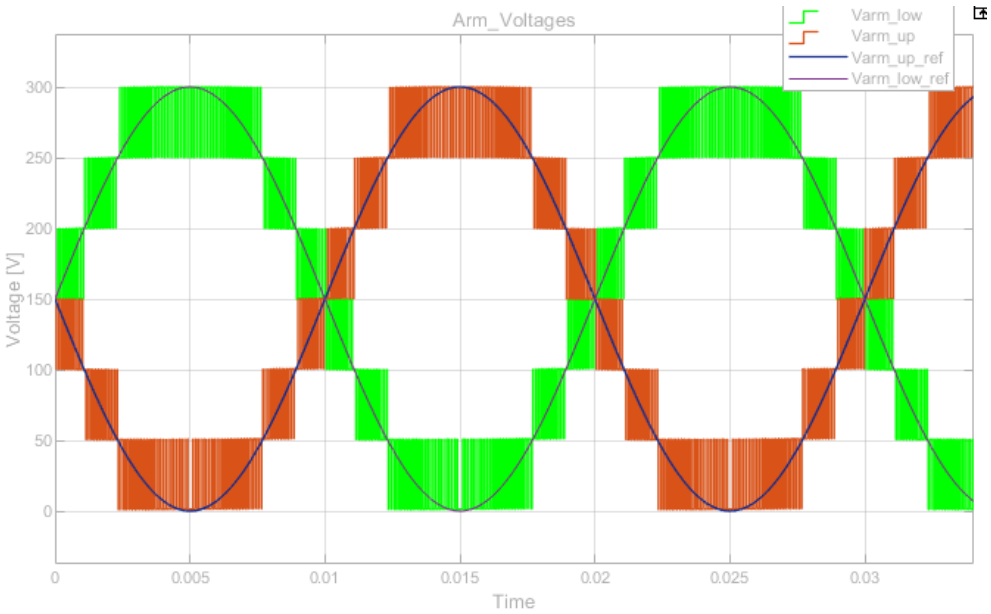

Figure 3.10 Average model arm voltage

From *Figure 3.3* and *Figure 3.10*, it is clear that the ideal condition of our actual module and average module are generating the same arm voltage with respect to the reference. Therefore, further calculations are carried out using average model.

So far, the battery as constant voltage source is considered. But in practical scenario, the battery voltage will change depending on the state of charge. Balancing of modules is performed based on the state of charge of the battery. Therefore, modelling of SoC is required.

3.1.4 Modelling SoC of the module

The energy stored in battery can be calculated as energy available in the battery and total capacity of the battery. Since our focus is realization of converter, the SoC can be estimated by simple coulomb-counting method [36], [37].

$$\begin{aligned} SoC_{N,k,u}(t) &= SoC_{N,k,u}(t_0) - \frac{1}{3600.\,Q_{max}}\left(\int_{t_0}^{t} i_{N,k,u}(t)dt\right) \\ SoC_{N,k,l}(t) &= SoC_{N,k,l}(t_0) - \frac{1}{3600.\,Q_{max}}\left(\int_{t_0}^{t} i_{N,k,l}(t)dt\right) \end{aligned} \tag{3.1}$$

where $SoC_N(t_0)$ is the N^{th} cell SoC at the initial time, $i_N(t)$ is the module current estimated by realizing the current flowing in the arm where the module is installed by knowing whether it is in inserted or bypassed mode and Q_{max} is the battery capacity in Ah.

$$\begin{aligned} i_N(t) &= i_{arm} * S_N \quad N = 1,2,\ldots\ldots, no.of\ arms \\ S_N &= \begin{cases} 1 & Higher\ MOSFET\ is\ ON \\ 0 & Higher\ MOSFET\ is\ OFF \end{cases} \end{aligned} \tag{3.2}$$

where $i_N(t)$ is the current flowing in the N^{th} module calculated by the current flowing in arm and the respective arm switching signal. When $S_N = 1$, the higher MOSFET is ON for the respective module i.e., inserted mode. Therefore, the current flowing in the module is arm current. The SoC of whole module can be calculated by knowing the number of cells present in a module. The module voltage is estimated as the product of number of cells present in each module with their respective SoCs. Considered lithium-ion cell voltage range is in between [3V to 4.2V] [35]. For sake of simplicity, a simple model with voltage linearly changing with the SoC is considered. Therefore, module voltage can be defined as:

$$V_{module} = no.of\ cells * (3V + 1.2 * SoC) \tag{3.3}$$

Since the module voltage is not constant anymore, it is modelled as a controlled voltage source. This is shown in *Figure 3.11*.

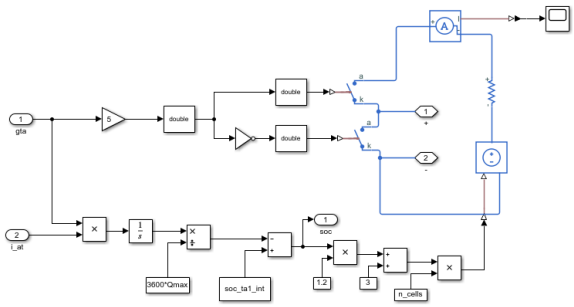

Figure 3.11 SoC model of MMC

From now on, battery voltage will not be constant. Its voltage depends on the current direction and whether the module is in inserted or bypassed mode. Therefore, each module in the MMC will have different voltage. Consequently, the balancing of modules is necessary to maintain constant voltage across DC bus which is studied in next section.

3.2 Balancing process

The modular multilevel converter configured with double star chopper cell permits balancing of modules without disturbing voltage across the load. The balancing process in MMC can be accomplished by three controls [38]. They are.

- Module balancing,
- Arm balancing, and
- Leg balancing.

To validate balancing operation, all the modules in each arm are made with unequal SoC ranging between 0.7 and 0.9 using random function generator in Matlab. The simulation parameters for balancing algorithm are given below in *Table 3.3*.

Simulation parameters

Simulation time	*6 s*
Battery capacity (Q_{max})	*0.1Ah*
SoC range	*0.7-0.9*

Table 3.3 parameters for SoC balancing.

3.2.1 Module balancing

The process of module balancing is to equalize all the modules present within a single arm. To perform this operation, we will use sorting algorithm. Usually when PDPWM signal is used as modulation technique, the module responsible for the first carrier signal is turned ON and stays in inserted mode for long time. This results in faster discharge of the battery in corresponding module with respect to other modules. Therefore, by using sorting algorithm, it is possible to control the module i.e., whether a particular module is inserted in the beginning or later by knowing the current direction and SoC of the module. The functioning of sorting algorithm is, when $I_{arm} > 0$ i.e., when current charges the module, the module with least SoC will be inserted first and when $I_{arm} < 0$ i.e., when the battery is discharging, the module with highest SoC will be inserted first.

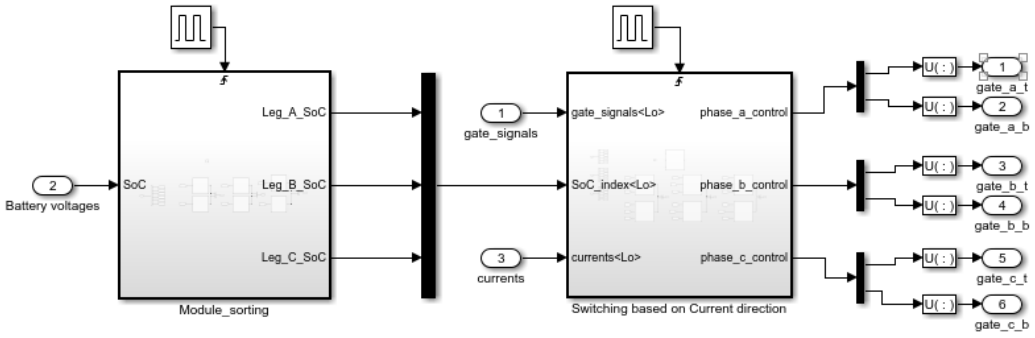

Figure 3.12 Module balancing

Since battery voltage dynamics will change very slowly, the sorting of battery modules will be performed 10 times per reference voltage period. This choice ensures us the reduction of switching losses because modules will be turned ON /OFF as per the sorting algorithm. The Matlab functions of both subsystems are mentioned below.

```
function SoC_index  = Sorting(SoC_arm)
    SoC_index = ones(6,1);
    [~,SoC_index] = sort(SoC_arm, 'descend');
end
```

Figure 3.13 Module sorting

```
function gate_Sorted  = gatecontrol(current, SoC_index, gates)
gate_Sorted = zeros(6,1);
i = sum(gates);
    if current>=0
        gate_Sorted(SoC_index(1:i)) = 1;
    elseif current<0
        gate_Sorted(SoC_index(end-i+1:end)) = 1;
    end
end
```

Figure 3.14 Switching based on current direction

In the first triggered subsystem modules will be sorted with 10 times per period. Based on their SoC, the index of 6 rows with 1 column array will be sent to the next subsystem as shown in *Figure 3.12* . This subsystem will decide, which module should turn on first based on the current direction in the arm, gate signal, and the sorted modules array. Therefore, all the modules in each arm will converge to equal SoC at the end, namely $\overline{SoC}_{k,u}$ *or* $\overline{SoC}_{k,l}$. The SoC balance of generic arm is shown below in *Figure 3.15.*

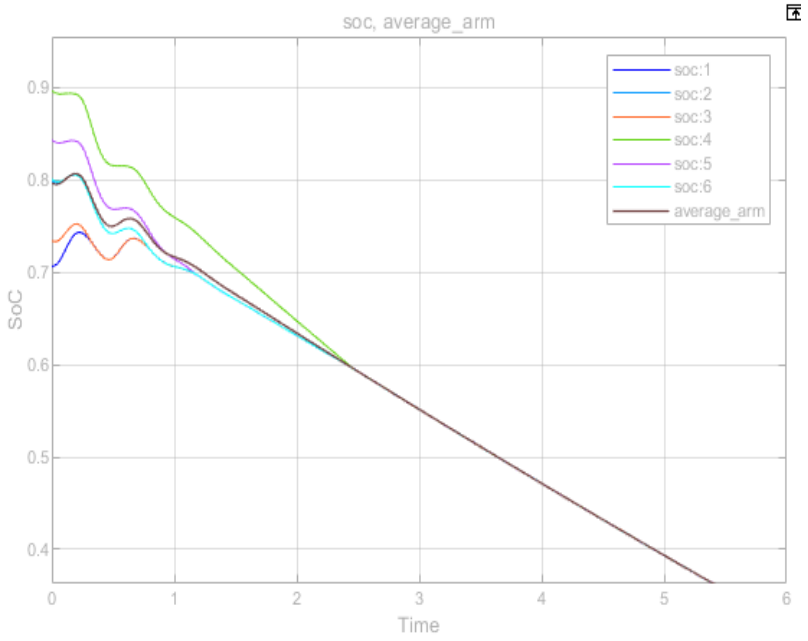

Figure 3.15 SoC balancing of single arm

From *Figure 3.15* all the modules in this arm are balanced after 2.5 seconds. It is worth mentioning that all the modules in different arms will converge to their average arm SoCs at different times based on the SoC variation of each arm.

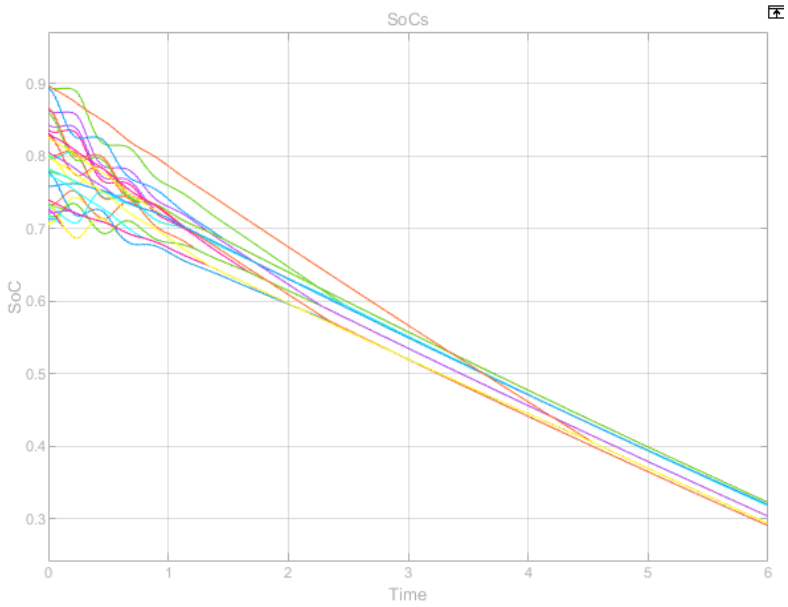

Figure 3.16 SoC balancing of all arms

After 4 seconds in the *Figure 3.16,* all arms in the MMC are converged to the average arms SoC, namely $\overline{SoC}_{k,u}$ *and* $\overline{SoC}_{k,l}$. But the balancing between the arms and legs is not possible by using sorting algorithm. Therefore, to achieve the arm and leg balance, it is necessary to generate the circulating current. In the following sections, other balancing methods are introduced to control the circulating currents.

3.2.2 Arm balancing

For arm balancing, it is necessary to control the circulating current for transferring power among the arms. By controlling DC bus reference, it is possible to produce an alternating circulating current with the same frequency of the phase output voltage. Modifying this current, it is possible to transfer power from lower to upper arm or upper to lower arm. It equalizes the SoCs between upper and lower arms of each leg. To check circulating currents reference, the upper arm SoCs are chosen as 0.75, 0.85, 0.8 and the lower arm SoCs are chosen as 0.95, 0.85, 0.9. The SoCs are selected in such a way that the average SoC of each leg is constant and the SoCs of upper and lower arms are different. Therefore, using the circulating current reference in *Figure 2.11*, the generated circulating currents are reported in *Figure 3.17.*

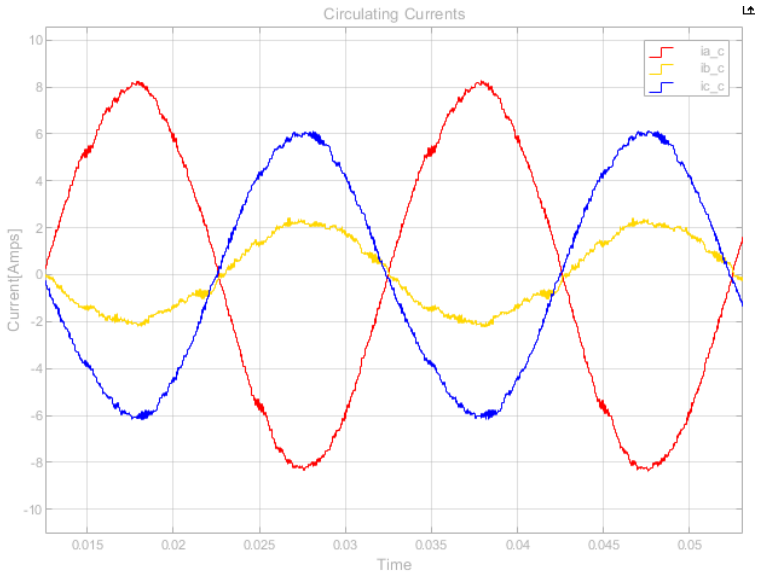

Figure 3.17 Circulating currents of arm balancing.

It can be seen in *Figure 3.17* that the circulating current magnitude of each phase is different. Here the phase-a (red color) has higher magnitude of 8A which is the limit for circulating current. This is due to the difference in average SoC of upper arm $\overline{SoC}_{a,u}$ and average SoC of lower arm $\overline{SoC}_{a,l}$, typically around 20%. The phase-c (blue color) has the magnitude of 6A circulating current because SoC difference between the arms here is 10%. The phase-b (yellow color) has the lowest magnitude where the reference is generated to maintain its average SoC. The frequency of circulating current is 50Hz in our case. The SoC of average arms is reported below in *Figure 3.18*.

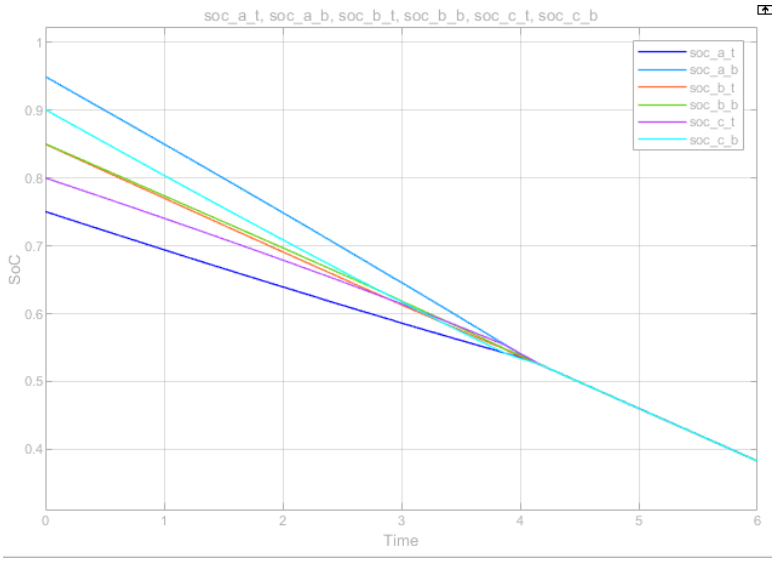

Figure 3.18 Average SoC of the arms

From the *Figure 3.18*, it is observed that the SoCs of all arms are converged to their average SoC after 4 seconds. In the later section, the change in DC circulating current reference to balance the leg SoCs to average SoC will be discussed.

3.2.3 Leg balancing

It is necessary to change the dc_{bus} voltage reference of each phase so that the energy is transmitted from highest charged leg to the lowest charged leg. This is achieved by controlling the DC component of circulating currents. To validate this control, each leg is assigned with the same SoC for all modules. The SoCs selected for all the modules in each leg are 0.7, 0.8, 0.9. The resulting circulating currents are mentioned below in *Figure 3.20*.

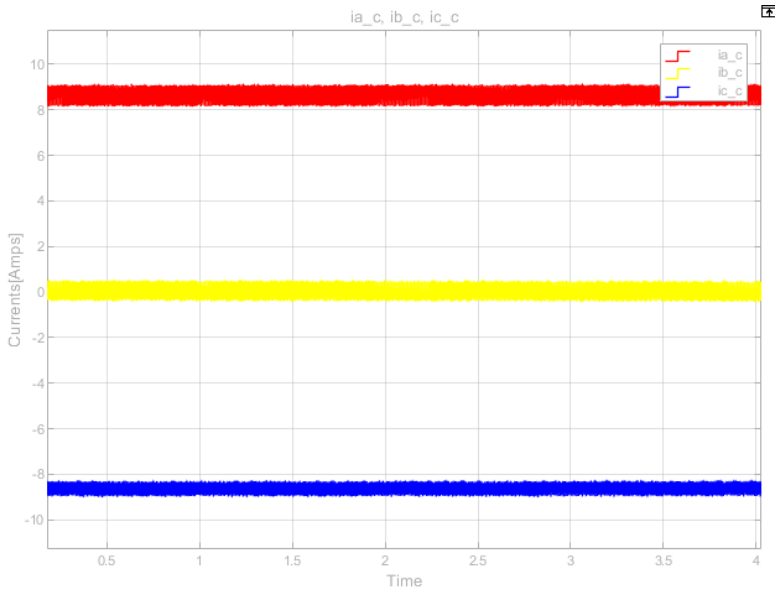

Figure 3.19 Leg balance circulating currents.

As anticipated, only the DC component of the circulating currents is present. From *Figure 3.19*, it is obvious that the current flows from the third leg to the first leg. Also, there is zero current in phase-b because the mean value of three leg average, $\overline{SoC}$ is equal to the phase-b average $\overline{SoC_b}$. The average SoC of the legs converging is reported in *Figure 3.20*.

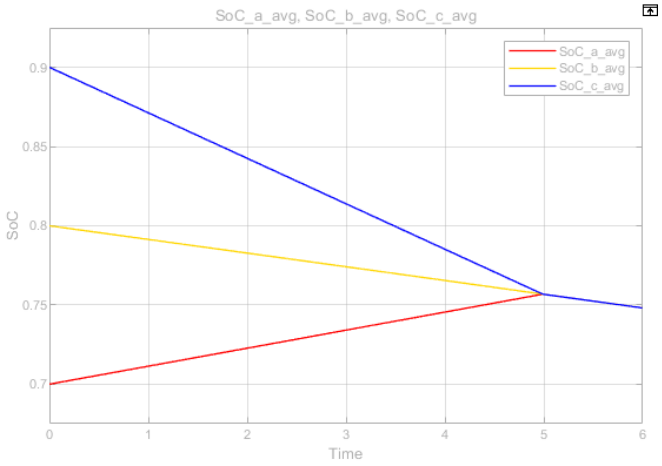

Figure 3.20 Leg average SoC

After realizing separate balancing for the module, arm and leg, the overall balancing is examined now. For this balancing process, simulation time is increased to 9 secs to check whether the overall modules SoC converges to its average $\overline{SoC}$.

3.2.4 Overall SoC balancing

To simulate the MMC for this balancing, the module SoC is considered different in each arm which is introduced by random values between 0.7 and 0.9. It is interesting to see the below *Figure 3.21* to *Figure 3.24*, on how the circulating current is strictly related to SoC of legs.

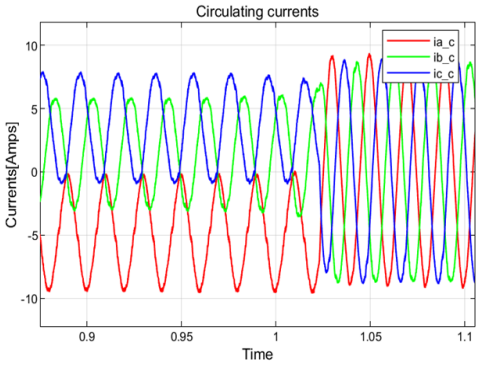

Figure 3.21 Circulating currents at leg balancing.

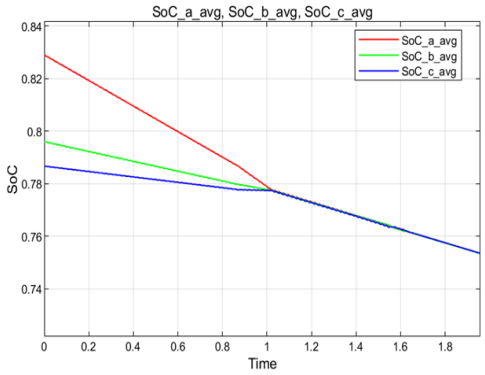

Figure 3.22 Average leg SoC balancing

From *Figure 3.21* the circulating currents consists of DC components and fundamental component where the frequency is equal to load reference frequency. When the average SoC of legs is converged to mean value as shown in *Figure 3.21*, the circulating currents becomes symmetrically inverted three-phase at 1.02 secs where all the DC components vanish.

Therefore, the DC components of circulating currents is strictly related to leg SoC balancing as shown in section *3.2.3*.

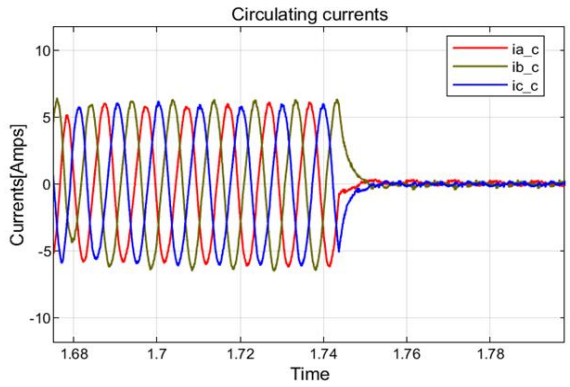

Figure 3.23 Circulating current at average arm balancing.

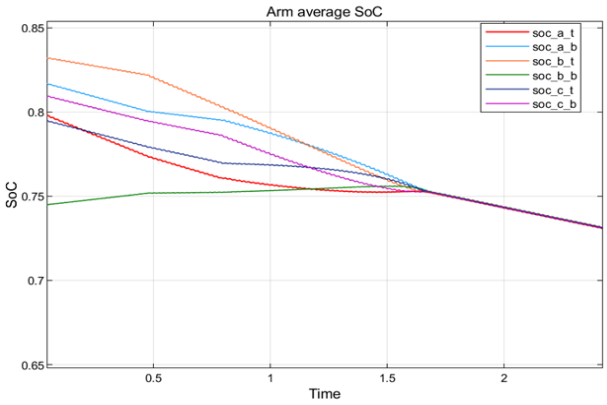

Figure 3.24 Average SoC of an arm.

From *Figure 3.23* and *Figure 3.24*, the time taken to converge the arm SoCs is 1.7 secs. From then, the circulating current is negligible. It is also worth mentioning that the average arm SoC converging is not always equal to the whole module converging. This module converging is based on the sorting algorithm. The speed converging depends on the number of times, the modules per period are swapped and the current magnitude in arm as shown in *Figure 3.12*. It is a tradeoff between the balancing time and switching losses. The SoC of all modules converging is shown in *Figure 3.25*.

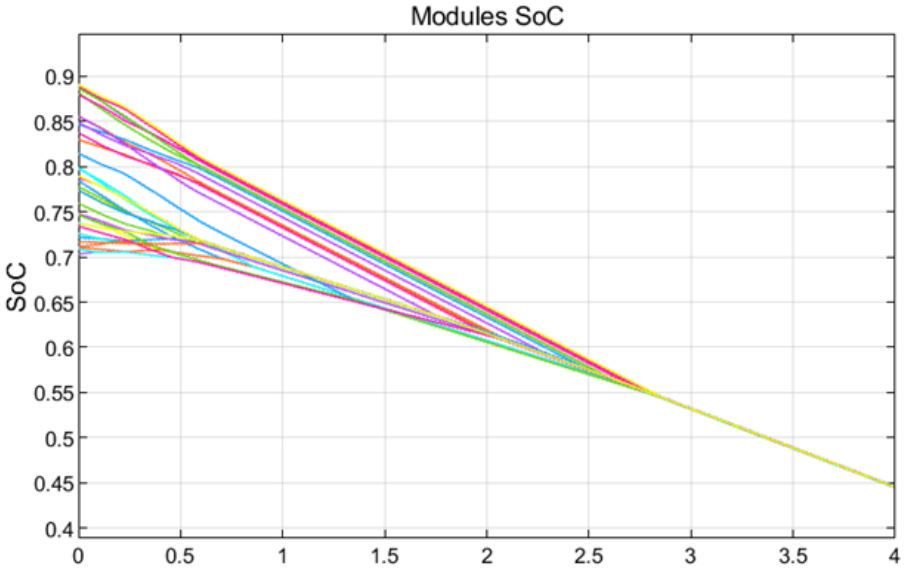

Figure 3.25 All modules SoC balancing.

From the *Figure 3.24*, the average arm balancing occurs at 1.69 secs which is different from overall SoC balancing. All the modules in our MMC are converged to their average $\overline{SoC}$ at 2.75 sec. This means that all modules are balanced. Next, we will realize the speed control of the induction motor by using this converter.

3.3 Speed Control of Induction Machine

Till now, we analyzed our MMC converter by using a load consisting of series resistor and inductor. But the main purpose of the thesis is to design a converter for battery electric vehicles which consists of electrical motors namely induction motor. Hence, field oriented control of induction machine is analyzed.

3.3.1 Field oriented control

The field-oriented control is a vector control, and its main focus is to control an induction machine with the concept of DC machine control. This is achieved by introducing the control of a fictitious machine [39]. In DC machines, there are two complete decoupled equations for flux and current control. Flux control is obtained through stator current control whereas torque can be controlled by regulating rotor current i.e., armature current. The stator and rotor windings are at 90° so that their magnetic coupling is null. In case of induction machine, current regulation in rotor cannot be achieved as only the stator winding is supplied. Therefore, we will model a fictitious machine where there will be decoupling between the two quantities of flux and torque. To model such a machine, we need to refer all the quantities oriented on rotor flux.

The dynamic model of induction machine is represented as:

$$\begin{aligned} \boldsymbol{V}_s &= r_s \boldsymbol{i}_s + l_s \frac{d}{dt}\boldsymbol{i}_s + L_m \frac{d}{dt}\left(\boldsymbol{i}_s + \boldsymbol{i}_r e^{jp\theta}\right) \\ 0 &= r_r \boldsymbol{i}_r + l_r \frac{d}{dt}\boldsymbol{i}_r + L_m \frac{d}{dt}\left(\boldsymbol{i}_s e^{-jp\theta} + \boldsymbol{i}_r\right) \\ T &= \frac{3}{2} p L_m \, \Im m[\boldsymbol{i}_s \boldsymbol{i}_r^* e^{-jp\theta}] \end{aligned} \tag{3.4}$$

It can be noted that, the stator equation is written on the stator reference, rotor windings written on the rotor (where the rotor windings are). In order to refer the rotor equation to a stationary reference frame (same as stator) the second equation of (3.4) has to be multiplied by $e^{jp\theta}$. The following equations can be written as:

$$\begin{aligned} \boldsymbol{V_s} &= r_s \boldsymbol{i}_s + l_s \frac{d}{dt}\boldsymbol{i}_s + L_m \frac{d}{dt}(\boldsymbol{i}_s + \boldsymbol{i}_r^s) \\ 0 &= r_r \boldsymbol{i}_r^s + l_r \frac{d}{dt}\boldsymbol{i}_r^s + L_m \frac{d}{dt}(\boldsymbol{i}_s + \boldsymbol{i}_r^s) - jp\omega_r l_r \boldsymbol{i}_r^s - jp\omega_r L_m(\boldsymbol{i}_s + \boldsymbol{i}_r^s) \\ T &= \frac{3}{2} p L_m \Im m\{\boldsymbol{i}_s \boldsymbol{i}_r^{s^*}\} \end{aligned} \tag{3.5}$$

where $\boldsymbol{i}_r^s = \boldsymbol{i}_r e^{jp\theta}$ is the rotor current referred to stator reference frame. Before converting the reference frame oriented on rotor flux, let us look at the definitions of stator, rotor, and mutual flux with respect to stator and rotor currents.

$$\begin{aligned} \boldsymbol{\Phi_m} &= L_m(\boldsymbol{I_s} + \boldsymbol{I_r}) \\ \boldsymbol{\Phi_s} &= L_s \boldsymbol{I_s} + L_m \boldsymbol{I}_r \\ \boldsymbol{\Phi_r} &= L_r \boldsymbol{I}_r + L_m \boldsymbol{I_s} \end{aligned} \tag{3.6}$$

where $L_s = l_s + L_m \; and \; L_r = l_r + L_m$. This L_s and L_r are the total inductances of stator and rotor.

In order to decouple the components of the stator current necessary to magnetize the machine and that necessary to produce torque, equation (3.4) referring to a reference frame oriented on the rotor flux vector using *Figure 3.26* can be written as:

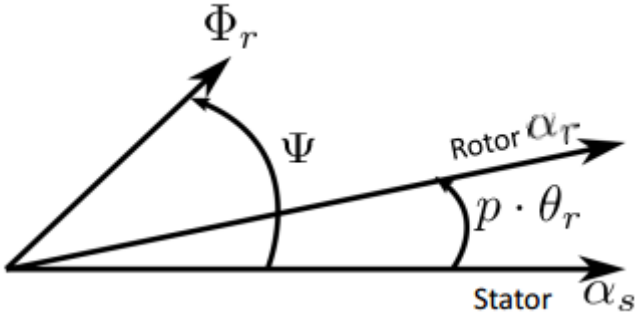

Figure 3.26 Vector diagram of reference frames

$$\begin{aligned} \boldsymbol{V}_s^{\Psi} &= r_s \boldsymbol{i}_s^{\Psi} + L_s \frac{d}{dt}\boldsymbol{i}_s^{\Psi} + L_m \frac{d}{dt}\boldsymbol{i}_r^{\Psi} + j\omega L_s \boldsymbol{i}_s^{\Psi} + j\omega L_m \boldsymbol{i}_r^{\Psi} \\ 0 &= r_r \boldsymbol{i}_r^{\Psi} + L_r \frac{d}{dt}\boldsymbol{i}_r^{\Psi} + L_m \frac{d}{dt}\boldsymbol{i}_s^{\Psi} + j(\omega - p\omega_r)(L_r \boldsymbol{i}_r^{\Psi} + L_m \boldsymbol{i}_s^{\Psi}) \\ T &= \frac{3}{2} p L_m \Im m\left[\boldsymbol{i}_s^{\Psi} \boldsymbol{i}^{\Psi^*}{}_r\right] \end{aligned} \tag{3.7}$$

In equation (3.7), ω is the rotating speed of the rotor flux and $p\omega_r$ is the electrical speed of the rotor with respect to the stator reference frame. As the rotor of the induction motor is short circuited, we are unable to control the rotor quantities. Therefore, by using the flux equations of (3.6), we can refer the rotor current with respect to stator current and rotor flux as,

$$\boldsymbol{i}_{\mathrm{r}}^{\Psi} = \frac{\boldsymbol{\Phi_r}}{L_r} - \frac{L_m}{L_r}\boldsymbol{i}_{\mathrm{s}}^{\Psi} \tag{3.8}$$

By substituting equation (3.8) in (3.7), we can obtain:

$$\begin{aligned} \boldsymbol{V}_s^{\Psi} &= r_s \boldsymbol{i}_s^{\Psi} + (L_s - \frac{L_m^2}{L_r})\frac{d}{dt}\boldsymbol{i}_s^{\Psi} + j\omega(L_s - \frac{L_m^2}{L_r})\boldsymbol{i}_s^{\Psi} + j\omega\frac{L_m}{L_r}\Phi_r + \frac{L_m}{L_r}\frac{d}{dt}\Phi_r \\ 0 &= r_r\frac{\Phi_r}{L_r} - r_r\frac{L_m}{L_r}\boldsymbol{i}_s^{\Psi} + j(\omega - p\omega_r)\Phi_r + \frac{d}{dt}\Phi_r \\ T &= \frac{3}{2}p\frac{L_m}{L_r}\Im m[\boldsymbol{i}_s^{\Psi}\Phi_r^*] \end{aligned} \tag{3.9}$$

This equations (3.9) are referred to the frame oriented on the rotor flux. From the first equation of (3.9), we can calculate the stator voltage required to get desired stator current. And from the third equation of (3.9), it is noted that the torque depends on the interaction of field with the current. In order to decouple the flux and torque equations lets call direct and quadrature axes as the real and imaginary axes of the reference frame oriented on the rotor flux. Projecting rotor equation of (3.9) in direct (d) and quadrature (q) axis it results:

$$\begin{aligned} 0 &= r_r\frac{\Phi_r}{L_r} - r_r\frac{L_m}{L_r}i_{sd} + \frac{d}{dt}\Phi_r \\ 0 &= -r_r\frac{L_m}{L_r}i_{sq} + (\omega - p\omega_r)\Phi_r \\ T &= \frac{3}{2}p\frac{L_m}{L_r}\Phi_r i_{sq} \end{aligned} \tag{3.10}$$

From (3.10), it can be noted that the torque depends only on the quadrature component of stator current oriented on the rotor flux, while the rotor flux is controlled by the direct component of the current:

$$i_{sd} = \frac{\varphi_r}{L_m} + \frac{L_r}{L_m r_r}\frac{d}{dt}\varphi_r \tag{3.11}$$

From (3.11), it is observed that to control the flux, only the direct axis component of stator current is required. Therefore, we can control both the torque and flux separately. Here a PI regulator is used to generate reference of i_{sd} by calculating error between the actual flux and reference flux. In order to implement rotor field-oriented control, it is necessary to know the position of rotor flux at every time. This rotor flux magnitude and position can be estimated by integrating rotor equation in the stator reference frame. The rotor equation from (3.6), considering (3.7) can be written as:

$$0 = \frac{d}{dt}\boldsymbol{\Phi_r} + \left(\frac{r_r}{L_r} - jp\omega_r\right)\boldsymbol{\Phi_r} - r_r\frac{L_m}{L_r}\boldsymbol{i_s} \tag{3.12}$$

Equation (3.12) is a complex differential equation. Integrating this equation, it is possible to estimate the amplitude and phase of rotor flux in the stator reference frame. The equation (3.12) can be written as:

$$\begin{aligned}\varphi_{r\alpha} &= \int\left(\frac{L_m r_r}{L_r}i_{s\alpha} - \frac{r_r}{L_r}\varphi_{r\alpha} - p\omega_r\varphi_{r\beta}\right)dt \\ \varphi_{r\beta} &= \int\left(\frac{L_m r_r}{L_r}i_{s\beta} + \frac{r_r}{L_r}\varphi_{r\beta} + p\omega_r\varphi_{r\alpha}\right)dt\end{aligned} \tag{3.13}$$

From (3.13), the position of rotor flux is found. This is shown in *Figure 3.27* below.

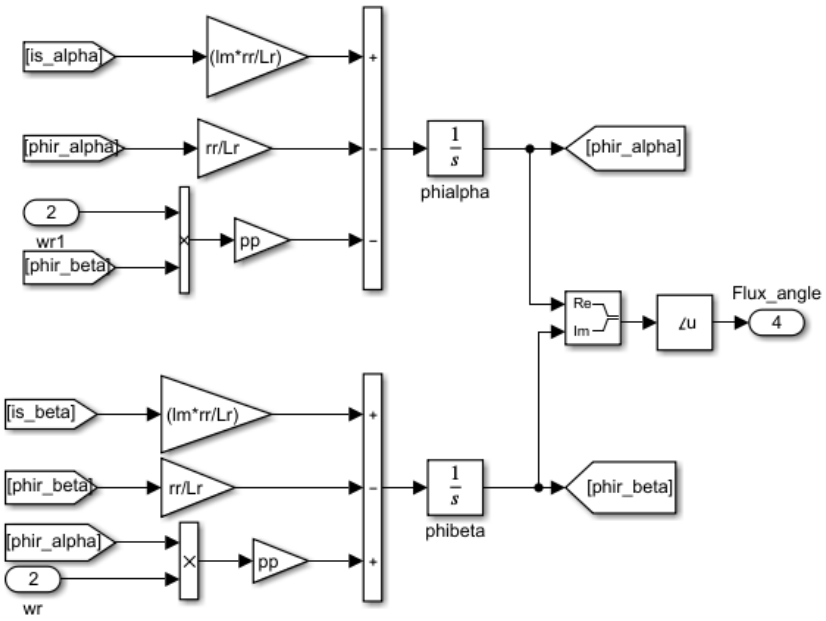

Figure 3.27 Rotor flux position computation

To generate the stator current, it is necessary to control the stator voltage. This is possible by finding the reference voltage, considering (3.9). Rewriting the equation in terms of direct and quadrature axis and rearranging terms, we get the reference voltages.

$$\begin{aligned}V_{sd} &= r_s i_{sd} + (L_s - \frac{L_m^2}{L_r})\frac{d}{dt}i_{sd} - \omega(L_s - \frac{L_m^2}{L_r})i_{sq} + \frac{L_m}{L_r}\frac{d}{dt}\varphi_r \\ V_{sq} &= r_s i_{sq} + (L_s - \frac{L_m^2}{L_r})\frac{d}{dt}i_{sq} + \omega(L_s - \frac{L_m^2}{L_r})i_{sd} + \omega\frac{L_m}{L_r}\varphi_r\end{aligned} \tag{3.14}$$

From (3.14), it is clear that the responses of quadrature and direct axis currents depend only on their voltages. Therefore, we can generate reference voltages by using PI regulator. Considering rotor flux is at steady state (no dynamic control of the rotor flux is implemented). The additional terms here are compensated by feed-forward action. Then the quadrature and direct voltage references, V_{sd} *and* V_{sq}, can be referred back to stator reference frame projected on three-phase by knowing flux position *(Figure 3.28*).

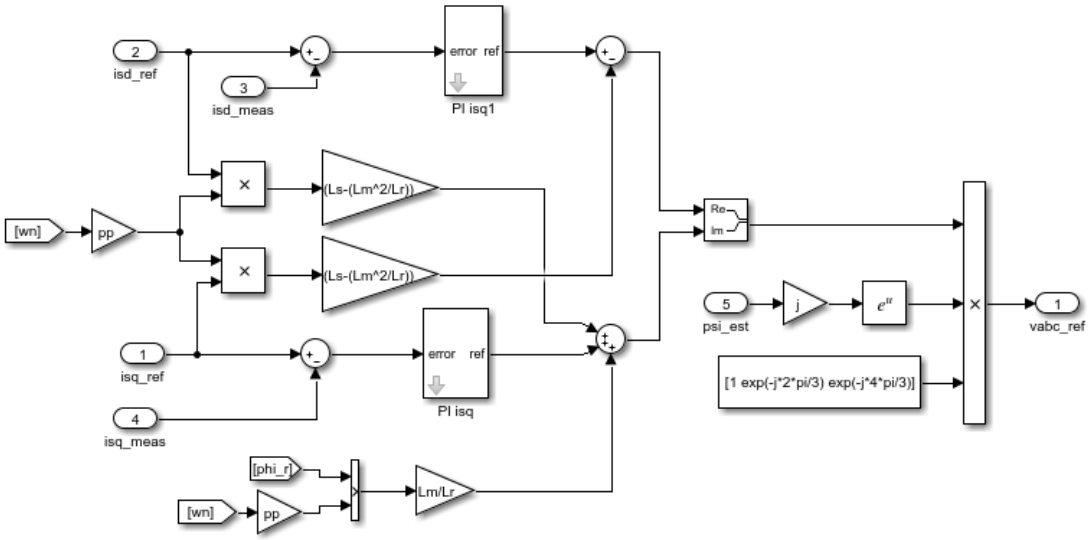

Figure 3.28 Voltage reference computation

The complete scheme of motor control using MMC converter is shown in *Figure 3.29.*

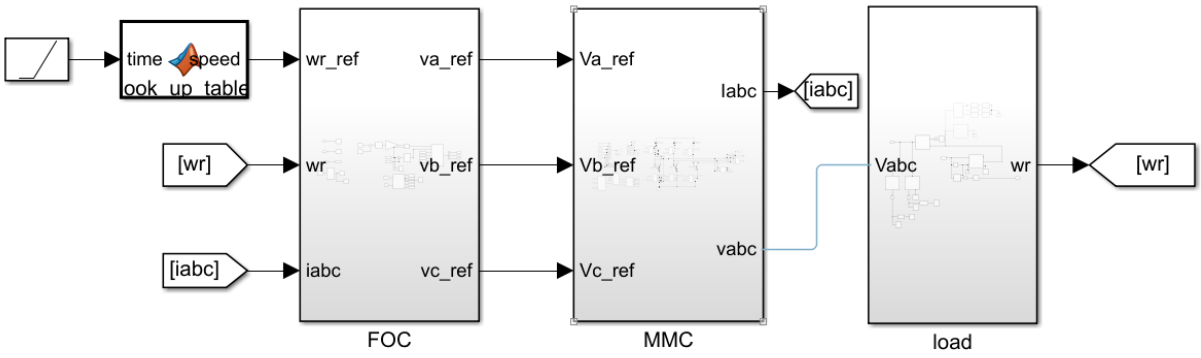

Figure 3.29 Motor control scheme with MMC

3.3.2 Simulation results of motor control

To simulate the above specified motor the parameters of induction motor and Matlab/Simulink simulation parameters are chosen from *Table 3.4* and *Table 3.5*

Simulation parameters	
Simulation time	*15 s*
Simulation step	*5 µs*
Battery charge	*100 mAh*
Initial SoC range	*0.7 to 0.9*
Mutual inductance	*1 mH*

Table 3.4 Simulation parameters for speed control

Induction Motor parameters	***Value***
Nominal Voltage (Vn)	*210V*
Nominal Current (In)	*50A*
Pole pairs (p)	*2*
Moment of inertia (J)	*0.01 kg.m^2*
Drag coefficient (b)	*0.05 Nm.rad/s*
Stator Inductance (Ls)	*78mH*
Rotor inductance (L_r)	*78mH*
Magnetizing inductance (L_m)	*68.7mH*
Stator resistance (r_s)	*0.55Ω*
Rotor resistance (r_r)	*0.4Ω*

Table 3.5 Induction motor parameters

In order to show the field weaking of the motor, the reference speed profile is chosen to have a speed greater than nominal speed for specific time. Referring to the speed profile in *Figure 3.30*, the reference speed is zero for first 0.1 seconds in order to magnetize the machine. Also, it can be seen between 3 and 6 secs, the reference speed is greater than nominal speed. The measured speed of induction machine is reported below in *Figure 3.30*.

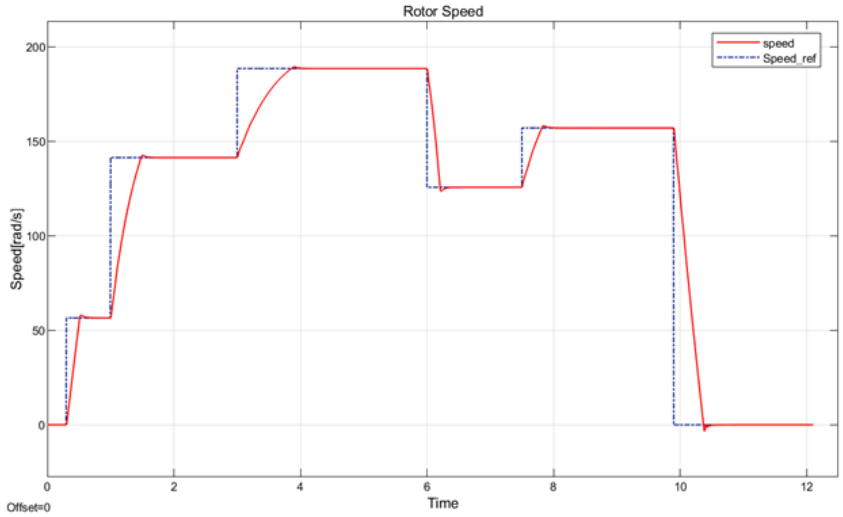

Figure 3.30 Reference and measured speed profile

From *Figure 3.30*, it is observed that our induction motor is following its reference speed. The flux profile during such operation is reported in *Figure 3.31*.

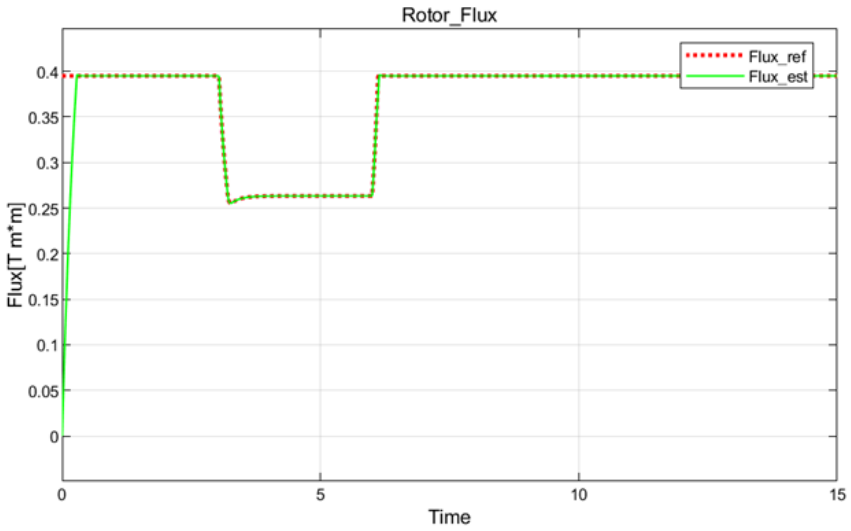

Figure 3.31 Rotor flux module profile

From the *Figure 3.31*, the flux weaking is visible between 3 and 6 secs. This is expected based on the speed profile of the motor. Therefore, speed control of the induction motor is achieved using MMC. Next, we will look at the SoC balancing operation during speed control.

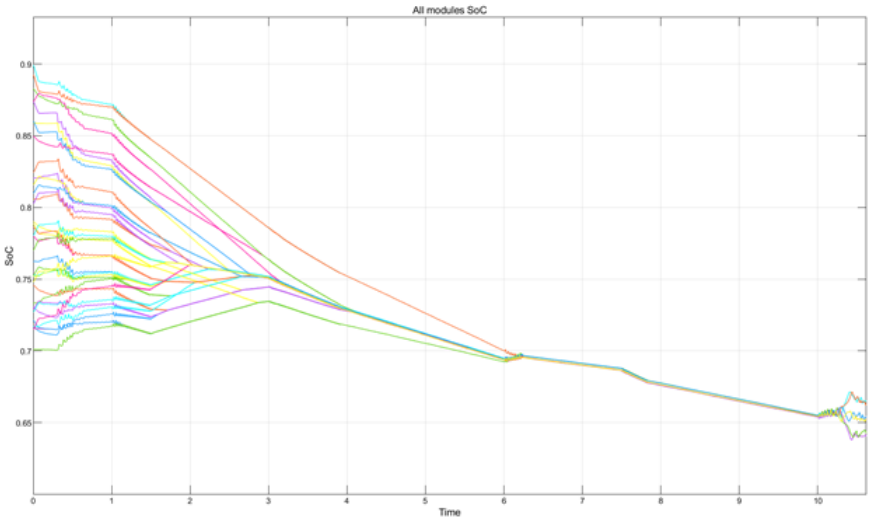

Figure 3.32 SoC balancing during speed control.

All modules SoC are converging to average SoC at about 5s. The speed of convergence depends on the allowable circulating current and on the capacity of the battery. In this simulation, 100 mAh is chosen but, in practical cases, it is much bigger. At approximately 6s, the battery charges for 0.2s. This is due to the fact that at the specified interval, the speed of the motor is greater than the reference speed as shown in *Figure 3.30* i.e., regenerative action.

Also, after 10 seconds in *Figure 3.32,* the SoC balancing is diverging when speed of the motor is 0 rad/sec(*Figure 3.30*). This is due to the reason that the flux reference is nominal even at zero speed. Then the direct stator current responsible to generate flux flows to the motor which shows the drawback in this balancing algorithm. Especially at low frequencies, the upper and lower arm balancing does not work as it depends on alternating voltage reference. In fact, at zero frequency, it is not possible to exchange power between upper and lower arms of the same leg for balancing their average SoC. This phenomenon can be minimized by not fluxing the machine when it is not moving and refluxing when it restarts since electrical dynamics are relatively fast with respect to the driver. Nevertheless, there are ongoing studies to solve this issue and this issue is not furtherly investigated since the main focus of this thesis is realizing the converter.

4 Selection of Components

The main components used in the design of PCB have been analyzed in this chapter. The selection of components is based on the requirements of the MMC board. The components involved in MMC board can be divided into three parts based on its operation:

- Power Part
- Measurement Part
- Communication part

4.1 Power part

Component	***Name***	***Manufacturer***
Optocouplers	*VOH1016AD*	*VISHAY*
	4N25	*VISHAY*
Power MOSFET	*IPP041N12N3 G*	*Infineon*
Gate Driver	*IRS2184*	*International Rectifier*
Insulated DC-DC Converter	*SPBW060F*	*MEAN WELL*
	TMA-1212S	*Traco power*
	TMA-1205S	*Traco Power*

Table 4.1 Component's name with the manufacturer

The main components used in the power part are listed in *Table 4.1*. A short explanation for each component is provided in this section.

4.1.1 Optocouplers

To control the half-bridge MOSFET, a voltage command is given to the gate-driver by using a micro controller. In order to isolate the ground of the micro-controller from the gate driver's ground (battery ground), an optocoupler comprising of a transistor and photodiode has been used. The optocoupler selection is based on its working speed that should be accorded with the module's switching frequency (10kHz). The insulation voltage here is selected as per the application requirement. It must be more than 1000 volts as the MMC board can be connected directly to the three-phase grid of 400V. Two optocouplers are used in our design. One is to provide the gate pulse signal to the driver, and the other is to control the shutdown pin of the gate driver.

4.1.1.1 VOH1016AD Optocoupler

In our design, the optocoupler used to provide the gate pulse signal to the driver is VOH1016AD. The reason for selecting this optocoupler is that its speed must be much greater than 1MHz. This is due to the fact that considering the worst-case scenario for which the duty cycle generated is 1%. This duty cycle has the speed of $100\mu s * 1\% = 1\mu s$ at 1MHz. So, the chosen optocoupler must have a speed much greater than 1MHz. The VOH1016AD chosen for the PCB design has below-mentioned specifications *Table 4.2*.

Speed	I_{th}***(ton)***	***Vcc***	I_f***(output)***	T_{rise}	T_{fall}	***Insulation***	***Vf***
2MHz	*2mA*	*15V*	*50mA*	*0.05µs*	*0.04 µs*	*5kV(rms)*	*1.1V*

Table 4.2 Main parameters of VOH1016AD

From the *Table 4.2*. we can say that it has a speed of 2 MHz and insulation voltage of 5kV which is greater than the required value. It has an input threshold of 2mA to turn on the input LED integrated with optical photodiode in order to produce the output. It can also work with the voltage supply of 15V and 50mA to have strong output signal in case of lengthy connection path and to reduce the effects of induced noise. This optocoupler can be turned-on using a microcontroller with an output voltage of 3.3V and maximum current for 4mA in each pin [40].

4.1.1.2 4N25 Optocoupler

In our design, the optocoupler used to provide voltage command to the shutdown pin of the gate-driver is 4N25 optocoupler. The command given from the master microcontroller is either continuously high or low. For this reason, optocoupler with less speed is chosen with the threshold current and voltage compatible with the values of the master microcontroller. The 4N25 is chosen [41] for the PCB design and its specifications are reported in *Table 4.3*.

Insulation	T_{rise}	T_{fall}	***Vf***	$Iout_{max}$
5kV(rms)	*2µs*	*2µs*	*1.3V*	*50mA*

Table 4.3 Main parameters of 4N25 optocoupler

4.1.2 Power MOSFET

In modular multilevel converters, each module consists of two semiconductors to form a half-bridge. The selected semiconductors must have low conduction and switching losses. The conduction losses can be reduced when the semi-conductor is in ON-state having low ON-resistance in order of milli-ohms. The switching losses occur when the device is transitioning

from conduction to blocking state or from blocking to conduction state. The semiconductors must also be selected considering the rise and fall times. These rise and fall times are directly proportional to parasitic capacitance at the junction of the semi-conductor. The device with low parasitic capacitance, having rise and fall time in the order of ten of nanoseconds, results in low switching losses. We know the current and voltage ratings of the MMC module as 50A and 60V. Hence, in order to have a reasonable margin, the chosen semiconductor device should have a blocking voltage greater than or equal to 90V. From the above considered reasons, MOSFETs have been used in our design. Here the current rating of the MOSFET should be greater than the module current rating.

With the above-mentioned considerations and available MOSFET in the market, an N-channel MOSFET (IPP041N12N3 G) is chosen which has high gate resistance. i.e., it requires less current to command the gate signal. The MOSFET selected [42], [43] has below-mentioned parameters as shown in the *Table 4.4* and *Table 4.5*.

Vds	***Idmax***	***Rds***	***Vgs***	***Pdiss***	***Max temp***	***Rthjun-case***	***Rg***
120V	*120A*	*3.8mΩ*	*±20V*	*300W*	*175°C*	*0.5K/W*	*1.2Ω*

Table 4.4 MOSFET voltage, current, and conduction loss parameters

Ciss	***Coss***	***Crss***	***Td(on)***	***Td(off)***	***Tr***	***Tf***
10400pF	*1320pF*	*61pF*	*35ns*	*70ns*	*52ns*	*21ns*

Table 4.5 MOSFET switching losses are parasitic capacitance parameters

where V_{ds} is the drain-source (blocking voltage), Id_{max} is the maximum allowable current, R_{ds} is the ON-resistance, V_{gs} is the maximum allowable gate-source voltage, P_{diss} is the maximum power dissipated, R_g is the gate resistance, $C_{iss,}$ C_{oss} and C_{rss} is the input, output, reverse transverse capacitance, $Td_{(on)}$ and $Td_{(off)}$ is the ON and OFF delay times, T_r and T_f is the rise and fall times of the MOSFET.

From the *Table 4.4,* we can see that the ON-resistance (drain to source resistance) of the selected MOSFET is 3.8mΩ. Therefore, the maximum power dissipated during conduction is as follows.

$$P_{diss_{max}} = R_{ds} I_{max}^2 = 50A^2 * 3.8m\Omega = 8W.$$

Also, the MOSFET IPP041N12N3 G has an internal gate resistance of 1.2Ω which plays a crucial role in reducing the noise and reducing the ringing caused by parasitic capacitance and inductance in the gate driver path. The thermal resistance of the selected MOSFET is 0.5 K/W and has a high dissipation power of 300W which is high enough from our power limit of 8W.

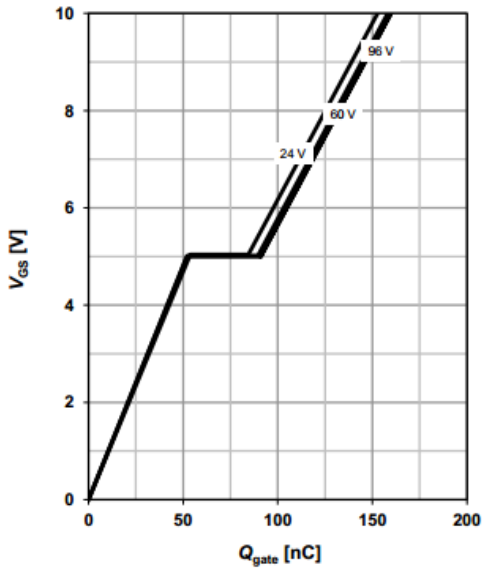

Figure 4.1 MOSFET gate charge with respect to Vgs

Referring to *Figure 4.1*, the gate capacitance with respect to the gate-source voltage is analyzed. At the gate-source voltage of 10V, the gate charge of the selected MOSFET is approximately 160 nC. Here the input, output and reverse transfer capacitances are in the order of ten- nano farads as shown in *Table 4.5*. From this, the rise and fall time are 52 and 21 ns respectively which result in low switching losses and the gate-source voltage is ± 20V. To turn ON the MOSFET +12V is given and to turn OFF -5V is given instead of 0V. It is due to the fact that the oscillations produced by parasitic elements during high load currents can reach higher than the threshold voltage of the MOSFET which may result in undesired switching of MOSFETs during turn-off command i.e., especially during the transition phase.

4.1.3 Gate driver

The main purpose of the gate driver is to provide a proper command to the semiconductor switches. In our design, it is a N-channel MOSFET which is used to turn ON and turn OFF based on the signal received from the master microcontroller. As we discussed in the above section, it is important that our driver should produce negative voltage with respect to the source terminal of the semiconductor switch in order to turn OFF the MOSFET and avoid

improper switching during transition. The driver should also operate at the voltage higher than the +10V with respect to the source terminal of MOSFET in order to achieve minimum drain-source resistance $R_{ds,min}$. The fall time and rise time of the gate driver should be less than the MOSFETs rise and fall time to achieve proper switching. Next, to turn on the upper MOSFET in half-bridge, we need to provide a gate-source voltage with respect to the source terminal of the upper MOSFET i.e., output terminal. The maximum voltage at output terminal in our prototype is the voltage of the battery consisting of 14 cells. When it is fully charged, the output of the battery will be $14 * 4.2 = 58.8V$, therefore the driver must be able to provide upper MOSFET gate-source voltage with the combined voltage of $V_s + V_{gs}$ where V_s is the voltage at source terminal of the upper MOSFET. Another main parameter considered while selecting the driver is the high pulsed output current in order to charge the gate capacitance quickly. The driver should also be capable of producing deadtime if we are using a half-bridge driver. This is to avoid short circuit of the DC side of the module.

By considering all the above conditions and the gate drivers available in the market, the best choice is IRS2184 [44], and the key specifications of this driver are mentioned in *Table 4.6.*

DT	***Tr***	***Tf***	***Vcc***	***Vs***	I_o^+	I_o^-	***Vb***
400 (ns)	*40ns*	*20ns*	*20*	*600*	*1.9A*	*2.3A*	*Vs+Vcc*

Table 4.6 Main parameters of the gate driver

Referring to the *Table 4.6*, the supply voltage of the gate driver V_{cc} can work up to + 20V. Therefore, we will have a wide range of available voltage to turn on the MOSFET. The chosen gate driver can drive MOSFETs with voltage up to 600V. Upper MOSFET source is connected to the output terminal having a maximum voltage of 60V in our prototype, which is much less than 600V. The driver has a peak current of 2.3 A which allows fast charging of the gate (whose charge is 160nC as shown in *Figure 4.1.* The internal circuitry of the IRS2184 gate driver is reported in *Figure 4.2***.**

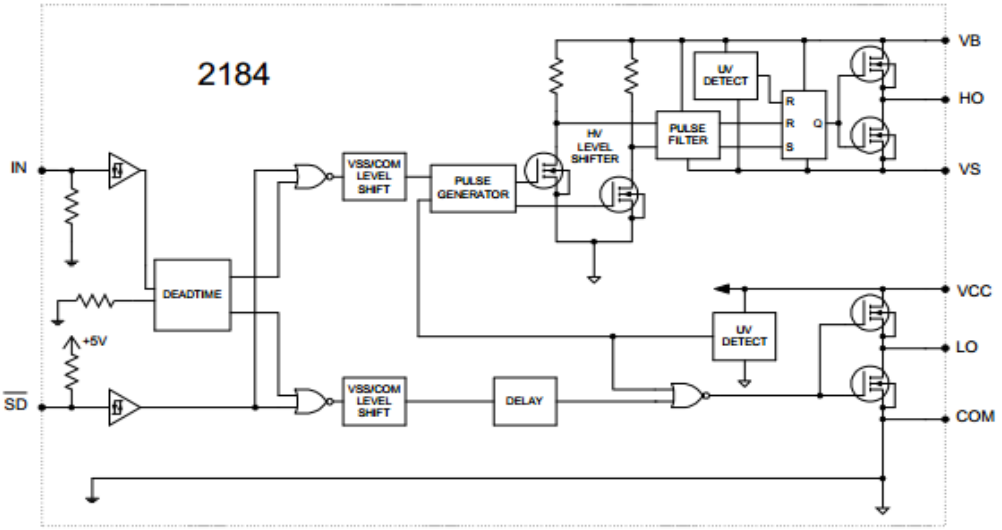

Figure 4.2 Functional block diagram of IRS2184 gate driver

The points LO and HO are the gate pulse voltage commands given to the MOSFETs with respect to their source voltages. Another main feature of the gate driver IRS2184 is that it has a shutdown pin. Using this, it is possible to control the gate driver with the external command given from the master microcontroller to turn ON or OFF during abnormal conditions. Here to provide *Vb* with respect to its source, usually a bootstrap capacitance is used. But in modular multilevel converter configuration, some of the modules (one which turned ON primarily)[5] have been switched ON for a longer time to charge or discharge the battery based on current direction and sorting algorithm. Therefore, to ensure constant gate voltage for a longer period, separate isolated DC-DC converters are used. By this, we produce the constant required voltage instead of the bootstrap capacitance.

4.1.4 Insulated Converters DC-DC

For supplying the components such as gate driver and to perform the bootstrap application, we need an insulated converter whose insulation is greater than 1000V. Each module will be supplied by an external source at 24V which is the main supply for all the components in the module. From that supply, we need 12V with respect to the lower MOSFET source terminal (battery reference terminal) and 12V with respect to the higher MOSFET source terminal (output terminal). Again, to turn OFF the higher MOSFET, -5V with respect to both source terminals is required. Therefore, we will use an insulated DC-DC converter. Additionally, the

[5] Depend on the sorting algorithm the MOSFET which is turned on primaly will be connected for longer time either to charge the module or discharge the module to achieve module balancing.

gate driver input requires 12V and -5V with respect to the battery terminal. Therefore, to get the required voltage with the input supply of 24V, different insulated DC-DC converters is required.

4.1.4.1 SPBW060F

Input supply to the MMC module is 24V and the components inside the module will work at either 12V or -5V. Therefore, it is required to convert 24V to 12V supply. Also, it should be insulated from the input supply ground (digital ground) with minimum isolation of 1000 volts, The chosen insulated converter should have high current rating in terms of hundreds of mA to provide the current required for all the components in the module. Therefore, SPBW060F is chosen [45] with the specifications reported in the *Table 4.7*.

V_{in}	V_{out}	$V_{out}accuracy$	I_{out}	Insulation	efficiency
(9-36) V	*12V*	*±1.5%*	*500mA*	*1.5kV*	*89%*

Table 4.7 Main parameters of SPB060F DC-DC Converter

Since the input supply 24V is coming from outside, a wide range of input voltage is chosen i.e., 9 to 36V. The power rating of this converter is 6W which can produce a maximum of 500mA. Here the assumed consumption current of the whole module is 50mA. The maximum ripple that can be produced at the output of this converter is very low i.e., typically 100mV_{p-p} with an accuracy of 1.5%. Hence the output voltage of the system is almost constant.

4.1.4.2 TMA-1212S

To produce the 12V with respect to the higher MOSFET source terminal, TMA-1212S insulated converter is selected [46]. As discussed earlier, we will use a DC supply instead of a bootstrap capacitor. It is able to produce continuous current in order to charge the gate capacitance. Here the peak current is carried by the capacitor which is placed between the terminals. The current required to charge the gate can be calculated from *Figure 4.1* considering $Iout_{DC-DC} = 175nC * 10kHz = 1.7mA$. The selected DC-DC converter characteristics mentioned are reported in *Table 4.8*.

Vin	Vout	$Iout_{max}$	Insulation	Accuracy
12V	*12V*	*84mA*	*1000V*	*10%*

Table 4.8 Main parameters of TMA-1212S

4.1.4.3 TMA-1205S

Similarly, to provide -5V supply with respect to the source terminal of the both MOSFETs, another insulated DC-DC power supplies are required. Therefore, TMA-1205S is chosen with main specifications reported in the *Table 4.9.*

Vin	***Vout***	$\boldsymbol{Iout_{max}}$	***Insulation***	***Accuracy***
12V	*5V*	*200mA*	*1000V*	*10%*

Table 4.9 Main parameters of TMA-1205S

4.2 Measurement part

In this section, measurement part components is discussed. Whose functioning and connections are described briefly in the next chapter. To calculate the voltages of the whole battery and of each cell, measurement device is required. In our prototype each battery consists of 14 cells, we need to choose the measuring device which is able to take 14 cells input and measure the voltage of the each of them. Then the measured voltages are sent to the master microcontroller through serial communication (I2C). The chosen components in the measurements part are tabled with their manufacturer names and number in *Table 4.10.*

Component	***Number***	***Manufacturer***
Battery Management System	*LTC6812*	*Analog devices*
Signal transformer	*SM91051ALE*	*BOURNS*

Table 4.10 Measurement part components with manufacturer

4.2.1 LTC6812

Based on requirements and the components available in the market, LTC6812 is the best choice [47] for our MMC configuration. The LTC6812 can measure 15 cells battery input with an error of less than 2.2mV per cell. It has the measurement speed of 256 µs which can be adjusted for filtering the noises. If the speed is high, noise elimination is low and if the speed is low, the noise elimination is high.

In our modular multilevel converter, each leg consists of 12 modules and all the modules can be connected with a daisy-chain using a single measurement controller. Using the master battery monitor IC[6] (first module in each leg), the data of all the modules is measured. Here we

[6] Master battery monitoring IC refered as the module which is communicating with measurement controller or the module which is configured with 4-wire communication.

can supply the battery monitoring device either using a battery or with an external 5V supply. In the proposed MMC configuration, external 5V supply is used. When any cell in the stack of battery is damaged, this battery monitoring device is able to communicate with the master microcontroller using over-voltage and under-voltage protection. To measure the cell voltages, it consists of a delta-sigma ADC with 16 bit resolution. This ADC has high resolution measurement with more accuracy and programmable noise filter. This device consists of 9 I/O pins which can be used for temperature measurement to measure the temperature and send the signal to the master microcontroller.

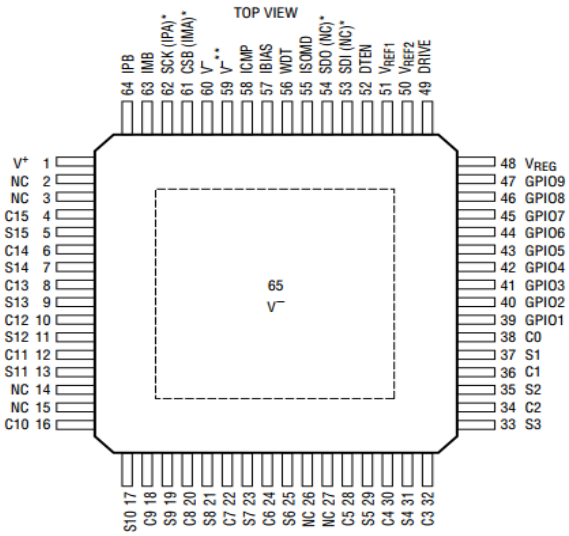

Figure 4.3 Pin layout diagram of LTC6812

The Layout diagram of the LTC6812 battery management system is shown in *Figure 4.3.*

Voltage	***Imax***	***ADC resolution***	***Communication***	***GPIO***	***Max Measurement error***
5V	*35mA*	*16bit*	*I2C/SPI*	*9*	*2.2mV*

Table 4.11 Main parameters of LTC6812

Another main feature of LTC6812 is that we can configure the ADC to work on different modes corresponding to different oversampling ratios. It has a fast mode with low noise rejection, normal mode, and a filter mode of 26 Hz which has very high noise rejection. A detailed discussion of LTC6812 is presented in the PCB design section**.**

4.3 Communication part

4.3.1 Signal transformer

The multiple LTC6812 devices of each module are connected in daisy chain isoSPI configuration. Since the ground of each module is different from the other modules, an isolation barrier is required to send the differential communication pulse. For this reason, the SM91501ALE transformer is chosen. The schematic of the transformer is reported in *Figure 4.4*.

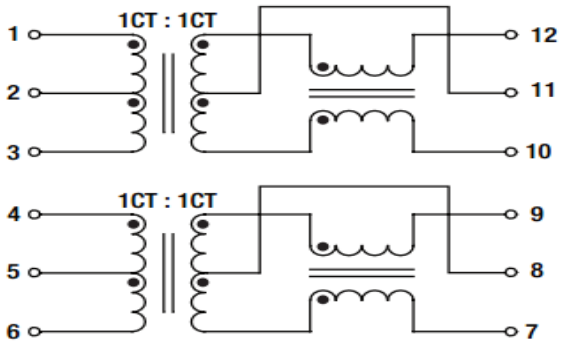

Figure 4.4 schematic of SM91501ALE signal transformer

The main specifications of the signal transformer SM91501AL are listed below in *Table 4.12.*

voltage	***Turns ratio***	***Leakage inductance***	***Open circuit inductance***	***Temp range***
1600V	*1:1*	*0.5µH*	*450µH*	*125 °C*

Table 4.12 Main parameters of SM91501ALE signal transformer

The daisy-chain connection of our modules may lead to an increase in the noise susceptibility in the communication part. Therefore, additional filtering is needed for high levels of noise reduction in electromagnetic interference. For providing this filtering, a transformer with common mode choke is selected to add common mode noise rejection from transients on the battery line. Since our communication has differential signals, common mode noise can be reduced with the use of a center-tapped transformer as shown in *Figure 4.5*. It also provides additional noise rejection by creating a low impedance path to the common-mode noise.

The daisy-chain connection of the LTC6812 and the transformer is shown in *Figure 4.5.*

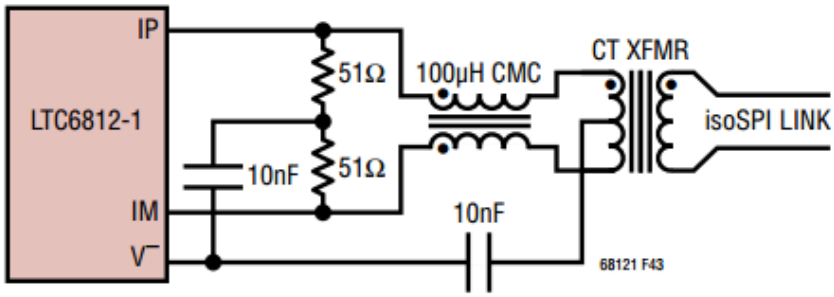

Figure 4.5 Connections of SM91501ALE signal transformer

While connecting the signal transformer to the LTC6812 following layout guidelines should be considered for better noise immunity of a data link.

- The signal transformer should be at least 2cm away from the LTC6812 to isolate the IC from magnetic field coupling.
- The signal transformer should be placed close to the isoSPI cable connector. Its path must be as direct as possible and isolated from both the adjacent circuitry and the ground metal.
- The ground plane of V^- should not be present under the signal transformer to reduce the leakage currents caused by the transformer magnetic field and the ground plane.

5 Hardware Design

In the previous chapter, the main components required for MMC module is selected. In this chapter, we will discuss the schematic by splitting the power part into the supply part, driving part, and output part. In each part, a detailed discussion about the connection is carried out. Later the measurement and communication part have also been discussed. Finally, the board design and placing of components in the board for reducing EMC noise is discussed.

5.1 Designing of Schematic

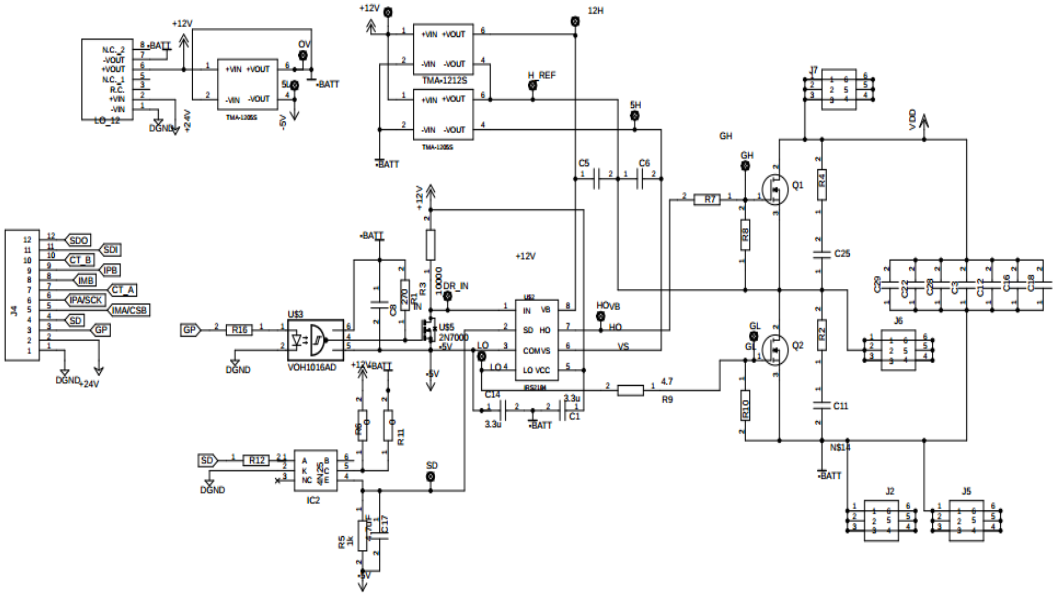

Figure 5.1 power part PCB

Referring to the *Figure 5.1*, there is a 12-pin connector which is used for the communication in the module such as external supply, master controller, between the boards, and measurement controller. Starting from the bottom of the J4 connector, pins 1 and 2 are to connected to the 24 V power supplier.

5.1.1 Supply Part

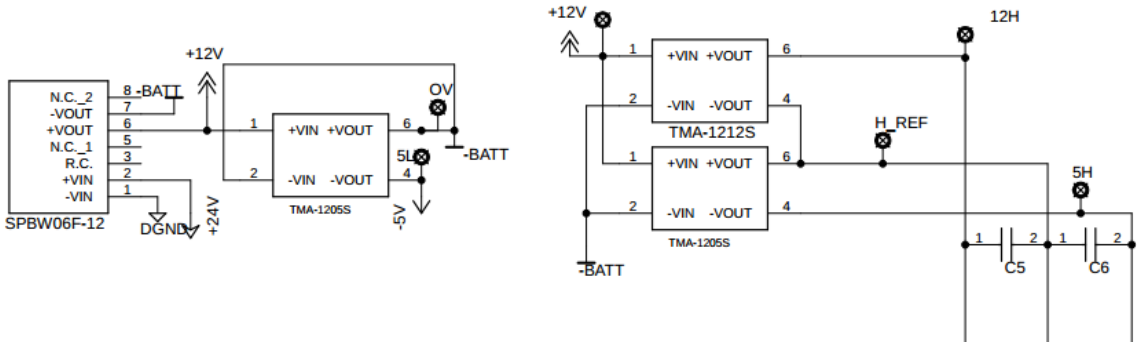

Figure 5.2 supply part PCB

The schematic of the supply part has been reported in *Figure 5.2***.** The external power supply of 24 V will be converted to 12V with respect to the battery ground which is the reference of our module by means of an insulated DC-DC converter, called SPBW06F-12. This has an input range of 9-36 V. A wide input range is selected, since the 24 V is coming from the external which might result in higher loop inductance causing fluctuations in input voltage. The 12V power supplier provides a constant output voltage 12 V with maximum current of 500 mA.

The output of the SPBW06F-12 converter is given to the supply for the gate driver. The 12V with respect to battery ground is again converted to 12V with respect to the source terminal of *Q1* MOSFET by another TMA-1212S insulated DC-DC converter. For turning OFF the *Q1* and *Q1* MOSFETs[7], -5V supply with respect to the half-bridge MOSFETs sources is provided. This is to avoid undesired switching of the MOSFETs as ripples on *Vgs* are caused by the loop inductance in the switching phase of the semiconductors. For this purpose, two insulated DC-DC converters of TRACO POWER TMA-1205S are taken to produce -5V with respect to the sources of half-bridge MOSFETs. To obtain -5V with respect to battery reference, the COM[8] pin of the driver is connected to -5V supply.

The capacitors *C1* and *C6* are dimensioned in such a way to provide the peak current which is responsible to charge the gate capacitance of MOSFETs and also to reduce the noise caused by parasitic elements. At present, it is chosen to be 3.3 uF but after testing, it can be modified by considering the noise of the system during the load testing.

[7] *Q1* MOSFET refers half-bridge converter upper MOSFET, *Q2* MOSFET refers half-bridge converter lower MOSFET,

[8] To provide -5V with respect to battery reference, the gate driver reference is connect to -5V. Therefore, when gate driver provides low signal, it is -5V with respect to the battery terminal.

5.1.2 Driver input part

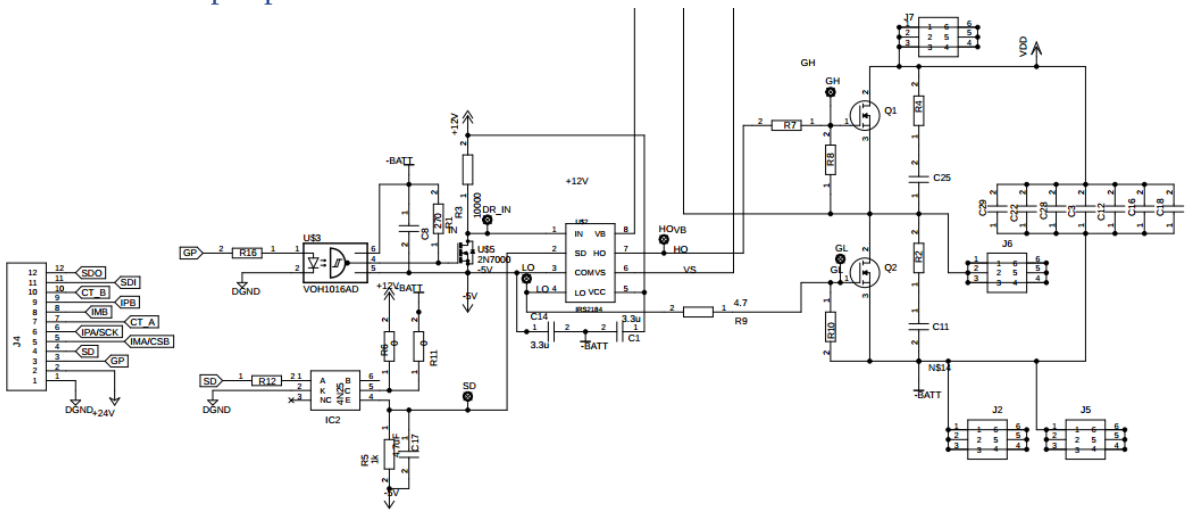

Figure 5.3 Driver part PCB

The detailed schematic of the driver part is shown in *Figure 5.3.* the Pin 4 from the connector J4 in *Figure 5.3* is responsible for providing a logic command to the shutdown pin of the gate driver. Pin 3 sends the gate pulse command by comparing reference signal with PWM signal in the master microcontroller with the output maximum voltage of 3.3V and current 4mA to the gate driver. Therefore, *R16* is dimensioned considering the maximum voltage from the master controller and voltage drop across the photodiode of the optocoupler (i.e., 1.1V) reported in *Table 4.2*.

$$R16 = \frac{3.3V - 1.1V}{4mA} = 550\Omega$$

A common resistor available in the market is selected whose value is 560 Ω. In order to ensure common reference for both optocoupler and gate-driver, the optocoupler's reference is also connected to -5V supply. Here the positive terminal of the optocoupler is connected to *-BATT* to provide 5V supply. The capacitor *C8* is used for reducing the noise in the system. Since the optocoupler is working in negated logic, we need another negation to provide proper output to the driver. This is performed by a general MOSFET 2N7000.

The output of VOH1016AD is connected to the gate of the 2N7000 through a pull-up resistor. Therefore, when the master controller sends the signal HIGH, the output of VOH1016AD is LOW, *Vgs* of the general MOSFET 2N700 is LOW. Hence the driver input will be 17V with respect to the *COM* terminal of the driver which is a HIGH signal for the input of the driver. Similarly, when the master controller sends a LOW signal, *Vgs* of 2N700 is HIGH, then the

input of the driver is -5V with respect to the negative terminal of the battery. In this way, we can achieve proper switching pulses from the master controller to the input of the driver.

Similarly, for providing a command to shut down pin *SD*, the low speed optocoupler 4N25 is used. The resistor *R12* is dimensioned by considering the forward voltage drop of the photodiode which is reported in *Table 4.3***.** The value of the resistor is dimensioned as

$$\mathrm{R12} = \frac{3.3V - 1.3V}{4mA} = 500\Omega$$

The resistor *R5* is calculated to limit the current flow and to provide the voltage required for the proper command to the *SD* pin. The maximum current that the transistor can handle is 50mA as reported in *Table 4.3*. *R5* is taken as 1kΩ, therefore maximum forward current from the transistor will be $I_{out} = \frac{17}{1000} = 17mA$. This value is inside the permissible limits of the maximum output current of the transistor. The capacitor *C17* is required to eliminate the disturbance in the system caused by parasitic elements.

The resistors *R7* and *R9* are external gate driver resistances. They play a major role in limiting the noise and ringing in the gate driver path caused by parasitic inductance and capacitance. The resistors *R8* and *R10* are pull-down resistors for the half-bridge to undesired turn ON of the MOSFETs when the module is not supplied.

During the transition, the MOSFET can produce high-frequency ripples proportional to the load current. To reduce these ripples, a snubber circuit consisting of resistors *R2* and *R4* with capacitors *C11* and *C25* are added between the drain and source of the MOSFETs. The resistor and capacitor value selected are 1.2Ω and 0.47µF, respectively. After testing the PCB, its value is changed based on the issues raised which have been discussed in the section involving hardware testing.

5.2 Measurement Part Schematic

The schematic of the measurement part is reported in *Figure 5.4*

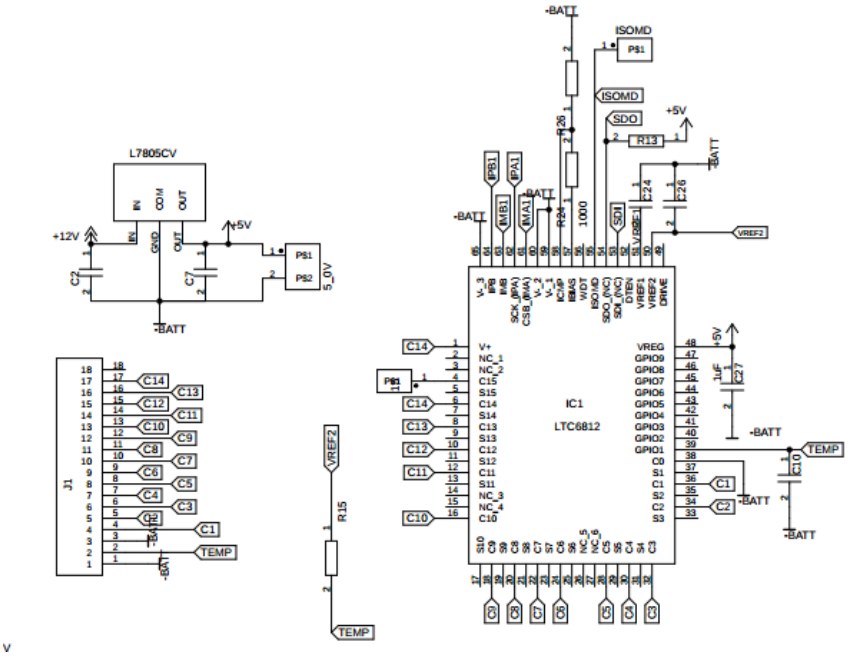

Figure 5.4 Measurement part PCB

From the left, there is J1 connector with 18 pins, of which the first 2 pins are used for measuring the temperature of the battery and the remaining pins are used to connect the cell voltages to the LTC6812. From the top left, there is the LM7805 voltage regulator which is responsible for providing 5V supply to the LTC6812 chip. The capacitor *C2* and *C7* are decoupling capacitors that are used to reduce the noise and are placed close to the battery management chip supply pin.

This LTC6812 can measure the cell voltages and, if opportunely tuned it can also balance the cell voltages with a passive balancing method. At present, we are using this chip only to measure the battery voltage i.e., only *C1* to *C15* pins of LTC6812 where the pins S1 to S15 are left unconnected. Since LTC6812 can measure 15 cells and our battery consist only of 14 cells, the *C15* can be left unconnected or it can be connected to the highest cell i.e.,14^{th} cell. Therefore, *C15* is connected to a pin 1 in order to check both the operations. Here the pin V^+ is connected to the highest cell as its voltage should be greater than or equal to the top cell voltage. The pin V^+ is responsible in providing power to the high voltage elements in the core circuit of LTC6812.

The pins *C0* to *C14* are connected from the battery reference to the 14 cells of the battery. The pin GPIO1 (general-purpose input-output pin) is used to measure the temperature of the battery. The capacitor *C10* of 1uF is used to eliminate the noise of parasitic elements. The Pin 48 is connected to the output of LM7805 with the capacitor *C27* which is used to eliminate the disturbance in the system caused by parasitic elements. The pins 49 and 50 of LTC6812 are reference voltages for measurements. *VREF1* is reference ADC voltage to measure the cell voltages and *VREF2* buffered second reference voltage to drive multiple 10k thermistors for measuring the temperature in the battery. The pins 49 and 50 are bypassed with 1uF capacitor to reduce the noise caused by parasitic elements.

The pin 55 is *ISOMD* is for selecting serial interface mode. To configure pins *53,54,61* and *62* i.e., chip selection bit *(CSB),* serial clock *(SCK),* serial data in *(SDI),* and serial data out *(SDO)* respectively to a 4- wire serial interface configuration, *ISOMD*[9] is connected to *V_*. To configure the battery management chip as a 2-wire communication isolated interface (isoSPI), *ISOMD* is connected to V_{reg}. In our prototype first board should be configured as 4-wire and subsequent board should configure as 2-wire configuration. Therefore, *ISOMD* pin is connected to the 1-pin connector to connect either *V-* or V_{reg}. The pin *SDO* is an open drain NMOS output pin. Therefore, it requires a 5K pull-up resistor. In proposed MMC, the first module of each leg will be configured as 4- wire serial mode interface and all the other modules are configured as 2- wire serial mode interface connected in a daisy chain.

5.2.1 Communication Part Schematic

To communicate with the other modules, LTC6812 consists of 2 ports for serial configuration which are *port A* and *B. Port A* can be configured as a 2-wire or 4- wire interface based on an *ISOMD* pin connection. *Port B* is always configured as MASTER port and has a 2-wire configuration. The communication is initiated by measurement chip[10] in the first module of each MMC leg which is configured as a 4- wire communication in *port A* and all the subsequent modules configured as 2- wire connected in a daisy chain with simply twisted wires. The final module in each MMC leg is terminated with a resistor.

[9] Depends on the *ISOMD* pin connect module will be configured either 4-wire or 2-wire configuration.
[10] Measure chip used in proposed module is ATmega328 controller. i.e., arduino board.

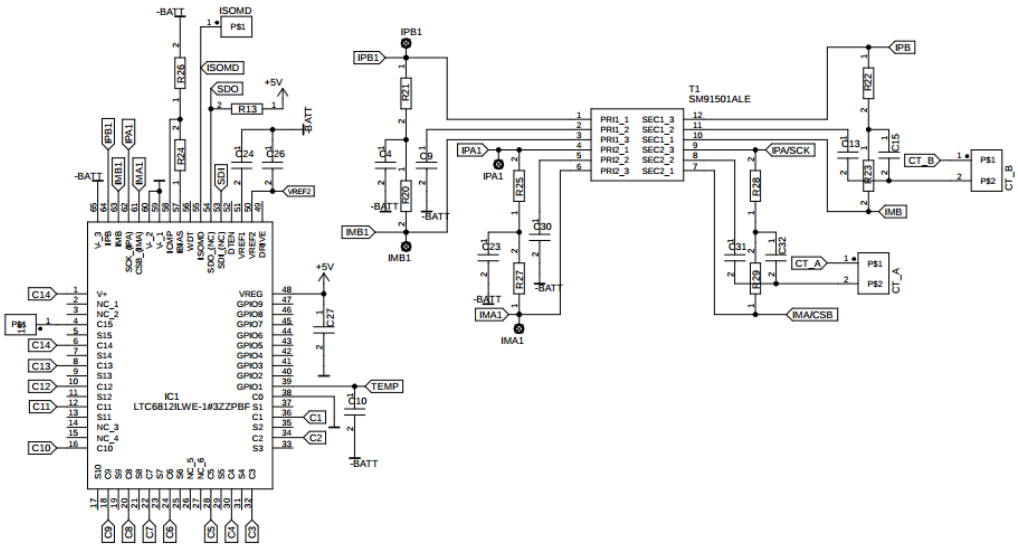

Figure 5.5 Communication part PCB

The strength of the differential interface is set by two external resistor *R24* and *R26* where the voltage divider is connected to the *IBIAS* pin. This pin is connected with the internal 2V supply with respect to the module reference as shown in *Figure 5.6.*

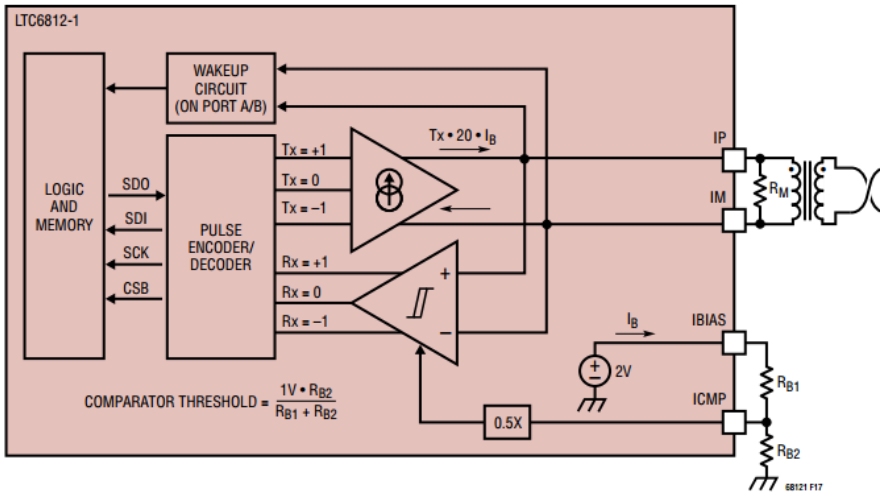

Figure 5.6 Circuit of isoSPI interface

In *Figure 5.6 R24* and *R26* are mentioned as R_{B1} and R_{B2}. The midpoint of the voltage divider is connected to the pin *ICMP* to receive the threshold voltage[11]. The resistor selection for a

[11] Input threshold voltage of LTC6812 is configured using *ICMP* pin. Therefore, if input signal is gereater than the configured threshold, then LTC6812 will detect the signal.

voltage divider is based on the trade-off between the power consumption for communication and signal losses due to noises. The current range for I_{Bias} is from 100µA to 1mA.

- If *R24* and *R26* is high, then I_{Bias} current will be less which results in less power consumption for communication in READY and ACTIVE states, but the signal strength will be low. Therefore, high susceptible for the disturbance.
- If *R24* and R*26* is low, then I_{Bias}current will be high which results in higher power consumption for communication in READY and ACTIVE states, but signal strength will be high. Therefore, less susceptible for the disturbance.

In the proposed MMC, the 12 modules are connected as a daisy chain externally with twisted wire cables which are susceptible to disturbance. Therefore, a resistor is selected to allow a maximum current of 1mA. Here the resistor *R24* and *R26* can be calculated as,

$$I_{Bias} = \frac{2V}{R_{24} + R_{26}} = 1mA$$

Therefore, their values are, $R24 = R26 = 1\ k\Omega$

The output current for serial configuration is 20 times the current passing through the *IBIAS.* Hence the drive current calculated is,

$$I_{DRV} = I_{IP} = I_{IB} = 20 * I_{Bias} = 20mA$$

The threshold strength of a receiving end is adjusted by connecting to the *ICMP* pin and voltage divider mid-point. The V_{ICMP} can be calculated as,

$$V_{ICMP} = 2V\,\frac{R26}{R24 + R26} = 1V$$

Therefore, the receiver comparator will detect the pulse whose amplitude is greater than V_{TCMP}, which can be calculated as half of the V_{ICMP} as shown in the above *Figure 5.6.*

$$V_{TCMP} = 0.5 * V_{ICMP} = 0.5V$$

The resistors *R20, R21, R22, R23, R25, R27, R28,* and *R29* are splitted terminating resistors, Also, the capacitors *C4, C23, C31,* and *C34* are connected to the center tap of the transformer and are bypassed with a 10nF capacitor to increase the noise immunity and create a low impedance path for common-mode noise. As our communication is a differential signal, the

common mode noise will be eliminated. Therefore, the final connection of multiple devices in the daisy chain will be similar to the below mentioned *Figure 5.7.*

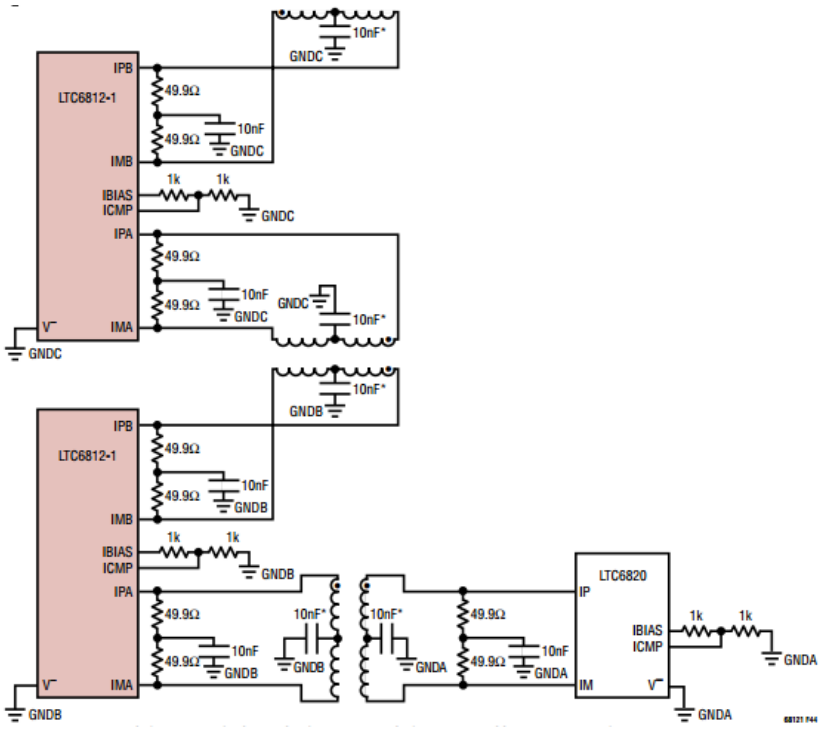

Figure 5.7 Daisy chain interference with different modules

5.3 Board design

The overall board design is shown in the *Figure 5.8.* This board consists of 4 layers in which third layer is dedicated to ground layer to reduce the EMI susceptibility, cross talk and to avoid ground loops.

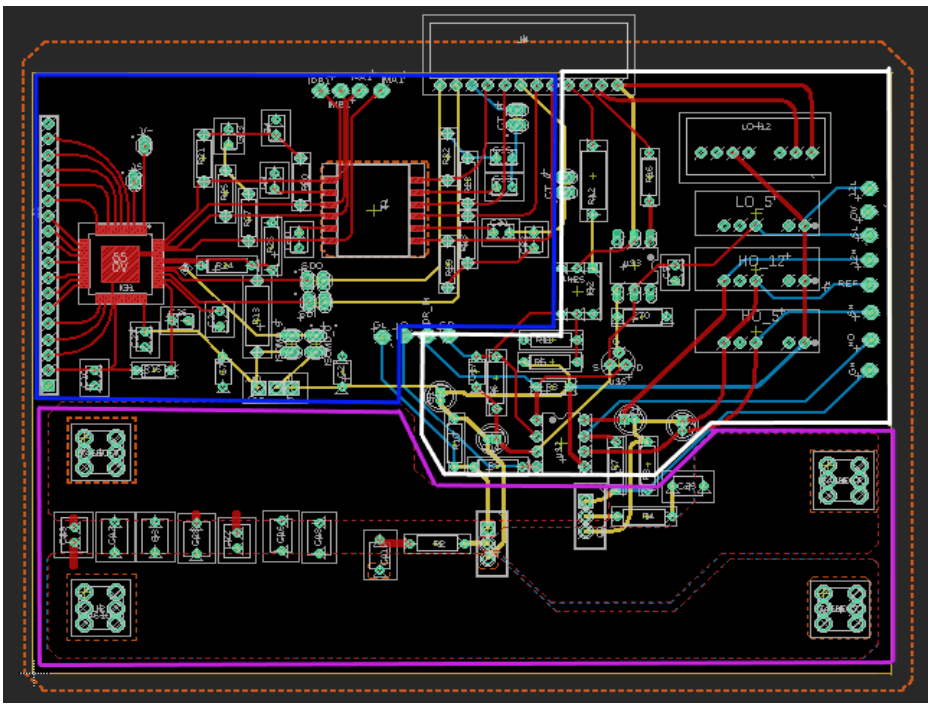

Figure 5.8 PCB Board

From the *Figure 5.8*, we can see that the board consists of 3 parts. Each part is given a different color. The power part area is colored in pink while the driver part on the right is in white color. The measurement part which is on the left side of the board is colored in blue. For the considered design, all the input terminals are on the left side of our board while the output terminals are on the right side. The communication connectors are located on top of the board.

5.3.1 Board power part

The lower part in the PCB design shown in the *Figure 5.8* is the power part. There are large polygons of copper traces between the input terminals and an output terminal of the module in the first and last layers of the PCB. The copper has thickness of 35µm to dissipate the maximum heat produced by the high currents and parasitic resistances in the PCB. There are many

capacitors connected *Ccomp*[12] in parallel close to the battery terminals. They are connected in order to compensate the loop inductance caused by the battery cables which are away from the module. Instead of a single big capacitor which has a high equivalent series resistance (ESR), many small capacitors are chosen as each small capacitor will have a lower ESR value. These selected capacitors then are connected in parallel which result in a smaller equivalent series resistor with higher capacitance.

The snubber circuit used to snub the overvoltage of the MOSFET is connected close to the drain terminal so that the snubber circuit works effectively. In between the two MOSFETs on the MMC board, there is a distance of approximately 1cm for placing the heatsinks. These MOSFETs can operate up to 175 degree Celsius. The input terminals of the battery are placed on the left side of the PCB while the output terminals of the module are placed on the right side.

5.3.2 Board driver part

While designing the driver part, the major consideration taken is that the driver part should be perpendicular to the power part in the board *Figure 5.9*. Therefore, the magnetic flux caused by the high current in the power part will have low linkage with the driver part.

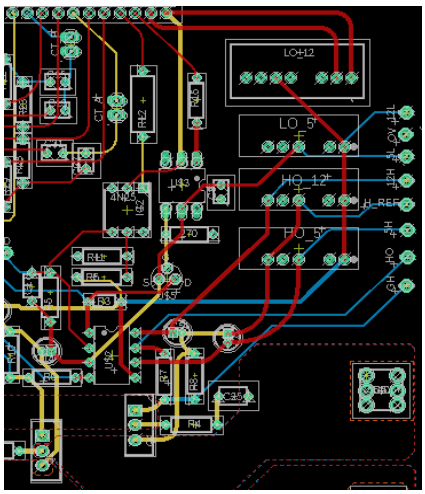

Figure 5.9 PCB driver part

All the DC-DC converters which are responsible for providing supply to the driver and gate pulse are connected on the right side of the board. Here the *Ccomp* for the supply is close to

[12] From now on, capacitors used to compensate the parasitic inductance due to the loop formed by battery cables will be called as *Ccomp*

the driver. Hence, any disturbance caused by parasitic elements will be mitigated by compensating capacitors. Another consideration is that the gate-source loop will be reduced as much as possible in order to avoid the ripples.

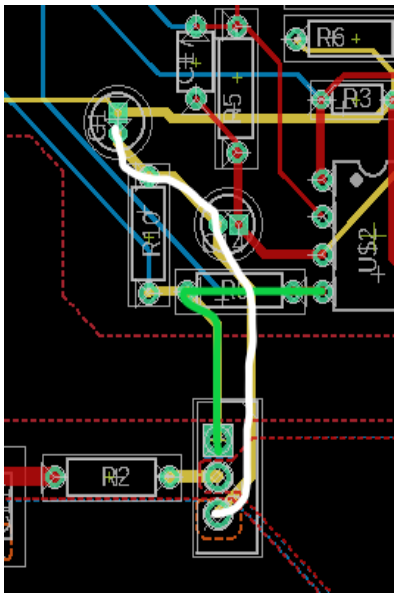

Figure 5.10 Driver track of Q1 MOSFET

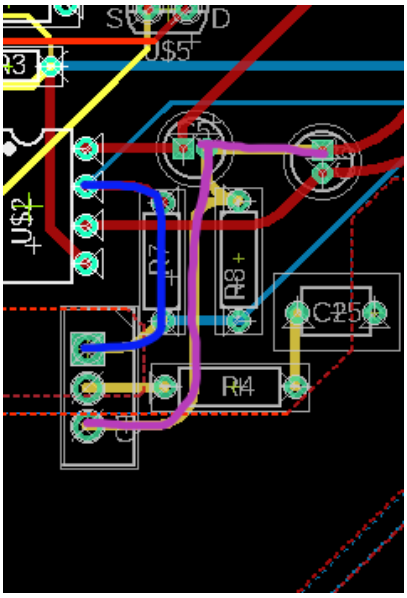

Figure 5.11 Driver track of Q2 MOSFET

The green color line in *Figure 5.10* relates the gate path of the *Q2* MOSFET, while the white line relates to the respective MOSFET source path. This is designed to have shortest path which is 1.8cm approximately. This value is little bit higher when compared to the *Q1* MOSFET path in order to keep the copper area for the battery or the drain terminals of *Q1* MOSFET so that it can dissipate the heat produced by the higher currents and PCB track resistance. Similarly, in *Figure 5.11*, the blue line relates the gate path to the *Q1* MOSFET while the pink line relates the *Q1* MOSFET source path whose distance is approximately 1.5cm. Here the snubber circuit resistors and capacitors are connected close to their respective drain and source terminals of the MOSFET. The capacitors *C1* and *C14* are connected close to the driver and the MOSFET to reduce the noises.

5.3.3 Board Measurement part

The measurement part is present at the top left of the PCB board *Figure 5.12 f*or the reason mentioned earlier as all the input ports should be on one side of the module. Here the 18-pin connector receives the temperature measurement as well as the 14 cell voltage signals with respect to the battery reference. These signals are given to the battery management chip. Therefore, LTC6812 is as close as possible to the 18-pin connector.

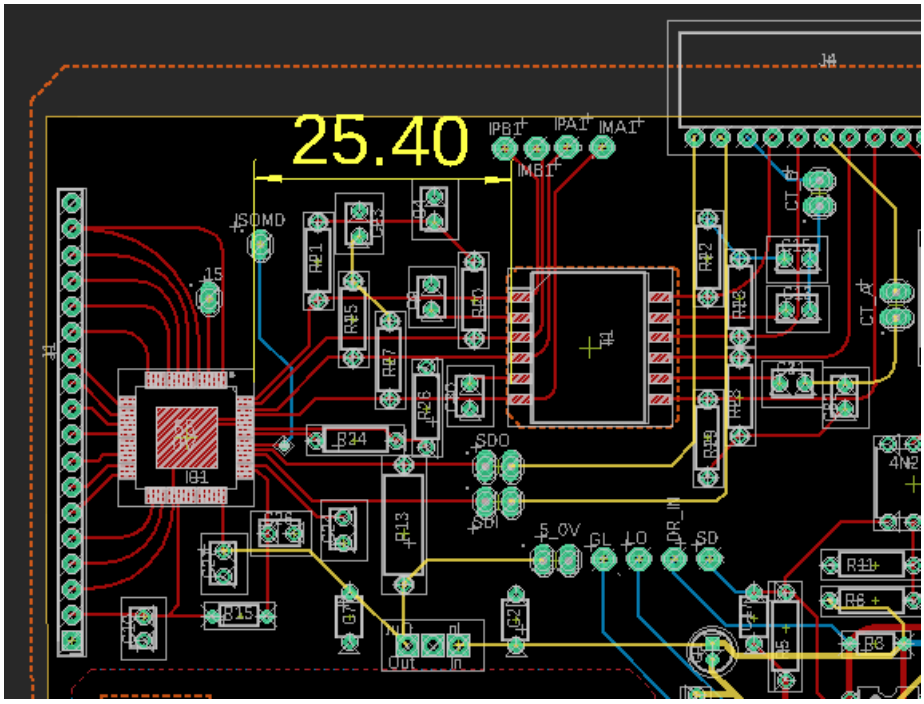

Figure 5.12 Measurement part PCB board

The communication lines, serial data out *(SDO)* and serial data in *(SDI)*, should be as small as possible and must be straight. All the communication parts in the module are placed on the top of our board. Due to the above-mentioned choice, the *SDO* and *SDI* lines are with minimum turns and with the minimum track. As stated in *5.2.1*, signal transformer is placed 2.5cm away from the LTC6812. This can be seen in the *Figure 5.12* with yellow color.

5.4 Final overall PCB

Afrer individually analyzing the power part, measurement part, and communication part the overall schematic and board of the module combining these three parts is shown in this section. The entire board design consists four layers, the first and fourth layer have copper polygons with 3.5µm to dissipate the heat produced by the rated load current. To debug the module, many single pin connectors have been used. The decoupling capacitors are placed close to their respective components. As mentioned earlier in power part is at the bottom, measurement part is on the left, and communication part on the top in the PCB board design. The overall schematic and board design of the module is shown in *Figure 5.13 to Figure 5.16.*

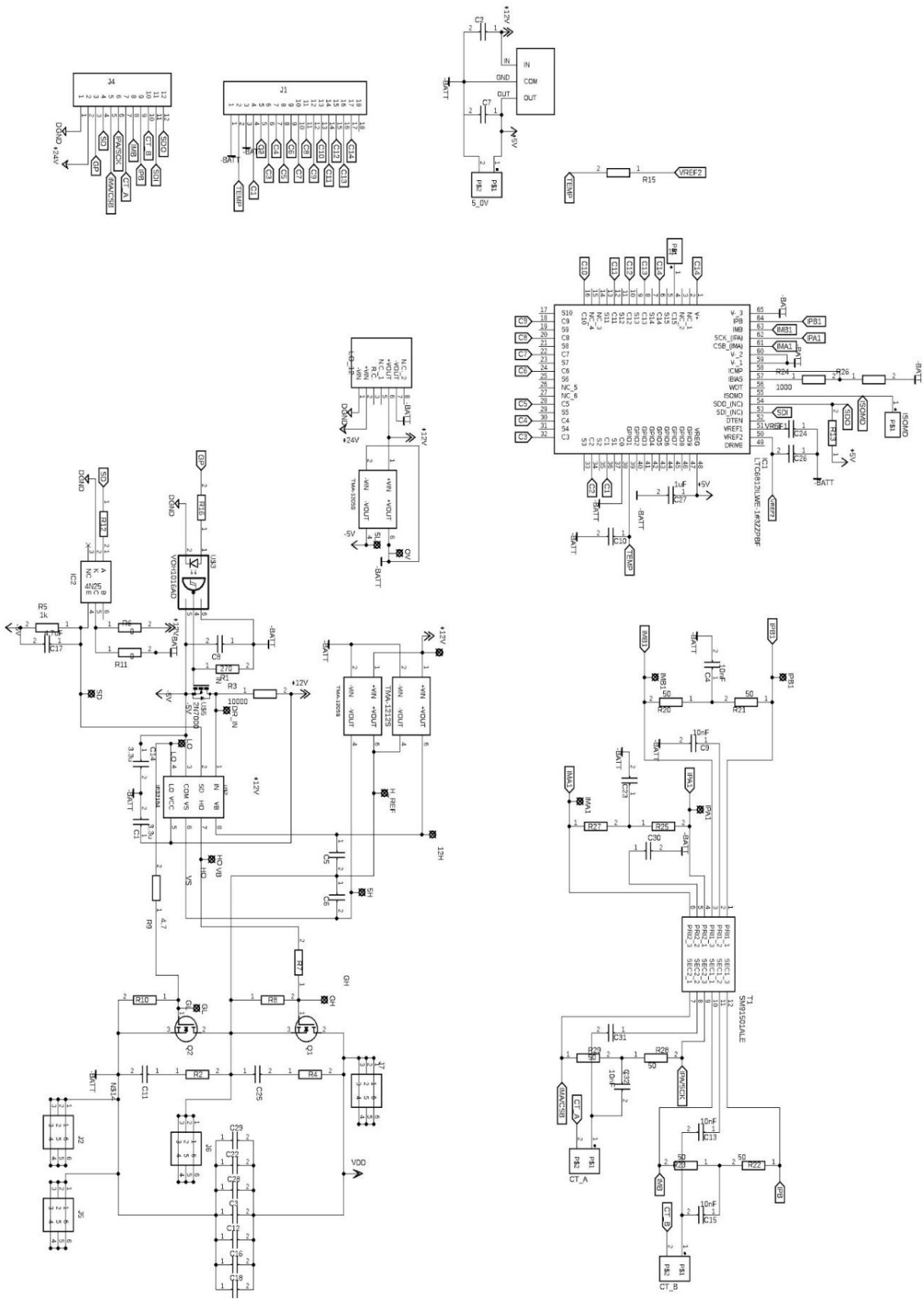

Figure 5.13 PCB schematic

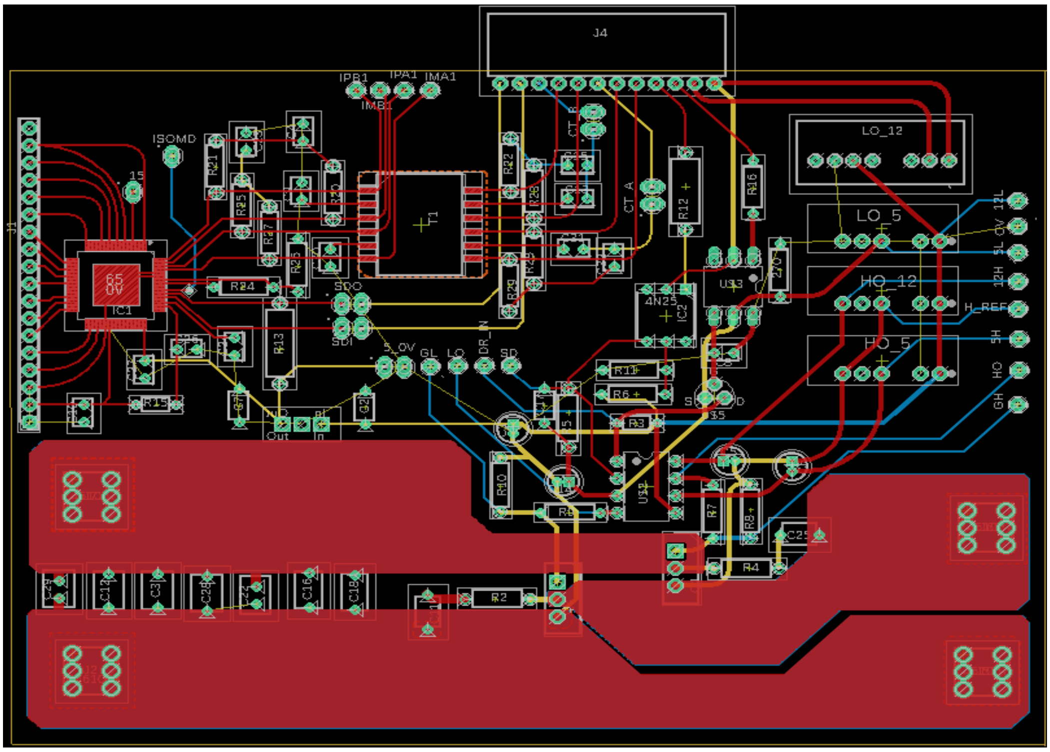

Figure 5.14 Layer 1 and 2 of PCB board

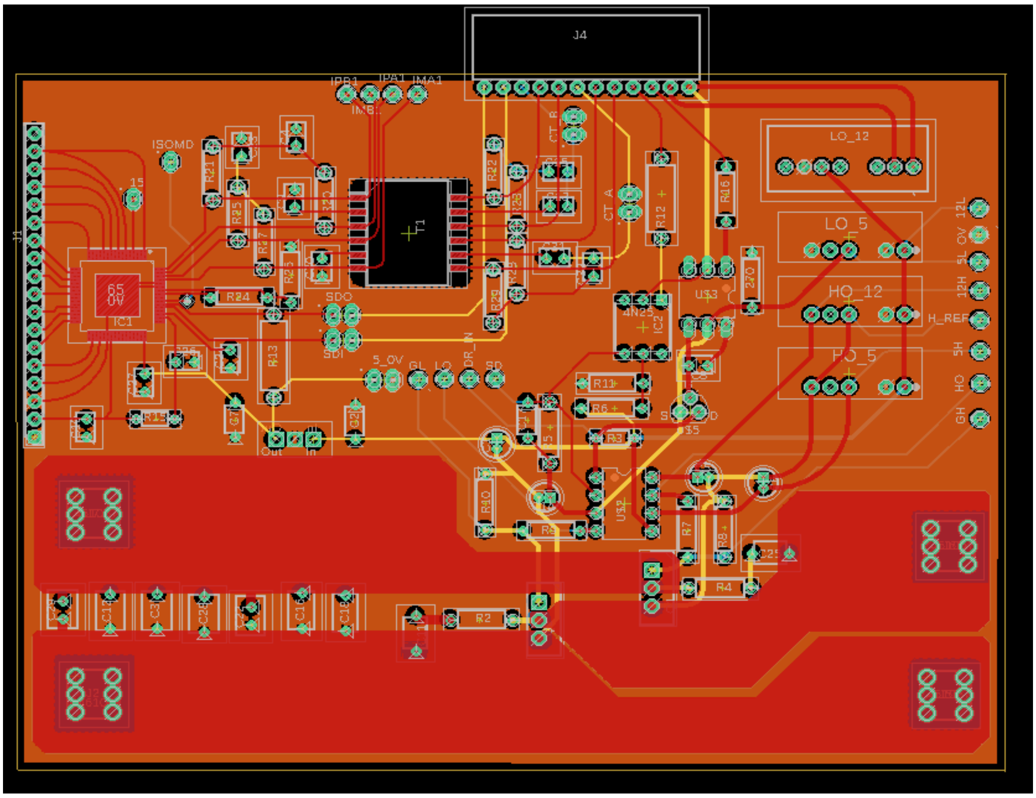

Figure 5.15 Layer 3 of PCB board

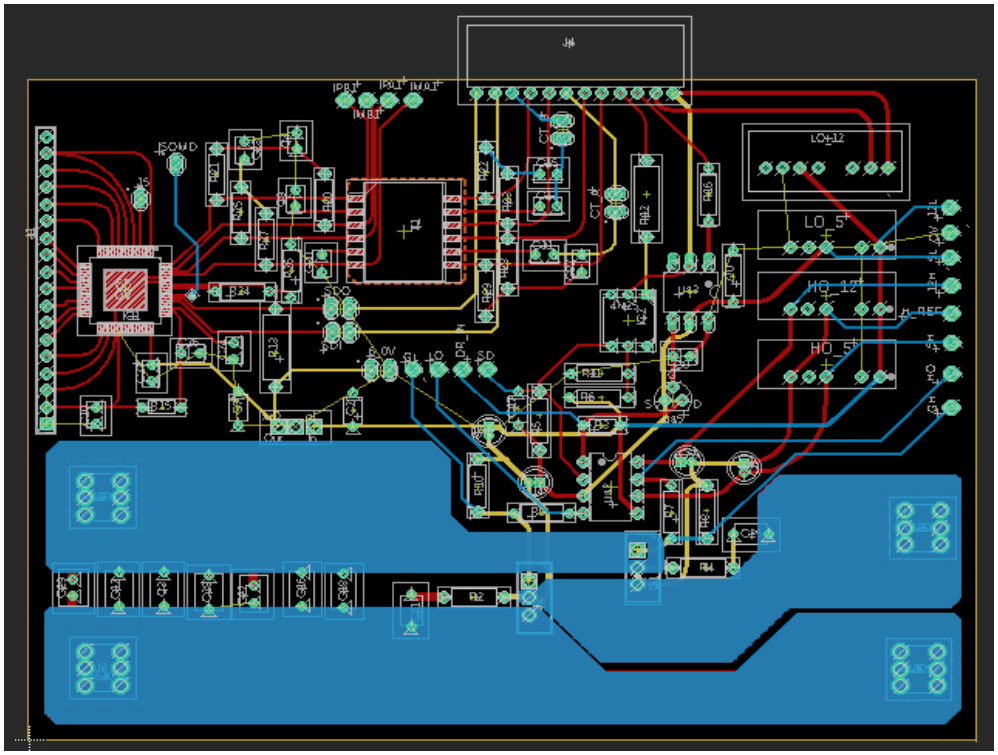

Figure 5.16 Layer 4 of PCB board

6 Hardware Testing

In this chapter, initially the driver part is tested without connecting the supply. This is to check whether the driver part is functioning properly and the gate pulse to turn ON the MOSFETs is affected by noise as well as the functioning of the shutdown pin. Next, we will connect the input to the half-bridge MOSFETs where the testing is performed without load. i.e., the load current will be zero to check any oscillation occurred by parasitic elements. Later, we will increase the load current step by step to check the waveforms and solve the associated problems.

6.1 Hardware setup

As shown in *Figure 6.1*, the hardware setup consists of two controllers. The first one being the master controller (LAUNCHXL-F28069M)[13] from texas instruments responsible for driving the module with proper gate pulse and shutdown command. The latter being measurement controller (ATmega128)[14] in the arduino board to measure the cell voltages from the battery management chip (LTC6812)[15]. There are four regulated power supplies, namely two EVENTEK KPS3010D DC supplies, one Lafayette supply, and one SM660-AR-11 of delta electronics supply in the hardware setup.

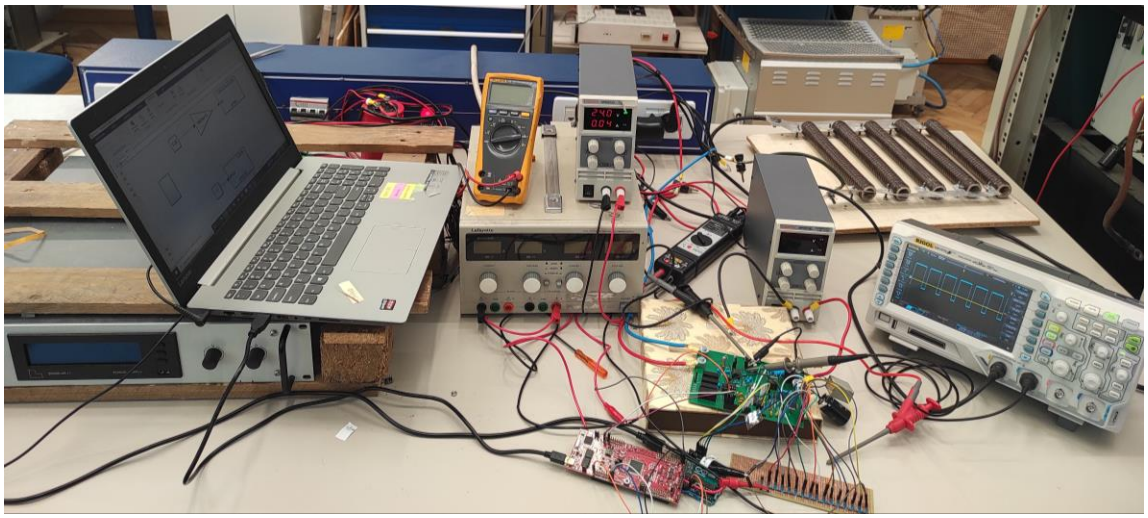

Figure 6.1 Hardware setup

[13] From now master controller refers LAUNCHXL-F28069M: TI board
[14] Measurement controller referes ATmega128: Arduinno board
[15] Battery management chipt refers LTC6812

One of the EVENTEK KPS3010D DC supplier is used to provide auxiliary input of 24V to the module, and the other is to provide input voltage of (0-30) V for testing. The third supply, Lafayette is used to create a battery model[16] of 60V which is discussed in the measurement part. The fourth supply, SM660-AR-11 is used for final testing of the model The load which is shown in *Figure 6.1* five parallelly connected 1Ω resistor and an inductor of 1mH for initial testing. For final testing of module to provide rated voltage (SM660-AR-11 from delta electronics) DC supply is used. To check the module output waveforms, RIGOL DS1074Z oscilloscope is selected because it contains four channels with a sampling rate of 1 GSa/s.

6.2 Driver part testing

To test the driver part, auxiliary input supply of 24V with current limit of 200mA is provided using EVENTEK KPS3010D regulated DC supply. The gate pulse is produced by a master microcontroller with a 25% duty cycle and waveforms are analyzed. At first, the function of the shutdown pin is analyzed. The waveforms are shown in *Figure 6.2* and *Figure 6.3* , which refer to the gate-source voltage of *Q2* MOSFET as a function of the shutdown pin. As the shutdown pin is HIGH, the gate driver generates the gate pulse with respect to the driver input.

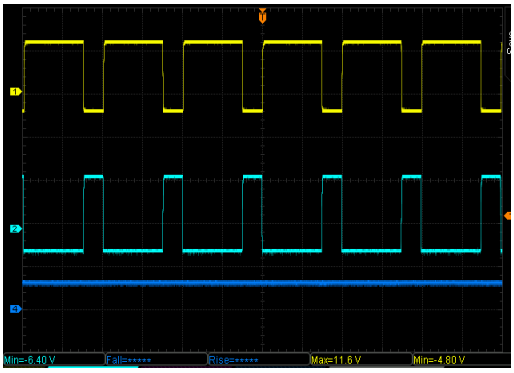

Figure 6.2 shut down pin HIGH (CH4), driver input (CH2), Vgs of Q2 MOSFET (yellow, CH1)

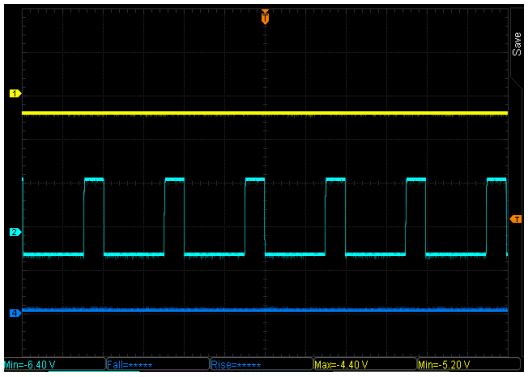

Figure 6.3 shut down pin LOW (CH4), driver input (CH2), Vgs of Q2 MOSFET (yellow, CH1)

[16] Here battery model replicates the functionality of a real battery in order to measure battery voltage along with cell voltages using regulated power supply.

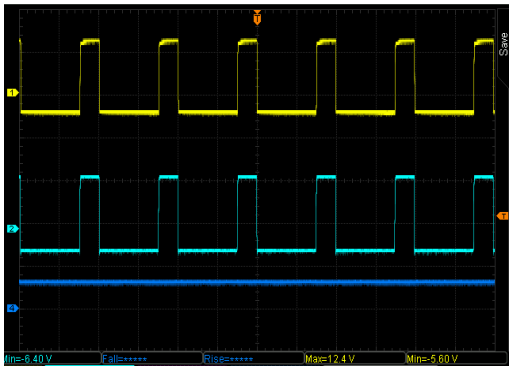

Figure 6.4 shut down pin HIGH (CH4), driver input (CH2), Vgs of Q1 MOSFET (yellow, CH1).

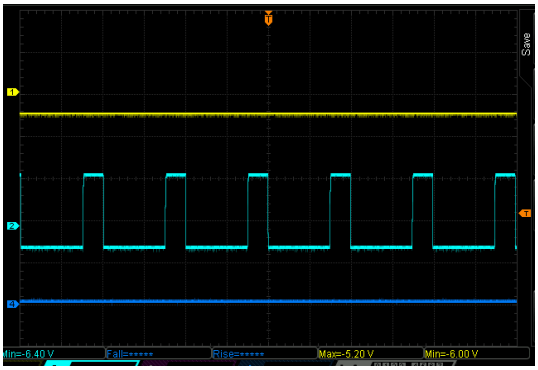

Figure 6.5 shut down pin LOW (CH4), driver input (CH2), Vgs of Q1 MOSFET (yellow, CH1).

In *Figure 6.4* and *Figure 6.5*, channel 1 which is in yellow color represents the gate-source voltage of *Q1* MOSFET and channel 2 which is in cyan color represents the gate driver input. Here the channel 4 represents the shutdown pin input. It is clear that when HIGH command is given to the shutdown pin from the master microcontroller, the driver generates gate pulse to the MOSFETs with respect to the input given to the driver as shown in *Figure 6.2* and *Figure 6.4*, when the shutdown pin receives a LOW command from the master microcontroller, the driver will not produce any gate pulse to the MOSFETs with respect to the driver input.

After checking the function of shut down pin, gate pulse output signals are analyzed now. The analysis is focused on the generation of the gate pulse and whether it is affected by any oscillations due to the parasitic elements. The gate-source voltage waveforms of the *Q1* MOSFET and *Q2* MOSFET are reported in the *Figure 6.6* to *Figure 6.9* considering the rise and fall of each MOSFET.

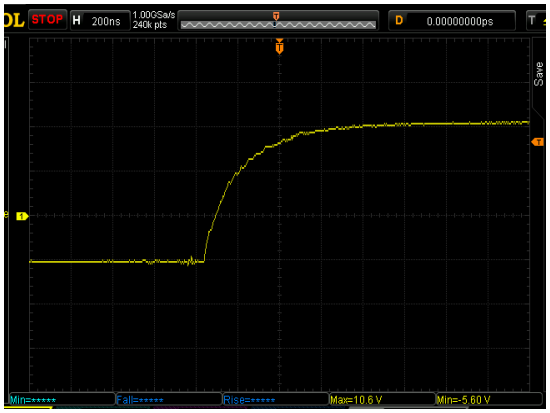

Figure 6.6 Q2 MOSFET Vgs rising edge

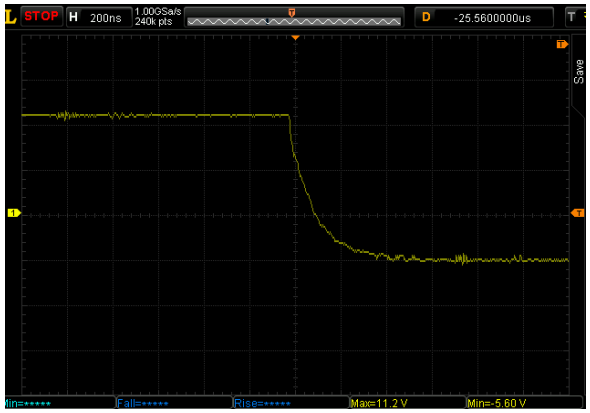

Figure 6.7 Q2 MOSFET Vgs falling edge

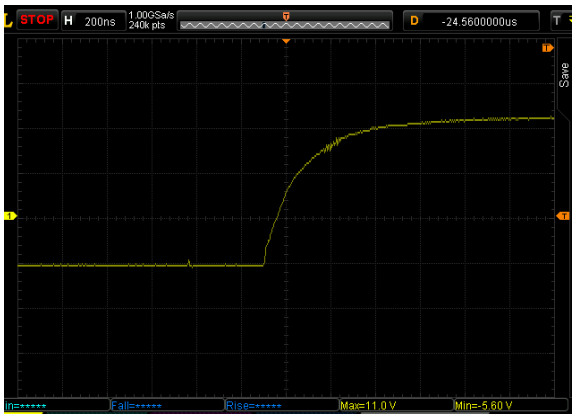

Figure 6.8 Q1 MOSFET Vgs rising edge

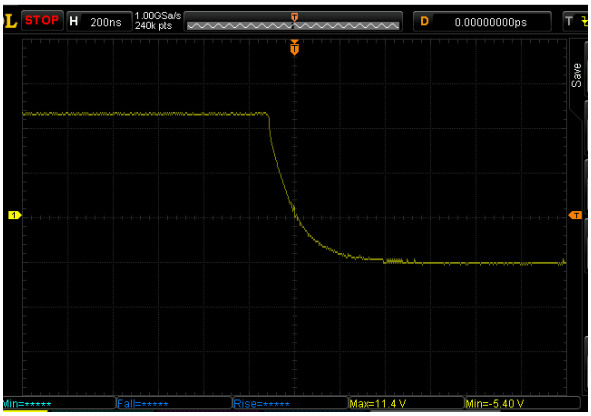

Figure 6.9 Q1 MOSFET Vgs falling edge

It can be noticed that the waveforms are well produced without causing any oscillations due to parasitic elements in the PCB without any load. Therefore, in the next section, we connect the input supply to the MOSFET terminals and check its performance while increasing the voltage up to 30V. To supply input to the module, DC regulated power supply (EVENTEK KPS3010D) is selected instead of battery in order to regulate the input voltage during testing. First, it is performed when the current is zero (no load) and later, by considering the load. The waveforms of the gate to source voltage and drain to source voltage of *Q2* MOSFET are shown in *Figure 6.10.*

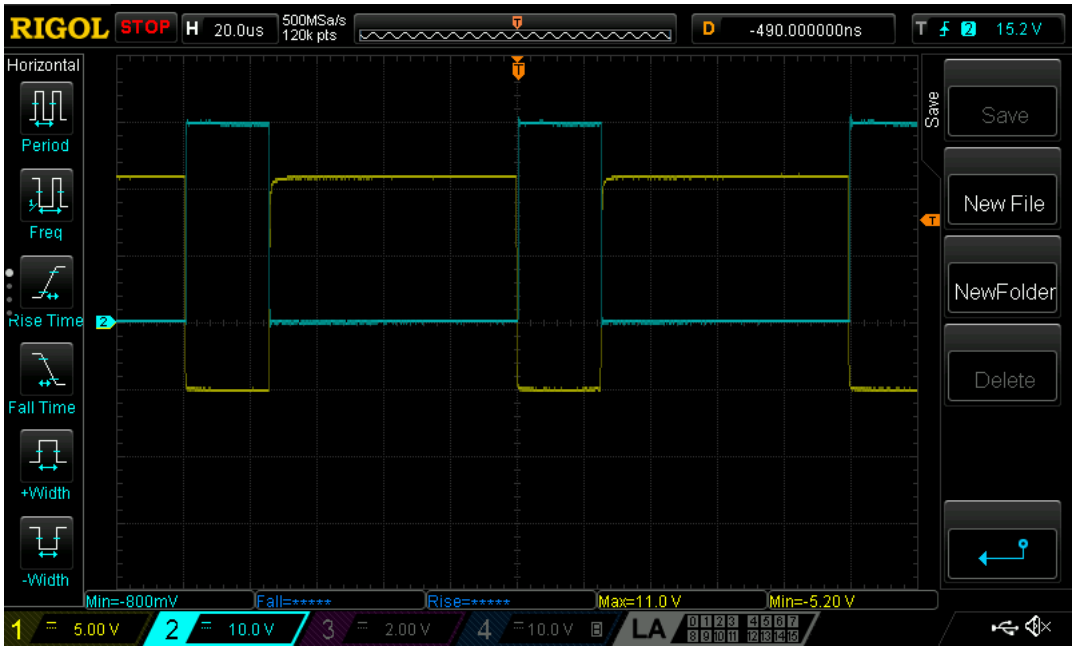

Figure 6.10 Q1 MOSFET Vgs (yellow, CH1), output voltage (cyan, CH2) Iload=0A

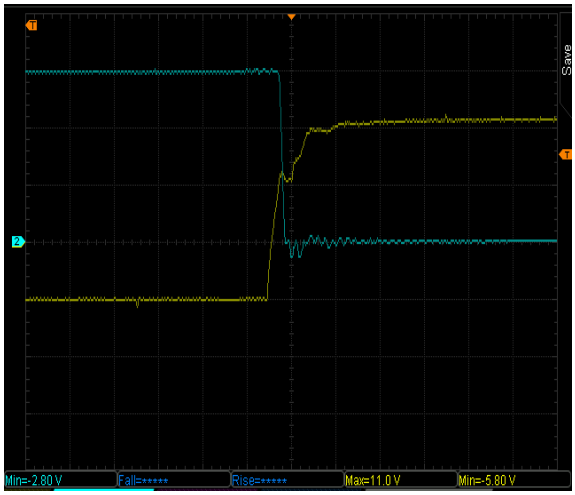

Figure 6.11 Q1 MOSFET Vgs rising edge (yellow, CH1), output voltage (cyan, CH2)

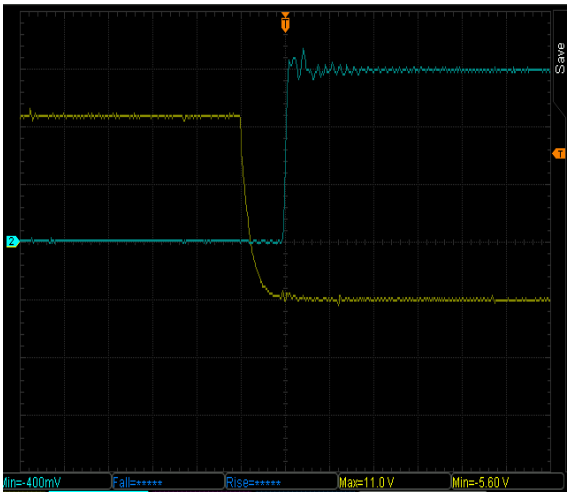

Figure 6.12 Q1 MOSFET Vgs falling edge (yellow, CH1), output voltage (cyan, CH2)

Both *Q1* and *Q2* MOSFETs has similar characteristics hence only *Q1* MOSFET is taken for analysis. As shown in the *Figure 6.11* and *Figure 6.12*, the rising and falling edges of the gate pulse are not affected when there is no load at the output. But if we see the *Figure 6.11*, there is a descending plateau that interrupts *Vgs* growth at 7V. This plateau is due to the parasitic capacitance of the MOSFET *Cgd*, with the gate path loop which creates the miller effect. Therefore, it is analyzed by increasing the current to understand the effect on our gate to source voltage.

To perform calculations with load current, resistance of 0.2Ω and inductance of 1mH are selected in order to achieve higher current as shown in *Figure 6.13* and *Figure 6.14*. The frequency of gate pulse taken is 10kHz with a duty cycle of 25%. The parameters are listed in *Table 6.1*.

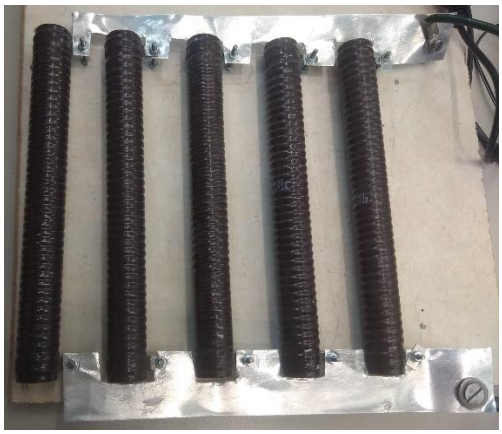

Figure 6.13 Load resistor.

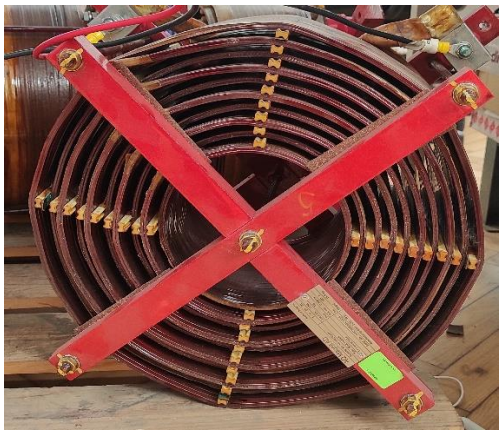

Figure 6.14 Load inductor

Parameter	***Value***
Resistance	*0.2Ω*
Inductance	*1mH*
Switching frequency	*10kHz*
Duty cycle	*25%*
Module input	*30V*

Table 6.1 Hardware testing load parameters

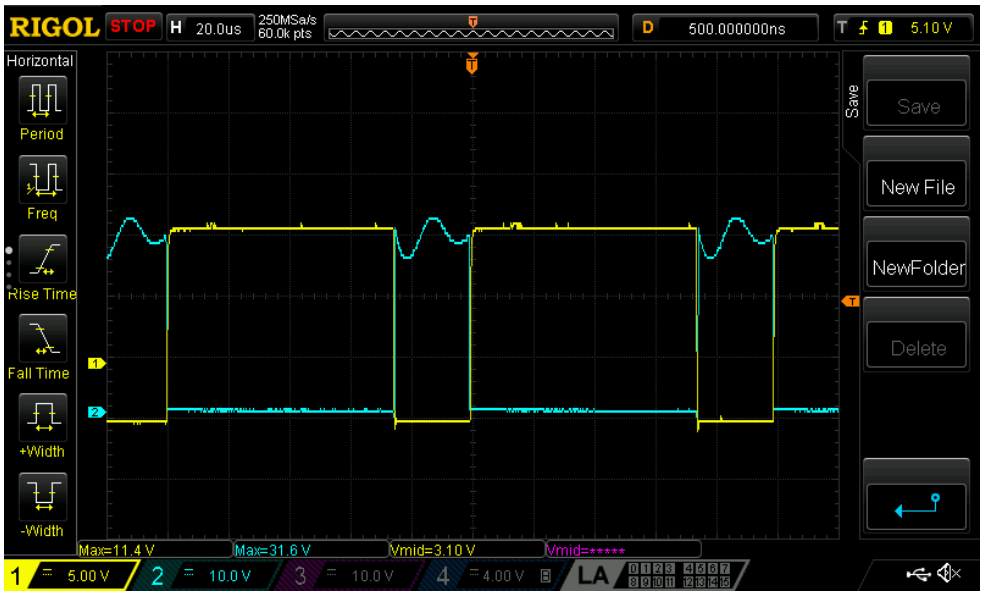

Figure 6.15 Vgs of Q1 MOSFET (yellow, CH1), output voltage (cyan, CH2) with Iload=25A

From *Figure 6.15*, we can observe that the oscillation (both high and low frequency) on the output voltage(drain-source voltage) of the *Q2* MOSFET is colored in cyan. This is due to the battery wire inductance which is approximately 20 cm long. The DC-busbar input capacitance *Ccomp* of the seven ceramic capacitors(4.7 uF) is not enough to compensate the battery loop inductance.

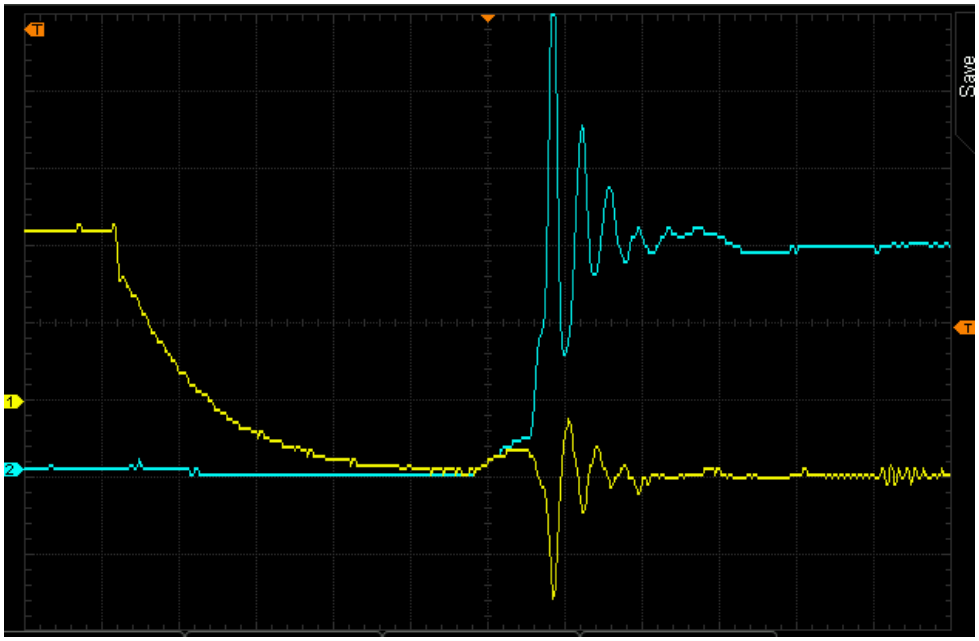

Figure 6.16 Vgs of Q2 MOSFET (yellow, CH1), output voltage rising edge (cyan, CH2)

The high frequency oscillations during the switching phase is shown in *Figure 6.16.* From *Figure 6.15* and *Figure 6.16,* it is clear that the drain-source voltage of the *Q2* MOSFET consists of both low and high frequency oscillations.

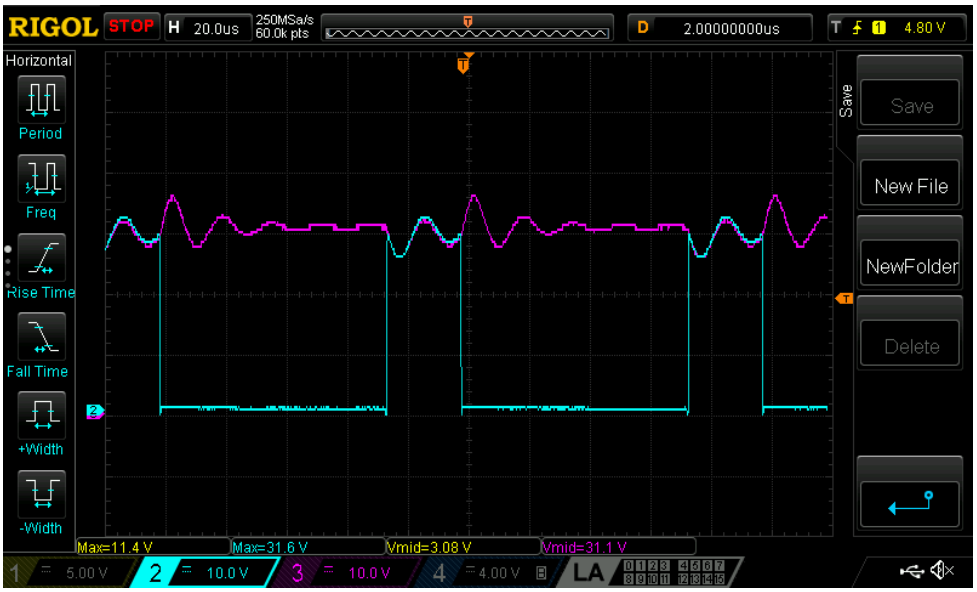

Figure 6.17 Output voltage (cyan, CH2) and the battery voltage (pink, CH3) with Iload=25A

From *Figure 6.17,* we can notice that the drain to source voltage of *Q2* MOSFET is colored in cyan while the battery voltage is in pink color, the low frequency oscillations due to the battery

wire loop inductance can be observed by measuring the battery voltage. Therefore, as shown in *Figure 6.18* another two electrolytic capacitor of 470 µF and 100µF is added in order to reduce the low-frequency ripples. This electrolytic capacitor can compensate the low frequencies effectively. One more 6.8µF ceramic capacitor is added to reduce the high-frequency ripples.

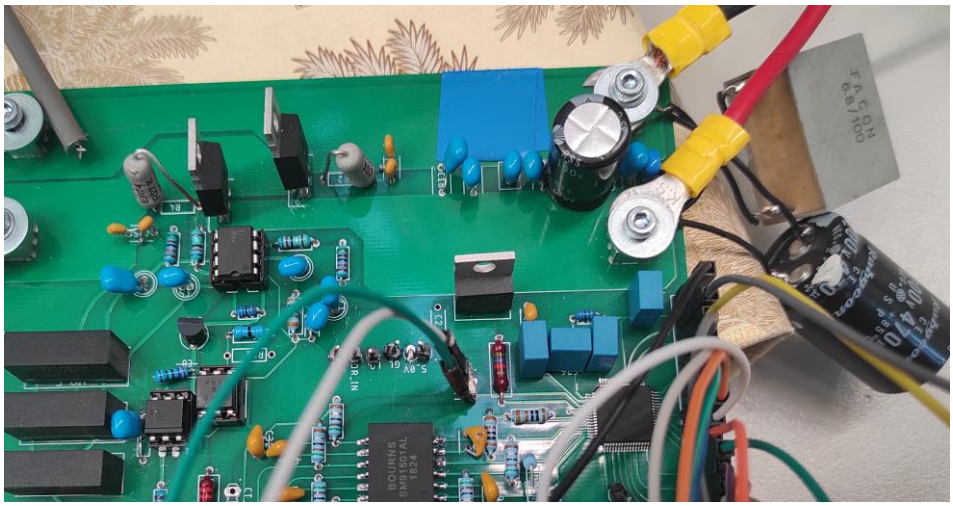

Figure 6.18 Placing of compensating capacitors.

The resulting waveform after adding the compensating capacitors can be seen in *Figure 6.19.*

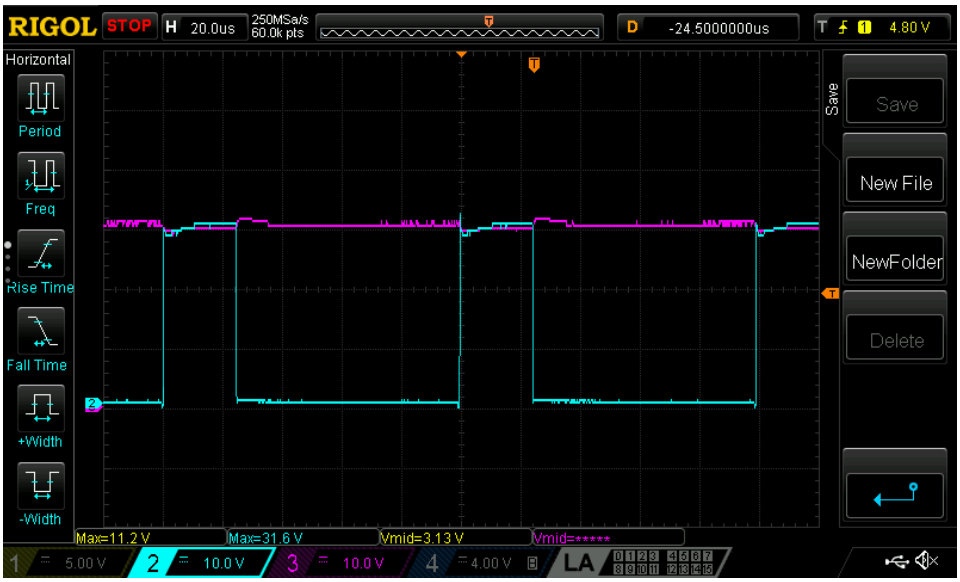

Figure 6.19 output voltage (cyan, CH2) and battery voltage (pink, CH3)

It can be observed that the battery voltage is almost constant after adding the compensating capacitors. However, another problem arose during testing, is due to the wrongly sizing of snubber circuit: it is more heated due to the time constant of the snubber circuit is $\tau = RC = 1 * 0.47uF = 0.47\ \mu\, secs$. Therefore, to reach the steady state, it will take $5\tau = 2.35\ \mu s$. As the rise time of the MOSFET is 52 ns, the snubber circuit will take more time to reach it's steady state. This may result in higher losses. When the module is tested for less than a minute, the temperature in the snubber circuit reaches 188°C in *Q1* MOSFET and 164°C in *Q2* MOSFET. This is depicted in the thermal graphs of the snubber circuit using FLUKE Ti32 thermal camera as shown in the *Figure 6.20* and *Figure 6.21*. The difference in temperature of *Q1* and *Q2* MOSFETs are due to *Ccomp* capacitors are placed close to the *Q2* MOSFET, The *Q1* MOSFET has longer path which results in higher spikes in the oscillation.

Figure 6.20 Previous snubber circuit temperature Q1 on the left and Q2 on the right

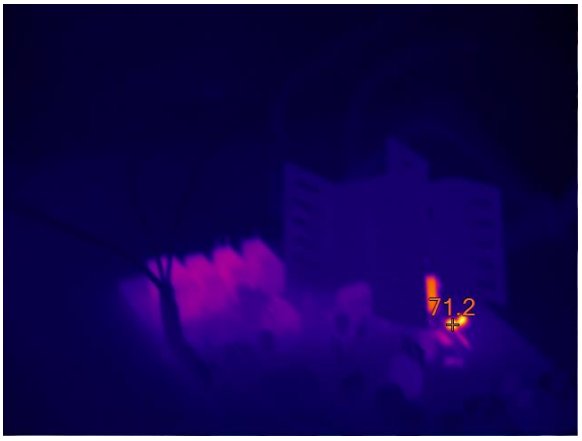

Figure 6.21 New snubber circuit temperature Q1 on the left and Q2 on the right

The temperature in the snubber circuit increases drastically with the load voltage of 30V and duty cycle of 25%. Therefore, we cannot further increase the voltage to reach the maximum limit of the system. For this purpose, the snubber circuit values are reduced to match the rise time of the MOSFET. The snubber capacitor of 47 nF and resistor of 0.27Ω is taken with the time constant of the system as $\tau = RC = 12.5\ nS$. Therefore, the snubber circuit will reach the steady state at 60ns which is approximately equal to the rise time of the MOSFET.

As previously mentioned, when the snubber circuit is changed, with the same inputs, the temperature is attained at a maximum of 71.3°C and it is stable with load current of 25 A. This limit is under the permissible limit of the capacitors working up to 125 degrees Celsius. After adding the compensating capacitors and snubber circuits, the voltage is increased to reach the

maximum value of 60V. But the gate-source voltage of both the MOSFETs have oscillations which is reaching beyond the working voltage of the gate driver (± 20V). Due to this, gate driver malfunctions when the voltage crosses 30V. This oscillations can be seen in the following *Figure 6.22* and *Figure 6.23.*

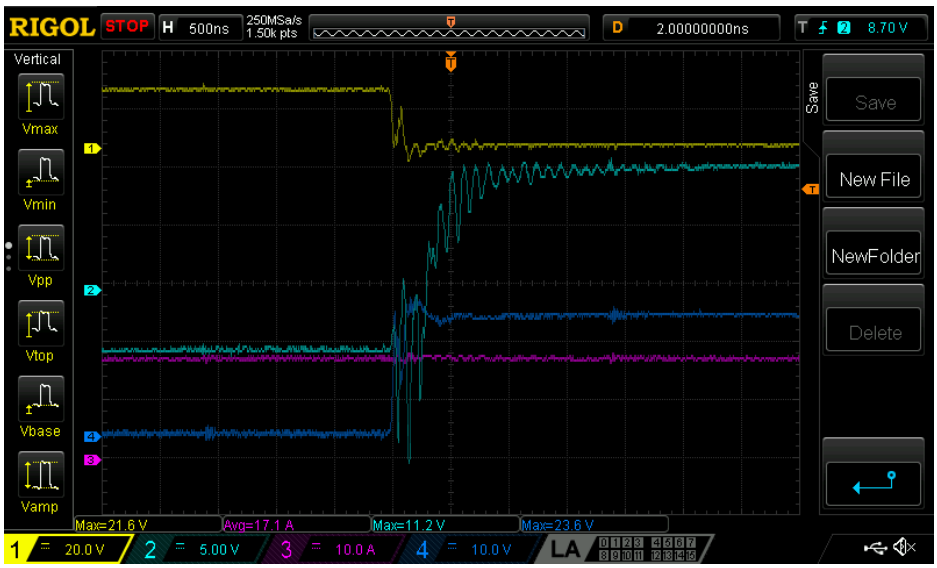

Figure 6.22 Raising edge Vgs of Q2 MOSFET (CH2), Iload (CH3), Vds of Q2 MOSFET (CH1), Vds of Q1 MOSFET (CH4)

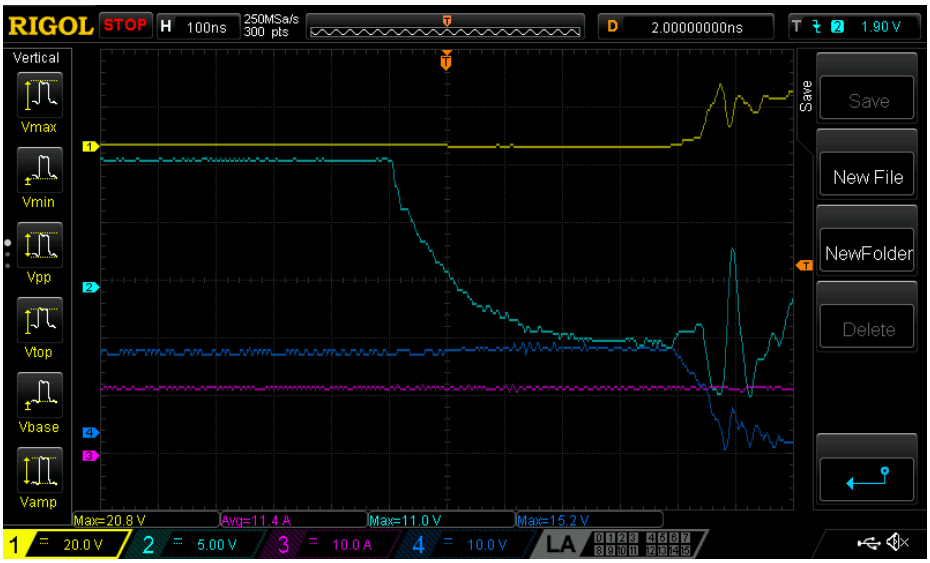

Figure 6.23 Falling edge Vgs of Q2 MOSFET (CH2), Iload (CH3), Vds of Q2 MOSFET (CH1), Vds of Q1 MOSFET (CH4)

It can be noticed from the *Figure 6.22*, the gate-source voltage of the *Q2* MOSFET oscillates, and its first negative peak reaches to -15V when the battery input is 20V which is closer to

capacitor working voltage (25V) and gate driver working voltage (±20V). Also, if we take a closer look at *Figure 6.23* gate-source oscillations, the first oscillation is going to be +4V instead of -5V. And the MOSFET threshold is 3V which makes the MOSFET to turn ON instead of turn OFF. These oscillations are due to the interaction of the high current with the gate loop.

To compensate these oscillations, the gate supply capacitor of 3.3 uF is not enough. This can be found by looking into the compensating capacitance with respect to drain-source voltage. The schemes showing capacitor voltage measurements are shown in *Figure 6.24* and *Figure 6.25.*

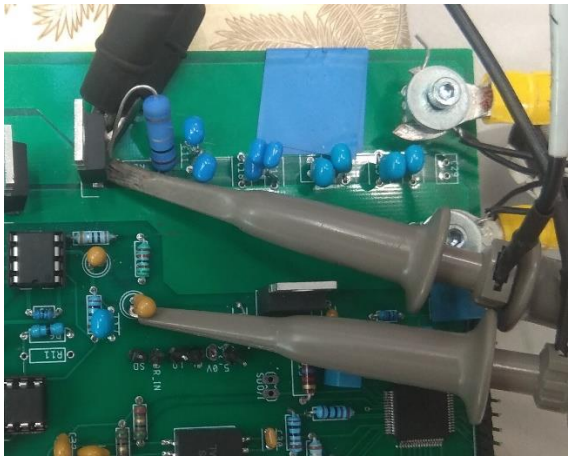

Figure 6.24 Positive 12V supply capacitor of Q2 MOSFET

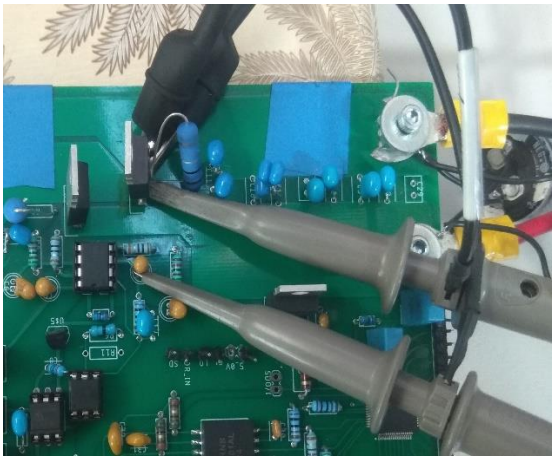

Figure 6.25 Negative 5V supply capacitor of Q2 MOSFET

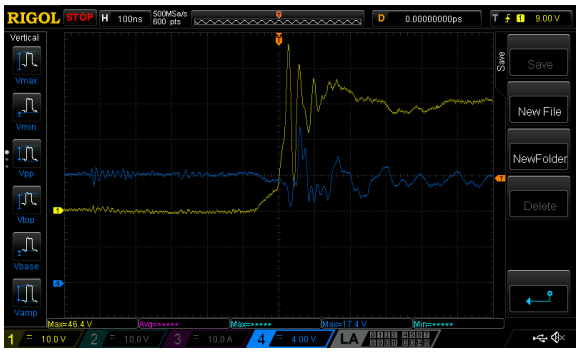

Figure 6.26 Positive 12V Q2 gate supply capacitance (blue, CH4), output voltage (yellow,CH1)

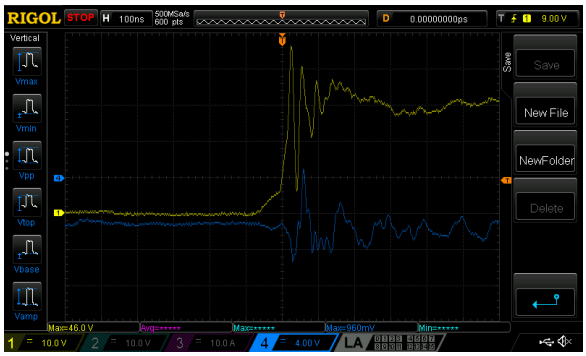

Figure 6.27 Negative 5V Q2 gate supply capacitance (blue,CH4), output voltage (yellow,CH1)

It can be seen in *Figure 6.26* and *Figure 6.27* that the gate-source supply voltage of 12V and the -5V oscillates at each switching interval. Particularly, -5V oscillation makes the MOSFET stay neither in the turn ON nor in the turn OFF state. The MOSFET works in its linear region

where it dissipates large amounts of heat. Here, the MOSFET is reaching the temperature of more than 100°C, less than 10 mins of testing with a load current 17A. Therefore, the gate supply capacitance is increased to 4.7 µF with voltage rating of 100 V as the oscillations are high. The final testing is performed with the rated voltage values (to provide 60V input, SM660-AR-11 of delta electronics DC power supply is used). To attain the rated current, the resistance and the duty cycle have been decreased, from 0.2Ω to 0.16Ω and from 25% to 21% respectively. The results are shown in the *Figure 6.28.*

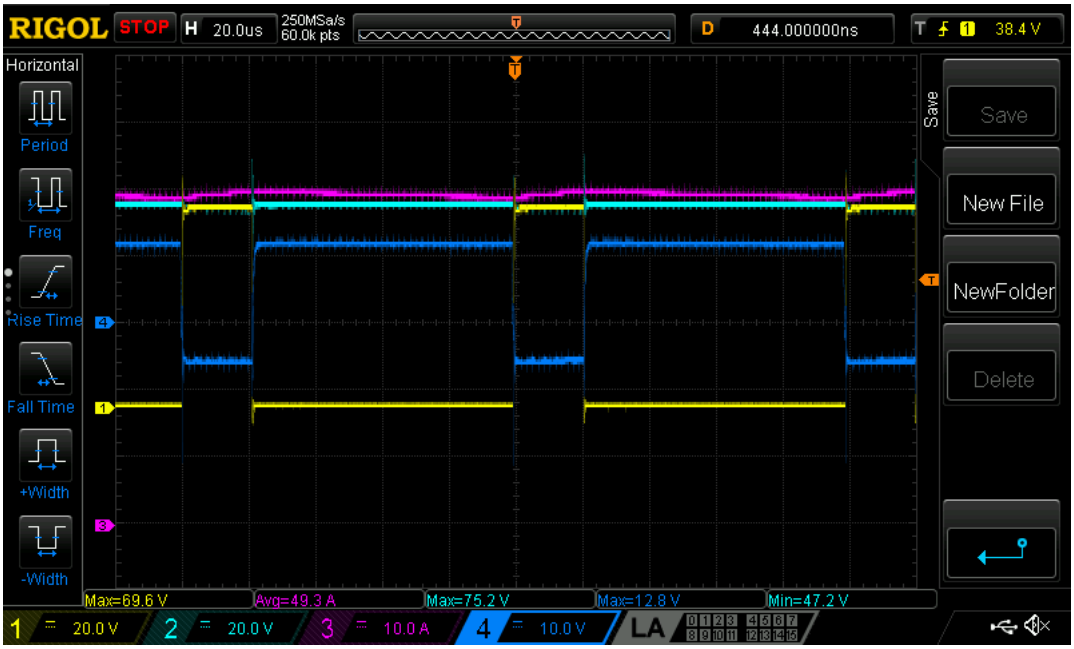

Figure 6.28 Vds of MOSFET Q1 (CH1), Battery voltage (CH2), Iload=50A (CH3), Vgs MOSFET Q1(CH4)

From *Figure 6.28*, it is clear that the MMC module has attained its maximum rating of 60V and 50A. The ripples(due to higher current) present in the gate-source voltage and in the output voltage of *Q1* and *Q2* MOSFETs does not affect the system performance. This can be observed from the *Figure 6.29.*

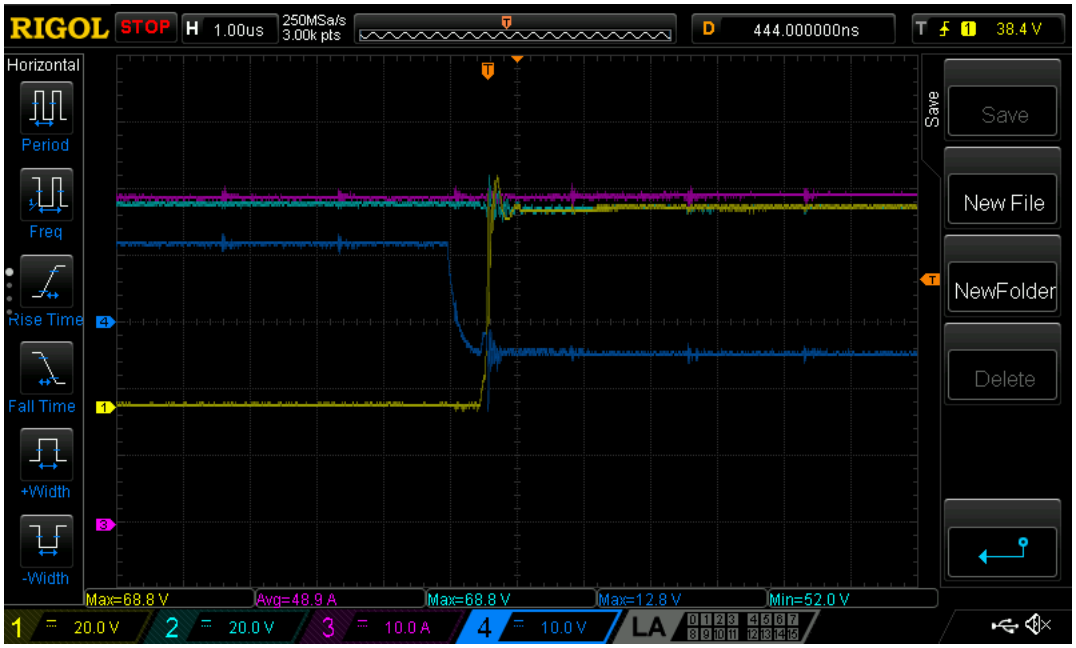

Figure 6.29 Zoomed view Vds of Q1 MOSFET (CH1), Battery voltage (CH2), Iload=50A (CH3), Vgs of Q2 MOSFET (CH4)

The gate-source voltage of the MOSFET does not cross the threshold of zero volts which makes the MOSFET to stay in turn OFF state. The output voltage of the module reaches the maximum voltage of 69V which is 15% higher than the voltage rating of the module. This is within the reasonable limit of the system, taking consideration that the selected MOSFETs can work up to 120V.

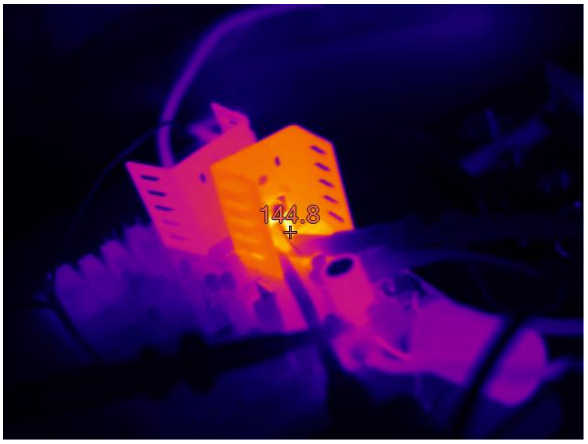

Figure 6.30 Thermal image without fan after 10 mins

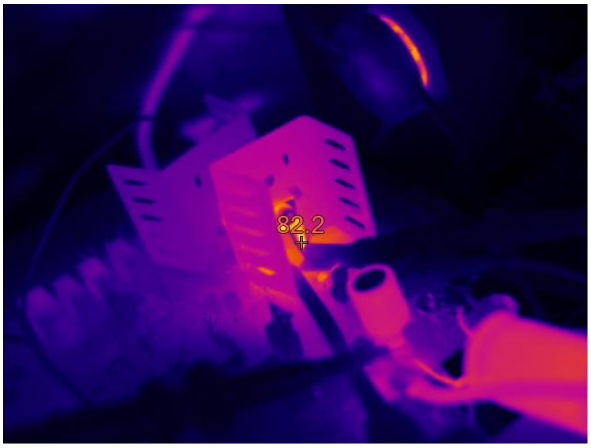

Figure 6.31 Thermal image with fan after 10 mins

If we look at the temperature of the module, it reaches 144° C when the rated load current flows for more than 10 mins. Therefore, in order to cool the system with the higher temperature, a fan can be added. Then the maximum temperature reaches 82° C after 10 minutes with the

addition of fan at which the module is stable. The thermal images[17] of the module with and without a fan are shown below in *Figure 6.30* and *Figure 6.31*.

6.3 Measurement part

For testing the measurement part, a battery model[18] has been designed. It is made of 14 cells with 100Ω voltage dividers and a current limiting resistor of 75Ω in series as shown in the *Figure 6.32.* The voltage dividers are used to obtain cell voltage. When the supply of 56V is given using Lafayette regulated power supply, voltage obtained across each point in the voltage divider is 4V. The reason to choose battery model instead of real battery is to regulate the voltage and check the performance of battery management chip. For measuring the cell voltages, measurement controller configured in serial communication is used. The following code is used to measure the cell voltages.

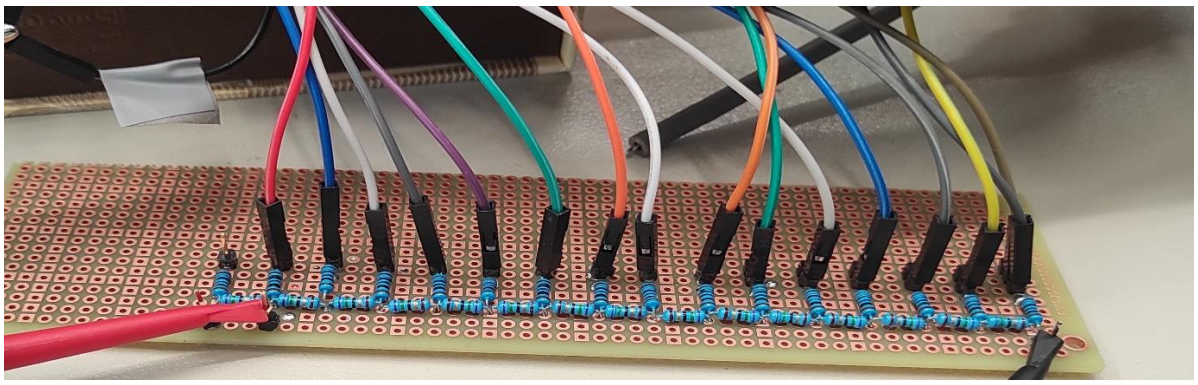

Figure 6.32 Measuring cell voltage using voltage divider

[17] If the thermal images are shown, then they are taken from FLUKE Ti32 Infrared camera.
[18] From now on battery model is mentioned, then it is the Lafayette regulated power supply with voltage divider.

```
wakeup_sleep(TOTAL_IC);
LTC6812_adcvsc(ADC_CONVERSION_MODE,ADC_DCP);
conv_time = LTC6812_pollAdc();
print_conv_time(conv_time);
wakeup_idle(TOTAL_IC);
error=LTC6812_rdcv(SEL_ALL_REG,TOTAL_IC,BMS_IC);
check_error(error);
print_cells(DATALOG_DISABLED);
wakeup_idle(TOTAL_IC);
error = LTC6812_rdstat(SEL_REG_A,TOTAL_IC,BMS_IC);
check_error(error);
print_sumofcells();
```

Figure 6.33 Code for measurning the cell voltages

Usually, when we start conversion, we need to power the LTC6812 chip with a wakeup signal. When there is no valid command to the chip, it will go to sleep state in order to reduce the power consumption to a minimum level. The second line in the code is the $ADCVSC$ command provided to the chip. It will measure all the fifteen cell voltages[19] as well as the sum of the cells. The selection of ADC mode which we discussed in the earlier chapter is provided by the command $ADC\_CONVERSION\_MODE$. This results in different sampling times for the measurement. The command ADC_DCP which is used for cell balancing functionality, at present in the proposed MMC module it is not used. Therefore, this command needs to be disabled. After measuring all the voltages, the values will be stored in respective registers. To print these voltage values, the following program in *Figure 6.34* is used.

[19] From now on if cell voltage is mentioned then it is voltage obtain from the voltage divider of battery model.

```
void print_cells(uint8_t datalog_en)
{
for (int current_ic = 0 ; current_ic < TOTAL_IC; current_ic++)
{
for (int i=0; i<15; i++)
{
Serial.print(" C");
Serial.print(i+1,DEC);
Serial.print(":");
Serial.print(BMS_IC[current_ic].cells.c_codes[i]*0.0001,4);
Serial.print(",");
}
Serial.println();
}
void print_sumofcells(void)
{
for (int current_ic =0 ; current_ic < TOTAL_IC; current_ic++)
{
Serial.print(F(" IC "));
Serial.print(current_ic+1,DEC);
Serial.print(F(": SOC:"));
Serial.print(BMS_IC[current_ic].stat.stat_codes[0]*0.0001*30,4);
Serial.print(F(","));
}
Serial.println("\n");
```

Figure 6.34 Code for printing cell voltages

The code for printing cell voltages is initiated using the print_cells command. The first 'for' loop in the code runs for the modules connected in the daisy-chain, in our case number of

modules connected in leg (1 to 2N). The inner 'for loop' provides the 15 cell voltages of each module connected in daisy-chain.

The command $serial.print(BMS\_IC[current\_ic].cells.c\_codes[i] * 0.0001,4)$ reads the data present in the BMS_IC register and converts that binary number into integer. It shows the number accuracy of 4 digits after decimal is selected by the above command. To print the sum of the cell voltages the following code is used.

When the print_sumofcells command is initiated, the chip will print the state of charge of the entire module BMS_IC[current_ic].stat.stat_codes[0]*0.0001*30,4 The binary value is converted to the integer value by the conversion code. The accuracy of 4 digits after decimal is selected. The final result of $ADCVS$ command is shown in *Figure 6.35.*

```
 IC 1: SOC:53.0340,

List of LTC6812 Command:
Write and Read Configuration: 1                          |Loop measurements with data-log output : 12                          |Set Discharge: 23
Read Configuration: 2                                    |Clear Registers: 13                                                  |Clear Discharge: 24
Start Cell Voltage Conversion: 3                         |Run Mux Self Test: 14                                                |Write and Read of PWM : 25
Read Cell Voltages: 4                                    |Run ADC Self Test: 15                                                |Write and  Read of S control : 26
Start Aux Voltage Conversion: 5                          |ADC overlap Test : 16                                                |Clear S control register : 27
Read Aux Voltages: 6                                     |Run Digital Redundancy Test: 17                                      |SPI Communication  : 28
Start Stat Voltage Conversion: 7                         |Open Wire Test for single cell detection: 18                         |I2C Communication Write to Slave :29
Read Stat Voltages: 8                                    |Open Wire Test for multiple cell or two consecutive cells detection:19 |I2C Communication Read from Slave :30
Start Combined Cell Voltage and GPIO1, GPIO2 Conversion: 9 |Open wire for Auxiliary Measurement: 20                            |Enable MUTE : 31
Start  Cell Voltage and Sum of cells : 10                |Print PEC Counter: 21                                                |Disable MUTE : 32
Loop Measurements: 11                                    |Reset PEC Counter: 22                                                |Set or reset the gpio pins: 33

Print 'm' for menu
Please enter command:

10
Conversion completed in:1.6ms

 IC 1,  C1:3.6905, C2:3.8029, C3:3.7889, C4:3.8115, C5:3.7629, C6:3.8164, C7:3.7896, C8:3.8152, C9:3.8181, C10:3.7952, C11:3.8060, C12:3.8092, C13:3.8160, C14:3.7071, C15:0.0002,

 IC 1: SOC:53.0130,
```

Figure 6.35 Measuring the cell voltages and battery voltage.

Using this battery measurement chip cell voltages can be continuously measured with the measurement controller in a loop. The delay time programmed is 0.5 seconds. The cell voltage measured with the loop is mentioned below in *Figure 6.36.* It can be noted that, while measuring the input cell voltages, the input of battery model voltage (Lafayette regulated power supply with voltage divider) is increased gradually. This battery model is used to check whether the cell voltage measurement changes with the change in input.

```
11
Transmit 'm' to quit
 IC 1,  C1:3.6880, C2:3.7975, C3:3.7839, C4:3.8044, C5:3.7569, C6:3.8083, C7:3.7835, C8:3.8114, C9:3.8115, C10:3.7898, C11:3.7984, C12:3.8029, C13:3.8117, C14:3.7073, C15:0.0000,

 IC 1,  C1:3.6887, C2:3.7977, C3:3.7835, C4:3.8039, C5:3.7566, C6:3.8108, C7:3.7839, C8:3.8107, C9:3.8098, C10:3.7883, C11:3.7991, C12:3.8021, C13:3.8110, C14:3.7075, C15:0.0000,

 IC 1,  C1:6.5535, C2:6.5535, C3:6.5535, C4:3.8031, C5:3.7569, C6:3.8096, C7:3.7835, C8:3.8107, C9:3.8098, C10:3.7899, C11:3.7993, C12:3.8013, C13:3.8101, C14:3.7065, C15:0.0000,

 IC 1,  C1:3.6894, C2:3.7980, C3:3.7838, C4:3.8048, C5:3.7563, C6:3.8115, C7:3.7839, C8:3.8115, C9:3.8113, C10:3.7894, C11:3.8010, C12:3.8027, C13:3.8120, C14:3.7074, C15:0.0000,

 IC 1,  C1:3.6885, C2:3.7977, C3:3.7840, C4:3.8053, C5:3.7583, C6:3.8093, C7:3.7833, C8:3.8120, C9:3.8120, C10:3.7909, C11:3.7989, C12:3.8026, C13:3.8120, C14:3.7074, C15:0.0000,

 IC 1,  C1:3.6880, C2:3.7995, C3:3.7845, C4:3.8054, C5:3.7567, C6:3.8107, C7:3.7855, C8:3.8124, C9:3.8125, C10:3.7901, C11:3.8004, C12:3.8048, C13:3.8130, C14:3.7086, C15:0.0003,

 IC 1,  C1:3.7452, C2:3.8546, C3:3.8416, C4:3.8628, C5:3.8145, C6:3.8676, C7:3.8406, C8:3.8691, C9:3.8692, C10:3.8478, C11:3.8575, C12:3.8601, C13:3.8689, C14:3.7649, C15:0.0000,

 IC 1,  C1:3.8644, C2:3.9760, C3:3.9608, C4:3.9832, C5:3.9316, C6:3.9881, C7:3.9611, C8:3.9901, C9:3.9899, C10:3.9670, C11:3.9773, C12:3.9806, C13:3.9910, C14:3.8858, C15:0.0000,

 IC 1,  C1:3.8631, C2:3.9746, C3:3.9607, C4:3.9832, C5:3.9324, C6:3.9869, C7:3.9604, C8:3.9894, C9:3.9901, C10:3.9668, C11:3.9770, C12:3.9797, C13:3.9896, C14:3.8848, C15:0.0000,

 IC 1,  C1:3.8973, C2:4.0080, C3:3.9935, C4:4.0159, C5:3.9638, C6:4.0213, C7:3.9930, C8:4.0225, C9:4.0225, C10:3.9995, C11:4.0091, C12:4.0133, C13:4.0227, C14:3.9181, C15:0.0000,

 IC 1,  C1:3.9037, C2:4.0148, C3:3.9984, C4:4.0210, C5:3.9700, C6:4.0269, C7:3.9992, C8:4.0276, C9:4.0280, C10:4.0059, C11:4.0155, C12:4.0193, C13:6.5535, C14:6.5535, C15:6.5535,

 IC 1,  C1:4.0123, C2:4.1248, C3:4.1108, C4:4.1329, C5:4.0796, C6:4.1381, C7:4.1093, C8:4.1409, C9:4.1397, C10:4.1164, C11:4.1263, C12:4.1299, C13:4.1410, C14:4.0353, C15:0.0000,
```

Figure 6.36 Cell voltages measurement in a loop

To send the acquired data from measurement controller to the master controller, it is not possible to use the SPI configuration. This is due to the reason; this configuration has been used previously for communicating with the battery management chip. Therefore, I2C configuration is used to communicate with the master microcontroller.

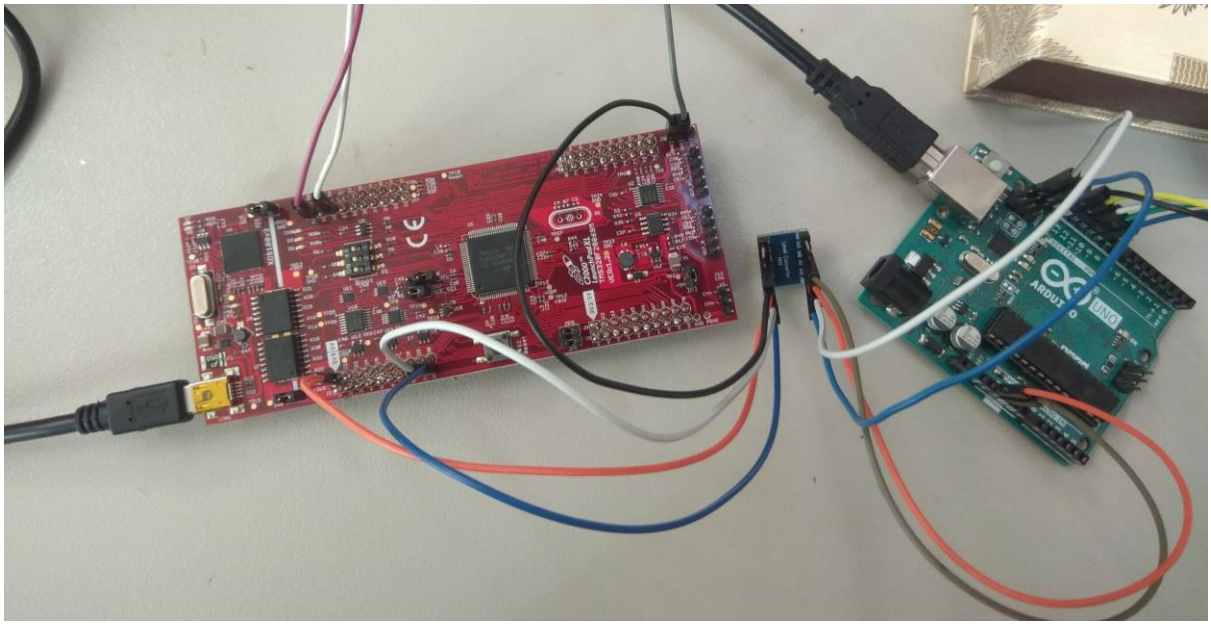

Figure 6.37 I2C communication between measurement controller and master controller.

The *Figure 6.37* illustrates communication between the two controllers. For the communication to work properly between the two controllers, logic level converter is necessary as measurement controller works with a 5V logic and master controller works with 3.3V logic. The code to send cell voltage data from measurement controller to master controller is reported below.

```
void requestEvent(){
uint8_t buff_tx[30];
for(j=0; j<15;j++)
{
buff_tx[2*j]=(BMS_IC[0].cells.c_codes[j]);
buff_tx[2*j+1]=(BMS_IC[0].cells.c_codes[j]<<8);
Wire.write(buff_tx,30);
```

Figure 6.38 Code for I_2C configuration

The cell voltages are represented in binary code in the battery management chip. Here, it is difficult to send a large number of bits through I2C in ATmega chips as I2C can usually send only a single byte at a time. So, we are limited to 255 as the large number [48]. Hence, we will split the large number and reassemble them on the master side. This ATmega chip consists of a 16-bit integer which can take 2 bytes as an integer data type. The second line in the code buff_tx[30] represents the array of 30 elements in which each cell voltage is split into two elements. The first eight bits are sent directly through I2C and the second eight bits are shifted to the right. Therefore, in the array, the first element refers to the lower significant bits and the second element refers to the higher significant bits. Similarly, for all the 15 cells, the resultant array is sent through I2C to the master microcontroller. On the receiving side, this data is again converted to uint16 for which the resultant value will be 16-bit value. The transmitted values of the master microcontroller can be seen in Matlab Simulink.

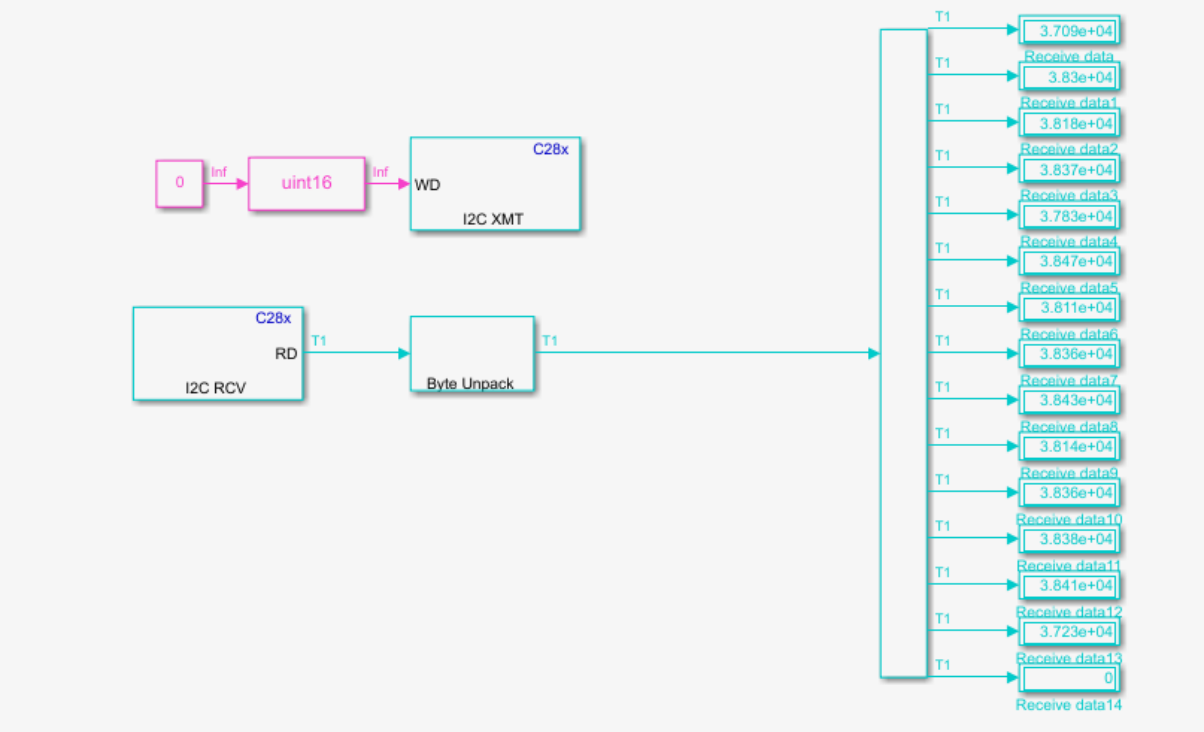

Figure 6.39 Voltage measured in the master microcontroller.

The values are multiplied by 10000 to have a higher resolution for measuring the cell voltage. From this measurement part, it is clear that we can send the battery voltage information to the master microcontroller, which is used for the sorting algorithm. This algorithm swaps the gate signals for module balancing and continuously monitors the cell voltages and battery voltage

7 Conclusion

7.1 Concluding remarks

In this thesis, a new kind of converter is designed for battery electric vehicles taking inspiration from HVDC systems. The modular multilevel converter based on double star chopper cell embedded with batteries. This converter is capable of increasing the efficiency and decreasing the space of traction drives since all the functionalities of present electric vehicles such as battery management system, traction inverter, and the on- board charging can be integrated within a single converter. The main problem of torque ripples, voltage, and current harmonics in classical two-level converter for traction applications is solved by MMC by increasing the number of modules. Possibility of bypassing modules make extra freedom to our MMC during faults. Also, possibility of swapping the modules and allowing circulating currents between the arms and phases make our MMC to converge all modules to a single state of charge which results in eliminating BMS. For charging the modules, we can either connect to household sockets of single phase or three phase supply. Also, we can connect directly to DC busbar for fast charging without additional need for power electronics since MMC will work for rated power.

At first, MMC is simulated with real MOSFET parameters and battery resistance in Matlab/Simulink to check the difference in generated output voltage with respect to the ideal modular multilevel converter. The main difference in output voltage drop, which is proportional to the current flowing in the module, is observed. Then, MMC is connected with RL load to perform the balancing operation using circulating current as a control variable. Thus, it has been observed that the fundamental component of circulating current is responsible for arm balancing, the DC component of circulating current is responsible for leg balancing, and the sorting algorithm is used for module balancing. Also, it was noticed that the speed of balancing operation depends on the allowed magnitude of the circulating current. Later, MMC is connected with an induction motor to perform speed control. The most important results validated are SoC balancing while performing the field-oriented control and flux reduction for achieving the higher speed of the motor.

The PCB design has begun with the selection of main components such as optocouplers for voltage insulation on the power side, master microcontroller, gate driver of half-bridge with initial peak current to charge the gate capacitance of semi-conductor, power MOSFET with

minimum ON-resistance and less rise and fall times to reduce conduction and commutation losses. To measure the cell voltage, a battery management chip (LTC6812) with less measurement error and high noise susceptibility is chosen with the possibility of connecting in daisy-chain for all the modules in the leg. PCB is designed with the power part at bottom and the measurement part at the left, and the communication on the top of the PCB.

Finally, the testing has been performed in the power part when the peak load current of 50A is applied. The maximum attained drain-source voltage of MOSFET is 70V which is much lower than the maximum allowable voltage of 120V. The Vgs signal of the MOSFET with ripples less than the turn ON threshold voltage does not affect its switching phases.

7.2 Future Work

The arm inductors (mutual inductor) dimensioning can be done in order to reduce the circulating currents caused by the voltage unbalance on the legs. Once the battery is installed in the module, the temperature measurement can be evaluated using the negative temperature coefficient (NTC) and send that signal to the master controller along with cell voltages. The measurement controller can communicate with other modules (daisy-chain) to measure the cell voltages. And the number of modules it can communicate through daisy chain without any disturbance can be verified. Instead of using the fan continuously to dissipate the module's heat, new control can be designed to turn on the fan after a specific temperature to reduce the losses. Furthermore, the noise generated by the adjacent modules in the converter, which affects the performance of the measurement and power parts can be evaluated.

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