



POLITECNICO
MILANO 1863

SCUOLA DI INGEGNERIA INDUSTRIALE
E DELL'INFORMAZIONE

EPFL

Microfabrication and Electrical Characterization of CMOS Compatible Foldable Electrodes for Dopamine Sensing in Brain

TESI DI LAUREA MAGISTRALE IN

- MATERIALS ENGINEERING AND NANOTECHNOLOGY -

- INGEGNERIA DEI MATERIALI E DELLE NANOTECNOLOGIE -

Author: **Andrea Pafundo**

Student ID: 259844

Advisor: Prof. Marco Carminati

Co-advisors: Prof. Sandro Carrara

Academic Year: 2025-26

Abstract

Nowadays neural implants are of growing interest in biology and medicine. Direct stimulation and sensing at neuron level can improve our understanding of the brain functioning, while introducing innovative solutions for the treatment of several disorders.

In the lively research environment formed around the topic, the Smart Micro Neural Dot project was born, aiming to the development of a wireless and miniaturized cortical visual prosthesis, based on an array of free-standing CMOS microstimulators. To this scope, penetrating foldable electrodes have been developed; however, their innovative design suggests a versatility that goes beyond vision restoration.

Electrochemical sensing represents a promising application, since neurotransmitters monitoring is of strong clinical relevance. For example, dopamine dysregulation is associated with neurological disorders, including Parkinson's and Alzheimer's disease. The aim of this thesis is to modify and optimize the fabrication process of these electrodes to meet the requirements of electrochemical measurements.

The devices are manufactured at the Center of Micro Nano Technology (CMi) of the Ecole Polytechnique Fédérale de Lausanne (EPFL). They comprise a $500 \times 500 \mu\text{m}^2$ CMOS chip and two shanks opposite to it. The latter are made of *Al* and are fully insulated by *SiO₂*, while a second metal layer acts as electrical interface. *Pt* was selected due to its high conductivity and its ability to perform dopamine sensing without surface functionalization, making dopamine also suitable for preliminary electrochemical validation. *SiO₂* provides metal insulation, exposing only sensing electrodes and test pads. Front-side fabrication is followed by substrate thinning and deep silicon etching of the backside, so to ensure devices release from processing wafer.

Electrical characterization verifies insulation effectiveness between metal layers. Finally, preliminary electrochemical impedance measurements confirm the predicted versatility of these CMOS-compatible electrodes, representing a step forward towards ultra-miniaturized neural implants.

Keywords: neural implants; brain-machine interfaces; cortical interfaces; cmos micro-fabrication; microelectrodes; platinum electrodes; electrochemical sensing; dopamine;

Abstract in lingua italiana

Oggigiorno gli impianti neurali sono di crescente interesse per biologia e medicina. La stimolazione e il rilevamento neuronali diretti migliorano la comprensione del funzionamento cerebrale, introducendo al contempo soluzioni innovative per il trattamento di diversi disturbi.

Nel vivo ambiente di ricerca sviluppatosi attorno al tema è nato il progetto Smart Micro Neural Dot, finalizzato allo sviluppo di una protesi visiva corticale wireless e miniaturizzata basata su un array di microstimolatori CMOS indipendenti. A tale scopo sono stati sviluppati microelettrodi pieghevoli penetranti; tuttavia il loro design innovativo suggerisce una versatilità che va oltre il solo ripristino della vista.

Il rilevamento elettrochimico rappresenta un'applicazione promettente, poiché il monitoraggio dei neurotrasmettitori è di rilevanza clinica. La disregolazione della dopamina, ad esempio, è associata a disturbi neurologici quali morbo di Parkinson e schizofrenia. L'obiettivo di questa tesi è ottimizzare il processo di fabbricazione degli elettrodi per adattarli alle misure elettrochimiche.

I dispositivi sono stati realizzati presso il Center of Micro Nano Technology (CMi) dell'École Polytechnique Fédérale de Lausanne (EPFL). Sono costituiti da un chip CMOS di $500 \times 500 \mu m^2$ e da due bracci opposti e da due bracci opposti, in Al e isolati da SiO_2 ; un secondo strato metallico funge da interfaccia elettrica. Il Pt è stato selezionato per l'elevata conduttività e la capacità di rilevare la dopamina senza funzionalizzazione superficiale, rendendola adatta a validazioni preliminari. L'isolamento è garantito da SiO_2 , lasciando esposti solo elettrodi e pad di test. Alla fabbricazione frontale seguono l'assottigliamento del substrato e un etching profondo del silicio dal lato posteriore per consentire il rilascio dal wafer.

La caratterizzazione elettrica ha verificato l'efficacia dell'isolamento tra gli strati metallici. Infine, misure preliminari di impedenza elettrochimica hanno confermato la versatilità di questi elettrodi, rappresentando un passo verso impianti neurali ultra-miniaturizzati.

Parole chiave: impianti neurali; interfacce cervello-computer; interfacce corticali; microfabbricazione cmos; microelettrodi; elettrodi di platino; rilevamento elettrochimico;

dopamina;

Contents

Abstract	i
Abstract in lingua italiana	iii
Contents	v
List of Tables	ix
List of Figures	xi
List of Acronyms	xv
1 Introduction	1
1.1 Overview on Neural Implants	1
1.1.1 Micro-wires Electrodes	1
1.1.2 Silicon Based Electrodes	3
1.1.3 Flexible Electrodes	6
1.2 Context of the Thesis	6
1.2.1 Smart Micro Neural Dot Project	7
1.2.2 Thesis Objectives	9
2 Electrodes Microfabrication	11
2.1 Electrodes Design	11
2.1.1 List of the Layers	11
2.1.2 Structural Layer	13
2.1.3 Foldable shanks	14
2.1.4 Electrical Layer	15
2.1.5 Top Insulation Layer	17
2.2 Front-side Fabrication	21
2.2.1 Substrate Choice	21

2.2.2	RCA and Wet Oxide Deposition	21
2.2.3	Aluminum Layer	23
2.2.4	First Photolithography	25
2.2.5	Aluminum Etching	35
2.2.6	Photoresist Strip	39
2.2.7	Silicon Dioxide Deposition	41
2.2.8	Platinum Layer	42
2.2.9	Front-side Insulation	48
2.3	Back-side Fabrication	51
2.3.1	Back-side Grinding	51
2.3.2	Hard Mask Deposition	54
2.3.3	Parylene Coating	54
2.3.4	Hard Mask Etching	57
2.3.5	Silicon Etching	59
2.3.6	Backside Insulation	64
2.4	Probes Release and Bending	65
2.4.1	Carrier Wafer	65
2.4.2	Electrodes Release	67
2.4.3	Shanks Folding	68
3	Experimental Results and Discussion	71
3.1	Electrodes Fabrication	71
3.1.1	Aluminum Deposition	71
3.1.2	Photolithography Inspection	73
3.1.3	Aluminum Shanks Inspection	74
3.1.4	Platinum Tracks Inspection	78
3.1.5	Insulation Layer and Electrodes Geometry Inspection	80
3.1.6	Wafer Preparation to Backside Etching	84
3.1.7	Back-side Silicon Etching	86
3.1.8	Probes Release	90
3.1.9	Deep Silicon Etching Issue	91
3.1.10	Probes Folding	94
3.2	Electrical Testing	95
3.2.1	Testing at Probe Station	95
3.2.2	Platinum Electrodes Inspection	100
3.3	Electrochemical Characterization	102
3.3.1	Introduction to Electrochemistry	102

3.3.2	Sample Preparation	105
3.3.3	Electrochemical Impedance Spectroscopy	109
	Conclusions and Future Developments	115
	Bibliography	117
	Acknowledgments	131

List of Tables

2.1	Titanium and Aluminum spider 600 process parameters	24
2.2	<i>AZ ECI 3000</i> suggested surface treatments	27
2.3	Etching rates on Cobra 100	38
2.4	Recipes available on <i>D250L PECVD</i> for SiO_2 deposition	41
2.5	Platinum process parameters on <i>Spider 600</i>	42
2.6	Recipes available on <i>SPTS APS</i> for SiO_2 etching	50
2.7	Si thinning recipe used for stress release	53
2.8	SiO_2 process parameters in <i>Spider 600</i>	64
3.1	Parameters for Wire Bonding	108

List of Figures

1.1	Tetrode and Wires Bundle	2
1.2	Michigan Probe	4
1.3	Utah Array	5
1.4	Smart Micro Neural Dot Project	7
1.5	Foldable Electrodes Concept	8
2.1	Scheme of the layers of the probes	12
2.2	Silicon Structural Layer Design	13
2.3	Area affected by etching processes	14
2.4	Foldable Aluminum Shanks Design	15
2.5	Platinum Layer Design for Three Electrodes	16
2.6	Platinum Layer Design for Multiple Electrodes	17
2.7	Standard Design of Foldable Probes	18
2.8	Multiple WEs Design of Foldable Probes	19
2.9	Small Electrodes Design of Foldable Probes	20
2.10	Design of Foldable Probes for WE Functionalization	21
2.11	100mm <i>Si</i> wafers	21
2.12	Dry and Wet Oxidation Times Comparison	23
2.13	<i>Si</i> wafer section	23
2.14	Wafer cross section after <i>Ti</i> and <i>Al</i> deposition	25
2.15	HMDS reaction on Si substrate	27
2.16	Spin coating steps	28
2.17	<i>AZ ECI 3007</i> spin curve	28
2.18	EC and EBR procedures	29
2.19	MLA focusing and edge detection mechanism	30
2.20	MLA 150 focus	30
2.21	Dose test examples	31
2.22	Positive and negative tone PR	31
2.23	Automatic development techniques	32
2.24	shanks design negative	33

2.25 Photolithography steps	34
2.26 Descum	34
2.27 Wet etching isotropicity	35
2.28 Optical Emission Spectroscopy Plot	37
2.29 Laser EPD plots	37
2.30 Etched Al Layer Scheme	38
2.31 Oxygen Plasma Asher	39
2.32 UFT Wet Bench Flowchart	40
2.33 Al pattern scheme	40
2.34 SiO ₂ deposition on Al scheme	42
2.35 Pt deposition scheme	43
2.36 Automatic cross detection on MLA 150	44
2.37 Alignment marks	44
2.38 Vernier scales	45
2.39 SIMS EPD system typical signal curves	46
2.40 Fences Formation on PR Walls during Sputtering	47
2.41 Thermal Reflow	47
2.42 Reflow Effects on Redeposition	48
2.43 Pt etching scheme	48
2.44 SiO ₂ deposition scheme	49
2.45 SiO ₂ etching scheme	50
2.46 Protection layer coating scheme	51
2.47 Grinding Mechanism and Edge Sharpening	52
2.48 Wafer Grinding scheme	53
2.49 Si Thinning for Stress Release scheme	54
2.50 Hard Mask Deposition scheme	54
2.51 Silanization Process and Effects	56
2.52 Parylene Deposition Method	56
2.53 Parylene Protection Layer scheme	57
2.54 Backside Alignment: Marks Regions and Mirroring	58
2.55 Hard Mask Etching scheme	59
2.56 Second back-side Photolithography scheme	60
2.57 Bosch Process Cycle	61
2.58 Back-side Si step definition, scheme	62
2.59 Deep Si Back-side Etching, scheme	63
2.60 SiO ₂ Backside Deposition scheme	65
2.61 Wafer Carrier Design	66

2.62	Wafer Carrier scheme	66
2.63	Wafer Positioning on the Carrier scheme	67
2.64	Released Electrodes scheme	68
2.65	Bending Device	69
2.66	Final Bent Probe scheme	69
3.1	Toho FLX 2320-S Functioning Principle	72
3.2	Common Problems in Photolithography	74
3.3	Aluminum Shank Optic Microscope	75
3.4	Secondary and Backscattered Electrons	76
3.5	Aluminum Shank Tip Topology	76
3.6	X-ray Emission Principle	77
3.7	Silicon Dioxide Energy Spectrum	77
3.8	Aluminum Step Profile	78
3.9	<i>AZ 10XT-20</i> Before and After Reflow	79
3.10	Platinum layer overview and trench details	80
3.11	Probe Standard Design (optic microscope)	81
3.12	Probe Multiple Electrodes Design (optic microscope)	82
3.13	Probe Multiple Electrodes Design (optic microscope)	83
3.14	Probe Electrodes for Functionalization Design (optic microscope)	84
3.15	Visible and IR Microscopy Setup	86
3.16	Frontside-Backside Alignment	87
3.17	Frontside-Backside Tip Alignment	88
3.18	Released Probe	91
3.19	Release Probes Bottom and Side Views	91
3.20	SEM Images of CF_4 residuals on sample backside)	92
3.21	CF_4 residuals and Si spectra	93
3.22	Released Probe, Comparison with Human Finger	94
3.23	Probe Station Impedance Measurement Setup	96
3.24	RC Parallel Circuit Bode Plots	96
3.25	Median Impedance between CE and the other Shank, Bode Plots	98
3.26	Impedance Magnitude Comparison	99
3.27	Impedance Magnitude Comparison	100
3.28	Platinum Tracks Short-circuiting due to Redeposition	100
3.29	Pt redeposition EDX analysis	101
3.30	Electrode-electrolyte Interfaces	103
3.31	Potentiostat Three Electrodes Configuration	105

3.32 PCB Design	106
3.33 Sample positioned and wire bonded on the PCB	108
3.34 Poor and Good <i>Al</i> insulation comparison	109
3.35 Experimental Setup Scheme for EIS	110
3.36 EIS of $2000\mu m^2$ <i>Pt</i> electrodes) Electrodes	112
3.37 EIS of $20'000\mu m^2$ electrodes and comparison with $2000\mu m^2$ ones	113
3.38 EIS Comparison of $2000\mu m^2$ electrodes and literature	114

List of Acronyms

BSE Back Scattered Electron

BSR Back Side Rinse

CD Critical Dimension/s

CE Counter Electrode

CMi Center of Micro Nano Technology

CMOS Complementary Metal-Oxide-Semiconductor

CVD Chemical Vapor Deposition

DC Direct Current

DI DeIonized

DMSO DiMethyl SulfOxide

DRIE Deep Reactive Ion Etching

DSP Double Side Polished

EBR Edge Bead Removal

EC Edge Clean

EDS/EDX Energy Dispersive Spectroscopy/X-ray spectroscopy

EPD End Point Detection/Detector

EPFL Ecole Polytechnique Fédérale de Lausann

FEA Finite Element Analysis

FFR Fast Fill Rinse

FWHM Full Width at Half Maximum

HMDS HexaMethylDiSilazane

IPA IsoPropyl Alcohol

IR Infra Red

MEA Micro Electrodes Array

MEMS Micro-Electro-Mechanical Systems

MFIA Multi-Frequency Impedance Analyzer

OES Optical Emission Spectroscopy

PBS Phosphate-Buffered Saline

PECVD Plasma Enhanced Chemical Vapor Deposition

PEB Post Exposure Bake

PI PolyImide

PM Process Module/s

PR PhotoResist

PTFE PolyTetraFluoroEthylene

QDR Quick Dump Rinser

RCA Radio Corporation of America

RE Reference Electrode

RF Radio Frequency

RIE Reactive Ion Etching

RPM Rotations Per Minute

RSD Relative Standard Deviation

SDD Silicon Drift Detector

SE Secondary Electron

SEM Scanning Electron Microscope/Microscopy

SIMS Secondary Ions Mass Spectroscopy

SNR Signal to Noise Ratio

SOI Silicon-on-Insulator

SRD Spin Rinse and Dry

SSP Single-Side Polished

TT Trickle Tank

TTV Total Thickness Variation

UV Ultra Violet

VPU Video Processing Unit

WE Working Electrode

1 | Introduction

Brain has always been one of the most fascinating systems in biology, due to its complexity and to the mysteries hidden behind it, yet to be discovered. A wide variety of signals are transmitted within the neural network, both due to neurons discharges and to the release of neurotransmitters, all contributing to: sensory perception, motion, cognition, and emotions [1]. The possibility of detecting both these signals, directly into the brain, can significantly improve our understanding on the system. Moreover, the development of prosthetic devices, based on neural electronic interfaces, can improve the treating of various disorders [2]. Through the years a wide variety of solutions have been proposed to achieve intracortical and deep brain stimulation and recording; here a brief summary of the main typologies of these devices is provided. Particular attention will be posed on *Si* based systems, to which the Smart Micro Neural Dot project, foundation of this thesis work, belongs to.

1.1. Overview on Neural Implants

Despite the wide variety of solutions that have been proposed to achieve stimulation and recording into the brain tissue, three main categories of electrodes can be defined: micro-wires, flexible electrodes and silicon based devices. To have clear understanding on the context in which this project is inserted, a brief discussion about the main advantages and limitations of all these typologies is required.

1.1.1. Micro-wires Electrodes

The earliest examples of neural implants were single-site metal wires, in which a metallic filament is insulated, except for the tip, and is then inserted into the brain. A pioneering case is given by Hubel in 1957, who used a tungsten wire, insulated up to the tip, to record single neuron action potentials [3]. Apart from tungsten, other materials that have been used in their fabrication are: platinum [4], platinum-iridium alloys [5] and titanium [6]. Usually insulation is achieved by coating the wire with bio-compatible polymers, such as parylene [7] or PTFE (teflon) [8]. Moreover, impedance reduction to improve

signal recording and noise can be obtained by surface treatments on the electrode tip, such as carbon nanotubes coatings [9]. Despite offering the possibility of achieving single neuron level recordings, in deep areas of the brain, these wires, as stated in their name, are limited to detection in a single site. In order to retrieve informations across a wide region of the neural network, multi-sites systems are required. These can be obtained either by fabricating wires able to simultaneously detect and discern multiple neuron signals or by arranging multiple wires into arrays, so to reach large lateral extension.

Some notable examples for the first approach are the stereotrode [10] and its evolution, the tetrode [11, 12], respectively composed of 2 and 4 metallic wires, encapsulated to the tip in an insulator and twisted together. They are based on the fact that different spike-amplitude ratios are detected, for cells with different distance ratios from the electrodes tips [10]. In more recent years a further evolution of the concept has been brought by implementations of heptodes [13, 14] that enhance recording and allow sorting of the spikes. Another possibility to achieve multi-site sensing, is to use long shafts or needles along which multiple electrodes are linearly distributed [15, 16]. However due to their rigidity these devices tend to induce inflammatory response and glial cells growth around them [17] reducing significantly their performances [18]. This makes them more suitable for acute recording than chronic implantation.

To improve the lateral reach of wire electrodes, they can be disposed in bundles, manually or semi-automatically. A similar system has been used, for example, even in clinical trials on the temporal lobe of patients affected by epilepsy [19].

Despite being able to reach single neuron stimulation and recording, metal micro-wires have some major limitations: they tend to degrade, loosing signal quality with time [20], moreover, due to their fragility, they require rigid catheters for the insertion, worsening the tissue damage during implantation.

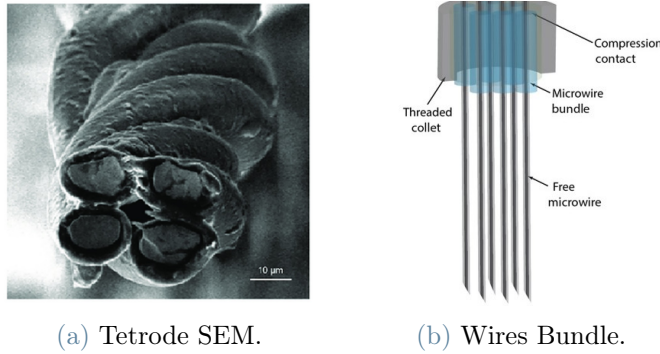


Figure 1.1: (a) Scanning Electron Microscope (SEM) image of a tetrode electrode, from [21]. Scheme of a wires bundle based system for neural recordings, taken from [22].

1.1.2. Silicon Based Electrodes

Advancements in micro and nano-machining technologies have offered the opportunity of avoiding the traditional production and assembly method used for wire-based neural implants, in favor of *Si*-based fabrication methods. These allow a precise control over shape and size of fabricated micro-electrodes, with a precision of 1μ or less, so that the integration of tens of channels in considerably small devices becomes possible [23]. Moreover miniaturization improves the organism response to the implantation, reducing inflammatory response and scar tissue formation [20, 24]. Since the electrodes fabricated for the project are also *Si*-based, a more extensive summary of the most renewed examples in literature is provided.

Michigan Electrode Array

One of the first *Si*-based devices was developed in 1970 by the University of Michigan [25]. It consists of a flat probe that acts as a substrate for thin-film deposited micro-electrodes, insulated by dielectric layers. On each probe multiple independent electrodes can be placed, offering the possibility both for cortical and deep brain detection, depending on the probe length, that goes from *mm* to few *cm*. Moreover, thanks to its flat surface, the probe is suitable for embedding of on-chip electronics for control of the device itself. The fabrication process is based on the selective diffusion of *B* into a silicon wafer, so to define shape and thickness of the final probe. Then *Si* insulation is achieved by Chemical Vapor Deposition (CVD) of SiO_2 or Si_3N_4 . Selective etching of the dielectric layer offers the access to the doped polysilicon substrate. Recording sites are obtained by metal layers on top of the dielectric; the metal are deposited and patterned to produce electrode sites and pads, by lift-off techniques. A second dielectric deposition and etching is used to expose the recording sites. After the wafer is thinned, it is placed in ethylenediamine-pyrocatechol, which selectively etches away the undoped silicon. This fabrication method allows to obtain a wide variety of sizes and shapes, depending on the target of application desired [26].

Another interesting possibility offered by these probes is to arrange them in arrays, in order to obtain record and stimulation of a large number of neurons in 3D space [27]. The main downside of this probes are related to their fragility and rigidity. In fact, due to the first, mechanical stress can lead to fractures, limiting their use for long term implantation [28]. While the second can induce foreign body response and glial scar tissue formation, due to mismatch in micro-movements of the probes with respect to the brain [29].

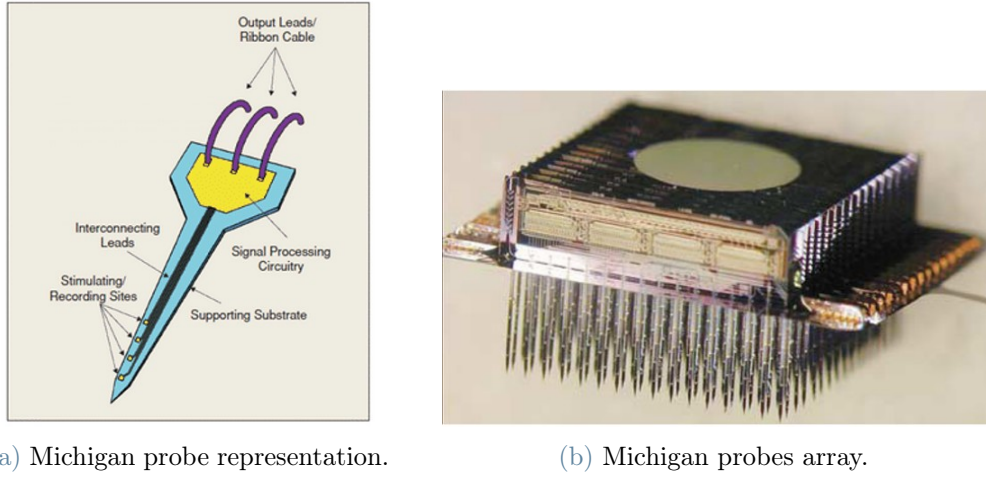


Figure 1.2: (a) Single Michigan probe representation. Taken from [30]. (b) 3D array of Michigan probes, from [31].

Utah Electrode Array

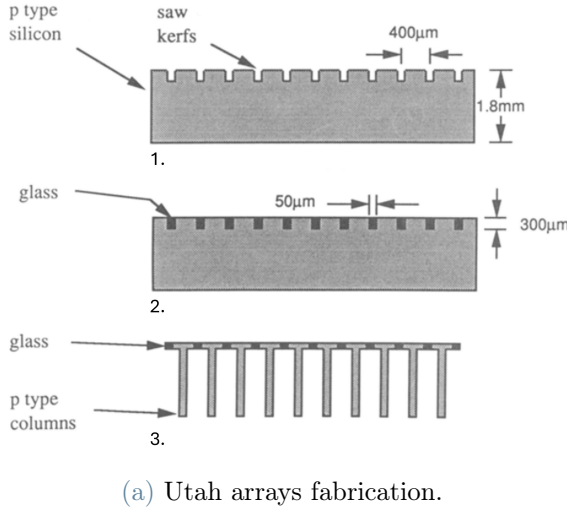
Another well known silicon based device is the Utah array developed by Norman and colleges in the 90s [32, 33], consisting in silicon column vertically oriented with respect to the substrate. A unique method was initially used for their fabrication: thermomigration [34]. Thanks to it electrical insulation of individual electrodes is achieved before any micromachining, by exploiting a pair of opposing p-n junctions between any two columns. Nowadays a different method is exploited, in which on one side of the wafer saw kerfs are carved and filled with fused frit glass, that is then let solidify. Then deep saw kerfs remove a significant portion of the material, leading to the production of an array of long independent electrodes "essentially suspended in a sea of glass substrate" [34].

Utah electrode array has an electrically active site at the tip of each column, while the remaining structure is insulated with biocompatible materials. In addition the tip are usually coated by *Pt* or *Au*. Finally, there is the possibility of having all the electrodes with the same height [32] or with different ones, so to detect signals coming from different regions of the cortex [35]. Further improvements of these devices consists in the fabrication of multiple active sites along each probe, singificantly increasing channel density with respect to traditional arrays [36]

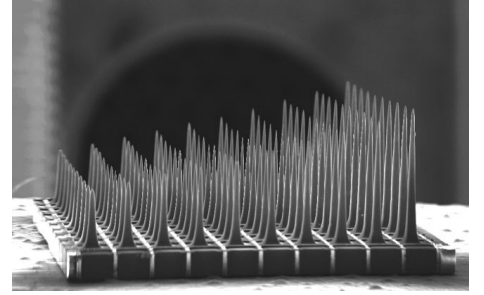
Utah arrays are well known in terms of clinical trials and have been used for a wide variety of applications, such as artificial limbs control [37], sensory feedbacks [38] and phosphenes generation to restore weak perception in visually impaired patients [39].

Due to their dimensions Utah arrays are limited for implantation in the cerebral cortex and are not suitable for deep brain stimulation or recording. However, the main issue is related to their structure, in fact, compared with the thin Michigan probe, they consists

of about 100 needles, usually capable of recording signals from a single site each, such a density of penetrating objects can induce strong foreign body response in chronic implants [20, 40].



(a) Utah arrays fabrication.



(b) Slant Utah array.

Figure 1.3: (a) Fabrication scheme of Utah arrays based on saw kerfs. Taken from [34]. (b) Slant Utah electrodes array, image from [35].

Recent Developments

In recent years, many other silicon based systems have been proposed, demonstrating the vivid research interest that these devices still offers. Some relevant examples, for which in-vivo tests have been performed, are reported:

- MEMS wafer processing technology is used for the realization of silicon probes, by sputtering Ti and TiN conductive layers on silicon-on-insulator (SOI) substrate. Then the probes are released and recording sites are modified with carbon nanotubes, grown by CVD, to increase the surface area significantly, reducing the overall impedance. These electrodes were tested in primates to record epileptic seizures [41].
- A linear, Michigan inspired, Micro Electrodes Array (MEA) has been fabricated. The device has 16 recording sites, a length of 25mm and a cross section of $30 \times 300 \mu m^2$. Recording sites have been modified with platinum black nanoparticles and nafion, a fluoropolymer, so to make them suitable both for spikes recording and dopamine detection, an important neurotransmitter [42].
- Neuropixels electrode are based on CMOS technology, that allows to dramatically reduce recording sites size, in order to increase the density of them on the probe.

Critical dimensions offered by CMOS technologies are in the order of $100nm$, unlike traditional photolithography, that can usually not go beyond $1\mu m$. This allowed the production of a single $10mm$ long electrode, with a cross section of $20 \times 70\mu m^2$, embedding in it almost 1000 recording sites [43].

1.1.3. Flexible Electrodes

It has been observed how one of the main issues of neural implants listed above, especially for chronic implantation, is given by the immune response caused by the movement between rigid bodies and the brain. A possible solution to reduce such response is to exploit flexible electrodes, in particular *parylene-C* and polyimide are used as substrates to embed thin film micro-fabricated MEA. These polymers are often used due to their compatibility and mechanical properties very close to the one of brain tissue [44]. Despite the advantage of inducing minimal inflammatory response, these electrodes share the same problem in deep implantation seen for metal micro-wires, the need of a rigid support for the insertion. So, together with the electrodes, it is crucial to design a support for implantation, that can then be removed afterwards [23]. The interest towards flexible multichannel electrodes has been significant in recent years both from academia and industry.

In the first, a notable example is the Neuroscroll, an over 1000 channels probe, fabricated by clean-room level processes on PI films and then rolled into W wires. In-vivo studies on rodents show highly stable and reliable recording for up to 105 weeks [45]. Other inserting results have been obtained by fabricating two mechanically robust ultra-flexible electrode shanks on PI substrate, each with 64 microelectronics, for long-term recoding in the brain cortex [46].

Commercially available flexible devices have been also released, such as the MicroFlex, a 24 channel array used both for stimulation and recording [47], or Neuralink, already known to the general public, possessing more than 3000 gold recording sites [48].

1.2. Context of the Thesis

Among the various applications of neural implants, one of the most researched are visual prosthetics, ultimately aiming to the restoration of vision in blind patients. This is usually done bypassing damaged sections and directly activating downstream parts of the visual system. Among the various methods to achieve such a goal [49], cortical implants have the key advantage to avoid entirely visual pathways and directly stimulate areas of the brain related to visual signals processing. This is especially advantageous since it allows to treat

patients with many different medical conditions and injuries. One of the most common methods is the stimulation of these areas by electric impulses, inducing generation of phosphenes [50]. These are a visual sensations that, after a training period, can allow the patients to proficiently distinguish objects [49]. To achieve this goal the Smart Micro Neural Dot project has been developed.

1.2.1. Smart Micro Neural Dot Project

To achieve a reliable chronic implantation in the cortical tissue, the projects aims to exploits an array of CMOS compatible microeletrodes, relying on a wireless powering system [51–54]. Avoiding presence of bulky cables connections to an external power source, in fact, is one major step forward into limiting foreign body repose in such implants. The working principle, as illustrated in fig. 1.4, exploits an external camera to black-and-white images of the environment, then these signals are elaborated by an external Video Processing Unit (VPU). The informations related to the images, converted into binary format, are transmitted via wireless from an external transmitter to an array of free-floating penetrating electrodes thanks to inductive coils. The electrodes convey electrical impulses to the brain cortex, for the production of phosphenes. Among the variolous challenges that designing such a system implies, the one of interest to the scope of this thesis is the fabrication of the electrodes themselves.

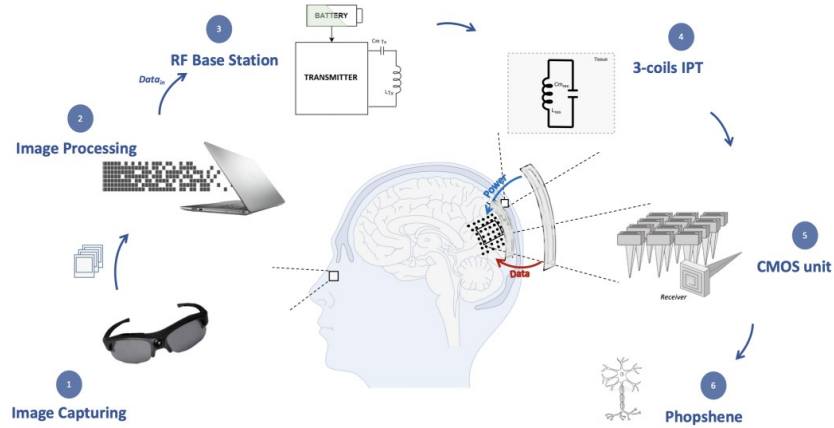


Figure 1.4: Schematic that shows the functioning principle behind the Smart Micro Neural Dot Project.

In order to produce these micro-electrodes, an innovative process has been proposed. Nowadays, the great majority of silicon based micro-electrodes are manually affixed to CMOS pads, consistently reducing the reliability and repeatability of the binding. Moreover, due to this approach scalability is also affected. The idea is then to produce elec-

trodes in which the CMOS circuitry is embedded in the electrodes itself. This is done by post-processing of a wafer on which CMOS front-end has been fabricated. Starting from this substrate, probes can then be fabricated by a combination of front-side and back-side machining in a clean-room level environment, this process will be discussed in great details in chapter 2. The probes obtained are composed of three main parts: a central chip, on which the circuitry are embedded into, and two shanks on the opposite sides of it. The three components are connected by hinges, that allow a 90° folding of the shanks with respect to the chip plane, in order to allow penetration of the cortical tissue. An active site is present on each tip, allowing stimulation and phosphene production in the implanted area. Each probe is able to convey a single pixel to the brain, so for image reconstruction implantation of an array is required.

This pioneering design offers numerous advantages with respect to the traditional examples of *Si*-based cortical implants, such as the Utah array:

- **Wireless:** the absence of wires for powering and signal transmissions reduce inflammatory body response.
- **Floating:** reduced mismatch in micro-movements between penetrating electrodes and brain, diminishing glial scar tissue formation.
- **CMOS-compatible:** Improved reliability and repeatability in the fabrication, avoiding any manual embedding of electrodes and electronics.
- **Micro-fabricated** Great scalability of the process, possibility of varying parameters, based on the final purpose.

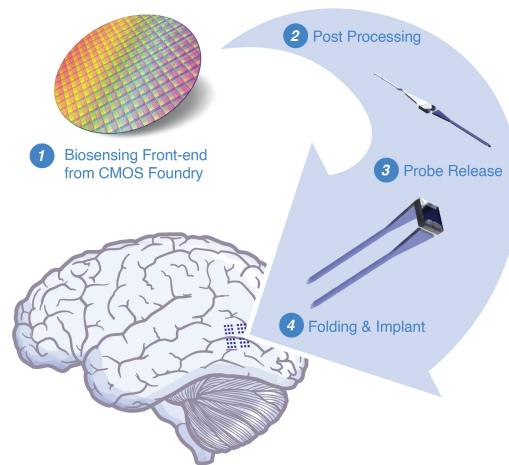


Figure 1.5: Scheme representing the basic idea behind foldable micro-electrodes, from the starting substrate to the implantation.

1.2.2. Thesis Objectives

Despite the initial purpose for which these electrodes have been conceived, it is evident that they offer a versatile and innovative approach into achieving neural stimulation and recording in the cortex. Among the the different possibilities offered by the system, electrochemical detection of neurotransmitters in the brain offer a great opportunity to verify it's versatility and an important step towards the realization of all-in-one devices, able to simultaneously process stimulation and detection.

This thesis work, in particular, focus on the realization of micro-electrodes for dopamine detection, that is clinically relevant neurotransmitter [42], strongly associated with Parkinson's disease [55] and schizophrenia [56]. In additon, thanks to its quasi-reversible redox behavior, it's a suitable analyte for preliminary electrochemical measurements, without the need for specific surface functionalization. At this scope, a modified version of the fabrication procedure, for the obtainment of foldable electrodes, has been developed. Moreover, according to previous experimental observations, some general optimizations have been implemented. It is also worth mentioning that, despite not being part of the discussion found in the following pages, an ultra miniaturized and fully digital potentiostat has already been developed [57]. The circuit is considerably smaller than the central chip of the probe, ensuring the possibility of future embedding into it.

In addition this thesis aims to perform, for the first time, electrical characterization of the devices, in order to ensure the independence between different channels of the electrodes. Finally preliminary electrochemical characterization is performed, so to estimate the impedance range of the system, once immersed in electrolytic solutions, and to compare its behavior with electrodes of similar size present in literature.

2 | Electrodes Microfabrication

Through the following chapter the design of the electrodes and the reasoning behind it will be described, together with their fabrication procedure. In particular four macro topics will be discussed: design, front-side fabrication, back-side fabrication, probe release and bending.

2.1. Electrodes Design

Having assessed the basic concepts behind the idea of foldable CMOS compatible neural probes, in section 1.2.1, a description of the actual samples produced during this project is imperative. In particular all the designed layers that need to be shaped for the fabrication of the probes will be shown, focusing on the reasons that brought to the choices made in term of geometries.

First of all, a general description of the layers present in the probes will be provided. Then, each layer will be addressed and discussed, starting from the one at the bottom going towards the top. As it will be discussed in next sections, this is not the order of fabrication of the layers, but this approach is more intuitive and avoid unnecessary confusions. Moreover, once the structure will be clarified, following the steps required for its fabrication will be much more natural.

2.1.1. List of the Layers

A scheme of the layers that are going to be enunciated is depicted in fig. 2.1.

- **Bottom Insulation Layer:** At the very bottom of the probes an insulation layer has to be present, in fact this is a surface directly exposed to the environment. The layer has to be an insulator, able to resist to the conditions of the cortical tissue and bio-compatible.
- **Structural Layer:** Its main purpose is to increase the stiffness of the probes. From previous studies [58], in fact, it has been proven that its absence cause bending of the thin foldable shanks. In addition it also constitutes the layer in which the chip

will be embedded in the final version of the probes, so it must be a material used in CMOS industry, in particular *Si* has been chosen.

- **Middle Insulation Layer n.1:** It has the scope of separating the structural layer from the metallic bendable shanks, insulating them electrically.
- **Layer for Bendable shanks** It has been decided to separate bendable shanks and electrical paths, so to have more freedom in changing number and position of the electrodes, without having to overturn the probes design. So the layer has a purely structural purpose, it must be sufficiently stiff not to bend during insertion into the brain, while being ductile enough to allow shanks folding without breakage.
- **Middle Insulation Layer n.2:** It separates the shanks from the electrical layer.
- **Electrical Layer:** It comprises all the electrodes, tracks and pads present on the shanks. It must be bio-compatible and electrically conductive, in addition, to achieve electrochemical sensing, it must be made of a material whose properties in such field are renewed.
- **Top Insulation Layer:** It has the same function of the insulation layer on the bottom, in fact the two combined encapsulate completely the probes. In addition to it, the layer also defines the exposed areas of electrodes and testing pads.

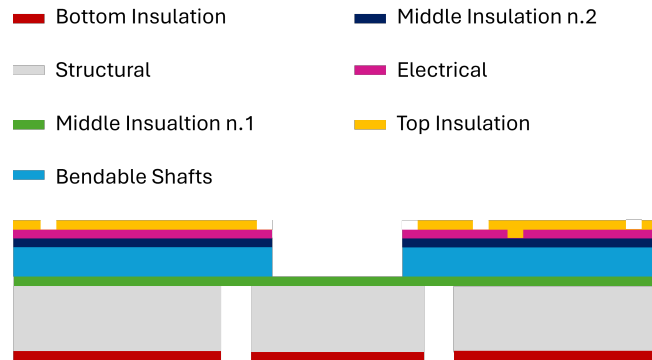


Figure 2.1: A simplified version of the design of the probes, in which each layer is identified with a different color, independently on its material.

Before proceeding further, it should be noted that all the insulation layers presented do not require any patterning, since they follow the shape of the other features presented, so they won't be discussed in the following subsections. The only virtuous exception is the top insulation, whose geometry determines the exposure to the environment of the electrical layer. To ensure an intuitive visualization of the top view of the probes, the same color scheme of fig. 2.1 will be applied to the following designs.

Finally it is worth to remind that, when it comes to *Si* based micro-fabrication techniques, the design, essentially, can be only performed in 2D, while the thickness of each layer is given by process parameters, these last ones will be discussed in depth in section 2.2 and section 2.3. The software used to design the probes is *KLayout*, an open source layout viewer and editor [59], able to generate files in a format compatible with the tools used for manufacturing the samples [60].

2.1.2. Structural Layer

As discussed in previous subsection, the purposes of the layer are to increase the stiffness of the whole structure and to define the square in which the integrated circuits will be allocated. In particular a $500 \times 500 \mu m^2$ square is located at the center of the probes, an area more that sufficient to host the custom ultra-miniaturized potentiostat that's been developed to control the fabricated electrodes [57]. It has been already demonstrated that such area could be reduced even further, previous versions of the probes have been produced with a central square of $250 \times 250 \mu m^2$. However, to facilitate electrical testing, one of the novelties of the following work, a larger surface area has been preferred.

The supports of the folding shanks matches the geometry of the latter, the reasons behind which will be discussed shortly; but one of the most important parameters to take into account is the distance between such supports and the central square. In fact, such distance has to be larger than the thickness of the layer itself, otherwise folding is prevented. In the case in exam its value is $74 \mu m$, while the structural layer is only $30 \mu m$ thick, so no hindrance is expected. Even considering some safety margins, there is still the possibility of increasing structural layer thickness without modifying the probes design, nevertheless it has been previously assessed that $30 \mu m$ of *Si* offer an adequate rigidity to the shanks, avoiding their bending and buckling during insertion in brain tissue [58].

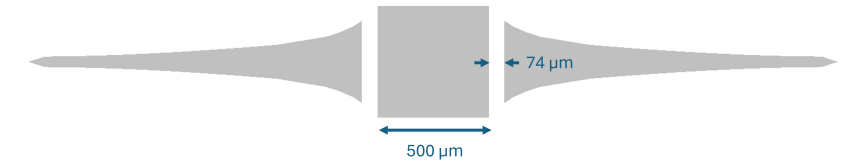


Figure 2.2: Design of the *Si* structural layer, a $500 \times 500 \mu m^2$ square is seen in the center, while the shanks support are distanced from it by $74 \mu m$

To avoid processing of the whole wafer, during patterning of each layer, that would cause a embrittlement of the substrate and an high possibility of catastrophic failure, only a

small portion of the surfaced is affected by etching steps. This is defined by an ellipse around each sample, as depicted in fig. 2.3, while the rest of the wafer will maintain its original thickness.

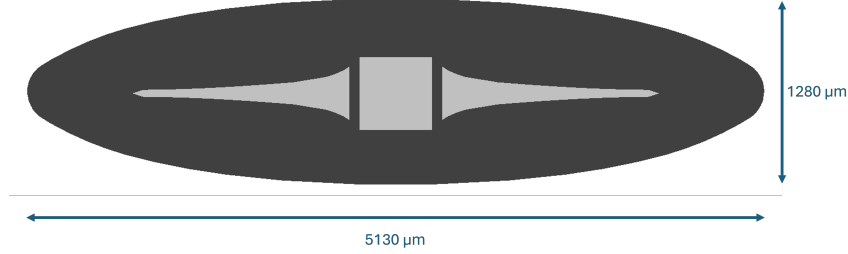


Figure 2.3: Ellipse that denotes the area affected by etching processes. Its major axis is about $5130\mu m$ long, while its smaller has a length of $1280\mu m$.

2.1.3. Foldable shanks

The key feature, that differentiate the probes in exam from other devices for neural stimulation and recording, is the CMOS compatible process through which they are produced. To be able to penetrate the cortex though, sharp and pointy structure are required, this is achieved, as anticipated, by foldable shanks. These structures are fabricated on the same plane of the central square, in which the electronic devices will be embedded, and are then bent, until they are orthogonal to it. So the material to use have to be flexible and ductile enough to be folded by a 90° angle, without failing, but at the same time, no deformation of the shanks has to occur during insertion. It has been shown in previous studies that aluminum meet such requirements [58]. In addition to it, such material is compatible with CMOS industry and thick layer of it can be deposited on top of wafers. In case of neural stimulation, as briefly discussed in section 1.2.1, two electrodes, one per shank, are sufficient to achieve the prefixed goal. For this reason, in that case, *Al* layer can be used both as structural layer and as electrical connection between the central chip and the electrodes on the shanks tips. If one aims to record electrochemical signal, three electrodes are required: a Working Electrode (WE), a Counter Electrode (CE) and a Reference Electrode (RE) [61]. The reasons behind it will be discussed in depth in section 3.3.1, at the moment it's sufficient to say that: to exploit *Al* shanks as electrical layer, while keeping at the same time three independent electrodes, a trench that separates one of the beams should be implemented. This approach has multiple limitations, first of all the presence of such a trench may alter structural stability of the shank that it splits. Secondly, it limits the number of electrodes that one could implement on a single shank, since for each one a trench would be needed, compromising stability even further.

For these reasons a more reliable and versatile approach has been selected, in which *Al* layer is used purely for its mechanical properties, it is then insulated and the electrodes are patterned on top of the shank, using a different metal layer. In particular a thickness of $4\text{ }\mu\text{m}$ has been selected, since it meets the discussed structural requirements.

The shape of the shanks is largely based on the one of the *Michigan Probe*, due to its proven structural stability [25]. The total length of each beam is $1656\text{ }\mu\text{m}$, so that, after bending, deep regions of the brain cortex can be reached. A portion of each shank, with a length of only $82\text{ }\mu\text{m}$, overlaps the area of the central square, connection between the two components is guaranteed simply by adhesion, the stability of such bond has been demonstrated in previous versions of the process.

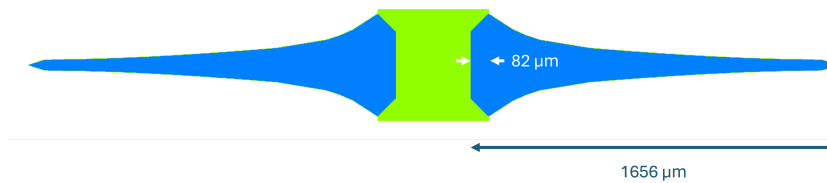


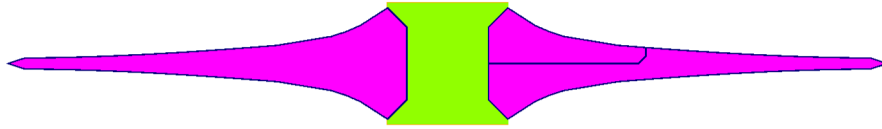
Figure 2.4: Aluminum shanks are depicted, both the total length of each shank and the one of the region anchored to the central chip are remarked. It can be noticed that between the *Al* shanks and *Si* components, a middle insulation layer is present (in green).

2.1.4. Electrical Layer

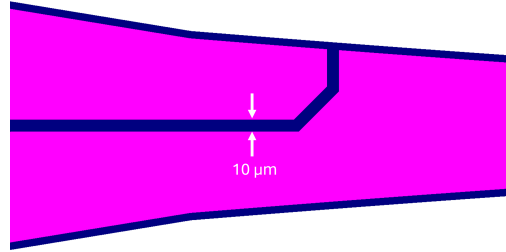
Having separated structural purposed layers from the electrical one, the only restrictions related to the material choice of the latter are related to its application. The material has to be conductive, biocompatible, and suitable for the electrochemical detection of the target molecule. The first material that comes to mind, when considering dopamine detection, i.e. the molecule that we aim to record with the fabricated device, is platinum. This is particularly advantageous since it matches all the enunciated characteristics and it even allows dopamine detection without a surface functionalization of the electrodes [42]

Let's now discuss the reasoning behind the design of the geometry of the layer. As a general rule, to minimize parasitic capacitances, metal track that connect pads and electrodes should be as narrow as possible. It can be easily seen from fig. 2.5, that a completely opposite approach has been chosen, in fact *Pt* covers almost entirely the surface of the properly insulated shanks. The beam that hosts two electrodes has the *Pt* layer split in two sections by a trench, with a width of $10\text{ }\mu\text{m}$. This approach has been chosen since, despite not being optimal from a Signal to Noise Ratio (SNR) point of

view, it ensures connection between pads for testing, that will be positioned at the base of the shank, and the electrodes along it, even after bending. The core idea behind this choice, then, is to ensure the resilience of the electrical layer and the functioning of the probes before and after folding procedure. Then, after such assessment will be completed, optimization of the design to increment SNR will be implemented.



(a) Platinum Layer on the Probes

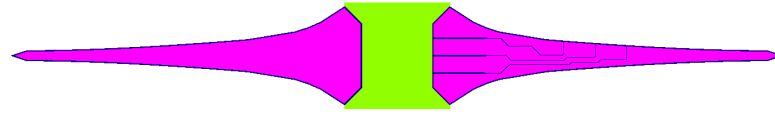


(b) Trench between Platinum Regions

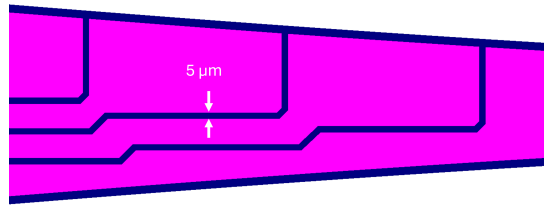
Figure 2.5: (a) The platinum layer (purple) cover the probes shank, separating them in three region, each one corresponds to an electrode. (b) Detail of the $10\ \mu m$ trench that separates the two electrodes on the shank on the right.

In addition, the possibility of having multiple working electrodes on a single shank has been explored, by simply increasing the number of trenches, separating the layer in four independent conductive paths. To be able to do so the width of the trenches goes from $10\ \mu m$, as in the previous case, at the base, while it's decreased down to $5\ \mu m$ as the shaft becomes narrower. It should be noted that the Critical Dimension (CD) of the fabrication process used for the production of the probes is $1\ \mu m$.

In this way, we did not only showed the versatility of the proposed design, but also introduced a first step towards the possibility of multi-sensing, i.e. the ability of combining multiple signals for an increased accuracy [62].



(a) Platinum Layer for Multiple Electrodes



(b) Trenches between Platinum Regions in Multiple Electrodes Case

Figure 2.6: (a) Similar to the previous case, platinum layer covers the shanks, this time on the right one four regions can be identified, separated by trenches (b) Each trench has a minimum width of $5\ \mu\text{m}$; this reduction is necessary to be able to accommodate all of them on the narrow shank.

2.1.5. Top Insulation Layer

As anticipated the top layer not only insulates the fabricated probes from the environment, but it also defines the final geometry of the electrodes present on them. This approach allows to experiment with sizes and shapes of these, without the need to modify the design of the underlying layers. This reason, combined with the fact that each wafer holds more than 100 samples, brought to the decision of fabricating multiple designs, each with a different scope.

In general, as anticipated, three electrodes have to be designed: WE, RE, CE. Working electrode is the surface on which the reaction we're interested to detect is supposed to occur, while the counter electrode balances the current flow. At the same time a reference electrode is used to set a known value of potential for an accurate measurement [61]; details are provided in section 3.3.1.

Standard Design

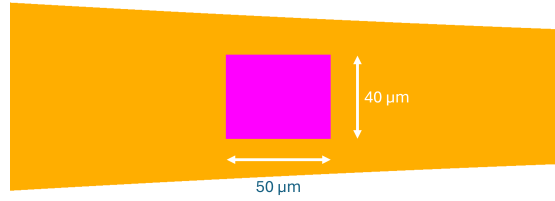
First of all, to perform comparative evaluations on the performances guaranteed by each variant of the design, a sort of standard has been defined. This is constituted by a probe in which no parameter has been brought to the extreme of the technology and reasonable

sizes has been used, so to minimize risk of failures during the fabrication.

WE and RE are both squares of $50 \times 40 \mu m^2$, these areas are easily obtained by the fabrication process used, which has a critical dimension (CD) of $1 \mu m$ [63, 64], while also being sufficiently small to be placed along the shank, at an adequate distance from their edges. Since, as a general rule [61], WE and RE should be as close as possible, they have been placed on the same shank. CE, instead, is a $40 \times 500 \mu m^2$. Thus, its area is 10 times larger than that of the other electrodes; this was done to avoid counter electrode saturation phenomena. The elongated shape is a constriction given by its positioning on the shank. At the base of the shanks, in the regions anchored to the central *Si* chip, three pads, once per electrode, are also exposed. These are necessary to perform electrical and electrochemical testing on the probes after their fabrication.



(a) Standard Design of Foldable Probes



(b) Working Electrode of the Standard Design

Figure 2.7: (a) The design used as a standard for the produced foldable probes is depicted. $20'000 \mu m^2$ CE can be observed on the shank on the left, while $2000 \mu m^2$ WE and RE are on the other. (b) Each trench has a minimum width of $5 \mu m$, this reduction is necessary to be able to accommodate all of them on the narrow shank.

Multiple Working Electrodes Design

Exploiting the *Pt* structures that can be seen in fig. 2.6, three WE are designed on the shank that allocates also the reference electrode. The dimensions considered are exactly the same of the standard design, since in this case the aim was to present the possibility of performing multi-sensing with the proposed device, so no additional change in the parameters was required. In addition, this design could be used to verify and quantify the benefit of modifying the distance between working and reference electrode, at such small scale.



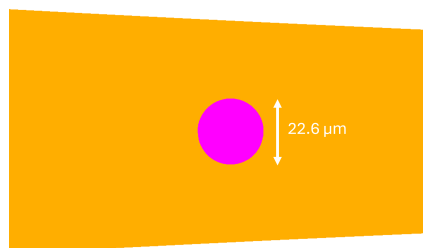
Figure 2.8: Three different working electrodes are present on the shank on the right, at an increasing distance from the reference one. In particular the closest is at about $100\ \mu m$ from RE, the one in the middle at $250\ \mu m$ and the furthest at $500\ \mu m$.

Small Electrodes Design

Ideally, to have deeper detection into the brain tissue, WE should be placed as close as possible to the tip of the shank. To do so miniaturization of the three electrodes is proposed, in particular, in this case, WE and RE have an area of about $400\ \mu m^2$ while the CE one is $4000\ \mu m^2$ wide. To avoid having to re-design also *Pt* layer underneath, positioning of the electrodes has remained unchanged with respect to the one present on the standard design, but the proposed areas would allow to place the WE at the tip of the device, so to guarantee detection at maximum depth. Finally, the shape of the electrodes have been changed, from square to circles, due to manufacturing reasons. In fact, the layer will be patterned by photolithography, a technique that exploits a photosensitive polymer as mask for the etching of the material underneath; details about the process are discussed in section 2.2.4. It is usually advised to avoid the presence of holes with sharp angles in the feature, since the polymer may accumulate in their proximity, resulting in a poor fidelity of the final trench with respect to the design. In the previous case, the area of the electrodes was large enough that, even in case of polymer accumulation, the reduction of the area resulting by it would be negligible. In addition, for the same area, rectangular shape allows to place the electrodes closer to the shank tip. With miniaturization instead, the balance between the two problems swaps, so circular areas have been selected.



(a) Small Electrodes Design Foldable Probes



(b) Working Electrode of the Small Electrodes Design

Figure 2.9: (a) In this case WE and RE are $400 \mu m^2$ circles, while CE is a $4000 \mu m^2$ one. (b) WE is depicted, the radius of about $22.6 \mu m$

Design for Functionalization

As stated in section 1.2.2 dopamine has been selected as molecule to detect, both due to it's medical relevance and since it does not require any functionalization of the electrodes to be sensed. It is then the perfect candidate to asses the functioning of electrodes fabricated following this novel procedure. At the same time, it would be optimal to demonstrate the possibility of detecting other relevant molecules with the same device; these, on the contrary, may require functionalization of the electrode surface, to be measured. The standard design proposed, due to the significant miniaturization employed on it, does now allow a practical manual functionalization of the working electrode. So a design in which much larger working and counter are exploited, is proposed. In this case the WE area is $20'000 \mu m$ large and covers the whole tip of the shank. The area of the RE and its position are the same of the standard one, so that, even if on the same shank, functionalizing the WE without affecting the reference one is a viable option. Finally, the area of the CE is increased up to $110'000 \mu m^2$, so to keep it larger than the working electrode one, and it now covers almost the whole shank.



Figure 2.10: Design of Foldable Probes for Functionalization, in which a $20'000 \mu m^2$ WE covers the tip of the right shank. While on the one on the left a very large, $110'000 \mu m^2$, counter electrode is placed.

2.2. Front-side Fabrication

Having discussed about the electrodes design, it is time to consider their actual fabrication. In particular we'll now focus on the processing of the front side, in which the functional parts and most of the structural components of the probes will be defined and produced.

2.2.1. Substrate Choice

The chosen substrate was a *Si/100mm/DSP/1-10/TTV2* Wafer [65] produced by *Ultrasil LLC*. The $100mm$ diameter was selected due to its high compatibility with most of the machines present in CMi and for being a common standard for research purposes [66]. One of the parameters of this specific substrate that was of most relevance for the scope of the project, and ultimately led to the choice, was the thickness of $380 \pm 10 \mu m$, in fact, this is the smallest value among the ready-to-use substrates present in CMi[67]. This is crucial since in a subsequent step, see section 2.3.1, the wafer is grinded to further reduce its thickness; thus choosing a small initial value reduce *Si* waste.



Figure 2.11: $100mm$ *Si* wafers, with various layers deposited on top, CMi homepage [68]

2.2.2. RCA and Wet Oxide Deposition

RCA Cleaning

After choosing the substrate, the first step required is its preparation for the scope of the

project, in particular this is composed of two steps: RCA cleaning and wet oxidation of the substrate; both are a service offered by CMI staff.

RCA is a standard cleaning procedure developed by W. Kern et al. in 1970 [69], aimed to removal of organic and metallic particles that may be present on Si substrates surface. In CMI is carried out on the Plade RCA wet bench, according to the following procedure:

1. RCA 1 for organic residuals removal, in a $H_2O : NH_4OH : H_2O_2$ (5 : 1 : 1) solution for 15 *min* at 25°C [NH_4OH : Ammonia 28%, H_2O_2 : Hydrogen peroxide 30%]
2. Rinse 1 min
3. Removal of SiO_2 generated during RCA 1 through an $HF : H_2O$ (1 : 10) solution for 15 *s* at 20°C (This step is optional and can be skipped for blanket silicon wafers with oxide on it) [HF : Hydrofluoric acid 49%]
4. Rinse 1 min
5. RCA 2 for metallic elements removal, in a $H_2O : HCl : H_2O_2$ (6 : 1 : 1) solution for 15 *min* at 75°C [HCl : Hydrochloric acid 37%, H_2O_2 : Hydrogen peroxide 30%]
6. Full rinse for 15 *min* with the Fast Fill Rinse (FFR) bath and the Trickle Tank (TT) bath
7. Drying of the wafers with the Spin Rinse and Dry (SRD) system [69].

Wet Oxidation

After RCA cleaning the wafers are placed in furnaces (*Centrotherm International AG, Germany*) so that thermal growth of 200 *nm* of SiO_2 can be performed. This layer is useful to our scope since it acts as an insulator between *Si* substrate and the layer that will be deposited in the next steps.

There are two main techniques for thermal growth of SiO_2 : dry and wet oxidation [70]. Dry oxidation is performed in a pure O_2 atmosphere, in a temperature range between 200°C and 1050°C and it's aimed on production of thin layers with an high control of thickness. For thicker layers (≥ 200 *nm*) wet oxidation is typically used, performed in a O_2/H_2 atmosphere in the same temperature range of dry oxidation. It is used to obtain thicker layers at a much higher growth rate [70]. A comparison between growth rate can be observed in fig. 2.12.

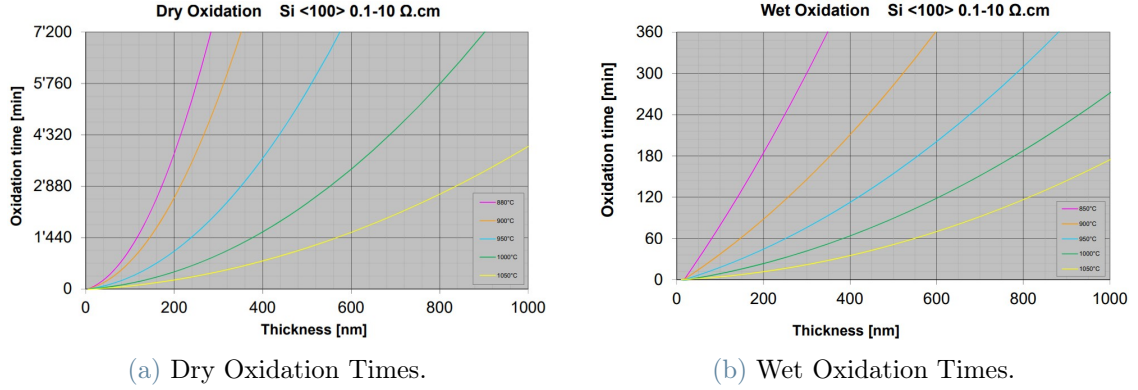


Figure 2.12: Growth time with respect to thickness can be observed at different temperatures, both for (a) dry oxide process and (b) wet oxide one. Taken from [71].

For our specific needs a precise control of the thickness is not required, for this reason the cheaper and faster wet oxide technique has been selected. RCA cleaning and SiO_2 growth are performed on both sides of the wafer, the final result can be schematically seen in figure fig. 2.13.



Figure 2.13: Si wafer section, SiO_2 present on both sides

2.2.3. Aluminum Layer

After substrate preparation the very next step consist in the deposition of a thick Al layer that constitute the structural material used for the bendable shanks previously described. In particular the metal layer is composed of: 10 nm of Ti , used as adhesion layer between the dielectric substrate and the metal, and 4 μm of Al . This specific thickness has been chosen since it provides an adequate structural support without preventing bending of the shanks [58].

Deposition of both materials is performed by sputtering through *Spider 600* (*Pfeiffer Vacuum, Germany*), a cluster tool able to deposit metallic and dielectric materials on wafers by RF, DC or pulsed DC sputtering. Sputtering has been chosen with respect to

other techniques, such as evaporation, due to the higher thickness that can be obtained through it, *LAB 600H* (*Bühler Leybold Optics, Germany*), for example, is able to deposit *Al* up to a maximum thickness of $2.5 \mu m$ [72].

Spider 600 is equipped with four Process Modules (PM) and a loadlock, connected to each other through transfer module; each PM it's equipped with a planar $200 mm$ target. Thanks to this configuration it's possible to deposit up to four different materials without exposing the sample to the atmosphere. The tool is equipped with a substrate holder able to heat up, so that depositions can be carried out in a range of temperature that goes between room temperature and $350^\circ C$, at a pressure $< 5.10 - 7 mbar$ [73]. *Ti* sputtering can be performed in PM1, while *Al* has to be deposited in PM4, both processes are carried out at room temperature, the details on their parameters are listed in table 2.1.

Material	PM	Target	Recipe	Source	Power [W]	Ar [sccm]	Dep. Rate [nm/min]	Ramp [s]
Ti	1	Ti_r	Ti(1)-#	RF	1000	15.0	84.8	5
Al	4	Al (AlSi)	Al-#	DC Maris	1000	15.0	198.0	5

Table 2.1: Titanium and Aluminum spider 600 process parameters [73]

To achieve the desired thickness it is required to compute the time of deposition. Since in *Spider 600* there is no shutter between substrate and target, the ramp up time to achieve nominal value of power has to be considered, thus the following procedure has to be followed [74]:

1. Computation of the deposited thickness during ramp time, according to

$$Thickness_{ramp} = \frac{t_{ramp}}{2} \cdot dep.rate$$

2. Deposited thickness during ramp up is subtracted to the final wanted thickness

$$Thickness_{remaining} = Thickness_{total} - Thickness_{ramp}$$

3. The remaining time is calculated through

$$t_{remaining} = \frac{Thickness_{remaining}}{dep.rate}$$

4. So the final time is given by

$$t_{total} = t_{ramp} + t_{remaining}$$

In our case we can apply the following procedure for *Ti* layer, according to data in table 2.1, obtaining:

$$t_{Ti} \approx 10 \text{ s}$$

It is important to note that the minimum unit of time accepted by the tool software is 1 s. While for *Al* deposition we have $Thickness_{ramp} \ll Thickness_{total}$ so it's safe to neglect the ramp up time and simply consider $t_{Al} = \frac{Thickness_{total}}{dep.rate}$, thus obtaining:

$$t_{Al} = 20 \text{ min} + 12 \text{ s}$$

One last consideration to make before proceeding to the next fabrication step is about the necessity of using dummy wafers to clean the targets before proceeding with deposition on the sample. In fact it is important to note that during handling and substitution of target, they are exposed to the atmosphere, so thin oxide films can form on their surface. Target cleaning recipes allow to sputter and deposit those oxides on dummies, without contaminating the processed wafer[73]. A section of the wafer after this step is schematically depicted in fig. 2.14, note that *Ti* layer has been neglected for simplicity reasons.

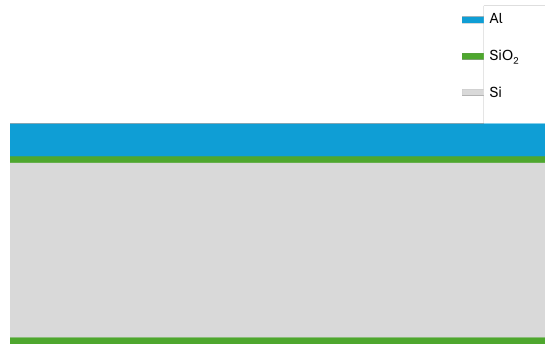


Figure 2.14: Wafer cross section after *Ti* and *Al* deposition

2.2.4. First Photolithography

Once the *Al* structural layer has been deposited, the very next step before etching the metal is to pattern the wanted design on top of the wafer surface; this can be achieved through photolithography. It is worth to explain some of the basics behind this technique

before proceeding further. Photolithography is a sequence of processing steps that allows the deposition and patterning of a photosensitive layer, typically a polymer, called photoresist (PR) [75]. Photolithography is composed of three main steps: coating, exposure and development.

Coating

First of all, before PR application, it's a good practice to obtain optimal results to clean the wafer surface. The cleaning methods are many[75] and they can be more aggressive ones: as RCA, seen in section 2.2.2, or Piranha solution based cleaning, a mixture of sulfuric acid, hydrogen peroxide and deionized (DI) water. The use of such aggressive methods has to be evaluated case by case, since it strongly depends on the possible contaminants present on the surface and on their compatibility with the materials present on it. In the most typical case, such as ours, in which surface has simply to be cleaned by dust particles that, despite the clean-room controlled environment, may be accumulated on the surface, the most used method are: blowing the surface using a nitrogen gun or, eventually, using a standard Acetone/IPA/DI water cleaning procedure. This last one is standard procedure to remove organic residuals, such as the ones coming from a previous photolithographic steps, without risking to damage the substrate. It consists in the wafer dipping in acetone, to dissolve organic compounds, followed by a rinsing with isopropanol (IPA); finally DI water rinse is used to remove possible ionic species [75].

Once the surface is adequately cleaned it is recommended to improve its adhesion with the polymer that has to be applied on it, to do so there are three main techniques: dehydration, HMDS application and O_2 plasma treatment.

- **Dehydration** simply consists in the removal of moisture present on the surface through heating, typically performed between 130°C and 160°C for a few minutes.
- **HMDS** consists in the application of hexamethyldisilazane, $[(CH_3)_3Si]_2NH$, that is a standard in the industry [75]. The substrate is heated between 130°C and 150°C and HMDS is introduced in a sealed chamber at gas phase. The reaction can be seen in fig. 2.15.
- **O_2 plasma** can be used as an alternative method to both clean and treat the surface, since it is able to remove efficiently PR present on the surface and also the humidity on it. The main drawback is the high hydrophilicity of the surface after such treatment, so coating has to be done without any further delay.

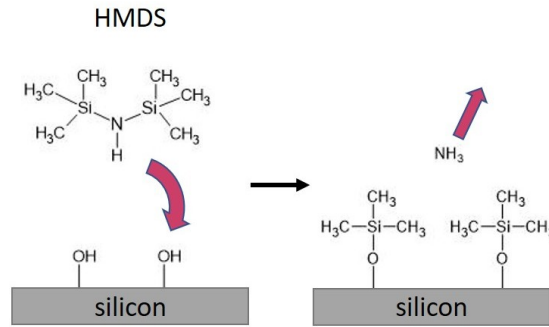


Figure 2.15: HMDS reaction in contact with Si substrate, taken from [75]

The selection of the appropriate treatment is related to the substrate material, in some cases to the underlying layers, and to the chosen PR. Typically metal layers are treated with dehydration, while with semiconductors and dielectrics HMDS is used. In table 2.2 we can see suggested treatments for *AZ ECI 3000* (Merck KGaA, Germany) an high resolution positive PR, depending on the substrate.

Substrate	Vapor HMDS	O ₂ Plasma	Dehydration
<i>Si</i>	✓✓	✓	✓
<i>SiO₂</i> , Fused silica, <i>SiN</i> , <i>Si₃N₄</i>	✓✓	✓	✓
Float glass, Pyrex	✓	✓✓	✓
<i>Al</i> , <i>Au</i> , <i>Pt</i> , <i>Ti</i>	...	✓	✓✓
<i>Ag</i> , <i>Cu</i> , <i>Cr</i> , <i>Fe</i>	...	×	✓✓
GaN, GaAs	...	×	✓✓

Table 2.2: *AZ ECI 3000* suggested surface treatment based on substrate material; Legend: ✓✓ Strongly recommended, ✓ Alternative process, ... Not effective, × detrimental [64]

Once the surface has been properly treated, PR coating can be finally performed, this is done usually by spincoating, in which a small amount of PR is deposited on top of the substrate, that is then rotated at high speed so to spread the polymer uniformly onto the flat wafer. This procedure can be performed both on automatic equipment, e.g. *ACS 200 Gen3*, (*SUSS MicroTec SE*, germany), and on manual one, e.g. *SM-200*, (*Sawatec AG*, Switzerland). There are many parameters that can be controlled during this process and their combination will determine the final thickness and uniformity of the PR. The primary one is the speed of rotation of the wafer, typically it goes from 500 *RPM* to 1000 *RPM* in the first seconds of spinning, so to guarantee a uniform spreading of PR, then it can be incremented up to 6000 *RPM* to determine the final thickness.

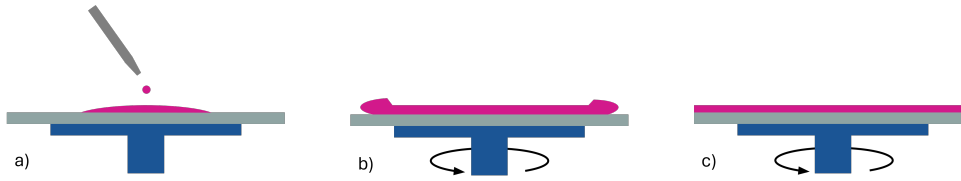


Figure 2.16: Spin coating steps: a) PR is dropped on top of the wafer, b) Wafer is gradually put in rotation to spread the PR, c) rotation reaches the nominal speed so that final thickness is reached.

Usually the so called spin-curves are provided with PR datasheets, so to determine the correct rotation speed to use to obtain the desired thickness, an example for *AZ ECI 3007* can be seen in fig. 2.17.

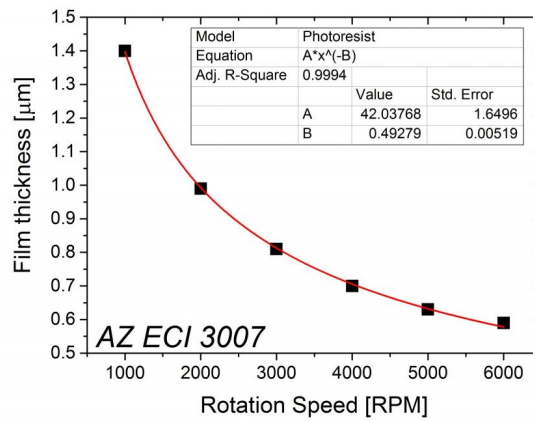


Figure 2.17: *AZ ECI 3007* spin curve, taken from [64]

Another relevant parameter that determine the final result are the type of dispense, that can be static or dynamic, with the wafer in rotation before PR pouring. In addition, automatic tools often offers the possibility of including sequences of: Back Side Rinse (BSR), Edge Clean (EC) or Edge Bead Removal (EBR), that are described in figure fig. 2.18.

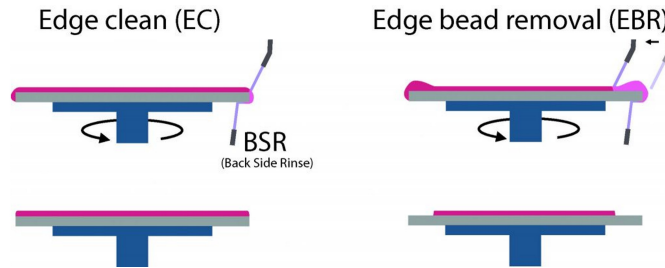


Figure 2.18: Schematic representation of EC procedure (on the left) and of EBR (on the right) in both cases BSR is performed. [75]

After the coating has been performed, many PR require a soft bake step, in which the substrate is heated for a few minutes in a temperature range that typically goes from 90°C to 120°C . This is done to remove the excess of solvent present in the liquid PR, that is usually in a range of 20 – 40%, by weight, bringing this values down to 3 – 8%; effectively stabilizing the polymer on the wafer surface.

Exposure

Exposure is the key step of photolithography, since it's the one in which the designed pattern is imprinted on the PR. To achieve this, the polymer is irradiated with UV light, triggering a series of chemical reactions that make it soluble, or insoluble, in an aqueous solution. There are two macro-categories of techniques that can be used to achieve this: mask based technologies and mask-less ones. The first ones require production of a mask, that has to be aligned with the processing wafer, so that light is blocked to reach regions that one does not desire to be exposed by it. This technique is usually preferred for high volumes production, since, once the mask has been produced, guarantees reliable and repeatable results. In the case of interest, designs are often changed and reworked, so producing a mask each time is detrimental in term of time and resources, thus direct laser writing, a common mask-less exposure technique, has been selected. In the following paragraph principles behind this technology will be unfolded. All photolithographic steps have been performed on *MLA 150 (Heidelberg Instruments, Germany)*, therefore it will be used as reference to explain the key elements of direct laser writing.

Once the wafer is placed on the holder of the tool an evaluation of the rotation of the wafer with respect to it has to be performed, in fact for a satisfactory first photolithography PR has to be exposed as intended on the design. A first preliminary alignment of the substrate is done by manual positioning of it, exploiting the main flat of the wafer, as the one that can be observed on wafers in fig. 2.11. A more refined evaluation of such rotation is then performed by the tool itself, that detects substrate thickness and edges thanks to a pneumatic focus system. A flow of N_2 coming from the write head hits the

sample and it's reflected toward a pressure sensor, this mechanisms is used to focus the laser at the correct working distance, then the write head moves to detect edges of the wafer, computing its position and rotation on the substrate [76].

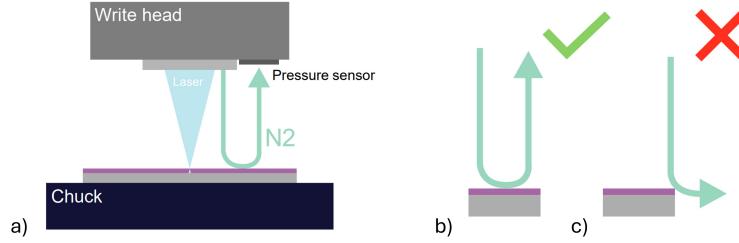


Figure 2.19: a) Automatic focusing mechanism of *MLA 150*, b) N_2 flow behaviour on wafer surface c) N_2 flow on wafer edges [76].

Once focusing is completed one should set the exposure parameters, that in *MLA 150* are: laser wavelength, dose and defocus. The wavelengths available on *MLA 150* are 375 nm and 405 nm , the latter is the one suggested for most of PRs, in addition to it one should also set laser dose, measured in mJ/cm^2 , that strongly depends on the selected PR and its thickness. Another important parameter is defocus, that defines the height of the PR at which the focus is done; it range from -10 and $+10$, it is important to note that a positive defocus will shift downwards into the PR [63], as depicted in fig. 2.20.

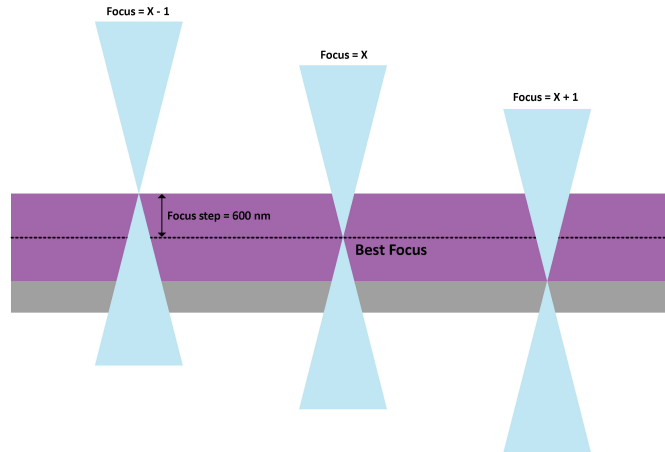


Figure 2.20: Focus of *MLA 150* depending on the set defocus value [63].

Typically defocus and dose parameters are listed in tables that group different kinds of PR, each with many typical thicknesses, so one could simply use the reported values. Nonetheless there are many cases in which one might want to obtain different values with respect to what is listed, some examples are: PR used is not listed, absence of parameters

for the thickness of interest or presence of materials underneath PR that may affect laser reflection on the surface. To solve this issue there are two routes, the first one is performing a simple interpolation of values, to obtain a linear relation between thickness, dose and defocus, that should provide reasonable values for thickness of interest. This approach is quick, but it only applies in cases in which some data for the PR used are present and even in those cases it may not always be reliable. The safest method, in fact, would be to perform the so called: dose tests. In them PR is exposed so that a series of patterns are produced on the wafer, each one represent a specific combination of dose and defocus. Then these patterns can be visually checked to determine the best combination of parameters to use in the case of interest.

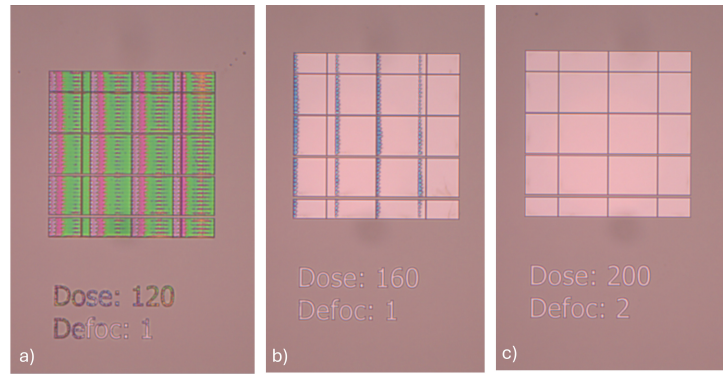


Figure 2.21: Dose test examples, performed on 4 μm of AZ 10XT. a) Severe underexposure, the pattern is barely visible. b) Underexposure, the pattern is more clear, but there are still some residues of PR. c) Perfect pattern reproduction, optimal parameters.

Before proceeding to the next step of photolithography we should discuss about the two main families of photoresists: positive tone PRs and negative tone ones. Positive PRs becomes more solubles in the areas irradiated by UV light, so after development only unexposed areas of the pattern are left. Negative PRs, instead, undergo photo-induced cross-linking, making exposed parts more resistant to dissolution into developer. So in this case only the exposed pattern is left at the end of the process.

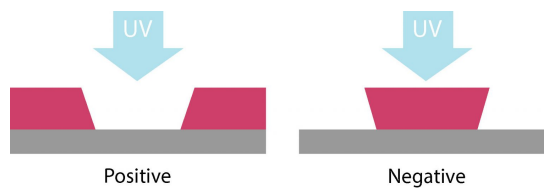


Figure 2.22: Positive (on the right) and negative (on the left) photoresists basic functioning principle [75].

Development

As hinted in previous paragraphs, the final step of photolithography is PR development, in which the polymer interacts with a solvent, usually aqueous based, that dissolves the exposed areas of the resist (or the unexposed ones in case of negative tone PR). This can be done both manually, by pouring a certain amount of developer into a glass beaker and then dipping the wafer into it, then typically the sample is left into the solvent for some minutes and finally it's rinsed with DI water. Alternatively, standard wafers, as the 10cm ones used on this process, can be developed in automatic tools as *ACS 200 Gen3*, (*SUSS MicroTec SE, Germany*). In this case two techniques, or a combination of the two, can be used, depending on PR thickness and viscosity: Spray and Puddle. In the first case the wafer is put in rotation and developer is sprayed onto it, in the second the sample is static and the developer is spread all over the surface [75]. Both manual and automatic developments can be repeated up to three times in case of unsatisfactory results, any more than that is typically related to underexposure problems.

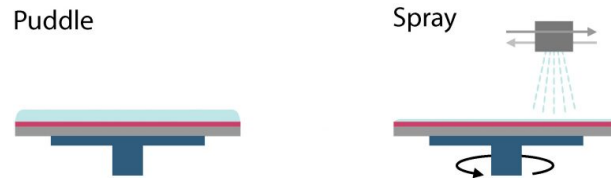


Figure 2.23: Automatic development techniques, puddle method (on the left) and spray method (on the right) [75].

First Photolithography

Now that the theory behind photolithography has been reviewed we can discuss about the steps that our sample has gone through. Before applying the photoresist, simply blowing *Al* surface with N_2 gun is sufficient to remove dust that may have been accumulated on it. No contamination with organic materials should be present at this point, nonetheless if one suspect it, a standard *Acetone/IPA/DI Water* cleaning can be performed. Since the subsequent step is the *Al* plasma etching, *AZ ECI 3027*, a positive tone PR able to achieve a critical dimension (CD) of $1\ \mu m$ has been selected[77]. Automatic coating will be performed by *ACS 200 Gen3*, (*SUSS MicroTec SE, Germany*), so a $4.21\ \mu m$ thickness has been chosen from the ones available on the tool, this PR height guarantees protection of the sample throughout the whole etching process [64]. As seen in table 2.2, dehydration is the recommended surface treatment for metal substrate, thus it is been included in the recipe on *ACS 200*; softbake is also included at the end of of the process. Alternatively coating can be performed manually on *SM-200*, (*Sawatec AG, Switzerland*), exploiting spin curves, as in fig. 2.17. In this case both dehydration and softbake have to

be performed on hot plates, according to the following parameters:

- Dehydration: 10 *min* at 135°C [78]
- Softbake: 90°C for $t = 30\text{ s} + 30\frac{\text{s}}{\mu\text{m}} \cdot \text{thickness}$ [64], so given $\text{thickness} = 4.2\text{ }\mu\text{m}$,
t = 2 min + 36 s

Once PR coating has been completed the wafer is positioned in an anti-static black wafer carrier, to avoid accidental exposure during transport. The resist is then exposed, thanks to *MLA 150* (*Heidelberg Instruments, Germany*). Laser wavelength used is 405 *nm*, while dose and defocus should be determined based on the most updated tables present on the tool, the exact values are related to internal parameters of the tool and may change after maintenance, here some indicative values are reported:

Dose = 320 $\frac{\text{mJ}}{\text{cm}^2}$ [64], **Defocus = +3.**

It is important to note that *AZ ECI 3027* is a positive PR, so the negative of the designed structure has to be exposed, e.g. for the shanks one can look at fig. 2.24

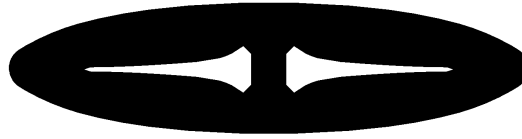


Figure 2.24: Design that have to be exposed to obtain the wanted *Al* shanks, the black region is the one irradiated by UV light.

Once exposure is completed, before proceeding with development, post exposure bake (PEB) is required, due to the fact that *AZ ECI 3027* is a chemically amplified resist. Since development will be done using, once again, *ACS 200*, PEB can be included in the recipe of the tool. Alternatively, if manual development is preferred, the bake is done on hot plates. In case of 4.2 μm of PR the parameters are the following: **90 s** at **110°C** [64]. The results of this photolithographic process are schematically shown in fig. 2.25:

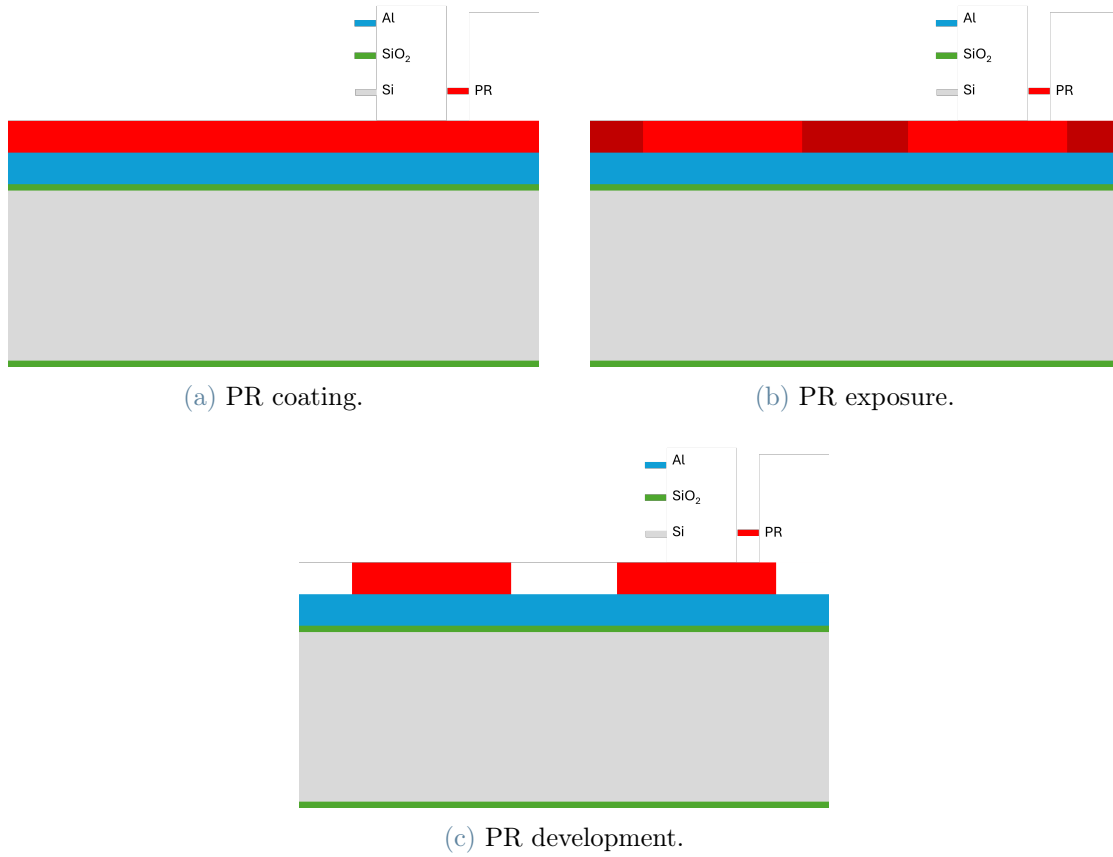


Figure 2.25: The three main stages of photolithography can be seen: (a) coating, (b) exposure, (c) development.

Descum

Before performing etching, to obtain optimal results, it is recommended to perform descum with O_2 plasma, to remove any residue of PR that may be present in trenches and holes. This has to be done even if visual inspection does not reveal any issue, in fact usually this residuals may not be visible with an optic microscope. If they're not removed, etching uniformity can be significantly affected by them. Descum will be performed by *GiGAbatch* (*PVA TePla, Germany*) an O_2 plasma asher able to work both at high power (600 W) and low power (200 W), respectively for PR stripping and descum [79].

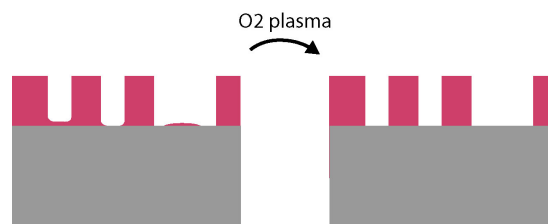


Figure 2.26: Wafer cross section before and after O_2 descum [79].

2.2.5. Aluminum Etching

Having imprinted the designed pattern on the PR, it is now necessary to transfer it onto the metal layer underneath. To do so, an etching step has to be performed. Once again, before discussing the case of interest, it is worth giving a brief introduction to the main etching techniques.

Wet and Dry Etching

First of all let's give a definition of etching: a microfabrication process during which one or more layers of materials are removed [80]. Etching techniques can be divided into two macro-categories: wet etching and dry etching.

When performing wet etching the sample is simply submerged in a liquid etchant and the dissolution of the layer of interest occurs due to chemical reaction with it. The main advantages of this technique are its simplicity and the high selectivity with the etched material, while the drawback is the isotropicity of the process. The typical under-etching that occurs with this method can be observed in fig. 2.27.

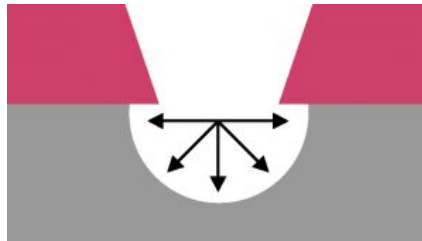


Figure 2.27: Due to isotropic behaviour of wet etching, the material is dissolved also underneath the protective layer, this phenomenon is called under-etching [77].

Dry etching instead use ions, gas or plasma to achieve the same result. Let's consider advantages and disadvantages of each one:

- **Ion Beam Etching:** In this case ions are accelerated toward the sample surface, the impact force is high enough to physically etch the exposed materials. This technique is also referred to as sputtering and can etch any material anisotropically. The main problems are related to the poor selectivity of the process and to redeposition, as it will be discussed in details in section 2.2.8.
- **Gas etching:** Similarly to wet etching, this technique is based on a reactive etchant, that in this case is a gas. Being strictly based on reactivity of the substrate with the introduced gas is highly selective, but once again is isotropic.

- **Plasma Etching:** In this case a reactive plasma is used as etchant, exploiting both physical and chemical etching. It's also referred to as Reactive Ion Etching (RIE) and it offers both high selectivity on materials and good anisotropic behaviour. The main downside lies in the complexity of the equipment needed to perform it [80].

Al Etching

The process in exam require the etching of a considerably thick layer of *Al*, 4 μm , so to perform it plasma etching has been chosen. In particular *PlasmaPro100 Cobra (Oxford Instruments, United Kingdom)* has been selected as an etching tool, since its primary target are *Al* and *Ti* alloys, whose removal can be achieved through chlorine based recipes. Another important advantage of this machine is its double End-Point-Detection (EPD) system. In fact it is equipped with both a laser interferometry/reflectometry EPD and a Optical Emission Spectroscopy (OES) one.

Let's briefly discuss about their functioning and advantages:

- **Optical Emission Spectroscopy** Technique that exploits characteristic optical emission that occurs during chemical reactions between etchant and target. In most cases one can exploit it simply considering the overall intensity of light present in the processing chamber. In fact, during etching, the light intensity level generated by the chemical reaction will sum up with the one of the plasma itself; so, when this level drops back to the base plasma one, the target material has been competently etched. Moreover, if one knows the characteristic wavelength of emission of the reaction, discretizing the plasma spectrum can give precise informations about byproducts presence over time.
- **Laser Interferometry/Reflectometry** OES gives global informations about the ongoing process; if one instead would like to know the etching state in a specific point of the sample, laser based EPD can be used. In it a laser beam incides orthogonally to the sample surface and is reflected back to the system; it can be based both on interferometry and on reflectometry. The first technique is used for transparent layers, since it exploits the fact that the beam is partially reflected by the top surface and partially by the interface with the layer underneath. Both reflected beams superimpose on the detector, their constructive or destructive interference generate a sinusoidal signal. The period of the sinusoid indicates also the etch rate, the shorter the period, the higher is the rate. If instead the material is not transparent to the laser a flat signal, given by a single reflection, will be present. In both cases the end of the etching can be detected due to the sudden variation in the signal, i.e. a change of reflection intensity, a flattening of the sinusoid or a change

in its periodicity [81].

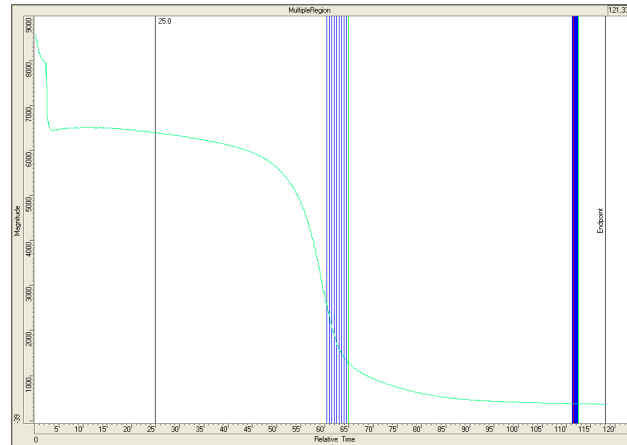


Figure 2.28: Optical Emission Spectrum of an O_2 cleaning recipe performed on *APS* (*STPS Technologies, United Kingdom*). At about 60 s a drop in light intensity is detected, the the system declares end-point at 112 s [81].

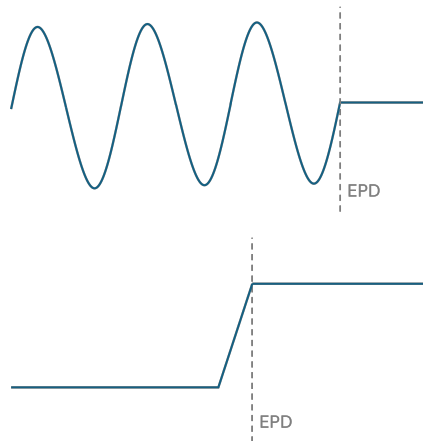


Figure 2.29: Scheme of typical laser EPD plots. Sinusoidal behaviour in case of transparent layers (on the top), flat lines for non transparent ones (on the bottom).

These tools allow the user to check in real time the complete etching of the material of interest, in fact simply computing the time of processing considering the nominal etching rate is often unreliable. This occurs due to many factors: the real thickness of the layer to be etched may not be exactly the nominal one, oxides may be present on the surface, slowing down the process in the initial stages, finally the width and depth of the trenches to be etched strongly affects the actual etching rate.

Let's consider the case of interest: we would like to etch 4 μm of *Al* and 10 *nm* of *Ti*, the recipe selected on *Plasma Cobra 100* is *Al_etch_w_breakthrough*. This is a Cl_2 based

process, with an initial breakthrough performed with BCl_3 to remove Al oxides that may be present on the wafer surface. According to the data in table 2.3 an etch rate of $510 \frac{nm}{min}$ is expected; no data for Ti are present but since the layer is very thin, we expect it to be etched in a few seconds, let's consider an over etch of 30 s to stay safe. Computing the expected time:

$$t_{etch} = \frac{4000}{510} \cdot 60 \text{ s} + 30 \text{ s} = 501 \text{ s} = 8 \text{ min} + 21 \text{ s}$$

Out of three processed wafers, still considering 30s of over etch, the times obtained were between **8min + 16s** and **10min + 5s**. Since the wafers have not been processed at the same time such differences may be related to: slightly different initial thicknesses, oxides accumulation over time of the last wafers processed and recalibration of the tool.

Target Materials	Recipe	Mask	Etching rates [$\frac{nm}{min}$]	Chemicals
Al, Ti, TiN	Al_etch_w_breakthrough	PR	510(Al) 250(Al) 50(SiO_2)	$BCl_3(BT)$ $Cl_2(main)$

Table 2.3: Etching rates on *Plasma Cobra 100* for the recipe of interest:

Al_etch_w_breakthrough [82]

At the end of the process one can expect the cross section of the wafer to be as in fig. 2.30.

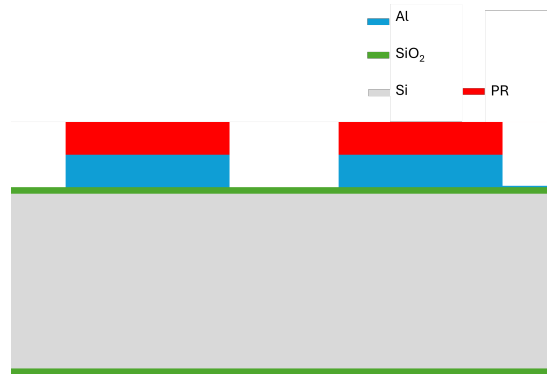


Figure 2.30: Wafer cross section after Al etching has been performed.

A final important consideration is that, since Al is etched by chlorine chemistry, trapped Cl_2 at the sidewalls of the pattern pose a serious corrosion problem for Al . In fact, as soon as it gets in contact with the water present in the atmosphere HCl starts to form. To avoid this issue, as soon as the sample has been processed it should be dipped in an high volume of DI water. This forces the production of HCl , that will be diluted and rinsed

right away, preventing *Al* damaging. A good practice is also to remove the PR right after wafer rinsing, so that any traces of *HCl* that may still be present are eliminated [82].

2.2.6. Photoresist Strip

Stripping is the term that defines all the methods designed to remove photoresist from a sample, this can be done both for rework, due to unsatisfactory photolithography results, or at the end of an etching process. In this second case a standard procedure is suggested:

1. 5 *min* of O_2 plasma at high power by *GIGAbatch (PVA TePla, Germany)*;
2. Wet etching by *SVC-14*, to be performed on UFT wet bench;
3. If necessary, other 5 *min* of O_2 plasma at high power [79].

The first step is required since after harsh processes, as dry etching, the top region of the PR can be burned and hardened, becoming resistant to dissolution in chemical strippers.

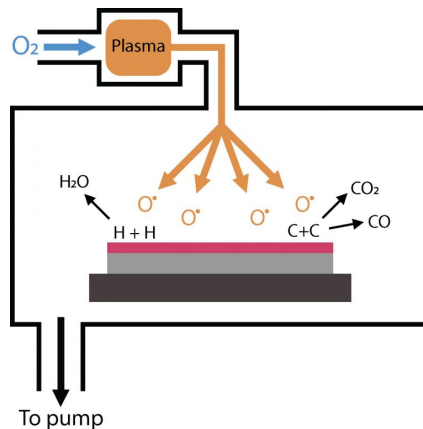


Figure 2.31: Functioning principle of O_2 plasma ashers for organic materials removal. From [75].

Once the hardened layer is removed, chemical etch can be performed, let's now discuss about the procedure that has to be followed for this step. The process is performed in *UFT Resist* wet bench, in which *SVC-14*, a polar solvent for photoresists based on DMSO (C_2H_6OS) [79, 83]. The sample is submerged in a sequence of baths aimed to the removal of the PR and the rinsing of the wafer to eliminate traces of solvent on it. In particular, as shown in fig. 2.32 the following procedure has to be followed:

1. Sample immersion for 5 *min* in *SVC-14* at 70°C in the first bath (3 in fig. 2.32);
2. Second immersion for other 5 *min* in *SVC-14* at 70°C . The second tank (4 in

fig. 2.32) typically has a lower concentration of PR dissolved in the bath, so it is used for fine stripping;

3. Quick Dump Rinser (QDR) bath in DI water, to remove most of the residual of PR and solvent;
4. Cascade bath in DI water, this allows fine rinsing of the sample;
5. Finally the wafer is moved is dried in Spin Rinse and Dry (SRD) unit [84].

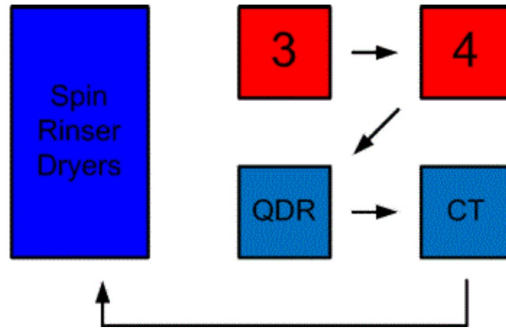


Figure 2.32: Flowchart of *UFT Resist* wet bench, representing the all the steps of chemical PR strip, in the order on which they have to be performed [84].

Eventually, if residuals of PR are still present on the wafer surface, additional O_2 plasma etching can be performed, typically for other 2 – 5 min [79]. An alternative to this procedure is to perform a purely plasma based etching, skipping entirely the use of chemicals. This can be a faster way of stripping PR, but it's also a more aggressive procedure, in fact prolonged exposure to O_2 plasma may oxidize some layers in the sample, so the use is strongly dependent on the substrate materials. At the end of the process the resist is completely removed and the patterned *Al* layer is left as top surface of our sample.

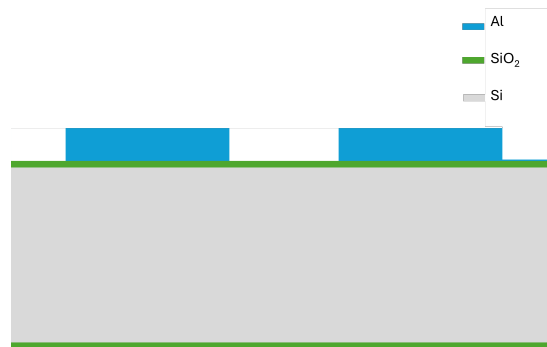


Figure 2.33: After PR stripping patterned *Al* is left as top layer of the wafer.

2.2.7. Silicon Dioxide Deposition

As discussed previously *Al* layer has a purely structural purpose for the shanks of the device, so it has to be insulated from the *Pt* layer that will be deposited afterwards. *SiO₂* has been selected as insulating material due to its renewed bio-compatibility [20] and low permittivity [85]. To deposit the oxide, Plasma Enhanced Chemical Vapor Deposition (PECVD) has been chosen as technique, since it allows to have high deposition rates while also ensuring a good thickness uniformity [66]. This process exploits two or more precursor gases, that are ionized by a plasma, and react with each other to form a thin film on the substrate. Plasma is generated by a Radio Frequency (RF) discharge between two electrodes and it ensures that the reaction occurs at a much lower temperature than a classic Chemical Vapor Deposition (CVD) [86]. The tool selected to perform deposition is *D250L PECVD* (*Corial, France*), used for the deposition of Si based compounds, such as oxides, carbides and nitrides [87]. Since a considerably thick layer (1 μm) of *SiO₂* is required and we do not require any specific parameter *A_SiO2_Fast* recipe was selected between the ones available on the tool (consider table 2.4).

Recipe	Film	Temp. [°C]	Dep. Rate [$\frac{\text{nm}}{\text{min}}$]	Ref. Index at 677nm	Unif. [%]	Stress [MPa]
A_SiO2_Fast	<i>SiO_x</i>	320	405	1.47	0.5	-190
A_SiO2_Fast_LF_150W	<i>SiO_x</i>	320	347.6	1.47	0.9	-346
A_SiO2_Fast_LF_100W	<i>SiO_x</i>	320	358.7	1.47	0.97	-338
A_SiO2_High_Density	<i>SiO_x</i>	320	22.7	1.47	0.5	-318

Table 2.4: Recipes available on *D250L PECVD* for *SiO₂* deposition [87].

Before processing the sample, it is highly suggested to perform chamber conditioning, during which 200 *nm* of the same material that we desire to use are deposited on the heated shuttle; this prevents contamination of the wafer with any other material that may be present due to previous processes. Then the substrate is positioned on the conditioned holder and deposition starts, given the etch rate in table 2.4 coating time is easily computed:

$$t_{dep.} = \frac{thickness}{dep.rate} = \frac{1000}{405} \text{ min} = 2 \text{ min} + 28 \text{ s}$$

The final expected result can be observed in fig. 2.34. After deposition, in-situ plasma cleaning of the shuttle has to be done, i.e. the etching of the material that has been deposited on it during processing. Then the process is automatically stopped by the tool, thanks to an Optical Emission Spectrometer for EPD [86].



Figure 2.34: SiO_2 layer uniformly cover Al shanks of the device.

2.2.8. Platinum Layer

Platinum deposition is one of the most crucial point of the electrodes fabrication, at least for what concerns the front-side processing. In fact Pt will constitute all the electrical components of the probes: the electrodes in contact with environment, the pads for electrical testing and the tracks connecting the two. In addition to this, Pt is mostly inert to chemical etching, so its patterning pose a challenge by itself. Thus in the next paragraphs all the issues related to this material will be addressed, together with the proposed solutions.

Platinum Deposition

Pt layer is deposited by *Spider 600* (Pfeiffer Vacuum, Germany), in particular 10 nm of Ti are used as adhesion layer, before depositing 200 nm of Pt . The tool has been chosen, once again, due to it's ability to deposit different materials in a single run, as discussed in section 2.2.3. Due to the the limited thickness the process could be alternatively performed by evaporation, e.g through *LAB 600H* (Bühler Leybold Optics, Germany), that is able to deposit Pt layers up to 300 nm [72]. It should be noted though, that the deposition rate that can be achieved is much lower: 24 $\frac{\text{nm}}{\text{min}}$ for *LAB 600H* [72] against the 306.8 $\frac{\text{nm}}{\text{min}}$ of *Spider 600*; so the second has been preferred.

Material	PM	Target	Recipe	Source	Power [W]	Ar [sccm]	Dep. Rate [nm/min]	Ramp [s]
Pt	3	Pt	Pt-#	DC Maris	1000	15.0	306.8	5

Table 2.5: Platinum process parameters on *Spider 600* [73]

Considering the parameters in table 2.5 and in table 2.1, one can compute the required times of deposition of Ti and Pt , thanks to the same formulae seen in section 2.2.3. So

we have:

$$t_{\text{Ti}} = 10 \text{ s}$$

$$t_{\text{Pt}} = 42 \text{ s}$$

It should be noted that, since PM 4 is not used for *Pt* deposition, *Ti* could also be deposited using a DC source at high voltage 1000V, this recipe has an higher deposition rate [73], so the time required is slightly smaller: $t_{\text{Ti}(\text{alternative})} = 8 \text{ s}$.

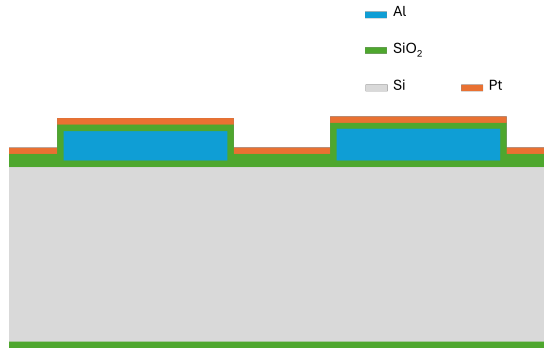


Figure 2.35: 200 nm of *Pt* are deposited on top of *SiO2*

Second Photolithography

Once the platinum has been deposited, photolithography is required to define its pattern, the process is similar to what described in section 2.2.4, but there are some key differences, especially in the exposure, since this new layer must be well aligned with the one underneath. First of all PR coating is performed, the procedure is similar to what has been described for *Al*. The chosen resist has been *AZ 10XT-20* with a thickness of 4 μm , due to its compatibility with high topology [88], as in the case of interest. Coating can be either performed in *ACS 200 Gen3*, (*SUSS MicroTec SE, Germany*), using a recipe with dehydration and high topology settings [89], or manually using *SM-200*, (*Sawatec AG, Switzerland*). In this second case, the steps to follow are:

1. Dehydration on hot plate at 135°C for 10 min [78];
2. Manual coating on *SM200*;
3. Softbake at 105°C for $t = 90 \text{ s} + 20 \cdot \text{thickness} \frac{\text{s}}{\mu\text{m}}$, so in our specific case
 $t = 2 \text{ min} + 50 \text{ s}$

The the sample has to be exposed, this will be once again performed on *MLA 150* (*Heidelberg Instruments, Germany*). Since, as said previously, alignment has to be considered, let's briefly discuss its functioning.

Ideally we would like to have the top layer to be perfectly aligned with the layer underneath, to do so, the positioning of the wafer in the tool and the computation of its rotation described in section 2.2.4 are not enough. In fact even a mismatch of few *mRad* can be extremely detrimental at such small scale; then, a system to manually set the tool to be aligned with the substrate is needed. In particular we would like to have features on the sample surface, that can be easily identified and allow us to visually check mismatch between two different layers, these are called: alignment marks. During the first photolithographic process, together with our design, a first series of alignment marks is exposed on the wafer; these features are positioned at known xy coordinates in the file that is imported in the tool. Once the second PR has to be exposed, the alignment option can be selected on the tool and coordinates of alignment marks of the first layer should be imported. *MLA* will then show, thanks to an high resolution camera, the position of those coordinates according to its internal settings, allowing the user to reset these values according to the actual location of the features. Finally another set of marks will be exposed, so that they should perfectly match the position of the one underneath.

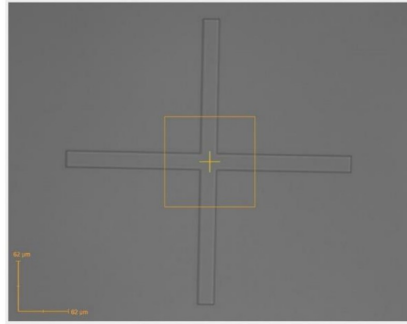


Figure 2.36: Image from high resolution camera of *MLA 150*. The yellow square represent the area inside which the tool is able to automatically detect the center of crosses and squares [76].

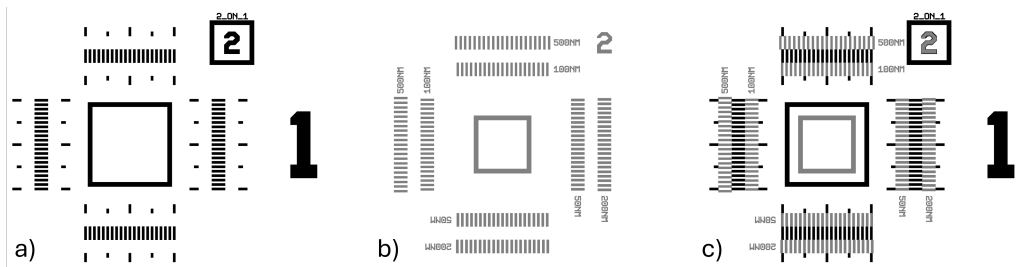


Figure 2.37: 2on1 alignment marks. a) Alignment mark exposed during the first photolithography, b) Alignment mark exposed during the second photolithography, c) At the end a superposition of the two will be obtained.

With this technique it's even possible to decide exactly which layer should be considered as reference for the alignment, e.g. *2on1* indicates alignment of the 2nd layer with the 1st one, *3on1* the 3rd with the 1st, *3on2* the 3rd with the 2nd, and so on.

At the end of photolithographic process, Vernier scale can be used to quantify the offset that is present between the two layers. As shown in fig. 2.38 they consist in two scales with constant pitch, the first one is patterned on the first layer and has a *pitch* = X , while the second is on the second layer and has *pitch* = $X + Y$. If the two layers are perfectly aligned then so will be the central bars of two scales. More realistically some offset will be present and one can quantify it by checking which n^{th} bars are actually aligned [60], then offset can be computed:

$$offset = n \cdot Y$$

Typically the second scale has also a label with its Y value, as can be noticed in fig. 2.37, ideally the offset value should be below the CD of the used PR.

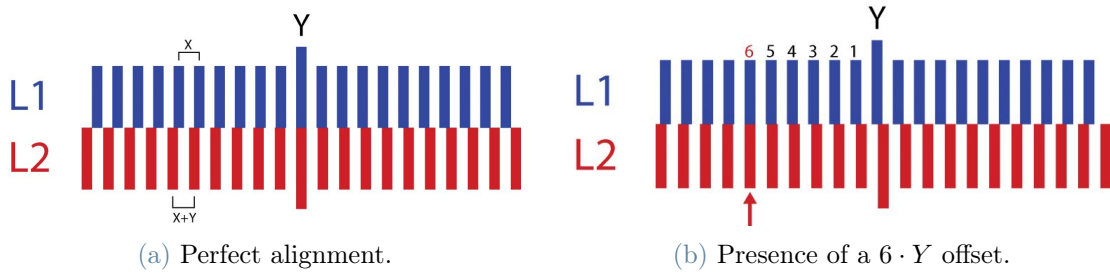


Figure 2.38: Comparison between: (a) perfectly aligned Vernier scales and (b) misaligned scales, it can be seen that an offset of $6 \cdot Y$ is present. [60]

Once exposure has been completed and the alignment has been evaluated as acceptable, PR development can be performed. This can be done both on *ACS 200* or manually submerging the sample in a solution of *AZ 400K* and DI water (1 : 3.5) [89].

Platinum Etching

As said at the beginning of this subsection, *Pt* is highly resistant to chemicals so wet and plasma etching often are not a viable option. In fact the first one has to be excluded apriori, since in CMi it can only be performed by Diluted Aqua Regia solution, i.e. $HCl(37\%) : HNO_3(70\%) : H_2O (3 : 1 : 2)$. This process does not guarantee any reliable etching rate, due to being designed as a stripping solution for the metal; in addition also *Al* layer would be affected, severely damaging our feature [90].

For what concerns plasma etching *Multiplex ICP*, (*Surface Technology Systems, United Kingdom*) provides a recipe for *Pt* etching based on Cl_2 chemistry. however, this process

has an extremely low etching rate of $35 \frac{nm}{min}$ and it requires very thick PR layers, due to the fact that the selectivity with respect to the mask is 1 : 8 [91]. Considering that usually, as a safety rule, PR thickness should be twice the minimum computed one, this would imply a thickness 16 times higher than the metal layer. Even if in our case *Pt* layer is only of 200 nm, so these downside do not represent a significant limitation, the use of such process has been excluded in favor of a purely physical etching, more versatile in term of processable thicknesses.

Nexus IBE350 (Veeco, USA) has been selected for this purpose, a broad-beam ion etcher that exploits accelerated *Ar* ions to etch a wide variety of materials purely by sputtering. The tool is able to operate in large range of voltages, from 50V up to 800V, so that both low ion damage or quick etching can be performed. Chamber contamination is prevented thanks to the high vacuum level in which the tool operates: $10^{-7}mbar$. In addition a Secondary Ions Mass Spectroscopy (SIMS) system provides a precise and real time end point detection capability [92]. This system exploits a different mechanism with respect to the EPD methods seen in section 2.2.5, in fact it determines which species are present in the chamber thanks to the mass-to-charge ratio of secondary ions. These charged species are the one that are sputtered from the surface and they are named secondary since they're not present if no etching is occurring. A mass analyzer detects part of these ions and isolates them according to their mass, so that real time curves for each etched element can be present. As soon as the signal intensity of the etched species drops, the one correspondent to the material underneath should increase, defining the end point of the process [81].

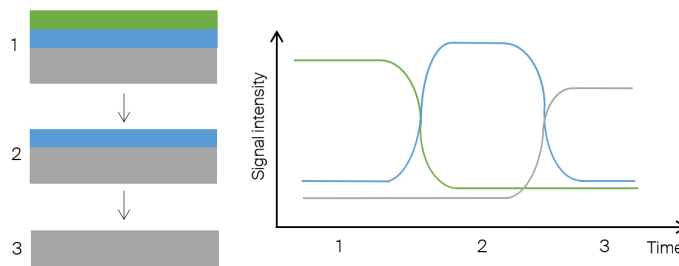


Figure 2.39: Evolution of intensity signals in a SIMS system, depending on the material that is currently etched. 1) Top layer (green) is being etched, so its signal is the most intense, the other two (blue and gray) stay at baseline level. 2,3) Every time etched material changes, previous signal drops, while a new suddenly increases. [76].

To obtain optimal results some precautions should be made to avoid *Pt* redeposition during sputtering. In fact, if steep PR walls are present, a common problem is the

formation of fences of the etched materials, due to it's accumulation on these walls, as depicted in fig. 2.40.

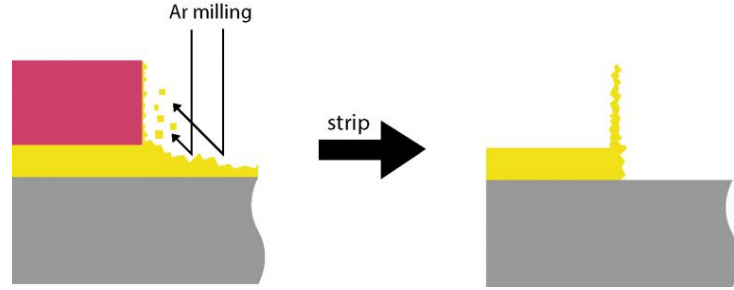


Figure 2.40: Mechanism of formation of fences on the walls of the PR, due to redeposition of the sputtered material in *Nexus IBE350* [77].

To avoid this problem two techniques are used: first of all the ion beam on *IBE350* does not hit the sample surface orthogonally, but the wafer is actually tilted and it's in rotation, so that even if some redeposition occurs it can still be removed by the beam itself. The suggested tilting angle on *IBE* is -10° , but it can be increased up to -70° if necessary; note that the angle is negative due to internal settings on the tool [92].

Tilting it's helpful but usually is not enough, so reflow of the photoresist is strongly suggested. This step consist in the heating of the PR above the softening point, typically is performed at 125°C on a hot plate for about 2 min [93], so that the polymer starts to flow, smoothening its walls. It must be considered that to obtain optimal results the width of PR features, should be at least three times larger than its height.

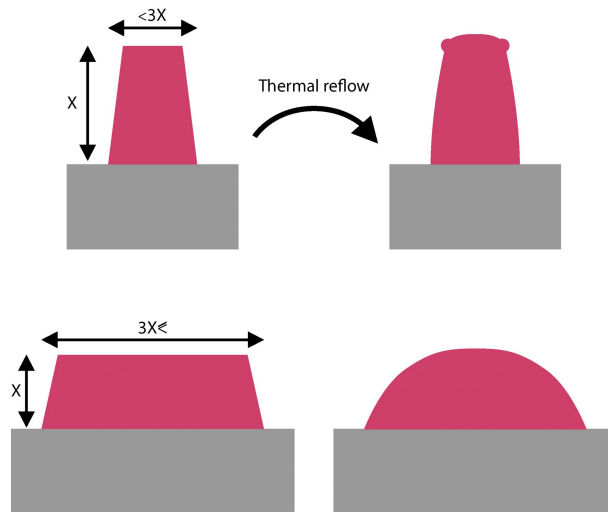


Figure 2.41: Thermal reflow of PR. It can be seen that if the thickness is too small with respect to the hight of the polymer an improper reflow will occur (on the top), while if $height > 3 \cdot thickness$ a rounded shape is obtained [75].

The now smooth and rounded walls of the PR will avoid Pt to redeposit on them and, at the same time, will facilitate its removal in case some redeposition occurs.

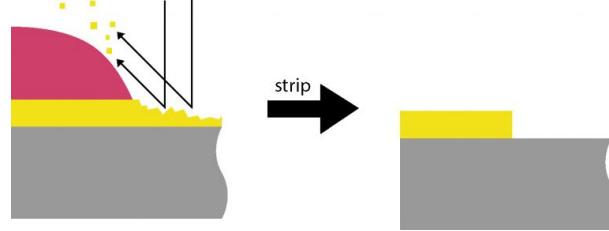


Figure 2.42: Rounded walls avoid Pt accumulation of Pt on PR walls, avoiding fences formation [77].

Photoresist Stripping

After Pt has been completely etched resist can be stripped from the sample surface, this is performed following the standard procedure seen in section 2.2.6, i.e. O_2 plasma, chemical etching based on $DMSO$ and, if required, O_2 plasma once again. At the end of the process the expected results are as in fig. 2.43.

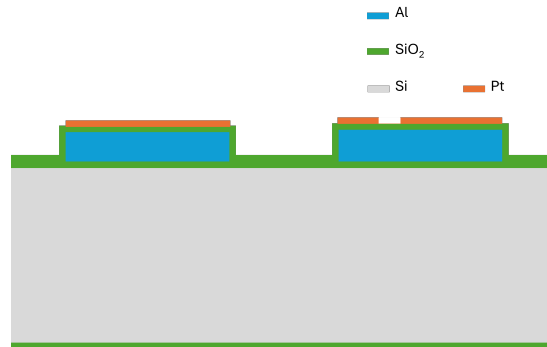


Figure 2.43: Wafer cross section scheme after Pt has been etched and PR has been stripped.

2.2.9. Front-side Insulation

The last step for what concerns the front-side fabrication is the deposition of the SiO_2 insulation layer, together with the patterning of the electrodes and pads seen in section 2.1.4.

Silicon Dioxide Deposition

The same procedure seen in section 2.2.7 is followed, so SiO_2 is deposited by PECVD, performed in *D250L PECVD (Corial, France)*. $1\ \mu m$ of material will be deposited that

will uniformly cover the surface of the whole sample. Once again SiO_2 has been chosen due being bio-compatibility and having a sufficiently low electrical permittivity.

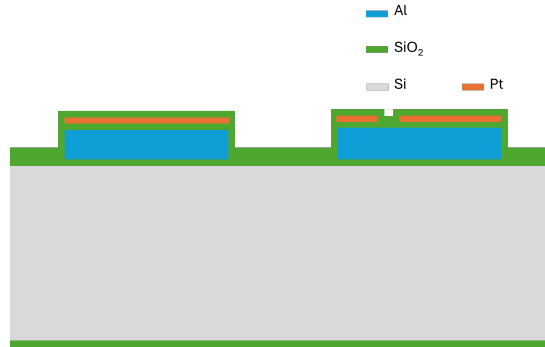


Figure 2.44: Wafer cross section scheme after SiO_2 has been deposited on its front-side.

Third Photolithography

The wafer is coated with $4.2\ \mu m$ of *AZ ECI 3027*, following almost the exact same procedure seen in section 2.2.4. there are only two differences, the first one is that the use of *HMDS* surface treatment should be preferred to dehydration, due to the SiO_2 substrate. The second one is that alignment has to be performed in this case. In particular it has been chosen to match SiO_2 pattern with the *Al* layer (3on1 alignment). This choice is due to the fact that the most critical point of this insulation layer is to perfectly cover the structural aluminum shanks, in addition this avoid summation of offsets that may be present.

Oxide Etching

To etch SiO_2 *APS* (*STPS Technologies, United Kingdom*) has been chosen, a plasma dry etching tool based on fluorine chemistry, optimized for dielectric removal. In fact, these materials tend to be difficult to etch by conventional RIE processes and require aggressive chemicals to be properly attacked. The system is equipped with an OES based End-Point detector, that allows to stop the process as soon as the dielectric material has been fully etched [94]. On *APS* there are many recipes for SiO_2 removal, that differs mainly for the etching rate and for their selectivity with respect to the mask. For our process *SiO2_PR_3:1* has been selected, since it offers a good compromise between these two parameters.

Recipe	Target	Chemistry	Etch Rate [nm/min]	Selectivity
SiO2_PR_1:1	SiO_2	CHF_3/He	WetOx:230 Si:95	1.7:1
SiO2_PR_2:1	SiO_2	C_4F_8/He	WetOx:440 Si:50	2.8:1
SiO2_PR_3:1	SiO_2	$C_4F_8/H_2/He$	WetOx:380 Si:35	4.2:1
SiO2_PR_3:1_SOFT	SiO_2	C_4F_8/He	WetOx:320 Si:35	3.7:1
SiO2_PR_5:1	SiO_2	$C_4F_8/H_2/He$	WetOx:235 Si:25	6.5:1
SiO2_PR_soft	SiO_2	$C_4F_8/H_2/He$	WetOx:170	>25:1

Table 2.6: Recipes available on *SPTS APS* for SiO_2 etching [94].

Alternative etching could also be performed by *PlasmaPro100 Cobra* (Oxford Instruments, United Kingdom) with CF_4 based chemistry, but the process is slower and has a worse selectivity with respect to the mask [82], so a thicker PR should be used, e.g. *AZ 10XT-60* after an overnight hard-bake at $65^\circ C$ [77].

PR Stripping

Due to the aggressive chemicals that are used for dielectrics etching, the resist surface tends to be significantly damaged, a compilation of dry and wet process for its removal are then especially important [94]. The process to follow is the standard one, described in section 2.2.6, but in this case O_2 plasma as a last step to completely remove of residuals should be performed. The cleaning of the sample from PR defines the conclusion of the front-side fabrication.

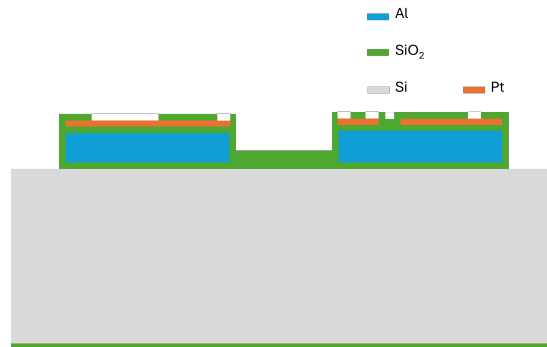


Figure 2.45: Wafer cross section scheme after SiO_2 has been etched and PR has been removed. The electrodes and pads now defined and exposed

2.3. Back-side Fabrication

As seen in the previous section, fabrication of the front-side has some challenges on its own that has to be taken into account. Despite that, the process follows a rather traditional fabrication procedure on *Si* substrate, this is important since we need our electrodes to be CMOS compatible. Now instead, backside processing has to be performed, that comprises the characteristic and innovative techniques used to produce the probes in exam.

2.3.1. Back-side Grinding

Back-side processing require in the following steps deep *Si* etching. To ease the process and reduce the high aspect ratio, that could pose significant challenges in the the release of the probes, the thickness of the whole wafer is reduced by mechanical grinding.

Front-side Protection

During grinding the wafer is subjected to a considerable amount of torsional stresses, so typically UV sensitive tape is used. This is able to reduce its adhesive power after exposure to UV light and it's used to protect the opposite side of the sample to process, i.e. the one clamped to the tool chuck.

Unfortunately the features on the front-side have a significantly high topology, so both the processing and the UV tape removal at the end of it could damage them. Thus, additional protection is require, this can be provided by coating it with a resist. The most used ones are non-photosensitive resists such as *MC PC 62E* or high viscosity photoresists as *AZ 10XT-60* [95]. In the case of interest, 10 μm of *MC PC 62E* are used as protection layer, the coating is manually performed on *SM-200*, (*Sawatec AG, Switzerland*), after treating the wafer surface with *HMDS* for adhesion improvement. Finally softbake is performed at 125°C for 10min (1 min/ μm) [95].

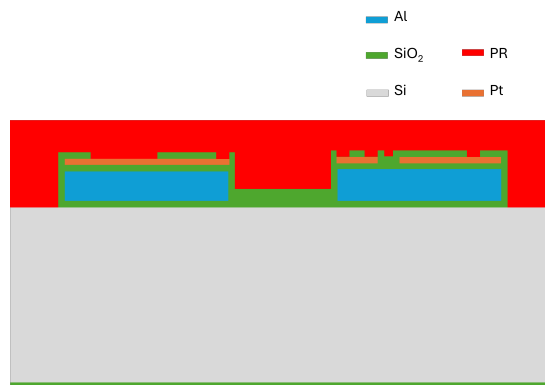


Figure 2.46: Protection coating on the wafer front-side, so to avoid features damaging.

Grinding Service

In CMI grinding is a service that is provided by the staff and it's performed on *DAG810* (*Disco Corporation, Japan*), an automatic surface grinder able to handle both wafer and small chips. The tool is equipped with a rotating diamond wheel, designed to process *Si*, III/V semiconductors as *GaN*, *GaAs* and glasses, such as *SiO₂* or Pyrex.

Samples are clumped to a rotating chuck by UV tape, while the spindle carrying the rotating wheel move downwards to remove material from the workpiece surface. Water is sprayed on the sample to cool it, remove dust particles and act as a lubricant. The grinding speed can be up to $30 \frac{\mu m}{min}$, obtaining a surface with a roughness below $100nm$ and a Total Thickness Variation (TTV) of maximum $1\mu m$ [96].

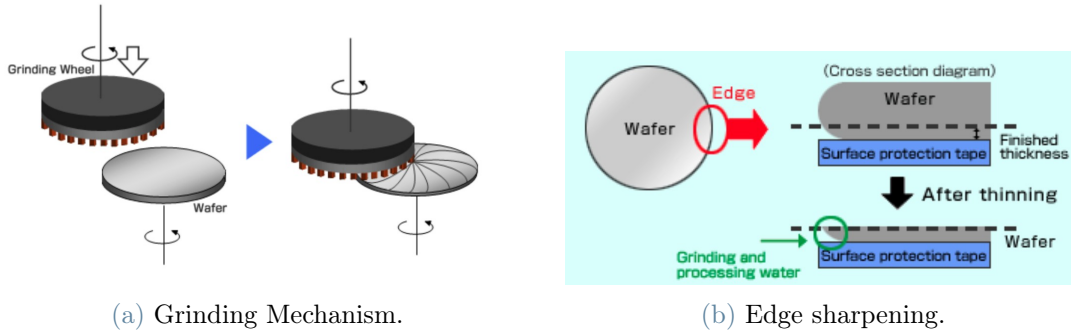


Figure 2.47: Grind mechanism can be seen. (a) The chuck is loaded with the sample and it's put in rotation, while a diamond wheel grind workpiece surface, (b) As wafer becomes thinner its edges becomes sharper and more fragile [96].

During this process the thickness of the wafer in exam is thinned down to $230 \mu m$, starting from a value of $380 \mu m$. Such value has been chosen since it offers a significant improvement in the aspect ratio of the wafer, for subsequent *Si* etching, without an excessive risk of wafer breakage. In fact, the more a wafer is thinned, the more it's rounded edges will become sharp, this combined with water cooling can induce breaking [96]. Finally a very thin wafer would be significantly fragile, this pose higher risk of critical failure both during handling and future processing.

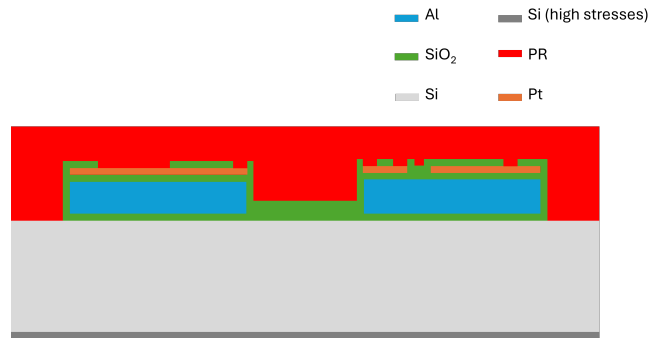


Figure 2.48: After grinding the thickness of the wafer is reduced, a region of with high internal stresses is present.

Backside Etching

During grinding the first layers of the sample are deeply affected, in particular three damaged regions can be defined. At the very top one can notice a roughness that depends on the wheel used, if no polishing is done afterwards a course surface is present. The second region is the most critical one, it ranges from $2 \mu m$ up to $10 \mu m$ from the surface and an high number of micro-cracks is present in it, these causes residual stresses in the wafer. Finally a third region in which crystal dislocations are present is found deeper into the sample, before retrieving the original crystalline structure [96].

To release internal stress due the second region presence, that could cause breakage of the wafer in subsequent processing, a backside *Si* thinning etching should be performed. This step is performed in *Rapier* (*STPS Technologies, United Kingdom*) a Deep Reactive Ion Etching (DRIE) tool for *Si* etching. The principles behind DRIE processes will be explained in section 2.3.5, while in this case a continuous isotropic etching process based on SF_6 is used. About $10 \mu m$ of *Si* will be etched, reducing surface roughness and releasing stresses [97].

$$t_{etch} = 1 \text{ min} + 40 \text{ s}$$

Recipe	Etch rate	Remarks
Si_Release	Vertical: $6 \frac{\mu m}{min}$ Lateral: $3 \frac{\mu m}{min}$	Continuous Isotropic Etching

Table 2.7: Si thinning recipe used for stress release [97].

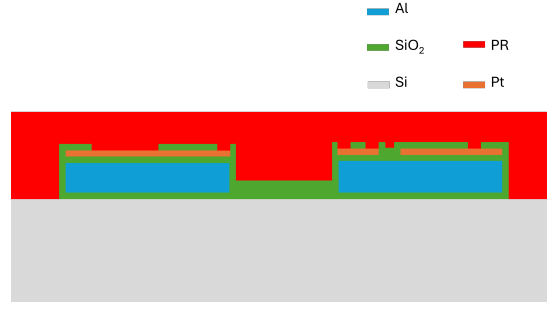


Figure 2.49: After stress release, by *Si* etching, the wafer is thinned down of about $10\mu m$.

Front-side Protection Removal

At this point the protection layer is not required anymore, so it can be removed. Since the resist did not endure any dry etching process, chemical removal by *SVC-14* is sufficient to completely strip the polymer. Regardless, *O₂* plasma in *GiGAbatch* can still be performed if some residues are observed on the sample.

2.3.2. Hard Mask Deposition

One of the mandatory processes to release the produced electrodes is to perform deep *Si* etching of $220\mu m$. To avoid the use of an extremely thick coating of photoresist, it has been chosen to deposit a *SiO₂* layer, on the wafer backside. This is called hard mask and to apply it *D250L PECVD* has been selected once again. In particular $1\mu m$ of oxide is sufficient to guarantee protection throughout the whole etching procedure [97].

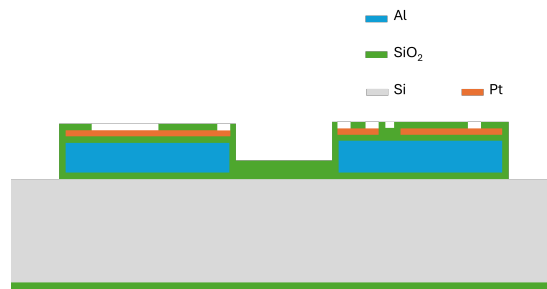


Figure 2.50: $1\mu m$ of *SiO₂* has been deposited on wafer back-side as hard mask for DRIE process.

2.3.3. Parylene Coating

Before proceeding with back-side processing the deposition of a sacrificial layer has to be performed, this layer plays two fundamental roles. The first one is to protect the features on the front-side during manufacturing, the second is to keep the probes fixed to the

Si wafer, before the final steps of probe release. *Parylene C* has been selected for this purpose, since it's a polymer resistant to acids, bases and solvents [98], while also having a high melting point of about 290°C [99]. This offers a significant advantage with respect to other protective layers, such as *MC PC 62E* seen in previous sections. In addition, *Parylene C* can be easily removed by O_2 plasma etching, thus being a perfect candidate as sacrificial layer [98].

Silanization

One of the main downsides of parylene is its poor adhesion to *Si* and *SiO₂*, in particular this has been a recurring problem in previous version of the process in exam, in fact due to the multiple fabrication techniques that the wafer has to go through, parylene detachment has been observed. In particular, having a non homogeneous layer, on the side of the wafer that has to be clutched on etching tool holders, is detrimental. Most of these machines exploit *He* flow on their chuck to dissipate the heat produced during etching processes [82, 94, 97]. To ensure correct cooling these tools are also equipped with systems to detect *He* leakage [94]; the more uneven is the substrate surface in contact with the holder, the higher the leak will be. If the outflow detected goes beyond a certain threshold the system will automatically abort the process, to avoid damaging the sample and the tool itself.

So to prevent parylene detachment, together with its consequences, before coating silanization is performed to improve the adhesion between the substrate and the polymer.

A174 adhesion promoter used, according to the following procedure:

1. A solution of IsoPropyl Alcohol (IPA), DI water and silane-A174 is prepared, with a volume ratio of 150 : 10 : 1;
2. Solution mixing is performed by mixing every minute for 10 *min* in total;
3. Sample is submerged into the solution, gently stirring it for 5 *min*;
4. Wafer rinsing with IPA;
5. Sample has to be baked at 100°C for 10 *min* [100].

At the end of the silanization process, coating should be performed as soon as possible due to the instability of silane layer in atmosphere [101].

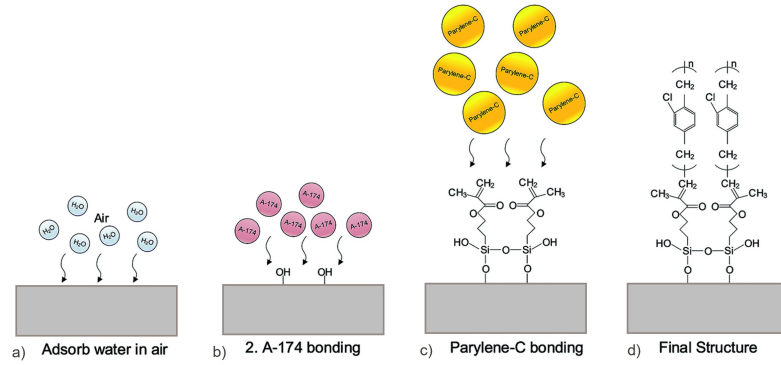


Figure 2.51: Silanization process and effects are illustrated. a) The hydrophilic substrate absorb water molecules from the atmosphere, b) OH group on the surface bond with $A-174$ heads, c) $A-174$ tails instead easily bond with *Parylene-C*, d) the end result is a good adhesion of parylene with the *Si* substrate. Taken from [102].

Parylene coating service

Parylene-C deposition is a service in *CMi* performed by *C-30-S* (*Comelec SA, Switzerland*). In the tool, under a vacuum of 10^{-3} mbar, a solid dimer is heated and vaporized at 150°C . The dimer molecules diffuse into a pyrolysis chamber, kept at 670°C , where they dissociate into monomers, which in turn diffuse into the polymerization chamber. This is kept in a temperature range between 25°C and 80°C , forcing monomer condensation and polymerization on the sample. The final thickness obtained depends on the load placed in the vaporization chamber, while the uniformity achieved is very high, with variations $< 1\%$ [98].

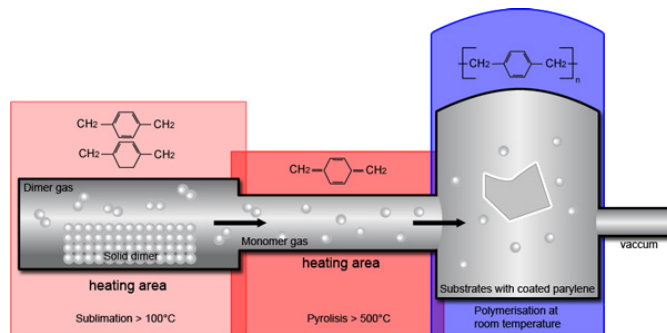


Figure 2.52: Parylene-C deposition procedure is illustrated. [98].

To avoid the usage of UV-tape, that could damage the feature present on the wafer, $5\mu\text{m}$ of *Parylene-C* are deposited on both sides of the sample.

Parylene etching

Since back-side processing still has to be performed, the polymer layer, now present on it, has to be removed. To do so an O_2 plasma etching recipe, on *PlasmaPro100 Cobra* (Oxford Instruments, United Kingdom), has been selected: *STS_Pyralin*. This method is highly directional and allows the complete removal of Parylene on the wafer back-side, without affecting the one on the front-side [82]. Alternatively *APS* (STPS Technologies, United Kingdom) could be used, since it can also perform O_2 plasma etching [94]. At the end of the full process the obtained result is depicted in fig. 2.53.

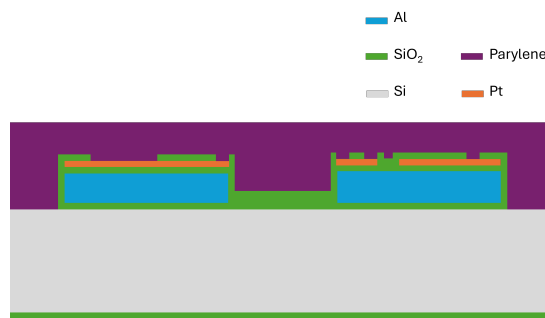


Figure 2.53: After deposition and etching of *Parylen-C*, the polymer is present only on the front-side of the sample, protecting the features on it.

2.3.4. Hard Mask Etching

As discussed in section 2.3.2, an hard mask has been deposited on sample backside, so to avoid *Si* wafer thinning during etching steps, without the need of PR. Nonetheless, the regions of the wafer under which the electrodes are positioned have to be freed by it, so to complete their fabrication. In particular a photolithographic step in which the front-side features are aligned with the ones on the back, is necessary.

First Back-side Photolithography

1 μm of *AZ ECI 3007* is deposited by spin coating on *ACS 200*, *HMDS* surface treatment should be performed beforehand, so to improve polymer adhesion to the substrate. To expose the resist *MLA 150* is used, but the key difference with respect to the cases seen previously is the backside alignment procedure. In this case, in fact, two layers on different sides of the sample will have to be aligned.

To do so, the wafer is positioned on the tool with its front-side positioned downwards, while the back-side camera, present on *MLA 150*, allows to identify the alignment marks already present on the surface. It is mandatory for the marks to be positioned in the blue regions that one can observe in fig. 2.54a, these corresponds to the holes present on the

tool holder, i.e. the only regions of the wafer visible from the back-side camera [76]. Other important considerations concern the fact that the wafer is flipped with respect to before, so the design should be also mirrored with respect to the y axis. Moreover, *MLA* coordinates system always refers to the upper surface, thus x value of imported coordinates should be always opposite with respect to the one on the design [76].

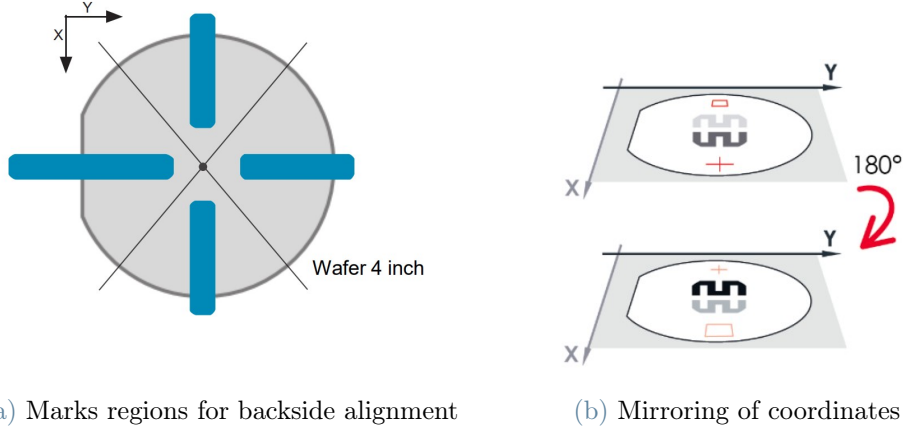


Figure 2.54: (a) Regions in which alignment marks can be positioned to perform backside alignment. (b) Mirroring with respect to y of the design coordinates [76].

During exposure on *MLA* there is no way to directly verify the alignment between front-side and back-side, but it is possible to do so exploiting the fact that *Si* is transparent to IR light. So one can observe, simultaneously, the features on the back-side, using light in the visible range, and the ones on the metal layers of the front-side thanks to IR light. In particular *DM8000* (*Leica Microsystems, Germany*), equipped with glass holder and IR back-side light, is used to perform such operation. Experimental results of these observations will be discussed in section 3.1.7. It must be noted that it is mandatory to perform such operation once development has been completed, to avoid accidental exposure of the resist, since the microscope required is not equipped with a filter for blue light.

Hard Mask Etching

Since SiO_2 has to be etched, the same process seen in section 2.2.9, i.e. a C_4F_8 plasma based dry etching. The process is performed in *APS* (*STPS Technologies, United Kingdom*), using the recipe *SiO2_PR_3:1*. The expected time of etching is:

$$t_{\text{etch}} = 2 \text{ min} + 38 \text{ s}$$

Photoresist Stripping

Previously the standard procedure illustrated in section 2.2.6, that combines wet and dry etching techniques, has been always used to remove the polymeric layer after photolithography. Unfortunately, in this case, such method is detrimental for our sample. In particular, the initial O_2 plasma step, performed in *GiGAbatch (PVA TePla, Germany)*, will also damage the protective *Parylene-C* layer, since the asher is designed to be effective on both sides of the samples. At the same time the usage of O_2 plasma can not be avoided either, since a wet chemical etch only, in *SVC-14*, is not sufficient to attack the burned PR that has undergone dry etching.

For the reasons above, an entirely O_2 based stripping method has been proposed, by the same recipes used to remove parylene layer, seen in section 2.3.3. Thus, either *STS_Pyralin* on *PlasmaPro100 Cobra (Oxford Instruments, United Kingdom)* [82], or *Pi_vertical* on *APS (STPS Technologies, United Kingdom)* can be used. These recipes are very highly energetic, so they could oxidize or damage layers in the samples, that is the reason why they are not typically used as a standard for PR removal. In our specific case, no oxidation sensitive layers are exposed to O_2 plasma, in fact on the backside only *Si* and *SiO₂* are present, so this alternative process is compatible with them. The clear advantage is the high directionality of such etching techniques and that the side locked on the tool chuck is protected, leaving *Parylene-C* unaffected.

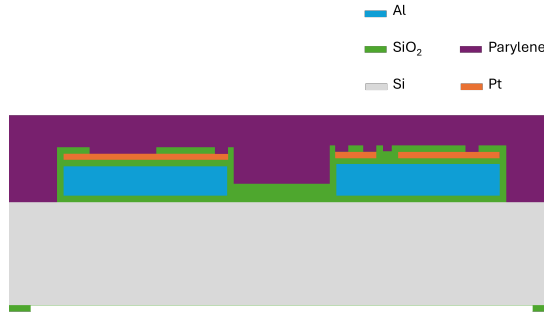


Figure 2.55: Wafer cross section after SiO_2 etching on backside and PR stripping.

2.3.5. Silicon Etching

One of the last steps before the probes release procedure is the backside etching of *Si*. This process is divided into two phases: the first is the definition of a step, that will determine the final thickness of the *Si* under the *Al* shanks, together with the one of the central chip. The second, instead, consists in a deep silicon etching, up until parylene layer on the front-side is landed.

Second Back-side Photolithography

First of all a new photolithographic process has to be performed, in particular $2\text{ }\mu\text{m}$ of *AZ 10XT-20* are coated in *ACS 200* after HMDS treatment is carried out. Also development can be done in the same automatic tool. The exposure, instead, is the most critical part, since in this case perfect alignment between *Al* shanks and the *Si* features is crucial. For this reasons two equally viable options could be followed.

Performing a backside alignment, with the same method used in section 2.3.4, so to directly align the exposed pattern with the *Al* layer. This method can guarantee a good alignment, but due to the poor resolution of the camera used to perform it, it could require multiple iterations before obtaining adequate results. Alternatively, if the *SiO₂* hard mask alignment assessment has already demonstrated a satisfying match between front-side features and the mask itself, then traditional alignment can be performed. In this second case the marks present on *SiO₂* mask layer will be used as reference.

Independently on the chosen method, it is mandatory to visually check alignment of the shanks with the patterns, by IR light microscopy, before proceeding any further.

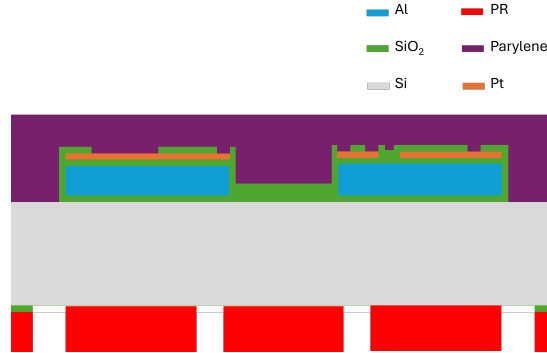


Figure 2.56: After the first *AZ 10XT-20* exposure and development, the features under the *Al* shanks and the central chip are protected by it.

Silicon Step Definition

Once photolithography has been completed, the first *Si* etching can be performed. By previous Finite Element Analysis (FEA) and experimental results [58], it has been calculated that $30\text{ }\mu\text{m}$ of *Si* guarantee enough stiffness to the shanks, so that no bending occurs during implantation, without preventing the shanks themselves to fold, due to their hindrance. For this reason, $30\text{ }\mu\text{m}$ have to be etched from the wafer backside, to define the step previously discussed. To perform such a deep etching in an anisotropic way, in fact steep vertical walls are desired, Deep Reactive Ion Etching (DRIE) technique, called Bosch process, has been selected; let's now discuss about the principle of functioning of such method.

It is based on working cycles, each one comprise three phases: deposition of passivation layer, anisotropic etching of the passivation layer and isotropic etching of *Si*.

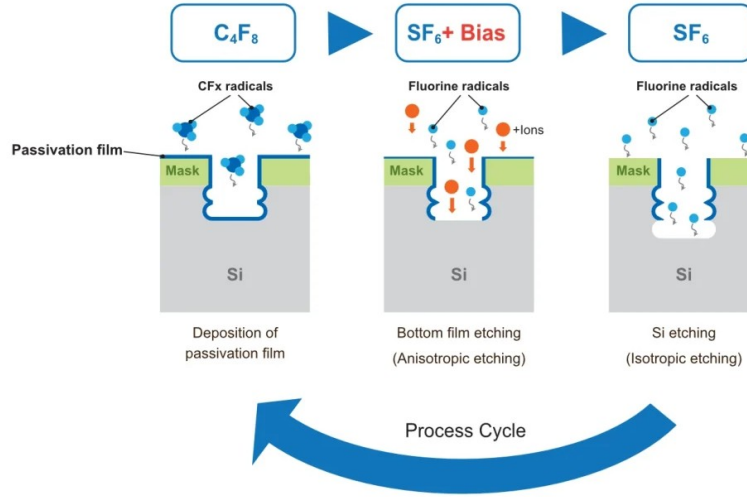
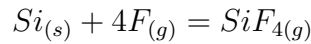


Figure 2.57: A Bosch process loop is depicted in figure, the three phases of passivation, anisotropic etching and isotropic etching can be seen, together with the chemicals used for each one of them, Taken from [103].

Deposition of the passivation layer is typically based on C_4F_8 molecules, these are cyclic organofluorine compounds that undergo plasma induced ring-opening. This results in CF_x radicals formation, active on both ends of the chain, so a polymerization reaction is induced, forming a thin film that covers the surface of the sample. After deposition, SF_6 gas is introduced into the chamber, this is decomposed by plasma in SFx ions and free radicals F . The first ones are accelerated by biasing, physically etching the passivation layer on the bottom of the trenches, exposing *Si*. without affecting the protective layer on trench sidewalls. In the last step fluorine atoms, isotropically etch *Si*, according to the reaction [104]:



Each step lasts only few seconds, in particular for the recipe used for the process in exam, *DRIE on Rapier (STPS Technologies, United Kingdom)*, the following times have to be considered: $t_{\text{pass.}} = 1.5 \text{ s}$, $t_{\text{anis.etch.}} = 1 \text{ s}$, $t_{\text{isot.etch.}} = 3 \text{ s}$ [97].

The etching rates, instead, are strongly dependent on the width of the trenches to process. For the selected recipe, it is stated that for trenches with a width $< 2 \mu m$ about $300 \frac{nm}{loop}$ are expected to be etched, While if the trench is larger than $200 \mu m$, than even values higher than $800 \frac{nm}{loop}$ can be obtained [97]. In addition these values can not be assumed constant, but also depends on the depth that is reached, in fact the deeper the aspect

ratio, the more difficult it will be for the gas molecules to reach the bottom of the trench, resulting in lower etching rates. To be able to assess the actual values, a common method is to perform etching for a small number of loops and measure the step that has been removed. This technique allows only to evaluate the initial etching speed, but it does not take into account its reduction as the process goes on. If one would like to obtain a final trench depth as precise as possible, iteration of the measurement can be performed, so to correct the number of loops based on the evolution of the etching rate. In the case in exam the final thickness of *Si* has simply structural purposes, so no such fine tuning is required. The etching rate is been evaluated based on the minimum trench width present in our features, obtaining $\approx 720 \frac{nm}{loop}$. So the total number of loops required to remove $30\mu m$ of *Si* is:

$$n_{loops} = \frac{\text{thickness}}{\text{etch/loop}} = \frac{30'000}{720} \approx 42$$

A final consideration to do is that, as discussed in section 2.2.3, descum should always be performed before any etching procedure. Up until now this step has always been performed in *Gigabatch* O_2 plasma asher, but this could damage *Parylene-C* layer. Thankfully, O_2 plasma is also implemented on *Rapier*, for this specific purpose, so *DRIE_w_descum* recipe has been selected; in which 10 s of O_2 plasma are conducted, etching about 100 nm of PR, before initiating *Si* etch [97].

Photoresist stripping

Due to the same considerations seen in section 2.3.4, PR stripping is performed in *APS* plasma etcher, so to avoid detachment of parylene layer. Once the resist has been removed the wafer profile expected is depicted in fig. 2.58

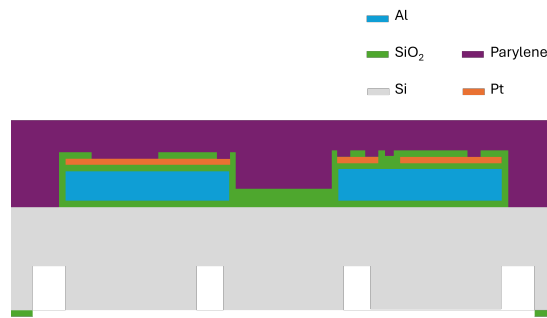


Figure 2.58: After the first DRIE *Si* etching is performed a $30\mu m$ step is present on the wafer backside.

Second Silicon Etching

Once the PR has been completely removed, *Si* etching can be performed once again.

2.3.6. Backside Insulation

The very last step before probe release is to apply an insulation layer on the probes backside. In previous version of the process the parylene has been selected as a material, due to its renewed bio-compatibility [7]. Despite that, the poor adhesion of the polymer to the *Si* substrate, combined with the nonhomogeneous O_2 plasma etching, that was causing the electrodes to flip over during release, damaging the backside insulation, have brought to the decision of changing the material used for it. In particular, SiO_2 has been chosen, being the same material exploited for the insulation of the front-side, as seen in section 2.2.9. Apart from its bio-compatibility, another important advantage of it, is that it can be processed in the same tool in which *Parylene-C* removal can be performed. This, as it will be discussed in the next section, allows to release the probes without handling the sample, avoiding risk of breakage.

To perform deposition of the oxide, *PECVD* in *D250L PECVD (Corial, France)* is not a valid option in this case, since the substrate holder is fixed at 320°C [86], that is above the melting temperature of parylene [99]. So SiO_2 is deposited by sputtering at room temperature in *Spider 600 (Pfeiffer Vacuum, Germany)*, following the recipe in table 2.8.

Material	PM	Target	Recipe	Source	Power [W]	Ar [sccm]	Dep. Rate [nm/min]	Ramp [s]
SiO_2	1	SiO_2	SiO2-#	RF	1000	15.0	54.0	30

Table 2.8: SiO_2 process parameters in *Spider 600* [73].

500 nm of silicon dioxide will be deposited, so the time of deposition can be computed with the formulations seen in section 2.2.3, taking into account the ramp, the total deposition time is:

$$t_{SiO_2} = 9 \text{ min} + 31 \text{ s}$$

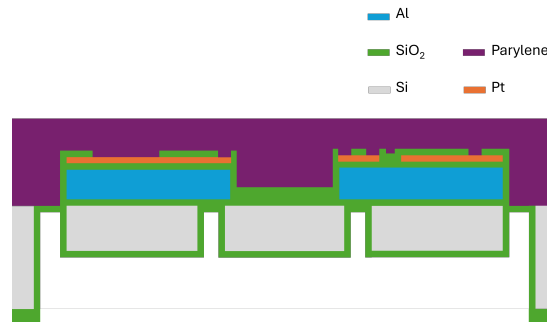


Figure 2.60: After the deposition of 500 nm of SiO_2 , the electrodes fabrication is completed, release and bending can be finally performed.

2.4. Probes Release and Bending

Having shaped all the layers required for the functioning of the electrodes in exam, all the samples have to be released from the wafer in which they are currently suspended in. Once such step is completed, the shanks of each one of them, are folded, so that the final probes can be obtained.

2.4.1. Carrier Wafer

Carrier Wafer Fabrication

Since probes release implies their detachment from the wafer they have been on up until now, it is necessary that a wafer, with sockets to accommodate the released electrodes, is produced. Starting from a *Si/100mm/SSP/Test* wafer [105], a photolithography is performed, so that sockets corresponding to the position of each probe are patterned on the *Si* surface. 2.6 μm of *AZ ECI 3027*, suggested for Bosch processes [77], are coated on *ACS 200* after HMDS surface treatment. Exposure is performed by *MLA 150*, while development can be done, once again, in *ACS 200*. Alternatively manual photolithography could be performed, by *SM-200* and wet benches.

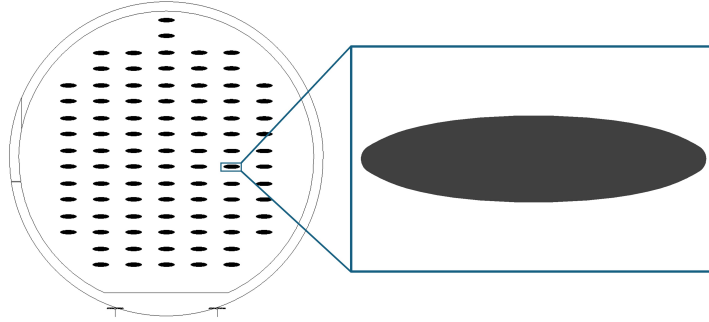


Figure 2.61: Wafer carrier design, the black ellipses corresponds to the sockets that will receive the released probes.

Once the resist has been patterned, DRIE is performed in *Rapier*, as for previous deep *Si* etchings. Ideally, trenches about $45\ \mu\text{m}$ deep would be enough to harbor the samples, whose total thickness, given the parameter defined in previous sections, should be $< 40\ \mu\text{m}$ thick. Nevertheless, to allow for the possibility of having thicker *Si* structural features and to facilitate probes transport in the carrier wafer, deeper trenches, of about $100\ \mu\text{m}$ have been preferred. Considering an etching rate of $800\ \frac{\text{nm}}{\text{loop}}$ [97] then, the total number of loops required is:

$$n_{\text{loops}} = 125$$

Note that descum should be performed before etching, this can be done either in *GiGAbatch* at low power or directly in *Rapier*, selecting a recipe that includes 10 s of O_2 plasma. After the etching has been completed photoresist can be stripped by the standard cleaning procedure, seen in section 2.2.6: combining high power O_2 plasma in *GiGAbatch* and chemical etching in *SVC-14*.



Figure 2.62: Wafer carrier cross section after deep *Si* etch and PR strip.

Wafer and Wafer Carrier Alignment

The two wafers, the carrier and the one with the electrodes on, can be easily aligned one on top of the other, by using the flat of the tow as reference for manual positioning. In fact, to achieve our scope, a slight mismatch is still acceptable, thus no further alignment

is required.

Despite this, it is imperative to keep the two wafers bound together during the subsequent process. To do so, the carrier wafer is positioned on a hot plate at 135°C , then *Quick stick 135* [106], a wax used to temporary sticking wafers together, is applied on the four cardinal points of the dummy wafer. Then the wafer to process is placed on top and is aligned, as described. As soon as the two are removed from the hot plate, the wax will rapidly cool down and solidify.

This method is advantageous, due to the fact that it's easy to rework, if necessary, and to unbind the two samples; in fact, it is sufficient to heat up the *Quick stick* once again to make the wax flow. In addition, carrier wafer can be used multiple times, after cleaning it with acetone, to remove wax residues.

At the end, each probe will be suspended above its respective socket, as depicted in:

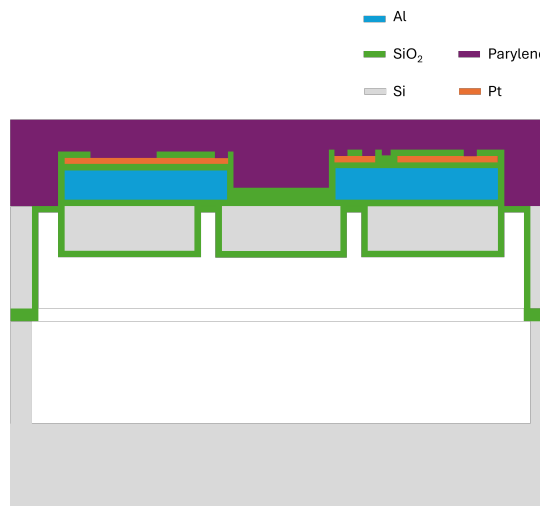


Figure 2.63: Once the wafer and the carrier have been properly aligned, each probe is upended on top of its socket, so to fall in it once released.

2.4.2. Electrodes Release

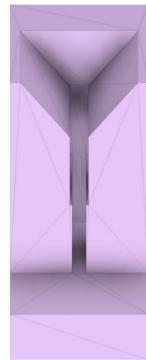
To release the probes two steps are required: the complete removal of the protective *Parylene-C* layer and the etching of $500\text{ }\mu\text{m}$ of SiO_2 , this will also cause a thinning of the oxide on the probes front-side. At the end of the two processes the samples will fall on the carrier wafer sockets, and they will be fully encapsulated in $500\text{ }\mu\text{m}$ of SiO_2 .

Both etching processes can be performed on *PlasmaPro100 Cobra* (Oxford Instruments, United Kingdom). Alternatively also *APS* (STPS Technologies, United Kingdom) would be able to etch moth materials, but it should be discarded due to the absence of a laser EPD system. This, in fact, not only allows to have a better control on the etching of the

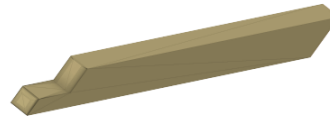
hundreds of μm [107].

The manual bending procedure is the following:

1. Probe placement on top of the guide, with the back-side facing upwards;
2. Initial bending of the probe, by pressure application on its center through the printed lever. The guide ensures an initial bending of the shanks at 45° ;
3. Further pressure application, causing the full bending of the shanks, at 90° with respect to the center of the probes.



(a) Guide for Bending



(b) Lever for Bending

Figure 2.65: (a) Guide to perform probes bending, in the upper part an angle of 45° is forced, while on the bottom steep vertical walls are present. (b) Lever used to perform the bending.

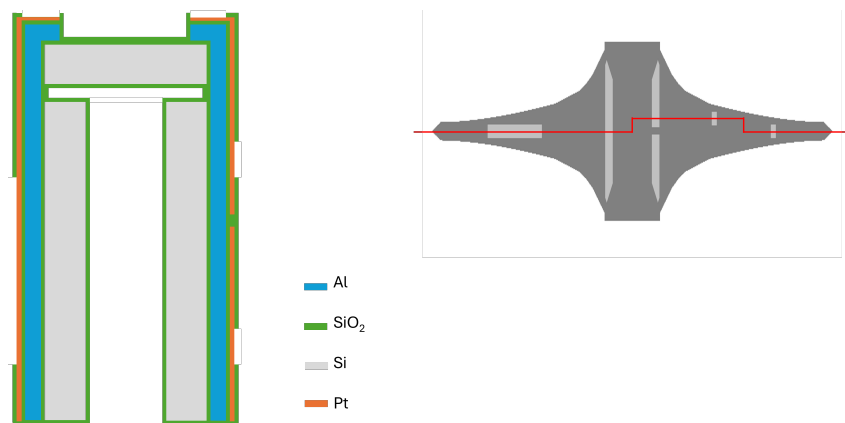


Figure 2.66: Cross section of the fabricated probes after bending (on the right). Top view of the probe used as a reference, to define the line along which the sections are retrieved (on the left). Note that the design is deformed for a better image legibility.

3 | Experimental Results and Discussion

In the previous chapter, we fully discussed the design of the foldable electrodes in the exam, along with all its variants and the purpose of each one. Then a full dissertation about the processes required for the fabrication of the probes has been provided, including the selected materials and the exploited tools.

It is now time to discuss the actual results obtained and all the techniques used to characterize the electrodes at each step of their fabrication. All the experimental work that has been performed during this thesis project can be divided into three macro topics: electrode fabrication, electrical characterization, and electrochemical characterization.

3.1. Electrodes Fabrication

The fabrication of the foldable probes has been performed following the procedure discussed in chapter 2, nevertheless to obtain optimal result it is mandatory to inspect the results obtained at each step of the process, so as to be constantly aware of the state of the fabrication and to identify possible criticalities as soon as they occur. Depending on the parameter that one desires to evaluate, many different techniques can be used, such as visual inspection through optical or electron microscopy, profile measurement, spectroscopy to identify materials, and many more. Through the following sections, all fabrication will be followed step by step, assessing the results obtained at each step, and discussing the techniques and tools used to perform the inspections.

3.1.1. Aluminum Deposition

As discussed in section 2.2.3 the first step of the process is the deposition of $4\text{ }\mu\text{m}$ of *Al* on front-side of the selected wafer by sputtering on *Spider 600* (*Pfeiffer Vacuum, Germany*). Evaluation of the residual internal stresses after the deposition of such a thick layer has been performed through *FLX 2320-S* (*Toho Technology, USA*), a dual wavelength stress

measurement systems that use a laser to measure changes in the radius of curvature, pre and post deposition; these are then correlated to their correspondent stress value [108].

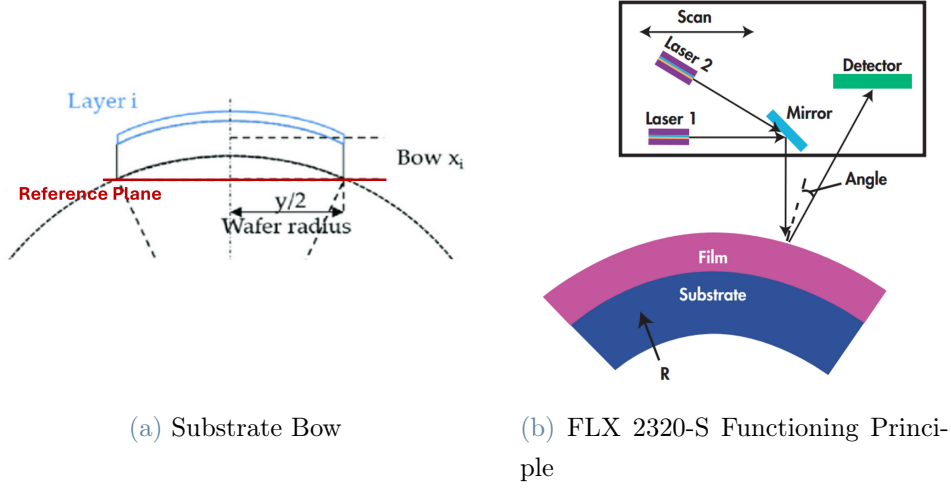


Figure 3.1: (a) Substrate bow with respect to the reference plane considered by the instrument (b) Laser angle detection system on FLX 2320-S, used to measure stresses induced by *Al* layer deposition.

The system provides informations about the wafer bow, x_i , with respect to a reference plane. This allows to retrieve the curvature radius, R_i , of the substrate, knowing the wafer radius, y , thanks to the following formula [109]:

$$R_i = \frac{y^2}{8x_i} + \frac{x_i}{2}$$

Once the radius of curvature before the film deposition, R_1 [m], and afterwards, R_2 [m], have been evaluated, an equivalent radius can be computed:

$$R = \frac{R_1 R_2}{R_1 - R_2}$$

And finally the internal stress is evaluated as:

$$\sigma = \frac{Eh^2}{(1 - \nu)6Rt}$$

in which: E [Pa]: elastic modulus of the material, ν : Poisson's ratio, h [m]: substrate thickness and t [m]: film thickness. Five wafers have been coated with *Al* and two measurements have been performed for each one of them, along the x and y axis of the substrate, so to obtain a more accurate measurement of the overall curvature. Having

considered an elastic modulus of $E = 188 \text{ GPa}$ and a Poisson ratio of 0.3 [109], the following results have been obtained: final average bow $\mathbf{x}_{av} = 61 \mu\text{m}$, with a Relative Standard Deviation (RSD) of 17.5%, and an average stress $\sigma = -77.6 \text{ MPa}$ with an RSD of 18.3%. It should be noted that a negative value denotes a tensile stress, typical of metallic layer [110]. The relative high standard deviation is related to multiple reasons: initial thickness of the substrates is not always the nominal one of $380 \mu\text{m}$, that has been used for the computation, the same is true for the initial bow of the bare substrate. In addition the value of stress computed may differ, since the thickness of the deposited layer may differ from the expected $4 \mu\text{m}$.

Regardless, it is worth to perform this evaluation, since it reveals a relatively high bow of the wafer after *Al* deposition. Although this did not cause any major issue in the fabrication itself, due to the fact that the automatic wafer detection system installed on *ACS 200 Gen3*, (*SUSS MicroTec SE, Germany*) was not always able to verify the presence of the sample during photolithography, causing process abortion. In order to avoid such occurrence first photolithography has always been performed manually on *SM-200*, (*Sawatec AG, Switzerland*). After *Al* etching and consequent stress release, the bow has been sufficiently reduced that no further limitation on usage of automatic photolithographic systems has been found.

3.1.2. Photolithography Inspection

The wafer have been manually coated with $4 \mu\text{m}$ of *AZ ECI 3027*, that have then been exposed in *MLA 150* (*Heidelberg Instruments, Germany*) with dose and de-focus values according to the updated table present on the tool. Manual development has been performed, after PEB at 100°C for 90 s, by submerging the sample in *AZ 716 MIF* for 2min; then the wafer is rinsed in DI water. Two cycles of immersion and rinsing have been performed to guarantee optimal results.

Before proceeding further, after each photolithography, visual inspection on the obtain results it is of great importance. In fact, if inadequate outcomes are assessed, the polymer can be stripped from the surfaced and the whole photolithographic process can be performed from the start, without any damage to the substrate. Such visual inspection has been performed by *DM8000* (*Leica Microsystems, Germany*), the standard optic inspection microscope used in CMI [111].

Apart from a good fidelity with the design, one should seek for the absence of two major issues: underexposure and photoresist residues, both shown in fig. 3.2. The first one occurs when the dose and defocus selected in the exposure step are not sufficient to properly irradiate the PR; in this case regions of polymer are not developed properly. In particular,

as for the case illustrated in fig. 3.2a, operating very close to the dose threshold of the PR, results in very regular and sharp undeveloped lines, due to the small fluctuations of the laser intensity that occur during exposure. When this problem occurs usually it affects most of the sample surface, so it is advise to repeat the entire process with a higher dose. The other issue that may be present is the presence of residues of undeveloped PR, these can occur systematically due to inadequate development or can be occasional, in the latter case, if just a few number of samples are affected on a wafer, one may decide to proceed despite their presence. Moreover, if they are small enough, they can be removed by performing another development cycle or by O_2 plasma descum. Finally it may occur that, during development, that some of the pattern features are damaged; this is most likely another occasional phenomena that could be ignored if most of the samples are unaffected. In case it extensively covers the wafer surface, this usually implies overexposure of the resit, that has cause a poor fidelity of the features with respect to the design.

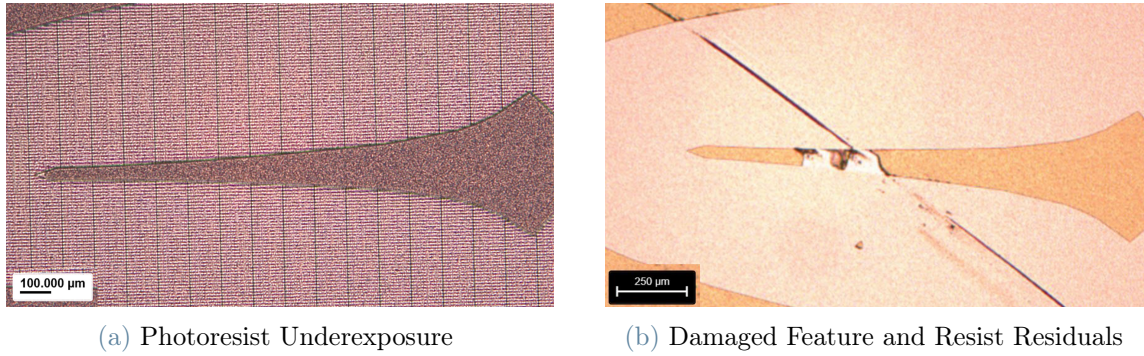


Figure 3.2: (a) Regular undeveloped PR lines, due to underexposure of the resit. (b) In this case two issue are shown: the damaging of the feature, it can be seen that a portion of the shank is missing, and the presence of residuals of PR (black line).

3.1.3. Aluminum Shanks Inspection

Having assessed the correct reproduction of the exposed designs on the resit, *Al* etching has been performed on *PlasmaPro100 Cobra* (*Oxford Instruments, United Kingdom*), by plasma dry etching based on Cl_2 chemistry; details on the process are found in section 2.2.5.

Once the etching has been completed and the resit has been removed, the three main characterizations of the results that can be performed are: visual inspection, spectroscopy and thickness measurements.

Visual Inspection

To assess correct design reproduction on the *Al* layer, first of all, the shanks were inspected on *DM 8000* optic microscope. This quick inspection already confirms sharp contours of the features and in general a proper transposition of the pattern, as depicted in fig. 3.3.

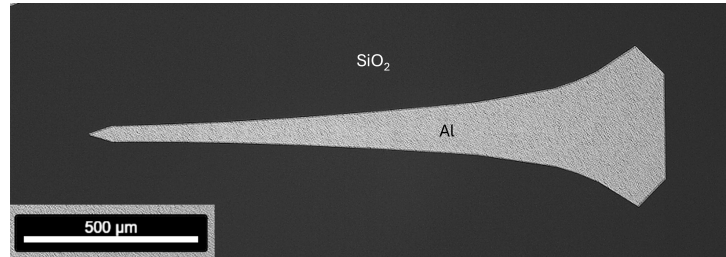


Figure 3.3: Aluminum shank obtained after etching and *PR* stripping.

For a better characterization of the microstructure obtained through the sputtering technique used, it has been decided to inspect the samples also by scanning electron microscopy. The tool used was *MERLIN* (*Zeiss, Germany*), a Field Emission Scanning Electron Microscope (FE-SEM), a high-resolution imaging and analytics system [112], based on *Gemini 2* (*Zeiss, Germany*) column and equipped with three different detectors, each optimized for a different task. Gemini 2 column is the chamber where electrons are emitted by a heated filament, then are accelerated, bundled, focused, and deflected, so that a focused beam of electrons is produced [113]. In SEM imaging, two types of scattered electrons are mainly used: Secondary Electrons (SEs) and Back Scattered Electrons (BSEs). The first ones are generated by inelastic electron-electron interactions, which typically occur in the first layers of the material. BSEs, on the other hand, are originated by elastic electron-nuclei scattering, and can provide informations about deeper regions of the material analyzed. A schematic representation of their origin are provided in fig. 3.4. The detectors present on *Merlin SEM* exploit information from these two types of scattered electrons to reconstruct images of the sample surface. In particular:

- **In-Lens Detector** Exploits SEs for high-resolution surface imaging. Strong tilting of the sample should be avoided to achieve optimal resolution.
- **HE-SE2 detector** Sensitive to both SEs and BSEs. It is used to produce the so-called pseudo-backscattered image, which enhances the topography of the image. The main downside is that edge contrast is lower, canceling out surface features.
- **EsB detector** An energy-selective backscattered detector, used to enhance contrast between materials present on the surface. Also, in this case, strong sample tilting should be avoided [113].

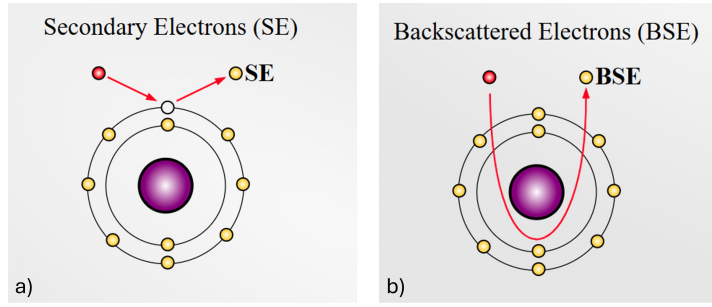


Figure 3.4: a) SEs generated by elastic interaction with electrons of the analyzed material. b) Primary electrons elastically scattered by material nuclei produce BSEs. Taken from [114].

HE-SE2 detector was used to characterize the surface topology of the *Al* shanks. It can be observed in fig. 3.5 that the sputtering process used to deposit the metal, produce a relatively rough surface, with a grain size that goes from hundred of *nm* to few μm ; this is in accordance to what was expected from the deposition technique selected. SEM imaging also confirms an adequate fidelity of the fabricated features with the design.

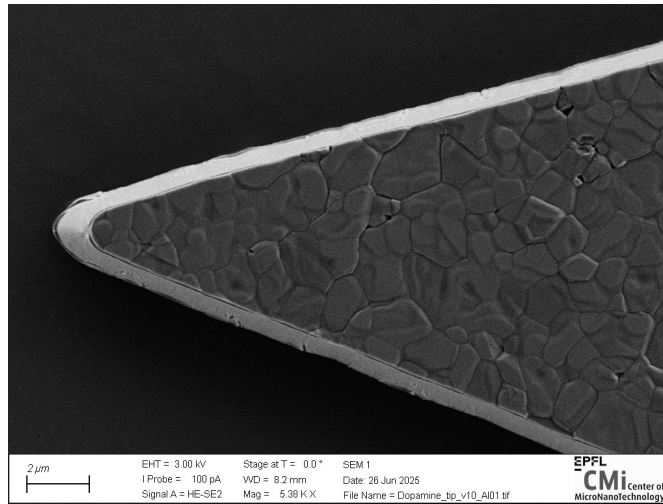


Figure 3.5: SEM image of the *Al* shank tip, it can be noticed the rough topology of the surface typical of *Al* sputtering.

Energy Dispersive Spectroscopy

To verify complete removal of *Al* in the etched regions, Energy Dispersive Spectroscopy (EDS) has been used. This technique allows to identify materials present on a sample surface by the characteristic X-ray emission wavelength that can occur due electron transition from an higher energy level to a lower one. *Merlin SEM* has been used to perform

the measurement, since it is equipped with *X-Max* (*Oxford Instruments, United Kingdom*), a detector Silicon Drift Detector (SDD) with a resolution of 127eV FWHM [115]. The functioning principle of this technique is that, when primary electrons interact with the valence electrons of a material by inelastic scattering, thus producing SE, a vacancy is generated. In case the scattered electron is not one of the highest energy ones, then such vacancy will be filled by an electron with higher energy, while a photon will be emitted to balance out the energy difference. Each element has one or more characteristic energies of emission, so their measurement can be used to identify their presence.

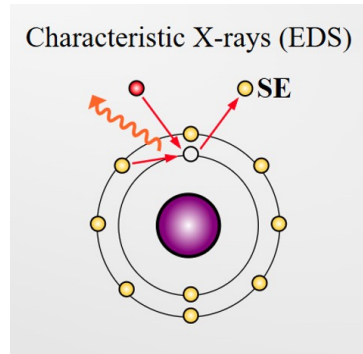


Figure 3.6: When a lower energy electrons is scattered, the vacancy is filled by an higher energy ones, with consequent characteristic photon emission. Taken from [114].

In the case in exam EDS was used to verify absence of *Al* and presence of *SiO₂* in the regions where the metal has been etched, exposing the insulation layer underneath; i.e. the black region in fig. 3.5. It can be seen in fig. 3.7 that presence of *O* and *Si* were confirmed, as well as the absence of *Al*.

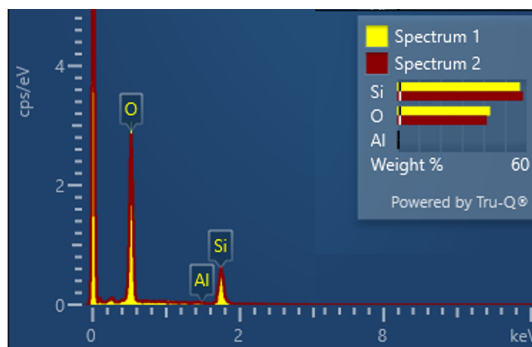


Figure 3.7: Two different regions, in which *SiO₂* was expected, have been analyzed, corresponding to Spectrum 1 and Spectrum 2. Both of them revealed presence of *O* and *Si* and the absence of an *Al* related signal. The unlabeled peak at very low energy is due to background noise and it's always present in the system used.

Thickness Evaluation

Having confirmed composition and geometry of the produced features, an evaluation of the actual deposited thickness has been performed by *Dektak XT* (*Bruker Corporation, USA*), a mechanical profilometer. The tool is able to determine, electro-mechanically, thin and thick step height by moving a diamond-tipped stylus over the sample surface [116]. The maximum vertical range is of 1 mm, while having a step-height repeatability of 5 Å [117]. The step measured was 3.7 μm, so difference of 7.5% is present with respect to the expected nominal value of 4 μm, such value is adequate to the scope of the shanks. In addition, rough surface of Al layer have observed, confirming the evaluations seen in fig. 3.5.

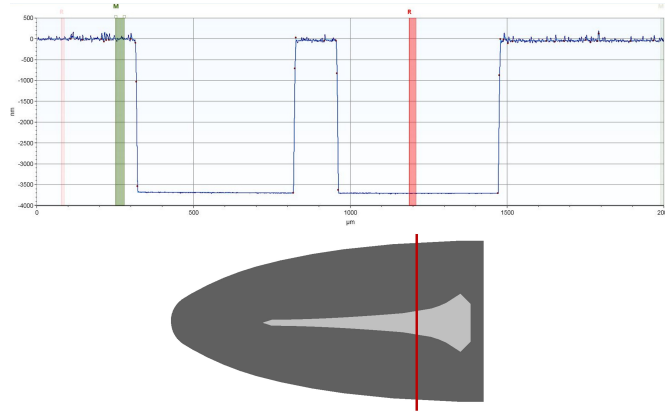


Figure 3.8: Profile of the Al step. The step is evaluated by computing the difference between the average height of the region M and the one of region R. An indication on the axis along which profile has been evaluated is also provided (on the bottom).

3.1.4. Platinum Tracks Inspection

The fabrication of the electrodes has continued as described in the section 2.2: 1 μm of SiO_2 has been deposited by PECVD in *D250L PECVD* (*Corial, France*) at a temperature of 320°C for 2 min and 28 s. Having completely and uniformly isolated the shanks of Al, 200 nm of Pt have been deposited by sputtering in *Spider 600*; with a processing time of 10 s for the Ti adhesive layer and 42 s for Pt. Automatic coating on *ACS 200* has been performed, no issue due to excessive wafer bending has been encountered. The chosen resist is *AZ 10XT-20*, with a thickness of 4 μm. After exposure on *MLA 150* and automatic development on *ACS 200*, reflow of the polymer has been performed. In fig. 3.9 the patterned resist before and after reflow can be observed, it should be noted that in picture a variation of the design seen in section 2.1.4 is shown. In this design the edges are rounded, so to facilitate optimal flow of PR during this step, anyhow, no reflow issues

have been found, even in the standard design with sharp edges.

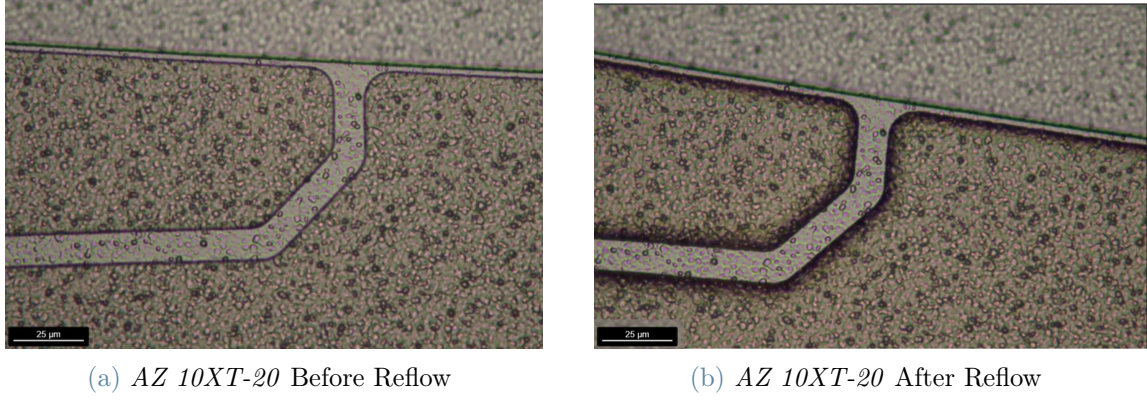
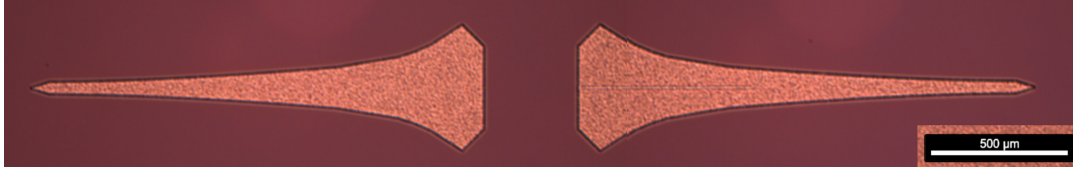
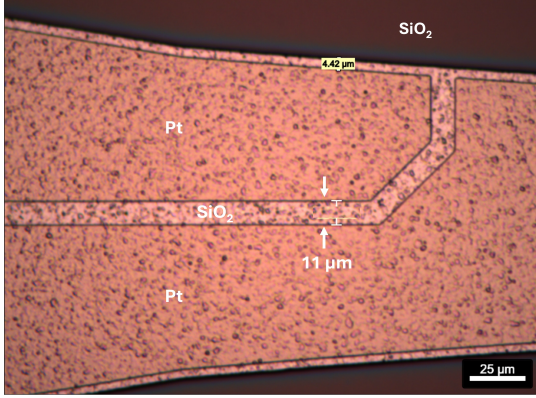


Figure 3.9: 4 μm of AZ 10XT-20, exposed and developed. (a) Before reflow of the polymer. (b) After reflow, a dark shadow due to the rounded edges of the resist can be observed.

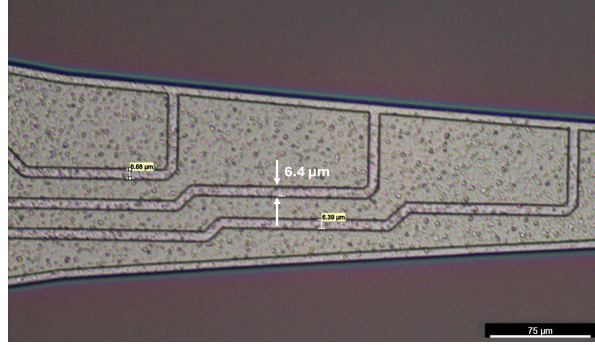
Having assessed a correct reflow and a proper alignment of the resist, *Pt* has been sputtered in *Nexus IBE350* (Veeco, USA), with the parameters defined in section 2.2.8, until EPD has been reached. The resist has been stripped and visual inspection of the features has been performed under optic microscope. Particular focus has been reserved to the alignment of the *Pt* layer and to the fidelity of the trench with respect to its design. It can be observed in fig. 3.10b that a trench width of about 11 μm has been obtained, over an ideal value of 10 μm . Such difference is compatible with the critical dimension of the photoresist used to perform the lithography, in fact AZ 10XT-20 has $CD = 1 \mu m$ [63, 88]. In addition it can also be seen that the layer is centered with respect to the shank beneath it. Similar evaluations have been performed for the multiple working electrodes designs, as in fig. 3.10c, for which trenches width of about 6.5 μm have been evaluated; once again compatible with the technology used. Finally, electrical characterization of the patterned *Pt* tracks has been performed at probe station, *TS150* (MPI Corporation, Taiwan), details about the topic will be discussed separately in section 3.2.1.



(a) Three electrodes Platinum layer (optic microscope)



(b) Platinum layer trench, three electrodes design (optic microscope)



(c) Platinum layer trench, multiple electrodes design (optic microscope)

Figure 3.10: (a) Image of the patterned platinum layer on the *Al* shanks of the three electrodes design. (b) Detail of trench that separates *Pt* in three electrode design and (c) in multi electrodes design.

3.1.5. Insulation Layer and Electrodes Geometry Inspection

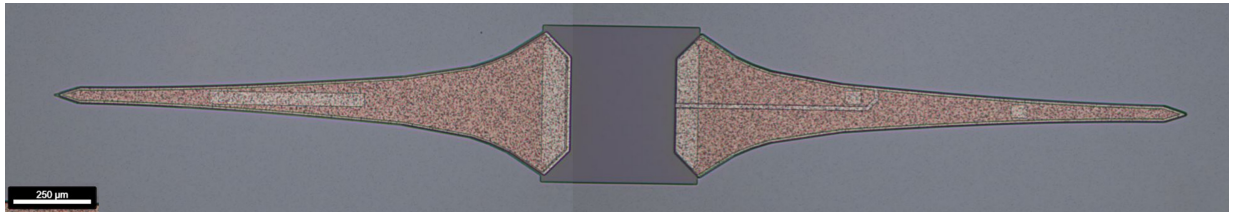
Having assessed geometrical and electrical properties of *Pt* layer, front-side fabrication has been completed, as described in section 2.2. $1\ \mu\text{m}$ of SiO_2 has been deposited, once again, by *D250L PECVD*, following the same parameters stated in the previous section. Then *ACS 200* has been used to perform automatic coating and development of $4.2\ \mu\text{m}$ *AZ ECI 3027*. The resist has been accurately inspected to assess its alignment with underlying layers, then SiO_2 etching has been performed in *APS (STPS Technologies, United Kingdom)*. The parameters discussed in section 2.2.9 have been used, while the process was stopped exploited the OES end point detector installed in the tool. After patterning of SiO_2 layer and PR stripping, visual inspection under optic microscope of the probes have been performed. Here an overview of these inspections is provided, for each of the fabricated designs.

Standard Design

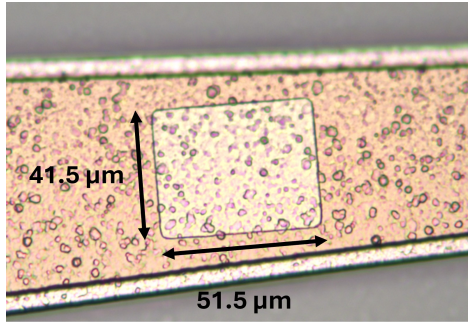
First of all, independently on the design, it has been confirmed that SiO_2 layer properly insulates the shanks, with special attention to their sidewalls. It can be observed

in fig. 3.11c that the chosen tolerances were sufficient to encapsulate the probes in the insulation layer. In fact, in correspondences of the electrodes tip, about $3\ \mu\text{m}$ of oxides exceed the shanks edges from one side (the top in figure), while the excess is of about $2\ \mu\text{m}$ for the other (bottom of the figure).

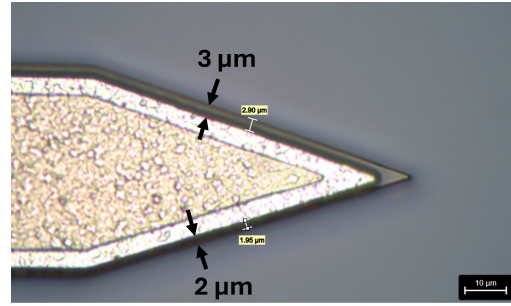
Then evaluation on the fidelity has been performed for each design, from fig. 3.11a one can notice that the proposed structure visually match with the design proposed in section 2.1.5. Moreover the sizes of the obtained electrodes are in agreement with the resolution of the process used. In fig. 3.11b it can be observed that the WE obtained has a length of about $51.5\ \mu\text{m}$ and a width of $41.5\ \mu\text{m}$, so the final are obtained is about 7.5% larger than the ideal one. This increment is acceptable for the scope of interest, nonetheless it has been observed that there is a systematic increment of the electrodes sizes in all the observed design. So it can be assumed that, for a more precise reproduction of the desired electrodes areas, a correction of $-1\ \mu\text{m}$ could be uniformly applied.



(a) Probe Standard Design (optic microscope)



(b) $2000\ \mu\text{m}^2$ Working Electrode (optic microscope)



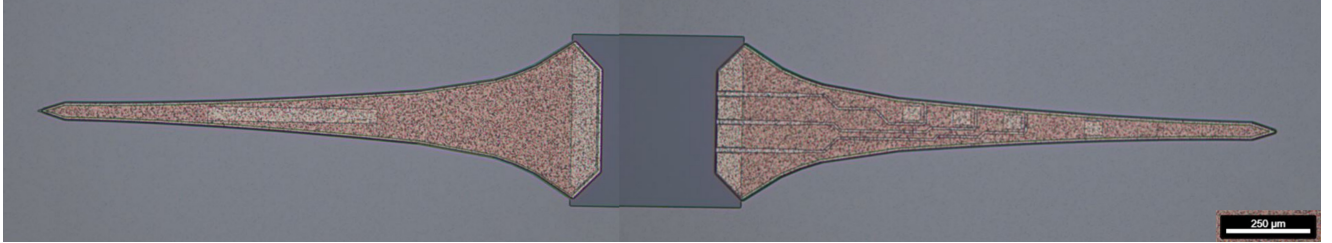
(c) Probe tip, full insulation of the Al shank can be observed (optic microscope)

Figure 3.11: (a) Image of the patterned SiO_2 layers that defines the standard design of the electrode. $20'000\ \mu\text{m}^2$ CE is present on left shank, while on the right there are $2000\ \mu\text{m}^2$ RE and WE. (b) WE on the probe shaft, dimensions are indicated. (c) Probe tip, with focus on shank encapsulation

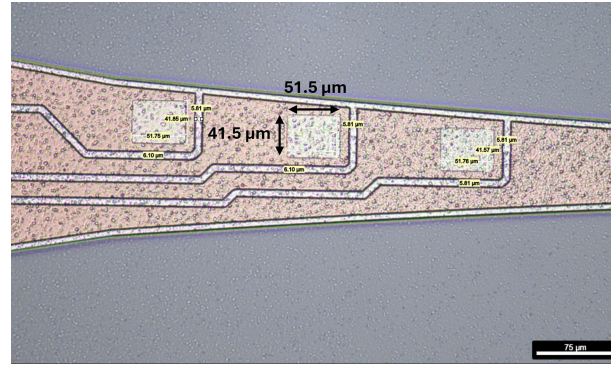
Multiple Electrodes Design

Similar considerations can be made for the design with multiple working electrodes, it should be noted, as it can be seen in fig. 3.12b, the increment in size of the WEs matches

the one seen in the standard design. This confirms a systematic error related to the fabrication process selected, but it also confirm an high repeatability of the electrodes patterning.



(a) Probe Multiple Electrodes Design (optic microscope)

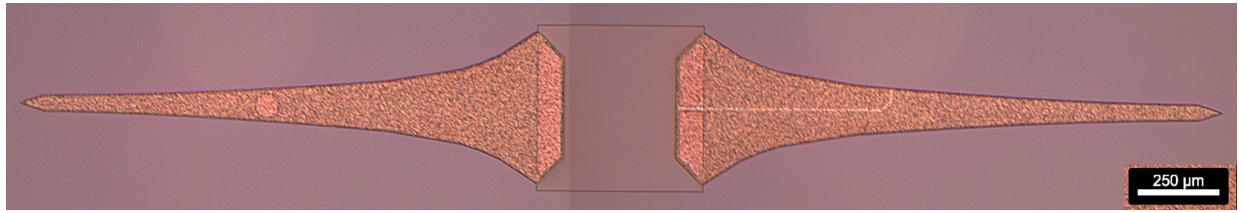


(b) Probe Multiple Working Electrodes (optic microscope)

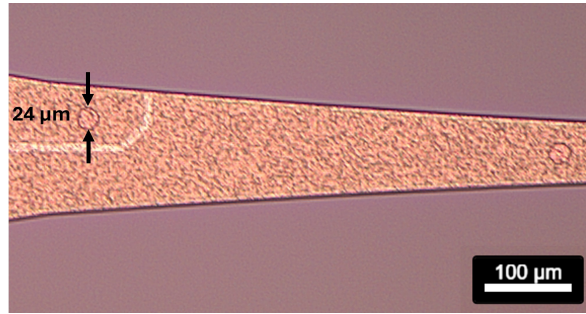
Figure 3.12: (a) Image of the patterned SiO_2 layers that defines the multiple electrodes design of the probe. Same sizes of WE, RE and CE of the standard design have been used (b) Three WE of the probe with their dimensions.

Small Electrodes Design

For what concerns the possibility of fabricating smaller electrodes, no limitation has been observed due to SiO_2 etching. Circular electrodes produced have a diameter of about $24 \mu\text{m}$, as shown in fig. 3.13b. This result was expected, considering the both the CD of the photoresist used [64] and the plasma based dry etching process selected to pattern the oxide [94]. The main limitation, as previously hinted, is related to the Pt layer. In fact, to obtain small WE and RE, positioned as close as possible to the tip of the shanks, it is necessary to reduce the trench width even further. Particular attention, then, will have to be posed on the presence of shorts circuits between tracks, related to improper Pt etching.



(a) Probe Small Electrodes Design (optic microscope)



(b) Probe Small Reference and Working Electrodes

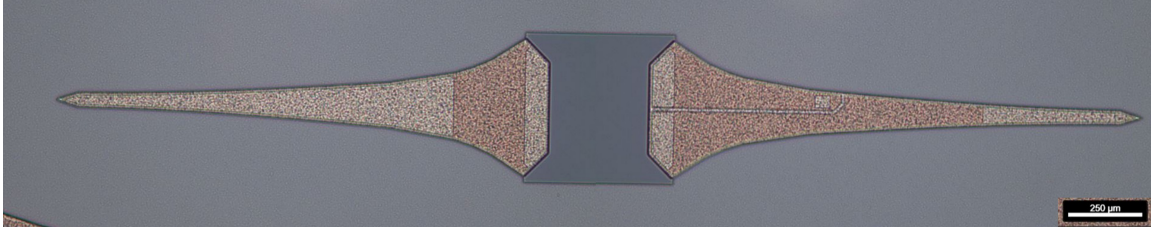
Figure 3.13: (a) Image of the patterned SiO_2 layers that defines the small electrodes design of the probe. On the left shank the $4000 \mu\text{m}^2$ CE can be observed, while on the right one $400 \mu\text{m}^2$ WE and RE are present. (b) Detail of RE and WE shank, with their diameter indicated.

Design for Functionalization

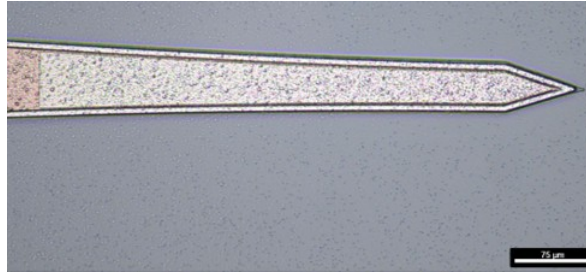
The last type of probes produced are the ones optimized for manual functionalization of the working electrode. In this case the whole shanks surfaces are exploited as electrodes. As anticipated in section 2.1.5 all the choices in the design were made with idea of making functionalization feasible. First of all the WE is close to the tip and sufficiently distanced from the reference one, so that drop casting a small drop of functionalization solution on top of it, without affecting the other, becomes possible. In addition having a sufficiently large area maximize the probability of functionalization, even by such a simple technique. The size and position of RE was not modified, since moving it closer to the central chip increase significantly the risk of accidentally covering its surface during insulation of the pads, as it will be discussed in section 3.3.2. Finally the size of the counter electrode was increased up to the largest possible for the probes in exam, this allows to keep a significant difference between the CE area and the WE one, despite the enlargement of the latter. It should be noted that one of the main characteristic to assess in the proposed design is the alignment of the insulation layer with the one underneath. In fact, in this case, even slight mismatches would expose *Al* layer together with *Pt* one, this should be avoided due to the high reactivity of *Al* in physiological and saline environments. It can be observed in fig. 3.14b that this requirement was met, since the exposed electrode (white) is fully

contained in the *Pt* track (orange).

Overall, the design is of interest for another reason: it shows the high versatility of the proposed fabrication process for the foldable probes. Especially considering that on the single wafer, all the designs shown could be produced simultaneously. However, to ensure a sufficient number of samples, it has been decided to fabricate up to 3 designs on each processed wafer.



(a) Probe Electrodes for Functionalization Design (optic microscope)



(b) Working Electrode for Functionalization (optic microscope)

Figure 3.14: (a) Image of the patterned SiO_2 layers that defines the electrodes optimized for functionalization. On the left shank the $110'000 \mu m^2$ CE is present, while on the right one there are the $2000 \mu m^2$ RE and the $20'000 \mu m^2$ WE. (b) WE on the shank tip.

3.1.6. Wafer Preparation to Backside Etching

Before being able to process the backside and to pattern the *Si* supports of the shanks and the central chip, many intermediate steps are required, as described in section 2.3. Here a brief summary of each one of them is provided, focusing on the parameters on which the attention must be focused to obtain optimal results.

- **Front-side Protection** $10 \mu m$ of protective polymer have been coated on the wafer front-side. Both *AZ P4K-AP* and *MC PC 62E*, after the first have been discontinued, have been used to this scope. To coat the wafer *SM-200*, (*Sawatec AG*, *Switzerland*) has been used. It is imperative to guarantee good adhesion between the resist and the substrate, so HMDS pretreatment has been performed.

- **Backside Grinding** The wafer has been grinded by *DAG810 (Disco Corporation, Japan)*, reducing its thickness until a final value of $230\ \mu\text{m}$ has been reached. Finally, to reduce internal stresses accumulated due to the mechanical process, $10\ \mu\text{m}$ of *Si* have been etched on *Rapier (STPS Technologies, United Kingdom)*, according to the recipe seen in section 2.3.1.
- **Front-side Protection Removal** Removal of protective resist has been performed by wet chemistry in *SVC-14*. To remove any residue of it $30\ \text{s}$ of O_2 plasma etch at high power have been also performed in *GIGAbatch (PVA TePla, Germany)*.
- **Hard Mask Deposition** $1\ \mu\text{m}$ of SiO_2 has been deposited on the wafer backside by *D250L PECVD (Corial, France)*.
- **Parylene Coating** To minimize risk of *Parylene-C* detachment, silanization has been performed, following the procedure described in section 2.3.3. Then $5\ \mu\text{m}$ of the polymer have been deposited in *C-30-S (Comelec SA, Switzerland)*. Visual inspection has been performed to ensure that no parylene detachment was present on the surface. Since in previous versions of the process flow this has been a major issue in the reliability of the fabrication, such inspection has been performed for each step until the final release. For simplicity it will not be reported in each one of them and it is sufficient to confirm that no parylene detachment has occurred during the subsequent processing, confirm the effectiveness of silanization.
- **Parylene Removal** *Parylene-C* has been removed from the wafer backside, by directional O_2 plasma in *PlasmaPro100 Cobra (Oxford Instruments, United Kingdom)*, until EPD was confirmed.
- **Backside Photolithography** $1\ \mu\text{m}$ of *AZ ECI 3007* has been coated and developed automatically on *ACS 200*. Particular attention should be given to the fact that backside alignment was required. However, since for the etching of the hard mask, no perfect matching of the features is mandatory, the details about alignment assessment will be explained in the next section.
- **Hard Mask Etching** SiO_2 has been etched by *APS* as for the previous oxide etching of the front-side.
- **PR Strip** To avoid damaging parylene layer, directional O_2 plasma recipe in *APS* has been used, assessing its removal by OES end point detector.

3.1.7. Back-side Silicon Etching

Etching *Si* on the backside is one of the most critical steps of the process in exam. There are three main requirements to take into account: aligning front-side features and backside ones during photolithography, defining a proper step height, performing deep *Si* until parylene layer is reached. Failing to perform accurately one of these steps could lead to the final failure of the probes themselves, so great care is required.

Features Alignment

Photolithography has been performed in *ACS 200*, by which the wafer back-side has been coated with $2\ \mu\text{m}$ of *AZ 10XT-20*. During exposure, backside alignment procedure, described in section 2.3.4, has been followed, then visual inspection of the actual alignment was done by *DM8000* (*Leica Microsystems, Germany*), an optic microscope equipped with IR lamp. The tool is able simultaneously operate in reflection mode, in the visible filed, thanks to its front-side lamp, and in transmission mode, in the near infra-red one. The wafer is placed on a borosilicate glass holder, with its front-side facing downwards. Near-IR light shines the wafer from the bottom, and is transmitted through *Si*. If materials that absorb wavelength in this range, such as metals, are present on the front-side, their shadow will be visible. At the same time the back-side of the wafer is irradiated with light in the visible range, so that also the features on this side can be observed. In particular in our case, this technique was used to asses the alignment of the deposited PR with the features already patterned on the front.

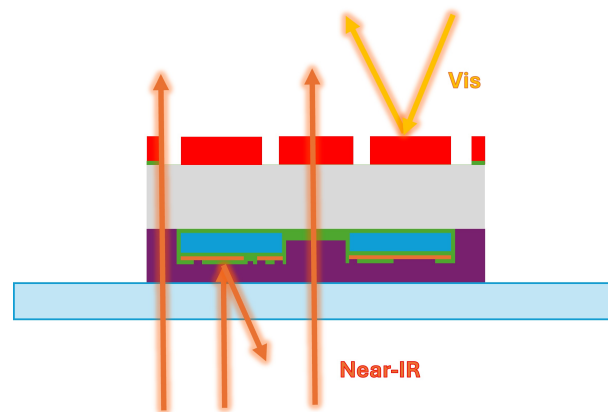


Figure 3.15: Scheme of the setup used to perform simultaneous visible (reflection mode) and IR (transmission mode) microscopy.

During sample inspection, there are two major parameters that can be regulated to highlight one of the two layers with respect to the other. The first one is the focus of the

microscope, in fact, the front sides are spaced by a few hundred of μm from each other, so the features present on them can not be in focus at the same time. The other parameter that can be modified is the relative intensities of visible and infrared lights.

So in general, when performing alignment assessment with this technique, one can keep the intensities of the two light sources fixed, while the lenses height is varied, as can be seen in fig. 3.16, in which the focus goes from the features on the wafer backside to the one on the front. This method is suitable when it is possible to find a ratio between intensities, that allows to obtained sharp images in both transmission and reflection mode. It has been observed that, increasing the magnification, leads to a partial lost in the transmissive IR signal, so higher intensity of it are required to be able to clearly distinguish features on the wafer front-side. The drawback of such increment is that it saturates the signal coming from reflected visible light, so the features on wafer backside are lost. Since in this second case it is difficult to visualize simultaneously both features with an acceptable accuracy, image superposition could be exploited, as shown in fig. 3.17. This is done between an image in which features on the back-side are in focus and one in which the other features are sharp.

One problem that one may have to consider is the calibration of the tool, in fact if it's not properly done, mechanically changes on the focus may result in lateral shift of the image, that would be detrimental for our scope. In order to verify if relevant shifts are present, one could use the microscope software to digitally apply rulers or reference lines on the live image, then changing the focus will reveal offset presence.

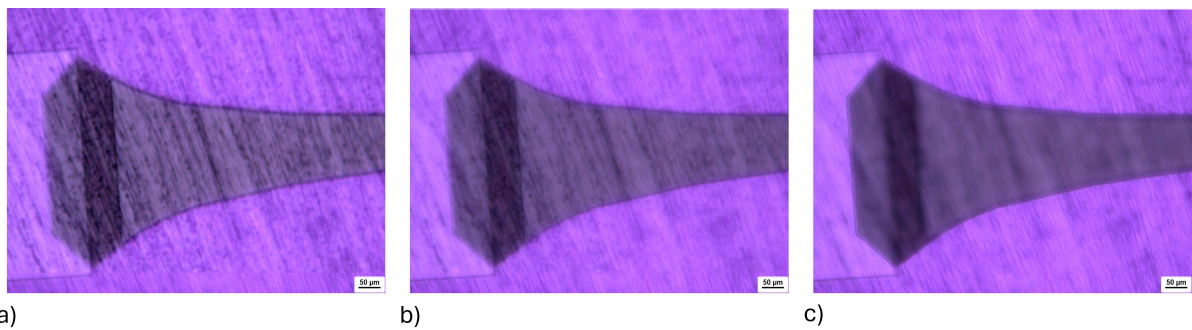


Figure 3.16: Alignment evaluation of probe's shank. Intensity ratio is kept fixed, while the plane of focus is changed. a) Focus on the features on wafer backside. c) Focus on the shank on the frontside. b) Superposition between a) and c), acceptable alignment is observed.

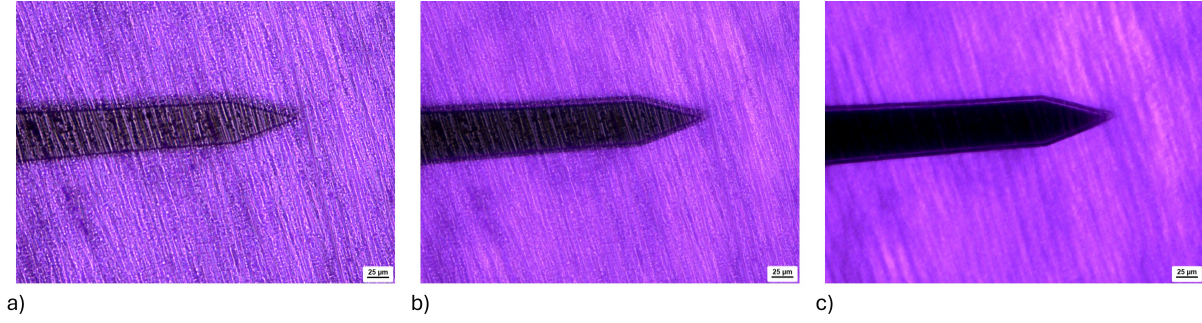


Figure 3.17: Alignment evaluation of the probes tip. Due to the high magnification is necessary to modify both focus and intensity, from a) optimize to view backside features to c) optimized to view backside features. b) Is given by superimposing a) and c).

It can be observed in fig. 3.16 that the central chip is well aligned with respect to the shank and, most importantly, the same can be said for backside and front-side shanks tips, as seen in fig. 3.17. This is crucial since misalignment between the two layers would cause a mismatch between the foldable shanks of the probes, that would lead to poor encapsulation of the device in SiO_2 protective layer. Moreover, severe misalignment may also cause problems during the shanks folding itself, due to unwanted hindrances.

Step Definition

Definition of *Si* step has been performed by *Rapier* (*STPS Technologies, United Kingdom*) through the Bosh process described in section 2.3.5. Descum was directly performed on the tool to remove any residue of photoresit that may have been present on exposed area of the wafer, this leads to a reduction in the polymer thickness of a few hundreds of nm. Then, as computed in section 2.3.5 42 loops are required to etch $30\ \mu\text{m}$ of *Si*, given the minimum trench width present on our features. It should be noted that etching rate may also vary between the center of the wafer and its edges. This could affect the subsequent deep *Si* etching step, in which parylene landing may not be reached simultaneously across the whole wafer. As a consequence, overetch of the probes that reach first the condition desired for release would occur. To ensure that all the shanks have a final thickness of at least $30\ \mu\text{m}$, the number of loops has been slightly increased, up to 45, so that the expected final step is of about $32.5\ \mu\text{m}$. No folding issues related to having slightly thicker *Si* supports is expected, due to large gap between the central chip and the shanks supports of about $74\ \mu\text{m}$.

Once the etching has been performed, evaluation of the actual etched step has been performed on *Dektak XT* mechanical profiler. In the central region of the wafer a step of about $35\ \mu\text{m}$ related to *Si* etching has been evaluated, starting from a measured value

of $36.8 \mu m$. This evaluation was done by considering the measured step height between the trenches and the top of the shanks, then the residual PR layer thickness has been removed. To compute the latter the following formula can be used [97]:

$$t_{final} = t_{initial} - v_{descum} \cdot time_{descum} - v_{etch} \cdot n_{loops}$$

So in the case of interest:

$$t_{final} = 2000 \text{ nm} - 10 \frac{\text{nm}}{\text{s}} \cdot 10 \text{ s} - 6 \frac{\text{nm}}{\text{loop}} \cdot 45 = 1630 \text{ nm}$$

Then, the etching rate of the process is slightly higher than expected, at least in the central region of the wafer; nevertheless the final step obtained is in a perfectly acceptable range, so the process can be carried on.

Deep Silicon Etching

The removal of the PR has been performed by the alternative, fully O_2 plasma based, procedure that has been described in section 2.3.5. *Pi_vertical* recipe on *APS* was used to performed the resist removal.

Then DRIE etching has been performed, once again, in *Rapier*, in this case no descum was required due to the absence of photoresist on the wafer backside. As it has been previously discussed, to asses correctly parylene landing, iteration is advised, in order to avoid excessive overetching. Ideally $190 \mu m$ should be etched, with an uncertainty of about $\pm 10 \mu m$. Using a conservative approach the minimum number of loops required to perform etching can be estimated by considering a residual thickness as low as possible and, on the contrary, the highest expected etching rate. So in this case $180 \mu m$ of *Si* are expected to be etched, at a rate of $780 \frac{\text{nm}}{\text{loop}}$, that is the etching speed measured during step definition. The rate is supposed to be constant, while in reality is expected to decrease as the depth of *Si* trenches becomes larger. The initial number of loops has then been set to 230, then visual inspection of the samples has been performed, under optic microscope. As long as *Si* layer is present on the bottom of the trenches, the light is reflected by it, while, as soon as parylene is exposed, a transparent layer is revealed. After the first deep *Si* etching, parylene landing was not reached in any point of the wafer, this was expected due to the conservative parameters that has been considered in the loops number evaluation. DRIE process was then iterated for a few loops at a time, until the great majority the samples was released from *Si*. After this step the probes are effectively suspended in the parylene layer.

3.1.8. Probes Release

Before proceeding with the final release of the probes, insulation layer on the wafer back-side has to be deposited. As discussed in section 2.3 it has been decided to use SiO_2 , so to obtain probes fully encapsulated in the oxide. However *D250L PECVD (Corial, France)* can not be used, since SiO_2 deposition recipes on it are performed at $320^\circ C$, a temperature not suitable for the *Parylene-C* protective layer on the wafer front-side. For this reason sputtering at room temperature, performed in *Spider 600*, has been used to deposit $500\text{ }\mu m$ of SiO_2 .

Then the wafer was bound to the carrier wafer, previously fabricated, by *Quick stick 135*, exploiting the main flats present on them to correctly align the two substrates.

PlasmaPro100 Cobra was used to perform both parylene and SiO_2 dry etching, respectively using O_2 and CF_4 chemistry. Complete Parylene removal has been assessed by exploiting both OES and laser end point detection systems, integrated in the tool. Moreover, 30 s of oxygen plasma overetch have been performed, so to strip any polymer residual from the wafer surface. Finally, visual inspection of the wafer frontside has been done, while keeping the sample in the tool loadlock. One of the advantages of using *PlasmaPro 100 Cobra* is that no further manipulation of the wafer has to be carried out. In fact, at this state, the probes are attached to the processing wafer just by a thin 500 nm SiO_2 layer, that could accidentally break due to vibrations and small impacts on the sample, resulting in an uncontrolled release. In the selected tool, instead, SiO_2 etching can be directly performed. To avoid an excessive overetch, that would damage the front side insulation layer of the probes, visual inspection through the camera integrated in the etcher, has been performed during the whole process. As soon as the fall of the probe visualized on camera was confirmed, the process has been interrupted after a few seconds of overetch. These few extra second were meant to guarantee a proper release on the whole wafer surface, due to the possible small differences in thickness and in etching rate between the center of the substrate and its edges.

The great majority of the samples has been released properly, and fell into the sockets of the carrier wafer vertically, no flipping or tilting has been observed; unlike previous version of the process, in which *Parylene-C* was used as backside insulator. An example of a released probe is depicted in fig. 3.18. Despite the accurate release of the samples, *Si* flakes have been also observed in the carriers, their presence is related to an issue that has occurred during deep *Si* etching and that will now be discussed.

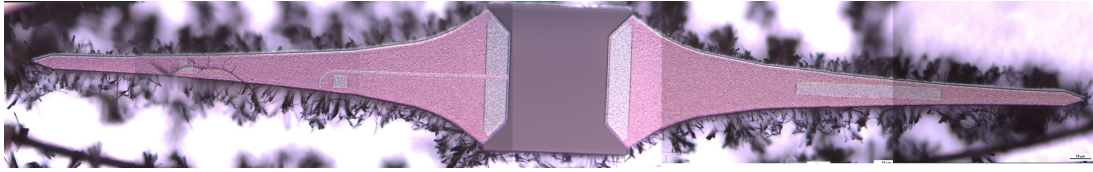
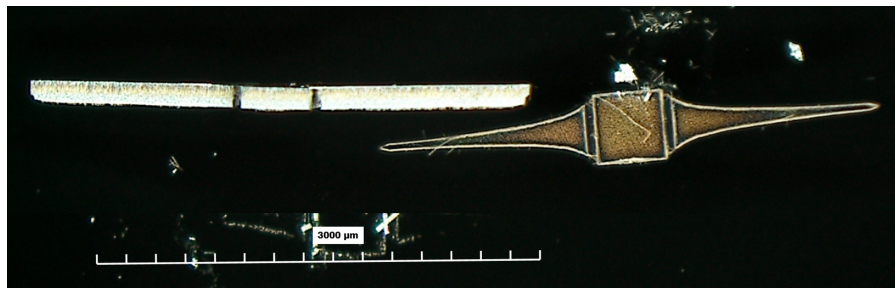


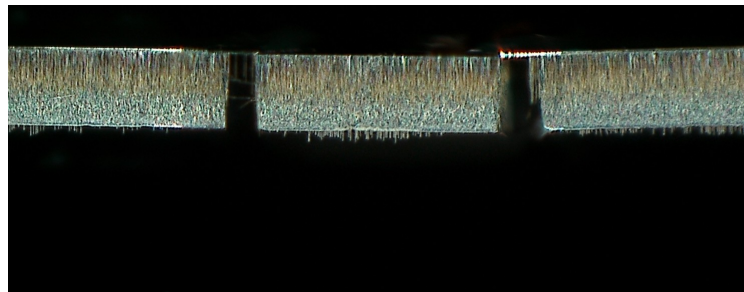
Figure 3.18: Released probe fallen into the socket of the carrier wafer. *Si* flakes can be observed.

3.1.9. Deep Silicon Etching Issue

During the etching of *Si*, steep walls were formed on the sidewalls of the features in exam. As one can observe in fig. 3.19 these walls have an height comparable to the one of the whole wafer after grinding, but are only limited to the contour of the *Si* supports and of the central chip. The features themselves have a final thickness of about $35\ \mu\text{m}$, as was expected from the process, while the walls have an approximate height of $150\ \mu\text{m}$, that is consistent with the thickness of the wafer after grinding, minus the step height. Additionally *Si* flakes observed in the cavities of the carrier wafer are composed of thin beams, of approximately the same height. This could denote a common origin of these phenomena.



(a) Probe Electrodes for Functionalization Design (optic microscope)



(b) Working Electrode for Functionalization (optic microscope)

Figure 3.19: (a) Side and bottom view of the samples released probes under optic microscope. (b) Detail of the probe sides; the apparent thickness of the probes, larger than shank-chip distance, can be observed.

To address a possible cause, *SEM* imaging has been used on a sample on which *Si* step definition and subsequent PR strip were already completed, but the final deep *Si* etching hadn't been performed yet. Residues of an undefined material have been found both on the features edges and in some of the asperities of the *Si* surface, caused by grinding process, as depicted in fig. 3.20.

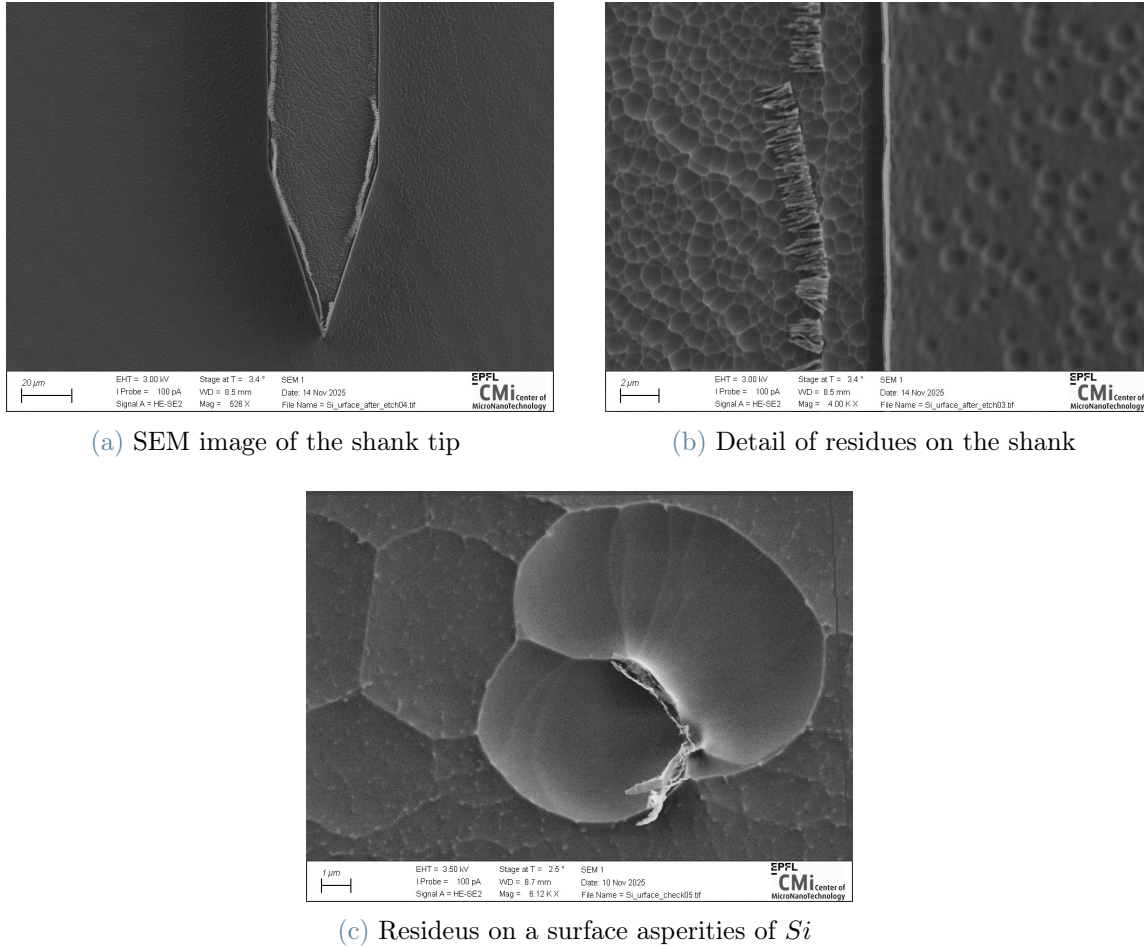


Figure 3.20: SEM images *Si* surface of the wafer backside. (a) Shank tip, on which sides polymer residuals are present, (b) a detail of the same region is shown. (c) Similar residues found on surface asperities

To identify the material present on the surface, some considerations can be made about SEM images seen. It can be seen that the material appears bright white on the electron microscope, this is the typical behavior dielectric materials. In fact, due to the accumulation of charges that occurs on their surface, their signal is over-saturated, making them appear much brighter than the surrounding metals and semiconductors. One major culprit is compatible with this analysis and could still be present on the backside surface:

the passivation layer used in the Bosh process to etch the *Si* step. In fact such layer is constituted by a highly fluoridated polymer, a class of materials known for their high chemical inertness. In bosh process itself they are typically removed by physical sputtering of accelerated SF_x ions. Ideally During *Si* etching, in a perfectly optimized cycle, no residuals on the trench sidewalls should be present, but if SF_6 step is short enough, some traces of the polymer could be left on the walls.

Such analysis is compatible also with the what can be observed in fig. 3.20a and in fig. 3.20b. In both pictures about $1.5\ \mu m$ of these walls appear to have detached from the sidewalls and to have fallen on its side, on top of the shanks. Such behavior would be compatible with a thin fluoropolymer, attached to PR sides, that have a residual thickness of about $1.5\ \mu m$, that fell once the resist was stripped. Accumulation of this passivation layer residues on *Si* asperities could also explain the silicon flakes that have been produced during DRIE process.

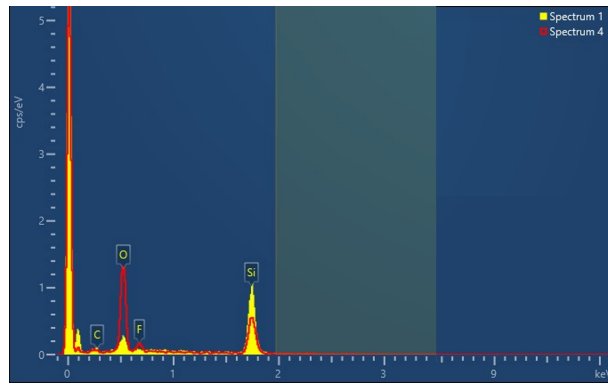


Figure 3.21: Comparison between *Si* spectrum (yellow) and the one (red) of the residues, that have been identified as CF_4 .

EDX analysis has also been performed to confirm this hypothesis, however x-ray spectroscopy on *Merlin SEM* is not optimized for light elements identification, so it's difficult to obtain strong and clear signals in this specific case. Nonetheless, some interesting considerations can be done by observing the comparison between bare *Si* spectrum and residues one, in fig. 3.21. A strong signal related to oxygen, is detected from the region on which residual material is present. This would imply for it to be an oxide, but this possibility can be excluded, since at no point in the process oxides have been deposited on the backside. The only exception is the SiO_2 hard mask, but its presence on *Si* sidewalls, that are defined after its complete removal, can not be explained. Moreover, absence of SiO_2 before performing *Si* step definition has been previously assessed with EDX analysis. A more plausible explanation is related to an erroneous identification of the element by the automatic system. In fact the characteristic energies of *C*, *O* and *F* are respectively:

0.277keV, 0.525keV and 0.677keV [115]. It should be reminded that the resolution of the detector is 127eV, that is comparable with the differences between the characteristic emission of these elements. In addition to it, at low energy, band broadening is common [118]. So it is reasonable to suppose that the system is misinterpreting two weak broad signals, related to a fluoropolymer with a single oxygen one.

To definitely prove this hypothesis, however, further tests should be performed. An example would be to use test wafers to perform the two subsequent DRIE process, so to evaluate if formation of steep walls is systematic and fine tuning of Bosh process is necessary.

3.1.10. Probes Folding

Despite the presence of steep *Si* walls, it was feasible to perform bending of the shanks. This was possible only after the manual removal of these residues from the edges of the central chips. This method is detrimental since it damages the *SiO₂* insulation layer present on the wafer backside, so the fabricated batch of released probes is not suitable for electrochemical testing after bending. However, the possibility of folding the probe's shanks is still a remarkable achievement, since it proves the feasibility of the process. In addition, it also ultimately confirms that, apart from these walls, the expected *Si* thickness of the shanks and central chip has been obtained.

To perform the folding, the guide and the lever seen in section 2.4.3 have been printed on *Photonic Professional GT+ (Nanoscribe, Germany)*. The guide was fixed on top of a *Si* dummy chip, for practical reasons. Then to perform folding, the probe was placed on top of the guide, with its frontside facing downwards. Then, the lever was used to apply a gentle pressure on the central chip, forcing an initial shanks bending at 45°. Finally, as the probe slid along the final portion of the guide, 90° folding angle was reached. The final released electrode can be seen in fig. 3.22.

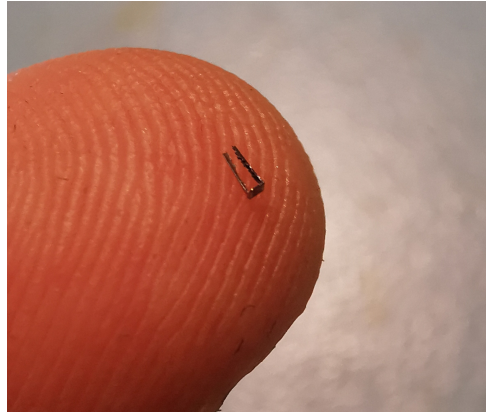


Figure 3.22: Comparison of the released and bent probe with human finger.

3.2. Electrical Testing

Up until now evaluation of the fabrication process, used to obtain the foldable electrodes in exam, have been discussed; this was crucial to identify possible criticalities as well as to address the key parameters in their production. At the same time, as hinted in section 3.1.4, it is also important to verify that the three electrodes produced on each sample are independent one with respect the others, i.e. no short circuits are present.

3.2.1. Testing at Probe Station

Direct electrical testing was performed on *TS150 (MPI Corporation, Taiwan)*, a probe station equipped with four independent terminals and a conductive chunk that can be used for grounding. The four terminals can be connected with the pads on the sample in exam through sharp tungsten carbide (WC) needles, whose position is controlled on the three spatial axis by manual micro-manipulators. Mechanical contact between needles and pads can be assessed thanks to the binocular digital camera equipped on the tool [119].

A wide variety of electrical measurements can be performed on the station, thanks to the two analyzer connected to it:

- *4155C Semiconductor Parameter Analyzer (Agilent Technologies, USA)*, used for DC characterization of devices under testing. The tool can work in range of $\pm 40\text{ V}$ and $\pm 100\text{ mA}$, with a resolution of $0.2\text{ }\mu\text{V}$ and 10 fA respectively.
- *Multi-Frequency Impedance Analyzer (MFIA) (Zürich Instruments, Switzerland)*, used instead for AC characterization, from DC up to 5 MHz . A DC bias up to $\pm 10\text{ V}$ can be applied, in a two probe configuration [119].

In the case in exam a two terminals configuration was used, as depicted in fig. 3.23, to perform impedance characterization between: WE-CE, WE-RE, RE-CE, so to asses the independence of the three from an electrical point of view. Moreover evaluation of the impedance of the *Pt* tracks, i.e. needles positioned on the same electrode, have been performed. This was done to confirm a proper connection between the exposed electrodes along the shanks and the testing pads on the central chip, but also as a reference, to be compared with the values measured between different electrodes.

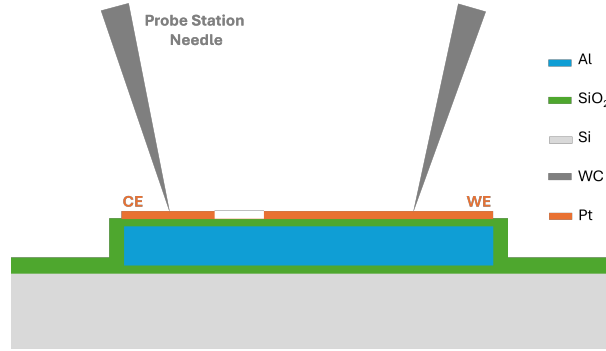


Figure 3.23: Scheme of the setup used to measure impedance between Working and Reference Electrodes (WE-RE). Analogous setups are used for all the other measurements.

Impedance was evaluated between 1 Hz and 1 MHz , 100 points have been considered according to a logarithmic distribution. To perform the characterization, MFIA from Zürich Instruments was used, considering the following measurement parameters: $R//C$ configuration, $V_{bias} = 0\text{ V}$, $V_{drive} = 300\text{ mV}$, LCR Impedance Measurement. Between these, it should be highlighted that the equivalent circuit, that describes in first order approximation the system in exam, is a resistance in parallel with a capacitance. This takes into account both resistive leakage currents that may flow through the insulation layer, but also the capacitive coupling between the metals that occurs at higher frequencies. The behavior that one should expect is describes in fig. 3.24, in which both impedance magnitude and phase of an ideal RC circuit are plot [120]. At low frequencies the impedance is dominated by resistive behavior, so it is almost constant in modulus and it has a zero phase. Then, as capacitance effect start be relevant, a phase shift from 0° to -90° is observed and the impedance magnitude decreases.

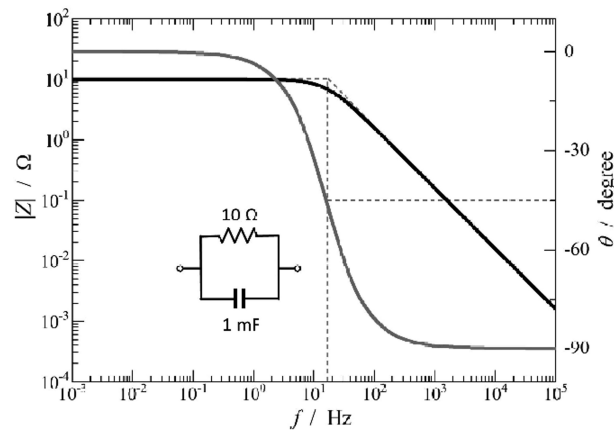


Figure 3.24: Bode plots representing impedance magnitude and phase over frequency of RC parallel circuit. Taken from [120].

In the model shown impedance is defined as:

$$Z = \frac{1}{\frac{1}{R} + j\omega C}$$

To characterize the devices produced, in principle, we would like to obtain impedance and phases, between different electrodes, that follows the behavior depicted above. At the same time, their impedance modulus should be many orders of magnitude higher than the internal one of the *Pt* tracks, so to confirm their insulation one with respect to the others.

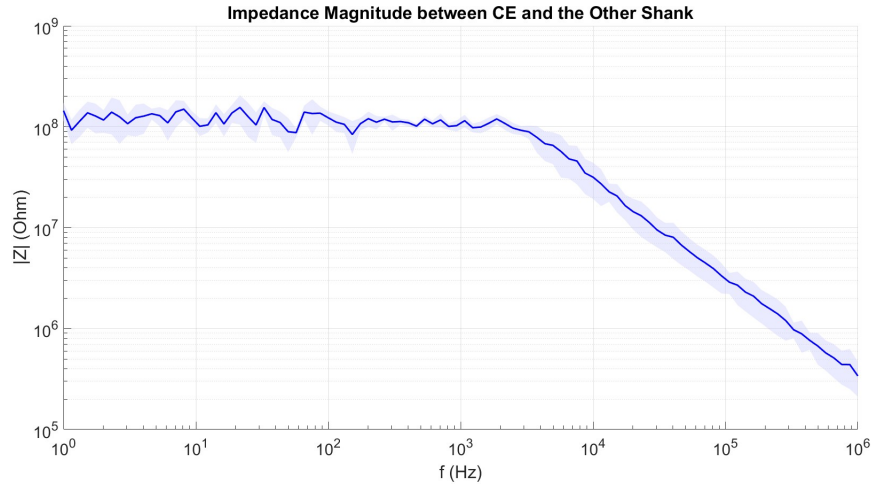
First of all the impedance between the counter electrode (CE) and working electrode WE, as well as the one between CE and reference electrode (RE) has been measured. The first is located on a different shank with respect with the other two, so the short circuiting between the two it's highly improbable. In fact, having characterized to different batch of samples, for a total of about 20 measurements, all the impedance measured had comparable values. In fig. 3.25 Bode plots of impedance magnitude and phase between CE and the other electrodes is shown, the plot shows the median value and the median absolute deviation (MAD) of the gathered data, This approach has been preferred with respect to arithmetic mean and standard deviation representation, due to the significant noise present on the measurements, especially at low frequencies. In fact median and MAD are more robust to outliers, while, at the same time, avoid the arbitrary discard of measured values. MAD is computed as follows:

$$MAD = median(|x_i - median(x)|)$$

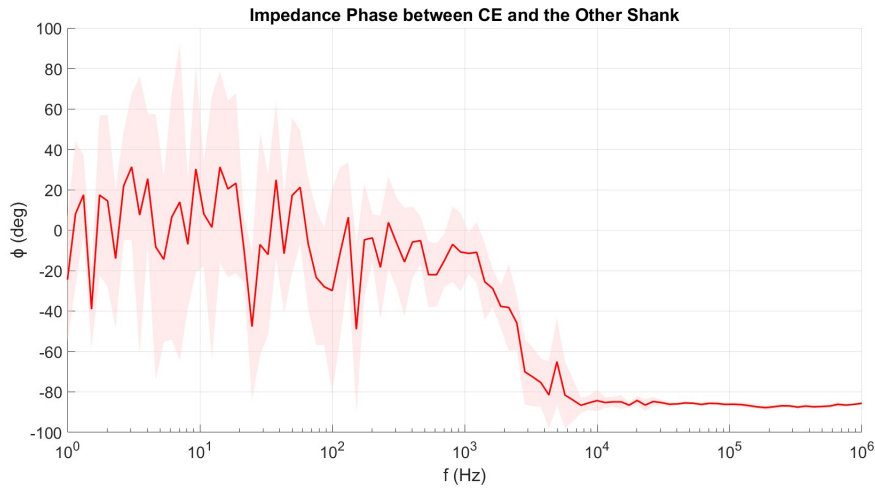
One of the most probable reasons the noise present in the gathered data is related to environmental vibrations, to which the system is sensitive to. In fact probe station and analyzers are located in a zone of the clean-room in which other instruments are present, in particular etchers and evaporators. The pumping systems required for their functioning produce significant vibrations, that are then transmitted to the probe station, since the latter is not positioned on an anti-vibration table. The problem affects, as can be observed in fig. 3.25b especially the signal phase at low frequencies, due to the large variations impressed to the small imaginary component of the impedance. As the value of the imaginary components grows in modulus, the effect of such vibrations almost disappears. Despite the noisy phase signals, some interesting considerations can be made:

1. At low frequencies an impedance of about $10^8 \Omega$ is obtained, this value seems basically independent on frequency, suggesting resistive behavior.

2. Cut-off frequency occurs around 3 kHz , then the magnitude starts to decrease. At the same frequency, also the phase shifts towards negative values, suggesting an increased relevance of the capacitive contribution.
3. For frequencies higher than 10 kHz of about -90° is observed, in agreement with the expected capacitive dominated behavior.



(a) Median Impedance Magnitude between CE and the Other Shank



(b) Median Impedance Phase between CE and the Other Shank

Figure 3.25: Bode plots of the median impedance between the counter electrode and the electrodes on the other shank, i.e. reference and working ones. (a) Impedance Magnitude (b) Impedance phase.

To better quantify the meaning of the values found, the curves have been compared with the ones originating from two reference conditions. The first one is the internal impedance of the Pt layer, that is supposed to be many orders of magnitude smaller than the one

discussed just now. This measurement was simply performed by positioning the two terminals on the exposed electrode and on its pad. The other reference measurement was done in open circuit condition, with the WC needles at a comparable distance with respect to the one used for actual measurements. This can help to identify the limits of the testing setup and compare the insulation level obtained with respect to an ideal open circuit condition. Fig. 3.26 shows that the impedance between CE and the other is comparable with the open circuit condition at low frequency, ensuring a optimal insulation of the *Pt* electrodes. The internal impedance of each electrode is in a range of few tens of Ω , proving the good conductivity of the metal layer together with the insulation effectiveness.

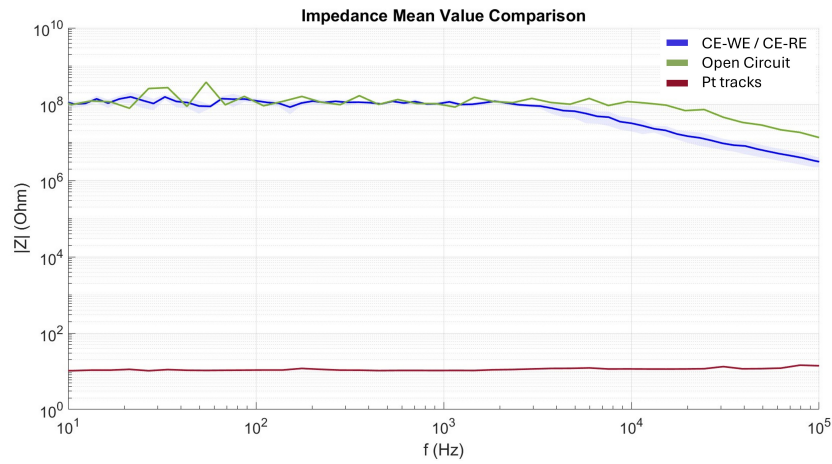


Figure 3.26: Median impedance magnitude shown in fig. 3.25a compared with open circuit condition and with the internal impedance of the *Pt* tracks.

The last impedance measurements that has to be done is the most critical: the absence of short circuits between RE and WE must be confirmed. In this case the two electrodes are located on the same shank, and are separated by $10\ \mu\text{m}$ trench, so they are much more prone to undesired connections, unlike the CE.

As shown in fig. 3.27, impedance modulus perfectly comparable with the one previously seen has been obtained, both in terms of numerical values and shape. The same has been observed for phases. The main difference resides in the number of short circuited samples. Going into the details, great difference in the process yield has been observed between the two analyzed batches. Out of about 20 samples tested per each batch, 85% of samples in one batch were functioning as expected, while the other had a success rate of only 35%. All failures were attributed to short circuiting, since the measured impedance values were in a range that goes from $100\ \Omega$ up to $10\ \text{k}\Omega$. To asses their presence and to have a better understanding on the reasons behind it, EDX analysis has been performed.

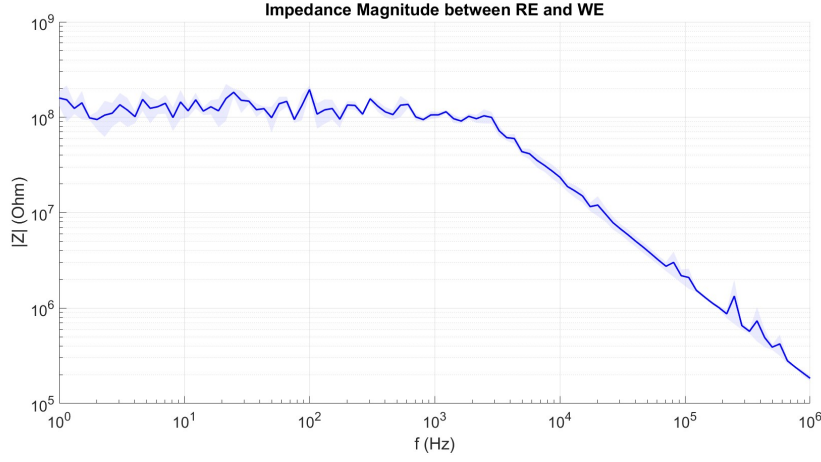


Figure 3.27: Median impedance magnitude shown in fig. 3.25a compared with open circuit condition and with the internal impedance of the *Pt* tracks.

3.2.2. Platinum Electrodes Inspection

In section 2.2.8 it has been discussed about the importance of performing photo-resist reflow, so to avoid *Pt* redeposition on its walls, that would lead to formation of steep fences once the polymer is removed. However, during *Pt* deposition and subsequent etching, some walls that can not be smoothed down are actually present on the wafer: the *Al* shanks on which the electrode are patterned. In an ideal situation, *Pt* redeposition on the shanks sides should not be an issue, due to the fact that the electrodes on top of the features are sufficiently distanced from its edges, to avoid connection with them. Nonetheless, in the batch that was mostly affected by the problem, it has been observed that a certain non-uniformity in the alignment of the *Pt* features, with respect to the underlying layers, was present. In particular, the probes in the central region of the wafer have been observed to have well aligned layers, while moving toward the external regions, *Pt* tracks were shifted to the point of overlapping with shanks edges. Such condition may have facilitated the short-circuiting between RE and WE, as shown in fig. 3.28.

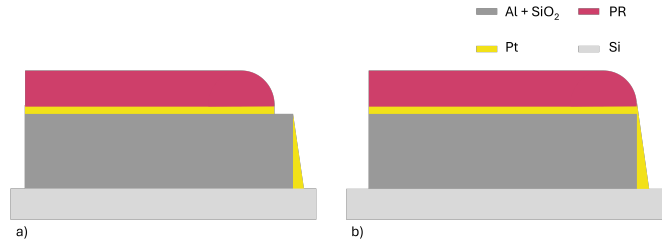


Figure 3.28: Scheme that illustrate the mechanism behind *Pt* tracks short circuiting, due to its redeposition along the shanks walls.

To demonstrate this hypothesis, EDX analysis was performed in *Merlin SEM*, the results are illustrated in fig. 3.29 and confirm the presence of platinum on the electrodes shanks.

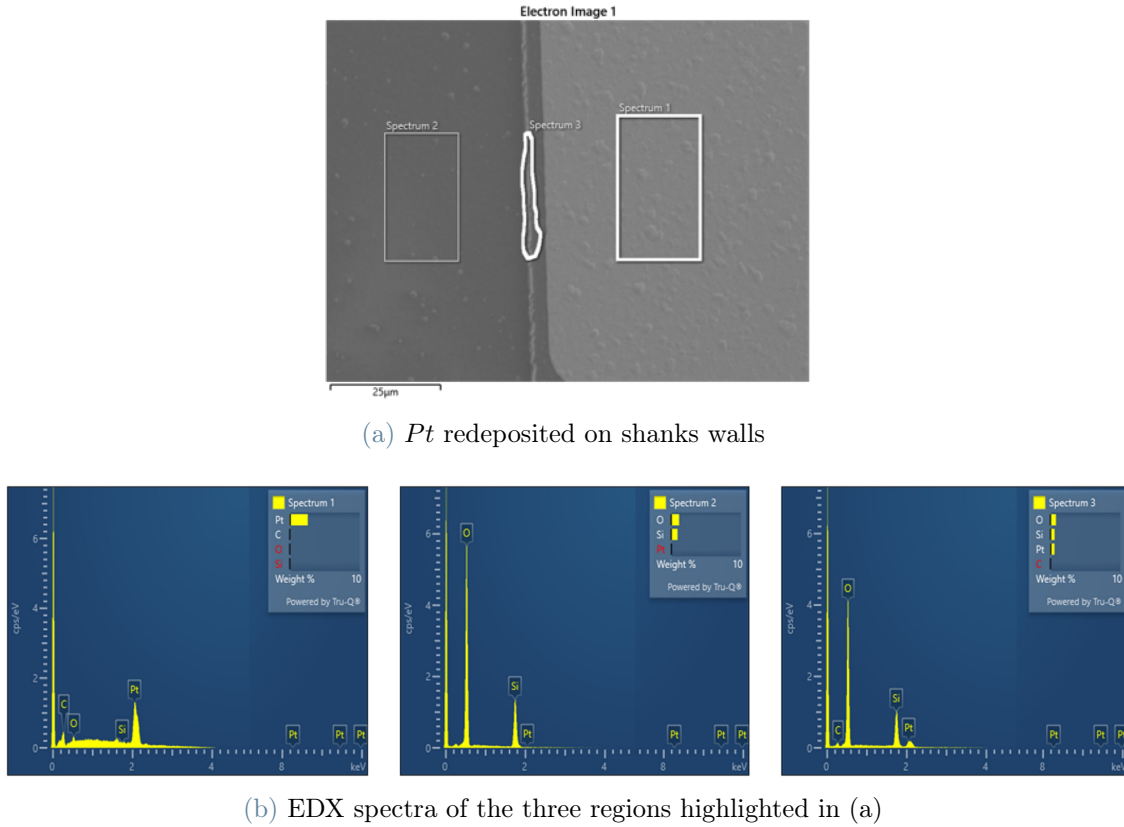


Figure 3.29: (a) SEM image that depicts the three inspected regions: *Pt* pad (spectrum 1), *SiO₂* central chip (spectrum 2), shank sidewall (spectrum 3). (b) Three spectra obtained in each region, in particular it is shown that non negligible *Pt* signal has been detected in Spectrum 3.

Platinum presence, combined with the unusual non-uniformity observed, explain the low yield of the second batch with respect to the first one. Moreover, the fact that not all the samples are equally shifted implies a certain distribution also on the thickness and uniformity of the accidental connections, this consideration is compatible with the wide range of impedance values measured on faulty samples. Retroactive identification of the causes that brought to the large inhomogeneity observed is not possible, however some hypotheses can be made. In fact, the two most probable possibilities are related to a non-uniformity in the deposition of the PR, that resulted in an uneven exposure of the pattern. Alternatively, it has been noticed that the wafer used as a substrate, had the highest bending value between the ones on which *Al* layer has been deposited. For the details regarding such bending consider section 3.1.1. A possible solution to remove the

risk of this kind of short-circuits would be to modify the process flow, in order to reverse the etching steps, i.e. depositing *Al*, *SiO₂* and *Pt* in sequence, to then perform etching of the three materials. This technique would allow to pattern platinum on a flat surface, removing entirely the risk of the observed redeposition. The main possible downside is related to the stress accumulation that may occur due to the stacking of multiple layers, without the release of it given by etching.

3.3. Electrochemical Characterization

After having assessed the effectiveness of the electrical insulation, together with the conductivity of the *Pt* tracks, one could move forward into the characterization of the fabricated electrodes, analyzing their behavior in solution. In the following section a brief introduction to electrochemistry will be provided, followed by a discussion about the technique that had been used for characterization: Electrochemical Impedance Spectroscopy (EIS). Setup configuration, testing parameters and results obtained will be discussed. This section has to be considered as the first step towards dopamine sensing, that the fabricated electrodes aim to achieve.

3.3.1. Introduction to Electrochemistry

Electrode-Electrolyte Interface

First of all, when performing electrochemical measurements, the presence of an electrolyte solution has to be considered, in fact electrical charges have to flow between the electrodes, passing through such medium. However, there is a key difference between metals and electrolytes, in fact, the first charge carriers are the electrons, while in the second this role is played by ions. This implies that at the solution-electrode interface a relationship between the two charge carriers type has to be present for current to flow. Two main classes of interfaces can be defined [61]:

- **Non-Faradaic Interface:** In this case the interaction occurs due to attractive and repulsive electrostatic forces between electrons and ions. Let's consider, for simplicity, a case in which a fixed potential is present on the surface of one electrode. Ions in solution with an opposite charge with respect to such potential will be attracted towards the electrode surface. Two regions can be distinguished the Stern layer, formed by the ions accumulated on the electrode, and a diffuse layer; such structure is called double-layer capacitance. Stern layer can be further divided into: Inner Helmholtz Plane (IHP) and Outer Helmholtz Plane (OHP). The first one is formed by ions specifically adsorbed on the electrode surface, while in the second

ions are accumulated to to electrostatic attraction, but no specific adsorption occurs. Diffuse region, instead, is defined as the one in which a different concentration of ions, with respect to the one in the bulk solution, is present.

- **Faradaic Interface:** If instead a red-ox species is present in solution, chemical reaction can cause direct transfer of electrons from the metal to the electrolyte, thanks to anions and cations production. Depending on the electrode material and on the solution used, such reaction could require consumption of material, that is usually undesired, or involve only species present in the electrolyte. A virtuous example of the second type of interaction is the one that occurs between platinum electrodes and dopamine. The molecule, in fact, can undergo a quasi-reversible oxidation at voltage between 0.2V and 0.4V. For this reason detection of the ionic current generated can be performed, without the necessity of functionalization of the *Pt* electrode surface.

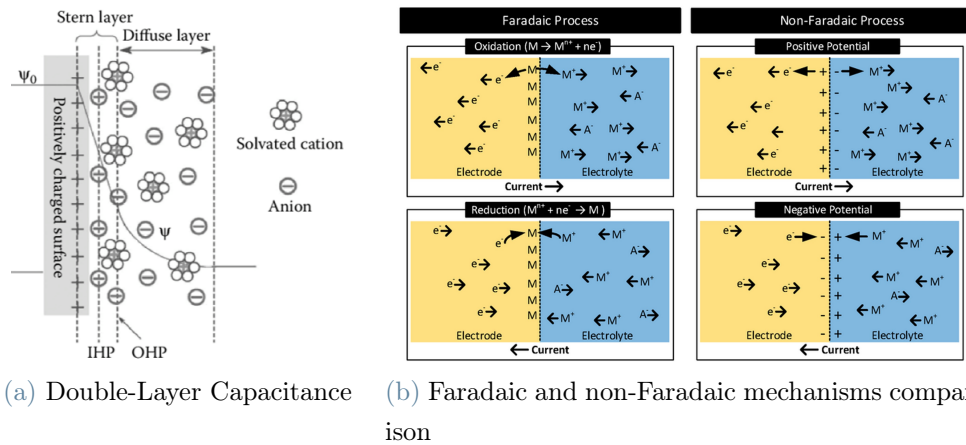


Figure 3.30: (a) Double layer capacitance scheme, IHP, OHP and diffuse layer are highlighted. From [121]. (b) Faradaic and Non-Faradaic mechanisms comparison, both for positively charge electrodes and for negatively charged ones. Taken from [122]

Electrochemical Sensing Instruments

The most commonly used configuration to measure electrochemical signals is the potentiostatic one, in which a voltage is imposed to the Counter Electrode and the current flowing through electrolytic solution into the Working Electrode is measured. Following this simple premise, multiple characterization and detection techniques can be performed. The three most relevant are [61]:

- **Chronoamperometry** Working electrode potential is kept fixed while current variation in time is measured. to perform sensing, it is possible to compare the measured

current values at different concentrations of the analyte in exam.

- **Cyclic Voltammetry** A periodic triangular signal is imposed, whose slope defines the scan rate of the measurement. The technique is usually performed to search for red-ox reactions, for which current over voltage plot present a characteristic double peak shape. Analyte identification can be performed thanks to the formal redox potential measurement, that is characteristic of each red-ox reaction and is defined as the average between the anodic peak potential and cathodic peak one.
- **Electrochemical Impedance Spectroscopy** A sinusoidal voltage is imposed, sweeping its frequency over a certain range. The measured impedance is strongly dependent, apart from the solution used, on interfacial properties of the electrode, such as surface roughness. Due to this reason, it's a suitable technique for the fabricated electrodes characterization.

Another important concept that has to be introduced, before discussing electrochemical measurements performed, is the role played by the three electrode configuration [61], that's also the basis of the design of foldable devices in exam.

Let's suppose to have a two electrode configuration, in this case a voltage difference between WE and CE is applied. Such drop can be decomposed in multiple contributions: the overpotential at CE-solution interface (ΔV_1), the ohmic drop due to solution ($i \cdot R_{sol}$) and the overpotential due to WE-solution ΔV_2 . All these values are current dependent, so it is not possible to experimentally separates their contribution. This implies that no precise control over the working electrode potential relative to solution can be obtained. Since, in principle, we would like to have such control, for example to impose the precise oxidation potential required by a red-ox species of interest, a different configuration is required.

A third electrode, called reference electrode (RE), is implemented and it's placed as close as possible to the WE, so to minimize resistance solution effects. In potentiostatic configuration, RE is connected to the inverting input of an Operational Amplifier (OpAmp), while the counter is connected to its output. Since RE is connected to an ideally infinite impedance, essentially no current flows through it, ensuring potential stability. At the same time a negative feedback loop corrects the value of CE potential, so that the difference between the working electrode and the reference electrode potentials remains equal to the target value. In this way accurate control of the WE potential relative to the solution is achieved. Finally it should be noted that some characteristic of the reference electrode are required to have stable and reproducible control. In particular the electrode has to be: stable in potential, both over temperature and in time, and not polarizable, so the passing current should not affect its potential. In order to achieve such stability RE

have to be based on reversible red-ox couples. A perfect example, that was used also used for the characterization of the fabricated electrodes, is the $Ag/AgCl$ reference electrode. Before proceeding with experimental setup description, one last consideration has to be done. The three electrodes that are present on the fabricated foldable device are all made of the same material, including the one whose final purpose will be to act as RE during dopamine sensing. However one may notice that Pt do not satisfy all the requirements stated above, for this reach it should be more actually referred to as pseudo-reference electrode. Nonetheless, having three Pt electrodes is still a common practice in micro-fabricated devices [23], due to the simplicity of fabrication, combined with the material chemical stability and bio-compatibility.

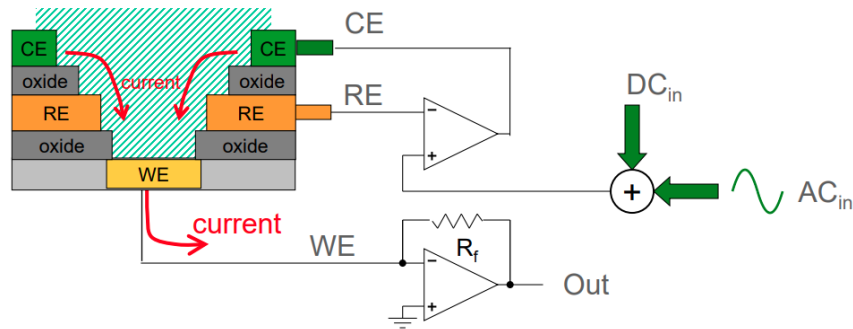


Figure 3.31: Three electrodes configuration scheme of a potentiostat. Gentle concession of prof. Carminati (Dipartimento di Elettronica, Informazione e Bioingegneria, PoliMi).

3.3.2. Sample Preparation

In order to test the micro-fabricated electrodes in solution the following approach has been followed to prepare the samples:

1. Samples fabrication was interrupted at the end of the front-side fabrication, i.e. at of the step discussed in section 2.2.9;
2. Wafer was diced, so to obtain small chips, on each a single device is present;
3. Placement of the samples on Printed Circuit Board (PCB) designed ad-hoc;
4. Wire bonding of the electrodes pads to the ones of the PCB;
5. Insulation of the wires and the exposed areas of the chip, such as Al exposed due to dicing;
6. Pin headers soldering to the PCB vias, so to allow connection to the potentiostat

used for measurement.

Printed Circuit Board

First of all the PCB to be used for testing had to be designed and produced. In order to do the first, *Altium Designer* (*Altium Limited, USA*) was used, a software package for PCBs design, from the schematic to the final layout, even offering the possibilities of performing simulations and analysis [123].

For the scope of interest a simple PCB constituted only by tracks and pads for electrical connection is required, the main parameters that has to be taken into account are the reduced dimensions and high proximity of the pads, that is required for a feasible wire bond connection. The elongated shape of the board has also to be considered; so that submersion of the PCB into the electrolyte can occur safely, without any risk of wetting for the external electrical connections. The final result of such constrictions is depicted in fig. 3.32, the board was then commissioned to *Eurocircuits N.V. (Belgium)* for its fabrication.

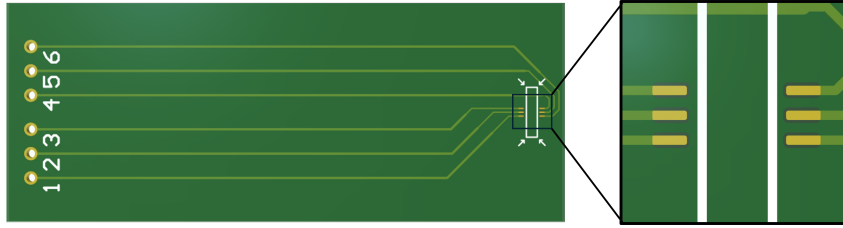


Figure 3.32: Designed PCB render, a detail of the pads for wire bonding is highlighted.

For a better matching with the constrictions imposed by the factory, the unit of measurement used during design was *mil*, i.e. one-thousandth of an inch, in SI units it is equivalent to $25.4 \mu\text{m}$. Each pad for wire bonding has a size of $6 \cdot 20 \text{ mil}^2$ and is distanced by its neighbors by 10 mil . Six pads in total are disposed on two rows, separated by a 64 mil gap, that is large enough to accommodate the small chips containing the samples to characterize. The number of pads was set to 6 so that the board is compatible for testing both the standard three electrodes samples and the multiple WEs ones. Finally vias, for pin headers connection, were based on factory datasheet of the latter.

Small Chips Fabrication

Before the actual wire bonding of the samples to the fabricated PCBs, dicing of the chip itself has to be performed. This was done starting from a wafer, whose production is identical to the one described for the released probes, with the exception that the process is interrupted after front-side SiO_2 patterning. Then, the front-side is coated

with the same protective layer used before grinding: *MC PC 62E*. More precisely 10 μm of the polymer were deposited by *SM-200*, (*Sawatec AG, Switzerland*) manual coater. In this case the protective layer is necessary, so that the particles that are released during mechanical *Si* dicing, performed in *DAD321* (*Disco Corporation, Japan*) [124], do not damage the features present on the wafer front-side.

The chips obtainment were then cleaned from the resin by manual immersion in Acetone, IPA and DI water rinsing, a standard not aggressive procedure for organic materials removal. The following immersion and rinsing times have been used:

$$t_{acetone} = 10 \text{ min} + t_{IPA} = 10 \text{ min} + t_{DIrinse} = 1 \text{ min}$$

Wire Bonding

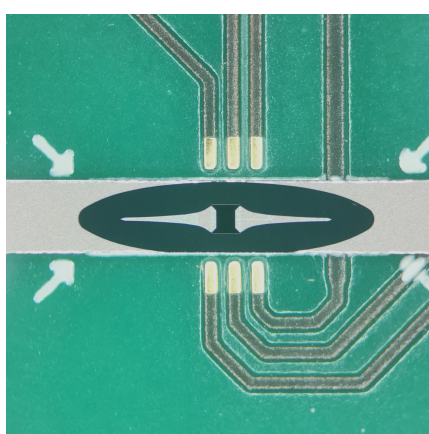
First of all chips have been positioned in the designated area of the PCB, that, for simplicity of alignment, has been highlighted by a rectangle and four arrows, printed on the board itself. In order to bond *Si* chip with the board, *H70E* (*Epoxy Technology, USA*) has been used, a bi-component eclectically insulating epoxy, designed for this specific purpose. After mixing the two components, considering a 1 : 1 weight ratio, a drop of the compound has been placed, using a small needle, at the center of the rectangle present on PCB. Then the chip has been position on top of the epoxy drop and aligned, as shown in fig. 3.33a. In order to facilitate the visualization of manual positioning a binocular microscope, *SMZ-1* (*Nikon Corporation, Japan*), has been used. The epoxy won't solidify properly unless it is cured at high temperature, according to the datasheet, it has been decided to bake the samples at 125°C for 15 *min*. This temperature is not high enough to damage neither the chips nor the PCB, but it ensures a strong connection in a reasonable curing time [125].

Afterwards, wire bonding has been performed by *5630i* (*F&S Bondtec, Austria*), an automatic bonder that exploits ultrasound vibration and pressure application to weld *Au* and *Al* wires on small chip pads. Wires of both materials have been successfully tested for bonding with the samples in exam, however final electrochemical tests have been performed with *Au* wire-bonded samples, due to its lower resistivity. Multiple parameters should be considered to obtain successful bonding, in particular one should regulate bonding time, force and ultra-sound power [126]. In fact, these parameter have to be high enough so that correct welding of the wire can occur, but at the same time should not be so high to damage the layers of the micro-fabricated samples. In our specific case the parameters in table 3.1 have been used, for *Au* wires. The last parameter that has to be checked is the loop hight, i.e. the height reached by the wire during the connection between one pad and the other. This value has be high enough to avoid undesired con-

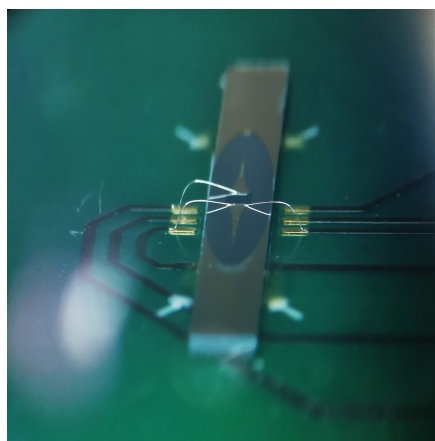
tact between wires and other regions of the sample. A correct bonding can be observed in fig. 3.33b. After bonding of the sample has been completed, visual inspection of the result can be made both on the digital camera installed on *5630i* and on *SMZ-1* microscope.

Location	Bond Time	US Power	Force
PCB Pad	35 <i>ms</i>	70 <i>digits</i>	35 <i>grams</i>
Sample Pad	35 <i>ms</i>	70 <i>digits</i>	35 <i>grams</i>

Table 3.1: Parameters used to weld $25\mu\text{m}$ *Au* wires on PCB and sample pads.



(a) Sample positioned on the PCB



(b) Successful Wire Bonding with *Al* Wires

Figure 3.33: (a) Sample is positioned in the center of the area designated by the rectangle on the PCB (b) Successful wire bonding of the sample through *Al* wires.

Sample Insulation

Despite the full insulation of SiO_2 that covers the micro-fabricated device, the samples can not be submerged in electrolytic solution as they are. In fact multiple exposed metals are still present: the *Pt* pads on the region of the foldable device, used for wires connection, the wires themselves, the *Au* pads of the PCB and finally the exposed *Al* on the chip edges. The insulation of the latter is especially important, due to the high chemical reactivity of the metal in the solution used for electrochemical testing: Phosphate Buffered Saline (PBS) solution, commonly used in biological research. *Al* dissolution in PBS not only is detrimental due to solution contamination, but it can also cause a sudden release of the internal stresses, inducing cracks in the SiO_2 layer, ultimately resulting in catastrophic failure of the device.

In order to prevent this occurrence, *H70E-2* (Epoxy Technology, USA) was used, an analogous version of the insulating epoxy previously considered, optimized for glob-top chip protection [127]. In this case the epoxy has to be placed into a syringe, connected to a pump, in order to obtain a precisely controlled dispense. Samples have been positioned on a hot pate at about 80°C , in order to facilitate the flow of the viscous epoxy on the chip to protect. *H70E2* drops have been dispensed in proximity of PCB pads and wires, the drops tend to maintain an hemispherical shape on the sample surface, so the flow can be controlled by carefully spreading the epoxy with the syringe tip. The most critical step is the insulation of the pads present on the sample, since the epoxy must not cover RE, WE or CE. In addition all the sides of the chip, both internally and externally, are insulated, so to avoid *Al* exposure to the solution. Finally wires have to be completely incorporated by the epoxy. Baking temperature and times are analogous to the one seen for *H70E*. Once the curing has been completed, if exposed areas are still present, it is possible to perform a second application.

One last consideration is that, the absence of damage on the electrodes shanks after electrochemical testing, once a proper insulation of the chip sides has been performed, confirms the effectiveness of SiO_2 layer in the insulation of the *Al* shanks.

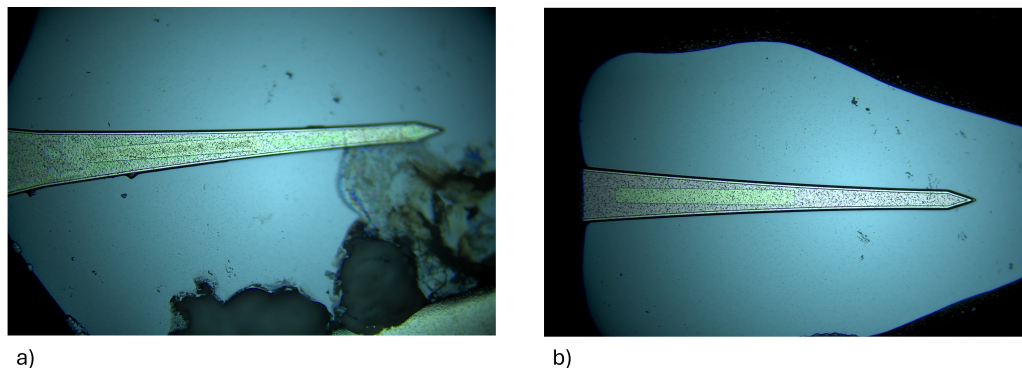


Figure 3.34: Comparison between CEs after electrochemical testing in PBS 10x, in case of a) poor insulation of *Al* on chip sides and b) full insulation. No damage has been observed in the second case.

3.3.3. Electrochemical Impedance Spectroscopy

As previously stated in section 3.3.1, Electrochemical Impedance Spectroscopy was chosen to characterize the fabricated electrodes in solution. The three electrodes of each sample have been characterized separately, exploiting them as working electrodes in the measurement setup. A *Pt* wire was used as counter electrode, while reference electrode of choice has been a standard *Ag/AgCl* RE. To avoid confusion, from now on, the characterized

electrodes will not be defined for the role that they are meant to have in the final device (WE, RE and CE), but simply for their geometrical area, and has to be always considered as working electrodes in this section.

Experimental Setup

1x PBS solution has been prepared, the following concentrations are expected: $NaCl$: 137 mM, KCl : 2.7 mM, Na_2HPO_4 : 10 mM, KH_2PO_4 : 1.8 mM [128]. Buffer solution has been poured in a beaker, while the samples has been submerged in it, after having it clamped so to be able to regulate its height with respect to the solution level. The same approach has been used to submerge in solution the Pt wire and the $Ag/AgCl$ reference electrode. Reference electrode has been placed as close as possible to the sample, avoiding contact between the two. CE instead has been fully submerged, to maximize the surface of the wire in contact with the solution.

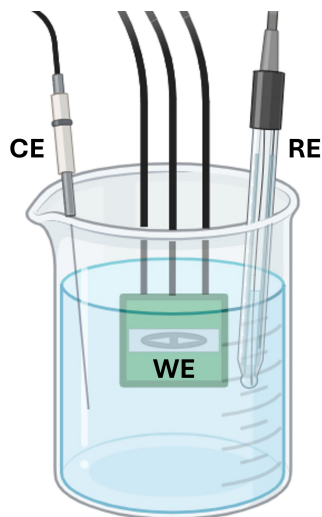


Figure 3.35: Scheme of the experimental setup used to perform EIS analysis. The three connections of the WE are related to each one of the Pt electrodes present on the sample. But it should be noted that their characterization occurred once at a time. (Image obtained with BioRender).

The three electrodes (sample, $Ag/AgCl$ RE and Pt CE) were connected to *Autolab PG-STAT302N* (Metrohm, Switzerland) a high current potentiostat/galvanostat with a bandwidth of 1 MHz [129], that has been used for impedance measurements. To control the system, *NOVA* (Metrohm, Switzerland) has been used, the dedicated software for the operation of the tool. The following parameters have been imposed:

- Potentiostatic mode;

- Highest current range of $10\ \mu A$, lowest current range $10\ nA$;
- Root mean square voltage of $10\ mV$;
- Frequency range from $0.1\ Hz$ to $100\ kHz$;
- Points measured per decade: 10.

After the characterization of each one of its electrodes, the sample was removed from the solution, rinsed with DI water and dried by N_2 gun. The same procedure has been followed for each sample that has been analyzed.

Measurements and Discussion

First of all it has been decided to characterize the $2000\ \mu m^2$ electrodes present on the foldable shanks of the device. According to the parameters set above, it has been found that the impedance magnitude varies in a range that goes from $10^9\ \Omega$, at $0.1\ Hz$, to $10^5\ \Omega$ at $100\ kHz$. This is shown in fig. 3.36a, that represents the mean value of impedance over the tested samples; while, the shaded area represents the standard deviation. Unlike previous electrical spectroscopies, in which the main noise source was introduced by mechanical vibrations, in this case using mean value and MAD has not been observed to bring significant advantages to the signal representation. An interesting consideration is that, at very low frequencies and at high frequencies, apart from a non negligible standard deviation of the samples, the signal obtained does not present strong noise. However, in the range of frequency that goes between $1\ Hz$ to $100\ Hz$, strong noise are present both in magnitude and especially in phase. This is the region in which the impedance passes from being resistive dominated $\phi \approx -20^\circ$, to capacitive dominated $\phi \approx -70^\circ$ to -80° .

Establish the exact reason behind this behavior is not trivial, since multiple factors could have brought to such behavior, that may be related to the sample itself, the setup used to perform the measurement or internal parameters of the tool. Nonetheless some interesting considerations can still be made, despite the noisy signals obtained.

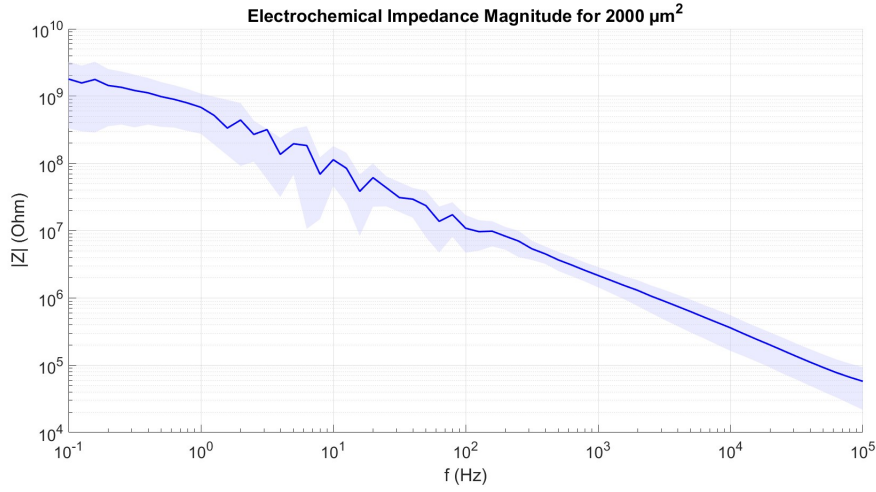
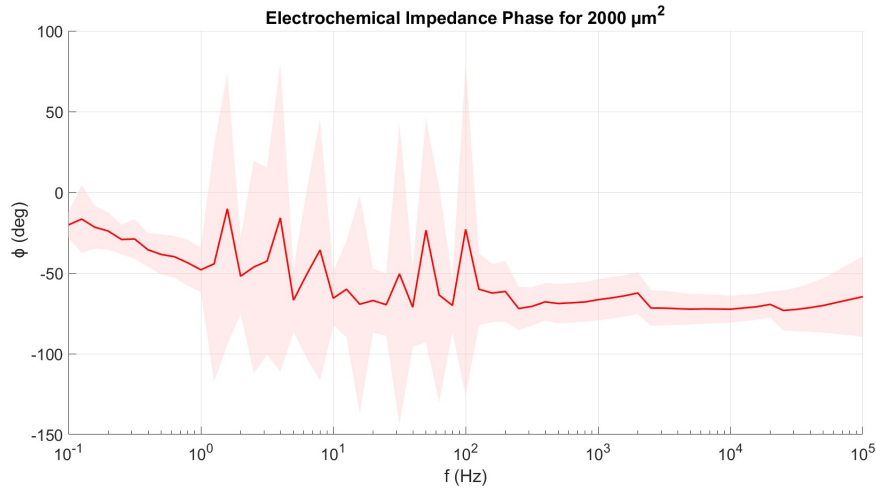
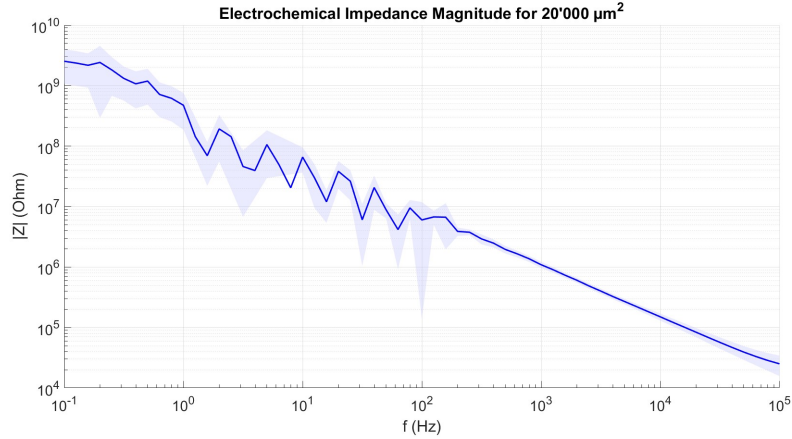
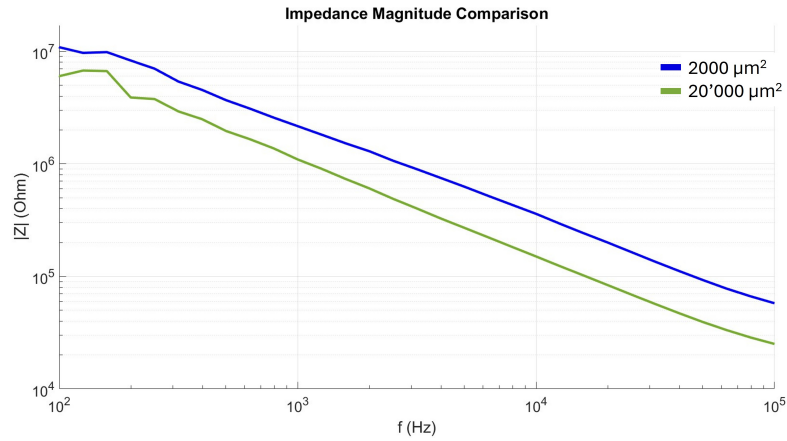
(a) Electrochemical Impedance Magnitude $2000\mu m^2$ Electrodes(b) Electrochemical Impedance Phase $2000\mu m^2$ Electrodes

Figure 3.36: Bode plots of the mean impedance of the electrode-electrolyte system. (a) Impedance Magnitude (b) Impedance phase.

If one considers the impedance spectra of the $20'000 \mu m^2$, the same noisy behavior is observed, as shown in fig. 3.37a. Due to such significant noise value, comparing the impedance moduli of the $2000 \mu m^2$ and the one of the $20'000 \mu m^2$ on the whole frequency range is not reliable. However, if one instead considers only the values for which more stable results have been obtained, i.e. above 100 Hz , the comparison between the two curves can be performed. In fig. 3.37b it is possible to observe that, as expected, to larger areas corresponds lower impedance magnitudes,

(a) Electrochemical Impedance Magnitude 20'000 μm^2 Electrodes

(b) Comparison between Electrochemical Impedances

Figure 3.37: (a) Electrochemical impedance magnitude of 20000 μm^2 electrodes. (b) Comparison between 20000 μm^2 electrodes impedance and the 2000 μm^2 one, between 100 Hz and 100'000 Hz.

For completeness a comparison between the measured impedance values for 2000 μm^2 fabricated electrodes and values reported in literature [130] is provided. The data provided are referred to circular *Pt* micro-electrodes, in PBS 1x solution. It can be seen the fabricated electrodes apparently have an impedance closer to the one of 300 μm^2 circular electrodes, than to the one of the electrodes with the same area. However, quantitative comparison between the reported data is not trivial. In fact the setup used may affect significantly the results, since the values reported were retrieved from measurements directly on-chip, while in our case a completely different approach has been used. Comparison with typical curves for similar electrodes, in the same conditions, is still useful from a qualitative point of view. In fact it can be verified that the impedance measured is in the range expected and its almost linear behavior it's also consistent with literature.

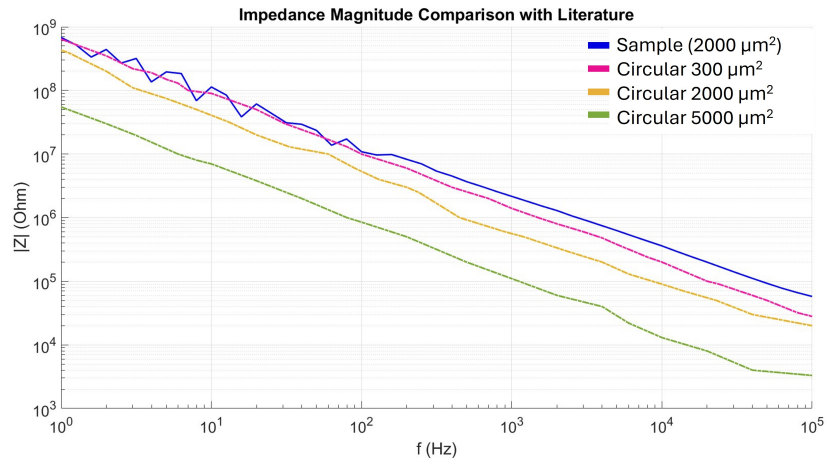


Figure 3.38: Comparison between impedance of 2000 μm^2 fabricated electrodes and circular *Pt* electrodes reported in literature [130].

Conclusions and Future Developments

During the course of this thesis I've discussed about the increasing relevance of neural implants, both in biology and in medicine, offering an overview on the main typologies of probes that have been developed through the years. An introduction to the context in which this project has been developed was also provided, presenting the idea of CMOS compatible foldable electrodes for cortical implantation.

Considerable modifications and optimizations have been implemented on the fabrication process, aimed to accommodate the multi-layer design required for embedding two or more electrodes on the device shanks. The feasibility in electrodes production have been successfully assessed by performing the full fabrication process, from bare substrate to the released probes. Eventual criticalities have been addressed and justified, also proposing solutions for further improvements in the design.

Moreover, electrical characterization on small flat chip has been performed, ensuring that insulation is achieved by SiO_2 deposition, and the possibility of embedding multiple independent channels on each shank. Finally, preliminary electrochemical characterization has been performed, showing a behavior qualitatively in accordance to what is expected for analogous electrodes of the same size.

Despite the encouraging results that have been obtained by this thesis project and by previous work on the topic, there is still a wide variety of studies that should be performed to have full assessment on the potentialities offered by this approach. Here a list on the most important steps towards the production of the final devices.

- **Resolution of issue on DRIE of Si.** Prevention into the formation of steep walls during Si backside etching is to be considered a priority. It is crucial to determine if this unforeseen problem has been caused by the modifications in previous steps of the fabrication process or by changes in operation parameters of the tool used.
- **Yield Improvement.** As seen, a considerable discrepancy between yields of the two batches analyzed under probe station has been observed. An alternative process

flow has been proposed and could be tested to significantly improved repeatability in the fabrication. Otherwise, fine tuning of the design and process parameters might be sufficient to reduce the possibility to incur in the issue described in section 3.2.2.

- **Released Probes Testing.** Electrochemical characterization of the probes should be also performed for the final released device. In order to do so a methodology to test these unique samples has to be developed.
- **Dopamine Sensing.** Up until now only preliminary electrochemical impedance measurements have been performed. However to fully characterize the electrodes fabricated, dopamine sensing, exclusively exploiting them, has to be performed. Once successful measurements will be obtained, the possibility of exploring sensing of other clinical relevant molecules can be explored.
- **Life Cycle Assessment.** The functioning of the devices in chronic implant has to be verified. A possibility is to perform accelerated aging tests on the electrodes, so to ensure their functioning after a long term implantation. One of the most critical aspect is the preservation of the SiO_2 insulation layer, in the brain tissue environment. It's degradation, in fact, could lead to premature failure of the devices
- **Full CMOS Integration.** Up until now fabrication of micro-electrodes on dummy wafers has been proven. The final step would be to definitively demonstrate their compatibility with CMOS technology, in a system that directly embeds circuitry in the central chip of the probes.

Bibliography

- [1] National Research Council (US) Committee on Research Opportunities in Biology. *Opportunities in Biology*. National Academies Press, Washington, DC, 1989. PMID: 25032449.
- [2] Kensall D. Wise, Amir M. Sodagar, Ying Yao, Mayurachat Ning Gulari, Gayatri E. Perlin, and Khalil Najafi. Microelectrodes, microelectronics, and implantable neural microsystems. *Proceedings of the IEEE*, 96(7):1184–1202, 2008. doi: 10.1109/JPROC.2008.922564.
- [3] David H. Hubel. Tungsten microelectrode for recording from single units. *Science*, 125(3247):549–550, 1957. doi: 10.1126/science.125.3247.549. URL <https://www.science.org/doi/abs/10.1126/science.125.3247.549>.
- [4] T.L. Rose and L.S. Robblee. Electrical stimulation with pt electrodes. viii. electrochemically safe charge injection limits with 0.2 ms pulses (neuronal application). *IEEE Transactions on Biomedical Engineering*, 37(11):1118–1120, 1990. doi: 10.1109/10.61038.
- [5] Abdulmalik Obaid, Mina-Elraheb Hanna, Yu-Wei Wu, Mihaly Kollo, Romeo Racz, Matthew R. Angle, Jan Müller, Nora Brackbill, William Wray, Felix Franke, E. J. Chichilnisky, Andreas Hierlemann, Jun B. Ding, Andreas T. Schaefer, and Nicholas A. Melosh. Massively parallel microwire arrays integrated with cmos chips for neural recording. *Science Advances*, 6(12):eaay2789, 2020. doi: 10.1126/sciadv.aay2789. URL <https://www.science.org/doi/abs/10.1126/sciadv.aay2789>.
- [6] Patrick T. McCarthy, Kevin J. Otto, and Masaru P. Rao. Robust penetrating microelectrodes for neural interfaces realized by titanium micromachining. *Biomedical Microdevices*, 13(3):503–515, June 2011. ISSN 1572-8781. doi: 10.1007/s10544-011-9519-5. URL <https://doi.org/10.1007/s10544-011-9519-5>.
- [7] Christina Hassler, Rene P. von Metzen, Patrick Ruther, and Thomas Stieglitz. Characterization of parylene c as an encapsulation material for implanted neural prostheses. *Journal of Biomedical Materials Research Part B: Applied Bio-*

- materials*, 93B(1):266–274, 2010. doi: <https://doi.org/10.1002/jbm.b.31584>. URL <https://onlinelibrary.wiley.com/doi/abs/10.1002/jbm.b.31584>.
- [8] Adrian J.T. Teo, Abhinay Mishra, Inkyu Park, Young-Jin Kim, Woo-Tae Park, and Yong-Jin Yoon. Polymeric biomaterials for medical implants and devices. *ACS Biomaterials Science & Engineering*, 2(4):454–472, 2016. doi: 10.1021/acsbiomaterials.5b00429. URL <https://doi.org/10.1021/acsbiomaterials.5b00429>. PMID: 33465850.
- [9] Edward W. Keefer, Barry R. Botterman, Mario I. Romero, Andrew F. Rossi, and Guenter W. Gross. Carbon nanotube coating improves neuronal recordings. *Nature Nanotechnology*, 3(7):434–439, July 2008. ISSN 1748-3395. doi: 10.1038/nnano.2008.174. URL <https://doi.org/10.1038/nnano.2008.174>.
- [10] Bruce L. McNaughton, John O’Keefe, and Carol A. Barnes. The stereotrode: A new technique for simultaneous isolation of several single units in the central nervous system from multiple unit records. *Journal of Neuroscience Methods*, 8(4):391–397, 1983. ISSN 0165-0270. doi: [https://doi.org/10.1016/0165-0270\(83\)90097-3](https://doi.org/10.1016/0165-0270(83)90097-3). URL <https://www.sciencedirect.com/science/article/pii/0165027083900973>.
- [11] Matthew A. Wilson and Bruce L. McNaughton. Dynamics of the hippocampal ensemble code for space. *Science*, 261(5124):1055–1058, 1993. doi: 10.1126/science.8351520. URL <https://www.science.org/doi/abs/10.1126/science.8351520>.
- [12] Vishal Kapoor, Eduard Krampe, Axel Klug, Nikos K. Logothetis, and Theofanis I. Panagiotaropoulos. Development of tube tetrodes and a multi-tetrode drive for deep structure electrophysiological recordings in the macaque brain. *Journal of Neuroscience Methods*, 216(1):43–48, 2013. ISSN 0165-0270. doi: <https://doi.org/10.1016/j.jneumeth.2013.03.017>. URL <https://www.sciencedirect.com/science/article/pii/S0165027013001222>.
- [13] Hiroshi Tamura, Hidekazu Kaneko, and Ichiro Fujita. Quantitative analysis of functional clustering of neurons in the macaque inferior temporal cortex. *Neuroscience Research*, 52(4):311–322, 2005. ISSN 0168-0102. doi: <https://doi.org/10.1016/j.neures.2005.04.006>. URL <https://www.sciencedirect.com/science/article/pii/S0168010205001070>.
- [14] Christopher Doerr and Thomas Schanze. Are heptodes better than tetrodes for spike sorting? *IFAC-PapersOnLine*, 48(20):94–99, 2015. ISSN 2405-8963. doi: <https://doi.org/10.1016/j.ifacol.2015.10.121>. URL <https://www.sciencedirect.com/science/article/pii/S240589631500121>.

- com/science/article/pii/S2405896315020121. 9th IFAC Symposium on Biological and Medical Systems BMS 2015.
- [15] Saman Abbaspoor and Kari L. Hoffman. Circuit dynamics of superficial and deep cal pyramidal cells and inhibitory cells in freely moving macaques. *Cell Reports*, 43(8), 2024. ISSN 2211-1247. doi: 10.1016/j.celrep.2024.114519. URL <https://doi.org/10.1016/j.celrep.2024.114519>.
- [16] Nathaniel J. Killian, Michael J. Jutras, and Elizabeth A. Buffalo. A map of visual space in the primate entorhinal cortex. *Nature*, 491(7426):761–764, November 2012. ISSN 1476-4687. doi: 10.1038/nature11587. URL <https://doi.org/10.1038/nature11587>.
- [17] Matthew P. Ward, Pooja Rajdev, Casey Ellison, and Pedro P. Irazoqui. Toward a comparison of microelectrodes for acute and chronic recordings. *Brain Research*, 1282:183–200, 2009. ISSN 0006-8993. doi: <https://doi.org/10.1016/j.brainres.2009.05.052>. URL <https://www.sciencedirect.com/science/article/pii/S0006899309010841>.
- [18] Justin C Williams, Joseph A Hippensteel, John Dilgen, William Shain, and Daryl R Kipke. Complex impedance spectroscopy for monitoring tissue responses to inserted neural implants. *Journal of Neural Engineering*, 4(4):410, nov 2007. doi: 10.1088/1741-2560/4/4/007. URL <https://doi.org/10.1088/1741-2560/4/4/007>.
- [19] Greg A. Worrell, Andrew B. Gardner, S. Matt Stead, Sanqing Hu, Steve Goerss, Gregory J. Cascino, Fredric B. Meyer, Richard Marsh, and Brian Litt. High-frequency oscillations in human temporal lobe: simultaneous microwire and clinical macroelectrode recordings. *Brain*, 131(4):928–937, 02 2008. ISSN 0006-8950. doi: 10.1093/brain/awn006. URL <https://doi.org/10.1093/brain/awn006>.
- [20] Vadim S. Polikov, Patrick A. Tresco, and William M. Reichert. Response of brain tissue to chronically implanted neural electrodes. *Journal of Neuroscience Methods*, 148(1):1–18, 2005. ISSN 0165-0270. doi: <https://doi.org/10.1016/j.jneumeth.2005.08.015>. URL <https://www.sciencedirect.com/science/article/pii/S0165027005002931>.
- [21] C. Wang, P. G. Stratton, P. Sah, and R. Marek. A protocol to investigate neural coupling of brain oscillations in rodents using in vivo electrophysiological recordings. *STAR Protocols*, 4(3):102414, September 2023. doi: 10.1016/j.xpro.2023.102414.
- [22] Abdulmalik Obaid, Mina-Elraheb Hanna, Yu-Wei Wu, Mihaly Kollo, Romeo Racz, Matthew R. Angle, Jan Müller, Nora Brackbill, William Wray, Felix Franke,

- E. J. Chichilnisky, Andreas Hierlemann, Jun B. Ding, Andreas T. Schaefer, and Nicholas A. Melosh. Massively parallel microwire arrays integrated with cmos chips for neural recording. *Science Advances*, 6(12):eaay2789, 2020. doi: 10.1126/sciadv.aay2789. URL <https://www.science.org/doi/abs/10.1126/sciadv.aay2789>.
- [23] S. Zhang, Y. Song, S. Lv, et al. Electrode arrays for detecting and modulating deep brain neural information in primates: A review. *Cyborg and Bionic Systems*, 6:0249, 2025. doi: 10.34133/cbsystems.0249.
- [24] John P. Seymour and Daryl R. Kipke. Neural probe design for reduced tissue encapsulation in cns. *Biomaterials*, 28(25):3594–3607, September 2007. doi: 10.1016/j.biomaterials.2007.03.024.
- [25] Kensall D. Wise, James B. Angell, and Arnold Starr. An integrated-circuit approach to extracellular microelectrodes. *IEEE Transactions on Biomedical Engineering*, BME-17(3):238–247, 1970. doi: 10.1109/TBME.1970.4502738.
- [26] R.J. Vetter, J.C. Williams, J.F. Hetke, E.A. Nunamaker, and D.R. Kipke. Chronic neural recording using silicon-substrate microelectrode arrays implanted in cerebral cortex. *IEEE Transactions on Biomedical Engineering*, 51(6):896–904, 2004. doi: 10.1109/TBME.2004.826680.
- [27] F Barz, A Livi, M Lanzilotto, M Maranesi, L Bonini, O Paul, and P Ruther. Versatile, modular 3d microelectrode arrays for neuronal ensemble recordings: from design to fabrication, assembly, and functional validation in non-human primates. *Journal of Neural Engineering*, 14(3):036010, mar 2017. doi: 10.1088/1741-2552/aa5a90. URL <https://doi.org/10.1088/1741-2552/aa5a90>.
- [28] Takashi D.Y. Kozai, Kasey Catt, Xia Li, Zhannetta V. Gugel, Valur T. Olafsson, Alberto L. Vazquez, and X. Tracy Cui. Mechanical failure modes of chronically implanted planar silicon-based neural probes for laminar recording. *Biomaterials*, 37:25–39, 2015. ISSN 0142-9612. doi: <https://doi.org/10.1016/j.biomaterials.2014.10.040>. URL <https://www.sciencedirect.com/science/article/pii/S0142961214010874>.
- [29] Roy Biran, David C. Martin, and Patrick A. Tresco. Neuronal cell loss accompanies the brain tissue response to chronically implanted silicon microelectrode arrays. *Experimental Neurology*, 195(1):115–126, 2005. ISSN 0014-4886. doi: <https://doi.org/10.1016/j.expneurol.2005.04.020>. URL <https://www.sciencedirect.com/science/article/pii/S0014488605001457>.
- [30] Meijian Wang and Liang Guo. Intracortical electrodes. In Liang Guo, editor, *Neural*

- Interface Engineering: Linking the Physical World and the Nervous System*, pages 67–94. Springer International Publishing, Cham, 2020. ISBN 978-3-030-41854-0. doi: 10.1007/978-3-030-41854-0_4.
- [31] Mohamad HajjHassan, Vamsy Chodavarapu, and Sam Musallam. Neuromems: Neural probe microtechnologies. *Sensors*, 8(10):6704–6726, 2008. ISSN 1424-8220. doi: 10.3390/s8106704. URL <https://www.mdpi.com/1424-8220/8/10/6704>.
- [32] P.K. Campbell, K.E. Jones, R.J. Huber, K.W. Horch, and R.A. Normann. A silicon-based, three-dimensional neural interface: manufacturing processes for an intracortical electrode array. *IEEE Transactions on Biomedical Engineering*, 38(8):758–768, 1991. doi: 10.1109/10.83588.
- [33] Almut Branner, Richard B. Stein, and Richard A. Normann. Selective stimulation of cat sciatic nerve using an array of varying-length microelectrodes. *Journal of Neurophysiology*, 85(4):1585–1594, 2001. doi: 10.1152/jn.2001.85.4.1585. URL <https://doi.org/10.1152/jn.2001.85.4.1585>. PMID: 11287482.
- [34] Kelly E. Jones, Patrick K. Campbell, and Richard A. Normann. A glass/silicon composite intracortical electrode array. *Annals of Biomedical Engineering*, 20(4):423–437, 1992. ISSN 1573-9686. doi: 10.1007/BF02368134. URL <https://doi.org/10.1007/BF02368134>.
- [35] A. Spiers, K. Warwick, M. Gasson, and V. Ruiz. Issues impairing the success of neural implant technology. *Applied Bionics and Biomechanics*, 3(4):154724, 2006. doi: <https://doi.org/10.1533/abbi.2006.0055>. URL <https://onlinelibrary.wiley.com/doi/abs/10.1533/abbi.2006.0055>.
- [36] M.M.H. Shandhi, M. Leber, A. Hogan, R. Bhandari, and S. Negi. A novel method of fabricating high channel density neural array for large neuronal mapping. In *2015 Transducers - 2015 18th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, pages 1759–1762, 2015. doi: 10.1109/TRANSDUCERS.2015.7181286.
- [37] Leigh R. Hochberg, Mijail D. Serruya, Gerhard M. Friehs, Jon A. Mukand, Maryam Saleh, Abraham H. Caplan, Almut Branner, David Chen, Richard D. Penn, and John P. Donoghue. Neuronal ensemble control of prosthetic devices by a human with tetraplegia. *Nature*, 442(7099):164–171, 2006. ISSN 1476-4687. doi: 10.1038/nature04970. URL <https://doi.org/10.1038/nature04970>.
- [38] Sharlene N. Flesher, Jennifer L. Collinger, Stephen T. Foldes, Jeffrey M. Weiss, John E. Downey, Elizabeth C. Tyler-Kabara, Sliman J. Bensmaia, Andrew B.

- Schwartz, Michael L. Boninger, and Robert A. Gaunt. Intracortical microstimulation of human somatosensory cortex. *Science Translational Medicine*, 8(361): 361ra141–361ra141, 2016. doi: 10.1126/scitranslmed.aaf8083. URL <https://www.science.org/doi/abs/10.1126/scitranslmed.aaf8083>.
- [39] Eduardo Fernández, Arantxa Alfaro, Cristina Soto-Sánchez, Pablo Gonzalez-Lopez, Antonio M. Lozano, Sebastian Peña, Maria Dolores Grima, Alfonso Rodil, Bernardeta Gómez, Xing Chen, Pieter R. Roelfsema, John D. Rolston, Tyler S. Davis, and Richard A. Normann. Visual percepts evoked with an intracortical 96-channel microelectrode array inserted in human occipital cortex. *The Journal of Clinical Investigation*, 131(23), 10 2021. doi: 10.1172/JCI151331. URL <https://www.jci.org/articles/view/151331>.
- [40] Michael P. Ward, Prasad Rajdev, Charles Ellison, and Pedro P. Irazoqui. Toward a comparison of microelectrodes for acute and chronic recordings. *Brain Research*, 1282:183–200, Jul 2009. doi: 10.1016/j.brainres.2009.05.052. URL <https://doi.org/10.1016/j.brainres.2009.05.052>.
- [41] F. Sauter-Starace, N. Torres-Martinez, V. Agache, C. Pudda, J. Dijon, B. Piallat, J. L. Divoux, N. Bourquin, J. F. Charmeux, F. Berger, A L Benabid, A. Sherdil, and S. Chabardès. Epileptic seizure recordings of a non-human primate using carbon nanotube microelectrodes on implantable silicon shanks. In *2011 5th International IEEE/EMBS Conference on Neural Engineering*, pages 589–592, 2011. doi: 10.1109/NER.2011.5910617.
- [42] Song Zhang, Yilin Song, Mixia Wang, Zhiming Zhang, Xinyi Fan, Xianteng Song, Ping Zhuang, Feng Yue, Piu Chan, and Xinxia Cai. A silicon based implantable microelectrode array for electrophysiological and dopamine recording from cortex to striatum in the non-human primate brain. *Biosensors and Bioelectronics*, 85:53–61, 2016. ISSN 0956-5663. doi: <https://doi.org/10.1016/j.bios.2016.04.087>. URL <https://www.sciencedirect.com/science/article/pii/S0956566316303736>.
- [43] James J. Jun, Nicholas A. Steinmetz, Joshua H. Siegle, Daniel J. Denman, Marius Bauza, et al. Fully integrated silicon probes for high-density recording of neural activity. *Nature*, 551(7679):232–236, 2017. ISSN 1476-4687. doi: 10.1038/nature24636. URL <https://doi.org/10.1038/nature24636>.
- [44] Brianna Thielen and Ellis Meng. A comparison of insertion methods for surgical placement of penetrating neural interfaces. *Journal of Neural Engineering*, 18(4):

- 041003, apr 2021. doi: 10.1088/1741-2552/abf6f2. URL <https://doi.org/10.1088/1741-2552/abf6f2>.
- [45] Yang Liu, Huilin Jia, Hongji Sun, Shengyi Jia, Ziqian Yang, Ao Li, Anqi Jiang, Yuji Naya, Cen Yang, Shengyuan Xue, Xiaojian Li, Bingyan Chen, Jingjun Zhu, Chenghao Zhou, Minning Li, and Xiaojie Duan. A high-density 1,024-channel probe for brain-wide recordings in non-human primates. *Nature Neuroscience*, 27(8):1620–1631, 2024. ISSN 1546-1726. doi: 10.1038/s41593-024-01692-6. URL <https://doi.org/10.1038/s41593-024-01692-6>.
- [46] Yixin Tian, Jiapeng Yin, Chengyao Wang, Zhenliang He, Jingyi Xie, Xiaoshan Feng, Yang Zhou, Tianyu Ma, Yang Xie, Xue Li, Tianming Yang, Chi Ren, Chengyu Li, and Zhengtuo Zhao. An ultraflexible electrode array for large-scale chronic recording in the nonhuman primate brain. *Advanced Science*, 10(33):2302333, 2023. doi: <https://doi.org/10.1002/adv.202302333>. URL <https://advanced.onlinelibrary.wiley.com/doi/abs/10.1002/adv.202302333>.
- [47] Omid Talakoub, Patricia Sayegh, Thilo Womelsdorf, Wolf Zinke, Pascal Fries, Christopher M. Lewis, and Kari L. Hoffman. Hippocampal and neocortical oscillations are tuned to behavioral state in freely-behaving macaques. *bioRxiv*, 2019. doi: 10.1101/552877. URL <https://www.biorxiv.org/content/early/2019/02/18/552877>.
- [48] Elon Musk. An integrated brain-machine interface platform with thousands of channels. *J Med Internet Res*, 21(10):e16194, Oct 2019. ISSN 1438-8871. doi: 10.2196/16194. URL <http://www.jmir.org/2019/10/e16194/>.
- [49] Lotfi B. Merabet, Joseph F. Rizzo, Amir Amedi, David C. Somers, and Alvaro Pascual-Leone. What blindness can tell us about seeing again: merging neuroplasticity and neuroprostheses. *Nature Reviews Neuroscience*, 6(1):71–77, jan 2005. doi: 10.1038/nrn1586.
- [50] Tal Sharf, Tejaswi Kalakuntla, Daniel J. Lee, and Krystel K. Gokoffski. Electrical devices for visual restoration. *Survey of Ophthalmology*, 67(3):793–800, May-Jun 2022. doi: 10.1016/j.survophthal.2021.08.008.
- [51] Gian Luca Barbruni, Paolo Motto Ros, Danilo Demarchi, Sandro Carrara, and Diego Ghezzi. Miniaturised wireless power transfer systems for neurostimulation: A review. *IEEE Transactions on Biomedical Circuits and Systems*, 14(6):1160–1178, 2020. doi: 10.1109/TBCAS.2020.3038599.
- [52] Gian Luca Barbruni, Paolo Motto Ros, Danilo Demarchi, Sandro Carrara, and Diego

- Ghezzi. Ultra-miniaturised cmos current driver for wireless biphasic intracortical microstimulation. In *2022 11th International Conference on Modern Circuits and Systems Technologies (MOCAS)*, pages 1–4, 2022. doi: 10.1109/MOCAS54814.2022.9837681.
- [53] Gian Luca Barbruni, Claudia Cordara, Marco Carminati, Sandro Carrara, and Diego Ghezzi. A frequency-switching inductive power transfer system for wireless, miniaturised and large-scale neural interfaces. *IEEE Transactions on Biomedical Circuits and Systems*, 18(3):679–690, 2024. doi: 10.1109/TBCAS.2024.3359481.
- [54] Gian Luca Barbruni, Francesca Rodino, Paolo Motto Ros, Danilo Demarchi, Diego Ghezzi, and Sandro Carrara. A wearable real-time system for simultaneous wireless power and data transmission to cortical visual prosthesis. *IEEE Transactions on Biomedical Circuits and Systems*, 18(3):580–591, 2024. doi: 10.1109/TBCAS.2024.3357626.
- [55] Lorraine V. Kalia and Anthony E. Lang. Parkinson’s disease. *The Lancet*, 386(9996):896–912, 2015. doi: 10.1016/S0140-6736(14)61393-3.
- [56] Oliver D. Howes and Shitij Kapur. The dopamine hypothesis of schizophrenia: Version iii—the final common pathway. *Schizophrenia Bulletin*, 35(3):549–562, 03 2009. ISSN 0586-7614. doi: 10.1093/schbul/sbp006. URL <https://doi.org/10.1093/schbul/sbp006>.
- [57] Ali Meimandi, Gian Luca Barbruni, Paolo Stefano Crovetto, and Sandro Carrara. Sub- $9 \times 29 \mu\text{m}^2$, 1.2nw, fully digital potentiostat design for dopamine sensing. *IEEE Sensors Journal*, 25(20):38792–38799, 2025. doi: 10.1109/JSEN.2025.3605728.
- [58] Junyan Qian, Melania Coronese, Andrea Pafundo, Ali Meimandi, Gian Luca Barbruni, Marco Carminati, and Sandro Carrara. Miniaturized foldable electrodes with direct cmos integration for implantable applications. *2025 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pages 359–363, 2025. URL <https://api.semanticscholar.org/CorpusID:284726558>.
- [59] KLayout. Introduction to klayout, 2026. URL <https://www.klayout.de/intro.html>.
- [60] CMi EPFL. Layout designs, 2025. URL <https://www.epfl.ch/research/facilities/cmi/process/photolithography/layout-design/>.
- [61] Allen J. Bard and Larry R. Faulkner. *Electrochemical Methods: Fundamentals and Applications*. Wiley, 2 edition, 2001.

- [62] Wafa Aidli, Daniele Fumagalli, Valentina Pifferi, and Luigi Falciola. From dual-mode to multi-modal electrochemical based sensors: A path toward accurate sensing. *Current Opinion in Electrochemistry*, 50:101655, 2025. ISSN 2451-9103. doi: <https://doi.org/10.1016/j.coelec.2025.101655>. URL <https://www.sciencedirect.com/science/article/pii/S2451910325000146>.
- [63] CMi EPFL. Mla 150, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/photolithography/mla-150/>.
- [64] CMi EPFL. Az eci 3000 process steps, 2025. URL <https://www.epfl.ch/research/facilities/cmi/process/photolithography/photoresist-selection/az-eci-3000/>.
- [65] Ultrasil LLC. Si/100mm/dsp/1-10/ttv2 datasheet, 2020. URL https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2020/05/100_p_ds_1_10.pdf.
- [66] Marc J. Madou. *Fundamentals of Microfabrication and Nanotechnology*. CRC Press, Boca Raton, FL, USA, 3rd edition, 2011. ISBN 978-1439839242.
- [67] CMi EPFL. List of materials, 2025. URL <https://www.epfl.ch/research/facilities/cmi/process/materials/>.
- [68] CMi EPFL. Cmi homepage, 2025. URL <https://www.epfl.ch/research/facilities/cmi/>.
- [69] CMi EPFL. Plade rca, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/thin-films/plade-rca/>.
- [70] CMi EPFL. Centrotherm furnaces, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/thin-films/centrotherm-furnaces/>.
- [71] CMi EPFL. Dry and wet oxidation curves, 2020. URL <https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2020/06/Dry-Wet-Oxidation-Curves.pdf>.
- [72] CMi EPFL. Lab600h recipes, 2020. URL <https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2020/03/LAB600H-recettes.pdf>.
- [73] CMi EPFL. Pfeiffer spider 600, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/thin-films/pfeiffer-spider-600/>.
- [74] CMi EPFL. Spider600 deposition time, 2024. URL <https://www.epfl.ch/>

- research/facilities/cmi/wp-content/uploads/2024/02/SPIDER600_How_to_calculate_deposition_time.pdf.
- [75] CMi EPFL. Introduction to photolithography, 2025. URL <https://www.epfl.ch/research/facilities/cmi/process/photolithography/introductiontophotolithography/>.
- [76] CMi EPFL. Mla 150 manual, 2023. URL https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2023/02/MLA150_manual_2023.pdf.
- [77] CMi EPFL. Photolith selection, 2025. URL <https://www.epfl.ch/research/facilities/cmi/process/photolithography/photoresist-selection-2/>.
- [78] CMi EPFL. Sm-200 user manual, 2024. URL https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2024/11/Sawatec_PR_manual_2024.pdf.
- [79] CMi EPFL. Photolithography inspection, rework, descum and stripping, 2025. URL <https://www.epfl.ch/research/facilities/cmi/process/photolithography/photolithography-inspection-stripping-and-descum/>.
- [80] CMi EPFL. Etch definitions, 2025. URL <https://www.epfl.ch/research/facilities/cmi/process/etching/etch-definitions/>.
- [81] CMi EPFL. End-point-detection system, 2025. URL <https://www.epfl.ch/research/facilities/cmi/process/etching/end-pointing-capabilities/>.
- [82] CMi EPFL. Plasma cobra 100, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/etching/oxford-plasmapro100-cobra/>.
- [83] Shipley Rohm and Haas. Svc-14 datasheet, 2024. URL https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2024/09/TDS_SVC14.pdf.
- [84] CMi EPFL. Uft resist wet bench, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/etching/uft-resist/>.
- [85] Dieter K. Schroder. *Semiconductor Material and Device Characterization*. Wiley, Hoboken, NJ, USA, 3rd edition, 2006.
- [86] CMi EPFL. Corial d250l pecvd, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/thin-films/corial-pecvd/>.
- [87] CMi EPFL. Corial d250l recipes, 2023. URL https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2023/07/Corial_D250L_Recipes.pdf.

- [88] Merck KGaA. Az 10xt series datasheet, 2021. URL https://www.microchemicals.com/dokumente/datenblaetter/tds/merck/en/tds_az_10xt_photoresist.pdf.
- [89] CMi EPFL. Az 10xt process steps, 2025. URL <https://www.epfl.ch/research/facilities/cmi/process/photolithography/photoresist-selection/az-10xt/>.
- [90] CMi EPFL. Arias acid wet bench, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/etching/arias-acid/>.
- [91] CMi EPFL. Sts multiplex icp plasma etcher, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/etching/sts-multiplex-icp/>.
- [92] CMi EPFL. Veeco nexus ibe350, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/etching/veeco-nexus-ibe350/>.
- [93] CMi EPFL. Pr reflow, 2023. URL https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2023/02/Reflow_etch-tests_CMi.pdf.
- [94] CMi EPFL. Stps aps, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/etching/spts-aps/>.
- [95] CMi EPFL. Mc pc 62e process steps, 2025. URL <https://www.epfl.ch/research/facilities/cmi/process/photolithography/photoresist-selection/az-p4k-ap/>.
- [96] CMi EPFL. Dag810 automatic surface grinder, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/etching/dag810-automatic-surface-grinder/>.
- [97] CMi EPFL. Spts rapier drie tool, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/etching/spts-rapier/>.
- [98] CMi EPFL. Comelec c-30-s, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/thin-films/comelec-c-30-s/>.
- [99] SCS Coatings. A guide to parylene service temperatures, 2022. URL <https://scscoatings.com/newsroom/blog/a-guide-to-parylene-service-temperatures/>.
- [100] CMi EPFL. Silanization for parylene, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/thin-films/comelec-c-30-s/parylene-silanization/>.

- [101] Joana Maciel, M. Cristina L. Martins, and Mário A. Barbosa. The stability of self-assembled monolayers with time and under biological conditions. *Journal of Biomedical Materials Research Part A*, 94A(3):833–843, 2010. doi: <https://doi.org/10.1002/jbm.a.32746>. URL <https://onlinelibrary.wiley.com/doi/abs/10.1002/jbm.a.32746>.
- [102] Jie Gao, Tianlan Chen, Cheng Dong, Yanwei Jia, Pui-In Mak, Mang-I. Vai, and Rui P. Martins. Adhesion promoter for a multi-dielectric-layer on a digital microfluidic chip. *RSC Adv.*, 5:48626–48630, 2015. doi: 10.1039/C5RA08202A. URL <http://dx.doi.org/10.1039/C5RA08202A>.
- [103] Samco Inc. Bosh process pricniple, 2026. URL <https://www.samcointl.com/news-events/tutorials/what-is-the-bosch-process/>.
- [104] M. A. Lieberman and A. J. Lichtenberg. *Principles of Plasma Discharges and Materials Processing*. Wiley, Hoboken, NJ, 2nd edition, 2005. ISBN 978-0-471-47192-9.
- [105] Siegert wafer. Si/100mm/ssp/test datasheet, 2020. URL https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2020/05/100_p_ss_01_100_test.pdf.
- [106] CMi - EPFL. Quick stick 135, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/packaging-miscellaneous/quickstick-qs135/>.
- [107] CMi - EPFL. Nanoscribe photonic professional gt+, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/photolithography/nanoscribe-photonic-professional-gt/>.
- [108] Toho Technology. Toho technology flx 2320-s datasheet, 2019. URL https://tohotechnology.com/wp-content/uploads/2019/09/Toho_FLX2320S_D1.pdf.
- [109] CMi - EPFL. Toho technology flx 2320-s, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/metrology/toho-technology-flx-2320-s/>.
- [110] W. D. Nix. Mechanical properties of thin films. *Metallurgical and Materials Transactions A*, 20(11):2217–2245, 1989. doi: 10.1007/BF02648436.
- [111] CMi - EPFL. Leica dm8000, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/metrology/mic-optic/leica-dm800-inspection-microscope/>.

- [112] Zeiss. Gemini columns, 2026. URL <https://www.zeiss.com/microscopy/en/products/sem-fib-sem/sem/geminisem-family.html>.
- [113] CMi - EPFL. Zeiss-merlin sem, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/metrology/zeiss-merlin/>.
- [114] Brandon Ohl. What is scanning electron microscopy, 2020. <https://msestudent.com/what-is-scanning\protect\penalty\z@-electron\protect\penalty\z@-microscopy\protect\penalty\z@-how-it-works\protect\penalty\z@-applications-and-limitations/>.
- [115] CMi - EPFL. Edx, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/metrology/oxford-instruments-edx/>.
- [116] Brunker Corporation. Bruker dektak xt user manual, 2020. URL <https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2020/06/DektakXT-User.pdf>.
- [117] CMi - EPFL. Bruker dektak xt, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/metrology/bruker-dektak-xt/>.
- [118] Pavan M. V. Raja and Andrew R. Barron. 1.12: An introduction to energy dispersive x-ray spectroscopy. [https://chem.libretexts.org/Bookshelves/Analytical_Chemistry/Physical_Methods_in_Chemistry_and_Nano_Science_\(Barron\)/01:_Elemental_Analysis/1.12:_An_Introduction_to_Energy_Dispersive_X-ray_Spectroscopy](https://chem.libretexts.org/Bookshelves/Analytical_Chemistry/Physical_Methods_in_Chemistry_and_Nano_Science_(Barron)/01:_Elemental_Analysis/1.12:_An_Introduction_to_Energy_Dispersive_X-ray_Spectroscopy), 2014. Accessed via LibreTexts, CC BY license.
- [119] CMi - EPFL. Mpi ts150 probe station, 2025. URL https://www.epfl.ch/research/facilities/cmi/equipment/metrology/mpi_ts150/.
- [120] Kigno Ariyoshi, Zyun SIROMA, Atsushi MINESHIGE, Takeno Mitsuhiro, Tomokazu Fukutsuka, Takeshi Abe, and Satoshi UCHIDA. Electrochemical impedance spectroscopy part 1: Fundamentals. *Electrochemistry*, 90:102007–102007, 10 2022. doi: 10.5796/electrochemistry.22-66071.
- [121] Ankit Tyagi and Raju Gupta. Carbon nanostructures from biomass waste for supercapacitor applications. In Sivashankar Krishnamoorthy, editor, *Nanomaterials: A Guide to Fabrication and Applications*. CRC Press, Boca Raton, FL, 2015. ISBN 978-1-4665-9126-4. doi: 10.1201/b19168-11.
- [122] Kurian Polachan, Baibhab Chatterjee, Scott Weigand, and Shreyas Sen. Human body–electrode interfaces for wide-frequency sensing and communication: A review. *Nanomaterials*, 11:2152, 08 2021. doi: 10.3390/nano11082152.

- [123] Altium Limited. Altium designer homepage, 2026. URL <https://www.altium.com/it/altium-designer>.
- [124] CMi - EPFL. Disco dad321, 2025. URL <https://www.epfl.ch/research/facilities/cmi/equipment/packaging-miscellaneous/disco-dad321/>.
- [125] Epoxy Technology. H70e epoxy datasheet, 2020. URL <https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2020/04/H70E.pdf>.
- [126] F&S Bondtec. F&s bondtec 56i manual, 2022. URL https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2022/06/56xxi_manual_en.pdf.
- [127] Epoxy Technology. H70e-2 epoxy datasheet, 2020. URL <https://www.epfl.ch/research/facilities/cmi/wp-content/uploads/2020/04/H70E-2.pdf>.
- [128] Merck KGaA. Pbs concentrations, 2025. URL https://www.sigmaaldrich.com/CH/it/support/calculators-and-apps/1x-phosphate-buffered-saline?srsltid=AfmB0orZp0e7hFa1EIcKT_3AJ-9Vn9vPIsIGLU8Qt1vPzB2ZOMP3ou7D.
- [129] Metrohm. Autolab pgstat302n product page, 2026. URL https://www.metrohm.com/en_gb/products/a/ut30/aut302n_s.html.
- [130] Adam Wang, Doohwan Jung, Dongwon Lee, and Hua Wang. Impedance characterization and modeling of subcellular to micro-sized electrodes with varying materials and pedot:pss coating for bioelectrical interfaces. *ACS Applied Electronic Materials*, 3(12):5226–5239, 2021. doi: 10.1021/acsaelm.1c00687. URL <https://doi.org/10.1021/acsaelm.1c00687>.

Acknowledgments

If you're reading this it, congratulations! You've survived all those long and technical pages! Or did you just skipped through to check if your name is in here? You did, didn't you?

Anyway, I would say it's time to thank all the wonderful people that made this long journey an experience worth living.

First of all, I want to thank my project supervisors, Prof. Carminati and Prof. Carrara. In you, not only I found guidance, thanks to your great experience in the field, but also someone always ready to listen to my personal needs. Your humanity, combined with your unquestioned professionalism, is something I will always be grateful for. I would also like to thank Dr. Gian Luca Barbruni. Without you I would have never been able to be part of such an incredible project; to be fair, this whole project wouldn't even exist. Thank you as well for all the suggestions you gave me, which helped me to never lose sight of the general picture. A special thanks goes to Ali Meimandi and Junyan (Dodo) Qian. I'm one hundred percent sure that without you I would probably still be crying at CMi. You've been the best lab supervisors that I could have ever asked for, always ready to give me a hand, answer a question, listen to an idea; no matter how busy your schedules were. I know that not everybody would have done that and you have my eternal gratitude. (Let me know how much do I owe you when we see each other again). Thank also to Lysiane: you've always handled every request, no matter how short-noticed it was, with a smile. Your work played an important role in the success of this thesis, and it didn't go unnoticed. I would like to thank Melania, my predecessor. If I had success it is definitely also because of you. We didn't meet often unfortunately, but you were always ready to encourage me and gave me suggestions whenever you saw in the clean-room. I'm deeply grateful for that. I want to say thanks to all the members of the BCI Lab at EPFL: Alireza, Anas, Chiara, Dimitrii, Farouk, Francesca, Giacomo, Hadi, Hamid, Junrui, Lin, Marco, Maroun, Martina, Morteza, Nehal, Roberta, Simone, Valeria and Yasaman; together with all the lovely people I've met in Neuchâtel: Alice, Arianna, Camilla, Ceren, Deniz, Fabio, Giada, Giovanni, Lorenzo, Maribel, Matteo, Paul, Quentin, Samuele and Valerio. From the very first day, you've welcomed me as if I had always been

there. I never felt like the outsider, which is something that is so uncommon in established groups, and you made me love every moment of my stay! Three people may have noticed that I hadn't mentioned them yet, but before Marta kills me, of course a special place in my heart goes to the members of the best office in Micro-city! Sabina, Marta, Caterina: I'll never forget all the mornings spent to convince you to wait a bit to "buy croissants in the cafeteria", all the coffee breaks, all the water-bottle breaks... well you get it. Thank you for sharing this journey with me: the excitement, the desperation, the late hours and especially all the laughs. I could not even imagine this whole period without you! Finally, before passing to Italian (sorry english-only readers, you had enough fun already), I want to thank an object. I know, it's strange... Anyway, thank you Wafer 1618, a.k.a. the *cursed wafer*. You caused blackouts, machine malfunctions; you even defied the laws of physics and created matter out of thin air... And yet, despite everything, without you my thesis would not be finished. So thanks. Still, you were a pain.

Ed ora è il momento di passare ai ringraziamenti in italiano. Prima di tutto non posso che ringraziare le persone senza le quali non sarei qui, ma proprio qui, in questo mondo: i miei genitori. Grazie per aver creduto in me, sempre, anche quando non ci ho creduto nemmeno io. Non mi avete mai fatto sentire sotto giudizio in questo percorso, mai una volta; mi avete sempre supportato incondizionatamente. Vi sarò sempre grato per questo. Ringrazio poi mio fratello. So bene che ultimamente sono sempre in giro e, anche quando sono a casa, ho sempre da fare. Stiamo insieme un infinitesimo del tempo che vorrei, ma tu non me lo fai mai pesare; anzi, sei sempre il primo a gioire non appena ci vediamo. Grazie, perché so che saremo sempre uniti, sempre e comunque! (Ma a FIFA sarò sempre scarso, ti avviso). Vorrei poi ringraziare Chiara e Davide: siete tra le persone che più mi hanno capito in questi anni, forse per esperienza diretta con questo folle e meraviglioso percorso che è l'università. Grazie per esserci sempre per me, sono felice che siate nella mia vita. Davide, scusa, ma il latino non lo imparerò mai. Ci abbiamo provato, ma ho altre qualità, diciamo... Ringrazio poi tutta la mia famiglia. A partire da mia nonna Angela, per passare poi ai miei zii e zie: Anto, Franco, Gianni, Ghilo, Lucio, Roby e Wendy. Senza dimenticare i miei adorati cugini: Francesca, Greta, Luca e Nicolò. Infine (scusate il momento emotional), non posso non ricordare quelli che questo ringraziamento non lo potranno purtroppo leggere, ma che per me sono stati fondamentali: i miei nonni, Giorgio e Vito, e i miei zii, Claudia e Donato. Grazie a tutti per essere una famiglia così affiatata. Adoro il fatto di essere sempre entusiasta di vedervi quando si fanno i grandi ritrovi, e di non dover mai pensare "oddio, speriamo di sbrigarci presto". No no, speriamo di farne più spesso! Avrei qualcosa da dire su tutti... ma siete tantissimi, concedetemi quindi di dedicare un po' di spazio alla persona senza cui non sarei chi sono: mia nonna Mary. Grazie perché mi hai insegnato ad essere curioso, che credo sia la caratteristica che

amo di più di me stesso, e non penso che lo sarei nemmeno lontanamente così tanto senza di te. Voglio dire, quante nonne leggevano l'enciclopedia al nipotino? Io dico nessuna! Ed infine, grazie a tutti i miei amici! Grazie Fra, sono sicuro che sarai sempre la persona a cui, non importa la distanza o il fuso orario, dirò ogni singola cosa che mi è successa o che mi è passata per la mente quel giorno. E so che tu farai sempre lo stesso. (Ti sento più di mia madre praticamente, ma mi sta bene così). Grazie Cate, Luca, Fra (non il Fra di prima, un'altra Fra) e Ferro perché, nonostante tutti i pacchi, nonostante ci vediamo cinque minuti ogni sei mesi, mi dimostraste sempre un amore e un affetto che sfido chiunque a trovare una singola persona come voi. Io ne ho trovate quattro e sono davvero fortunato! Poi devo assolutamente dire grazie ad: Aki, Arianna, Bombi, Figio, Laba, Lanza, Mandre, Nika, Sguinza e Zanca. Da quando mi avete accolto nel vostro gruppo, nemmeno poi così tanto tempo fa, mi sento come se ne avessi sempre fatto parte. Grazie per tutte le serate stupende che mi avete fatto passare. E chiaramente grazie a tutti i miei compagni di studi, i pendolari che non pendolano: Albi, Ale, Angelica, Carola, Diego, Elena, Gaia, Giulio, Joan, Max, Paola, Simo (1 e 2) e Thomas. Sono arrivato in magistrale un po' intimorito, perché non conoscevo nessuno... e guardateci ora! Mi mancherà da morire il venerdì dei dolci! Se vogliamo organizzarlo ancora, non sarò io a dire di no. E infine, un ringraziamento molto particolare a due persone che dubito sospettino di essere citate, e che io stesso ho incontrato solo una manciata di volte. Ma ogni tanto basta un singolo incontro, un singolo discorso fatto durante una cena in riva al mare, perché un bambino possa rimanere folgorato e decidere cosa vuole fare per tutta la sua vita. Beh, sappiate che tutto questo è anche merito (e un po' colpa, diciamocelo) vostro. Grazie Simona e Carlo.



