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SCUOLA DI INGEGNERIA INDUSTRIALE
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# FULL QUALIFICATION TEST ON MILITARY AIRCRAFT ELECTRICAL POWER DISTRIBUTION SYSTEM

TESI DI LAUREA MAGISTRALE IN
ELECTRICAL ENGINEERING

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**ABSTRACT**

The purpose of this thesis is to assess all Safety of Flight (SOF) testing and qualification procedures for an Electrical Power Distribution System of a military helicopter. The entire project was completed by ASE S.p.A, a company specializing in the design, development, and manufacturing of electric generation and distribution systems for the aerospace and defense industries.

It is the first time in history that AC and DC power distribution systems of military aircraft have been the subject of a thesis or article. Additionally, my project is unique in that the aircraft for which this system is designed is completely self-cooling and meets all military standards.

The first section of this work describes in detail the mechanical and performance characteristics of all the machines and units that comprise the Electrical Power Distribution System. The central body of the study is focused on the test procedures aimed at obtaining the qualification so that the aircraft can carry out the first flight. It is divided into 3 main chapters:

1. Acceptance Test Procedure (ATP): testing of all system components to ensure they meet the parameters and performance requirements specified in the project.
2. Qualification Test Program (QTP): a detailed description of all the tests required to qualify for the initial flight.
3. Qualification Test Results (QTR): a collection of all test results obtained during the scheduled tests of the QTP.

For the sake of simplicity, only the most significant findings are reported. The qualification plan analyzes three vital components: AC and DC Power Distribution Panels and the Battery PDP. The qualification plan is largely separated into Safety of Flight (SOF) and Full Flight (FULL) qualification, which must be accomplished in sequence. Indeed, the SOF must be completed first, as it contains the fundamental requirements for the power system to perform a first flight. Once you have completed this portion of the qualification process, you can proceed to FULL to complete the plan. Between each individual test, whether in the SOF or FULL qualification phase, the individual units must be tested to ensure their electrical and mechanical integrity and that they generally conform to the values stated during the design process. The Environmental refers to all environmental tests such as Temperature, Altitude, Vibration and Explosive Atmosphere tests. The Electromagnetic Compatibility (EMC / EMI) tests concern the transmission and reception of electromagnetic energy in relation to the undesirable effects that could occur. They have the objective of guaranteeing the correct functioning of the various devices in the same environment, also allowing the avoidance of negative electromagnetic phenomena during system operation.

This acceptance test procedure (ATP) ensures that each component works properly just before and after each individual test. Due to the fact that the system has not yet been fully validated for the SOF part, the tests associated with FULL have not been conducted but are only stated theoretically. Again, with regards to the SOF, the results of the electrical performance tests conducted on the system throughout the distribution phase are listed. An example of an acceptance procedure for the three components that comprise the system: AC and DC Electrical Power Distribution System, Battery PDP, and Fuse Box is also reported.

The effectiveness of vent hole shielding was examined in detail using a computational model with Mathcad. The impact of hole size, hole depth, and hole-to-hole separation distance was investigated in this analysis using finite-difference time domain simulation. Additionally, an innovative mathematical relationship centered on these same parameters was introduced and demonstrated to be highly predictive of simulated data. Finally, experimental data from laboratory measurements is used to validate simulation and analytical predictions.

I worked personally on the entire qualification process (which lasted six months) of this power distribution system for aeronautical use, and I also carried out all of these tests personally and in total autonomy. I was also involved in product development, such as modification of advanced testing procedures according to international standards and customer specification, and optimization of the EMI shielding effectiveness.

**ABSTRACT**

Lo scopo di questa tesi è di valutare tutte le procedure di test e qualifica, per il raggiungimento della certificazione della Safety of Flight (SOF) di un sistema di distribuzione di energia elettrica per un velivolo militare. L'intero progetto è stato gestito e progettato da ASE, società specializzata nello sviluppo e produzione di sistemi di generazione e distribuzione elettrica per l'industria aerospaziale e della difesa.

È la prima volta nella storia che i sistemi di distribuzione elettrica, sia in corrente alternata che corrente continua di apparati militari, sono stati oggetto di una tesi. Inoltre, il mio progetto è unico in quanto, l'elicottero per il quale è progettato questo sistema, è privo di sistemi di raffreddamento attivi soddisfando al contempo tutti i requisiti certificativi previsti. Per permettere il raffreddamento, senza ventole, dei componenti all'interno delle scatole di distribuzione, è stato elaborato un calcolo per lo schema di foratura delle pareti delle scatole, che potesse dimensionare correttamente diametro e distanza dei fori di areazione potenza e al contempo evitare emissioni elettromagnetiche al di fuori dei limiti consentiti dalla specifica dei requisiti. L'efficacia della schermatura dei fori di areazione è stata esaminata in dettaglio utilizzando un modello computazionale con Mathcad. L'impatto della dimensione del foro, della profondità del foro e della distanza di separazione da foro a foro è stato studiato in questa analisi utilizzando la simulazione nel dominio del tempo alle differenze finite. Inoltre, è stata introdotta un'innovativa relazione matematica incentrata su questi stessi parametri che si è dimostrata altamente predittiva dei dati simulati. Infine, i dati sperimentali delle misurazioni di laboratorio vengono utilizzati per convalidare la simulazione e le previsioni analitiche.

La prima sezione di questo lavoro descrive in dettaglio le caratteristiche meccaniche e prestazionali di tutte le macchine e le unità che compongono il Sistema. La seconda parte è incentrato sulle procedure di prova finalizzate all'ottenimento della qualifica necessaria affinché l'aeromobile possa effettuare il primo volo. È suddiviso in 3 capitoli principali:

1. Procedura di Test di Accettazione (ATP): test di tutti i componenti del sistema per garantire che soddisfino i parametri e i requisiti di prestazione specificati nel progetto.
2. Procedure dei Test di Qualifica (QTP): una descrizione dettagliata di tutti i test necessari e delle relative procedure che devono essere eseguite al fine di raggiungere la qualifica dei requisiti minimi necessari per permettere il volo iniziale e la fase sperimentale del velivolo.
3. Risultati dei Test di Qualifica (QTR): una raccolta di tutti i risultati dei test ottenuti durante le prove programmate del QTP.

In questo elaborato, per maggiore chiarezza, si riportano solo i rilievi più significativi tra tutti i test svolti.

Il piano di qualifica analizza tre componenti vitali: le scatole di distribuzione dell'alimentazione AC, le scatole di distribuzione dell'alimentazione DC e il pannello di distribuzione dell'alimentazione dalla batteria.

Il piano di qualifica è quindi diviso in due parti: la qualifica Safety of Flight (SOF) e la Full Flight (FULL). Queste due fasi di qualifica devono essere eseguite in sequenza. In effetti, la qualifica SOF deve essere prima completata, poiché contiene i requisiti fondamentali affinché il sistema di alimentazione possa eseguire i primi voli sperimentali. Una volta completata questa parte del processo di qualifica, si può procedere a completare la certificazione per il raggiungimento della FULL. Il raggiungimento delle due qualifiche prevede:

- Test funzionali per dimostrare che tutte le prestazioni dell'unità oggetto di qualifica soddisfino i requisiti imposti dal cliente.

- Test di tipo ambientale che verificano che in tutte le condizioni ambientali richieste dalla specifica dei requisiti del cliente l'unità funzioni correttamente senza subire danni o degrado delle sue prestazioni o funzionalità. Gli standard di riferimento sono la RTCA/DO-160G e la MILSTD810G.
- Test di Compatibilità Elettromagnetica (EMC/EMI) verificano che le unità oggetto di qualifica non siano suscettibili quando sottoposti ad interferenze elettromagnetiche o non emettano disturbi elettromagnetici che possano influenzare il comportamento degli apparati montati nelle loro vicinanze. Per quanto riguarda i limiti previsti durante i test, la normativa di riferimento è la RTCA/DO-160G.

Alla fine di ogni test di qualifica l'unità deve essere testata per garantire che ogni componente non abbia subito nessun danneggiamento o calo di performance. Allo stato attuale il progetto in questione ha già raggiunto la certificazione SOF ed i test associati alla FULL non sono ancora stati condotti ma verranno solo indicati. Vengono riportati i risultati dei test solo per la qualifica SOF di prestazione elettrica condotti sull'impianto di distribuzione.

Ho lavorato personalmente all'intero processo di qualificazione (durato sei mesi) di questo sistema di distribuzione di energia per uso aeronautico, e ho svolto tutte queste prove personalmente. Sono stato anche coinvolto nello sviluppo del prodotto, come la modifica di procedure di test avanzate e l'ottimizzazione dell'efficacia della schermatura EMI.

# Table of contents

# 1 INTRODUCTION

In this thesis, the qualification plan with all necessary tests and procedures for an aeronautical the Electrical Power Distribution System (EPDS) of the aircraft will be investigated in order to obtain the qualification to be installed on aircraft to carry out tests in first flight. Specifically, four main components of this Electrical Power Distribution System will be analyzed in detail: AC Power Distribution Panel (AC PDP 1 and AC PDP 2), DC Power Distribution Panel (DC PDP 1 and DC PDP 2), Battery PDP and Fuse Box.

In the first chapter, the three units will be described from a technical point of view, thus giving a detailed light on their main features and how the different components interface with the aircraft and with each other.

The second chapter will give a deep investigation on the preliminary tests that have to be conducted on the units in order to prove their correct operation from the electrical and mechanical point of view, in two different phases: at the beginning and at the end of a qualification test, having as reference the documentation of Acceptance Test Procedure (ATP).

The third chapter will have as main focus the Qualification Test Procedure (QTP). The QTP is divided in two main parts: SOF and FULL. The SOF qualification includes the tests that have to be done on the various components to guarantee the minimum requirements for flying. Instead, the FULL qualification concerns all the other tests that have to be completed to conclude the qualification plan.

The QTP describes in a precise and detailed way all the tests necessary for a component to be enabled to be mounted on an aircraft to take the first flight. All these tests, in addition to being passed, must comply with the strict standards that are listed in chapter §7.2 of the appendix.

The last section of Qualification Test Results analyzed a detailed computational analysis of the effectiveness of vent hole size shielding. The hole size, thickness-hole depth, and hole-to-hole separation distance were investigated in this analysis using finite time domain simulation. Additionally, a mathematical relationship centered on these same parameters was introduced and demonstrated to accurately predict simulation data for AC PDP 1. Finally, data from experimental measurements performed in an EMC/EMI laboratory are used to validate the simulation and analytical prediction.

Thanks to these focused analysis, there will be presented relevant results both on the ATP and on the QTP part of the Electrical Power Distribution System, which will be discussed in the final chapter.

# 2 SYSTEM DESCRIPTION AND SPECIFICATIONS

## 2.1 GENERAL

The Electrical Power Generation and Distribution System on the X Military Helicopter comprises of 3 phase 115 V AC and 28 V DC system. AC System is composed of two Power Distribution Panels AC PDP 1 and AC PDP 2 (for confidentiality there are no photos of the aircraft and not even sensitivedata covered by privacy). The following power sources are under the control of the AC Power Distribution System:

- N°2 Brushless Starter Generators (S/G 1 and S/G 2)
- N°1 AC External Power Unit (APU)
- N°1 Auxiliary Power Unit (AC EXT Power)

The AC Power Distribution System has the following loads:

- Heaters
- Windshield heater
- Hydraulic pump
- N°2 Transformer Rectifier Unit (TRU)
- Starter Rectifier Unit (SRU)

AC PDP 1 serves as the primary interface between the AC Starter/Generator 1 and the AC External Power Supply. Additionally, provisions are provided for the supply of the AC power Starter/Generator 2 and Auxiliary Power Unit in the event that the AC Generator 1 is unable to generate power.

AC PDP 2 serves as the primary interface between AC Starter/Generator 2 and the AC Auxiliary Power Unit. AC Power Distribution Panels contain all of the circuit breakers, power contactors, power relays, and overload sensors necessary to manage electrically powered aircraft.

A 9 kW Transformer Rectifier Unit distributes AC electrical power from AC Bus 1 to the DC Electrical Distribution System. The DC system is divided into three distribution panels (PDPs): DC PDP 1, DC PDP 2, and Battery PDP.

DC PDP 1 and DC PDP 2 are power distribution panels that contain the power contactor and associated control relays required to connect TRUs to Generator Buses for generation. They also include the power contactors, overload protection, and isolation devices that are used to protect and support Emergency Buses. Additionally, they incorporate a current sensor and a Fault Isolation Logic (FIL) Board, which is in charge of current protection and fault isolation.

The Battery PDP contains the circuit breakers, current sensors, and contactors, as well as the accompanying control relays, required to regulate and protect the external power and battery connection to the aircraft's electrical network through emergency busses. The Battery PDP contains two PCPs: one to manage the external power contactor and another to protect the internal components of PDP from lightning.

The two TRUs are the power source of the DC Power Distribution System. The other DC power sources are the Battery and the DC External Power Unit.

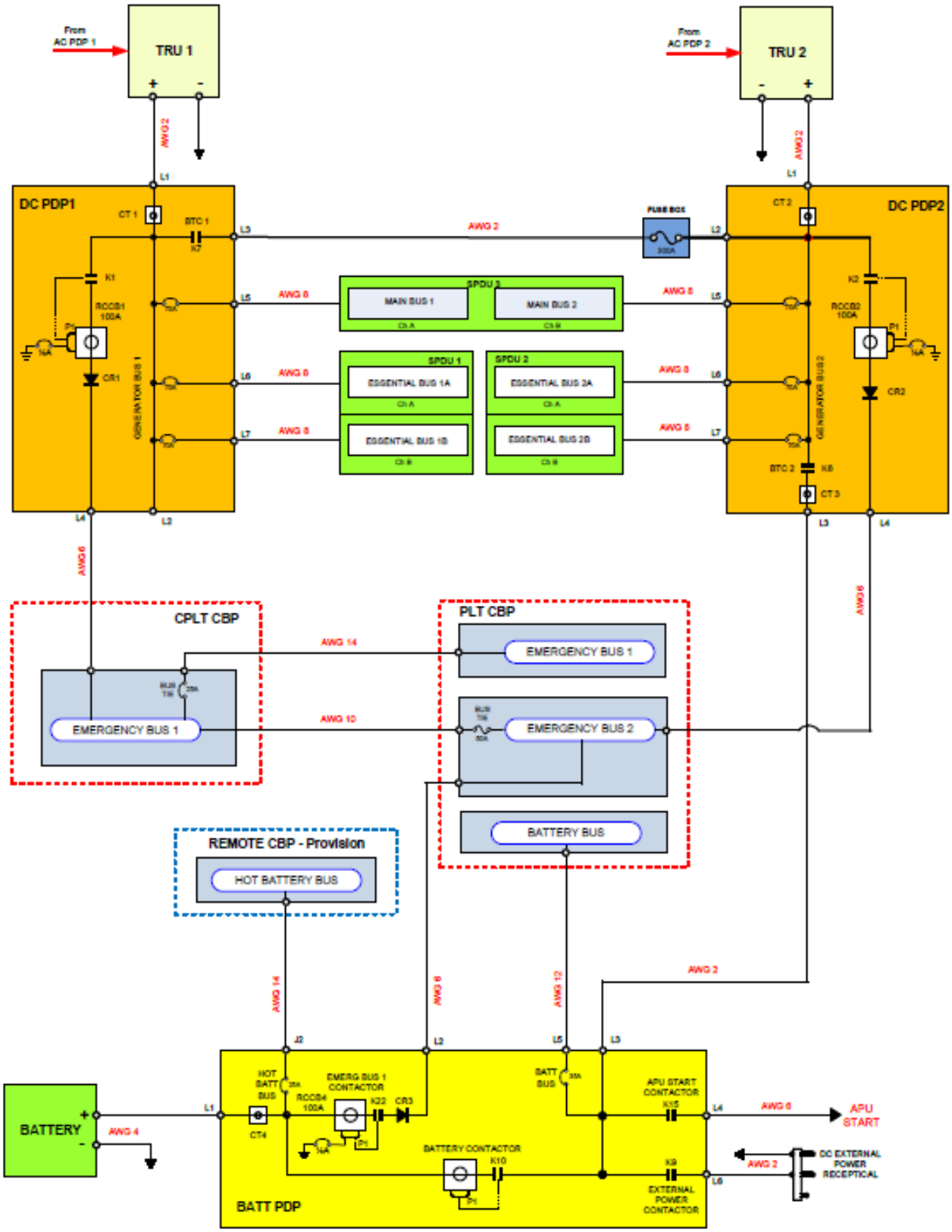


Figure 1: DC Generation System Block Diagram.

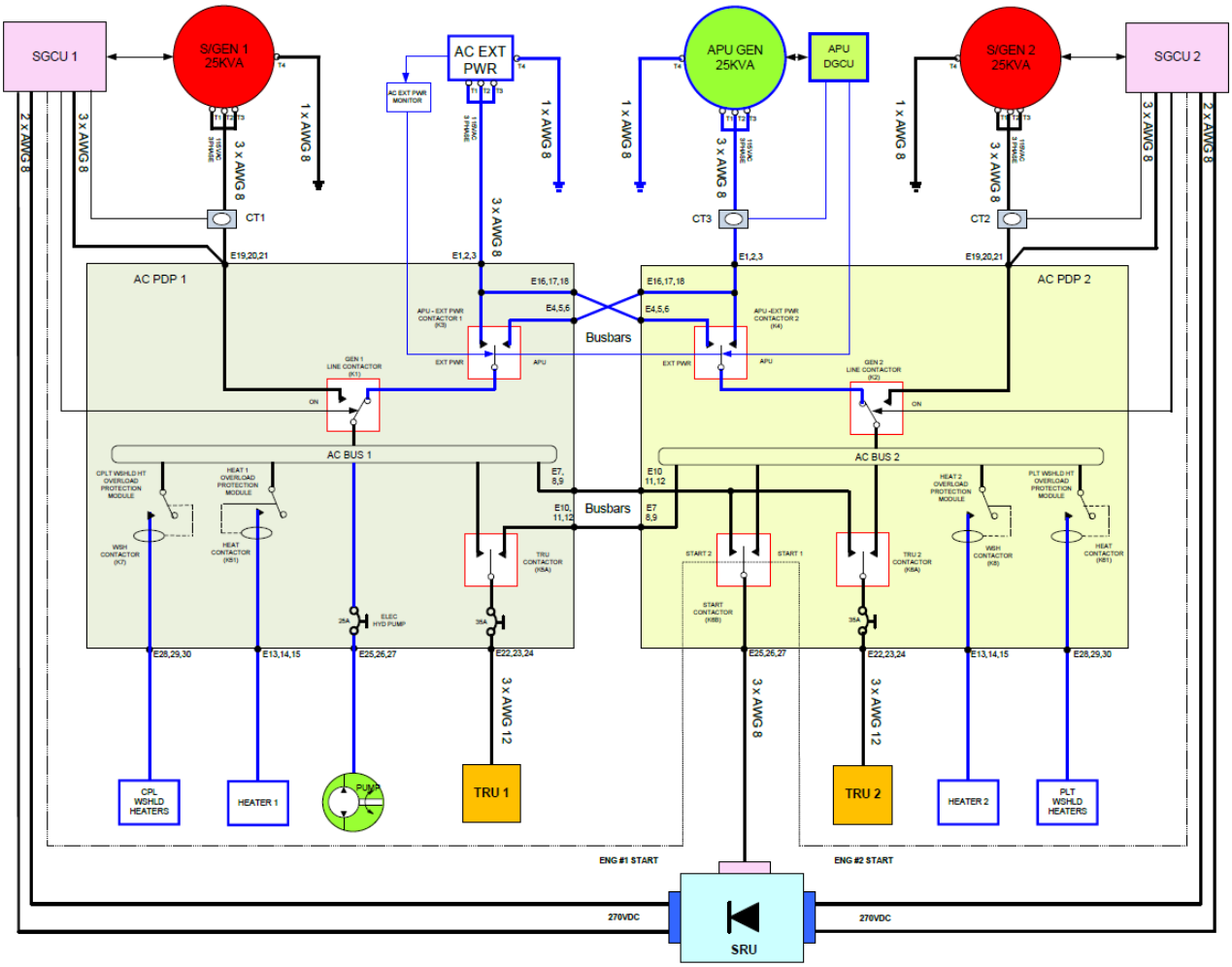


Figure 2: AC Generation System Block Diagram.

## 2.2 AC ELECTRICAL POWER DISTRIBUTION SYSTEM

### 2.2.1 AC PDP 1

The purpose of this first part is to describe the design, performance and qualification requirements for the AC Power Distribution System. The function of the AC Electrical Power Distribution System is to take power from the available power sources and supply it to the appropriate distribution components in accordance with the operational requirements of the aircraft. The system shall provide also protection and communication functions to the helicopter. The system will be connected to the AC Starter Generators, the AC Emergency APU and the External Power of the helicopter. A 3D view of AC PDP 1 is presented in Figure 3.


Figure 3: 3D view of AC PDP 1.

The functions of AC PDP 1 are the following:

- Reconfigure the AC networks to guarantee flight safety;
- Protect themselves against internal short circuits;
- Protect themselves against external short circuits (transfer line, feeders);
- Protect the AC Electrical Distribution networks;
- Provide interface with AMMCs and SGCUs;
- Ensure its own Testability.

The Figure 4 identifies the AC distribution interfaces of AC PDP 1:

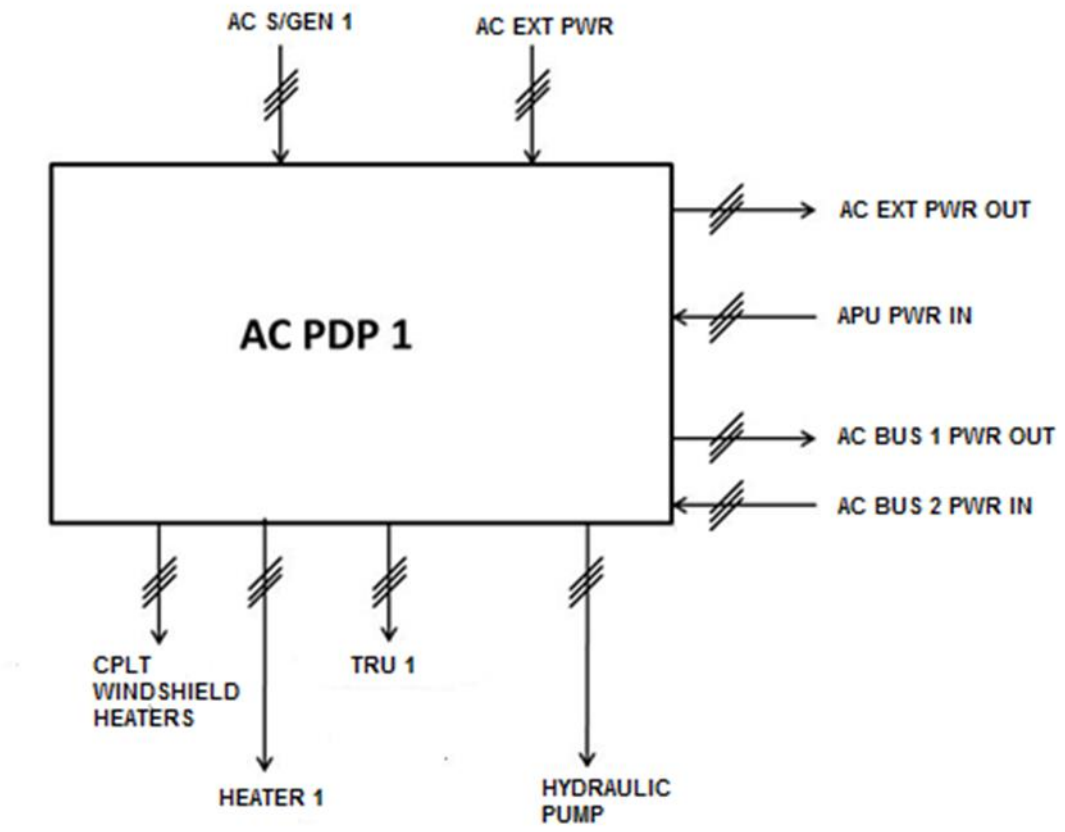


Figure 4: AC PDP 1 interface block diagram.

#### 2.2.1.1 Overload Protection Module Description

The Overload Protection assembly is a PCB dedicated to overcurrent protection for the following loads: co-pilot Windshield heaters and Heater 1. The PCB has two separate circuits, each with its own interface connector, that protect the feeder bus between AC BUS 1 and the loads. Both circuits have the same overcurrent curve, so they protect the feeder bus between AC BUS 1 and the loads. The module monitors the current supplied by each phase of the protected circuit feeder cables and detects the event of overload or short circuit, single phase and 3 phase fault that exceeds an overcurrent trip curve.

The block diagram of the module is represented in
Figure 5.

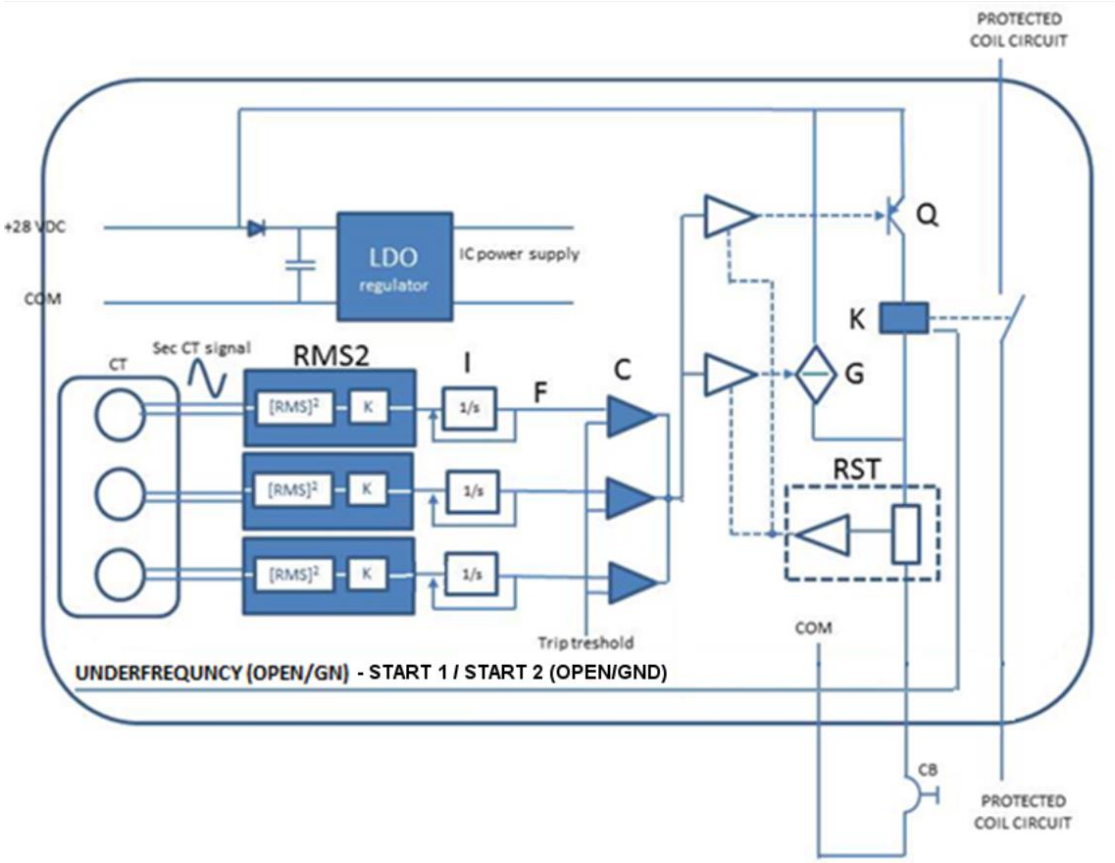


Figure 5: Overload Protection block diagram

It is composed by the following sections:

1. CT: Three single phase current transformers (defined further on)
2. LDO: Low Dropout regulator, it provides single power supply to ICs, compatible with abnormal surge voltage DC (80 V cat. Z)
3. RMS2: it calculates RMS value of the CT signal and reports the square value at the output with an adaptable gain
4. I: it integrates the signal from RMS2 with output limit and dead zone
5. C: comparator that sets the trip signal to command the protection:
   - flip flop 1 commands the relay K
   - flip flop 2 commands the current generator G
6. K: protection relay that closes the contact in series to the coil of the protected external contactor
7. G: 2A current generator, thermal protected
8. RST: Reset circuit:
   - when detects CB open it resets the flip flop that commands G when CB is closed by crew for reset purpose it resets the flip flop that commands K

This module operates in conjunction with the LH Windshield Heating Contactor to provide overload protection (K7). The module is rated for a load current of 25 A rms. The module generates a trip curve that matches up to the "non-intervention" curve depicted in Figure 6:

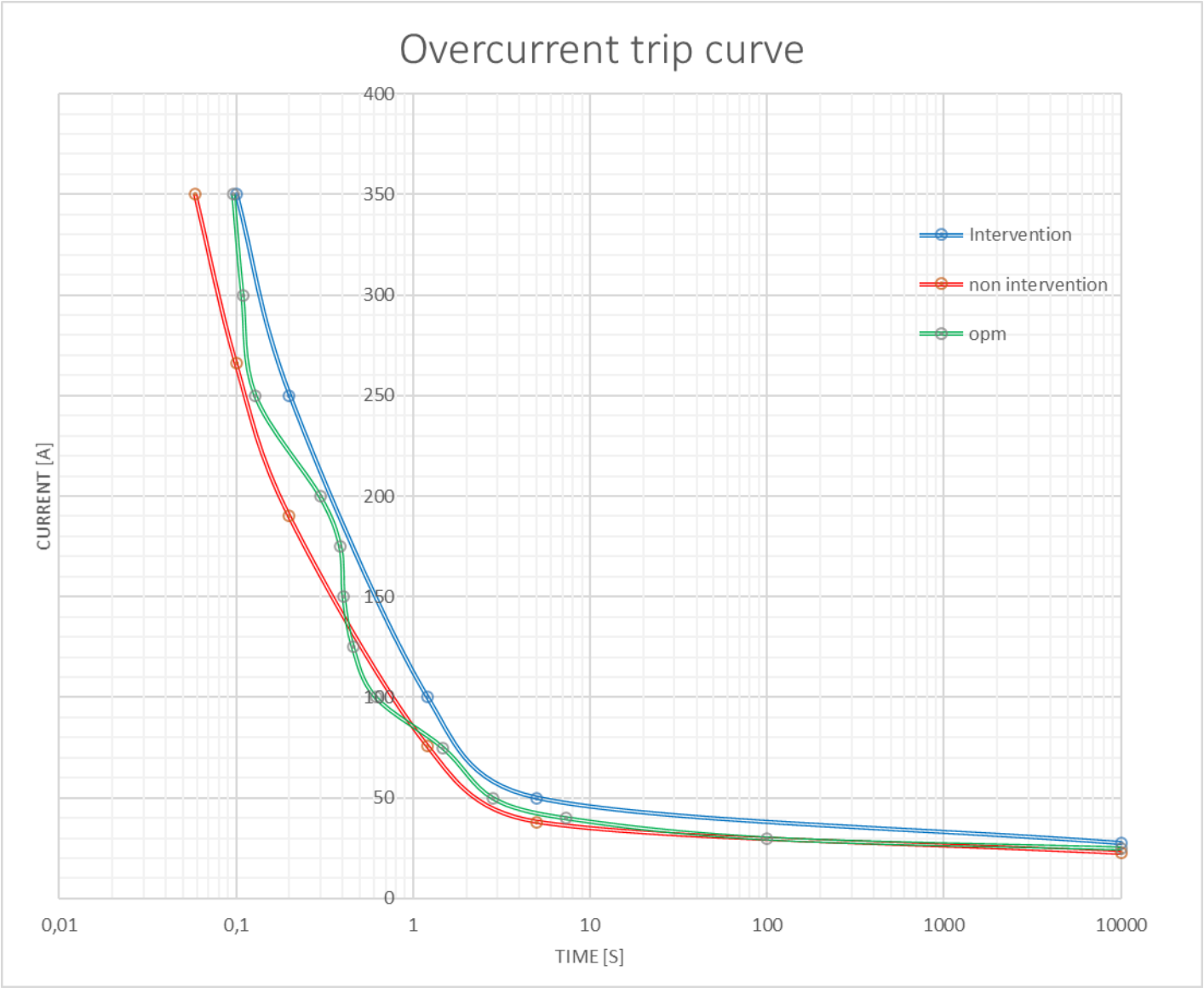


Figure 6: Overcurrent Protection Module trip curve

This module operates in conjunction with the associated contactor to provide overload protection. The module, in combination with its associated contactor, protects loads with the following ratings:

115/200 V 3 phase 314/400 Hz

#### 2.2.1.2 Auxiliary Circuits Assembly Description

AC PDP 1 incorporates an assembly realized with a PCB that is dedicated to perform the function. It contains the following sections:

- Diodes in series to the coils of contactors and relays to avoid the inversion of polarity (one diode for each coil)
- Transient voltage suppressors for protection of OPM circuits against lightning
- Transient voltage suppressors for protection of coils against lightning
- Fuses in series to the voltage monitoring interface (POR sense) at the input of Generator Line contactor (three fuses, one for each phase).

### 2.2.2 AC PDP 2

A 3D view of AC PDP 2 is presented in Figure 7.


Figure 7: 3D view of AC PDP 2

AC PDP 2 is the primary interface with AC Starter/Generator 2 and also provides an interface with the AC APU supply. In both cases, appropriate rated 3 phase contactors are used to switch AC power from the sources to a distribution bus bar, AC BUS 2.

Furthermore, provision is made for the supply of AC power from AC Starter/Generator 1 or AC External Power in the event that power from AC Generator 2 is unavailable.

A 9 kW TRU distributes AC power from AC Bus 2 to the DC EPDS. AC PDP 2 also includes proper current transformer assemblies for circuit protection. The AC PDP 2 also includes the necessary current transformer assemblies for circuit protection.

An AC PDP 2 high level internal schematic is defined in Figure 8.

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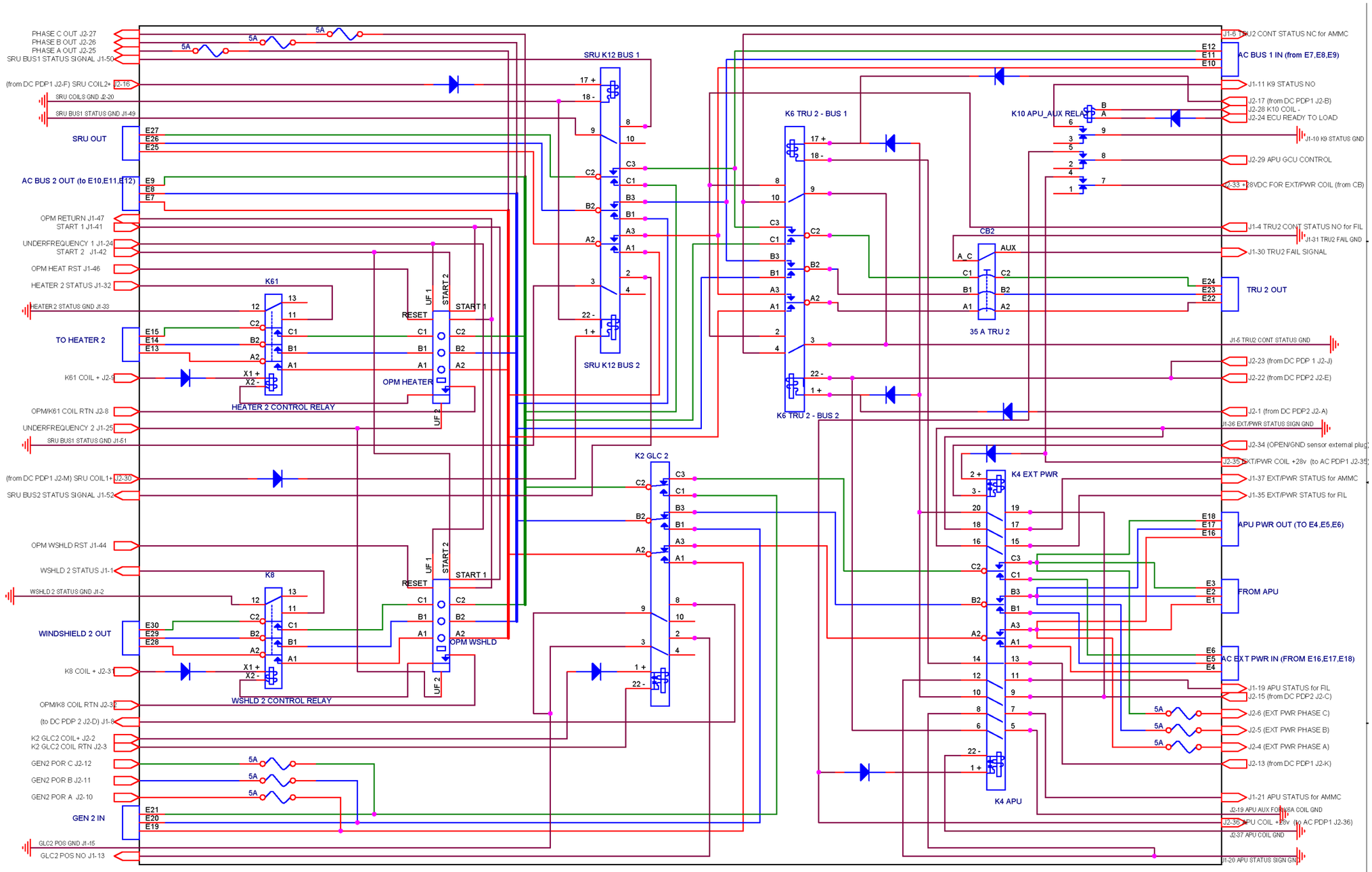



Figure 8: AC PDP 2 high level internal schematic

#### 2.2.2.1 AC PDP 2 FUNCTIONS

The functions of AC PDP 2 are the following:

- Reconfigure the AC networks to guarantee flight safety;
- Protect themselves against internal short circuits;
- Protect themselves against external short circuits (transfer line, feeders);
- Protect the AC Electrical Distribution networks;
- Provide interface with AMMCs and SGCUs;
- Ensure its own Testability.

The following Figure 9 identifies the AC distribution interfaces of AC PDP 2:

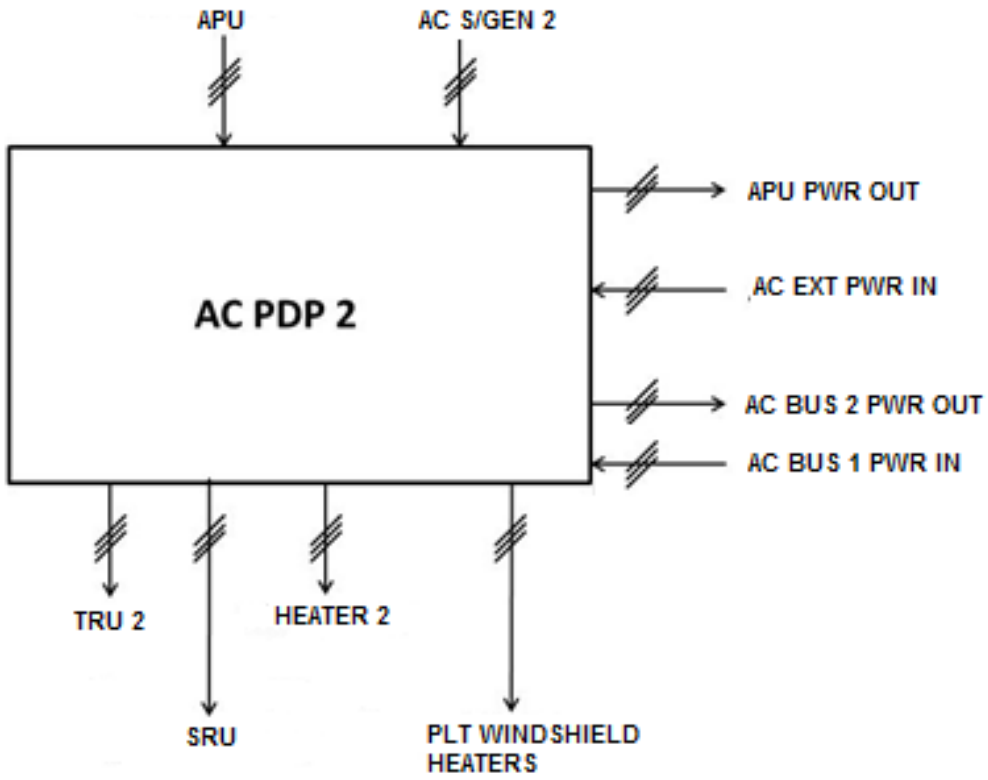
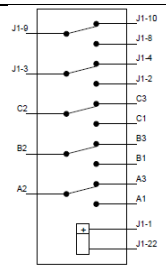
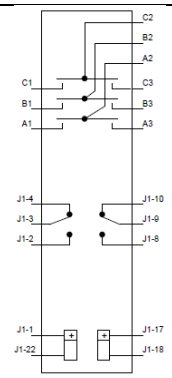
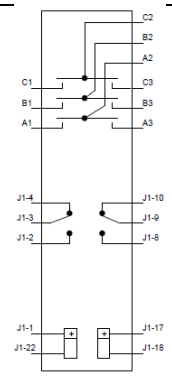
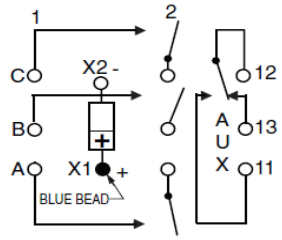
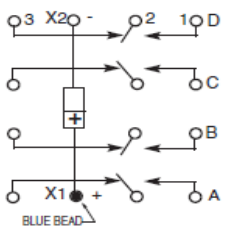



Figure 9: AC PDP 2 interface block diagram.

### 2.2.2.2 MAIN COMPONENTS DESCRIPTION

Table 1: AC PDP2 Contactor and relay list

| ID | P/N | Manufacturer | Function | |
|---|---|---|---|---|
| K2 | L-A7N-011 | Leach Esterline | GEN2 Line Contactor |  |
| K4 | LC-B9N-017 | Leach Esterline | AC EXT PWR & APU Contactor |  |
| K6 | LCA5A | Leach Esterline | TRU 2 Contactor |  |
| K12 | LCA5A | Leach Esterline | SRU Contactor | |
| K8 | FCAC-325-CX3 | Tyco | PLT WSHDL Heater Contactor |  |
| K61 | FCAC-325-CX3 | Tyco | Heater 2 Contactor | |
| K10 | FCB-405-AY3 | Tyco | DGCU APU Auxiliary Relay |  |

The preceding table illustrates that only two distinct contactor or relay manufacturers were used in the design of the AC PDP. Only one example is given below for each contactor or relay, along with detailed information about the characteristics that influenced our selection.

**GLC2 – GENERATOR 1 LINE CONTACTOR DESCRIPTION (K2):**
GLC2 is the Generator 2 Line Contactor. GLC2 is a 3 pole, double throw contactor that connects 3 phase 115VAC electrical power from AC S/GEN 2 or the alternative APU/AC EXT PWR source to AC BUS 2.
The part number is **L-A7N-011 Leach Esterline**.

**K2 coil data:**

| | |
|---|---|
| Nominal operating voltage | 28 V DC |
| Maximum operating voltage | 29 V DC |
| Pick-up voltage | 18 V DC maximum (20 V at high temperature test) |
| Drop-out-voltage | 7 V DC maximum |
| Resistance at 25 °C | 65 Ohms ± 10% |
| Current at 25 °C & 28 V dc | 0.400 A |
| Coil Transient Suppression | 42 V max |

**K2 contacts data:**
MAIN

| | |
|---|---|
| Type | 2 poles double throw |
| Voltage | 115 V ac 400 Hz 3Φ / 28 V DC |
| Current ac | 90 A resistive/inductive/motor |
| Overload at 115/200 V ac 400 Hz | 630 A |
| Rupture at 115/200 V ac 400 Hz | 900 A |
| Operate (Pick-up) time at coil nominal voltage (including bounces) | 0.040 sec maximum |
| Release (Drop-out) time at coil nominal voltage (including bounces) | 0.100 sec maximum |
| Contact voltage drop at rated load | 150 mV |

AUXILIARY

| | |
|---|---|
| Type | 1 sets 2 poles double throw |
| Voltage | 115 V AC 400 Hz / 28 V DC |
| Current | 5 A resistive<br>3 A inductive |

**PLT WSHLD HT CONTACTOR (K61):**
PLT WSHLD HT Contactor is used to provide power for the heating system of the windshield for co-pilot position in the helicopter. PLT WSHLD HT is a 3 pole, double throw contactor to connect 3 phase 115VAC electrical power from AC BUS 2 to the PLT Windshield Heating System.
The part number is **FCAC-325-CX3 Tyco.**

**K61 coil data**

| | |
|---|---|
| Nominal operating voltage | 28 V DC |
| Maximum operating voltage | 30.8 V DC |
| Pick-up voltage | 18 V DC maximum |
| Drop-out-voltage | 7 V DC maximum |
| Resistance at 25 °C | 290 ohms ± 10% |
| Current at 25 °C & 28 V dc | 0.097 A |

**K61 contacts data:**

MAIN

| | |
|---|---|
| Voltage | 115 V AC 400 Hz 3Φ / 28 V DC |
| Current ac | 25A resistive - inductive 12A – motor 10A |
| Overload at 115/200 V ac 400 Hz | 80 A |
| Operate (Pick-up) time at coil nominal voltage (including bounces) | 0.015 sec maximum |
| Release (Drop-out) time at coil nominal voltage (including bounces) | 0.015 sec maximum |
| Voltage drop at rated load | 175 mV |

AUXILIARY

| | |
|---|---|
| Type | 1PDT |
| Voltage | 115 V AC 400 Hz / 28 V DC |
| Current | 2 A resistive<br>1 A inductive |

**Preventions adopted for K61 protection:**

The following countermeasures have been adopted with adequate components located in the Auxiliary Circuits Module:

- series diodes to the coil for protection against inversion of polarity
- Transient voltage suppressors against lightning and for limiting exported voltage transients to 42V

**TRU 2 CIRCUIT BREAKER Description:**

This CB is placed on the TRU 2 line, in order to protect it against over current events. It is a 3 poles circuit breaker with auxiliary contact. The part number is **84 313 335 Crouzet.** The current rating is 35 A with a working temperature in the range -55°C/+90°C.

**Overload Protection Assembly Description:**

Overload protection assembly is a PCB dedicated to perform the overcurrent protection for loads: PLT WINDSHIELD HEATERS and HEATER 2.

The PCB has two independent circuits with a unique interface connector, installed in close proximity to the protected contactors such that it enables the maximum protection of the feeder bus between AC BUS 2 and loads, but both circuits performs the same overcurrent curve.

## 2.3 DC ELECTRICAL POWER DISTRIBUTION SYSTEM

### 2.3.1 DC PDP 1 AND DC PDP 2

The Electrical Power Generation and Distribution System on the Aircraft comprises of three-phase 115 VAC system and 28 VDC system. The Electrical Power Distribution Panels (EPDS) includes all the Circuits Breakers, Power Contactors, Power Relays, Functional and Fault Isolation Logic Board, Bus Bars and Overload Sensors to manage the Helicopter DC Power Distribution System.

The AC Electrical Power Distribution System's function is to take power from available power sources and distribute it to the appropriate distribution components in accordance with the aircraft's operational requirements. The system must also provide the helicopter with protection and communication capabilities. The system will be linked to the helicopter's AC Starter Generators, AC Emergency APU, and External Power.

The function of the DC Electrical Power Distribution System is to take power from the available power sources and supply it to the appropriate distribution components in accordance with the operational requirements of the aircraft. The system shall provide also protection and communication functions to the helicopter. The system will be connected to the TRUs of the helicopter.

The Electrical Power Distribution Panels (EPDS) includes all the Circuits Breakers, Power Contactors, Power Relays, Functional and Fault Isolation Logic Board, Bus Bars and Overload Sensors to manage the Helicopter DC Power Distribution System.

The DC EPDS is composed by four items, which are three Power Distribution Panels (PDP 1, PDP 2 and BATTERY) and a FUSE BOX, in order to distribute the DC electrical power available from the following power sources:

- TRU 1 (through AC EPDS)
- TRU 2 (through AC EPDS)
- Battery
- EXT Power (28VDC)

to the following aircraft distribution busses:

- Main Bus 1
- Essential Bus 1
- Main Bus 2
- Essential Bus 2
- Emergency Bus 1
- Emergency Bus 2
- Battery Bus
- Hot Battery Bus

DC PDP1 contains the following contactors and relays:

- K1: Emergency Bus 1 Contactor (DC PDP1)
- K7: Bus Tie 1 Contactor (DC PDP1)
- K13: GLC1 Auxiliary Relay (DC PDP1)

Moreover, DC PDP1 contains also:

1. CT1: TRU 1 Input Hall Effect Current Sensor (DC PDP1) for FIL fault protection for DC network
2. CR1: Emergency Bus Primary Supply Diode (DC PDP1) connected to Emergency BUS1
3. RCCB1: Emergency Bus Primary Remote Controlled Circuit Breaker (DC PDP1) sensing of output current from Emergency BUS 1 contactor

4. 70A CB: Three Circuit Breakers (DC PDP1) protection of line connecting PDP to Buses
5. 7.5A CB: SGCU Power Protection Circuit Breaker (DC PDP1) protection of power lines from PDP to SGCU1

DC PDP2 contains the following contactors and relays:

- K2: Emergency Bus 2 Contactor (DC PDP2)
- K6: Bus Tie 2 Contactor (DC PDP2)
- K14: GLC2 Auxiliary Relay (DC PDP2)

Moreover, DC PDP2 contains also:

1. CT2: TRU 2 Input Hall Effect Current Sensor (DC PDP2) for FIL fault protection for DC network
2. CT3: Bus Tie 2 Output Hall Effect Current Sensor (DC PDP2) for FIL fault protection for DC network downwards DC PDP 2
3. CR2: Emergency Bus Primary Supply Diode (DC PDP2) connected to Emergency BUS2
4. RCCB2: Emergency Bus Primary Remote Controlled Circuit Breaker (DC PDP2) sensing of output current from Emergency BUS 2 contactor
5. 70A CB: Three Circuit Breakers (DC PDP2) protection of line connecting PDP to Buses
6. 7.5A CB: SGCU Power Protection Circuit Breaker (DC PDP2) protection of power lines from PDP to SGCU2

The DC PDP 1 and DC PDP 2 are able to control the fault isolation capability by the use of a dedicated electronic board called “Fault Isolation Logic Board”.

- Command opening and closing of two contactors
- Output two digital signals for fault indication of SGCUs

#### 2.3.1.1 Fault Isolation Logic

Fault Isolation Logic Board will implement a Fault Isolation Logic circuitry that trigger an overcurrent fault condition according to the figure shown below. Fault Isolation Logic Board is powered by an external 28VDC source. Internal circuits use 5VDC and 12VDC sources, derived using a DC/DC converter and a linear voltage regulator.

Upon reception of an overcurrent fault trigger the Fault Isolation Logic Board will initiate the following overcurrent Fault Isolation Logic:

- If CT1 or CT2 or CT3 sense an overcurrent → OVC_OUT active
  → DC PDP 1 shall open BTC1 within 50ms.
- If failure is still present → DC PDP 2 shall open BTC2 within 1s

Any subsequent fault condition risen by the Fault Isolation Logic will be latched until a reset is performed. Fault Isolation Logic overcurrent protection will be inhibited during APU starting phase.

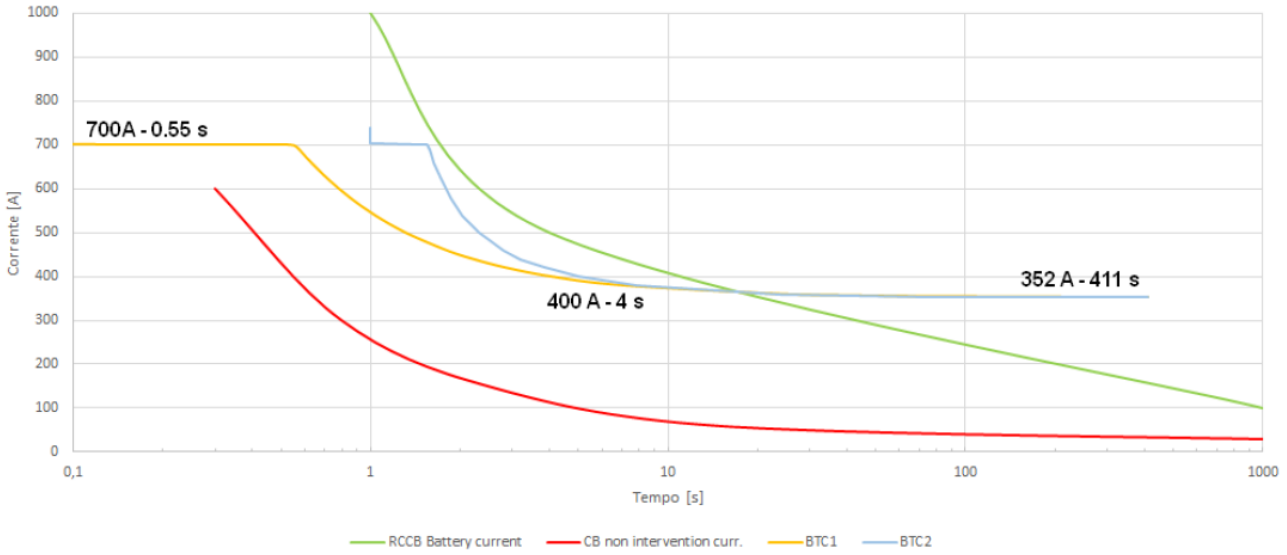



Figure 10: Overcurrent trip curves for BTC1 and BTC2

#### 2.3.1.2 POWER SUPPLY REDUNDANCY

Internal components (such as relays, contactors, and sensors) are powered directly from the 28VDC bus. Thus, to avoid power loss during power bus short circuits, a second redundant power source is drained on the emergency bus after the power diode. All of these power supply lines are protected by 3A or 7.5A circuit breakers and are connected in a reversible fashion via 5A diodes. An external connector provides an additional power supply for the APU GCU and N°2 relays. This output is secured with a 7.5A CB.

### 2.3.2 BATTERY PDP

The DC BATTERY PDP is a power distribution panel that contains the power contactors that connect Generator Bus 2 to external power and aircraft battery supply sources. Additionally, it contains a remote-control circuit breaker and isolation device that enable the battery supply to be connected to Emergency Bus 1. Furthermore, two current sensing devices are included, one for battery overload protection and another for battery current status indication.

An External Power Monitor monitors the external power supply to prevent connecting an unacceptably high voltage supply to the DC power system. The BATTERY contains the following contactors and relays:

- K9 External Power Contactor – EPC (BATTERY)
- K10 Battery Contactor (BATTERY)
- K15 APU Start Contactor (BATTERY)
- K22 Emergency Bus Backup Contactor (BATTERY)

The BATTERY contains also:

1. T8: Battery Current Monitor Sensor (BATTERY) monitor charge/discharge current
2. T9: Battery Current Protection Sensor (BATTERY) monitor battery current for control of K10
3. CR4: Emergency Bus 2 Backup Power Diode (BATTERY) connected between K22 and output to Emergency Bus 2
4. RCCB4: Emergency Bus Backup Remote Controlled Circuit Breaker (BATTERY) sensing of output current from K22

#### 2.3.2.1 DC BATT PDP FUNCTIONS

The DC BATTERY PDP shall:

- Connect the DC Power sources (Battery and DC External Power) onto the busses of the following table:

| NAME |
|---|
| HOT BATTERY BUS |
| MAIN BUS 2 |
| BATTERY BUS |
| EMERGENCY BUS 1&2 |

  - Reconfigure the DC networks to guarantee flight safety;
  - Protect the DC networks against DC Power Source failures;
  - Protect themselves against internal short circuits;
  - Protect themselves against external short circuits (transfer line, feeders);
  - Protect the DC Electrical Distribution networks;
  - Ensure the starting functions for APU;
  - Monitor the Battery and monitor the battery warning up;
  - Monitor the DC EXT/PWR;
  - Provide interface with AMMCs;
  - Ensure its own Testability.

The high level internal schematic of Battery PDP is given below.

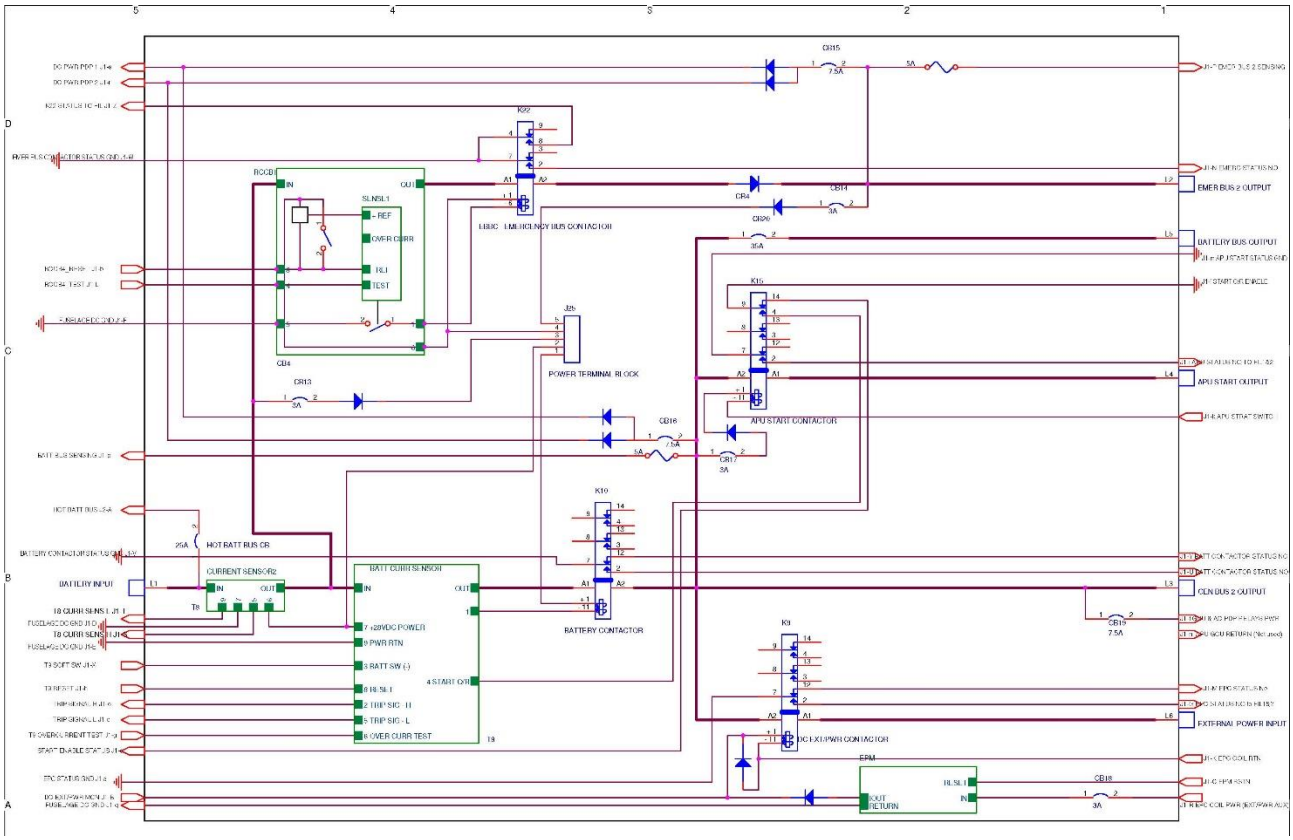



Figure 11: DC BATTERY PDP high level internal schematic

### 2.3.2.2 HOT BATTERY BUS CIRCUIT BREAKER DESCRIPTION (PROVISION)

This CB is placed directly on battery input line, in order to protect it against over current events. It is a single poles circuit breaker with auxiliary contact. The part number is **84 306 325 Crouzet.** The current rating is 25 A with a working temperature in the range -60°C/+125°C.
The CB trip intervention curve is given in Figure 12.

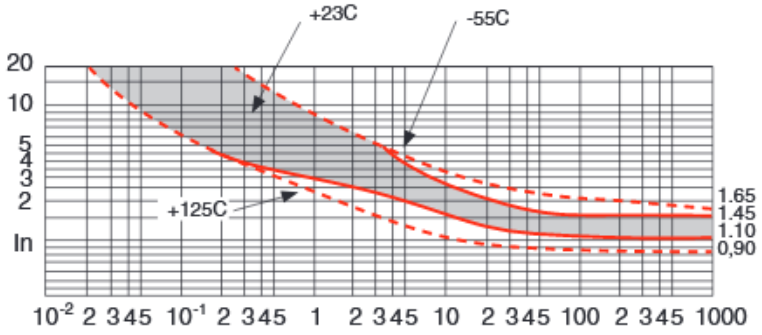



Figure 12: Hot Battery and Battery Bus CB trip curve

**BATTERY BUS CIRCUIT BREAKER DESCRIPTION:**
This CB is placed on the Battery Bus output, in order to protect it against over current events. It is a single pole circuit breaker with auxiliary contact. The part number is **84 306 335 Crouzet.** The current rating is 35 A with a working temperature in the range -60°C/+125°C.

Figure 12 illustrates the CB trip intervention curve.

### 2.3.2.3 EXTERNAL POWER MONITOR (EPM) BOARD

DC BATTERY PDP incorporates a method for monitoring the external power supply in order to avoid connecting an unacceptable overvoltage supply to the DC power system or disconnecting the external power supply in the event of under-voltage. If the external supply voltage limits of trip curve are exceeded, the sensor monitoring circuit (EPM) will provide an open control signal to prevent the EPC from being closed. The EPM shall monitor the DC voltage at the input terminals of the External Power Contactor. When an over voltage condition is detected, the EPM opens the External Power Contactor and latches the alarm. Additionally, the EPM will include a RESET function that will allow this alarm to be unlatched. The RESET function will be performed via an externally supplied Ground signal pulse.

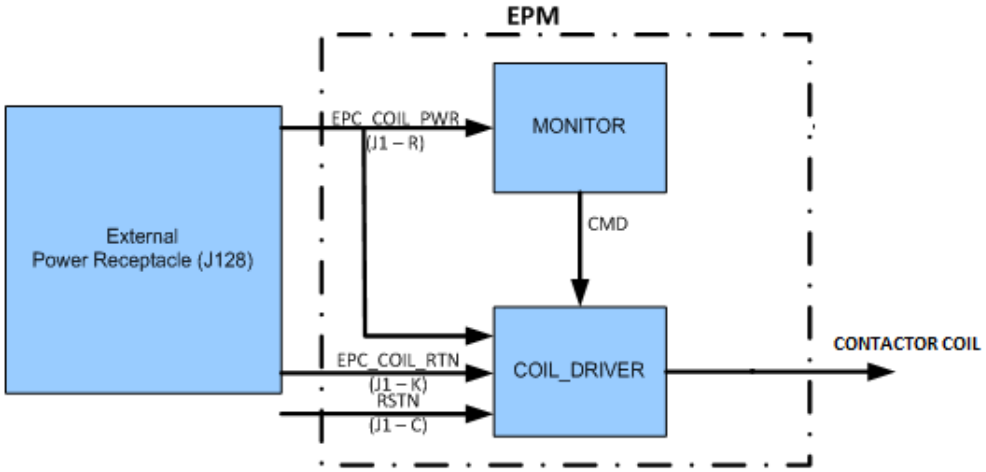



Figure 13: EPM Board

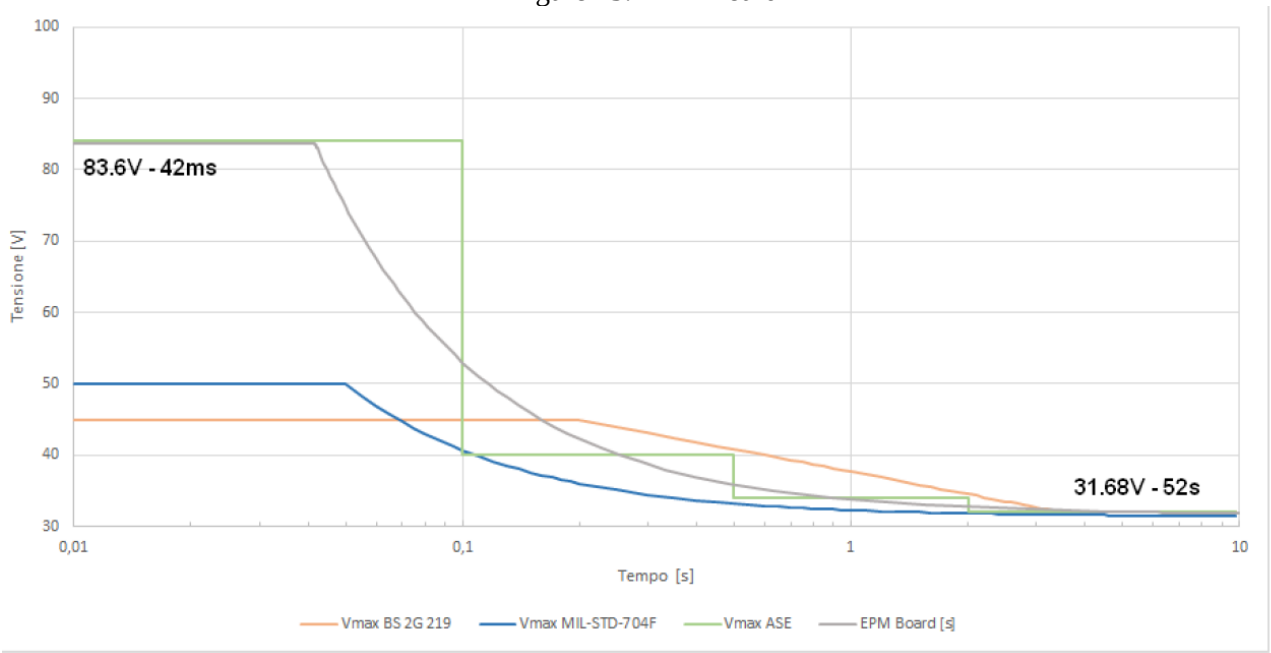



Figure 14: External Power Overvoltage trip curve

# 3 PRODUCT ACCEPTANCE TEST PROCEDURE

## 3.1 GENERAL

In this chapter it is described the Product Acceptance Test Procedure of the entire EPDS system. The purpose of the Acceptance Test Procedure (ATP) is to verify that the unit under test works properly following the general specifications. PATS (or simply ATP) means a series of tests aimed at ascertaining whether the machines comply with the design parameters and are able to guarantee the project performance. Several relevant standards were considered during the preparation of this procedure, which must conform to them. All the specific and technical information presented in this chapter is based on military and industrial standards.

ATPs are the basis of the whole qualification process and are performed before each sequence of tests valid for the qualification that will make these components suitable for use on an aircraft. The following chapter explains in detail the main operations to perform an ATP and the main tests that are performed on the machines.

## 3.2 STATIC TESTS FOR AC PDP

### 3.2.1 ELECTRICAL CHARACTERISTICS

The AC PDP interfaces the utilization equipment AC power generation system that has the following characteristics:

- Nominal voltage of 115VAC (line to neutral/line to line).
- Variable frequency nominally in 400 Hz.
- Phase sequence of A-B-C.
- Neutral connected to airframe.

### 3.2.2 BONDING AND GROUNDING

The PDP chassis presents a continuous low-impedance from the mounting pads to the aircraft structure. As a general definition, the bonding structure is the surface that mates to the aircraft structure. In order for the machines to be suitable for qualification, the resistances between the different metal components must be measured and verified:

1. The maximum resistance between the circular connector and the bonding structure must be 2.5mΩ.
2. The maximum resistance between the top cover and the bonding facility must not exceed 2.5mΩ (perform the measure on the internal corner of top cover).

### 3.2.3 CONTINUITY AND DIODES CHECK

The DC power supply is set to 28 VDC + 0.5 V and 100 mA, and it is connected to the pins under test, which are connected to the related diodes. The aim of these test is to verify the presence of the freewheeling diode between pins of the AC PDPs:

1. The voltage V diode from pin (high) toward another pin (low) shall be less than 15V.
2. The measure from pin B (high) toward pin C (low) shall be an open circuit (diode with inverse polarization).

### 3.2.4 HIGH VOLATGE INSULATION RESISTANCE

Insulation resistance between the PDP chassis and the circular connector pins is at least 20 MΩ at 500 VDC (Auxiliary circuits assembly and overload protection assembly must be disconnected for this test). The insulation resistance of the PDP must not be less than 10 MΩ with 500 VDC ± 5 VDC between test points.

### 3.2.5 LOW VOLTAGE INSULATION RESISTANCE

The insulation resistance of the PDP shall not be less than 10 MΩ with 30 VDC ± 5 VDC between the test points

### 3.2.6 DIELECTRIC STRENGHT

The PDP chassis to power terminations is isolated to withstand 1500 VAC RMS for 5 seconds or 1000 VAC RMS 50 or 60 Hz for 1 minute between pins, with no disruptive discharge and a leakage current of less than 15 mA (auxiliary circuits and overload protection assemblies must be disconnected for this test). It must be able to handle the voltages below when the main contacts of each contactor are open.

## 3.3 DYNAMIC TESTS FOR AC PDP

### 3.3.1 CONTACTORS OPERATION CHECK

The purpose of this test is to verify that each contactor and relay drains the correct amount of current from the DC power supply and that the resistance between the appropriate pins on the ATP test box is less than 500mΩ.

### 3.3.2 NO LOAD OPERATION CHECK

The AC1 power supply is set to 115 VAC 1 VAC and connected to the input studs E7, E8, and E9. DC1 output voltage is adjusted to 28 VDC 0.1 VDC with current limitation set to 3.0A 0.1A and connected to the ATP test box 28 VDC input of test bench. This ATP test box is connected to an AC PDP for the purpose of verifying that the input and output phases are in phase, as well as the opening and closing time of contactors and relays in no load condition.

### 3.3.3 VOLTAGE DROP OPERATION CHECK

The purpose of this test is to determine the voltage drop between the input and output studs while a resistive load bench is connected and absorbing 10A.

### 3.3.4 OVERCURRENT PROTECTION MODULE CHECK

For AC PDP 1, the OPM board is connected to K7-copilot windshield relay and K51-heater relay (K8 and K61 relays for AC PDP 2). The output studs of these relays are connected to the appropriate resistive load bench. The purpose of this test is to verify that the OPM intervention time (between current injection and interruption, with reference to oscilloscope channel 1) is less than the value reported in the table, as well as to verify that the CB HT and CB WS intervention in the ATP Test Box.

| TEST | Three-phase current [A] | Intervention Time [s] |
|---|---|---|
| 1 | 20 ± 2 | 600 ÷ 610<br>NON INTERVENTION |
| 2 | 39 ± 2 | 10 ÷ 35 |
| 3 | 70 ± 2 | 2 ÷ 3.5 |

### 3.3.5 TRANSIENT VOLTAGE SUPRESSOR CHECK

Silicon transient voltage suppressors (TVS) are clamping devices that limit voltage spikes by low impedance avalanche breakdown of a rugged silicon p-n junction. They are used to protect sensitive components from electrical overstress such as that caused by induced lightning, inductive load switching, and electrostatic discharge. When a transient appears, the TVS becomes active, clamping it to a harmless level. Its electrical parameters-such as breakdown voltage ($V_{BR}$), leakage current ($I_D$), and capacitance-should be "invisible" to the circuit and have no effect on performance. The reverse standoff voltage ($V_{WM}$), which approximates the circuit operating voltage, is normally 10% below breakdown voltage. This assures minimal standby leakage current and compensates for voltage excursions caused by temperature variations. The TVS clamps instantly when transients occur, limiting the spike voltage to a safe level while diverting damaging currents away from the protected part.

**TEST PROCEDURE:**

1. Set the DC2 Power Supply to 125 VDC ± 1 VDC, 300 mA ± 10 mA output limited. This value is NOT the output current limit which tables below refer to.

2. Connect DC2 Power Supply positive pole to “DC2 +” terminal and negative pole to “DC2 –” terminal of A946.4W test bench.
3. Set the pulse generator such as a single square wave will be generated (amplitude 5 V, duration 10ms) moving the selector SW2 in the correct position as required by Table 2 and
4. Table *3*.
5. Connect the oscilloscope to “SCOPE +” (positive) and “SCOPE –” (negative) pins. Output current is limited by means of resistor switching as shown in following figure.
6. Connect “TVS1 OUT” (positive) and “TVS2 OUT” (negative) terminals to the pins given in Table 2 and
7. Table *3* with the output current limited as detailed in those Tables. Verify that the TVS clamping voltage is within the limits.

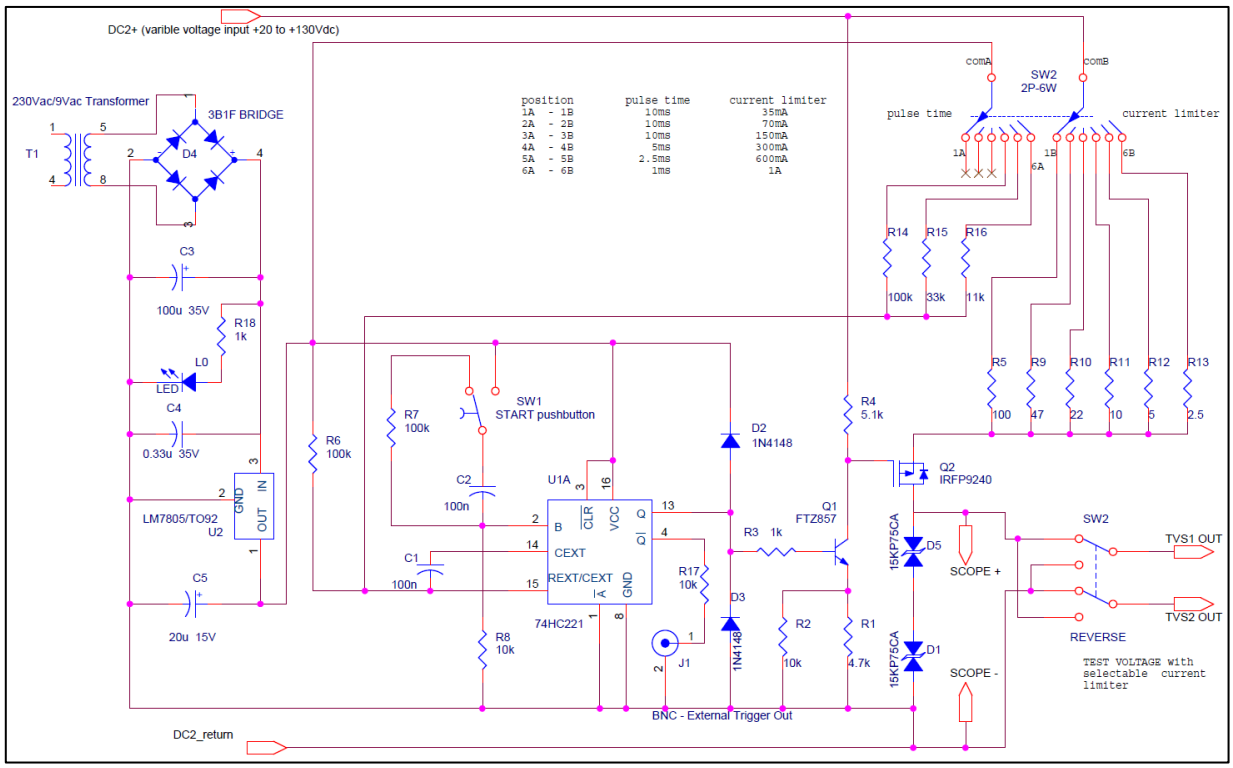



Figure 15: TVS check electrical connection.

Table 2: TVS Direct Test 1 for AC PDP 2

| DIRECT TEST | | | | |
|---|---|---|---|---|
| PULSE CONFIGURATION | | | TVS under test | LIMITS |
| Out POS | Out NEG | LIMITATION | | |
| J2-2 | J2-3 | 35 mA ± 5 mA | D9 | 80 ÷ 110 VDC |
| J2-1 | J2-22 | 35 mA ± 5 mA | D31 | 80 ÷ 110 VDC |
| J2-17 | J2-13 | 35 mA ± 5 mA | D33 | 80 ÷ 110 VDC |
| J2-16 | J2-20 | 35 mA ± 5 mA | D25 | 80 ÷ 110 VDC |
| J2-30 | J2-20 | 35 mA ± 5 mA | D19 | 80 ÷ 110 VDC |

Table 3: TVS Reverse Test 1 for AC PDP 2

| REVERSE TEST | | | | |
|---|---|---|---|---|
| PULSE CONFIGURATION | | | TVS under test | LIMITS |
| Out POS | Out NEG | LIMITATION | | |
| J2-3 | J2-2 | 35 mA ± 5 mA | D10 | 30 ÷ 50 VDC |
| J2-22 | J2-1 | 35 mA ± 5 mA | D32 | 30 ÷ 50 VDC |
| J2-13 | J2-17 | 35 mA ± 5 mA | D34 | 30 ÷ 50 VDC |

| | | | | |
|---|---|---|---|---|
| J2-20 | J2-16 | 35 mA ± 5 mA | D26 | 30 ÷ 50 VDC |
| J2-20 | J2-30 | 35 mA ± 5 mA | D20 | 30 ÷ 50 VDC |

# 4 QUALIFICATION TEST PROCEDURE (QTP)

## 4.1 GENERAL

The Qualification Test Procedure (or simply QTP) indicates all the tests necessary for the machines to obtain flight qualifications for tests on a prototype aircraft. The machines can be considered fit for flight only if all the tests in the QTP are successfully passed. The two macro areas in which the QTP is divided are: SOF and FULL qualification. The SOF qualification includes: electrical system performance, environmental and EMI tests. As in the previous chapter, all technical and numerical information refer to different standards and specifications that will be reported in the "Reference" section. The following chapter only concerns the Safety of Flight qualification plan that allows the treated components to be installed on a prototype aircraft to perform tests in flight. In order for these components to be suitable for series production, additional tests must be carried out in the FULL qualification plan which is not the subject of this thesis (Figure 16).

**Test Site:**
All "S/G Channel Performance" Tests and all ATPs were carried out in the Special Test Department of ASE S.p.A. Via Verdi, 33 - 20010 San Giorgio su Legnano (MI). All the qualification tests (QTP) are conceptually split as shown in the following block of the Figure 16 flowchart.

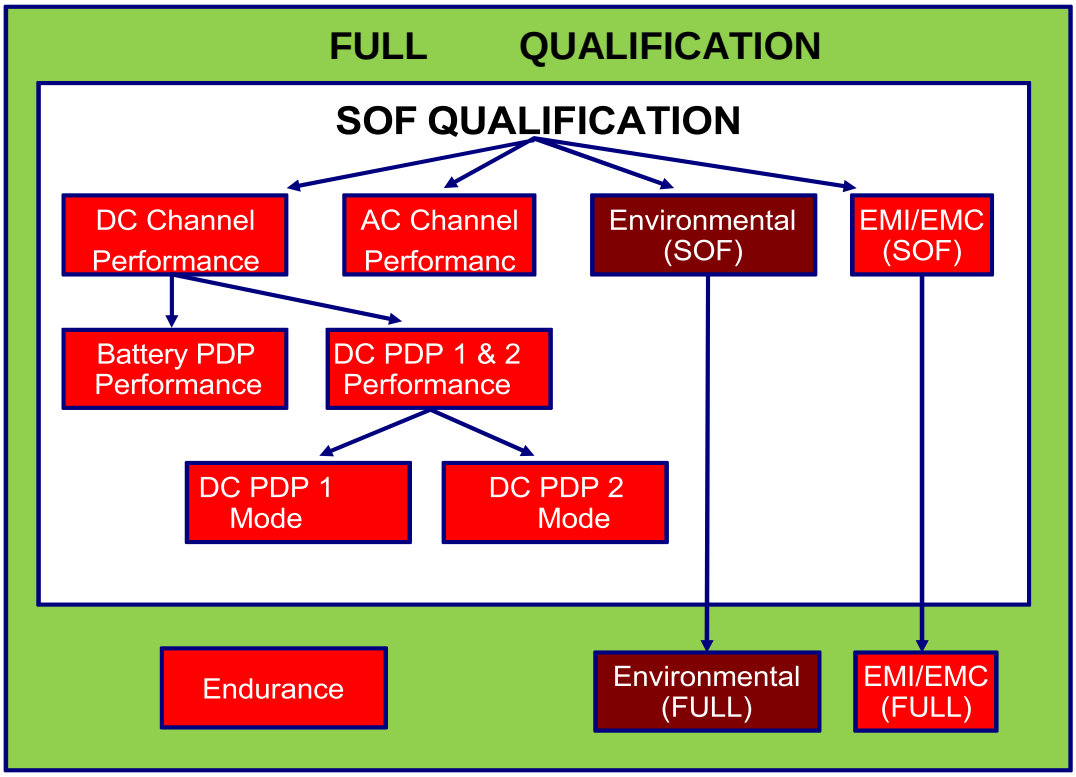


Figure 16: Qualification Test Procedure flowchart

## 4.2 AC PDP 1 AND AC PDP 2 PERFORMANCE TESTS

Aim of the Performance Tests is to verify the AC EPDS compliance against the functional requirements defined in the Technical Specification. Since the requirement are split between PDPs, the same partition will

be followed during the definition of the Test Procedures. The Performance tests will be grouped into “AC PDP 1 Performance Tests” and “AC PDP 2 Performance Tests”, focusing on the requirement allocated to the related PDP. During the Performance Tests, operation, switching and protection features will be verified on the EUT (i.e. the AC EPDS).

### 4.2.1 GENERAL TEST SETUP AC PDP 1 AND AC PDP 2

The test setup detail shown in Figure 17 is proposed in order to verify the bus voltage from the source, the Contactor for trip condition and the distribution of load to the bus connected to the AC PDP 1 and AC PDP 2.

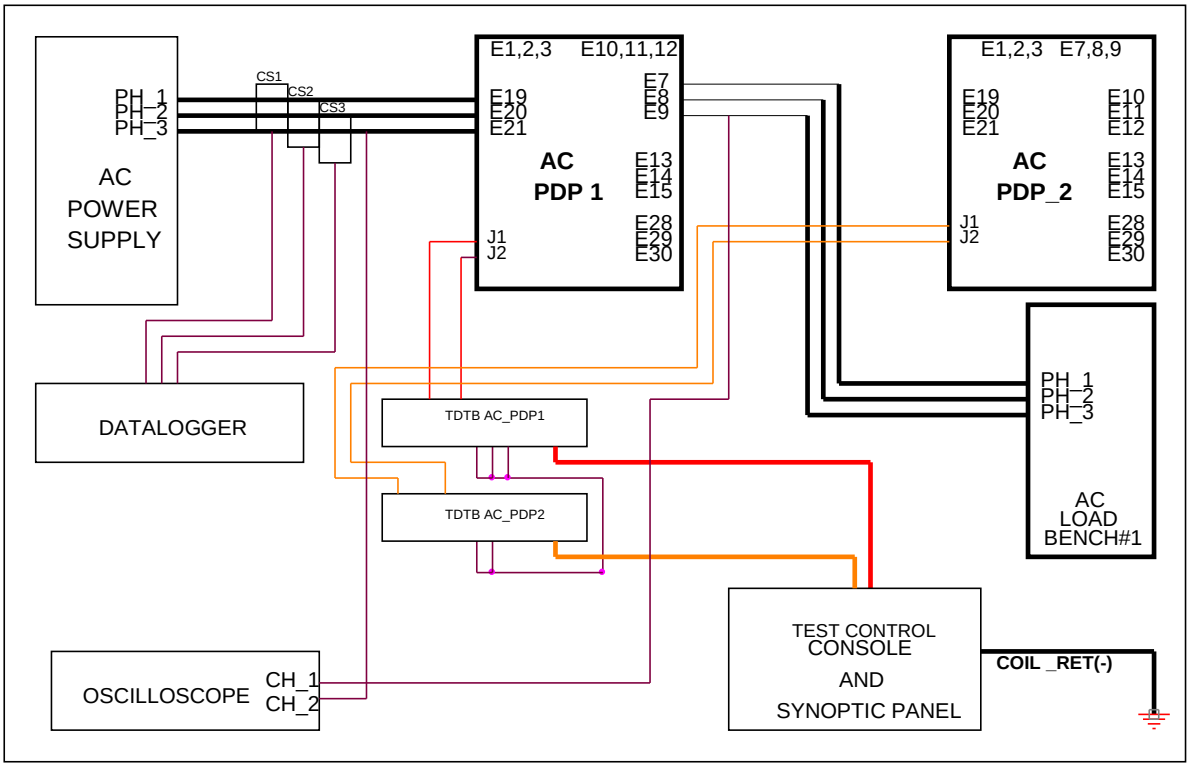



Figure 17: Test setup detail for the AC PDP 1 and AC PDP 2 Power Distribution Unit

### 4.2.1 QUALIFICATION TEST BOX

The Qualification Test Box will provide the discrete input/outputs for the EUT for the excitation of contactors & relays, simulation (if required) and verification of the status signals. There will be test points and LEDs for the visual displays of the signals from the EUT.

### 4.2.2 OPERATION – AC PDP 1 AND AC PDP 2

AC PDPs functional tests will be carried out in order to proof the capability to operate in normal and abnormal condition.

#### 4.2.2.1 Contactor Controls and Power Distribution

Aim of the test is to verify that contactors close when the external signal is sent from the Qualification Test Box and all the closure conditions are “true”. The bus voltage will also be verified at the load box connected at the studs of the PDP.

#### 4.2.2.2 System Continuous Capacity

Aim of the test is to verify the System is able to manage required continuous output currents.
The continuous capacity test will be carried out by imposing the worst load conditions.

### 4.2.3 AC PDP PROTECTION TESTS

A dedicated test session will be carried out in order to verify the protections performed by OPM modules. After the verification of the right protection intervention, also the manual-in-flight resetting system has to be verified. System behavior to be verified: Main contactor opened and bus voltage will be disconnected at the outputs of Heaters and windshields. Intervention of TRU circuit breaker will be verified.

## 4.3 DC PDP 1 AND DC PDP 2 PERFORMANCE TESTS

The performance of DC PDP 1 and DC PDP 2 will be verified by connecting the equipment to the EPDS by means of the Qualification Test Box. The DC PDP 1 and DC PDP 2 will be connected also to the DC power source and to the load bench.
The EUT contactors will be driven externally by the signals provided from the Qualification Test Box. The corresponding status signals are verified by either Digital Multimeter/DSO by connecting to the appropriate pins in the Qualification Test Box.

### 4.3.1 GENERAL TEST SETUP DC PDP 1 AND DC PDP 2

The test setup details shown in Figure 18 is proposed in order to verify the bus voltage from the source, the Contactor for the trip condition and the distribution of load to the bus connected to DC PDP 1 and DC PDP 2.

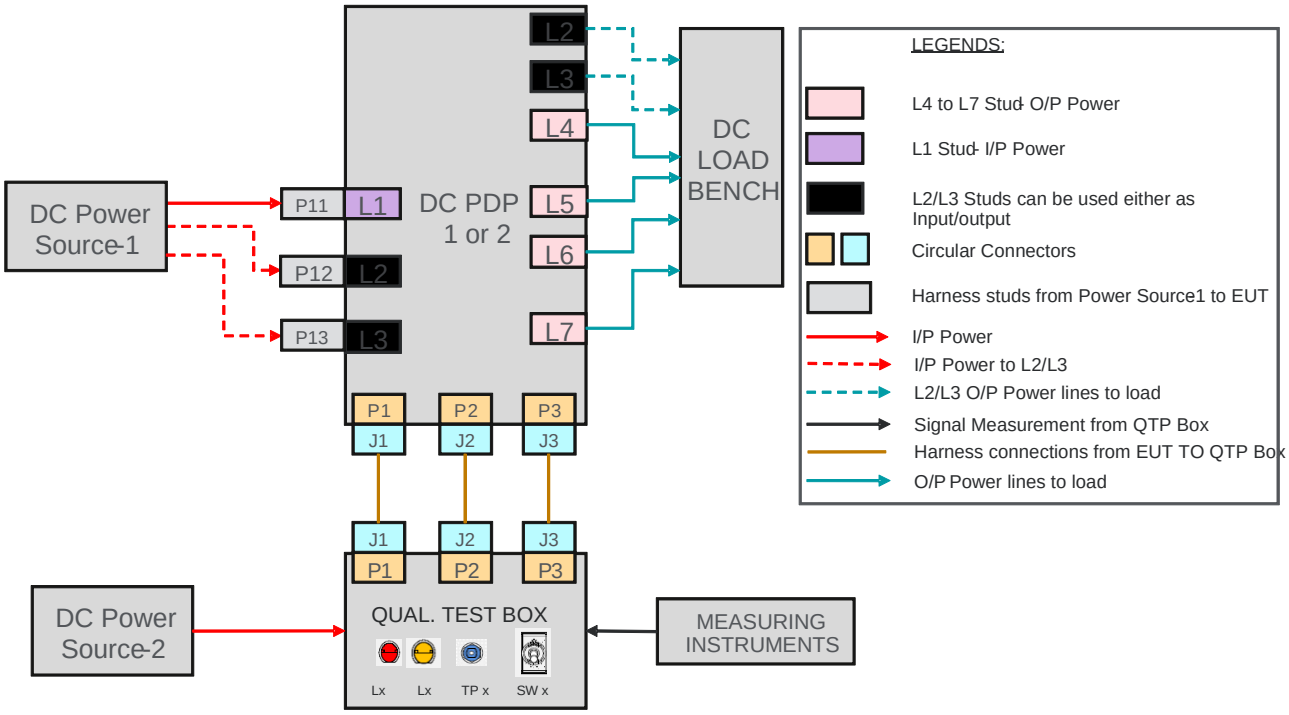


Figure 18: Test setup detail for the DC PDP 1 and DC PDP 2 Power Distribution Unit.

1. The power input is fed from the DC power source-1 at the L1 input stud of the DC PDP.
2. The studs L2 and L3 can be either used as input power or Output load.
3. The power input for the contactors in the DC PDP, not coming from the EPDS itself (i.e. from the bus bars), is provided by the DC-Power Source-2 through the Qualification Test Box.

4. The Qualification Test Box will provide the excitation voltage, test points for measuring the signal and visual display of LED for the status signal from the DC PDP under test.
5. Instruments like DMM or Oscilloscope can be connected in the desired test points in Qualification Test Box for measuring the signal values during the testing.
6. There are DC load bench (Capacity: 0-32V/0-450A) connected to the outputs of the bus voltages at the studs (L4 to L7) of the DC PDP 1 and DC PDP 2.

### 4.3.2 QUALIFICATION TEST BOX

The Qualification Test Box will provide the discrete input/outputs for the EUT for the excitation of contactors & relays, simulation (if required) and verification of the status signals. There will be test points and LEDs for the visual displays of the signals from the EUT. The Qualification Test Box details will be explained in the QTP document.

### 4.3.3 OPERATION - DC PDP 1 AND DC PDP 2

The DC PDP 1 and the DC PDP 2 will be tested in order to verify the capability to operate in normal and abnormal condition.

#### 4.3.3.1 Contactor Controls and Power Distribution

Aim of the test is to verify that contactors close when the external signal is sent from the Qualification Test Box and all the closure conditions are “true”. The bus voltage will also be verified at the load box connected at the studs of the PDP.

#### 4.3.3.2 Continuous Capacity

Aim of the test is to verify the PDP is able to give required continuous output currents, keeping the minimum output voltages required under each load condition.
The test will be carried out at the minimum load current required for the normal operation and for the failure modes of operation of DC PDP 1 and for DC PDP 2 under specific conditions.

#### 4.3.3.3 Short Circuit Capacity and Overload Conditions

Aim of the test is to verify if the load current at the studs exceeds the short circuit or overload current drawn(>100A). When the load current connected at the stud (L4) falls in anyone category, the RCCB inside the PDP will sense and control the load by disconnecting it.
System behavior to be verified: Main contactor opened and bus voltage will be disconnected at the stud (L4).
Also, the system will verify the overload conditions (fault) of the current drawn at the any stud (L5 to L7) is more than the rated current of the circuit breakers (CB). System behavior to be verified: CB opened when the fault condition is reached.

#### 4.3.3.4 FAULT Isolation LOGIC (FIL) Board

In the DC PDP 1 and in the DC PDP 2, there is a fault isolation board which will provide the following functions:

1. Manage of input commands
2. Provide output signals
3. Provide Fuse monitoring (only DC PDP 2)
4. Provide fault isolation sequence when an overcurrent is sensed by main current sensors inside the PDP.

The FIL board will be verified applying to the EPDS under test the resistive load required to trigger the protections.

## 4.4 BATTERY PDP PERFORMANCE TESTS

The system performance of Battery PDP will be verified by connecting the equipment to the rest of the EPDS by means of the Qualification Test Box. The DC BATTERY PDP will be connected also to the DC power source and to the load bench.

The EUT contactors will be driven externally by the signal provided from the Qualification Test Box. The corresponding status signals are verified by either Digital Multi meter/DSO by connecting to the appropriate pins in the Qualification Test Box.

### 4.4.1 GENERAL TEST SETUP- BATTERY PDP

The below Figure 19 displays test setup detail for the verification of the bus voltage from the source, the verification of the Contactor for the trip condition and for the verification of distribution of load to the other bus connected to the Battery PDP.

1. The power input is fed from the DC power source-1 at the L1/L3/L6 input pin of the Battery PDP.
2. The power input for the contactors in the Battery PDP, not coming from the EPDS itself (i.e. from the bus bars), is provided by DC-Power Source-2 through the Qualification Test Box.
3. There are DC load benches (Capacity: 0-32V/0-400A) connected to the outputs of the bus voltages at the studs of the Battery PDP.
4. The Qualification Test Box will provide the excitation voltage, test points for measuring the signal and visual display of LED for the status signal from the DC PDP under test.
5. Instruments like DMM or Oscilloscope can be connected in the desired test points in Qualification Test Box for measuring the signal values during the testing.

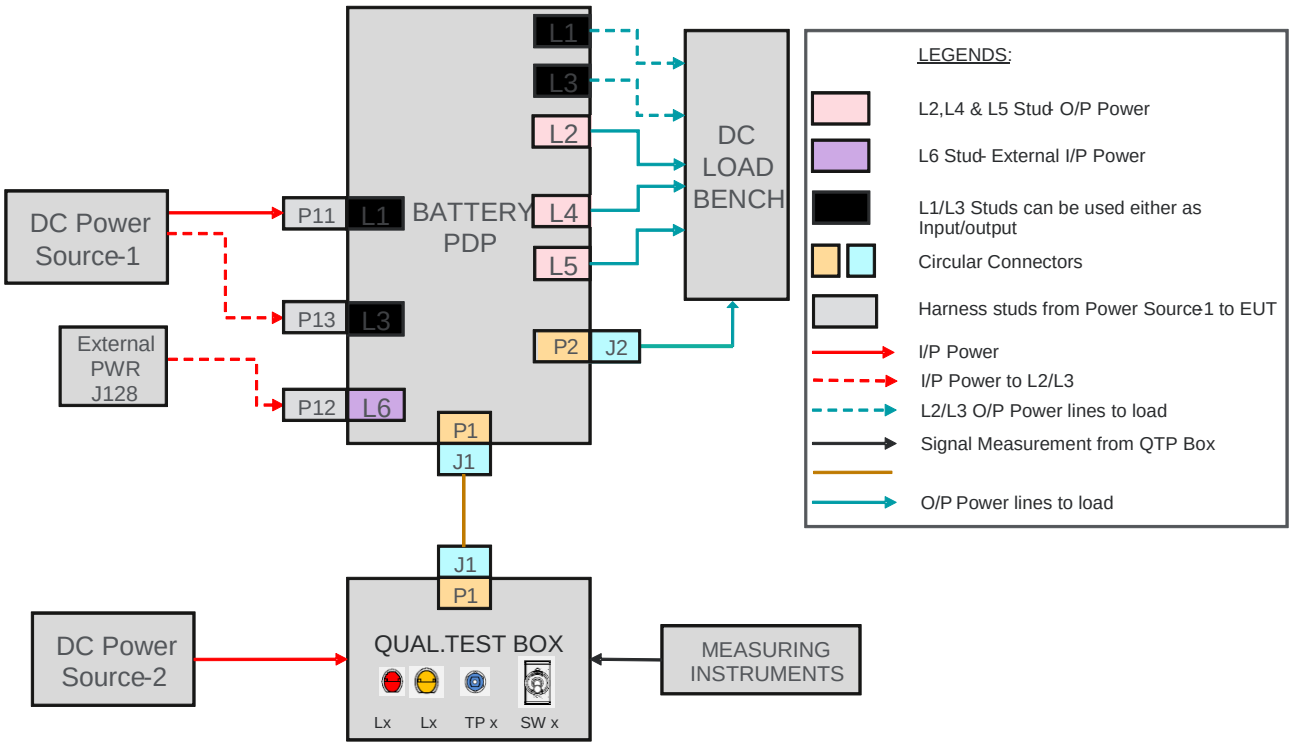



Figure 19: Test setup detail for the Battery PDP Power Distribution Unit.

### 4.4.2 CONTACTOR CONTROLS AND POWER DISTRIBUTION

Aim of the test is to verify the external power contactor closes when the external signal is sent from the Qualification Test Box and all the closure conditions are “true”. The bus voltage will also be verified at the load box connected at the studs of the PDP.

### 4.4.3 CONTINUOUS CAPACITY

Aim of the test is to verify the System is able to give required continuous output currents, keeping the minimum output voltages required under each load condition. The test will be carried out at the minimum load current required for the Battery PDP under specific conditions.

### 4.4.4 SHORT CIRCUIT CAPACITY AND OVERLOAD CONDITIONS

Aim of the test is to verify if the load current at the studs exceeds the short circuit or overload current drawn. When the load current connected at the stud (L2 or L3) falls in anyone category, the RCCBs inside the PDP will sense and control the load and disconnect the contactors.
System behavior to be verified: Main contactor opened and bus voltage will be disconnected at the stud (L2) and stud (L3).

### 4.4.5 BATTERY PDP DC EXTERNAL POWER MONITOR (EPM)

The Battery PDP external DC power input validation is done by connecting the DC power source simulating the External Power Unit and verifying the input voltage for over-voltage and reverse polarity.

The below mentioned steps are a trace for the EPM validation.

The EPM inside the Battery PDP will monitor the external power at the PDP inputs and correspondingly will provide the output latching voltage for the external power coil contactor if the voltage is within the permissible limits.

1. Connect the test setup as mentioned in Figure 19.
2. Provide external DC voltage input above the mentioned level of input (Over Voltage trip curve available in related Functional Test QTP) at the external DC power receptacle input of the Battery PDP.
3. If the input voltage is over the admitted limits, the EPM will open the External Power Contactor (K9) and latch the alarm condition.
4. It will be verified also the latch condition is released only by an external reset switch using a Ground signal pulse provided by an external source.

## 4.5 QTP ENVIRONMENTAL TEST FOR SOF (SAFETY OF FLIGHT)

### 4.5.1 OPERATIONAL VIBRATION, ENDURANCE AND FUNCTIONAL SHOCK TEST

#### 4.5.1.1 General

The purpose of this test is to ensure that the units are capable of withstanding the mechanical stresses stipulated in the applicable technical specifications. Each item will be installed on an electromechanical shaker one at a time during the test. Before changing the direction of the mechanical forcing, performance vibrations, endurance vibrations, and functional shocks will be applied sequentially along a specified axis.

### 4.5.2 REFERENCE

Vibration tests will be performed in accordance with **MIL STD 810G, Method 514, category 14**. The items will be exposed to 45 minutes of performance-level vibrations, followed by 90 minutes of resistance-level vibrations and again 45 minutes of performance-level vibrations [1].
At the end of the exposure to vibrations along each axis, functional shocks will be applied to the element along each axis, three positive and three negative. Resonance searches will be performed at the beginning, end and during mechanical forcing along each axis.

A detailed graph of the vibration military standard is given following Figure 20.

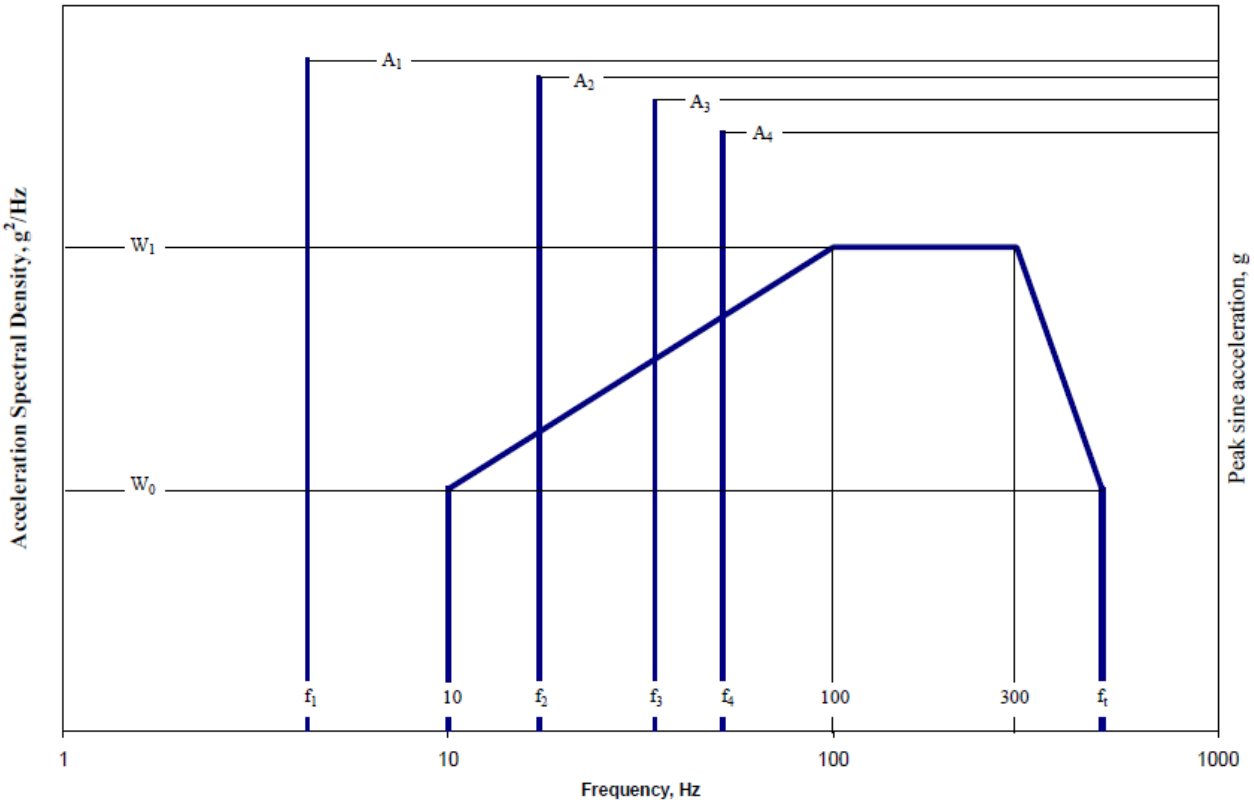


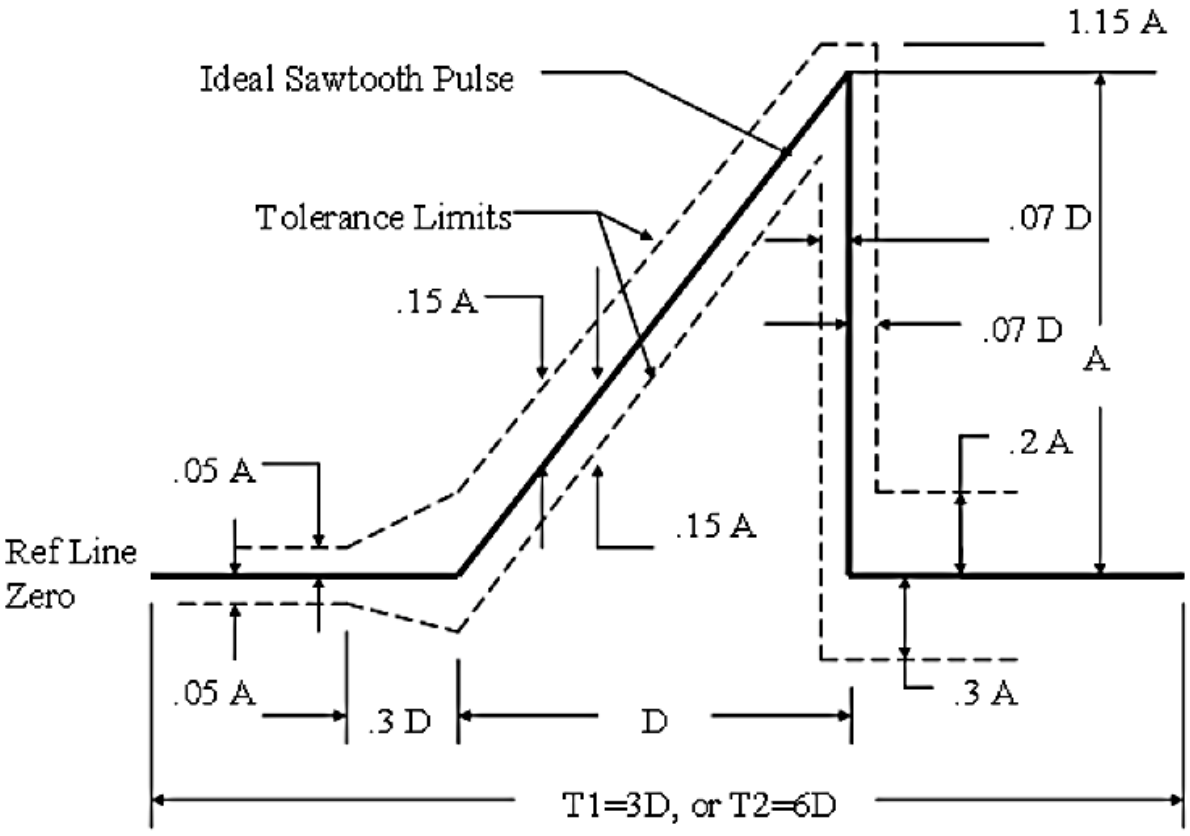

Figure 20: Helicopter vibration profile according to Cat.14 of method 514 of MIL-STD-810G.

The equipment must continue to provide its function within performance standards after exposure to shocks experienced during normal aircraft operations (Operational Shocks) and not to detach from the main structure during an emergency landing (Crash Safety) [2].

The DC PDP 1, DC PDP 2 and BATTERY shall be tested as per **RTCA DO-160G, Section 7, Category B** (equipment tested for standard shock and crash safety).

*Table 4:* Terminal saw tooth shock pulse tolerance limits according to RTCA DO-160G.

| Test (Impulse) | Peak value (A) [g] | Nominal duration (D) [ms] |
|---|---|---|
| **Standard Operational Shock** | 6 | 11 |
| **Standard Crash Safety Impulse** | 20 | 11 |




D = Duration of nominal pulse.
A = Peak acceleration of nominal pulse.
T1 = Minimum time during which the pulse shall be monitored for shocks produced using a conventional shock testing machine.
T2 = Minimum time during which the pulse shall be monitored for shocks produced using a vibration generator.

Figure 21: Terminal saw tooth shock pulse configuration according to RTCA DO-160G.

#### *4.5.2.1 Test Setup Details*

The test is performed by forcing the equipment using the electro-dynamic shaker defined displayed in Figure 22. The agitator is coupled to a sliding table, allowing the machine to force the EUT along the three orthogonal axes using a simple device. In fact, the EUT must not be transferred to the appliance (the element that joins the EUT and the agitator head or the EUT and the sliding table). The shaker vertically oriented in order to give force along the longitudinal axis of the EUT.

Figure 22: Electromechanical Shaker setup

## 4.6 ELECTROMAGNETIC COMPATIBILITY AND ELECTROMAGNETIC INTERFERENCE TEST (EMC/EMI)

### 4.6.1 EMC FOR CIVIL QUALIFICATION

For Civil Certification the following Sections of **RTCA/DO-160G** will be considered:

Section 15: Magnetic Effect
Section 17: Voltage Spike
Section 18: Audio Frequency Conducted Susceptibility – Power Input
Section 19: Induced Signal Susceptibility
Section 20: Radio Frequency Susceptibility (Radiated and Conducted)
Section 21: Emission of Radio Frequency Energy
Section 22: Lightning Induced Transient Susceptibility
Section 25: Electrostatic Discharge

Applicable requirements are those ones reported in the following Table 5:

Table 5: EMC requirements definition.

| PDP | RTCA DO applicable sections and appropriate requirement category | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **15** | **17** | **18** | **19** | **20** | **21** | **22** | **25** |
| AC PDP 1 & 2 | Z | A | R | Z N | YY | H | A4K4M3 (shielded wires) B3H3L3 (unshielded wires) *(1) | A |
| DC PDP 1 & 2 (FOC) | Z | A | Z | Z N | YY | H | A4K4M3 (shielded wires) B3H3L3 (unshielded wires) *(1) | A |
| BATT PDP | Z | A | Z | Z N | YY | H | A4K4M3 (shielded wires) B3H3L3 (unshielded wires) *(1) | A |

All EMI/EMC tests will be carried out on the EUT connected together to form the complete AC or DC power distribution system (all PDPs connected together with wirings fully-representative of the aircraft installation in terms of wire length, size, shielding, etc.), unless otherwise specified.

The EMI/EMC tests of Table 6 will be carried out to reach the SOF qualification.

Table 6: EMI/EMC tests for the DC EPDS and FUSE BOX SOF qualification.

| Test Type | Reference | Category / description | Means of Compliance | Note |
|---|---|---|---|---|
| **Magnetic Effect** | RTCA DO-160G Section 15 | Cat. Z (D<0.3m) | By test | Test performed on standalone items |
| **Voltage Spike** | RTCA DO-160G Section 17 and DEF-STAN 59-411 DC03 | Cat. A | By test | |
| **Radio Frequency Susceptibility (Radiated and Conducted)** | RTCA DO-160G Section 20 | Cat. Y (conducted) Cat. Y (radiated) | By test | |
| **Emission of Radio Frequency Energy** | RTCA DO-160G Section 21 | Cat. H | By test | |
| **Electrical Bonding.** | 249F0000Q001 | DC Resistance 2.5mΩ from connector back-shell to chassis | By test | ATP test carried out on each S/N. |
| **PDP Chassis Isolation** | 249F0000Q001 | 1000 V rms for 1 minute. | By test | ATP test carried out on each S/N. |
| **Insulation Resistance** | | 100MΩ @500VDC | By test | ATP test carried out on each S/N. |

## 4.7 MAGNETIC EFFECT (RTCA DO-160G SECTION 15)

### 4.7.1 PURPOSE

This test determines the magnetic effect of the EUT to assist the installer in choosing the proper location of the EUT aboard the helicopter.

### 4.7.2 OPERATING CONDITIONS DURING TESTS

The AC PDPs contains contactors and other components (electronic board, protection board and current sensors). The worst case is when both electromagnetic devices are excited (MODE 1). These devices are supplied with the 28VDC bus.
MODE 2 will be tested anyway, in order to get the value for the passive EUT.
The three phase AC power line inputs stud E19,E20,E21 of the AC PDPs are connected to the AC outputs E28,E29,E30 through the power contacts of the [K1 + K7] and [K2 + K8] contactors and to the AC outputs E22,E23,E24 through the power contacts of [K5] contactor. These power lines are not part of the EUTs and they are not used for the PDU supply. For these reasons the test is not applicable to AC power cables.

### 4.7.3 TEST PROCEDURE

If Horizontal Component of Ambient magnetic Field Strength produced by the Earth (or HCAFS) at the location of the test lab is unknown, measure it. Otherwise use the known value.

1. Ensure the measuring compass is not deflected by more than ± 0.5 degrees when moving along the planned path to the EUT location (field uniformity check).

If HCAFS is 14.4A/m ±10% assume *Dc* = 1 degree and jump to step 0. *Dc* is the angular deflection used to determine equipment category.

2. If HCAFS is outside 14.4A/m ±10% limits, assume *Dc* equal to 1[°] * 14.4[A/m] / HCAFS.

Configure the EUT for testing connecting the switching panel shown in Figure 23. All other devices (switch panel) shall be considered as test support equipment during the EUT test.

3. **MODE 2 TEST**: set the system in operating MODE 2 defined
4. Measure the distance between the magnet pivot and the nearest part of the EUT at which a deflection angle of *Dc* exists. Record the value and compare it with the equipment class
5. **MODE 1 TEST**: set the system in operating MODE 1 defined
6. Measure the distance between the magnet pivot and the nearest part of the EUT at which a deflection angle of *Dc* exists. Record the value and compare it with the equipment class

Repeat steps from 0 to 6 for each face of each PDP.

If distances measured during steps 4 and 6 are between Class Z limits, record the compliance with the requirement for the EUT according to **RTCA/DO-160G** [3].

| Equipment Category | Distance for a Deflection of Dc |
|---|---|
| Y | D = 0.0m |
| Z | 0< D ≤ 0.3m |
| A | 0.3< D ≤ 1m |
| B | 1m < D ≤ 3m |
| C | greater than 3.0 m |

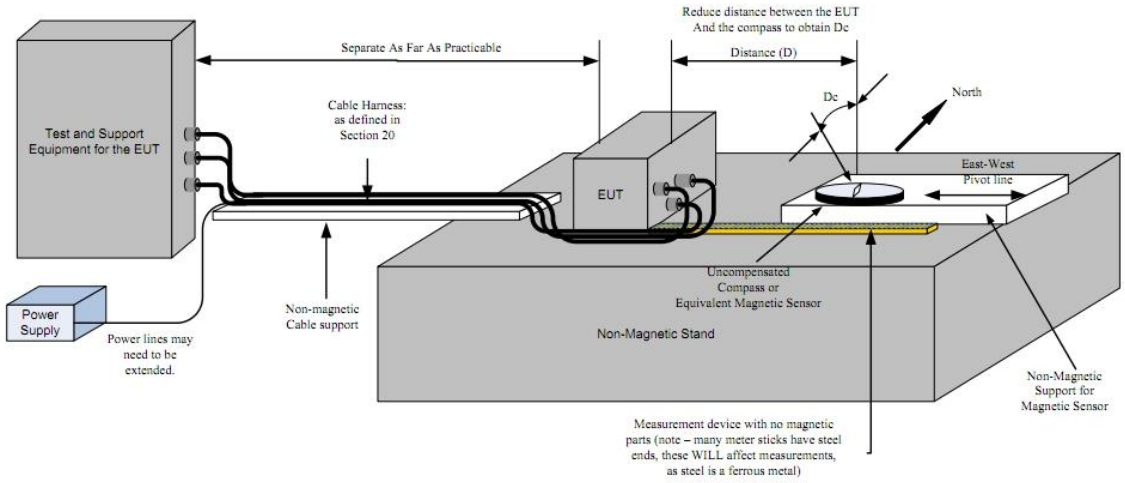



Figure 23: Magnetic effect test setup

## 4.8 VOLTAGE SPIKE (RTCA DO-160G SECTION 17)

### 4.8.1 PURPOSE

This test determines whether the EUT can withstand the effect of voltage spikes arriving at the AC system EUTs on its power lead, either ac or dc. The main adverse effects to be anticipated are:

- Permanent damage, component failure, insulation breakdown.
- Susceptibility degradation, or changes in EUTs performance.

### 4.8.2 OPERATING CONDITIONS DURING TESTS

AC EPDS input power are the 28VDC K1, K5 and K7 coil supply and the three phase AC power leads connected from INPUT stud E19,E20,E21 and OUTPUT stud E28, E29, E30 with load and OUTPUT E22, E23, E24 without load.

AC EPDS input power are the 28VDC K2, K6 and K8 coil supply and the three phase AC power leads connected from INPUT stud E19,E20,E21 and OUTPUT stud E28, E29, E30 with load and OUTPUT E22, E23, E24 without load.

**MODE 1 (OPERATIVE MODE):** Contactors K1, K5 and K7 energized in AC PDP 1 with through CTs and OPM electronic board channel Windshield 1 protection module.
Contactors K2, K6 and K8 energized in AC PDP 2 with through CTs and OPM electronic board channel Windshield 2 protection module.
**MODE 2 (REST MODE):** Contactors K1, K5 and K7 are de-energized, together with CTs and OPM electronic board on AC PDP 1.
Contactors K2, K6 and K8 are de-energized, together with CTs and OPM electronic board on AC PDP 2.

All the DC power input pins: [J2-2; J2-3], [J2-31; J2-32], [J2-1; J2-22] of AC PDP 1; supplied by the 28VDC bus will be tested simultaneously, injecting both positive and negative polarity transients through the C1 socket on the DB25UC-AC.EMI Switch Panel (see
Figure 24).

All the DC power input pins: [J2-2; J2-3], [J2-31; J2-32], [J2-1; J2-22] of AC PDP 2; supplied by the 28VDC bus will be tested simultaneously, injecting both positive and negative polarity transients through the C1 socket on the DB25UC-AC.EMI Switch Panel (see
Figure 24).

The three phase AC power line (connected to K1-K5-K7_AC PDP 1) will not be tested since they cannot be negatively affected by 600V peak transients.

The three phase AC power line (connected to K2-K6-K8_AC PDP 2) will not be tested since they cannot be negatively affected by 600V peak transients.

In facts, during ATP, they are tested against 1 minute 1000Vrms dielectric withstand test (between phases, between input and output, between all terminals and case).

The test on AC PDPs will be carried out in MODE 1 and MODE 2.

### 4.8.3 TEST PROCEDURE – RTCA DO-160G CAT.A

Before starting the test on the EUTs, verify the spike generator device is able to give wave shape in accordance with Figure 25, RTCA DO-160G cat. A.

1. Figure 24.
2. Connect the pulse generator in order to inject spikes along J2-2 lead (K1 coil positive). K1 coil return lead is J2-3 of the AC PDP 1.
3. Connect the pulse generator in order to inject spikes along J2-31 lead (K7 coil positive). K7 coil return lead is J2-32 of the AC PDP 1.
4. Connect the pulse generator in order to inject spikes along J2-1 lead (K5 coil positive). K1 coil return lead is J2-22 of the AC PDP 1.
5. Connect the pulse generator in order to inject spikes along J2-2 lead (K2 coil positive). K2 coil return lead is J2-3 of the AC PDP 2.
6. Connect the pulse generator in order to inject spikes along J2-31 lead (K8 coil positive). K8 coil return lead is J2-32 of the AC PDP 2.
7. Connect the pulse generator in order to inject spikes along J2-1 lead (K6 coil positive). K1 coil return lead is J2-22 of the AC PDP 1.
8. Set the system in operating **MODE 2** defined
9. Apply a series of 50 positive polarity spikes on 28VDC line within a period of one minute.
10. Apply a series of 50 negative polarity spikes on 28VDC line within a period of one minute.
11. During steps 10 and 11 verify the status of the system as described in above. Any deviation will be recorded as a test failure.
12. Set the system in operating **MODE 1** defined
13. Apply a series of 50 positive polarity spikes on 28VDC line within a period of one minute.
14. Apply a series of 50 negative polarity spikes on 28VDC line within a period of one minute. During steps 13 and 14 verify the status of the system as described. Any deviation will be recorded as a test failure.
15. Remove the pulse generator and restore J2-1, J2-2 and J2-31 for AC PDP 1 and AC PDP 2 lead continuity.

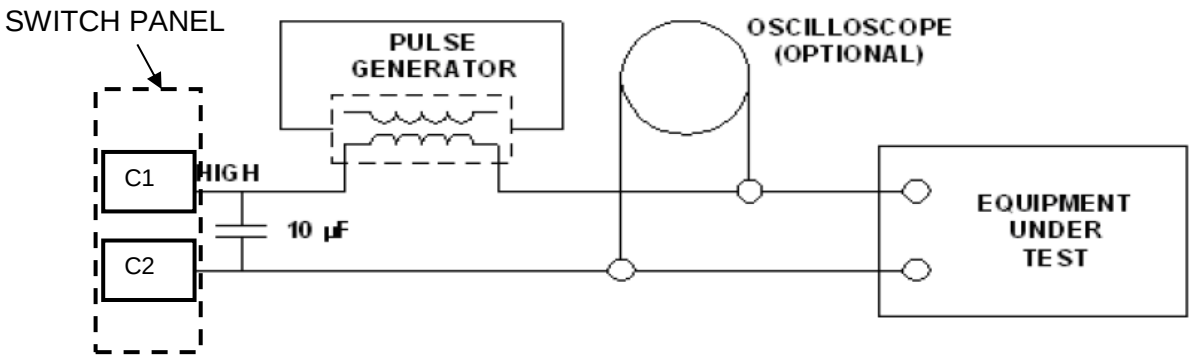



Figure 24: Voltage Spike Test Setup for DC (Figure 17-2 of RTCA DO-160G).

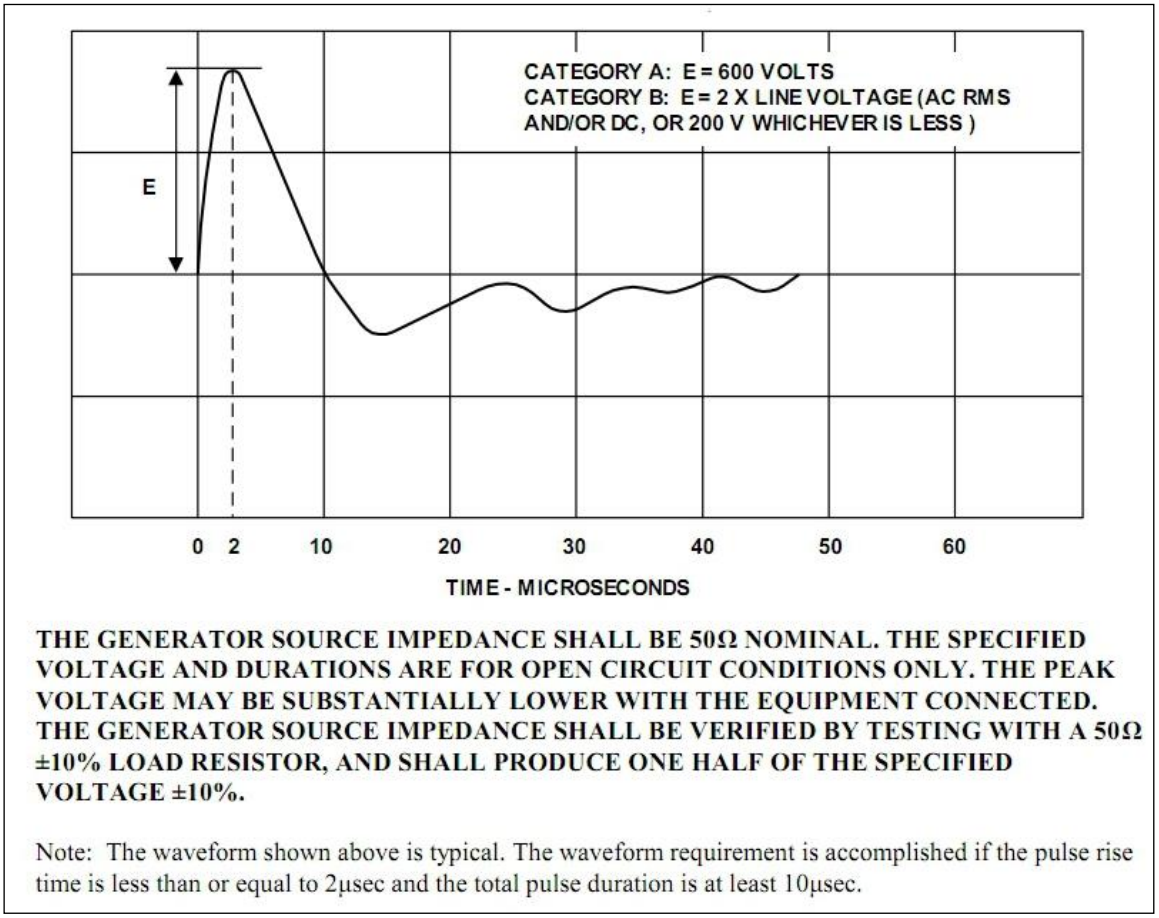



Figure 25: Voltage Spike Waveform (Figure 17-1 of RTCA DO-160G).

## 4.9 RADIO FREQUENCY SUSCEPTIBILITY (RADIATED AND CONDUCTED RTCA DO-160G SECTION 20)

### 4.9.1 PURPOSE

These tests determine whether equipment will operate within performance specifications when the equipment and its interconnecting wiring are exposed to a level of RF modulated power, either by radiated RF field or by injection probe induction onto the power lines and interface circuit wiring.

### 4.9.2 APPLICABILITY

The test is applicable to the EUTs with the following classification:
AC PDP 1: Category Y (both Conducted and Radiated).
AC PDP 2: Category Y (both Conducted and Radiated).

NOTE(1): Cat Y provide test levels for bench testing supporting compliance to HIRF Special Conditions and for showing backdoor T-PED tolerance
NOTE(2): Cat Y required limits are:

- 300mA in the range 0.5-100MHz
- From 300mA to 100mA with slope as per Figure 20-6 of RTCA/DO-160G in the range 100-400MHz

NOTE(3): Cat Y CW value is 200V/m for all frequency ranges
NOTE(4): the cable bundles subjected to test are: J1, J2 of AC PDP 1 and J1, J2 of AC PDP 2. All other interfaces are not tested because they are bus bars connected between different terminal blocks by means of contactors to distribute the generators current to the loads, so the current pass through the box without interfere with the box functioning.

### 4.9.3 TEST PROCEDURE CONDUCTED SUSCEPTIBILITY (CS) 10KHZ TO 400MHZ

Install the induced current monitor probe 50mm from the connector back-shell with the injection probe 50mm from the monitor probe. Considering that the trip/release time of relay and contactor is less than 60ms, the dwell time will be 1 second (minimum time required because the EUT has not working cycle, the contactors don't change their status during both MODE 1 and MODE 2).
Configure the EUTs for testing as shown in below

1. Perform Probe Calibration as described in **Section 20.4 of RTCA DO-160G** standard, point *b*.
2. Configuration #1 Test: set the EUT in **MODE 2**

Set the signal generator to 10kHz. Adjust and control the forward power to achieve the induced current on the cable for the selected curve of Figure 27 (curve Y). If necessary, limit the forward power to no more than 6dB above the calibration value determined at point 1. NOTE: The current and voltage levels shall be recorded.

3. For frequency scan rate policy, refer to **RTCA DO-160G, Section 20.3, point *e***.
4. Verify the status of the EUT as described. Any deviation will be recorded as a test failure. NOTE: The threshold of any failure should be recorded and then the power to be increased to the target level to determine if any other failures are recorded.
5. Steps 5 to 7 shall be performed three times: the first time using un-modulated (CW) waveform, the second time using 1kHz square wave modulation with at least 90% depth and the third time using 300Hz to 3kHz square wave amplitude modulated >90% with a superimposed 1Hz square wave modulation >90%. The frequency is linearly swept from 300Hz to 3kHz during the ON period of the 1Hz square wave and reset in the OFF period (during OFF period of the 1Hz modulation, Susceptibility test shall be suspended)
6. Configuration #2 Test*:* set the EUT in operating **MODE 1**
7. Repeat steps 5 through 8.
8. Configuration #3 Test*:* set the EUT in operating **MODE 2**
9. Repeat steps 5 through 8.
10. Configuration #4 Test*:* set the EUT in operating **MODE 1**
11. Repeat steps 5 through 8.
12. Repeat test on each EUT in **MODE 1** and **MODE 2**.

NOTE(2): modulation applied for Category Y in frequency range 10kHz to 400MHz is:

- CW
- 1kHz square wave modulation with at least 90% depth
- 300Hz to 3kHz square wave amplitude modulated >90% with a superimposed 1Hz square wave modulation >90%. The frequency is linearly swept from 300Hz to 3kHz during the ON period of the 1Hz square wave and reset in the OFF period (during OFF period of the 1Hz modulation, Susceptibility test shall be suspended)

### 4.9.4 RADIATED SUSCEPTIBILITY (RS), 400MHZ TO 45GHZ – TEST PROCEDURE

Note: the following procedure refers to "Anechoic Chamber Method", Section 20.5 of RTCA DO-160G standard. The Dwell Time must be 1 second minimum (minimum time required because the EUT has not working cycle, the contactors don't change their status during both MODE 1 and MODE 2). The above mentioned standard section defines the procedure from 400MHz to 18GHz. According to 249F0000Q001 document, the range must be extended to 45GHz, following the same procedure related to 400MHz-18GHz range.

Before placement of the EUT inside the test chamber, perform Radiated Field Calibration as described in Section 20.5 of RTCA DO-160G standard, point *b*. The forward power to the transmit antenna shall achieve the total field strength indication from the isotropic probe defined by RTCA DO 160G standard for category Y (CW).

1. Configure the EUTs for testing as shown
2. When the beam width does not totally cover the system under test, multiple area scans shall be performed. However, it is required that each EUT within the system and at least one half wavelength of wiring of that EUT shall be exposed in its entirety during the test.
3. **MODE 2 Test**: set the EUT in **MODE 2**

Subject the EUTs to the radiated field at the level calibrated during step 0.

4. Scan the frequency range to the upper limit (45GHz) using modulation policy reported below (RTCA DO-160G Section 20.5, point *e*).
5. Verify the status of the EUT as described. Any deviation will be recorded as a test failure.
6. **MODE 1 Test**: set the EUT in operating **MODE 1**

Repeat steps 0 through 5.

NOTE(1): this shall be performed for both vertical and horizontal antenna polarization.
NOTE(2): modulation applied for Category Y in frequency range 400MHz to 18GHz is:

- CW
- 1kHz square wave modulation with at least 90% depth

NOTE(3): for what concerns peak values in the range between 400MHz and 18GHz, 1kHz pulse modulation of at least 90% depth. The pulse width shall be at least 4μs. This signal should in addition be switched on and off at a rate of 1Hz with a 50% duty cycle (as per **Category R**).

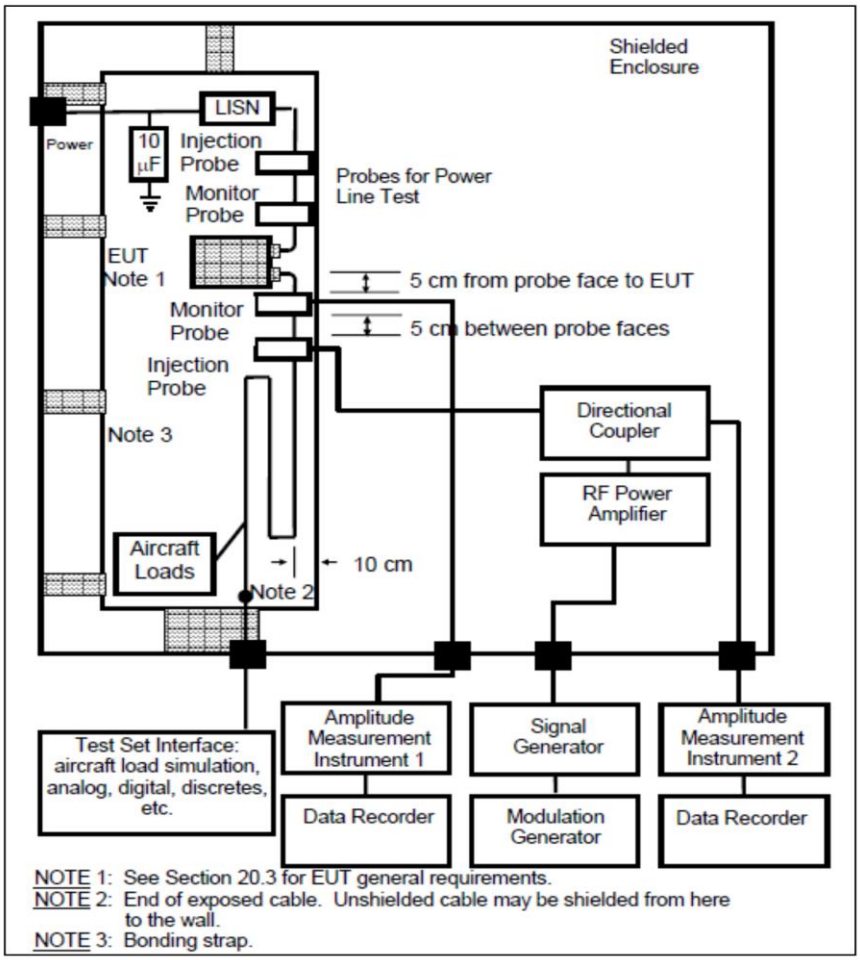



Figure 26: Conducted Susceptibility test setup.

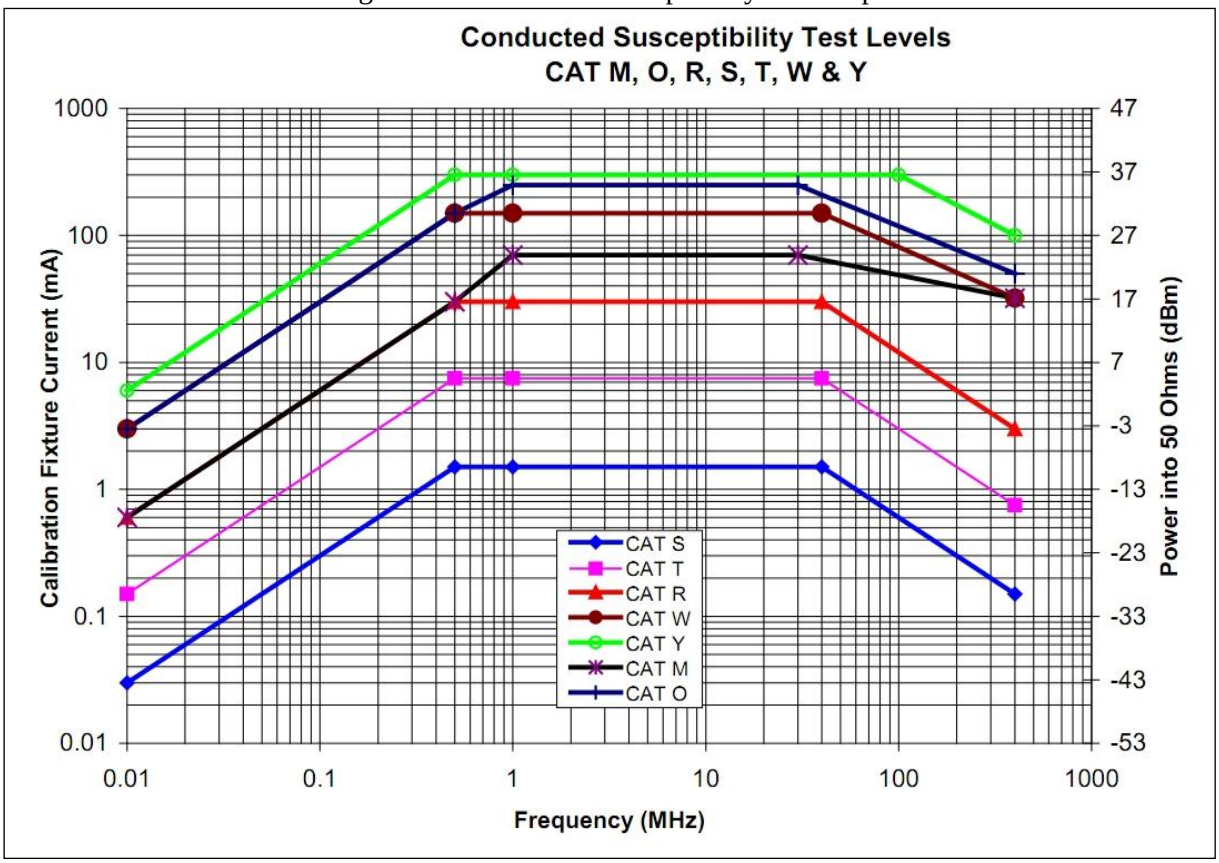



Figure 27: Conducted Susceptibility test levels.

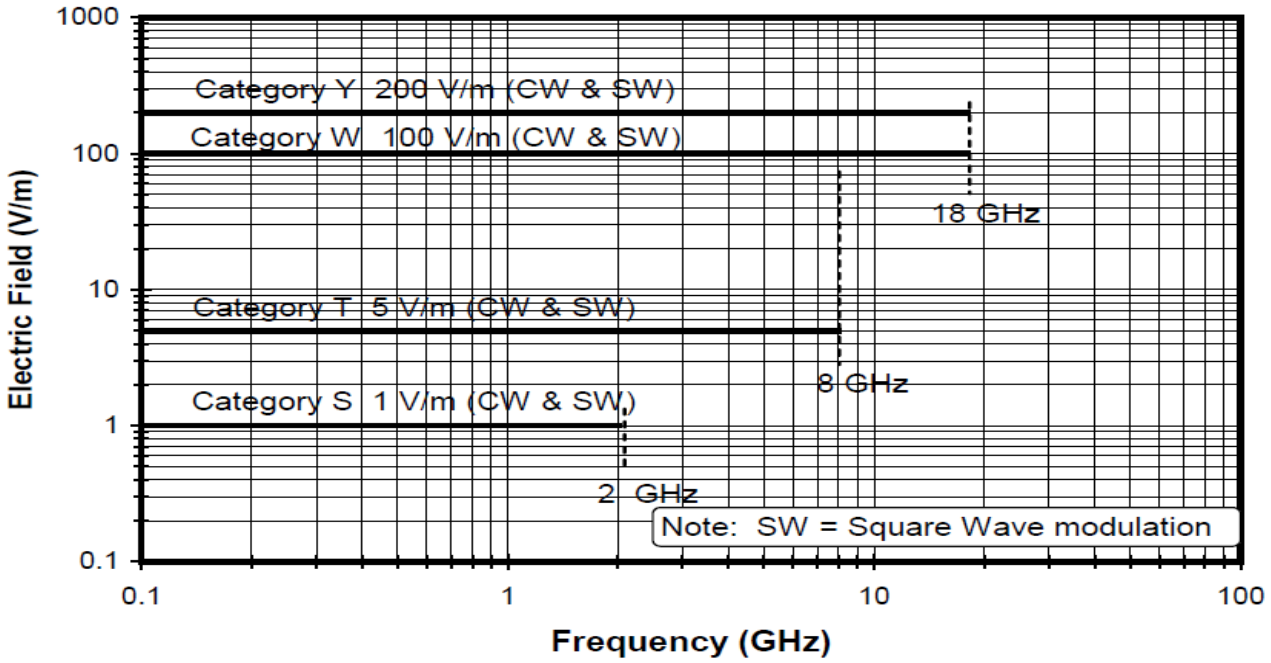



Figure 28: Radiated Susceptibility test levels.

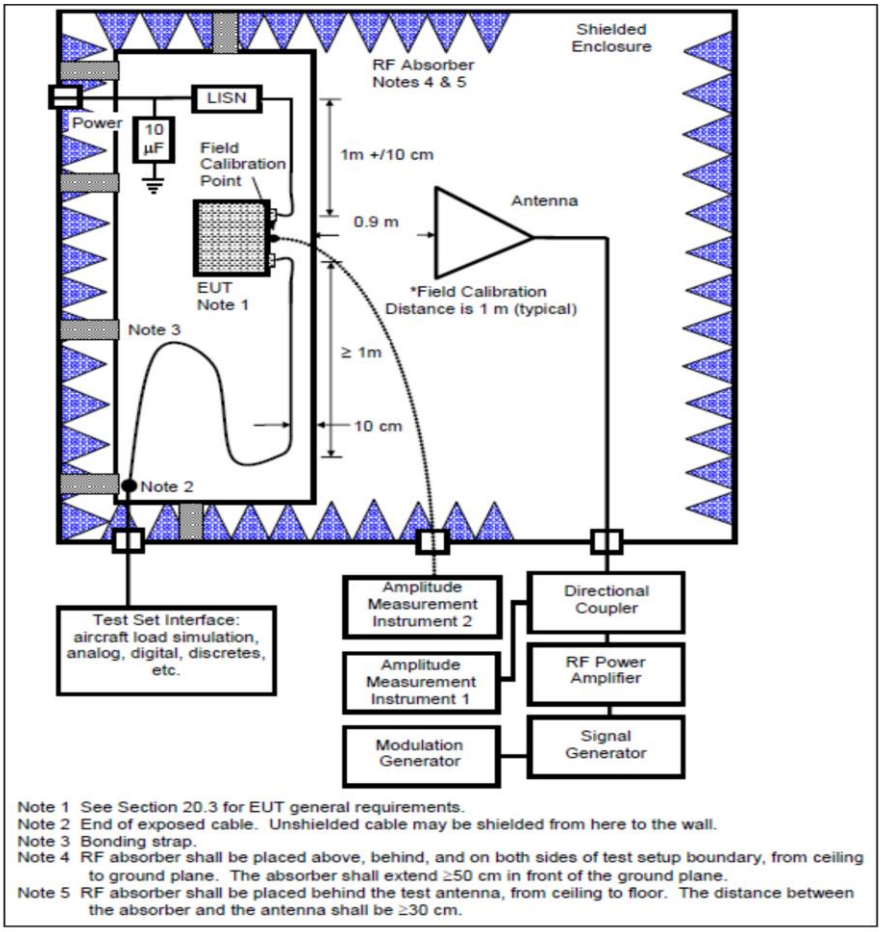



Figure 29: Radiated Susceptibility test setup.

## 4.10 EMISSION OF RADIO FREQUENCY ENERGY (RTCA DO-160G SECTION 21)

### 4.10.1 PURPOSE

The purpose of this test is to verify the EUT does not emit undesired RF noise in excess of the levels specified. This category is defined for equipment located in areas which are in direct view of a radio receiver's antenna and located outside of the aircraft.

### 4.10.2 APPLICABILITY

The test is applicable to the EUTs with the following classification:

AC PDP 1: Category H
AC PDP 2: Category H

### 4.10.3 TEST PROCEDURE CONDUCTED RF EMISSION (CE)

Measure conducted emissions from 150kHz to 152MHz. interference currents generated by the EUT shall be measured by using a clamp-on interference measuring device.

Table 7: Bandwidth and measurement times for Emission of Radiofrequency Energy test.

| Frequency Band | 6dB Bandwidth | Min Dwell Time [s](2) | Min Sweep Time for Frequency Band [s] | Min Measurement Time for Analog Measurement Receivers |
|---|---|---|---|---|
| 0.15MHz to 30MHz | 1kHz | 0.015 | N/A | 0.015 sec/kHz |
| 30MHz to 100MHz | 10kHz | 0.015 | N/A | 1.5 sec/MHz |
| 100MHz to 400MHz | 10kHz | 0.015 | 9 | 1.5 sec/MHz |
| 0.4GHz to 0.96GHz | 100kHz | 0.015 | 1 | 0.15 sec/MHz |
| 0.96GHz to 6GHz | 1MHz | 0.015 | 1 | 15 sec/GHz |

NOTE(2): Dwell time is compliant with the equipment operation because the EUT has not working cycle, the contactors don't change their status during both MODE 1 and MODE 2

1. Refer to Table 7 to refer to bandwidth and measuring times.
2. Verify the test setup has been built and configured as described in Figure 30.
3. Configure the EUTs for testing as shown in Figure 30.
4. Place CE Probe on J1 and J2 bundle at 5cm from the AC PDP 1 (if EUT connector plus back shell length exceeds 5cm the probe shall be placed as close to the connector back shell as possible and the position noted)
5. Place CE Probe on J1 and J2 bundle at 5cm from the AC PDP 2 (if EUT connector plus back shell length exceeds 5cm the probe shall be placed as close to the connector back shell as possible and the position noted)
6. For all the previous measurements, record the interface field and verify it is not out of the **RTCA-DO-160G** limits, see
7. Figure 31 (power lines) and
8. Figure 32 (interconnecting bundle). Primary power lines are not considered to be interconnecting cable bundles. Antenna feed cables are considered to be interconnecting cables while in a non-transmitting or receive mode.
9. Verify the status of the system as described. Any deviation will be recorded as a test failure

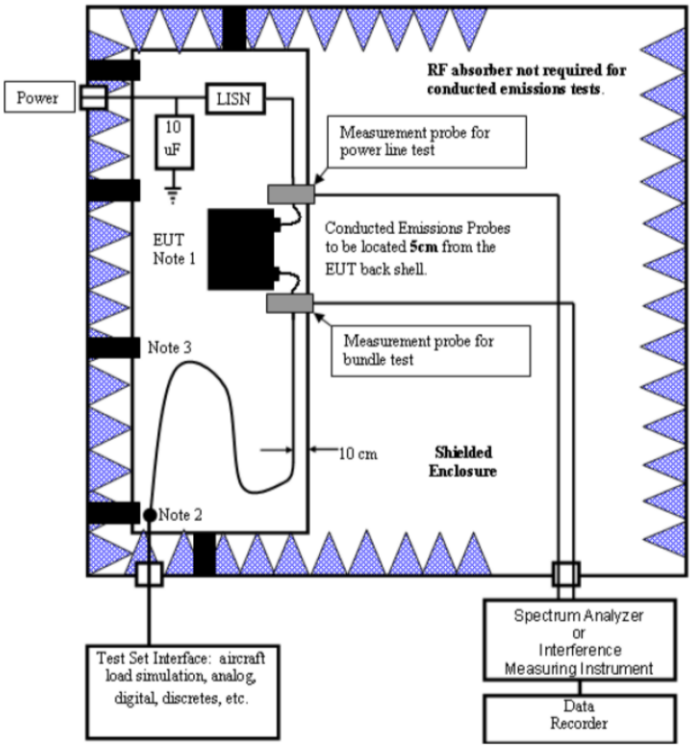
NOTE(1): The test will be done on interconnecting lines:

- J1 and J2 of AC PDP 1;
- J1 and J2 of AC PDP 2;

The test will not be applied to AC power lines connected to power stud INPUT / OUTPUT subject to 115VAC due to the fact that the EUT is a Power Distribution Unit, which takes the power produced by the generators to deliver it to loads, without the capability to modify or introduce any disturb (the power passes through the box).

#### *4.10.3.1 Acceptance Criteria*

Acceptance criteria and related limits are specified in **RTCA-DO-160G, for category H**
Figure 31 and
Figure 32).




**Note 1** See Section 20.3 for EUT general requirements.
**Note 2** End of exposed cable. Unshielded cable may be shielded from here to the wall.
**Note 3** Bonding strap.

Figure 30: Typical Test Setup for Conducted RF Interface Test.

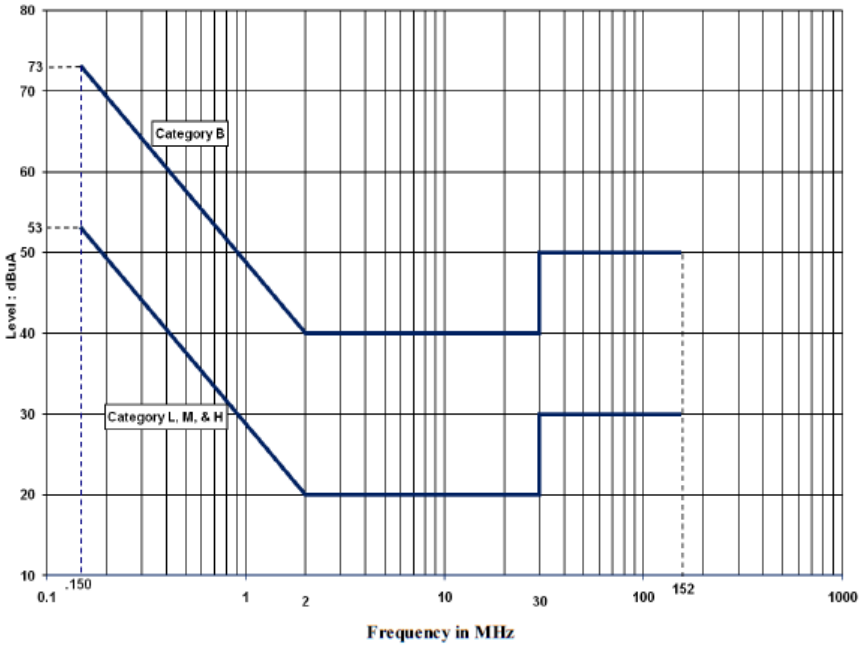



Figure 31: Conducted Emission limit - Category H - Power Lines.

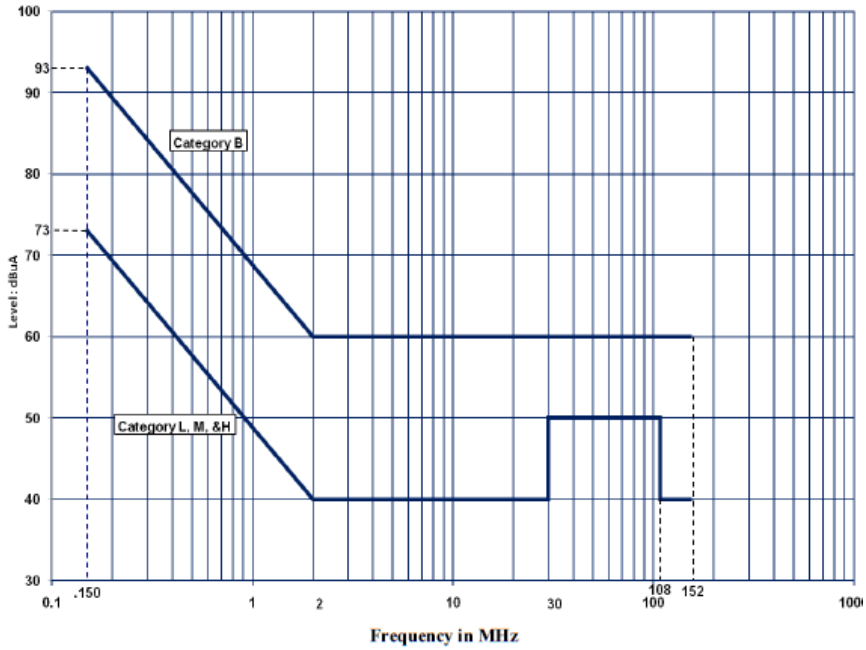



Figure 32: Conducted Emission limit - Category H – Interconnecting Bundle.

### 4.10.4 TEST PROCEDURE RADIATED RF EMISSION (RE)

Measure radiated emissions from 100MHz to 6000MHz

1. Refer to Table 7 to refer to bandwidth and measuring times.
2. Measure the ambient level prior to radiated emission test on EUT and verify that it is at least 6dB below the **RTCA DO-160G** limits.
3. Verify the test setup has been built and configured as described in figure below
4. Configure the EUTs for testing as shown
5. When the bandwidth does not totally cover the system under test, multiple area scans shall be performed. However, it is required that each EUT within the system and at least one half wavelength of wiring of that EUT shall be exposed in its entirety during the test

6. Place the appropriate antenna above the ground plane, as described by RTCA DO-160G
7. For the previous measurement, record the interference field and verify it is not out of the RTCA DO-160G limits
8. Verify the status of the system as described. Any deviation will be recorded as a test failure.

NOTE(1): Radiated ambient data (EUT "OFF" and test support equipment "ON") is required only if EUT emissions are greater than 3dB below the selected category limit

#### 4.10.4.1 Acceptance criteria

Acceptance criteria and related limits are specified in **RTCA-DO-160G, for Cat. H** and Figure 34.

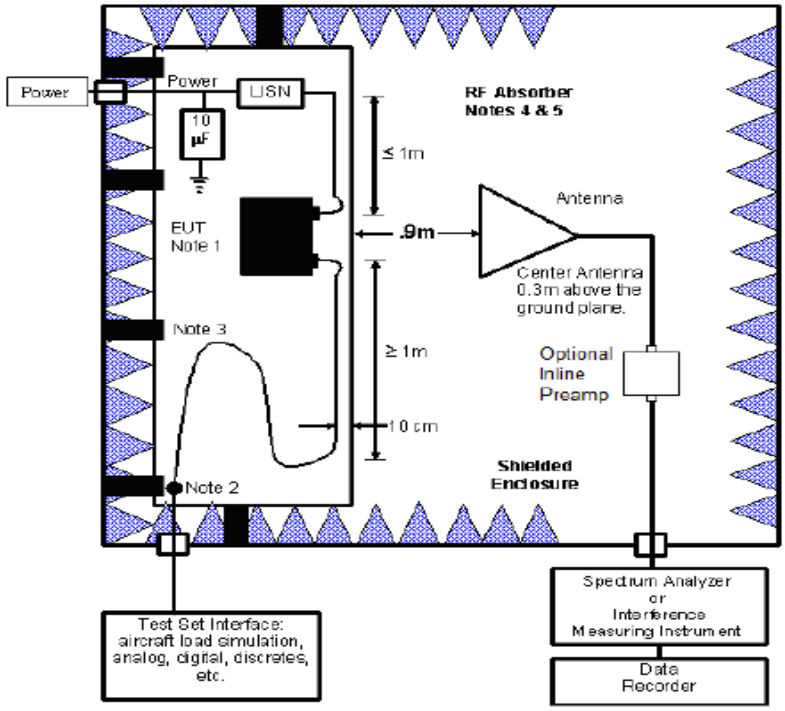



Figure 33: Radiated Emission test setup.

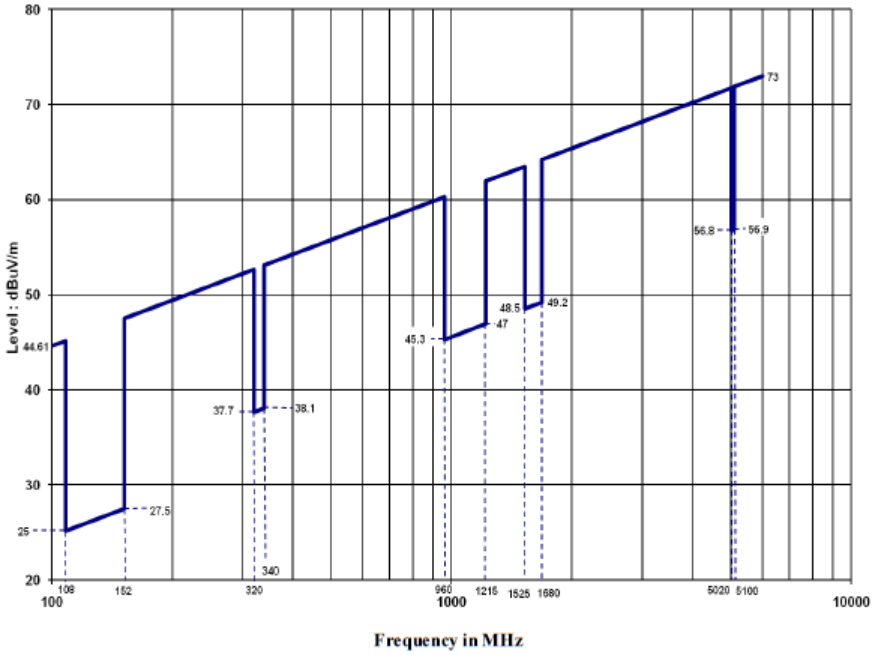



Figure 34: Maximum level of Radiated RF Interference – Category H.

# 5 QUALIFICATION TEST RESULTS (QTR)

## 5.1 AC PDP 1 AND AC PDP 2 PERFOMANCE TEST

This Performance Test Report details results of the tests carried out in order to reach qualification performance of the AC Electrical Power Distribution System (EPDS). The EPDS is composed by two AC Power Distribution Panels: AC PDP 1 and AC PDP 2.

Table 8: Test results for performance test AC PDP 1.

| Test Type | Test Result (PASS/FAIL) |
|---|---|
| Rated Capacity 16 kVA (46.4A) | PASS |
| Overload capacity 24 kVA (70A) | PASS |
| Overload capacity 25 kVA (72.5A) | PASS |
| OVERCURRENT | PASS |
| Under-frequency signal | PASS |
| Start 1 signal | PASS |
| Start 2 signal | PASS |
| OPM intervention curve for the Windshield | PASS |
| OPM intervention curve for the Heater | **FAILED** |

Table 9: Test results for performance test AC PDP 2.

| Test Type | Test Result (PASS/FAIL) |
|---|---|
| Rated Capacity 16kVA (46.4A) | PASS |
| Overload capacity 20 kVA (58A) | PASS |
| Overload capacity 28kVA (81.2A) | PASS |
| OVERCURRENT | PASS |
| Under-frequency signal | PASS |
| Start 1 signal | PASS |
| Start 2 signal | PASS |
| OPM intervention curve for the Windshield | PASS |
| OPM intervention curve for the Heater | PASS |

### 5.1.1 TEST CONDITIONS

All measurements and tests were carried out under the following conditions:
Temperature: +15°C ÷ +35ºC
Relative Humidity: 20% ÷ 85%
Atmosphere Pressure: 84kPa ÷ 107kPa

### 5.1.2 THERMAL STABILIZATION

Items are considered thermally stabilized when the temperatures of all their instrumented parts change no more than ±1°C in 5 minutes.

### 5.1.3 TEST EQUIPMENT

The following instrumentation (in Table 10) was used to perform the tests mentioned in this QTR document:

Table 10: Equipment for qualification test.

| Description | | Supplier | Model or Part Number | Serial Number |
|---|---|---|---|---|
| General purpose 28VDC power supply | | TTI | EX354D | 265739 |
| AC Load Bank #1 | | ASE S.p.A. | BT005 | N.A. |
| AC Load Bank #2 | | ASE S.p.A. | BT005 | N.A. |
| ATP Test Box | | ASE S.p.A. | DB15UC-AC | N.A. |
| Interface Harness | | ASE S.p.A. | DB22W | N.A. |

### 5.1.4 TEST INSTRUMENTATION AND ACCURACY

The following instrumentation (in Table 11) was used to perform the tests described in this document.

Table 11: Instrumentation for environmental qualification test.

| Description | Model | Supplier | Range | Accuracy | Parameter Measured | Calibration expiration |
|---|---|---|---|---|---|---|
| Meteo station | HM 30 | Thommen | -40 to +60°C | ±0.3°C | Ambient Temp. | 10/2022 |
| | | | 0 to 100% RH | ±1.5% RH | Ambient Humidity | |
| Data logger | 34970A | Agilent | 100Vdc input | 0.005% FS max | DC Voltage/ sensor outputs | 08/2022 |
| | | | 100Vac input | 0.17% FS on rms | AC Voltage rms | |
| | | | -100÷400°C | 1°C | Temperature | |
| Multimeter (6.5 digit) | DMM4040 | TEKTRONIX | 1000Vdc | 0.0026% FS max | Voltage | 06/2022 |
| | | | 3Adc | 0.07% FS max | Current | |
| | | | 100MΩ | 0.31% FS max | Resistance | |
| Oscilloscope | DL 850 | Yokogawa | 850/250V peak 0.04/2MHz | 1.5% | Voltage waveforms | 09/2022 |
| Micro-ohmmeter | CA6240 | CHAUVIN ARNOUX | 400u to 400 Ω | 5 % | Insulation resistance | 01/2023 |
| Dielectric strength tester | / | PESATORI | 0 to 3 kV Ileakage = 20 mA | 5 % | Dielectric strength | 12/2022 |

### 5.1.5 GENERAL TOLERANCES

Unless otherwise indicated during the test procedures, the maximum permissible tolerance for the test conditions (i.e. imposed test parameter) were listed below:

| | | | |
|---|---|---|---|
| Environmental | | Temperature | ± 3°C |
| | | Altitude | ± 5% of the specified pressure |
| | | Speed | ± 50rpm |
| Mechanical | **Sinusoidal Vibration**: | Acceleration | ±10% |
| | | Frequency | ±2% |
| | **Random Vibration**: | PSD value below 500Hz | +3dB; -1.5dB |
| | | PSD value 500Hz÷2000Hz | +3dB; -3dB |
| | | Overall g rms value | +20%; -5% |
| Electrical | | Force | ± 2% |
| | | Voltage | ± 1V |
| | | Current | ± 2A |
| | | Frequency | ± 2Hz |
| | | Power | ± 5% |

### 5.1.6 THE TEST SETUP

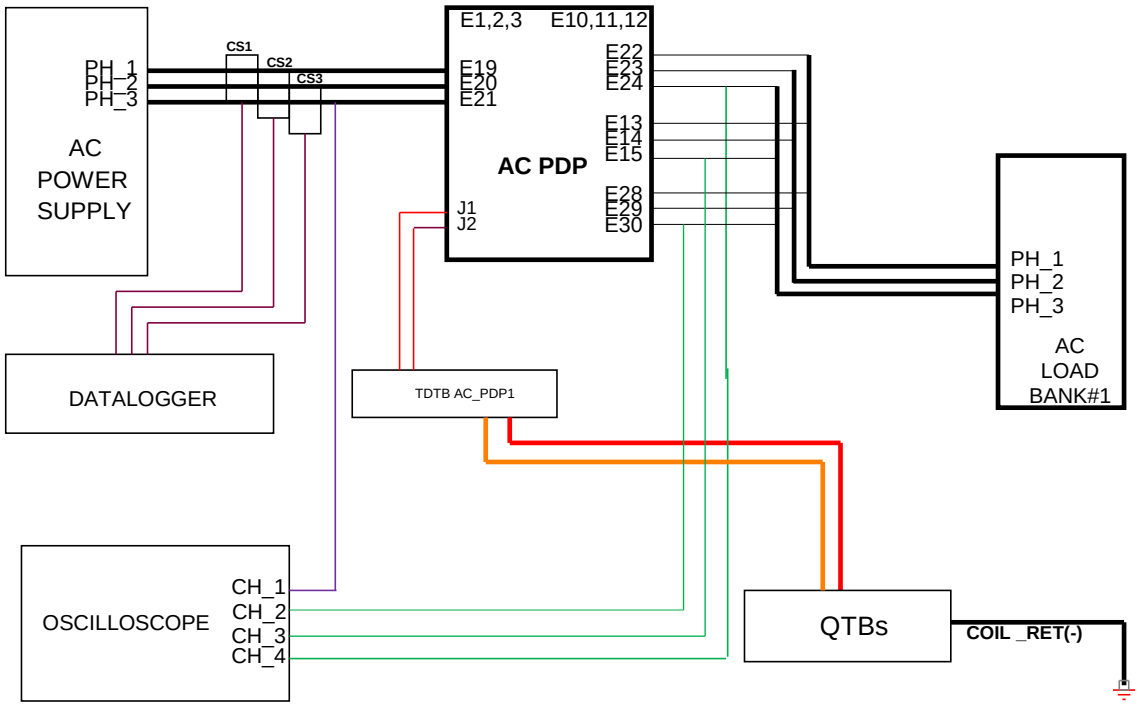



Figure 35: Test setup for performance of AC PDP 1 and AC PDP 2.

### 5.1.7 EUT STARTING STATE

The EUTs starting state (Initial Condition) is reported in Table 12 where all power contactors and relay must be de-energized.
Initial Condition will be verified by console of the AC Test Benches see Led ON LINE is OFF. At the end of all performance test this condition will be verified before initiate other test.
Before start with any functional test verify that all switches in the Control Console shall be in down position.

Table 12: Power Distribution Initial Condition

| Item Description | Condition |
|---|---|
| AC PDP 1 | ON LINE OFF |
| AC PDP 2 | ON LINE OFF |

NOTE: led ON LINE is the general synoptic light signal of the Control Console and it gives information about state of the Control Console.

### 5.1.8 TEST SEQUENCE

Tests are planned to be carried out according to the below sequence. The only constraint is about the first and the last step (pre-test and post-test ATPs). The tests within the two ATPs may be swapped depending upon actual test facility availability.

**Initial:**

1. Pre-test ATP on all EUTs

**Functional Tests:**

1. Performance test on AC PDP 1 Component and Characteristics.
2. Performance test on AC PDP 2 Component and Characteristics.
3. Overload Protection Module Test curve verification for AC PDP 1 and AC PDP 2.

**Final:**

1. Post-test ATP on all EUTs.

↓↓↓

**"Functional Test on the AC EPDS" session successful**

## 5.2 PERFORMANCE TEST ON AC PDP 1 AND AC PDP 2

Aim of the test is to verify components and characteristics of the AC PDP 1 and AC PDP 2. It is possible to verify the rating and overload characteristics of contactors and relays where is possible to drive directly the coil by pins of the circular connector and when the contactor is not protected by over-current. Where is not possible the test will be carried out in another modality.

The EUT will be driven by a control console of the AC Test Benches equipment. It is useful for simulating the external equipage of an A/C or avionic system. The console has a synoptic panel for checking the contactor state (ON/OFF).The test will be carried out in the following sub-steps:

1. Rated load – Contactors control and power distribution
2. Rated load – Continuous capacity
3. Overload condition
4. OPM module – Protection intervention and manual-in-flight resetting system.

### 5.2.1 INITIAL OPERATIONS

Before starting the performance test, it is required to verify the Start Initialization, particularly in the following reported stud (energy bar) that was de-energized. (0 Volt). In the following tables all the electrical interfaces and connector functions are described in order to simplify the setting of cables and connections of setup.

Table 13: Connections and electrical interfaces in AC PDP 1.

| Stud | I/O | Function |
|---|---|---|
| E1, E2, E3 | I | EXT AC POWER IN |
| E4, E5, E6 | I | APU POWER IN |
| E7, E8, E9 | O | AC BUS 1 OUT |
| E10, E11, E12 | I | AC BUS 2 IN |
| E13, E14, E15 | O | HEATER 1 POWER OUT |
| E16, E17, E18 | O | EXT AC POWER OUT |
| E19, E20, E21 | I | AC S/GEN 1 POWER IN |
| E22, E23, E24 | O | TRU 1 POWER OUT |
| E25, E26, E27 | O | HYDRAULIC PUMP POWER OUT |
| E28, E29, E30 | O | CPLT WINDSHIELD HEATER POWER OUT |

Table 14: Connections and electrical interfaces in AC PDP 2.

| Stud | I/O | Function |
|---|---|---|
| E1, E2, E3 | I | APU POWER IN |
| E4, E5, E6 | I | EXT AC POWER IN |
| E7, E8, E9 | O | AC BUS 2 OUT |
| E10, E11, E12 | I | AC BUS 1 IN |
| E13, E14, E15 | O | HEATER 2 POWER OUT |
| E16, E17, E18 | O | APU POWER OUT |
| E19, E20, E21 | I | AC S/GEN 2 POWER IN |
| E22, E23, E24 | O | TRU 2 POWER OUT |
| E25, E26, E27 | O | SRU POWER OUT |
| E28, E29, E30 | O | PLT WINDSHIELD HEATER POWER OUT |

### 5.2.2 TEST SETUP DETAILS

The instrument and equipment of Table 10 and Table 11 are used and an oscilloscope as measuring instrument is chosen to record the following parameters:

1. Voltage input (Three-phase AC)

2. Current output ( T1, T2, T3 External Current sensor)
3. Voltage output (Three-phase AC)
4. Time of act of K1 contactor (AC PDP 1) and K2 contactor (AC PDP 2)
5. Temperature (look at detailed view of the positions of thermocouples)
6. Steady state current
7. Transient current consumption

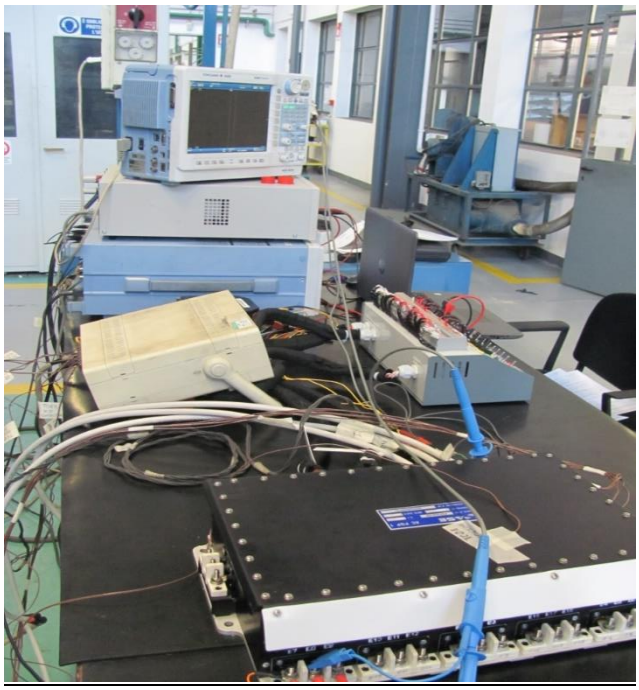


Figure 36: Test setup optimized for AC PDP 1.

Figure 37: Test setup optimized for AC PDP 2.

### 5.2.3 RATED LOAD FOR AC PDP 1

Table 15: Rated load condition and closed contactors for AC PDP 1.

| Load | Stud | | Contactor |
|---|---|---|---|
| | In | Out | |
| 16kVA (46.4A) | E19, E20, E21 | E13, E14, E15 (=17.4A)<br>E22, E23, E24 (=11.6A)<br>E28, E29, E30 (=17.4A) | K1<br>K5<br>K7<br>K51 |

### 5.2.4 OVERLOAD CONDITION FOR AC PDP 1

Table 16: Overload condition and closed contactors for AC PDP 1.

| Load | Time | Stud | | Contactor |
|---|---|---|---|---|
| | | In | Out | |
| 24kVA (69.6A) | 5min | E19, E20, E21 | E13, E14, E15 (=27.6A)<br>E22, E23, E24 (=14.4A)<br>E28, E29, E30 (=27.6A) | K1<br>K5<br>K7<br>K51 |
| 25kVA (72.5A) | 5s | E19, E20, E21 | E13, E14, E15 (=28.1A)<br>E22, E23, E24 (=16.3A)<br>E28, E29, E30 (=28.1A) | K1<br>K5<br>K7<br>K51 |

### 5.2.5 RATED LOAD FOR AC PDP 2

Table 17: Rated load condition and closed contactors for AC PDP 2.

| Load | Stud | | Contactor |
|---|---|---|---|
| | In | Out | |
| 16kVA (46.4A) | E19, E20, E21 | E13, E14, E15 (=15.2A)<br>E22, E23, E24 (=16.0A)<br>E28, E29, E30 (=15.2A) | K2<br>K6<br>K8<br>K61 |

### 5.2.6 OVERLOAD CONDITION FOR AC PDP 2

Table 18: Overload condition and closed contactors for AC PDP 2.

| Load | Time | Stud | | Contactor |
|---|---|---|---|---|
| | | In | Out | |
| 20kVA (58.0A) | 5min | E19, E20, E21 | E13, E14, E15 (=19.6A)<br>E22, E23, E24 (=18.9A)<br>E28, E29, E30 (=19.6A) | K2<br>K6<br>K8<br>K61 |
| 28kVA (81.2A) | 5s | E19, E20, E21 | E13, E14, E15 (=27.8A)<br>E22, E23, E24 (=25.5A)<br>E28, E29, E30 (=27.8A) | K2<br>K6<br>K8<br>K61 |

### 5.2.7 OPERATION – RATED LOAD AND OVERLOAD TESTS

The main objectives of the sub-tests are:

1. **Contactor controls and power distribution**: ensure that contactors shut when the Qualification Test Box sends an external signal and that all closure requirements are "true." The bus voltage will also be measured at the load box, which will be linked to the PDP's studs.

2. **Continuous capacity**: verify the system is able to manage required continuous output currents. The continuous capacity test will be carried out by imposing the worst load conditions (G19 – Cruise Combat condition)

3. **Overload**: verify if the overload conditions (fault) of the current drawn at any stud is more than the rated current of the circuit breakers (CB). So the temperature of the units is controlled by means of thermocouples and CBs shall be verified to be opened when the fault condition is reached according to the trip curve reported in Figure 38: Circuit breakers trip curve.

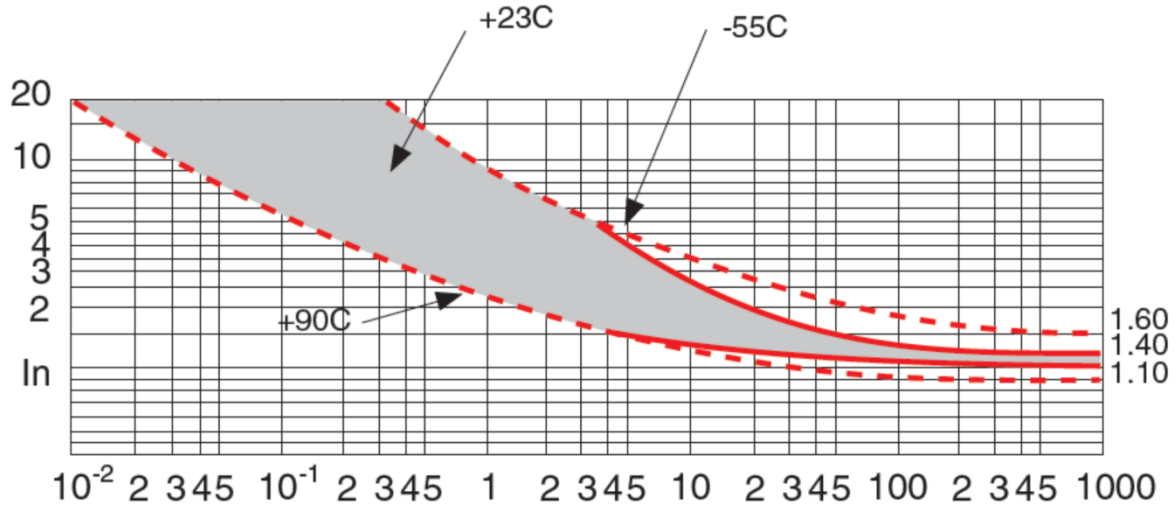



Figure 38: Circuit breakers trip curve.

### 5.2.8 TEST PROCEDURE OF AC PDP 1

| STEP | ACTION | CHECK |
|---|---|---|
| | **PRE-REQUISITES** | |
| 1. | Ensure the EUT has passed the pre-test ATP | |
| 2. | Ensure that the EUT and all the switches are in the starting state described in §5.1.7 | |
| 3. | Perform test setup operations as detailed in Figure 35 | |
| 4. | Connect terminals of AC Power Supply to the input studs E19, E20, E21 | |
| 5. | Set AC Power Supply to give 115V±0.5V voltage | |
| 6. | Connect AC Load Bank #1 to power output studs:<br>- L1=E22, E23, E24; L2=E13, E14, E15; L3=E28, E29, E30 | |
| | **INITIAL OPERATIONS** | |
| 7. | Set the data-logger to acquire the system parameters defined in § 5.2.2 | |
| 8. | Set the oscilloscope to acquire frequency coherence of phase-to-phase INPUT and OUTPUT studs | |
| | **TEST CORE – CONTACTOR CONTROLS AND POWER DISTRIBUTION** | |
| 9. | Start recording parameters with the data-logger | |
| 10. | Turn ON the AC Power Supply | |
| 11. | Verify that the system is ONLINE (related switch and led on test box) | |
| 12. | Close K1, K5 on BUS 1 side, K7, and K51 contactors by means of test box switches | |
| 13. | Set AC Load Bank in order to absorb 46.4A±5A (16kVA) | |
| 14. | Verify current from external current sensors CS1, CS2 and CS3 (46.4A±5A, 16kVA) | |
| 15. | At E22, E23, E24 studs verify that output voltage is 115V±0.5V and output current is 11.6A±5A | |
| 16. | At E13, E14, E15 studs verify that output voltage is 115V±0.5V and output current is 17.4A±5A | |
| 17. | At E28, E29, E30 studs verify that output voltage is 115V±0.5V and output current is 17.4A±5A | |
| 18. | Keep the rating condition for 5min | |
| 19. | Turn OFF the AC Load Bank | |
| 20. | Stop and save data-logger acquisition | |
| | **TEST CORE – CONTINUOUS CAPACITY** | |
| 21. | Start recording parameters with the data-logger | |
| 22. | Maintain K1, K5 on BUS 1 side, K7 and K51 in closed condition by mean of test box switches | |
| 23. | Set AC Load Bank in order to absorb 46.4A±5A (16kVA) | |
| 24. | Verify current from external current sensors CS1, CS2 and CS3 (46.4A±5A, 16kVA) | |
| 25. | Keep the rating condition for a time not less than 15min (thermal stabilization §5.10.2) | |
| 26. | Monitor the internal temperature of the EUT and verify it is not over 85°C after thermal stabilization is reached | |
| | **TEST CORE – OVERLOAD** | |
| 27. | Set AC Load Bank in order to absorb 69.6A±5A (24kVA) | |
| 28. | Verify current from external current sensors CS1, CS2 and CS3 (69.6A±5A, 24kVA) | |
| 29. | Maintain this 69.6A±5A (24kVA) overload condition for 5min | |
| 30. | Verify that overload conditions (fault) of the current drawn at any stud is more than the rated current of the circuit breakers (CB), according to Figure 38 | |
| 31. | Verify that CB opens in the right time of intervention according to the related temperature and following curve described in Figure 38 | |
| 32. | Monitor the internal temperature of the EUT and verify it is not over 85°C | |
| 33. | Set AC Load Bank in order to absorb 72.5A±5A (25kVA) | |
| 34. | Verify current from external current sensors CS1, CS2 and CS3 (72.5A±5A, 25kVA) | |
| 35. | Maintain this 72.5A±5A (25kVA) overload condition for 5s | |
| 36. | Verify that overload conditions (fault) of the current drawn at any stud is more than the rated current of the circuit breakers (CB), according to Figure 38 | |

| STEP | ACTION | CHECK |
|---|---|---|
| 37. | Verify that CB opens in the right time of intervention according to the related temperature and following curve described in Figure 38 | |
| 38. | Monitor the internal temperature of the EUT and verify it is not over 85°C | |
| | **FINAL OPERATIONS** | |
| 39. | Remove all AC Load applied at the system | |
| 40. | Stop and save data-logger acquisition | |
| 41. | Open all the contactors | |
| 42. | Verify 0VAC at output studs | |

### 5.2.9 PERFORMANCE TEST RESULTS FOR AC PDP 1

The purpose of the test is to confirm that the external power contactor closes when the external signal from the Qualification Test Box is supplied, and that all of the closure conditions are "true." The bus voltage also tested at the load box, which is linked to the PDP's studs.

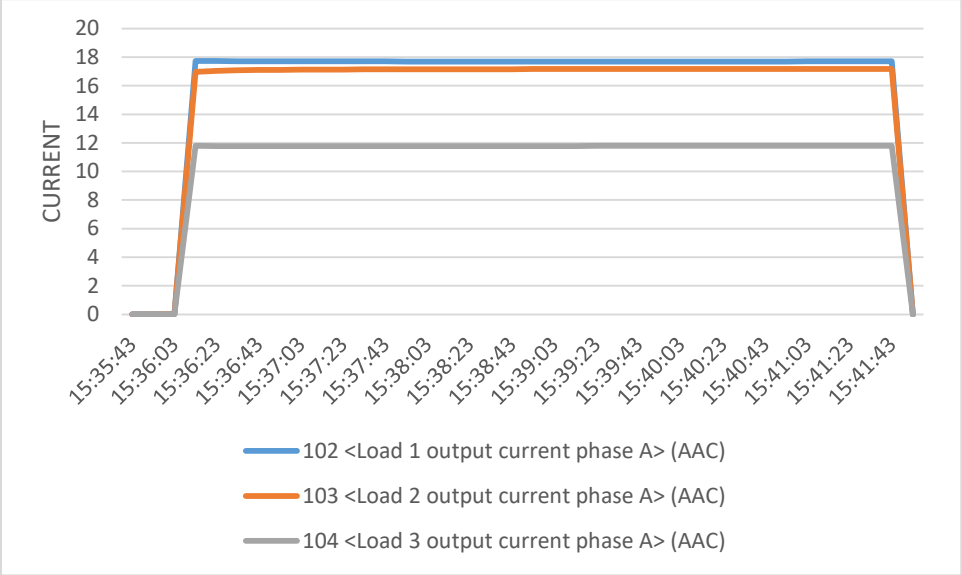



Figure 39: Current distribution during contactor control

The continuous capacity test ensures that the system can supply the needed continuous output currents while preserving the minimum output voltages under previous load conditions (Total AC load 48,25A). The rating condition is maintained for more than 15 minutes.
Figure 40 displays current variations during a 15-minute continuous capacity test.

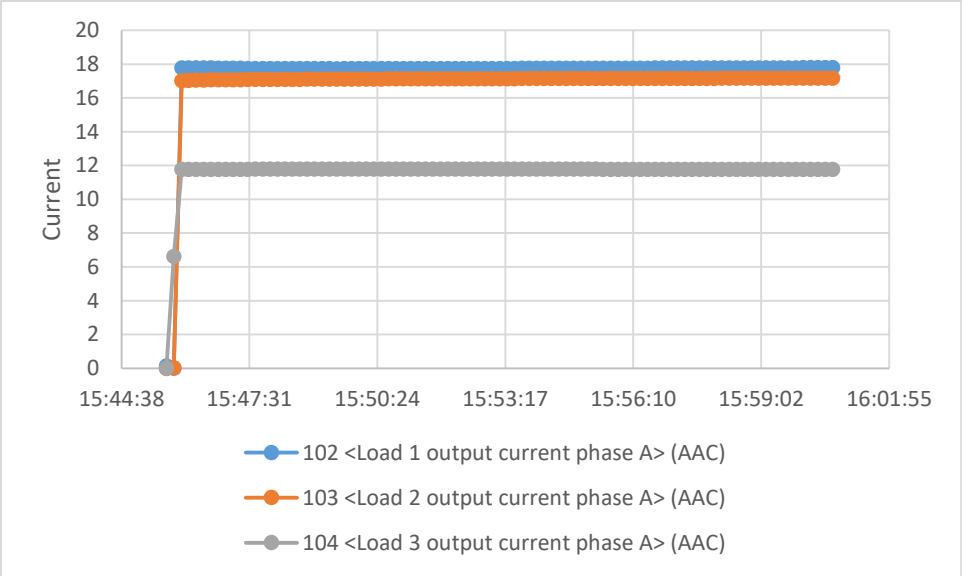



Figure 40: Output current distribution during continuous capacity

Table 19: Measured output currents and input voltage during continuous capacity

| TIME | Load 1 output current phase A | Load 2 output current phase A | Load 2 output current phase A | Output voltage phase A |
|---|---|---|---|---|
| **10:46:18** | 0,040763 | 0,036574 | 0,005429 | 115,2317 |
| **10:47:18** | 17,41011 | 18,28019 | 12,52358 | 114,9898 |
| **10:49:19** | 17,39109 | 18,28782 | 12,55133 | 114,9914 |
| **10:51:20** | 17,40388 | 18,28175 | 12,56232 | 114,9951 |
| **10:53:21** | 17,42151 | 18,27217 | 12,57128 | 114,992 |
| **10:55:17** | 17,4334 | 18,26423 | 12,57931 | 114,9971 |
| **10:57:18** | 17,44525 | 18,25864 | 12,58375 | 114,9982 |
| **10:59:19** | 17,45409 | 18,18764 | 12,58764 | 115,0051 |
| **11:01:20** | 17,46332 | 18,19058 | 12,59058 | 115,0149 |

According to the observed output voltage of 114.98 V AC and input voltage of 115.23 V AC on phase A, the total load consumption is 48.25 A, therefore the dissipated power is equal to:

$$P = (V_{in} - V_{out}) \times 3 \times I_{PhA} = 36.15W$$

Table 20: Thermocouples position for AC PDP 2

| TC | Location |
|---|---|
| TC01 | K1 Contactor |
| TC02 | K3 Contactor |
| TC03 | K5 Contactor |
| TC04 | OPM Board |
| TC05 | Housing |
| TC06 | Circuit Breaker 1 |
| TC07 | Circuit Breaker 3 |
| TC08 | Protection Board |

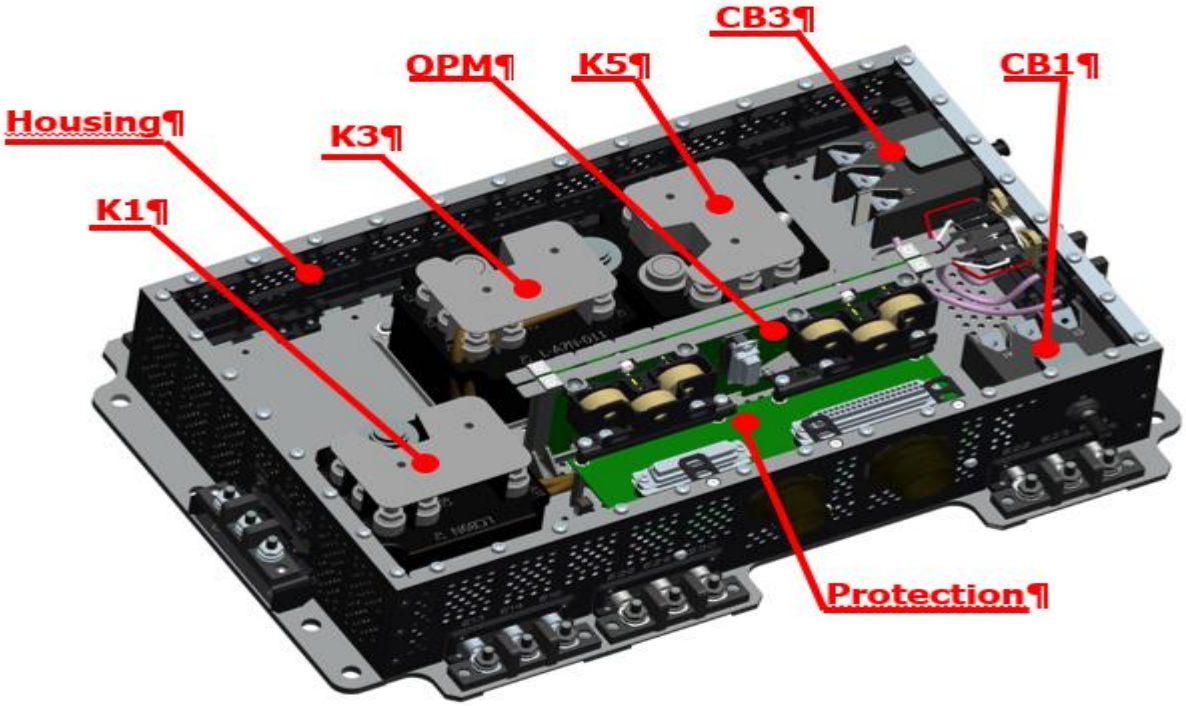



Figure 41: Thermocouple location for the AC PDP 1

Following figure displays temperature variations during a 15-minute continuous capacity test.

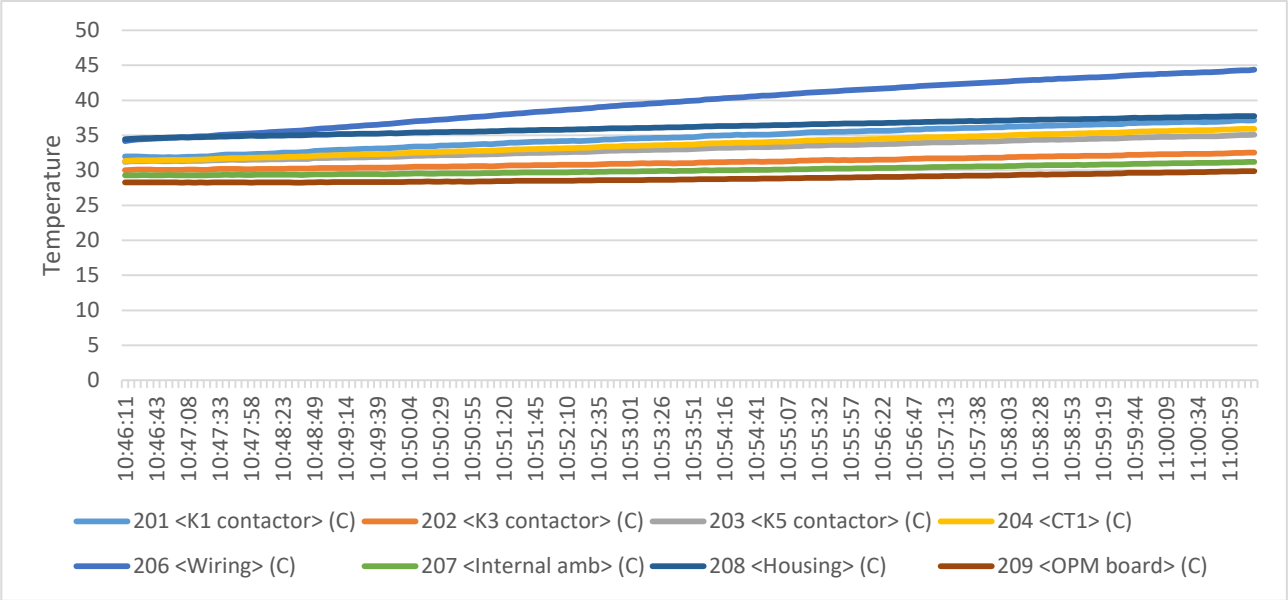



Figure 42: Temperature changes during continuous capacity

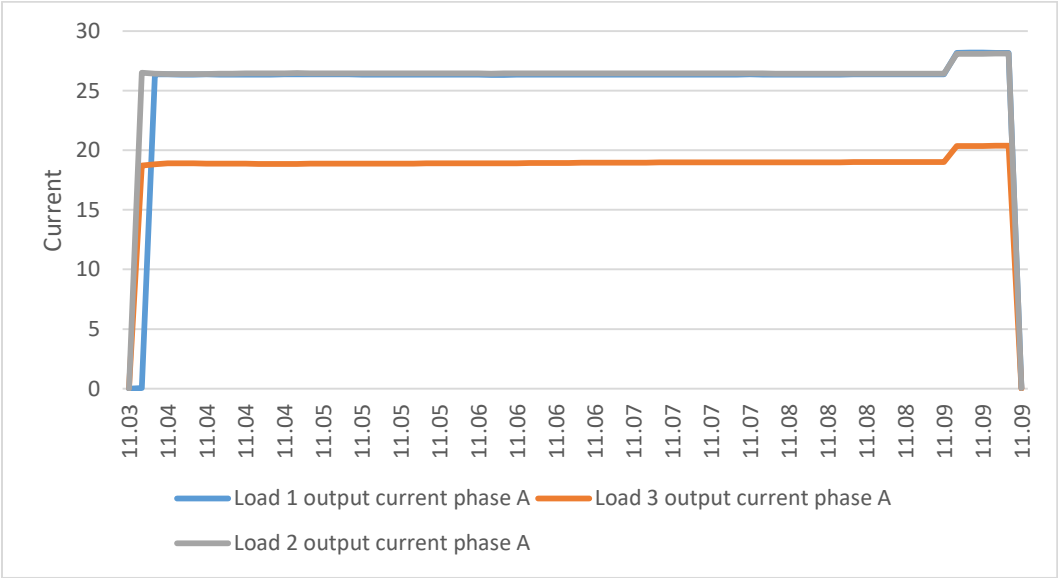



Figure 43: OVERLOAD condition 71,8A

Table 21: Measured current and voltage values during overload condition

| Time | Load 1 output current phase A | Load 3 output current phase A | Load 2 output current phase A | Input voltage phase A |
|---|---|---|---|---|
| **11:11:03** | 0,007676 | 0,036315 | 0,004644 | 115,2785 |
| **11:11:04** | 26,36769 | 18,86098 | 26,46089 | 114,6885 |
| **11:11:05** | 26,36545 | 18,86236 | 26,46717 | 114,6896 |
| **11:11:06** | 26,34814 | 18,90852 | 26,45211 | 114,6874 |
| **11:11:07** | 26,35144 | 18,96139 | 26,45733 | 114,687 |
| **11:11:07** | 26,35083 | 18,98941 | 26,43763 | 114,637 |
| **11:11:08** | 26,34967 | 18,99175 | 26,43573 | 114,6348 |
| **11:11:08** | 26,36434 | 19,01716 | 26,42568 | 114,6395 |
| **11:11:09** | 28,17452 | 20,37979 | 28,10379 | 114,56 |
| **11:11:09** | 0,039082 | 0,004127 | 0,035148 | 115,237 |

### 5.2.10 TEST PROCEDURE OF AC PDP 2

**PRE-REQUISITES:**

1. Before starting the test, ensure the EUT has passed the pre-test ATP
2. Ensure that the EUT and all the switches are in the starting state described in §5.1.7
3. Perform test Set-Up as reported in Figure 35.
4. Connect terminals of AC Power Supply to the input studs E19, E20, E21
5. Set AC Power Supply to give 115V±0.5V voltage
6. Connect AC Load Bank to power output studs:
   - E22, E23, E24
   - E13, E14, E15
   - E28, E29, E30

**INITIAL OPERATIONS:**

7. Set Oscilloscope to acquire frequency coherence of phase-to-phase input and output studs.
8. Set the data logger for acquiring of the system parameters defined in §5.2.2

**TEST CORE –CONTACTOR CONTROLS AND POWER DISTRIBUTION:**

9. Start recording parameters with the data-logger
10. Turn ON the 3 phase 115 VAC AC Power Supply
11. Verify that the system is ONLINE (related switch and led on test box)
12. Close K2, K6 on BUS 2 side, K8, and K61 contactors by means of test box switches
13. Set AC Load Bank in order to absorb **in total** 46.4A±5A (16kVA)
14. Verify current from external current sensors CS1, CS2 and CS3 (46.4A±5A, 16kVA)
15. At E22, E23, E24 studs verify that output voltage is 115V±0.5V and output current is 16A±5A
16. At E13, E14, E15 studs verify that output voltage is 115V±0.5V and output current is 15.2A±5A
17. At E28, E29, E30 studs verify that output voltage is 115V±0.5V and output current is 15.2A±5A
18. Keep the rating condition for 5min
19. Turn OFF the AC Load Bank
20. Stop and save data-logger acquisition.

**TEST CORE – CONTINUOUS CAPACITY:**

21. Start recording the parameters with the data-logger
22. Maintain K2, K6 on BUS 1 side, K8 and K61 in closed condition by mean of test box switches
23. Set AC Load Bank in order to absorb 46.4A±5A (16kVA)
24. Verify current from external current sensors CS1, CS2 and CS3 (46.4A±5A, 16kVA)
25. Keep the rating condition for a time not less than 15min (thermal stabilization §4.8.2)
26. Monitor the internal temperature of the EUT and verify it is not over 85°C after thermal stabilization is reached

**TEST CORE – OVERLOAD:**

27. Set AC Load Bank in order to absorb 58.0A±5A (20kVA)
28. Verify current from external current sensors CS1, CS2 and CS3 (58.0A±5A, 20kVA)
29. Maintain this 58.0A±5A (20kVA) overload condition for 5min
30. Verify that overload conditions (fault) of the current drawn at any stud is more than the rated current of the circuit breakers (CB), according to

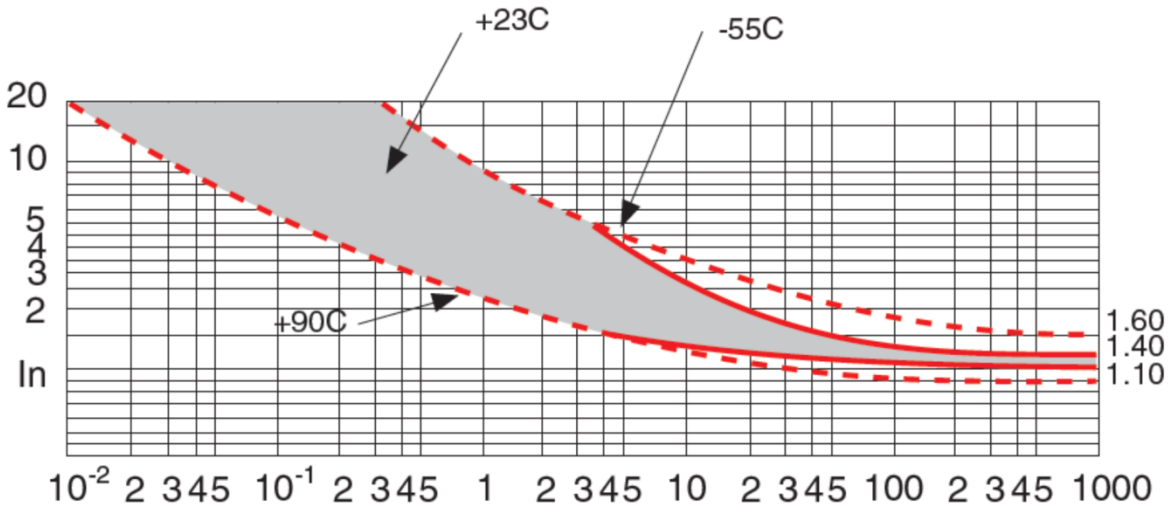



Figure 38.

31. Verify that CB opens in the right time of intervention according to the related temperature and following curve described in

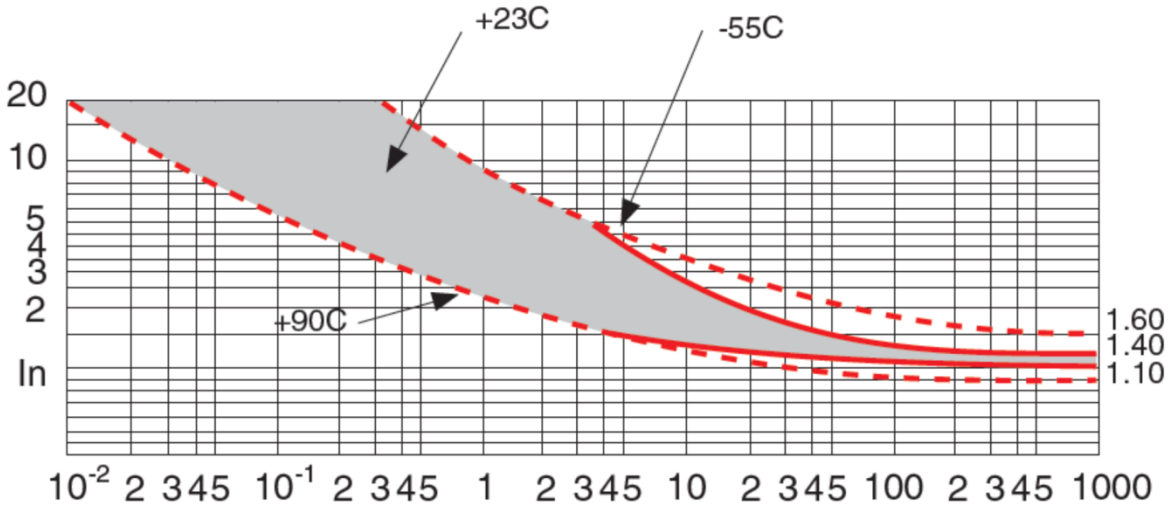



Figure 38.

32. Monitor the internal temperature of the EUT and verify it is not over 85°C
33. Set AC Load Bank in order to absorb 81.2A±5A (28kVA)
34. Verify current from external current sensors CS1, CS2 and CS3 (81.2A±5A, 28kVA)
35. Maintain this 81.2A±5A (28kVA) overload condition for 5seconds
36. Verify that overload conditions (fault) of the current drawn at any stud is more than the rated current of the circuit breakers (CB), according to

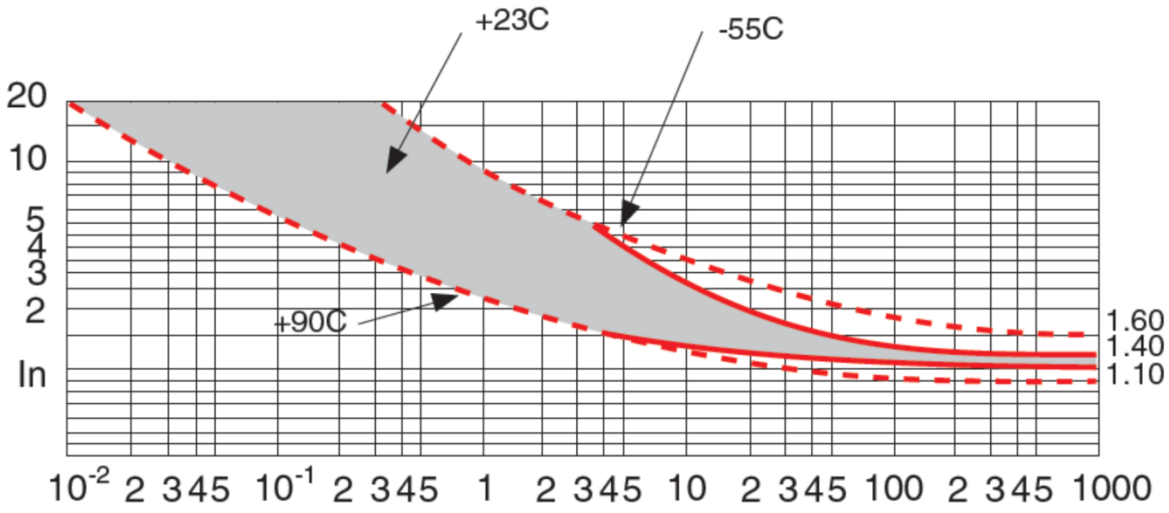



Figure 38

37. Verify that CB opens in the right time of intervention according to the related temperature and following curve described in

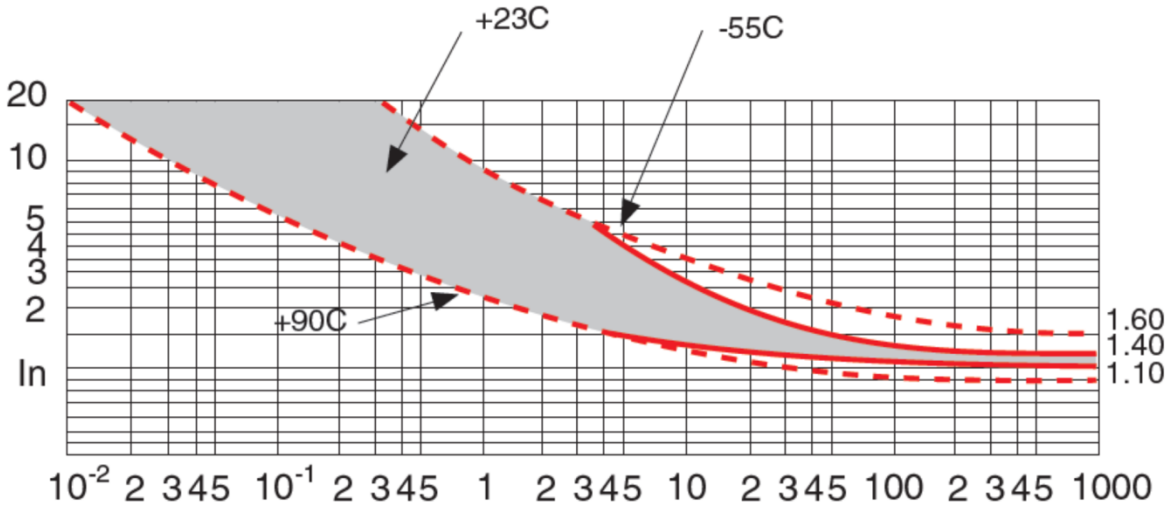



Figure 38.

38. Monitor the internal temperature of the EUT and verify it is not over 85°C

**FINAL OPERATIONS:**

39. Remove all AC Load applied at the system
40. Stop and save data-logger acquisition
41. Open all the contactors
42. Verify 0VAC at output studs

### 5.2.11 PERFORMANCE TEST RESULTS AC PDP 2

The purpose of the test is to ensure that the external power contactor closes when the external signal from the Qualification Test Box is sent, and that all of the closure conditions are "true." The bus voltage will also be checked at the load box, which will be connected to the PDP's studs. AC Load Bank is absorbing 47A as Total load during the Contactor Controls and Power Distribution test for 5 minutes.

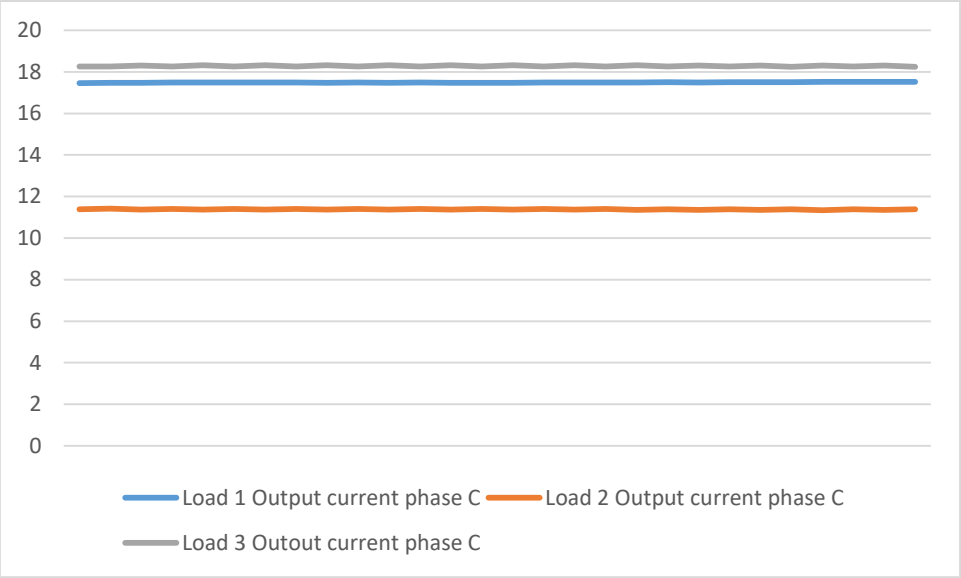


Figure 44: Measured output current currents during contactor control and power distribution

Table 22: Thermocouples position for AC PDP 2.

| TC | LOCATION |
|---|---|
| TC01 | K2 Main Contactor |
| TC02 | K4 Contactor |
| TC03 | K6 Contactor |
| TC04 | K12 Contactor |
| TC05 | OPM Board |
| TC06 | Housing |
| TC07 | CB2 |
| TC08 | Protection board |

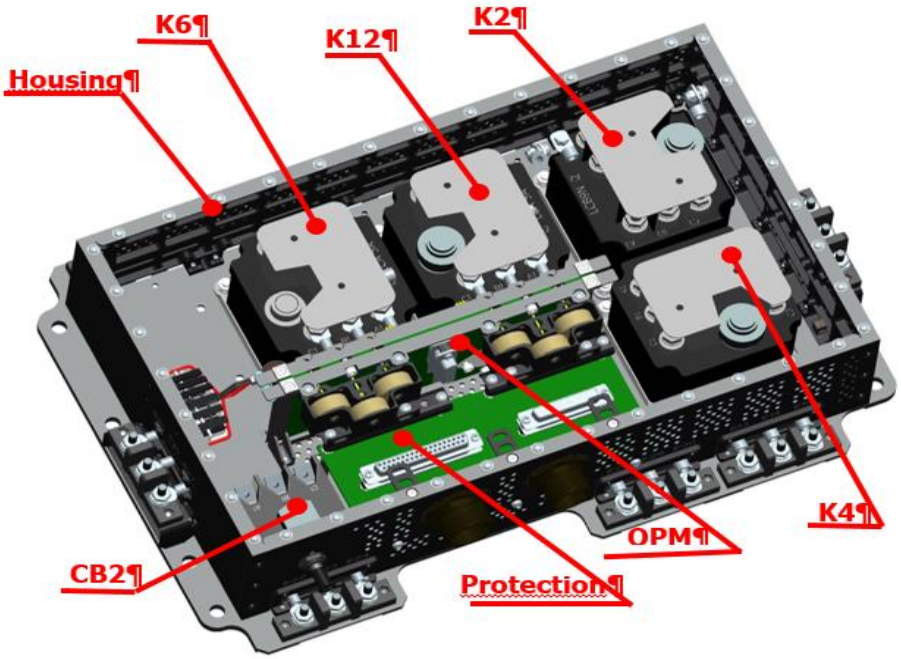


Figure 45: Thermocouple location for the AC PDP 2

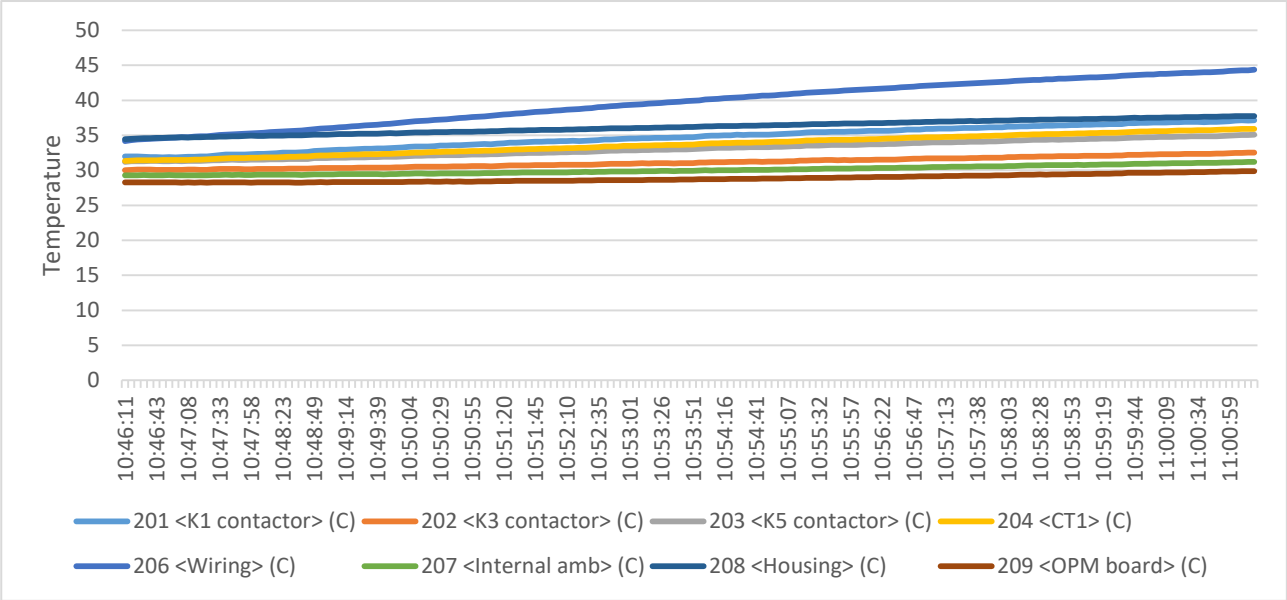



Figure 46 displays temperature variations during a 15-minute continuous capacity test.

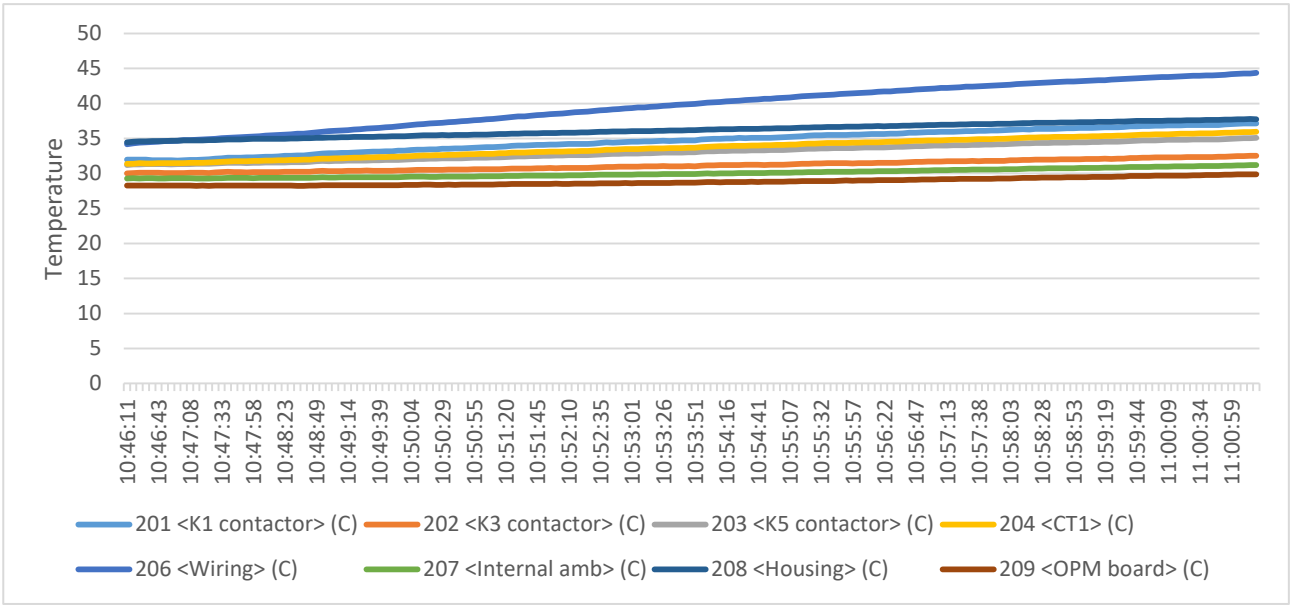



Figure 46: Temperature changes during continuous capacity

The purpose of the continuous capacity test is to ensure that the system can provide the required continuous output currents while maintaining the minimum output voltages under previous load condition (Total AC load 47 A). Rating condition is kept more than 15 minutes.

Table 23: Measured currents and voltage during continuous capacity.

| Time | Load 1 Output current phase C | Load 2 Output current phase C | Load 3 Output current phase C | Voltage phase C |
|---|---|---|---|---|
| **10:45:07** | 17,17681 | 10,86118 | 19,36064 | 114,5621 |
| **10:45:14** | 17,16691 | 10,88284 | 19,30834 | 114,565 |
| **10:45:21** | 17,18225 | 10,86025 | 19,35806 | 114,5617 |
| **10:45:28** | 17,16975 | 10,88326 | 19,3072 | 114,5615 |
| **10:45:35** | 17,17153 | 10,85973 | 19,35754 | 114,5618 |

Based on the observed output voltage of 114.56 V AC and the observed input voltage of 115.23 V AC on phase A, the total load consumption is 47.26 A, and thus the dissipated power equals:

$$P = (V_{in} - V_{out}) \times 3 \times I_{PhA} = 20.84W$$

**POWER DISSIPATION**: P=20.84W

Following continuous capacity test, the overload conditions are applied, as shown in Table 24 and Figure 47 by the levels of current readings during the overload condition.

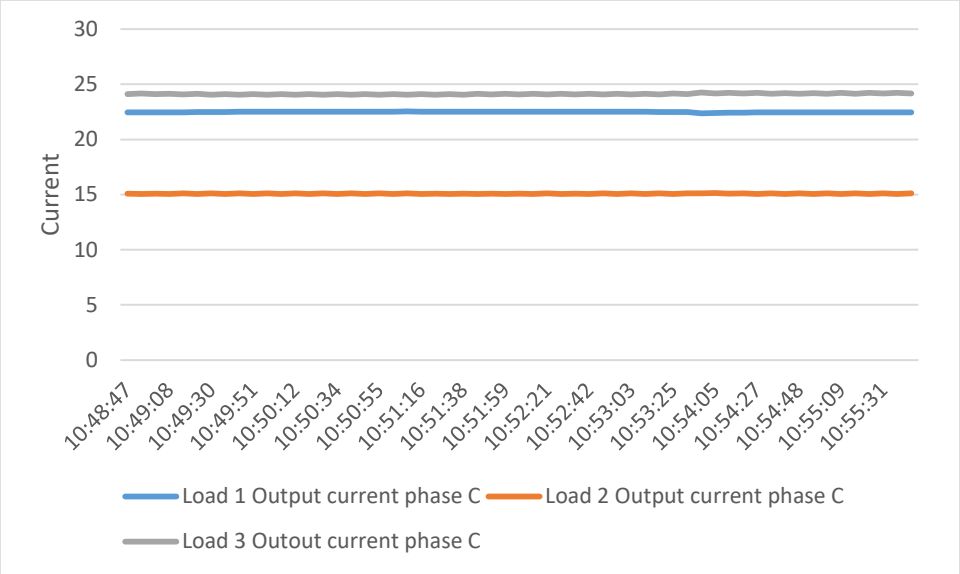



Figure 47: Measured output current during overload condition 61 A.

Table 24: Measured output currents and voltage during second overload 82A condition.

| Time | Load 1 Output current phase C | Load 2 Output current phase C | Load 3 Output current phase C | Voltage phase C |
|---|---|---|---|---|
| **16:15:17** | 27,24858 | 18,584 | 34,58844 | 113,8274 |
| **16:15:25** | 28,73846 | 19,85101 | 34,54448 | 113,8322 |
| **16:15:32** | 28,7454 | 19,86117 | 34,47461 | 113,8283 |
| **16:15:39** | 28,75778 | 19,95873 | 34,39941 | 113,8426 |
| **16:15:46** | 28,76564 | 19,9593 | 34,3613 | 113,8389 |
| **16:15:53** | 28,7711 | 20,0233 | 51,44097 | 113,6704 |

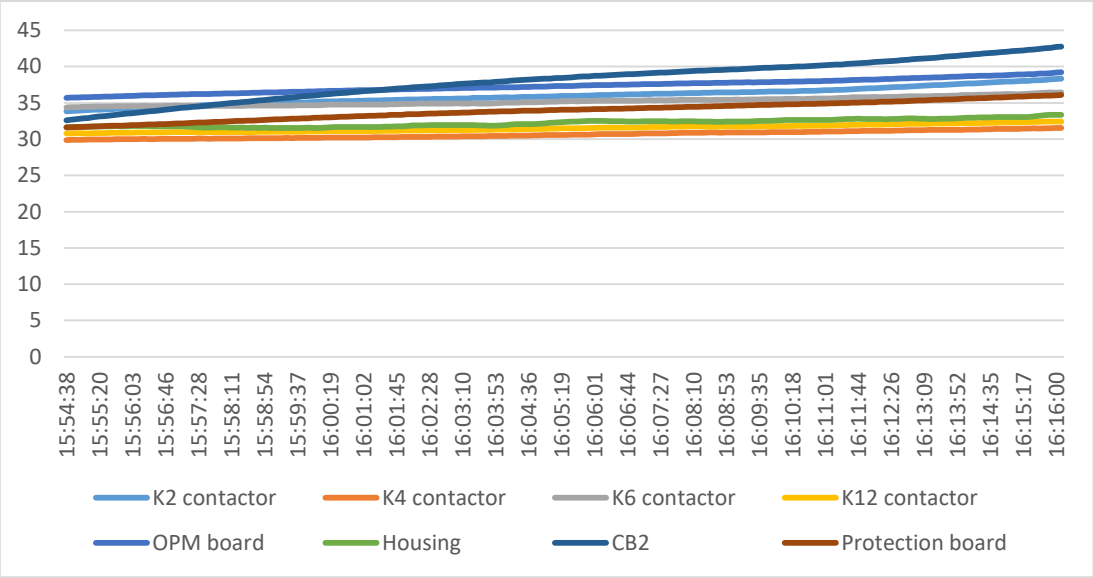


Figure 48: Temperature readings during overload tests

## 5.3 OVERCURRENT PROTECTION MODULE BOARD TEST

The Overcurrent Protection Module Board is a simple hardware printed circuit board which drives two external power contactors according to two three-phases measured input currents. If the current exceeds the limits set by a current-time intervention curve, the contactor is disconnected after a time directly proportional to the magnitude of the overcurrent and the corresponding circuit breaker is tripped. The overcurrent condition is kept in memory by the OPM Board until a reset signal is provided.

After the verification of the right protection intervention, also the manual-in-flight resetting system has to be verified. Main contactor opened and bus voltage will be disconnected at the outputs of heaters and windshields. Intervention of TRU circuit breaker will be verified.
Moreover, the correct opening/closing of contactors K7/K8 and K51/K61 (AC PDP 1/AC PDP2) has to be verified when signals of Under-frequency, Start 1 and Start 2 are applied/removed.

The exact relation between disconnect time and overcurrent is presented in
Figure 49. It shows the trip curve defining the way the board operates when an event of overload, short circuit, single phase or three phases fault exceeds an overcurrent trip curve.

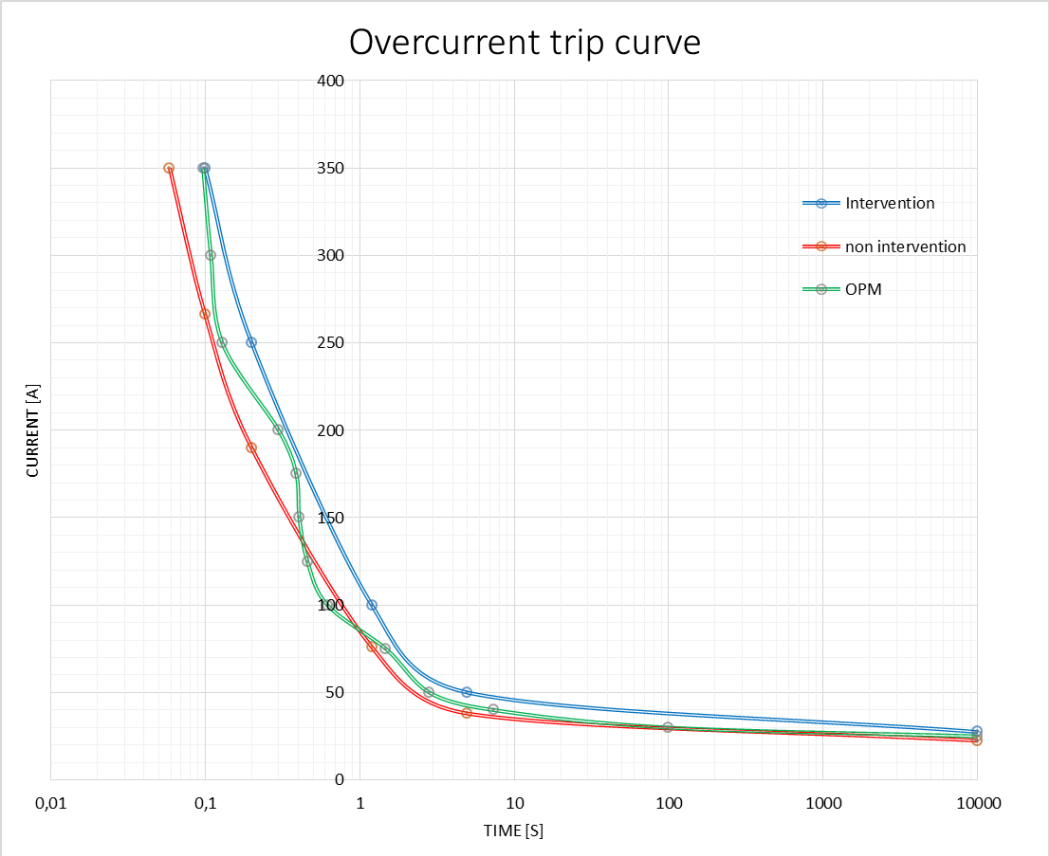



Figure 49: Overload protection module trip curve.

### 5.3.1 OPM BOARD TEST PROCEDURE OF AC PDP 1

| STEP | ACTION | CHECK |
|---|---|---|
| | **PRE-REQUISITES** | |
| 1. | Ensure the EUT has passed the pre-test ATP | |
| 2. | Ensure that the EUT and all the switches are in the starting state described in §5.1.7 | |
| 3. | Perform test setup operations as detailed in Figure 35 | |
| 4. | Connect terminals of AC Power Supply to the input studs E19, E20, E21 | |
| 5. | Set AC Power Supply to give 115V±0.5V voltage | |
| 6. | Connect AC Load Bank #1 to power output studs:<br>- E13, E14, E15<br>- E28, E29, E30 | |
| | **INITIAL OPERATIONS** | |
| 7. | Set the data-logger to acquire the system parameters defined in §5.2.2 | |
| 8. | Set the oscilloscope to acquire frequency coherence of phase-to-phase INPUT and OUTPUT studs | |
| | **TEST CORE – OVERCURRENT** | |
| 9. | Start recording parameters with the data-logger | |
| 10. | Turn ON the AC Power Supply | |
| 11. | Verify that the system is ONLINE (related switch and led on test box) | |
| 12. | Close K1, K7 and K51 contactors by means of test box switches | |
| 13. | Set AC Load Bank in order to absorb 25A±5A for each phase | |
| 14. | Verify current from external current sensors CS1, CS2 and CS3 (25A±5A) | |
| 15. | At E13, E14, E15 studs verify that output current is 23A+/-2A | |
| 16. | At E28, E29, E30 studs verify that output current is 23A+/-2A | |
| 17. | Keep the rating condition and wait for thermal stabilization §5.1.2 | |
| 18. | Monitor internal temperature of the EUT and verify it is not over 85°C after thermal stabilization is reached | |
| 19. | Set AC Load Bank in order to absorb 30A±5A for each phase | |
| 20. | Verify current from external current sensors CS1, CS2 and CS3 (30A±5A) | |
| 21. | Verify that the time of intervention of the OPM board follows properly the trip curve of Figure 49 | |
| 22. | Once the trip occurred, RESET the initial condition by means of test box | |
| 23. | Verify that the initial steady state condition is restored | |
| 24. | Repeat steps 19, 20, 21, 22 and 23 with the following load conditions:<br>• 40A±5A<br>• 50A±5A<br>• 75A±5A<br>• 100A±5A<br>• 125A±5A<br>• 150A±5A<br>• 175A±5A<br>• 200A±5A<br>• 250A±5A<br>• 300A±5A<br>• 350A±5A | |
| 25. | Remove all AC Load applied at the system | |
| 26. | Stop and save data-logger acquisition | |
| 27. | Open all the contactors | |
| 28. | Verify 0VAC at all the studs | |
| | **TEST CORE – UNDERFREQUENCY** | |
| 29. | Start recording parameters with the data-logger | |
| 30. | Close K1, K7 and K51 contactors by means of test box switches | |
| 31. | At E13, E14, E15 studs verify that output voltage is 115V±0.5V | |
| 32. | At E28, E29, E30 studs verify that output voltage is 115V±0.5V | |
| 33. | Turn ON the “Underfrequency” signal | |
| 34. | Verify that K7 and K51 contactors open automatically when the signal is turned on | |
| 35. | Verify 0V at E13, E14, E15 and E28, E29, E30 | |
| 36. | Turn OFF the “Underfrequency” signal | |
| 37. | Verify that K7 and K51 contactors close automatically when the signal is turned off | |

| STEP | ACTION | CHECK |
|---|---|---|
| 38. | At E13, E14, E15 studs verify that output voltage is 115V±0.5V | |
| 39. | At E28, E29, E30 studs verify that output voltage is 115V±0.5V | |
| 40. | Stop and save data-logger acquisition | |
| **TEST CORE – START 1** | | |
| 41. | Start recording parameters with the data-logger | |
| 42. | Verify that K1, K7 and K51 contactors are in closed condition | |
| 43. | At E13, E14, E15 studs verify that output voltage is 115V±0.5V | |
| 44. | At E28, E29, E30 studs verify that output voltage is 115V±0.5V | |
| 45. | Turn ON the “Start 1” signal | |
| 46. | Verify that K7 and K51 contactors open automatically when the signal is turned on | |
| 47. | Verify 0V at E13, E14, E15 and E28, E29, E30 | |
| 48. | Turn OFF the “Start 1” signal | |
| 49. | Verify that K7 and K51 contactors close automatically when the signal is turned off | |
| 50. | At E13, E14, E15 studs verify that output voltage is 115V±0.5V | |
| 51. | At E28, E29, E30 studs verify that output voltage is 115V±0.5V | |
| 52. | Stop and save data-logger acquisition | |
| **TEST CORE – START 2** | | |
| 53. | Start recording parameters with the data-logger | |
| 54. | Verify that K1, K7 and K51 contactors are in closed condition | |
| 55. | At E13, E14, E15 studs verify that output voltage is 115V±0.5V | |
| 56. | At E28, E29, E30 studs verify that output voltage is 115V±0.5V | |
| 57. | Turn ON the “Start 2” signal | |
| 58. | Verify that K7 and K51 contactors open automatically when the signal is turned on | |
| 59. | Verify 0V at E13, E14, E15 and E28, E29, E30 | |
| 60. | Turn OFF the “Start 2” signal | |
| 61. | Verify that K7 and K51 contactors close automatically when the signal is turned off | |
| 62. | At E13, E14, E15 studs verify that output voltage is 115V±0.5V | |
| 63. | At E28, E29, E30 studs verify that output voltage is 115V±0.5V | |
| **FINAL OPERATIONS** | | |
| 64. | Open all the contactors | |
| 65. | Stop and save data-logger acquisition | |
| 66. | Stop AC Power Supply | |

### 5.3.2 OPM BOARD TEST RESULTS FOR AC PDP 1

The value recorded during the test for intervention curve is shown in the figures below.

**LOAD 1**-Power output studs E13, E14, E15;
**LOAD 2**- Power output studs E28, E29, E30.

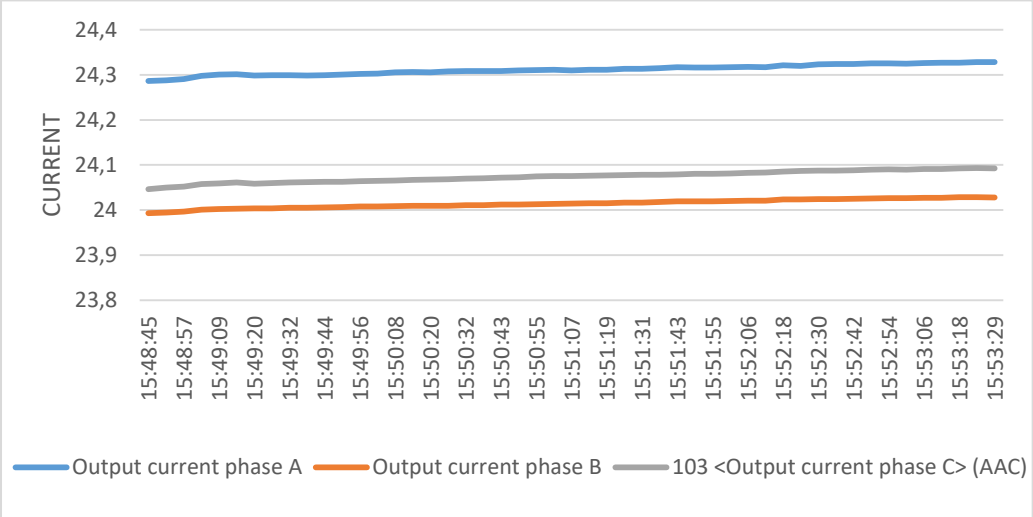



Figure 50: 25A LOAD rated condition

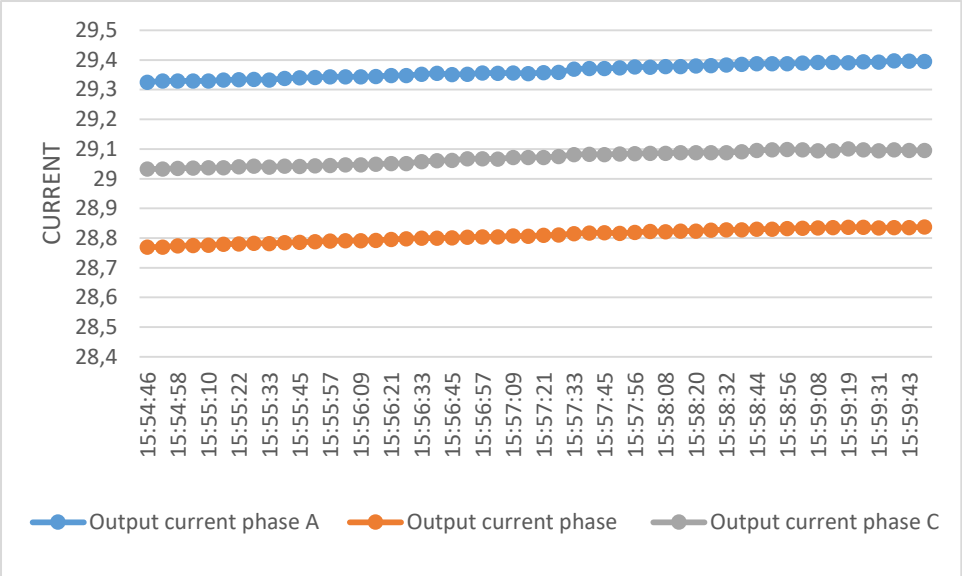



Figure 51: 30A LOAD NO INTERVENTION

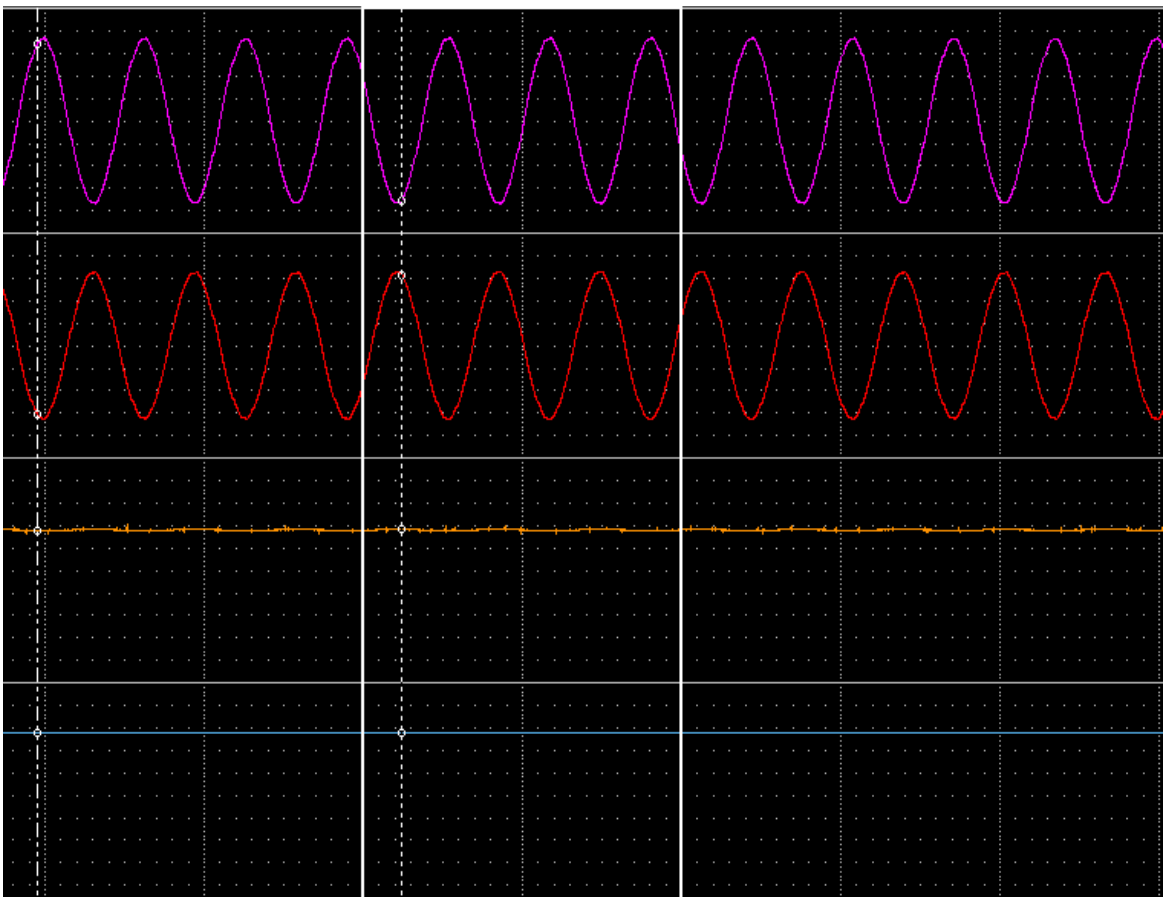


Figure 52: 30 A LOAD NO INTERVENTION DATA FROM OSCILLOSCOPE

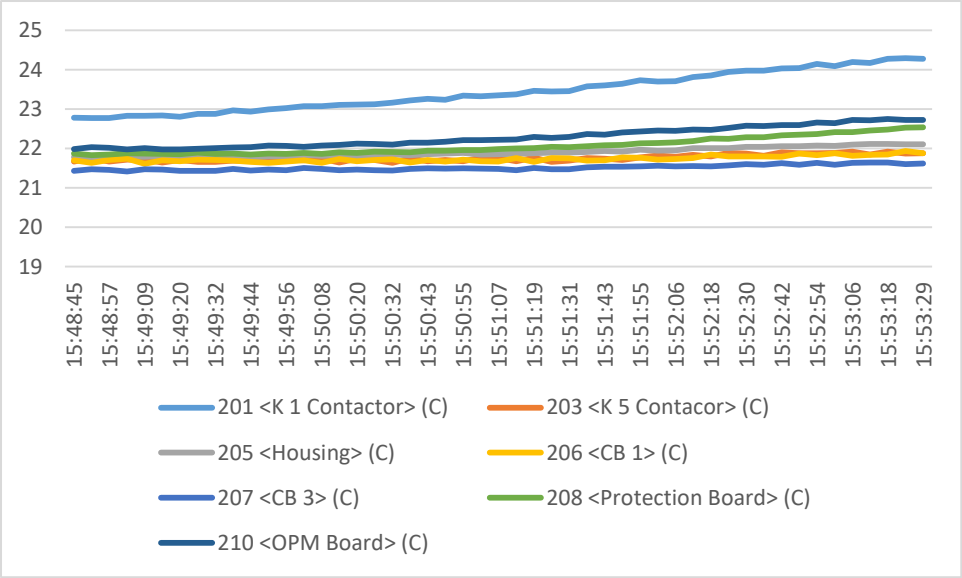



Figure 53: TEMPERATURE CHANGES DURING 40 A LOAD

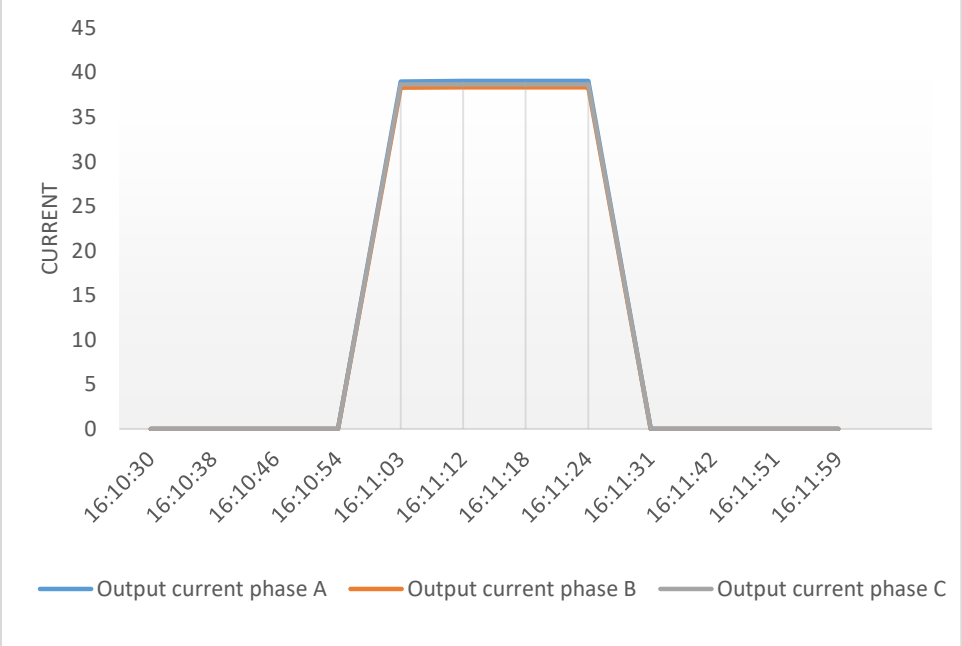



Figure 54: 40 A LOAD

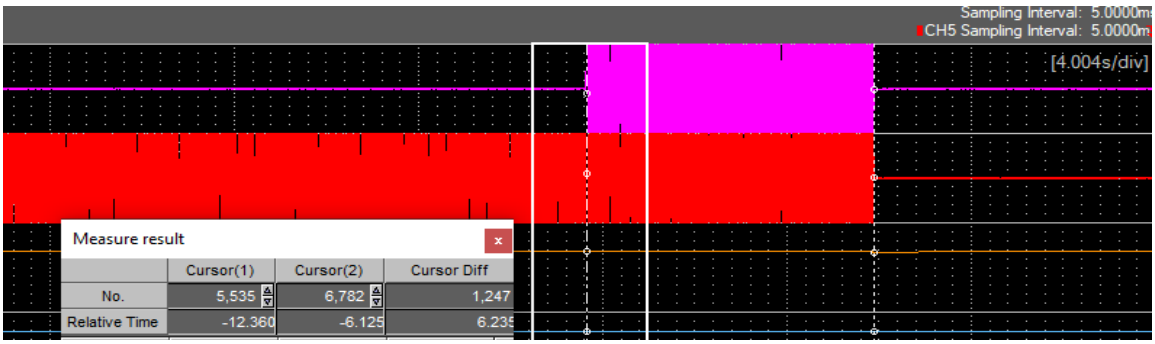



Figure 55: Load 50 A (6.235sec)

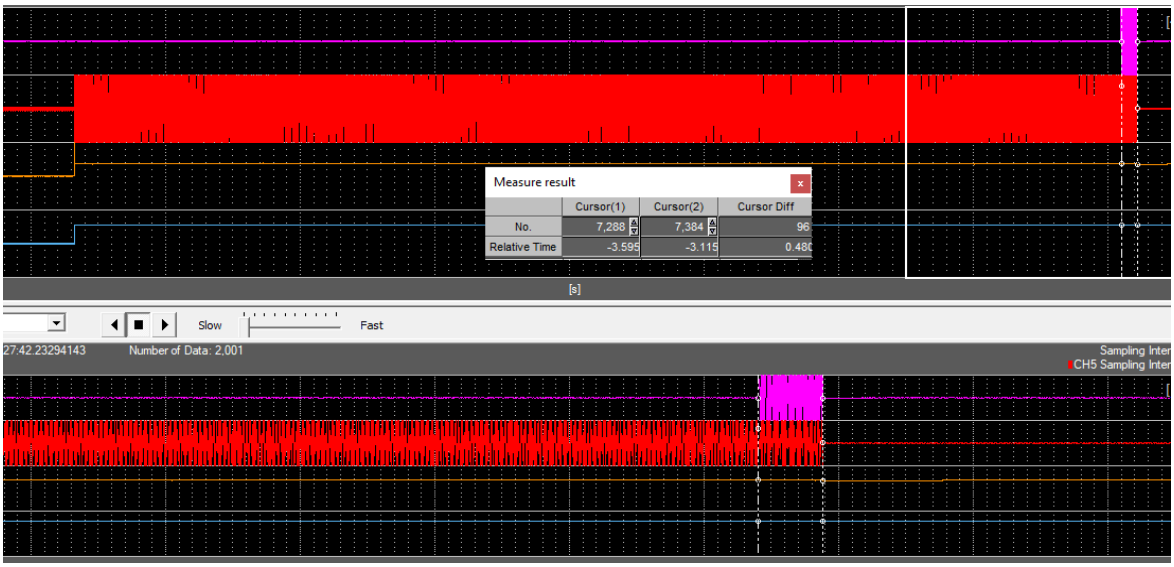



Figure 56: 100 A LOAD (480ms)

Table 25: Value recorded for the WIINDSHIELD 1 (LOAD 2) intervention time AC PDP 1.

| **INTERVENTION TIME (ms)** | **Load 2 (Amper)** |
|---|---|
| ∞ | **24.75** |
| ∞ | **29** |
| ∞ | **33** |
| **20000** | **39** |
| **62350** | **48** |
| **2940** | **59** |
| **2610** | **74** |
| **2340** | **80** |
| **465** | **100** |
| **325** | **125** |
| **280** | **150** |
| **165** | **175** |
| **95** | **200** |

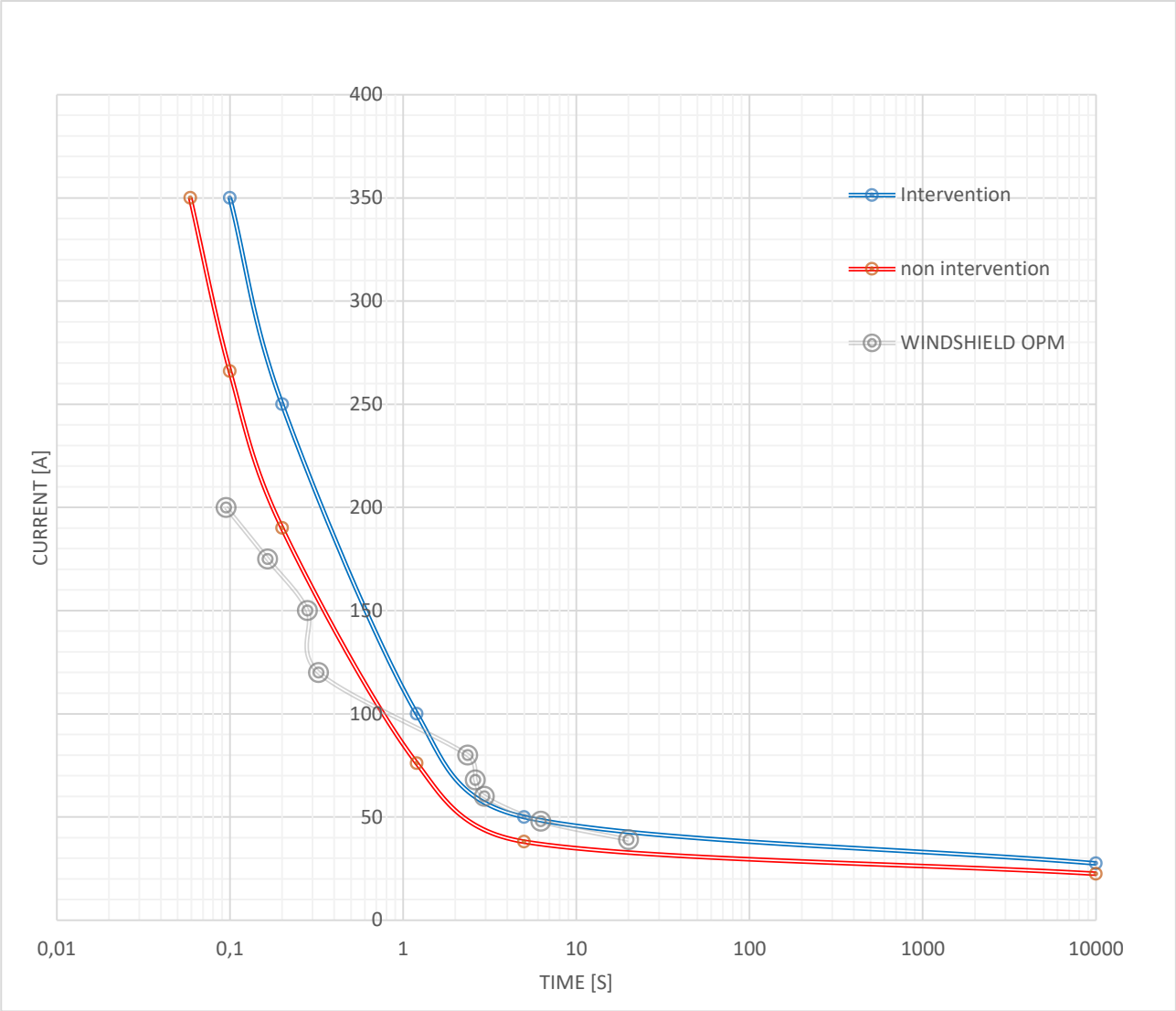



Figure 57: OVERCURRENT TRIP CURVE OF WINDSHIELD OPM

### 5.3.3 TEST PROCEDURE OF AC PDP 2

**PRE-REQUISITES:**

1. Before starting the test, ensure the EUT has passed the pre-test ATP.
2. Ensure that the EUT and all the switches are in the starting state described in §5.1.7
3. Perform test setup operations as detailed in
4. Figure 35
5. Connect terminals of AC Power Supply to the input studs E19, E20, E21
6. Set AC Power Supply to give 115V±0.5V voltage
7. Connect AC Load Bank #1 to power output studs:
   -E13, E14, E15
   -E28, E29, E30

**INITIAL OPERATIONS:**

8. Set Oscilloscope to acquire frequency coherence of phase-to-phase input and output studs
9. Set the data logger for acquiring of the system parameters defined in § 5.2.2

**TEST CORE –OVERCURRENT:**

10. Start recording parameters with the data-logger
11. Turn ON the 3 phase 115 VAC Power Supply
12. Verify that the system is ONLINE (related switch and led on test box)
13. Close K2, K8 and K61 contactors by means of test box switches
14. Set AC Load Bank in order to absorb 25A±5A for **each phase**
15. Verify current from external current sensors CS1, CS2 and CS3 (25A±5A)
16. At E13, E14, E15 studs verify that output current is 23A+/-2A
17. At E28, E29, E30 studs verify that output current is 23A+/-2A
18. Keep the rating condition and wait for thermal stabilization
19. Monitor internal temperature of the EUT and verify it is not over 85°C after thermal stabilization is reached
20. Set AC Load Bank in order to absorb 30A±5A for **each phase**
21. Verify current from external current sensors CS1, CS2 and CS3 (30A±5A)
22. Verify that the time of intervention of the OPM board follows properly the trip curve
23. Once the trip occurred, RESET the initial condition by means of test box
24. Verify that the initial steady state condition is restored
25. Repeat steps 19, 20, 21, 22 and 23 with the following load conditions:
    1) 40A±5A
    2) 50A±5A
    3) 75A±5A
    4) 100A±5A
    5) 125A±5A
    6) 150A±5A
    7) 175A±5A
    8) 200A±5A
    9) 250A±5A
    10) 300A±5A
    11) 350A±5A
26. Remove all AC Load applied at the system
27. Stop and save data-logger acquisition
28. Open all the contactors
29. Verify 0 VAC at all the studs.

**TEST CORE – UNDERFREQUENCY:**

30. Start recording the parameters with the data-logger
31. Maintain K2, K8 and K61 in closed condition by mean of test box switches

32. At E13, E14, E15 studs verify that output voltage is 115V±0.5V
33. At E28, E29, E30 studs verify that output voltage is 115V±0.5V
34. Turn ON the “Underfrequency” signal
35. Verify that K8 and K61 contactors open automatically when the signal is turned ON
36. Verify 0 V at E13, E14, E15 and E28, E29, E30
37. Turn OFF the “Underfrequency” signal
38. Verify that K8 and K61 contactors close automatically when the signal is turned OFF
39. At E13, E14, E15 studs verify that output voltage is 115V±0.5V
40. At E28, E29, E30 studs verify that output voltage is 115V±0.5V
41. Stop and save data-logger acquisition.

**TEST CORE – START 1 SIGNAL:**

42. Start recording parameters with the data-logger
43. Verify that K2, K8 and K61 contactors are in closed condition
44. At E13, E14, E15 studs verify that output voltage is 115V±0.5V
45. At E28, E29, E30 studs verify that output voltage is 115V±0.5V
46. Turn ON the “Start 1” signal
47. Verify that K8 and K61 contactors open automatically when the signal is turned on
48. Verify 0V at E13, E14, E15 and E28, E29, E30
49. Turn OFF the “Start 1” signal
50. Verify that K8 and K61 contactors close automatically when the signal is turned off
51. At E13, E14, E15 studs verify that output voltage is 115V±0.5V
52. At E28, E29, E30 studs verify that output voltage is 115V±0.5V
53. Stop and save data-logger acquisition.

**TEST CORE – START 2 SIGNAL:**

54. Start recording parameters with the data-logger
55. Verify that K2, K8 and K61 contactors are in closed condition
56. At E13, E14, E15 studs verify that output voltage is 115V±0.5V
57. At E28, E29, E30 studs verify that output voltage is 115V±0.5V
58. Turn ON the “Start 2” signal
59. Verify that K8 and K61 contactors open automatically when the signal is turned ON
60. Verify 0V at E13, E14, E15 and E28, E29, E30
61. Turn OFF the “Start 2” signal
62. Verify that K8 and K61 contactors close automatically when the signal is turned OFF
63. At E13, E14, E15 studs verify that output voltage is 115V±0.5V
64. At E28, E29, E30 studs verify that output voltage is 115V±0.5V

**FINAL OPERATIONS:**

65. Open all the contactors
66. Stop and save data-logger acquisition
67. Stop AC Power Supply
68. Remove all AC Load applied at the system

### 5.3.4 OPM BOARD TEST RESULTS FOR AC PDP 2

The graphic depicts the temperatures from starting to end of the OPM test.

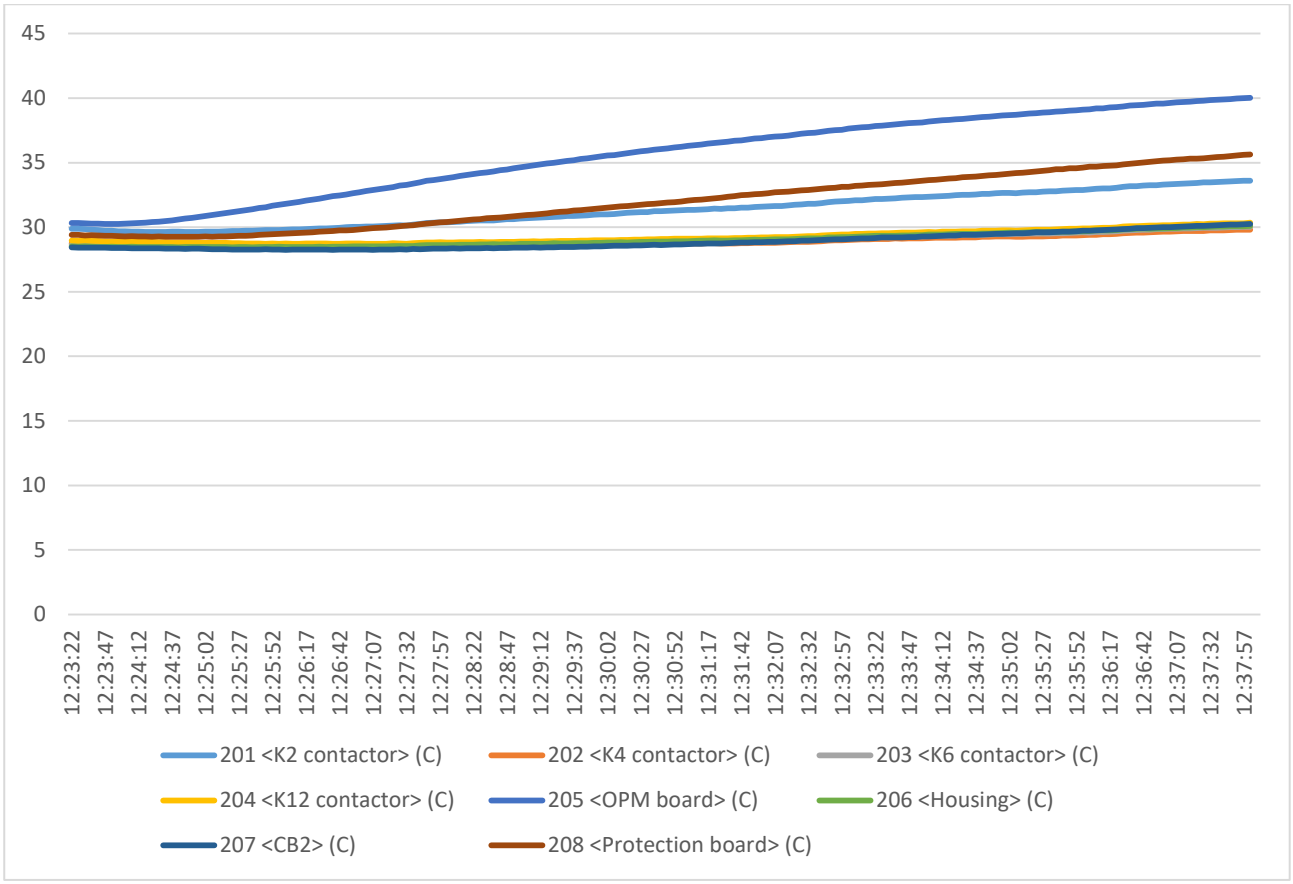



Figure 58: Temperatures recording during OPM test.

In the following tables are displayed the value recorded during the test for intervention curve.

- **LOAD 1**-Power output studs E13, E14, E15;
- **LOAD 2**- Power output studs E28, E29, E30.

NOTE():the symbol "∞" indicate the no intervention time as expected.

Table 26: Value recorded for the HEATER 2 (LOAD 1) intervention time AC PDP 2.

| TIME (ms) | I Load (Amper) |
|---|---|
| ∞ | **24.75** |
| ∞ | **29** |
| ∞ | **33** |
| ∞ | **35** |
| 18000 | **39** |
| 5500 | **48** |
| 2500 | **74** |
| 465 | **100** |
| 300 | **125** |
| 265 | **150** |
| 130 | **175** |
| 95 | **200** |
| 70 | **250** |

Table 27: Value recorded for the WINDSHIELD 2 (LOAD 2) intervention time AC PDP 2.

| TIME (ms) | II Load (Amper) |
|---|---|
| ∞ | **25.25** |
| ∞ | **31** |
| ∞ | **33** |
| ∞ | **35** |
| 20000 | **41** |
| 5600 | **49.4** |
| 2450 | **76** |
| 480 | **100** |
| 310 | **124** |
| 270 | **150** |
| 140 | **173** |
| 100 | **198** |
| 80 | **250** |

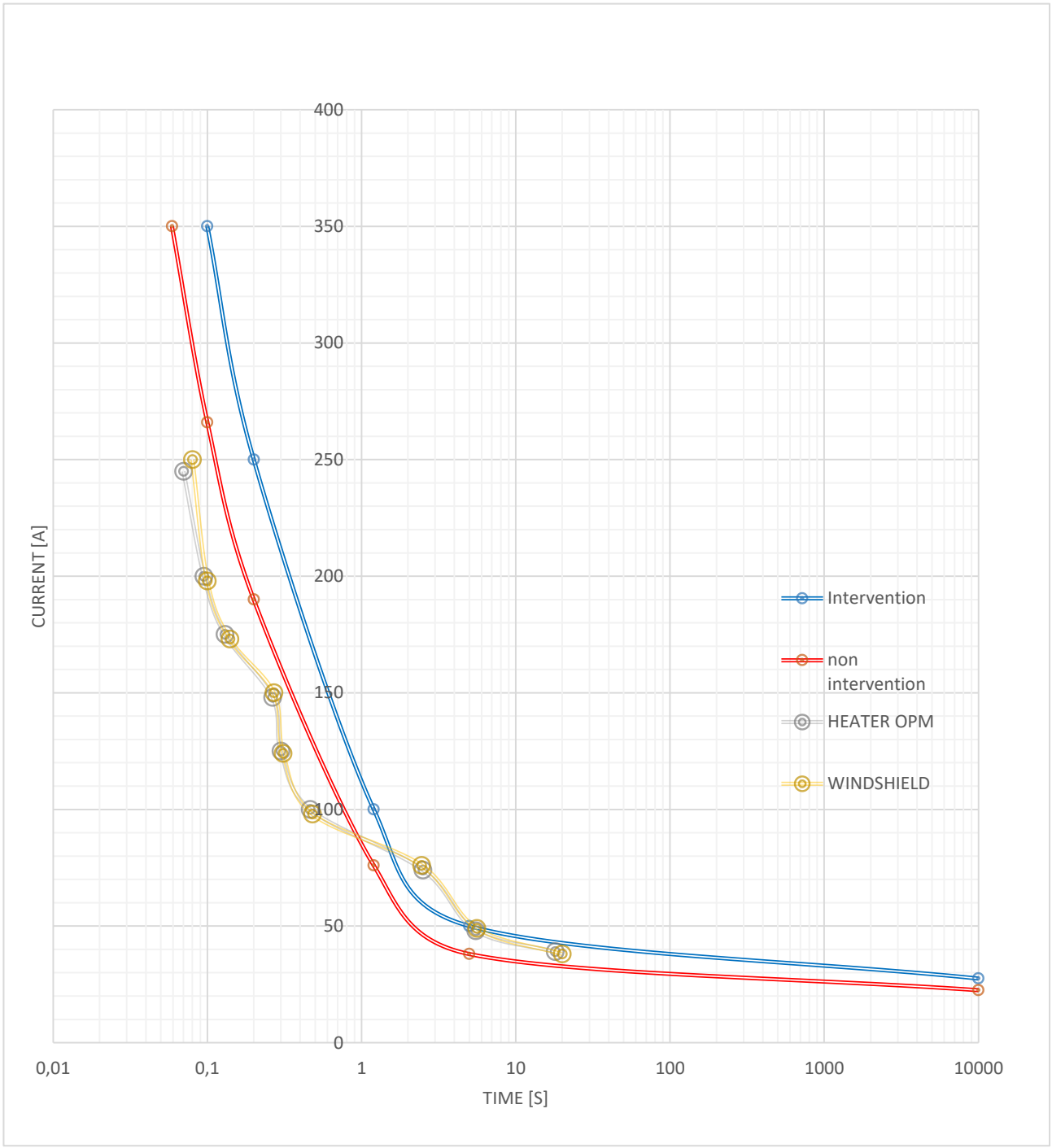



Figure 59: Overcurrent trip curve of WINDSHIELD and HEATER OPM

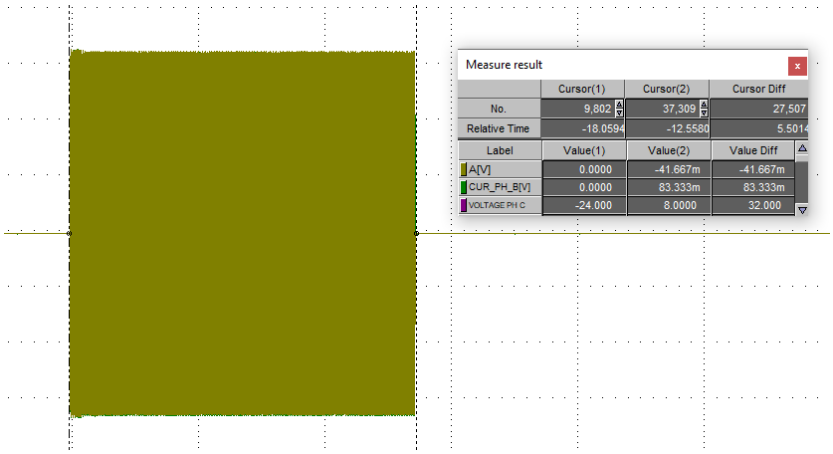



Figure 60: Load Bank is absorbing 50A (5.5 seconds)

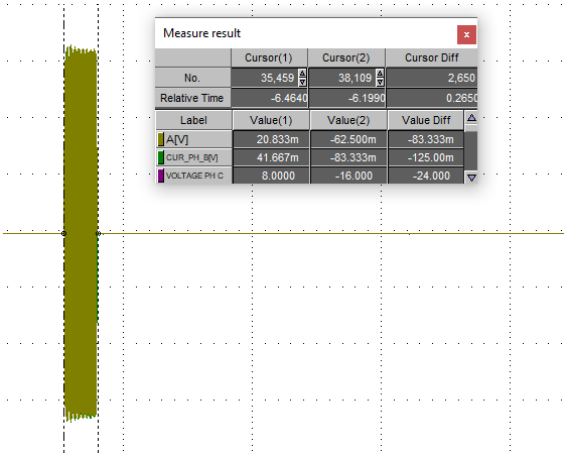



Figure 61: LOAD BANK IS ABSORBING 150A (265MILLISECONDS)

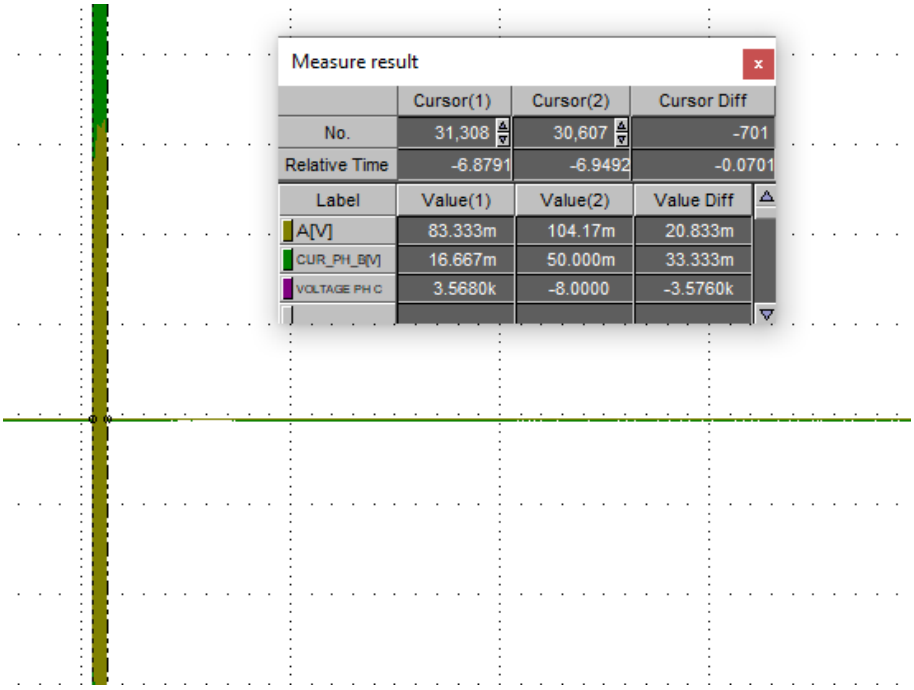



Figure 62: LOAD BANK IS ABSORBING 250 A (70MILLISECONDS)

The following graphics illustrate the changing of temperatures during Turn ON and OFF the “Underfrequency”, “Signal 1”and “Signal 2” according to the specified time.

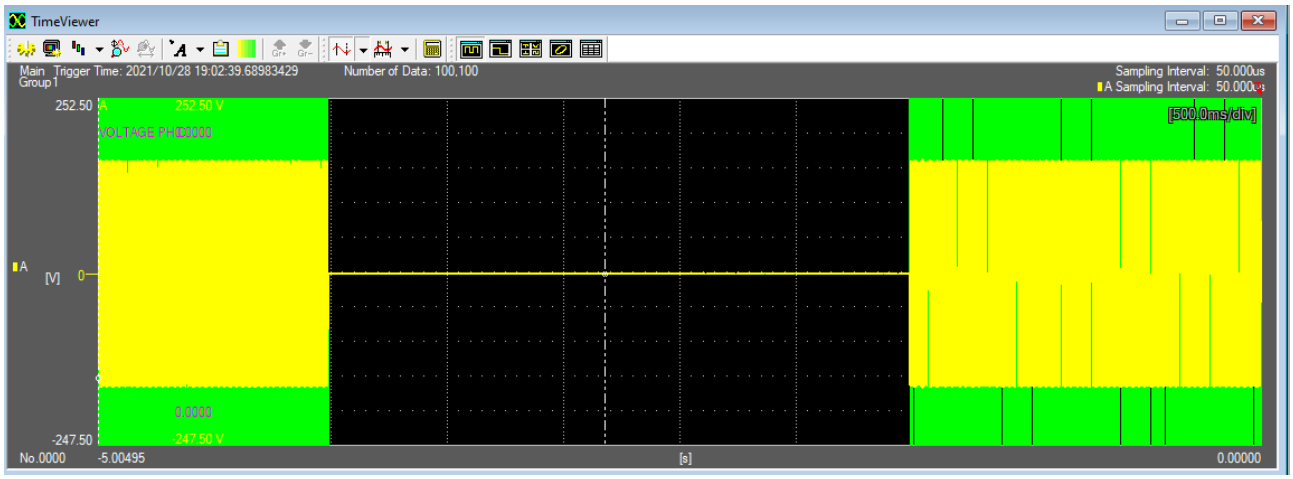



Figure 63: Turn ON and Turn OFF the “Under-frequency” signal

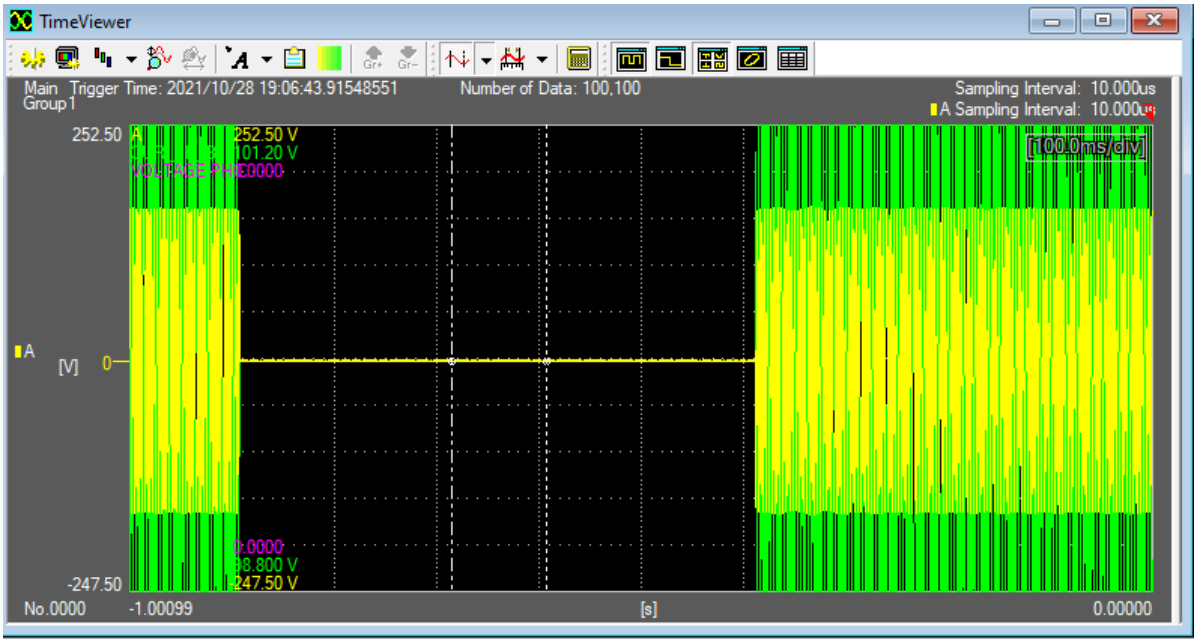



Figure 64: Turn ON and Turn OFF the “Start 1” signal

## 5.4 CONCLUSION AC EPDS

Except for the K7 relay during the overload test, no trip of the K1 main contactor with other contactor happened during the performance test on **AC PDP 1** before, during, or after the application of the rated load and overload circumstances. According to the HEATER 1 intervention failure of the relay, the reason of the failure was a manufacturing problem, especially because three other relays passed the test properly.

For all power contactors and relays, no out-of-limit temperatures were recorded before, during, or after application, and no internal component temperatures increased above the limit during the Rated condition.

During the performance test on **AC PDP2**, no trip of the K2 main contactor with other contactor occurred before, during, or after the application of the rated load and overload conditions.

No out-of-limit temperatures were recorded before, during, or after application for all power contactors and relays, and no internal component temperatures climbed over the limit during the Rated condition.

1. Before, during, and after the application of the Rated test for K2 contactor or components, no damage, trip, or bad condition was verified.
2. No damage, trip, or bad condition was verified before, during, or after the K8 contractor or component's Rated load test was applied.
3. No damage, trip, or bad condition was verified before, during, or after the K61 contractor or component's Rated load test was applied.
4. There were no bad condition during or after the Overload conditions were applied to line contactor K2 with K8 and K61.

Then the load current steps from 25A to 250A were completed to ensure that the OPM intervention was completed **in the time frame expected**. During the operation, no errors were identified.

The results of applying “Under-frequency” test approves that K8 and K61 contactors open automatically when the signal is turned on and vice versa.

The K8 and K61 contactors open and close automatically when the Signals are turned on and off, as evidenced by the results of the Start 1 and Start 2 tests.

As a result, the performance test of AC PDP 2 components and characteristics is **PASSED** the test.

## 5.5 DC PDP 1 AND DC PDP 2 PERFORMANCE TEST

This Test Report contains the results of the tests carried out in order to reach SOF qualification performance level of the DC PDP 1 and DC PDP 2 for EPDS of X military Helicopter.

Table 28: Test results for vibration and acceleration tests on DC PDP 2.

| Test Type | Test Result (PASS/FAIL) |
|---|---|
| Rated State- Contactors control and power distribution | PASS |
| Continuous Capacity | PASS |
| Short circuit capacity | PASS |
| Overload condition | PASS |
| FIL Logic board | PASS |

### 5.5.1 TEST CONDITIONS

All measurements and tests were performed at ambient conditions stated in the following:
Temperature: +15°C ÷ +35°C
Relative Humidity: 20% ÷ 85%
Atmosphere Pressure: 84kPa ÷ 107kPa

### 5.5.2 THERMAL STABILIZATION

Items are considered thermally stabilized when the temperatures of all their instrumented parts change no more than ±1°C in 5 minutes.

### 5.5.3 TEST INSTRUMENTATION AND ACCURACY

The following instrumentation in Table 29 was utilized to carry out the tests specified in this QTR document:

Table 29: Instrumentation for the qualification tests.

| Description | Model | Supplier | Range | Instrument Accuracy | Parameter Measured | Calibration expire date |
|---|---|---|---|---|---|---|
| Oscilloscope | DL 850 | Yokogawa | 850/250V peak 0.04/2MHz | 1.5% | Voltage waveforms | 09/2022 |
| Meteo station | HM 30 | Thommen | -40 to +60°C | ±0.3°C | Ambient Temp. | 11/2022 |
| | | | 0 to 100% RH | ±1.5% RH | Ambient Humidity | |
| Data logger | 34970A | Agilent | 100Vdc input | 0.005% FS max | DC Voltage/ sensor outputs | 08/2022 |
| | | | 100Vac input | 0.17% FS on rms | AC Voltage rms | |
| | | | -100÷400°C | 1°C | Temperature | |
| Multimeter (6.5 digit) | DMM4040 | TEKTRONIX | 1000Vdc | 0.0026% FS max | Voltage | 06/2022 |
| | | | 3Adc | 0.07% FS max | Current | |
| | | | 100MΩ | 0.31% FS max | Resistance | |
| Microohmeter | CA6240 | CHAUVIN ARNOUX | 0 to 100 MΩ | 5 % | Insulation resistance | 01/2023 |
| Dielectric strength tester | M005 | HIPOT IIII | 0 to 3 kV Ileakage = 20 mA | 5 % | Dielectric strength | 12/2022 |

### 5.5.4 TEST EQUIPMENT

The following instrumentation (depicting Table 30) was used to carry out the tests detailed in this document:

Table 30: Equipment for the qualification tests.

| Description | Manufacturer | Model or Part Number | Serial Number |
|---|---|---|---|
| General Purpose 28VDC power supply | Elektro-Automatik | PS 2048-10 B | MM009 |
| DC Load Bank | Magneti Marelli | G27LDC | 0001 |
| ATP Test Box | ASE S.p.A. | DB16UC-DC/1<br>DB16UC-DC/3 | N.A. |
| Interface harness | ASE S.p.A. | DB23W<br>DB24W | N.A. |

DC PDP 1 and DC PDP 2 which are tested with same Boxes during environmental tests since required control inputs and output signals are the same for both. In following table part numbers of Quality Test Box is reported.

Table 31: Part number of Qualification Test Box.

| EUT | QTB |
|---|---|
| DC PDP 1<br>DC PDP 2 | DB16UC-DC/1 |

### 5.5.5 EUT STARTING STATE

Table *32* presents the EUT's beginning condition (Initial Condition), where all power contactors and relays must be de-energized.

The initial condition has been verified by the console of the DC Test Benches, and the LED ON LINE is turned off. This condition must be checked at the end of all performance tests before proceeding to the next. Before beginning any functional test, ensure that all switches in the Control Console are in the down position.

Table 32: Power Distribution Initial Condition

| Item Description | Condition |
|---|---|
| DC PDP 1 | ON LINE OFF |
| DC PDP 2 | ON LINE OFF |

NOTE: led ON LINE is the general synoptic light signal of the Control Console and it gives information about state of the Control Console.

### 5.5.6 GENERAL TOLERANCES

Unless otherwise indicated during the test procedures, the maximum permissible tolerance for the test conditions (i.e. imposed test parameter) were listed below:

| | | |
|---|---|---|
| Environmental | Temperature | ± 3°C |
| | Altitude | ± 5% of the specified pressure |
| | Speed | ± 50rpm |

| | | | |
|---|---|---|---|
| Mechanical | **Sinusoidal Vibration**: | Acceleration | ±10% |
| | | Frequency | ±2% |
| | **Random Vibration**: | PSD value below 500Hz | +3dB; -1.5dB |
| | | PSD value 500Hz÷2000Hz | +3dB; -3dB |
| | | Overall g rms value | +20%; -5% |

| | | |
|---|---|---|
| Electrical | Force | ± 2% |
| | Voltage | ± 1V |
| | Current | ± 2A |
| | Frequency | ± 2Hz |
| | Power | ± 5% |

### 5.5.7 TEST SETUP

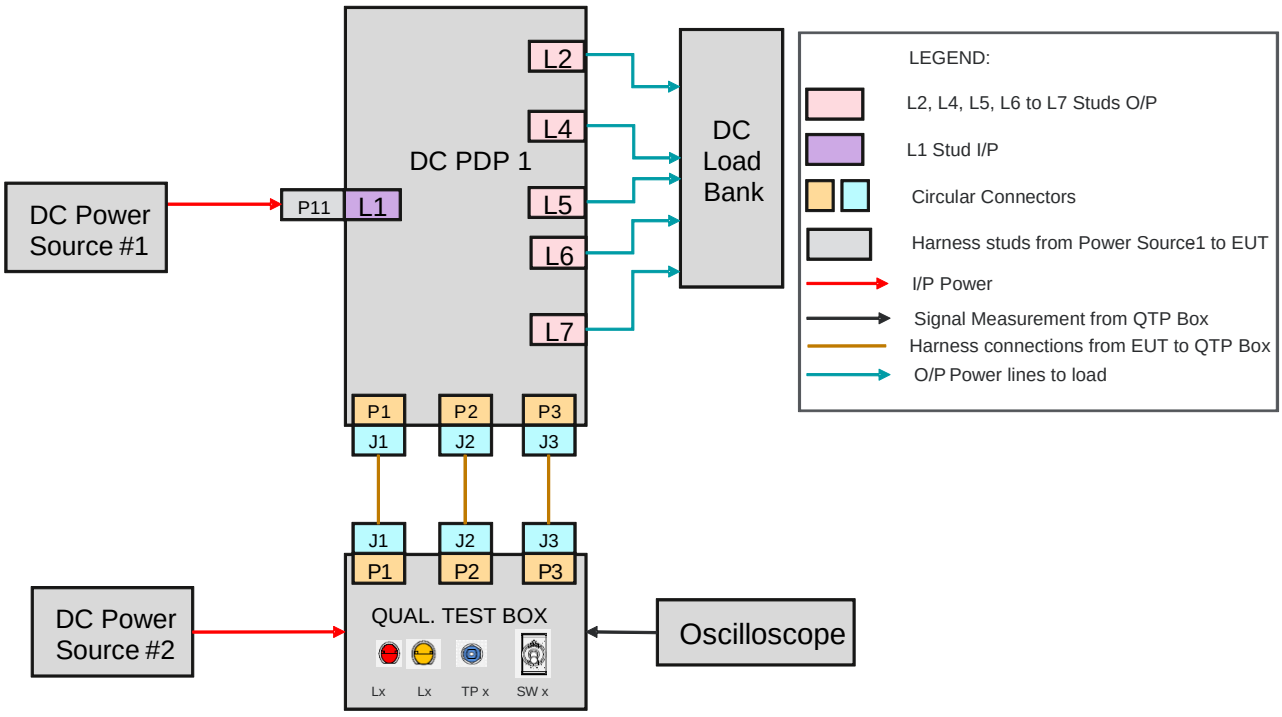



Figure 65: Test setup for performance of DC PDP 1.

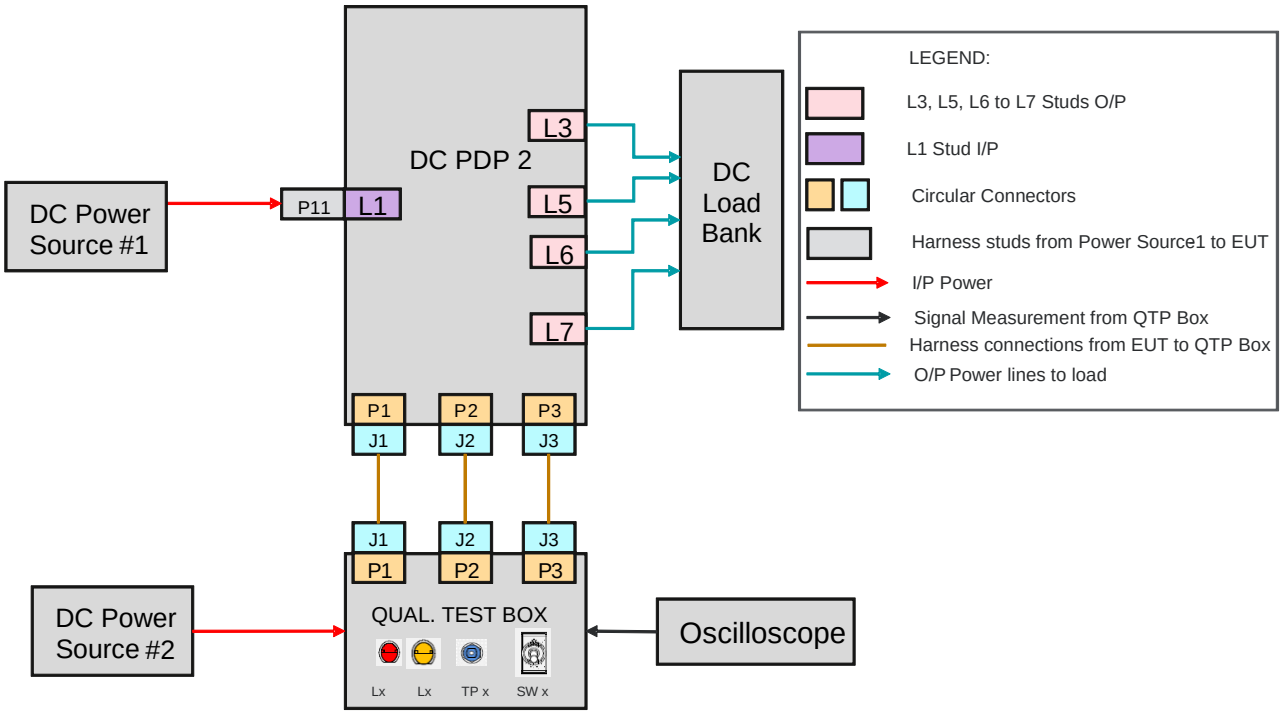



Figure 66: Test setup for performance of DC PDP 2.

### 5.5.8 TEST SEQUENCE

Tests are planned to be carried out according to the below sequence. The only constraint is about the first and the last step (pre-test and post-test ATPs).

**Initial:**

1. Pre-test ATP on EUT

**Functional Tests:**

1. Performance test on EUT set as per DC PDP 2 and set as per DC PDP 1.

**Final:**

1. Post-test ATP

↓↓↓

**"SOF Test on the DC EPDS" session was a successful.**

### 5.5.9 PERFORMANCE TEST ON DC PDP 1 AND DC PDP 2

The test carried out in the following sub-steps:

5. Rated load – Contactors control and power distribution
6. Rated load – Continuous capacity
7. Short circuit capacity
8. Overload condition
9. FIL logic board

### 5.5.10 TEST SETUP DETAILS

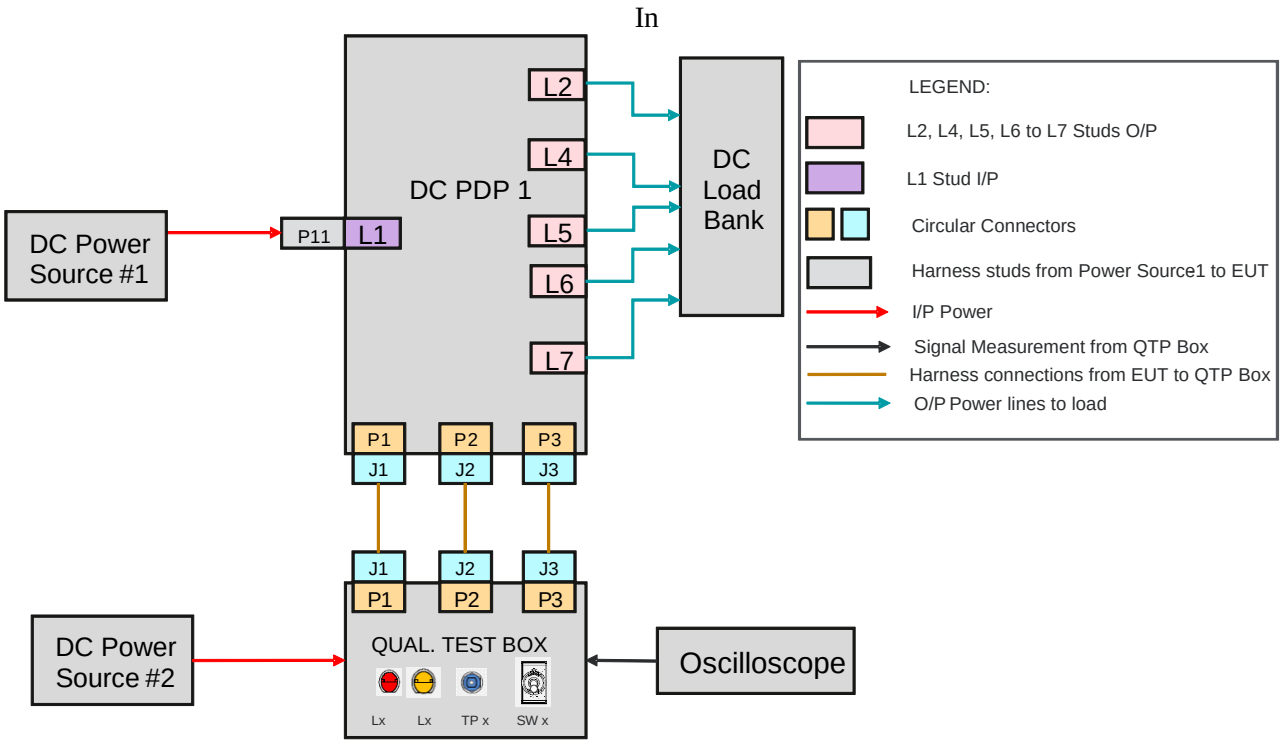


Figure 65and

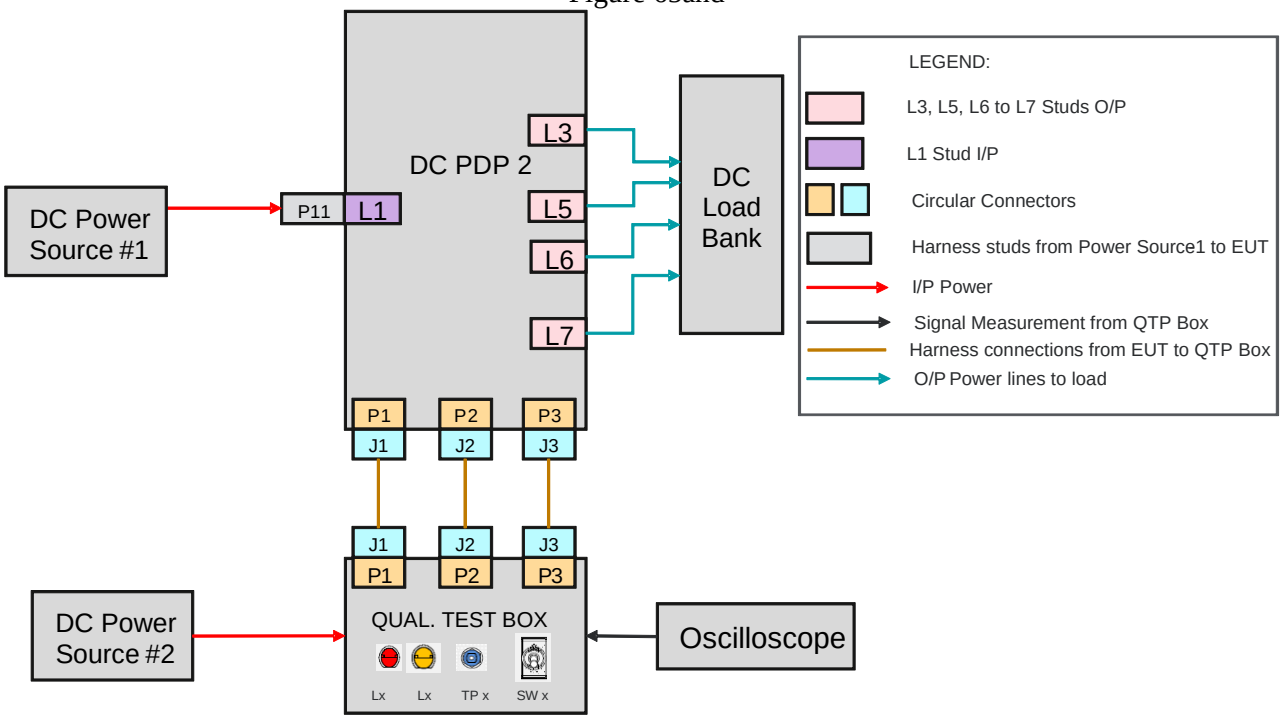



Figure 66 the test setup for DC PDP 1 and DC PDP 2, alternatively, is depicted. The instrument and equipment of Table 29 and Table 30 are used and an oscilloscope as measuring instrument is chosen to record the following parameters:

1. Voltage input
2. Current output
3. Voltage output
4. Time of act of contactors
5. Temperature.

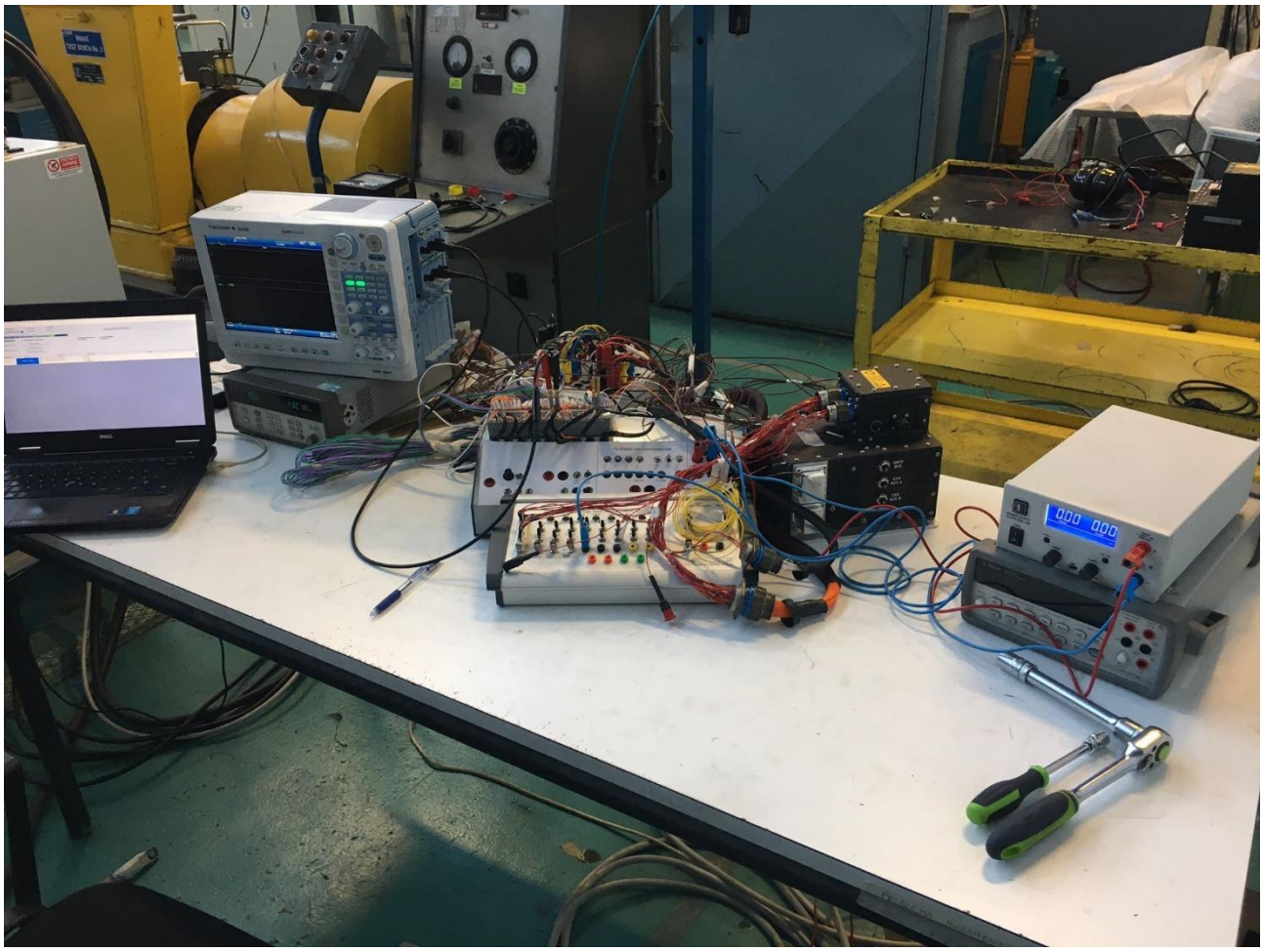


Figure 67: Performance Test setup for DC PDP

All electrical interfaces and connector functions are described in order to simplify cable and connection configuration in the tables below.

Table 33: Connections and electrical interfaces in DC PDP 1.

| Stud | I/O | Function | Current | Power/Signal |
|---|---|---|---|---|
| L1 | I | TRU 1 Power IN | 300A nominal | POWER |
| L2 | I/O | BUS TIE to DC PDP 2 | 150A nominal | POWER |
| L3 | O | Supply to SPDU – MAIN BUS 3 | 70A max | POWER |
| L4 | O | EMERGENCY BUS 1 | 100A nominal | POWER |
| L5 | O | Supply to SPDU – MAIN BUS 1 | 70A max | POWER |
| L6 | O | Supply to SPDU – ESS BUS 1A | 70A max | POWER |
| L7 | O | Supply to SPDU – ESS BUS 1B | 70A max | POWER |

Table 34: J1, J2 and J3 connectors of DC PDP 1.

| Connector | Part Number | Function |
|---|---|---|
| J1 | D38999/20WA98SN (socket contact) (MIL-C-38999) | Power supply for SGCU 1 |
| J2 | D38999/20WD97PN (pin contact) (MIL-C-38999) | Signal connector 4pin / AWG #16 |

| | | |
|---|---|---|
| | | 8pin / AWG #20 |
| J3 | D38999/20WG35PN (pin contact) (MIL-C-38999) | Signal connector<br>79pin / AWG #22 |

Table 35: Connections and electrical interfaces in DC PDP 2.

| Stud | I/O | Function | Current | Power/Signal |
|---|---|---|---|---|
| L1 | I | TRU 2 Power IN | 300A nominal | POWER |
| L2 | I/O | BUS TIE to DC PDP 1 and<br>supply to SPDU – MAIN BUS 4 | 150A nominal | POWER |
| L3 | I/O | BUS TIE to BATTERY PDP | 150A nominal | POWER |
| L4 | O | EMERGENCY BUS 2 | 100A nominal | POWER |
| L5 | O | Supply to SPDU – MAIN BUS 2 | 70A max | POWER |
| L6 | O | Supply to SPDU – ESS BUS 2A | 70A max | POWER |
| L7 | O | Supply to SPDU – ESS BUS 2B | 70A max | POWER |

Table 36: J1, J2 and J3 connectors of DC PDP 2.

| Connector | Part Number | Function |
|---|---|---|
| J1 | D38999/20WA98SN (socket contact) (MIL-C-38999) | Power supply for SGCU 2 |
| J2 | D38999/20WD97PN (pin contact) (MIL-C-38999) | Signal connector<br>4pin / AWG #16<br>8pin / AWG #20 |
| J3 | D38999/20WG35PN (pin contact) (MIL-C-38999) | Signal connector<br>79pin / AWG #22 |

### 5.5.11 OPERATION – RATED LOAD AND OVERLOAD TESTS

The main objectives of the two sub-tests are:

**Contactor controls and power distribution**: verify that contactors close when the external signal is sent from the Qualification Test Box and all the closure conditions are “true”. The bus voltage will also be verified at the load box connected at the studs of the PDP.

**Continuous capacity**: verify that the PDP is able to give required continuous output currents, keeping the minimum output voltages required under each load condition. The test will be carried out at the worst load required in normal operation and for the failure modes of operation of DC PDP 1 and for DC PDP 2 under specific conditions.

**Overload**: verify if the load current at the studs exceeds the short circuit or overload current drawn (>100A). When the load current connected at the stud (L4) falls in anyone category, the RCCB inside the PDP will sense and control the load by disconnecting it. So main contactor shall be verified to be opened and bus voltage to be disconnected at the stud (L4).

Also, the system will verify if the overload conditions (fault) of the current drawn at the any stud (L5 to L7) is more than the rated current of the circuit breakers (CB). So CB shall be verified to be opened when the fault condition is reached.

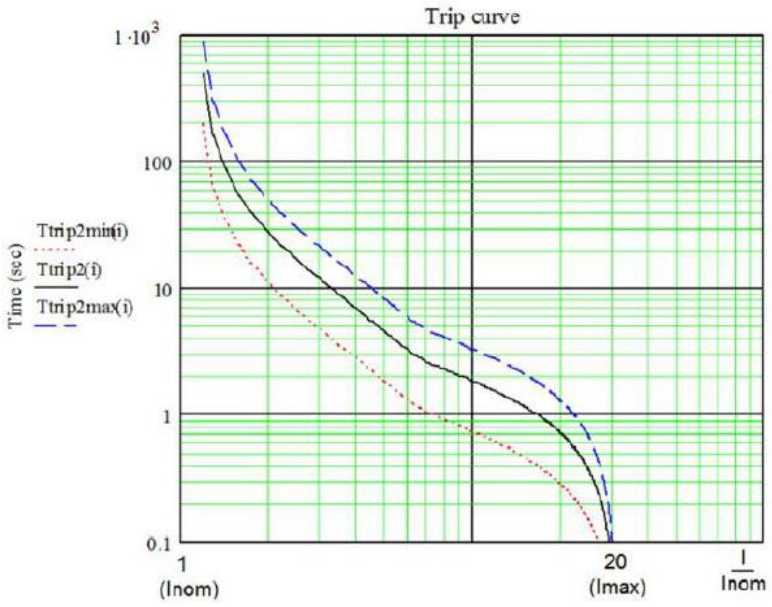



Figure 68: RCCB1 (DC PDP 1) and RCCB2 (DC PDP 2) trip curve.

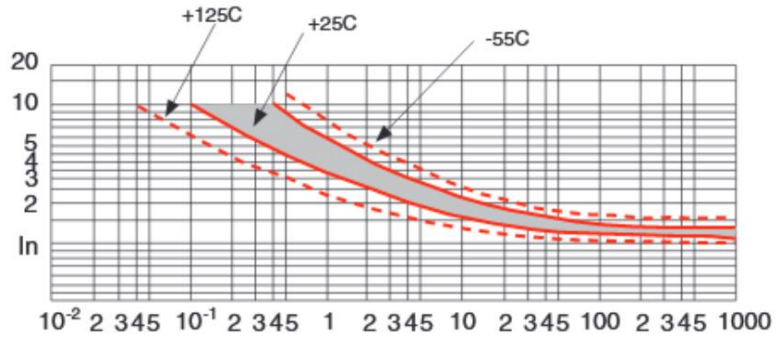
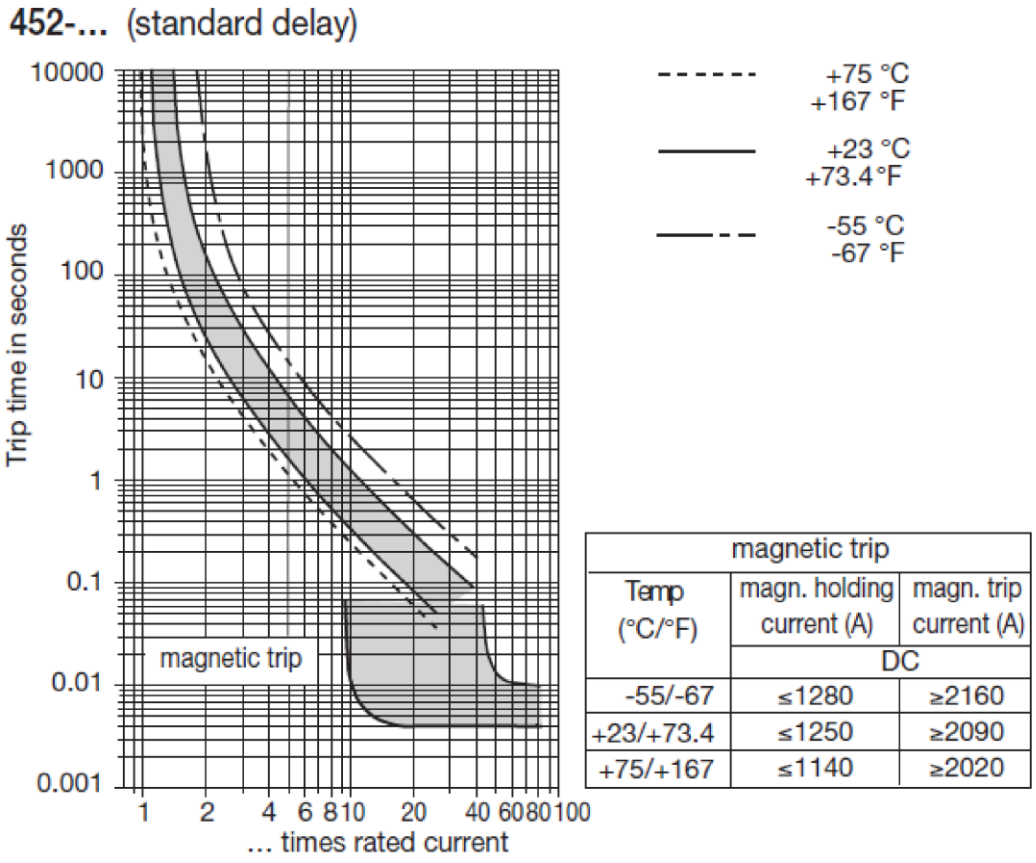



Figure 69: 7.5A-circuit-breaker trip curve.




| magnetic trip | | |
|---|---|---|
| Temp (°C/°F) | magn. holding current (A) | magn. trip current (A) |
| | DC | |
| -55/-67 | ≤1280 | ≥2160 |
| +23/+73.4 | ≤1250 | ≥2090 |
| +75/+167 | ≤1140 | ≥2020 |

Figure 70: 70A-circuit-breakers trip curve.

## 5.6 FIL LOGIC BOARD TEST

In the DC PDP 1 and in the DC PDP 2 the Fault Isolation Logic board provides the following functions:

1. Manage of input commands
2. Provide output signals
3. Provide fuse monitoring (only FIL board of DC PDP 2)
4. Provide fault isolation sequence when an overcurrent is sensed by main current sensors inside the PDP

The aim of the test is to verify that the FIL board works correctly by applying to the EUT the resistive load required to trigger the protections.

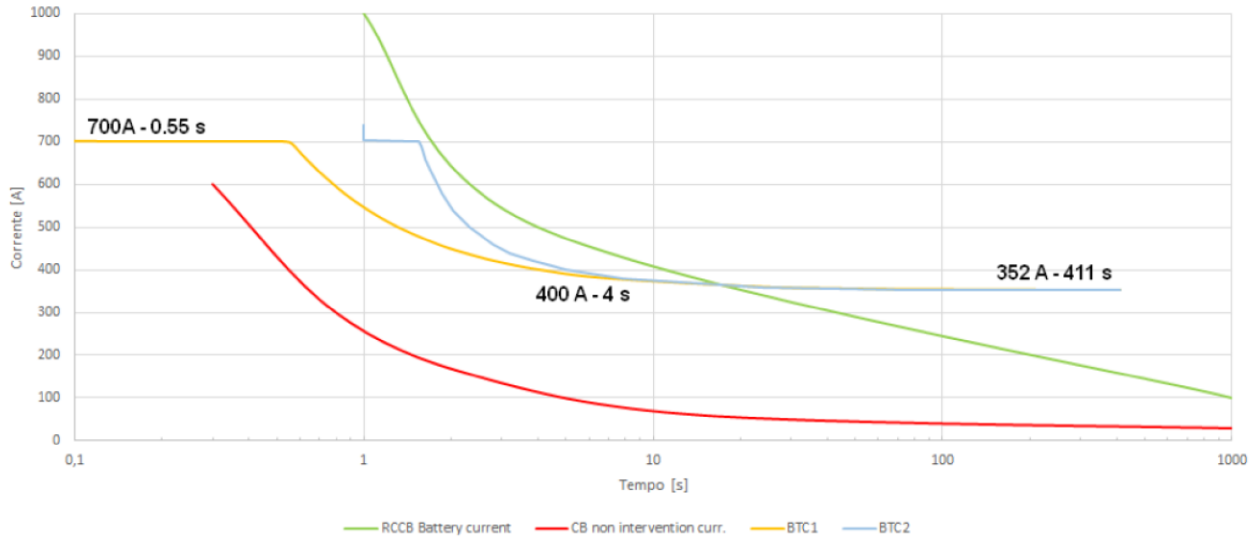



Figure 71: Overcurrent trip curves for bus tie contactor (BTC1-K7 (DC PDP 1) and BTC2-K6 (DC PDP 2)).

## 5.7 FUNCTIONAL TEST RESULTS FOR DC PDP

### 5.7.1 RATED LOAD AND OVERLOAD TEST RESULTS

The aim of the test is to ensure that the external power contactor closes when the external signal from the Qualification Test Box is provided, and that all of the closure conditions are "true". The bus voltage will also be verified at the load box, which will be connected to the studs of PDP.

EUT has been set as DC PDP 2 for this test because as per test procedures (in appendix part) this is the worst condition, with the maximum applied load (183.6A±5A against 133.9A±5A).
Following figure illustrates temperature changes during contactors control and power distribution test.

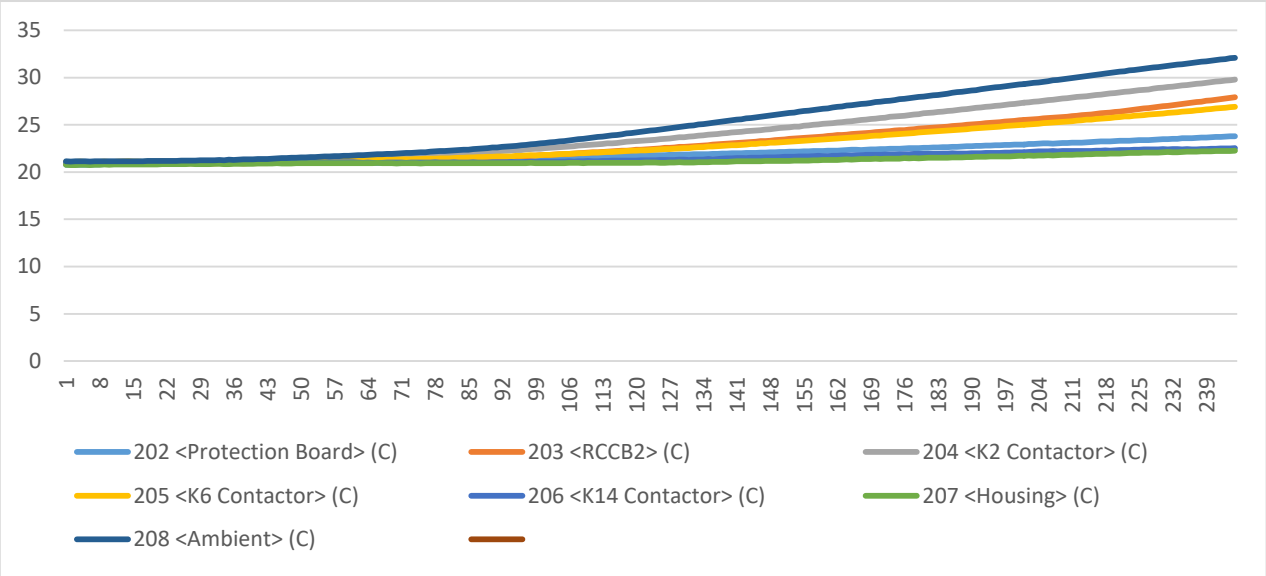



Figure 72: Thermocouples readings during contactors control and power distribution.

The table below depicts the recorded current and voltage values during the contactor control and power distribution test.

The continuous capacity test ensures that the system can supply the needed continuous output currents while preserving the minimal output voltages under previous load conditions (Total DC load 174 A). The rating condition is maintained for more than 15 minutes.

Table 37: Measured currents during continuous capacity.

| Time | L1 Current | L3 Current | L4 Current | L5 Current | L6 Current | L7 Current |
|---|---|---|---|---|---|---|
| **17:31:11:327** | 0,08358 | 0,0066 | 0,000484 | 0,00374 | 0,00187 | 0,0066 |
| **17:46:26:311** | 174,4127 | 26,27233 | 19,65688 | 64,88855 | 40,81881 | 23,30591 |
| **17:46:29:311** | 174,3995 | 26,27233 | 19,65697 | 64,90043 | 40,81551 | 23,30635 |
| **17:46:32:311** | 174,4017 | 26,27057 | 19,65675 | 64,89559 | 40,8143 | 23,30899 |
| **17:46:35:311** | 174,3973 | 26,27365 | 19,65583 | 64,88415 | 40,81199 | 23,30415 |
| **17:46:38:311** | 174,3973 | 26,27057 | 19,65609 | 64,87337 | 40,81342 | 23,30415 |
| **17:46:41:311** | 174,3775 | 26,26881 | 19,65688 | 64,87491 | 40,811 | 23,30679 |
| **17:46:44:311** | 174,3797 | 26,26837 | 19,65627 | 64,87117 | 40,80803 | 23,30063 |
| **17:46:47:311** | 174,3445 | 26,26529 | 19,6553 | 64,87337 | 40,80517 | 23,30107 |
| **17:46:50:311** | 174,3533 | 26,27057 | 19,65613 | 64,87909 | 40,80506 | 23,30151 |
| **17:46:53:311** | 174,3445 | 26,26881 | 19,65653 | 64,85842 | 40,80407 | 23,30459 |

According to the recorded values during the maintained rating condition for more than 15 minutes, the DC Load Bank absorbs 174A as total and the distribution owing to output studs is as follows:

- $L_3$=26.3A
- $L_4$=19.7A
- $L_5$=64.8A
- $L_6$=40.8A
- $L_7$=23.3A

Table 38: Measured voltages during continuous capacity.

| Time | L1 Voltage | L3 Voltage | L4 Voltage | L5 Voltage | L6 Voltage | L7 Voltage |
|---|---|---|---|---|---|---|
| **17:31:11:327** | 28,5764 | 28,57706 | 28,45442 | 28,57618 | 28,57651 | 28,57618 |
| **17:46:26:311** | 27,88837 | 27,85641 | 27,26315 | 27,73344 | 27,77333 | 27,8054 |
| **17:46:29:311** | 27,88771 | 27,85719 | 27,2637 | 27,73289 | 27,77333 | 27,80551 |
| **17:46:32:311** | 27,88782 | 27,85542 | 27,2637 | 27,7341 | 27,77234 | 27,80672 |
| **17:46:35:311** | 27,88837 | 27,85553 | 27,26315 | 27,73267 | 27,7719 | 27,80595 |
| **17:46:38:311** | 27,88683 | 27,85619 | 27,26249 | 27,73399 | 27,77201 | 27,80562 |
| **17:46:41:311** | 27,88683 | 27,85509 | 27,26271 | 27,73278 | 27,77278 | 27,80452 |
| **17:46:44:311** | 27,88672 | 27,85586 | 27,26359 | 27,73289 | 27,77234 | 27,80562 |
| **17:46:47:311** | 27,88782 | 27,85498 | 27,26249 | 27,73377 | 27,77168 | 27,80551 |
| **17:46:50:311** | 27,88815 | 27,8563 | 27,26204 | 27,73377 | 27,77245 | 27,8054 |
| **17:46:53:311** | 27,88628 | 27,85586 | 27,26171 | 27,73234 | 27,77212 | 27,80496 |

After thermal stabilization, the EUT has been kept in DC PDP 2 configuration because it is again the worst condition and the DC Load Bank is adjusted to a load of 213,9A, and this overload condition is maintained for 5 minutes. The DC Load Bank absorbs 213,9 A as a total, according to the recorded values during the maintained initial overload condition for approximately 5 minutes, and the distribution due to output studs is as follows:

- $L_3$=37.5A
- $L_4$=19.5A
- $L_5$=64.6A
- $L_6$=45.8A
- $L_7$=46.7A

Table 39: Measured currents during overload condition

| Time | L1 Current | L3 Current | L4 Current | L5 Current | L6 Current | L7 Current |
|---|---|---|---|---|---|---|
| **18:18:50:322** | 0,20236 | 0,00924 | 0,001892 | 0,00066 | 0,00154 | 0,00528 |
| **18:23:50:306** | 213,9752 | 37,55025 | 19,4828 | 64,63911 | 45,82528 | 46,76141 |
| **18:24:14:306** | 213,6849 | 37,51242 | 19,48197 | 64,59446 | 45,79173 | 46,61755 |
| **18:24:50:306** | 213,3505 | 37,4517 | 19,48166 | 64,53639 | 45,75566 | 46,43498 |
| **18:25:14:306** | 213,1591 | 37,41079 | 19,48016 | 64,50076 | 45,72871 | 46,32676 |
| **18:25:50:306** | 212,8754 | 37,36856 | 19,47893 | 64,45721 | 45,6966 | 46,18115 |
| **18:26:14:306** | 212,7148 | 37,33204 | 19,47713 | 64,42465 | 45,67548 | 46,09448 |
| **18:26:50:306** | 212,4773 | 37,28761 | 19,47581 | 64,38682 | 45,64722 | 45,97438 |
| **18:27:14:306** | 212,3453 | 37,26738 | 19,47515 | 64,36438 | 45,63281 | 45,91015 |
| **18:27:50:306** | 212,1935 | 37,23746 | 19,47449 | 64,33755 | 45,61147 | 45,81468 |
| **18:28:14:306** | 212,0813 | 37,21986 | 19,47379 | 64,31863 | 45,5975 | 45,75354 |
| **18:28:32:306** | 211,9955 | 37,19919 | 19,47462 | 64,31093 | 45,58563 | 45,71482 |

Table 40: Measured voltages during overload condition.

| Time | L1 Voltage | L3 Voltage | L4 Voltage | L5 Voltage | L6 Voltage | L7 Voltage |
|---|---|---|---|---|---|---|
| **18:18:50:322** | 28,58797 | 28,58797 | 28,5061 | 28,58764 | 28,58786 | 28,58797 |

| | | | | | | |
|---|---|---|---|---|---|---|
| **18:23:50:306** | 27,70083 | 27,65675 | 27,0788 | 27,54447 | 27,56639 | 27,5665 |
| **18:24:14:306** | 27,69862 | 27,65598 | 27,07825 | 27,54314 | 27,56529 | 27,56551 |
| **18:24:50:306** | 27,69796 | 27,65477 | 27,07703 | 27,54292 | 27,56364 | 27,56518 |
| **18:25:14:306** | 27,6962 | 27,654 | 27,07571 | 27,54226 | 27,56298 | 27,56375 |
| **18:25:50:306** | 27,69554 | 27,65212 | 27,07483 | 27,53984 | 27,56155 | 27,56221 |
| **18:26:14:306** | 27,69289 | 27,64915 | 27,07186 | 27,53796 | 27,55846 | 27,55945 |
| **18:26:50:306** | 27,69091 | 27,64749 | 27,07053 | 27,5351 | 27,55648 | 27,55736 |
| **18:27:14:306** | 27,69014 | 27,64727 | 27,06965 | 27,53499 | 27,55615 | 27,55681 |
| **18:27:50:306** | 27,68893 | 27,64617 | 27,06877 | 27,53422 | 27,55482 | 27,55615 |
| **18:28:14:306** | 27,68871 | 27,64562 | 27,06866 | 27,53301 | 27,55482 | 27,55438 |
| **18:28:32:306** | 27,68738 | 27,64628 | 27,06833 | 27,5329 | 27,55449 | 27,55493 |

Temperature values were recorded from thermocouples during overload condition.

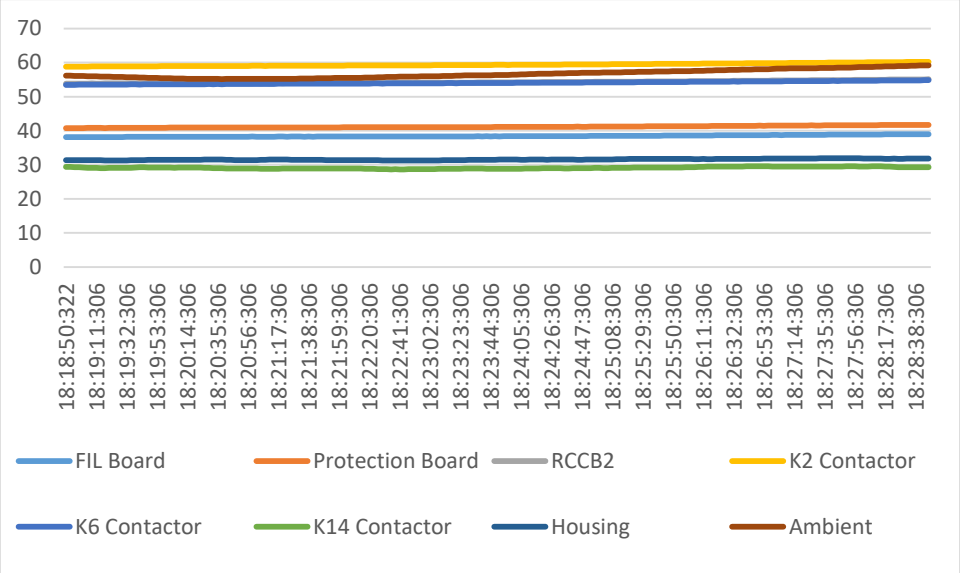



Figure 73: Temperature values during overload condition

DC load Bank is adjusted to absorb 280A current, this value is verified by internal current sensor. This second overload condition is applied 5 seconds, circuit breaker is triggered in the appropriate intervention time - 44milliseconds according to following curve described in Figure 70.

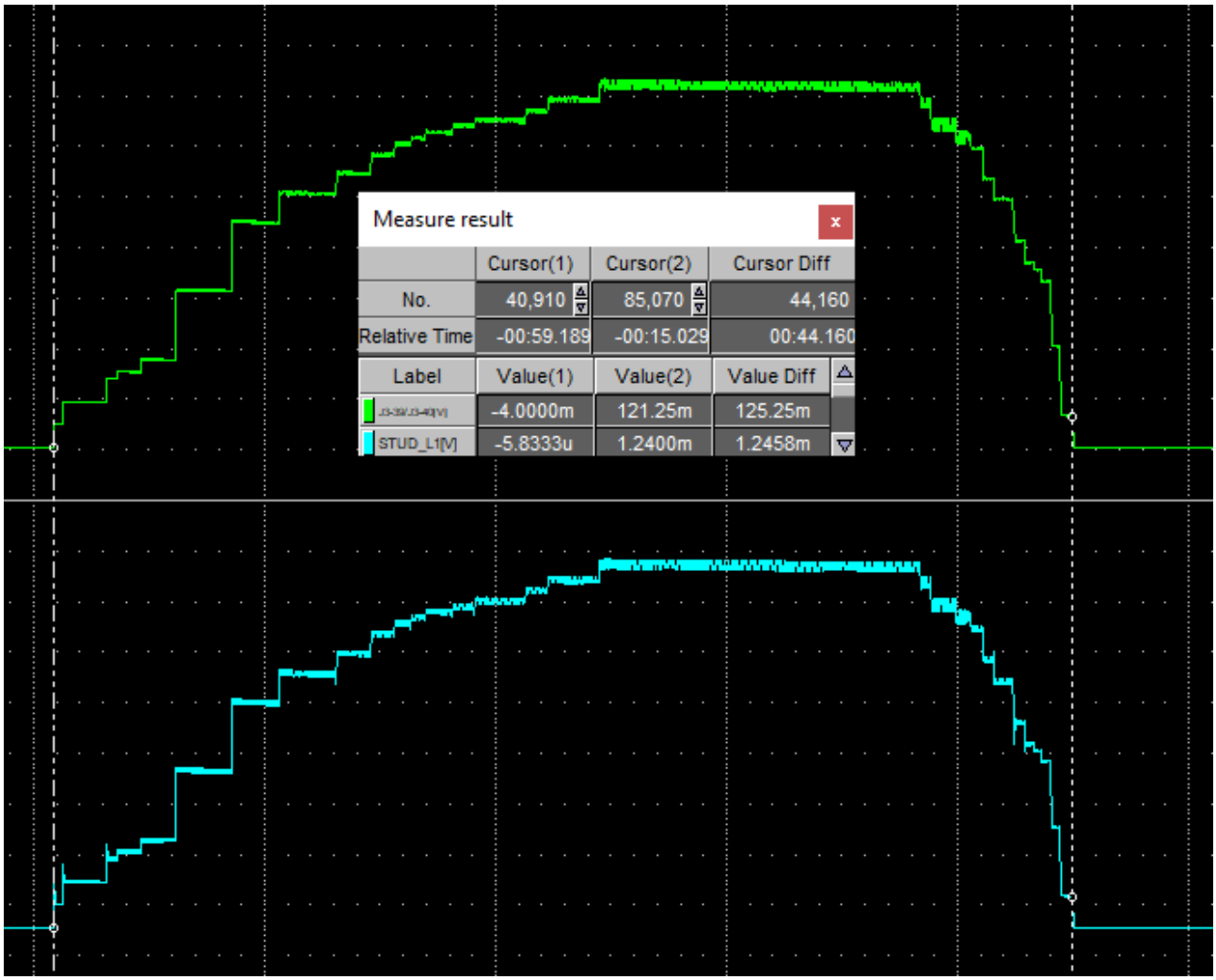



Figure 74: Intervention time of 280A overload test.

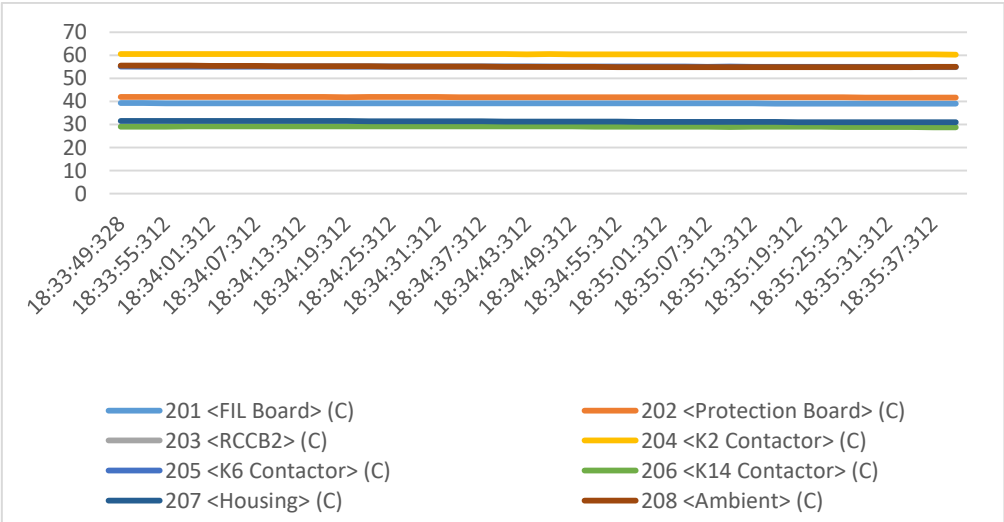



Figure 75: Temperature recordings during 280A overload test

## 5.8 FIL LOGIC BOARD TEST RESULTS

Table 41: Error identification

| | Steps | PIN ID1 | PIN ID2 | SIDE | ID ERROR |
|---|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| 12 and 13 | GROUND | OPEN | SIDE 1 | GROUND |
| 14 and 15 | OPEN | GROUND | SIDE 2 | GROUND |
| 16 and 17 | OPEN | OPEN | ID ERROR | OPEN |
| 18 and 19 | GROUND | GROUND | ID ERROR | OPEN |
| 20 and 21 | OPEN | GROUND | SIDE 2 | GROUND |

Table 42: Contactor drivers – K6 Status

| STEPS | DC EXT PWR | APU | AC EXT PWR | EMR BUS CONTACTOR | OVERRIDE | K6 STATUS |
|---|---|---|---|---|---|---|
| **23 & 24** | GROUND | OPEN | OPEN | OPEN | OPEN | CLOSED |
| **25 &26** | GROUND | OPEN | OPEN | OPEN | GROUND | OPEN |
| **27 & 28** | OPEN | GND | OPEN | OPEN | OPEN | CLOSED |
| **29 & 30** | OPEN | OPEN | GND | OPEN | OPEN | CLOSED |
| **31 & 32** | OPEN | OPEN | OPEN | GND | OPEN | CLOSED |
| **33 & 34** | GND | GND | GND | GND | GND | OPEN |
| **35 & 36** | OPEN | OPEN | OPEN | GND | OPEN | CLOSED |
| **37 & 38** | OPEN | OPEN | OPEN | GND | GND | OPEN |

Table 43: Contactor drivers – K14 Status

| TRU TEST N° | TRU COMM OFF | TRU 2 FAIL | K14 STATUS |
|---|---|---|---|
| **39 & 40** | GND | OPEN | CLOSED |
| **41 & 42** | OPEN | OPEN | OPEN |
| **43 & 44** | GND | GND | OPEN |
| **45 & 46** | GND | OPEN | CLOSED |

During all tests, the following table summarizes the verification of measuring currents from the internal current sensor.

Table 44: Measuring verification of internal current sensor

| Tests | Measured voltage from CT2 | Equivalent current |
|---|---|---|
| Contactor Controls | 864mV | 172.8A |
| Continuous Capacity | 870mV | 174A |
| Overload 5min | 1064mV | 212.8A |
| Overload 5 sec | 1400mV | 280A |
| 100A | 460mV | 92A |
| 340A | 1690 mV | 338A |
| 400A | 1940mV | 388A |
| 500A | 2440 mV | 488A |
| 600A | 3010mV | 602A |
| 700A | 3500mV | 700A |

Table 45: Measured currents and voltages during 338A load test

| TIME | L1 Current | L3 Current | L1 Voltage | L3 Voltage | L4 Voltage | L5 Voltage | L6 Voltage | L7 Voltage |
|---|---|---|---|---|---|---|---|---|
| **12:08:28** | 0,01232 | 0,0396 | 0,03803 | 0,19982 | 0,01713 | 0,03803 | 0,03803 | 0,03803 |
| **12:08:52** | 0,01496 | 0,0176 | 28,1006 | 28,10093 | 27,96947 | 28,1006 | 28,10082 | 28,0995 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **12:09:07** | 338,0792 | 338,3047 | 26,89853 | 26,70129 | 26,7306 | 26,8593 | 26,86007 | 26,85963 |
| **12:09:10** | 337,9771 | 338,2211 | 26,89842 | 26,70624 | 26,7274 | 26,85632 | 26,85687 | 26,85643 |
| **12:09:13** | 337,9199 | 338,153 | 26,89214 | 26,70702 | 26,72277 | 26,8528 | 26,85136 | 26,85225 |
| **12:09:16** | 337,8047 | 338,0166 | 26,88927 | 26,70558 | 26,71792 | 26,84861 | 26,84828 | 26,84795 |
| **12:09:19** | 337,6701 | 337,8802 | 26,88387 | 26,70426 | 26,71517 | 26,84376 | 26,84387 | 26,84475 |
| **12:09:22** | 337,5355 | 337,7812 | 26,88156 | 26,70151 | 26,71175 | 26,84035 | 26,84024 | 26,84035 |
| **12:09:25** | 337,4395 | 337,6338 | 26,87748 | 26,69864 | 26,70834 | 26,83726 | 26,83682 | 26,83737 |
| **12:09:28** | 337,378 | 337,603 | 26,87484 | 26,69578 | 26,70349 | 26,83351 | 26,83351 | 26,83296 |

DC load Bank is connected to L3 power output studs as an initial step during FIL LOGIC Board, and DC load Bank is adjusted to absorb 338A by shutting K2 and K6 contactors. Current verified from internal current sensor and this condition is kept 5 minutes.

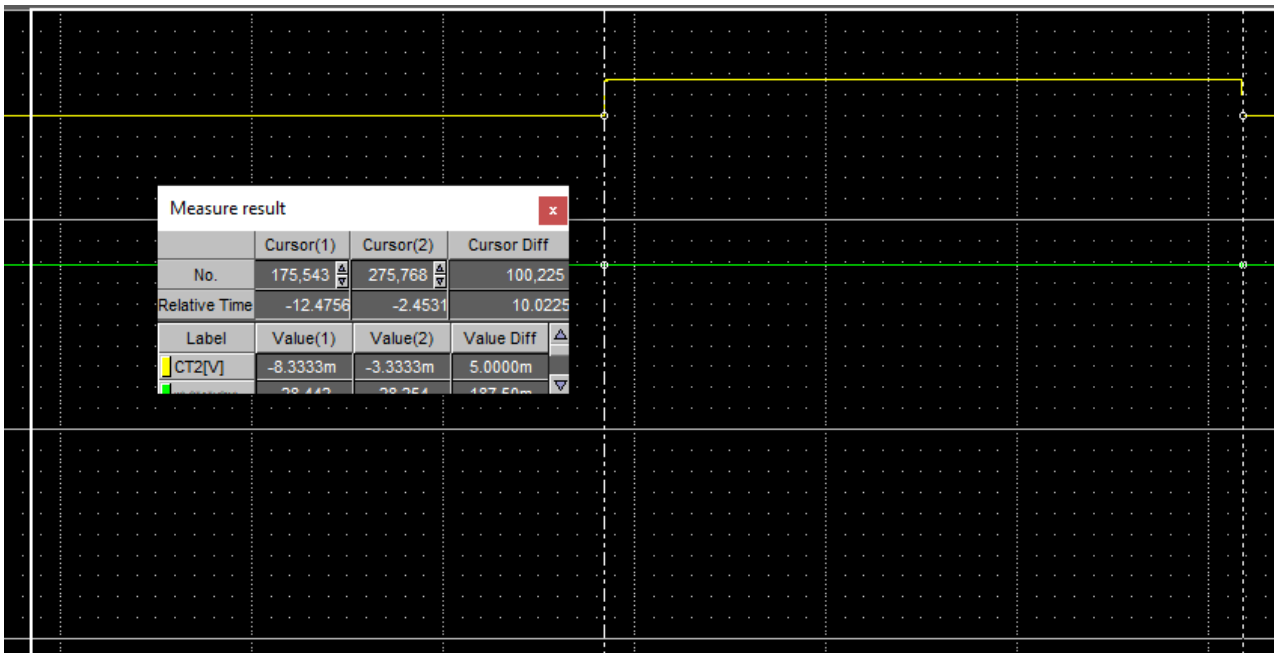



Figure 76: Intervention time of 338A overload condition.

Then DC load bank is set to absorb 402A current and this fault condition is kept 5 seconds. K6 contactor is tripped after appropriate intervention time - 4seconds. Following table demonstrates recorded current and voltage values during 402 A overload condition.

Table 46: Measured currents and voltages during 402A overload condition.

| Time | L1 Current | L3 Current | L1 Voltage | L3 Voltage | L4 Voltage | L5 Voltage | L6 Voltage |
|---|---|---|---|---|---|---|---|
| **12:22:04** | -0,02727 | 0,0462 | 28,10401 | 28,10401 | 27,98798 | 28,10346 | 28,10423 |
| **12:22:07** | 401,6273 | 402,3447 | 26,35903 | 26,18372 | 26,19353 | 26,31077 | 26,31496 |
| **12:22:10** | 402,4676 | 403,0882 | 26,40421 | 26,22394 | 26,22471 | 26,33964 | 26,33942 |
| **12:22:13** | -0,02639 | 0,0506 | 28,15834 | 0,000262 | 28,01531 | 28,12936 | 28,12605 |
| **12:22:16** | -0,02551 | 0,0506 | 28,10445 | -0,03349 | 27,98864 | 28,10423 | 28,10523 |

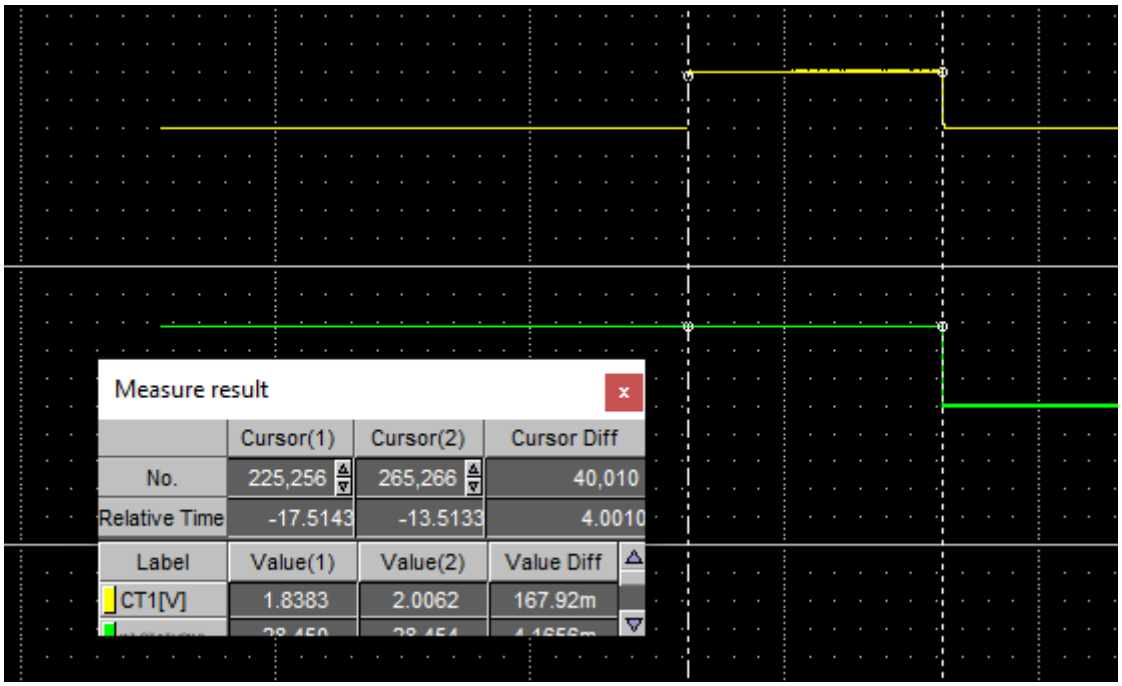



Figure 77: Intervention time of 402A overload condition.

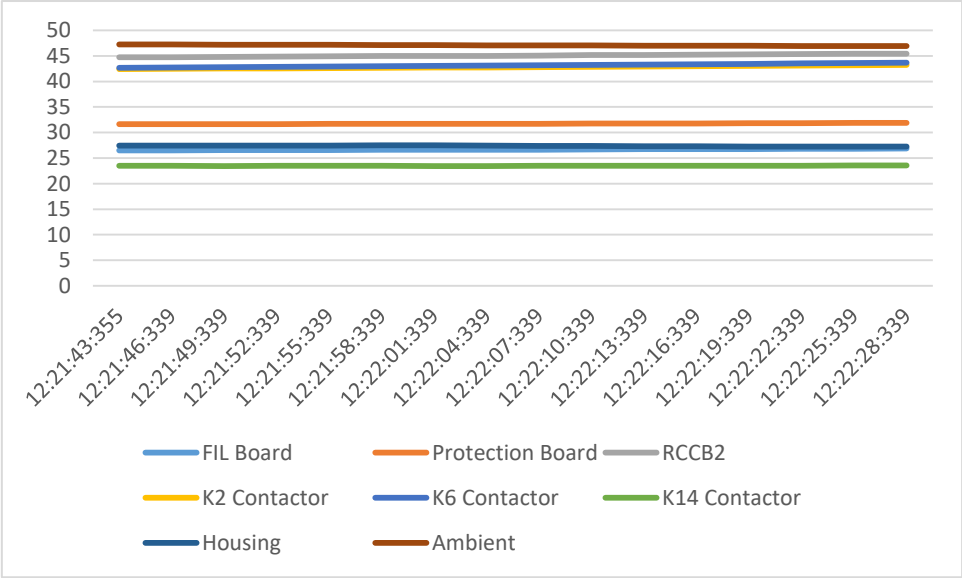



Figure 78: Temperature changes during 402A overload condition.

After resetting FIL condition by means of test box switches, DC load Bank is adjusted 492A current for maintaining 4 seconds and this value is verified by internal current sensor (TABLE 16) According to the trip curve, K6 opened at the optimal time for intervention. The current and voltage values recorded during the 402 A overload situation are shown in the table below.

Table 47: Measured currents and voltages during 492A overload condition

| Time | L1 Current | L3 Current | L1 Voltage | L3 Voltage | L4 Voltage | L5 Voltage | L6 Voltage | L7 Voltage |
|---|---|---|---|---|---|---|---|---|
| **12:29:09** | 0,03431 | 0,0242 | 28,10732 | 28,10853 | 25,48842 | 25,33106 | 25,724 | 25,78097 |
| **12:29:12** | 492,7923 | 493,5038 | 26,17281 | 25,89888 | 25,98582 | 26,09468 | 26,09468 | 26,09502 |
| **12:29:15** | 0,03167 | 0,0198 | 28,11415 | 0,02993 | 27,99944 | 28,11051 | 28,10996 | 28,11018 |

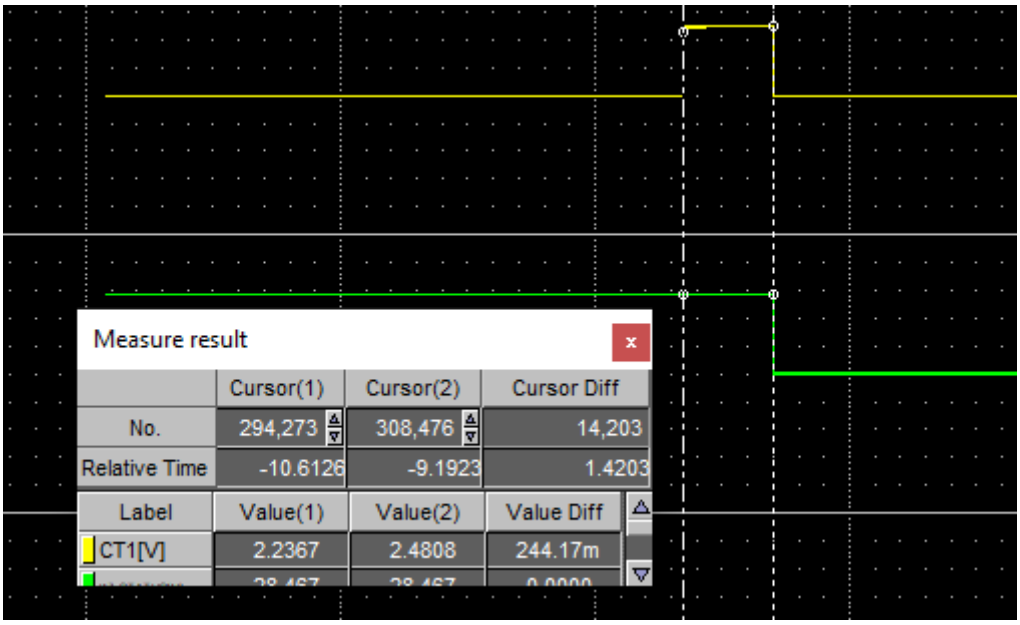


Figure 79: Intervention time of 492A Overload condition.

DC Load Bank is configured to absorb 597A current after checking OVC OUT signal is in Ground condition and resetting FIL condition using test box switches. This overload condition is maintained for 3 seconds. Following table demonstrates recorded current and voltage values during this fault condition.

Table 48: Measured currents and voltages during 597A overload condition.

| Time | L1 Current | L3 Current | L1 Voltage | L3 Voltage | L4 Voltage | L5 Voltage | L6 Voltage | L7 Voltage |
|---|---|---|---|---|---|---|---|---|
| **12:33:52** | -0,02551 | 0,0132 | 28,11084 | 28,11007 | 27,99966 | 28,11062 | 28,10974 | 28,11007 |
| **12:33:55** | 597,0609 | 597,8718 | 25,79651 | 25,46924 | 25,59497 | 25,70153 | 25,70175 | 25,7023 |
| **12:33:58** | -0,02903 | 0,0154 | 28,12352 | -0,27382 | 28,00671 | 28,11713 | 28,11624 | 28,11569 |

The figure below illustrates that K6 contactor is triggered at the proper intervention time (86ms).

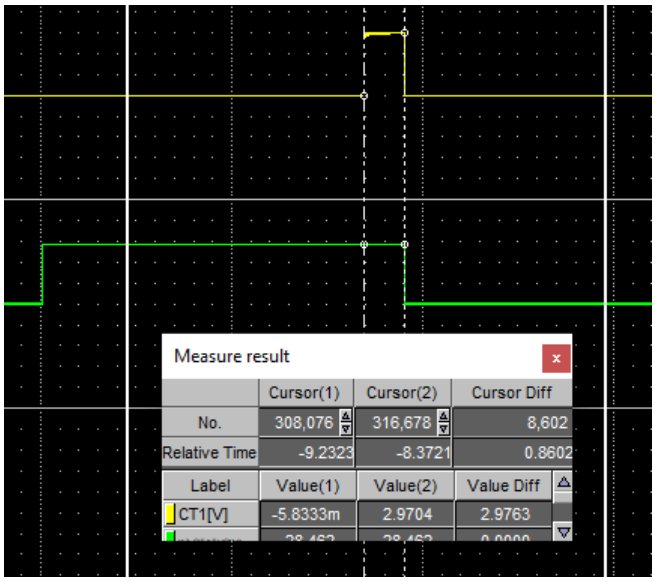


Figure 80: Intervention time of 597A overload condition.

The DC load bank is set as a last overload step to absorb 700A current. This overload condition only lasts a second. The K6 contactor is triggered at the appropriate intervention time, as shown in the figure below (645ms).

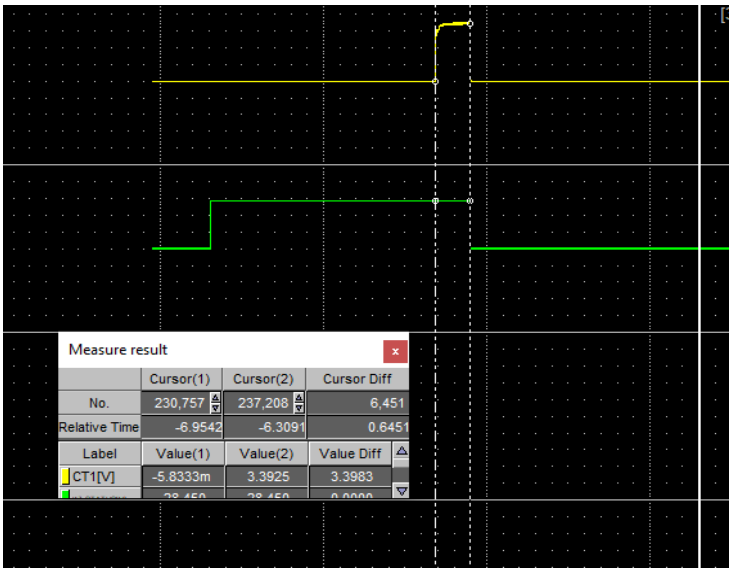


Figure 81: Intervention time of 700A overload condition.

Table 49: Recorded parameters during RCCB2 verification

| CURRENT (A) | INTERVENTION TIME (s) |
|---|---|
| **338** | 10.0225 |
| **402** | 4.001 |
| **492** | 1.4203 |
| **597** | 0.8601 |
| **700** | 0.6451 |

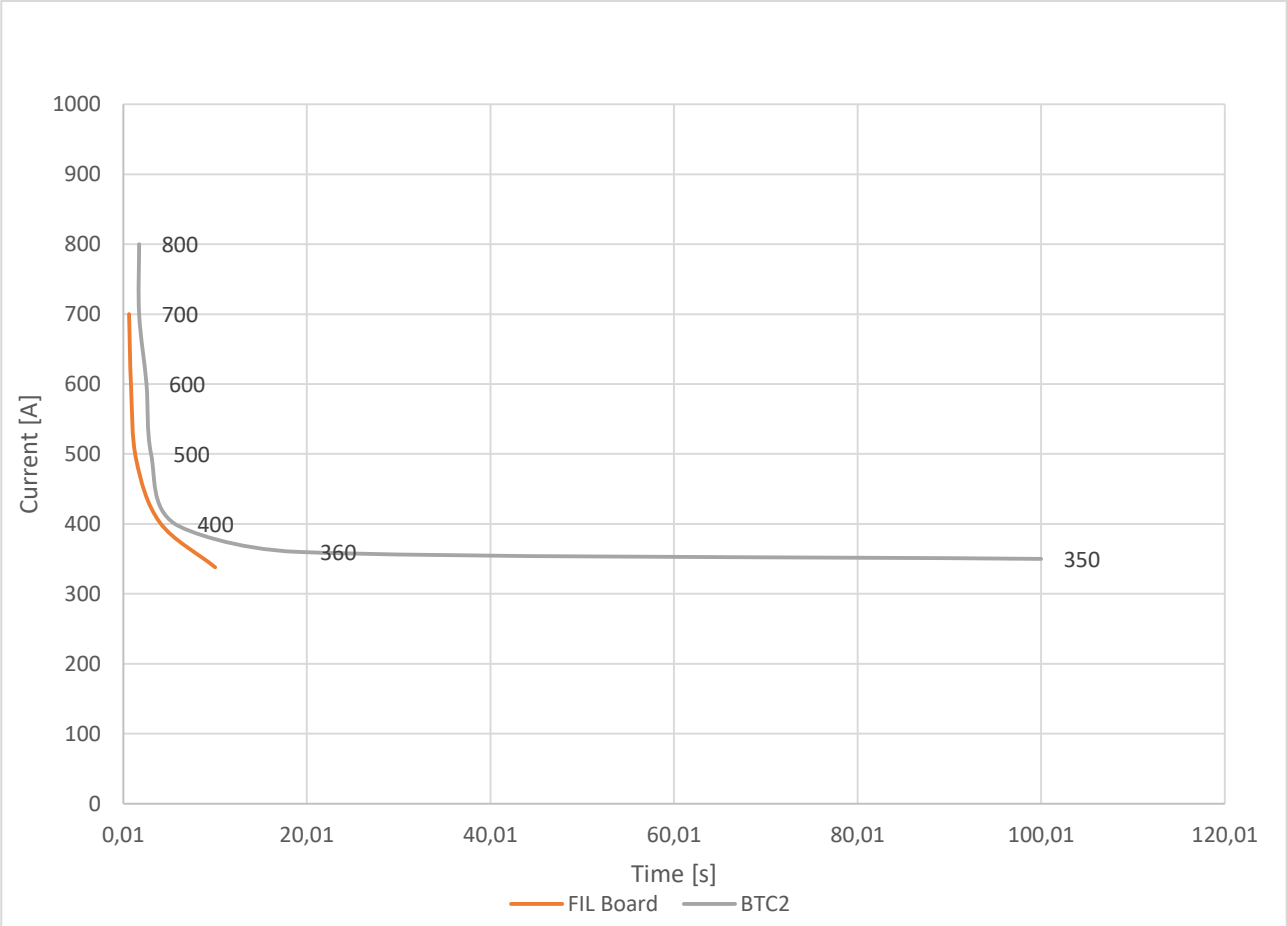


Figure 82: Overcurrent intervention curve

## 5.9 CONCLUSION FOR DC PDP 1 AND DC PDP 2

During the performance test on DC PDP 2, no out-of-limit values were recorded, starting with the steady state condition (172A). The recorded value revealed no faulty condition, nor was it erroneous or outside the present absorption level's limit.

Following that, a rating continuous capacity test at 174 A was performed using power contactors K2 and K6. During the test, all temperatures before, during, and after thermal stabilization were recorded when the rated capacity was applied. Then there is no contactor damage or trip during continuous capacity, as well as no over-temperature, deviation, or derating.

The two separate overload test conditions were applied at the end of the continuous capacity test. The current readings from the CT2, as well as the performance level, were monitored during this test. There was no unexpected contactor trip, opening, or damage during or after overload 1 (212A) at 5 minutes and overload 2 (280A) at 5 seconds.

340A, 402A, 492A, 597A, and 700A loads are applied to the L3 power output stud and K 6 contactor at the appropriate time of intervention during the FIL logic board fault condition test. Due to the maximum withstand current of diode (120A), the power diode broke during a 500A overload test at L4.

## 5.10 BATTERY PDP PERFORMANCE TEST

This Qualification Test Report (QTR) describes the results of performance tests carried out in order to perform the qualification of the BATTERY of the DC Electrical Power Distribution System.

Table 50: Test results for temperature on BATTERY PDP.

| Test Type | Test Result (PASS/FAIL) |
|---|---|
| Rated load – Contactors control and power distribution | PASS |
| Rated load – Continuous capacity | PASS |
| Short circuit capacity | PASS |
| Overload condition | PASS |
| EPM board – Input voltage for overvoltage and Reverse polarity | **FAILED** |

### 5.10.1 TEST CONDITIONS

All measurements and tests were carried out under the following conditions:

Temperature: +15°C ÷ +35ºC
Relative Humidity: 20% ÷ 85%
Atmosphere Pressure: 84kPa ÷ 107kPa

If measurements or tests have been performed under different ambient conditions, it has been reported in the following paragraph within the data of the test.

### 5.10.2 THERMAL STABILIZATION

Items are considered thermally stabilized when the temperatures of all their instrumented parts change no more than ±1°C in 5 minutes.

### 5.10.3 TEST EQUIPMENT

The following equipment (Table 51) has been used to carry out the tests outlined in this QTR document:

Table 51: Equipment for BATTERY PDP Qualification test.

| Description | Supplier | Model or Part Number | Serial Number | Calibration Expiration |
|---|---|---|---|---|
| General purpose 28VDC power supply | TTI | EX354D | 265739 | 08/2022 |
| DC Load Bank | Magneti Marelli | G27LDC | 0001 | - |
| ATP Test Box | ASE S.p.A. | DB16UC-DC/3 | N.A. | - |
| Interface harness | ASE S.p.A. | DB23W | N.A. | - |

### 5.10.4 TEST INSTRUMENTATION AND ACCURACY

To perform the tests described in this document, the following instrumentation Table 52 was used.

Table 52: Instrumentation for BATTERY PDP functional qualification test.

| Description | Model | Supplier | Range | Accuracy | Parameter Measured | Calibration Expiration |
|---|---|---|---|---|---|---|
| Data logger | 34970A | Agilent | 100Vdc input | 0.005% FS max | DC Voltage/ sensor outputs | 04/2022 |
| | | | 100Vac input | 0.17% FS on rms | AC Voltage rms | |
| | | | -100÷400°C | 1°C | Temperature | |
| Multimeter (6.5 digit) | DMM4040 | TEKTRONIX | 1000Vdc | 0.0026% FS max | Voltage | 08/2022 |
| | | | 3Adc | 0.07% FS max | Current | |
| | | | 100MΩ | 0.31% FS max | Resistance | |
| Oscilloscope | DL 850 | Yokogawa | 850/250V peak 0.04/2MHz | 1.5% | Voltage waveforms | 09/2022 |
| Megaohmeter | 1867 | QUADTECH | 0 to 100 MΩ | 5 % | Insulation resistance | 06/2023 |
| Dielectric strength tester | / | PESATORI | 0 to 3 kV I leakage = 20 mA | 5 % | Dielectric strength | 12/2022 |

### 5.10.5 GENERAL TOLERANCES

Unless otherwise indicated during the test procedures, the maximum permissible tolerance for the test conditions (i.e. imposed test parameter) were listed below:

| | | | |
|---|---|---|---|
| Environmental | | Temperature | ± 3°C |
| | | Altitude | ± 5% of the specified pressure |
| | | Speed | ± 50rpm |
| Mechanical | **Sinusoidal Vibration**: | Acceleration | ±10% |
| | | Frequency | ±2% |
| | **Random Vibration**: | PSD value below 500Hz | +3dB; -1.5dB |
| | | PSD value 500Hz÷2000Hz | +3dB; -3dB |
| | | Overall g rms value | +20%; -5% |
| Electrical | | Force | ± 2% |
| | | Voltage | ± 1V |
| | | Current | ± 2A |
| | | Frequency | ± 2Hz |
| | | Power | ± 5% |

### 5.10.6 TEST SET-UP DETAILS

The test setup for the Battery PDP is depicted in figures below. The instrument and equipment of Table 51 and Table 52 are used and an oscilloscope as measuring instrument is chosen to record the following parameters:

1. Input current
2. Input voltage
3. Output current
4. Contactors' action time
5. Steady state current
6. Output load voltage
7. Temperature

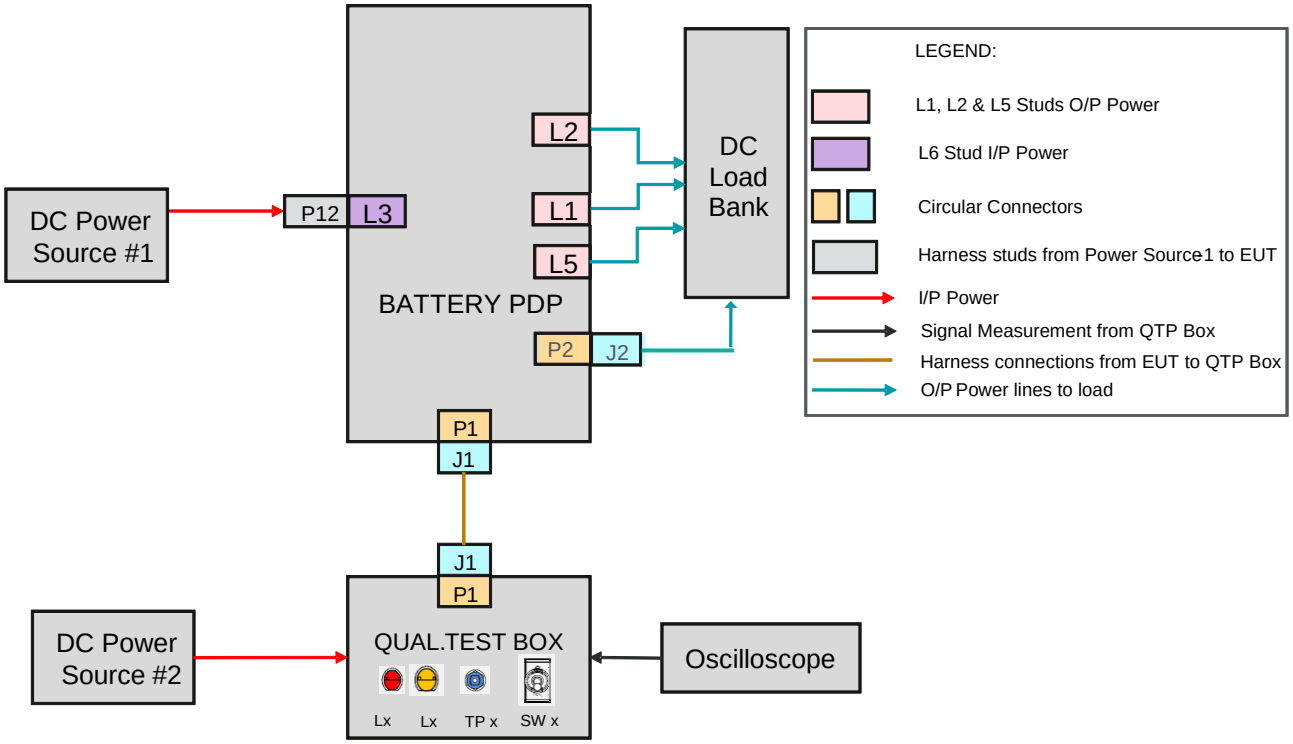



Figure 83: Test setup for operation performance of BATTERY PDP.

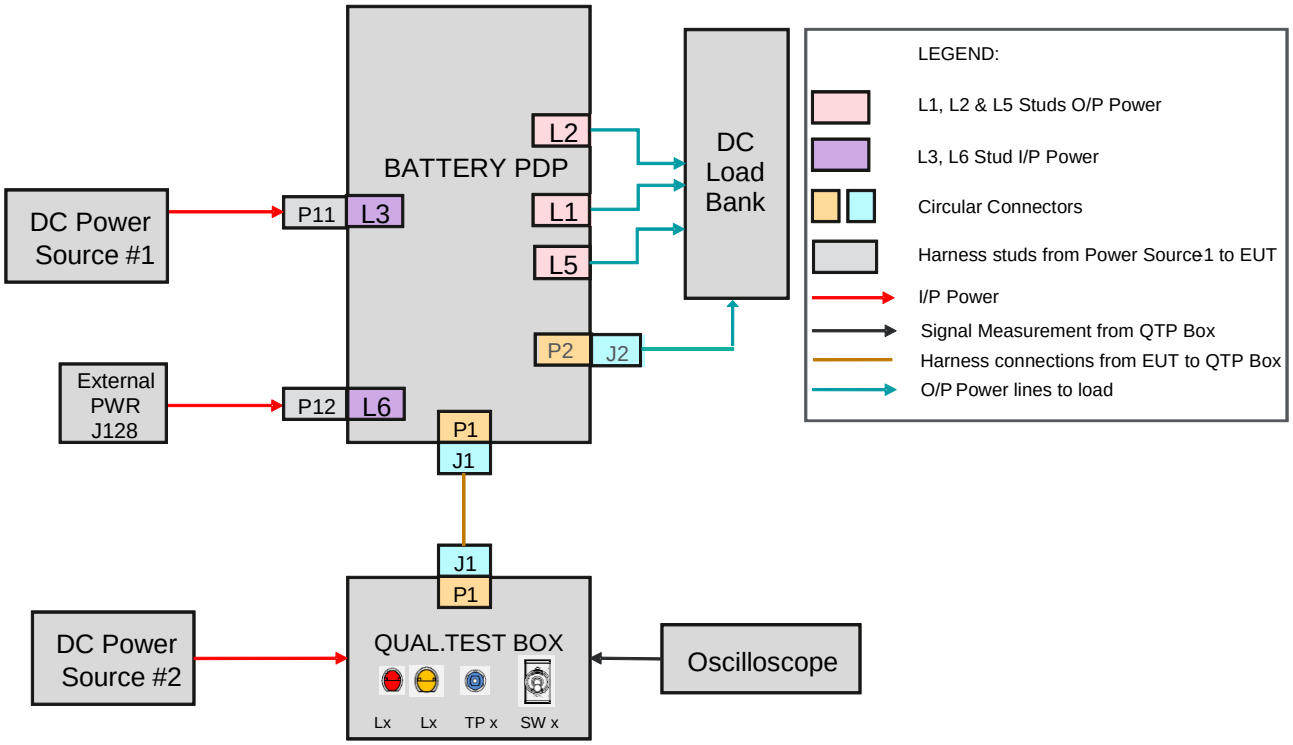



Figure 84: Test setup for performance of BATTERY PDP EPM.

Figure 85: General test setup for Battery performance

### 5.10.7 TEST SEQUENCE

Tests are planned to be carried out according to the below sequence. The only constraint is about the first and the last step (pre-test and post-test ATPs).

**Initial:**

2. Pre-test ATP on all EUT

**Functional Tests:**

3. Performance DC BATTERY Component and Characteristics

**Final:**

4. Post-test ATP

↓↓↓

**"Functional Test on the DC BATTERY PDP" session successful.**

### 5.10.8 PERFORMANCE TEST ON BATTERY PDP.

By connecting the equipment to the Qualification Test Box, the DC Power Source, and the DC Load Bank, the goal of the test is to validate the system performance of the BATTERY.

The EUT contactors will be driven externally by the signal provided from the Qualification Test Box. An oscilloscope and data logger are used to verify the appropriate status signals, and the parameter is recorded.

The test will be carried out in the following sub-steps:

1. Rated load – Contactors control and power distribution
2. Rated load – Continuous capacity
3. Short circuit capacity
4. Overload condition
5. EPM board – Input voltage for overvoltage and Reverse polarity

In Table 53and Table 54 all the electrical interfaces and connector functions are described in order to simplify the setting of cables and connections of setup.

Table 53: Connections and electrical interfaces in BATTERY PDP

| Stud | I/O | Function | Power/Signal |
|---|---|---|---|
| L1 | I/O | BATTERY | POWER |
| L2 | O | EMERGENCY BUS 2 | POWER |
| L3 | I/O | BUS TIE to DC PDP 2 | POWER |
| L4 | O | APU START | POWER |
| L5 | O | BATTERY BUS | POWER |

Table 54: J1 and J2 connectors of BATTERY PDP

| Connector | Part Number | Function |
|---|---|---|
| J1 | D38999/20WG41PN<br>(pin contact)<br>(MIL-C-38999) | Signal connector<br>(Number of contacts 41) |
| J2 | MS3450W12-5S<br>(socket contact)<br>(MIL-DTL-5015) | Power connector<br>(1 contact)<br>HOT BATTERY BUS |

### 5.10.9 OPERATION – RATED LOAD AND OVERLOAD TESTS

The main objectives of the two sub-tests are:

**Contactor controls and power distribution**: verify the external power contactor closes when the external signal is sent from the Qualification Test Box and all the closure conditions are “true”. The bus voltage will also be verified at the load box connected at the studs.

**Continuous capacity:** verify the System is able to give required continuous output currents, keeping the minimum output voltages required under each load condition.
The test will be carried out at the minimum load current required for the Battery PDP under specific conditions

**Overload:** verify if the load current at the studs exceeds the short circuit or overload current drawn. When the load current connected at the stud (L2) falls in anyone category, the RCCBs inside the PDP will sense and control the load and disconnect the contactors.
Also, the system behavior is verified in order to obtain main contactor opened and bus voltage disconnected at the stud (L5).

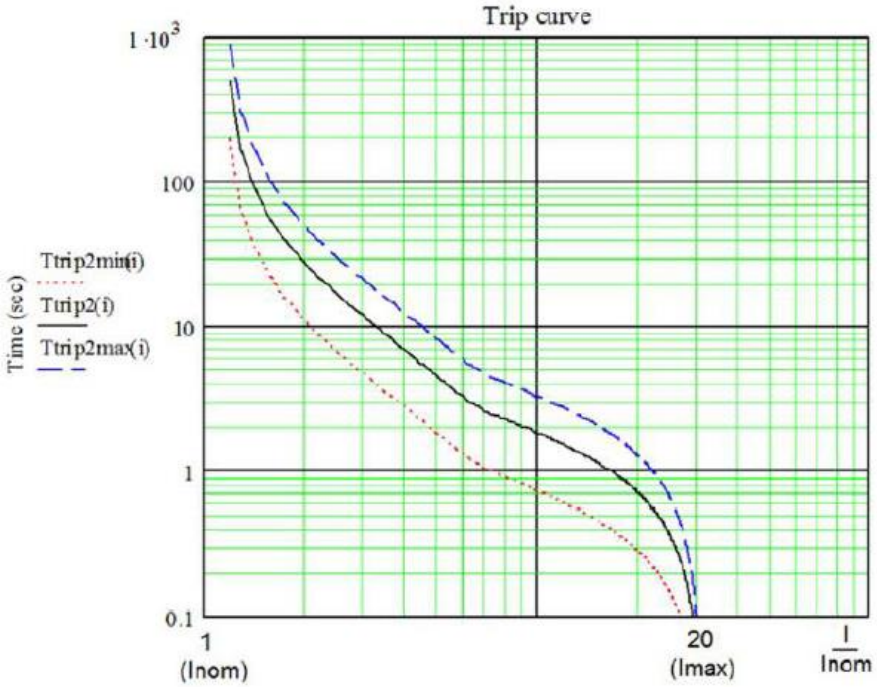



Figure 86: RCCB overcurrent trip curve.

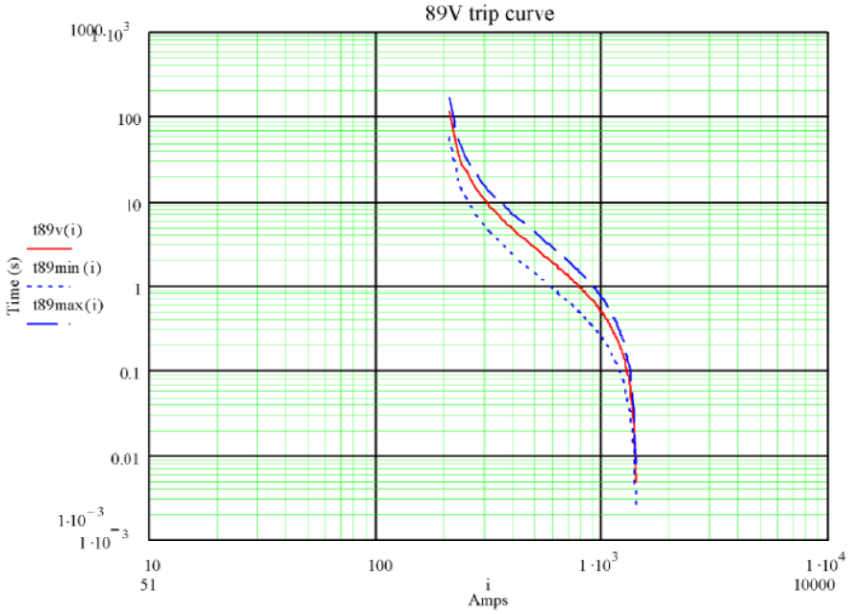



Figure 87: T9 BATTERY charge trip curve.

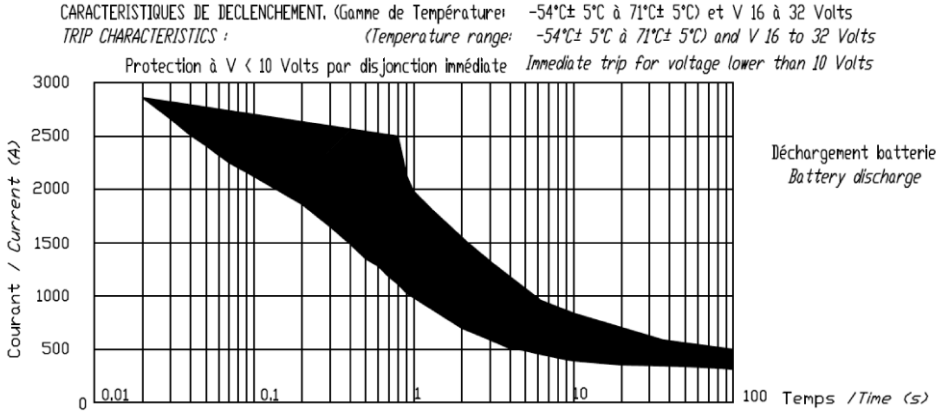



Figure 88: T9 BATTERY discharge trip curve.

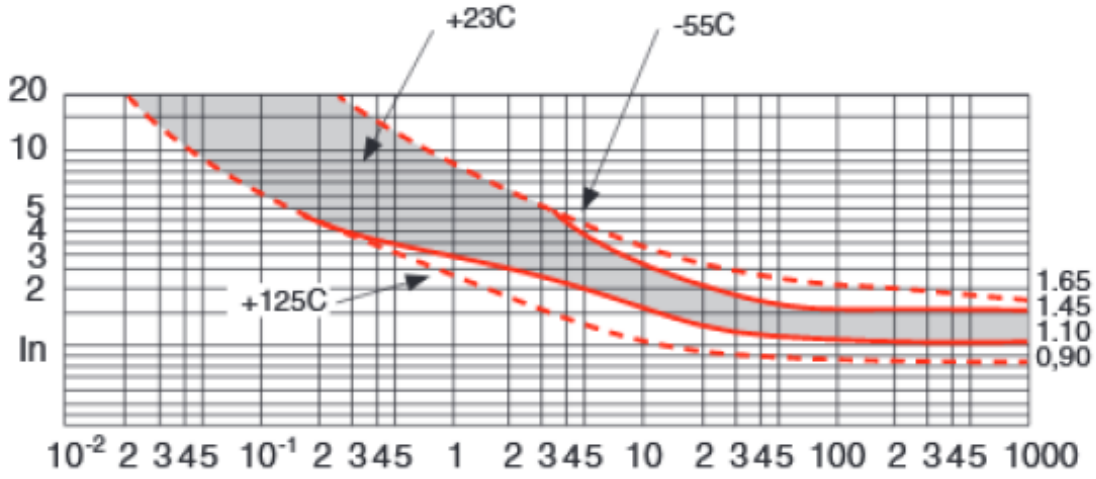



Figure 89: Hot Battery and Battery Bus CB trip curve.

### 5.10.10 RATED AND OVERLOAD TEST PROCEDURES OF BATTERY

**PRE-REQUISITES**

1. Ensure the EUT has passed the pre-test ATP;
2. Ensure that the EUT and all the switches are in the starting state;
3. Perform test setup operations as detailed in

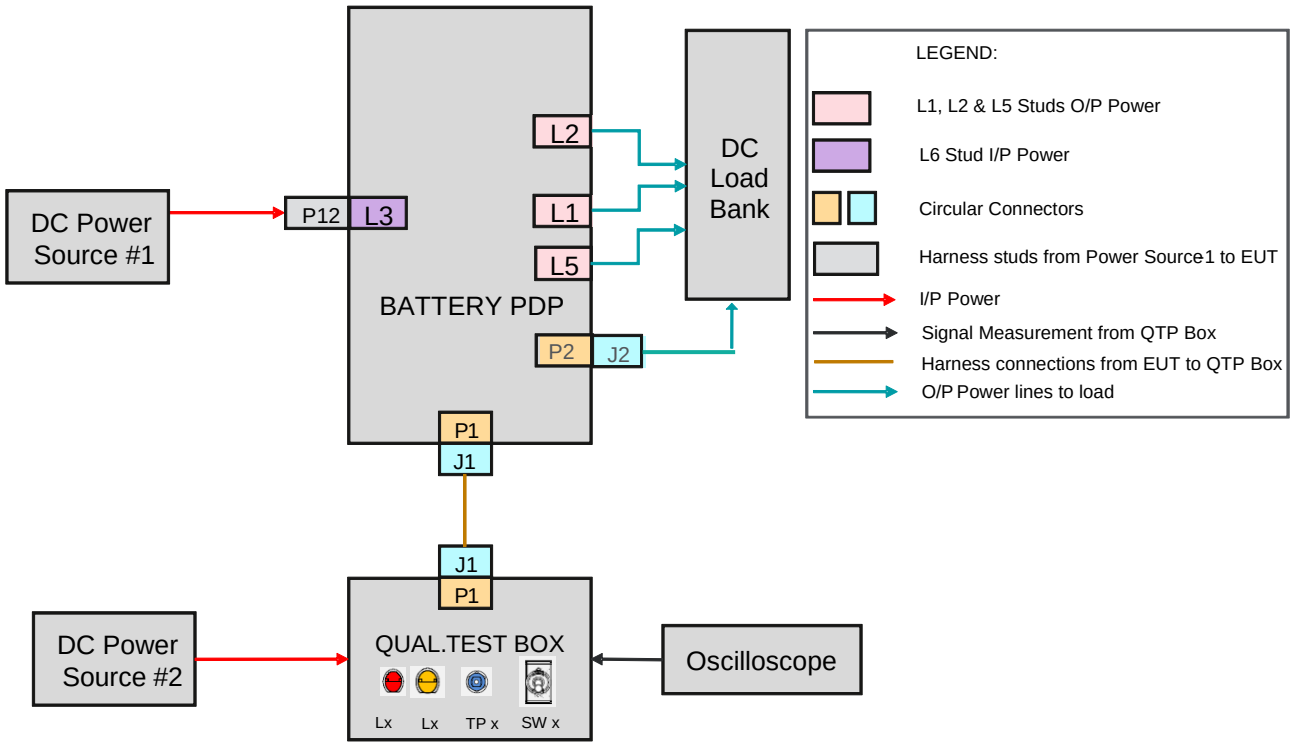



Figure 83

4. Connect positive terminal of DC Power Supply #1 to the input stud L3;
5. Set DC Power Supply #1 to give 28V±0.5V voltage;
6. Connect DC Load Bank to power output studs L1 and L5 and J2 connector.

**INITIAL OPERATIONS**

7. Set the data-logger to acquire the system parameters defined in §5.10.6
8. Set the oscilloscope to monitor parameters by means of test box.

**TEST CORE – CONTACTOR CONTROLS AND POWER DISTRIBUTION**

9. Start recording parameters with the data-logger
10. Turn ON the DC Power Supply #1
11. Verify that the system is ONLINE (related switch and led on test box)
12. Close K10 and K22 contactors by means of test box switches
13. Set DC Load Bank in order to absorb 38.2A±5A
14. Verify current from internal current sensors T8 and T9 test points on test box
15. At L1 stud verify that output voltage is 28V±0.5V and output current is 25.5A
16. At L5 stud verify that output voltage is 28V±0.5V and output current is 12.6A
17. At J2 stud verify that output voltage is 28V±0.5V and output current is 0.1A
18. Keep the rating condition for 5min
19. Turn OFF the DC Load Bank
20. Stop and save data-logger acquisition.

**TEST CORE – CONTINUOUS CAPACITY**

21. Start recording parameters with the data-logger
22. Maintain K10 and K22 contactors in closed condition by means of test box switches
23. Set DC Load Bank in order to absorb 38.2A±5A
24. Verify current from internal current sensors T8 and T9 test points on test box
25. Keep the rating condition for a time not less than 15min
26. Monitor the internal temperature of the EUT and verify it is not over 85°C after thermal stabilization is reached

**TEST CORE – BATTERY OVERLOAD**

27. Maintain K10 and K22 contactors in closed condition by means of test box switches
28. Set DC Load Bank in order to absorb 50.6A±5A
29. Verify current from internal current sensors T8 and T9 test points on test box
30. Maintain this 50.6A±5A overload condition for 5min
31. Monitor the internal temperature of the EUT and verify it is not over 85°C
32. Set DC Load Bank in order to absorb 77A±5A
33. Verify current from internal current sensors T8 and T9 test points on test box
34. Maintain this 77A±5A overload condition for 5s
35. Monitor the internal temperature of the EUT and verify it is not over 85°C
36. Remove all DC Load applied at the system and disconnect all the terminals
37. Open all the contactors
38. Stop and save data-logger acquisition
39. Turn OFF the DC Power Supply #1

**TEST CORE – OVERLOAD (HOT BATT BUS CB, CB20, T9 – BATTERY CHARGE, RCCB4)**

40. Connect DC Load Bank to J2 connector
41. Maintain DC Power Supply #1 set to give 28V±0.5V voltage
42. Start recording parameters with the data-logger
43. Turn ON DC Power Supply #1
44. Close K10 contactor by means of test box switch
45. Stabilize the system by applying rating load condition for 5min (38.2A±5A as per Table 11)
46. Set DC Load Bank in order to absorb 50A±5A
47. Verify current from internal current sensors T8 and T9 test points on test box
48. Verify that overload conditions (fault) of the current drawn at J2 is more than the rated current of the HOT BATT BUS CB, according to trip curve of Figure 89
49. Verify that HOT BATT BUS CB activates in the right time of intervention according to the related temperature and following curve described in Figure 89
50. Monitor the internal temperature of the EUT and verify it is not over 85°C
51. Remove the load applied to the system and disconnect the terminals

52. Connect DC Load Bank to L5 output power stud
53. Stabilize the system by applying rating load condition for 5min (38.2A±5A as per Table 11)
54. Set DC Load Bank in order to absorb 50A±5A
55. Verify current from internal current sensors T8 and T9 test points on test box
56. Verify that overload conditions (fault) of the current drawn at L5 is more than the rated current of the CB20, according to trip curve of Figure 86
57. Verify that CB20 activates in the right time of intervention according to the related temperature and following curve described in Figure 86
58. Monitor the internal temperature of the EUT and verify it is not over 85°C
59. Remove the load applied to the system and disconnect the terminals
60. Connect DC Load Bank to L1 output power stud
61. Stabilize the system by applying rating load condition for 5min (38.2A±5A as per Table 11)
62. Set DC Load Bank in order to absorb 200A±5A
63. Verify current from internal current sensors T8 and T9 test points on test box
64. Verify that overload conditions (fault) of the current drawn at L1 is more than the rated current of the current protection sensor T9, according to charge trip curve of Figure 87
65. Verify that T9 activates in the right time of intervention according to the related temperature and following curve described in Figure 87
66. Monitor the internal temperature of the EUT and verify it is not over 85°C
67. Remove the load applied to the system and disconnect the terminals
68. Close K22 contactor
69. Connect DC Load Bank to L2 output power stud
70. Stabilize the system by applying rating load condition for 5min (38.2A±5A as per Table 11)
71. Set DC Load Bank in order to absorb 200A±5A
72. Verify current from internal current sensors T8 and T9 test points on test box
73. Verify that overload conditions (fault) of the current drawn at L2 is more than the rated current of the RCCB4, according to trip curve of Figure 86
74. Verify that RCCB4 activates in the right time of intervention according to the related temperature and following curve described in Figure 86
75. Monitor the internal temperature of the EUT and verify it is not over 85°C
76. Remove all DC Load applied at the system
77. Stop and save data-logger acquisition
78. Turn OFF the DC Power Supply
79. Open all contactors
80. Verify 0V at output studs

**TEST CORE – OVERLOAD (T9 – BATTERY DISCHARGE)**

81. Switch DC Load position with DC Power Supply position in order to test the battery discharge condition
82. Connect positive terminal of DC Power Supply #1 to the input stud L1
83. Set DC Power Supply #1 to give 28V±0.5V voltage
84. Connect DC Load Bank to power output studs L3
85. Maintain K10 and K22 contactors in closed condition by means of test box switches
86. Stabilize the system by applying rating load condition for 5min (38.2A±5A as per Table 11) with L1 as input and L3 loaded with 25.5A±5A
87. Set DC Load Bank in order to absorb 200A±5A
88. Verify current from internal current sensors T8 and T9 test points on test box
89. Verify that overload conditions (fault) of the current drawn at L3 is more than the rated current of the current protection sensor T9, according to discharge trip curve of Figure 88
90. Verify that T9 activates in the right time of intervention according to the related temperature and following curve described in Figure 88
91. Monitor the internal temperature of the EUT and verify it is not over 85°C

**FINAL OPERATIONS**

92. Remove all DC load applied at the system

93. Stop and save data-logger acquisition
94. Turn OFF the DC Power Supply
95. Open all contactors
96. Verify 0V at output studs

## 5.11 BATTERY PERFROMANCE TEST RESULTS

### 5.11.1 CONTACTOR CONTROLS AND POWER DISTRIBUTION

The purpose of the test is to ensure that the external power contactor closes when the external signal from the Qualification Test Box is sent, and that all of the closure conditions are "true." The bus voltage will also be checked at the load box, which will be connected to the PDP's studs.

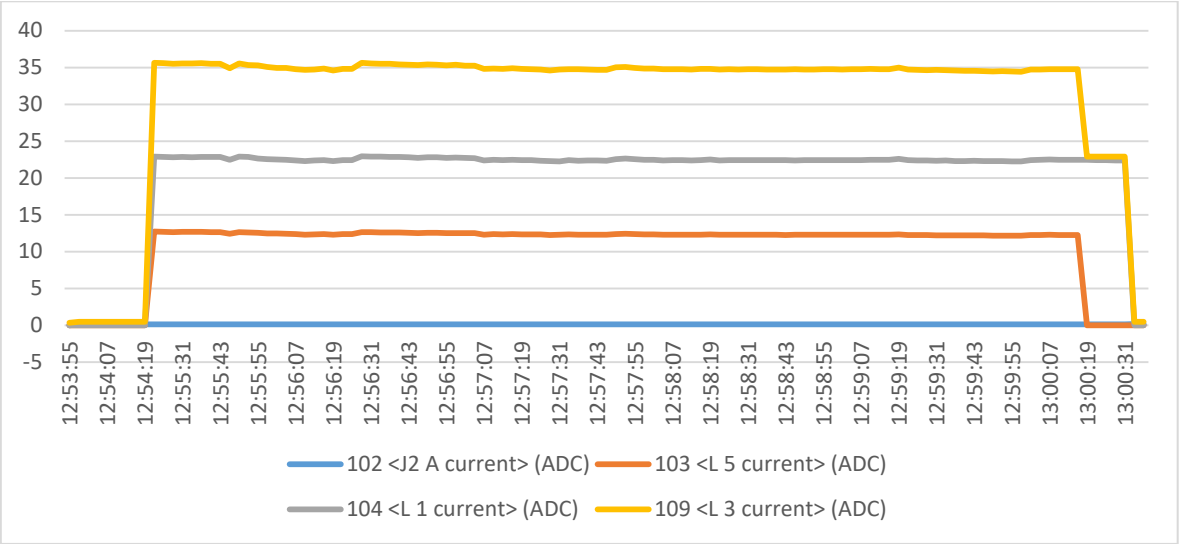



Figure 90: The output currents at L1, L3, L5 and J2 studs.

DC Load Bank is absorbing 34.9 A as Total load during the Contactor Controls and Power Distribution test for 5 minutes.

Table 55: Measured output current and voltages during contactor control and power distribution.

| STUD | OUTPUT CURRENT | OUTPUT VOLTAGE |
|---|---|---|
| **L1** | 22.8 A | 28 V |
| **L5** | 12.3 A | 28 V |
| **J2** | 0.136 A | 28 V |

### 5.11.2 CONTINOUS CAPACITY

The purpose of the continuous capacity test is to ensure that the system can provide the required continuous output currents while maintaining the minimum output voltages under previous load condition (Total DC load 34.9 A). Rating condition is kept more than 15 minutes.

The current from the internal current sensor T8 is verified by measuring 113 mV on the test bench's test points, which equals 22,6 A.

Following figure depicts changes in temperature during continuous capacity test for 15 minutes.

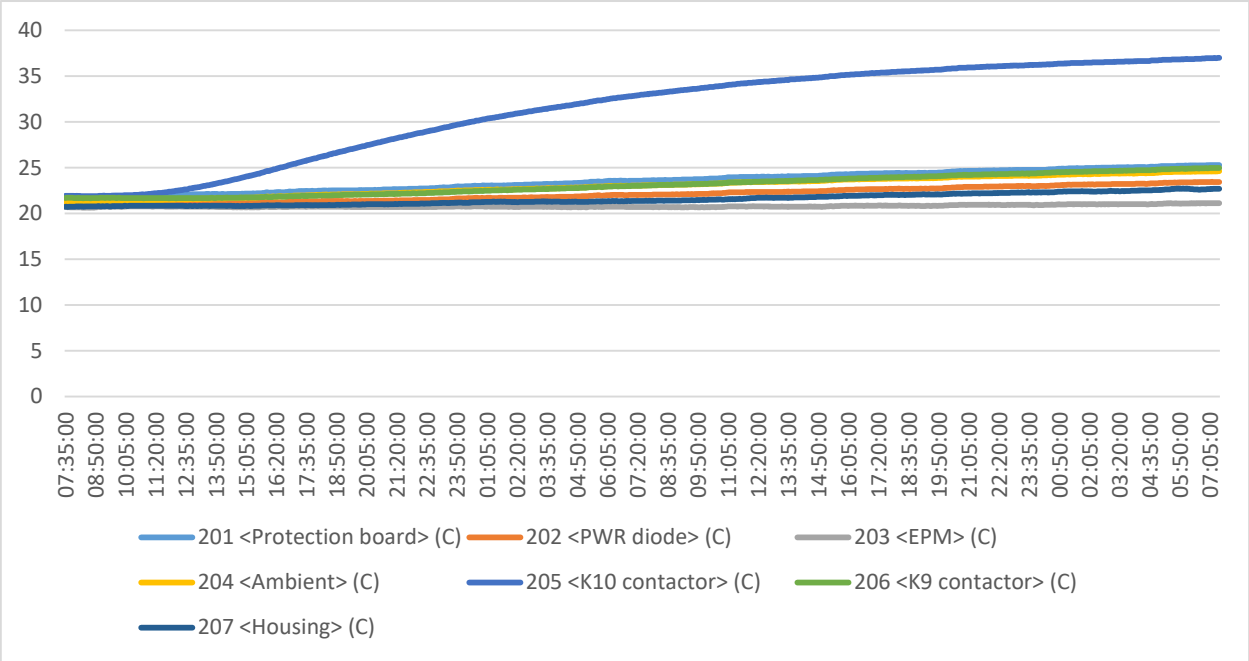



Figure 91: Changes in temperature during Continuous capacity

### 5.11.3 BATTERY OVERLOAD

K10 and K22 contactors are maintained closed for 5 minutes by test box switches and a DC load bank set to 60 A as an overload condition. Figure 92 shows output current and voltage in the same graph during battery overload test for 60 A.

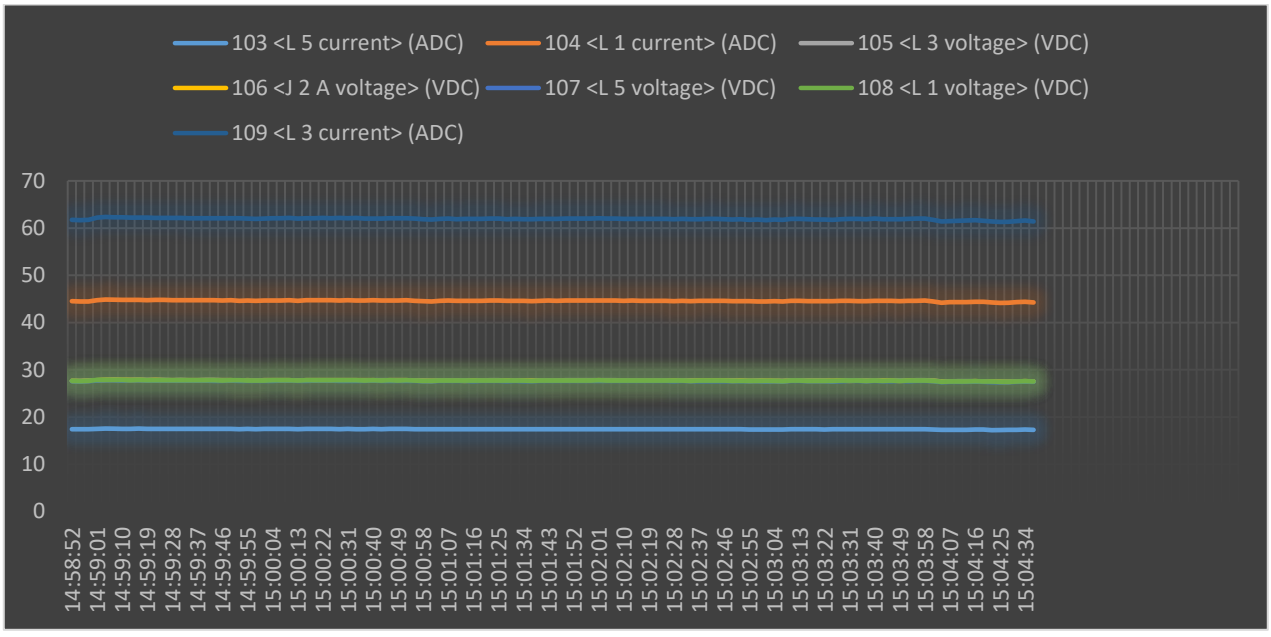



Figure 92: Battery overload first test- 60 A for 5 min

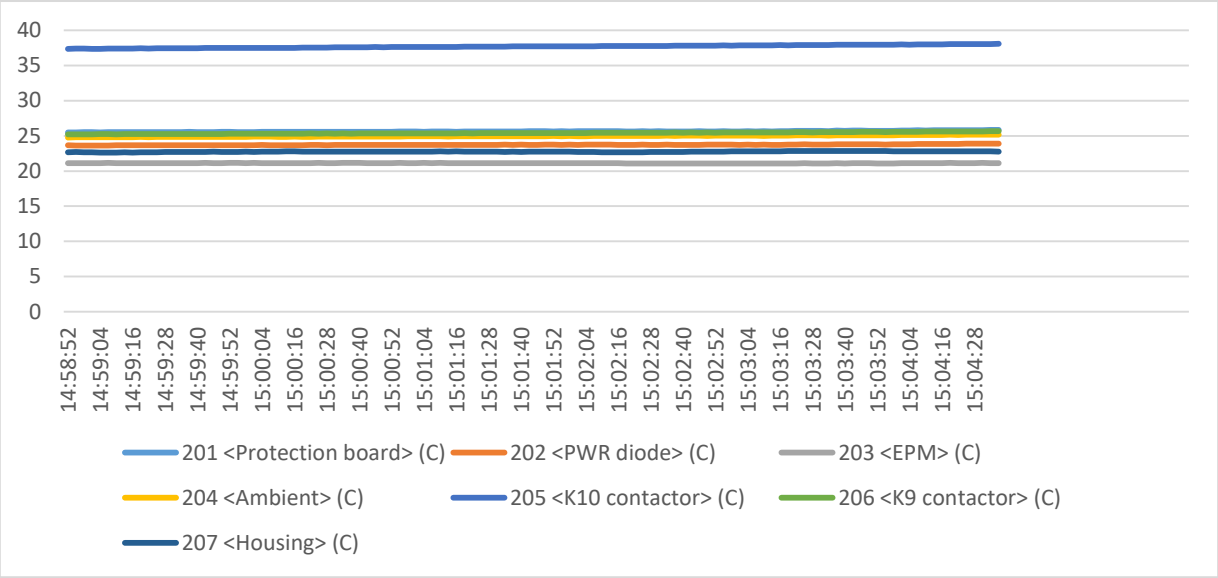



Figure 93: Changes in Temperature during battery Overload – 62A

Table 56: Measured current and voltages during overload 62A condition

| TIME | J2 A current | L 5 current | L 1 current | L 3 voltage | J 2 A voltage | L 5 voltage | L 1 voltage | L 3 current |
|---|---|---|---|---|---|---|---|---|
| **14:58:55** | 0,194342 | 17,37398 | 44,4364 | 27,61011 | 27,60024 | 27,49402 | 27,56823 | 61,69602 |
| **14:59:55** | 0,195101 | 17,44112 | 44,68846 | 27,77569 | 27,74499 | 27,63681 | 27,72404 | 61,99927 |
| **15:00:55** | 0,194918 | 17,41149 | 44,59195 | 27,71667 | 27,70929 | 27,63214 | 27,73424 | 61,991 |
| **15:01:55** | 0,195175 | 17,41385 | 44,64489 | 27,75887 | 27,72817 | 27,64939 | 27,71797 | 62,00058 |
| **15:02:55** | 0,194717 | 17,36387 | 44,51788 | 27,66697 | 27,65048 | 27,54653 | 27,63702 | 61,78229 |
| **15:03:55** | 0,195157 | 17,41999 | 44,61962 | 27,75909 | 27,71059 | 27,64625 | 27,70788 | 62,00014 |
| **15:04:37** | 0,193632 | 17,26714 | 44,25537 | 27,51127 | 27,48458 | 27,41492 | 27,48599 | 61,4176 |

Considering the above data, it can be calculated the dissipated power during this test, which is:

$$P = \left((V_{L3} - V_{L1}) \times I_{L1}\right) + \left((V_{L3} - V_{L5}) \times I_{L5}\right) = \left((27.51 - 27.48) \times 44.25\right) + \left((27.51 - 27.41) \times 17.47\right) = 3.06W$$

**Power dissipation: P=3.06W**

After verifying Battery First Overload test for 60 A, The DC load bank is adjusted at 74.4 A load as a Second Overload Test and maintained this overload condition for 5 seconds.

Following figure demonstrates the monitored output current and voltage during the second Overload test.

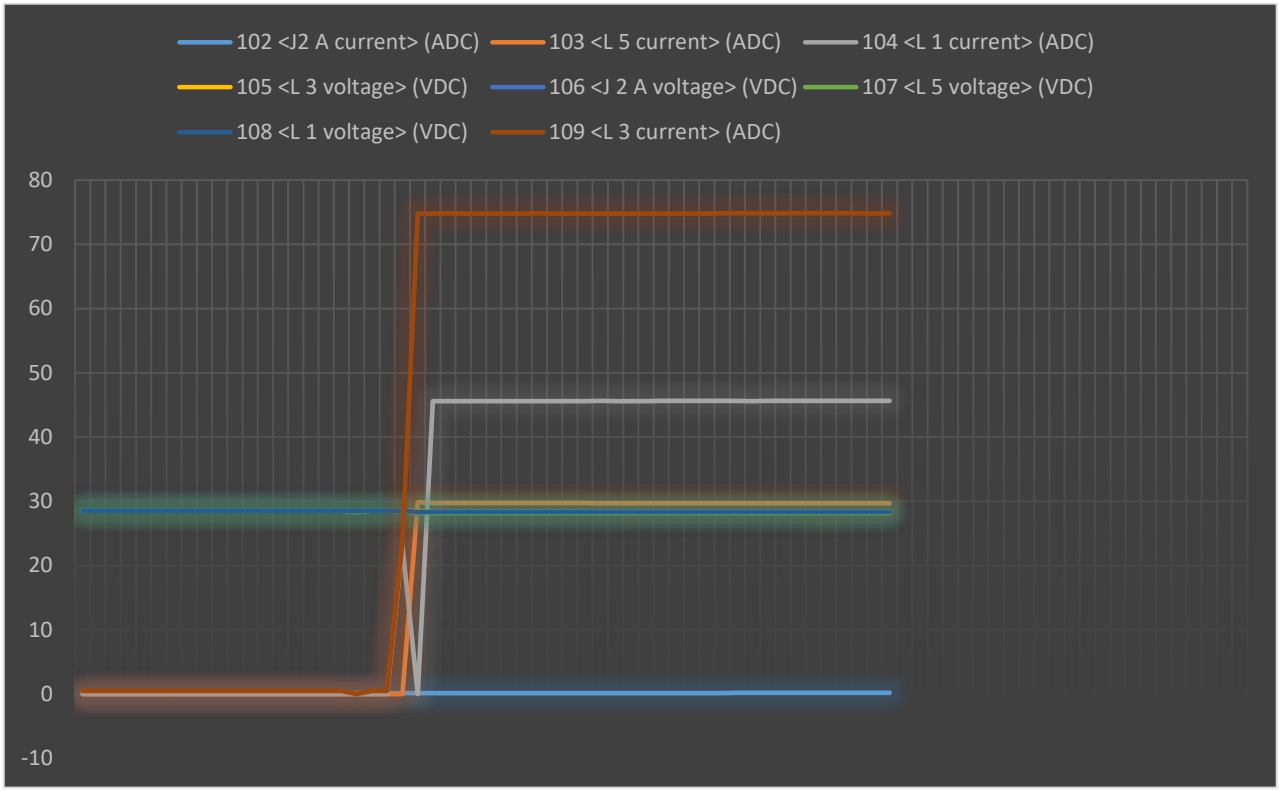



Figure 94: Battery overload second test- 74.4 A for 5 s.

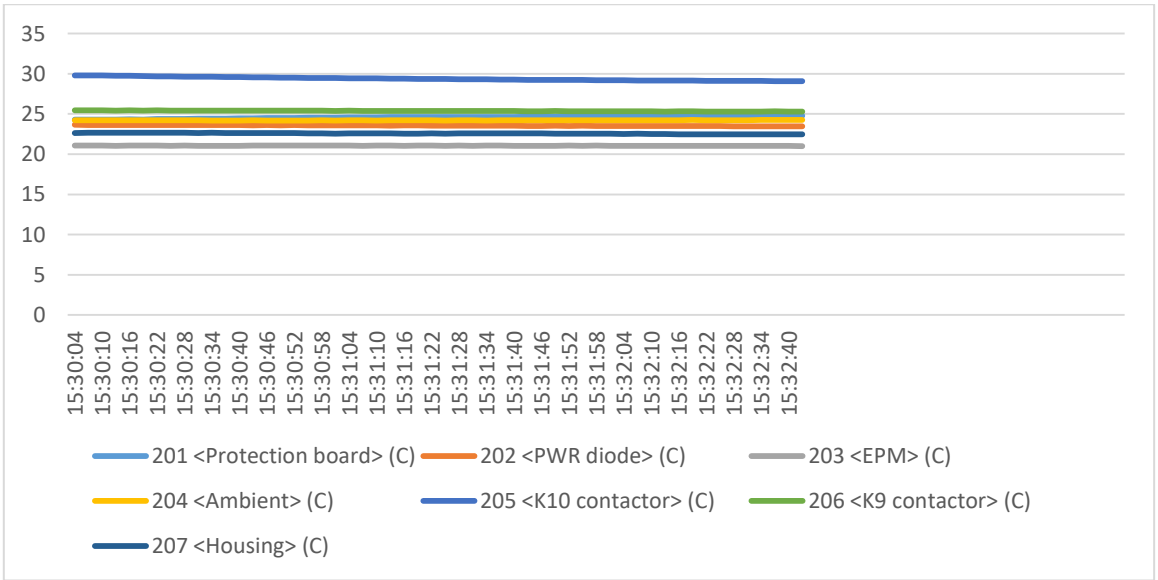



Figure 95: Temperature variations during Battery Overload -74.4 A

Table 57: Measured current and voltages during second overload 74,8A condition.

| Time | J2 A current | L 5 current | L 1 curren | L 3 voltage | J 2 A voltage | L 5 voltage | L 1 voltage | L 3 current |
|---|---|---|---|---|---|---|---|---|
| **15:31:13** | 0,139008 | 29,76057 | 45,57098 | 28,39102 | 28,36259 | 28,20971 | 28,35825 | 74,8047 |
| **15:31:25** | 0,139038 | 29,73809 | 45,58863 | 28,39254 | 28,36997 | 28,21264 | 28,35695 | 74,81472 |
| **15:31:37** | 0,139021 | 29,72375 | 45,59908 | 28,39135 | 28,36834 | 28,20917 | 28,35543 | 74,80164 |
| **15:31:49** | 0,139099 | 29,71739 | 45,60453 | 28,39601 | 28,36823 | 28,20906 | 28,35749 | 74,81428 |
| **15:32:01** | 0,139051 | 29,70776 | 45,61825 | 28,3972 | 28,36259 | 28,20938 | 28,35945 | 74,80426 |
| **15:32:13** | 0,197636 | 29,69386 | 45,62958 | 28,40176 | 28,36596 | 28,20461 | 28,36162 | 74,85175 |
| **15:32:25** | 0,197911 | 29,68611 | 45,62217 | 28,39536 | 28,36172 | 28,20211 | 28,35597 | 74,84304 |
| **15:32:37** | 0,197898 | 29,67713 | 45,62675 | 28,39666 | 28,3627 | 28,2007 | 28,35445 | 74,81951 |
| **15:32:43** | 0,197976 | 29,67317 | 45,62588 | 28,39764 | 28,36313 | 28,1956 | 28,35977 | 74,84173 |

### 5.11.4 OVERLOAD - BATTERY CHARGE

During the Overload (BATTERY CHARGE) test, a DC load bank is connected to the J2 connector and 28 V DC Power Supply is applied. K10 is maintained closed for 5 minutes by test box switches and the system rating load condition (35.8 A) is applied in order to stabilize the system. Following figure demonstrates that during overload condition-fault of the current drawn at J2, HOT BATT BUS CB is activated after the appropriate intervention time (43.7 seconds) based on the relevant temperature and following curve described in Figure 87.

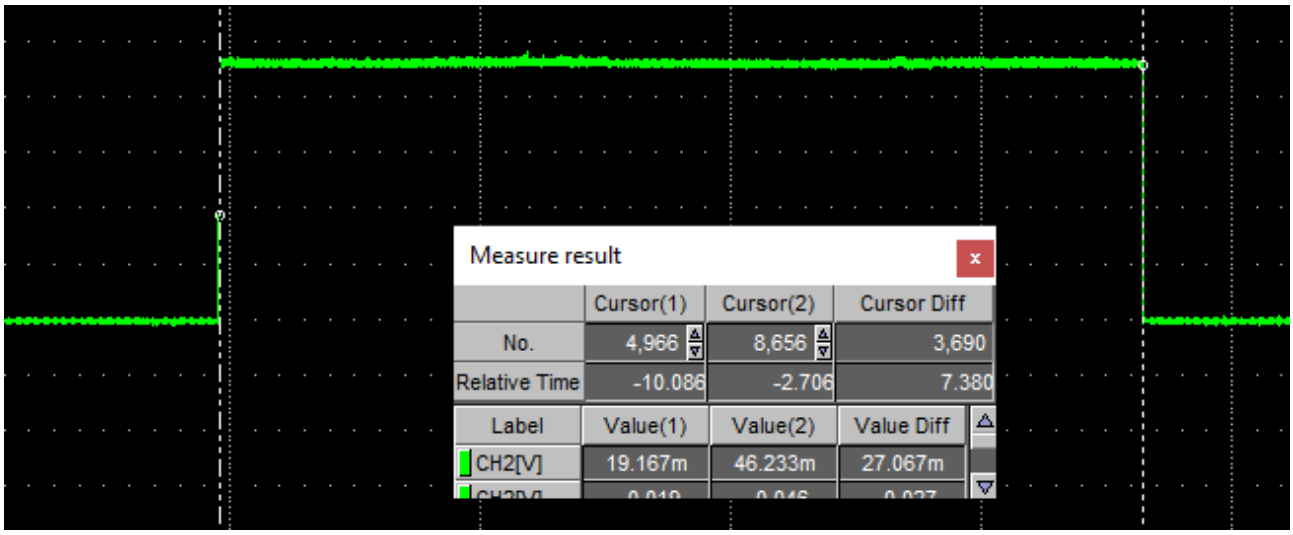



Figure 96: J2 connector – 50 A (7,38s).

After disconnecting the terminals and eliminating the applied loads from the system, L5 output power stud is connected to the DC load bank. Subsequently, the system rating load condition (35.8 A) is applied in order to stabilize the system. Then DC Load bank is adjusted in order to absorb 50 A. CB20 is activated after the appropriate intervention time (43.7 seconds) based on the relevant temperature and trip curve described in Figure 87.

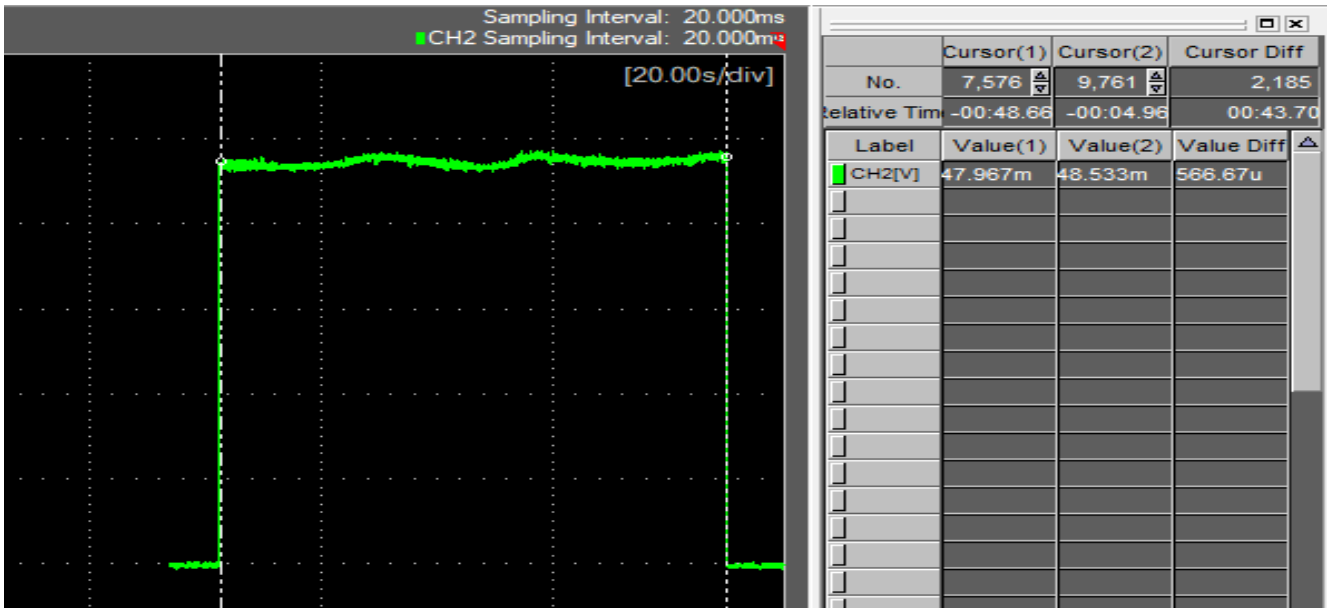



Figure 97: L5 power output stud - 50 A ( 43.7s).

Afterwards when the applied load has been removed and the terminals have been disconnected, DC load bank is connected L1 output power stud and the system rating load condition (35.8 A) is applied in order to stabilize the system for 5 minutes. Then DC load Bank is adjusted in order to absorb 300 A. T9 current protection sensor is triggered at the proper intervention time (9 seconds).

The figure below illustrates that the T9 current protection sensor is triggered at the appropriate moment of strong reliance on the temperature and trip curve described in Figure 87.

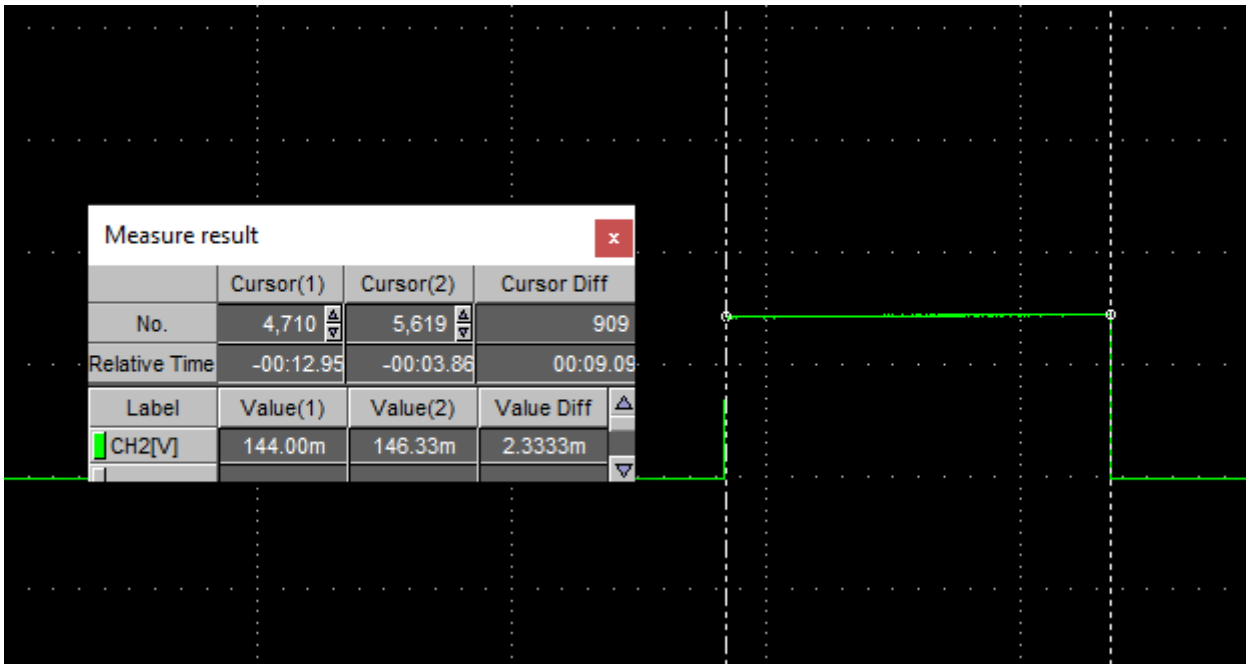



Figure 98: L1 output power stud – 300A (9sec).

After eliminating the applied load and disconnecting the terminals, K22 is closed using test box switches and the rating load condition (35.8 A) is applied for 5 minutes to stabilize the system. Besides, DC load is connected L2 output power stud and adjusted to absorb 200 A.

Following figure are verifying that RCCB4 activated in the appropriate intervention time- 41s according to the related current of the RCCB4 and according to trip curve in Figure 86.

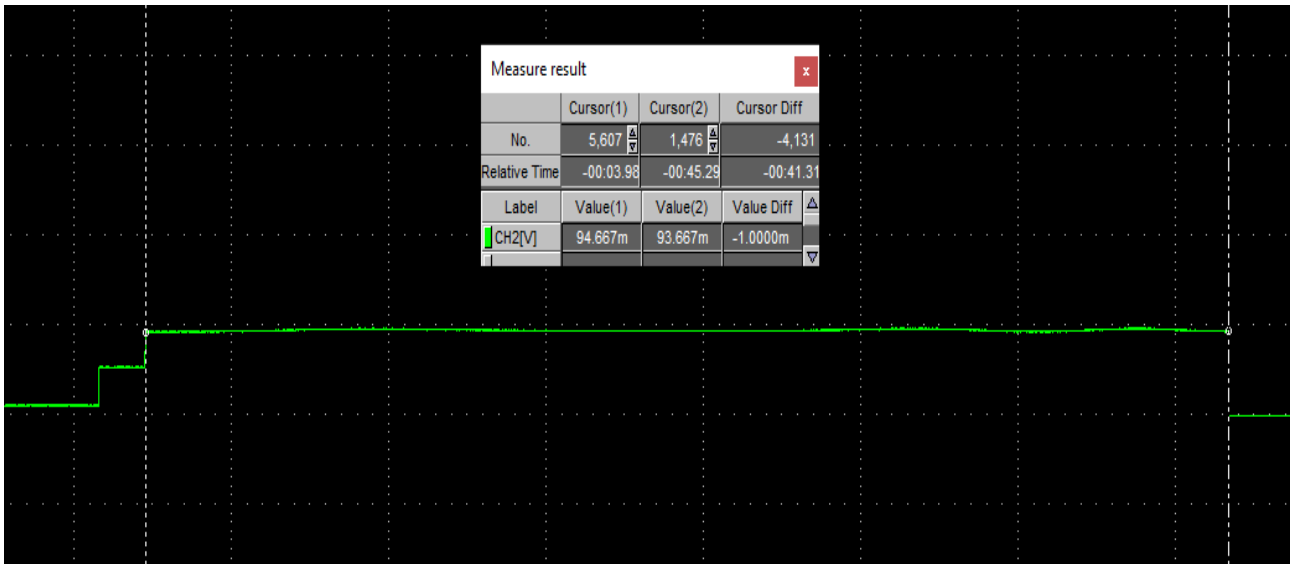



Figure 99: L2 output power stud - 200A (41 sec).

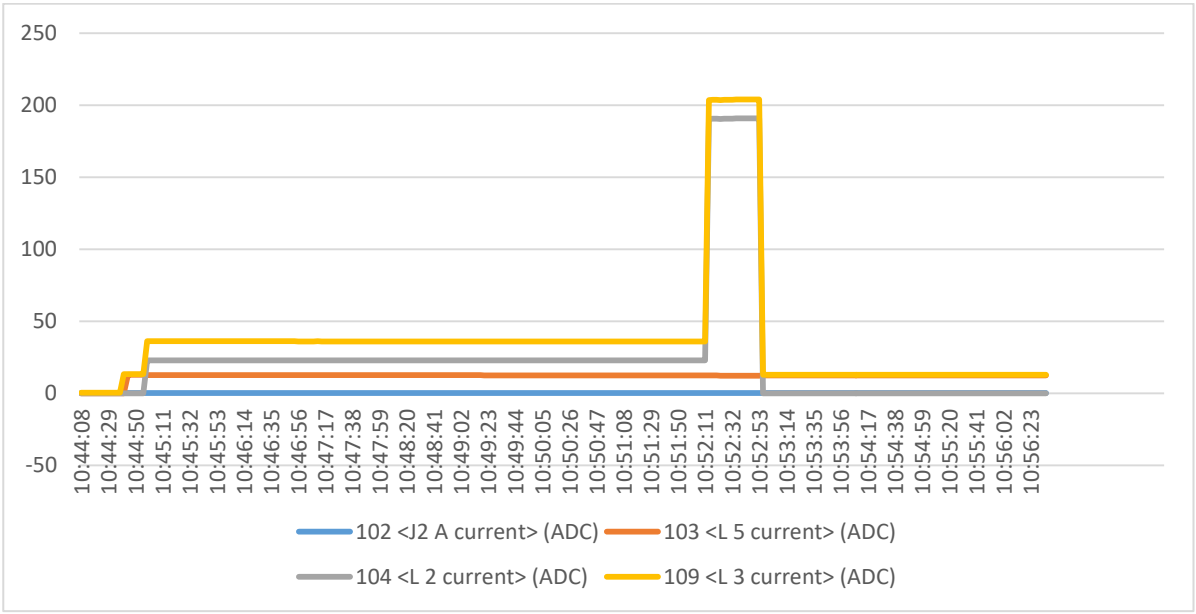



Figure 100: L2 output power stud is absorbing 200 A for 41s.

### 5.11.5 OVERLOAD - BATTERY DISCHARGE

In order to test battery discharge, the DC load position and DC Power Supply position are switched as a starting point of overload (BATTERY DISCHARGE).
L1 input stud is connected to positive terminal of DC power supply and DC load bank is connected to L3 power output stud. K10 and K22 are maintained closed for 5 minutes by test box switches and the system rating load condition (38.2 A) is applied in order to stabilize the system with L1 as an input and L3 loaded with 25.5 A.

After this procedure, the DC load bank is set to 400 A. According to the test procedure, 200 A load was required, however the trip curve required 400 A load to activate the protection. Because 200 A is insufficient to activate on protection. Thus the current drawn at L3 is more than the rated current of the T9 current protection sensor, T9 is activated at the appropriate time of intervention (17.2 s) based on the temperature and discharge trip curve in Figure 88.

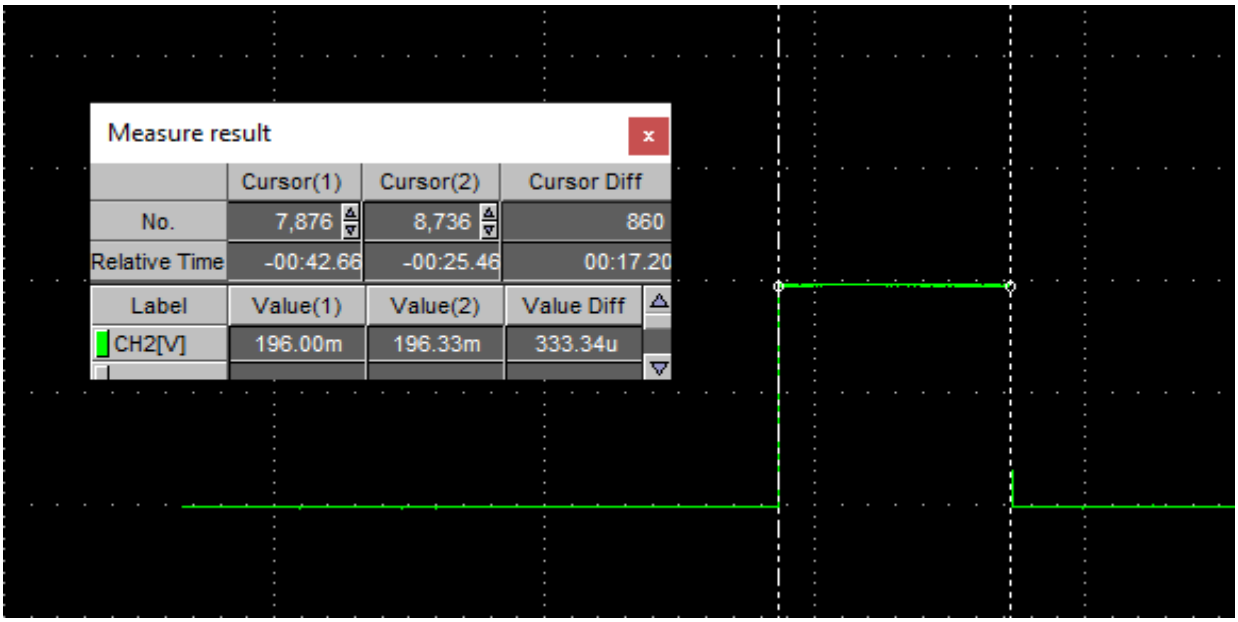



Figure 101: L3 stud is loaded with 400A (17.2 s).

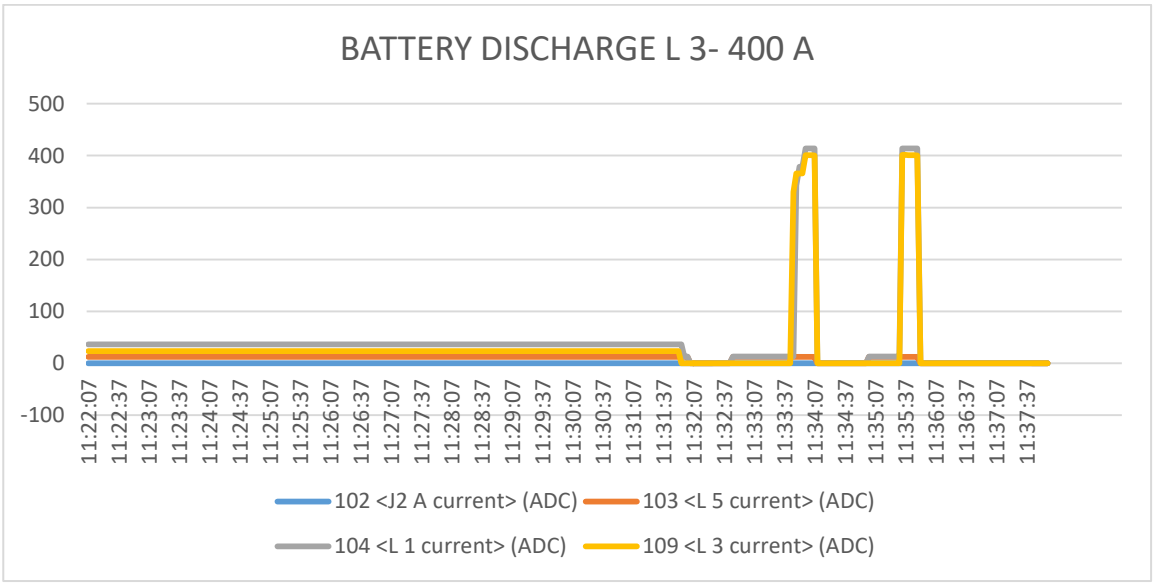



Figure 102: Battery discharge -400A (17.2 sec).

## 5.12 EXTERNAL POWER MONITOR (EPM)

External Power Monitor (EPM) inside the BATTERY monitors the external power at the PDP inputs and correspondingly provides the output latching voltage for the external power coil contactor if the voltage is within the permissible limits. By connecting DC Power Source to BATTERY External Power Unit is simulated and input voltage for overvoltage and reverse polarity are verified.

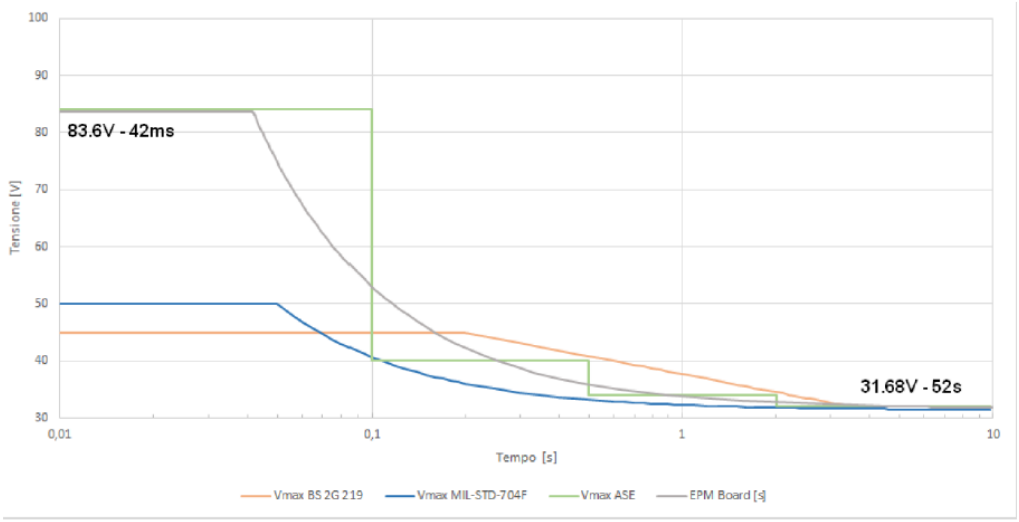



Figure 103: External Power Overvoltage trip curve.

### 5.12.1 EPM TEST PROCEDURES

**PRE-REQUISITES**

1. Ensure the EUT has passed the pre-test ATP
2. Ensure that the EUT and all the switches are in the starting state
3. Perform test setup operations as detailed in

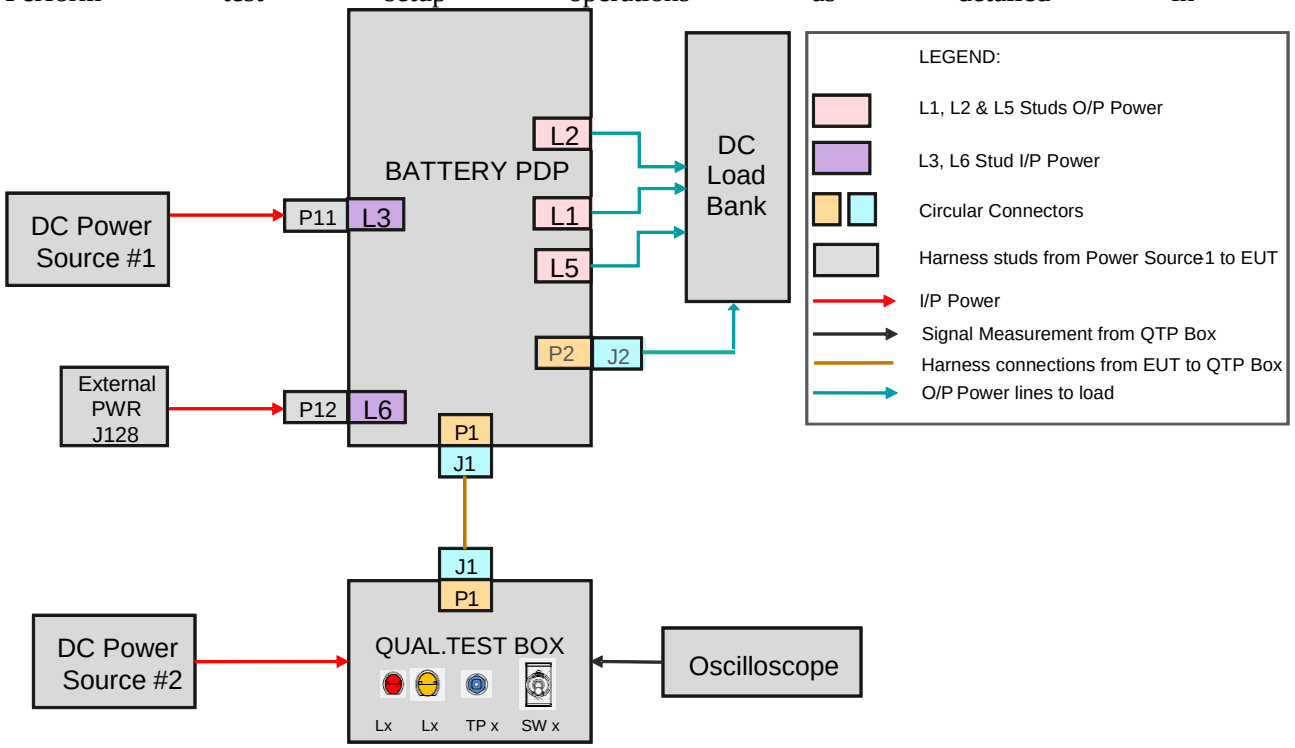



Figure 84.

4. Set DC Power Supply to give 28V±0.5V voltage

5. Set programmable External Power Supply to give the following steps:

- STEP 1: 28V±0.5V input voltage for 5min
- STEP 2: 32V±0.5V input voltage for 1min
- STEP 3: 35V±0.5V input voltage for 10s
- STEP 4: 38V±0.5V input voltage for 1s
- STEP 5: 42V±0.5V input voltage for 0.8s
- STEP 6: 50V±0.5V input voltage for 0.5s
- STEP 7: 58V±0.5V input voltage for 0.2s
- STEP 8: 66V±0.5V input voltage for 100ms
- STEP 9: 74V±0.5V input voltage for 70ms
- STEP 10: 83V±0.5V input voltage for 50ms.

6. Connect positive terminal of DC Power Supply #1 to the input L3 stud
7. Connect positive terminal of External Power Supply to the input L6 stud

**INITIAL OPERATIONS**

8. Set the data-logger to acquire the system parameters defined in § 5.10.6
9. Verify K9 External Power contactor is in closed position
10. Set the oscilloscope in order to trigger to a positive slope with a 5s-time duration

**TEST CORE – EPM**

11. Start recording parameters with the data-logger
12. Start the acquisition of the waveform by means of the oscilloscope
13. Turn ON the DC Power Supply #1
14. Apply STEP#1
15. Verify that the system is ONLINE (related switch and led on test box)
16. Verify K9 contactor is closed after turning on of DC Power Supply and External Power Supply
17. Reset the system
18. Maintain rating voltage condition for 5min in order to stabilize the system
19. Apply STEP#2
20. Verify that K9 contactor opens in the right time of intervention according to the related temperature and following curve described in Figure 103
21. Apply test points 14, 15, 16 and 18
22. Apply STEP#3
23. Verify that K9 contactor opens in the right time of intervention according to the related temperature and following curve described in Figure 103
24. Apply test points 14, 15, 16 and 18
25. Apply STEP#4
26. Verify that K9 contactor opens in the right time of intervention according to the related temperature and following curve described in Figure 103
27. Apply test points 14, 15, 16 and 18
28. Apply STEP#5
29. Verify that K9 contactor opens in the right time of intervention according to the related temperature and following curve described in Figure 103
30. Apply test points 14, 15, 16 and 18
31. Apply STEP#6
32. Verify that K9 contactor opens in the right time of intervention according to the related temperature and following curve described in Figure 103
33. Apply test points 14, 15, 16 and 18
34. Apply STEP#7
35. Verify that K9 contactor opens in the right time of intervention according to the related temperature and following curve described in Figure 103
36. Apply test points 14, 15, 16 and 18
37. Apply STEP#8
38. Verify that K9 contactor opens in the right time of intervention according to the related temperature and following curve described in Figure 103

39. Apply test points 14, 15, 16 and 18
40. Apply STEP#9
41. Verify that K9 contactor opens in the right time of intervention according to the related temperature and following curve described in Figure 103
42. Apply test points 14, 15, 16 and 18
43. Apply STEP#10
44. Verify that K9 contactor opens in the right time of intervention according to the related temperature and following curve described in Figure 103
45. Apply test points 14, 15, 16 and 18

**FINAL OPERATIONS**

46. Stop and save data-logger acquisition
47. Open all contactors
48. Turn OFF the DC Power Supply and the programmable External Power Supply
49. Verify 0V at output studs.

**ACCEPTANCE TEST CRITERIA**

- No unexpected contactor nor relay trip shall occur during Continuous capacity test.
- No unexpected over-temperature condition in a Continuous capacity test.
- No unexpected contactor opening damage shall occur during or after overload 5 seconds.

### 5.12.2 EPM TEST RESULTS

The purpose of this results are to describe the correct operation of the External Power Monitor circuit inside the DC BATTERY PDP. The EPM logic board has been stressed in order to verify its correct operation.

If the voltage is within the permissible limits, the EPM inside the Battery PDP will monitor the external power at the PDP inputs and provide the output latching voltage for the external power coil contactor. The EPM will open the External Power Contactor and latch the alarm condition when an overvoltage condition is detected. To unlatch this alert, the EPM will have a RESET function. The RESET function will be achieved using a Ground signal pulse provided by an external source.

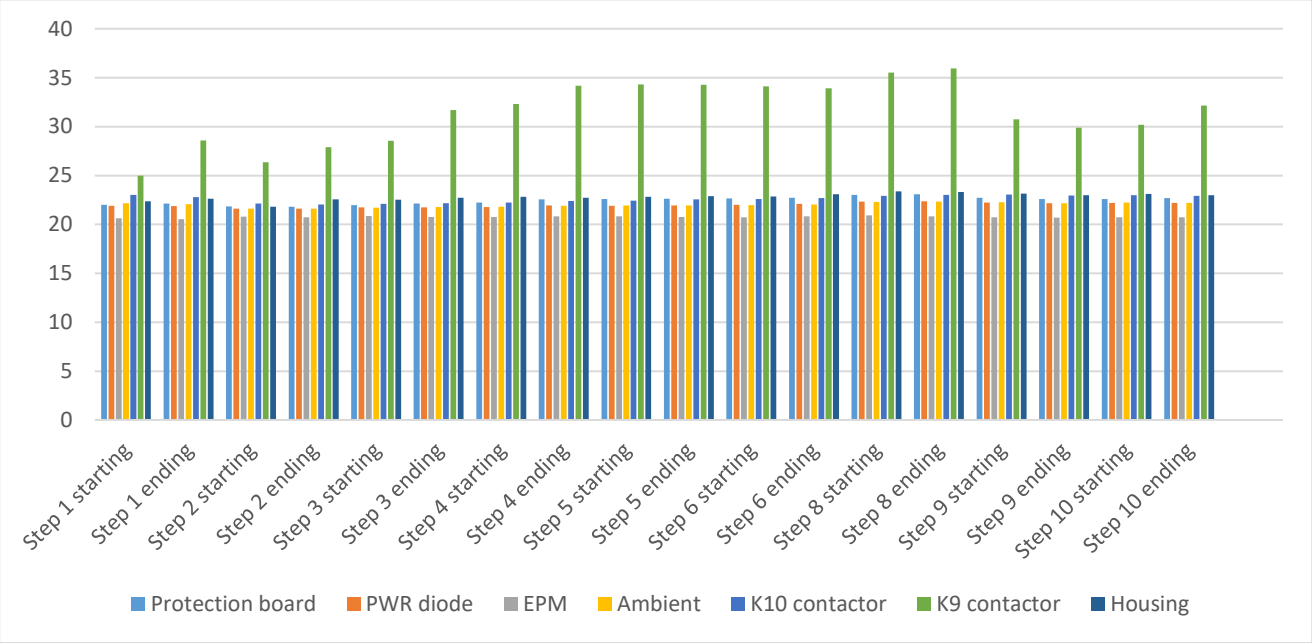



Figure 104: Changes in temperature from STEP 1 to STEP 10.

L3 input stud is connected to the positive terminal of the DC Power Supply, and L6 input stud is connected to the positive terminal of the External Power Supply. The DC Power Supply is set to 28 volts, while the Programmable External Power Supply is configured to the following:

- STEP 1: 28V±0.5V input voltage for 5min;
- STEP 2: 32V±0.5V input voltage for 1min;
- STEP 3: 35V±0.5V input voltage for 10s;
- STEP 4: 38V±0.5V input voltage for 1s;
- STEP 5: 42V±0.5V input voltage for 0.8s;
- STEP 6: 50V±0.5V input voltage for 0.5s;
- STEP 7: 58V±0.5V input voltage for 0.2s;
- STEP 8: 66V±0.5V input voltage for 100ms;
- STEP 9: 74V±0.5V input voltage for 70ms;
- STEP 10: 83V±0.5V input voltage for 50ms.

Table 58: External Power Overvoltage trip curve intervention time.

| Steps | Input voltage | Applying time | Time of intervention |
|---|---|---|---|
| **1** | **28V** | **5 min** | **No intervention** |
| **2** | **32V** | **1 min** | **6 s** |
| **3** | **35V** | **10 s** | **640 ms** |
| **4** | **38V** | **1 s** | **368 ms** |
| **5** | **42V** | **0.8 s** | **248 ms** |
| **6** | **50V** | **0.5 s** | **163 ms** |
| **7** | **58V** | **0.2** | **128 ms** |
| **8** | **66V** | **100 ms** | **112 ms** |
| **9** | **74V** | **70 ms** | **106 ms** |
| **10** | **83V** | **50 ms** | **98 ms** |

The figure shows the maximum voltage threshold proposal to implement for the EPM Board.
The proposed curve, in brown, represents an intermediate value between the values imposed by the MIL-STD-704F (light blue color) and BS 2G 219 (orange color).

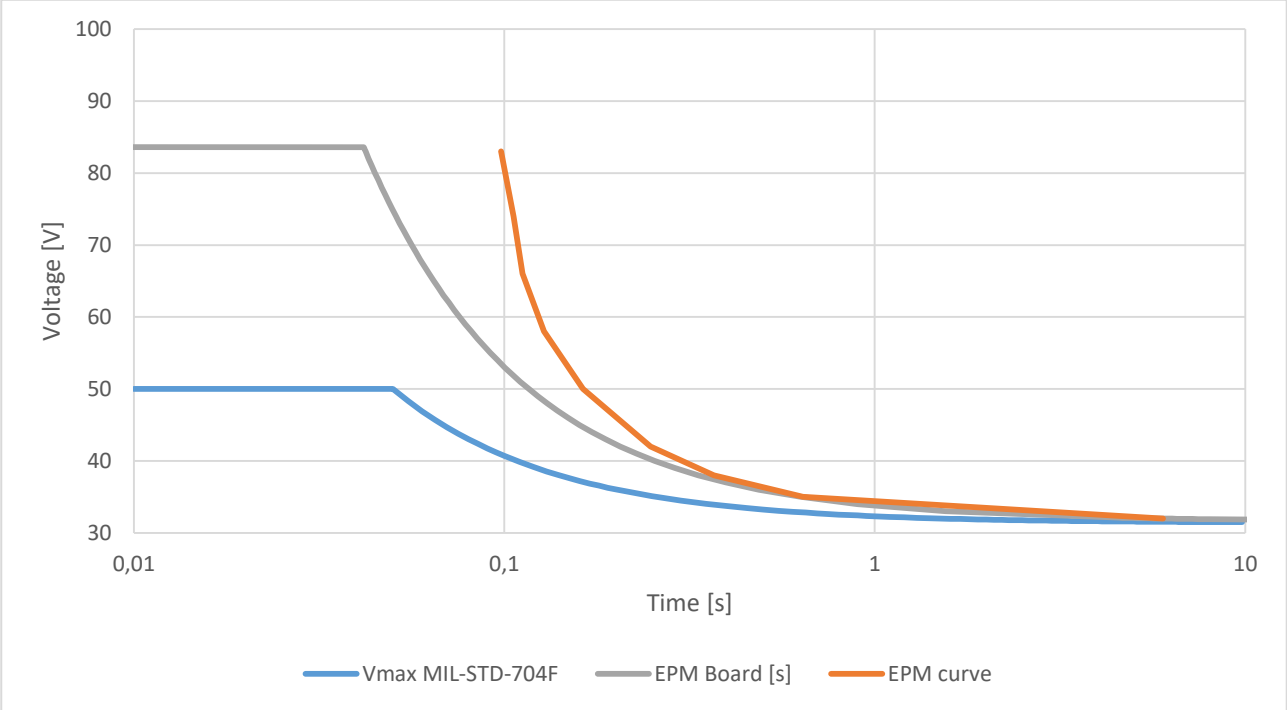



Figure 105: EPM trip curve.

The grey curve in

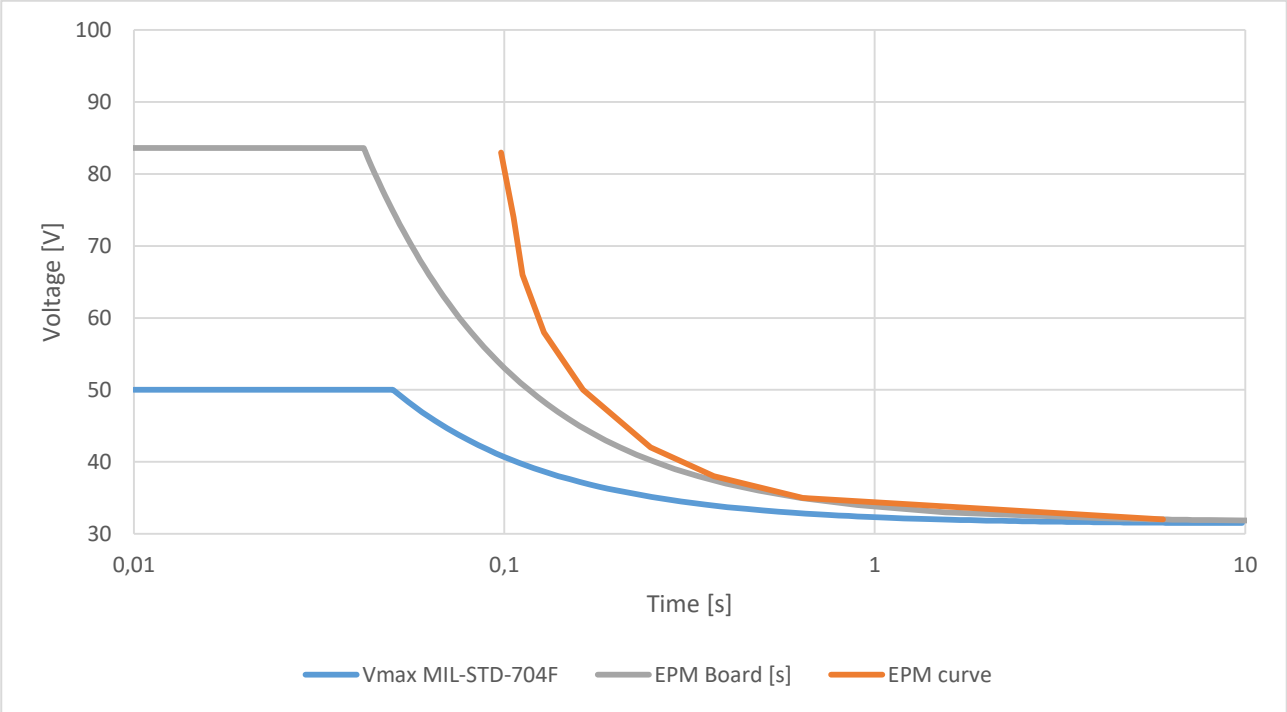



Figure 105 is the intervention curve required by technical specification. As can be seen, the measured intervention curve is slower than the requirement, due to the opening time of the contactor with TVS protections for lightning. The maximum difference is at 83V, where it can be seen that the output voltage is removed after 0.098s instead of 0.042s required (DO-160G section 16, 16.6.2.4 Abnormal Surge Voltage DC).

All the required parameters have been monitored and recorded by means of data logger and oscilloscope. Their trends in time are reported in following figures respectively. According to the following figures all the parameters behavior is maintained correctly, no trip occurs in un-proper manner during **STEP 1**.

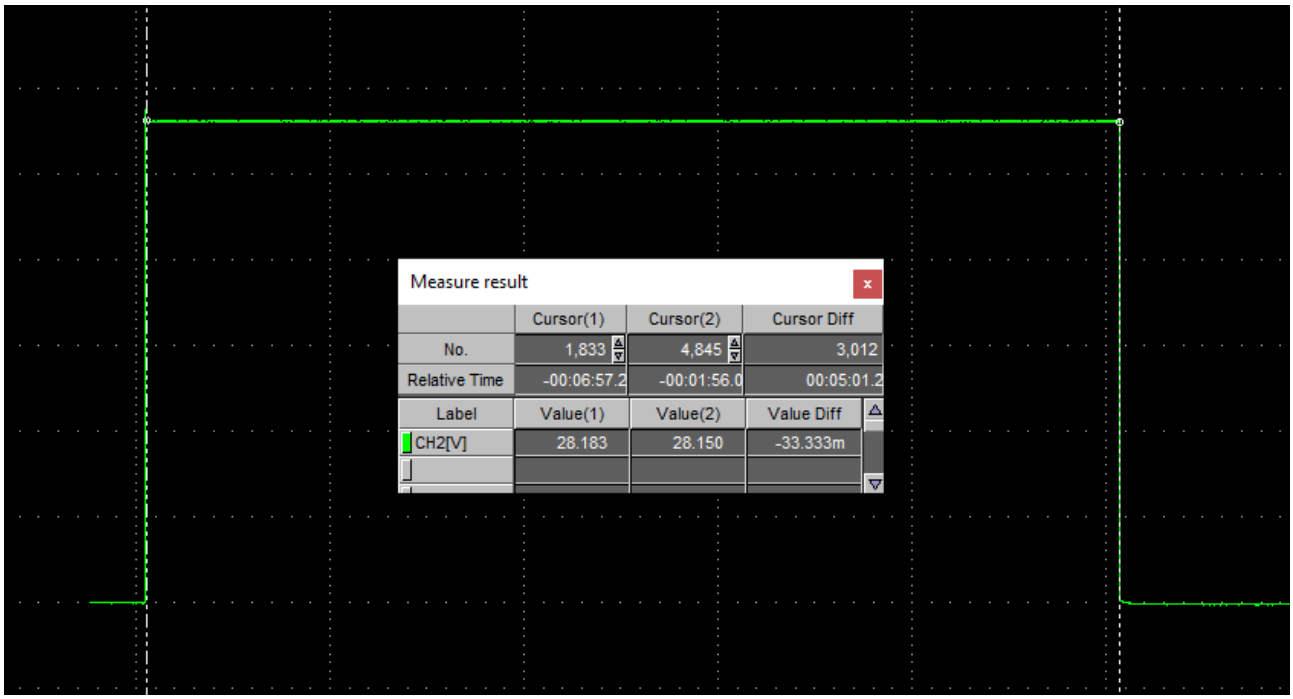



Figure 106: Step 1 result from oscilloscope

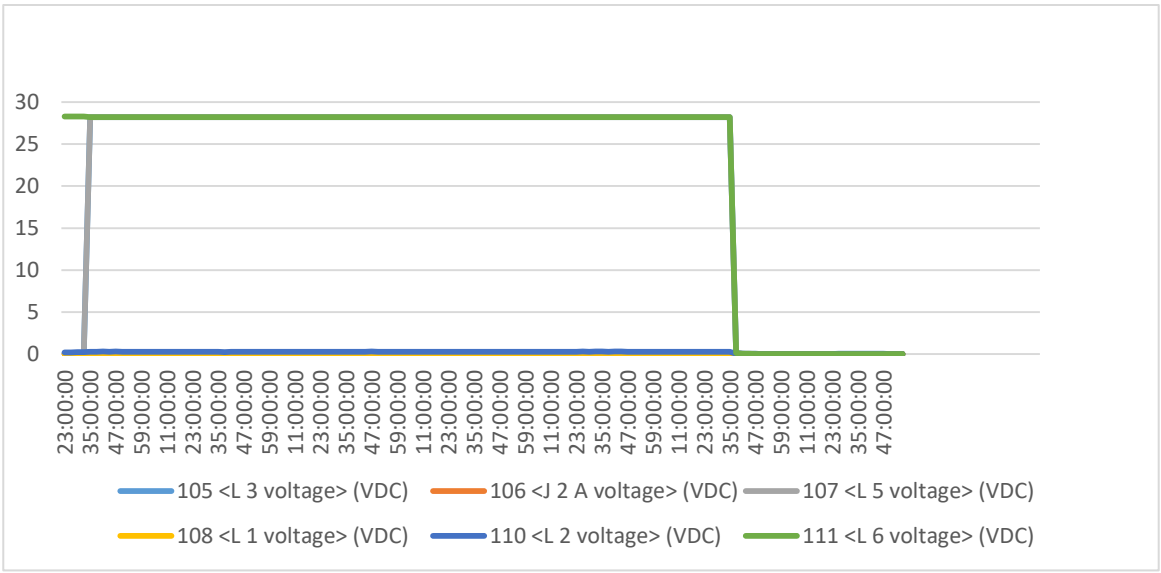



Figure 107: STEP 1-28 V for 5 minutes.

The Programmable External Power Supply is adjusted to give 32V±0.5V input voltage for 1min. After stabilizing the system, keep the rating condition in order for 5 minutes.
During **STEP 2**, K 9 contactor opened at the appropriate time of intervention **(6 s)** based on the temperature and trip curve in Figure 103.

After stabilizing the system, keep the rating condition in order for 5 minutes. The Programmable External Power Supply is adjusted to give 35V±0.5V input voltage for ten seconds.

During **STEP 3**, K 9 contactor opened at the appropriate time of intervention **(640 milliseconds)** based on the temperature and trip curve in Figure 103.

After keeping the rating condition in order for 5 minutes to stabilize the system, **STEP 4** is applied-programmable external power supply is configured to supply 38V input voltage for one second.
As a result, K9 contactor is opened at the appropriate time of intervention **(368 milliseconds)** based on the temperature and following curve depicted in Figure 103.

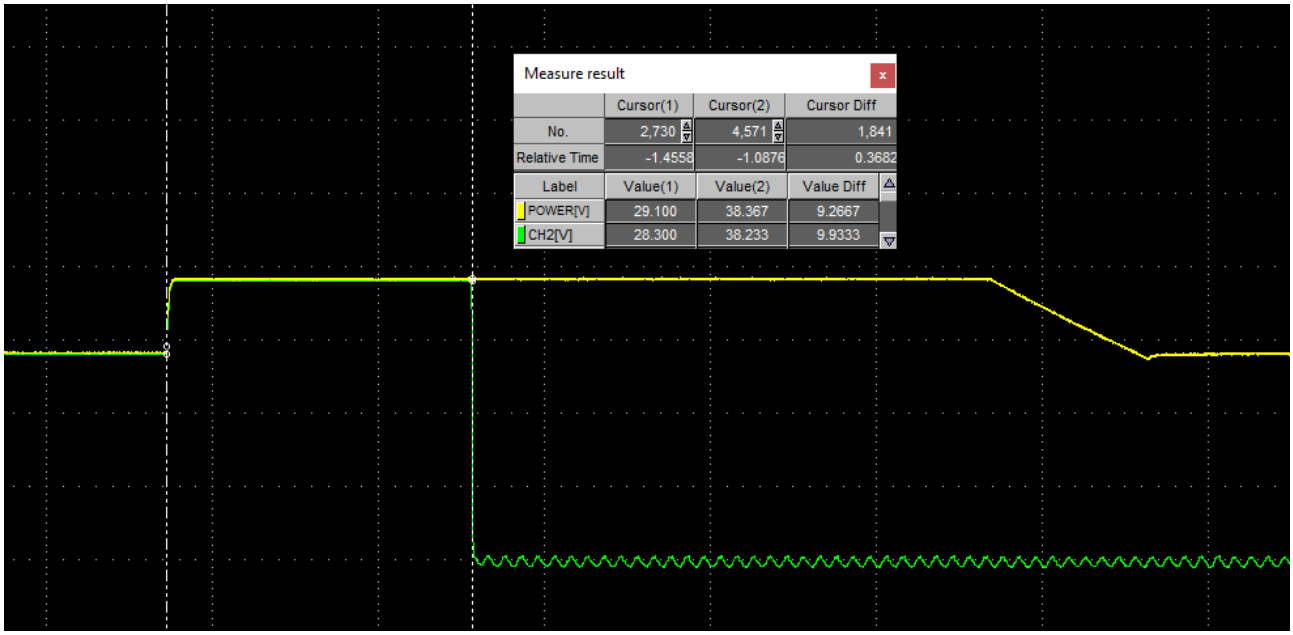


Figure 108: Step 4 results from oscilloscope

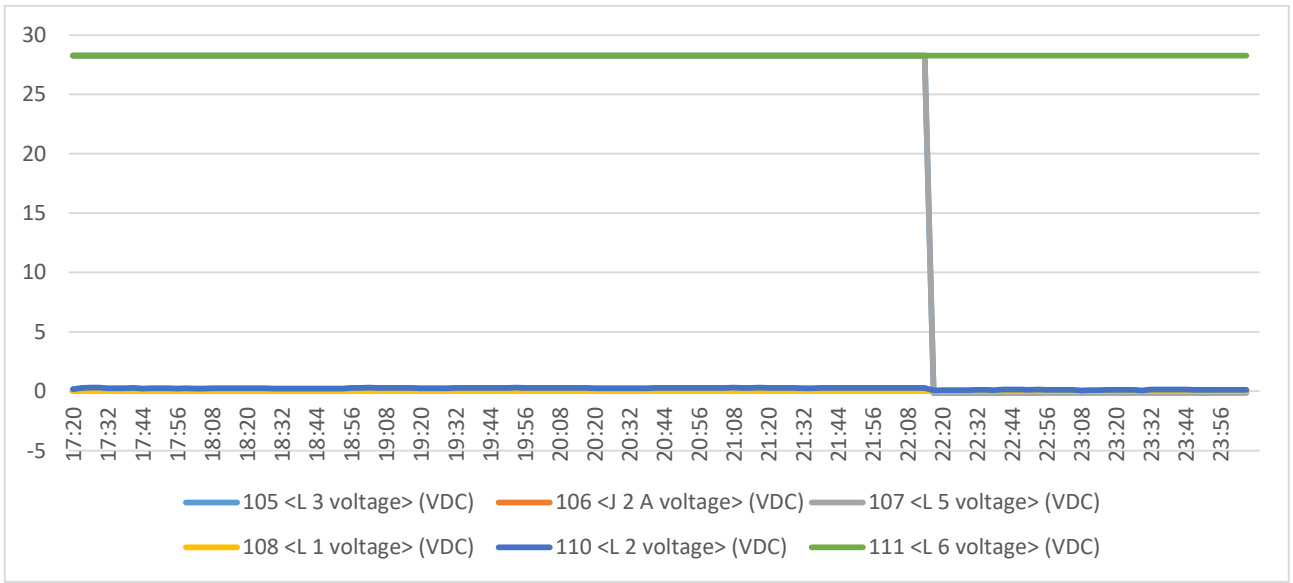


Figure 109: STEP 4 - 38V input voltage for 1s.

After stabilizing the system, keep the rating condition in order for 5 minutes. The Programmable External Power Supply is adjusted to give 42V±0.5V input voltage for 800 milliseconds. During **STEP 5**, K 9 contactor opened at the appropriate time of intervention – **248 milliseconds** based on the temperature and trip curve in Figure 103.

The 50V input voltage of The Programmable External Power Supply has been set for 0,5 seconds after stabilizing the system, keep the rating condition in order for 5 minutes.

**STEP 6**: The K 9 contactor activated at the appropriate time of intervention-**163 milliseconds** based on the temperature and trip curve in Figure 103.After holding the rating condition in action for 5 minutes to stabilize the system, the 58V input voltage of the Programmable External Power Supply is set for 0,2 seconds.

**STEP 7**: Based on the temperature and trip curve in Figure 103, the K 9 contactor opened at the appropriate time of intervention-**128 milliseconds**. After keeping the rating condition in order for 5 minutes to stabilize the system, the Programmable External Power Supply is programmed to provide 74V input voltage for 70milliseconds. During **STEP 9**, the K 9 contactor opened at the appropriate period of intervention- **106 milliseconds** based on the temperature and trip curve in Figure 103. After 5 minutes of keeping the rating condition in order to stabilize the system, for 50 milliseconds, the Programmable External Power Supply is set to provide 83V input voltage. Based on the temperature and trip curve in Figure 103, the K 9 contactor opened at the appropriate time of intervention- **98 milliseconds** during **STEP 10**.


Figure 110: Step 10 results from oscilloscope.

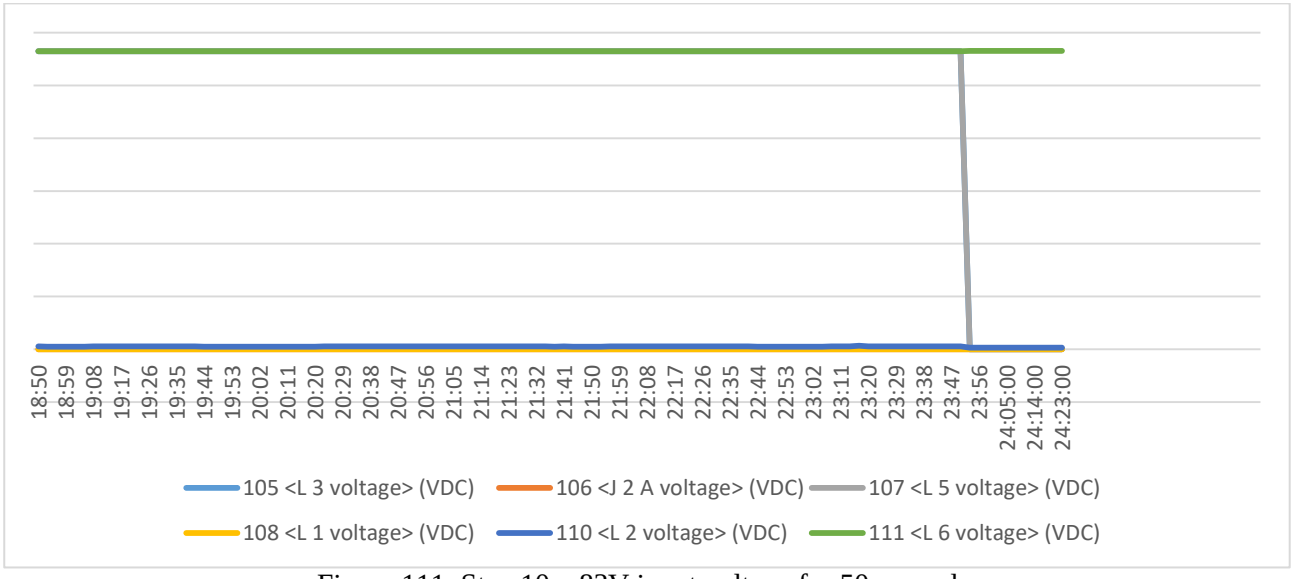



Figure 111: Step 10 – 83V input voltage for 50 seconds.

## 5.13 CONCLUSION FOR BATTERY PDP PERFORMANCE TEST

During the Performance Test session, no out-of-limit values were recorded. With respect to the present absorption level, the recorded data have revealed no bad, erroneous, or out-of-limit situation.

Neither an unexpected contactor nor a relay trip occurred during the Continuous capacity test. In the continuous capacity test, an unanticipated over-temperature event never occurred. During or after the 5 second overload, no unexpected contactor opening or damage occurred. The examination of the RCCB T9 trip curves in both battery CHARGE and DISCHARGE operations was completed well, and the recorded results show that the element responds correctly to all tested loads. No trip occurred before the time limit, the current sensor T9 interfered at the appropriate time intervals following the prescribed trip curve and all current thresholds were validated.

The EPM logic board was strained as a last test to ensure proper operation. According to all recorded parameters, the EPM logic board behaved lightly slower than the requirement, due to the time taken by the contactor to open, therefore there are some out of limits.

All of these evidences, as well as the absence of any damage to the board's elements, have been validated by the final ATP.

In this way DC BATTERY Performance requirements have been assessed with out of limits for the EPM curve only.

## 5.14 QUALIFICATION TEST REPORTS (SOF ENVIRONMENTAL)

### 5.14.1 VIBRATION AND ACCELERATION TEST ON DC PDP

This Test Report details results of the vibration and acceleration tests carried out in order to reach qualification performance of the DC PDP 1 Power Distribution Panel

Table 59: Test results for vibration and acceleration tests on DC PDP 1

| Test Type | Test Result (PASS/FAIL) |
|---|---|
| Vibration | PASS |
| Operational shock | PASS |
| Crash safety impulse | PASS |
| Crash safety sustained test | PASS |

### 5.14.2 TEST SEQUENCE

Tests are planned to be carried out according to the below sequence. The only constraint is about the first and the last step (pre-test and post-test ATPs).

**Initial:**

1. Pre-test ATP on EUT

**Functional Tests:**

2. Fixture resonance survey
3. Resonance search
4. Endurance vibration
5. Eventual resonance dwell
6. Resonance search
7. Operational shocks
8. Resonance search
9. Crash safety impulse
10. Resonance search

**Final:**

1. Post-test ATP
2. Crash safety sustained
3. Post-test ATP

↓↓↓

**“SOF Test on the DC EPDS” session was a successful.**

#### 5.14.2.1 Initial Research Resonance for X axis

Two resonance searches will be conducted for each of the tested axes prior to and following the vibration test for the following reasons:

- To determine the EUT's resonance frequencies (along each axis);
- To detect mechanical damage to the EUT early on, such as cracks or loosening, by detecting significant shift in the resonance response between pre- and post-vibration resonance searches.

The resonance search will be conducted using a sinusoidal scan between 10Hz and 500Hz at a maximum sweep rate of 1octave/minute. The search must be conducted along three mutually perpendicular axes, beginning with the Z axis.

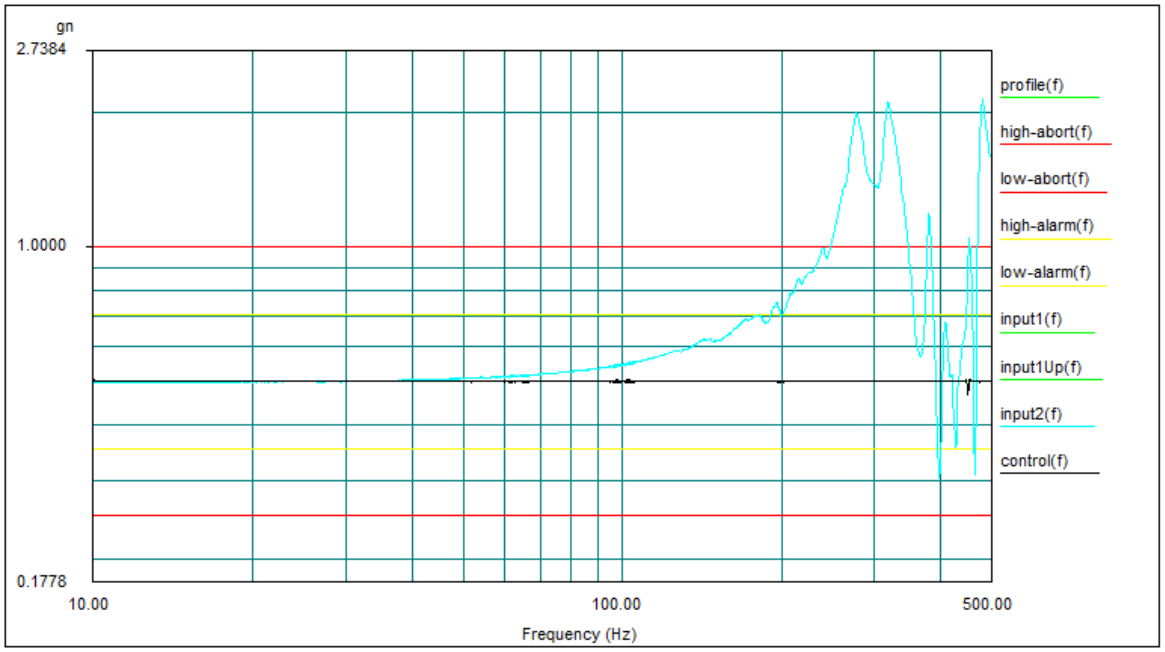



Figure 112: X AXIS RESONANCE RESEARCH INITIAL

#### *5.14.2.2 Endurance and Dwell Test for X axis*

Following the initial research, a resonance vibration test at the endurance level for 4 hours per axis (12 hours total) is performed.

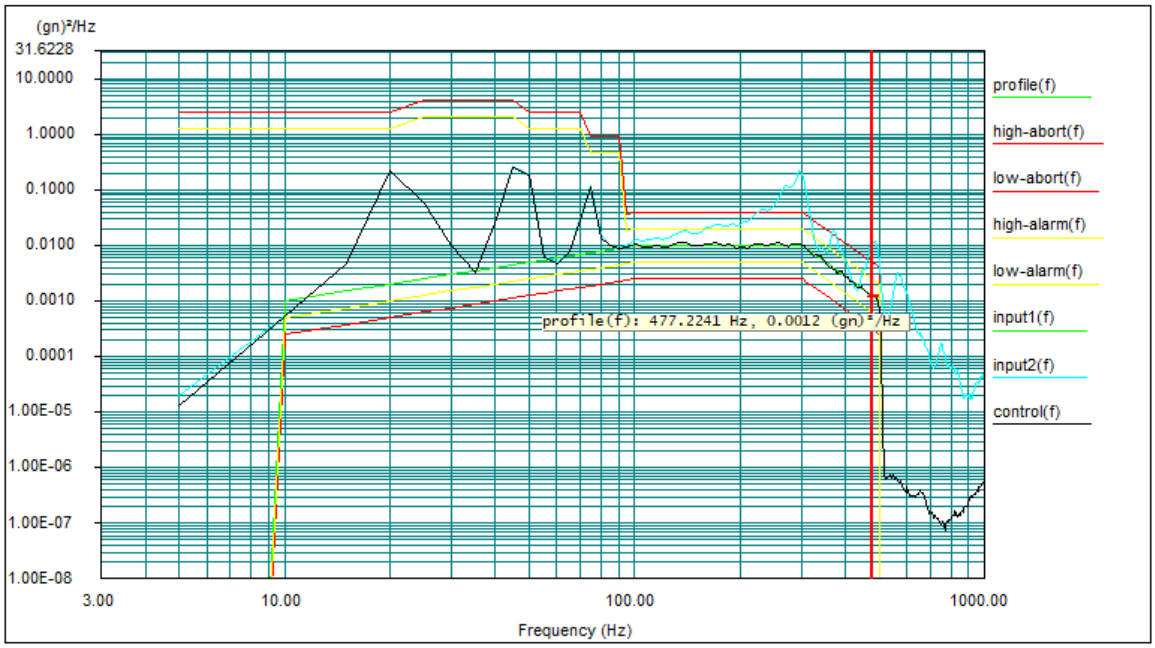



Figure 113: X AXIS ENDURANCE FOR 4 HOURS

At the end of the 4-hour endurance test, one or more (if necessary) resonance dwells are applied. Each dwell test must last 30 minutes.

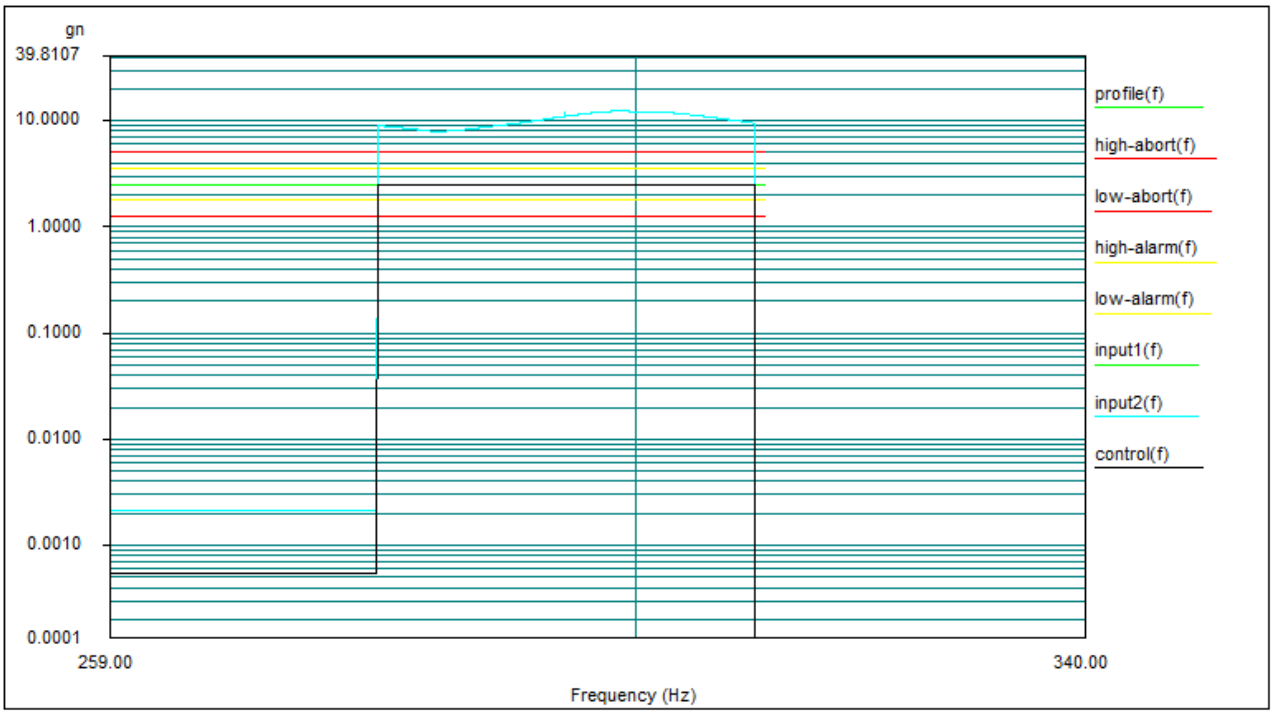



Figure 114: X AXIS DWELL AT 294 HZ

### 5.14.2.3 Operational Shock Test for X axis

Shock testing according to **MIL-STD 810, Method 516** procedures is intended to test products while they are in operation to see if any functional problems occur and to determine if they survive without damage. Shock testing was also carried out in accordance with RTCA DO-160G Section 7, Category A. [4].

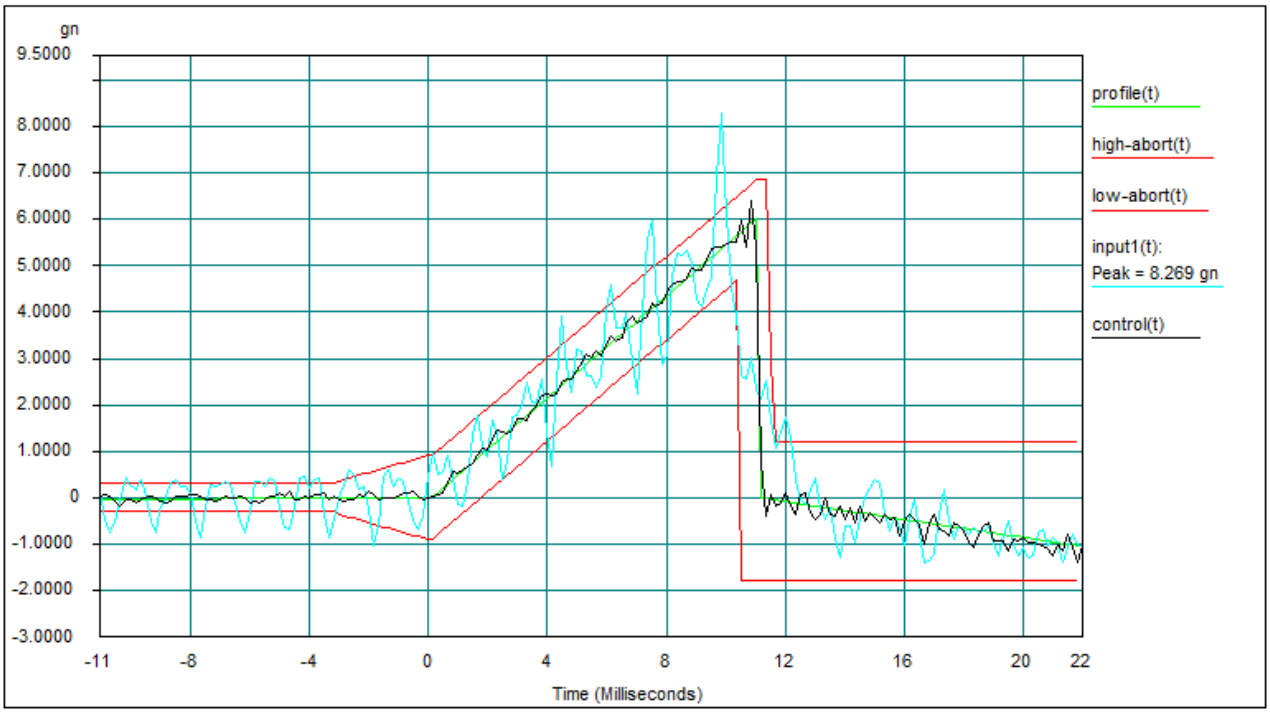



Figure 115: X AXIS FUNCTIONAL SHOCK 6G POSITIVE

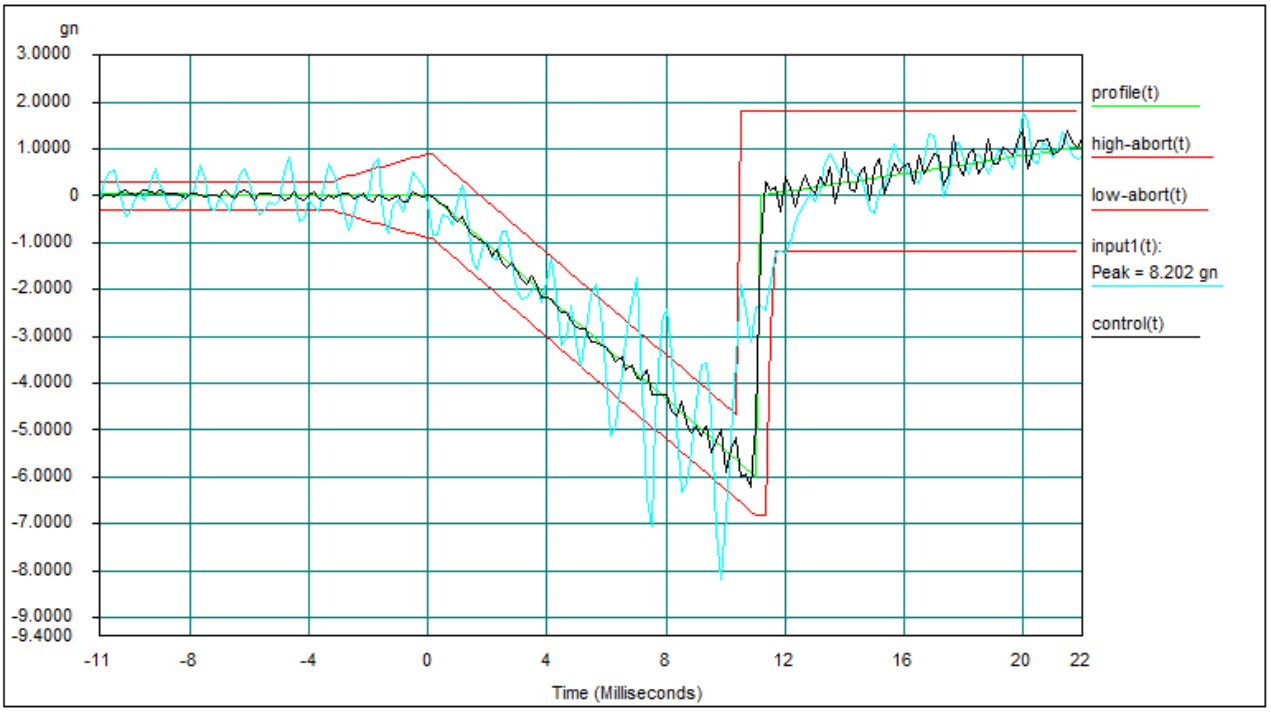



Figure 116: X AXIS FUNCTIONAL SHOCK 6G NEGATIVE

**Crash Safety Impulse Test for X axis:**

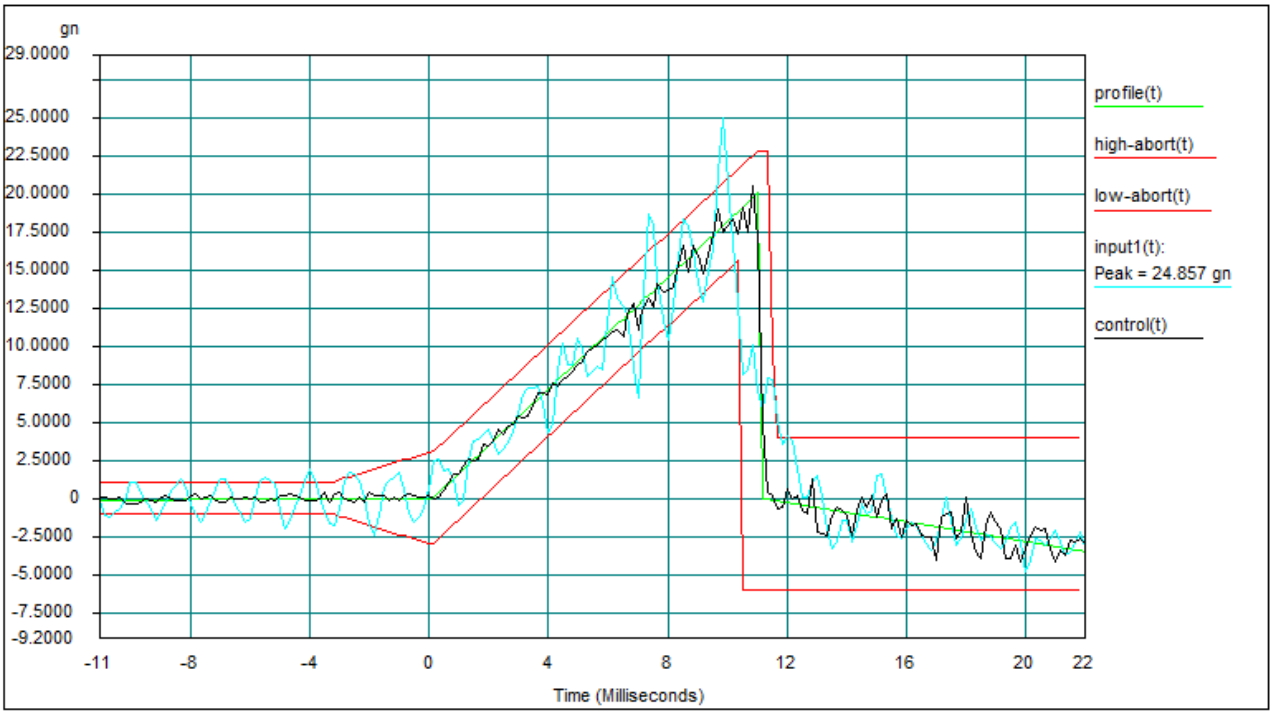



Figure 117: X AXIS FUNCTIONAL SHOCK 20G POSITIVE

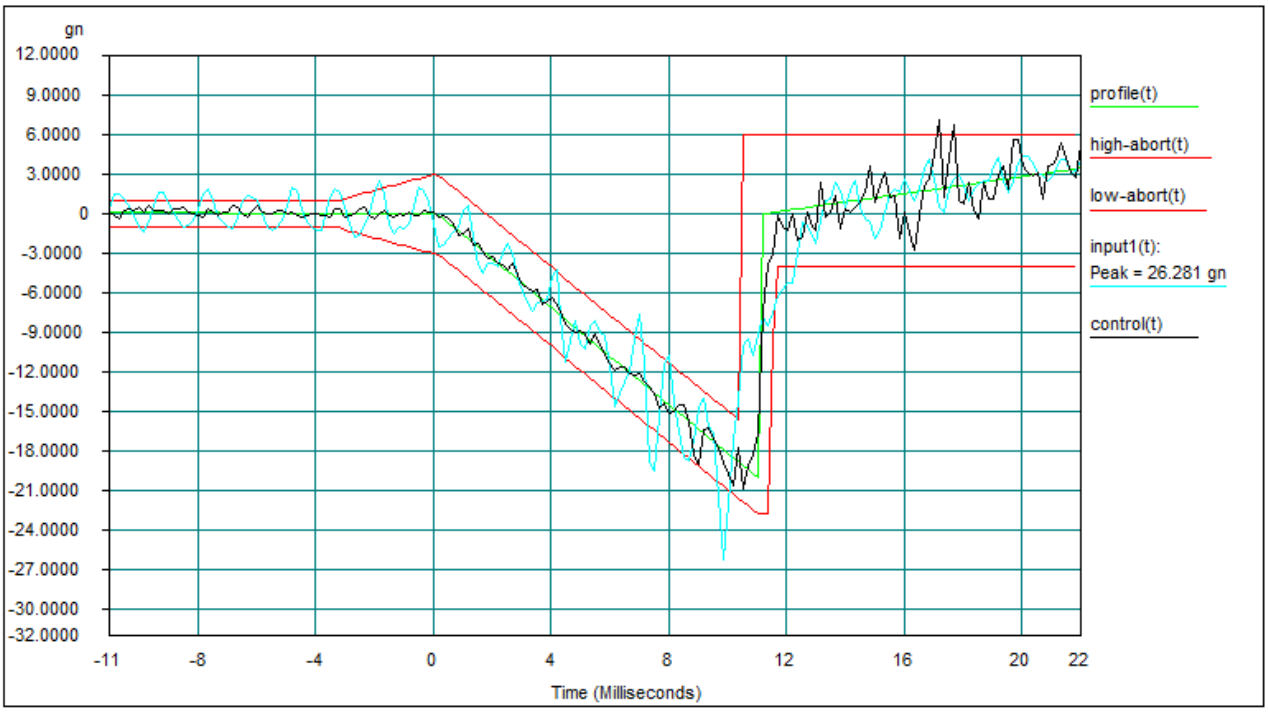



Figure 118: X AXIS FUNCTIONAL SHOCK 20G NEGATIVE

#### 5.14.2.4 Final Research Resonance for X axis

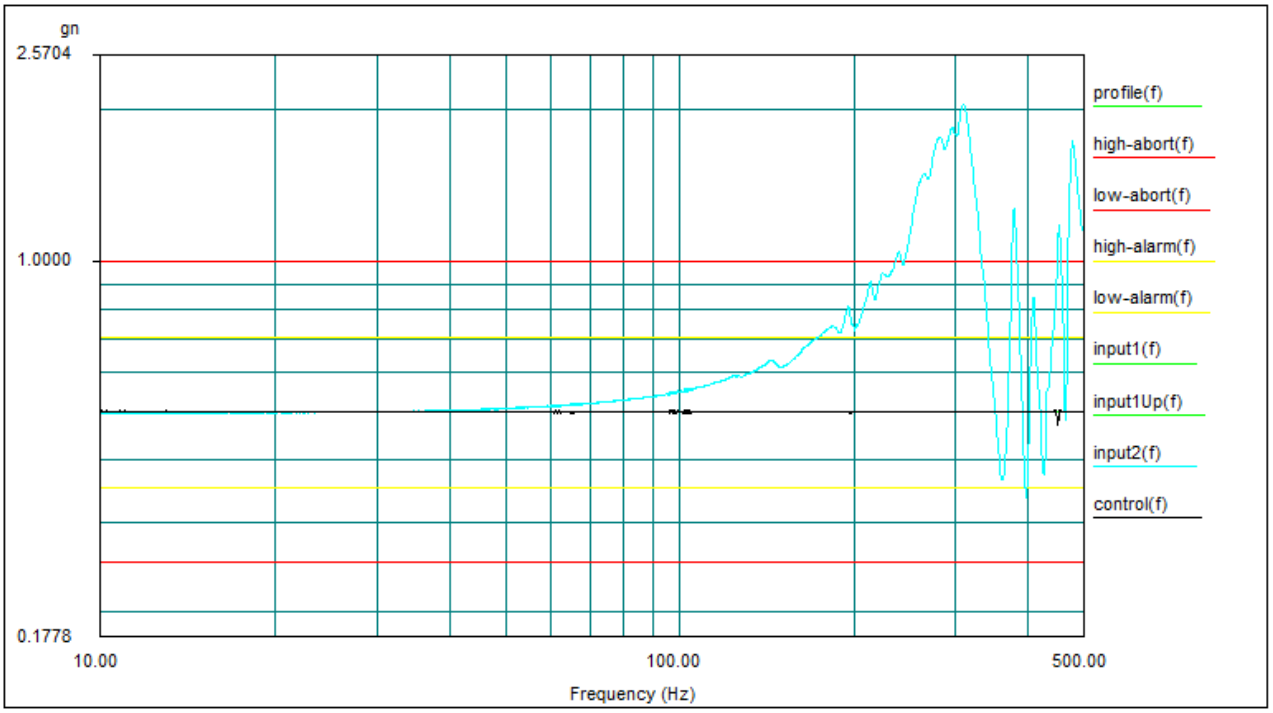



Figure 119: X AXIS FINAL RESONANCE RESEARCH

By comparing the initial and final research resonances for the X axis, we can easily observe that there are no significant differences in frequencies and amplitudes in between pre-vibration and post-vibration resonance searches.

### 5.14.2.5 Crash safety sustained (acceleration) test

The EUT must continue to perform within performance standards after being exposed to shocks experienced during normal aircraft operations (Operational Shocks) and must not detach from the main structure during an emergency landing (Crash Safety).

According to the procedure **RTCA DO-160G, Section 7, Category B** (equipment tested for standard shock and crash safety), each running EUT is examined in non-operating conditions at the same level of stress along each direction, with an acceleration peak of 20g sustained for a minimum of 5s in each direction for each axis with a non-operating EUT (total of 6 accelerations per EUT).

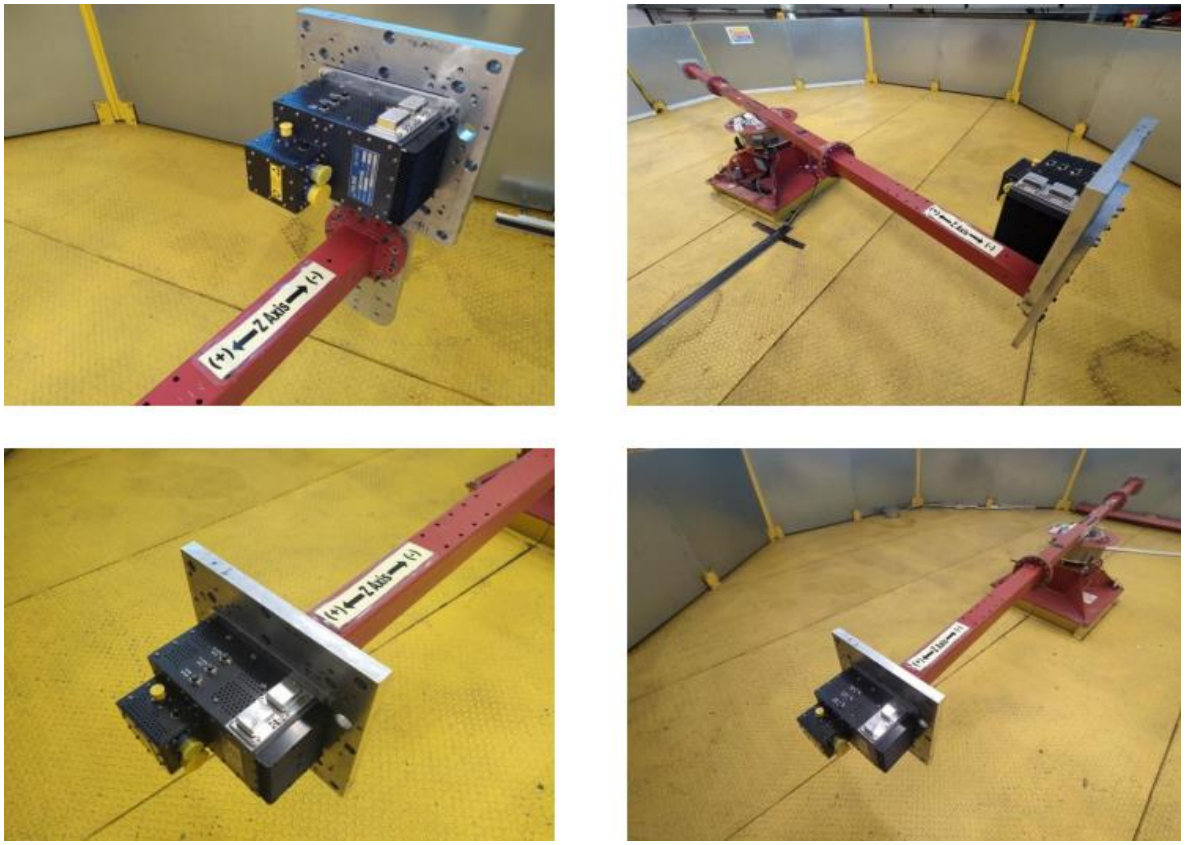



Figure 120: ACCELERATION TEST SETUP FOR Z AXIS

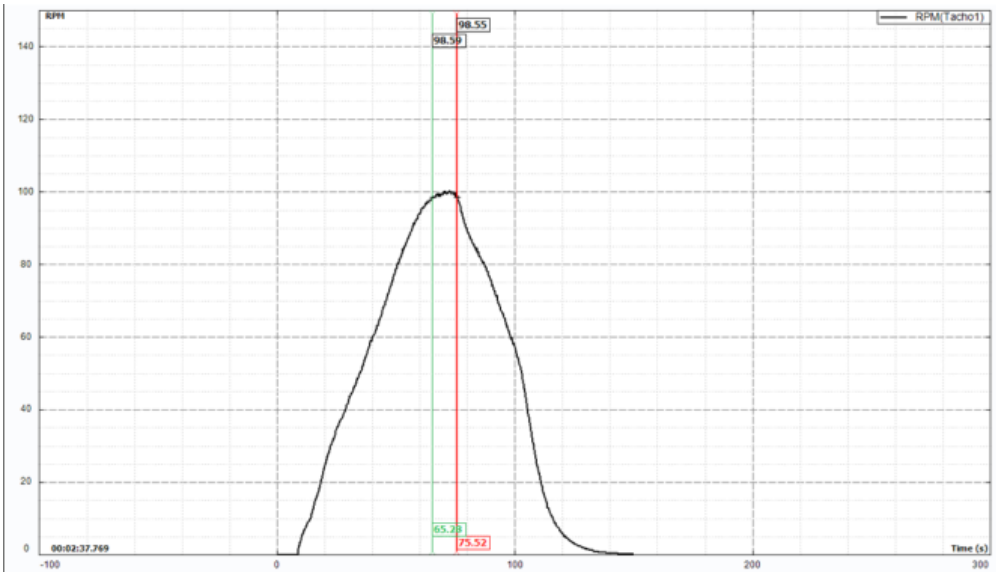



Figure 121: CRASH SAFETY SUSTAINED TEST FOR Z AXIS

### 5.14.3 CONCLUSION FOR VIBRATION AND ACCELERATION TEST

In sinusoidal scan recordings, no mechanical failures or noteworthy changes in resonance frequencies were observed (referred to the previously performed sweep). During the mechanically forced procedures, there was no unexpected EUT behavior.

The Acceptance Test Procedure is conducted at the beginning and end of all tests and is similar to each other. The initial and final Research Resonance values are remarkably similar. During and after the vibration and functional shock on the **DC PDP 1**, no changes or mechanical damage occurred on the test item.

As a result, the Vibration, Endurance, Crash Safety impulse test and Crash Safety Sustained test of the DC PDP 1 Component has been **PASSED**.

## 5.15 EMC/EMI TEST RESULTS

### 5.15.1 TEST SETUP

Laboratory instruments such as multimeter, ohmmeter, oscilloscope, etc. are not shown in the figure for clarity.

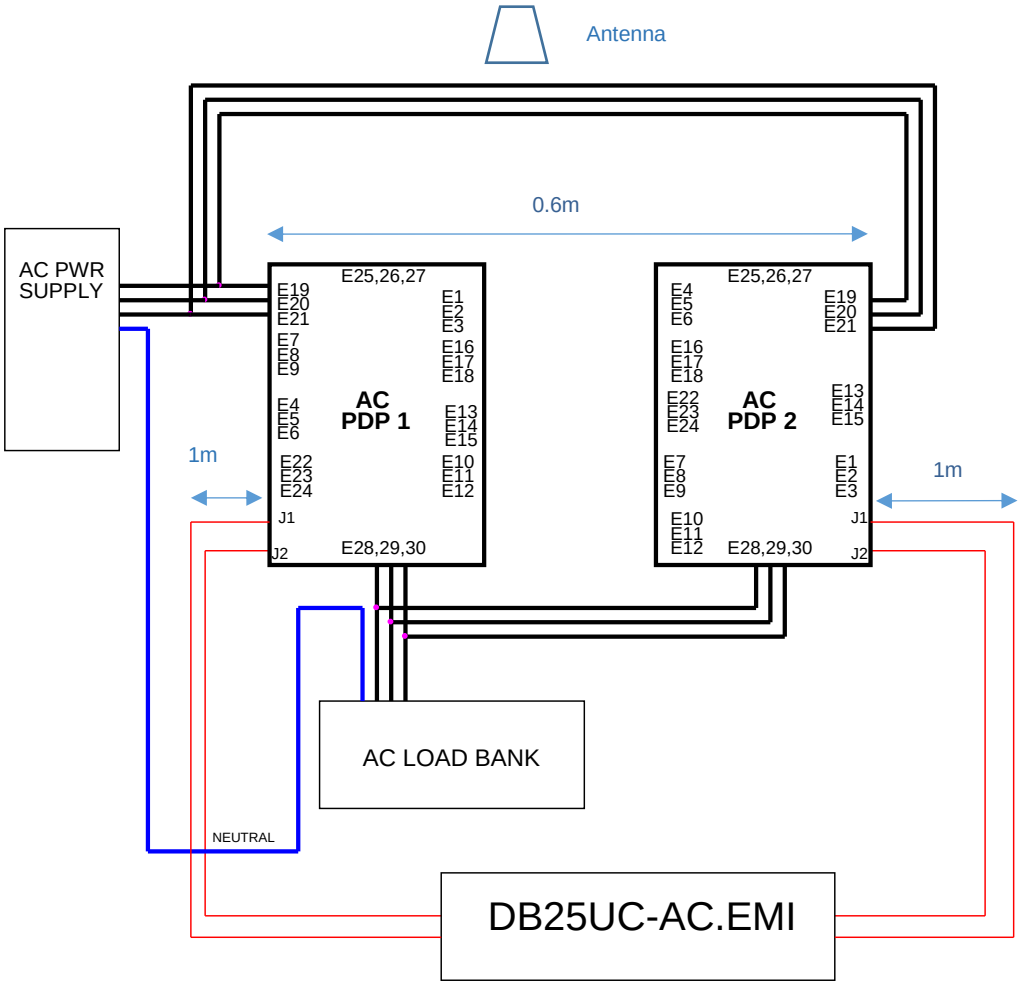



Figure 122: Test setup for EMI/EMC Test.

### 5.15.2 TEST SEQUENCE

Tests are planned to be carried out according to the below sequence. The only constraint is about the first and the last step (pre-test and post-test ATPs).

**Initial:**

1. Pre-test ATP on EUT

**EMC Tests:**

2. Electrical Bonding Measurement
3. [Section 21] Conducted emission – Current measurement
4. [Section 21] Radiated Emission – Electric field
5. [Section 20] Radio frequency conducted susceptibility
6. [Section 20] Radio frequency radiated susceptibility
7. [Section 17] Voltage Spikes
8. [Section 15] Magnetic effect

**Final:**

9. Post-test ATP

↓↓↓

**"EMC Test on the AC EPDS" session successful.**

### 5.15.3 EMC/EMI TEST RESULTS

This Test Report contains results of the EMC/EMI tests carried out in order to reach Safety of Flight qualification performance of the AC Electrical Power Distribution System (composed by AC PDP 1 and AC PDP 2).

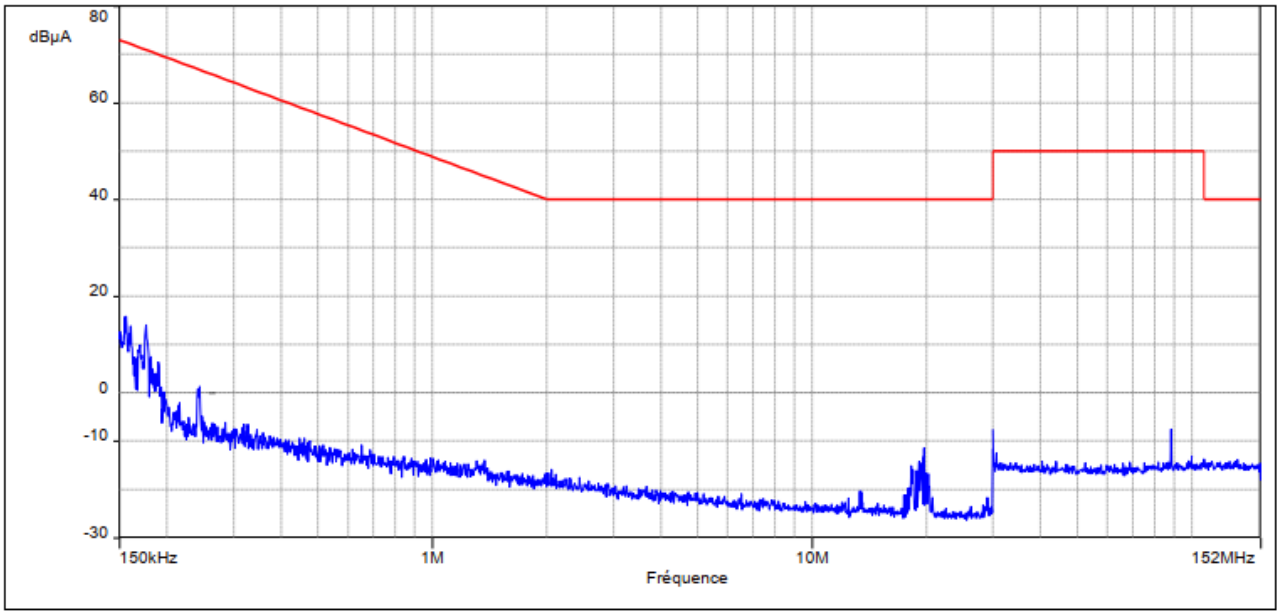
Table 60: Test results for EMC SOF tests on AC PDP SYSTEM.

| Test Type | Test Result (PASS/FAIL) |
|---|---|
| **Section 15** | FAIL |
| **Section 17** | PASS |
| **Section 20** | PASS |
| **Section 21** | PASS |

Based on the EME criticality of the functions performed by the system / equipment, the equipment location within the aircraft and the equipment wiring harness configuration and routing. To obtain the qualification, the machines must pass the following tests:

**Conducted Emissions** – From 150 kHz to 152 MHz

This test determines the current noise level emitted on each interconnecting cable when the equipment is powered. The purpose of this test is to verify that electromagnetic emissions from the EUT do not exceed the specified requirements for power input leads, including returns.

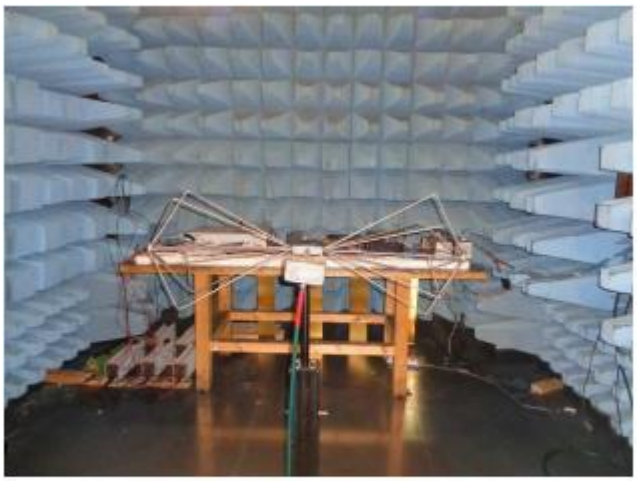



| Frequency | Step | RBW | VBW | Sweep time |
|---|---|---|---|---|
| 150kHz to 1MHz | 8192Pts | 1kHz | 3kHz | 15000 ms/MHz |
| 1MHz to 10MHz | 8192Pts | 1kHz | 3kHz | 15000 ms/MHz |
| 10MHz to 30MHz | 8192Pts | 1kHz | 3kHz | 15000 ms/MHz |
| 30MHz to 100MHz | 8192Pts | 10kHz | 30kHz | 1500 ms/MHz |
| 100MHz to 152MHz | 8192Pts | 10kHz | 30kHz | 1500 ms/MHz |

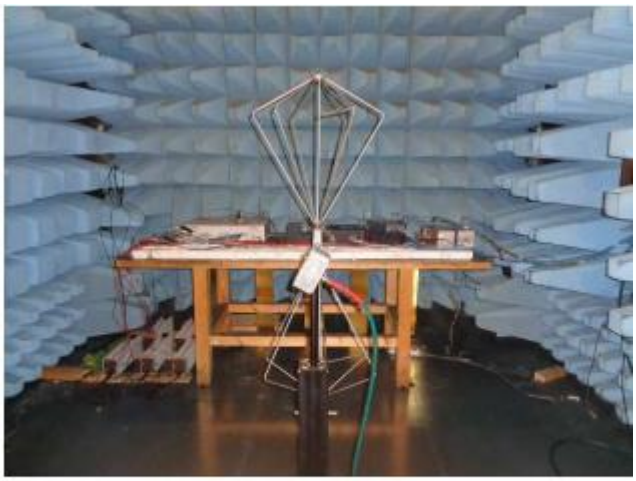
Figure 123: Radio Frequency Conducted Emission

**Radiated Emissions -** Electric Field from 100 MHz to 6GHz:

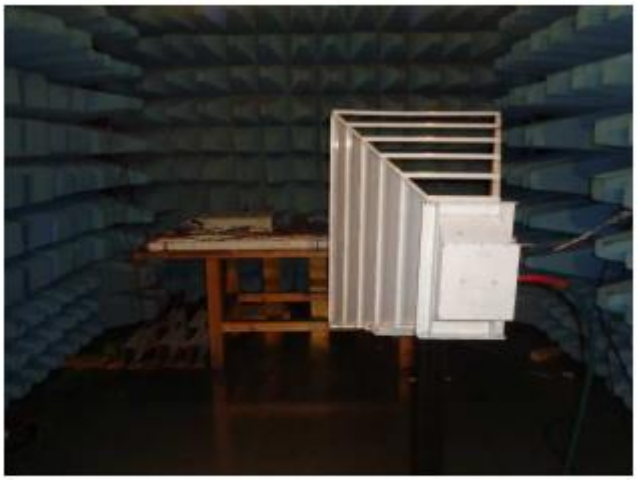
This test determines the electric field level emitted by the equipment when it is powered. The purpose of this test is to verify that electric field emissions from the EUT and its associated cabling do not exceed specified requirements.



Frequency range 100 MHz to 200 MHz
Antenna in horizontal polarization



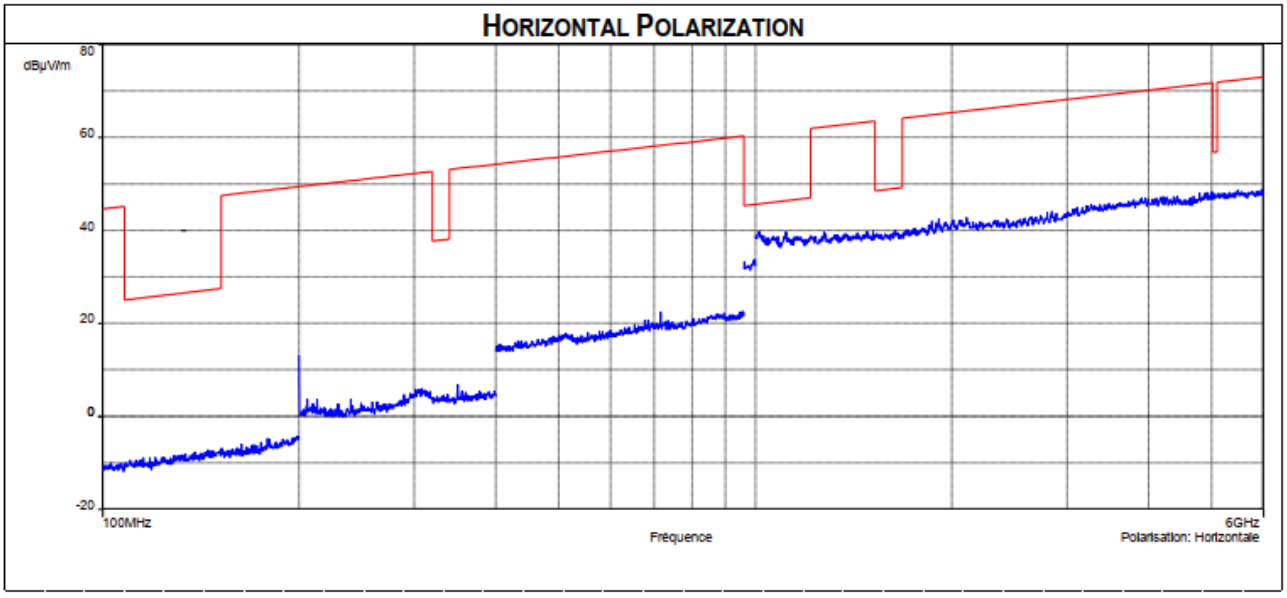
Frequency range 100 MHz to 200 MHz
Antenna in vertical polarization



Frequency range 200 MHz to 1000 MHz
Antenna in horizontal polarization – Position 1

Frequency range 200 MHz to 1000 MHz
Antenna in vertical polarization – Position 1

Figure 124: Test setup for Radiated emission

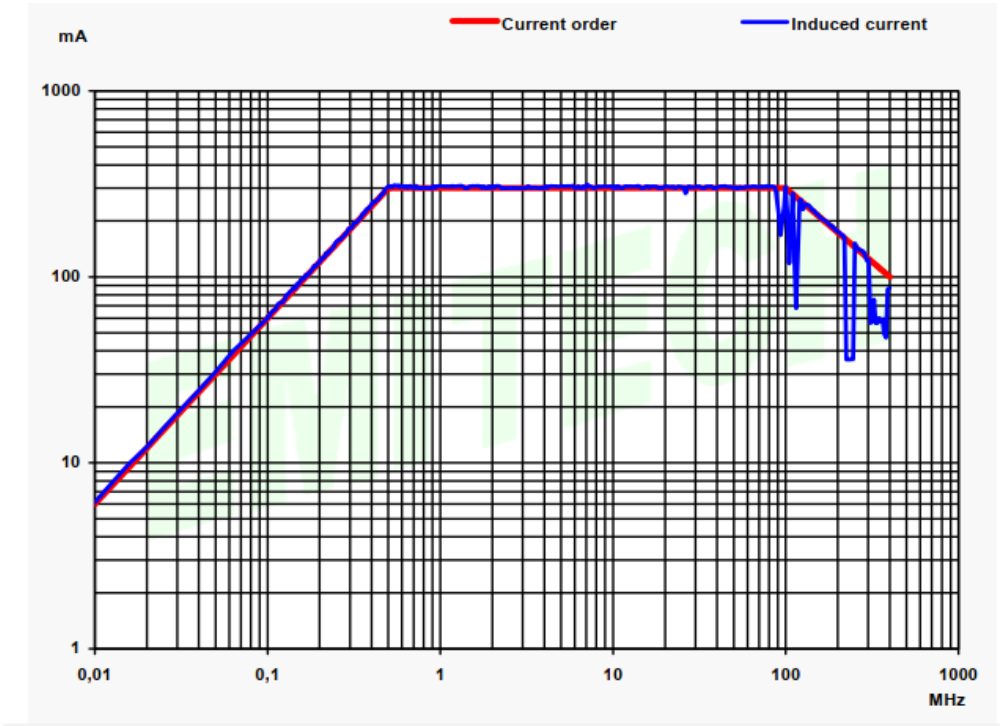



| Frequency | Polarization | Step | RBW | VBW | Sweep time |
|---|---|---|---|---|---|
| 100MHz to 200MHz | Horizontal | 8192Pts | 10kHz | 30kHz | 1500 ms/MHz |
| 200MHz to 400MHz | Horizontal | 8192Pts | 10kHz | 30kHz | 1500 ms/MHz |
| 400MHz to 960MHz | Horizontal | 8192Pts | 100kHz | 300kHz | 150 ms/MHz |
| 960MHz to 1GHz | Horizontal | 8192Pts | 1MHz | 3MHz | 15 ms/MHz |
| 1GHz to 6GHz | Horizontal | 8192Pts | 1MHz | 3MHz | 15 ms/MHz |

Figure 125: Radio frequency Radiated emission

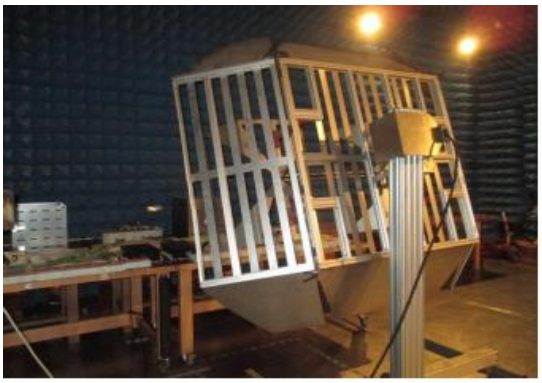
**Conducted Susceptibility –** from 10kHz to 400MHz:

The purpose of this test is to verify the ability of the EUT to withstand Radio Frequency signals coupled onto EUT associated cabling. This test determines whether equipment will operate within performance specifications when its interconnecting wiring is exposed to a RF conducted level by injection probe induction onto the power lines and interface circuit wiring (RTCA/DO 160 G Section 20, Category Y).

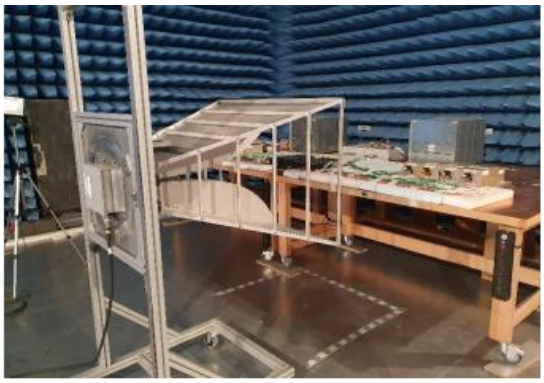



Note :
**"Current order"**: Maximum specified current during test
**"Induced current"**: Measured current during test on EUT bundle.

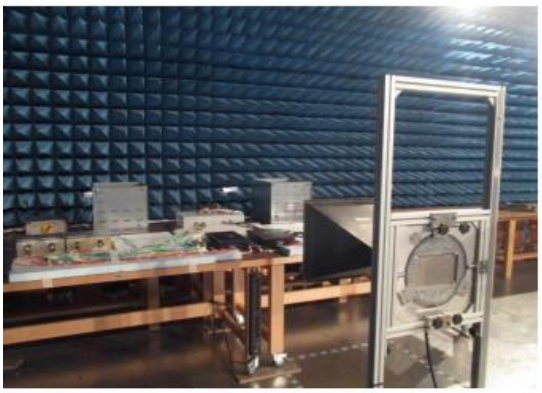
Figure 126: Radio frequency conducted susceptibility



Test from 100MHz to 200MHz



Test from 200MHz to 1GHz



Test from 1GHz to 5GHz

Test from 5GHz to 5.85GHz

Figure 127: Test setup for Radiated susceptibility

**Radiated Susceptibility –** from 100MHz to 18GHz in vertical and horizontal polarizations:

The purpose of this test is to verify the ability of the EUT and associated cabling to withstand electric fields. This test determines whether equipment will operate within performance specifications when equipment and its interconnecting wiring are exposed to an RF electric field level.

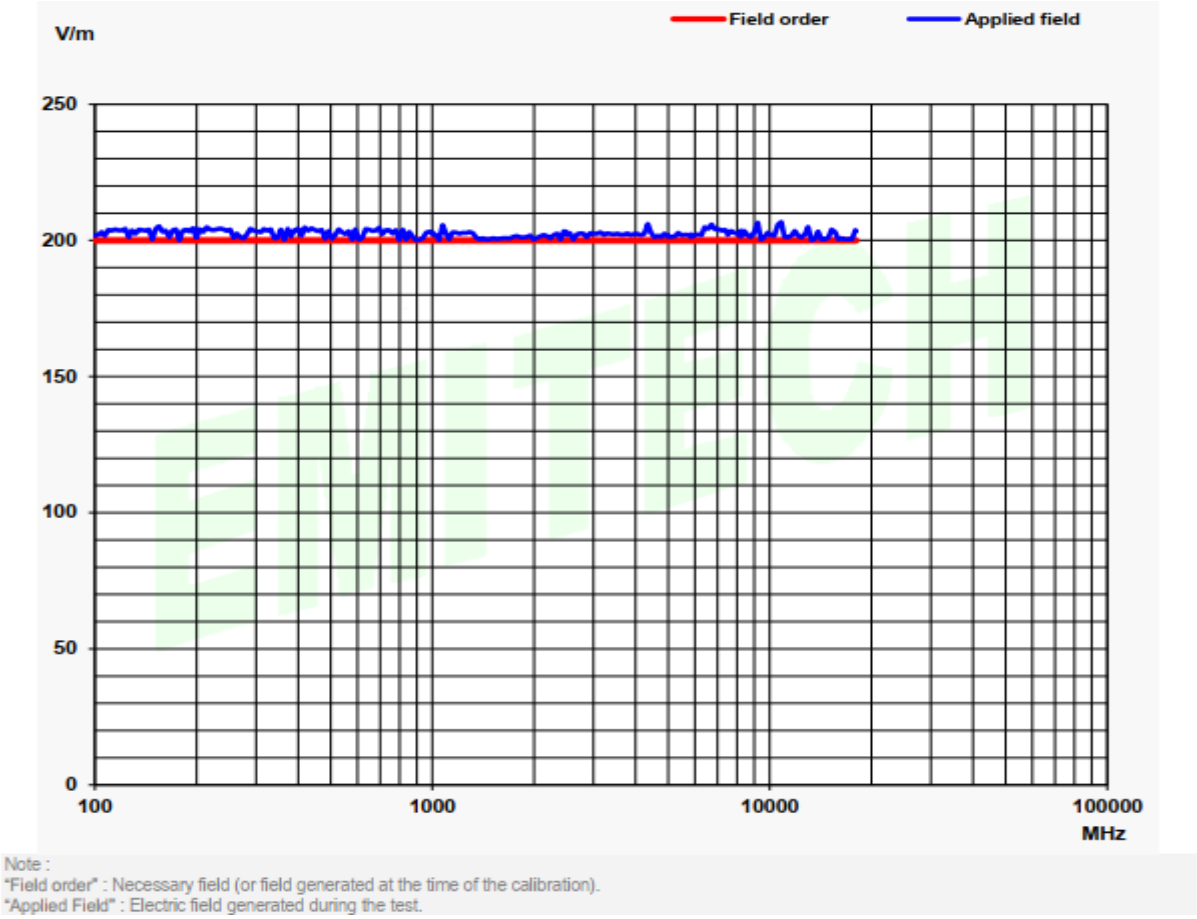



Figure 128: Radio frequency radiated susceptibility

**Voltage Spike:**
This test determines whether the equipment can withstand the effects of Voltage Spike induced on the power leads of the equipment.
The main adverse effects to be anticipated are:

- Permanent damage, component failure, insulation breakdown.
- Susceptibility degradation or changes in equipment performance.

This test determines whether the equipment can withstand the effects of voltage spikes arriving at the equipment on its power leads, either AC or DC [5].

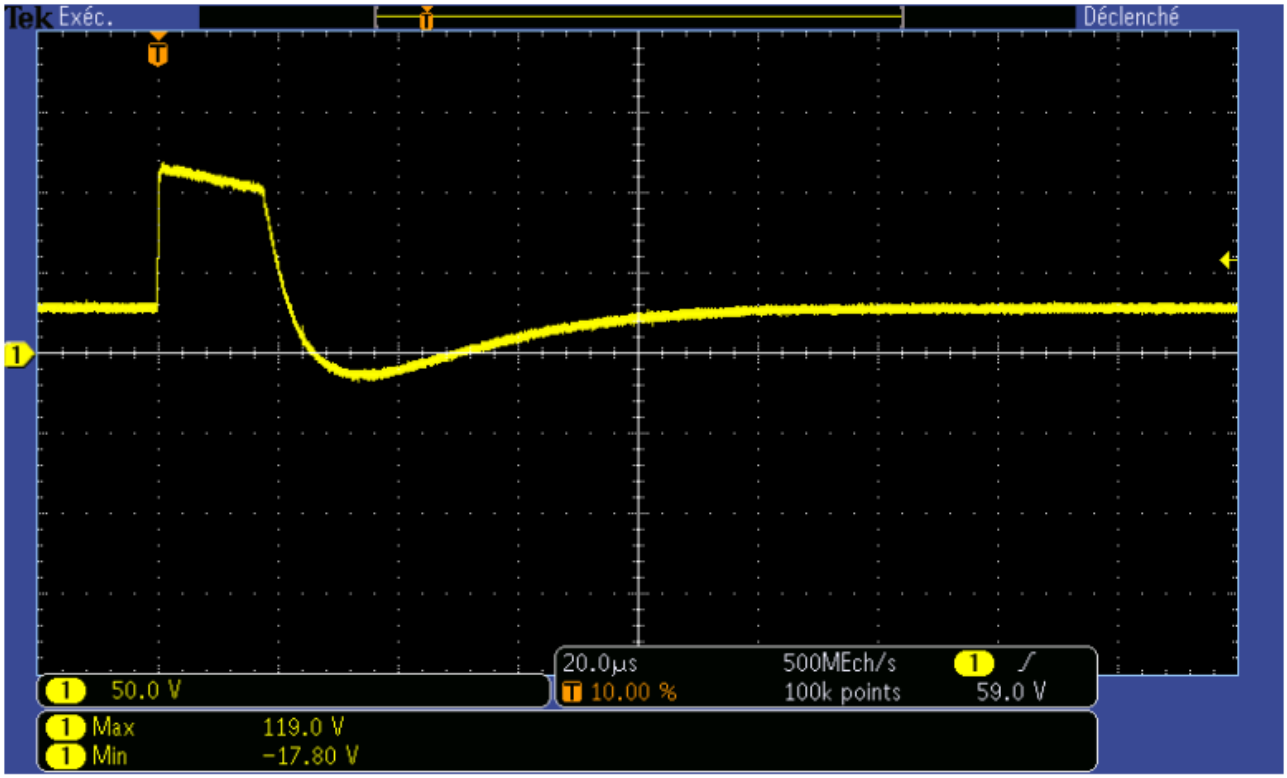


Figure 129: Positive voltage spike Injection on J2-3 of AC PDP 1

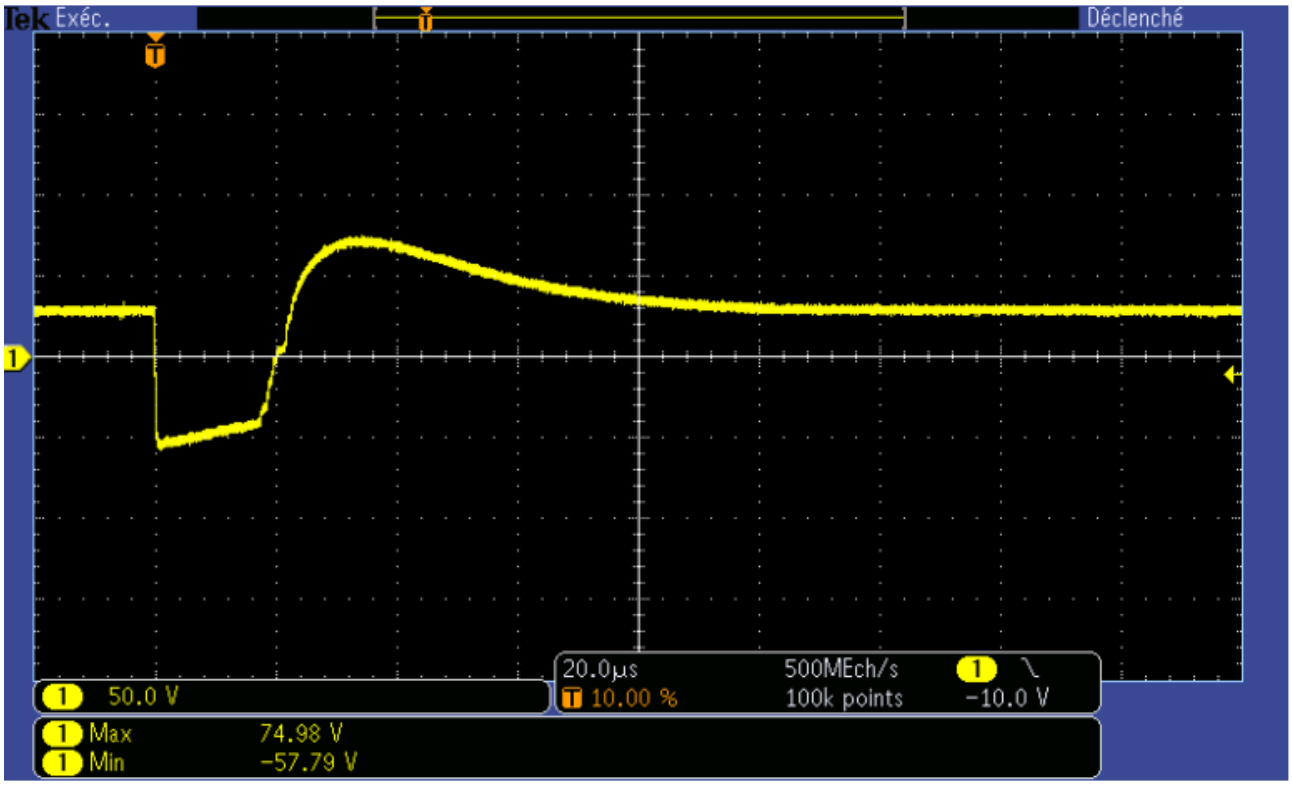


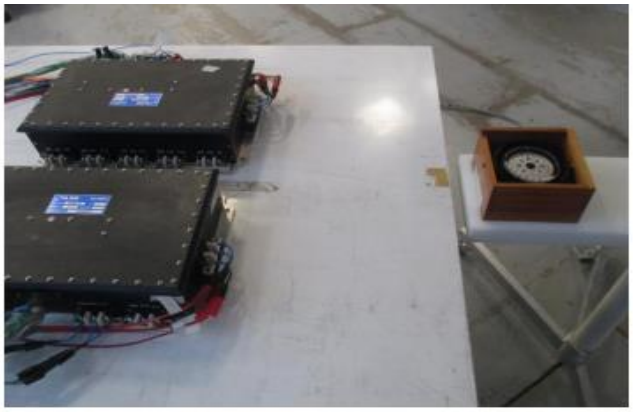
Figure 130: Negative voltage spike Injection on J2-3 of AC PDP 1

**Magnetic Effect:**

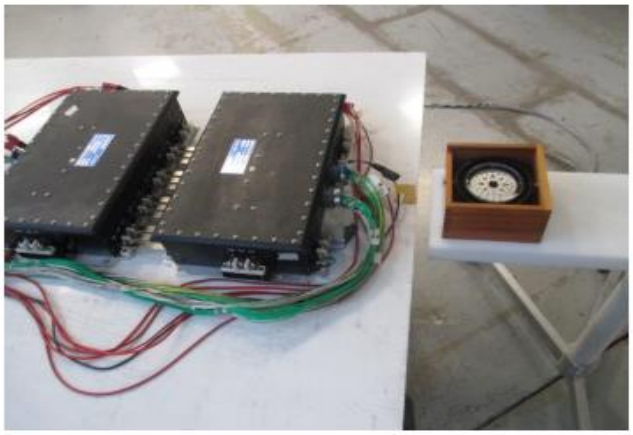
This test determines the magnetic effect of the equipment to assist the installer in choosing the proper location of the equipment in the aircraft. This test determines the magnetic effect of the equipment and is primarily intended to determine or demonstrate the closest permissible distance to compasses or compass sensors (flux gates) at which that unit is permitted to be installed. This test ensures that equipment can operate properly without causing interference to nearby equipment, determining equipment compliance with the applicable equipment performance standard, or assisting the installer in determining the proper location of the equipment in the aircraft [6].

The distance between the magnet pivot and the nearest part of the equipment at which a deflection of Dc, is measured with the equipment operated in its functional mode defined by the customer. Dc is 1 degree deviation when the horizontal component of the earth's magnetic field is 14.4 A/m +/- 10% at the test location. To define the horizontal component of the magnetic field of earth, we use the measurement made using a magnetometer at the location of position X assuming that the value of Y component is negligible. The average value is usually around 21080 nT or 16.7 A/m for EMITECH in Montigny le Bretonneux. Recording at the moment of the test: 22.2 A/m Dc calculation:

$$Dc := 14.4 \left( by\ value\ of\ H \left(\frac{A}{m}\right) issued\ from\ recording \right) := 0.65°$$



Side 1



Side 2

Figure 131: Test setup for Magnetic Effect

## 5.16 OPTIMIZATION OF EMI SHIELDING EFFECTIVENESS

This section concentrates on the chassis of electronic systems, specifically the effect of air vent holes on analytical interference shielding. This study investigates the effect of aperture hole size on shielding performance using Finite-Difference Time Domain (FDTD) simulations. Then, a numerical analysis is proposed, which allows for the mathematical quantification of expected shielding as a function of hole count, size, depth, and hole-to-hole separation distance. The numerical analysis is shown to be much more accurate than the FDTD results. Due to the increasing proliferation of higher data rate digital electronics, chassis enclosures with enhanced electromagnetic interference (EMI) shielding at these higher frequencies are required [5].

Shielding effectiveness SE is determined by a number of constants and variables, including complex permittivity εr and permeability μr, material type, material thickness t, dielectric properties σac, frequency, φ and free space permittivity ε0. Shielding effectiveness can be calculated as the ratio of incident to transmitted electric fields. When a metal screen is positioned between a radiating source and a set of monitoring points in simulations, the transmitted fields match the observed field levels. When no metal screen is present, incident fields are determined by examining field levels at the same points.

$$SE := 20\ \log\frac{E\ incident}{E\ transmitted}$$

This test evaluates the shielding effectiveness of vent holes on a system chassis by examining the effect of aperture size, hole-to-hole proximity distance, and hole depth on shielding performance. The analysis is carried out with the aid of a finite-difference time domain (FDTD) simulator. A mathematical relationship is developed to serve as a guide for electrical and mechanical design engineers.

**Step 1: Cutoff frequency calculation**

$$f_{co1} := \frac{c}{2d\ 10^{-3}} = 5 \times\ 10^{10}\ \text{Hz}$$

$$f_{co2} := f_{co1} \times 10^{-9} = 50\ Hz$$

$$f_{co3} := \frac{f_{co2}}{3} = 16.667\ Hz$$

**Step 2: Shielding Effectiveness calculation**

$$SL\ (f.d,t) := 56 - 3.5d - 20\log(f) + 25\frac{t-1}{d}\ \ for\ f \le \frac{fco}{3}$$

$$SLcutoff := SL\ (f_{co3}, d, t) = -8.289 \times 10^{3}$$

$$SH\ (f,d,t) := SLcutoff\left[1{,}5\ \left(1 - \frac{f}{fco}\right)\right]^{\frac{2}{3}}\ for\ \frac{fco}{3} < f < fco$$

**Step 3: Result**

$$Tdb := 10\log\left[1 + 0.25\left[\frac{3a^2\lambda}{\pi d^3\ \cos\theta}\right]^2\right] + 32\ \frac{t}{d}$$

$$a := 3.25 \times 10^{-3}$$

$$\theta := 0$$

$$d := 3.1 \times 10^{-3}$$

$$t := 1.5 \times 10^{-3}$$

$$P := 100\pi \frac{d^2}{4\,a^2} := 71.457$$

**Step 4: Comparision**

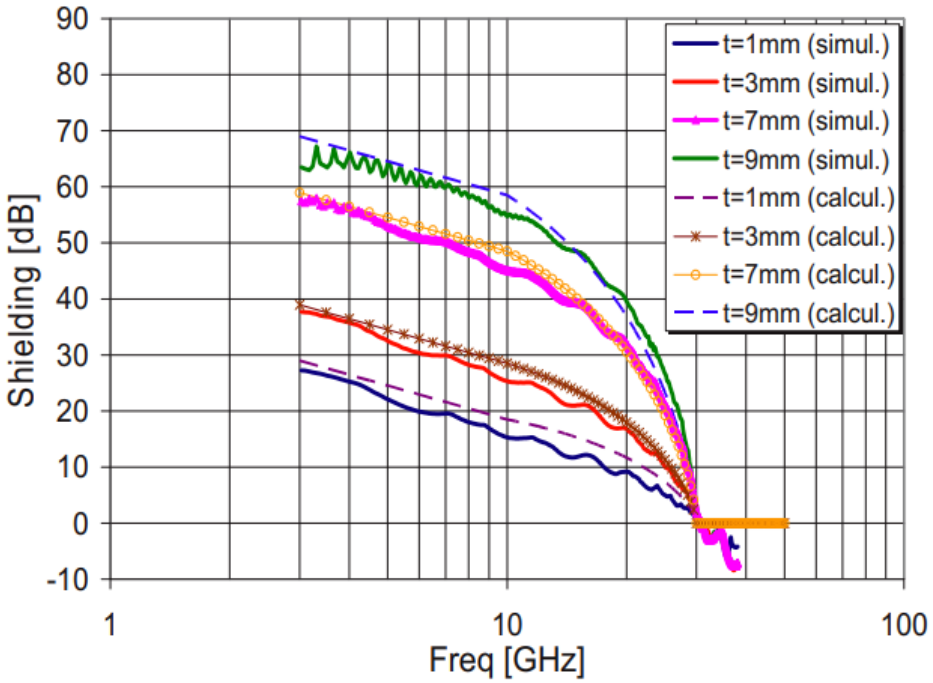



Figure 132: Simulated shielding effectiveness values for 5mm holes size

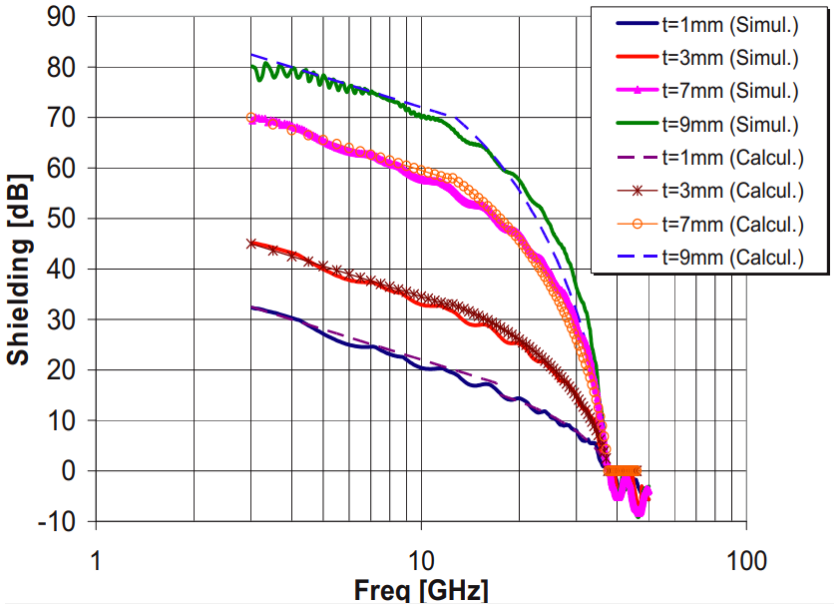



Figure 133: Simulated shielding effectiveness values for 4 mm holes size

To determine the effectiveness of hole shielding, a laboratory experiment was conducted. While the test environment is far from ideal, we felt it would shed light on the relative difference. Following figure depicts the prototype box enclosure developed for this purpose, while figure depicts shield screens with single and multiple holes. In this experiment, a signal generator was used to generate an incident waveform signal. The

metal enclosure's emission levels were determined using a double-ridged horn antenna connected to a spectrum analyzer. Throughout the experiment, emissions were monitored using a 60-cm-distance antenna horn figures show the results of the measurement for 9mm square holes. The authors believe that the various peaks on the plots are caused by resonances in the enclosure cavity. These measurements demonstrate that the cutoff frequency is largely determined by the hole opening size and is insensitive to the hole metal thickness. This is consistent with waveguide theory.

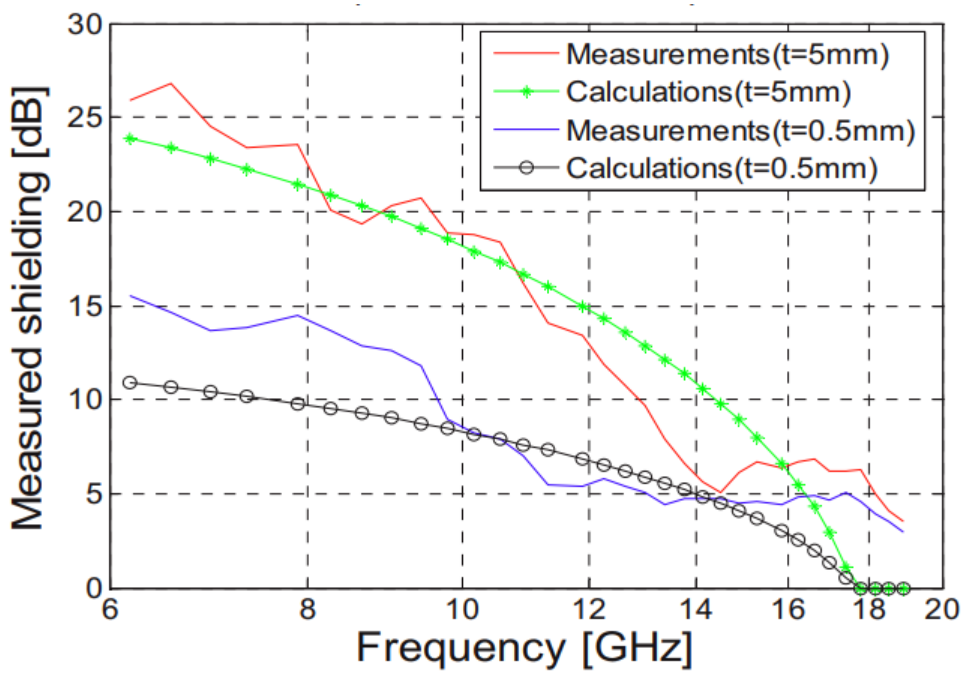



Figure 134: Measurement results of metal enclosure prototype

These measurements confirm that the cutoff frequency is primarily determined by the opening size of the hole and is unaffected by hole metal thickness. This is consistent with waveguide theory.

# 6 CONCLUSION

In light of the results obtained from the QTP qualification plan, it can be seen that all the necessary tests have been successfully passed in order to achive the Safety of Flight (SOF).

Functional tests are carried out on each of the units in accordance with the specifications of customer. Only one chosen relay for K7 Heater (which is part of AC PDP 1) failed during performance tests of AC Power Distribution Panel due to a supplier manufacturing defect. A more reliable new relay is suggested to the client for future development. The DC Power Distribution Panels have successfully passed the full performance test according to procurement specification. However, only the final test (83V) of the EPM board failed during the Battery PDP performance test. The measured intervention curve is slower than the requirement, because of the opening time of the contactor with TVS lightning protection and a redesign of the protection shall be considered.

Environmental SOF (Vibration and Temperature) test was successfully completed in both of PDPs (AC and DC) without any damage and noticeable problem. Research resonance before and after vibration and acceleration test is similar according to MIL STD 810G (United States Military Standard) and RTCA/DO 160G section 8. According to the RTCA/DO-160G (Radio Technical Commission for Aeronautics) standard, the EMI/EMC test on AC and DC Power Distribution Panels was successfully completed and can be considered positive, demonstrating the correct design of the cooling hole pattern. We redesigned the self-cooled with natural air ventilation panel to improve the EMI shielding effectiveness of the DC PDP. However, the AC Power Distribution Panels passed the EMI/EMC SOF test with minor deviations from the DEFENCE STANDART 59-411 standard, the test can be considered passed.

Thanks to these results, the EPDS can be considered to fulfill the specification requirements, and the certificate of conformity and Declaration Design Performance (DDP) can be issued. The DDP is a critical document that the customer must have in order to fly.

# 7 REFEERENCES

## 7.1 BIBLIOGRAFIA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[6] R. T. C. f. Aeronautics, «https://do160.org,» [Online]. Available: https://do160.org/electrostatic-discharge/.

[7] RTCA, «https://do160.org,» [Online]. Available: https://do160.org/voltage-spike/.

[8] RTCA, «https://do160.org/,» [Online]. Available: https://do160.org/magnetic-effect/.


## 7.2 STANDARDS

The following is a list of relevant standards which have been considered during the preparation of this document and which it must conform to:

1. DEF-STAN 59-411 DC03 Ministry of Defence – Defence Standard for EMC
2. DEF-STAN 59-41 Ministry of Defence – Defence Standarts for EMC
3. MIL-PRF-21480B Performance Specification Generator System, Electric Power, 400 Hz, Alternating Current, Aircraft and General Specification
4. MIL-HDBK-217F Reliability Prediction of Electronic Equipment
5. MIL-STD-704F Aircraft Electric Power Characteristic
6. MIL-STD-202G Test method standard electronic and electrical component parts
7. MIL-STD-704F Aircraft Electric Power Characteristic
8. MIL STD 810G Environmental Engineering Considerations and Laboratory Tests
9. RTCA DO-160G Environmental Conditions and Test Procedures for Airborne Equipment
10. MIL-STD-2175 Castings, Classification and Inspection of Military System
11. MIL-STD-1472 Human Engineering Design Criteria for Military System, Equipment and Facilities
12. MIL-C-5541 Chemical films and Chemical Film Materials
13. MIL-S-7742 Screw, Threads, Standard Aeronautical
14. MIL-A-8652 Anodic Coatings for Aluminum and Aluminum Alloys
15. MIL-P-5517 Plastic parts in aircraft hydraulic equipment general test
16. MIL-C-38999 Military Standard for Electrical Connector
17. MIL STD 704F Aircraft Electric Power Characteristics

## 7.3 LIST OF ACRONYMS AND ABBREVIATIONS

Acronyms, terms, symbols and abbreviations are defined in this section to establish their meaning in the context of their use in this document. Annexed documents may define additional acronyms, terms, symbols and abbreviations. The following acronyms appear in the text of the present document:

AC Alternating Current
ATP Acceptance Test Procedure
ATR Acceptance Test Report
BTC Bus Tie Contactor
BLS Brushless
BLS GEN Brushless Generator
BLG Brushless Generator
CDR Critical Design Review
CFD Computational Fluid Dynamic
DC Direct Current
EPDS Electrical Power Distribution System
EPSGS Electrical Power Starting and Generating System
EUT Equipment Under Test
FFT Fast Fourier Transform
GCU Generator Control Unit
GCS Generator Control Switch
GEN Generator (the same of BLG or BLS GEN)
GND Ground
HECS Hall Effect Current Sensor
LC Line Contactor
N.A. Not Applicable
P/N Part Number
PLC Power Line Cycle
PSMC Power System Monitor Controller
QTP Qualification Test Procedure
QTR Qualification Test Report
S/G Starter/Generator
S/N Serial Number
SC Start Contactor
SCRT Short Circuit
SoF Safety of Flight
TC Thermocouple
CCW Counter Clockwise
CW Clockwise
DC Direct Current
DRL Data Requirement List
RMS Root Mean Square
EMC Electromagnetic Compatibility
EMI Electromagnetic Interference
DDP Declaration of Design and Performance