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Digitally Assisted Integrated Front- End for a Chemiresistive Oxygen Sensor

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Author: **Faruk Koklukaya**

Student ID: 247057

Advisor: Prof. Andrea Giovanni Bonfanti

Co-advisors: Prof. Máté Bezdek, Dr. Amrith Sukumaran

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Abstract

This thesis presents the design and analysis of an integrated mixed-signal interface implemented in a 22-nm CMOS process, targeting a photoactivated oxygen sensing system. The work was conducted at the Center Suisse d'Electronique et de Microtechnique (CSEM), Zürich, in collaboration with the Bezdek Group at ETH Zürich. The target sensor operates based on a dye-sensitized chemiresistive mechanism, where variations in oxygen concentration are translated into changes in electrical resistance under controlled optical excitation.

The work begins by analyzing the sensing principle and translating application-level specifications, including oxygen concentration range and resolution, into equivalent electrical requirements. In particular, a minimum detectable concentration variation of 100 ppm is mapped to an equivalent resistance change, which defines the resolution target of the electronic readout system.

To address these requirements, a resistance-to-digital converter (RDC) based on a Schmitt trigger-driven relaxation oscillator is developed. The proposed architecture converts the sensor resistance into an oscillation frequency, which is subsequently digitized through a period measurement counter. To compensate for the inherent nonlinearity of the oscillator, a piecewise-linear (PWL) calibration methodology is implemented in the digital domain.

In addition to the readout circuit, the thesis includes the design of a dedicated LED current driver to provide stable optical excitation of the sensor. The complete system thus integrates optical activation, resistance readout, and digital processing within a unified architecture.

The design is validated through circuit-level simulations and system-level analysis, demonstrating the ability to achieve the required resolution while maintaining low power consumption and scalability. The proposed approach provides an efficient and compact solution for integrated gas sensing applications.

Keywords: mixed-signal interface, resistance-to-digital converter (RDC), relaxation oscillator, Schmitt trigger, piecewise-linear (PWL) calibration, photoactivated oxygen sens-

ing, chemiresistive sensor, LED driver

Abstract in lingua italiana

Questa tesi presenta la progettazione e l'analisi di un'interfaccia integrata mixed-signal implementata in tecnologia CMOS a 22 nm per un sistema di rilevamento dell'ossigeno basato su un sensore fotoattivato. Il lavoro è stato svolto presso il Center Suisse d'Electronique et de Microtechnique (CSEM), Zurigo, in collaborazione con il gruppo Bezdek presso l'ETH di Zurigo. Il sensore di interesse opera secondo un meccanismo chemioresistivo sensibilizzato da coloranti, in cui le variazioni della concentrazione di ossigeno sono convertite in variazioni della resistenza elettrica sotto opportuna eccitazione ottica.

Il lavoro inizia con l'analisi del principio di funzionamento del sensore e con la traduzione delle specifiche a livello applicativo, quali l'intervallo di concentrazione di ossigeno e la risoluzione richiesta, in requisiti elettrici equivalenti. In particolare, una variazione minima rilevabile di 100 ppm viene mappata in una corrispondente variazione di resistenza, che definisce il requisito di risoluzione del sistema di lettura elettronico.

Per soddisfare tali requisiti, viene sviluppato un convertitore resistenza-digitale (RDC) basato su un oscillatore a rilassamento pilotato da un trigger di Schmitt. L'architettura proposta converte la resistenza del sensore in una frequenza di oscillazione, che viene successivamente digitalizzata mediante un contatore di periodo. Per compensare la non linearità intrinseca dell'oscillatore, viene implementata una strategia di calibrazione a tratti lineari (PWL) nel dominio digitale.

Oltre al circuito di lettura, la tesi include la progettazione di un driver di corrente per LED dedicato, necessario a garantire un'eccitazione ottica stabile del sensore. Il sistema completo integra quindi il controllo dell'eccitazione ottica, la lettura della resistenza e l'elaborazione digitale all'interno di un'unica architettura.

Il progetto è validato mediante simulazioni a livello di circuito e analisi a livello di sistema, dimostrando la capacità di soddisfare i requisiti di risoluzione mantenendo al contempo un basso consumo di potenza e una buona scalabilità. L'approccio proposto rappresenta una soluzione compatta ed efficiente per applicazioni di sensing integrato di gas.

Parole chiave: interfaccia mixed-signal, convertitore resistenza-digitale (RDC), oscil-

latore a rilassamento, trigger di Schmitt, calibrazione a tratti lineari (PWL), sensore chemioresistivo, rilevamento fotoattivato dell'ossigeno, driver di corrente per LED

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1 | Introduction and Chemical Background

1.1. Background and Motivation for Oxygen Sensing

Reliable oxygen sensing is essential in environmental monitoring, industrial process control, and biomedical applications [1, 2]. Conventional oxygen sensing approaches include electrochemical, optical, and metal-oxide-based technologies, each offering different trade-offs in terms of sensitivity, operating conditions, and system complexity [2, 3].

Although conventional electrochemical and metal-oxide oxygen sensors can provide accurate detection, they often involve trade-offs in power consumption, operating temperature, or instrumentation complexity [2, 3]. Consequently, there is a strong demand for sensing solutions that operate at room temperature while maintaining high sensitivity and selectivity.

1.2. Dye-Sensitized Chemiresistive Sensors

A promising strategy to overcome these limitations is chemiresistive sensing based on carbon nanomaterials. Carbon nanotube (CNT)-based chemiresistors have emerged as attractive candidates due to their high sensitivity, low power consumption, and capability for room-temperature operation [4, 5].

Despite these advantages, achieving high selectivity and environmental robustness remains challenging for conventional CNT-based sensors. In particular, performance degradation due to humidity and interference from other gases limits their practical applicability. While these approaches provide a strong foundation for gas sensing, combining light activation with chemiresistive transduction remains relatively unexplored.

In this context, Wettstein *et al.* introduced a hybrid sensing material consisting of single-walled carbon nanotubes (SWCNTs) and titania (TiO_2), functionalized with a rhenium-based molecular photosensitizer, forming the composite SWCNT- TiO_2 -Re [1].

Inspired by the operating principles of dye-sensitized solar cells (DSSCs), the sensor employs a photoactivated sensing mechanism [6, 7]. The molecular photosensitizer absorbs visible light and generates photoexcited electrons, which are injected into the SWCNT-TiO₂ hybrid network. This process increases the carrier density within the conductive network, enabling a resistance-based sensing response. Unlike traditional sensing technologies that rely on thermal activation, this approach utilizes visible light to trigger the sensing state. As a result, the injected electrons modulate the carrier concentration of the SWCNT network, leading to a measurable resistance variation [1].

1.3. Sensing Mechanism: Photoactivation and O₂ Trapping

1.3.1. Photoinduced Response

The sensing mechanism is activated using a green light source with a wavelength of $\lambda = 516$ nm and an irradiance of approximately 0.02 mW/mm². Upon illumination, the sensitizer harvests visible light and promotes the injection of photoexcited electrons into the SWCNT-TiO₂ network, thereby modifying the electrical resistance of the device [1]. Upon illumination, the sensitizer harvests visible light and promotes the injection of photoexcited electrons into the SWCNT-TiO₂ network, thereby modifying the resistance of the device. The overall photoactivation mechanism is illustrated in Fig. 1.1.

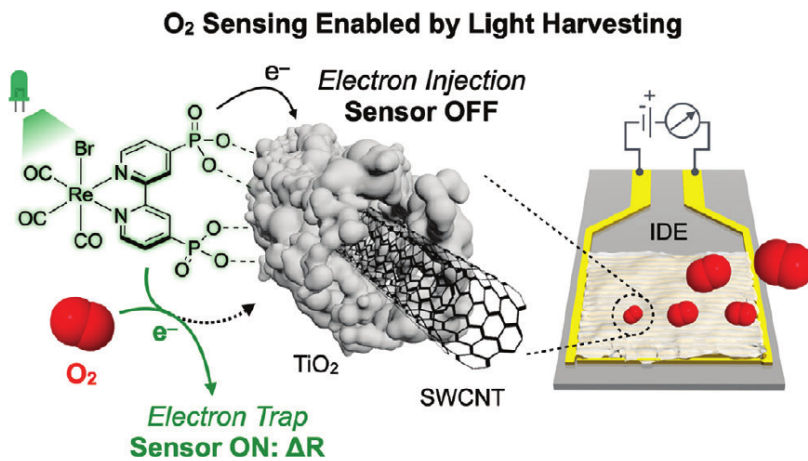


Figure 1.1: Schematic illustration of the photoactivated sensing mechanism in the SWCNT-TiO₂-Re system. Under green-light illumination, photoexcited electrons are injected into the hybrid network and the sensing state becomes sensitive to oxygen-induced electron trapping. Adapted from [1].

This characteristic demonstrates that the sensor operates exclusively under optical excitation. As shown in Fig. 1.2, the resistance changes reversibly when the green light is switched ON and OFF, highlighting the central role of optical activation in the sensing process. The increase in resistance under illumination and its gradual recovery when the light is switched off confirm the photoactivated nature of the sensing mechanism.

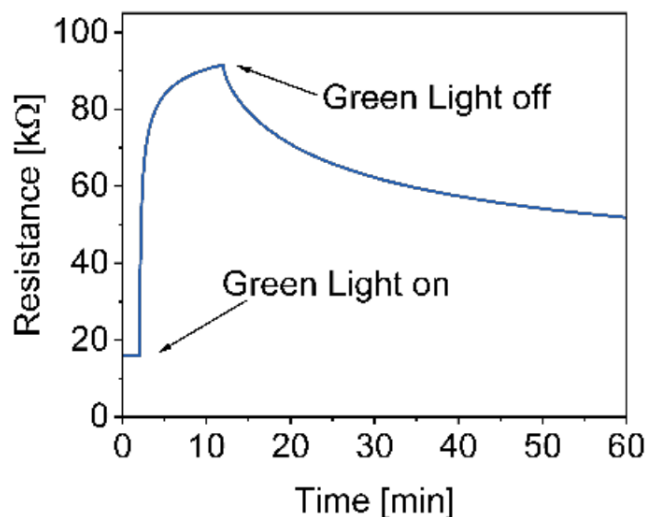


Figure 1.2: Resistance response of the sensor under green light ON/OFF cycling, showing reversible behavior during optical excitation. Adapted from Supplementary Fig. S28A in Supporting Information of [1].

As a result, the sensing system inherently requires a stable and well-controlled optical source to ensure repeatable and reliable operation.

1.3.2. Oxygen Interaction and Resistance Decrease

In the presence of oxygen, photoexcited electrons are captured by O_2 molecules, which modify the charge distribution within the sensing material, leading to a decrease in resistance. The corresponding transient response during oxygen exposure is shown in Fig. 1.3.

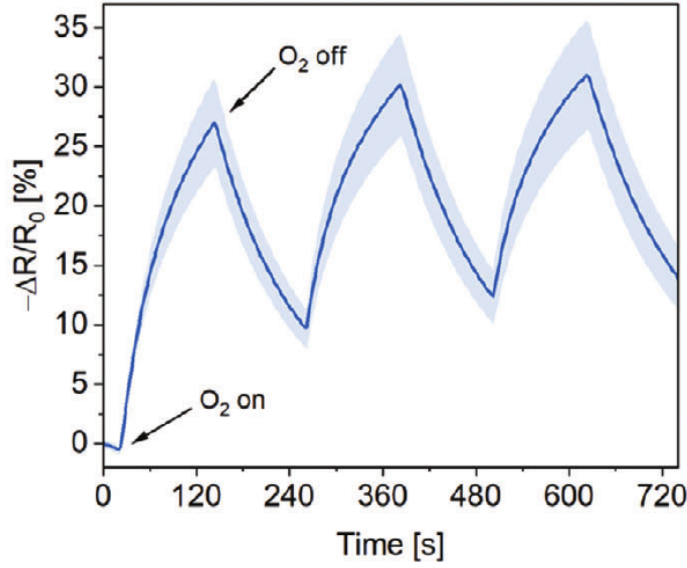


Figure 1.3: Transient sensor response during repeated oxygen exposure and removal cycles, showing reversible resistance modulation associated with oxygen interaction. Adapted from [1].

The observed resistance variation is not instantaneous but exhibits a transient behavior. This is due to the finite kinetics of oxygen adsorption and desorption processes, as well as electron trapping and release mechanisms at the sensor surface. As a result, the system requires a certain time to approach equilibrium after each change in oxygen concentration.

It is important to note that the sensor is continuously illuminated during this measurement. Therefore, the resistance modulation originates from the interaction between photoexcited electrons and oxygen molecules, rather than from changes in the optical excitation itself.

Experimental observations indicate a fast response, with the maximum rate of resistance change occurring within approximately 6 seconds after gas exposure. The recovery process is slower, requiring around 9 minutes of nitrogen (N_2) purging to restore the initial resistance value R_0 .

1.4. Sensor Performance: Selectivity and Stability

1.4.1. Gas Selectivity

Selectivity is one of the main challenges in practical gas sensing, particularly for chemiresistive platforms operating under ambient conditions [4, 8]. In this work, the selectivity

mechanism is evaluated by comparing the response to oxygen against common interfering gases.

The selectivity characteristics of the sensor are shown in Fig. 1.4. The SWCNT-TiO₂-Re sensor exhibits high selectivity toward oxygen compared to other gases. When exposed to interferants such as CO₂, H₂, CH₄, and N₂O at concentrations of 1000 ppm, the sensor response remains negligible. In contrast, exposure to O₂ produces a significant resistance variation, demonstrating the selectivity of the light-activated sensing mechanism.

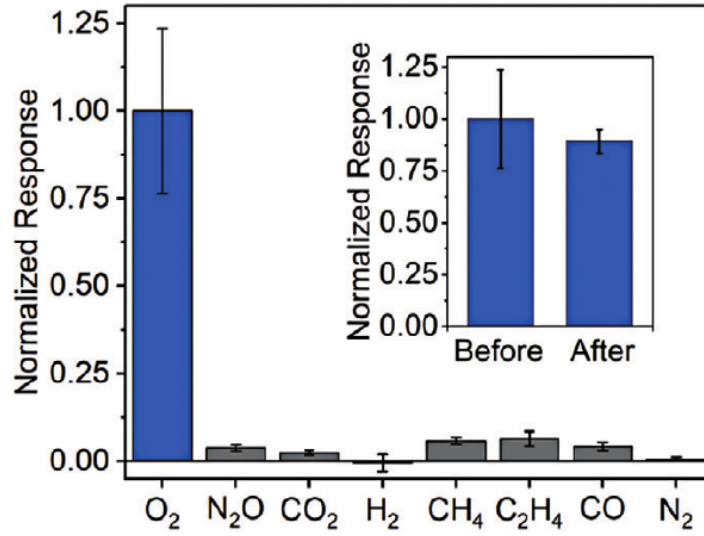


Figure 1.4: Comparison of the normalized sensor response to oxygen and to common interfering gases, showing the high selectivity of the SWCNT-TiO₂-Re sensor toward O₂. Adapted from [1].

This behavior indicates that the rhenium-based sensitizer plays a crucial role in suppressing undesired interactions, thereby improving selectivity and preventing sensor poisoning effects.

1.4.2. Stability and Humidity Tolerance

In addition to selectivity, environmental robustness is another key requirement for practical sensor deployment. Humidity interference is a well-known limitation in many carbon-nanotube-based chemiresistive sensors and must be carefully considered when evaluating real-world applicability [1, 8].

An important advantage of this sensing approach is its robustness under varying environmental conditions. The sensor maintains stable operation over a relative humidity (R.H.)

range of 0% to 80%. In addition, long-term measurements demonstrate that the device preserves its sensing performance for periods exceeding three months under ambient conditions [1].

1.5. Thesis Contributions and Structure

From an electronic system perspective, the described sensing mechanism translates into a resistance-based signal that depends on both optical excitation and gas interaction. Consequently, the design of the sensing interface requires two key elements: a stable light source for photoactivation and a high-resolution readout circuit capable of capturing small resistance variations.

In this context, the main contributions of this work are the design and implementation of an integrated mixed-signal front-end in a 22-nm CMOS process to drive and read a photoactivated oxygen sensor. In particular, the system includes a high-resolution Schmitt trigger-based Resistance-to-Digital Converter (RDC) and a stable 10 mA LED driver to ensure controlled and repeatable optical excitation.

The remainder of this thesis is structured as follows:

- **Chapter 2** translates the sensor behavior into electronic specifications and introduces the overall chip architecture.
- **Chapter 3** presents the analog and digital implementation of the RDC.
- **Chapter 4** describes the design of the LED driver circuit.
- **Chapter 5** discusses the obtained results and performance.
- **Chapter 6** concludes the thesis and outlines future developments.

2 | Sensor Interface and Integrated Circuit Architecture

2.1. Translation of Sensor Characteristics into Electrical Specifications

The design of the integrated readout electronics starts from the sensing requirements defined at the application and sensor levels. In this work, the target oxygen sensor is intended to operate over a wide concentration range while preserving sensitivity to relatively small concentration variations. Therefore, before introducing the electronic architecture, the gas-level requirements must first be translated into equivalent electrical specifications.

2.1.1. Gas-Level Specifications

The key application-level specifications are summarized in Table 2.1. These values are derived from the sensor characterization data and from the target use conditions discussed with the sensor development team.

Parameter	Target Value / Description
Measurement Range	0.01% – 20% O ₂
Required Concentration Resolution	100 ppm
Response-Time Target	Approximately 6 s
Selectivity Requirement	Oxygen-only sensing of interest
Nominal Illumination Wavelength	516 nm
Light Modulation Scheme	Continuous illumination

Table 2.1: Gas-level and sensing-level specifications used as the starting point for the electronic design.

These requirements define the target sensing scenario, but they are not yet directly usable for integrated-circuit design. Since the readout electronics interacts with the sensor electrically, the gas-level quantities must be converted into resistance-domain specifications.

2.1.2. From Gas Resolution to Resistance Resolution

Experimental sensor data reported in the literature indicate that, around ambient conditions (20% O₂), small oxygen concentration variations in the range of 50–500 ppm produce measurable changes in the normalized resistance variation $\Delta R/R_0$.

As illustrated in Fig. 2.1(A), step-wise decreases in oxygen concentration lead to a corresponding increase in $\Delta R/R_0$, with larger concentration changes producing larger resistance variations. This demonstrates the sensitivity of the sensor to small variations in oxygen concentration.

Fig. 2.1(B) summarizes this behavior by plotting the steady-state normalized resistance variation as a function of oxygen concentration change, showing an approximately linear relationship over the considered range. This local linear behavior is particularly important because it allows the required gas resolution to be mapped into an equivalent resistance variation at the operating point.

This relationship can be used to translate the gas-level resolution requirement into an equivalent resistance-domain specification.

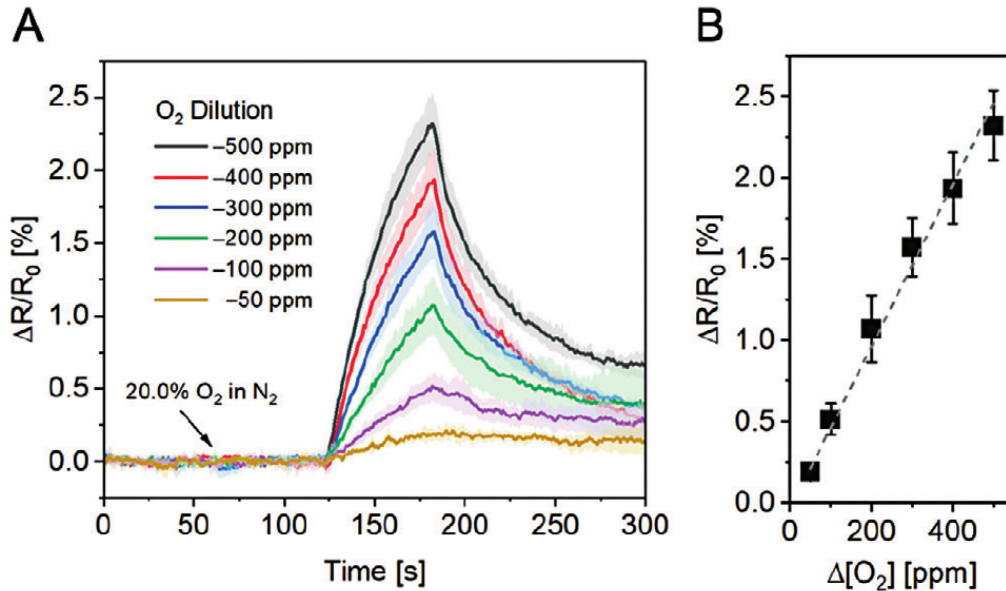


Figure 2.1: Sensor response to small oxygen concentration variations around 20% O₂. Plot (A) shows the transient resistance response for concentration decreases between 50 and 500 ppm, while plot (B) shows the corresponding normalized resistance variation as a function of oxygen concentration change, demonstrating approximately linear behavior. Adapted from [1].

From the approximately linear relationship shown in Fig. 2.1(B), a concentration variation of 100 ppm corresponds to an approximate normalized resistance change of:

$$\frac{\Delta R}{R_0} \approx 0.5\% \quad (2.1)$$

It is important to note that this proportionality is used as a local approximation around the chosen operating point near 20% O₂ concentration in air. Over the full concentration range, the overall sensor response is nonlinear; however, the local linear approximation is the relevant quantity for defining the minimum detectable resistance variation associated with a 100 ppm concentration change.

In the proposed interface, the sensor operating point is arranged around a nominal baseline resistance of:

$$R_0 = 54.7 \text{ k}\Omega \quad (2.2)$$

Using (2.1) and (2.2), the minimum resistance change associated with the required gas resolution is:

$$\Delta R = R_0 \cdot \frac{\Delta R}{R_0} = 54.7 \text{ k}\Omega \times 0.005 \approx 274 \text{ }\Omega \quad (2.3)$$

Equation (2.3) provides the key link between the application-level sensor requirement and the electronic design target: a concentration variation of 100 ppm must be represented electrically as a resistance change of approximately 274 Ω .

To ensure robust detection in the presence of quantization, circuit nonidealities, and calibration residuals, the readout resolution must be significantly smaller than this value. In this work, a design margin of approximately 5 $\times$ is adopted, leading to the requirement:

$$R_{\text{LSB}} \leq \frac{274 \text{ }\Omega}{5} \approx 50 \text{ }\Omega \quad (2.4)$$

Therefore, the resistance-to-digital converter (RDC) is designed to achieve a target resolution of approximately 50 Ω or better. This approximation forms the basis for the subsequent derivation of the required resistance resolution of the readout circuit.

2.1.3. Resistance Range and Electrical Operating Point

In addition to the minimum detectable variation, the electronic interface must support a sufficiently wide measurable resistance range. Although the nominal operating point is centered around 54.7 k Ω , design margin is required to account for device-to-device variation, environmental changes, aging, and calibration spread.

For this reason, the electrical input range of the readout circuit is defined as:

$$R_{\min} = 750 \, \Omega, \quad R_{\max} = 75 \, \text{k}\Omega \quad (2.5)$$

This range safely covers the intended operating point while providing sufficient flexibility for characterization, calibration, and future sensor revisions.

The translation from gas-level quantities to electrical design quantities is summarized in Table 2.2.

Gas / Sensor-Level Quantity	Derived Electrical Quantity
O ₂ measurement range: 0.01% – 20%	Supported resistance range: 750 Ω – 75 k Ω
Required concentration resolution: 100 ppm	Equivalent resistance change: $\approx 274 \, \Omega$
Local sensor sensitivity near 20% O ₂	$\Delta R/R_0 \approx 0.5\%$ per 100 ppm
Baseline operating point	$R_0 \approx 54.7 \, \text{k}\Omega$
Robust detection requirement	RDC target resolution: $\leq 50 \, \Omega$

Table 2.2: Translation of gas-level specifications into electrical requirements for the sensor interface.

2.1.4. Optical Excitation Requirement

The sensing mechanism is photoactivated and therefore requires controlled optical excitation. According to the reported characterization conditions, the sensor is operated under green-light illumination with a nominal wavelength of 516 nm. Consequently, the electronic interface must include a dedicated current-controlled block to bias an external LED in a stable and repeatable manner.

In this work, the LED bias current is set to:

$$I_{\text{LED}} = 10 \, \text{mA} \quad (2.6)$$

This value is treated as a design target for the optical excitation branch of the IC and is used to define the corresponding current-generation circuitry.

The analysis presented in this section establishes the main electrical requirements that drive the architecture of the integrated interface:

- a measurable resistance range of $750\ \Omega$ to $75\ \text{k}\Omega$,
- an RDC resolution smaller than $50\ \Omega$,
- a stable LED excitation current of $10\ \text{mA}$.

These requirements are used in the following section to define the overall IC architecture.

2.2. Proposed IC Architecture

The proposed integrated circuit (IC) acts as the electronic interface between the photoactivated oxygen sensor and an external digital controller. Its primary functions are to provide controlled optical excitation, accurately measure the sensor resistance, and convert this information into a digital format suitable for further processing.

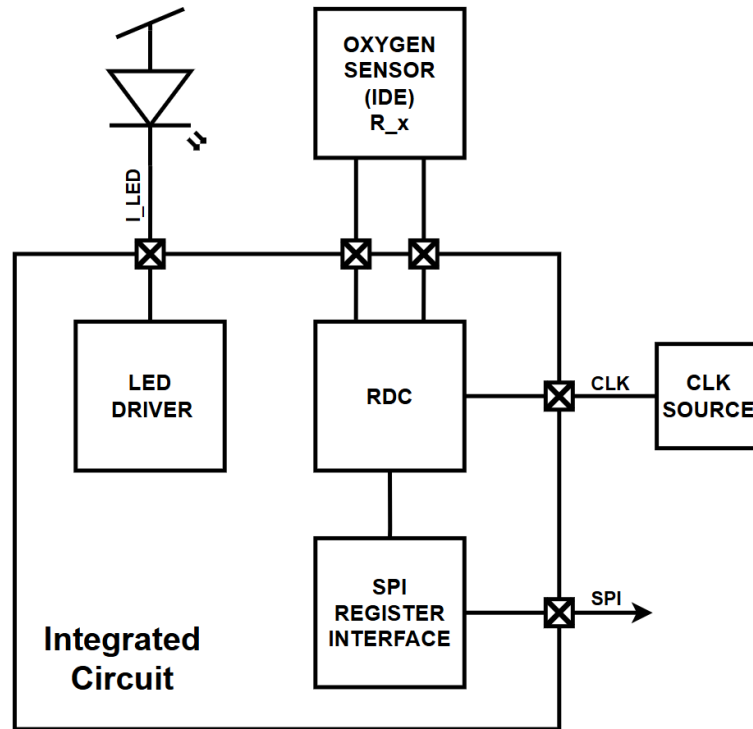


Figure 2.2: Proposed IC architecture for the photoactivated oxygen-sensing interface. The IC includes a LED current driver for optical excitation, a resistance-to-digital converter (RDC) for sensor readout, and an SPI register interface for communication. The external oxygen sensor is modeled as a two-terminal resistance R_x connected to the RDC input.

As shown in Fig. 2.2, the architecture is organized into three main functional blocks:

- **LED Current Driver:** This block generates a controlled current (I_{LED}) used to bias the external LED, enabling optical activation of the sensing material. Stable current generation is essential to ensure repeatable and consistent sensor response.
- **Resistance-to-Digital Converter (RDC):** The RDC is the core readout block of the system. It measures the external sensor, modeled as a two-terminal resistance R_x , and converts the resistance value into a digital representation using a time-based conversion method. The RDC receives a 100 MHz reference clock signal (CLK) from an external clock source to perform accurate period measurement.
- **SPI Register Interface:** The SPI interface provides communication between the IC and an external controller. It enables configuration of internal parameters, programming of calibration data, and readout of measurement results.

The external oxygen sensor, implemented using interdigitated electrodes (IDE), is connected to the IC through two terminals corresponding to the resistance R_x . These terminals are interfaced directly with the RDC input. Since the sensor is a passive two-terminal element, its behavior is fully characterized by the resistance between its terminals.

In parallel, the external LED is driven by the on-chip current driver through the signal I_{LED} , providing the optical excitation required for sensing operation. The use of an external LED allows flexibility in optical design while keeping the IC compact.

A clock input (CLK) is provided from an external clock source and is used by the RDC for time-based conversion. The digital output data is transmitted through the SPI interface, enabling integration with higher-level digital systems.

This architecture allows the integration of optical excitation control and resistance readout within a single IC, forming a compact and efficient sensor interface tailored for oxygen sensing applications.

2.3. Architecture-Level Operation

The operation of the complete interface can be described at a high level as a sequence of four steps:

1. The IC biases the external LED with a controlled current, thereby establishing the optical conditions required for sensor activation.
2. Under illumination, the sensor resistance varies according to the oxygen concentra-

tion in the surrounding environment.

3. The RDC converts the resistance-dependent analog behavior into a digital quantity by means of a time-based measurement principle.
4. The resulting digital data is made available to an external controller through the SPI interface, which also supports configuration and calibration functions.

An external reference clock is used for the digital timing and for the RDC measurement process. This choice provides stable time quantization and simplifies the synchronization of the digital backend.

The adopted architecture is intentionally mixed-signal: the sensor interaction and current excitation occur in the analog domain, whereas measurement control, data handling, and calibration are implemented digitally. This partition allows the interface to remain power efficient while preserving programmability and scalability.

2.4. Design Specifications Summary

The main design targets derived from the previous discussion are collected in Table 2.3. These parameters serve as the top-level specifications for the circuit blocks developed in the following chapters.

Parameter	Target Value
Sensor resistance range	750 Ω – 75 k Ω
Nominal baseline resistance	54.7 k Ω
Equivalent resistance change for 100 ppm O ₂	$\approx$ 274 Ω
Target RDC resolution	$\leq$ 50 Ω
LED excitation current	10 mA
Light Modulation Scheme	Continuous illumination
Clock source	External reference clock

Table 2.3: Top-level specifications adopted for the design of the sensor interface IC.

2.5. Chapter Summary

This chapter established the connection between the sensing requirements and the electrical design targets of the proposed integrated interface. The discussion started from gas-level specifications, including the oxygen measurement range and the required concentration resolution, and translated them into resistance-domain requirements that are directly usable for circuit design.

By using the measured local sensitivity around the nominal operating point, a 100 ppm oxygen variation was mapped to an electrical resistance change of approximately $274\ \Omega$. Based on this result, the RDC target resolution was set to approximately $50\ \Omega$, while the supported input range was fixed to $750\ \Omega - 75\ \text{k}\Omega$. In parallel, the photoactivation requirement led to the inclusion of a dedicated LED current-generation block targeting a nominal bias current of 10 mA.

These specifications were then used to define the overall architecture of the proposed IC, which combines optical excitation, resistance readout, and digital communication. The next chapter focuses on the detailed implementation of the resistance-to-digital conversion path, whereas the subsequent chapter addresses the LED current-generation circuitry.

3 | RDC Circuit Design

3.1. Chapter Overview

This chapter presents the design and analysis of the Schmitt trigger-based resistance-to-digital converter (RDC). The proposed RDC combines an analog relaxation oscillator with a digital back-end for period measurement, calibration, and external interfacing. The chapter covers the analog front-end, the digital processing architecture, the mixed-signal integration strategy, the calibration methodology, and the main performance metrics of the system.

The chapter is structured as follows. Section 3.2 describes the analog front-end, including the Schmitt trigger design, threshold derivations, oscillator operation and non-ideal effects. Section 3.3 presents the digital back-end, including the period counter, the calibration engine, and the SPI register interface. Section 3.4 discusses the mixed-signal interaction between the analog oscillator and the digital processing blocks. Section 3.5 introduces the calibration methodology used to linearize the count-to-resistance transfer function. Section 3.6 evaluates the system performance in terms of resolution and figure of merit. Section 3.7 summarizes the practical implementation flow and tools used in the development of the system.

3.2. Analog Front-End Design

The analog front-end of the proposed resistance-to-digital converter (RDC) is introduced in this section. Since the choice of architecture strongly impacts performance, power consumption, and scalability, the rationale behind the selected solution is first discussed, followed by the detailed circuit implementation.

3.2.1. RDC Architecture Selection Rationale

Different architectures can be used to interface resistive sensors, including resistance-to-voltage conversion followed by analog-to-digital conversion (ADC), dual-slope techniques,

or time-domain conversion methods. Among these, time-domain approaches based on relaxation oscillators represent an attractive solution for integrated sensor interfaces.

In particular, relaxation oscillator-based resistance-to-digital conversion has been widely used due to its simple architecture, direct digital output, and reduced number of analog components [9]. Unlike voltage-domain approaches, which require high-resolution analog front-end circuits and dedicated ADCs, time-based converters directly map the sensor resistance into a measurable oscillation period or frequency, thereby reducing circuit complexity, silicon area, and power consumption.

Another important advantage of oscillator-based interfaces is their suitability for wide resistance ranges. As reported in the literature, relaxation oscillator architectures can support large dynamic ranges while maintaining relatively low non-linearity and reduced sensitivity to circuit parameters [9]. Furthermore, the resulting quasi-digital output signal is robust and can be easily processed by digital back-end circuits or external controllers.

Alternative approaches based on resistance-to-voltage conversion followed by ADC can achieve higher accuracy, but they require more complex analog circuitry and introduce additional design overhead, especially when multiple sensing channels are needed. In contrast, oscillator-based approaches are particularly suitable for highly integrated systems and scalable sensor arrays, where simplicity and efficiency are critical [10].

For these reasons, a Schmitt trigger-based relaxation oscillator is selected in this work as the core architecture for the resistance-to-digital converter.

3.2.2. Schmitt Trigger Design

The Schmitt trigger used in this work is based on the standard 6-transistor CMOS topology. The design is adopted from [11], and it is shown in Fig. 3.1. In this topology, M_{N3} and M_{P3} act as feedback transistors, which shift the switching thresholds depending on the output state and thereby introduce hysteresis.

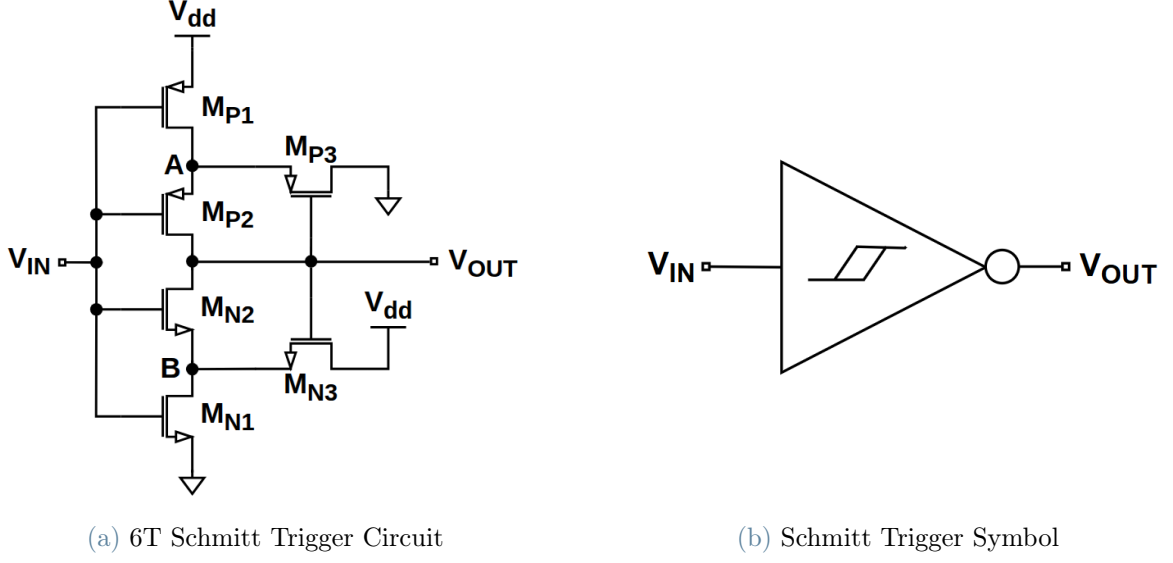


Figure 3.1: Schmitt trigger implementation used in the Proposed RDC.

3.2.3. Threshold Derivations

The threshold voltages V_{TH} and V_{TL} are derived based on the current-voltage characteristics of the N-subcircuit (M_{N1}, M_{N2}, M_{N3}) and P-subcircuit (M_{P1}, M_{P2}, M_{P3}) at the transition points.

V_{TH} Derivation (Rising Input)

When the input voltage V_{IN} is low, the output voltage is $V_{OUT} = V_{DD}$. In this condition, the feedback transistor M_{N3} is ON because its gate is connected to V_{OUT} . As a result, node **B** is pre-charged through M_{N3} , and its voltage is approximately given by

$$V_B \approx V_{DD} - V_{TN3} \quad (3.1)$$

In this initial stage, transistors M_{N1} and M_{N2} are OFF, so no current flows in the NMOS branch and the circuit remains stable. As V_{IN} starts to increase, transistor M_{N1} turns ON first and begins to sink current from node **B**, while M_{N3} tends to keep node **B** high. The switching process starts when transistor M_{N2} reaches the edge of conduction, which occurs when its gate-source voltage satisfies

$$V_{GS,N2} = V_{IN} - V_B = V_{TN} \quad (3.2)$$

This condition yields the following expression for the internal node voltage:

$$V_B = V_{IN} - V_{TN} \quad (3.3)$$

At the transition point, transistor M_{N2} is at the verge of conduction, resulting in negligible current through this branch. Therefore, by Kirchhoff's current law, the current flowing through M_{N1} must be equal to the current flowing through M_{N3} . Assuming both transistors operate in saturation, the current balance is

$$k_{N1}(V_{IN} - V_{TN})^2 = k_{N3}(V_{DD} - V_B - V_{TN})^2 \quad (3.4)$$

Substituting $V_B = V_{IN} - V_{TN}$, this simplifies to

$$k_{N1}(V_{IN} - V_{TN})^2 = k_{N3}(V_{DD} - V_{IN})^2 \quad (3.5)$$

Solving this equation gives the upper switching threshold

$$V_{TH} = \frac{V_{DD} + \sqrt{\frac{k_{N1}}{k_{N3}}} V_{TN}}{1 + \sqrt{\frac{k_{N1}}{k_{N3}}}} \quad (3.6)$$

At this point, a small increase in V_{IN} initiates the switching process, leading to a rapid transition of the output voltage. As V_{OUT} drops, the gate voltage of transistor M_{N3} decreases, weakening its pull-up effect on node **B**. This reduction further strengthens the pull-down path through M_{N1} , resulting in a regenerative transition and a fast switching of the output from V_{DD} to ground.

V_{TL} Derivation (Falling Input)

When the input voltage V_{IN} is high, the output voltage is at $V_{OUT} = 0$. In this condition, the feedback transistor M_{P3} is ON because its gate is connected to V_{OUT} . As a result, node **A** is pulled down through M_{P3} , and its voltage is approximately given by

$$V_A \approx |V_{TP3}| \quad (3.7)$$

In this initial state, transistors M_{P1} and M_{P2} are OFF, so no current flows in the PMOS branch and the circuit remains stable. As V_{IN} starts to decrease, transistor M_{P1} turns ON

first and begins to source current into node **A**, while M_{P3} tends to keep node **A** low. In this configuration, M_{P3} attempts to hold node **A** at a low potential, while M_{P1} attempts to pull it up. The switching condition is therefore determined by the balance between these opposing currents. The switching process starts when transistor M_{P2} reaches the edge of conduction, which occurs when its source-gate voltage satisfies

$$V_{SG,P2} = V_A - V_{IN} = |V_{TP}| \quad (3.8)$$

This gives the exact relation for the internal node voltage at the switching point:

$$V_A = V_{IN} + |V_{TP}| \quad (3.9)$$

At this critical condition, the current through M_{P2} is approximately zero, and by applying Kirchhoff's current law at node **A**, the current through M_{P1} must be equal to the current through M_{P3} . Assuming both transistors operate in saturation, the current balance is written as

$$k_{P1}(V_{DD} - V_{IN} - |V_{TP}|)^2 = k_{P3}(V_A - |V_{TP}|)^2 \quad (3.10)$$

Substituting $V_A = V_{IN} + |V_{TP}|$, this simplifies to

$$k_{P1}(V_{DD} - V_{IN} - |V_{TP}|)^2 = k_{P3}V_{IN}^2 \quad (3.11)$$

Solving this equation gives the lower switching threshold

$$V_{TL} = \frac{\sqrt{\frac{k_{P1}}{k_{P3}}}(V_{DD} - |V_{TP}|)}{1 + \sqrt{\frac{k_{P1}}{k_{P3}}}} \quad (3.12)$$

At this point, a small decrease in V_{IN} initiates the switching process, leading to a rapid transition of the output voltage. As V_{OUT} rises, the gate voltage of transistor M_{P3} increases, weakening its pull-down effect on node **A**. This reduction further strengthens the pull-up path through M_{P1} , resulting in a regenerative transition and a fast switching of the output from ground to V_{DD} .

3.2.4. Relaxation Oscillator and Period Calculation

The resistance-to-digital conversion is achieved using a relaxation oscillator, where the input resistance directly determines the charging and discharging dynamics of a capacitor. The Schmitt trigger provides well-defined switching thresholds, and the capacitor voltage oscillates between V_{TL} and V_{TH} , forming a hysteretic switching system [11, 12]. As a result, the oscillation period becomes a function of the unknown resistance, enabling its estimation through time-domain measurement.

Before proceeding with the mathematical derivation, it is useful to describe the overall operating principle of the relaxation oscillator. The Schmitt trigger, together with the capacitor and the input resistance, forms a feedback loop in which the capacitor voltage is periodically charged and discharged between two threshold levels [13, 14].

When the output of the Schmitt trigger is high, the capacitor charges through the input resistance. Once the capacitor voltage reaches the upper threshold V_{TH} , the Schmitt trigger switches state and its output becomes low. Consequently, the capacitor begins to discharge until it reaches the lower threshold V_{TL} , at which point the output switches again. This cyclic behavior generates an oscillation signal whose period depends on the input resistance.

The simplified schematic of the relaxation oscillator is shown in Fig. 3.2.

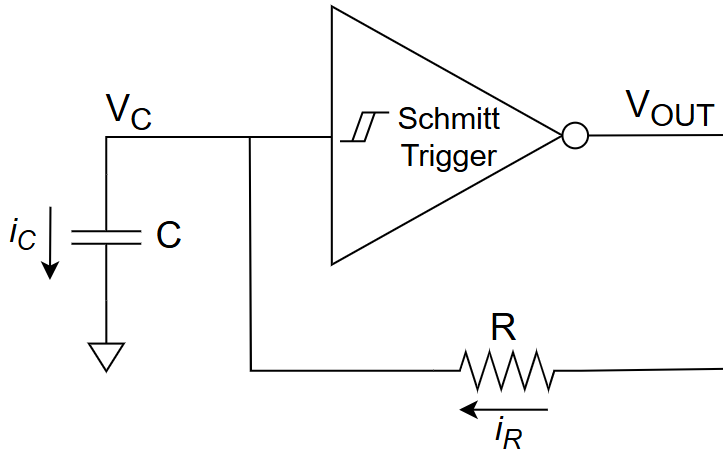


Figure 3.2: Simplified schematic of the Schmitt trigger-based relaxation oscillator used in the RDC. The resistance and the timing capacitor form a feedback loop that generates an oscillation signal with a period dependent on the resistance value.

General Time Constant Derivation

The capacitor voltage evolves according to the difference between the driving voltage and the capacitor voltage, determining the current through the input resistance. This behavior can be described using Kirchhoff's current law at the capacitor node. From first principles, the current through the capacitor i_C must equal the current through the resistor i_R . Using the constitutive relation for a capacitor and Ohm's law, the following differential equation is obtained [12, 14]:

$$C \frac{dv_c}{dt} = \frac{V_{\text{OUT}} - v_c}{R} \quad (3.13)$$

To find the time required for the voltage to change, the variables are separated and integrated:

$$\int \frac{dv_c}{V_{\text{OUT}} - v_c} = \int \frac{dt}{RC} \Rightarrow -\ln(V_{\text{OUT}} - v_c) = \frac{t}{RC} + K \quad (3.14)$$

Evaluating the integral between an initial voltage $V_C(0)$ and a final voltage $V_C(t)$, the general time equation becomes:

$$t = RC \cdot \ln \left(\frac{V_{\text{OUT}} - V_C(0)}{V_{\text{OUT}} - V_C(t)} \right) \quad (3.15)$$

Charging Phase (t_{charge})

During the charging phase, the Schmitt trigger output is high ($V_{\text{OUT}} = V_{DD}$). The capacitor charges from the lower threshold V_{TL} to the upper threshold V_{TH} :

$$t_{\text{charge}} = RC \cdot \ln \left(\frac{V_{DD} - V_{TL}}{V_{DD} - V_{TH}} \right) \quad (3.16)$$

Discharging Phase ($t_{\text{discharge}}$)

During the discharging phase, the Schmitt trigger output is low ($V_{\text{OUT}} = 0$). The capacitor discharges from the upper threshold V_{TH} to the lower threshold V_{TL} :

$$t_{\text{discharge}} = RC \cdot \ln \left(\frac{V_{TH}}{V_{TL}} \right) \quad (3.17)$$

Total Period Calculation

The total period T of one oscillation is the sum of the charging and discharging times:

$$T = t_{\text{charge}} + t_{\text{discharge}} \quad (3.18)$$

which can be written as

$$T = RC \cdot \ln \left(\frac{V_{DD} - V_{TL}}{V_{DD} - V_{TH}} \cdot \frac{V_{TH}}{V_{TL}} \right) \quad (3.19)$$

This result shows that the oscillation period is proportional to the input resistance R . Therefore, by measuring the oscillation period, the unknown resistance can be accurately reconstructed, forming the basis of the resistance-to-digital conversion. It is also important to note that the oscillation period is not purely proportional to R , but also depends on the ratio of the Schmitt trigger thresholds V_{TH} and V_{TL} . Therefore, any variation in these thresholds directly affects the linearity of the resistance-to-period conversion.

3.2.5. Non-Ideal Effects

In practice, the performance of the proposed RDC system is influenced by several non-idealities arising from both the analog oscillator and device-level variations. These effects lead to deviations in the oscillation period and therefore directly impact the accuracy of the resistance-to-digital conversion.

Schmitt Trigger Threshold Voltage Shift

The oscillation frequency is strongly dependent on the upper and lower switching thresholds (V_{TH} and V_{TL}) of the Schmitt trigger. In ideal analyses, these thresholds are often assumed to be constant. However, in practical CMOS implementations, the switching thresholds depend on the operating point of the circuit and are influenced by internal node voltages and bias conditions [11–13].

In particular, any variation in V_{TH} or V_{TL} directly modifies the charging and discharging time of the timing capacitor, as observed in the period expression derived in Section 3.2.3. These variations alter the effective switching points of the relaxation oscillator, leading to a resistance-dependent distortion in the oscillation period. As a result, even small deviations in the threshold voltages introduce non-linear distortion in the resistance-to-period relationship.

To evaluate this effect, the block-level configuration of the relaxation oscillator shown in Fig. 3.3 is used. In this representation, the sensor is modeled as a variable resistance R_x , and the oscillator consists of a Schmitt trigger, a timing capacitor, and a feedback resistance network. This abstraction allows isolating the functional dependence of the thresholds on the sensor resistance without introducing unnecessary circuit-level complexity.

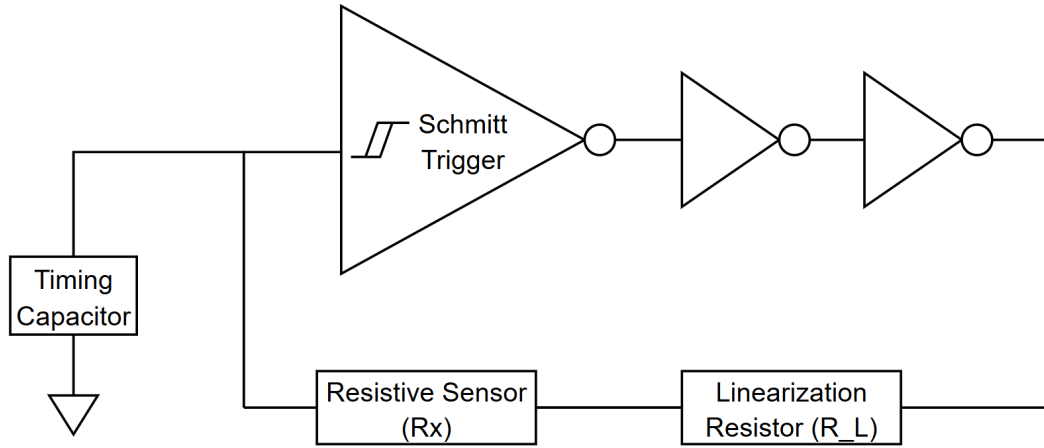


Figure 3.3: Block-level representation of the relaxation oscillator used for threshold extraction. The sensor resistance R_x is swept across its operating range, and the corresponding Schmitt trigger threshold voltages V_{TH} and V_{TL} are measured.

By sweeping the sensor resistance R_x over the full operating range, the corresponding switching thresholds are extracted from transient simulations. This approach enables direct observation of how the Schmitt trigger behavior varies with the oscillator operating point.

The variation of the upper threshold voltage is shown in Fig. 3.4. It can be observed that V_{TH} decreases as the sensor resistance increases. This behavior is attributed to the shift in internal node voltages caused by the change in charging and discharging dynamics of the capacitor.

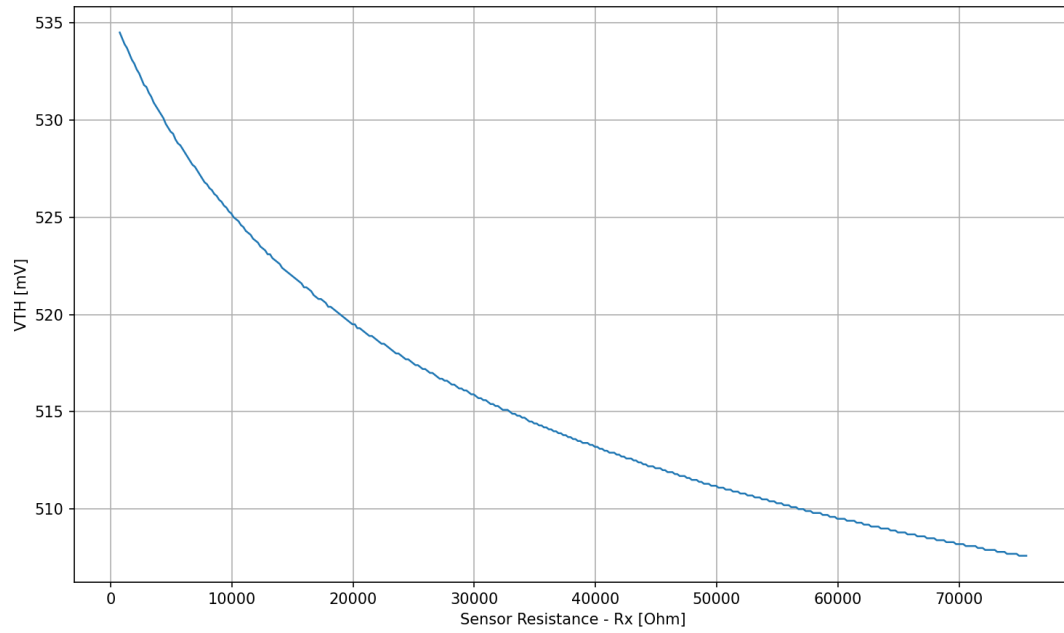


Figure 3.4: Variation of the upper switching threshold V_{TH} as a function of the sensor resistance R_x .

Similarly, the variation of the lower threshold voltage is shown in Fig. 3.5. In contrast to V_{TH} , the lower threshold V_{TL} increases as the sensor resistance increases.

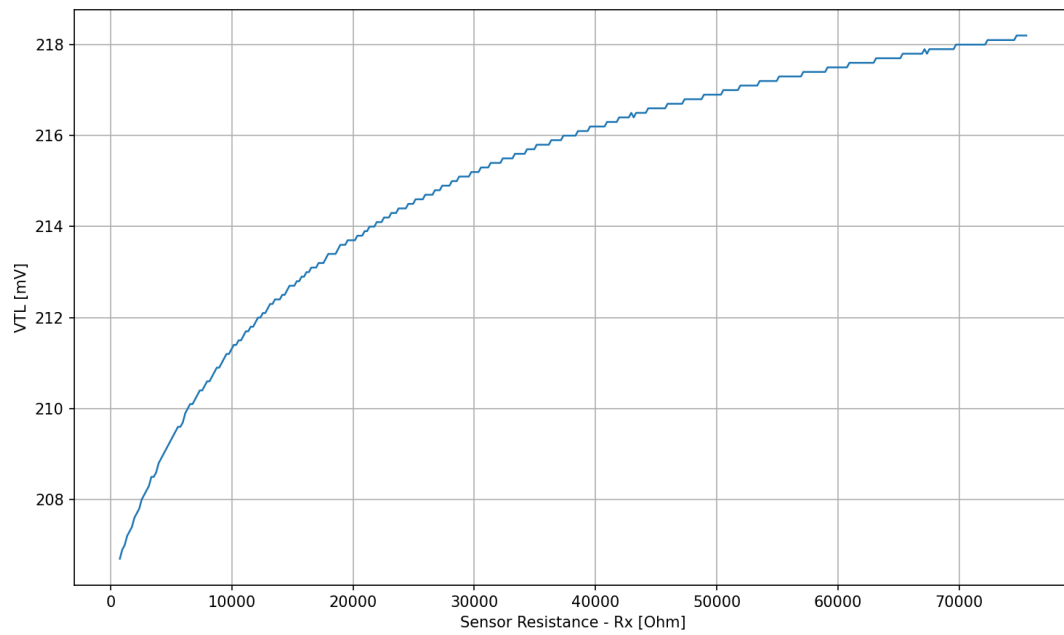


Figure 3.5: Variation of the lower switching threshold V_{TL} as a function of the sensor resistance R_x .

As a result of these opposing trends, the hysteresis window ($V_{TH} - V_{TL}$) decreases with increasing resistance. This reduction directly affects the oscillation period and introduces a resistance-dependent distortion.

Since the oscillation period depends on the switching thresholds V_{TH} and V_{TL} , any variation of these thresholds directly introduces distortion in the resistance-to-period relationship. In particular, the resistance-dependent shift of the Schmitt trigger thresholds leads to a non-linear mapping between resistance and oscillation period.

Effect of the Linearization Resistor

As discussed in the previous subsection, the variation of the Schmitt trigger thresholds introduces a resistance-dependent distortion in the oscillation period.

To partially mitigate this effect, a linearization resistor R_L is introduced in series with the sensor resistance. The role of this resistor is to modify the effective charging and discharging dynamics of the timing capacitor, thereby reducing the sensitivity of the oscillation period to threshold variations.

In particular, the presence of R_L reduces the relative influence of threshold variations on the effective voltage swing experienced by the capacitor. As a result, the dependence of the oscillation period on the threshold values becomes less pronounced.

Fig. 3.6 shows the oscillation period as a function of sensor resistance for both configurations, with and without the linearization resistor. The simulated characteristics are also compared with the corresponding ideal linear trends. It can be observed that the inclusion of the linearization resistor modifies the overall slope and reduces part of the non-linear distortion in the period response.

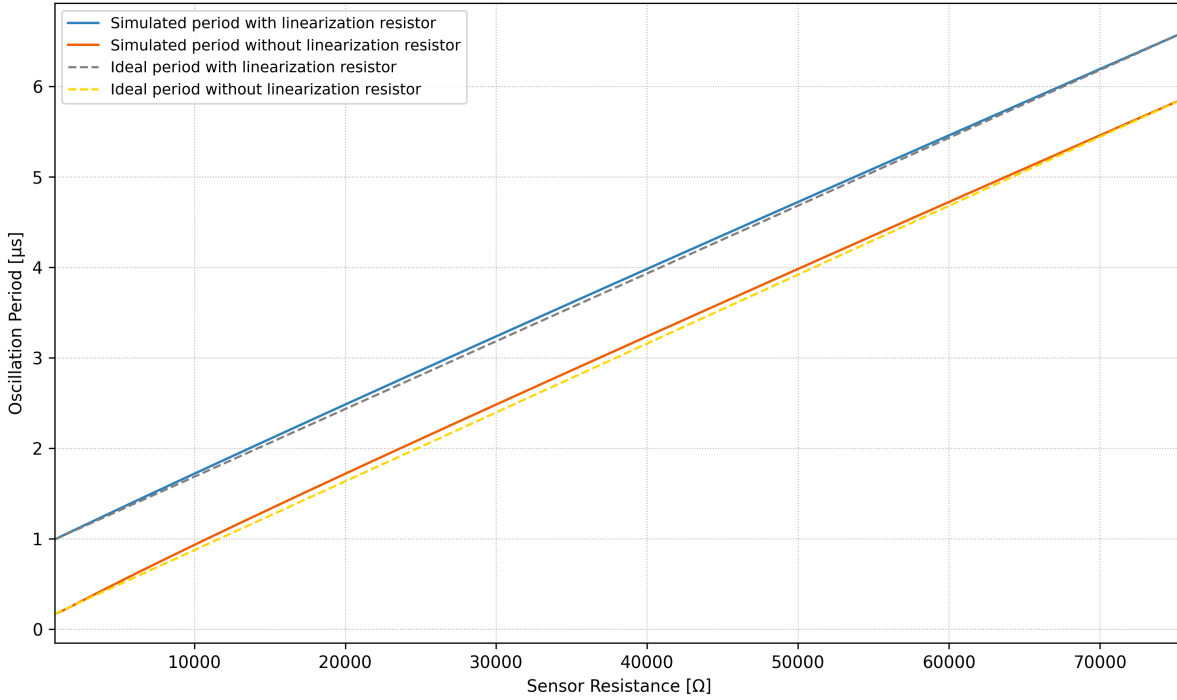


Figure 3.6: Oscillation period as a function of sensor resistance with and without the linearization resistor. The simulated characteristics are compared with the corresponding ideal linear trends, illustrating the effect of the linearization resistor on the overall transfer behavior.

While the improvement can be qualitatively observed from the transfer characteristic, a more direct evaluation of the non-linearity reduction is obtained by analyzing the period error.

Fig. 3.7 shows the period error as a function of the sensor resistance for both cases. The error is defined with respect to the corresponding ideal linear behavior. Without the linearization resistor, the error exhibits a pronounced curvature over the full range, reflecting the strong non-linear dependence of the oscillator period on resistance.

When the linearization resistor is introduced, the error profile becomes significantly flatter, indicating that the deterministic non-linearity of the system is reduced. This demonstrates that the linearization resistor effectively compensates part of the resistance-dependent distortion introduced by the variation of the Schmitt trigger thresholds.

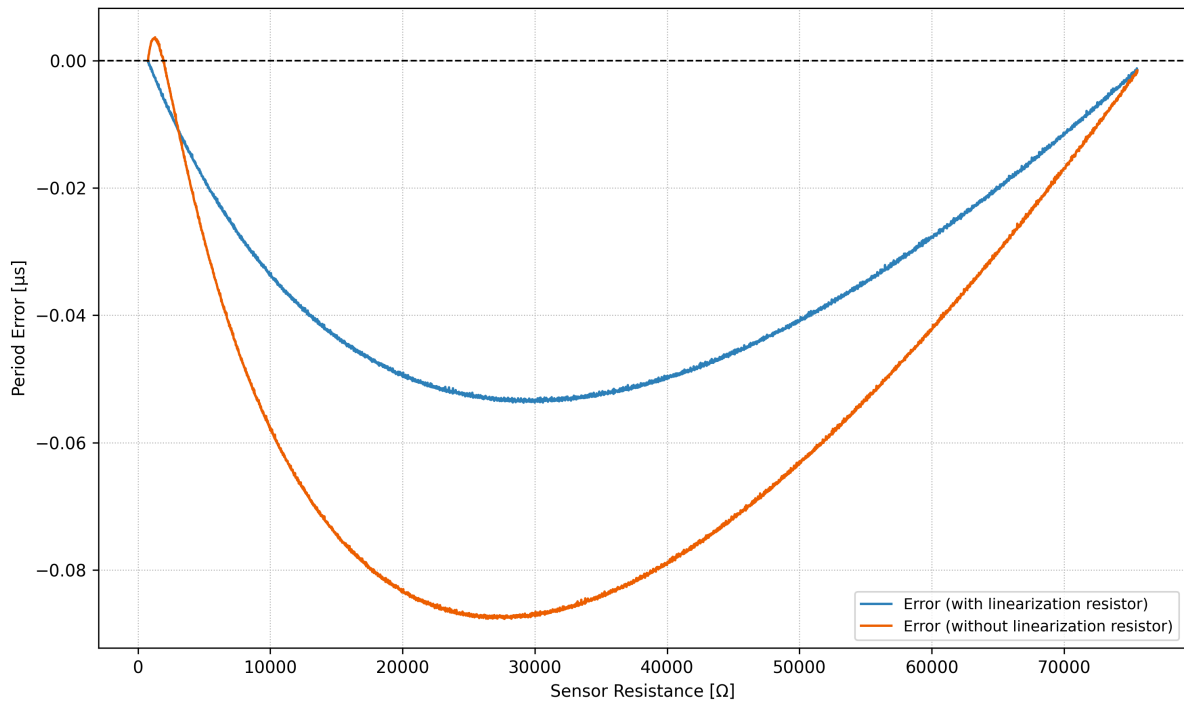


Figure 3.7: Period error as a function of sensor resistance with and without the linearization resistor. The inclusion of the linearization resistor reduces the curvature of the error profile, improving the linearity of the RDC transfer characteristic.

However, it is important to emphasize that this approach does not completely eliminate the non-linearity. Residual error remains across the operating range, which motivates the use of digital calibration techniques, as discussed in Section 3.5.

Process, Voltage, and Temperature (PVT) Variations

In addition to the intrinsic non-linearity caused by threshold variations, the performance of the proposed RDC is also affected by process, supply voltage, and temperature variations.

These variations influence key device parameters such as threshold voltage, carrier mobility, and parasitic capacitances. As a result, both the Schmitt trigger switching thresholds and the effective charging and discharging dynamics of the timing capacitor are modified. Consequently, the oscillation period becomes dependent not only on the input resistance, but also on the operating conditions of the circuit.

Temperature variations affect carrier mobility and threshold voltage, leading to changes in the oscillation period and in the switching thresholds. Similarly, supply voltage fluctuations directly impact the Schmitt trigger thresholds and the amplitude of the capacitor voltage swing, further altering the timing behavior of the oscillator.

Process variations introduce deviations in device parameters across different circuit instances, resulting in variations in the nominal transfer characteristic from chip to chip. In contrast to temperature and voltage effects, these variations are typically static after fabrication.

Digital PWL calibration is effective in compensating for static non-linearities and process-induced variations in the transfer characteristic. However, it does not inherently correct dynamic variations caused by temperature and supply fluctuations, unless calibration is performed under the same conditions or updated adaptively. Therefore, residual errors due to PVT variations remain and represent an important limitation of the system.

Summary of Non-Ideal Effects

The dominant non-idealities in the proposed RDC can be categorized into two main groups: deterministic distortions and environmental variations.

Deterministic effects, such as the dependence of the Schmitt trigger thresholds on the operating point, introduce systematic non-linearity in the resistance-to-period characteristic. These effects can be partially mitigated at the circuit level using techniques such as the linearization resistor, and further corrected through digital calibration.

In contrast, process, voltage, and temperature variations introduce shifts in the transfer characteristic due to changes in device parameters and operating conditions. While process-induced variations can be compensated through calibration, temperature and supply-related variations result in residual errors, as they are not inherently corrected by static calibration.

Overall, these non-idealities define the accuracy limits of the proposed RDC and motivate the combined use of analog design techniques and digital calibration.

3.3. Digital Back-End Design

The digital back-end acts as the computational core of the RDC system, transforming the raw asynchronous oscillation from the analog front-end into a calibrated digital representation of resistance. The architecture is designed for high-resolution reciprocal counting and real-time linearization using a programmable hardware engine [12, 13].

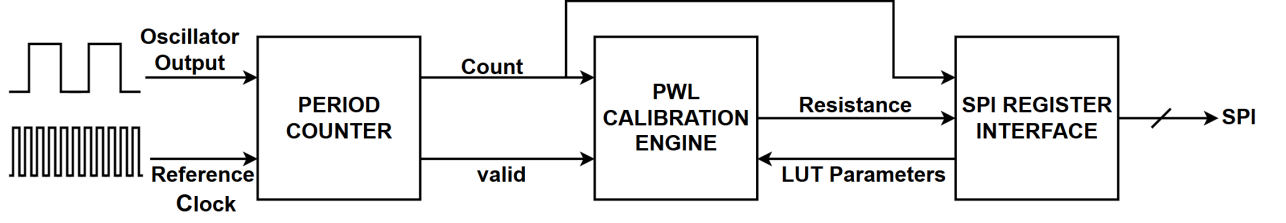


Figure 3.8: Proposed digital back-end architecture illustrating the Input Synchronizer, Period Counter, and PWL Calibration Engine.

3.3.1. Signal Synchronization and Edge Detection

Since the relaxation oscillator operates as an independent analog block, its output (**Oscillator Output**) is asynchronous to the 100 MHz (**Reference Clock**) digital system clock. Processing such a signal directly would lead to metastability and unpredictable digital behavior [13].

To mitigate this, a three-stage flip-flop synchronizer is implemented at the input. This chain reduces the probability of metastability to an acceptably low level. Following synchronization, a transition-sensing logic identifies the rising edges of the oscillator, providing a single-cycle pulse that triggers the counting logic.

To maintain high resolution across the wide sensor resistance range (750 Ω to 75 $k\Omega$), the system utilizes the *reciprocal counting* method. Instead of counting oscillator cycles over a fixed time window, this block measures the number of high-speed reference clock cycles (N_{clk}) over a predefined number of oscillator edges (**EDGE_SPAN**) [12].

The measurement sequence consists of two primary phases:

1. **Transient Blanking:** The system ignores the first N pulses (set by **TARGET_START**) to ensure the analog relaxation oscillator has reached a stable steady-state, avoiding power-on measurement artifacts.
2. **Reference Accumulation:** A counter accumulates the 100 MHz clock cycles over a predefined number of oscillator. The accumulation continues until the oscillator edge counter reaches the **EDGE_SPAN** limit.

In practice, the number of oscillator edges is fixed to **EDGE_SPAN**, and the accumulated clock cycles correspond to the total measurement duration over multiple oscillation periods.

The resulting count represents the total measured time interval and can be expressed as:

$$\text{Count} = \frac{T_{\text{meas}}}{T_{\text{clk}}} = \frac{N_{\text{edges}} \cdot T_{\text{osc}}}{T_{\text{clk}}} \quad (3.20)$$

The meaning of this expression can be understood by interpreting the measurement process in the time domain. The oscillator produces a periodic signal with period T_{osc} . The measurement is performed over a fixed number of oscillation cycles, defined by `EDGE_SPAN`. Therefore, the total measurement time can be written as:

$$T_{\text{meas}} = N_{\text{edges}} \cdot T_{\text{osc}} \quad (3.21)$$

During this time interval, a counter driven by the reference clock accumulates the number of clock cycles. Since each clock cycle has a duration of T_{clk} , the total number of counted cycles is given by:

$$\text{Count} = \frac{T_{\text{meas}}}{T_{\text{clk}}} \quad (3.22)$$

where T_{osc} is the oscillation period, T_{clk} is the reference clock period, and N_{edges} is fixed by `EDGE_SPAN`.

This formulation shows that the counter performs a time-domain measurement: it quantifies how many reference clock cycles fit within a predefined number of oscillator periods.

Since the oscillation period T_{osc} is a function of the input resistance (as derived in Section 3.2.3), the measured count is directly proportional to the resistance value. Therefore, the digital back-end effectively converts the resistance-dependent time interval into a discrete count value suitable for further processing.

Because the reference clock operates at a much higher frequency than the oscillator, the time interval is measured with high resolution, thereby minimizing quantization error even for low oscillation frequencies.

3.3.2. Programmable PWL Calibration Engine

Due to the non-linear relationship between the measured count and the sensor resistance observed in the analog front-end, a digital linearization stage is required.

To perform real-time linearization in hardware without the area overhead of floating-point arithmetic, a Piecewise Linear (PWL) engine is implemented [14].

Hardware Architecture

The engine calculates the final resistance using the linear approximation:

$$R_{\text{final}} = (m_i \cdot \text{Count}) + b_i \quad (3.23)$$

where m_i and b_i are the slope and intercept for the i -th segment. The hardware identifies the correct segment using a priority-search logic that compares the input count against programmable edge boundaries stored in internal memory.

Fixed-Point Arithmetic

To ensure high precision and efficient hardware implementation, the engine utilizes Q16.16 fixed-point arithmetic. The 18-bit count is multiplied by a 32-bit slope, and the resulting 64-bit product is added to the 32-bit intercept. The final result is bit-shifted and clamped to produce the reconstructed resistance in Ohms.

3.3.3. SPI Register Interface and Memory Map

To provide flexibility and post-fabrication adjustability, the digital back-end features an SPI-accessible register map. This allows an external controller to program the Look-Up Tables (LUTs) for the PWL engine.

These registers are programmed during the calibration phase and remain fixed during operation, enabling real-time resistance reconstruction.

Table 3.1: Register Map for Digital Back-End Configuration.

Address Range	Name	Description
0x0000 – 0x0018	edge_mem	PWL Segment Boundaries (Edges)
0x0100 – 0x0117	m_mem	Segment Slopes (m_i) in Q16.16
0x0200 – 0x0217	b_mem	Segment Intercepts (b_i)

This digital architecture enables the transformation of the analog time-domain signal into an accurate resistance estimate while maintaining low computational complexity and scalability.

3.4. Mixed-Signal Integration

The proposed RDC system is inherently a mixed-signal architecture, combining an analog relaxation oscillator with a digital processing back-end. The interface between these two domains plays a critical role in ensuring reliable operation, accurate time-domain measurement, and robust overall integration.

3.4.1. System-Level View

The complete system-level architecture of the proposed RDC is shown in Fig. 3.9. The analog front-end converts the sensor resistance into an oscillation signal, which is then processed by the digital back-end through synchronization, period measurement, and calibration.

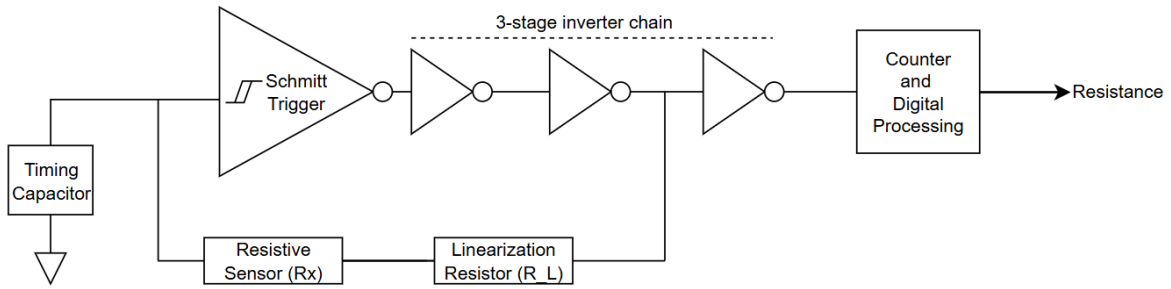


Figure 3.9: System-level architecture of the proposed RDC, illustrating the interaction between the relaxation oscillator and the digital processing blocks.

To provide a more detailed view of the implemented circuit, the transistor-level schematic of the integrated RDC is shown in Fig. 3.10.

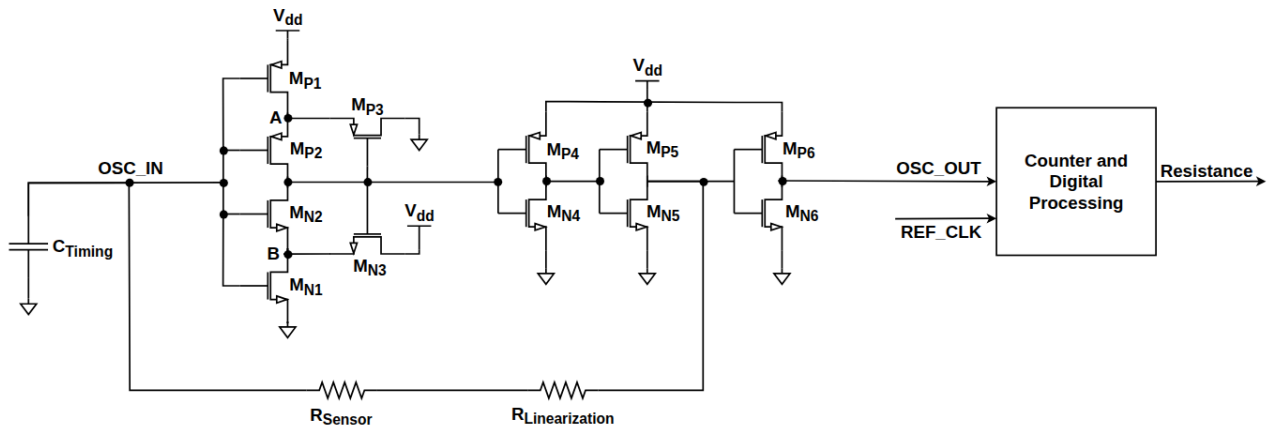


Figure 3.10: Full transistor-level implementation of the Schmitt trigger-based RDC, including the relaxation oscillator and interface to the digital back-end.

3.4.2. Time-Domain Operation

The interaction between the analog and digital domains can be understood through the time-domain behavior of the system. Fig. 3.11 shows a representative transient waveform of the RDC operation.

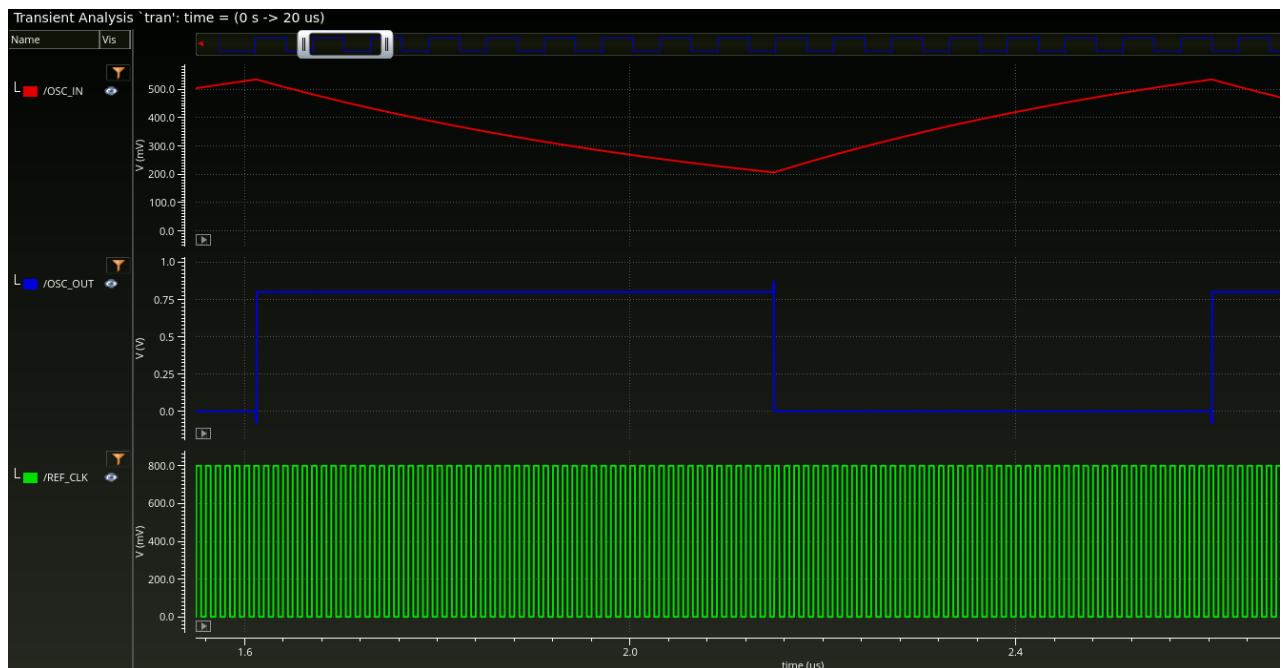


Figure 3.11: Representative transient waveforms of the RDC operation, showing the capacitor voltage, oscillator output, and reference clock used for period measurement.

The capacitor voltage exhibits a periodic charging and discharging behavior between

the Schmitt trigger thresholds, while the oscillator output provides a digital-like signal that is processed by the digital backend. The high-frequency reference clock is used to measure the duration of multiple oscillation periods, forming the basis of the time-to-digital conversion.

3.4.3. Transistor-Level Design and Sizing

The performance of the RDC strongly depends on the sizing of the transistors in the Schmitt trigger and the associated circuit components. The chosen device dimensions determine the switching thresholds, propagation delay, and overall stability of the oscillator.

The transistor sizing and key component values used in the implemented design are summarized in Table 3.2.

Table 3.2: Transistor sizing and component values of the proposed RDC front-end (matched to Fig. 3.10).

Component	Function	W/L
MP1	PMOS pull-up transistor (output stage)	10
MP2	PMOS switching transistor (input-controlled)	10
MP3	PMOS feedback transistor (hysteresis)	20
MN1	NMOS pull-down transistor (output stage)	6
MN2	NMOS switching transistor (input-controlled)	6
MN3	NMOS feedback transistor (hysteresis)	20
MP4	PMOS of inverter stage 1 (buffer)	10
MN4	NMOS of inverter stage 1 (buffer)	6
MP5	PMOS of inverter stage 2 (buffer)	66
MN5	NMOS of inverter stage 2 (buffer)	21
MP6	PMOS of inverter stage 3 (output buffer)	10
MN6	NMOS of inverter stage 3 (output buffer)	6
R_{Sensor}	Resistive Sensor	750 – 75 k Ω
$R_{Linearization}$	Linearization Resistor	10 k Ω
C_{Timing}	Timing Capacitor	50 pF

The sizing is selected to achieve a trade-off between switching speed, noise sensitivity, and power consumption. In particular, the feedback transistors control the hysteresis behavior of the Schmitt trigger, while the timing capacitor and resistive network determine the oscillation period range.

3.4.4. Analog-to-Digital Interface

The primary interaction between the analog and digital blocks occurs through the oscillator output signal. Although this signal resembles a digital waveform, it is asynchronous with respect to the system clock and must be treated accordingly.

The oscillator output is first passed through a synchronization stage implemented using a multi-stage flip-flop chain, ensuring reliable clock-domain crossing. After synchronization, rising edges are detected and used to trigger the period measurement counter.

3.4.5. Clock Domains and Synchronization

The digital system operates using a single reference clock (100 MHz), which drives all synchronous logic in the digital back-end. Since the oscillator is not aligned with this clock, a clock-domain crossing occurs at the interface.

To mitigate metastability, a multi-stage synchronizer is used, followed by edge detection logic. This ensures stable operation and prevents unpredictable behavior in the digital domain.

3.4.6. System Integration Considerations

The integration of the analog and digital subsystems introduces several important design considerations:

- integrity of the oscillator output signal at the interface,
- proper synchronization of asynchronous transitions,
- accurate time-domain measurement in the presence of noise,
- programmability of the calibration stage for system-level correction.

3.5. Calibration Methodology

This section presents the calibration methodology used to linearize the count-to-resistance transfer function and enable accurate resistance reconstruction. The proposed approach combines system-level modeling, numerical fitting, and hardware-oriented implementation strategies.

3.5.1. Need for Calibration

In an ideal time-based converter, a simple proportionality between the oscillation period and the input resistance could be assumed. However, in the proposed architecture, the oscillation period depends not only on the RC time constant but also on the threshold voltages V_{TH} and V_{TL} , as discussed in Section 3.2.3.

As a result, the relationship between the measured digital count and the sensor resistance deviates from an ideal linear behavior. This effect is illustrated in Fig. 3.12, which compares the simulated count-to-resistance characteristic with an ideal linear approximation.

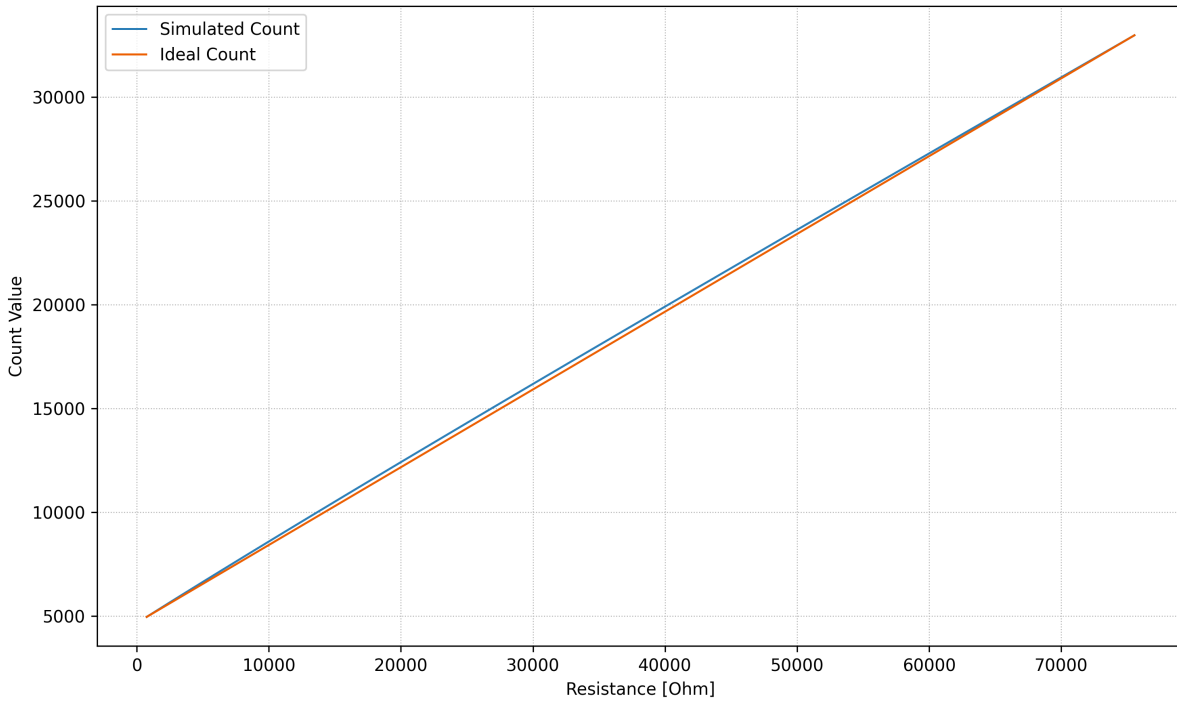


Figure 3.12: Comparison between the simulated count-to-resistance characteristic and an ideal linear approximation. The deviation between the two curves highlights the non-linear behavior of the proposed RDC.

Although the overall response remains monotonic across the full operating range, a visible deviation from linearity is observed. This deviation indicates that a direct linear mapping from count to resistance would introduce reconstruction errors.

To quantify this non-linearity more explicitly, the error between the ideal linear behavior and the simulated response is evaluated as a function of the resistance. The resulting error profile is shown in Fig. 3.13.

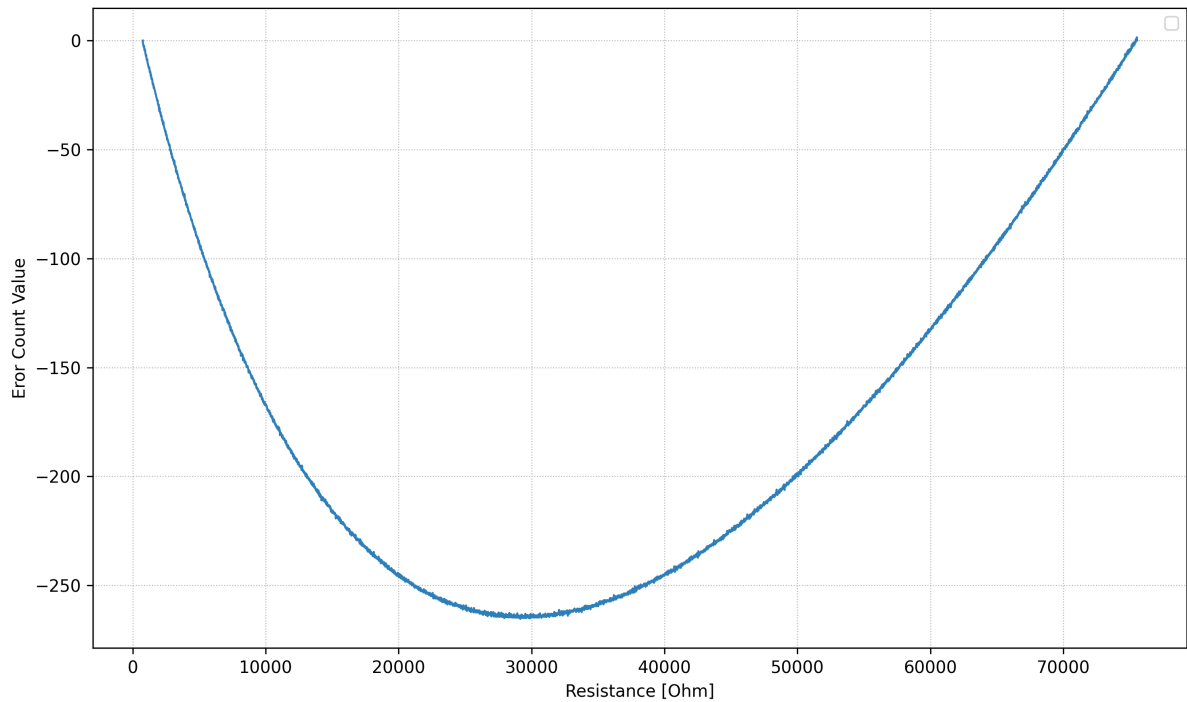


Figure 3.13: Count-to-resistance error relative to an ideal linear model, shown as a function of the sensor resistance. The pronounced curvature confirms the presence of deterministic non-linearity in the RDC transfer characteristic.

It can be observed that the error exhibits a clear non-linear behavior, with a pronounced curvature across the resistance range. This behavior arises primarily from the resistance-dependent variation of the Schmitt trigger thresholds, which modifies the effective charging and discharging dynamics of the oscillator. As a result, the oscillation period exhibits a non-linear dependence on the sensor resistance.

3.5.2. Piecewise Linear (PWL) Methodology

The relationship between the measured digital count and the sensor resistance is inherently non-linear due to the resistance-dependent variation of the Schmitt trigger thresholds, which affects the behavior of the relaxation oscillator. To enable efficient hardware implementation, this non-linear transfer characteristic is approximated using a piecewise linear (PWL) model [14].

In this approach, the full measurement range is divided into multiple segments along the count axis, and each segment is represented by a local linear function. The adopted segmentation of the measured transfer characteristic is shown in Fig. 3.14. Rather than fitting the entire range with a single global function, the PWL method approximates

the response locally, thereby reducing the calibration error while keeping the hardware complexity moderate.

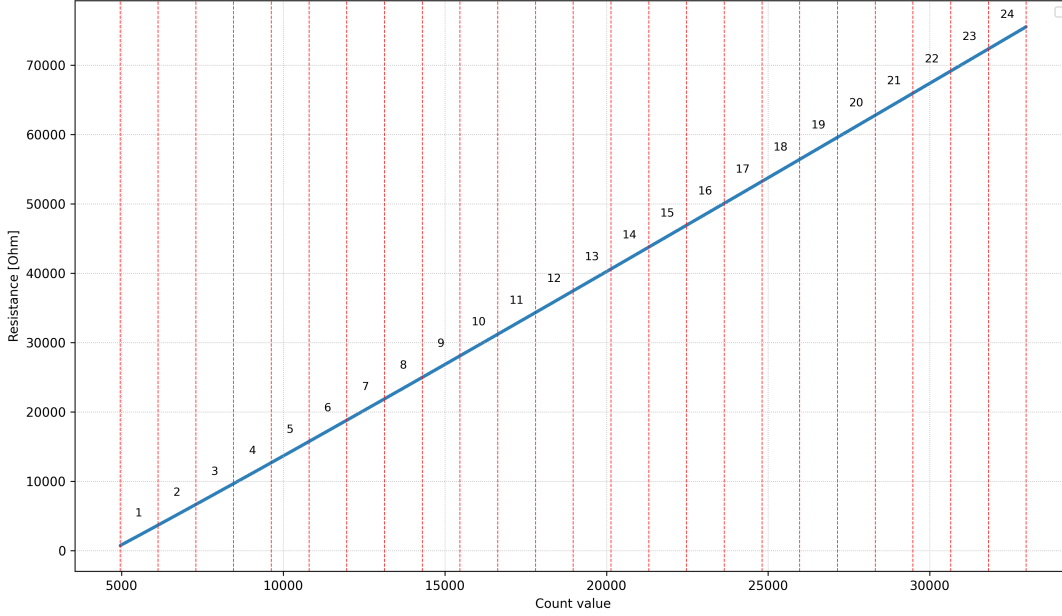


Figure 3.14: Piecewise linear segmentation of the measured count-to-resistance characteristic. The full operating range is divided into multiple count intervals, each approximated by a separate linear model.

A zoomed-in view of one representative segment is provided in Fig. 3.15, showing how the measured data points within a limited interval can be accurately approximated by a straight line. This local approximation is described by

$$R = m_i \cdot \text{Count} + b_i \quad (3.24)$$

where m_i and b_i are the slope and intercept corresponding to segment i . This formulation directly corresponds to the hardware implementation described in Section 3.3.2, where the PWL calibration engine computes the resistance using a segment-wise multiply-add operation.

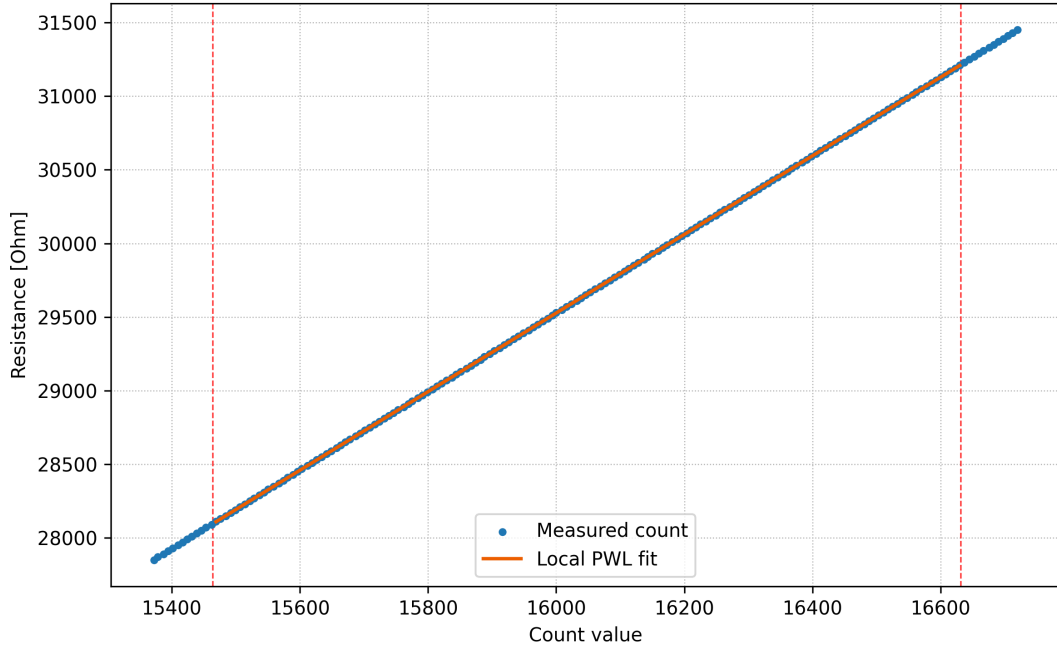


Figure 3.15: Zoomed-in view of a representative PWL segment (segment $i = 10$). Within this interval, the measured transfer characteristic is accurately approximated by a linear function with segment-specific slope and intercept parameters. The red dashed lines indicate the segment boundaries.

This approach provides a favorable trade-off between approximation accuracy and hardware complexity. Increasing the number of segments improves the approximation accuracy at the cost of additional memory and computational overhead.

3.5.3. Offline Calibration Using Python

The PWL calibration parameters are extracted using measured data and a software-based processing flow.

The calibration process starts from a dataset obtained by applying known resistance values to the RDC and recording the corresponding digital count outputs. In practice, the sensor resistance (or an equivalent programmable resistance source) is swept across the entire operating range, and for each resistance value, the corresponding digital count is measured. This results in a dataset of paired values:

$$\{(\text{Count}_k, R_k)\}, \quad k = 1, 2, \dots, N \quad (3.25)$$

The full dataset is then divided into multiple segments along the count axis, consistent with the segmentation strategy shown in Fig. 3.14. In this work, a uniform segmentation is adopted, where the count range is divided into a fixed number of equal intervals. This choice simplifies hardware implementation, as it avoids the need for irregular segment boundary storage.

For each segment, a linear approximation is obtained using least-squares regression to determine the optimal slope and intercept parameters (m_i, b_i) [15]. These parameters minimize the approximation error between the measured resistance values and the linear model. The local fitting principle within one segment is exemplified in Fig. 3.15.

The resulting coefficients are then converted into a fixed-point representation and stored in lookup tables for hardware implementation.

3.5.4. Fixed-Point Representation and Hardware Storage

The PWL coefficients (m_i, b_i) and segment boundaries are represented using fixed-point arithmetic in order to enable efficient hardware implementation.

In this work, a Q-format fixed-point representation is used, where fractional precision is preserved while maintaining simple arithmetic operations. The coefficients are precomputed offline and stored in lookup tables (LUTs).

During operation, the digital back-end performs the following steps:

- determines the segment corresponding to the measured count,
- retrieves the corresponding coefficients from the LUT,
- computes the resistance using a multiply-add operation.

This approach enables real-time resistance estimation with low computational overhead and high efficiency.

3.5.5. Calibration Flow

The complete calibration process can be summarized as follows:

1. Apply a set of known resistance values across the full operating range
2. Measure the corresponding digital count outputs from the RDC
3. Construct the (Count, R) dataset
4. Divide the count range into multiple segments

5. Perform linear fitting within each segment to obtain (m_i, b_i)
6. Convert the coefficients into fixed-point format
7. Store the parameters in LUTs via the register interface

This calibration flow is performed prior to normal operation and enables the digital back-end to reconstruct the resistance in real time using the programmed LUT parameters.

3.6. Performance Evaluation

The performance of the proposed RDC is evaluated in terms of resolution, noise-limited accuracy, and figures of merit (FoMs), following the conventions commonly used for time-based converters in the literature [16, 17].

The reported performance metrics are evaluated after applying the PWL calibration methodology described in Section 3.5, unless otherwise stated.

3.6.1. Resolution and Noise Analysis

The nominal average resolution of the RDC is determined from the overall count-to-resistance transfer characteristic. Using two representative operating points at the boundaries of the input range, the effective resolution is calculated as:

$$R_{\text{LSB}} = \frac{R_{\text{max}} - R_{\text{min}}}{\text{Count}_{\text{max}} - \text{Count}_{\text{min}}} = \frac{75150 - 750}{32833 - 4954} \approx 2.6 \, \Omega \quad (3.26)$$

This value represents an average resolution across the full input range and corresponds to the quantization-limited resolution under ideal conditions.

To evaluate the noise-limited performance, transient noise simulations were performed using a maximum noise frequency $f_{\text{max}} = 100$ MHz, consistent with the system reference clock frequency. The analysis was conducted at the worst-case operating point corresponding to the maximum sensor resistance $R_{\text{sensor}} = 75 \, \text{k}\Omega$. A total of 200 transient runs were executed to capture statistical variations.

The statistical distribution of the reconstructed resistance values obtained from the 200 transient noise simulations is shown in Fig. 3.16. The approximately Gaussian shape of the histogram confirms that the noise behavior can be modeled as a Gaussian random process and supports the use of the standard deviation as a meaningful metric for noise-limited resolution.

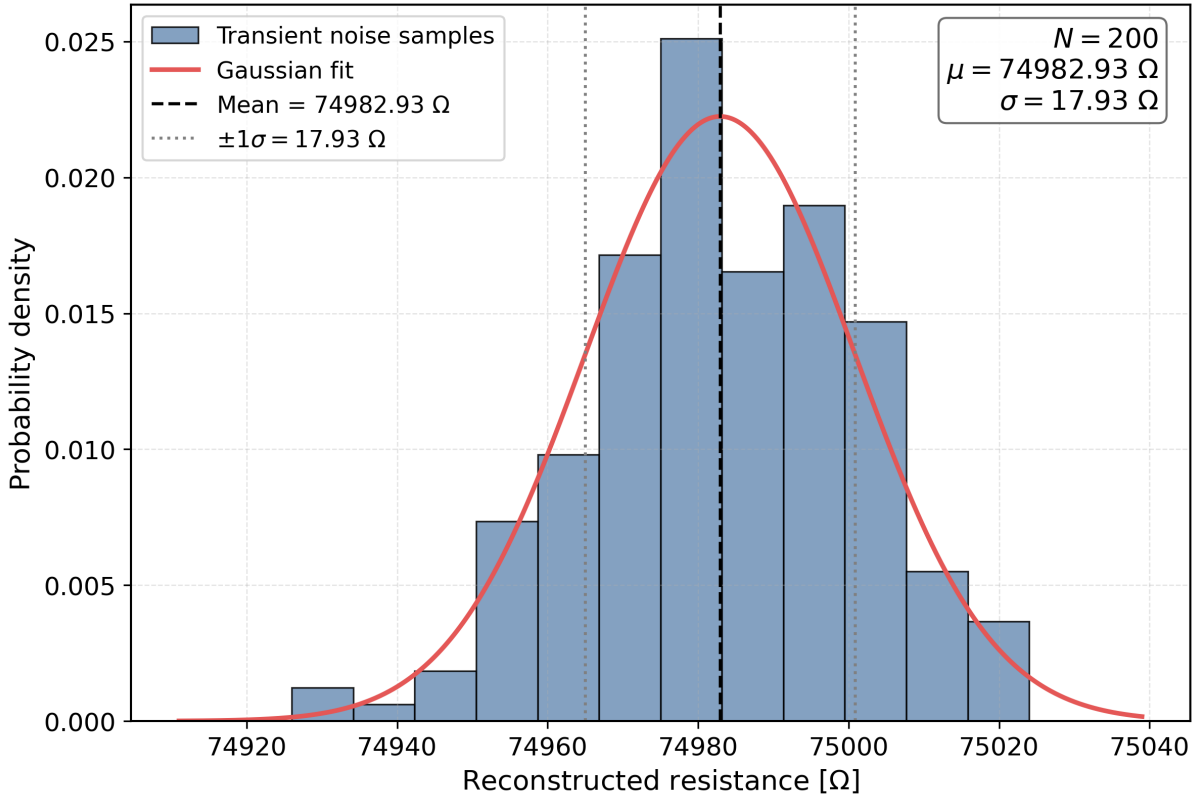


Figure 3.16: Histogram of the reconstructed resistance values obtained from 200 transient noise simulations at $R_{\text{sensor}} = 75 \text{ k}\Omega$. The distribution is approximately Gaussian, with mean $\mu = 74982.93 \Omega$ and standard deviation $\sigma = 17.93 \Omega$.

The reconstructed resistance values exhibit a standard deviation of approximately:

$$\sigma_R \approx 17.93 \Omega \quad (3.27)$$

Due to the applied calibration, deterministic non-linearities are largely compensated, and the remaining error is dominated by stochastic noise sources. Since the noise level significantly exceeds the nominal resolution ($\sigma_R \gg R_{\text{LSB}}$), the effective precision of the RDC is dominated by circuit noise rather than quantization [13].

Therefore, the practical resolution of the system is approximately 18Ω (RMS) under worst-case conditions, which satisfies the design target of $R_{\text{LSB}} \leq 50 \Omega$ defined in Chapter 2.

3.6.2. Signal-to-Noise Ratio and ENOB

Following the definition adopted in state-of-the-art RDC and ADC comparisons [12, 16, 17], the signal-to-noise ratio (SNR) is computed as:

$$\text{SNR} = 20 \log_{10} \left(\frac{R_{\text{range}}}{2\sqrt{2} \sigma_R} \right) \quad (3.28)$$

where $R_{\text{range}} = R_{\text{max}} - R_{\text{min}} = 74250 \, \Omega$.

This formulation assumes a full-scale sinusoidal equivalent input and relates the RMS noise to the peak-to-peak resistance range [12].

Substituting $\sigma_R \approx 18 \, \Omega$, the resulting SNR is:

$$\text{SNR} \approx 63.3 \, \text{dB} \quad (3.29)$$

The corresponding effective number of bits (ENOB) is obtained as:

$$\text{ENOB} = \frac{\text{SNR} - 1.76}{6.02} \approx 10.2 \, \text{bits} \quad (3.30)$$

3.6.3. Figure of Merit (FoM)

The efficiency of the converter is evaluated using both the energy-based (Walden) FoM and the signal-based (Schreier) FoM [16, 17].

The conversion time t_{conv} corresponds to the measurement duration determined by the selected EDGE_SPAN and the reference clock frequency, as described in Section 3.3.

The Walden FoM is defined as:

$$\text{FoM}_W = \frac{P \cdot t_{\text{conv}}}{2^{\text{ENOB}}} \quad (3.31)$$

while the Schreier FoM is given by:

$$\text{FoM}_S = \text{SNR} + 10 \log_{10} \left(\frac{1}{2Pt_{\text{conv}}} \right) \quad (3.32)$$

Using the measured and estimated values:

- $P \approx 50 \mu\text{W}$,
- $t_{\text{conv}} \approx 185 \mu\text{s}$,
- $\text{ENOB} \approx 10.2 \text{ bits}$,
- $\text{SNR} \approx 63.3 \text{ dB}$,

the resulting figures of merit are:

$$\text{FoM}_W \approx 7.75 \text{ pJ/conversion} \quad (3.33)$$

and

$$\text{FoM}_S \approx 140.6 \text{ dB} \quad (3.34)$$

3.6.4. Discussion

The results indicate that, while the nominal quantization resolution is approximately 2.6Ω , the effective precision is limited by circuit noise, with a standard deviation of approximately 18Ω . This corresponds to an effective resolution of approximately 10 bits.

The results also highlight an inherent trade-off between accuracy and conversion time. Increasing the observation window (e.g., larger `EDGE_SPAN`) would reduce noise through averaging, but at the cost of longer conversion time.

Furthermore, while the PWL calibration effectively compensates for deterministic non-linearity, it does not mitigate stochastic noise sources. As a result, the overall system performance is ultimately limited by noise in the oscillator and front-end circuitry.

The obtained FoM values demonstrate a favorable trade-off between energy efficiency and accuracy for a time-based RDC architecture.

3.7. Implementation and Tools

The implementation combines analog circuit design, digital hardware development, and software-based calibration using industry-standard tools and custom processing scripts.

3.7.1. Digital RTL Implementation

The digital back-end is implemented in SystemVerilog. The design includes the period measurement counter, the programmable PWL calibration engine, and the SPI register interface described in Section 3.3. These components enable real-time resistance reconstruction and external configuration of calibration parameters.

3.7.2. Analog Simulation and Data Collection

The analog front-end is simulated using Cadence-based design tools. Transient and transient noise simulations are performed by sweeping the input resistance across the target range, allowing extraction of the oscillation behavior and the corresponding digital count values under realistic operating conditions.

3.7.3. Calibration Parameter Extraction

The calibration parameters are extracted through an offline data processing flow implemented in Python. The measured count-resistance dataset is processed to determine the segment-wise PWL coefficients using least-squares fitting, as described in Section 3.5.

3.7.4. Fixed-Point Conversion and LUT Programming

The floating-point calibration parameters obtained from Python are converted into fixed-point representation to match the hardware implementation. The resulting coefficients are stored in lookup tables (LUTs) and programmed into the digital back-end through the SPI register interface.

3.7.5. Design Flow Summary

The complete implementation flow of the RDC system can be summarized as follows:

Count Extraction $\rightarrow$ Python Calibration $\rightarrow$ Fixed-Point Conversion $\rightarrow$ SPI
Programming $\rightarrow$ Real-Time Operation

This workflow establishes a direct link between circuit-level simulations and the final hardware implementation, enabling efficient calibration and accurate real-time resistance reconstruction.

4 | LED Driver Circuit Design

This chapter presents the design, the mathematical analysis, and the simulation results of the LED driver circuit. The driver is responsible for providing the stable bias current required for the optical excitation used to activate the dye-sensitized gas sensor. To ensure that the chemical response is accurately captured without artifacts, the implementation focuses on achieving high output impedance, fast startup behavior, and robustness against power supply variations. The adopted architecture follows design strategies used in low-power reflectance-mode PPG systems [18] and is aligned with integrated optical front-end solutions reported in the literature [19].

4.1. Motivation and Design Specifications

The sensing mechanism of the SWCNT-TiO₂-Re hybrid material is inherently photoactivated. As detailed in Chapter 1, the sensor resistance is only modulated by oxygen interaction when under constant green light illumination ($\lambda = 516$ nm) [1].

From an engineering perspective, any drift or noise in the LED intensity is indistinguishable from a gas-induced resistance change. Therefore, the primary requirement is a highly stable current source. While commercial solutions often provide programmable currents [19], this work targets a highly optimized, fixed-current architecture to minimize silicon area and power overhead. The target specifications for the driver are:

- **Target Current:** 10 mA fixed output.
- **Supply Voltage:** 1.8 V for internal bias, with an external 3.3 V supply for the LED branch to accommodate the high forward voltage (V_f) of green LEDs. Although the LED is biased from a higher supply, the output stage is implemented using devices compatible with 3.3 V operation, ensuring that the internal 1.8 V core circuitry is not exposed to excessive voltage stress.
- **Output Impedance:** Designed to be sufficiently high (on the order of several hundreds of k Ω to M Ω) to ensure minimal current variation across the expected output voltage swing. This is achieved using a regulated cascode structure to suppress the

effect of channel-length modulation and improve current stability [20].

4.2. System Architecture Overview

The LED driver is composed of three primary functional blocks, organized to provide a stable operating point while avoiding the degenerate zero-current states common in self-biased references [14]:

1. **Constant- g_m Reference:** Generates a stable reference current I_{ref} that is relatively independent of supply voltage [12, 13].
2. **Startup Circuit:** Ensures the reference loop exits the stable "zero-current" state upon power-up by injecting a starting charge [21].
3. **Säckinger Regulated Cascode Stage:** A high-performance output stage that mirrors I_{ref} to the 10 mA target while providing extreme output impedance via active gain-boosting [20, 22].

4.3. Constant- g_m (Beta-Multiplier) Reference

The current generator is based on a beta-multiplier topology, often referred to as a constant- g_m reference, shown in Fig. 4.1. This circuit is chosen because it defines the transconductance (g_m) of the NMOS devices primarily by a passive resistor, reducing sensitivity to process, supply voltage and temperature variations [12, 14].

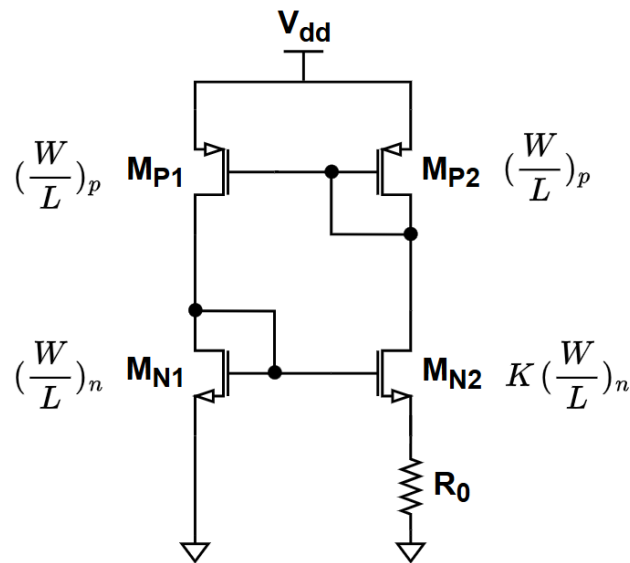


Figure 4.1: Simplified schematic of the constant- g_m (beta-multiplier) current reference used for core bias generation.

4.3.1. Qualitative Operation

The circuit consists of a PMOS mirror and an NMOS mirror with a resistor R_0 in the source of one branch. The PMOS Mirrors loop forces the currents in both branches to be equal. Because M_{N2} has a larger aspect ratio than M_{N1} , the V_{GS} difference is dropped across R_0 . As described in standard literature [13], this results in a transconductance that is independent of both the MOSFET threshold voltage and the power supply.

4.3.2. Quantitative Analysis

Assuming the transistors operate in the saturation region and follow the square-law model, the gate-source voltage for the NMOS pair (M_{N1} , M_{N2}) can be expressed as:

$$V_{GS1} = V_{GS2} + I_{ref}R_0 \quad (4.1)$$

Substituting the saturation current equation $V_{GS} = V_{th} + \sqrt{\frac{2I_{ref}}{\mu_n C_{ox}(W/L)}}$, and defining the sizing ratio $K = \frac{(W/L)_2}{(W/L)_1}$, we derive the reference current as:

$$I_{ref} = \frac{2}{\mu_n C_{ox}(W/L)_1 R_0^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (4.2)$$

This expression shows that I_{ref} is independent of V_{DD} to a first-order approximation, significantly improving the Power Supply Rejection Ratio (PSRR) compared to simple resistive-biased mirrors [12].

4.4. Startup Circuitry

A well-known limitation of self-biased current references, such as the beta-multiplier circuit discussed in the previous section, is the existence of two stable operating points. In addition to the desired state where I_{ref} flows, a degenerate "zero-current" state exists where all branch currents are zero and all transistor gate-to-source voltages are below their respective thresholds [14]. To ensure that the LED driver reaches its operational state immediately upon power-up, a dedicated startup mechanism is required.

In this work, a capacitively-coupled startup circuit is implemented, based on the architecture proposed by Mandal et al. [21]. This topology is selected due to its ability to reliably force the circuit out of the zero-current state while introducing no static power consumption during steady-state operation. Compared to conventional startup circuits based on diode-connected devices or resistive leakage paths, this approach provides faster

4.4.1. Circuit Architecture

The diagram shows a CMOS inverter with a startup circuit. The inverter consists of a PMOS transistor M_{P1} and an NMOS transistor M_{N1} . The PMOS transistor M_{P1} has its source connected to V_{dd} and its gate connected to the output node. The NMOS transistor M_{N1} has its source connected to ground and its gate connected to the input node. The input node is also connected to the output node. A startup circuit is enclosed in a dashed box and includes a capacitor C_s connected between the input and output nodes. The startup circuit also includes a PMOS transistor M_{PS1} and an NMOS transistor M_{NS1} . The PMOS transistor M_{PS1} has its source connected to V_{dd} and its gate connected to the input node. The NMOS transistor M_{NS1} has its source connected to ground and its gate connected to the output node. A resistor R_0 is connected between the output node and ground. The output node is also connected to the gates of M_{P1} and M_{N1} . The input node is also connected to the gates of M_{PS1} and M_{NS1} .

4.4.2. Operational Theory and Pulse-Injection

1. **Power-On Transient:** At $t = 0$, the supply voltage V_{dd} begins to ramp up. The coupling capacitor C_S acts as a short circuit for the high-frequency components of

the ramp. As explained in [21], the voltage at the startup node (connected to C_S and the inverter input) is initially pulled high, following the relation:

$$V_{G,NS2}(t) \approx V_{dd}(t) \cdot \frac{C_S}{C_S + C_{gate,NS2}} \quad (4.3)$$

where $C_{gate,NS2}$ represents the parasitic gate capacitance of the switch. This transient voltage activates the startup condition, with M_{NS2} conducting and propagating the transient signal to the common gate node of the NMOS mirror (M_{N1} and M_{N2}).

2. **Regenerative Phase:** As the gates of M_{N1} and M_{N2} rise above V_{th} , the beta-multiplier loop enters its active region. The regenerative feedback between the PMOS and NMOS mirrors rapidly drives the branch currents toward the target I_{ref} . During this transition, the voltage at the drain of M_{N1} (the sense node) begins to rise.
3. **Steady-State Cut-off:** Once I_{ref} is established, the sensing NMOS M_{NS1} turns on, while the PMOS M_{PS1} is turned off. This auxiliary inverter flips its state, pulling the gate of the injection switch M_{NS2} to ground. This action terminates the startup pulse and ensures that M_{NS2} is completely cut off.

4.4.3. Quantitative Considerations and Efficiency

The sizing of C_S is critical to ensure a sufficient charge injection to overcome the parasitic capacitances of the main mirror. In this 22nm implementation, C_S is sized at 2 pF to guarantee startup across all PVT corners.

The primary advantage of this Mandal-type startup circuit in the context of a next-generation gas sensor interface is its power efficiency. Because the gate of M_{NS2} is held at ground during normal operation, the startup branch contributes zero static current to the system's power budget. This characteristic is vital for the low-power operation of the LED driver, as it allows for frequent, high-speed power-cycling without the energy penalty associated with traditional resistive or diode-based startup networks [18].

4.5. Säckinger Regulated Cascode Output Stage

To drive 10 mA accurately into the varying load of a green LED, a standard cascode is insufficient due to its limited output impedance. A Säckinger regulated cascode is therefore employed to improve current stability and suppress the effect of channel-length modulation [20]. The adopted architecture is also consistent with the gain-boosted current-mirror

architecture commonly used in low-power optical front-ends and fast-settling analog circuits [18, 22].

4.5.1. Circuit-Level Operation of the Regulated Cascode

To provide a circuit-level understanding consistent with the previous sections, the operation of the regulated cascode stage is described with reference to the schematic shown in Fig. 4.3.

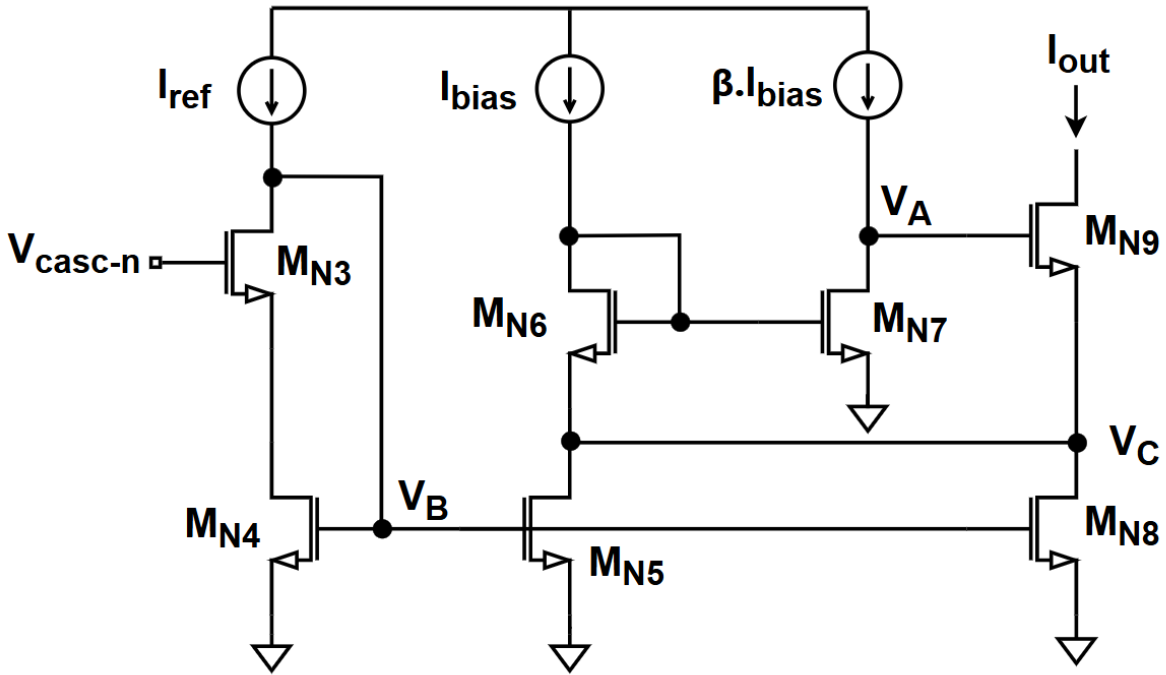


Figure 4.3: Regulated cascode output stage.

Qualitative Operation

The underlying idea of the regulated cascode is the same as in the classical enhanced-output-impedance current mirror: an auxiliary circuit senses an internal node and ensures that the drain-source voltage of the output transistor MN9 remains nearly constant, thereby increasing output resistance [20, 22].

In the implemented topology, the three current branches shown in Fig. 4.3, labeled I_{ref} , I_{bias} , and βI_{bias} , represent bias currents derived from the global current-reference network. The left branch establishes the reference-side operating point together with MN3 and MN4, while the remaining branches provide biasing for the regulating elements and the output branch containing MN9.

The key nodes are V_A , corresponds to the output node of the driver, and V_C which is the intermediate node between MN8 and MN9.

Variations at the output node V_A tend to modify the operating condition of the output transistor MN9. The regulating circuit counteracts these variations by maintaining the internal node V_C approximately constant. This ensures that the drain-source voltage of MN9 remains stable, thereby reducing current variations.

As a result, the circuit behaves as a regulated current source, where the output current is defined by the reference network and maintained through local regulation.

Relation to Classical Wide-Swing and Gain-Boosted Mirrors

The adopted structure is conceptually related to modified wide-swing current mirrors with enhanced output impedance described in the literature [20]. In these circuits, additional bias branches ensure that the output transistor remains in saturation while improving the output resistance.

Similarly, in the present implementation, the regulation ensures that the operating condition of the output branch remains stable despite variations at the output node. This leads to reduced sensitivity of the output current to voltage variations compared to conventional cascode current sources.

Small-Signal Interpretation

From a small-signal perspective, the regulated cascode behaves as a feedback structure that reduces the dependence of the output current on the output voltage.

When V_A changes, the internal regulation maintains V_C approximately constant, thereby stabilizing the operating point of MN9. This reduces the effect of channel-length modulation and increases the effective output resistance.

Compared to a simple cascode stage, this results in improved current stability.

Implications for LED Driving

For the present application, maintaining a stable output current is essential, since variations in current directly affect the optical intensity of the LED.

By stabilizing the drain-source voltage of MN9 through regulation of V_C , the circuit reduces the effect of channel-length modulation and improves current accuracy.

As a result, the regulated cascode stage offers:

- reduced sensitivity of the output current to supply and output-voltage variations;
- improved immunity to changes in LED forward voltage;
- enhanced stability of the optical excitation level delivered to the sensor.

These properties are particularly important for reliable operation of the sensing system.

4.6. Complete LED Driver Implementation

After presenting the individual building blocks of the LED driver, namely the constant- g_m reference, the startup circuitry, and the regulated cascode output stage, the complete transistor-level implementation can now be introduced.

The full LED driver schematic is shown in Fig. 4.4. This integrated view highlights how the reference generation, bias distribution, and regulated output stage are combined to realize a stable and robust current source for optical excitation.

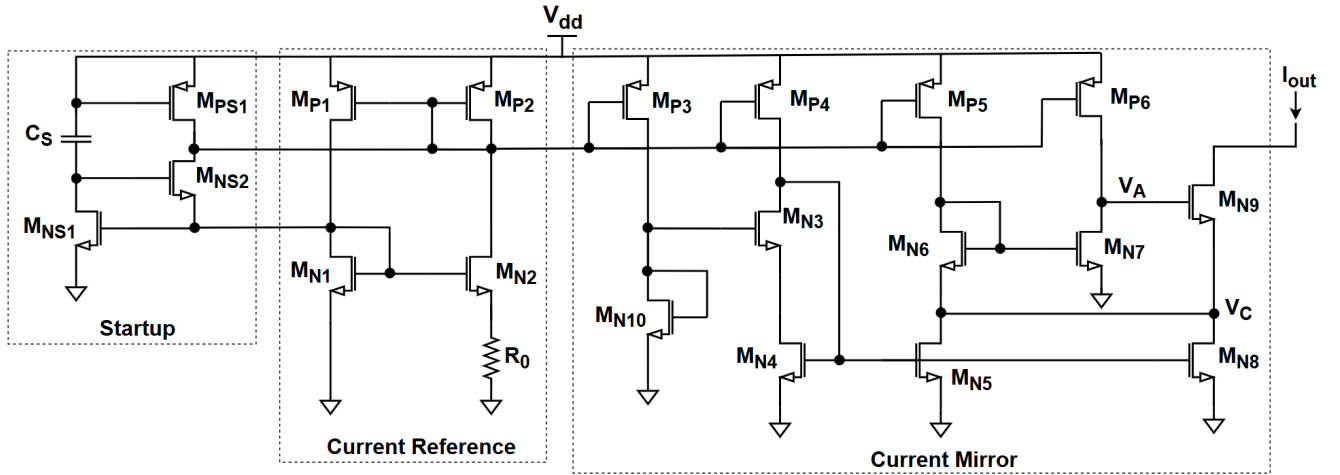


Figure 4.4: Complete schematic of the implemented LED driver, including startup circuit, constant- g_m current reference, and regulated cascode output stage.

4.6.1. Overall Operation and Current Flow

The operation of the complete LED driver can be understood by following the flow of the reference current I_{ref} through the different circuit blocks.

First, the constant- g_m reference generates a stable reference current that is largely independent of supply voltage and process variations. This current is distributed across

the circuit through current mirrors, creating the necessary bias currents for both the regulating amplifier and the output branch.

During startup, the capacitive injection circuit ensures that the reference loop exits the zero-current operating point. Once the system reaches steady-state, the startup circuitry becomes inactive and does not contribute to the static power consumption.

The regulated cascode output stage uses the reference-derived currents to establish the operating point of the output branch. The regulating loop, formed by MN6 and MN7, senses the internal node V_C and adjusts the control voltage V_A accordingly. This feedback mechanism forces the output transistor MN9 to operate under nearly constant drain-source voltage conditions.

As a result, the output current is maintained close to its nominal value, which is ultimately set by the reference circuit and its associated current-scaling ratios.

4.6.2. Transistor Sizing and Design Considerations

The relationship between the reference current and the output current is determined by the current-mirror ratios implemented in the circuit. In particular, the output branch is dimensioned such that:

$$I_{out} \approx k \cdot I_{ref} \quad (4.4)$$

where k is defined by the relative (W/L) ratios of the mirror transistors.

The transistor dimensions are expressed in terms of relative (W/L) ratios, following standard analog design practice.

Table 4.1: Transistor sizing and component values of the LED driver (matched to schematic)

Component	Function	W/L
MPS1	Startup PMOS	5
MNS2	Startup inverter NMOS	5
MNS1	Startup injection NMOS	1.3
MP1	Reference PMOS mirror	4
MP2	Reference PMOS mirror	20
MN1	Reference transistor	2.4
MN2	Reference transistor (with R_0)	800
MP3	Bias mirror PMOS	2
MP4	Bias mirror PMOS	20
MP5	Bias mirror PMOS	4
MP6	Bias mirror PMOS	16
MN3	Cascode bias transistor	10
MN10	Auxiliary bias transistor	1
MN4	Control branch transistor	10
MN6	Regulating amplifier (upper)	2
MN7	Regulating amplifier (lower)	2
MN5	Control transistor (regulation path)	2
MN8	Cascode output device	800
MN9	Output transistor (I_{out})	800
R_0	Reference resistor	2.2 k Ω
C_S	Startup capacitor	2 pF

The output transistor MN9 is intentionally sized larger to support the required 10 mA LED current, while the regulating and bias branches operate at reduced current levels to minimize overall power consumption.

The reference resistor R_0 sets the operating point of the constant- g_m reference and directly determines the generated current level. The startup capacitor C_S ensures sufficient charge injection during power-up, allowing the circuit to exit the zero-current operating state reliably.

The regulating amplifier (MN6–MN7) is dimensioned to provide sufficient loop gain for stabilization, while avoiding excessive static current consumption. The control path transistors (MN5–MN8) are sized to ensure proper transmission of the regulation signal to the output branch.

Overall, the sizing strategy balances three main objectives: achieving the desired output current level, maintaining sufficient loop gain for regulation, and minimizing power consumption in auxiliary branches.

4.6.3. Integration of Functional Blocks

The complete LED driver demonstrates how the three main functional blocks operate together as a unified system:

- The constant- g_m reference provides a stable baseline current.
- The startup circuit guarantees reliable activation under all conditions.
- The regulated cascode stage ensures high output impedance and current stability.

This partitioning enables independent optimization of each block while ensuring that the combined system meets the overall design targets.

4.6.4. Performance Evaluation

To evaluate the behavior of the implemented LED driver, transient simulations were performed under different operating conditions, including process variations, supply voltage changes, and temperature variations. The results are illustrated in Fig. 4.5–4.7.

Process Variations

The output current was analyzed across standard process corners (TT, FF, SS, SF, FS), as shown in Fig. 4.5. The simulated current values range from approximately 9.60 mA (FF corner) to 10.46 mA (SS corner).

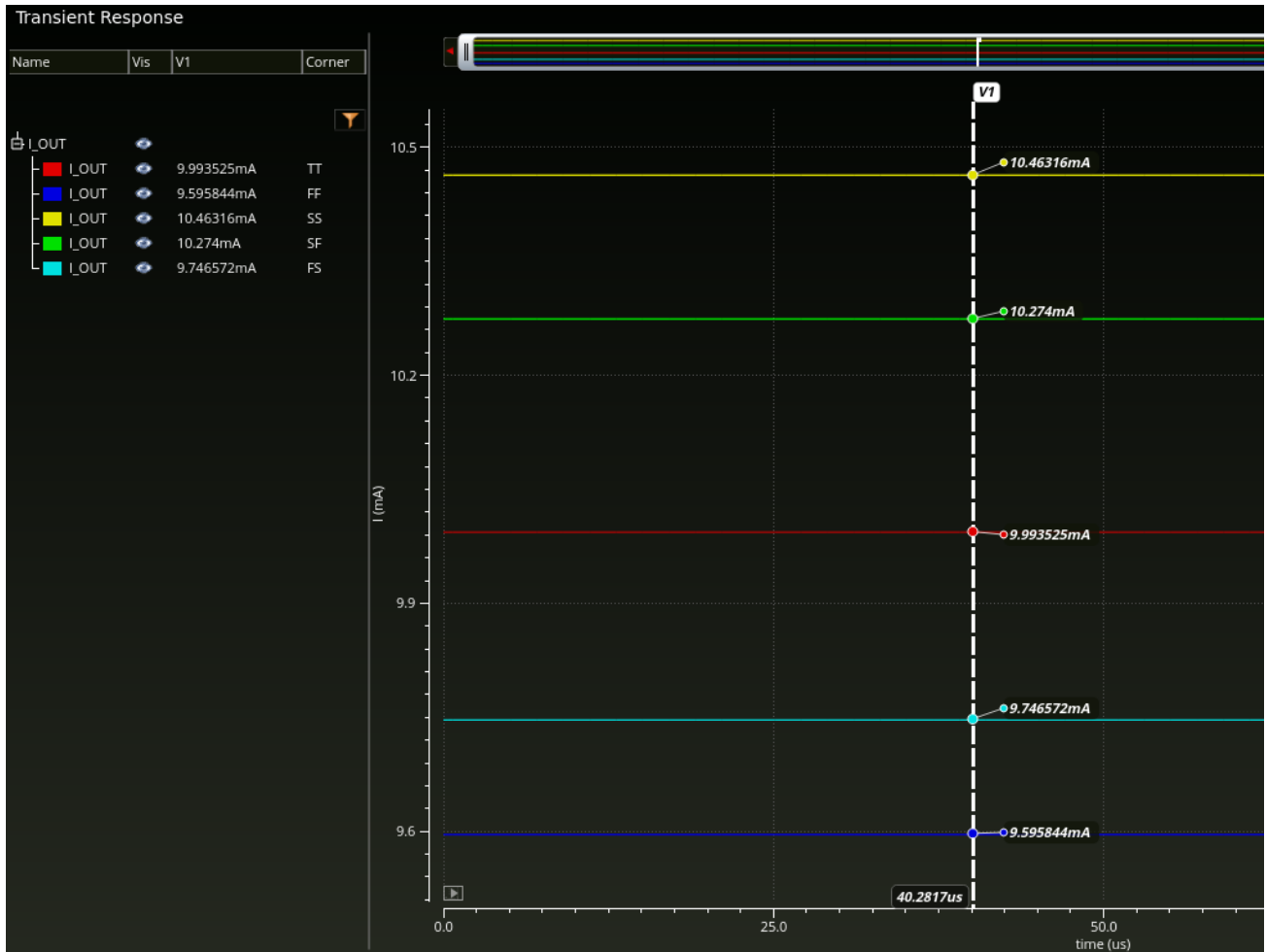


Figure 4.5: Transient response of the LED driver output current across process corners (TT, FF, SS, SF, FS).

This corresponds to a variation of approximately $\pm 5\%$ around the nominal 10 mA target. The observed deviation is mainly due to process-dependent variations in threshold voltage and carrier mobility, which directly affect the reference current circuit.

Supply Voltage Sensitivity

The supply voltage was swept between 1.5 V and 2.0 V, and the corresponding output current is shown in Fig. 4.6. The output current varies between 9.89 mA and 10.06 mA over this range.

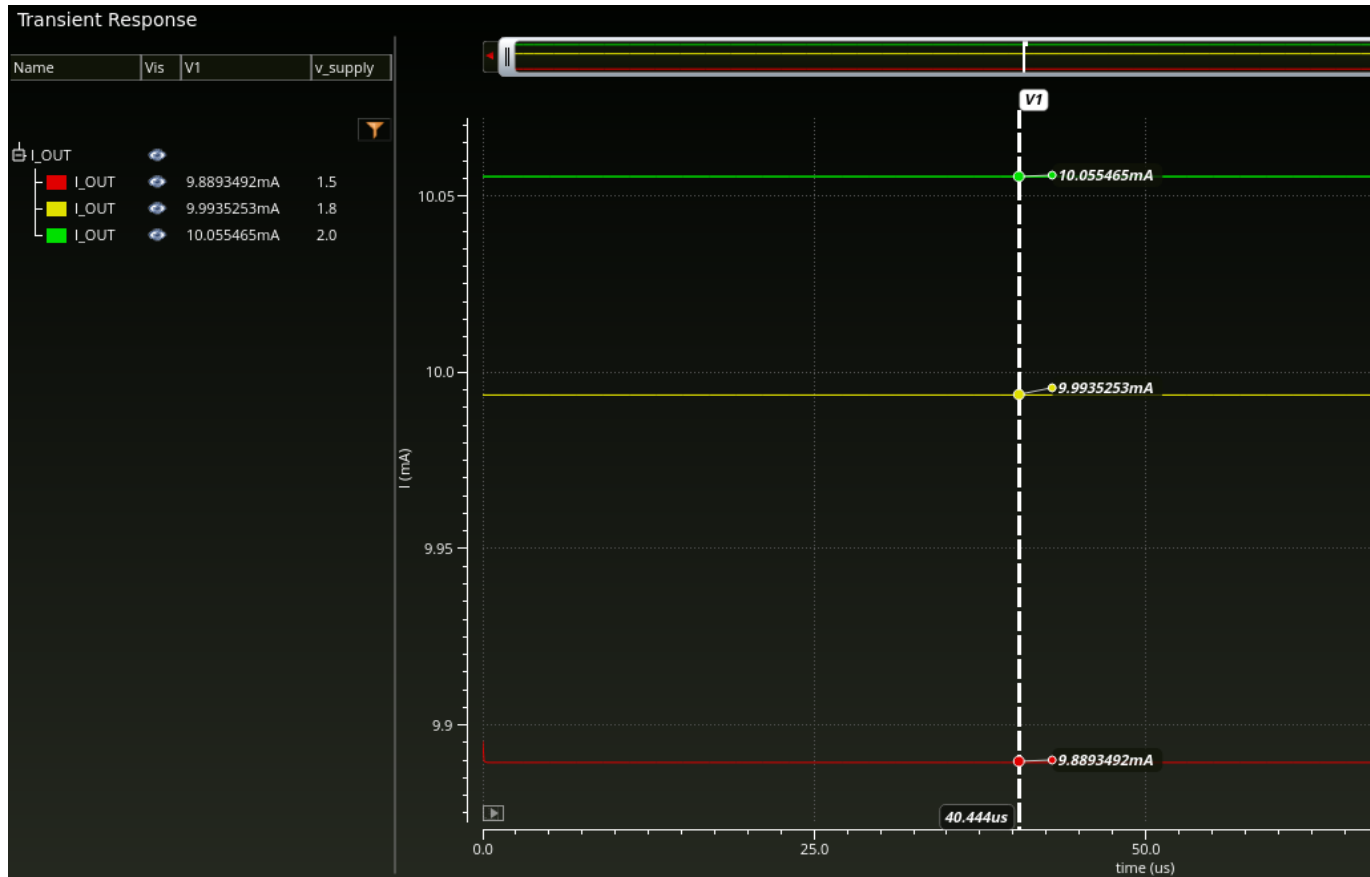


Figure 4.6: Transient response of the LED driver output current for different supply voltages (1.5 V, 1.8 V, and 2.0 V).

This corresponds to a variation of approximately $\pm 2\%$ relative to the nominal current. The relatively low sensitivity to supply voltage confirms the effectiveness of the constant- g_m reference and the regulated cascode stage in improving power supply rejection.

Temperature Dependence

The performance of the LED driver was also evaluated across temperature variations from 30°C to 40°C , as shown in Fig. 4.7. The output current varies from approximately 9.78 mA to 10.21 mA.

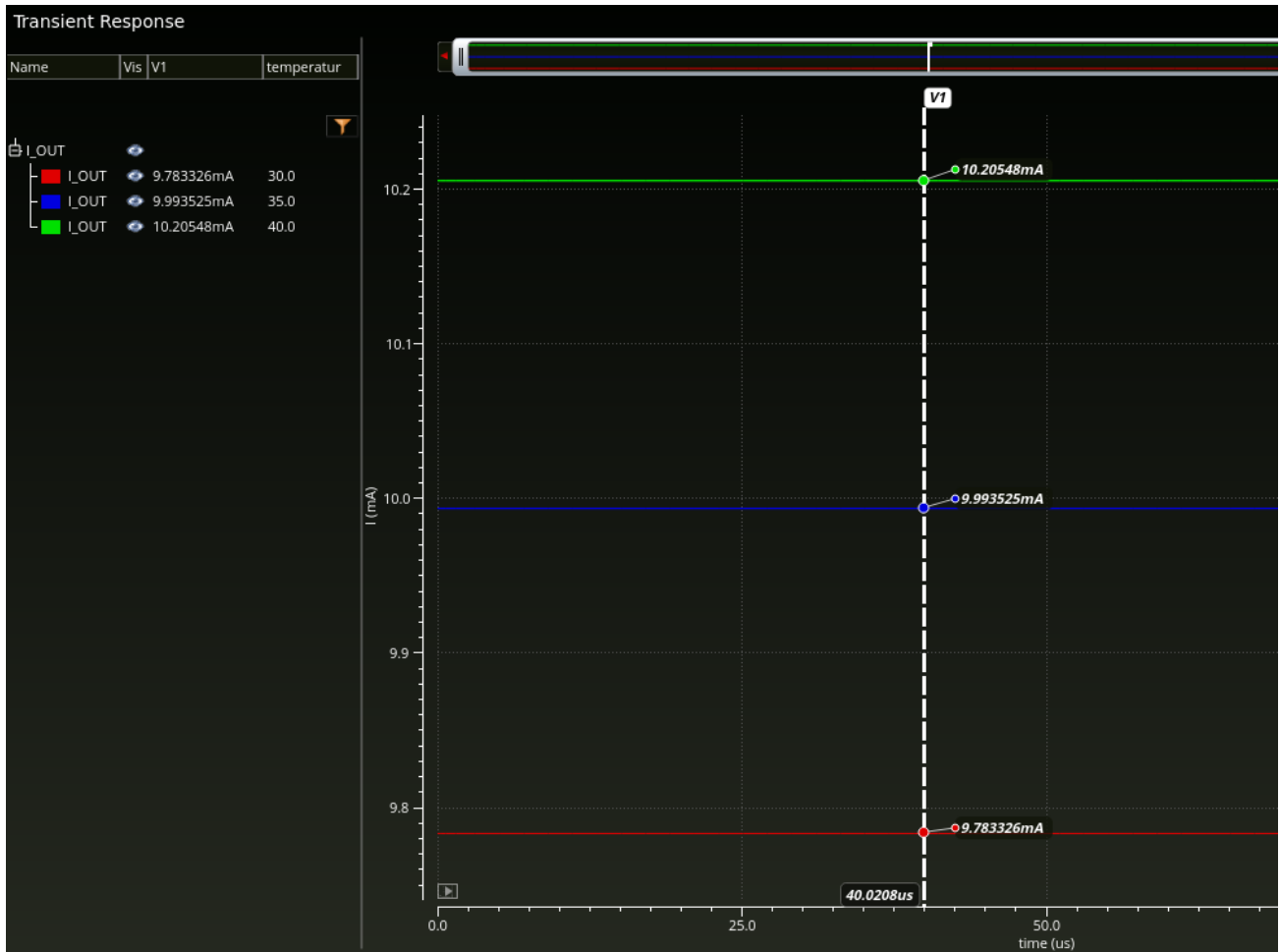


Figure 4.7: Transient response of the LED driver output current for different temperatures (30°C, 35°C, and 40°C).

This corresponds to a deviation of approximately $\pm 2\%$. The variation is primarily attributed to temperature-dependent changes in mobility and threshold voltage, which influence the reference current.

Discussion

Overall, the LED driver maintains the output current within a few percent of the target value under typical operating conditions. While ideal current invariance is not achieved, the observed variations remain within acceptable limits for the intended sensing application.

The remaining deviation is mainly due to the sensitivity of the current reference circuit.

5 | Results and Discussion

This chapter presents the final simulation-based results of the proposed mixed-signal sensor interface and discusses them with respect to the design targets defined in Chapter 2. In contrast to Chapter 3 and Chapter 4, where the circuit operation and performance evaluation methodology were introduced in detail, the present chapter focuses on the obtained results, their interpretation, and their significance at the system level.

5.1. RDC Performance

5.1.1. Transfer Characteristic

The measured transfer characteristic of the proposed RDC is shown in Fig. 5.1, where the input resistance is mapped to the corresponding digital count over the full operating range. The response is monotonic over the entire range from $750\ \Omega$ to $75\ \text{k}\Omega$, which confirms the correct operation of the Schmitt trigger-based relaxation oscillator and the reciprocal counting back-end.

As expected, the raw count-to-resistance relationship is inherently non-linear. This behavior primarily originates from the resistance-dependent variation of the Schmitt trigger thresholds, which modifies the effective charging and discharging dynamics of the relaxation oscillator, as discussed in Chapter 3.

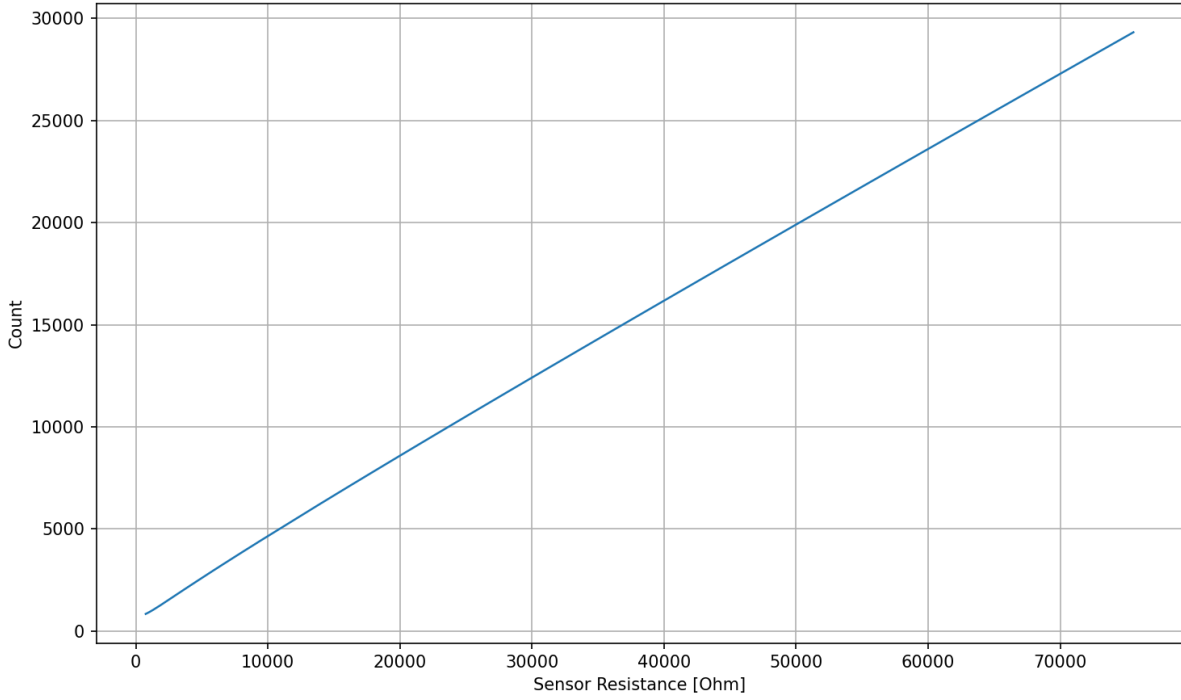


Figure 5.1: Measured transfer characteristic of the proposed RDC, showing the relationship between the input resistance and the corresponding digital count over the full operating range.

5.1.2. Calibration Accuracy

To compensate for the non-linearity of the raw transfer characteristic, the PWL calibration method described in Section 3.5 is applied. The resulting calibration accuracy is evaluated by comparing the reconstructed resistance with the original resistance used during characterization.

Fig. 5.2 shows the residual reconstruction error after calibration. The error remains bounded over the full input range, confirming the effectiveness of the adopted piecewise-linear approximation. The remaining deviation is mainly attributed to the finite number of PWL segments and to residual non-linearities that are not fully captured by the segment-wise linear model.

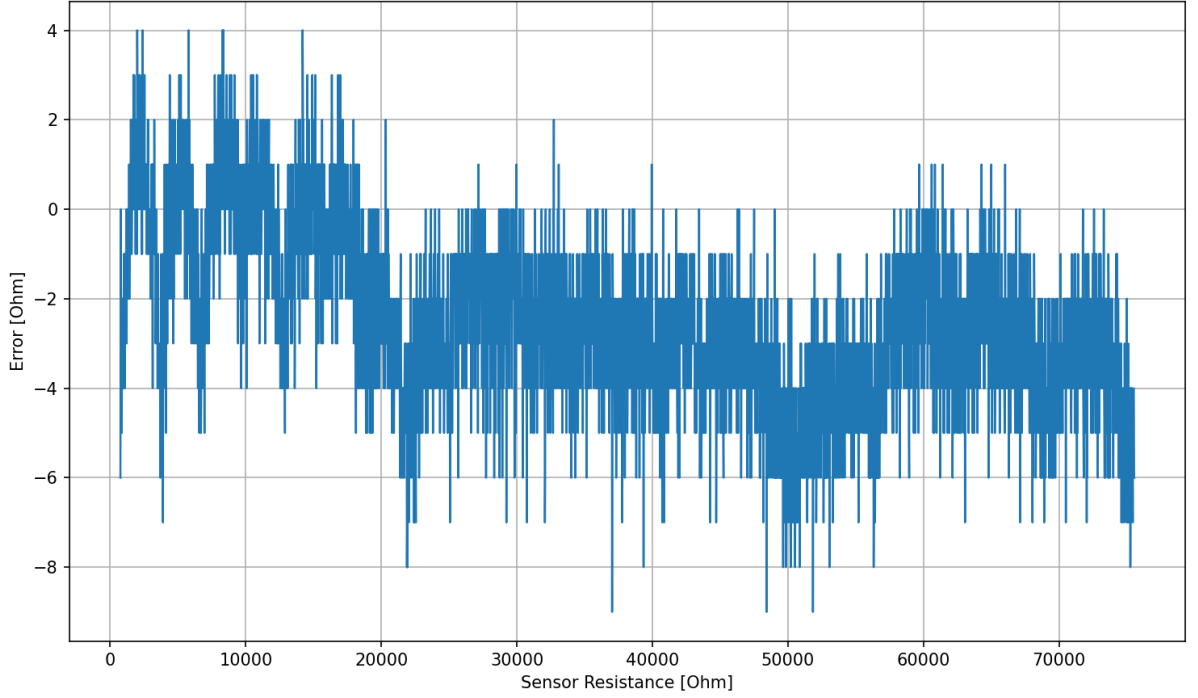


Figure 5.2: Residual reconstruction error of the calibrated RDC over the full input resistance range. The error remains bounded after applying the PWL calibration methodology.

5.1.3. Performance Summary

The nominal average resolution derived from the calibrated count-to-resistance characteristic is approximately 2.6Ω . However, transient noise simulations at the worst-case operating point ($R_{\text{sensor}} = 75 \text{ k}\Omega$) show a standard deviation of $\sigma_R = 17.93 \Omega$, indicating that the effective precision is dominated by circuit noise rather than quantization.

Consequently, the practical resolution is approximately 18Ω (RMS), which remains comfortably below the design target of 50Ω established in Chapter 2. The corresponding signal-to-noise ratio and effective number of bits are 63.3 dB and 10.2 bits, respectively. Using a conversion time of $185 \mu\text{s}$ and an estimated power consumption of $50 \mu\text{W}$, the RDC achieves a Walden FoM of $7.75 \text{ pJ/conversion}$ and a Schreier FoM of 140.6 dB.

5.1.4. Comparison with the State of the Art

Table 5.1 compares the proposed RDC with representative time-based resistive sensor interfaces from the literature. The comparison focuses on architectures that are reasonably comparable in terms of operating principle and reported performance metrics.

The compact closed-loop single-VCO architecture reported by Sacco *et al.* achieves 16.1-

Table 5.1: Performance Summary and Comparison With the State of the Art

	This work	JSSC20 [23]	JSSC13 [24]	ISSCC17 [25]	JSSC19 [26]
Topology	time (count)	time (VCO)	time (PLL)	time (FDC)	time (PLL)
Sensor type	external resistor	external resistor	external resistor	internal VCO	external resistor
Technology (nm)	22	180	130	65	180
Area (mm²)	–	0.064	0.20	0.007	0.26
Power (μW)	50	171	125	68	3410
t_{conv} (ms)	0.185	1	0.05	8	0.014
ENOB	10.2	16.1	8.9	13.6	9.9
Temp. range ($^{\circ}$C)	30 to 40	-40 to 125	-20 to 80	-40 to 85	-40 to 175
FoM_W (pJ/c.s.)	7.75	2.4	13.03	14.21	50
FoM_S (dB)	140.6	163.5	134.4	132.3	131.5

bit ENOB with a conversion time of 1 ms while consuming 171 μ W, corresponding to a Walden FoM of 2.4 pJ/c.s. and a Schreier FoM of 163.5 dB [23]. This design represents one of the most advanced high-resolution time-based RDC implementations.

Earlier time-domain interfaces, such as PLL-based and frequency-domain converters reported in [24–26], demonstrate different trade-offs between resolution, power consumption, and conversion speed. In particular, higher-resolution designs typically rely on longer observation times or more complex architectures, leading to increased conversion times.

Compared to these works, the proposed RDC operates with a significantly shorter conversion time of 185 μ s, while maintaining competitive energy efficiency with a Walden FoM of 7.75 pJ/conversion. Although the achieved resolution of 10.2 bits is lower than that of long-conversion high-resolution designs, the proposed architecture offers a favorable trade-off between conversion speed, hardware simplicity, and energy efficiency.

This makes the proposed RDC particularly well suited for real-time resistive sensing applications, where fast measurement and moderate resolution are preferred over ultra-high precision.

5.1.5. Discussion

The obtained results confirm that the proposed RDC successfully meets the electrical design targets derived in Chapter 2. In particular, the effective resolution of approximately 18 Ω is significantly better than the required 50 Ω , ensuring sufficient sensitivity for the targeted oxygen concentration resolution.

The results also show that the ultimate limitation of the RDC is not quantization, but

rather stochastic circuit noise. While the PWL calibration effectively compensates deterministic non-linearity in the transfer characteristic, it does not reduce the intrinsic noise of the oscillator and front-end electronics. As a consequence, the practical resolution is determined by the statistical spread of the reconstructed resistance values rather than by the nominal digital step size.

Overall, the proposed RDC provides a favorable trade-off between resolution, conversion speed, and energy efficiency, making it well suited for compact mixed-signal interfaces in photoactivated resistive sensing applications.

5.2. LED Driver Performance

Because the LED driver has already been discussed in detail in Chapter 4, this section summarizes only the final performance results that are most relevant at the system level.

The purpose of the driver is to provide a stable optical excitation current for the external green LED. The simulated results confirm that the driver maintains the output current close to the target value of 10 mA under process, supply, and temperature variations. The main results are summarized in Table 5.2.

Table 5.2: Summary of the LED driver performance

Parameter	Value
Target output current	10 mA
Process-corner range	9.60 – 10.46 mA
Supply-voltage range (1.5–2.0 V)	9.89 – 10.06 mA
Temperature range (30°C–40°C)	9.78 – 10.21 mA
Startup behavior	Stable, no abnormal transient behavior

The process-corner analysis shows the largest spread, with the output current varying from 9.60 mA to 10.46 mA. In contrast, the sensitivity to supply voltage and temperature is much smaller, remaining within approximately $\pm 2\%$ of the nominal target. These results confirm the effectiveness of the constant- g_m reference and the regulated cascode stage in stabilizing the LED current.

From the perspective of the complete sensing system, the achieved current stability is sufficient to ensure a repeatable optical excitation level. This is essential because any substantial fluctuation in the LED intensity would directly translate into uncertainty in the sensor resistance and, consequently, in the reconstructed oxygen concentration.

5.3. System-Level Discussion

The combined results of the RDC and the LED driver confirm the feasibility of the proposed mixed-signal sensor interface for photoactivated oxygen sensing. The RDC provides calibrated high-resolution resistance readout over the full target range, while the LED driver ensures the stable optical activation required by the sensing material.

At the system level, three design trade-offs are particularly evident. First, increasing the number of PWL segments improves linearization accuracy but also increases memory usage and digital complexity. Second, increasing the observation window in the RDC would improve noise averaging and resolution, but at the expense of longer conversion time. Third, the highly digital nature of the architecture improves scalability and compactness, but it shifts the design challenge toward managing oscillator noise and calibration residuals rather than conventional analog accuracy limitations.

Overall, the proposed integrated interface satisfies the system requirements derived from the sensing application and demonstrates a viable solution for compact photoactivated gas-sensing electronics.

6 | Conclusions and Future Developments

6.1. Conclusions

This thesis presented the design and analysis of an integrated mixed-signal interface for a photoactivated oxygen sensing system. The work addressed the complete signal chain, combining optical excitation, resistance readout, and digital processing within a unified architecture.

The proposed resistance-to-digital converter (RDC), based on a Schmitt trigger-driven relaxation oscillator, demonstrated correct operation over a wide resistance range from $750\ \Omega$ to $75\ \text{k}\Omega$. The nominal average resolution, determined by the count-to-resistance mapping of the reciprocal counting process, is approximately $2.6\ \Omega$. However, transient noise simulations at the worst-case operating point show a standard deviation of $\sigma_R = 17.93\ \Omega$, indicating that the effective precision is dominated by circuit noise rather than quantization. Consequently, the practical resolution is approximately $18\ \Omega$ (RMS), which remains comfortably below the design target of $50\ \Omega$ established in Chapter 2.

The results show that the overall performance is primarily limited by stochastic circuit noise rather than quantization. Despite this limitation, the RDC achieves a favorable trade-off between conversion speed, resolution, and energy efficiency, with a conversion time of $185\ \mu\text{s}$ and a Walden FoM of $7.75\ \text{pJ/conversion}$.

In parallel, the designed LED driver provides a stable $10\ \text{mA}$ output current across process, voltage, and temperature variations, ensuring consistent optical excitation of the sensor. The integration of both blocks confirms the feasibility of the proposed mixed-signal sensing interface.

Overall, the developed architecture meets the electrical design targets and provides a compact and efficient solution for photoactivated resistive sensing applications.

6.2. Future Developments

Several directions can be explored to further improve the proposed system.

First, the noise performance of the RDC could be enhanced by increasing the observation window or by optimizing the analog front-end design, particularly the Schmitt trigger and oscillator topology. Reducing noise sources at the circuit level would directly improve the effective resolution.

Second, the digital calibration flow can be further optimized. In particular, the Python-based calibration script could be improved in terms of segmentation strategy and fitting accuracy. Adaptive or non-uniform segmentation methods could reduce the approximation error while maintaining reasonable hardware complexity.

Third, the impact of process, voltage, and temperature (PVT) variations could be addressed more effectively by implementing adaptive or on-chip calibration techniques. This would allow the system to compensate dynamic variations rather than relying only on static calibration.

Finally, the proposed architecture could be extended toward full system integration, including on-chip memory for calibration parameters and enhanced digital control. Such improvements would further increase the robustness and scalability of the solution for real-world sensing applications.

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A | Appendix A

This appendix presents the Python script used to extract the piecewise-linear (PWL) calibration coefficients from the measured count-to-resistance dataset. The script performs segmentation, linear fitting, and conversion of the coefficients into Q16.16 fixed-point format for integration into the digital backend.

A.1. Calibration Script

```
import numpy as np
from pathlib import Path
import matplotlib
matplotlib.use("Agg")
import matplotlib.pyplot as plt

# =====
# USER SETTINGS
# =====
DATA_FILE = Path("count_vs_resistance_data.txt")

K = 24                # Number of segments
Q = 16                # Q16.16 format
SCALE = 1 << Q

OUT_PREFIX = "pwl_uniform"

# =====
# Load data (count, resistance)
# =====
data = np.loadtxt(DATA_FILE)
C = data[:,0]
R = data[:,1]
```

```

# Sort data
idx = np.argsort(C)
C = C[idx]
R = R[idx]

Cmin, Cmax = C[0], C[-1]

# =====
# Interpolation reference
# =====
def R_interp(Cin):
    Cin = np.clip(Cin, Cmin, Cmax)
    return np.interp(Cin, C, R)

# =====
# Uniform PWL model
# =====
edges = np.linspace(Cmin, Cmax, K + 1)
m = np.zeros(K)
b = np.zeros(K)

Re = R_interp(edges)
for k in range(K):
    c0, c1 = edges[k], edges[k + 1]
    r0, r1 = Re[k], Re[k + 1]
    m[k] = (r1 - r0) / (c1 - c0)
    b[k] = r0 - m[k] * c0

# =====
# Error evaluation
# =====
def pwl_eval(Cin):
    Cin = np.clip(Cin, edges[0], edges[-1] - 1e-12)
    k = np.searchsorted(edges, Cin, side="right") - 1
    k = np.clip(k, 0, K - 1)
    return m[k] * Cin + b[k]

Rhat = pwl_eval(C)
err = R - Rhat

```

```

rmse = np.sqrt(np.mean(err ** 2))
maxae = np.max(np.abs(err))

print(f"RMSE = {rmse:.6f} ohm")
print(f"MaxAE = {maxae:.6f} ohm")

# =====
# Convert to Q16.16 FIXED-POINT
# =====
edges_q16 = np.round(edges * SCALE).astype(np.int64)
m_q16      = np.round(m      * SCALE).astype(np.int64)
b_q16      = np.round(b      * SCALE).astype(np.int64)

np.savetxt(f"{OUT_PREFIX}_edges_q16.txt", edges_q16, fmt="%d")
np.savetxt(f"{OUT_PREFIX}_m_q16.txt",      m_q16, fmt="%d")
np.savetxt(f"{OUT_PREFIX}_b_q16.txt",      b_q16, fmt="%d")

# =====
# Plot error vs resistance
# =====
order = np.argsort(R)
R_sorted = R[order]
err_sorted = err[order]

plt.plot(R_sorted, err_sorted)
plt.xlabel("Resistance (Ohm)")
plt.ylabel("Error (Ohm)")
plt.grid(True)
plt.savefig(f"{OUT_PREFIX}_error_plot.png")

```

A.2. Notes

The script performs the following operations:

- Loads the measured count-to-resistance dataset.
- Computes a uniform segmentation of the input range.
- Performs piecewise-linear fitting for each segment.

- Evaluates the approximation error (RMSE and maximum error).
- Converts the coefficients into Q16.16 format for hardware implementation.

The generated lookup tables are used by the digital PWL engine described in Chapter 3 for real-time resistance reconstruction.

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List of Symbols

Symbol	Description	Unit
R	Sensor resistance	Ω
R_x	Input/sensor resistance	Ω
$R_{\min}$	Minimum measurable resistance	Ω
$R_{\max}$	Maximum measurable resistance	Ω
R_{LSB}	Resolution (quantization step)	Ω
σ_R	Standard deviation of resistance (noise)	Ω
C	Timing capacitor	F
T	Oscillation period	s
t_{conv}	Conversion time	s
V_{TH}	Upper switching threshold voltage	V
V_{TL}	Lower switching threshold voltage	V
V_{DD}	Supply voltage	V
I_{LED}	LED driving current	A
I_{ref}	Reference current	A
Count	Digital count value from RDC	–
N_{edges}	Number of oscillator edges	–
m_i	Slope of PWL segment i	Ω/count
b_i	Intercept of PWL segment i	Ω
SNR	Signal-to-noise ratio	dB
ENOB	Effective number of bits	bits
FoM_W	Walden figure of merit	pJ/conversion
FoM_S	Schreier figure of merit	dB

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