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Predictive diagnostic of IGBT Power Converters on photovoltaic plants

TESI DI LAUREA MAGISTRALE IN
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Abstract

As the use of renewable energy plants has become increasingly prevalent, the Insulated-Gate Bipolar Transistor (IGBT) has emerged as a critical component in Power Electronics Converter Systems (PECS). In order to ensure reliable and efficient operation of these systems, it is important to accurately predict the lifetime of IGBTs. This master thesis provides an overview and critical analysis of various lifetime modelling studies for IGBTs, which can be found in the literature.

The aim of this thesis is to provide a comprehensive understanding of the available modelling approaches, including physics-based, data-driven, and hybrid models, and to compare their strengths and weaknesses. The literature review examines the various factors that affect the lifetime of IGBTs, including operating conditions, thermal cycling, and device design. It also discusses the limitations of existing models and potential areas for future research. This thesis provides valuable insights for researchers, engineers, and manufacturers who are involved in the design, operation, and maintenance of power electronics systems in renewable energy applications. By summarizing and analysing the state-of-the-art in lifetime modelling for IGBTs, this thesis contributes to the ongoing effort to improve the reliability and sustainability of renewable energy systems.

Key-words: Reliability, IGBT, Power Electronics Converters, lifetime model.

Abstract in italiano

Con la crescente diffusione degli impianti a energia rinnovabile, il transistor bipolare a porta isolata (IGBT) è diventato un componente fondamentale dei sistemi elettronici di potenza. Per garantire un funzionamento affidabile ed efficiente di questi sistemi, è importante prevedere con precisione la durata di vita degli IGBT. Questa tesi di laurea magistrale fornisce una panoramica e un'analisi critica dei vari studi di modellazione della durata di vita degli IGBT presenti in letteratura.

L'obiettivo di questa tesi è quello di fornire una comprensione completa degli approcci di modellazione disponibili, compresi i modelli basati sulla fisica, quelli guidati dai dati e quelli ibridi, e di confrontare i loro punti di forza e di debolezza. La revisione della letteratura esamina i vari fattori che influenzano la durata di vita degli IGBT, tra cui le condizioni operative, i cicli termici e la progettazione del dispositivo. Vengono inoltre discussi i limiti dei modelli esistenti e le potenziali aree di ricerca future. Questa tesi offre spunti preziosi a ricercatori, ingegneri e produttori che si occupano di progettazione, funzionamento e manutenzione di sistemi elettronici di potenza in applicazioni di energia rinnovabile. Riassumendo e analizzando lo stato dell'arte della modellazione della durata di vita degli IGBT, questa tesi contribuisce allo sforzo in corso per migliorare l'affidabilità e la sostenibilità dei sistemi di energia rinnovabile.

Parole chiave: Affidabilità, IGBT, convertitori elettronici di potenza, modello di vita.

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Introduction

The increasing use of renewable energy has led to a growing demand for reliable and efficient power electronics systems. Insulated-Gate Bipolar Transistors (IGBTs) have become a critical component in these systems due to their ability to handle high voltages and currents while maintaining high switching frequencies. However, IGBTs are subject to various forms of degradation and failure over time, which can lead to reduced system efficiency and reliability. Therefore, it is important to accurately predict the lifetime of IGBTs in order to ensure optimal system performance and minimize maintenance costs.

There are several factors that affect the lifetime of IGBTs, including operating conditions, thermal cycling, and device design. In order to accurately predict the lifetime of IGBTs, various modelling approaches have been proposed in the literature. These models can be classified into three main categories: physics-based models, data-driven models, and hybrid models. Each of these approaches has its own strengths and weaknesses, and the choice of model depends on the specific application and available data.

The aim of this master thesis is to provide an overview and critical analysis of the available lifetime modelling approaches for IGBTs, with a focus on their application in renewable energy systems. This will include a review of the relevant literature and a comparison of the different modelling approaches. The thesis will also examine the limitations of existing models and potential areas for future research.

Overall, this thesis will contribute to the ongoing effort to improve the reliability and sustainability of power electronics systems in renewable energy applications. By providing a comprehensive understanding of the available lifetime modelling approaches for IGBTs, this thesis will enable researchers, engineers, and manufacturers to make more informed decisions about the design, operation, and maintenance of these systems.

Reliability is of paramount importance in power electronics due to several reasons.

Firstly, power electronic systems are often used in critical applications such as medical equipment, transportation systems, and power grids. Any failure in these systems can lead to catastrophic consequences, such as loss of life, property damage, and economic

loss. Therefore, ensuring the reliability of power electronic systems is crucial to maintain the safety and stability of these critical applications.

Secondly, power electronic systems often operate under harsh conditions, such as high temperatures, high voltages, and high currents. These conditions can cause component degradation and failure over time, leading to system malfunction and downtime. Therefore, designing and testing power electronic systems for reliability is essential to ensure they can withstand these harsh operating conditions.

Thirdly, power electronic systems often contain complex control and protection circuits that require precise operation. Any component failure or malfunction can lead to incorrect system operation, which can cause damage to the system or its surroundings. Therefore, ensuring the reliability of power electronic systems is crucial to maintain the accuracy and precision of these control and protection circuits.

In conclusion, reliability is of utmost importance in power electronics to ensure the safety, stability, and accurate operation of critical applications. Designing and testing power electronic systems for reliability is essential to ensure they can withstand harsh operating conditions and maintain precise operation over time.

1 Reliability Engineering on Power Electronics

1.1. Reliability engineering

The Reliability is defined as the ability of an item to perform the required function under stated conditions for a certain amount of time [1]which is often measure by probability of survival and failure rate.

It is relevant to the durability (i.e., lifetime) and a availability of the item. The essence of reliability engineering is to prevent the creation of failures.

The deficiencies in the design phase have effect on all produced items and the cost to correct them is progressively increased as the development proceeds.

In the subsequent chapters, there will be a focused discussion on the failure mechanisms, test methods, and studies for lifetime models of power semiconductor modules. These discussions will provide deeper insights into the physical mechanisms and behaviours of the modules, leading to the development of the lifetime models of a power module.

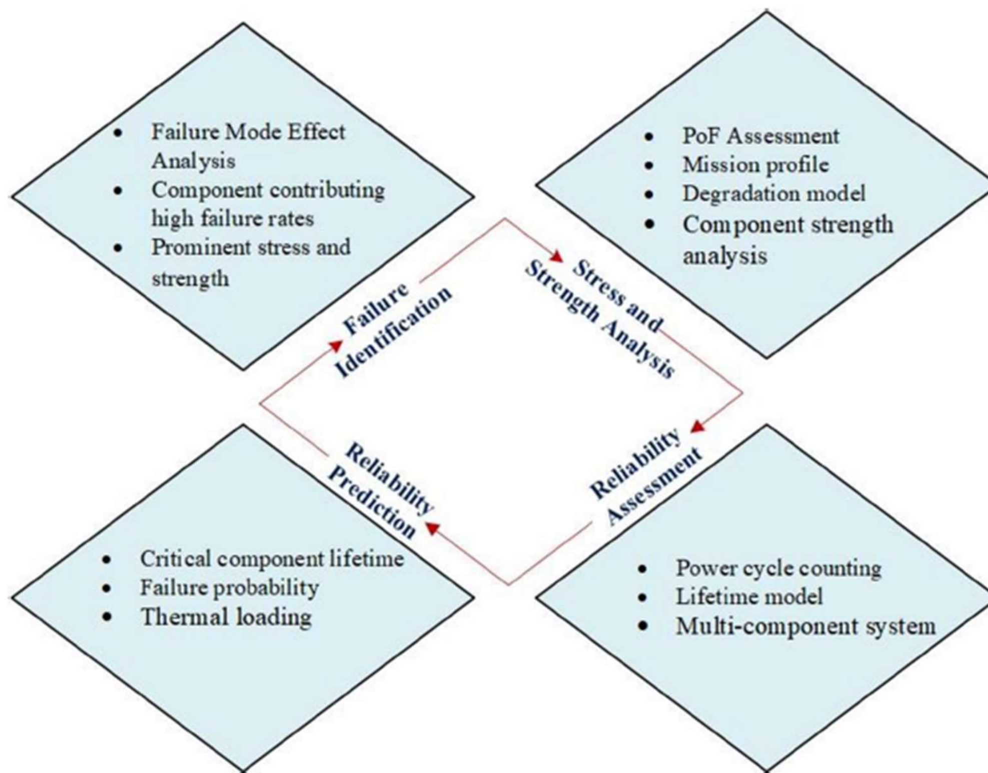


Figure 1 Scheme of design for reliability (DfR)

1.2. Reliability in Power Electronics

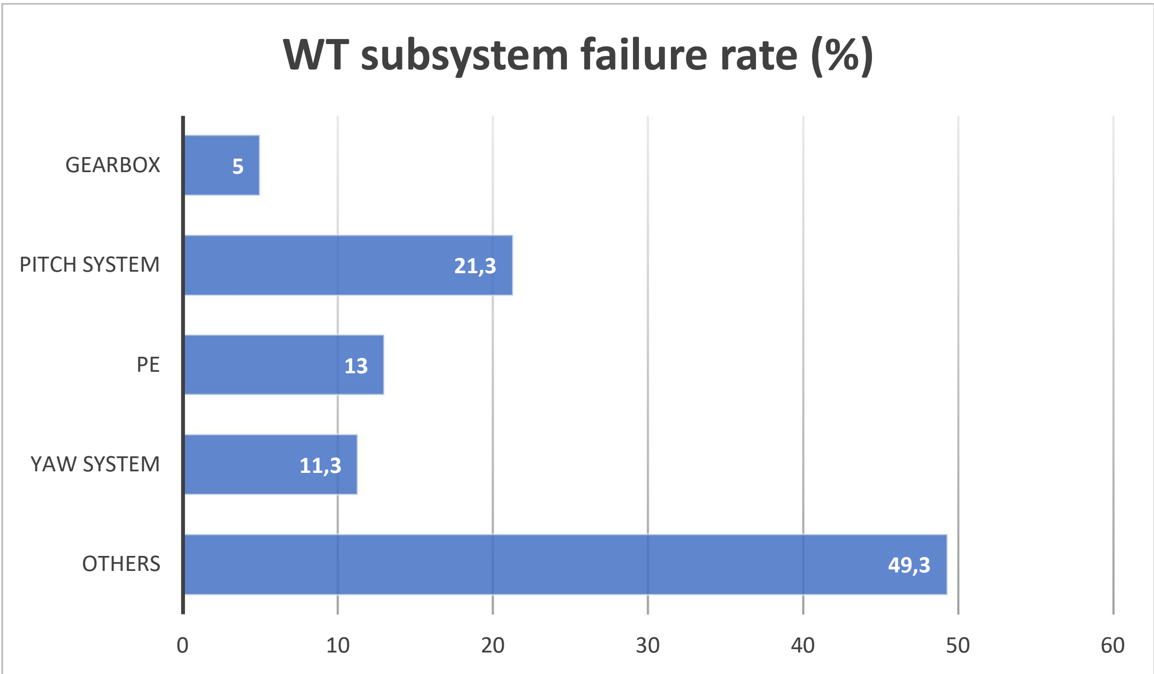
The performance requirements of power electronics products are increasingly demanding in terms of cost, efficiency, reliability, environmental sustainable materials, size, and power density. Of which, the reliability performance has influences on the safety, service quality, lifetime, availability, and life cycle cost of the specific applications.

In Table 1 [2] the typical design target of lifetime different applications is listed

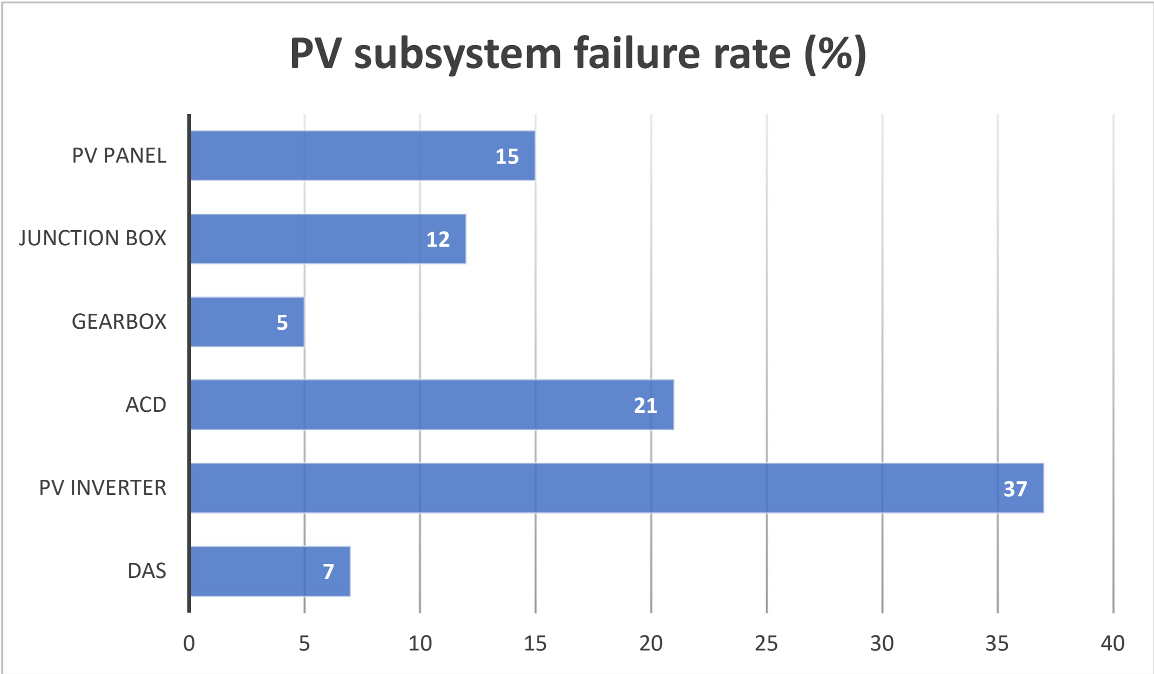
This field emerged as a relatively new branch of Power Electronic (PE) supporting the fast progress towards advanced Power Electronics Converter Systems (PECS), with significantly improved reliability ratings.

With the increasing penetration of renewable energy sources and the increasing adoption of more efficient variable-speed motor drives, the failure of PECS in Wind Turbine (WT), Photovoltaic (PV) Systems, and motor drives are becoming an issue.

Field experience in renewable reveal that PECS are usually one of the most critical assemblies in terms of failure level, lifetime, and maintenance cost, Figure 1 [3]. [4]



(a)



(b)

Figure 2 Failure rate of subsystems on WT (a) and PV system(b).

Usually, PECS operates under increasingly severe temperature profiles, fast Temperatures Cycling (TC) between extreme temperature levels.

Accordingly, the reliability requirements for power semiconductor modules as fundamental components of PECS are significantly increased. Power modules manufacturers have been working on new power modules design and packaging technologies in order to increase endurance and prolong the lifetime of power modules in the futures, and subsequently enable high performance of the PECS, also concerning reliability.

In future the inclusion of reliability aspects will further improve the design of PECS, therefore the integration of lifetime models of the system components into the design process is the next step.

Applications	Typical design target of Lifetime
Aircraft	*24 years (100,000 hours flight operation)*
Automotive	*15 years (10,000 operating hours, 300,000 km)*
Industry motor drives	*5-20years (60,000 hours in at full load)*
Railway	*20-30 years (10 hours operation per day)*
Wind Turbines	*20 years (24 hours operation per day)*
Photovoltaic plants	*5-30 years (12 hours per day)*

Table 1 Typical lifetime target in different PE applications.

In recent times, there has been an increasing diffusion of renewable energy plants, such as Photovoltaic Systems (PV) and Wind Turbine (WT) systems, which has led to an increased role of inverters.

The primary role of inverters in such plants is to convert the DC power produced by photovoltaic modules into AC power, which can then be transported through the grid or used on-site.

A basic PV inverter comprises of a DC/DC converter stage in series with a DC/AC inverter stage, Figure 2 [5] . Inverters can be classified in various ways based on their purpose, topology (single or multi-stage, isolated or non-isolated, single-phase or three-phase), and power handling capabilities.

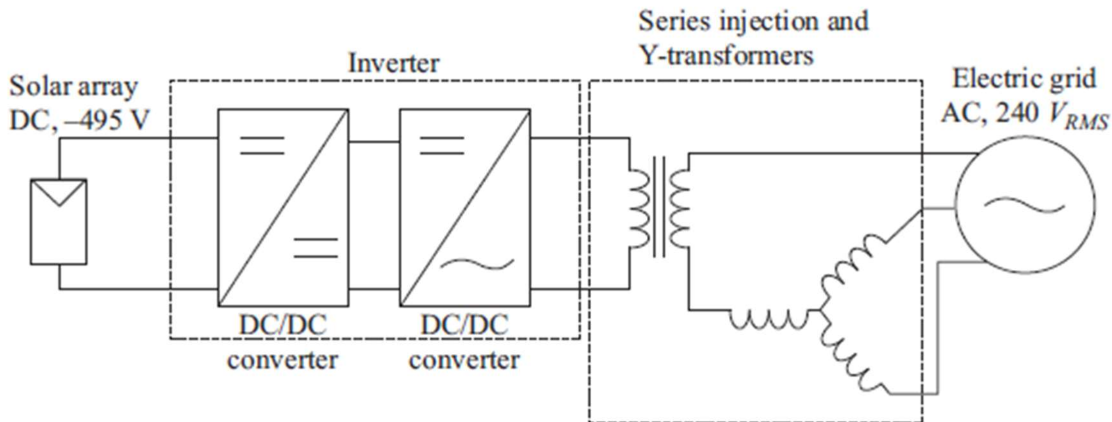


Figure 3 Power flow through a PV system.

The reliability of the power device require a deeper and vast knowledge of different topics:

- Mechanical design and thermal capabilities of power modules
- Physics of failures (PoF) and the material science
- PE and its application field

Most of the models and carried out by the power modules manufacturers are empirical lifetime models (based on experience and statistical analysis of data gained in running accelerated cycling tests.) they are used for the characterization of Power Cycling (PC), capabilities of power modules. In the sense of the empirical lifetime modelling approach, this requires developing a specific model for each failure mode.

The models that will be presented are used by engineers as the only means for an end-of-life (EOL) estimation of power modules and, further then for the prediction of PECS reliability under specifies mission profiles.

The models are obtained with the conduction of accelerated test to filed conditions. Normally the test are PC and TC, the goal of the tests is to collect relevant data for building the lifetime model.

With new concepts of power modules packages, and ever-increasing lifetime expectations for power semiconductor devices operating under very challenging environmental conditions, the researchers started investigations that consider physics-based lifetime models.

The physical modelling of failure includes the analysis and modelling of actual failure mechanisms as, the stress and strain development under thermal loading. For this PC tests are required. They contribute to the validation of the extrapolation of existing empirical models.

Therefore, PoF can improve the lifetime estimation and enable the reliability engineering to be integrated into the development and research cycles of the overall design process of PECS.

The model can be defined as a tool for the EOL estimation of a power modules exposed to cyclic thermal loading.

Controlling the test conditions can be assumed that failures are only due to wear-out effects, for example, interconnection failures are reported as the most common causes of failure of power modules operated in the cycling test.

The critical parts of the power modules in PC or TC experiments are the three interconnections:

- Wire bonds
- The chip solder joint
- Substate-baseplate solder layer

1.3. Introduction to the power module

The power module on a power converter is an electronic component that integrates one or more power semiconductor devices (such as MOSFETs, IGBTs, or thyristors) with other necessary components (such as diodes, capacitors, and resistors) in a single package. The module is designed to handle high power and high voltage levels in various applications such as motor drives, renewable energy systems, and industrial automation.

The power module typically consists of the following main components:

- Power semiconductor device: these are the devices that switch the current on and off in the circuit. The most common power semiconductor devices used in power modules are insulated gate bipolar transistors (IGBT), metal-oxide-semiconductor field-effect transistors (MOSFETs), and thyristors.

  The power semiconductor devices are attached to the baseplate through a process called soldering or wire bonding.

- Diode: these are used to control the flow of current in the circuit. they allow current to flow in only one direction and prevent reverse current from flowing. Diodes are typically used in conjunction with IGBT in power modules to provide a freewheeling path for the current when the IGBT is turned off.
- Capacitors: these are used to store energy in the circuit and help to smooth out any fluctuation in the voltage.

- Resistors: these are used to limit the flow of current in the circuit and to provide a means of voltage division.
- Baseplate: this the metal plate that forms the base of the power module. It acts as a heat sink to dissipate the heat generated by the power semiconductor devices.

The module is then encapsulated in a protective housing, which helps to prevent electrical shorts and provides mechanical protection.

Power modules offer several advantages over discrete power components, including smaller size, reduced power losses, improved reliability, and simplified circuit design. They are widely used in high-power and high-reliability applications, where compactness and efficiency are critical.

The IGBT and diode components are essential parts of the power module, as they are used for switching high power loads and controlling the flow of current and voltage in the circuit.

1.4. Overview on power diodes

The diodes that are considered are for hight power applications. They differ from the low-voltage diode in dimension and current capability.

In this case the layers of doped materials are arranged in a more complex manner. The thickness and the width of the layers in the diode vary depending on how much current it will have to carry. The cross-sectional area of high-power diode can go from the order of square micrometres to even square centimetres when the current flow reaches several thousand amperes.

The basic cross-section of a power diode is made of three layers, characterized by different doping indexes, indicates as N_d which quantifies the number of doped atoms per cm^3:

- n^+ layer: highly phosphorous doped
- n^- layer: low phosphorous doped
- p^+ layer: highly boron doped

The drift region, usually called n^- layer is typically not found in low-power diodes. Is the layer responsible for absorbing the depletion layer of the reverse-biased $p^+ n^-$ junction. This region is the primary structural feature of high-power diodes and determines the breakdown voltage based on its thickness and structure. A thicker drift region can hold a higher breakdown voltage.

The I-V characteristics of high-power diodes exhibit the same behaviour as low-power diodes. The diode is switched on only after reaching a threshold voltage and enters an ohmic region where the voltage grows linearly depending on the current. This ohmic behaviour is mainly determined by the drift region, which provides an equivalent internal resistance when the diode is switched on.

1.4.1. Power losses

Power diodes experience two types of losses: conduction losses when the diode is on and reverse recovery losses when it turns off, Figure 3 [6].

Conduction losses ($P_{loss\ cond_D}$)can be calculated simply by multiplying the current passing(I_d), through the diode by the voltage difference across its poles (V_d), which can be easily calculated using Ohm's law. The resulting voltage is then multiplied by the current to obtain the power losses by conduction.

$$V_d = V_{f0} + I_d R_{on} \quad (1.a)$$

$$P_{loss\ cond_D} = V_D I_D = V_{F_0} I_D + I_D^2 R_{on} \quad (1.b)$$

In contrast, reverse recovery losses are more difficult to compute theoretically due to their nonlinear behavior.

During the switching-off phase, the current and voltage in the diode do not drop immediately to zero; they become negative for a very short interval of time. It is easier to measure the energy lost during reverse recovery experimentally, for example, through oscilloscope measurements of current and voltage, and then tabulate the results with their dependence on the current during the on state and the supply's voltage.

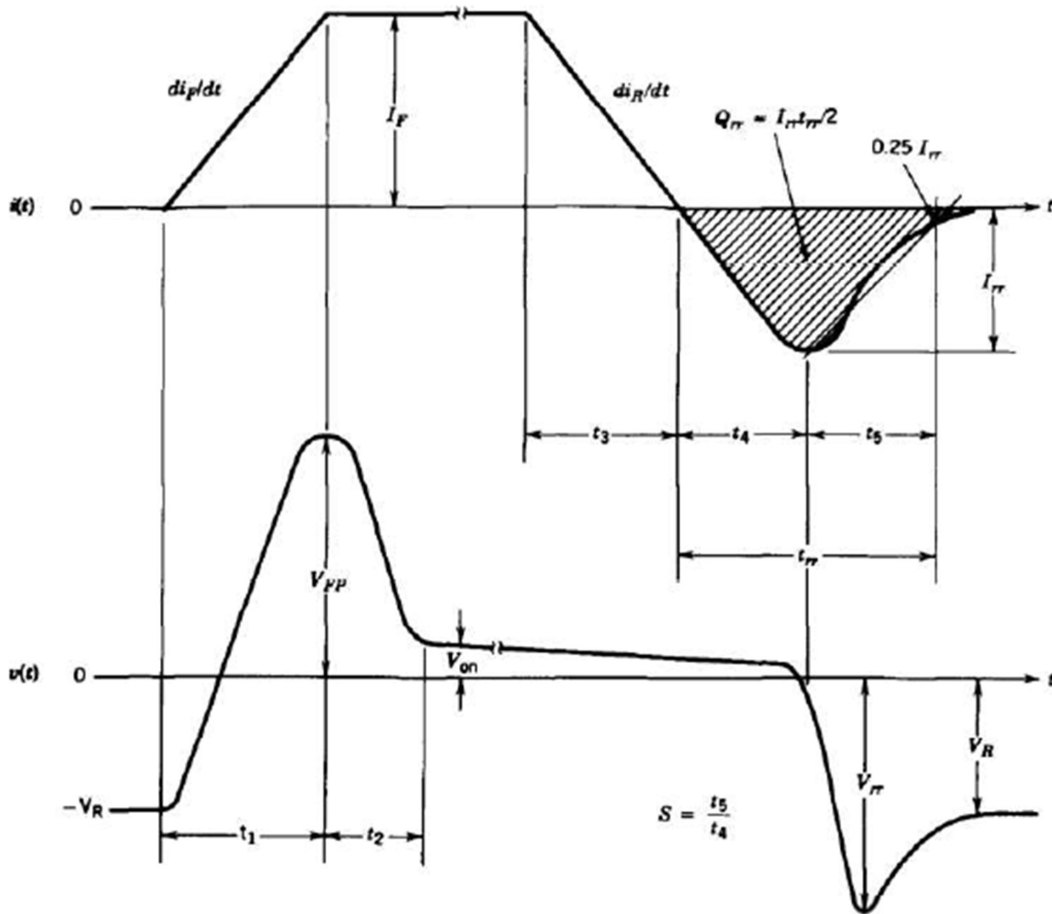


Figure 4 Voltage and current waveform of a power diode.

1.5. Overview in Insulated Gate Bipolar Transistor (IGBT)

The IGBT is the combination of Metal Oxide Semiconductor Field Effect Transistor) (MOSFET) and Bipolar Junction Transistor (BJT) on the same silicon wafer to achieve a circuit a new device that combines the best qualities of both types of devices.

This is the device of choice in most new applications, other names for this device include GEMFET, COMFET, and bipolar-model MOSFET or bipolar-MOS transistor.

A standard n-channel IGBT has a vertical cross section similar to that of a MOSFET but differs in having an additional p^+ layer on the drain.

The doping levels N_d are similar, except for the higher doping coefficient in the p^+ drain region.

One drawback of the IGBT is the presence of a parasitic thyristor between the drain and source, which can cause unwanted turn on. This can be minimized with changes to the p layer in the body region.

Punch-through IGBTs have a buffer layer that significantly improves operation, while non-punch through IGBTs lack this layer.

In the forward direction, I-V characteristics are similar to a BJT, but the controlling parameter is gate-source voltage (like a MOSFET), rather than input current (as in a BJT).

1.5.1. Power Losses

The power losses of an IGBT can be categorized into conduction losses and switching losses, which exhibit complementary characteristics.

In the linear region of the IGBT, the drain current i_d and the voltage v_{DS} (1.c) are linearly related through the internal resistance of the IGBT ($R_{on(IGBT)}$).

$$v_{DS} = V_{DS_{th}} + R_{on(IGBT)} * i_D \quad (1.c)$$

Due to the low voltage v_{ds} that is typical of an IGBT, conduction losses (1.d) are not very significant, but they occur over a much longer duration than switching losses. At slow switching frequencies (less than 100 Hz), region of the IGBT, a slight increase in the drain current can result in a dramatic increase in the voltage, v_{DS}, causing the power loss to be very high.

$$P_{loss_{cond_{IGBT}}} = v_{DS} * i_D \quad (1.d)$$

On the contrary, conduction losses typically outweigh switching losses in magnitude, but switching losses occur over a brief duration, usually a few microseconds or hundreds of nanoseconds. Neglecting switching losses is feasible at slow switching frequencies, but at very high frequencies, the average value of switching losses may exceed that of conduction losses.

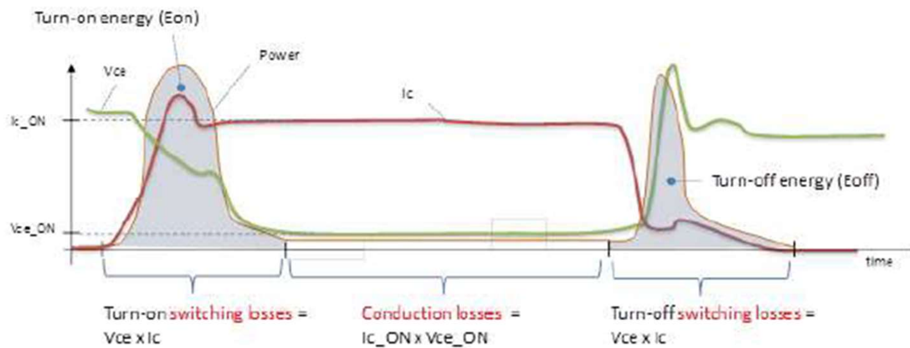


Figure 5 IGBT Power Losses

Similar to power diodes, the switching losses of an IGBT are challenging to calculate theoretically. Typically, suppliers include these losses in a datasheet, along with their dependence on the DC-link voltage and drain current.

1.6. Thermal stress and its effects on IGBTs

Power semiconductor packages or modules face significant reliability challenge due to the high-current operating conditions and multiples interfaces between materials with different coefficient of thermal expansion (CTEs).

The power semiconductor devices are typically attached to a power substrate, which is then connected to a base plate made of copper.

Electrical interconnections are established using wire bonds, which connect the power semiconductor devices to the power substrate and the output connector, Figure 5 [5].

The module is subsequently encapsulated for mechanical and environmental protection. However, these multiple interfaces can create significant thermos-electrical stresses that can lead to potential reliability problems. In particular, thermos-electrical fatigue induced failure due to CTE mismatches and temperature excursions during operation are major failure mechanisms, often resulting in bond wire fatigue and solder fatigue.

The studies and methods presented in the next chapters are specifically focused on the bond wire fatigue.

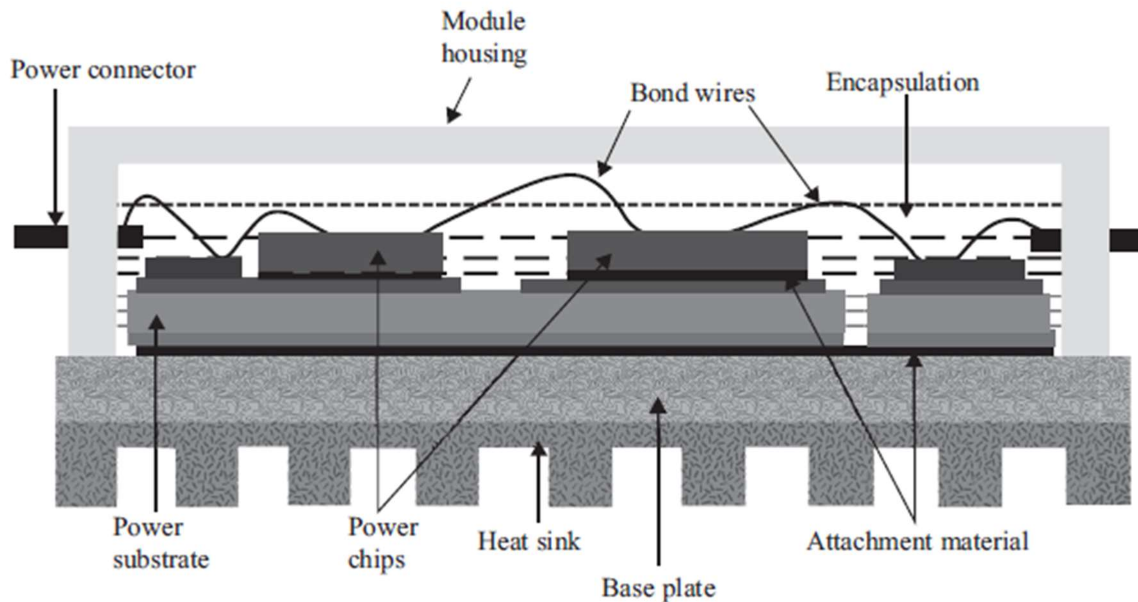


Figure 6 Structural details of an IGBT module.

1.6.1.1. Bond wire fatigue

Mechanical issues related to bond wire fatigue encompass bond wire lift-off and bond wire heel cracking.

Bond wire fatigue is caused by the repeated flexure of the bond wire and the shear stresses that arise between the bond pad and bond wire. In a standard power electronics module, there may be numerous bond wires that provide electrical interconnection from power devices to the power substrate, from the power substrate to external connectors, and between power devices, amounting to hundreds of bond wire in total, Figure 6. [7]

A considerable number of these bond wires are affixed onto the active regions of the power semiconductors devices. Consequently, these are subjected to thermal fluctuations caused by the power dissipation in the power devices as well as the self-heating of the wire due to ohmic heating.

While aluminium bond wires are commonly used, copper bond wires are becoming increasingly prevalent in certain applications.

Typically, aluminium bond wires are hardened by alloying with a few thousand parts per million of magnesium or silicon to impede the corrosion mechanism in pure aluminium bond wire.

Wire bond failure typically arise from the repeated flexing of the bond wire, or the shear stresses generated between the bond wire and its termination. Copper bond wire

offer a cost-effective alternative to their aluminium counterparts, and their slower intermetallic growth in copper bond terminations confers enhanced reliability for high-power packages and modules.

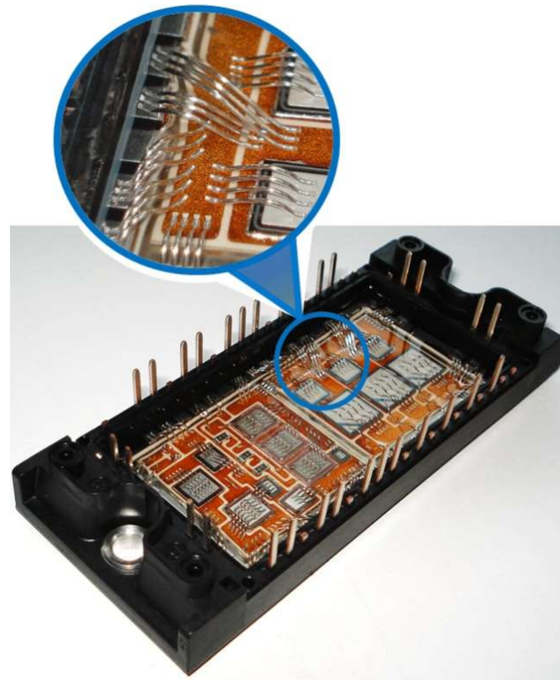


Figure 7 Bond wire connections on a power module

1.6.1.2. Bond wire lift-off

Bond wire detachment typically happens at the connection points between aluminium bond wires and silicon power devices as a result of significant temperature variations. Nevertheless, the detachment of bond wires rarely happens at the points where bond wires are connected to copper traces or pads. This is due to the fact that there are fewer temperature changes between the bond wires and the copper pads on the power substrate compared to those at the bond wire connections on the power semiconductor dies.

The fractures that result in bond wire detachment are typically initiated at the end of the bond wire and gradually extend until the bond wire detaches completely.

The number of thermal cycles to failure (N_f), can be modelled using the Manson-Coffin relation.

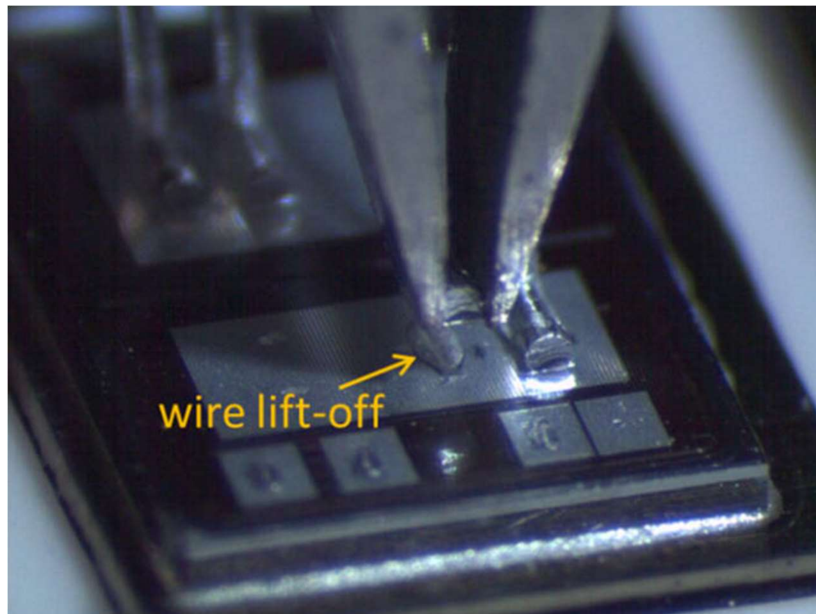


Figure 8 Bond wire lift off on power module.

1.6.1.3. Bond wire heel cracking

During extended endurance tests, it's common to observe the cracking of bond wire heels caused by thermo-mechanical effects. The bond wires experience flexure fatigue due to the expansion and contraction that occurs during temperature cycling, Figure 8. The height of the wire bond loop is a crucial factor, as it determines the angle at which the heel of the bond wire is positioned. Additionally, the encapsulation of the package or module can contribute to this type of failure. It's worth noting that heel cracking tends to occur at a slower rate than the lift-off failure mechanism.

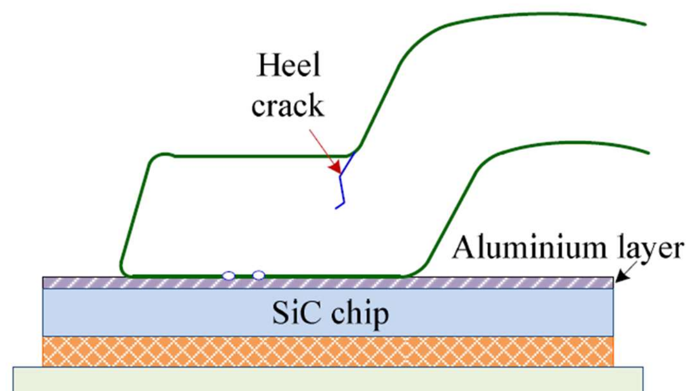


Figure 9 Bond wire heel cracking

1.6.2. High temperature power electronics converters

Power electronics converters have found their way into many applications, e.g., switched-mode power supplies in adapters and chargers, motor drives, and solid-state transformers to interconnect electric grids. Some applications have been calling for power electronics converters that can operate at high temperature environment.

PEC's operating at elevated temperature usually have degraded performance, such as reduced efficiency, lower noise immunity, and decreased system reliability, compared to those operating at room temperature. Nevertheless, harsh-environment applications, such as deep earth drilling, automotive, avionics, and space exploration, have been utilizing converters in high-temperature environments and are continuously pushing the temperature limits higher and higher with the advances in device technologies and converter design methodologies. [8]

For example, on oil and gas application, the downhole electronics usually operate at 150-170°C ambient temperature. Due to the declining reserve of easily accessible natural resources, the industry tends to drill deeper, and the temperatures may exceed 200°C.

In automatic and avionics applications, in order to reduce the cost, weight and volume of wiring sensors and electrics circuits are being moves close and closer to engines, brakes, etc. where temperature exceeds 125°C. the trend to replace purely mechanical and hydraulic system in vehicles and aircraft with electromechanical or mechatronic systems demands high-temperature power electronics as well, because these power electronics converters need to be close to the actuators.

Usually to keep converters cool, there are two ways:

- Cooling
- Protective enclosure to prevent the environment from heating up converters.

The main drawback of these two solutions is that the installation of cooling or enclosure system increases the cost, volume, and weight of the converters.

Therefore, ideally, would prefer reliable power electronics that can withstand high temperature by itself.

The uncertainty of the performance and the lifetime of individual components at high temperature make it challenging to design and operate converters properly. In particular, in a wide temperature range.

1.6.2.1. High temperature power electronics modules

Conventional power packaging technologies have many concerns with operating at high temperature, including electrical parasitic contributions, intermetallic formations, and long-term reliability depending on bonding surface [9].

At high temperature above the traditional operating temperatures, and above the traditional operating temperatures of semiconductor electronics (i.e above 120°-150°), some failure modes manifest themselves more readily. For example, polymeric materials utilized for voltage isolation and encapsulation degrade more readily at high temperatures, presenting a major reliability problem for power semiconductor modules.

The need for high power converter density, high operating voltage, and high temperature for power semiconductor devices in the power electronics industry presents additional reliability challenges for power semiconductor devices and packaging technologies.

Material properties are of great importance in high-temperature power electronics modules. Trade-offs between materials properties, such as thermal, electrical, and mechanical properties, and the reliability, modules size, and the total cost must be carefully made when designing high-temperature power electronics modules.

1.6.2.2. Power Semiconductor Devices-Packaging

Packaging is the major limiting factor. A packaged power semiconductor device consists of power semiconductor due bonding material for die and substrate attach, sub-strate, base plate, bond wires, encapsulant, and case.

Semiconductor technologies rapidly advance forward and have promising properties at high temperature. for example, SiC and GaN at 200°C still outperform Si at 25°C.

The discussion about temperature limits of different parts of a power semiconductor package is summarized in the Figure 9 below.

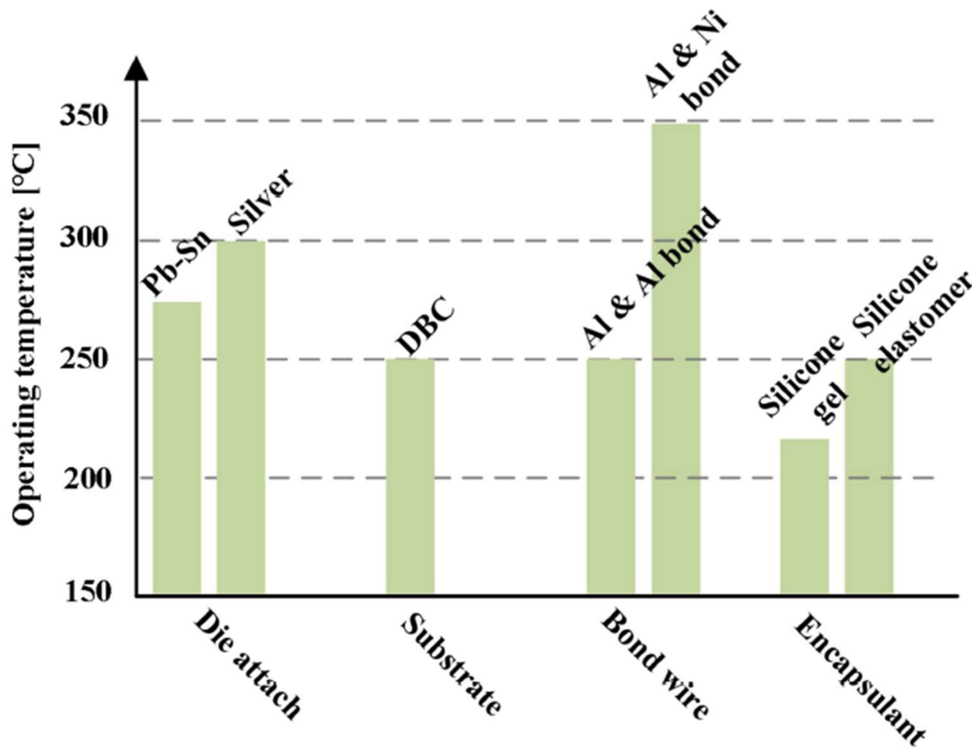


Figure 10 Different power semiconductor package temperature limits

Apart from packaging material, packaging scheme is also a prominent factor that affects a power semiconductor package's electrical and thermal performance at high temperature.

1.6.2.3. Die top surface electrical interconnection.

To have reliable wire bonding at high temperature or over a wide temperature range, the material of bond wire and the metallization of bonding pad need to be carefully selected.

Preferable the same material should be used for bond wire and metallization of bonding pad, since interdiffusion and interface corrosion occur between dissimilar metals at high temperatures, which degrade bond strength.

Aluminium bond wire is the most widely used top-side electrical interconnections for the power semiconductor devices in power electronics modules.

New electrical interconnection solutions are required for high-temperature power electronics modules to improve both enhanced thermal management and reduced parasitic inductance for the power electronic modules.

- Aluminium ribbon bonding, as a replacement of many paralleled bond wires, offers a higher current capability, a lower parasitic inductance at higher frequencies, as well as lower and more consistent bond loop heights the conventional bond wires.
- Copper wire bonding is another potential top-side electrical interconnection for high-temperature power electronics modules. In addition to their higher current-carrying capability over the conventional aluminium bond wire, copper wires offer a high pull strength and a high foot shear strength with improved reliability.
- Gold, this is extremely reliable, however the high cost of gold makes it not favourable in large high-power die packaging, which require more raw material than small low-power dies.

1.6.3. Aging of semiconductors in an IGBT module

Thermal stresses have a significant impact on the aging of semiconductors in an IGBT module. High temperatures, as discussed can damage the semiconductor connections in the module, rendering it unable to deliver electrical power as expected, even if the semiconductors are in good condition [8]. However, these are only some of the ways that a module can exhibit aging characteristics.

An IGBT module can fail due to several other phenomena, including encapsulation failure, die-attach failure, bond wire failure, silicon bulk defects, oxide layer faults, and aluminium metal faults. Of these effects, bond wire failure and die-attach failure are more significantly impacted by thermal behaviour.

2 Models for lifetime estimation of Power Modules

This chapter will introduce and explain what are the tests that are carried out to determine the reliability of the power module, a critical component for the proper operation of inverters.

The tests considered here are those that consider power and temperature cycles and also how these are modified to consider accelerated tests.

After that, methods will be introduced to determine the junction temperature of the IGBT, a key variable in various component life models.

The first method talks about the Monitoring Measurement Unit and online monitoring of Temperature sensitive electrical parameters, parameters of the IGBT that vary over time and can be considered to monitor the degradation of the component, also is presented what are the main variables in literature. The second method is the more traditional one, which is the use of an electro-thermal model, i.e., the Foster or Cauer model, to find the temperature at the junction.

2.1. Reliability cycling tests.

PC and TC test are performed and well established among the manufacturers of power modules as the means for a lifetime estimation of products.

In the following, some international standard test can be found:

- Joint Electro Device Engineering Council (JEDEC)
- Military Standard for microcircuits (MIL-STD-883)
- International Electrotechnical Commission

Environmental testing for thermal shock:

- MILT-STD-883 Methods 1011.0
- IEC68-2-14

Temperature Cycling:

- JEDS22-A-104D
- MIL-STD-883 Method 1010 Condition C

- IEC68-2-14
- JEDS22-A-104D

High and Low temperature storage:

- IEC68-2-2
- IEC68-2-1

Endurance testing includes power cycling:

- JEDS22-A-122

Vibration:

- IEC68-2-6

Lead Integrity:

- IEC-2-21

Solder Ability:

- IEC-2-20

Autoclave and mounting torque:

- JESD22-A110AAB

The exact procedures are mostly product-oriented, and hence defined independently by manufacturers.

In this paper, the focus is on the TC and PC test, that are the test mainly used for lifetime model analysis, they are empirical of physics-based models.

2.1.1. Temperature cycling test – TC

The test is conducted to examine the change in electrical characteristics and physical structure of the power packages or modules to alternate exposures at extremes of high and low temperatures.

The differences in the coefficients of thermal expansion (CTEs), of the different layers, in the power packages or modules, can create cracking and delamination of packages in internal structures and changes in electrical characteristics resulting from thermos-mechanical damage.

The power packages or modules must be placed in a temperature cycling test chamber so that there is no substantial obstruction to the flow of circulating air across each device under test.

The range of temperature of the cycle is usually from -40°C to +125°C for the required number of cycles. The dwell time at each extreme temperature is greater than 10 minutes and the temperature of the device must be reach in less than 15 minutes [10].

The package or module lifetime in years is then given by:

$$(N\ x\ \alpha_T)/365 \tag{2.a}$$

Where N is the number of days to failure and α_T, is the acceleration.

The lifetime model here considered was the Manson-Coffin, the acceleration coefficient is found thanks to the relation between the filed cycle counts N_1 and N_2, Δ_1 and Δ_2 are the temperature range, K is and experimental facto.

$$\alpha_T = \frac{N_1}{N_2} = \left(\frac{\Delta T_1}{\Delta T_2}\right)^K \tag{2.b}$$

2.1.2. Power cycling test – PC

In this case the power module is mounted on a heat sink similar to a typical power electronics application, then is heated up electrically by conduction losses. The heated up is stopped when the maximum target junction temperature in the power module is achieved, and the power module cools down to a specified temperature, thus completing the power cycling test.

Figure 11 Power cycle set-up example.

The gradient of temperature junction inside is considerable, in the Figure 10, below a graph of the temperature evolution is show.

To control the temperature during the test the heat sink temperature is adjusted.

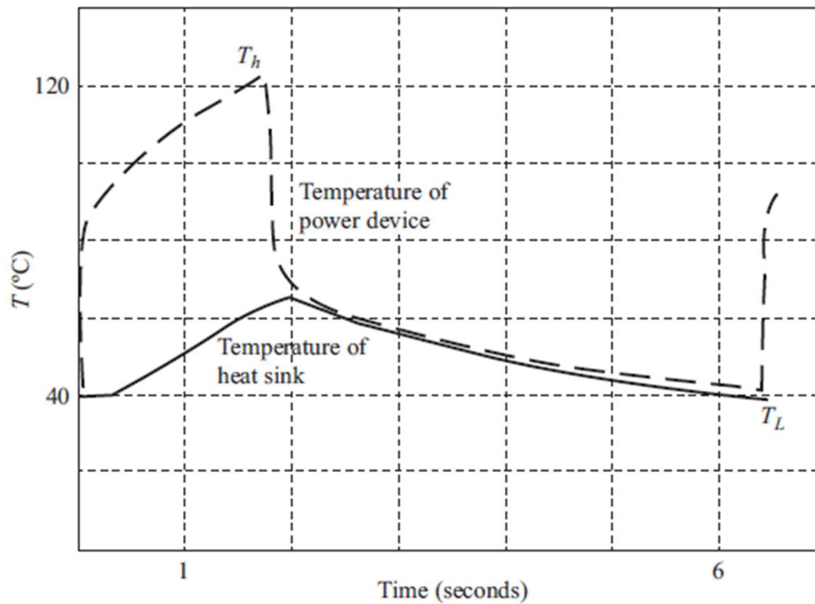


Figure 12 Powe cycling plot for a power module.

The graph indicates a case where T_h is the upper limit, after that the active heating of the device is stopped and cooling commences immediately. Later the device junction temperature decreases. Once the T_l is reached the load current is turned on to initiate active heating again and the cycle is repeated.

The medium temperature for the power cycling test is defined as:

$$T_m = T_L + \frac{T_h - T_L}{2} \quad (2.c)$$

The thermos-mechanical stress caused by the repetitive heating/cooling on/off cycles can lead to failure cracks in the power module.

Usually, 6000 cycles for temperature variation of 100°C and 3000 cycles for a variation of junction temperature of 125°C, this is valid for large power packages or modules according to JESD22-A122. A usual on/off cycle is 5 minutes of on time and 5 minutes of off time.

A long power cycle time usually creates a higher stress in the devices. Between the different CTE of the layers in the module. Difference in CTEs of different layers of materials in the power package or module during the temperature excursion create thermos-mechanical stress at the interfaces between these layers [5].

It can be seen that the temperature variation is higher on the junction of the power semiconductor devices than in the heat sink.

Taking in consideration that this stress is repeated overt test, cracks may occur in the solder attachment between the devices and power substrate. When these cracks reach the bottom of the power chip, they cause an increase in thermal resistance and a subsequent increase in junction temperature of the power semiconductor devices. The stress also can lead to the fatigue of materials and interconnections.

There are two main challenges:

- The interdependency of various failure modes and the failure analysis of failure power modules.
- The measurement of T_j due to the transient nature.

2.1.3. Accelerated cycling tests.

PECS, such as those used in civil and electrical vehicles, require long-lasting lifetime guarantees that span years or even decades. However, collecting system information for reliability assessment under real-life conditions over an extended period of time is not practical due to the fast-paced technology changes.

Manufacturers of power modules must provide warranties for their products. As a result, accelerated PC and TC tests have become the industry standard for lifetime estimation of power modules.

These tests are designed to speed up the failure modes that occur in real-world applications due to thermally induced wear and tear. Endurance and reliability test setups for semiconductor devices, such as IEC 60747-34 and IEC 60747-9 [11] [12], are defined by the IEC International Standards. However, the exact procedures for PC and TC tests, such as load current levels and heating-cooling times, are mostly product-specific and independently defined by manufacturers.

2.2. Measurements of Power Module characteristics

Any changes in the health status of the IGBT as result of common failures in power modules are reflected in IGBT temperature junction change.

In order to measure power switch characteristics under different fault and operating conditions, a monitoring and measurement unit (MMU) was developed, as illustrated in Figure 12., this provide a condition monitoring, and correlate the failure precursors by developing a machine learning algorithm to assess the health status with on field device degradation by measuring of the temperature sensitive electrical parameters (TSEPS), this is the mainstream choice for temperature junction estimation /monitoring compared to thermal-electric models.

The MMU design process involved modifying the power switch driver of the inverter circuit [13], by incorporating selector switches and data processing tools to enable efficient measurement of the characteristics. To prevent the MMU from failure due to high voltage and current thresholds, a protection circuit was included in the design, consisting of a diode, Zener diode, and current limiting resistor connected across the inverting and noninverting inputs. The Zener diode and diode in antiparallel configuration across the power switch clamp the off-state voltage, while the embedded resistor restricts the current through the off-state of the Zener diode.

The MMU employs two current sources, a low current source of 100 mA for sensing temperature-sensitive electrical parameters and a high current source of 50 A for providing high current pulses during the monitoring process. To ensure uninterrupted monitoring during converter operation, a double pole changeover (DPCO) switch is incorporated in the MMU circuit.

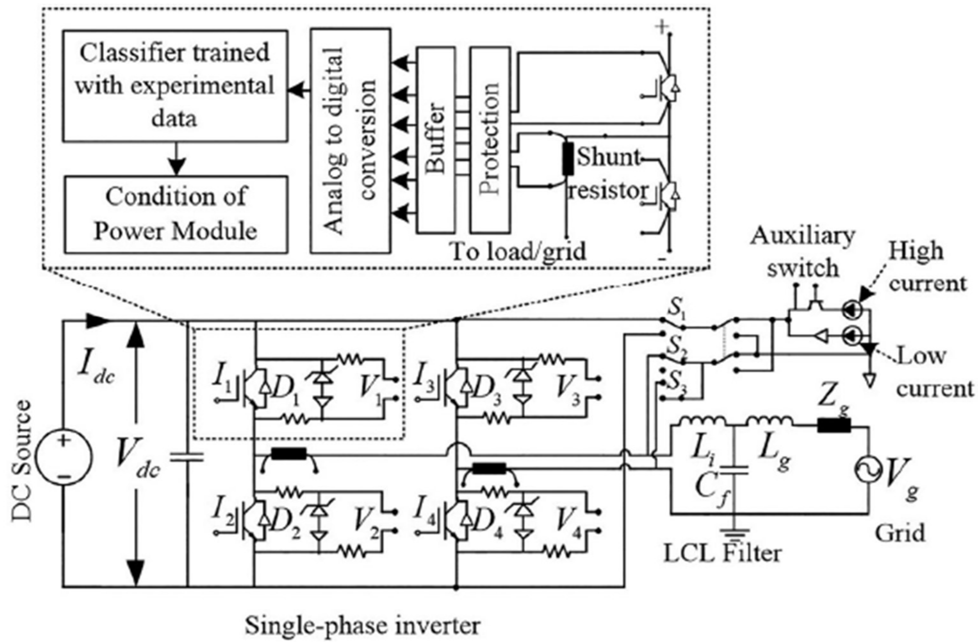


Figure 13 Scheme of grid connected single phase inverter with MMU.

2.2.1. Thermo Sensitive Electrical Parameters

The most promising way to conduct online temperature measurements on fully packed devices is via thermosensitive electrical parameters (TSEPs).

Sensing the junction temperature during converter operation is notoriously difficult, and the selection of a measurement method is made with careful consideration.

Direct access to chips is prevented by module packaging and dielectric gel, which therefore limits the use of optical and physical contact methods such as infrared cameras or optical fibres. The main disadvantage is that these solutions are also limited by temperature range and have a relatively low response time.

The electrical method is preferred for online temperature measurements in power electronic converters, there are two principal families in the literature:

- The use of supplementary sensors located on the chip surface.
- The use of TSEPs of the chip

The first solution is not popular as requires alteration of the package device, although the results that provide are accurate with an ample time resolution that enables tracking of the temperature ripple in the IGBT due to the alternating output current in the inverter application.

Other solutions include sensors integration in the power chip structure. However, this solution allows a local measurement of the temperature and present some issues.

Is important to find TSEPs that are specifically adapted to online temperature measurements the use of either static or dynamic characteristics are both to considerate.

- Static characteristic I(V): this characteristic of all power devices depends on the temperature, a natural way to estimate the junction temperature of a device is simultaneously measure its forward voltage and the current crossing it. This method does not require any additional current sensor because the current in the device can be measured at load level.

- Dynamic characteristics: another way to estimate the junction temperature during the operation of a converter is the measurements of dynamic parameters of power devices.

The online TSEP's [14] allow the measure without modification of the chip, this approach use the chip as the temperature sensor and are often considered to provide a measurement that is influenced by its total active area. The online TSEPs can be described as embedded temperature junction measurements. Offline TSEPs are those measurements where the IGBT is physically removed from the application and tested in the laboratory.

Figure 14 Characteristics of different TSEPs

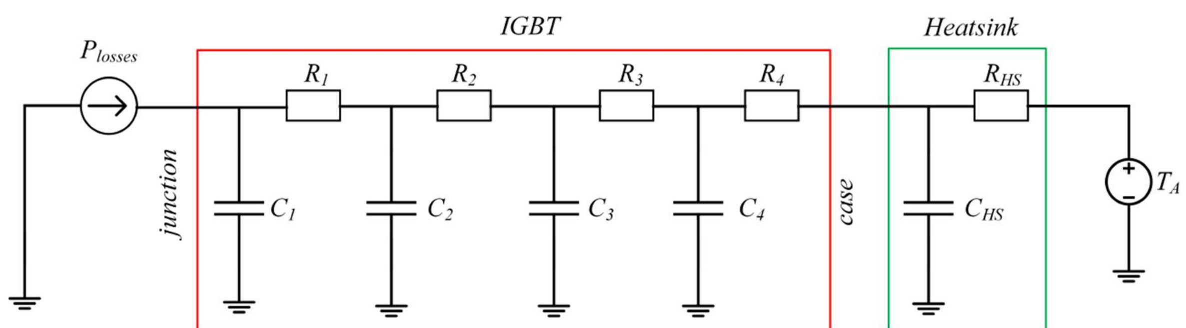
TSEP measurements (temperature range 25°C-175°C)		Parameters			
		Terminal	Sensors required	Sensitivity error	Relative sensitive error
Turn on state	$V_{GE(th)}$	Gate-emitter	Voltage, and current	-10 mV/°C	0.15 % /°C
	$I_{c(sat)}$	Collector-emitter	Current	14 mA/°C	0.36 % /°C
	$\frac{dI_c}{dt}$	Collector-emitter	Current	9 A/µS/°C	0.18 % /°C
	$t_{d(on)}$	Gate-emitte/Collector-emitter	Voltage, and current	-0.36 nS/°C	0.14 % /°C
On/off phase	$V_{CE(sat)}$	Collector-emitter	Voltage	8 mV/°C	0.22 % /°C
	$I_{c(leak)}$	Collector-emitter	Current	10 mA/°C	0.62 % /°C
Turn off state	$\frac{dV_{CE}}{dt}$	Collector-emitter	Voltage	-34 V/µS/°C	0.24 % /°C
	$\frac{dI_c}{dt}$	Collector-emitter	Current	-22 A/µS/°C	0.27 % /°C
	$I_{c(tail)}$	Collector-emitter	Current		0.15 % /°C
	$t_{d(off)}$	Gate-emitte/Collector-emitter	Voltage, and current	0.38 nS/°C	0.26 % /°C
	$V_{GE(miller)}$	Gate-emitter	Voltage	-1 mV/°C	0.01 % /°C
	$t_{V_{GE(miller)}}$	Gate-emitter	Voltage	0.11 nS/°C	0.05 % /°C

2.2.2. Thermal modelling

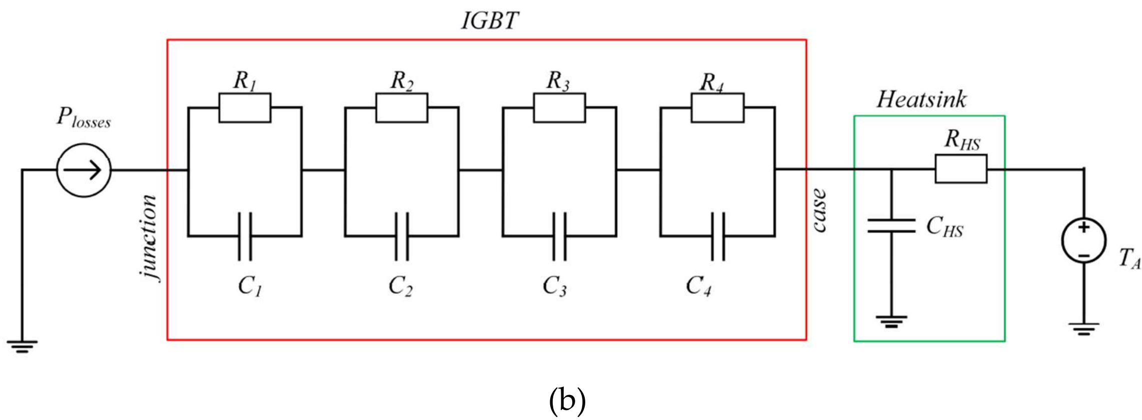
One-dimensional thermal networks such as the Cauer and Foster models offer a simplified solution to thermal issues in Power Electronics (PE).

These networks consist of thermal circuit elements like thermal resistances (R_{th}) and thermal capacitances (C_{th}). While C_{th} is used to model the transient response, only R_{th} can be used to model the steady-state thermal behaviour, similar to an electric circuit [15]. The Cauer model is physically interpretable since the internal node of the Cauer network is directly associated with the layers of the power module, unlike the Foster model where only the input node with respect to the power source corresponds to an actual physical point of the power module. Despite their differences, both thermal models return the same transient behaviour of the input node, i.e., the same overall thermal system impedance, (Z_{th}), even for different sets of R_{th} and C_{th} used to define the Cauer and Foster models.

The Foster model provides an advantage in that It offers a straightforward analytical expression for Z_{th}. This expression can be used to numerically calculate the thermal response of the overall power module structure under an application-given mission profile. In real operation conditions, the power module's layers experience different temperature distributions in both lateral and vertical directions. With non-constant temperatures over the surface area, the main question with physics-based lifetime modelling is which temperature value should be used in the corresponding lifetime models: the average, maximum, or minimum temperature.



(a)



(b)

Figure 15 (a) Caieur thermal model, (b) Foster thermal model

2.3. Lifetime models for IGBTs

The Power Electronic Converter Semiconductors (PECS) are equipped with power modules that are designed to handle high levels of switching current and blocking voltage. However, during field or test operations, the power losses generated by these modules cause temperature variations that create thermos-mechanical stresses within the modules, eventually leading to wear-out and degradation of functionality.

To develop a lifetime model for these power modules, the power losses of the PECS must first be calculated using electrical circuit simulations. These calculations are then translated into temperature profiles via thermal modelling. Since direct temperature measurements of the power module layers are not practical, thermal modelling and simulation are necessary to gain knowledge and information about the temperature distribution within the power module structure.

Since the electrical properties of switching devices are temperature-dependent, accurate determination of the temperature behaviour might require the use of thermos-electric modelling. Thermal modelling is thus an essential component of the lifetime prediction approach.

The lifetime modelling approach is based on the correlation of the number of cycles to failure, N_f, with the corresponding temperature profile obtained from either PC or TC tests. Lifetime modelling of power modules is highly dependent on cycling test results, and two distinct approaches can be employed: empirical lifetime models and physics-based lifetime models.

Detecting and inspecting degradation in electronics is challenging due to the complex architecture and micro- to nano-scale size of electronic products. Unlike mechanical systems and structures, faults in electronic products do not necessarily result in failure or loss of designated electrical performance or functionality. Therefore, quantifying

product degradation and predicting the progression from faults to final failure is difficult.

As a result, the implementation of diagnostic and prognostic systems that can directly monitor faults or the conditions in which faults occur in electronics can be more challenging.

Prognostics and health management (PHM) is a method that enables the evaluation of a system's reliability in its actual life-cycle conditions to predict the onset of failure and mitigate system risks. Safety-critical mechanical systems and structures, such as propulsion engines, aircraft structures, bridges, buildings, roads, pressure vessels, rotary equipment, and gears, have experienced advancements in sensor systems developed specifically for in-situ fault diagnosis (condition monitoring) and health and usage monitoring, resulting in improved performance and safety.

2.3.1. Empirical lifetime models

Empirical lifetime models have been developed based on extensive data collected over many years for different module technologies, is expressed in terms of the number of cycles to failure,N_f This model is derived from empirical observations and large databases of PC test results.

Empirical models are used to describe the dependence of N_f on various parameters of PC tests, such as maximum, mean, or minimum temperature, cycle frequency, heating and cooling times, load current, as well as the power module's properties, including blocking voltage class and the geometry of bond wires. PC tests are conducted to investigate the influence of PC test parameters on N_f-results. The dominant failure mechanisms observed during PC experiments are failures of bond wires and solder interconnecting layers, which typically limit the end-of-life of power modules.

However, the main drawback of this kind of model is that is purely statistical and do not directly describe and asses the deformation mechanisms of power modules invoked under complex thermal loadings.

2.3.1.1. Empirical lifetime models example

The Power Modules are exposed to periodic thermos-mechanical stress, the Coffin-Manson law can be used to relate the number of cycles to failure, N_f, and the temperature change reached in the applied power cycles.

They have strong influence on the number of the number of cycles to failure.

The experience gain in PC experiments indicated that the other PC parameters besides the temperature change (ΔT) also have a strong influence on the number of cycles to failure.

2.3.1.2. LESIT project, Arrhenius approach

In the 90's, the LESIT [16] project was conducted for standard power modules with Al2O3 ceramic substrate and copper baseplate from different manufacturers.

As a result, the influence of the average junction temperature, $T_{j,m}$, was included in to the Coffin-Manson N_f-model via the Arrhenius approach as

$$N_f = a * \left(\Delta T_j\right)^{-n} * e^{\frac{E_a}{k_b T_{j,m}}} \tag{2.d}$$

- ΔT_j is the peak to peak variation of the junction temperature cycle
- $T_{j,m}$ is the mean temperature in Kelvin.
- k_b is the Boltzmann constant.
- $a, n\ and\ E_a$ are the model parameters determined by fitting to the experimental PC data.
- E_a represents the activation energy that characterizes the deformation process.

This analytical lifetime model corresponds to linear functions in a log-log, i.e., $\log(N_f) - \log(\Delta T_j)$, plane for different average junction temperatures, $T_{j,m}$.

2.3.1.3. SEMIKRON lifetime model

For advanced power modules with sintered chips, SKiM modules.

The modules exhibit a significant lifetime improved as the classical solder process for the die attach is replaced by Ag diffusion sintering technology, the Al wire bond geometry is optimized, and the height of the bond wire loops was increased.

With this new optimization the failures modes present were bond wire lift-off and heel cracking, so that the developed lifetime model corresponds only to the failure mechanisms due to thermos-mechanical stress of bond wires [17].

$$N_f = A * \left(\Delta T_j\right)^{\alpha} * ar^{\beta_1 * \Delta T_j + \beta_0} * \frac{C + t_{on}^{\gamma}}{C+1} * e^{\frac{E_a}{K_b T_{j,m}}} * f_{diode} \tag{2.e}$$

- A is the scaling factor.
- $\Delta T_{j,m}$ is the absolute medium junction temperature in Kelvin.
- k_b is the Boltzmann's constant.
- E_a is the activation in energy in eV.
- $f_{diode}$is the de-rating factor applied for the test on free-wheeling diodes.

- β_0 and $\beta_1$are the model coefficients determined together with the other model parameters $A,\ \alpha,\ C, \gamma, E_a,\ f_{diode}$ using a least square fitting procedure.

In comparison to the previous model is shown that:

- Wire bond lifetime is less affected by the medium junction temperature than the lifetime of the chip solder, which is reflected by lower activation energy E_a.
- The chip solder degradation is dominant for high temperatures.
- For intermediate temperature range both failure mechanisms, i.e., solder failure and bond wire lift-off occur and lead gradually to the module's EOL.

2.3.1.4. INFINEON lifetime model

After PC test were conducted by ABB, they manage to characterize the influence of the heating time t_{on}has a severe impact on the lifetime of power modules and represents an important ageing accelerator, here is mentioned the lifetime model of 5th generation IGBT devices [18].

$$N_f = K * \left(\Delta T_j\right)^{\beta_1} * e^{\frac{\beta_2}{T_{j,max}}} * t_{on}^{\beta_3} * I^{\beta_4} * V^{\beta_5} * D^{\beta_6} \qquad (2.f)$$

- t_{on} heating time
- $T_{j,max}$ absolute maximum junction temperature
- I current per wire bond stitch
- D diameter of bond wires
- V blocking voltage of chip on the PC capabilities

The impact of these parameter is assumed to have power law nature and, thus, the dependency of number of cycles on the heating time, I, V and D can be described by a linear log-log characteristic. The model presented is purely based on large number of PC test results from different module technologies.

The limitation of the model proposed are:

- In this model the limitations due to substrate baseplate solder failures are not included.
- The lifetime model presented is not applicable for the power modules used in traction applications, as the assumed relation between the blocking voltage and chip thickness does not apply to modules for traction applications, because the relation between the blocking voltage and chip thickness is not considered.

- The model parameters cannot be set independently during the PC experiment. The heating time and a certain maximum temperature are correlated by the nature of power module and PC tests.

2.3.1.5. Monte Carlo analysis

This analysis that is going to be presented, takes into consideration the thermal stress parameters and the dynamic of the mission profile during a year, in a PV plant.

The goal is to consider the uncertainties in the lifetime estimation process, and how this is able to impact on the reliability, by applying the simulation of Monte Carlo (MC) method on a certain number of samples [19]. With this test, the researcher was able to compute the accumulated damage distribution by applying a variation to the static parameters. If the high dynamics of the mission profile is not included, it can happen that the estimation model is underestimated.

The stress parameters [18] [20] that are present by the semiconductor manufacturers are typically:

- Junction temperature-T_j
- Temperature swing-ΔT_j
- Minimum junction temperature-$T_{j\,min}$
- Heating time-t_{on}
- Current per bond wire-I_B
- Bond wire diameter-D
- Voltage class-V_c
- Activation energy-E_a
- Bond wire aspect ratio-ar

For an empirical lifetime model in, that predicts the bond-wire failure for IGBTs, it can be noticed that there are several model parameters that may introduce uncertainty, in this case the model used was the following:

$$N_f = K * \left(\Delta T_j\right)^{\beta_1} * e^{\frac{\beta_2}{T_{j,min}+273}} * t_{on}^{\beta_3} * I^{\beta_4} * V^{\beta_5} * D^{\beta_6} \quad (2.g)$$

Where β1 to β6, are the model fitting parameters, A the technology factor.

N_f is the number of cycles to failure and n_i the number of cycles. After this has been found the Miner damage model [21]is used to compute the lifetime consumption of the semiconductor (LC).

$$LC = \sum_i \frac{n_i}{N_{fi}} \qquad (2.h)$$

For model fitting parameters (β1 and β2), the interval of variance is already given.

The junction temperature parameters in the model will also vary. It is widely accepted that a normal distribution with a certain variation range (e.g 5%) is assumed for the lifetime model parameters representing the variations in the semiconductor device manufacturing process.

The bed-test in this case is a two-level invert used in a PV application with a traditional linear controller, and an algorithm to extract the maximum power, and MPPT.

What can make the difference in the lifetime estimation is the junction temperature parameter variation applied to a dynamic or to a static mission profile, that in the case of the PV plant means a fluctuation on the energy produced on day (with or without clouds).

Three different types of MC simulations will be considered in this paper for estimating the lifetime of semiconductor devices in the PV applications:

- Monte Carlo with static parameters (MC-SP)
- Monte Carlo with semi-dynamic parameters (MC-SDP)
- Monte Carlo with dynamic parameters (MC-DP)

Afte the MC simulation were done, the end-of-life cumulative distribution function (cdf), and the unreliability function F_{sys} can be determined.

$$F_{sys}(x) = 1 - (1 - F_{T1}(x)) \qquad (2.i)$$

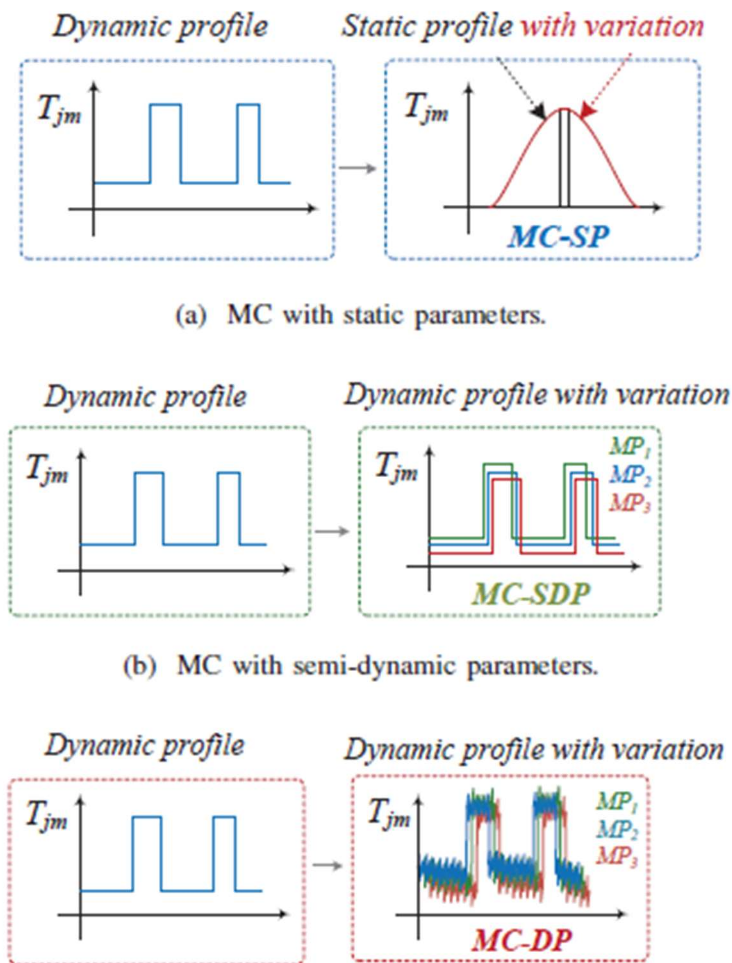


Figure 16 Conversion to the dynamic mission profile to the different parameter variance and profile

A population of 10 000 devices was used in the three MC methods. Among the three MC methods the MC-SP is the fastest method and MC-DP is the slowest.

To illustrate the execution time, the MC-SP was executed in 1 second for the PV application, which had a mission profile of almost 104 000 samples, while the MC-DP needed 300 seconds. In Fig. 12a a lifetime model parameter variation of 5% the cdf plots for the PV inverter can be observed.

All three MC methods showed different unreliability functions.

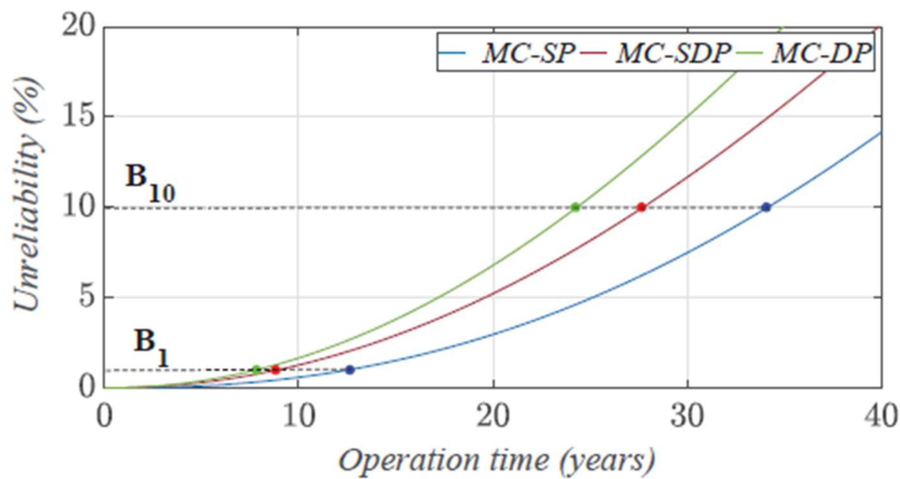


Figure 17 Comparison of unreliability function for 5% lifetime model parameter variation using MC-SP, MC-SDP, MC-DP.

The MC-SP results in the longest expected lifetime, while the MC-DP results in the shortest.

There is also a difference on the time consumption for the computational burden. Therefore, it can be seen how the introduction of uncertainties on the thermal stress parameters on the lifetime model (in this case Couffin-Mason), and in the mission profile, has an impact in terms of time, computational burden, and complexity [19].

2.3.2. Physics based lifetime models.

Physical modelling is necessary in order to understand the failure and deformation mechanisms of power module assemblies. By modelling the stress and strain development, it is possible to directly correlate these factors to the number of cycles to failure. This is the basis for PoF analysis, which provides a more detailed physical description of observed failure mechanisms and can be a promising alternative to the empirical lifetime models already presented previously [5].

Direct measurement of stress and strain in electronic packages requires high-resolution methods such as infrared and scanning electron microscopy. Alternatively, stress-strain simulations can be conducted using computational mechanics, such as Finite Element Analysis (FEA). However, FEA requires detailed knowledge of the material and geometry properties of the power module assembly, which may not be readily available.

An alternative method for stress-strain modelling is based on numerical approaches to calculate the stress-strain response under given temperature profiles, and then using a parameterization procedure based on the experimental data. This is described in more detail in the following section.

There are several existing physics-based lifetime models of power modules in the literature. These models are briefly summarized to highlight the state-of-the-art for PoF analysis in Power Electronics.

2.3.3. Exponential fitting model

The conventional way to estimate junction temperature can be resumed in the following steps:

1) Calculating the power losses at each step
2) Multiplying the losses with the thermal impedance
3) Adding the generated heat in the device to the case temperature.

However, due to the solder degradation and thereby change in the thermal impedance, the estimated junction temperature may not be accurate. The advantage of the method that is that it doesn't require the measurement of the temperature at the junction.

This approach introduces a non-invasive fault diagnosis on power converters. It takes in consideration the variation of on-state resistance as the main failure precursor. The variance on this variable can be caused due to bond-wire degradation, gate-oxide degradation, and cracks and delamination in the die attach solder. Therefore, the exponential degradation model is developed thanks to experimental data [22].

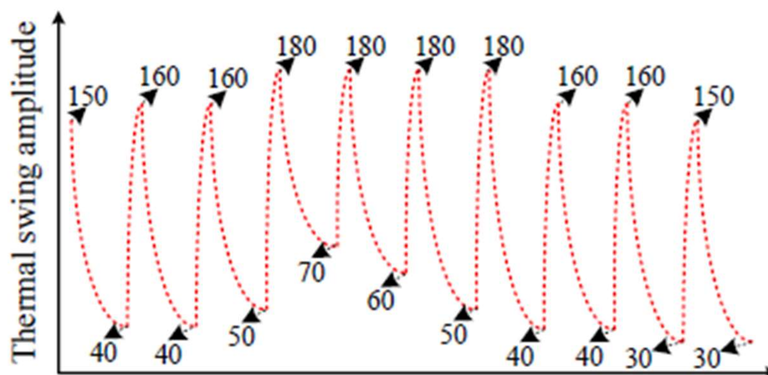


Figure 18 Thermal swings applied.

The degradation growth can be modelled from the experimental data due to lack of information on the physical modelling of the device.

The On-state resistance can be expressed as the sum of the individual resistance of the different layers on the power device ($R_{ds,on}$). On this case the test on the power

device includes accelerated temperature cycles, see fig. 16, to accelerate the aging mechanisms.

The test-configuration included the measurement taken in order to compute the On-state resistance, therefore each V_{ds} and I_D are detected and transmitted to data acquisition system together with the T_c.

The power device is used as main load without adding an external load.

As it can be observed from Fig. 17, the $R_{ds,on}$ increases exponentially with respect to thermal cycles in the defined RUL estimation zone with an initial value (R_{init}).

The degradation process can be modelled with an exponential curve, and an added offset value as:

$$R_{ds,on}(t) = \alpha e^{\beta t} + R_{init} \tag{2.j}$$

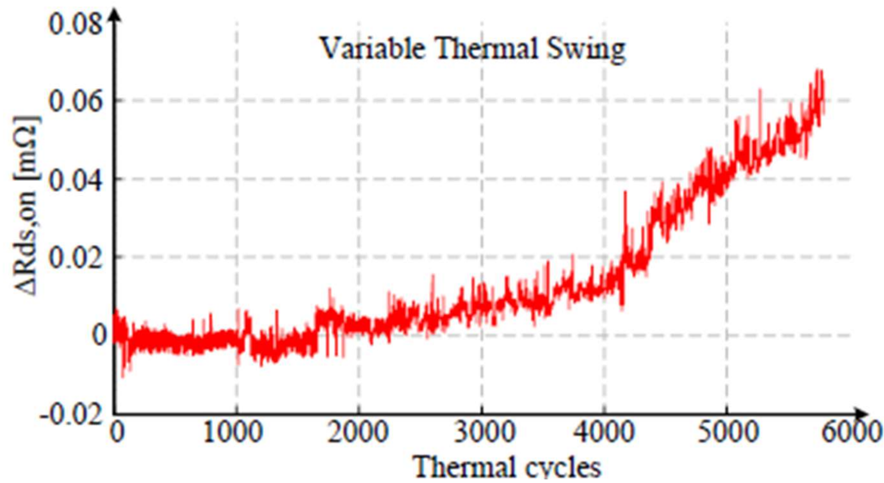


Figure 19 On-state resistance variation after the thermal swings.

The clear that fault growth trajectory of the degraded switches can be estimated within sufficient error margin, when α and β are computed using all the data points. However, this leads to “offline” estimation. It is worth recalling that α and β are assumed as constants in Eq. (12). The relation between α and β and state estimate is quite difficult to obtain as it requires detailed physical description of the device. Furthermore, incorporating such relations would reduce the robustness of the RUL estimation tool. In order to make the estimation online but still avoid the physical relations, “least squares” fitting is used to achieve exponential fitting. The exponential

curve can be written in the form as in Eq. , ignoring the initial value, and taking the natural logarithm of both sides.

$$ln\Delta R_{ds,on} = \ln\alpha + \beta x \quad (2.k)$$

$$\alpha = e^{a} \quad (2.l)$$

$$\beta = b \quad (2.m)$$

$$\Delta V_{ce,on}(\%) = \alpha e^{\beta x} \quad (2.n)$$

$$a = \frac{\sum_{i=1}^{n} x_i^2 y_i \sum_{i=1}^{n} y_i \ln y_i - \sum_{i=1}^{n} x_i y_i \sum_{i=1}^{n} x_i y_i \ln y_i}{\sum_{i=1}^{n} y_i \sum_{i=1}^{n} x_i^2 y_i - \left(\sum_{i=1}^{n} x_i y_i\right)^2}$$

$$b = \frac{\sum_{i=1}^{n} y_i \sum_{i=1}^{n} x_i y_i \ln y_i - \sum_{i=1}^{n} x_i y_i \sum_{i=1}^{n} y_i \ln y_i}{\sum_{i=1}^{n} y_i \sum_{i=1}^{n} x_i^2 y_i - \left(\sum_{i=1}^{n} x_i y_i\right)^2} \quad (2.o)$$

By inputting different amounts of data acquire the fitting curve, fitting are performed on 50, 150, and 250 data of DUT8 and DUT9 respectively.

The prediction error is 55.4%, 36,5%, 4.9% with fitting 12%, 35%, 58% of the aging data on DUT8. And the prediction error is 65.8%, 7.9%, 9.2% with fitting 11%, 34%, 57% of the aging data on DUT9.

The safe RUL threshold value for the tested switch is determined as 50mΩ, that correspond to 12% of its initial value.

This model has much larger error especially at early stage, therefore, this method is difficult to provide a decent result when the data is not sufficient. One possible way to reduce the measurement error and model uncertainties include the Kalman filter [23].

The advantage of this method is the non-intrusive measurement of the power devices and that it doesn't need an estimation of the temperature junction, variable that is

usually used on the empirical lifetime methods, for example on the Coffin-Manson Model.

2.3.4. LSTM neural network

In this method here presented the V_{ce-on} is the online aging precursor taken in consideration [24] [25], the measurement is provided thanks to a measurement circuitry, Figure 18.

In order to estimate the remaining useful lifetime (RUL) of a system, a precursor is typically used. This estimation can be achieved through two different approaches: model-based and data-driven.

Model-based approaches are often empirical and rely on exponential equations, as previously presented. On the other hand, data-driven approaches utilize machine learning algorithms to generate more fitting equations. In the case of RUL estimation, a long short-term memory (LSTM) recurrent neural network (RNN) is commonly used [26] [27].

One disadvantage of RNNs is the issue of vanishing and exploding gradients. However, LSTMs are capable of learning long-term dependencies in sequences of data, making them well-suited for processing time series data to predict future results. The standard LSTM network includes an input gate, forget gate, output gate, and memory cell state [28].

The gates are comprised of neurons that decide which information to input, forget, or output based on the previous output and current input, as well as memory information.

The cell state acts as the memory of the network, storing information that needs to be remembered and accessed and updated by the LSTMs at a different time in the future. The operation process of an LSTM cell is illustrated below.

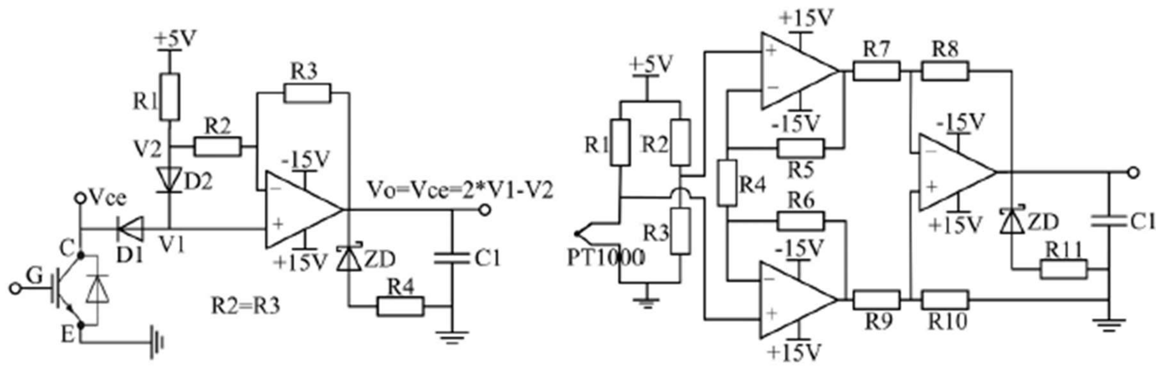


Figure 20 Online voltage measurement circuit, and temperature measurement ciruit

The function tanh is used to overcome the vanishing gradient problem, and the activation function f is usually a sigmoid function that can output between 0 and 1 to mimic open and close the gate. Xt and ht represent the input and output information of the LSTM, and Xi, Xf, Xo respectively denotes the control signal of input gate, forget gate, output gate. After each operation, the new value c’ will replace the previous one in the memory cell. Fig. 9 shows the information transfer and update between the LSTM cells. The cell state of the LSTM consists of a long-term state (ct) and a short-term state (ht). The modulation unit, input gate, forget gate and output gate which form the core of an LSTM cell are denoted by gt, it, ft and ot respectively. The current memory cell and previous one is denoted by ct and ct-1, ht as well as ht-1 represent the output of the current LSTM cell and the previous one.

The information flow in the LSTM cell is characterized by following Eq. (13).

$$g_t = \tanh\,(W_c[h_{t-1}, x_t] + b_c)$$
$$i_t = \sigma\,(W_i[h_{t-1}, x_t] + b_i)$$
$$f_t = \sigma\,(W_f[h_{t-1}, x_t] + b_f)$$
$$o_t = \sigma\,(W_o[h_{t-1}, x_t] + b_o)$$
$$c_t = \mathrm{g_t} o i_t + c_{t-1} * f_t$$
$$h_t = o_t \mathrm{o} \tanh\,(c_t) \qquad (2.p)$$

The weight matrix and biases vector of input gate, output gate, forget gate and memory cell are respectively denoted by Wi, Wo, Wf, Wc and bi, bo, bf, bc. All these trainable parameters are shared between all the time steps and are tuned while presenting the network with training samples. σ represents the sigmoid activation function and denotes the element wise multiplication operator.

The neural network is trained by feeding the time series data which obtained from the aging test sequentially. First, the weights of the network are initialized randomly. In the forward pass the output of the network is obtained, then the output is compared with the actual result, and the neurons in the LSTM network will remember the characteristic information, and then stored in the memory cell. Meanwhile, the data in the memory cell will be refreshed every training.

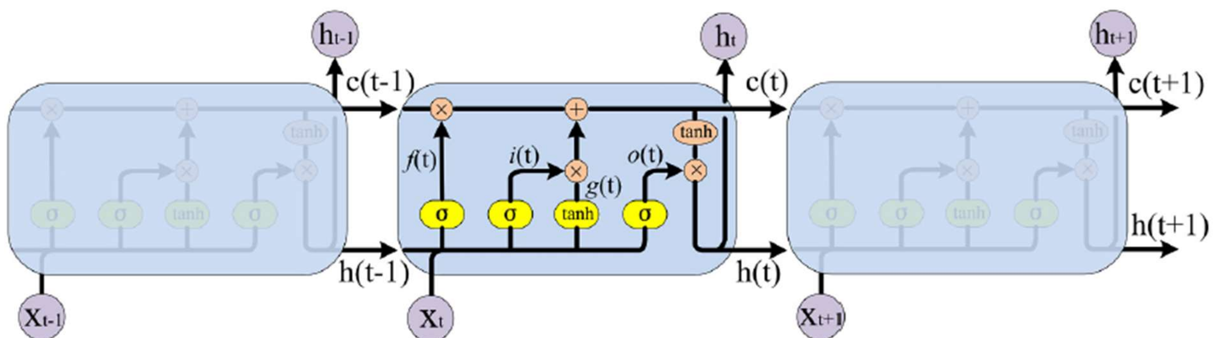


Figure 21 The structure of LSTM cell.

Validation (LOOCV) methodology which is useful for small data set condition [22-24]. The basic idea of LOOCV is to split the data into N-1 training-set and one validation-set, the training-set is used to train LSTM network and the validation-set is used to test the trained network, and then repeat this step N times. LOOCV methodology is equivalent to training the neural network with N times the original data set, which can "make full use" of limited data to find suitable model parameters

and prevent over-fitting. The prediction results on DUT8 and DUT9 of LSTM neural network trained by LOOCV methodology are shown in Figs. 10 and 11.

The purple curve denotes the actual measured data, the green one denotes the input data to LSTM and exp. fitting, the red line represents the prediction result of the network, the blue one is the exponential fitting curve. Comparing the actual test data with the LSTM prediction results, when the DUTs meet the same failure criteria, i.e. the ΔVce-on grows to a failure threshold, the prediction error respectively is 7.6%, 6.4%, 2.5% with inputting 12%, 35%, 58% of the aging data on DUT8.

And the prediction error is 9.4%, 3.2%, 2.2% with inputting 11%, 34%, 57% of the aging data on DUT9. It can be seen that the LSTM algorithms can give a quite accurate estimation of the IGBTs' RUL even input very few data. Furthermore, the prediction results keep being updated as the recent input data increases since the LSTM network has a function of autonomous learning and memory.

In conclusion in the methods presented Various temperature fluctuations were utilized in accelerated aging experiments of IGBT, which revealed that Vce-on increases with cycle number, with a positive temperature dependency. In addition, a novel machine learning technique, specifically an LSTM network, was employed to estimate the Remaining Useful Life (RUL) of discrete IGBTs. The results demonstrated that the proposed LSTM neural network can provide a relatively precise lifetime estimation, with a maximum error within 9.4%, 6.4%, and 2.5% when inputting 12%, 35%, and 58% of the aging data, respectively. Compared to two traditional models, the LSTM can detect anomalies and prevent failures even in the early stages, and can also update the prediction results as the input data increases

As a data-driven approach, LSTM neural network can be regarded as the method digging into the real-time "black-box" relations between the time-sequence data. It is not limited to one specific fitting model, like the exponential function, and therefore may be more applicable as the operation profiles are becoming much more complicated.

2.3.5. Aging state evaluation of power module and lifetime based on junction-to-case thermal resistance.

In this case, the relation between two external parameters is analysed, the saturation voltage drop in-between collector and emitter that reflect the aging state of bonding wires, and the junction-to-case, that reflect the fatigue state of the solder layer.

The relationship between the junction-to-case thermal resistance and the aging degree of IGBT power modules, nine IGBT upper tubes were tested according to the ΔTc power cycles experiment.

The IGBT down tube connected to the gate reverses voltage to maintain the off state. Power cycles experiment circuit is shown in Fig. 20. The IGBT on the tube is used to conduct a repeat on and off in the experiment.

In the ΔTc power cycles experiment, the junction-to-case thermal resistance of each IGBT sample is measured once in every 100 times. To get a more accurate number of power cycles, when the junction-to-case thermal resistance is about to increase by 20%, it is measured once per cycle. The thermal resistance test system of Xi'an Yibang Electronic Technology Co. Ltd. YB-6911 was used in junction-to-case thermal resistance experiment. The test system meets the JEDEC51–1 standard. The test heating current of which is 20A and the accuracy is±10 mA.

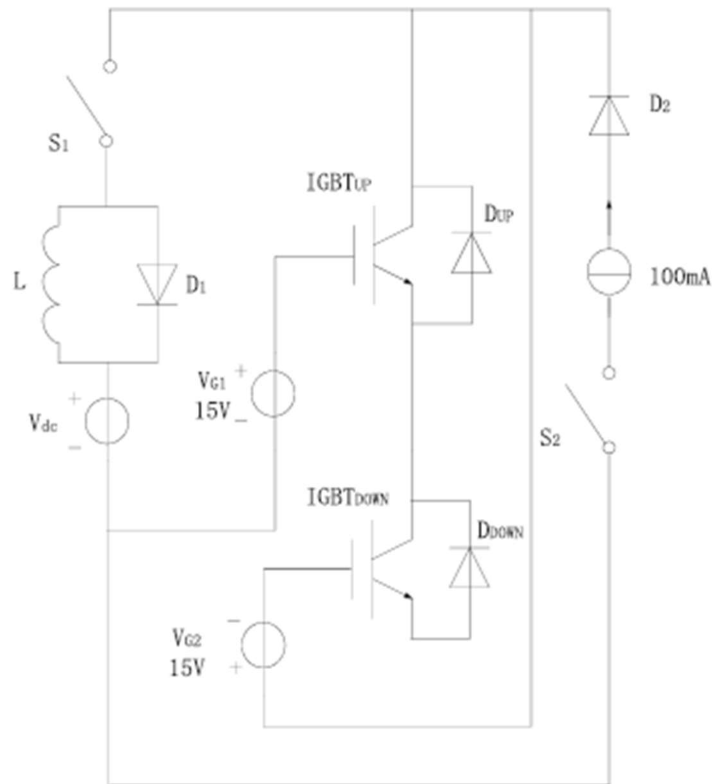


Figure 22 IGBT samples power cycles experiment circuit diagram

When the ΔTc power cycles 6000 times, the junction-to-case thermal resistance change rate in each IGBT sample and exceeds 20%, which means that it meets its failure criterion.

The Fig 21 below shows that the junction-to-case thermal resistance of the IGBT increases with the number of power cycles. The error exists due to manufacturing, experiment errors and other factors.

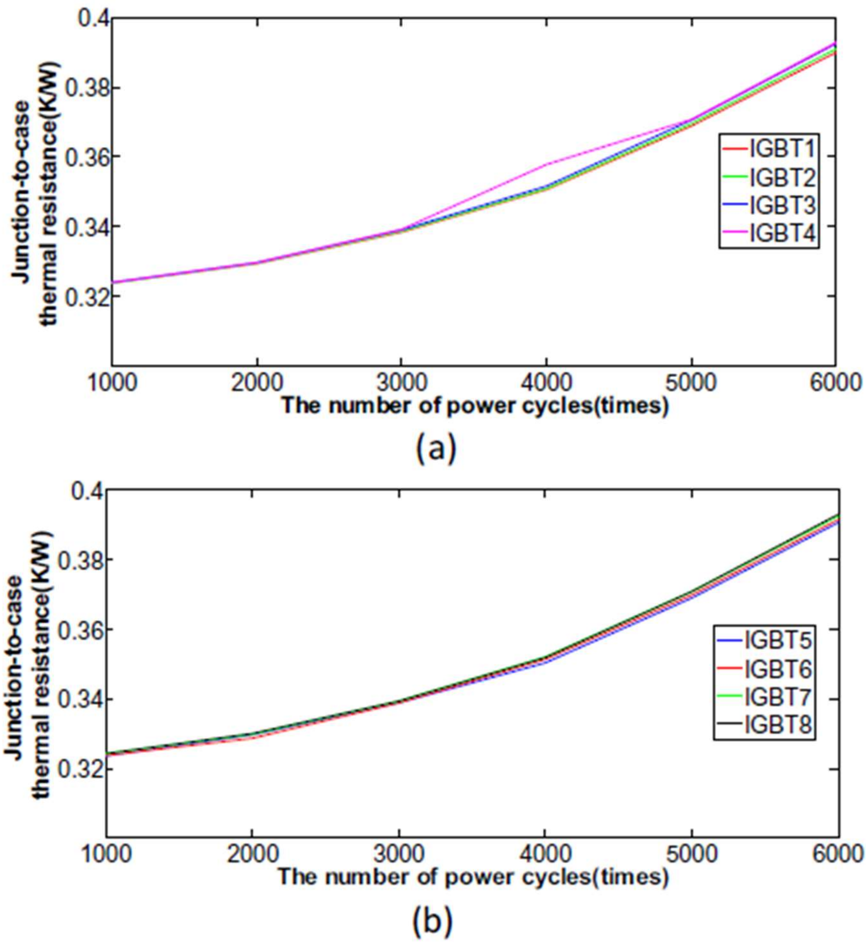


Figure 23 Relationship between junction-to-case thermal resistance and the number of power cycles.

The junction-to-case thermal resistance can reflect the aging state of IGBT. With this study, the purpose was to selects the average junction-to-case thermal resistance as a parameter to evaluate the aging state of IGBT, and to combine the junction-to-case thermal resistance change rate with the number of power cycles. The relationship between them is further studied.

The average junction-to-case thermal resistance change rate of IGBT gradually increases with the increase of the number of power cycle, with a behaviour similar junction-to-case thermal resistance saw.

$$\Delta R_{th} = \frac{(R_{th} - R_{th0})}{R_{th0}} * 100\% \quad (2.q)$$

Where ΔR_{th} is the average junction-to-case thermal resistance rate, and R_{th} is the average thermal resistance of the semiconductor, R_{th0} is the average thermal resistance of the new IGBT.

To find a general functional relationship to describe the relationship of $\Delta R_{th} - n$ in detail, this study uses exponential fitting and polynomial fitting method to search the functional relationship.

$$\Delta R_{th} = \sum A_i e^{\mathrm{B}_i n} \quad (2.r)$$

To summarize, the polynomial fitting method can accurately determine the functional relationship between the average junction-to-case thermal resistance change rate (or average saturation voltage drop change rate) and the current effective working life cycle. This functional relationship can provide a more precise estimate of the current effective working life cycle and remaining lifetime of IGBT power modules. The proposed method is of significant for evaluating the aging state and remaining lifetime of IGBT power modules.

Furthermore, the functional relationships between the average change rate of junction n-to-case thermal resistance and the number of power cycles, as well as the change rate of average saturation voltage drop and the number of power cycles, can be used to judge the degree of aging for any IGBT. However, it is important to note that the study was limited to the aging state of a single type of IGBT module under the same experimental conditions. Therefore, further research on the aging status of different types of IGBT modules will be necessary in future work.

If the aging state evaluation of power module based on saturation voltage drop is considered as an alternative of the junction-to-case thermal resistance change rate the ΔTc power cycles experiment is performed on the upper tube of nine double-tube half-bridge IGBTs in model MMG75S120B.

The goal is to do IGBT modules single-pulse test and obtain its junction temperature, current as well as saturation voltage drop, the test is suspended once in every 100 power cycles. For the accurate number of power cycles, before saturation voltage drop increases by 5%, it is measured once per power cycle, until the number of power cycles on the condition that the saturation voltage drop up to 5% is found. Figure 22 shows single pulse test circuit, R for power resistance, Vdc for the program-controlled DC power.

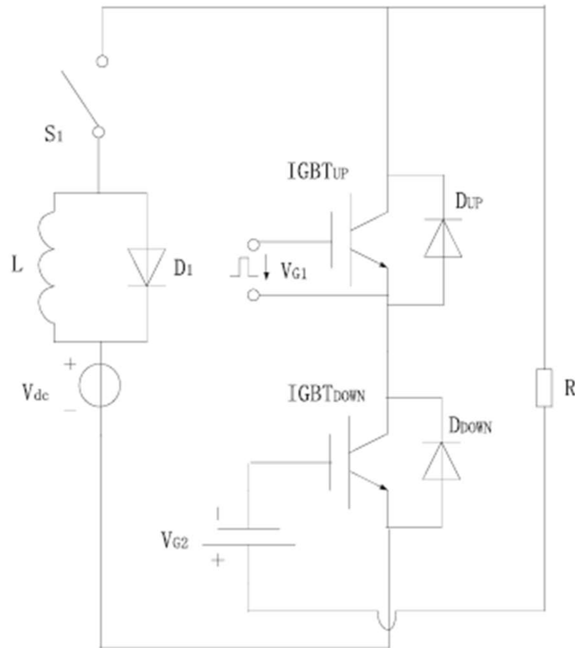


Figure 24 Power cycles test circuit diagram

The IGBT saturation voltage drop is influenced by junction temperature and current, so the test points need to consider both. The test points are selected by the following way. One is that the temperature increases from 25 °C to 125 °C, increasing by 10 °C at a time. Another is that current increases from 5A to 150A, increasing by 5A each time.

The experiment process is as follows.

(1) The IGBT is put into the incubator and the temperature of the incubator is set according to the temperature test point.

(2) After setting temperature test point, when IGBT reaches thermal equilibrium, it can be considered that IGBT junction temperature is the temperature set by the incubator.

(3) The controllable DC power control circuit current is set in turn for the current test point and IGBT is also triggered by a single pulse. Then saturation voltage drop value is measured.

After 3000 cycles of power cycles, the average saturation voltage drop gradually increases and the increasing rate is getting higher and higher, which indicates that the average saturation voltage drop can be used to evaluate the aging state of IGBT. In order to combine the change rate of saturation voltage drop with the number of power cycles, the relationship between the change rate of average saturation voltage drop (has the same form as the the junction-to-case thermal resistance change rate) and the number of power cycles is further studied. The curve obtained from the experimental data is shown in Figure.23.

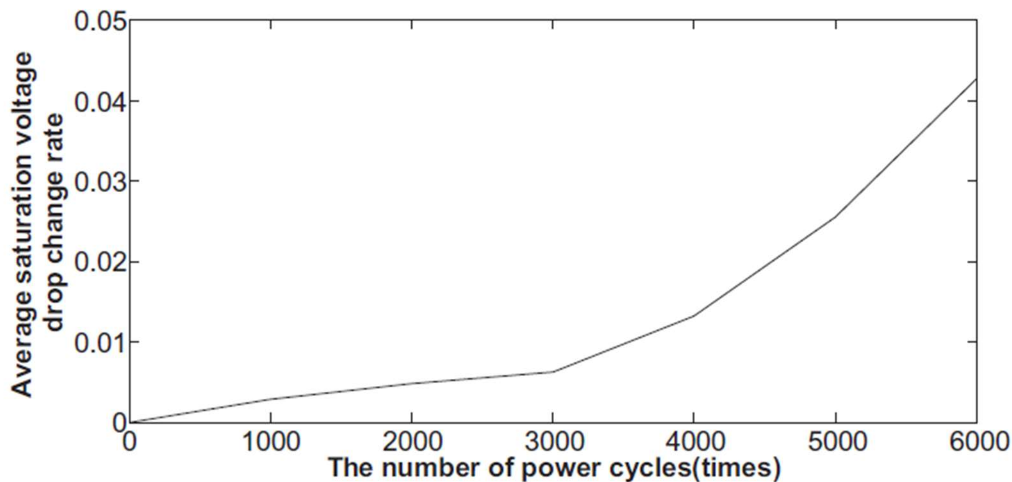


Figure 25 Relationship between average saturation voltage drop change rate and number of powers cycles

Fig. 13 shows that as the number of power cycles increases, the change rate of the average saturation voltage drop is 1% with 3000 times before the power cycle, which is not obvious. After the number of power cycles exceeds 3000, the change rate of the average saturation voltage drop increases in a rapid speed.

In summary, the study mentioned has demonstrated that the use of polynomial fitting method can accurately establish the functional relationship between the change rate of average junction-to-case thermal resistance or average saturation voltage drop and the current effective working life cycle of IGBT power modules.

This relationship allows for a more precise estimation of the remaining lifetime and evaluation of the aging state of the components. While this method has shown great potential for the assessment of the aging state of IGBTs, it is important to note that this study only focused on the same type of IGBT module under the same experimental conditions, and therefore, it may not be applicable to different types of IGBT modules.

Future research should address this limitation and investigate the aging status of various IGBT modules to enhance the applicability of this method. Overall, this research is significant for manufacturers and researchers who are involved in the study of power electronics and inverters, particularly in the context of increasing demand for PECS due to renewable energy and changing climate.

Additionally, it is important to consider the use of AI methods and the understanding of the physics of failure in converter design and optimization.

3 Overview of the predictive diagnosis approach used.

The previous chapter explored various methods for determining the lifetime of IGBTs in power electronics, such as cycling tests, electrothermal models, and machine learning techniques. While each of these methods has its advantages and disadvantages, it is essential to compare and evaluate them to determine which method is most suitable for specific applications.

In this chapter, we will examine the advantages and disadvantages of each of these lifetime methods in more detail. Specifically, we will compare the polynomial fitting method used to determine the functional relationship between the average junction-to-case thermal resistance change rate (or average saturation voltage drop change rate) and the current effective working life cycle, the monitoring measurement unit used to calculate different temperature-sensitive electrical parameters, the LSTM network used to estimate the Remaining Useful Life (RUL) of discrete IGBTs, the junction to case thermal resistance and voltage drop relation , and the compute of aging thanks to polynomial mode.

We will consider various factors when evaluating the advantages and disadvantages of each method, such as accuracy, cost, complexity, and applicability to different types of IGBT modules. Ultimately, this comparison will provide valuable insights into which lifetime method is the most appropriate for specific scenarios and applications.

Overall, this chapter aims to provide a comprehensive understanding of the various lifetime methods available for IGBTs and to aid in selecting the most suitable method for different applications.

3.1. Discussion of the strengths and limitations of the different approach

The table summarizes different prediction approaches for estimating the remaining lifetime of power modules. The Coffin-Manson model with static parameters is a simple and fast empirical method, but it requires multiple test conditions for accurate predictions. The Coffin-Manson model with Monte Carlo-Semi Dynamic Parameter is faster and does not need conversion of the dynamic profile to the static, but it may not account for all the parameters, leading to potential errors. The Coffin-Manson model with Monte Carlo-Dynamic Parameter provides better accuracy by considering the variance of all parameters, but it is computationally burdensome and may result in greater error.

The Exponential fitting model is a data-driven approach that allows for real-time updates and non-intrusive measurement. However, it may have low accuracy at the early stages of the module's life, and the Kalman filter may be needed to reduce measurement error. The LSTM network is a data-driven approach that provides real-time updates, better accuracy, wide applicability, and the ability to detect anomalies and prevent failures at an early stage. However, it requires large amounts of data and is more complex than the empirical methods.

Overall, the LSTM network appears to be the most promising approach for predicting the remaining lifetime of power modules due to its high accuracy and ability to detect anomalies and prevent failures early on. However, it requires a significant amount of data and may be more complex than the other methods.

Lastly, the empirical model of Junction-to-case thermal resistance and Voltage drop relation can estimate the remaining lifetime and compute aging degree, but it is not valid for all IGBTs.

Summary of prediction approaches			
Approach	Category	Advantages	Disadvantages
Coffin-Manson model, Static Parameters	Empirical model	Simple Fast	Multi test conditions required Fastest
Coffin-Manson model, Monte Carlo-Semi Dynamic Parameter	Empirical model	Fast	No need of conversion of the dynamic profile to the static, higher number of simulations
Coffin-Manson model, Monte Carlo-Dynamic Parameter	Empirical model	Better accuracy Consider variance of the therma stress parameters	If it takes in consideration the variance of all the parameters, the computational burden is higher, therefore slower, greater error
Exponential fitting model	Data-driven	Real-time update Non intrusive measurement	Low accuracy at early stage Need of Kalman filter to reduce the error measurement
LSTM network	Data-driven	Real-time update Better accuracy Wide applicability Detect anomalies and prevent failures at early stage Low maximum error respect to the empirical methods	Large data based Complex
Junction-to-case thermal resistance and Voltage drop relation	Empirical model	Estimate remining lifetime Compute aging degree	Not valid for any IGBT

4 Conclusions and future developments

4.1. Conclusions

In conclusion, this thesis provides a detailed analysis of various lifetime methods available for IGBTs in power electronics. We have compared and evaluated these methods based on their advantages and disadvantages, and we have provided valuable insights into which method is most appropriate for specific scenarios and applications.

This analysis is particularly beneficial for manufacturers or researchers who are beginning to study inverters and PECS. The information presented in this thesis can serve as a starting point for selecting the most appropriate method for evaluating the aging state and remaining lifetime of IGBT power modules.

Furthermore, with the increasing use of power electronics in renewable energy plants, it is becoming more critical to consider the physics of failure of the converter. This involves understanding the root cause of failure and how it can be mitigated to improve the reliability and performance of power electronics systems.

This thesis provides a valuable contribution to the field of power electronics and provides guidance for manufacturers and researchers in selecting appropriate methods for evaluating the lifetime of IGBT power modules.

4.2. Implications and suggestions for future research

It is worth noting that the demand for power electronics and PECS is expected to grow significantly in the coming years. This is largely due to the increasing deployment of renewable energy sources such as solar and wind power. As climate change continues to affect the planet, there is a growing need for cleaner, more sustainable sources of energy, and power electronics are a critical component of this transition.

This growth, however, is not without limitations and challenges. As a result, it is becoming increasingly important to ensure the reliability, longevity, performance, and safety, of power electronics systems, particularly IGBTs. The methods and techniques discussed in this thesis are essential for evaluating the aging state, model lifetime and

parameters of degradation of IGBTs, ensuring that power electronics systems operate safely and effectively for as long as possible.

To address these concerns, various lifetime estimation methods have been mentioned and compared, including polynomial fitting, empirical lifetime modelling that includes variance of the parameters, and machine learning. While each method has its advantages and disadvantages, the development of AI and machine learning methods holds promise in improving the accuracy and efficiency of lifetime estimation.

Additionally, we anticipate that AI methods will become increasingly prevalent in evaluating the lifetime of IGBTs in the future. These methods can provide more accurate and reliable estimates of remaining useful life, and as such, their incorporation into future research and development efforts is highly recommended.

AI and machine learning techniques have the potential to significantly enhance the accuracy and reliability of lifetime studies in power electronics. By leveraging vast amounts of data generated from testing and simulation, machine learning algorithms can identify complex patterns and relationships that may not be immediately apparent through traditional analysis methods. This can help to improve the accuracy of lifetime predictions, as well as enable early detection of potential failure modes.

Furthermore, the use of AI and machine learning can also enable more efficient and cost-effective testing procedures. By optimizing test protocols and identifying key parameters that influence lifetime, researchers can reduce the number of required experiments and improve the quality of results.

Overall, the integration of AI and machine learning into lifetime studies has the potential to revolutionize the field and provide valuable insights that were previously unattainable. As technology continues to advance, we can expect to see increasingly sophisticated and accurate models for predicting lifetime in power electronics.

Moreover, the demand for power modules and inverters is not limited to the renewable energy sector. The increasing popularity of electric and hybrid vehicles also drives the demand for these components. Power modules and inverters play a critical role in the performance, efficiency, and reliability of electric vehicles. They are responsible for controlling the power flow between the battery, motor, and other electrical components of the vehicle. As such, further research and development in this field are needed to ensure the reliability and safety of these components, particularly in the context of changing climate and environmental concerns.

In conclusion, as the demand for power electronics and PECS continues to grow, it is essential that we develop and refine reliable methods for evaluating the lifetime of critical components such as IGBTs. This will require ongoing research and development efforts, as well as a willingness to adapt and evolve our approaches as new technologies and methodologies emerge. By doing so, we can ensure that power electronics systems play a vital role in the transition to a cleaner, more sustainable energy future.

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