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Executive Summary of the Thesis

POWER OPTIMIZATION STRATEGIES FOR THE ELECTRONIC CONTROL OF PHOTONIC INTEGRATED CIRCUITS

Laurea Magistrale in Electronics Engineering - Ingegneria Elettronica

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1. Introduction of the thesis work

In the recent years, Silicon Photonics (SiP) has become the main solid-state optics technological platform, thanks to the possibility of realizing compact and dense photonic integrated circuits (PICs). Indeed, by using Silicon as an optical material, this technology can exploit the traditional CMOS microelectronics processes in order to reach significant levels of integration density. SiP devices are employed in the classical telecommunication C-band (around 1550 nm of wavelength), due to the transparency of silicon in the InfraRed (IR) frequency region. The primary photonic building block is the waveguide, made of a silicon core and an oxide (SiO_2) cladding, a structure that guarantees a high light confinement due to the large refractive index difference between the two materials. Starting from the waveguide, far more complex photonic devices can be implemented and integrated in the same photonic chip [1]. Large-scale SiP systems have been designed with an increasing number of photonic devices, however requiring a stabilization feedback to counteract the effect of fabrication geometrical defects and thermal variations. The optical properties of silicon are in fact greatly affected by these phenomena, determining detrimental effects on the designed behaviour of each photonic device.
A multichannel closed-loop electronic control, with local on-chip sensors and actuators, is thus required in order to tune and stabilize the functionality of integrated optical architectures [2] (Fig. 1). Several kinds of sensors have been successfully investigated in the past years to monitor the behaviour of photonic devices, whereas the actuation strategy mostly relies on the integration of resistive heaters to locally change the temperature of the photonic chip. This approach is simple and easy to implement even in other technological platforms, like Silicon Ni-

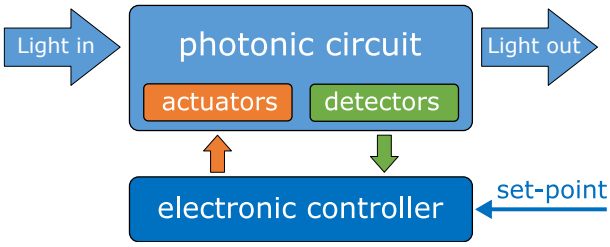

Figure 1: Schematic view of the closed-loop control scheme for photonic systems.

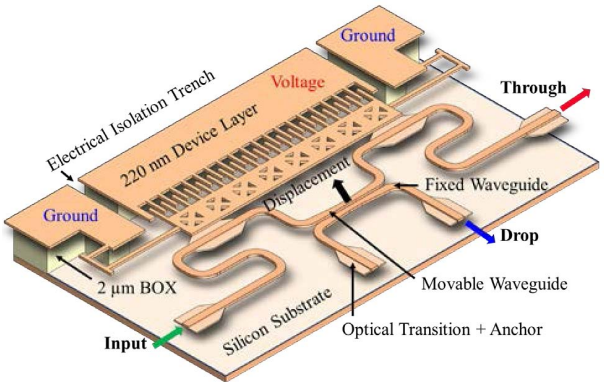

Figure 2: MEMS actuator realizing a tunable optical coupler by modifying the displacement between two waveguides [4].

tride, necessary to operate photonic circuits in different optical spectral regions [3], although being characterized by a low power efficiency. Still, this issue can be overcome with novel actuation techniques which are being investigated to optimize the power consumption of the electronic control layer: efficient MEMS devices have been realized [4], driven by an electric field applied to two electrodes, without dissipating any static power (Fig. 2). The electronic control platform should thus be able to adapt to these new kinds of devices.

2. Hardware overview of the electronic control system

A custom electronic system has been conceived to control the working point of several photonic devices. The proposed electronic board needs to extract information about the amount of optical power flowing in specified points of the PIC and properly drive the actuators, in order to perform an effective stabilization action on the optical behaviour. With the growing density of integrated components on the same chip, a multichannel control system has been designed, able to address up to 144 photonic devices. Its architecture is modular in order to facilitate the setup of the PIC on the optical bench. The photonic chip is thus placed on a small host board, where it is coupled to the optical fibers and connected via wire-bonding to a pre-amplification stage, needed to acquire the signals coming from the chip with the best resolution possible. The host board is then connected to the multichannel control board, called Helios 3, which acquires and generates all the required signals. Helios 3 is made of a motherboard and several external modules, which can be connected to it via six PCI-express connectors. The possibility of modifying the set-up of the electronic instrument by connecting different modules to the motherboard gives great flexibility to the overall system.

Fig. 3 shows the motherboard architecture. On the right side, the digital core of the system, i.e. an FPGA, is hosted, connected to the PCI-express connectors to operate the pluggable modules. The FPGA acts as the controller of all the electronic framework, by realizing the filtering and processing of the acquired information to generate the control signals needed to minimize the functionality errors of the photonic components.

Each pluggable module accepts 16 digital signals, 24 analog signals and 4 power supplies. Two modules have already been fabricated and validated:

- a 16-channels acquisition module for the read-out of the signals coming from the host-board front-end circuitry. The incoming signals are further amplified and filtered on the module, then digitized and sent to the FPGA.
- a 24-channels actuation module able to drive SiP thermo-optic actuators.

Considering the large number of signals and modules present in the system, the power supply circuit becomes a particularly critical section. In

Figure 3: Photograph of the Helios 3 motherboard.

this thesis, a specific power module needed to supply the whole platform has been designed, with particular care dedicated to optimizing its power efficiency. The module, described in Section 3, allows to supply the system using a laptop battery charger and is able to deliver up to 90W.
In addition, to further expand the capability of the platform, Section 4 describes the design of an additional actuation module, able to drive thermo-optic actuators in silicon nitride platforms and MEMS actuators, which both require different current and voltage dynamics with respect to standard SiP heaters.

3. Power supply module

The power supply module has been designed in order to generate all the voltages required by the motherboard and the external pluggable modules. To correctly estimate the maximum power budget of all the possible Helios 3 setup, a worst-case scenario has been considered by summing the power dissipation of motherboard, 80% of the maximum FPGA power requirement and the presence of 6 actuation modules, leading to an estimate of 90W. The dedicated power circuitry has thus been arranged on a specific board, which accepts a DC voltage of 19V from an external AC adapter without the use of any bulky bench-top power supply. To achieve a high power efficiency, DC/DC converters were employed to generate the reference power supply voltages, i.e. ±6.5V and ±13V, which are delivered to the motherboard and modules (Fig. 4). Local LDOs then generate the specific levels needed by the circuitry. The power module also generates a dedicated power supply (+5V) for the FPGA.
Two types of switching regulator have been employed to respectively create positive (LT3681) and negative (LTC7149) voltages, with the effective employment of 10 ICs to improve the reliability of the module by doubling the generation of each voltage (Fig. 5). A nominal switching frequency of 2 MHz has been selected in order to stay far from the frequencies employed to control the optical circuitry (0 - 100 kHz), resulting in a good compromise between device power efficiency and components size. The DC-DC converters have also been set to operate both in Continuous Current Mode (CCM) and Burst Mode operation, in order to enhance the efficiency in light load condition. The selected power inductor guarantees a ripple current $\Delta I_L < 0.6\, I_{OUT(MAX)}$ in all the operating conditions of the converters, achieving an acceptable trade-off between output ripple amplitude and component size. In order to minimize the conducted emissions and the electromagnetic interferences generated by each converter, the following choices has been done:

- the power supply has been conceived as a stand-alone module, connected via vertical connectors towards the motherboard. This allows to better shield the rest of the system. Particular care has also been dedicated to the layout of each DC/DC converter, with the purpose of minimizing the current loops created by the circuits.
- adequate filtering stages have been located at the input and at the output of each converter, in the form of π LC filters with $f_{cut} = 100\,\text{kHz}$. Ferrite beads have been used with respect to standard inductors in order to provide effective filtering action on the switching harmonics while reducing the Q-factor of the LC tank.

Protective measures have been taken in order to safeguard the system from overcurrent and input reverse polarity. Each IC presents a soft-start circuitry in order to limit the in-rush current in the inductor at the start-up, achieving a clean exponential startup transient without overshoots. In addition, resettable fuses have been connected at the output of each converter to disconnect the module when the intended load current is overcome.

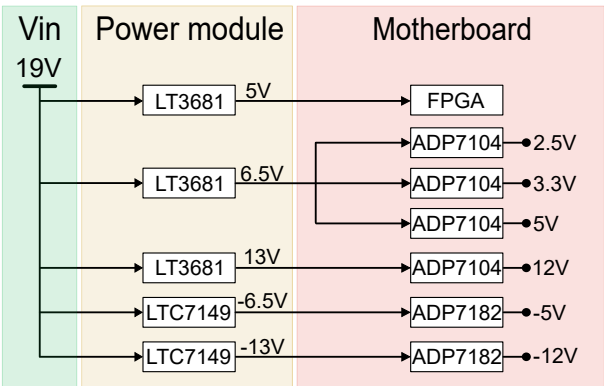

Figure 4: Diagram of the distributed power supply tree employed in Helios 3 platform, including the power module and the motherboard LDOs.

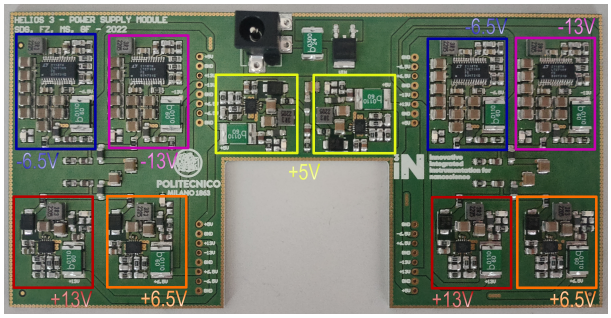

Figure 5: Photograph of the designed high-efficiency power supply module.

For the implementation of the power module, a four layer PCB has been adopted, with an horse-shoe shape in order to give room to dissipate the heat generated by the FPGA. All the circuitry has been arranged on the top layer, with copper planes all over the PCB area to ensure thermal stability of the ICs. Large traces have been designed to handle large current loads.
The module has been fabricated and validated, showing good results in terms of generated voltage levels stability. In Fig. 6, 5 mV output ripple can be appreciated at -6.5V power supply when LTC7149 is operating in Burst Mode condition, denoting a small output oscillation amplitude even in light load condition. Figure 7 shows the comparison of the DC-DC output voltage spectral density when operating in the two working conditions. The CCM switching harmonics are correctly attenuated by the output filter, resulting in much smaller switching noise. Similar results have been obtained for the other converters. The measurement thus certificates that the use of DC/DC converters to supply Helios 3 has no harmful effect on the performance and resolution of the system, and demonstrates the correct design of the overall power supply.

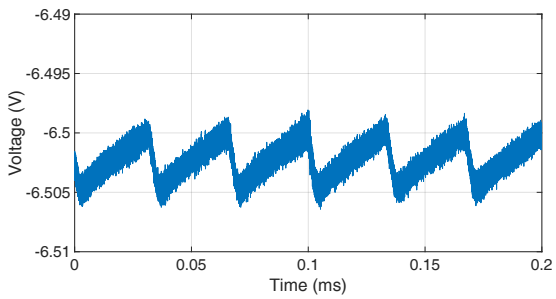

Figure 6: Output ripple of the -6.5V DC/DC converter, operating in Burst Mode Condition.

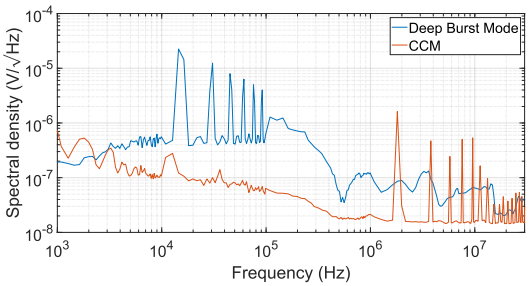

Figure 7: Frequency spectrum of the -6.5V DC/DC converter, in Burst Mode Condition (blue) and Continuous Current Mode (orange).

4. High Power - High Voltage actuation module

After the discussion on the Helios 3 platform and its power supply module, an actuation module able to drive both SiN heaters, which require an important current capability (High Power), and MEMS actuators, which are driven with an extended voltage range (High Voltage), is presented. This module adds another important functionality to the overall electronic framework, thanks to the increase not only of the number of actuators that Helios 3 can drive, but also of the type. It is important to highlight that the necessity of driving MEMS devices, which may require voltages up to 30V, was not considered at the beginning of the Helios 3 project, therefore specific design choices were required.
The module was designed in order to correctly handle high voltages, so an important aspect of the realization was the re-conception of the power supply needed to drive the novel actuators. A step-up DC/DC converter has thus been employed to generate a stable power supply of +24V or +36V starting from the +13V provided from the PCIe connector: the two power supply levels have been chosen taking into account the different dynamic range of the two types of actuators. In addition, to drive the SiN heaters, an output current of 50mA is required. Since the whole module is powered by a single power supply +13V, the number of parallel actuation channels has been lowered from 24 to 16. The design phase of the DC/DC power circuitry has followed the same steps of the converters employed in the power supply module, with the predefined 2 MHz switching frequency.
The final actuation chain is shown in Fig. 8.

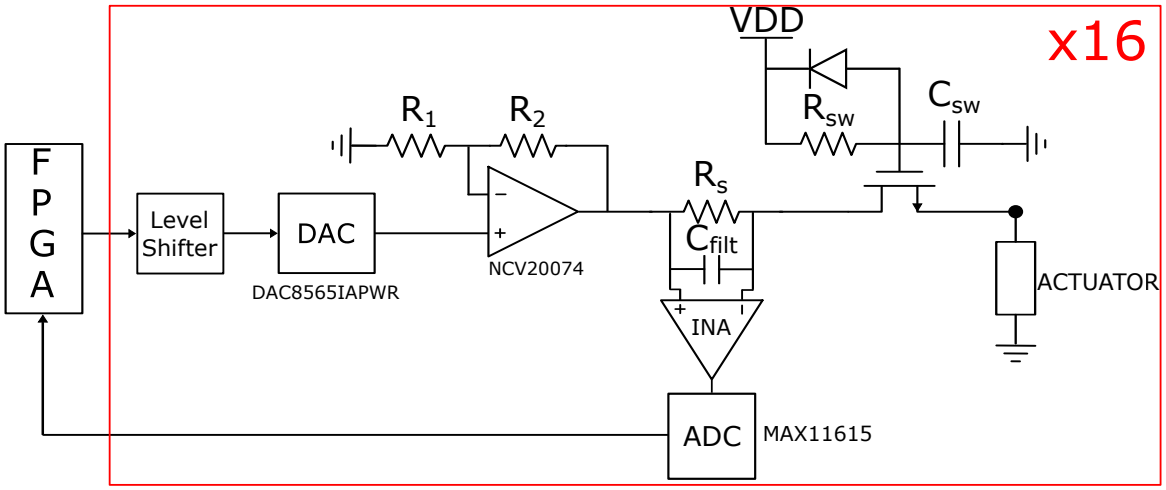

Figure 8: Schematic view of the High Power - High Voltage actuation chain.

The actuation signals are generated by a 16-bit 4-channel DAC (DAC8565, Texas Instruments), able to reach a required accuracy of 1 mV. Its high update frequency (520 kbps) per each channel is reached by translating to +5V the voltage levels of digital signals coming from the FPGA, allowing the generation of modulated signals up to 50 kHz with good spectral purity. A driver stage is then needed to simultaneously extend the DAC voltage range to the 30V MEMS voltage dynamics while providing enough output current for heaters: the selected 4-channels Op Amp (NCV20074, On Semi) ensures a bandwidth of 250 kHz with a gain of 12 and it is able to deliver up to 65 mA. To drive all the 16 channels, 4 DACs and 4 drivers have been used in the module. A real-time current monitoring circuit has also been placed at the output of the drivers, so that any actuator failures can be detected. The average actuation current is sensed by a shunt resistor R_s placed in series to the actuation node, amplified by a custom INstrumentantion Amplifier (INA) and correctly acquired by an ADC. Two 8-channels ADCs (MAX11615, Maxim Integrated) have been adopted: they features a 12-bit accuracy with a sampling rate for each channel (11,6 kbps), enough to monitor the average value of the actuation current. Lastly, a protection device between the actuators and the driver output is required to safeguard the actuators during system startup/switch-off. A low on resistance analog switch (MAX4602, Maxim Integrated) has been selected and its activation/deactivation is handled by an RC network. The layout of the module has been carried out with 4-layer PCB, with a dedicated area to implement the power circuitry. The VHDL firmware required to operate the module has been completed, handling the communication between DACs/ADCs and FPGA. The characterization of the signal generation circuit has been performed. Fig. 9 shows square modulated signals around 10 kHz with a DC level close to 30V, generated when a supply voltage of 36V is selected. It is possible to see that the driver is able to correctly generate these signals, with sharp transitions even at high amplitudes, and that up to 30V are correctly provided to the MEMS actuators. In order to validate also the actuation of SiN heaters, the actuation chain has been powered up by +24V power supply and a low resistive load has been connected to the output. The capability of the circuit to provide high currents, detected with the monitoring circuit, has been verified. The INA output has thus been acquired with the ADC, transmitted to the FPGA and shown in the graphical user interface on a personal computer. The user interface has been programmed to convert the ADC input voltage into the actuators current level, conveniently displayed in a real-time graph. In Fig. 10, the sensed current is portrayed when a sinusoidal waveform at 800 Hz with a 10V DC bias and 1V amplitude is used to drive a 480 Ω load. The measurement confirms that the driver successfully drives the actuator, the ADC correctly measures and converts the INA output, and that the communication between the module and the FPGA is successful, thus validating the overall circuit operation.

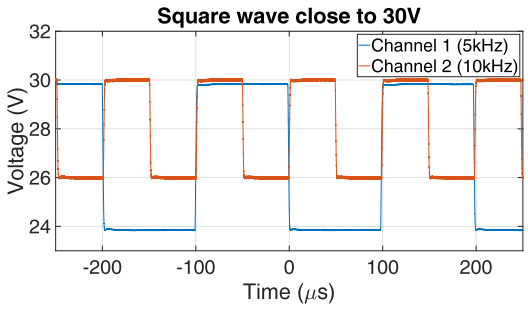

Figure 9: Square wave modulation of two channels close to 30V (maximum positive voltage).

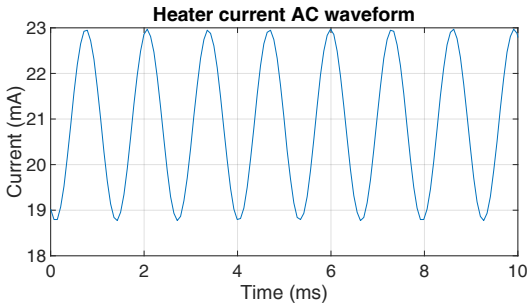

Figure 10: Actuation current detected with the monitoring circuit when an AC waveform is applied to a resistive heater.

5. Conclusions

The aim of this thesis was to complete the design of an electronic system able to control large-scale photonic integrated circuits. The multichannel modular board Helios 3, able to handle up to 144 optical devices and fully reconfigurable in order to adapt to any experimental need, has thus been completed, by designing its missing parts. The electronic board required power optimization strategies to enhance the efficiency of the whole system. For this purpose, a power supply module has been fabricated and fully characterized, with the employment of DC/DC converters to efficiently generate stable and reliable power supplies without impacting the performance of the electronic control. An external pluggable module, required to drive heaters in SiN technology and power efficient MEMS actuators, has then been realized in order to improve the flexibility of the system to different types of actuators. This second module has also been completely validated, including the VHDL firmare required to operate it with an FPGA. The overall electronic system (Fig. 11) is now fully electrically validated and ready to be authenticated in scientific experiments of closed-loop photonic control, enabling robust and reliable tuning and stabilization of large-scale photonic systems.

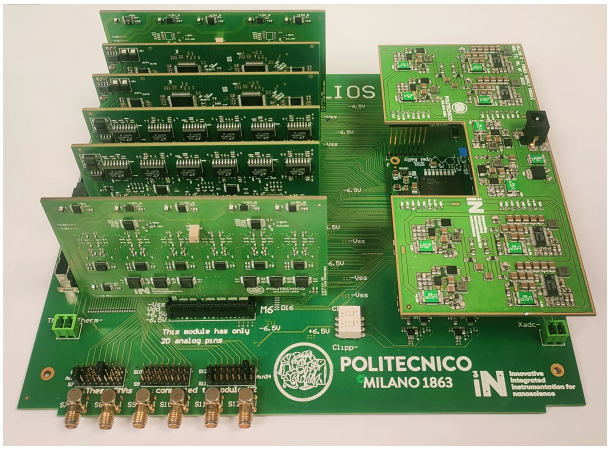

Figure 11: Photograph of the Helios 3 electronic system.

References

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