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EXECUTIVE SUMMARY OF THE THESIS

Development of a high parallelism ATE test solution for the next generation of GPS processors

TESI MAGISTRALE IN ELECTRONICS ENGINEERING – INGEGNERIA ELETTRONICA

AUTHOR: CARLOTTA MARIALUISA GUIDI

ADVISOR: MARCO SAMPIETRO

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1 Introduction

The aim of this thesis is to illustrate the final test applied on a new GPS device of STMicroelectronics, Teseo V, using an ATE composed by a new tester, V93000 Exa Scale. A GPS converts the received modulated RF signal to modulated intermediate frequencies (IF). To test all its circuit blocks the necessary equipment is tester, board, sockets, and software. Their features are needed to satisfy the mass production requirement. The tester applies a defined waveform and elaborates the signals received from the DUT in accordance with the test program. I focus my attention on RF block tests such as LNA, PLL and VCO, AGC, VGA, Filters and their gain compression. Tests are studied to exploit the potential of V93000 to obtain the best test time, precise and reliable measurements and the high capability to test in parallel eight device.

2 Test and Product Engineering

In the last years, many changes have occurred in the semiconductor industry, which are mostly related to the diffusion of complex semiconductor devices. The integration of these circuits has created many new business opportunities, but at the same time it has made the test process much more challenging. To this aim it is necessary to adopt high quality and efficient methods for testing and evaluating device performance. The result of test process over the mass production must be analyzed by using statistical methods to avoid releasing defective products and to have better understating of overall design and test process performance. Test engineer's goal is to monitor results of each production step and establishes control criteria to ensure that final products meet the quality according to the customer expectations and matching production test time requirement.
Two types of test processes are performed:
- Electrical Wafer Sort (EWS): tests wafers before assembly, included in Front-End.

- Final test (FT): test on chip after packaging, included in Back-End [1].

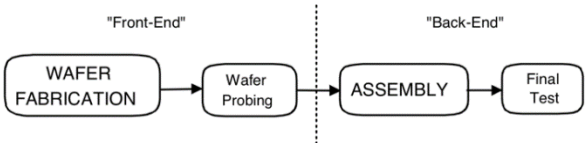

Figure 2-1 Manufacturing Flow Chart of an Integrated Circuit [2]

2.1 Final test

The final test process ensures that the performance of the device doesn't change due to mechanical stress that happens during packaging process. Devices that pass the final test can be shipped to customers since they satisfy design requirements and customer specifications.

2.2 ATE

The equipment necessary to perform the final test is composed by specific hardware and software known as automated test equipment (ATE), the load board and test sockets are used to interface ATE to device under test (DUT). The instructions to be sent to DUT are defined in the test program based on the device behaviour that we want to verify. The results for each device are recorded in a file of a specific format, relative database, data log and standard test data format (STDF), which can be used to execute subsequent analysis.

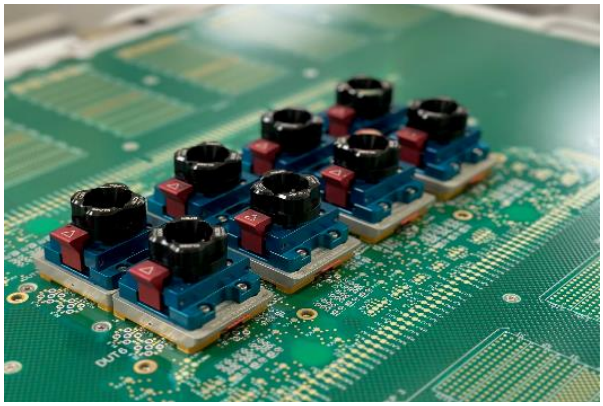

Figure 2-2 Board and sockets with manual actuators on V93000.

3 GPS device

GPS (Global Positioning System) is one of the most applicative devices that receives radio frequency waves in different bands, as shown in figure below. A GPS is a part of the Global Navigation Satellite System (GNSS), which refers to a constellation of satellites providing signals from space.

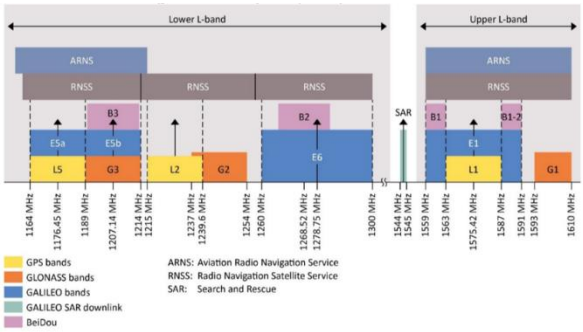

Figure 3-1 GNSS systems, upper L bands and lower L bands [3]

GPS can be modelled as a typical wireless communication system, in which data signal is processed, filtered, amplified, and modulated or demodulated. In a GPS receiver the signal entering in the RF blocks is amplified, down-converted, and filtered, then converted to a digital signal. The main working blocks are Low Noise Amplifier (LNA), Mixer, Phase lock Loop and VCO, IF gain amplifier with AGC, IF Filter, oscillator and demodulator.

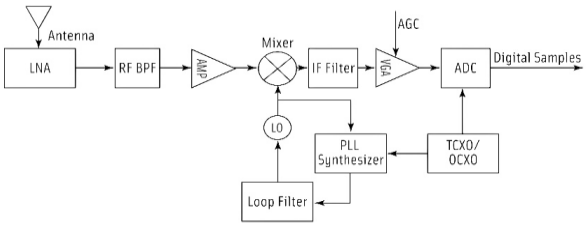

Figure 3-2 General block diagram of a GPS device [4]

3.1 LNA

The RF signal coming from the antenna has low amplitude, therefore it must be amplified by a LNA (Low Noise Amplifier). Ideally the amplification is assumed to be linear, but due to design factors, there are non-linearity effects which

lead to Gain Compression. Considering an input x(t), the LNA output can be represented as

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots$$

[3. 1]

To understand the distortion effect, define $x(t) = A\cos(wt)$ as input. Therefore, by using a **narrow band pass filter** around the fundamental frequency after LNA, the gain is mostly determined by first harmonic of the output, while other harmonics are removed. The equation [3. 2] given below shows LNA gain result.

$$Gain = \frac{output\ (fund\ freq)}{input\ (A)} = \frac{a_1 A + \frac{3a_3 A^3}{4}}{A} = a_1 + \frac{3a_3 A^2}{4}$$

[3. 2]

assuming that α_1 and α_3 are positive and negative respectively, the output power decreases with the increase of A. The input compression point A_{-1dB} is defined as the point in which the difference between linear and non-linear output in fundamental frequency is 1dB [5].

$$20\log|a_1 A_{-1dB}| - 20\log\left|a_1 A_{-1dB} + \frac{3}{4}a_3 A_{-1dB}^2\right| = 1dB$$

[3. 3]

3.2 Mixer

Mixer can down-converts the RF signal to the desired IF signal using a local oscillator (LO). Its output has two main components: "ω_{RF}-ω_{LO}" and "ω_{RF}+ω_{LO}", a band pass filter is used to remove the undesire one. ω_{LO} is the LO frequency and it can be chosen in order to move the signal at the target frequency [6].

3.3 VCO and PLL

VCO (Voltage Controlled Oscillators) can tune their oscillation frequency range from ω_1 to ω_2 through a control voltage V_{cont}.
The PLL is circuit block which can obtain a constant synchronization in time and compensate any change in frequency of the reference signal. PLL is composed by a VCO, an LPF, which removes any high frequency elements from the signal, and a phase detector (PD) which form a negative feedback loop.
The VCO produces a signal which enters the phase detector. Here the phase of the signals from the VCO and the incoming reference signal are compared and an error voltage, corresponding to phase difference between the two signals, is produced. The PLL loop is said "locked" if $\Phi_{out}(t)$ tracks $\Phi_{in}(t)$, which means that $\Phi_{out}(t) - \Phi_{in}(t) = costant\ value$ [6].

3.4 AGC

AGC (Automatic Gain Control) is a closed loop control system implemented to continuously adjust the receiver's gain to optimally fit the ADC input dynamic range. Its task is maintaining a relative constant output signal while the input signal is varying in amplitude over time [7].

3.5 Linear Voltage Regulator

Voltage linear regulator is widely used to allow electronic circuit power supply to operate at constant voltage despite any change occurring at regulator input voltage or in load current.

4 Test Program and Hardware Required

4.1 Tester - ADVANTEST V93000 EXA Scale

This test system can be used on a wide range of devices, offering great performance while maintaining low costs of test. Its innovative technology includes highly integrated RF, mixed signal card and it incorporates per-pin testing capabilities ensuring maximum efficiency for multisite applications. For Teseo V the tester in used is V93000-CX model, in which 1 card cage and 9 slots are used [8].

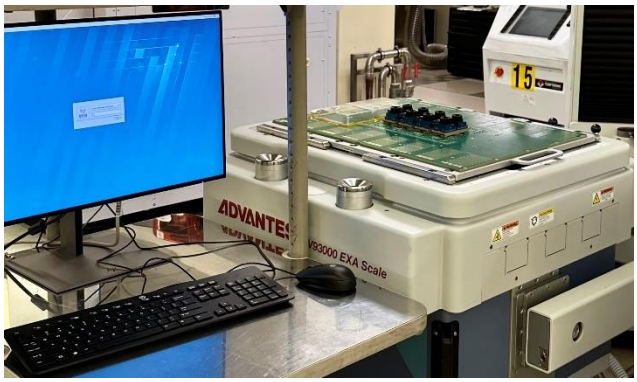

Figure 4-1 ATE in STMicroelectronics clean room in Agrate.

4.2 Test Board and Sockets

The board consists in 8 sites in which 8 devices can be test in parallel. It acts as interface between tester and DUT (device under test) through the sockets. Inside the socket some spring probes are installed, they connect the DUT balls and board pogo pads.

4.3 Software

Smart test 8.5 is a software designed based on the Java program using eclipse interface to run test programs dedicated to tester V93000. The test program structure is of hierarchical type and test program file must contain several files (i.e. DUT board description).

5 Test Program Structure-Details and Resulting Graph

The developed test program first evaluates the device in terms of DC characteristics, and then tests the performance of RF blocks and functionality of the memory.

5.1 RF block test

RF block consists of LNA, RFA, programmable chains, PLL and filters which should be able to provide a proper functionality.

5.1.1 LNA test:

The test method evaluates LNA performance in terms of S-parameters, gain and compression point for above different GPS bands.

5.1.2 Mixer

Once a signal with frequency in the range between 1 to 2 GHz is received, the mixer down converts it to an IF of 4 MHz or 91 KHz depending on the selected band. The operative range of intermediate frequencies depends on user's application, and it can be selected by SPI commands. During the evaluation it is verified if the output signal can be found at the expected frequency and if the mixer does not attenuate its amplitude.

5.1.3 PLL test

in TeseoV a fractional PLL is used. In this test the input reference frequency is set at a certain value, and SPI prepares the relative setup. Once the setup is prepared the test method must verify the output frequency on pins GPIO24, GPIO25 and PLL lock state on pin GPIO94. If PLL is locked, GPIO94 generates a logic one.

5.1.4 VCO test:

In the developed test method, we apply a reference frequency at 18 MHz, 19 MHz, and 21 MHz. Once PLL is locked VCO divided output must generate a tone at frequency of 33 MHz as shown in the figure below.

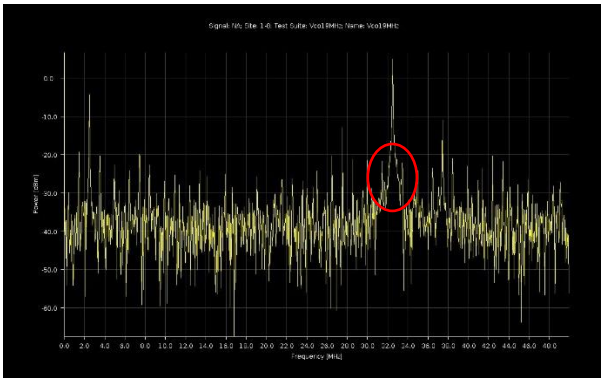

Figure 5-1 VCO power in frequency.

5.1.5 RFA test:

RFA test includes evaluation of three programmable chains in terms of gain. AGC, VGA, compression point, filtering response and capability of 90-degree phase shift are evaluated. These chains are G2, GC, and Lband that can be selected by using a dedicated address through SPI. The difference is the range of frequency of input that they can manage.

5.1.6 AGC test

AGC block should show two separate knees at the beginning and end of its input-output characteristics with a flat zone in between. The test starts changing the input power from -75 dBm to -10 dBm. During this input power sweep we measure the output power and plot the graph of

input-output characteristics for all eight sites of the board.

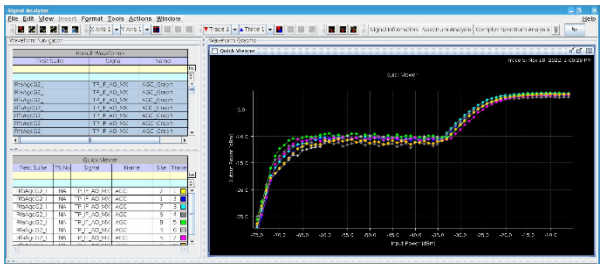

Figure 5-2 AGC graph of G2 chain.

5.1.7 VGA test

The test selects the different VGA gains through SPI and measures the output power in dBm. The difference between output and input power results in the gain value thus it must be calculated for all possible gain selections.

5.1.8 Gain compression test

The test varies the input of LNA from a minimum to maximum value. In order to find the compression point, every sampled output power in dBm and its adjacent are compared: if their difference are below 1 dB the compression point is reached.

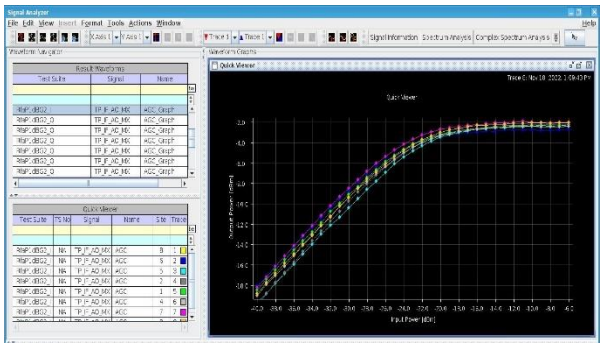

Figure 5-3 Compression point search.

5.1.9 Filters test

When mixer translated the input into IF bands, the next step is to remove interferences and noise through an LPF. To evaluate filter response, at the beginning of the test method SPI selects chain G2, which can manage signals with maximum IF frequency of 13 MHz. The signals with frequency greater than 13 MHz are attenuated. To construct the filter response, frequency of the input signal discretely varies from 100 KHz to 30 MHz.

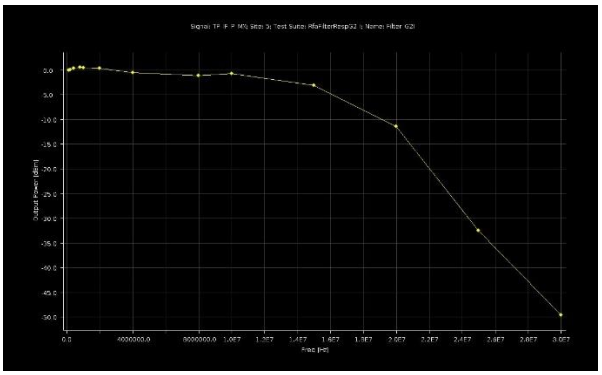

Figure 5-4 Frequency response of G2 chain filter.

6 Analysis of the Results

After test program development completion on the new platform, its reliability, stability and test time must be evaluated. In the following section tester-to-tester correlation, hardware performance of new tester, and test time are discussed to highlight the excellent results achieved.

6.1 Results Comparison tester-to-tester

This analysis is based on 8000 units tested on both starting and new platforms. V93K works much more efficiently in terms of CPK and standard deviation.

At the beginning of the activity, it was noticed that the starting platform encountered a considerable loss on RF path so specific focus have been put on V93K board design to improve this aspect. The gain result for chain G2 and LNA test on V93K shows good performance and results are very well aligned with expected datasheet value.

Also, LPF filters response represent a critical device parameter for Teseo5. As showed in Figure 6-1, V93000 filter response follows the ideal trend with flat amplitude of 0 dB (blue line) respect to the starting platform.

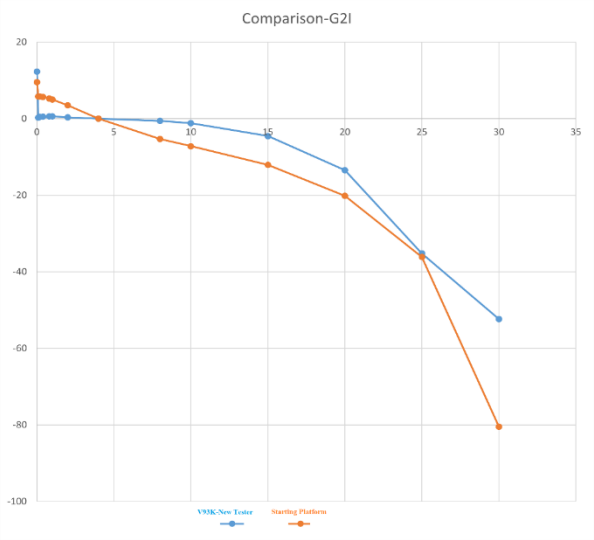

Figure 6-1 Filter Bode diagram of G2-I chain.

6.2 Reliability of V93K

Several trials are performed to ensure test reliability:

- in the site-to-site correlation we verify if the results of all eight sites are close to each other.
- the loop trial (endurance test) consists in a loop of one and half an hour of the test program on eight good devices. This test verify the loop stability and it is successful if the yield result is greater than 95 %.
- Spike analysis is performed to find voltage spikes that can cause possible damage to the device. In practice, the oscilloscope probe is placed on the board pogo pins and the shape of the signal is observed during test program execution.

6.3 Test Time

Test Time is one of the most important parameters, because its reduction increases the DUT evaluation rate. During the test time comparison, V93K showed an overall test time of 18 seconds compared with 25 seconds of the starting platform. The most important reasons are the ability to control slew rate of instruments providing voltage or current ramp, the possibility of parallel measurement, and the compiler performance. The table Table 1 shows test time for each test block of the developed test program.

Testflow/Test suite name	Avg test time [ms]
Flow PreRun	11.544
Flow Main	17324.172
Flow Main.ContinuityPre	184.544
Flow Main.LeakagePre	225.707
Flow Main.Otp	602.831
Flow Main.Parametric	2319.63
Flow Main.Functional	9074.423
Flow Main.Rf	3453.8
Flow Main.Bist	796.506
Flow Main.ContinuityPost	437.935
Flow Main.LeakagePost	228.482
Test time	17344.673

Table 1 Time of all Testflow.

7 Conclusion

Some ST important automotive customers have already received and validated inside their application samples tested on V93K Exa Scale. The analysis demonstrates that V93K is fully compliant to mass production requirements in terms of test time and parallelism efficiency.

The activity discussed on this thesis represents, not only an important improvement for ST supply chain on a top runner device, but also helped to identify the future testing platform for ST next generation RF and digital products.

I want to highlight that this thesis is not only research and evaluation work, in fact ST offered me the possibility to have an effective training on the job: I learned how to implement and validate tests for functionality and performance evaluation of a complex System on Chip (SoC) and the use of laboratory instrumentation as spectrum analyzer and oscilloscope.

8 Bibliography

[1] R. Gordon , F. Taenzler and M. Burns, An Introduction to Mixed-Signal IC Test and Measuremen, 2011.

[2] "University Wafer," [Online]. Available: https://www.universitywafer.com/semiconductor-technology.html.

[3] Infineon, "BGA123L4 as Low Current Low Noise Amplifier".

[4] A. Joseph, "Measuring GNSS Signal Stregth".*GNSS solutions.*

[5] S. Sarkar, A. Sarrafinazhad and A. Ghoncheh, "Rahsoft," [Online]. Available: https://rahsoft.com/2021/04/25/drawbacks-of-non-linear-system-gain-compression/.

[6] B. Razavi, RF microelectronics (2nd).

[7] I. Rosu, "Automatic Gain Control (AGC) in Receivers," [Online]. Available: https://www.qsl.net/va3iul/Files/Automatic_Gain_Control.pdf.

[8] "Advantest," [Online]. Available: https://www.advantest.com/.