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Executive Summary of the Thesis

Microfabrication and Electrical Characterization of CMOS Compatible Foldable Electrodes for Dopamine Sensing in Brain

Laurea Magistrale in - Materials Engineering and Nanotechnology -
- Ingegneria dei Materiali e delle Nanotecnologie -

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Introduction

Brain is one the most fascinating and unknown systems in biology, a wide variety of signals are transmitted within the neural network, contributing to: sensory perception, motion, cognition, and emotions [20]. The possibility of directly sensing and stimulating these signals, thanks to brain computer interfaces (BCI), can not only significantly improve our understanding on the system but it also offer the opportunity to treat various clinical disorders [21]. Among the many applications, electrochemical detection of neurotransmitters is of great interest, due to their role as regulators in synaptic communications and brain functions. A notable example is dopamine, whose dysregulation is associated to debilitating conditions such as Parkinson's disease [17] and schizophrenia [16]. This thesis work aims to develop CMOS compatible foldable microelectrodes for intracortical dopamine detection. In particular, these devices comprise a central 500×500 μm^2 Si chip, to accommodate CMOS based circuitry, and two shanks, on which the electrode active sites are positioned. These can then be folded by 90° to allow penetration into the brain tissue. This innovative design has been initially presented into the the context of the Smart Micro Neural Dot project; which aims to revert blindness thanks to the generation of phosphenes, exploiting an array of floating wireless powered electrodes implanted into the brain [3–5]. In order to accommodate multiple independent channels on the shanks, substantial modifications and optimizations of the fabrication process have been developed and implemented. Moreover, electrical characterization and preliminary electrochemical measurements have been performed, to asses the correct functioning of the electrodes.

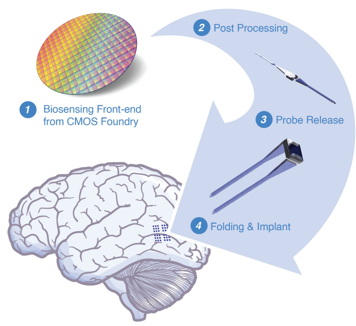

Figure 1: Concept behind CMOS compatible foldable electrodes.

1. Foldable Electrodes Microfabrication

Fabrication of the electrodes is performed by clean-room level techniques and has been conducted at the Center of Micro Nano Technology (CMi) of the Ecole Polytechnique Fédérale de Lausanne (EPFL). The process can be divided into three macro-areas: front-side fabrication, back-side fabrication and probe release.

1.1. Front-side Fabrication

Si/100mm/DSP/1-10/TTV2 wafer has been chosen as substrate, among the ready-to-use ones present in CMi, mainly for its small thickness, so as to reduce Si waste in subsequent steps. 200 nm of SiO_2 has been grown on the wafer surface for insulation purposes. On top of it 4 μm of Al has been deposited by sputtering, exploiting 10 nm of Ti as adhesion layer. Sputtering was performed in *Spider 600 (Pfeiffer Vacuum, Germany)* which has been chosen due to its high deposition rate of 198.0 $\frac{nm}{min}$ [10]. This layer constitutes the foldable, 1656 μm long, shanks of the probe, so Al was chosen due to its mechanical properties, since it allows 90° folding, without bending or buckling during insertion into brain tissue, as proven by previous studies on the device [22]. In order to pattern the layer, direct laser writing photolithography has been used, in which a photosensitive polymer is deposited on the wafer surface and selectively exposed to laser in UV range (405 nm) [8]. For the photoresists (PR) used the expected critical dimension (CD) is 1 μm [7]. To etch Al, dry plasma etching has been used based on Cl_2 chemistry on *PlasmaPro100 Cobra (Oxford Instruments, United Kingdom)*, the technique was preferred with respect to wet etching ones due to the steep walls that can be obtain and the absence of underetch [12]. To insulate the shanks from the electrical layer, yet to be deposited, a uniform 1 μm thick SiO_2 layer was used, obtained by Plasma Enhanced Chemical Vapor Deposition (PECVD) on *D250L PECVD (Corial, France)* [14]. The material chosen for the active sites of the electrodes was Pt, due to its biocompatibility and the well known ability in performing electrochemical sensing of dopamine, without further surface functionalization [25]. 200 nm of platinum were deposited by sputtering in *Spider 600*, once again using 10 nm of Ti as adhesive layer, and patterned by purely physical ion beam etching (IBE) in *Nexus IBE350 (Veeco, USA)*. Physical etching has to be used due to inertness of Pt to most chemical etchant, however thermal reflow of the photoresist had to be perform to avoid Pt redeposition on the steep walls of the polymer [11]. Finally full front-side insulation has been obtained by depositing 1 μm of SiO_2 by PECVD, then, to expose Pt electrodes and pad for testing, the oxide has been etched by C_4F_8 based plasma etching on *APS (STPS Technologies, United Kingdom)* [13].

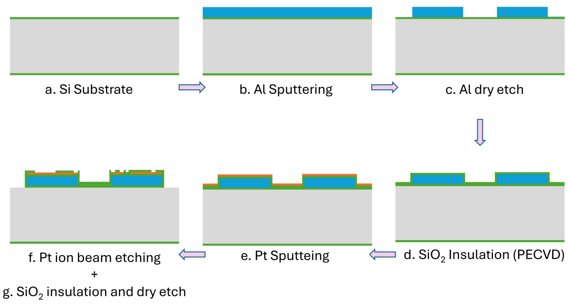

Figure 2: Main steps in front-side fabrication.

Different designs have been explored in the electrodes realization, each with a specific scope. As a general rule, to perform electrochemistry measures in a stable and repeatable way a minimum of three electrodes is required: a working electrode (WE), on which the reaction occurs, a counter electrode (CE), that feeds the current to the working one, and a reference electrode (RE) to set a known value of potential, for accurate measurements [6]. The "standard" design that has been proposed comprises a 2000 μm^2 square WE and an analogous RE on one shank, while CE is on the other shank and it's 10 times larger then the other two, so to avoid saturation phenomena. The other proposed designs are variations of such "standard":

- Multiple electrode design, to explore the possibility of multi-sensing, that would increase accuracy by combining multiple signals [1];
- Small circular electrodes design, 400 μm^2, to verify scalability of the process, considering that smaller electrodes could be placed closer to the shanks tip, achieving sensing deeper into the cortex;
- Large $20'000$ μm^2 WE, in order to facilitate electrodes functionalization by drop casting tests.

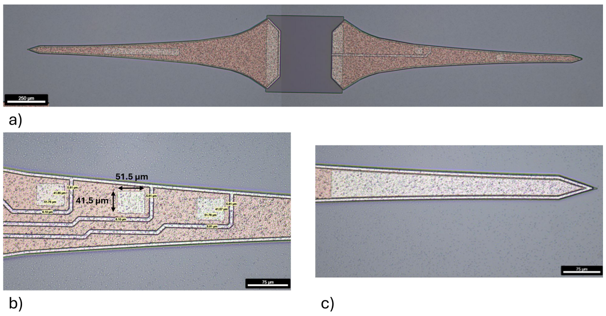

Figure 3: a) Standard electrode design overview. b) WEs present on the multiple electrodes design. c) Large WE optimized for functionalization.

1.2. Back-side Fabrication

Backside processing started with wafer grinding to reduce its thickness, in order to facilitate subsequent deep reactive ion etching (DRIE) steps. First of all, features on the front-side has been protected by covering them with a non-photosensitive resists, then wafer thickness has been reduced from 380 μm to 230 μm by mechanical grinding, performed on *DAG810 (Disco Corporation, Japan)*. Then, to release internal stresses induced by the process, additional 10 μm have been etched by *Rapier (STPS Technologies, United Kingdom)* exploiting SF_6 chemistry [15]. 1 μm of SiO_2 is then deposited on wafer backside, to act as hard mask in DRIE. Before proceeding further parylene has been deposited to act both as thermal resistant front-side protection layer and as sacrificial layer for final probe release. In order to improve its adhesion with substrate silanization has been also performed. Two DRIE have been then performed, the first, exploiting photolithography, aimed to the definition of a 35 μm step. While the second allows Si removal in the regions in proximity of the shanks. Hard SiO_2 mask avoided general wafer thinning, that would have most likely caused critical failure due to substrate embrittlement. On the other hand, the step previously etched defines the central Si chip, on which CMOS circuit will be embedded, and the structural supports of the shanks, that increase their rigidity and avoid undesired bending. For a successful fabrication of the device, it was crucial to asses alignment between front-side features and backside ones, so before Si etching, IR transmission microscopy, on *DM8000 (Leica Microsystems, Germany)*, has been exploited to do so. Finally 500 nm of SiO_2 have been deposited by ambient temperature sputtering in *Spider 600*, since process temperatures of PECVD previously used were not compatible with parylene [23].

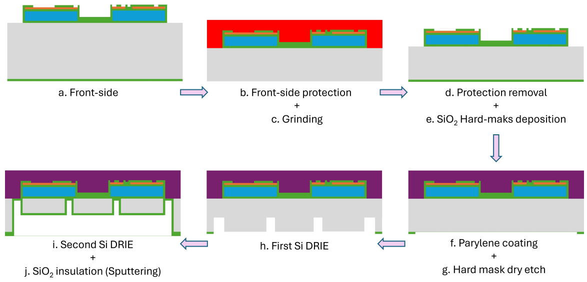

Figure 4: Mains steps of back-side fabrication

1.3. Probe Release

After having completed both front-side and back-side fabrications, the probes could be considered as suspended on the processing wafer by 5 μm of parylene and 500 nm of SiO_2, so etching of both materials was required to release them. In order to obtain safe and controlled release of the devices, a carrier wafer was produced, consisting of a Si wafer, on which 100 μm deep sockets have been etched. Processing and carrier wafers are aligned and binded together by *Quick stick 135*, a wax used for temporary connections between silicon components. Then the two etchings have been performed on *PlasmaPro100 Cobra*, exploiting O_2 and CF_4 plasma dry etching in succession. The great majority of the probes has been successfully released and has fallen into its corresponding socket. In order to perform shanks folding, a guide and a lever have been printed by *Photonic Professional GT+ (Nanoscribe, Germany)*, a 3D printer with a resolution up to few hundred of μm [9]. The lever has been used to gently push each probe along the printed guide, imposing to the shanks an initial folding angle of 45° and then setting the final 90° one, as desired.

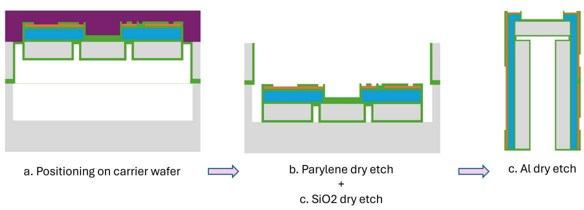

Figure 5: Probe release and final bending.

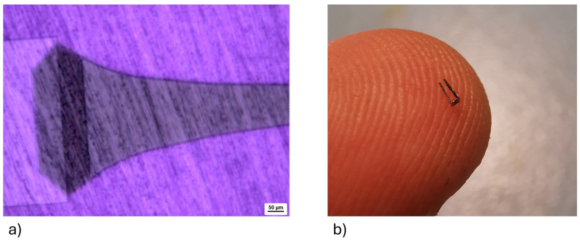

Figure 6: a) Front-side features (black shank) and backside ones (white square and shank support) alignment, IR transmission microscopy. b) Final release and folded electrodes, compared with human finger.

2. Electrical Testing

In order to asses insulation offered by SiO_2 and to demonstrate full independence between three electrodes present on each sample, electrical characterization of *Pt* tracks has been performed. In particular *Multi-Frequency Impedance Analyzer (MFIA) (Zürich Instruments, Switzerland)* installed on *TS150 (MPI Corporation, Taiwan)* probe station, was used to determine impedance value between different electrodes in a wide range of frequencies: from 1 Hz to 100 kHz. The impedance measured at low frequencies, between WE-CE, RE-CE, WE-RE, was of about 10^8 Ω and constant, showing a resistive-dominated behavior. Then, at about 3 kHz, capacitive behavior became relevant, causing a linear decrease of the impedance magnitude. Moreover, at bout the same frequency, the impedance phase shifted to $-90°$, confirming this hypothesis. Such behaviour is in agreement with a resistor in parallel with a capacitor [2], a model that, in first order, well describes the tested devices. Finally, to have some relative reference values and definitively asses independence between different *Pt* electrodes, it has been decided to measure the internal impedance of platinum tracks. In addition, also the one in open circuit condition has been evaluated, keeping the needles of the probe station terminals at a comparable distance with respect to the one used for previous measurements. A comparison between these curves can be seen in fig. 7. Impedance measured between insulated electrodes is, at low frequencies, in the same order of magnitude as the one measured in open circuit condition, being, at the same, time 7 order of times larger then the one measured in the platinum tracks. This not only assess the full independence of the three electrodes, but also a good internal conductivity of each one of them.

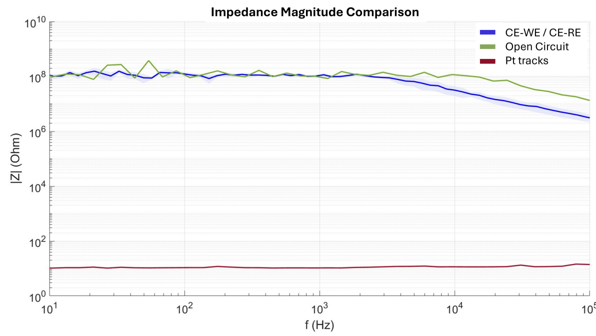

Figure 7: Impedance magnitude comparison between insulated electrodes, open circuit condition and *Pt* tracks

3. Electrochemical Impedance Spectroscopy

A common method used to electrochemically characterize electrodes is the electrochemical impedance spectroscopy (EIS), in which a sinusoidal voltage is imposed, sweeping its frequency over a certain range and measuring the overall impedance. Which is given by contributions of solution, electrodes and double layer capacitances related to the electrode-solution interface [6]. Such value it's also highly dependent on surface topology of the electrode. In order to perform these measurements on the electrodes, it has been decided to produce chips, each containing a single device on it. So the same procedure seen before has been followed until completion of the front-side fabrication. Them the wafer has been mechanically diced into small chips by *DAD321 (Disco Corporation, Japan)*.

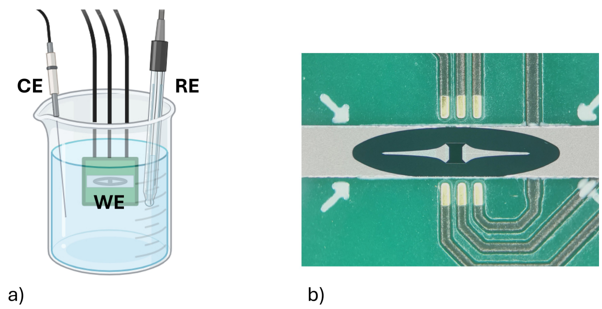

Figure 8: a) Setup used to perform EIS. b) Chip placed in the dedicated space of the custom PCB.

These chips have been placed and bound to custom made printed circuit boards (PCB) thanks to *H70E (Epoxy Technology, USA)*, a non-conductive thermosetting epoxy. PCB pads and device testing pads have been connected through *Au* wires (⌀25 μm) exploiting *5630i (F&S Bondtec, Austria)* wire bonder. Electrical insulation of wires, pads and exposed *Al* due to dicing process has been performed by *H70E-2 (Epoxy Technology, USA)* a non-conductive epoxy, completely analogous to the one previously used, except for its characteristic glob top topology at the application, that facilitates component encapsulation within it. The system obtained then has been partially submerged in phosphate buffered saline solution, so that the device was fully immersed, while the PCB connectors were not in contact with the liquid. The device has been connected to *Autolab PGSTAT302N (Metrohm, Switzerland)*, a high current potentiostat/galvanostat with a bandwidth of 1 MHz [19]. Each electrode of the probe was tested one by one, acting as working electrode, while a long *Pt* wire has been use as counter and a standard *Ag/AgCl* RE as reference. A sinusoidal voltage, with $V_{RMS} = 10\,mV$, has been applied, sweeping its oscillation frequency from 0.1 Hz to 100 kHz, measuring 10 points per decade. Impedance measurements were then compared with values reported in literature for *Pt* electrodes of similar sizes in the same solution [24].

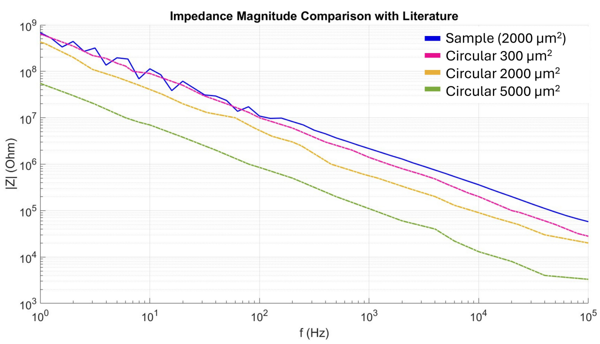

Figure 9: Fabricated 2000 μm^2 electrodes EIS in PBS, compared with EIS reported in literature for *Pt* electrodes of different sizes.

Although quantitative comparison can not be safely performed due to the different setups used, it can still be observed that the range of magnitude of the impedance is coherent with respect to what declared in literature. Other two important considerations can be made. First of all, as expected, the larger $20'000\ \mu m^2$ electrodes had a lower impedance with respect to the 2000 μm^2 ones. Finally the observed behavior is coherent with what has been found in literature, with an almost linear decrement in the impedance magnitude.

Conclusions

This thesis has demonstrated the feasibility into the fabrication of CMOS compatible microelectrodes for electrochemical sensing of dopamine. It has shown step by step the process required into obtaining such electrodes, starting from the substrate up to the final probe release. It has shown the versatility of the innovative foldable electrodes design, initially developed for the Smart Micro Neural Dot project, opening to the possibility of their use in many more fields than initially anticipated. Moreover electrical characterization of the device has been performed for the first time, demonstrating the possibility of having two or more independent electrodes on each shank, thanks to the effective insulation technique used. Finally, preliminary electrochemical tests have been performed, an important step towards dopamine sensing, that is aimed to be achieved with the devices. Despite these successes, further research has to be performed on the topic. Some future works include:

- Electrochemical tests on the final release probes;
- Sensing of dopamine and possibly other clinically relevant molecules, thanks to surface functionalization of the electrodes;
- Life cycle assessment, to ensure reliability of the electrodes in long-term implants;
- Embedding of CMOS circuitry into the central chip and integration with the electrodes present on the shaft. In case of dopamine detection, an ultra-miniaturized, fully digital potentiostat has already been developed to this scope [18].

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