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Executive Summary of the Thesis

Implementation and Characterization of 64-Channel Systems for Counting and Timing Operation

Laurea Magistrale in Electronics Engineering - Ingegneria Elettronica

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1. Introduction

Light signal analysis is useful in many domains, including medicine and biology. To fulfil the expanding needs and requirements of many applications, the Time-Correlated Single Photon Counting (TCSPC) [1] technology was created, providing precision measurements that enhance traditional methods. Multichannel systems, in particular, have been developed to accommodate parallel measurements such as 2D imaging. The thesis study examines and characterizes two 64-channel systems, a timing module [2] and a counting one. The goal is to assure the appropriate operation of both systems while also analysing their output signals to acquire an accurate description of their characteristics. The two systems are described first, and then the suitable system closure approach is outlined. Following that, the temperature control loop required for system operation is explained. Finally, both 64-channel modules' implementation and characterization are discussed, followed by suggested future developments and concluding observations.

2. Time Correlated Single Photon Counting

TCSPC is a single photon counting application based on periodic stimulation of a sample with a low intensity laser and monitoring of photon arrival time at each interval. A START signal is periodically sent to both the laser and to the measurement system to initiate the time-frame. The electrical signal produced by a detected photon serves as STOP signal. The period between both signals, which is proportional to the photon arrival time, is measured and converted using a TDC (Time-to-Digital Converter) or a TAC (Time-to-Analog Converter) followed by an ADC. Finally, using software tools, this number is processed and stores, generating a complete histogram after several measurements. A different technique, the "reverse start-stop," in which the detected photon acts as the START and the laser serves as the STOP, improve its efficiency, by decreasing the dead time. Moreover, in order to limit the dispersion produced by laser jitter, the STOP signal is delayed, allowing the arrival time to be measured in relation to the laser signal that generates it.

2.1. Temperature effect

SPADs, the main detectors used in TCSPC, can produce signals even without detecting photons due to factors like thermal generation or tunnelling effect. This leads to unwanted counts called DCR (Dark Count Rate). The primary source of device noise comes from the statistical fluctuations of this parameter, so it needs to be minimized. To do that, the operating temperature should be lower than room temperature. However, it should be balanced so that implementing a cooling system does not become overly challenging.[3]

3. 64-Channel System

With the growing number of TCSPC applications, multichannel TCSPC systems have gained popularity. These systems enable the association of each incoming photon with important details like wavelength, time elapsed since the experiment began, and spatial coordinates (in scanning applications). Throughout this project, two multi-channel systems are described: a counting module and a timing module. The timing module may perform both timing and counting operations for 64 parallel channels. Because having one acquisition channel per SPAD is inefficient, a routing circuit is used to decrease this number to 32. The system consists of various boards, as shown in figure 1. They are:

- Detection board: The detection board was designed to perform both timing and counting operations [4]. It comprises the detectors, which convert light into electrical signals, and their corresponding control circuits called AQCs [5]. The generated electrical signals are then sent to the Acquisition boards. Additionally, the system includes an Intermediate Board that enables the use of different SPAD matrices with the same detection board.
- Acquisition board: The acquisition board receives timing and counting signals from the detection system and then it performs time-amplitude conversion (TAC) and analog-digital conversion (ADC), utilizing the FPGA to process digital information. The acquired data is then transmitted externally through either the FTDI USB3.0 chip (for timing signals) or VHDCI connectors (for counting signals). The second board that complains the system is not present in figure 1. Additionally, the acquisition board supplies power to various components of the detection head, and it incorporates one I2C bus.
- Power board: The power board, situated at the bottom of the module, has multiple responsibilities. It provides shielding and supplies 12V power to both acquisition boards. Additionally, it powers the detection board and regulates the detectors temperature. As part of its second objective, the power board generates specific voltages internally and delivers them to the detection head.
- Interconnection board: The interconnection board (T-board) facilitates communication between the FPGAs on both acquisition boards, as well as between the master acquisition board and the power one. It also receives external Stop and Gate signals.

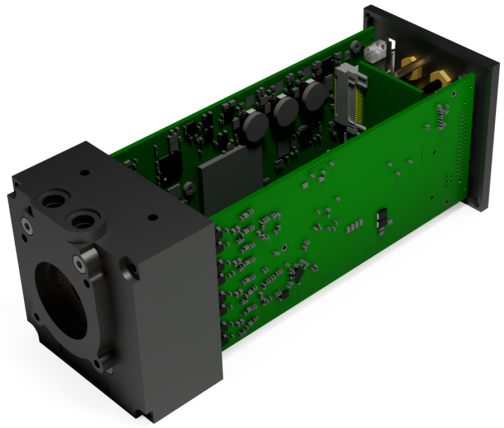

Figure 1: 3D view of the timing module. [2]

The counting module is a simplified version of the timing system. It just handles counting signals and buffers them for output. It can utilize the same detection head by switching to a counting AQC. As counting operations do not require high accuracy, the power board for the counting system is a simplified version compared to the timing one. In terms of the Acquisition boards, they just buffer the output signals and send them externally.

4. Detection Head closure

The detection board is designed to fit between two mechanical components (Fig. 2), the cover

Figure 2: 3D views of the cover (left) and mezzanine (right).

and mezzanine, both made of Roger material, forming the head system. Once assembled, the head system is securely attached to the entire system. The cover, a square component measuring 60x60mm, features a 10mm diameter hole for photon entrance and an inner C-shaped cavity to house the electronics of the board. The mezzanine, positioned at the bottom, includes a cylindrical chamber where the SPADs are located. The Peltier hot side is situated beneath it, and the chamber is isolated using two O-rings. To effectively eliminate internal humidity, the chamber is filled with nitrogen through two valves on one side of the head.

4.1. Closing procedure

Proper detection head closure is crucial in both systems to preserve the inner chamber, where SPADs and other fragile components are situated, well-isolated in order to minimize humidity transfer and to implement the temperature control loop in a system as stable as feasible. To that end, the following head closing procedure is presented:

1. Placing the Peltier and the intermediate board: To maintain precise temperature control, the Peltier cell is positioned at the bottom of the chamber, with its cold side in contact with the intermediate board. To ensure proper alignment, an aluminium support is placed beneath the intermediate board, which must be at the same level as the detection board within the PCB window. Each component is securely affixed using a heat-conductive glue, promoting efficient heat transfer between them.
2. Closing the inner chamber: Prior to closing the head, a desiccant salt is introduced into the chamber to absorb humidity. The closure of the head involves placing a pair of O-rings between the detection board and both the mezzanine and the cover, preventing humidity transfer. The entrance window is then sealed by affixing a glass with Epoxy glue, which requires IR treatment to be seal.
3. Drying the chamber: Finally, the inner chamber is filled with nitrogen via the two valves on one side. Nitrogen will allow the chamber to maintain extremely low humidity levels.

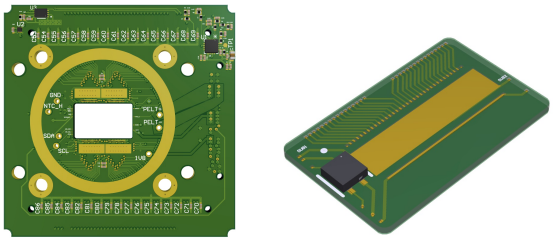

Figure 3: Front view of Detection board (left) and one example of Intermediate board (right).

4.2. Detection head tests

Before sealing the head, tests are performed to check the communication of the I2C buses, which will be used then to implement losses tests. If there are significant losses or insufficient drying, humidity will increase when the temperature decreases. To ensure proper drying, the filling process is developed at around 40^{o}C for a few hours. Maximum humidity levels are drastically lowered with this filling method (from 80% to 10% relative humidity at -10^{o}C). Finally, by repeating the tests after a prolonged period, the humidity values stay nearly unchanged, confirming the minimal amount of system losses.

5. Temperature Control

SPAD's characteristics improve significantly for working temperatures below room temperature. As a result, these systems are kept at -10^{o}C, requiring a temperature control loop to manage them. It was traditionally solved by monitoring the current temperature, comparing it to a target value, and adjusting the Peltier bias to compensate for the difference. Instead, this method provides a non-linear relationship between temperature differential and Peltier voltage drop, requiring the recalculation of PID parameters each time. A new temperature control technique is

devised to address this constraint [6]. It consists of two steps (Fig.4):

1. The PID blocks compute the exchanged heat variation as a function of the actual temperature difference. Because the relationship is linear, PID parameters can only be calibrated once.
2. This exchanged heat variation is translated into a new bias point (in current) for the Peltier via a block A(s).

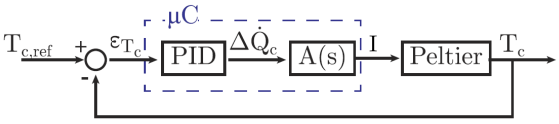

Figure 4: Block scheme of the proposed algorithm.

The non-linear function that A(s) should implement is:

$$\frac{1}{2}R\Delta I^2 + \Delta I(RI - \alpha T_{c,ref}) + \Delta\dot{Q}_c - \alpha\Delta T_c I - K_p\Delta T_c = 0 \quad (1)$$

Instead, there is no need to calculate this equation since the ratio $\frac{\Delta\dot{Q}}{\Delta I}$ in question may be simply derived by performing an adequate characterization of the Peltier behaviour and making some assumptions. Doing that, the curve exchanged heat vs bias current is obtained (Fig.5), which may be interpolated by a second order polynomial curve (Eq.2), from which the previously required relationship can be easily achieved.

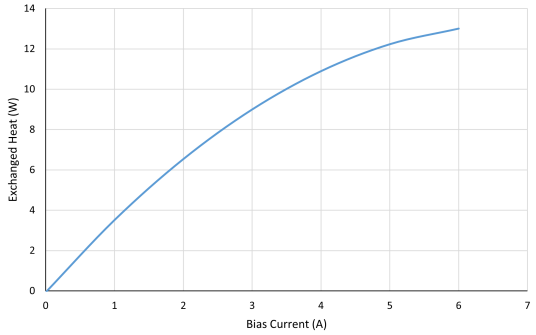

Figure 5: $\dot{Q}$ as a function of I with ΔT=0.

$$\dot{Q}(I) = -0.2811 \cdot I^2 + 3.8671 \cdot I - 0.0714 \quad (2)$$

6. Counting Module characterization

In this chapter, the counting module is mounted using the procedures from the previous chapters, and its functioning is examined. Following that, it is used to achieve various SPADs attributes such as the DCR and PDE (Photon Detection Efficiency), as the system is capable of operating at the appropriate working temperature (-10ºC).

6.1. Functional tests

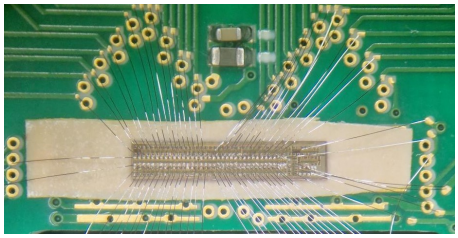

Figure 6: AQC counting bonded and placed on the detection board.

First, the temperature loop is tested to ensure that it responds to different target values and that the humidity protection process is operational. The AQC (Fig.6) and one SPAD can then be bonded to test their functionality. The right behaviour may be verified by analysing the AQC's output signals, as illustrated in figure 7, where the quenching phase is easily distinguished. Then, using the corresponding inter-

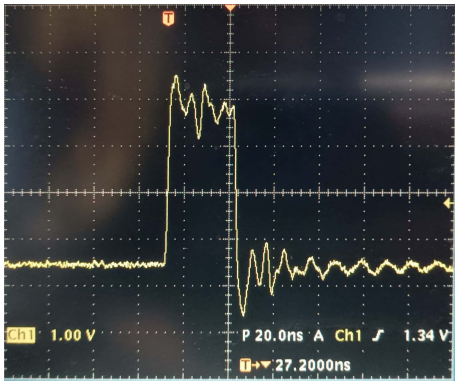

Figure 7: Single SPAD counting output.

mediate board, an 8×8 SPAD matrix is installed, and it is verified that each channel produces the identical prior output response.

6.2. 8x8 SPAD matrix characterization

Once the system's correct operation has been confirmed, it may be utilized to characterize two SPAD matrix typologies (R15 and S13), getting their DCR and PDE levels. Both experiments are carried out at the appropriate operating temperature. The following graphs depict the acquired results of PDE (Fig.8)and Dark Counts (Fig.9) values (N_d) in a determined measurement (T_m). So, the last step, is to obtain the DCR values per channel, by using the following equation (Eq.3):

$$DCR = \frac{N_d}{T_m} \tag{3}$$

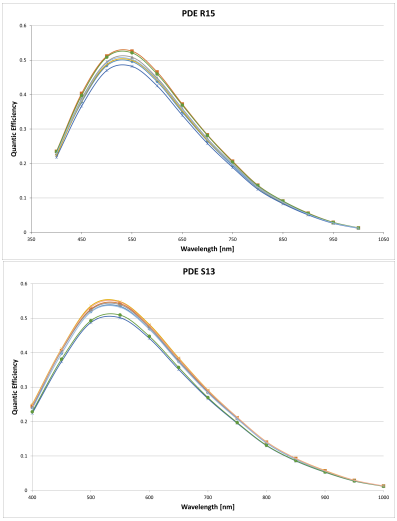

Figure 8: PDE obtained graph for R15 (top) and S13 (bottom) SPAD matrix typologies.

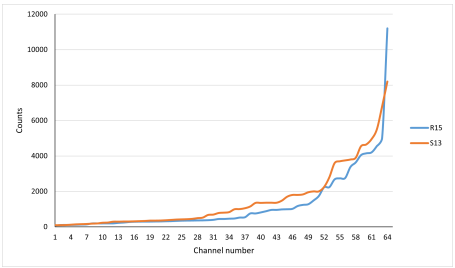

Figure 9: Dark Count values for R15 and S13 SPAD typologies.

7. Timing Module conclusion and characterization

The module will be concluded and characterized in this chapter. First, the system's correct functionality will be confirmed. The entire system is then installed and characterized to gather relevant information on signal dispersion and crosstalk.

7.1. Functional system tests

First, like in the previous chapter, the detection system's correct operation will be checked. The detection system is isolated from the rest of the system for simplicity, using demo acquisition and power boards. The proper behaviour of the AQC timing 's outputs (timing and counting) with a single SPAD is checked by observing them, as illustrated in figure 10. Reset and

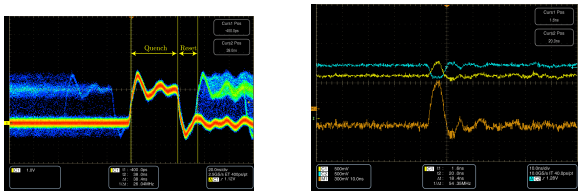

Figure 10: AQC's output signals: counting(left) and timing (right).

Quenching time can be readily estimated from this acquired counting signal, so we can see how they change by varying CtQ and CtR (CtS and Vth have no influence). The real power and acquisition boards can then be attached. The histogram of a single SPAD (Fig.11) may be acquired by utilizing a Labview interface to manipulate the head voltages and a C# interface to plot the results, ensuring that the system is functioning properly.

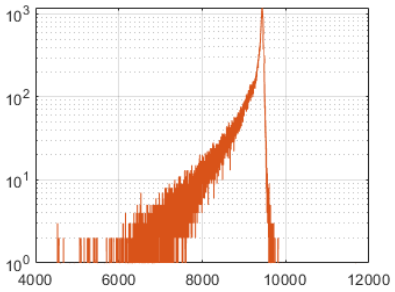

Figure 11: Single SPAD response in log scale.

7.2. Single Channel characterization

The FWMH value (50ps) may be calculated from the previous response (Fig.11), which is an unacceptable number. As a result, multiple modifications are made in an attempt to minimize this figure. To begin, the AQC supply voltage and command values are modified to lower it. It is proved that increasing Vov and Vth, or decreasing the low-voltage supply (1.8V), reduces jitter. As a result, the minimal value of FWMH (43ps) is found with the following values: V_{DD}=1.7V, V_{ov}=5V, and Vth=1.6V. Following that, changes were made to the acquisition chain. The goal is to make faster the edge of the STOP signal, hence minimizing its temporal dispersion. A "Stella Attiva" circuit has been added between the "T-board" STOP input and the external delayer to accomplish this. This, along with an increase in measurement time in the FPGA, results in an FWMH value of 41ps. Furthermore, the jitter's dependency on the introduced delay has been removed, reducing it from 56ps to 44ps for large delay values. Following these enhancements, we can infer that the additional jitter is merely introduced by the Acquisition chain.

7.3. Two Channel characterization

The next stage is to examine the crosstalk between two channels, which may be influenced by the high levels of jitter. The response curves for different CtS levels are derived by analysing the worst-case situation, two neighbouring channels: The signal picks are on the right, with the others

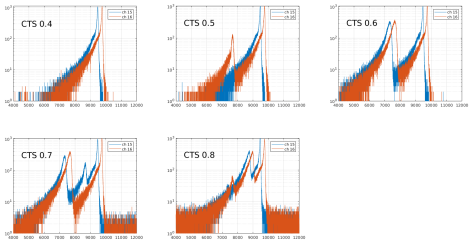

Figure 12: Crosstalk analysis for different CtS values.

being the result of crosstalk. It is observed that crosstalk levels are extremely high, almost as intense as signal ones. To lessen it, both SPADs are replaced with triple-epitassia ones, which offer greater dynamic performances. Because the improvement is insufficient, a novel experiment is created to easily analyse crosstalk, by analysing the DNL (Differential Non-Linearity) induced on a channel (called "disturbed") as effect of the other one (called "disturbing").
The idea is to modify the acquisition firmware to record a "disturbed" event only if a "disturbing" one occurs concurrently and within an established temporal frame, resulting in a detector in free running mode with a punctual disturbance (Fig.13). The centre region relates to dis-

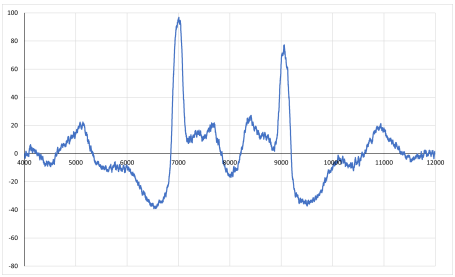

Figure 13: Single channel response of channel 15 being affected by a punctual disturbance.

turbances that occur during the sensing phase and are impacted by V_{ov} fluctuations, whereas the upper picks indicate quenching step disturbances that are influenced by V_{quench} values.At this time, various changes have been made to the system in order to improve the DNL, recognizing which parts of the system affect it the most. First, the bonding configuration is altered (Fig.14), comparing the worst scenario (blue curve) with other having close channels only on the intermediate board (grey curve), in the AQC (orange curve), distant in both parts (yellow curve), or connected to different AQC modules (green curve). It is evident that the highest improvement comes when channels are distant on the intermediate board, implying that these traces have a significant influence on the DNL. Following that, some modifications are made on

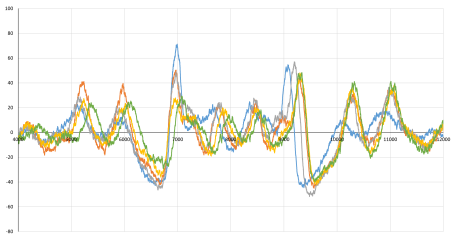

Figure 14: DNL for different set-up

the SPAD voltages connections, which may have

a substantial impact on the DNL. The goal is to isolate as much V_{sub} and V_{cat} of the SPADs as possible. Both voltages are supplied externally to the "disturbing" to do this. As a result, the DNL improves, demonstrating that supply connections are a significant cause of disturbances. The last step is to determine if there is any optical crosstalk as a result of the light emitted during an avalanche operation on the SPAD. To evaluate its impact, the "disturbed" detector was physically screened from the other. Since the DNL response stays essentially unchanged, this effect is likely to be negligible. Finally, for the sake of completeness, the INL (Integral Non-Linearity) was plotted (Fig.15) to compare the initial situation with the one after the introduced modifications. The INL has certainly improved substantially, becoming much more uniform.

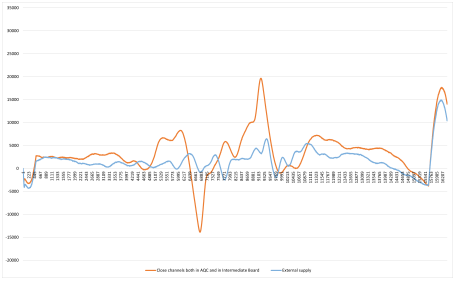

Figure 15: INL comparison after system enhancements.

8. Conclusions

Both modules, as demonstrated throughout the project, are viable solutions for multi-channel systems with a significant number of channels, allowing them to function for diverse SPAD matrix typologies. However, the timing module design is not optimal, presenting significant signal jitter and crosstalk. On the one hand, in terms of jitter, the T-board portion in charge of receiving the STOP signal, which is the most influential jitter source, should be redesign. For crosstalk reduction, on the other hand, enhancements should be focused on the Detection and Intermediate boards, by coupling more efficient SPAD supply voltages and removing the Intermediate board traces, which are the primary crosstalk causes.

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