POLITECNICO
MILANO 1863

SCUOLA DI INGEGNERIA INDUSTRIALE
E DELL'INFORMAZIONE

Validation of a CMOS driving circuit operating up to Cryogenic Temperatures for Single-Photon emitting Diodes

Tesi di Laurea Magistrale in
Electronics Engineering - Ingegneria Elettronica

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Academic Year: 2020-21

Abstract

The approach to quantum mechanics that has sparked the world of physics's fervor over the last decade is resulting in a true quantum revolution in the most diverse fields of physics and engineering this century. In the field of data exchange security, the vulnerability of channels that use traditional encryption systems to the looming computing power quantum computers are estimated to reach has prompted the scientific community to develop new protocols that increase data transmission security levels. One of the most promising communication protocols whose secrecy is based on quantum properties of matter is undoubtedly the Quantum Key Distribution (QKD), which has demonstrated its efficiency in establishing secure intercontinental quantum communications by exploiting a network of optical fibers or satellites orbiting the planet.

Within this technological context, it can be found the QUASIX project (single photon integrated source for QUAntum SIlicon Communications in Space), funded by the Italian Space Agency (ASI) and coordinated by Consiglio Nazionale di Ricerche (CNR) with Istituto di Fotonica e Nanotecnologie (IFN-CNR) and Istituto per la Microelettronica e Microsistemi (IMM-CNR), in collaboration with Politecnico di Milano, Scuola Superiore Sant'Anna di Pisa and Università di Padova, which aims to create an integrated optoelectronic system that can allow the implementation of QKD protocols in space and in which this thesis work has been inserted, aimed at validating the integrated driver for single-photon emission in Erbium-doped diodes.

This work is the continuation of the two previous thesis works that involved two major activities: in a first phase, the characterization of optical sources and electronics at temperatures of 77K, fundamental for a chip whose specifications include operation at cryogenic temperatures, and secondly the design of the integrated electronic system, including the temperature sensor, the stage that deals with the driving of the photon source and the ancillary electronics to complete the system, up to the submission to the foundry of the final circuit.

While waiting for the chip to be realized in order to conduct circuit's testing and validation phases, the characterization activity of the adopted CMOS technology was resumed, aimed

at the extraction of the simulation models BSIM3v3 to 77K, with the goal of obtaining a more complete model than the previous one in order to use it in a future version of this chip, and at the calibration of the temperature sensor by means of an updated measurement setup to achieve high accuracy.

Then the focus shifted to the cryogenic probe, in particular on the implementation of a more performing probe, meeting the requirement for a greater number of connections and broadband connections for triggers and for the reading of the output signal from the chip, more ergonomic and that disperses less heat along its structure; on the creation of two test cards, one attached to the probe that houses the temperature sensor and on which the low-frequency wires have been soldered, and one mobile suitable to accommodate the QUASIX chip, the Erbium diode, discrete components and high- and low-frequency connectors; finally on the microcontroller firmware for digital communication with the ASIC. As a conclusion of this thesis work, once the chip shipped from the Foundry arrived, electrical characterization and analysis of the performance of ASIC and, in parallel, of the Erbium-doped diodes has been run.

Keywords: Quantum; QUASIX; ASIC; characterization; integrated; probe; temperature; cryogenic; erbium-doped; diode; measurements; PCB; firmware; DAC

Abstract in lingua italiana

Nell'ultimo decennio, l'approccio alla meccanica quantistica che ha suscitato il fervore del mondo della fisica sta dando vita, in questo secolo, a una vera e propria rivoluzione quantistica nei campi più svariati della fisica e dell'ingegneria. Nell'ambito della sicurezza dello scambio di dati, la vulnerabilità dei canali che utilizzano sistemi di crittografia tradizionali alle incombenti potenze di calcolo che si stima possano raggiungere i computer quantistici ha stimolato il mondo scientifico a realizzare nuovi protocolli per il raggiungimento di livelli di sicurezza maggiori per la trasmissione di dati. Tra i più promettenti protocolli di comunicazione la cui segretezza si fonda su proprietà quantistiche della materia si fa spazio la Quantum Key Distribution (QKD), che ha dimostrato la sua efficienza nell'instaurare comunicazioni quantistiche intercontinentali sicure sfruttando un network di fibre ottiche o satelliti in orbita attorno al pianeta.

In questo contesto, si pone il progetto QUASIX (single photon integrated source for QUAntum SIlicon Communications in Space), finanziato dall'Agenzia Spaziale Italiana (ASI) e coordinato dal Consiglio Nazionale delle Ricerche (CNR) con l'Istituto di Fotonica e Nanotecnologie (IFN-CNR) e l'Istituto per la Microelettronica e Microsistemi (IMM-CNR), in collaborazione con il Politecnico di Milano, la Scuola Superiore Sant'Anna di Pisa e l'Università di Padova, che si pone come obiettivo quello di realizzare un sistema optoelettronico integrato che possa permettere l'implementazione di protocolli QKD nello spazio e nel quale si è inserito questo lavoro di tesi, volto a validare il driver integrato per sorgenti di fotoni costituite da diodi drogati con erbio.

Questo lavoro è la prosecuzione dei due precedenti lavori di tesi durante i quali sono avvenute, in una prima fase, le caratterizzazioni delle sorgenti ottiche e dell'elettronica a temperature di 77K, fondamentali per un chip le cui specifiche comprendono l'operatività a temperature criogeniche, attività riprese anche in questo elaborato, e secondariamente la progettazione del sistema elettronico integrato, comprendente il sensore di temperatura, lo stadio che si occupa del driving della sorgente di fotoni e l'elettronica ancillare a completamento del sistema, fino ad arrivare alla sottomissione alla fonderia del circuito finale. In attesa che il chip venisse realizzato in modo poi da poter condurre la fase di test e validazione del circuito, si è ripresa l'attività di caratterizzazione della tecnologia CMOS

adottata, finalizzata all'estrazione dei modelli simulativi BSIM3v3 a 77K, con lo scopo di ottenere un modello più completo del precedente nell'ottica di utilizzarlo in una futura versione di questo chip, e alla calibrazione del sensore di temperatura mediante un setup di misura aggiornato per ottenere un'elevata accuratezza.

Successivamente il lavoro si è focalizzato sulla sonda criogenica, in particolare sull'implementazione di una sonda più performante, ovvero adeguata all'esigenza di un numero di connessioni più alto e di connessioni a banda larga per i trigger e per la lettura del segnale in uscita dal chip, oltre che più ergonomica e che disperdesse meno calore lungo la sua struttura; sulla realizzazione di due schede di test, una fissata alla sonda che alloggia il sensore di temperatura e sulla quale sono stati saldati definitivamente i fili delle linee a bassa frequenza e una mobile atta ad ospitare il chip QUASIX, il diodo all'erbio, la componentistica discreta e i connettori ad alta e bassa frequenza; infine sul firmware microcontrollore per la comunicazione digitale con l'ASIC. Come conclusione di questo lavoro di tesi, una volta ricevuto il chip dalla fonderia, si è passati alla caratterizzazione elettrica e all'analisi delle performance dell'ASIC e, in contemporanea, dei diodi drogati all'erbio.

Parole chiave: Quantistico; QUASIX; ASIC; caratterizzazione; integrato; sonda; temperatura; criogenico; erbio; diodo; misure; PCB; firmware; DAC

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Introduction

Over the last decade, several fields of physics and engineering have benefited significantly from the increased ability to manipulate the characteristic phenomena of quantum mechanics such as *entanglement* and *state overlap*. It is referred to as the "quantum revolution," and it encompasses all novel applications that make use of the quantum states of individual photons, atoms, and electrons, or superconductors.

The quantum revolution, fueled by fabrication advancements and a deep understanding of quantum mechanics by the scientific community, will elevate quantum technologies to increasingly significant positions in a variety of fields of research and in everyday life. A well-known quantum cryptography protocol known as *Quantum Key Distribution (QKD)* is an example of this, as it represents a true breakthrough in the field of high-security telecommunications, providing a channel for the exchange of information with arbitrary security, potentially infinite. More precisely, astutely utilizing quantum mechanics principles, the encryption key used by the interlocutors to conceal and then decipher the message's meaning is made susceptible to interception by an "eavesdropper" outside the channel.

Due to its distinguishing characteristic, this type of quantum communication holds a place of respect in a wide variety of applications that require an extremely secure communication channel, proving to be one of the most promising branches of telecommunications. It is not surprising that the QKD market will soon experience significant growth, owing to the interest of numerous investors worldwide and the technological advancements made to these systems. Consider how the Internet, which began as a simple communication infrastructure, has evolved into an unimaginable mass phenomenon accessible to everyone, from the most humble individuals to the world's most powerful government officials. Today, the Web serves as an environment for exchanging resources, culture, and experiences that our society can no longer live without. However, this digitalization phenomenon inevitably results in heightened attention being paid to the issue of personal data protection and user safeguard. Military applications, digital healthcare in hospitals, internet banking, and e-commerce are just a few of the numerous fields in which security is critical.

Quantum Key Distribution *networks* that operate on a *global scale* via dedicated satellites are particularly well suited to these areas, enabling secure communications over a wide range. Currently available on the market, the primary QKD systems are mostly realized using discrete components, which are not ideal for bringing these applications into space. Complete integration of such quantum systems on silicon would provide benefits in terms of compactness and portability in space, as well as optimal solutions for controlling them with extreme precision and accuracy.

1 | Quantum Key Distribution and QUASIX Project

1.1. Cryptography

In information theory, cryptography is defined as the totality of the techniques put into practice to conceal the information contained in a message so that the only entity able to derive it is the recipient. In particular, taking digital systems into account, cryptography manifests itself in all those algorithms designed to protect sensitive and personal information exchanged between two or more users, avoiding unwanted reading by unauthorized entities. These algorithms, combining the message to be exchanged with additional information called *encryption key*, constitute systems known as *cryptosystems*.

1.1.1. Cryptosystems

The ultimate purpose for which cryptographic algorithms are made is to safeguard and protect the information to be shared at least during the period of validity of the latter. To accomplish this, such algorithms employ special functions dubbed *trapdoor functions* to generate the encryption keys. This mechanism is based on mathematical functions that are simple to execute in one direction but enormously complicated and computationally inefficient in the reverse direction without the use of specific *trapdoors*, information that significantly simplifies the resolution of their inverse functions.

This is how the primary cryptosystems used today, by exploiting the hardly avoidable limits of current computational power via particular asymmetric mathematical problems that are simple to verify but difficult to solve, guarantee the indecipherability of the information for as long as it is valid, assuming the trapdoors remain secret. To illustrate, a mathematical problem of this type is factorization in prime numbers, upon which a cryptosystem known as *RSA*, one of the most widely used cryptosystems for secure data transmission, is based. Indeed, this problem belongs to the class of problems that are not deterministic in polynomial time, that is, it is not sufficient a time proportional to a

power of the problem's dimension using a deterministic Turing machine. In other words, as the number of digits in the prime number increases, the time and number of operations required to solve the problem skyrocket.

Nevertheless, the indecipherability of information encoded by cryptosystems based on unoptimized mathematical solutions is constantly undermined by the possibility, however remote, of resolving such problems with innovative technologies. Among the algorithms that should be addressed in this context is Shor's algorithm. It is a quantum algorithm developed in 1994 by Peter Shor to solve the problem of integer factorization in a non-traditional manner [20]. Using quantum mechanics features, this approach is able to optimize the factorization of large integers problem, drastically reducing the solving time required by a classical method implemented on a standard computer. It is required to be implemented on a quantum computer, a system in which information is coded in basic units known as qubits, which, in contrast to their traditional counterparts, are capable of defining non-conventional operations.

As a result, quantum computers, if capable of managing a sufficiently large number of qubits, will pose the greatest risk to RSA cryptosystems. In addition, the computing power of quantum computers has already demonstrated its incredible efficiency when compared to that of traditional computing systems, demonstrating how, in a matter of minutes, a quantum computer is capable of solving calculations that would take a traditional computer thousands of years to complete [16].

1.2. Quantum Key Distribution

On the one hand, when applied to a computational environment, quantum mechanics generates a plethora of implications that compromise the security of traditional cryptographic systems; on the other hand, when their properties are explored and applied to create communication channels, quantum mechanics can generate protocols that overcome the fundamental limitations of traditional cryptography.

By investigating the transmission of digital information via an elementary quantum system, such as a polarized photon, one can develop quantum cryptography systems with features that are not accessible via conventional communication protocols. In this way, a quantum communication channel can be established in which exchanged information cannot be captured without the consent of the speaking parties, owing to the *Heisenberg uncertainty principle*. This is possible because information interception would result in an unpredictable and uncontrollable modification of communication, as observed by legitimate users of the transmission channel.

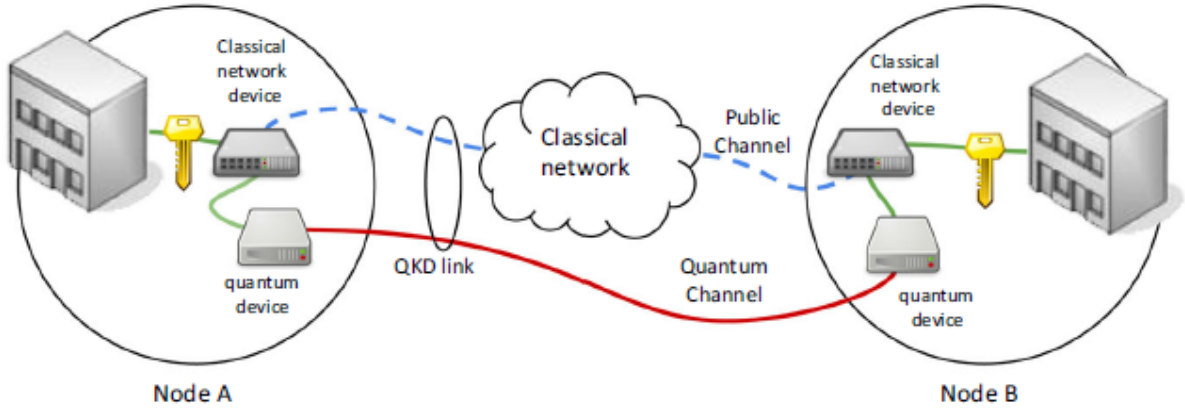

Figure 1.1: A schematic representation of a link implementing the QKD between Alice (node A) and Bob (node B). The link consists of two channels: a quantum one (outlined in red) in which photons are exchanged and a traditional public channel (outlined in blue) in which normal digital bits are exchanged [15].

Thus, a quantum channel constructed in this manner can be used in conjunction with a traditional public channel to distribute security keys between the channel's users, with the assurance that the communications will not be intercepted by potential "eavesdroppers," even if the channel's speaking parties do not initially share private information. *Quantum Key Distribution (QKD)* or a system for quantum distribution of encryption keys is the term given to the system thus built. A quantum communication channel of this type, due to the poor performance in terms of bit rate, is not used to send the actual encrypted information, but purely to exchange the encryption key, which is a series of bits randomly generated at the time of the procedure. Figure 1.1 shows a schematic rappresentation.

Assuming that two users, conventionally referred to as *Alice* (transmitting node) and *Bob* (receiving node), wish to establish a quantum communication in which private information is transmitted via appropriately polarized single photons, a potential eavesdropper will be unable to obtain any information secretly from the communicating parties due to Heisenberg's uncertainty principle.

Indeed, by guaranteeing the impossibility of measuring a quantum state without causing it to be perturbed by the measurement itself, this principle ensures that it will be impossible for an eavesdropper, referred to as *Eve*, to obtain any details about the communication between Alice and Bob without introducing perturbations that reveal their presence. Therefore, if the number of perturbated photons that Bob has received does not exceed a certain threshold, then it means that during their propagation no measurements were made on them and therefore Eve does not have any information about photons sent by Alice.

From a subsequent public consultation on an ordinary non-quantum channel (and thus susceptible to interception by Eve), Alice and Bob can conclude, with a high probability, whether the original quantum transmission was disrupted during the transit, for example, as a result of a wiretap by Eve. To verify this, after the exchange, Alice and Bob can check if Eve was listening during their communication simply by comparing the actual correspondence of random subsets of the exchanged photons. If after the comparison the transmission is found to be free of disturbances, then Alice and Bob agree to use the encryption key generated by the quantum exchange previously occurred to encrypt the secret information to be shared. In case the transmission has been disturbed, then the two interlocutors discard all the bits exchanged by means of the quantum channel and repeat the operation.

Such systems for quantum distribution of encryption keys have two main implementations: the *BB84 protocol* [6], which makes use of single appropriately polarized photons and the *Ekert scheme* [8], which is based on the use of *entangled* photon pairs and exploits *Bell's inequality* to ensure system safety. In the following, we will concentrate on the first.

1.2.1. The BB84 protocol

In 1984, at the University of Montréal, physicist and cryptographer Charles H. Bennet and computer scientist Gilles Brassard collaborated to create the world's first working quantum cryptography protocol, dubbed the BB84 protocol. This protocol, which serves as the foundation for all subsequent QKD systems, which in turn are considered variants of BB84, encodes information using four quantum states. These states are obtained by polarizing photons and assigning them a value of 0 or 1 based on their polarization.

To obtain a beam of photons arbitrarily polarized is resorted to a polarizing filter or a crystal of calcite, a polarizing apparatus whereby, having fixed its internal orientation, the emerging photon beam will be polarized according to this orientation. While polarization is a continuous variable, Heisenberg's uncertainty principle prevents measurements on polarized photons from detecting more than one bit of information about their polarization. Consider, thus, a photon beam emerging from a polarizing apparatus whose internal polarization axis is set at an α angle. This beam is directed to a polarizing filter oriented with a β angle. The photon behaves probabilistically at this point, with a probability of being transmitted equal to $\cos^2(\alpha - \beta)$ and a complementary probability of being absorbed equal to $\sin^2(\alpha - \beta)$. As can be seen from the two formulas, there are two relative orientations of the axis of the beam and of the filter such that photons behave deterministically, that is, when the axes are parallel (certain transmission) and when the

axes are perpendicular (certain absorption). In all the remaining cases, when the axes are not orthogonal, some photons will be transmitted and others will be absorbed with a corresponding probability that follows the previously illustrated trend.

An alternative to obtain more information about angle α by measuring the transmitted photon is to use an additional polarizing filter oriented according to a hypothetical third angle. However, this is not possible, because the light beam exiting the polarizer with angle β emerges exactly with polarization β and has no memory of the previous polarization α.

An additional strategy could be adopted. If from a single photon only one bit of information can be obtained, it would be enough to multiply it by copying it to obtain a greater number of the same photon with the same polarization. In this way, it is possible to make multiple measurements and trace more than one bit of information from a single photon. Unfortunately, according to the postulates of quantum mechanics, the cloning operation would violate the *principle of no-cloning* [23], which asserts that an unknown a-priori quantum state cannot be copied exactly, i.e. cloned.

Considering what has been exposed thus far, the BB84 protocol encodes the bits of information using four polarizations corresponding to four distinct quantum states. It employs two bases of polarization, one linear (horizontal and vertical) and one diagonal (north-east south-west, north-west south-east). Each photon belonging to a particular base and

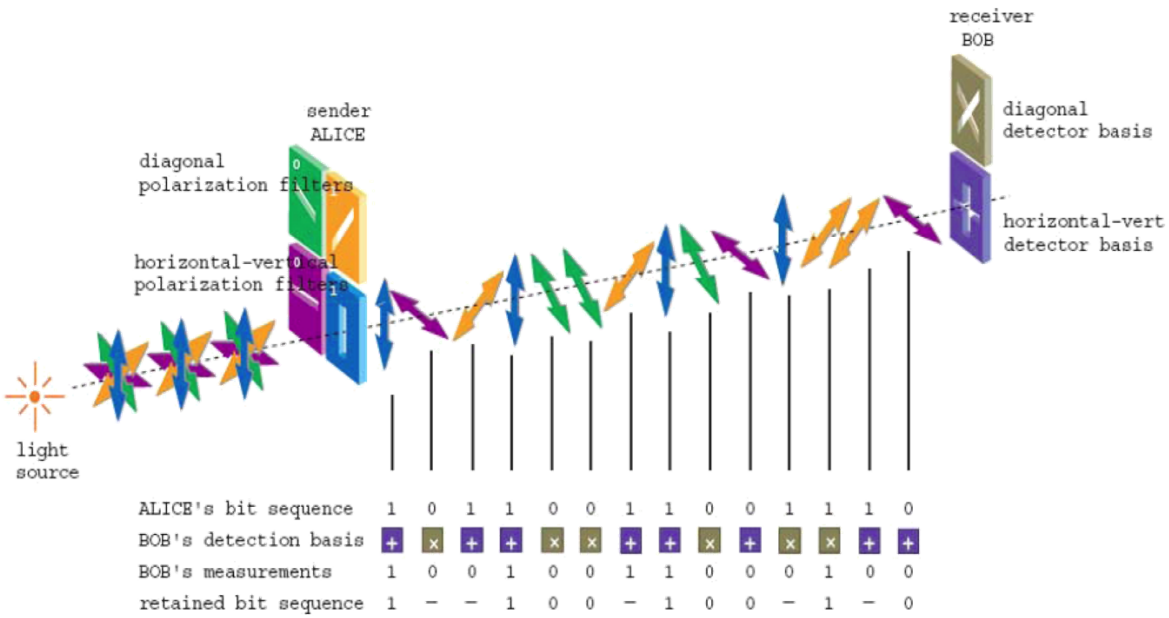

Figure 1.2: Example of quantum communication between Alice and Bob [2].

possessing one of the two possible polarizations associated with that base is then assigned to a digital bit, either 0 or 1, thereby establishing a coding convention. For example, a convention could be to associate the digital value 0 with the horizontal polarization and 1 with the vertical polarization in the linear base and, in the diagonal base, to associate the value 0 with the angle 45° polarization and the value 1 with the angle −45° polarization.

As illustrated in the preceding paragraph, any QKD system is structured around two channels: a quantum one for generating the encryption key and a traditional public one for validating the generated key before proceeding to the actual data exchange. As a result, we will analyze the QKD process in its two primary phases, which correspond to the different channels of communication used.

The first phase entails the selection of a random sequence of bits and a corresponding random sequence of bases of polarization with which Alice encodes these bits. Through the quantum communication channel, photons polarized according to these bases are sent to Bob. Each polarized photon thus represents a bit of the initial string in relation to a base chosen by Alice previously. In a completely uncorrelated way with respect to the steps Alice has taken, Bob generates a sequence of polarization bases from his side, which he will use to decode the train of traveling photons in a quantum channel and interpret the measurement result using a digital value, as illustrated in Figure 1.2. The bits that are actually saved in the final stages of the process because they are considered "correct" and will eventually be used to generate the encryption key for the subsequent encryption of the secret information after a validation phase via the public channel, will be nothing more than those correctly received by Bob and corresponding to the photons for which the base chosen by Bob will coincide with the one adopted by Alice.

Before proceeding to the next phase, it is prudent to dwell on the following considerations. According to the preceding reasoning, when Bob measures a received photon using a different polarization base than Alice, the measurement operation would give a random digital value in the output. So, statistically speaking, on a huge number of photons sent, the interpretation of Bob's measurement is correct only in half of the cases, that is, when Bob chooses the same polarization base as Alice for photon reading.

However, in practice, this is an ideal estimate that does not account for the quantum channel's inherent losses; thus, in addition to the reduction caused by the choice of different bases, a portion of the photons sent by Alice will undoubtedly be absorbed by the channel, further reducing the useful bits received by Bob. Along with quantum channel losses, another factor that definitely contributes to a further reduction in the photons actually received by Bob is represented by the quantum efficiency of a real detector, that

as such, will certainly be less than 100% and thus contribute an additional source of reduction in the number of bits actually received by Bob.

Continuing with the description, the protocol's second phase occurs via a traditional channel of communication that is no longer private. It begins with a verification of what Bob received in the previous phase, through a public message exchange. Bob communicates the bases he used to interpret the photons he received successfully, allowing Alice to discard all those bases that do not match the bases she chose. As a result, Bob will presumably have all those bits corresponding to the bits that Alice chose to send him at the beginning of the first phase. To conclude, Bob sends a subset of the bits obtained thus far so that Alice can verify the correspondence. If the photons transmitted in the quantum channel were not victims of eavesdropping, Alice and Bob agree on the bits encoded by those photons, despite the fact that they were never shared publicly.

Quantum Transmission															
Alice's random bits	0	1	1	0	1	1	0	0	1	0	1	1	0	0	1
Random sending bases	D	R	D	R	R	R	R	R	D	D	R	D	D	D	R
Photons Alice sends	⤢	↕	⤡	↔	↕	↕	↔	↔	⤡	⤢	↕	⤡	⤢	⤢	↕
Random receiving bases	R	D	D	R	R	D	D	R	D	R	D	D	D	D	R
Bits as received by Bob	1		1		1	0	0	0		1	1	1		0	1
Public Discussion															
Bob's bases of received bits	R		D		R	D	D	R		R	D	D		D	R
Alice discards wrong bases			✓		✓			✓				✓		✓	✓
Presumably shared data			1		1			0				1		0	1
Bob reveals a subset					1									0	
Alice confirms it					✓									✓	
Outcome															
Shared secret bits			1					0				1			1

Figure 1.3: A representation of the BB84 protocol at a small scale. The table clearly distinguishes the first *quantum* phase, in which Alice transmits a sequence of bits of information encoded according to a specific polarization of photons via the quantum channel, from the second *classical* phase, in which Alice and Bob analyze a subset of hypothetically valid bits received by Bob via a public channel to determine whether Eve has possibly intruded. If Bob's subset contains a sufficient number of valid bits to safely exclude Eve's intrusion, the QKD can be considered terminated and the encryption key shared. Empty bits denote missed readings [6].

When quantum communication is disrupted, the situation is quite different. If Eve intercepts the photons and wants to get a bit of information by measuring a certain photon, the latter will be irreversibly altered, resulting in a possible disagreement on the corresponding bits exchanged between Alice and Bob, that otherwise should coincide. Although this operation results in the loss of secrecy of the underlying bits, it, however, has no effect on the security of the protocol since a random subset of all valid bits is chosen. Therefore, after verification, a substantial part of the key generated in a quantum way remains secret. However, for this control to succeed, it is essential that the position of the bits to be compared is chosen randomly, making it highly improbable that Eve's possible intrusion will go undetected.

If after the confrontation, Alice and Bob agree on the decided subset of bits, then they can conclude that the broadcast was not significantly disturbed by Eve and that, therefore, the remaining photons sent and received with the same base also match, allowing them to be used to encrypt and transmit subsequent communications over a public channel. Figure 1.3 gives a detailed example of the entire BB84 protocol, including the quantum transmission phase, which was already discussed in Figure 1.2, as well as the subsequent public discussion phase and the resulting ultimate encryption key.

Eve can, however, prevent Alice and Bob from communicating by suppressing the messages exchanged between the two interlocutors on the public channel or by interfering excessively with their quantum communication. However, in both cases, Alice and Bob jointly agree that their communication has almost certainly been suppressed and are not misled into believing that their communication is secure when it is not. Additionally, there is a final scenario in which Eve intentionally intercepts a few photons. In this case, Bob's key will be different from Alice's because, during the verification phase of the subset of bits, the two interlocutors will be unaware of Eve's presence, despite having nicked some bits of the key. Eve does not obtain the encryption key, but rather obstructs the secret key's proper delivery.

1.2.2. QKD, research and future development

In principle, any two-level quantum system could be used to construct a quantum cryptography system. However, all implementations made use of photons in practice. This is because, in general, photon implementations allow for precise control of their interaction with the surrounding environment, in addition to the fact that photon implementations can leverage the countless tools developed for optical telecommunications over the preceding decades.

Significant application interest, and the focus of much research, is the development of systems capable of transmitting quantum information over distances of the order of tens of kilometers through the use of optical fibers. The wavelengths typically used are between 1300 and 1550nm, which correspond to the wavelength range used in modern fiber optic telecommunications, though photon detectors operating at these wavelengths are typically less efficient than those operating at, for example, 800nm. The wavelength is determined by the glass optical fibers that are primarily used today, which have a lower infrared attenuation than optical fibers developed to operate at other wavelengths. Indeed, the great limit of a quantum channel composed of optical fibers is represented by the inevitable dispersions that limit its maximum extent, since the photon beam conveyed on fiber will be more and more attenuated the longer the distance it will have to travel to reach the recipient of the information [10].

In addition to the quantum channel that connects the two users of communication, it is necessary to mention the primary sources and detectors of photons adopted on the sender and receiver sides, respectively. Generally, the photon sources used in the practical implementation of QKD systems consist in the use of weak laser pulses or entangled photon pairs [12]. On the receiving side, however, the adopted detectors play a key role in the success of quantum cryptography and it is of fundamental importance, in fact, that the receiver is able to capture the photons sent to it. Among the various photodetectors adopted, the most common solution is represented by the use of *Avalanche PhotoDiodes (APD)*.

Since the first experimental projects, significant progress has been made in the last two decades, particularly in terms of reliability and application range. In fact, today there are several companies that market QKD systems, becoming that of quantum cryptography, in fact, an application no longer relegated to the world of research but now ready to give rise to quantum encryption networks. Among the numerous companies that market hardware for implementing the QKD, ID Quantique, MagiQ Technologies and Quintessence Labs should be mentioned. All systems offered by these companies are based on the use of the normal existing fiber optic infrastructures and cover ranges of slightly more than 100 kilometers.

As previously stated, the totality of quantum systems that utilize photons to realize their own quantum states can currently take advantage of a broad range of optical telecommunications technologies that have been well established over decades of development. However, systems that rely on such instruments are not without flaws of their own. Along with all channel losses due to dispersion, one of the most significant limitations in the implementation of fiber optic QKD systems that encode information via photon polar-

ization, such as the BB84 protocol, remains the transformations induced on the photons' polarization by a long optical fiber, which have been observed to be unstable over time and a source of the onset of optical noise. Additionally to the optical noise generated by the quantum channel, an optical noise generated by the detector is added. As a result, a figure of merit was defined to aid in quantifying the contribution of such optical noise, the Bit Error Rate (BER) being a critical parameter for a telecommunications system defined as the relationship between the number of incorrect revelations and the total number of revelations. Therefore, the contribution from the quantum channel appears to be the limiting factor, especially when one considers that an extension on fiber would inevitably require quantum repeaters, which are currently not mature enough to be implemented.

In light of the foregoing, in order to circumvent the limitations imposed by a quantum channel comprised of optical fibers, the problem was faced from another perspective, namely by testing systems that implement QKD protocols in free space. Substituting the use of fiber optics with free space transmission has a number of advantages, one of which is that the atmosphere has a large transmission window around the wavelength of $770nm$, within which photons can be easily captured using highly efficient commercial detectors. Additionally, the atmosphere is very little dispersive at these wavelengths and is substantially isotropic, meaning it is not subject to stress, in contrast to the optical fiber, which demonstrates birefringence properties. Finally, there is another transmission window of interest around the $1550nm$ wavelength because it is compatible with fiber optic communication, giving the possibility to realize more versatile hybrid communications.

Some disadvantages of free space propagation are represented by the possible interference on the proper functioning of the system of daylight or light reflected by the moon, that can be coupled with the receiver increasing the error on the reading of the received photons. However, these errors can be corrected by combining spectral filters and spatial filters at the side of the receiver, or by using time discrimination techniques with coincidence windows typically lasting a few nanoseconds [10]. However, it is clear that the performance of systems in free space depends drastically on weather conditions.

1.2.3. Quantum Space Applications

In order to obtain worldwide coverage of systems that take advantage of photon polarization to realize the quantum distribution of encryption keys, the most promising horizon on which research is approaching is represented by telecommunications systems that explore the use of satellites and links with space. Moving, therefore, the quantum channel mostly into empty space, where losses are substantially negligible, the big limit imposed by the

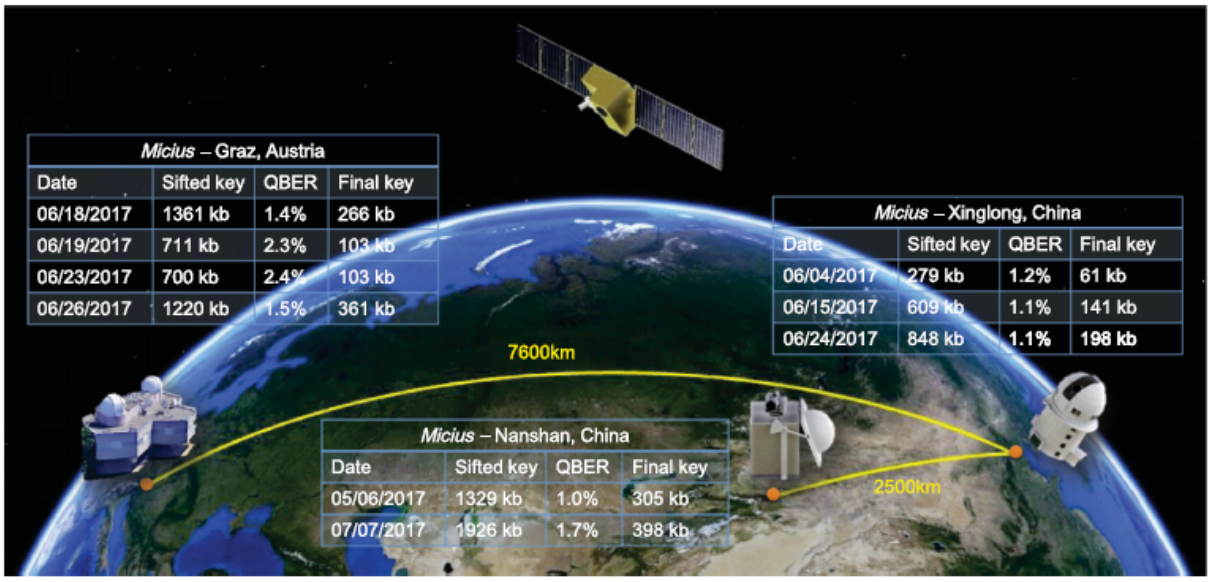

Figure 1.4: Connections between the three ground stations (Graz, Nanshan, and Xinglong) and the major experimental results obtained (respective length of the keys generated during the connection, QBER and date of the experiment) [13].

fiber optic vanishes, thus allowing the connection of two extremely distant points on the earth without having to resort to still-under-development repeaters.

First among all nations to mobilize in this perspective, China on August 16, 2016, launched into orbit, from the Jiuquan Satellite Launch Center, the first satellite in the world dedicated to experimentally examining the feasibility of quantum communications in space [24]. This satellite, called *Micius* after an ancient Chinese philosopher, implements the BB84 protocol and to do so the transmitter, located inside the satellite, adopting very weak laser pulses, works with photons at a wavelength of approximately 850nm and with a repeating frequency of 100MHz. Micius, which orbits at an altitude of about 500 kilometers, has established a quantum link with the Xinglong astronomical observatory covering a distance of 1200 kilometers, demostrating that it can go well beyond the few hundred kilometers possible on fiber, at a bit-rate in the kilohertz range [14].

As a result of this initial realization, further global-scale quantum network experiments have been successfully conducted, establishing a link between locations in China and Europe at a distance of 7600 kilometers [13]. The connection was realized through three *ground stations*: two in China, located in Xinglong and Nanshan, at a distance of approximately 2500 kilometers from each other, and one in Austria, located in Graz, at a distance of 7600 kilometers from Xinglong. The satellite completes 94-minute orbits around the Earth and passing over the three ground stations enables a *downlink* of a

duration of 300 seconds, cyclically achieving a *key rate* of about 3 kbps over a physical distance of about 1000 kilometers under favorable weather conditions. The system was able to generate secure encryption keys with a data transfer rate of 833 kbps between the three locations. The major performances of such communications, as well as the three ground stations, are depicted in Figure 1.4.

To give an idea of the versatility of the satellite and its real application potential, Micius was used as a vector to transmit a 5.34 kB image of the philosopher Micius from Beijing to Vienna and vice versa, as well as an image of Schröedinger from Vienna to Beijing, using a combination of the quantum satellite network between Vienna and Xinglong and the 280 kilometers of fiber optic QKD metro networks connecting the Xinglong ground station to Beijing.

Furthermore, a 75-minute videoconference was held on 29 September 2017 between the Chinese Academy of Sciences and the Austrian Academy of Sciences, which collaborate on the Micius project, transmitting approximately 2GB of data and consuming approximately 2 kB of the quantum keys generated between Austria and China [13]. The project demonstrated the feasibility of intercontinental quantum key distribution networks, paving the way for the eventual realization of a truly global quantum communication network. In this perspective, in fact, the same bodies that have promoted research are already planning to launch other satellites on into higher orbits, so as to allow more effective and longer-lasting quantum communications.

1.3. The QUASIX project

Within this context, the QUASIX project (*single photon integrated source for QUAntum SIlicon Communications in Space*) finds its place. Funded by the Italian Space Agency (ASI), it aims to create an integrated source of single photons in silicon for quantum communications in space and on which the thesis work was focused. From the interest of large countries, first of all China, and the significant funding from private entities, QUASIX seeks to develop new space components in anticipation of the imminent expansion of encrypted quantum communications in space. The project, a collaboration between Istituto di Fotonica e Nanotecnologie (IFN) and Istituto per la Microelettronica e Microsistemi (IMM) of Consiglio Nazionale delle Ricerche (CNR), Politecnico di Milano, Scuola Superiore Sant'Anna of Pisa and Università di Padova, aims to create single photon sources using Erbium-doped silicon diodes capable of emitting individual photons at a rate between MHz and GHz at a wavelength of around $1500nm$.

The project's necessity to realize a silicon-based source stems from the desire to find a

source that is easily embeddable and scalable in standard CMOS manufacturing processes, allowing for the creation of a compact and effective integrated system in which the diode and associated integrated control electronics are contained in a single package.

The two CNR institutes in Milan and Catania are responsible for realizing the silicon Erbium-doped diode in order to obtain a reliable photon source with the required bandwidth and repetition rate. The University of Padova's research group is developing an integrated optics system for the QKD protocol; they are using a Sagnac interferometer with intensity and polarization modulators to manage photons correctly for encryption. Due to the system's inherent losses, the idea is to generate multiple photons using the photon source and then control the beam attenuator to achieve single photon precision. Instead, the Pisa research group is focusing on the diode's packaging; once the photon source is implemented, it is critical to transmit photons via the appropriate channel, which could be optic fiber or free space. Instead, Politecnico di Milano is in charge of designing a custom electronic integrated circuit capable of driving the diode correctly in all conditions and meeting all required specifications.

From the QUASIX project comes this thesis work, developed in the I^3N laboratory of the electronics department of the Politecnico di Milano, which aims to validate the custom driving chip realized in integrated CMOS technology dedicated to driving the single photon source, continuation of the previous thesis work of Fabio Olivieri and Luca Orsenigo [17, 18], whose work will be summarized in the next chapter.

2 | Cryogenic Driver for Single Photon Source

This chapter will provide an overview of the work completed in the previous theses [17] [18] and the obtained results, with the goal of introducing the key concepts necessary for comprehension of this thesis work and clarifying the starting point from which the work was continued.

2.1. Electronics specifications

To conduct an effective design, the following specifications had to be followed. To facilitate testing of the single-photon source, a wide driving voltage range of 0-5V was chosen, as determining the optimal polarization to apply to diodes at various temperatures requires conducting separate experiments.

In the past, electroluminescence spectrum measurements were made with exploring different bias values to assess the optimal polarization condition compatible with the power limits imposed by the CMOS technology available for the project. Although no emission has been observed in direct polarization, electroluminescence peaks became increasingly prominent only in reverse polarization and at voltages less than -3V, arousing interest in using these diodes in these bias conditions. As a result, the power supply voltage for the driving electronics was chosen to maximize the dynamics allowed by the used CMOS technology, which is 5V.

The pulse duration is important; in fact, it must be brief in order to limit the amount of time the detector, which is typically an *Avalanche PhotoDiode (APD)*, remains lit for photon acquisition. This is because APDs have intrinsically low dark counts, which increase with the duration of the photon detection time window. Dark counts are the primary source of detector noise, and it is essential to minimize their effects.

The pulse duration has an effect on the photon emission as well. As in the previous specification, a short pulse is advantageous in this case because it is necessary to limit the

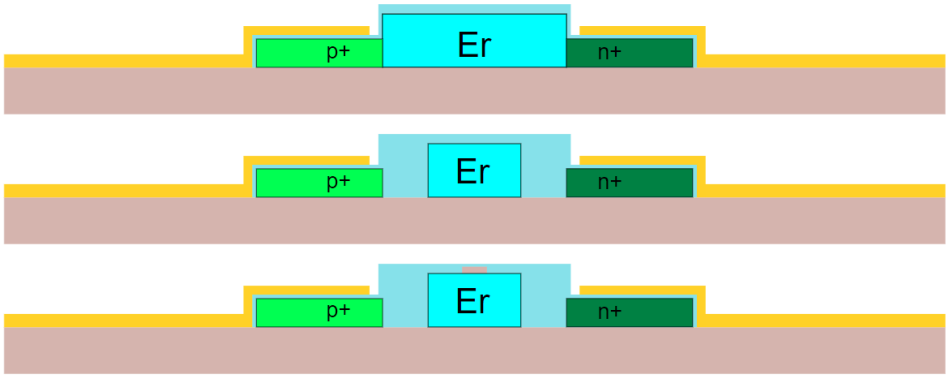

Figure 2.1: Three test structures designed by the CNR's research group.

number of photons emitted by the source so that the optical attenuators can reduce the photons sent by the pulse to an average value of 1, thereby preventing information theft. Additionally, the Sagnac interferometer's operation is based on the possibility of using two distinct two-pulse phase modulations that travel in opposite directions during the same cycle; longer pulses would require longer fiber networks, which is not easily implemented in an integrated system.

As a photon source, a good substitute for low emission regime lasers for commercially available QKD systems is erbium-doped diodes. In the past, the implantation of erbium atoms in silicon was used to attempt stimulated laser light emission, but these experiments failed due to the low emission power achieved. This is why erbium-doped silicon diodes have been used rather in the realization of integrated photonic systems with low photon emission [9]. In addition, the $1550nm$ light output makes these diodes perfect for transmission in both optic fiber and free space.

By implanting erbium with oxygen on silicon, it is possible to create a n doped region, as erbium acts as a donor atom in this case. Thus, as illustrated in Figure 2.1, by implanting the p region adjacent to the erbium doped region, it is possible to create a diode that exhibits electroluminescence and that is similar to conventional diodes, in terms of electronic behavior. The square-shape erbium-doped regions of the various test devices, designed by the CNR's research group, have side dimensions ranging from the order of magnitude of a half micron to a hundred of μm.

Due to the lack of commercially available systems for driving diodes that operate over a wide temperature range and the requirement for a fully integrated design in order to have a compact system suitable for space applications, it was necessary to design a driver dedicated to the project's requirements using LFoundry's $150nm$ CMOS technology.

Concerning power consumption, there are not strict specifications. To provide a point of reference, consider that some front-ends for space applications dissipate approximately $10mW$ of power [22]. To make a rough estimate of the current required by the diode, the optical power required by the system and the characteristics of the device being developed by the CNR research team can be used as references. With a maximum optical power requirement of about $1\mu W$, obtaining this value over a pulse duration of 5ns requires pulses of approximately $40 \cdot 10^3$ photons, which must be compared to the active zone's $500 \cdot 10^3$ erbium atoms. With one atom of active erbium for every ten, and 100 electrons required for each photon emitted, currents of $100\mu A$ are required from the diode to complete the expected emission [18].

Temperature is another critical design parameter; indeed, the optical electroluminescence of photon sources varies with temperature, which is problematic because the optic emitted power must be kept constant in order to implement a reliable QKD protocol. As a result, the system includes a temperature sensor, which adjusts the driving voltage applied to the diode in response to the measured temperature. An integrated electronic temperature sensor may be suitable for the system; indeed, with a Micius orbiting time of 94 minutes and a larger than expected temperature range of $300K$, it is reasonable to assume a temperature change of $1K$ every $9s$, a very slow bandwidth in comparison to what electronics can achieve.

Finally, because the project is intended for space applications, the circuit must operate at low temperatures. As a result, and in order to test with liquid nitrogen, a minimum value of $77K$ has been chosen. Certain electronic operating parameters vary at cryogenic temperatures; for this reason, temperature range was a primary design constraint. To provide a quantitative overview of the project specifications, Table 2.1 lists the major project parameters and their recommended values.

Parameter	**Suggested value**
Voltage driving range	$0V - 5V$
Repetition Rate	$50MHz - 2GHz$
Pulse duration	$5ns$
Temperature	$77K - 300K$

Table 2.1: Table of project specifications.

2.2. Summary of Cryogenic Characterization of the Technology

The QUASIX project, which seeks to develop an optoelectronic system for quantum cryptography applications in space, requires electronics that can operate over a wide temperature range. Specifically, the fundamental specification demanded from the system's electronics is to provide proper driving of erbium diodes in a low photon emission regime between $77K$ and $300K$.

However, the operation of conventional CMOS technologies at temperatures considerably below $218K$ is rarely examined by semiconductor companies, which, due to a lack of economic interest in cryogenic applications, do not investigate the creation of circuital models that accurately describe the behavior of the technology when temperatures are very low. Indeed, the standard design kits provided by the major foundries for the design of integrated circuits on a specific technological process, known as *Process Design Kit (PDK)*, typically ensure accurate modeling of the devices implemented over a temperature range of $-40°C$ to $125°C$. As a result, if a circuit is to operate at temperatures other than those at which the validity of the offered circuit models is assured, it is important to characterize and model the CMOS technology that will be employed at those temperatures.

As previously stated, the electronics are implemented using a typical CMOS process with a technology node of $150nm$ provided by the company Lfoundry, for which 1.8V, 3.3V, and 5V devices modeled in the temperature range $-40°C$ - $150°C$ can be used. Due to the fact that the integrated system must operate correctly at temperatures considerably below $233K$ $(-40°C)$, it was necessary to integrate the given models with a special characterization of the technology at low temperatures, which was accomplished using liquid nitrogen.

It is critical to emphasize that, in a prior thesis work [17], the cryogenic characterization of the MOSFET devices was not performed across the entire range of cryogenic temperatures outside the ones covered by the available PDK models, but rather with a focus on 77K. This approach was chosen in order to generate models suitable for the most critical condition, as the major technological parameters of relevance exhibit a monotonous relationship with temperature.

2.2.1. The BSIM3v3 Model

Characteristics such as completeness, robustness, scalability, diffusion, experimental validation, longevity and effective applicability to the considered technology have been evaluated for the choice of the model. For this reason, and taking into account the low temperatures investigated, the choice fell on a model with a number of content of empirical fitting parameters and that was as much based on the physics of operation of the device, so that the variability of parameters at cryogenic temperature can be attributed to precise physical causes. Finally, the aim was to create a model that could represent an industrial standard of reference for modeling CMOS technology, without excessive descriptive information beyond the scope of this project.

Given its ten-year standardization and deployment of inside circuit simulators of the major integrated circuit design tools, as well as its widespread use, the *Berkeley Short-channel IGFET Model (BSIM)* was chosen [19]. The BSIM models were developed in response to the necessity to incorporate short channel effects caused by the constant scaling of the technologies into the major circuit simulators.

The cryogenic characterization was specifically designed to extract this model in the BSIM3v3 version, a compact model based on the device's physics that is optimized for the description of MOSFET transistor operation in all their possible operating regions.

The BSIM3v3 model is notable for its scalability and precision of the equations defining transistors behavior. This version employs a single set of parameters for all possible geometries and, in contrast to prior models, a single drain current equation is defined for all operating regions, removing the discontinuities that are present in the first models. Additionally, both the threshold voltage and substrate current expressions are improved over earlier versions.

Additionally, the BSIM3v3 also takes into account numerous physical phenomena that alter the operation of transistors as their size decreases. This is why BSIM3v3 is suitable for scaled technologies with channel lengths down to $150nm$.

Finally, because the BSIM3v3 model is based on the device's operating physics, it has become the industry standard for modeling technologies with channel lengths greater than about 100nm, because the parameters extracted for a given technology can be used to predict the behavior of future generations and the effect of scaling before the device is even manufactured. Based on these considerations, the BSIM3v3 model, despite its complexity and large number of parameters, proved to be the ideal model to use for the extraction of the technology's parameters.

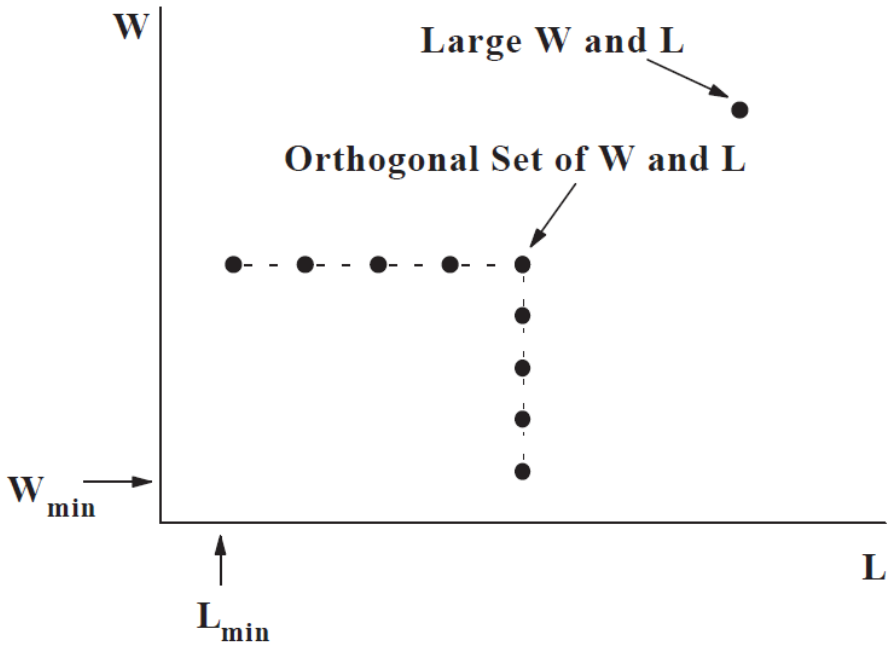

Figure 2.2: Required geometries for the BSIM3v3 model extraction [18].

2.2.2. Extraction prerequisites and definition of the implemented test

Transistors with a precise aspect ratio are required to implement the extraction of the BSIM3v3 model. As illustrated in Figure 2.2, the model's reference guide requires the use of a large device ($W = 10\mu m$; $L = 10\mu m$) to extract all parameters that do not depend on short or narrow channel effects (such as the body effect coefficients $K1$ and $K2$ or the ideal threshold voltage V_{T0} for large devices) and two sets of transistors with orthogonal form factors, one with fixed large W and variable L and one with fixed large L and variable W, used to extract parameters related to short and narrow channel effects, respectively. Following these conditions, the measurements were conducted at $1.8V$ and $5V$ on 33 different transistors with channel length ranging between $0.15\mu m$ and $10\mu m$ and width between $0.5\mu m$ to $10\mu m$. These characterizations were carried out for both n- and p-channel devices.

To acquire the DC parameters, four distinct drain current measurements had to be done for each of the given geometries, with the objective of obtaining two characteristic curves and two trans-characteristic curves under four different biasing conditions. Specifically, the four required measurements necessary are the following ones:

1. I_{DS} vs V_{GS} @$V_{DS} = 50mV$ for different V_{BS};
2. I_{DS} vs V_{DS} @$V_{BS} = 0V$ for different V_{GS};
3. I_{DS} vs V_{GS} @$V_{DS} = V_{DD}$ for different V_{BS};
4. I_{DS} vs V_{DS} @$V_{BS} = V_{BB}$ for different V_{GS}, where V_{BB} represents the maximum body tension applicable.

In the case of n-type transistors operating at $1.8V$, the four measurements were the following:

- Settings for I_{DS} vs V_{GS} @$V_{DS} = 50mV$ for different V_{BS} measurement are:
  - V_G sweep $0 \div 1.8V$, with increments of $25mV$;
  - V_S step $0 \div 1.8V$, with increments of $100mV$;
  - V_D step $0.05 \div 1.05V$, with increments of $100mV$;
  - $V_B = 0V$;
- Settings for I_{DS} vs V_{DS} @$V_{BS} = 0V$ for different V_{GS} measurement are:
  - V_G step $0 \div 1.8V$, with increments of $100mV$;
  - $V_S = 0V$;
  - V_D sweep $0 \div 1.8V$, with increments of $25mV$;
  - $V_B = 0V$;
- Settings for I_{DS} vs V_{GS} @$V_{DS} = V_{DD}$ for different V_{BS}; measurement are:
  - V_G sweep $0 \div 1.8V$, with increments of $25mV$;
  - $V_S = 0V$;
  - $V_D = 1.8V$;
  - V_B step $0 \div -0.4V$, with increments of $50mV$;
- Settings for I_{DS} vs V_{DS} @$V_{BS} = V_{BB}$ for different V_{GS} measurement are:
  - V_G step $0 \div 1.8V$, with increments of $100mV$;
  - $V_S = 0V$;
  - V_D sweep $0 \div 1.8V$, with increments of $25mV$;
  - $V_B = -0.4V$;

In the case of p-type transistors, identical tests were made, but all applied voltages were inverted due to differing doping and diffusion properties of the substrate. The same test flow has been used for the $5V$ transistors, with the applied voltage ranges increased to $5V$ and the sweep step increased to $50mV$ to maintain a measurement time comparable to that for the $1.8V$ transistors.

The next chapter will cover the structure and functioning of the measurement setup and the equipment used to get characteristic and trans-characteristic curves for each device evaluated under the appropriate bias conditions. After completing all necessary measurements, it is critical to have specific process parameters as starting data, such as the thickness of the oxide T_{ox}, the dopant concentration in the channel N_{ch}, and the depth of the junction X_j. Indeed, these values are used to establish the initial physical quantities for the extraction procedure.

2.2.3. Measurements results and MOSFETs' performances at Cryogenic Temperature

After a preliminary qualitative analysis of the measurements, it was demonstrated that the transistors function correctly at 77K. No anomalous effects, such as *kink effect* or *hysteresis*, emerged, as those effects are typically common at even lower temperatures and require specific modeling [7, 21]. For the objectives of deriving the parameters of the chosen model, the latter experimental evidence is critical. Indeed, because it lacks a model of such effects, it would no longer be appropriate for the intended objectives if these phenomena occurred.

From a practical standpoint, it should be emphasized that each device was also characterized at room temperature prior to the cryogenic tests in order to have comparison measurements at a standard working temperature ($300K$), as well as to validate the integrity and correctness of the tested devices before immersing them in liquid nitrogen.

When comparing the drain current measurements at the two temperatures, it was discovered that at $77K$ there is a $30 - 40\%$ increase in the drain current, which is mostly due to the increased mobility of the carriers and to the reduction of the threshold voltage of approximately $100mV$ compared to $300K$ operation.

2.2.4. Accuracy of the Extracted Models

The *Model Builder Program (MBP)* software, developed by the American company Keysight for the characterization and modeling of integrated circuits, was used to extract the DC

parameters of the BSIM3v3 model. The BSIM3v3 model at $77K$ was extracted using the software for all four types of tested transistors, both n-channel and p-channel, at $1.8V$ and $5V$.

The fitting of the experimental curves using the extracted model was achieved with an error that fluctuates around $2-3\%$ and reaches approximately 10% in the worst cases, according to the comparison between the experimental curves and the curves simulated with the obtained parameters, for each of the four types of transistors tested.

When comparing the experimental curves of an nMOS transistor at $1.8V$ with $\frac{W}{L} = \frac{10\mu m}{10\mu m}$ with the same curves obtained with the extracted model, the maximum error turned out to go from 2.5% in the measured trans-characteristic with $V_{DS} = V_{DD}$ to 3.3% in the measurement of the characteristic curve with $V_{BS} = -0,4V$.

The comparison of the extracted parameters V_{th0}, the ideal threshold voltage for a big transistor ($W = 10\mu m; L = 10\mu m$), and μ_0, the ideal mobility at the rated temperature considered, with the values provided by the models is also crucial.

In the case of $5V$ n-type transistors, the extraction gave values of $1.104V$ and $0.2214\frac{m^2}{V \cdot s}$ for the parameters V_{th0} and μ_0, respectively, whereas the values of the model supplied at room temperature are respectively $0.726V$ and $0.0505\frac{m^2}{V \cdot s}$, demonstrating that at low temperatures, mobility and threshold voltage increase, as expected from MOS operating physics.

2.3. Synthesis of the Driver and Temperature Sensor Design

In this paragraph, the design process and related simulations with corresponding outcomes of the QUASIX chip, developed in the preceding thesis [18] will be discussed briefly in order to explain the need for a new cryogenic probe and the results gained from subsequent measurements on the realized chip.

2.3.1. Temperature sensor

It is important to construct an integrated temperature sensor in order to properly detect the temperature of the photon source and control the driving action in accordance with the system's operating temperature range.

The operation of the temperature sensor is based on a *PTAT circuit*, proportional to absolute temperature. As a result, the sensor outputs a voltage signal that follows the

temperature trend of the chip based on a proportionality coefficient between the two physical values. This circuit often employs the parasitic BJT in trans-diode configuration, which is implementable with a standard CMOS process. Born from a CMOS process, these devices are not optimized to function as bipolar transistors; as a result, they have a low current gain β, with values close to the unit, and are hence referred to as parasites. A possible implementation of such a circuit involves the use of two transistors of *pnp* type; the PTAT signal is the ΔV_{BE} differential voltage generated by forcing two nominally equal currents, I_{BAIS}, on the emitter terminals and fixing bases and collectors to ground. The n-discriminating factor required to generate a non-nill ΔV_{BE} voltage between the emitter nodes of the BJTs must be placed in the inverse saturation current.

Starting from the emitter current expression of a *pnp* bipolar transistor it is possible to express ΔV_{BE} as:

$$\Delta V_{EB} = \frac{KT}{q} ln(n) \tag{2.1}$$

a simple solution that is particularly intriguing because of the linear relationship between ΔV_{BE} and temperature. The main drawbacks of this simple structure are the K/q coefficient of $86.3\mu V/°C$, which requires extremely accurate reading electronics, and n being inside a logarithm, thus having a low impact on the value of ΔV_{BE}, especially if, for reasons of power dissipation and occupied area, it cannot be too large. Clearly, enhancing the sensor's sensitivity by boosting the proportionality factor is a crucial aspect of this device's design. Moreover, according to the specifications, the sensor must ensure good rejection of power supply disturbances and reliability across the whole temperature range. To increase the value of the temperature coefficient to a reasonable order of $1mV/°C$ while simultaneously enhancing the applicable control over it, the PTAT signal can be converted and transferred to the output stage in the form of a current, to then be reconverted into an output voltage. This result can be achieved with two nearly symmetrical stages like the ones shown in Figure 2.3.

This stage, comprised of two current mirrors, forces the same current to the emitter nodes of both BJTs. Since the currents of M1 and M2 are same, their command voltages V_{GS1} and V_{GS2} are equivalent, and since $V_{G1} = V_{G2}$, so are their supply voltages V_{S1} and V_{S2}. This indicates that the voltage developed on the two emitters is transferred across the only non-symmetrical element of this stage, the resistor R_1, which converts the PTAT voltage into the current signal:

$$I_{temp} = \frac{KT}{q} \frac{1}{R_1} ln(n) \tag{2.2}$$

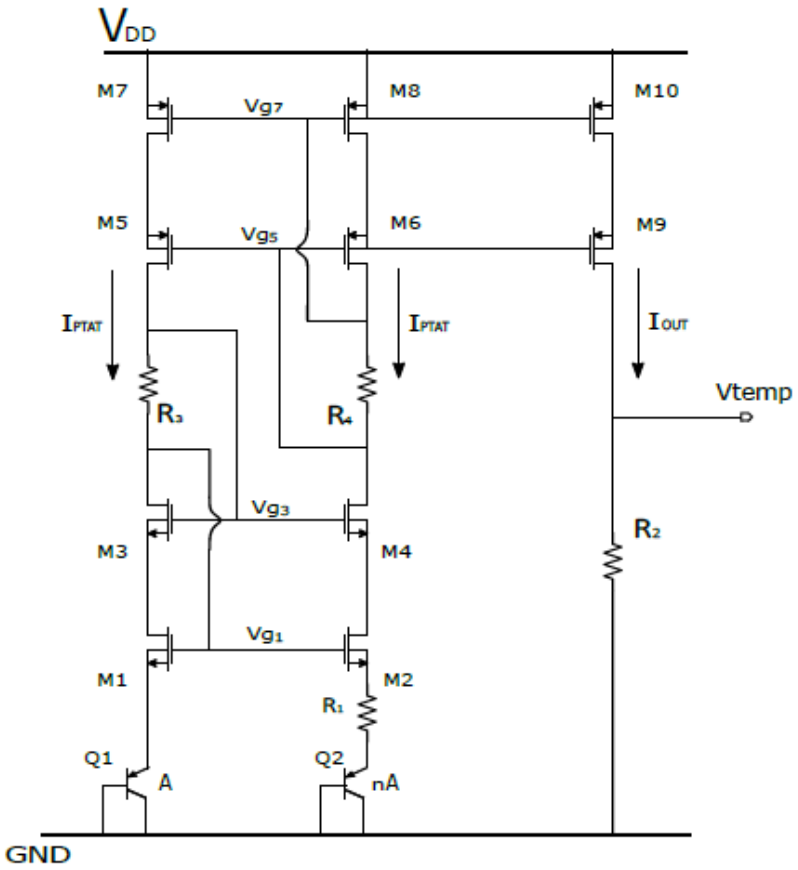

Figure 2.3: Illustration of the PTAT core.

The resulting current is subsequently mirrored at the second stage of the PTAT core, where it is transformed into voltage as it flows through the resistance R_2, whose expression becomes:

$$V_{temp} = \frac{KT}{q}\frac{R_2}{R_1}ln(n) \tag{2.3}$$

where the $\frac{R_2}{R_1}$ factor allows for more control over the proportionality coefficient value, and it does not introduce, albeit in a first approximation, any temperature dependence due to resistors variations, since it is expressed as a ratio. The chosen implementation adopts a $\frac{R_2}{R_1}$ ratio of 24 and a factor n equal to 4 to obtain a temperature coefficient of $2.87mV/°C$.

Since in self-biasing circuits the current does not depend directly from the biasing voltage, a bootstrap topology and a cascode structure were also introduced to reduce the effects of power supply disturbances, along with a start-up circuit, which is required in these types of structures to inject sufficient initial current and drive the circuit into a stable working point. Overall, this solution avoids the need for additional biasing voltages, but it becomes necessary the introduction between the two cascode mirrors of two resistors

R_3 and R_4 of $53k\Omega$, one per side, each to maintain the correct biasing conditions for the various transistor. The sizing of transistors and resistors was carried out taking into account the need of a minimum overdrive voltage of $100mV$ at low temperatures, and the fact that the PTAT current is itself the bias current and thus susceptible to variations along the temperature range. To accomplish this, transistors were sized with low form factors, and two switches were added over R_3 and R_4, now of $100k\Omega$ each, while two additional resistors, R_5 and R_6 of $53k\Omega$ each, have been put in series to the previous ones. As a result, at 77K $\Delta V_R \geq V_{OV}$ is ensured because the reduction in current at low temperatures is counterbalanced by an increase in the same resistances, and, at $27°C$, all transistors operate in saturation region thanks to the bypassing of R_3 and R_4 actuated by the switches.

The temperature sensor also consists of an output buffer, a classical two-stage single-ended OTA with Miller compensation adopted to decouple the PTAT core from its load so as not to alter the gain of the temperature coefficient during the reading phase and to provide a low impedance voltage reading. A full transistor approach was adopted to set a consistent bias for the buffer rather than a simple resistor placed in the current mirror's reference branch in order to compensate for temperature-related variations. Also, the V_{G1} node of the PTAT core was chosen as a reference voltage for the buffer in order to avoid the introduction of other blocks to generate a voltage and because it exhibits a linear dependence on temperature with a coefficient of $-1.56mV/°C$, a negative slope that overcompensates the positive one of the temperature-dependent threshold voltage, resulting in a current reference that presents a 23% positive variation at 77K compared to room temperature.

In order to improve the frequency response of the buffer, which depends on temperature-sensitive parameters, such as the transconductance of transistors and the equivalent output resistances of the two stages, a switch was added over R_N to have a selectable value for the Miller resistance, as it can be seen in Figure 2.4. At cryogenic temperatures, by lowering Miller's resistance to $1k\Omega$ the zero of the buffer is moved to higher frequencies, to compensate for its drop caused by to the increased transconductance of the output transistor. Conversely, at room temperature the switch is disengaged and the equivalent R_N becomes $5.8k\Omega$. Moreover, to increase the reliability of the structure, a $5k\Omega$ resistor was inserted after the buffer to decouple the second pole of the OTA from an eventual capacitive load, such as the connection to a PAD, which would shift the second pole of the buffer to lower frequencies, degrading the margin phase and thus the buffer's stability.

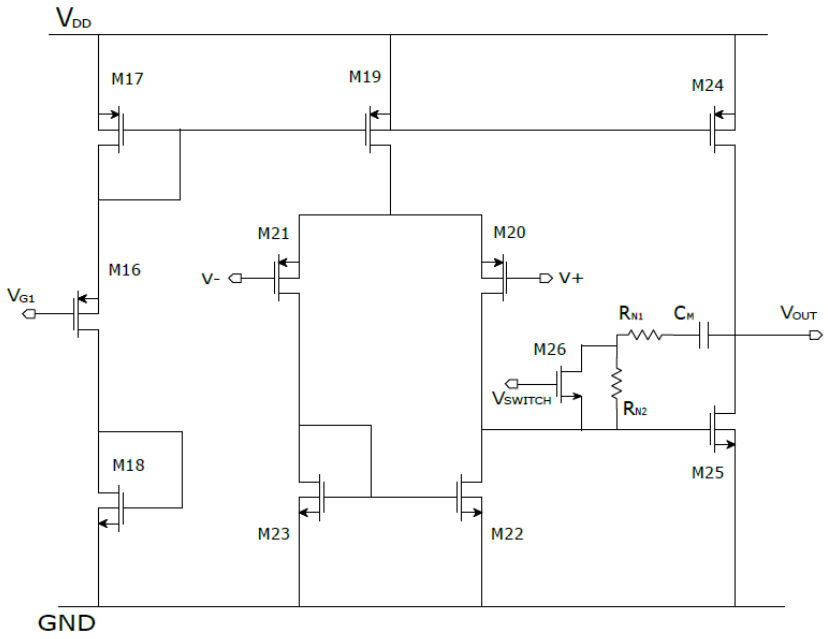

Figure 2.4: In this illustration of OTA utilized in buffer configuration, it is possible to observe the switch used to adjust the Miller resistance value.

2.3.2. Simulations results

Starting with the PTAT cell, the selected sizing of the components resulted in $137.25\mu W$ of dissipated power at $27°C$ and 5V biasing voltage. Regarding the factor n, it was decided to employ 4 BJTs in parallel to achieve $n = 4$ and $ln(n) = 1.386$, as the adopted technology does not allow for the emitter area to be sized. In the temperature range of $-40°C$ to $40°C$, the output voltage of the PTAT temperature sensor follows a linear trend with the temperature coefficient $k = 3.04mV/°C$. Using this temperature coefficient to extrapolate the value to 77K yields a voltage of $V_{temp|77K} = 222.2mV$, which only differs by 4.68% from the value of $232.6mV$ obtained from a point simulation at 77K.

With the selected component sizes, a PSRR of 45dB was obtained, and the noise spectral density at the output of the PTAT core was $987\mu V/\sqrt{Hz}$ at $f = 1Hz$ and of $1\mu V/\sqrt{Hz}$ at $f = 1MHz$, which is acceptable for the application in which this sensor will be used due to the low rate of temperature changes that permit digital filtering. A Montecarlo analysis on mismatch yielded an output standard deviation of $122.9mV$ attributable primarily to the mismatch of the transistors of the current mirror structure. Furthermore, such a mismatch together with inherent asymmetry of the structure could, in principal, result in a ΔI_{PTAT} that, when amplified by the same factor R_2, produces a non-negligible offset at the output of the PTAT core. However, this issue might be resolved during the phase

of calibration. From a further 1000-point Montecarlo analysis concerning both process and mismatch variations, with the aim to check the reliability of PTAT core and to find eventual malfunction conditions, the PTAT output voltage resulted to be linear with temperature, even in the six unfortunate cases in which some transistor was operating in ohmic regime.

Regarding the start-up circuit, the transistors have been dimensioned to ensure that the structure may initiate the bias of the PTAT core and then turn off. It was simulated with transient analysis both at $27°C$, with a Montecarlo simulation over 1000 points, and at 77K, always demonstrating the ability to start-up the circuit and subsequently shut-off in the expected manner. The main disadvantage of such a simple arrangement is that, under steady-state conditions, a current of $42.5\mu A$ flows through the inverter, dissipating $212.5\mu W$. This is not a significant disadvantage, however, because there are no severe specifications about the power dissipated. In the end, the output buffer OTA was designed to deliver a current of $9.3\mu A$ and $39.1\mu A$ at room temperature from the first and second stages, respectively, which, when combined with the $5.5\mu A$ of the biasing network, results in approximately $270\mu W$ of dissipated power. At 77K, the currents supplied by the two stages increase to $11.9\mu A$ and $52\mu A$, respectively.

The OTA has been compensated to be stable in buffer configuration with a capacitive load of 10pF and decoupling resistance $R_{out} = 5k\Omega$. At 27ºC, a 1000-point Montecarlo simulation yielded a worst case phase margin of 69° and GBWP of 1.16MHz, while at 77K, a phase margin of 75.22° was obtained at a GBWP of 3.29MHz, with a gain margin of 30db, which was previously a critical parameter at 77K. The simulated noise is completely negligible with respect to the one of the PTAT core, in particular values of $15\mu V/pHz$ at $f = 1Hz$ and of $89nV/pHz$ at $f = 1MHz$ have been obtained. From the analysis of the Montecarlo simulations on the offset at 1σ, it turns out to be $2.49mV$. In conclusion, with a simple design has been implemented a reliable temperature sensor, which meets the service requirements for the driving circuit.

2.3.3. Driver amplifiers

To implement the high and low driving voltages, two DACs are utilized, which alternately apply the two voltages to the Erbium-diode at a desired rate and pulse duration. In order to fully exploit the 5V dynamic range of the DACs, rail-to-rail amplifiers were utilized in the output stage. Their design reflects the necessity to meet the requirement of 5ns pulses with a minimum repetition rate of 50MHz, to ensure rapid pull-up and pull-down phases.

R-2R topologies convert the digital inputs of the DACs into currents entering the virtual

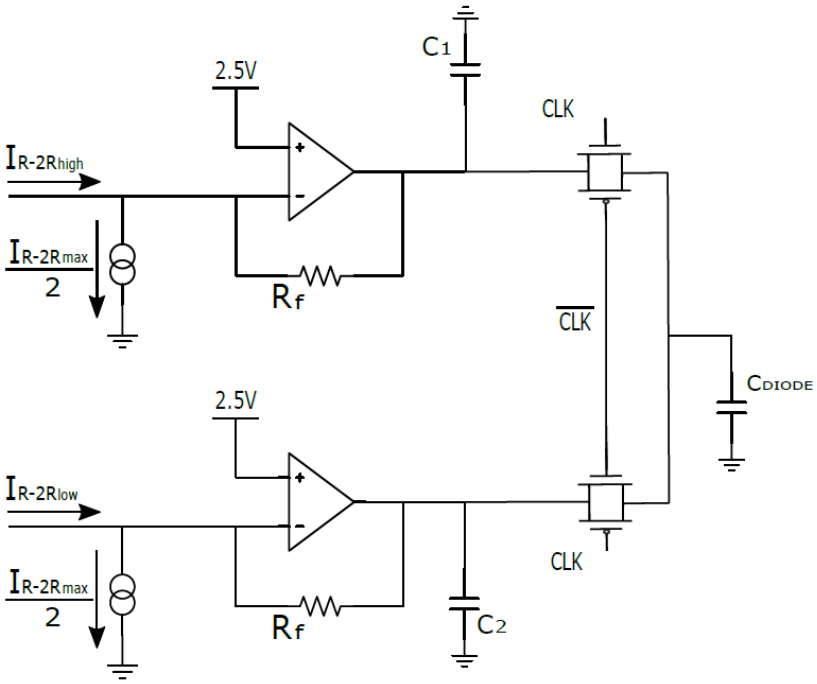

Figure 2.5: Illustration of driving architecture with switched capacitors.

ground input nodes of the amplifiers. A portion of this current is drained by current generators added at the negative inputs in order to match the output dynamic range to the positive input voltage set to $\frac{V_{DD}}{2}$. The feedback resistors were designed such that $I_{R-2R|max} \cdot Rf = 5V$, where $I_{R-2R|max} = 400\mu A$ represents the network's maximum current. These design choices are at the expense of more dissipated power and more current at rail-to-rail output stages when I_{R-2R} is less than the current drained from current generators, but they eliminate the need to implement a rail-to-rail input stage, which would have been extremely challenging to implement across the wide temperature range required by the project.

To allow for 5ns pulses with a duration of 20ns and a dynamic range of 5V, the Figure 2.5 switched capacitor structure was added to supply the diode with the necessary charge. The structure is made of two capacitors which are recharged by amplifiers. This configuration has the benefit of reducing charge and discharge times of the diode capacitance because it bypasses limitations such as slew rate, bandwidth, and output resistance, while simultaneously reducing the current at the rail-to-rail outputs to a nearly constant value equal to the average current of the load (maximum value of $\sim 1.25mA$ given by the charge/discharge of the capacitance at the output node). The drawback of the resulting architecture is that the final voltage applied to the diode is the result of a capacitive divider due to the sharing of charges between the diode capacitor and the added capacitors.

A value of 100nF was chosen for C_{ext} in order to have a maximum error on the voltage applied to the photon source of $\Delta V = 249.99\mu V$, considering maximum voltage dynamic range of 5V and a total load capacitance of $5pF$.

Given that the diodes to be examined could achieve a pulse rate of less than 1MHz, a simple and compact structure similar to the one in Figure 2.5 but without the two external capacitors was designed. A *class AB output stage* with output transistors connected in a common-source configuration was also required to optimize the utilization of the supply voltage and supply current, as well as to provide a constant input gm. It uses two translinear loops to perform class-AB action and set quiescent currents at the output stage, which are controlled by a feedback configuration of the stage to prevent the output voltage from saturation at one of the two biasing voltages. In conclusion, the output is cascaded at the first differential stage, but to avoid a three-stage structure that typically has lower gain and greater noise, the class-AB control stage is merged into the cascode branch, resulting in a conventional two-stage OpAmp.

Two driving architectures were implemented, both based on the same topology of rail-to-rail amplifiers, differing only in transistor size and compensating structure. One with better performance but at the expense of two added PADs and external capacitors, referred to as "Switched" and a fully integreted compact one that can nevertheless reach pulse frequencies on the order of 1MHz, referred to as "Fast". The solution with external capacitors does not require the classical Miller compensation because, due to the high value of the load capacitors, what would have been the second pole, given by $R_{out}C_{out}$, becomes the dominant one, making the pole given by the output resistance and output capacitance of the first stage (R_{eq1} and C_1) the second pole. However, it is notably sensitive to specific output voltage transitions that result in an increase in R_{eq1} and a shift of the second pole to lower frequencies, thereby reducing the phase margin, a circumstance that does not affect the stability of the Miller compensation solution because the dominant pole would decrease in frequency without degrading the phase margin. In "Switched," these issues have been resolved by adjusting the size of the transistors in use so as to shift the second pole to higher frequencies.

2.3.4. Simulation and results

Similar to the temperature sensor OTA, the V_{G1} node serves as the polarization reference node. At 300K, the current at the input stage's tail generator is $43.3\mu A$, while $64.2\mu A$ flows through the class-AB control branches. At 77K, these values become $43.8\mu A$ and $79.3\mu A$, respectively. The currents for the "Switched" solution are $82\mu A$ and $102\mu A$,

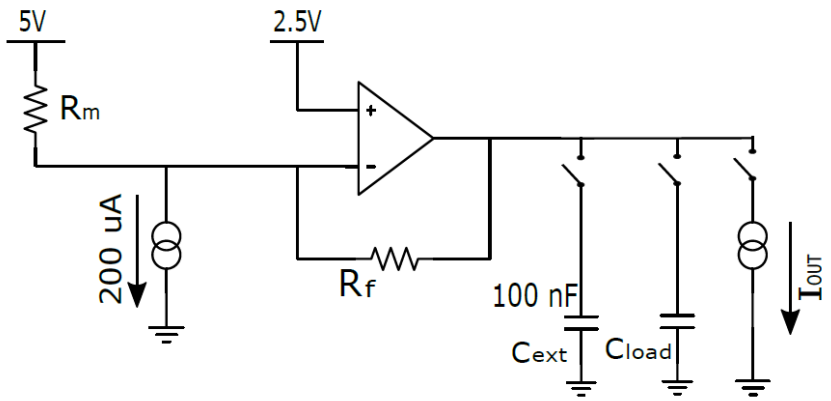

Figure 2.6: Illustration of the implemented structure for simulation.

respectively, due to the above-mentioned differences in size. At 300K, the DC gains for "Switched" and "Fast" are 88.67dB and 80dB, respectively, falling to 76.6dB and 70.8dB at cryogenic temperatures. It is interesting to note that the DC gain falls at the extremes of the output dynamics because one of the two output transistors is in ohmic regime while the other is off. With the applied sizing , a PSRR of 72dB and a noise of $22\mu V/Hz$ at $f = 1Hz$ and $54.6nV/Hz$ at $f = 1MHz$ at room temperature are likewise obtained, while a Montecarlo simulation on the offset yielded a value of $320.5\mu V$ and a standard deviation at 1σ of $2.96mV$, which is less than an $LSB = 4.8mV$.

All simulations have been performed on the architecture of the final application, as depicted in Figure 2.6, in which we find the equivalent resistance of the R-2R network, for simulations of different input codes, as well as a capacity and an output current generator, elements that permit simulations under different capacitive load and injected current/drained output conditions. For both architectures, the OTAs kept the output voltage variation below the 10% of the dynamics for current injected/drained of $4mA$, and these performances increased at 77K. For the "Fast" architecture, a phase margin of 70.42° with a GBWP of 4.34MHz at 300K and a phase margin of 67.2° at a GBWP of 8MHz at 77K are obtained with a capacitive load of 5pF. Instead, for "Switched" solution with just the 100nF load, a phase margin of 88.46° and 88° at a GBWP of 17.8kHz and 40.15kHz are respectively obtained at 300K and at 77K. For the "Fast" architecture, a simulation with variable capacitive load, which would be pointless for the "Switched" one because a capacitive load of a few pF is negligible, and a fixed output of 2.5V revealed a phase margin of 45° for a 33pF capacitive load. By varying the output voltage, a minimum phase margin of 56° was obtained for an output voltage of 4.6V at 300K and a minimum phase margin of 50.3° was obtained for an output voltage of 4.68V at 77K. In either instance, the "Switched" solution has a phase margin of more than 85° at both

ends of the temperature range.

System stability was simulated with V_{out} at 2.5V and C_{load} at 5pF, as the injected/drained output current varied. The "Fast" amplifier shows an overall better phase margin for increasing drained current values, instead the "Switched" OTA shows a phase margin of 45° in case of injected currents of $555\mu A$ at 300K and $1.13mA$ at 77K, current values high enough not to constitute a problem. Differently designed, the two structures display entirely distinct transitory responses. Focusing on the "Fast" variant, the performance is limited by the OTA's slew rate, bandwidth, and time constant, which is the product between the C_{out} closed loop output resistance. At room temperature, taking initially in analysis a single pull-up circuit and modeling the output of the stage and the relative capacitive load of the diode, the three phases of the transient can be distinguished more easily: in the first phase, the charge accumulated on Miller capacitance is transferred directly to the diode. At this time, in the second phase, the Miller capacitance must recover the lost charge, so the response of an internal loop between the two output transistors and the class-AB control begins, followed by the third phase in which the global loop supersedes the smaller inner loop and completes the transient. In contrast, the pull-down phase does not exhibit this type of behavior because it presents a conventional left poles and zero response. The duration of the simulated pulses is 500ns, and their repetition rate is 1MHz. At full dynamic, pull-up and pull-down transients of signals are faster than those at half dynamic. At cryogenic temperatures, if the rise and fall times at full dynamic are comparable to the ones at 300K, it is conceivable to see faster pull-up and pull-down transients at half dynamic. Importantly, the rail-to-rail output covers a dynamic range from 22.7mV to 4.95V, allowing complete freedom in testing the diode structure doped with erbium.

In the case of switched capacitor design, rail-to-rail amplifiers must maintain the correct voltage on the external capacitors, which charge the diode's capacitance when the relative transmission gate is closed. The transient period depends solely on the time constant given by the product of the equivalent resistance of the transmission gate, which is around 60Ω, and the capacitance of the diode. The "Switched" solution is faster than the "Fast" solution, and at 77K it becomes even faster. This solution has a disadvantage in terms of output dynamic, in that OTAs cannot withstand the large currents required to maintain the steady-state voltage on external capacitors; hence, the equilibrium maximum voltage range is reduced. Using a pulse rate of 50MHz, a voltage dynamic range of 5V and a total load capacitance of 5pF as an illustration, the OTA must supply an average of $1.25mA$, which, when added to the $200\mu A$ sunk from the virtual ground node, results in $1.45mA$ injected current for pull up and $1.05mA$ injected current for pull down, bringing the

negative input node of the pull-up OTA to 2.276V while for the pull-down one to 2.545V. From an initial range of 14.95mV to 4.93V, the low and high driving voltages settle to 132.95mV and 4.77V, respectively, in steady state. Fortunately, for half the dynamic voltage in the output range, this impact results in a modest 40mV decrease in amplitude relative to the initial values.

2.3.5. Ancillary Electronics

Ancillary electronics is necessary for the digital input of the driving electronics to be processed and converted into a current signal that can be applied to the rail-to-rail operational amplifiers. Since 20 bits are required at the input (half for the "high" values applied to the diode and half for the "low" values), it was decided to utilize 10 Pads at 1.8V as digital input, and alternatively save the values in an array of flip-flops. A digital logic is applied to the stored values to turn the four most significant bits into a thermometric value, achieving more monotonicity with output static characteristics. After being transformed to 5V digital signals by level shifters, the 21 digital values acquired by each DAC then control the switches that determine the amount of current injected by the R-2R architecture to the output amplifier's virtual ground.

Given that each pad in the chosen technology measures $80\mu m$ by $120\mu m$, a substantial amount of silicon space is conserved. Indeed, even if 5V logic did not require level shifters, it would still be more convenient to adopt 1.8V input logic since the total area occupied by the digital circuitry required to save the phase and execute thermometric conversion is reduced by a factor of 2.8 when compared to 5V logic (which normally occupies 4 times the area of 1.8V logic). The fact that 1.8V digital cells are already implemented by LFoundry is a further benefit of this design, as it increases its reliability.

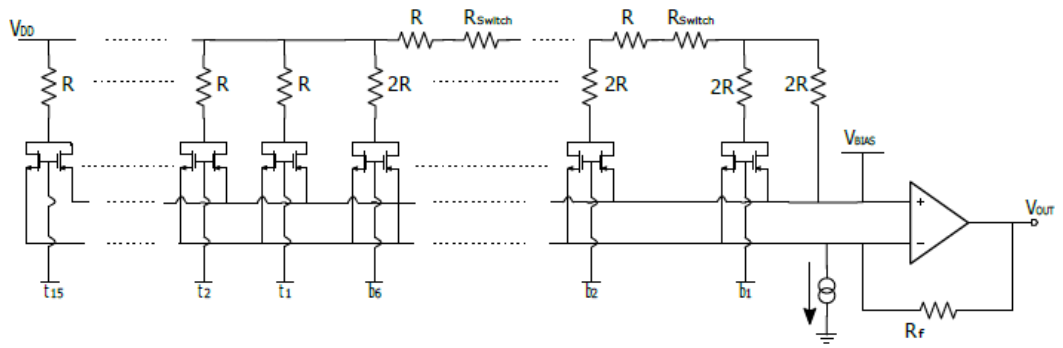

Figure 2.7: Illustration of the final structure made up by R-2R and thermometric networks.

To accurately address the two arrays of flip-flops that store "high" and "low" values, a "select" signal is used to indicate whether the values being saved are for the lower ("0") or higher ("1") output voltages, while the values at the input are recorded on the rising edge of the "save" signal. In order to improve the temperature stability and dependability of the cells, their set and reset ports have been fixed at 1.8V. The arrays of flip-flops are directly connected to the control logic that converts the 6+4 input bits into the 6+15 bits used to control the switches. This logic consists of six inverters and a four-input, fifteen-output thermometric decoder. In addition, because this is an inverting logic, the control signals of the switches are inverted relative to their inputs. Given that level shifters transform 1.8V digital signals to 5V before applying them to the gate of 5V transistors, both 1.8V and 5V transistors and power supply are necessary. Due to the increase in threshold voltage, the simulated discharge of the drain nodes of 5V nMOS transistors controlled by a 1.8V inverter at 77K resulted in commutation times on the scale of milliseconds rather than nanoseconds. This is the main weakness of such a construction. To address this issue, the width W of these transistors was changed from 0.8 to 4, resulting in switching times on the order of nanoseconds across the entire temperature range.

The intermediate stage of the driver consists of the resistive network, which is divided into two sections based on the encoding type, along with the switches and the current generator to the negative node of the rail-to-rail amplifiers, as it is shown in Figure 2.7. Regarding the resistive network controlled by the six binary bits, an R-2R structure was implemented. Its operating principle is based on a series of resistors in parallel that generates binary-coded currents. The initial current flowing from the supply through

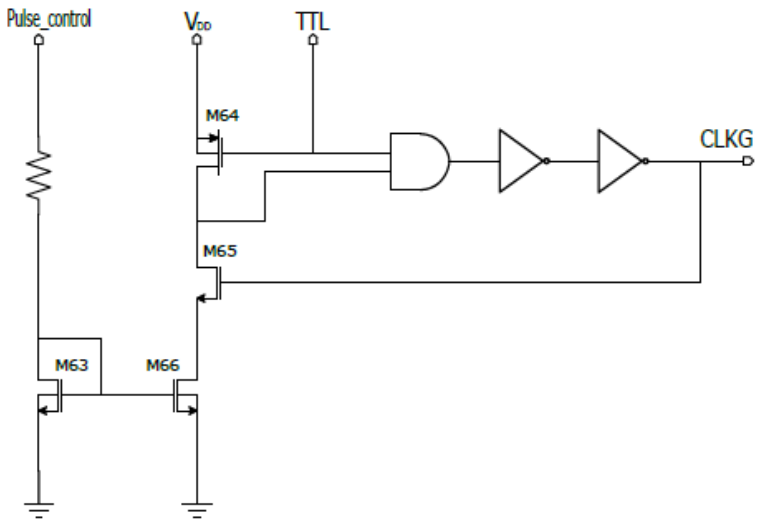

Figure 2.8: Illustration of the pulse generator structure.

the resistors divides in half at each bifurcation and, based on the binary code applied to the system's input, reaches the summing node, virtual ground, before proceeding to the output. This structure is especially favorable in terms of area occupancy, as it requires just 2n resistances in total. Each of the 15 thermometric bits resulting from the coding of the 4 input MSBs drives a switch, and each switch makes it possible to sink the same amount of current to the negative input of the OTA to ensure monotonicity at the expense of area occupation, as the total number of resistors required for this implementation is $2n - 1$, where n is the number of thermometric bits. With each increment of the code, the output current increases by one LSB. Considering b and t as the number of binary and thermometric bits, respectively, the total number of resistors required for this type of mixed structure is $2b + 2t - 1$, with each resistor set to $100k\Omega$ in order to limit the current at the negative input node of rail-to-rail amplifiers to $400\mu A$.

The current generator at the negative input pin provides the current required for the correct polarization of the voltage output, compensating for the temperature-related changes in this voltage. Such generator has been realized through the use of a single nmos and a resistor at the source of a value of $R_{source} = 125$, whose variations in value along the temperature range may be utilized to regulate the source voltage and consequently, also controlling the value of the gate voltage, the current. The gate voltage is given by the conventional biasing structure already developed for the OTAs biasing, while a rppolyhe technology resistance has been chosen as the source resistance to balance the overcompensation of the biasing branch and the corresponding increase in current. A crucial role in the polarization of the output voltage is also played by the feedback resistance, which was selected to be $13.44k\Omega$ so that at 77K it can compensate for the drop in the resistor network's current.

The pulse generation circuit, depicted in Figure 2.8, has been built to allow for easy adjustment of the voltage pulse duration delivered to the diode. The pulse duration might range from 5ns to 100ns and must be consistent across the entire temperature operating range. This circuit uses the delay periods of digital cells to generate nanosecond-scale pulses. Starting from an equilibrium condition in which the TTL signal is at "0", with M64 active and CLKG at zero, M65 deactivated, and the other input of the AND at "1", the TTL signal is then set to "1", resulting in the opposite condition for the two transistors M64 and, after the signal has been propagated to CLKG, M65. At this stage, the drain of the M65 is reduced in voltage until the AND port input threshold is crossed and CLKG is reset to "0". The duration of the generated output pulse is dependent upon the time necessary for M65 to discharge its drain node and the propagation time of the signal from the input of the AND gate to the output of the system. This simple topology is limited by

the maximum repetition rate of the pulses; hence, the TTL signal must remain at a high logic level until the generated output reaches a low logic level to turn off M64; otherwise, the case with both M64 and M65 enabled would exhibit an unpredictable behavior. In order to adjust the duration of the pulse, it is necessary to manage the sinking current from M65's drain. To do this, a standard current mirror with an externally controllable biasing voltage determines the maximum drain current of M65.

2.3.6. Final Architecture

The final architecture consists of two DACs for the "Switched" structure and two for the "Fast" structure. A specific digital input logic is shared by the DACs employed for a given "high" or "low" diode driving voltage. A pair of transmission gates, triggered by an external pad, controls the selection of "Switched" or "Fast"; their transistors are larger than those of other switches on the chip in order to introduce the lowest possible route resistance. As for the driving of the pair of transmission gates related to the choice between "high" and "low" output voltage, it can be provided by an external signal or by the signal of the pulse generator just treated, with the selection made by an extra pad labeled "Pulse/Clock." All switch pads that imply a setting selection, such as "Pulse/Clock" and the temperature sensor switch pad, are equipped with a pull-down resistor so that the default value of those pads is always "0".

Regarding power supplies, since some digital components of the circuit operate at high frequency and could, in theory, introduce disturbances to the analog component, which must drive the diode with high accuracy and precision, it was decided to separate the analog domain from the digital domain by utilizing two distinct ground signals, 5V power supplies, and 1.8V power supplies for the digital logic. Each macro section of the ASIC features external control pads to provide for maximum flexibility throughout the chip's testing phase and, if necessary, to adjust its electronic behavior. The signals brought outside the temperature sensor are those for controlling the switches ($V_{Switch_{PTAT}}$ and $V_{Switch_{OTA}}$), that set internal resistance levels for the PTAT core and the OTA Miller resistance, as well as the outputs V_{temp}, the output of the PTAT core, and V_{OUT}, the output of the buffer. In addition, in order to have control over the biasing voltages of the rail-to-rail amplifiers and the OTA of the temperature sensor, it was decided that the voltages V_{G1} and V_{BIASp}, the biasing voltage for pMOS transistors, may be controlled externally. I_{ctrl}, $I_{tail|FAST}$ and $I_{tail|SWC}$, source nodes of the tail transistor of the first stage of the temperature sensor's OTA and of the rail-to-rail OpAmps correspondingly, which are generally set to 5V, allow for direct gain and stability control of the entire stage. The diverse pads for the "Fast" and "Switched" solution enable users to deactivate one of

the two architectures while the other is active, hence minimizing disruption. The biasing nodes of the cascode structures, V_{mirror}, which permit direct actions on the OTAs' second stage, were located externally and short-circuited for all DAC amplifiers so that they all have the same voltage.

Regarding the rail-to-rail front-end polarization, it was decided to supply the resistive network with a different bias than the digital and analog 5Vs that supply the rest of the circuit, while the 2.5V at the positive input of the OpAmp is supplied directly from the outside. This was done to control the value of the LSB current and thus reduce the LSB voltage and dynamic range, thereby enhancing the accuracy of the driving electronics. In order to have a greater degree of control over the output voltage, two pads were added so that the gate voltage V_{BIASn} of the current generators at the inverting input node of rail-to-rails could be directly driven. A pad manages two gates associated with the current generators of the two amplifiers allocated to the "high" and "low" voltage outputs, respectively. The final configuration of the chip consists of 37 Pads, occupying a total of $1.217mm^2$. The arrangement of the pads was the limiting issue in terms of area occupation. In the lower portion of the chip is the input digital logic, on the left are the resistor networks and switches, the four rail-to-rail operational amplifiers are in the center, and in the upper portion is the temperature sensor.

The temperature was also considered during layout design, for instance, by taking into account at cryogenic temperatures phenomena such as the higher bulk resistivity, faced by increasing the area occupation of the connections to bulk, or the increase in mechanical-stress-induced mismatch due to a significant thermal expansion/contraction, for which dummy devices were placed at the ends of rows of interdigitated traces. Furthermore, in order to prevent the propagation of disturbances through the substrate of high-frequency digital electronics, digital blocks related to pulse generation have been isolated in Deep-Nwells (DNWELL).

Following the design, parasitism was extracted to bring simulations closer to reality. With the exception of the pulse generator, pre-parasitism and post-parasitism simulations contain few differences. More parasitic capacitances and equivalent resistances degrade pull-up and pull-down transients in the "Switched" architecture as a result of the addition of the two transmission gates, which allow for the selection between the two architectures. In addition to the "Fast" architecture, the produced driving pulses exhibit longer settling times and dumped oscillations when compared to simulations performed with an ideal surrounding system. This is as a result of the non-negligible equivalent capacity of the resistive network to the negative inputs of the amplifiers, C_{switch}, which adds a high frequency pole that decreases the phase margin, being close to the GBWP. The "Switched"

architecture, on the other hand, has proven to operate appropriately at all temperatures and voltages, ensuring functionality up to high repetition rates. C_{switch} has no influence on the architecture with switched capacitors because the feedback loop's GBWP is significantly smaller compared to the "Fast" structure.

In conclusion, the static characteristic of the DACs, simulations at both 300K and 77K have been performed to evaluate INL and DNL: it is possible to observe that at room temperature the first and last bits are ineffective, whereas at cryogenic temperatures all input digital codes are utilized, without reaching the bottom of the voltage dynamic range. DNL exhibits peaks at each multiple of $2^6 = 64$ and yields results less than 0.05LSB. Also INL exhibits a good characteristic, with a maximum value less than 2.5 LSB. In contrast, the system's dynamic characteristics make it ideal for a first stage of testing, particularly the switched capacitor architecture, whose performance is close to the state of the art.

3 | Cryogenic Characterization

As explained in the previous chapter, cryogenic characterization of the $150nm$ CMOS technology is a procedure to extract the parameters required to model the transistor behavior in its target operating temperature as close to reality as possible, ensuring a correct circuit design.

Indeed, the first modeling made in Fabio Olivieri's thesis [17] produced an accurate representation of the device's behavior, allowing for the design of a first circuit [18]. However, it was determined that this modeling, which took a specific set of MOSFETs into account, needed to be updated. By re-characterizing the transistors whose previous measurements were discarded as being deemed incorrect, due to an erroneous setting of the compliance value of the measuring instrument, and supplementing them with a new set of MOSFET devices with smaller form factors than the previous ones, the goal was to continue the characterization work begun previously in order to generate a more complete circuit model that was also easily usable on a standard circuit simulator for integrated circuit design, in anticipation of a future version of this chip.

Along with the characterization of the transistors, the poly-resistances of this technological node were also analyzed, as they were exposed to a punctual characterization at $77K$, exactly like the MOSFETs. In this case the characterization was used to account for the variability at cryogenic temperatures rather than to actually create a model.

It was also decided to characterize a device that is critical to the temperature sensor's performance, namely the parasitic BJT in trans-diode configuration that is present in the CMOS technology. The cryogenic characterization in this case was not restricted to the temperature of $77K$, but was performed over the complete cryogenic temperature range.

The measurement setup, on the other hand, has undergone structural changes in order to improve on numerous fronts the characterization of the BJTs. It was no longer sufficient to simply immerse the probe and the device to be tested in nitrogen; rather, a sampling study of the BJT's behavior at several points in the Operating Temperature range, corresponding to different heights above the liquid nitrogen level, was conducted.

Similarly to what happened with poly-resistors, the BJT characterization work was focused on comparing experimental results with simulations results given by the foundry's models in order to obtain a calibration of the integrated temperature sensor, rather than extracting the parameters of a model and inserting them into a circuit simulator as for the MOSFETs case.

3.1. Measurement Setup and Definition of the Tests

Before beginning the experimental measurements, it was necessary to mount the test chips provided by the company on special supports, which would allow the devices to be tested to be properly connected to the measurement setup used for the characterization. The samples used for this purpose are made up of matrices containing all of the different types of transistors available in the CMOS process, each accessible via dedicated pads.

On each row of these test structures, except the last one, an either n- or p-channel MOSFET with variable aspect ratio is placed. On this chip it is possible to select transistors with different L and same W, or similarly vary W for fixed values of L. In the last row, the access pads to the poly-resistances are distributed. The pads of the devices of interest

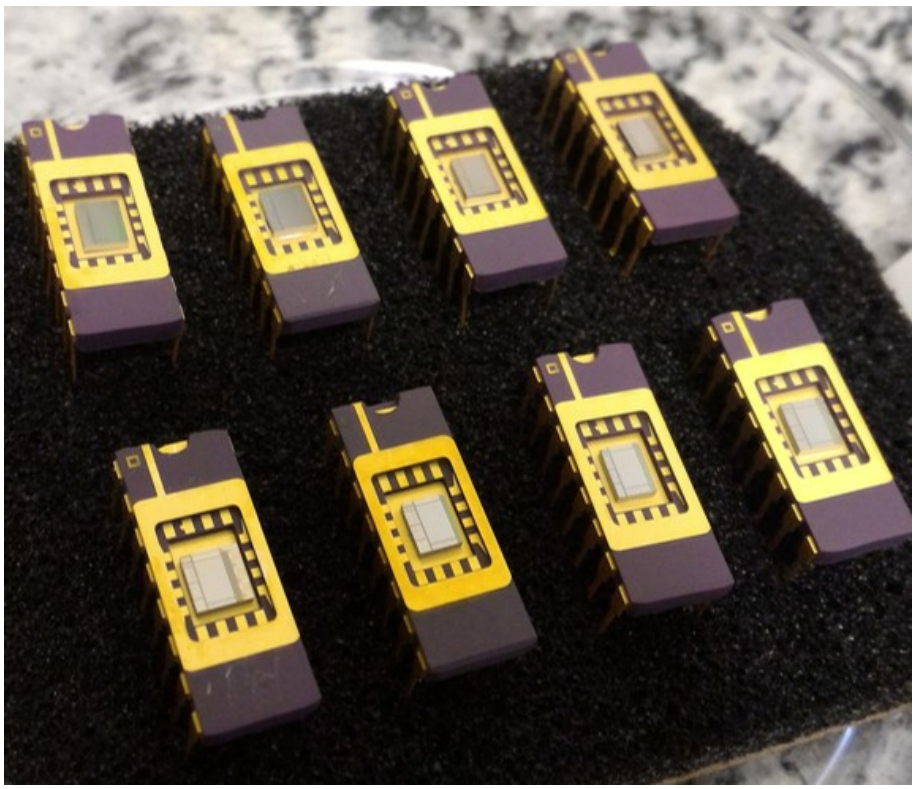

Figure 3.1: Picture of chips that have been mounted on the chip-carrier.

were bonded to ceramic Dual-InLine chip carriers, Figure 3.1.

The previously bonded samples used for the first characterization were reused for this second characterization after a visual examination under a microscope to ensure that the bonding wires corresponding to the devices to be remeasured were still all attached. The old samples with damaged bonding were remapped and bonded again. Table 3.1 displays the form factors of previously tested transistors as well as those that were added or remeasured during this phase.

Device	Type	Tested Aspect Ratios $[\frac{\mu m}{\mu m}]$
1v8lvt	nMOS	$\frac{10}{10}$ $\frac{10}{0.5}$ $\frac{10}{0.3}$ $\frac{10}{0.15}$ $\frac{2}{10}$ $\frac{1}{10}$ $\frac{0.5}{10}$ $\frac{5}{2}$ $\frac{2}{2}$ $\frac{0.32}{0.15}$
1v8lvt	pMOS	$\frac{10}{10}$ $\frac{10}{0.5}$ $\frac{10}{0.3}$ $\frac{10}{0.15}$ $\frac{2}{10}$ $\frac{1}{10}$ $\frac{0.5}{10}$ $\frac{5}{2}$ $\frac{2}{2}$ $\frac{0.32}{0.15}$
5v0rvt	nMOS	$\frac{10}{10}$ $\frac{10}{5}$ $\frac{10}{2}$ $\frac{10}{1}$ $\frac{10}{0.8}$ $\frac{2}{10}$ $\frac{0.8}{10}$ $\frac{5}{5}$ $\frac{2}{5}$ $\frac{0.8}{5}$ $\frac{0.8}{0.8}$
5v0rvt	pMOS	$\frac{10}{10}$ $\frac{10}{5}$ $\frac{10}{2}$ $\frac{10}{1}$ $\frac{10}{0.8}$ $\frac{2}{10}$ $\frac{0.8}{10}$ $\frac{5}{5}$ $\frac{2}{5}$ $\frac{0.8}{5}$ $\frac{0.8}{0.8}$

Table 3.1: Table summarizing the form factors of devices that have been previously tested (black), those that have been retested (green), and those that have been added (blue). Specifically, measurements were made at $1.8V$ with a low threshold voltage (marked by the term $1v8lvt$) and at $5V$ with a regular threshold voltage (indicated with the abbreviation $5v0rvt$).

The *Keithley 4200-SCS* instrument, an automated and programmable semiconductor characterization system capable of measuring I-V curves, was used to measure the characteristic and trans-characteristic curves of each device, tested under the bias conditions indicated in Paragraph 2.2.2.

The instrument is composed of four SMUs (Source Measure Units), which are measurement units capable of forcing and reading currents and voltages. Each SMU has the ability to sweep or step voltages or currents, as well as impose fixed bias values.

The measuring range of measurable currents extends from $105mA$ to $1pA$ for the SMU3 and SMU4, and down to about $1fA$ for the SMU1 and SMU2, which are equipped with an additional specific preamplifier to enlarge the measurement range, while voltages can be measured from $210V$ to $1\mu V$. The currents and voltages that can be forced instead

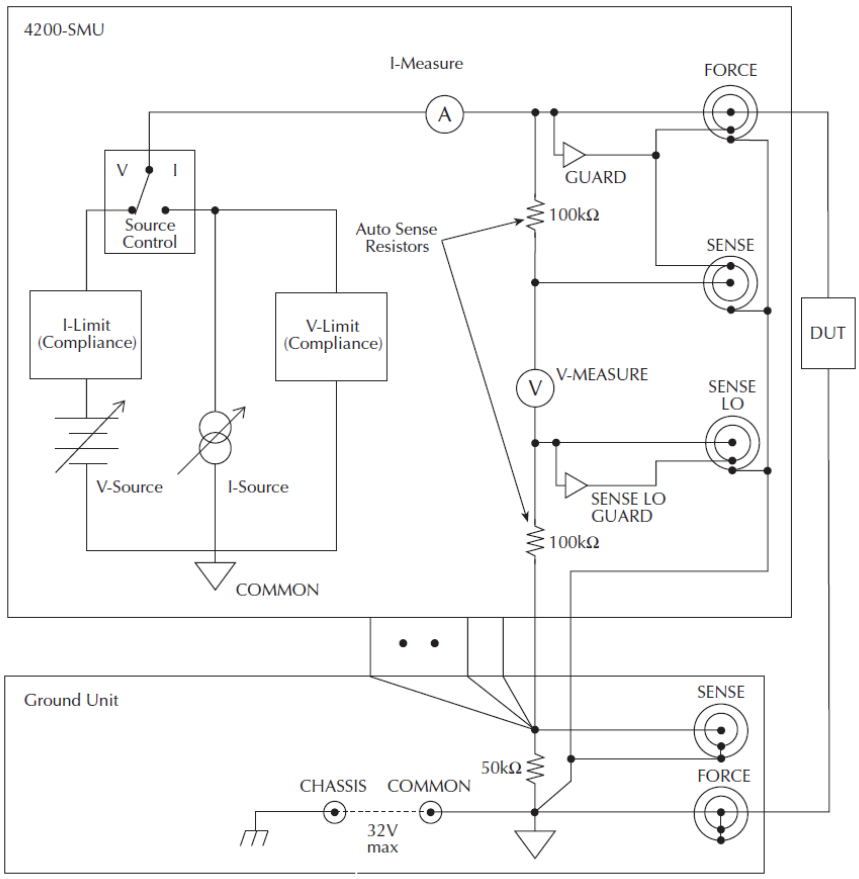

Figure 3.2: Internal diagram of an SMU of the measuring instrument. In the example shown, the DUT is connected between the force terminal and ground.

are included in the intervals $105mA - 5pA$ and $210V - 1\mu V$. Each SMU is made up of a voltage or current generator connected in series with an ammeter and in parallel with a voltmeter, as shown in Figure 3.2. The circuits labeled with V-limit and I-limit in Figure 3.2 limit the voltage or current to the safety value (*compliance*) established during the measurement test definition phase.

The Force and Sense terminals are triaxial connectors used to apply the Force or Sense signal to the Device Under Test (DUT). The signal, applied on the central pin of the triaxial structure, is surrounded by a double shield, one internal (guard) and one external connected to the instrument's ground. The innermost shield guard is driven by a voltage buffer set to the same value as the force or sense signal. It is used to eliminate the effect of leakage currents caused by the finite resistance of the insulator in the shielded cable that connects the DUT to the instrument, that may introduce significant errors in the measurement.

The packaged samples were mounted on specifically designed PCBs, to allow for an easier contact with the device's pads and connection to the measuring instrument via coaxial cables. Each terminal of a tested transistor was thus connected to an SMU of the instrument (in order from SMU1 to SMU4, the gate, drain, source, and bulk terminals were connected).

Each resistor, on the other hand, has three terminals, which are conventionally referred to as A, B, and SA, with SA being the substrate terminal. A current measurement was made for each of them by applying a voltage sweep to one of the pads to obtain the corresponding characteristic curve. Specifically, taking into account the three terminals, the measurement is: I_A vs V_B @V_A and $V_{SA} = 0V$ for V_B varying from $0V$ to $5V$ with a $50mV$ step.

The setup depicted in Figure 3.3 was used for cryogenic characterization. The chip, mounted on a special PCB and placed at the end of a probe, was placed inside a liquid nitrogen-filled dewar. The probe has a metal box at the opposite end of the sample with BNC connectors, each corresponding to a pin of the chip-carrier installed.

3.2. Experimental Results

Figure 3.4 reports, as an example, the experimental curves of the four measurements carried out on a $1.8V$ n-type transistor with $\frac{W}{L} = \frac{0.32\mu m}{0.15\mu m}$. The experimental characteristic curves are still those typical of a standard transistor, confirming the correct behavior of the

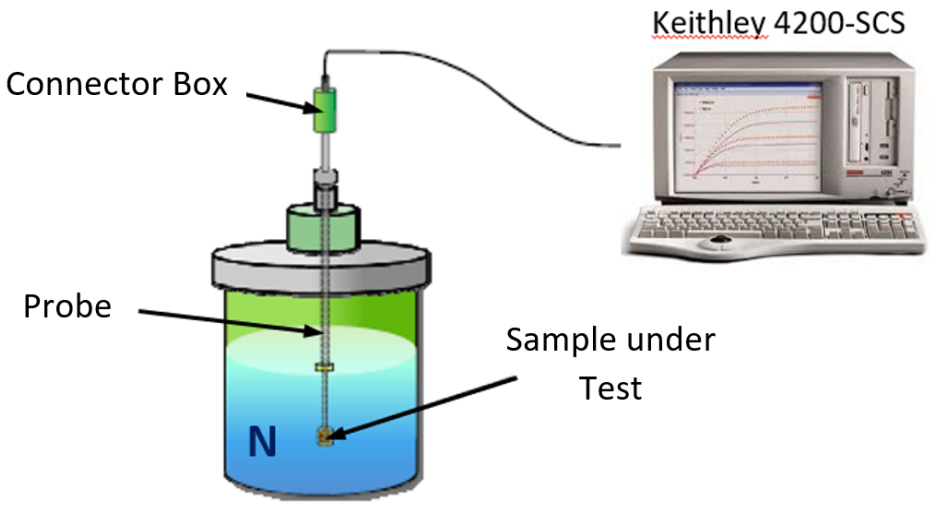

Figure 3.3: Illustration of the cryogenic characterization setup.

device at 77K. The same observations apply to each of the tested transistors, regardless of the type of device ($1.8V$ or $5V$), the type of channel (n or p) and the aspect ratio considered.

As proof of what has just been said, Figure 3.4 to Figure 3.11 are reported, showing the experimental curves of the measurement tests carried out for each type of tested device, both for transistors with large form factor and for devices with small W or L and for both types of channel (n and p).

As happened previously, for these devices as well, no anomaly effect has occurred, such as the kink effect or the hysteresis, which, as already explained, are phenomena that usually appear at temperatures that are even lower than $77K$ and which would require modeling that the BSIM3v3 is unable to provide.

3.3. Comparison between Room Temperature and Cryogenic Temperature

Since the same measurement test was also performed at room temperature for each measured device, it is interesting to make some considerations regarding the effect of low temperature on the functioning of the devices. For this purpose, Figure 3.12 shows as

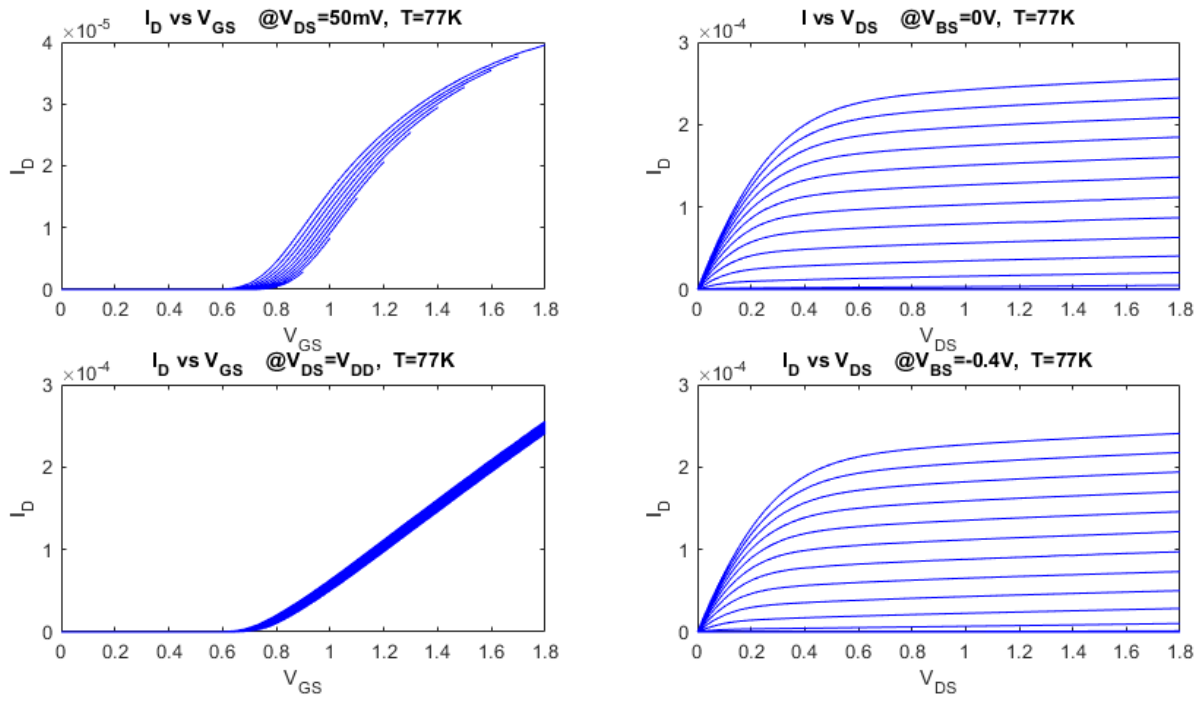

Figure 3.4: Measurements of a $1.8V$ nMOS transistor with $\frac{W}{L} = \frac{0.32\mu m}{0.15\mu m}$

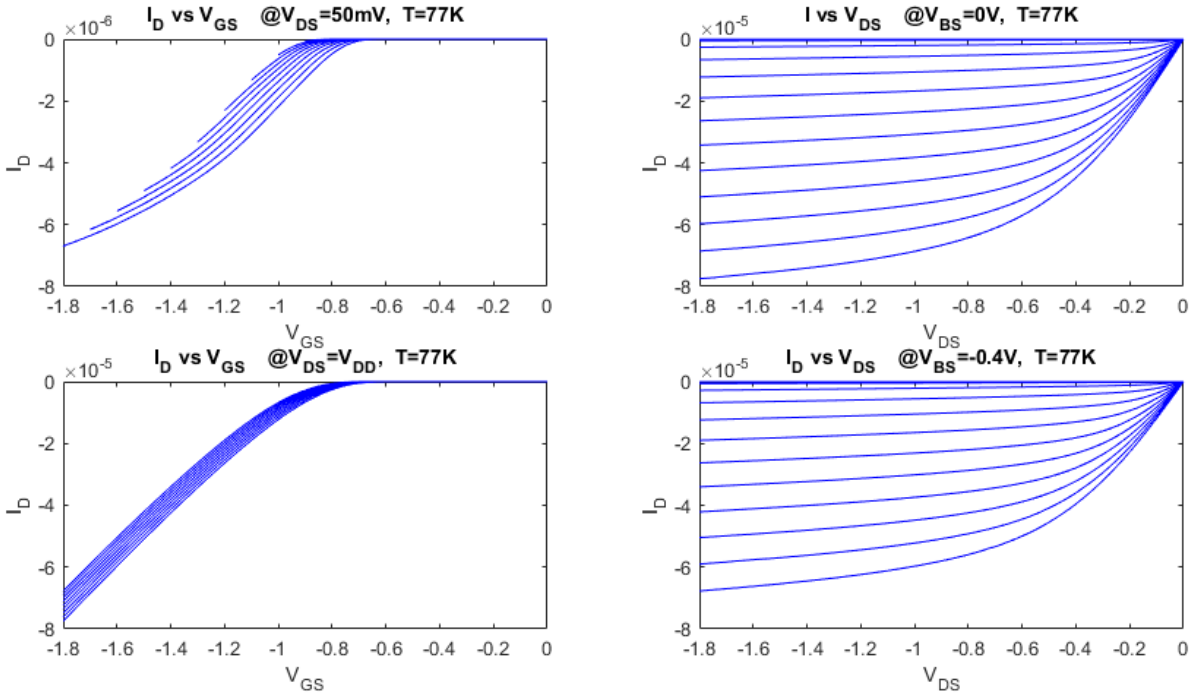

Figure 3.5: Measurements of a $1.8V$ pMOS transistor with $\frac{W}{L} = \frac{0.32\mu m}{0.15\mu m}$

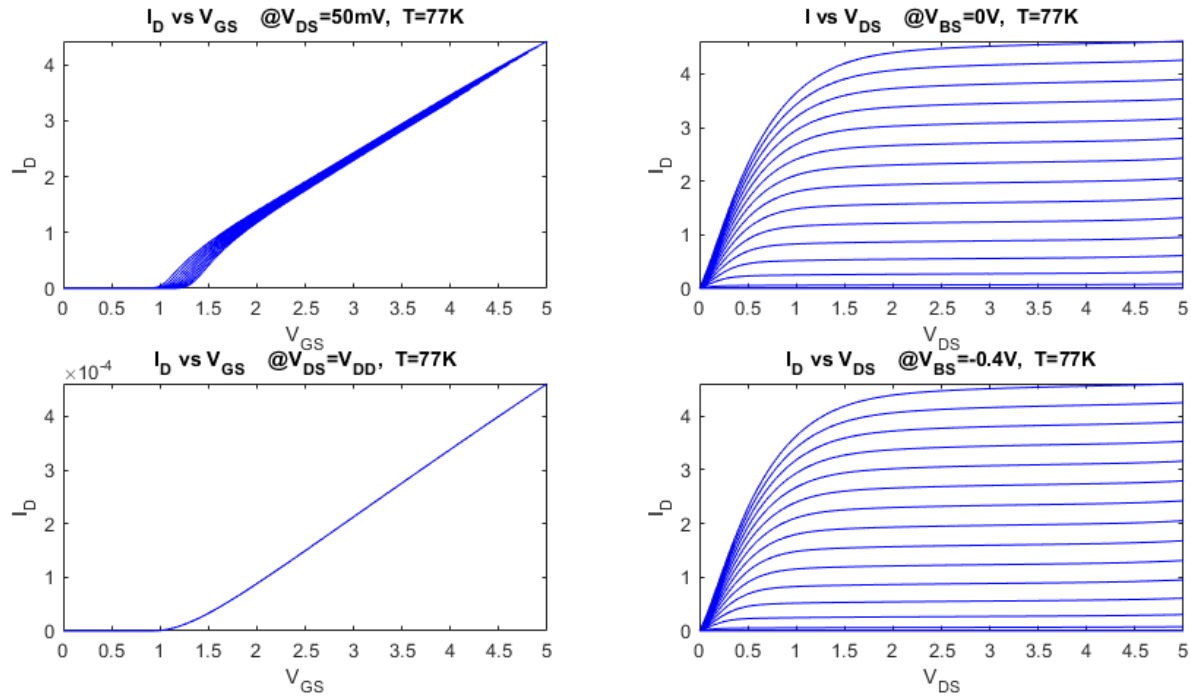

Figure 3.6: Measurements of a $5V$ nMOS transistor with $\frac{W}{L} = \frac{0.8\mu m}{0.8\mu m}$

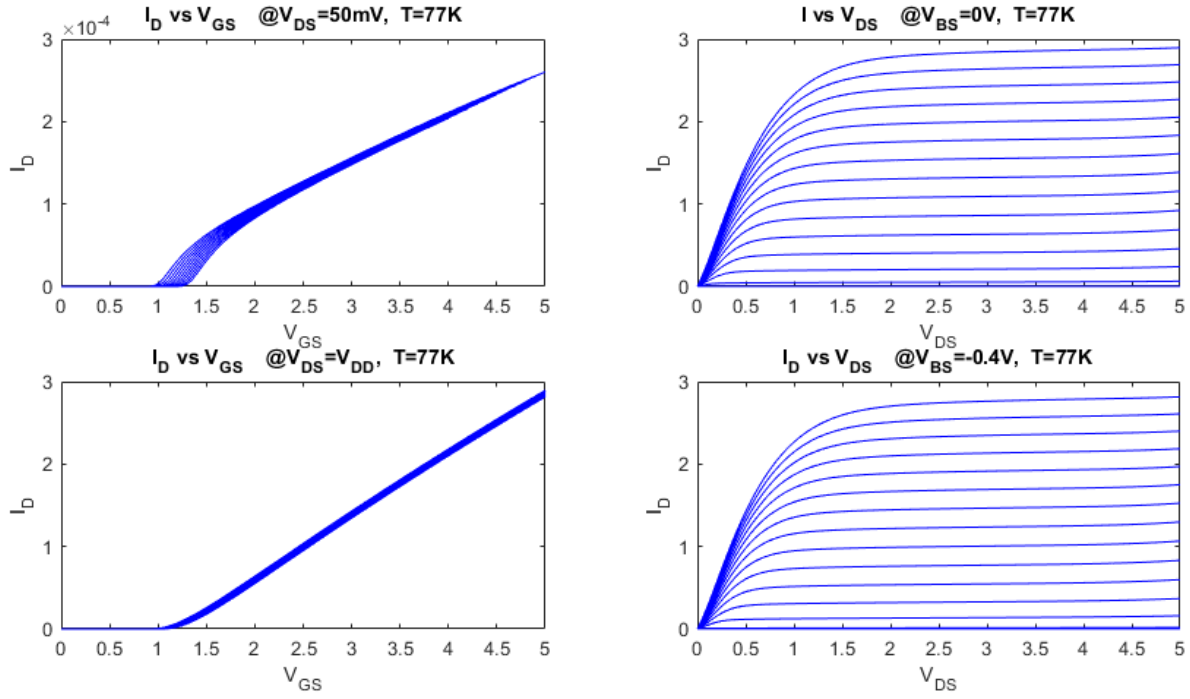

Figure 3.7: Measurements of a $5V$ nMOS transistor with $\frac{W}{L} = \frac{10\mu m}{0.8\mu m}$

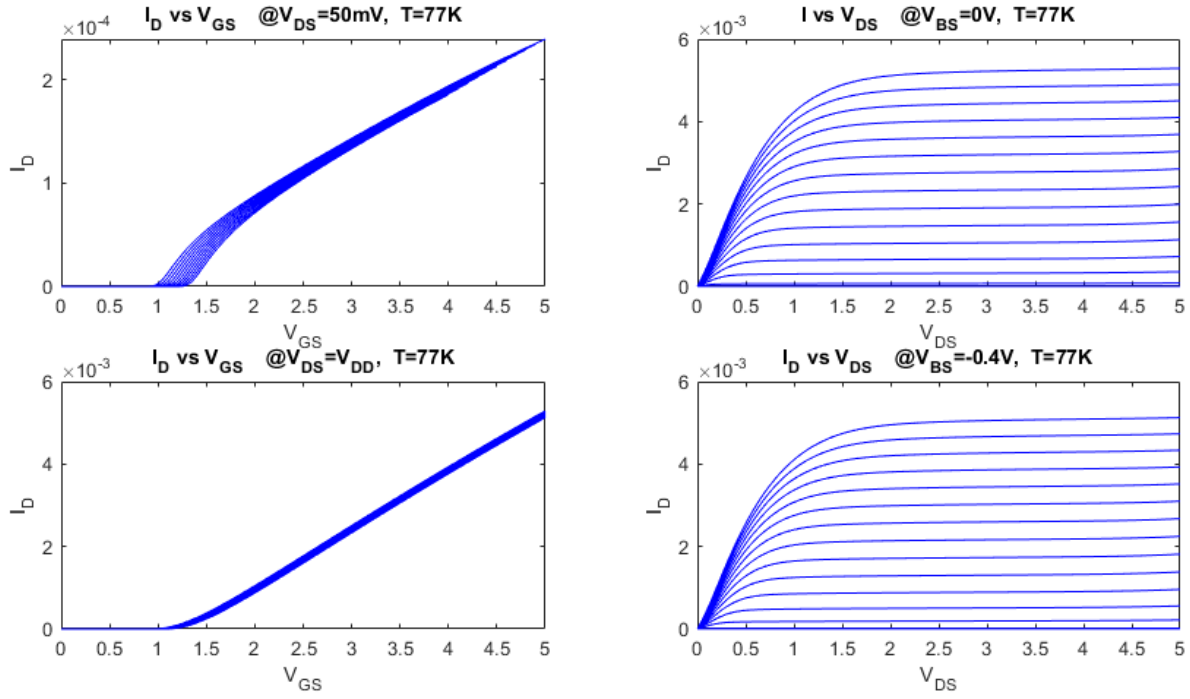

Figure 3.8: Measurements of a $5V$ nMOS transistor with $\frac{W}{L} = \frac{10\mu m}{1\mu m}$

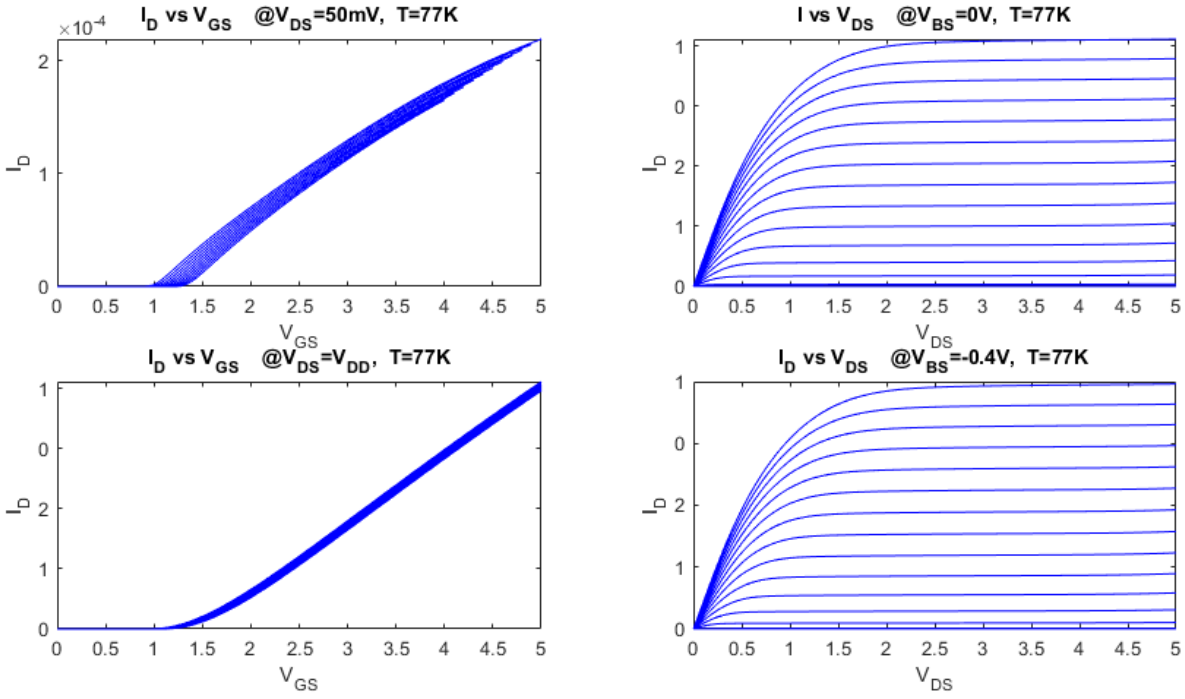

Figure 3.9: Measurements of a $5V$ nMOS transistor with $\frac{W}{L} = \frac{10\mu m}{2\mu m}$

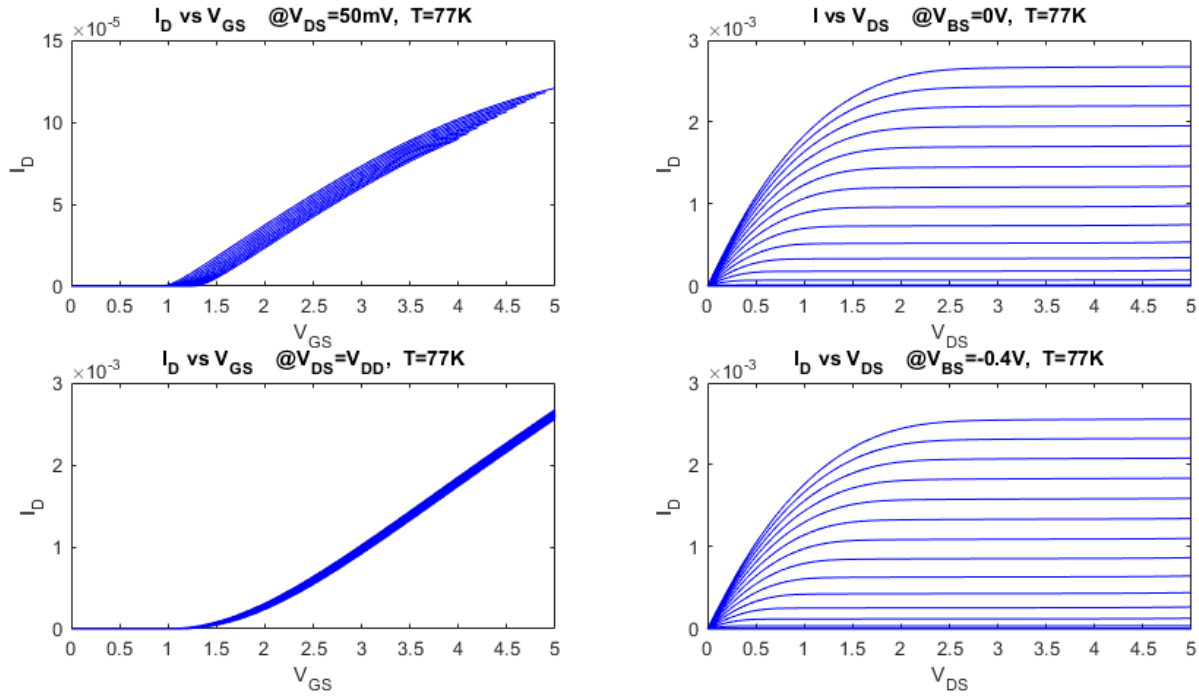

Figure 3.10: Measurements of a $5V$ nMOS transistor with $\frac{W}{L} = \frac{10\mu m}{5\mu m}$

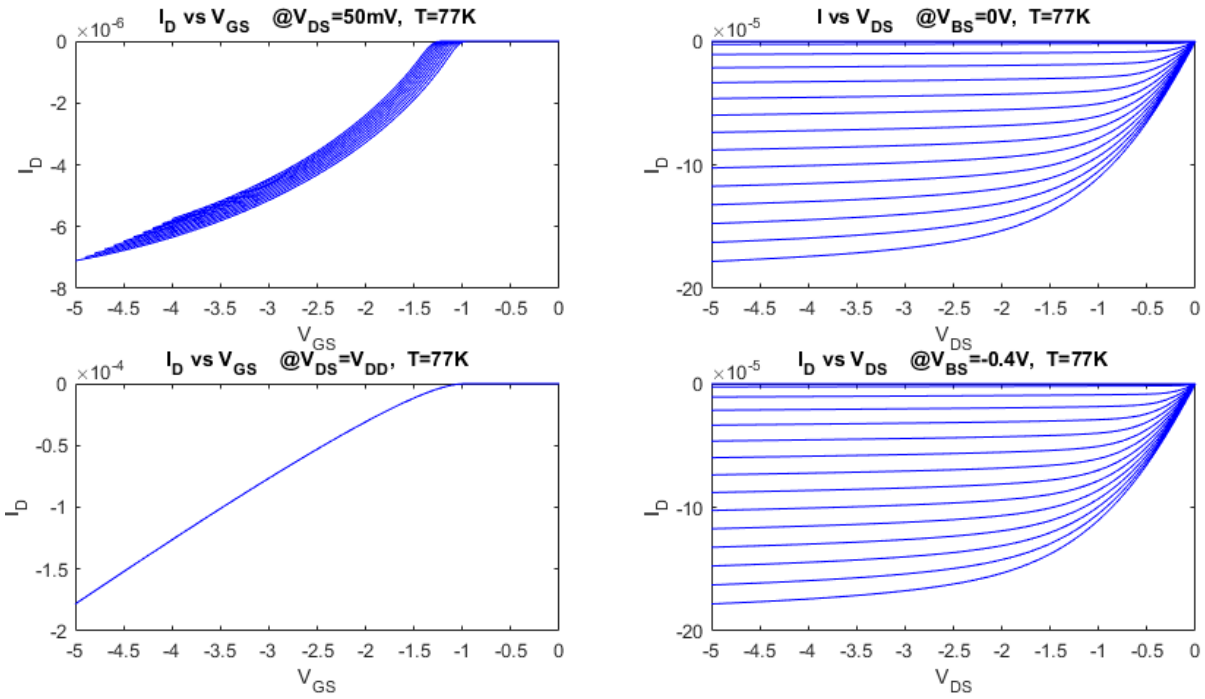

Figure 3.11: Measurements of a $5V$ pMOS transistor with $\frac{W}{L} = \frac{0.8\mu m}{0.8\mu m}$

an example the characterizations at $300K$ and $77K$ of a $1.8V$ nMOS transistor with $\frac{W}{L} = \frac{2\mu m}{2\mu m}$. By comparing the measurements, it can be seen that at $77K$ for $V_{GS} = 1.8V$ and $V_{DS} = 1.8V$ there is an increase in the drain current of approximately $135 - 140\%$ and in the threshold voltage of approximately $100mV$ compared to the values at $300K$.

The first effect can be substantially recalled to the increase in the mobility of carriers at cryogenic temperature due to the reduction of scattering phenomena between electrons and phonons [4, 5]. As for the increase in the threshold voltage as the temperature decreases, it is possible to understand its physical origin by analyzing the following expression:

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_A\epsilon_{Si}(2\phi_F + V_{BS})}}{C_{ox}} \tag{3.1}$$

where V_{FB} is the flat-band voltage, ϕ_F is the Fermi potential, N_A is the donor concentration (in the case of p-type substrate), ϵ_{Si} is the dielectric constant of silicon, V_{BS} is the bulk-source voltage and C_{ox} is the capacitance per unit area of the gate oxide. The increase in the threshold voltage is due to the increase in the Fermi potential ϕ_F which occurs as the temperature decreases [11] and appears to be the dominant effect on the variation of the threshold voltage as the temperature changes.

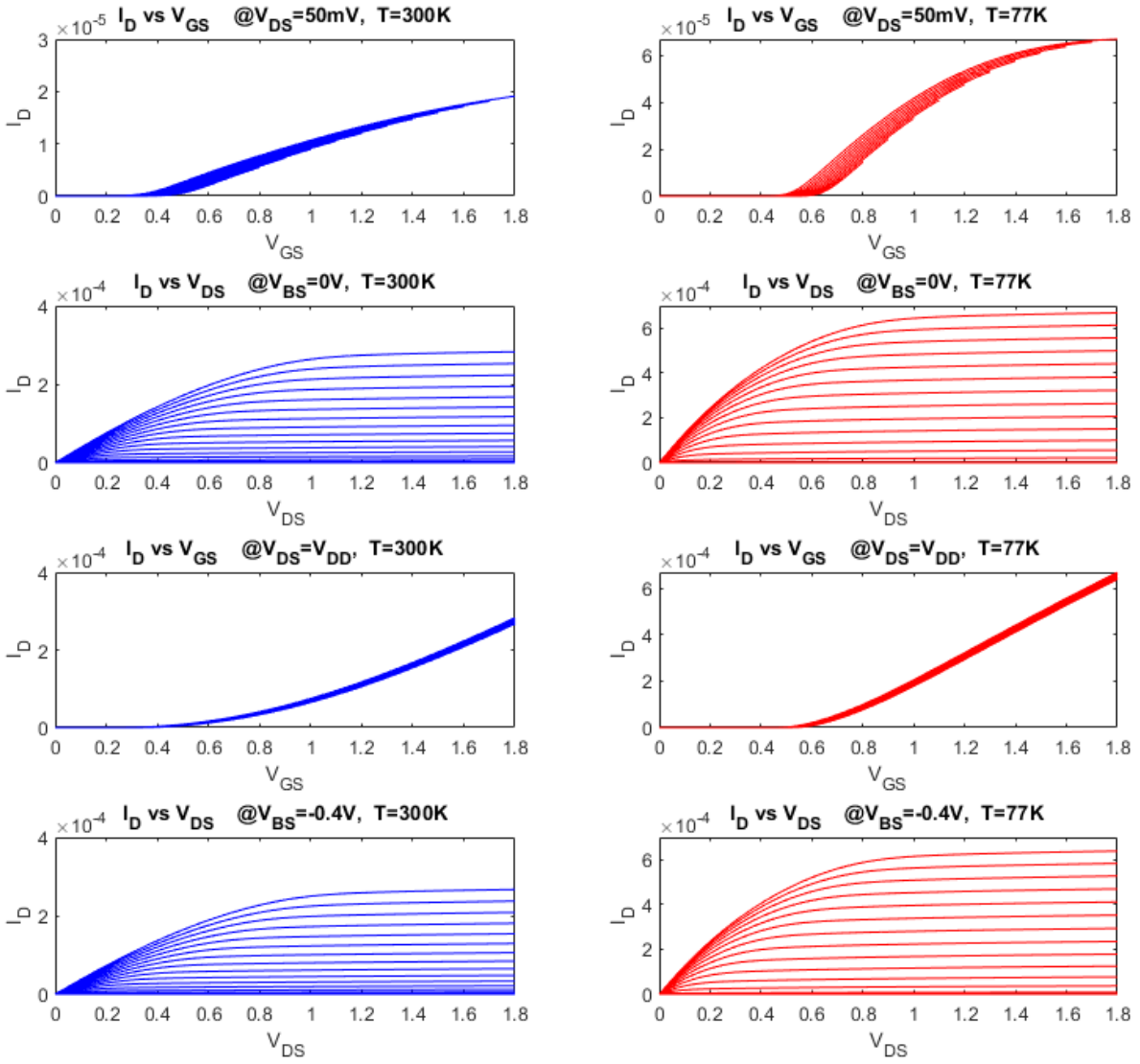

Figure 3.12: 300K and 77K measurements of a $1.8V$ nMOS transistor with $\frac{W}{L} = \frac{2\mu m}{2\mu m}$. On the left, the measurements are at 300K. On the right, those at 77K.

3.3.1. Poly-Resistors

Concerning the resistors taken into exam, they also showed a certain increase or decrease with respect to their nominal value as the temperature varied, depending on the technology with which they were implemented, as summarized in the Table 3.2.

During the design phase these values need to be considered to choose the best resistor technology for the required application. For example, rnpolylt resistors are important when a stable value across the whole temperature range is required, at the cost of more occupation area, since their resistivity is quite low. Furthermore, the characterization of

the resistances can be useful in understanding the results of the experimental measurements on the final chip.

3.4. Model Extraction

The *Model Builder Program (MBP)* software was used to extract the DC parameters of the BSIM3v3 model as it was the case for the previous models. This program, starting from a set of experimental measurements, allows to perform specific automatic extraction routines, based on the selected reference model. Thanks to this software, the BSIM3v3 model at 77K was extracted for all four types of transistors tested, at 1.8V and 5V and both *n*-channel and *p*-channel. These models, consisting of simple text files containing the list of all the used parameters and their respective extracted values, will then be inserted into the simulator libraries to be adopted in the design phase and recalled to verify the behavior of the designed system in the simulations performed at 77K. The extracted models are shown in Appendix A.

Prior to concluding the discussion on the extraction of the DC parameters for the BSIM3v3 77K model, it is necessary to consider the extracted model's accuracy by comparing the experimental curves to the same curves simulated using the obtained parameters.

According to this analysis, fitting the experimental curves with the extracted model resulted in an error of between $5-6\%$ and up to about 20% in the worst cases, for each of

Name	Comment	Value @300K	Value @77K	Δ[%]
rppolyh_5_50	High resistive	22.86k	51.13k	123.7
rppolyh_2_20	High resistive	29.09k	65.88k	126.5
rnpolylt_5_50	Low Temp coeff	1.39k	1.40k	0.719
rnpolylt_2_20	Low Temp coeff	1.34k	1.47k	9.701
rppolyl_5_50	Low resistive	3.28k	3.74k	14.02
rppolyl_2_20	Low resistive	3.39k	3.89k	14.75
rppolyl_1_20	Low resistive	6.93k	7.95k	14.72

Table 3.2: Table showing the major characteristics of poly-resistors and their variation at cryogenic temperatures. The resistors' names contain information about their doping, a qualitative indicator of their value (reported in the comments), and finally the width W [μm] and length L [μm]. In the final column, the percentage variation in resistance from 300K to 77K is reported.

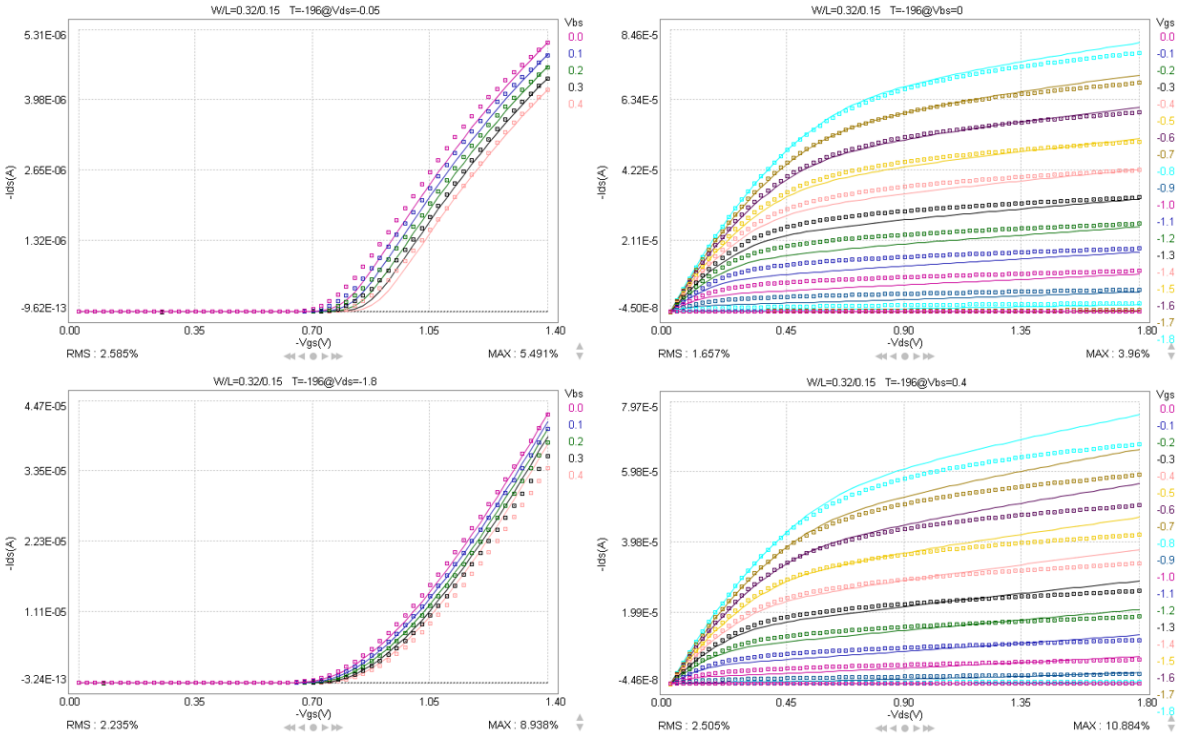

Figure 3.13: Comparison of experimental and calculated curves for a 1,8V pMOS transistor with $\frac{W}{L} = \frac{0.32\mu m}{0.15\mu m}$. The continuous line represents the extracted model, while the squares represent the points on the experimental curves.

the four types of transistors tested.

Observing, for example, the comparison shown in Figure 3.13 between the experimental curves of the characterization of a 1.8V pMOS transistor with $\frac{W}{L} = \frac{0.32\mu m}{0.15\mu m}$ and the same curves obtained with the extracted model, it can be observed that the maximum error goes from 3.96% in the characteristic at the top right, measured with $V_{BS} = 0V$, to 10.88% for the measurement of the characteristic curve with $V_{BS} = 0.4V$ shown at the bottom right.

A final observation, albeit qualitative, as proof of the goodness of the results obtained, can be made by observing the values of the extracted parameters called V_{th0} and μ_0 and comparing them with those of the provided models. Specifically, these two parameters represent the ideal threshold voltage for a large transistor ($W = 10\mu m$; $L = 10\mu m$) and the ideal mobility at the considered nominal temperature. In order to be able to make a comparison also with the results of Paragraph 2.2.4 let us consider, for example, the $5V$ n-type transistors. For the parameters V_{th0} and μ_0, the values $1.114V$ and $0.226\frac{m^2}{V \cdot s}$ were obtained from the extraction, not far from the previous $1.104V$ and $0.2214\frac{m^2}{V \cdot s}$, while,

as a reminder, the values from the provided model at room temperature are respectively $0.726V$ and $0.0505\frac{m^2}{V \cdot s}$. Therefore, as a corollary of what has been said in Section 3.3, at low temperature there is an increase in mobility and threshold voltage, in line with what is expected from the operating physics of MOS structures.

In conclusion, considering the given observations and the obtained results, it can be said that the obtained model well reflects the observed experimental behavior, with fairly limited margins of error for characterizations of this kind. Therefore, the new models can be added to the provided standard libraries and can be used to verify and predict the behavior at 77K of the system in its new version using standard integrated circuit design tools.

3.5. BJT Chracterization

The purpose of characterizing BJT was to qualitatively determine how closely the models provided by the company approximated their real behavior. This stems from the fact that bipolars were used in the construction of an integrated temperature sensor, as previously explained in Chapter 2. BJTs in trans-diode configuration did not require an accurate model, whereas they would have required one if they had been used in a gain stage, for example. Therefore the base-emitter junction was characterized, followed by a comparison of the experimental results to those generated by the circuit simulator.

As before, it was necessary to mount in the C-DIP (Ceramic Dual Inline Package) and then bond the BJT chip provided by LFoundry, which was then inspected under a microscope to ensure proper bonding. The chip contains four different types of BJTs, namely *npn*, *pnp*, *npn12*, and *pnp12*, where the latter are nothing more than 12 bjt in parallel, as implied by the name. The tests focus primarily on *pnp* devices because this type of bipolar is used in the integrated temperature sensor, but *npn* devices were also measured for completeness.

As mentioned at the beginning of the chapter, BJTs were characterized by sampling their behavior at various temperatures ranging from room temperature to the temperature of liquid nitrogen. The technique used to conduct such sampling requires that the cryogenic probe be inserted in successive steps into the dewar, gradually lowering its height above the nitrogen level and thus lowering its temperature. Therefore, a calibrated temperature sensor is required to monitor the temperature at the end of the cryogenic probe that houses the chip with the BJT. The *DT-670 Series silicon diodes* in particular were used for this purpose, as they provide excellent accuracy over a wide temperature range, having been calibrated across the entire 1.4K to 500K temperature range [1]. To ensure proper

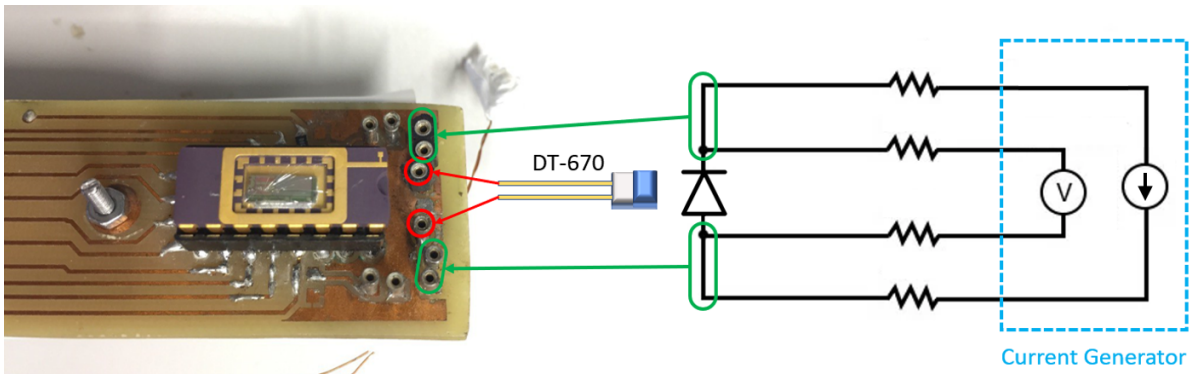

Figure 3.14: The figure depicts the cryogenic board that holds the bipolar sample placed near the DT-670 device. At the end of the circuit board are turned-pin sockets dedicated to the temperature sensor (circled in red) and to the 4-wire polarization and reading of its operating voltage (circled in green) via a current generator. Ammeter and voltmeter (V) of the generator are used to measure the diode's supply current and the voltage that develops at its nodes.

operation, the DT-670 has been polarized with a forward bias current of $10\mu A$, as specified in the relative datasheet, by means of a current generator, as illustrated in Figure 3.14.

The cryogenic board that houses the C-DIP with the chip includes a socket for the Dual Inline connector above the temperature sensor's turned pin sockets, as shown in Figure 3.14. This may result in a misalignment of the devices in the measurement chip and the sensor, depending on the length and anchorage of the latter. After connecting the cryogenic probe to the Keithley 4200-SCS, which was once again used to perform these measurements, and filling the dewar with liquid nitrogen to a level sufficient to completely cover the temperature sensor and chip and not much further to ensure a higher sensitivity in reading the temperature at different heights, we moved on to the probe's anchoring phase, which is critical for obtaining more accurate measurements.

To provide structural support, a clamp was used to connect the probe's steel tube to a rigid horizontal rod. The clamp is slightly loosened when the probe is manually moved vertically. The probe's flange is responsible for sealing the mouth of the dewar, preventing unwanted thermal exchanges between its interior and exterior that could affect the measurements. It also serves a structural purpose: when tightly secured to the tube and resting on the dewar, it aids in further stabilizing the probe. Nevertheless, due to the low reliability of the supports, it was necessary to manually hold the probe during static measurement phases, most notably during the initial insertion phases, when the probe was at its highest point of travel.

$V_{Emitter}$	$I_{Collector npn12}$	$I_{Collector npn}$	Current Ratio
630mV	$3.740\mu V$	$298.0nV$	12.55
640mV	$5.524\mu V$	$445.0nV$	12.41
650mV	$8.157\mu V$	$664.1nV$	12.28
660mV	$12.03\mu V$	$986.1nV$	12.20
670mV	$17.73\mu V$	$1.464\mu V$	12.11
680mV	$26.04\mu V$	$2.171\mu V$	11.99
690mV	$38.09\mu V$	$3.210\mu V$	11.70

Table 3.3: The table depicts the current trend of $npn12$ and npn bipolars as the V emitter varies within a range of values centered on the threshold voltage of the devices, which is approximately $660mV$. In the final column, the ratio of currents corresponds to the factor 12.

The bipolars characteristic curves are determined by polarizing the base, substrate, and collector nodes to ground and forcing a current sweep with a range of $0.5\mu A$ to $10\mu A$ and steps of $0.1\mu A$ in the emitter, range of values expected from the device when the chip is operational between $300K$ and $77K$. As a result, the voltages and currents at all of the BJT's terminals are recorded along with the emitter current and temperature change. The measurements are identical for $npn12$ and $pnp12$ bipolars with the exception that the current sweep begins at $0.5\mu A$ and ends at $50\mu A$ with steps of $0.5\mu A$. Emitter current and voltage and collector current are plotted from Keithley to ensure that the device is operating properly. For the purposes of this analysis, the characteristic of interest will be obtained by taking into account the trend of the emitter voltage of the chosen BJT as temperature changes fixed two arbitrarily chosen DC current values of the entire sweep.

Additionally, using the Cadence circuit simulation software, two schematics were created to compare the experimental measurements of the bipolars to the circuit model provided by LFoundry. One schematic consists of a *pnp* type BJT, in transdiode configuration with the collector connected to ground, in series to a current generator. In the second schematic, the parallel of 12 *pnp* bipolars, each identical to the previous one, is connected in the same way to the current generator. The simulations provide for a DC current stimulus via current generator through the emitter of the bipolars as the nominal temperature ranges from $26.85°C$ to $-196.15°C$ to subsequently plot the emitter voltage at varying temperature. As DC bias currents, $4\mu A$ and $10\mu A$ were chosen for *pnp* and $10\mu A$ and $50\mu A$ for 12 *pnp* in parallel.

3.5.1. First Results

After performing the initial measurements on the bipolar *pnp* transistor, it was discovered that the device was defective. Indeed, Keythley's graphs demonstrated that the device behaved abnormally even when a current was forced through the emitter. Therefore, the device bondings were rechecked on the assumption that some were missing or were not intact, but no bonding had been damaged. As a result, the emphasis of the measurements has shifted to *pnp*12, but first, the same measurement at room temperature of *npn* and *npn*12 was required to ensure that the label "12" accurately indicated a device that was 12 times more conductive. As shown in the Table 3.3, the currents of the two types of BJT, fixing the emitter voltage, are effectively 12 times greater.

The results of the first set of measurements that were performed show a strongly non-linear trend of the emitter voltage as the temperature varies, as it can be seen in Figure 3.15. The measurements collected at $77K$ and $300K$ are consistent with the simulations performed in Cadence on the 12 *pnp* in parallel, while some non-optimal factors could have compromised the intermediate measurements, for example the speed in taking the single measurements; the time that each of them actually took may have been less than the time needed to completely stabilize the temperature at that specific level. Another factor that contributed to the inaccuracy can be traced back to the thermal insulation given by the flange which is not sufficient to completely cancel some turbulence due to thermal exchanges between the external and internal environment; a final hypothesis concerns the temperature sensor which may have not been perfectly aligned with the chip causing a

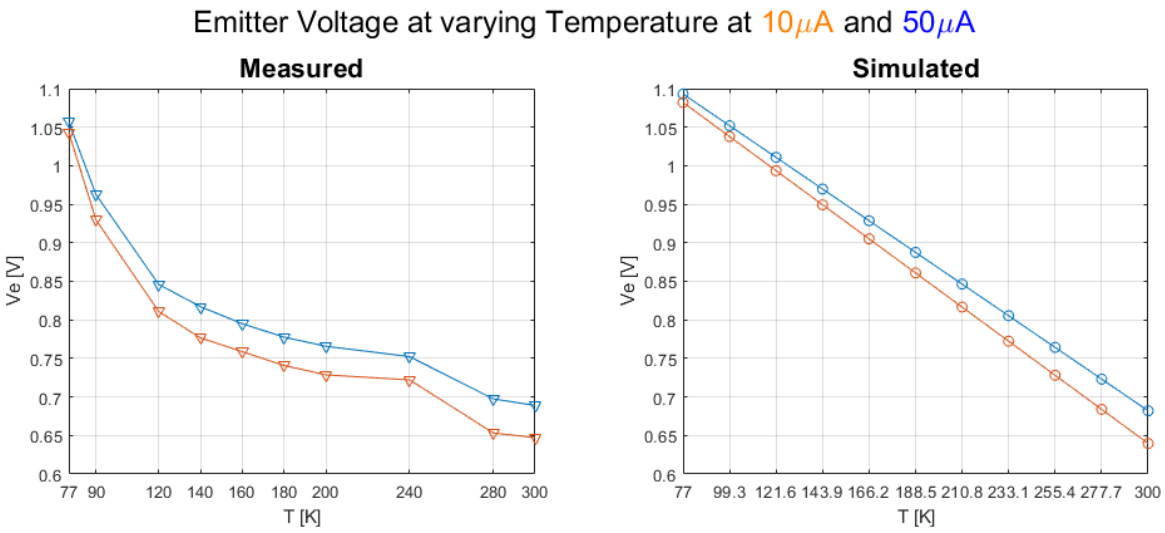

Figure 3.15: First comparison between experimental results and simulations for the *pnp*12 device.

further uniform translation of all the measurements.

3.5.2. Improved Setup and Final Results

This first characterization showed apparently meaningless anomalies, but from the analysis of the samplings it was suspected that the problem was most likely related to the measurement itself rather than the device, thus, it was intended to improve the setup's accuracy and precision.

To avoid relying on a human factor for the probe's firmness, that is, on a person holding the probe throughout the procedure, the stability of the anchorage of the steel rod has been increased, a significant benefit for increasing the settling time at thermal regime for each level. The measures have therefore become much slower, but also much more faithful. Another improvement addresses the temperature sensor's misalignment with respect to the BJTs. To eliminate any offset that could result from the measurements, the position of the temperature sensor with respect to the chip and the BJTs themselves has been improved by using a sort of plastic dome designed specifically to protect the chip on which the temperature sensor was placed, which was further sealed with Teflon to increase safety and precision.

The most significant improvement made to the setup is represented by the addition of a thermal filter which has considerably increased the rejection to temperature variations due to simple internal drafts or vortices following the movement of the probe or the

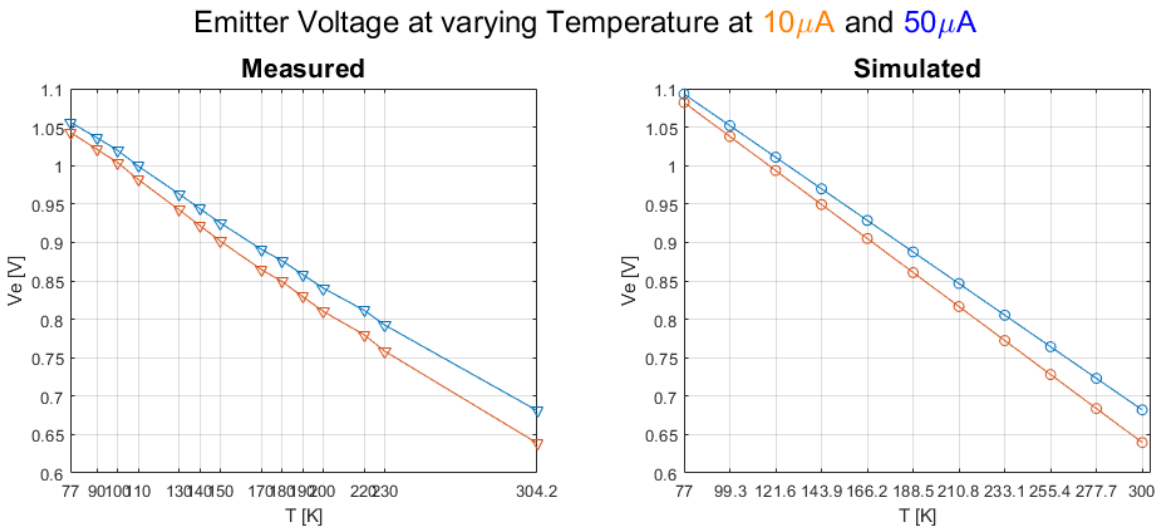

Figure 3.16: Comparison between measurements and simulations of the bipolar *pnp*12 after the improvement of the setup.

transit of people near the dewar, or caused by air currents between doors and windows. This modification further slowed down the collection of measurements by lengthening the settling time at the equilibrium temperature, but in favor of a significantly greater accuracy. To conclude the series of modifications, in order to avoid unwanted thermal losses, the flange has been sealed to the dewar with insulating tape, and to avoid any jolts of the end part of the probe and collisions of the filter against the walls of the dewar a guide for the steel tube has been added.

Following these updates, the same measurements were repeated, and the results were significantly more similar to the simulations, as illustrated in Figure 3.16. Overall, a marked linearity over the entire range of temperatures, with a $1.78\frac{mV}{K}$ gradient for measurements at $10\mu A$ and $1.65\frac{mV}{K}$ gradient for those at $50\mu A$ with respect to the $1.98\frac{mV}{K}$ and $1.84\frac{mV}{K}$ grandients of the simulated curves, denotes the great improvement of the new measures compared to the previous ones, despite some difficulties in their collection near the opening of the dewar, an area which is slightly more unstable from a thermal point of view. Since the accuracy of the temperature sensor is not considered a very strict specification, the measurements obtained in these regions were deemed sufficiently valid.

In conclusion, considering the observations made and the results obtained, it can be stated that a good agreement has been obtained between the experimental measurements and the simulations obtained from the models, differing at most by a mismatch of the order of $40mV$ which does not involve any anomalous behavior of the temperature sensor.

4 | Cryogenic Probe

To undertake a thorough and precise characterization of the QUASIX chip in order to confirm its behavior and determine if a satisfactory driver was obtained, it was required to make significant modifications to the measurement setup, which was no longer acceptable for the new requirements. Underlying this significant transformation are technological and practical considerations that the previous probe could not address. First of all, the number of pins and the frequency spectrum that some trigger and output signals require make it extremely difficult to monitor with the probe now in use. The implementation of the new setup has also taken into account the practicability and manageability of positioning the probe and executing a substantial number of distinct tests. In addition to the modifications made to the probe, two test cards have been produced in line with the new probe and tailored to the project, as well as a control panel with a firmware interface for the management and automation of the set of tests to be performed on the ASIC. Additionally, shift registers were added to the system's front-end to minimize the number of pads to be driven. The design of the new probe and the selection of components with all the updated version's features will be discussed, as well as the implementation and validation of the auxiliary circuitry.

4.1. Project of the Cryogenic Probe

The old probe is essentially a hollow steel tube with a 26mm outer diameter, a movable flange, and a connecting box. The steel tube has, at the end designated for nitrogen immersion, a 60mm-long housing for the test boards, into which the PCBs are screwed and bolted. On the opposite end of the tube is a metal box with a USB port for 4-wires reading, which is mostly utilized for the temperature sensor, as well as 16 BNC connectors for coaxial cables with switches that ground the connections. The wires are terminated with a 16-pin Header male connection that must be put into the corresponding female connector soldered on the PCB, a solution taken to enable the test board's portability. The test cards created for measuring chips with this probe share the existence of at least one female 16-pin Header connector positioned on one of the shorter sides of the PCB, if not

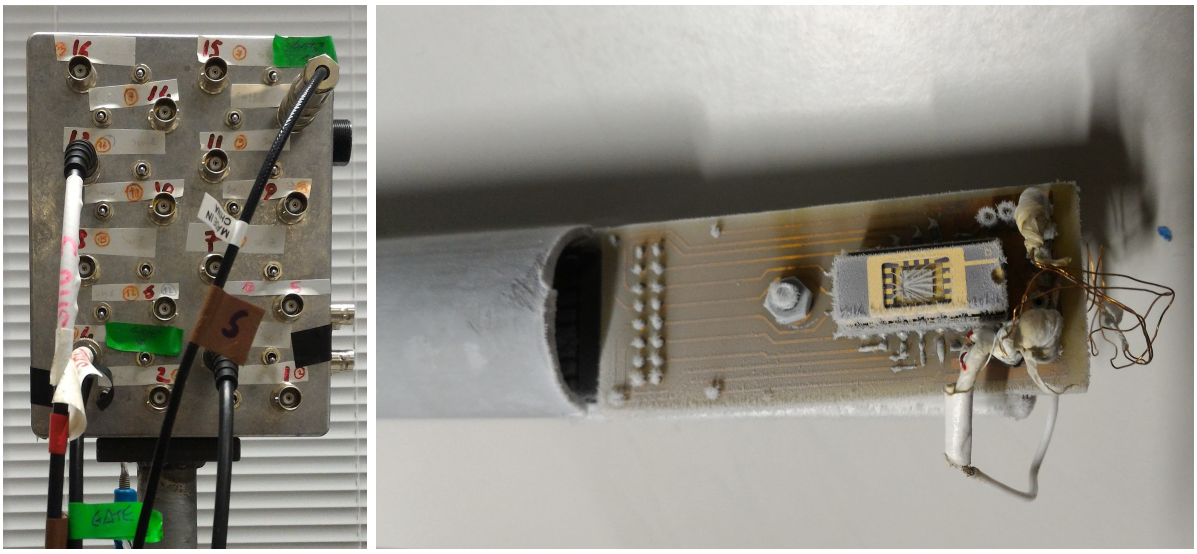

Figure 4.1: Details of the first cryogenic probe. On the left is the probe's metal box, and on the right is a sample installed on the probe's PCB and freshly extracted from the liquid nitrogen bath.

both, and a socket designed to accommodate the support on which the measuring device is soldered. The mobile and detachable flange provides structural support throughout the measurement and seals the mouth of the dewar by being screwed to the tube near the dewar once the desired probe mounting location has been determined.

4.1.1. A New Design

The cryogenic probe utilized for the previously described characterizations would not have been able to handle the QUASIX chip's 37 pins, which include power supply, triggers, inputs/outputs, and grounds. A temporary option to attempt to measure the ASIC with such a probe would be to test a subset of pins at a time, but even this would have been a difficult operation because the minimum number of pins required to perform a test on the chip that is actually useful in the best case scenario, i.e. a perfect functioning of the chip on the first try, exceeds the number of connections available on the probe. In addition, given the frequency band requirements of the output signal, connectors with a bandwidth of around ten gigahertz or somewhat less were required for both signal reading and input trigger signals to the processor. The handling of the structure is a further significant issue. According to the probe's design, all the cables required for the desired measurements are routed to the metal box located at one of the probe's two ends. This morphological choice results in a major load for measurements employing several cables and a wiring that becomes less neat and manageable as the number of cables increases,

both of which increase the danger of damage to the chip under test or its bonding at the opposite end of the probe. To minimize these problems, it became necessary to remove as much weight from the probe as feasible, including what would be gained by increasing the connections and management electronics. Since it is not a thermally hermetic structure, the probe's steel tube might be narrowed relative to its original diameter, resulting in a lighter structure, but also a lesser heat dissipation from the external environment towards the end at lower temperatures. Therefore, it was necessary to replace the old probe with a new, more effective kind.

Since it was not necessary to use all 37 pads simultaneously, the initial specifications stated, for convenience, that the DC lines be reduced to 24 while maintaining the relevant switches for grounding and that at least four coaxial cables with connectors suitable for high frequency type MMCX be provided for triggers and signals lasting 5ns. Pre-assembled cables were chosen to ensure their durability. Additionally, four cables were maintained for the temperature sensor. Due to the increase in connections, it was decided to construct the connector box with SMA inputs instead of BNC or, if practicable and if there was a benefit, to design a mixed solution, while the BNC connections are mostly moved to a bench control panel that is separate from the probe. In addition, to facilitate the fabrication of the PCB, we desired to extend the housing for the test cards. A second significant difference from the previous design is the use of two test cards instead of one, a mobile and dedicated one for the chip being tested and a fixed one with two connectors, one to collect the cables coming from the connector box and the other to connect to the mobile probe above. Lastly, as PCBs are custom-made for testing different chips, regardless of the chip, and therefore many will be produced, it is preferable that the connector be relatively affordable to maintain a reasonable cost per every PCB.

4.1.2. Choice of Components and Realization

In light of the aforementioned parameters, the following components were chosen for the new cryogenic probe. For cryogenic applications, the tube was constructed from nonmagnetic stainless steel 308. In addition to the 18 percent chromium found in the composition of stainless steel 308, nickel makes up 9 percent of the material. The inclusion of chromium in this alloy boosts the tensile strength of stainless steel, which is balanced by the nickel content, which gives the material its flexibility. This stainless steel kind is ideal for structural components. The length of the tube from the end to be immersed in nitrogen to the connecting box is 1.80 meters. The diameter of the central rod is 19mm, while the diameter of the card housing, which measures 95mm in length, is 33mm. In the final section, multiple holes were drilled to reduce heat transmission through the steel,

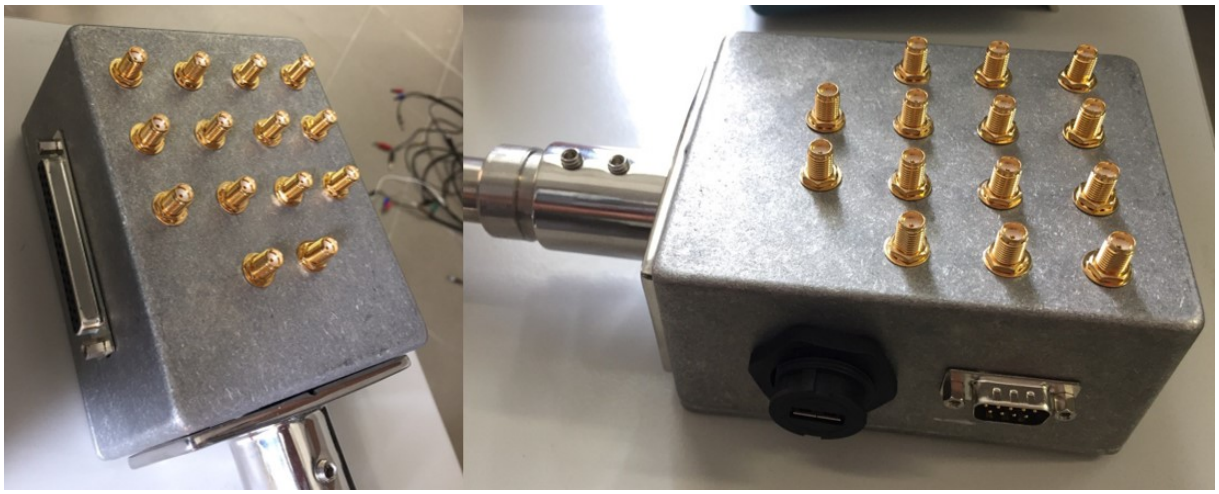

Figure 4.2: In these pictures, the connector box is shown. The connector for the nine digital lines and the USB port for reading the temperature sensor are visible on the right. On the left is displayed the low frequency line connector. On the front side are high frequency SMA connectors.

hence increasing thermal insulation, as well as a hole for the boards' fastening screw. This probe also features a flange with the same diameter as the main rod.

The connector box, Figure 4.2, features 14 front SMA connectors for micro-coaxial cables for high-frequency lines, eschewing a hybrid solution with BNC connectors, which, as will be discussed later, have been relocated to the control panel. On one side, it has two D-Subminiature (D-sub) connectors, one with 37 pins for generic low frequency signals including 8 power supply, 5 voltage references, and 4 for the ground, and the other with 9 pins for the eight digital lines and associated digital ground. This sort of connector is used to connect all slower signals to the exterior in order to eliminate cross-talk issues. As with the initial probe, there is also a USB connector for the 4-wire readout of the temperature sensor.

The cables attached within the connector box travel through the probe's full tube to reach the test board's side, where they are joined or soldered to the PCB based on the type of cable. Samtec's MMCX connectors are connected to the MMCX-SMA micro-coaxials, which have a signal wire diameter of 0.81mm and a feeding wire diameter of 1.13mm and a length of roughly 2 meters to reach the test board. Depending on the application and how crowded the PCB is, it may be advantageous to use the right-angle cable combination and MMCX vertical jack plug connectors, so the connection with the cable is from above and the micro-coaxial cable can reach even the farthest points of the PCB, as opposed to the straight cable and MMCX connector right-angle jack plug, with which the cable is

closer to the board.

The diameter of the end shown in Figure 4.3, which must be restricted so as not to collide with the mouth of the Dewar, is an essential factor to consider. In fact, the vertical plug connectors cannot be placed too close to the probe's edge because they would exceed the probe's true diameter and risk interfering with Dewar's insertion and extraction of the probe. Therefore, when the PCB is not extremely packed, right-angle connectors are the most practical option. In addition, the 50Ω matched load of the connectors ensures outstanding performance up to 6 GHz. As for the stranded cables of the general lines and the digital ones, it was decided to permanently solder them to the fixed test board, which is one-of-a-kind for all applications utilizing this probe. In contrast to the prior probe, the 37+9 lines do not require a connector on the side of the PCB to be soldered to. A solution of this type would result in weak connections that are easily desolderable because the surfaces to be soldered are so small, necessitating frequent and inconvenient maintenance, and with a large number of cables that demand mapping in addition to soldering, the required work would have been unnecessarily extensive.

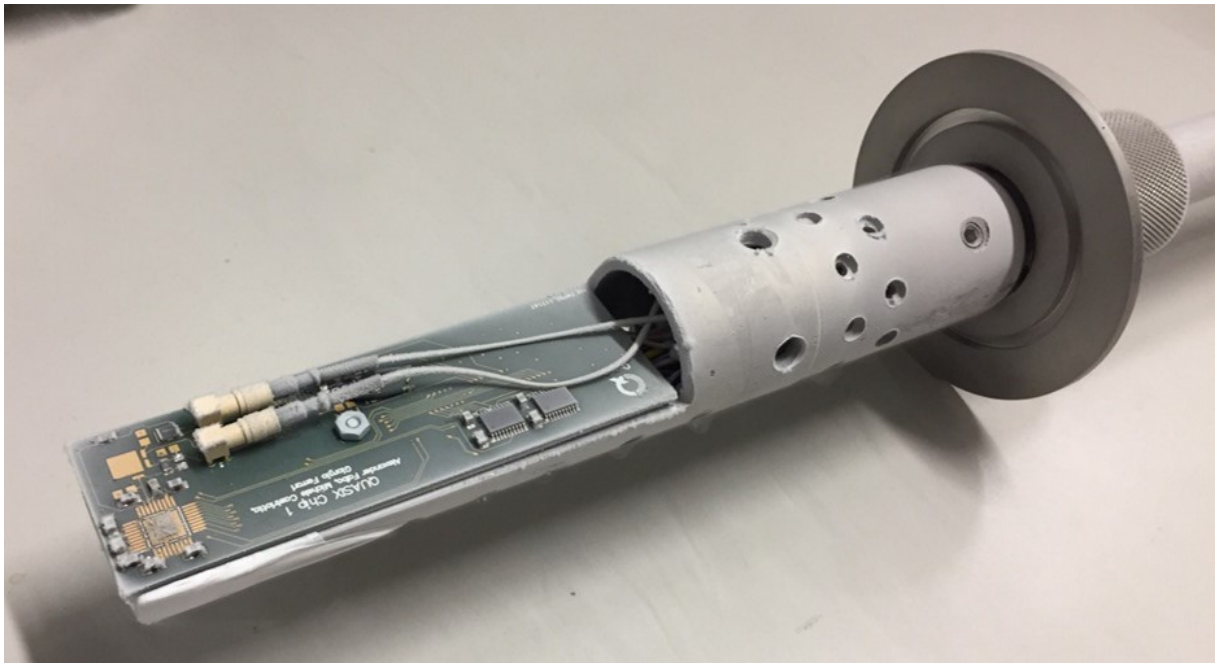

Figure 4.3: In the picture, it can be seen the end of the new cryogenic probe to which the test board is attached immediately after a nitrogen immersion.

4.2. Auxiliary Test Boards

To avoid confusion when reading this paragraph, it is customary to refer to the side of the card facing the connector box and its half board as the top, and the side that first touches the nitrogen during the dive and its remaining half as the bottom, for any treated card.

4.2.1. Fixed Board

The fixed board is composed of four metal layers referred to as top, inner, ground, and bottom. The board is nearly entirely comprised of the top layer, which contains the connectors and tracks. The inner and bottom layers have been used to construct additional connections, while the ground layer grants low impedance ground connections. Its dimensions are such that the PCB may be fitted into the housing and secured with two screws inserted via holes in the board's center and lower end. The 21.5mm width has been chosen to guarantee that, after being connected to the fixed card, the mobile card remains slightly above the housing's cut. Through a mezzanine connector DF9B-51P-1V(69), an SMT Board-to-Board Connector with 51 pads with a 1mm pitch, the two boards interact. Despite its compact size, this connector's trapezoidal mating region maintains a secure connection between the fixed card and the mobile card above it, hence preventing accidental misinsertion. In addition, it has an easy lock mechanism that ensures firm insertion and extraction properties and a smooth insertion and extraction sensation [3].

Some of the 51 pads are dedicated to connections with the ground because they are not all used for lines. The "ideal" ground state can only be achieved if the ground's impedance is significantly lower than all the others in the circuit. When possible, it is preferable to strive towards this state by employing an abundance of connections. As expected, the fixed test board must intercept and gather all stranded cables of the generic and digital lines emerging from the connector box. These cables are connected to the connector in the upper half of the card via a routing network established on both sides of the card to maximize space. It is also designed to accommodate the DT-670 temperature sensor with its dedicated connectors. The flat shape is intended to accommodate the pads of the temperature sensor and allow its attachment without the need for special interlocking and anchoring techniques, as was the case with the turned-pin-shaped connectors of the initial probe.

The 4 wires of the temperature sensor, which have been soldered in 4 vias on the lower end of the PCB, are carried to 6 pairs of way where the connectors for the temperature sensor

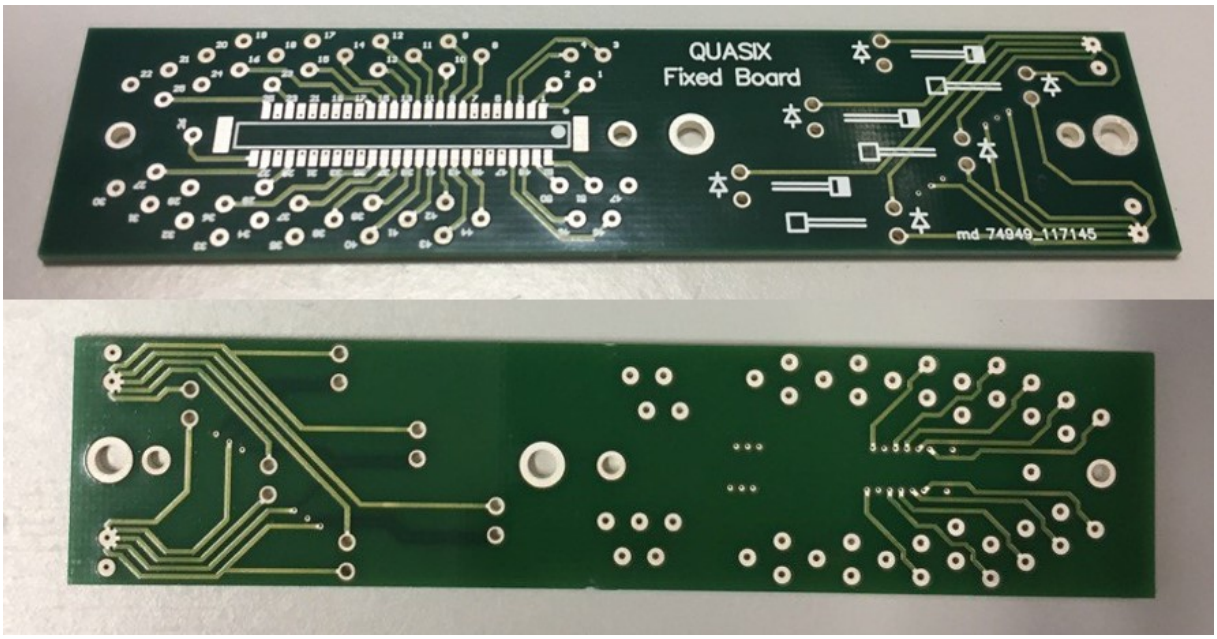

Figure 4.4: The picture depicts the front and rear of the fixed test board.

have been inserted and soldered, with the insertion location for the connections varying from time to time. To make the schematic and PCB more comprehensible, symbols were affixed to the PCB adjacent to each pair of channels to show where the diode should be put and in which direction. The connectors are arranged in two diagonally parallel lines to the board's axis, with the sensor inputs pointing up and down alternately. This structure allows the temperature sensor to be positioned at different heights in order to line it as closely as possible to the location of the chip under test on the PCB above, making the mobile card easy to produce and the fixed card extremely versatile.

4.2.2. Moving Board

To maximize available space and create a neater, more functional board, the width of the mobile board matches the diameter of the probe's last segment. This PCB, shown in Figure 4.5, was constructed with four layers, top, inner, ground, and bottom, similar to the fixed board, but their use was considerably more intensive. In addition to the ASIC and the erbium diode, the top layer has everything required to perform frequent alterations, such as moving, removing, or adding elements using the soldering machine. Some components had to be soldered only after the chip had been placed and bonded, including anything that fell within the operating space of the bonding machine and could impede its operation, such as the power supply's stabilizing capacitors that were located extremely close to the chip.

It is useful to specify that the bonding machine requires a PCB with a stable support surface, so nothing has been soldered on the bottom layer prior to this procedure. However, after bonding, it would have been preferable to have as few components as possible on that layer, as soldering on the side opposite the chip necessitates extreme caution so as not to damage the bonding. On the upper side of the circuit board, near the vias that contact the connector on the bottom layer, there are two shift Registers that will be discussed in detail in the following paragraph. In contrast, the board's primary circuitry is located beneath the topmost layer.

Here is the Quasix chip, positioned as low as possible on the board and compatible with the power supply pads, tracks, and capacitors. It is mounted on a 5mm x 5mm ground pad for chip positioning tolerance. Around this pad are 37 pads corresponding to 10 pins for input signals, the output to the diode, switches for tuning internal resistors when changing from room temperature to 77K, digital pins of the input logic, for the selection of drivers and for the selection of the trigger, power supplies and digital and analog references, ground, pins for 100nF external capacitors, output of the temperature sensor before and after the buffer, and signal triggers.

There are also four pins for the investigation of four internal nodes in the event of chip problems that cannot be deduced from the analysis of the other nodes alone. Unlike other nodes, which are permanently linked, these nodes can be detached by removing a 0Ω resistor from the line that links them to the connector if the chip does not exhibit any odd behavior or if the source of any failure can be determined by examining the other pins. To reduce the length of the connection, the erbium diode is positioned close to the QUASIX chip. The diode footprint consists of a big 4.5mm x 4.5mm ground pad to accommodate the sample, as well as two smaller pads connected to the driver output and the MMCX connector to which the diode nodes will be connected. Free space has been left adjacent to the pad so that it can be enlarged to accommodate larger samples in the future.

To be able to test the output voltage of the chip while the diode is present, an additional pad connected to one of the low-frequency lines of the mezzanine connector has been added to the footprint. If the second terminal of the diode is attached to this pad rather than the one linked to the high-frequency connector, it is possible to simultaneously measure the output voltage of the driver and excite the diode. In this instance, it was possible to install a capacitance next to this pad to reduce the impedance, which would eventually be replaced with a 0Ω, avoiding bias while ensuring an even lower impedance or preventing resonances between the capacitance and the inductance of the lengthy connection. Similar to what was done for this pad, the footprint of a filtering capacitor was introduced in

parallel with the MMCX to maintain the low pad impedance during pulse.

The footprints of two 100nF capacitors for "Switched" type DACs and a capacitor connected from the output of the chip to the ground were positioned between the chip and the diode in order to analyze the behavior of varying the load capacitance or resistance without the diode. To prevent adaption issues caused by a lengthy PCB track, the MMCX connectors for clock and high frequency reading of the chip output are positioned right above the chip and diode. The proximity of the connectors is also crucial because the propagation delay of the tracks must be considered. For example, three centimeters of track will result in a delay of around 0.2ns and, if the track is inadequate, spurious signals of that duration arise, which are sufficient to cause the clock to generate erroneous command signals.

If it is necessary to slow down the fronts, a series resistance created along the clock signal connector track can be soldered in place of a 0Ω. In order to adjust the clock signal connector, a 50Ω parallel resistor was installed. It was decided to utilize a high voltage chip resistance capable of withstanding a voltage of 5V to its heads, resulting in a power dissipation of 500mW per pulse clock. It is interesting to note that on the ground layer, a cut has been practiced around this connector and its adaption resistance to prevent high frequency disturbances from spreading over the entire layer. This cut

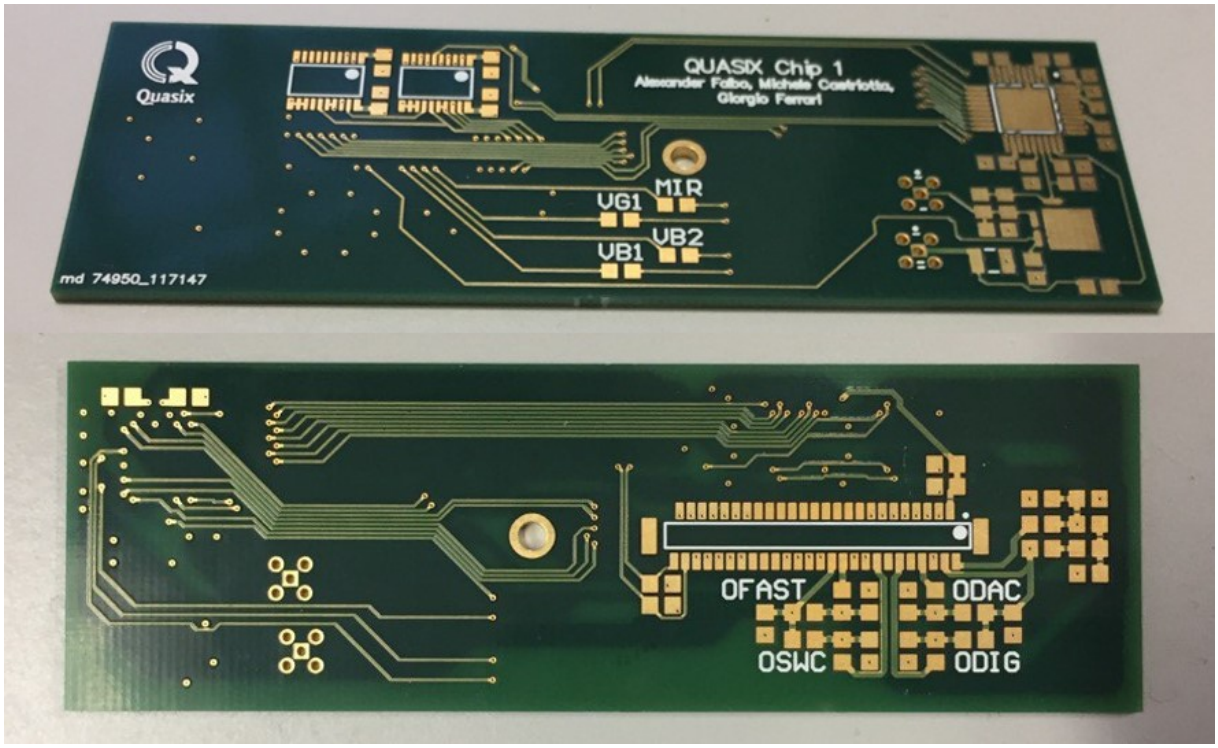

Figure 4.5: The picture depicts the front and rear of the moving test board.

also includes the 50Ω resistance to ensure that the current traveling through it has a way back to the "basic" MMXC. If the clock's current had encountered the bottleneck between the two groundplanes, it could have taken different courses than those through the microcoaxial, potentially causing interference or cross-talk. Power supply and voltage reference connections were made on the inner layer using broader tracks than those used for all other connections. Moving on to the bottom layer, components to be put in this layer were distributed in consideration of the tube's wall thickness. Attention must be paid not to connect items too closely or to place vias in such a way as to avoid short circuits, as the board leans on these edges and has less marginal space.

The bottom layer is mostly dedicated to the mezzanine connector DF9B-51S-1V(69) and components that would have been inconvenient to install on the top layer. These are the Save and Select digital signal stabilization capacitors for front-end logic and 0Ω resistors, as well as stabilization capacitors for 1.8V digital power supplies, 2.5V digital power supplies for the OTA reference node of DACs, and analog 5V power supplies, digital and R-2R network of the DAC, as well as those of the 5V voltage references of the tail generators of the differential input stage of the temperature sensor OTAs, the two "Fast" DACs. In this regard, it can be observed from in Figure 4.5 that, depending on where it is decided to solder 0Ω resistors, the 5V DAC, ANA, and DIG power supplies can be supplied by up to 3 different generators, if it is of interest to analyze or act individually on one or more of them, or from a single generator, in the schematic the VDD ANA 5V, in order to use as few lines as possible when the circuit is functioning properly. This also applies to the voltage references of the "Fast," "Switched", and temperature sensor OTAs, as well as the 2.5V reference voltage, which can be replaced by a resistive divider on the voltage supplied by VDD ANA 5V, although we try to avoid this solution due to the unclaimed variation of the resistances of the divider from room temperature to cryogenic temperature.

4.3. Shift Registers

Using shift Registers to serialize the input signals to the microprocessor was an additional innovation we sought to implement in order to better manage the delivery of input signals. This decision was made due to the possibility of employing the number of pins to manage a single path of input data instead of ten distinct paths, which will then be given to the ASIC simultaneously and in parallel according to the chip's original functionality. The integration of a shift register integrated in CMOS technology at 150nm was not an option in this thesis work since the QUASIX chip had already been sent to the foundry for its

production several months before. It is however possible that its implementation will be considered during future project development.

4.3.1. Specifications and Selection

Since the objective was not the design of the shift register so much as the creation of a setup to check the chip as soon as it came, it has been opted to select a shift register capable of meeting certain requirements. The control logic of the integrated driver, which is implemented via logic ports employing 1.8V transistors, necessitates the use of input signals of the same voltage; thus, the shift register must be able to deliver data at this voltage. A voltage more than 1.8V could cause damage to the front-end electronics of the chip, whilst a voltage less than 1.8V would create a malfunction due to the incomplete ignition of specific logic transistors, resulting in an incorrect code and an unexpected driving voltage. The maximum throughput is not a binding parameter because the input signals to the chip carry the information for adjusting the pulse's amplitude and polarity to polarize the diode so that its emission remains as stable as possible despite thermal changes in the surrounding environment that could affect its proper operation. The sampling frequency of the output voltage from the temperature sensor was chosen of 500mHz. This is because these signals are expected to follow the trend of the surrounding temperature, which is particularly sluggish.

In light of all the above, the Dual supply 8-bit serial-in/serial-out or parallel-out shift register 3-state, also known as 74LVC8T595PW or TSSOP20, whose internal structure can be seen in Figure 4.6, was selected. This device is a shift register with serial input and serial output or 8 parallel output bits, equipped with storage registers and 3-state outputs. The shift registers and storage registers each have their own clocks. On the positive-edge transitions of the SHCP input, data is shifted. The data in the shift register is transferred to the storage register whenever the STCP input transitions from negative to positive. If both clocks were to be short-circuited, the shift register would always be one clock pulse ahead of the storage register. The two power nodes can be supplied with any voltage between 1.1V and 5.5V, allowing the device to translate between any of the following voltage nodes: 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, and 5.0V; in this case, the voltage is converted from 5V, which is set to the known VccA, to 1.8V, which is placed to the pin Vccb. In addition, this device is equipped with electrostatic discharge (ESD) protection and a suspension mode, during which the Qn outputs are in the high-impedance OFF state when VCC(A) is at GND level.

This extremely compact device is supplied with 20 leads, which are placed in groups of

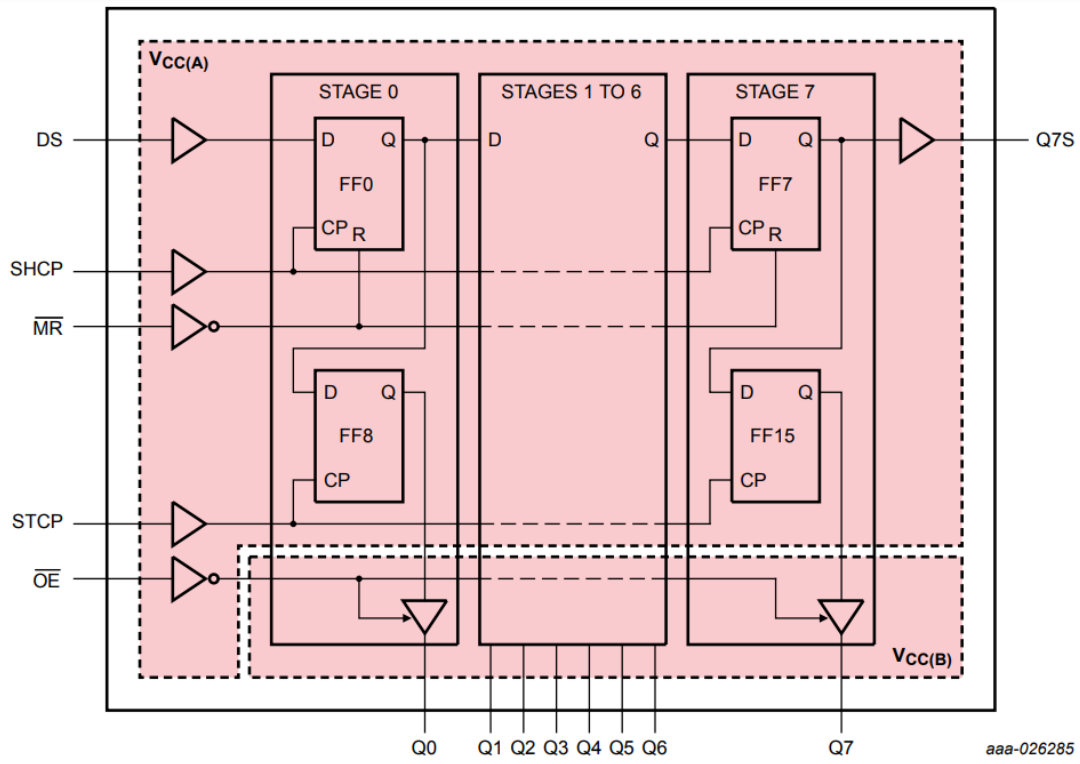

Figure 4.6: Internal structure of the shift register where the shifts and storage registers are visible, followed by a buffering stage that enables the transfer data to output or keeps the outputs at high impedance. Pins configuration, where pins Master Reset (MR), "SHift" Clock Pulse (SHCP), "STorage" Clock Pulse (STCP), Output Enable (OE), Digital Signal (DS) and serial output (Q7S) are referenced to VCC(A) and pins Qn, the parallel outputs, are referenced to VCC(B) [3].

ten along the two longest sides of the packaging. We chose a component with a footprint that made soldering on the test board very simple. The diagram depicts the internal construction and pin configuration of the device. Since this device has a maximum of eight parallel outputs, only two were used to match the chip's input pins, leaving six outputs unused. By connecting the Q7s node of the first register, representing the serial output, to the DS node of the second register, corresponding to the serial input, the devices were connected in series. In the same manner, the pads associated with the output signal enable, storage register and shift register clock pulses, and master reset have been interconnected between the two devices. This was done to get a single equivalent device with 16 output pins by connecting the two devices in series. The two distinct storage and shift register clock pads were short-circuited since it was deemed unnecessary to make use of the storage stage. As noted in the preceding paragraph, the shifts were placed near the top of the PCB to keep them as close to the connector as possible, so avoiding

digital control signals from crossing the board and introducing noise to the remainder of the circuit. In addition, the two devices were placed as tightly together as possible to avoid digital signal delays that could undermine the system's functionality.

4.3.2. Setup, Validation Test and Results

The device specifications ensure proper operation in a temperature range of $-40°C$ to $+125°C$, which is an industry standard. However, for the purposes of the project, the Shift Registers must be able to withstand temperatures as low as $-196°C$; therefore, their functionality was tested in liquid nitrogen before they were soldered to the mobile test board. The device has been soldered onto a PCB designed for such a packaging, connected to a special socket of an additional test board by means of header connectors. This configuration provides access to 16 of the device's 20 pins through a 16-line connector. To spare 3 pins, all four grounds of the device were short-circuited to each other, using only one line. During a second test launch, after modifying a connection on the test board, the remaining pin, which was designated as the Q7s serial output, would be evaluated.

Using an Arduino UNO microcontroller, the shift register was polarized and tested. The input terminals MR, SHCP, STCP, OE, and DS at the digital pins 8, 9, 10, 11, and 13 on the board were connected with jumper wires. On a breadboard, a resistive divider between a 680Ω resistance and a 390Ω resistance has been connected to the 5V power supply to provide the VCCB power to which the output pins refer. Thus, we acquired a voltage of approximately 1.84V, which is accurate enough for our needs, while connecting the VCCA pin and the ground line straight to the respective pins on the board. Finally, the microcontroller's analog pins were used to read the parallel outputs. Since these pins are insufficient for all of the device's output pins, the lines associated with pins Q6 and Q7 were examined using an oscilloscope. The sole difference in the setup for testing in liquid nitrogen is the use of the first cryogenic probe. The prior probe was used because it is compatible with the card on which the device is installed and because the number of pins to be controlled with this probe is limited and controllable. In contrast to tests conducted at room temperature, the lines of the board mounted on the probe are conducted to the BNC connectors of the connector box to which the power supply and read/write pins of the Arduino UNO have been connected.

The test, taken from the datasheet of the stated product whose list of signals is depicted in Figure 4.7, intends to transmit a pulse to the DS serial input of the device and propagate it through all the outputs via the clocks of the two groups of registers, which are in anti-phase. Once the signal reaches the final Q7 output, the STCP is halted in order to test

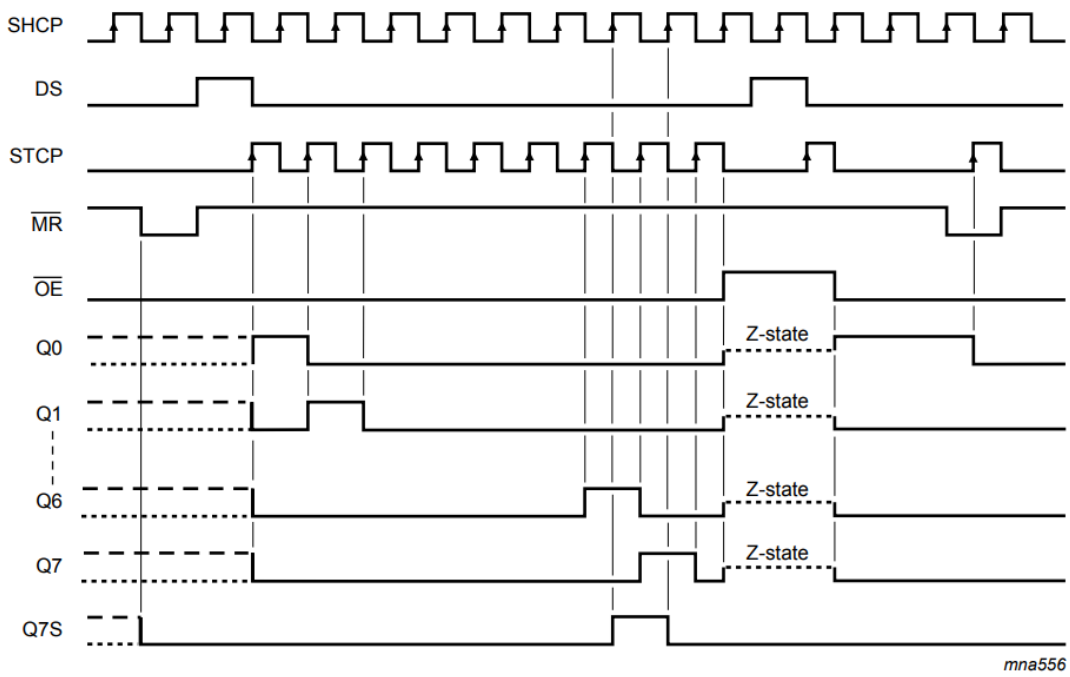

Figure 4.7: The test to which shift Registers were subjected is depicted in figure [3].

the OE, which is deactivated (active low), causing the outputs to transition to Z-state. At this time, a second pulse is given to the input, which, due to the rising edge of the STCP signal, is brought to the output of the storeging registers, where it waits for the output buffers to be rehabilitated, bringing the OE back down. As the initial and final command of the test, with the exception of the SHCP signal, which is a square wave with a 50 percent duty cycle present for the whole duration of the test, the preloaded values in the shift registers are reset with the MR signal enabled (active low) to ensure that all outputs begin and end in the same low value circumstance.

It is interesting to observe that the first pulse propagates first from the serial output Q7s and then manifests at the last parallel output Q7, because Q7s is the output of the last flip-flop of the group of shift registers, which are always in advance of their corresponding storage registers. If the two clock signals were identical, pins Q6 and Q7s would have identical trends. Appendix B contains the Arduino script that implements the test. As for the frequency of the clock signals, the chip's input frequency specification is certainly not the most stringent, and even if the temperature of the chip underwent faster-than-predicted changes, the datasheet indicates that the shift register would continue to operate correctly up to hundreds of MHz. Rather, it was desired to confirm that the shift register continued to operate appropriately at such low frequencies and was not designed to operate above a minimum frequency.

The shift register, which was examined under both temperature settings, exhibited no abnormal behavior and continued to function normally, even at 0.5Hz of operating frequency. Therefore, the TSSOP20, which was confirmed to be compliant with its system purpose, was additionally placed and validated on a mobile test board prior to being permanently soldered to the board that contains the QUASIX chip.

4.4. Control Panel and Firmware Interface

In this section, the bench control panel and its firmware interface will be described in detail, allowing the reader to comprehend the decisions made during the testing phase, as well as the control of the set of measurements to be performed on the ASIC.

4.4.1. Bench Control Panel

The control panel is a bench metal box containing a board developed expressly for this setup, an Arduino DUE attached to the board's underside, and many connectors and switches. As shown in Figure 4.8, on the top of the panel, there are 29 BNC connectors, each with its own switch, and two additional groups of switches: Md switches and digital line switches. Md switches, 1 through 4, are free "modules" that will be utilized in future applications; hence, they are not relevant to this thesis. The remaining eight digital switches activate and disable the digital lines used to transmit digital words programmed by the graphic user interface and driven via hardware by the Arduino DUE, and send them directly on the 9-wire multipole cable, one of which is allocated to the digital ground.

On the panel, there are eight power supplies, labeled Power DAC 1 through 4, as well as positive power supplies 1 and 2 and negative power supplies 1 and 2. The user interface allows for the configuration of the power supplies for the four "Power" DACs. There are five other DACs, numbered 1 through 5, whose outputs may likewise be modified via the interface. However, these were not designed to serve as power supply because they lack an output buffer. They are more suited as reference voltages than power supply due to their inability to deliver more than 10ma. All other BNCs permit connection through BNC cables to the mobile board connected to the probe.

The switches on each of these BNCs permit to link the connector either directly to the chip or to ground. For instance, if the BNC9 is linked to the gate of a transistor, when its switch is in the low position, the gate is grounded; if the switch is in the high position, whatever is attached to the BNC9 on the panel is brought to the gate.

Power supplies, DACs, and generic BNCs have a BNC type as a connector because,

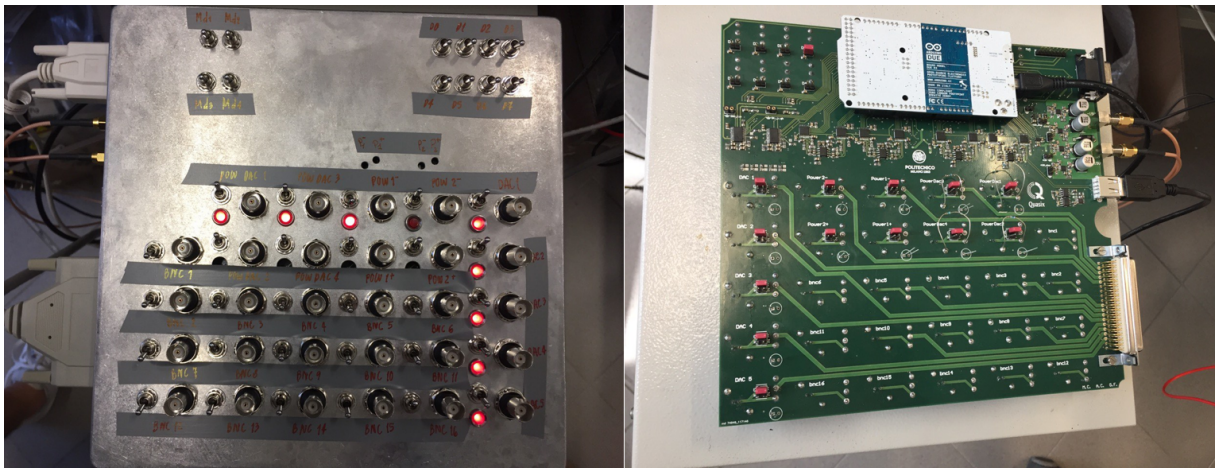

Figure 4.8: The control panel exploited during testing phase for the administration and automation of the set of measurements to be performed on the ASIC. On the left is a view of the device's exterior, including its primary connectors and switches. The underside of the internal PCB to which the Arduino UNO is connected is depicted on the right.

assuming that the Power DAC 1 connector is connected to the output of the corresponding power supply, but it has the need to read the current generated by the circuit with this specific connector, a power supply in this case would be useless because a measuring instrument should rather be connected. On the internal circuit board, near Power DAC 1 and 3, the negative power supply 1 and 2, and the DAC 1 through 5, there are "caps" that link the BNC to the corresponding power supply. By removing the cap the internal circuit is disconnected obtaining a simple BNC that can be connected to the measurement device. The BNC connections with these caps are additionally fitted with an LED that, when lighted, indicates that the respective BNC is connected to the board. If it is turned off, the BNC is detached and it may be attach whatever is required.

The power supplies 2, 3, and 4, as well as those adjustable with the trimmer, are equipped with an ADC for measuring the generated current, which is enabled by the Graphic User Interface. This feature is not available on the Power DAC 1.

The reading is accomplished by amplifying a voltage proportional to the currents flowing through a PGA, Programmable Gain Amplifier, whose voltage output is sent to an ADC that digitizes it via a multiplexer that controls all the power supplies. For the sake of simplicity, it was decided to define a single gain for all power supplies. In order to avoid saturating the PGA and the ADC, a minimal gain is set when the currents to be read are considerable. However, when the currents to be read are rather small, on the order of nA or even pA, the PGA gain can be increased to take advantage of the entire dynamic range of the ADC. In this instance, the gain is also programmed via the GUI, and its value can

range from below 1 up to 32.

The same holds true for the temperature sensor driven by a $10\mu A$ continuous current through a USB cable that directly links the panel to the connector box; the voltage that forms at its ends can be read by the PGA followed by the ADC. The gain of this PGA can be set independently of the power supply gain, as well as enable or disable the sensor reading. Finally, for DACs 1 to 5 only the voltage can be defined, but the current cannot be read.

4.4.2. Firmware Graphic User Interface

In Figure 4.9, the image of the user interface used to control via Arduino the internal board contained in the bench box is displayed. In the Status section, there is a switch to enable serial communication with the Arduino on the selected COM port (often COM3). If the "Arduino DUE" LED is green, the port is open and functioning; if it is red, an issue has occurred. If the "MCU busy" LED is lit in green, it signifies that Arduino is carrying out a task according to the instructions. If the light is dark green, it is awaiting a new command. The Terminal section displays as text on the screen every signal obtained by the interface, whether the command was executed correctly or not via "warnings/errors," and the response that this command generates in order to have control over the panel's behavior and the GUI itself. The "Terminal Clear" button clears the terminal. The DAC section allows for the management of the voltages supplied by the DACs, which are set to zero by default and have a complete scale of [-5V, +5V]. Entering a value between +5V and -5V displays the voltage value generated by the 16-bit DAC in the box. On the circuit board, a 10Ω series resistor is installed at the DAC output, with the option to change it and add a capacitance towards GND. Due to the fact that the maximum driveable capacitance is 4nF and the maximum current is 20mA, care must be taken.

In the power supply section, it can be choosen the channels that will measure the provided current. Simply select the desired channel and I n the text field, the current value in mA will be shown. As stated previously, the current cannot be read for the Power DAC 1. When the PGA that reads the current supplied is overloaded, the LED adjacent to each power supply illuminates bright red, in those cases it is often enough to reduce the gain of the PGA.

In the digital panel, it is possible to choose the voltage value associated with the high and low logical levels. For the shift registers, standard 0V - 5V levels are used. By checking the digital lines to be activated, you can select which lines the bit sequence will be transmitted on. Not checked lines always transmit a logical "0". In a dedicated

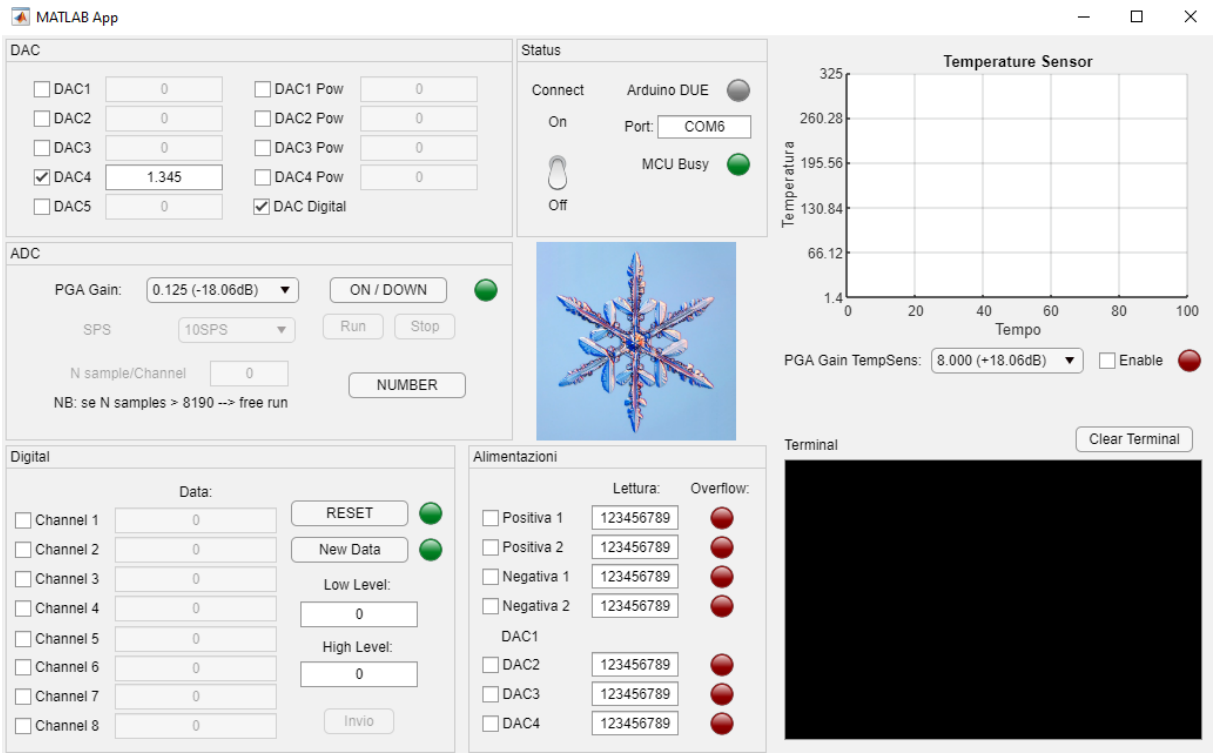

Figure 4.9: The Graphic User Interface used to control the custom board part of the bench control panel is displayed.

excel file, it is possible to specify, for each digital line, the pattern of up to 32 bits to be transmitted. When "New Data" button is clicked, the file is loaded, and when "Invio" is pressed, only the first two bytes for the specified channels are sent bit by bit. Then, by clicking "Invio" again, the last two bytes are sent. To send the same pattern again (from the initial transmission), "RESET" button must be pressed.

For what concerns the ADC panel, there is a box for selecting the sampling rate in Sample Per Second (10sps by default). However, a value of 1sps has been maintained, a more than enough frequency for constant currents readings; hence, fast readings are unnecessary. This section also displays the gain of the PGAs that measure the power supply currents. The current is measured at the head of a 100Ω resistor, thus $I_{Alim} \cdot 100\Omega \cdot G_{PGA} < 5V$. Additionally, the amount of samples to be taken for each selected channel can be specified. When 65535 is entered, the free-run mode is activated. At any time, the acquisition can be cancelled by pressing the stop button. It must be paid particular attention to the possibility of ADC saturation, which has a dynamic range of 2.5V. In the event of saturation, the terminal displays an error message. Lastly, a terminal is signaled if the value read by the ADC may have been corrupted during reading. In the final section about the temperature sensor, a graph depicts the sensor's temperature readings over time,

checking the little square to activate the data collection. Additionally, the corresponding PGA's gain can be specified, near the PGA's overflow led.

5 | Experimental Results

This chapter is intended to summarize the results derived from the previous design and simulations phases by describing the measurement outcomes of the finalized QUASIX chip. Following are also the characterizations of the erbium diodes realized by the CNR's research group in order to determine the optimal operating range for the correct operation of the diodes prior to their integration into the driving system.

5.1. Characterization of the QUASIX Chip

It was chosen to conduct the testing on a first test board without the erbium-doped diode, which will be used solely for chip validation. The resistance and capacity at the system output, which substitute the diode in its absence, might be desoldered after the validation, once the working diodes have been realized and can be mounted on the board. However, mounting on a new board the chip and diode to keep the previous one available for secondary inspections targeted on the chip may be a more practical solution.

The measurements may be categorized into four groups: the characterization of the temperature sensor, the validation of the pulse generator, the quasi-state characteristic of the Switched and Fast configuration, and the switching speed for the two typologies. All of these tests were conducted at room temperature and at 77K, with the exception of the integrated temperature sensor, which was characterized over the whole operating temperature range. Starting with the integrated temperature sensor, its complete structure is presented in the figure for simple reading.

To measure the temperature, a Proportional To Absolute Temperature (PTAT) circuit has been designed, Figure 5.1. The working principle of the circuit is based on the parasitic bipolar transistors available in a CMOS process, Q1 and Q2, biased with the same emitter current I_E by the cascode current mirror M5-M8. Since the two bipolar transistors have a different area, the emitter-base voltage V_{EB} are different generating a ΔV_{EB}, across the emitter nodes of two BJTs, linearly dependent on absolute temperature. Since the source voltages of M1 and M2 are the same due to the equality of the currents, the ΔV_{EB} defines

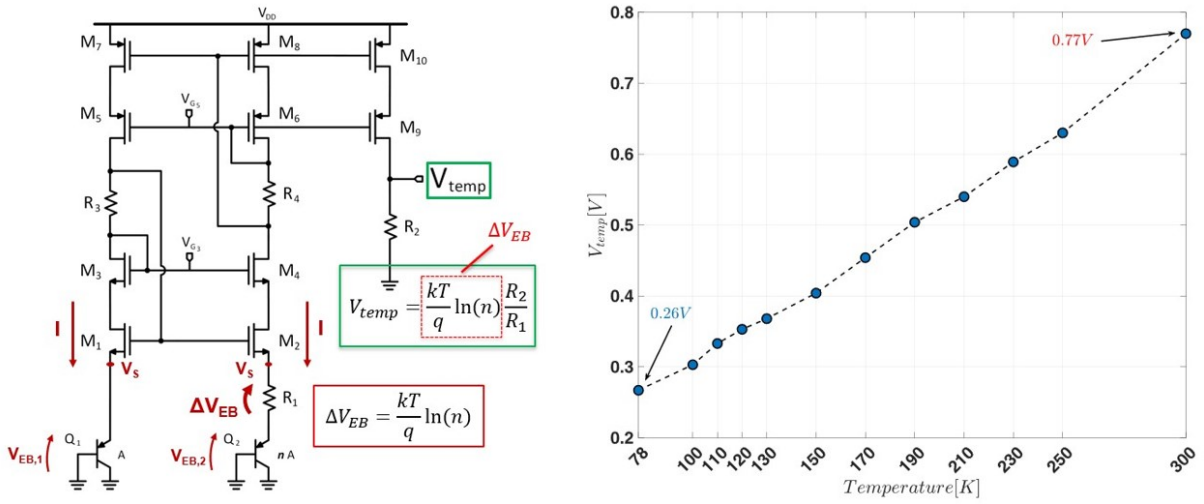

Figure 5.1: Schematic and experimental characteristic on a wide temperature range, from 77K to 300K, of the temperature sensor.

the voltage drop on the resistor R1 and consequently the current in the PTAT circuit. The PTAT output current is mirrored on the resistor R2 producing the output voltage (V_{temp}) [18].

The measurement requires the use of the calibrated discrete temperature sensor DT-670 [1]. Therefore, when the temperature changed, using the calibrated diode, it was possible to convert the output voltage signal of the integrated sensor into the respective working temperature value of the photon source. The experimental results show good linearity over a wide temperature range (77K - 300K), as demonstrated in Figure 5.1. At 77K the measured Vtemp value is practically identical to the simulated value of about 265mV compared to the simulated value of 232mV, with the voltage V_{switch} at 0V, while with V_{switch} at 5V (off) the measured value becomes 292mV. At room temperature with $V_{switch} = 0V$,

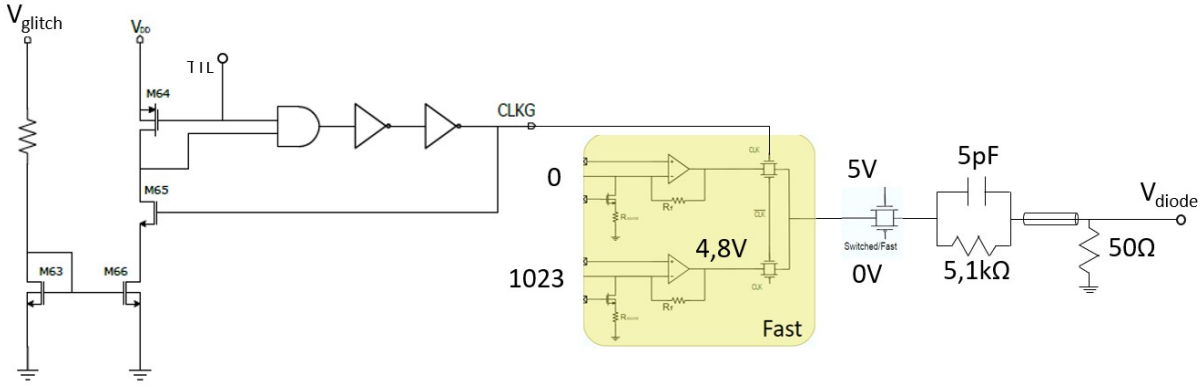

Figure 5.2: Illustration of the pulse generator and the following driven circuitry.

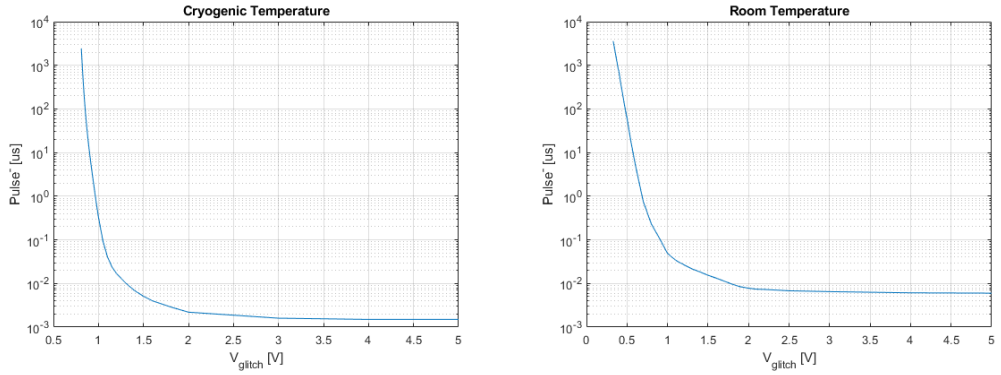

Figure 5.3: Sperimental results of the pulse generation test, at room and cryogenic temperature.

measurements and simulations are different, respectively 767mV and 900mV, and with them also the slope of the line that best approximates the curve, whose proportionality factor $k = 2.27mV/°C$, compared to the approximately $k = 3mV/°C$ simulated. The obtained slope and the measured slope are different, but considering mismatches and variability they are however coherent values with the simulated values from Montecarlo analysis, which has shown a proportionality factor at 3σ of $2.15\frac{mV}{°C}$ in the temperature range from RT down to 233K.

In order to facilitate comprehension of the next test, the Figure 5.2 depicts what concerns of the pulse generator and the following driven circuitry. An external TTL signal, generated by an arbitrary pulse generator and led to the chip via one of the high frequency MMCX cables, activates the variable pulse generator by controlling an internal AND gate. Thus, the signal is delayed and inverted, transforming into a digital signal that acts on the output switches of two DACs to switch the output voltage of the entire system. The delay is provided by a cascade of an AND gate and two inverters, with a minimum duration for the scope of this application of 5ns and a maximum duration of 100ns, adjustable via a second external signal, V_{glitch}.

The experimental results shown in the Figure 5.3 are obtained at both the temperature conditions and at varying V_{glitch}. At 300K, the V_{glitch} has been varied from 330mV up to 5V, resulting in a gradual decrease of the duration of the generated pulse, starting from a window of 3.6ms down to a duration of 6ns. The same procedure was also applied at cryogenic temperature, at which, however, the voltage that regulates the duration of the pulse this time has started from 810mV to reach again 5V, thus obtaining time windows from 2.434ms down to 1.5ns.

Providing a concise summary of the structure shown in Figure 5.4, the designed DAC has

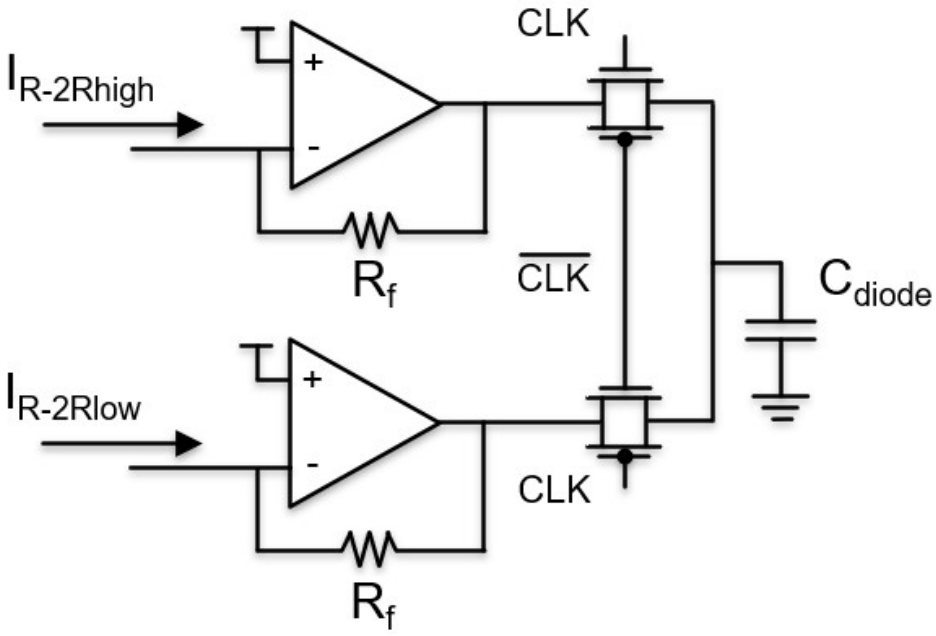

Figure 5.4: Illustration of the driver.

a voltage range of 0 V to 5 V and 10 bits. The adopted topology is an R-2R structure, which is more robust to temperature fluctuations on the first order. In addition, to obtain more monotonicity and greater accuracy of the static characteristic, a segmented design is employed in which the least significant 6 bits are binary-weighted and the remaining 4 bits, where non-idealities have a greater impact, are thermometric-weighted.

Regarding the DAC output amplifier, a rail-to-rail amplifier is utilized to take advantage of the complete 5V dynamic range. As previously stated, the pulse generator generates the control signal to switch between the two DACs, starting from an external trigger signal that determines the clock signal's repetition rate. The duration of the pulse can be varied from a few nanoseconds to hundreds of nanoseconds by an external voltage V_{glitch}.

An automatic measurement was made to obtain the quasi-static characteristic of the DACs. This measurement consists in automatically generating the digital signal send to the shift registers and, starting from the lowest value corresponding to the code 0, the input data increases every 100ms. The output generated by the driver was monitored using an oscilloscope, so that all codes could be scanned completely and autonomously and the output DAC value for each input code could be obtained.

From a first phase of measurements, the quasi-static characteristic of the driver turned out to be that of a 9-bit DAC, both for the "Fast" configuration and for the "Switched". In fact, when the input was provided with the digital values corresponding to the 1024

levels obtainable with 10 bits, the output of the DACs started to increase only when exceeded the digital code 480, that is half of the input dynamics was ineffective. It should be added that the "Switched" DAC characteristic was only achieved after fixing an unwanted oscillation issue at the trans-impedance amplifier output. It was thought that these oscillations were due to a positive feedback cause by a capacitive coupling between the output and the current generator gate that defines the DAC offset.

To mitigate this problem, about $10\mu F$ capacitance was added to the board at the gate of the two current generators of the two DACs belonging to the "Switched" architecture. One of the two DACs gave positive results, while the other still had oscillations, which suggests that the solution is another and will have to be investigated in future. It was later discovered that by bringing the resistive network's supply voltage to a value of 3.91V, the characteristics of 10-bit DACs appears at the output. At room temperature, polarizing one of the two gates of the current generators that regulate the output voltage offset to 0.84V while the other to 0V, to avoid oscillations, the resulting characteristic exploits all the input digital codes. This works both for the architecture "Switched" and "Fast" with an INL of less than -3LSB and a DNL of less than 0.5LSB. At 77K, polarizing instead both gates at 1.09V, a different curve gain makes the last 30 codes ineffective, still obtaining an INL lower than -3LSB, as in the previous case, and a DNL that does not exceed an LSB.

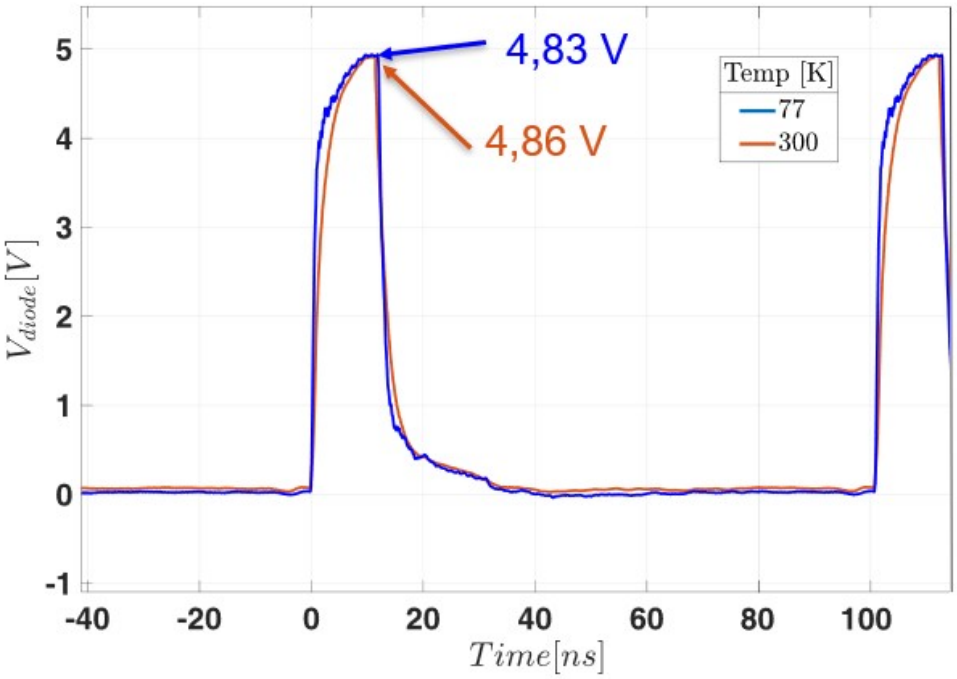

Figure 5.5: Final dinamic performances of the driver.

During the test to obtain the switching speeds, a resistance of$5.1k\Omega$ and a load capacity of 4.7pF were put in series at the output of the driver. The clock signal is led to the pulse generator by a high-frequency cable, while the output is read by an oscilloscope, whose input has been set to 50Ω to adapt the impedance in order to avoid reflections or capacitive loads due to the parassitism of the cable to be driven.

In conclusion, the dynamic performance of the driver has been characterized and reported in Figure 5.5. The system is able to drive a capacitance of 5pF with a pulse duration of 10ns at a frequency of 10MHz. With digital input ranging from 0 to 1024, pulses of this duration lead to a reduced output dynamic range of about 2.7LSB, reaching a maximum voltage of 4.86V at room temperature and 4.83V at 77K.

5.2. Erbium Diodes

The CNR research team manufactured two Erbium diode samples designated 005 and 007. Each sample collects a group of diodes, each of them is composed of a n pad (left) in which is restricted a phosphorus doping, a p pad (right) doped with boron, and a central square area doped with erbium and oxygen. Each diode of the set is differentiated by the size of the erbium- and oxygen-doped region; however, some of the diodes may not be measurable due to manufacturing flaws. In this scenario, sample 005 has measurable diodes with side $100\mu m$, two with $50\mu m$, $15\mu m$, $1\mu m$, and $0.48\mu m$, whereas sample 007 contains diodes with side $100\mu m$, $50\mu m$, and $15\mu m$ that survived the manufacturing process.

Since erbium is an electrical donor, it was intended to prevent the formation of an intrinsic zone between erbium and boron. For this reason, the boron doping is not limited to the right pad, but it is also present in the corresponding junction zone and in the central square, making a 500nm overlapping with the doping in erbium. This is true for all structures of both samples, with the exception of the 480nm diode, in which boron doping begin exactly where erbium doping stops, with no overlap. The left junction region, on the other hand, is erbium-doped so that there is no intrinsic zone between the two n-type dopings. The only difference between sample 007 and the other is the amount of oxygen utilized to activate the erbium in the centre square; in sample 007 there is half of the amount of oxigen present in the other sample.

5.2.1. Electrical Characterization of the 005 Sample

After gluing and bonding the sample, a microscope examination revealed that all connections were successful. To be considered, it was initially determined that all equipment

were compatible and free of fractures. The samples were adhered to a test board with a header-type connector, in order to polarize the samples using the Keithley 4200-SCS measurement.

After completing the measurement setup, the I-V curve of each diode was measured. The measurement consists in varying the anode voltage throughout the range of -0.5V to 0.5V while measuring the corresponding current with the cathode voltage remaining constant at 0V. This voltage range was selected so that the devices would not be subjected to undue strain. During the test, all devices were kept in the dark to avoid the effect of any photocurrents.

Side [μm]	Cathode range	Forward 0.5V	Reverse -0.5V
100 (HG)	$1\mu A$	146.8 nA	-55.33 pA
50 (LJ)	Auto	103.3 nA	-19.45 pA
50 (KI)	$1\mu A$	138.9 nA	-78.15 pA
15 (BA)	$1\mu A$	34.59 nA	-253.4 pA
1 (CD)	$1\mu A$	34.64 nA	-64.94 pA
0.48 (FE)	$1\mu A$	643.2 nA	-19.45 nA

Table 5.1: In the table are compiled the currents corresponding to the various diodes relative to the first measurement, which consisted of a voltage sweep from -0.5V to 0.5V, with the anode current range set to "$1\mu A$. Each diode Additionally, each diode has been identified with a couple of letters, which are useful for mapping the connections and distinguishing the two $50\mu m$ diodes."

The reported characteristics demonstrate that the devices behave "similarly" to a p-n junction diode. However, as demonstrated by the graph Figure 5.6:

- the characteristics are not optimal: it can be observed an exponential trend in forward bias, but not with the desired exponent;
- the impact of the size of the Er-doped area is unclear;
- The $480nm$ diode is abnormal: the reverse bias current is significantly higher than that of the other devices; in forward bias, the pattern is not exponential but more closely resembles a power law with 2.5 as exponent.

As reported in Table 5.1 the measured currents are not consistent with the diode sizes. For instance, with equal forward polarization applied to their nodes (+0.5V):

- the two $50\mu m$ diodes are crossed by two currents that differ by approximately $40nA$ on a total current of about 100nA;
- in first approximation, the ratio of the sides of two diodes must equal the ratio of the currents crossing them, a relationship that exists only for the diodes LJ and BA.

Following the optical measurements, which will be discussed later, a crack emerged on the $1\mu m$ diode along the connection between the pad and the erbium-doped zone that was not there previously. In addition, some diodes had to be reconnected since many connections were damaged. As a result, a second set of measurements, whose outcomes are depicted in Figure 5.6 and reported in Table 5.2, similar to the previous ones was conducted, with the only difference being that the voltage sweep range was expanded from -1.2V to +1.2V, with the assurance that this range did not exert substantial strain on the devices.

Side [μm]	Forward 1.2V	Forward 0.5V	Reverse -0.5V	Reverse -1.2V
100 (HG)	43.59 μA	148.7 nA	-3.226 nA	-4.356 nA
50 (LJ)	76,28 μA	101,4 nA	-2,484 nA	-2,712 nA
50 (KI)	103.9 μA	142.0 nA	-3.226 nA	-3.319 nA
15 (BA)	37.05 μA	45.41 nA	-3.260 nA	-2.864 nA
1 (CD)	34.31 μA	39.98 nA	-2.983 nA	-2.657 nA
0.48 (FE)	3.568 μA	785.6 nA	-55.90 nA	-88.29 nA

Table 5.2: The table displays the currents corresponding to the different diodes collected during the second measurement, which consisted of a voltage sweep from -1.2V to 1.2V with "Best Fixed" set as the current range for the nodes.

The behavior of the diodes in forward polarization regime did not vary significantly, except for the $480nm$ diode, which at +0.5V is traversed by a current that is $142nA$ higher than the previous measurement, nearly 20% higher. What has changed is the behavior of the devices in reverse bias regime, with the exception of the $480nm$ diode, which brings a larger reverse saturation current, as previously occurred. This may be due to the inclusion of "Best Fixed" as the node range setting during the measurement setting phase, which establishes a single, optimal range for all measurements. In order to obtain more precise readings, the cathode range was set to "Auto," and as a result, the values of the inverse saturation currents were identical to those of the initial measurement.

In conclusion, the polarized live current of the $480nm$ diode at +0.5V is approximately 20% more than the first results. In addition to this, the diodes of sample 005 exhibit no

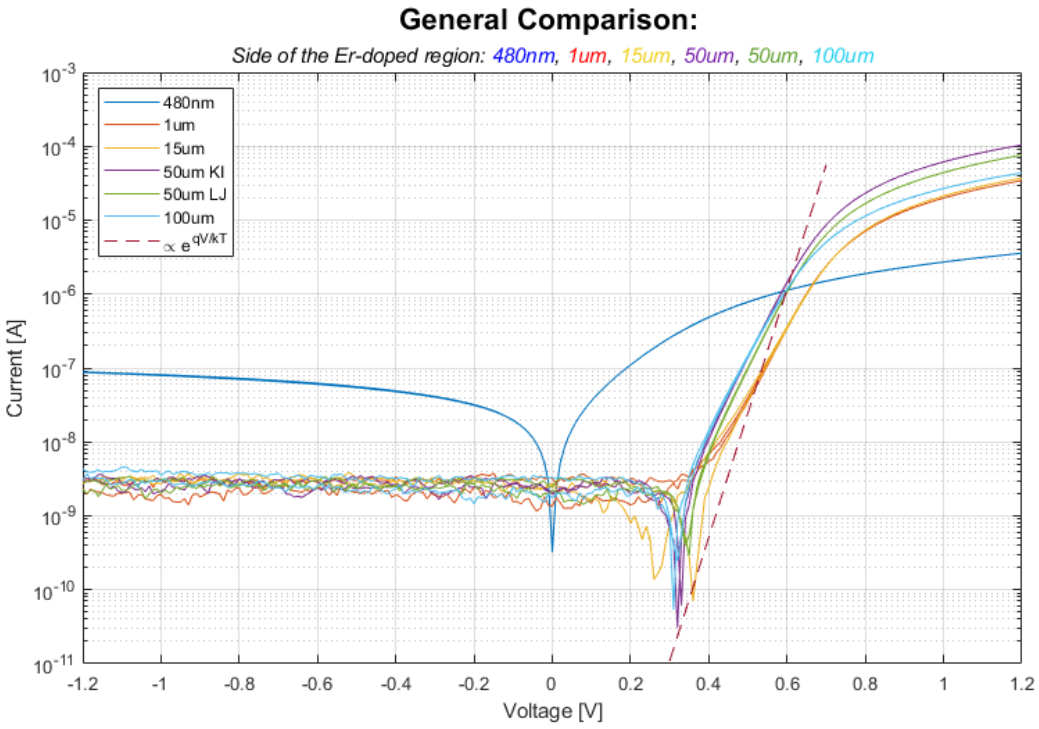

Figure 5.6: The characteristics of each diode in sample 005 are presented on a logarithmic scale graph, in comparison with the unfulfilled exponential trend. As voltages approach +1.2V, it can be seen that the curve becomes resistive. Only the graph of the second measure with the range [-1.2,1.2] has been reported to avoid redundancy.

electrical behavior change from the initial data.

5.2.2. Electrical Characterization of the 007 Sample

During the bonding procedure for this sample, one of the $100\mu m$ side diode pads was damaged by excessive vibration. Measurements continued for the remaining two diodes. Also for this sample, measurements provided for a voltage sweep similarly to the previous test, but the variation range of the anode was [-1.2V, 1.2V].

The device with a side of $15\mu m$, whose characteristic is shown in Figure 5.7, exhibits a resistive behavior across its entire operating range, with a resistance of around $40k\Omega$. A possible cause can be traced back to parallel spurious resistances:

- a $40k\Omega$ surface resistance of the metallization in parallel to the diode, but such a high resistance value requires a thin, narrow, and long metallisation path, and only the first condition appears possible in this instance;
- or due to some unwanted path that connects the two pads underneath the diode.

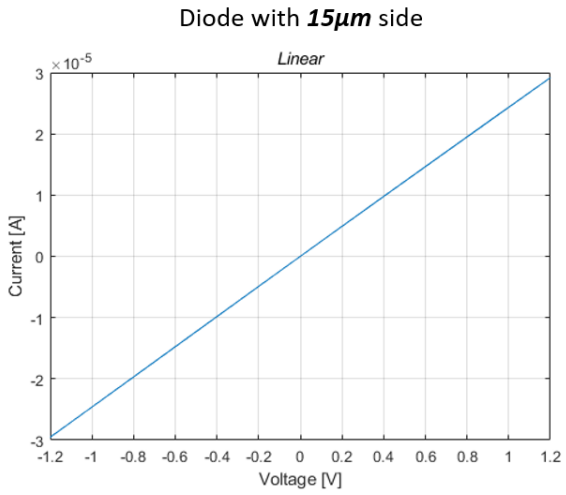

Figure 5.7: Characteristic of the diode with $15\mu m$ side manifesting a resistive behaviour with $R_{eq} = 40k\Omega$ across its entire operating range.

Instead, as demonstrated in Figure 5.8, the characteristic of the $50\mu m$ side diode lacks proper symmetry, therefore we cannot attribute this tendency to the two rectifying junctions that, under both polarization conditions, would have alternately stayed in reverse, making the diode non-conductive. In this instance, a symmetrical characteristic of the two junctions in reverse polarization ought to have developed. Unfortunately, it is not known which zone has forward polarization and which zone has reverse polarization, as there is no apparent differentiation between the magnitudes of the two polarization zones or a pattern that can be traced vaguely to that of a p-n junction diode. For these reasons,

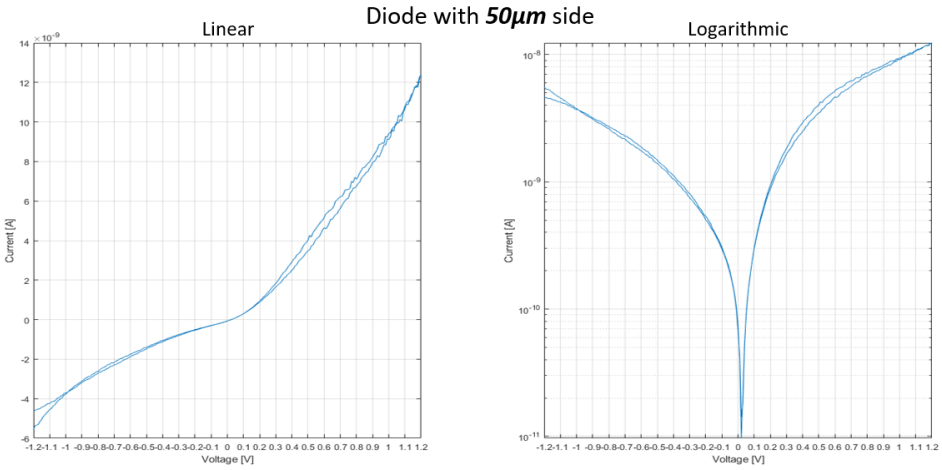

Figure 5.8: Characteristic of the diode with $50\mu m$ side displayed in linear scale (left) and logarithmic scale (right). In forward polarization regime, the trend of the current is strongly linear, with $R_{eq} = 92.5M\Omega$ plainly observable.

we can only suppose, as in the previous situation, that a parallel resistance can increase the current under conditions of reverse polarization, in addition to a notably large series resistance that reduces the current under conditions of direct polarization. In this regard, evaluating the trend of the characteristics reveals a linear region with a resistance of approximately 92.5 MOhm, a very high resistance but not so high as to suggest an open circuit.

As was also determined by the tests conducted at the probe station, the diodes exhibit aberrant behavior that is traceable to extremely large resistive elements that influence their currents. Due to the absence of p-n junction diode electrical activity, nothing is expected of their photoluminescent and photogenerative properties.

5.2.3. Optical Characterization of the Diode Samples

The optical characterization was performed on an optical bench in the Nanophotonics and Plasmonics laboratory of the Politecnico di Milano's physics department. The objective of this characterization was to determine, at room temperature, whether the devices of samples 005 and 007 exhibit electroluminescence and photoluminescence, as well as which could be the optimal operating regime for the application at hand, in order to better address the electronic design specifications. In addition, the devices made in the Molecular Nano-Engineering Lab of the Waseda University (Japan), as previously characterized in the prior thesis [17] were also taken up for comparative purposes.

Before proceeding with the optical measurement, using a white light, a retractable mirror, and a monitoring chamber, the sample of interest was properly aligned with the reading optics. The device to be measured was illuminated by the white light, which was only activated during the placement of the sample. This light, which has been reflected by the sample itself, is then directed towards the monitoring chamber by way of a retractable mirror, which, when raised and positioned vertically, deflects the light emanating from the monitoring chamber. Except while the sample is being positioned, all of the sample's light is directed towards the photodetector. The measurements are performed in the dark using a microscope to collect the photons released by the test sample and a special lens made of mirrors and a beam-splitter to direct them to a SPAD capable of counting the photons emitted in the wavelength range of interest. For photoluminescence and photogeneration experiments, an optical pump source that will illuminate the diode with $900nm$ and $1550nm$ light was prepared.

The first optical measurements were performed on sample 005 and consisted of the electroluminescence map on a chosen area straddling the junction between the central square

and one of the pads. In the analysis of electroluminescence intensity, the diode in reverse regime at -0.5V and in forward bias at 0.5V was evaluated.

From the first optical measurements made, no emission from erbium doped diodes was revealed, neither from former Waseda diodes nor from QUASIX ones, despite the employment of a SPAD for detection. Apparently, there are no precise explanations; we can only theorize about plausible causes:

- During this initial measuring session, the lens that focuses light on the SPAD received little scrutiny. The focus may not have been properly calibrated, decreasing the efficiency of data collecting.
- In addition, electroluminescence measurements were performed with filters in front of the SPAD, despite the fact that in the absence of the optical pump source, used for photoemission, no filter should be employed, as the only observable light is the light emitted by the sample.
- Another possible cause is an aging phenomena of Japanese nanodiodes, which is likely owing to the fact that these nanodiodes are almost superficial devices, that is, poorly protected.
- With the CNR diodes, moderate currents have been maintained, and the reverse breakdown has not been investigated, as it has been deemed prudent to behave with caution in the absence of certainty regarding the optical setup and the limits of the devices.
- For various alignment tests, the sample was illuminated with a $900nm$ laser, a wavelength close to that previously employed (it was $980nm$). One difference, however, is the type of laser, which is an impulsive femtosecond laser this time. Short yet powerful impulses may have harmed the diodes.

All tested diodes were polarized at a greater voltage during successive testing, reaching +1.2V forward voltage and -1.2V reverse voltage. In addition, the optical filters were eliminated in the belief that doing so would allow the SPAD to detect a few more photons at 1550nm, which was the case.

The emissions collected from the Waseda devices are equivalent to those obtained in the initial thesis work [17]. However, after applying a low-pass filter with a cut-off wavelength of $1450nm$ in order to select the spectral region of interest, there was almost no signal trace, a result that is not very encouraging as it suggests that the revealed signal is a queue and it cannot be assumed a peak emission.

As for the samples of the CNR research group, the $100\mu m$ device generates a negligible amount of current, on the order of nA, and optical analysis reveals no emission, despite the fact that this sample's alignment should not be critical, as it is very extensive and the SPAD has always been properly aligned to it. The $1\mu m$, although it exhibited consistent electrical behavior with previous measurements, lacked photoemission. In addition, a crack developed on the anode of the latter diode, and as a result of this damage, the signal immediately diminished. The $480nm$ device exhibited the expected electrical behavior, bringing to 1.2V direct polarization a current of around $4\mu A$, as at 0.5V the characteristic is no longer exponential and tends to be linear. Its behavior is comparable to that of Wasaeda, since, when irradiated by a $1550nm$ laser, it is the only one to generate a somewhat larger current. Unfortunately, there was no tunable laser to confirm that this photocurrent is dependent on erbium. In fact, the photocurrent increased even with white light from the lamp. No photoemission has been reported in this case neither. The bondings of the $50\mu m$ devices have been damaged while looking for focus, before such diodes could be measured.

During this second session of testing, no photosignals from the new devices were detectable. Compared to the approximately $10\mu A$ flowing through the Wasaeda devices, the 005 sample diodes carry less current overall.

6 | Conclusions and future developments

This thesis work has focused on the characterization of a fully integrated CMOS driving circuit for a single-photon emitting diode for quantum cryptography in space, within the QUASIX project. In this preliminary phase of the project, the driving circuit has been designed to ensure high flexibility and temperature robusteness in the driving of the diode. The architecture based on two DACs permits the diode to be driven with a repetition rate of 10 MHz, a pulse duration of 20 ns, and a voltage range of 0 V to 5 V. The static performances of the DAC, evaluated at both room temperature and cryogenic temperature, and the good linearity of the integrated temperature sensor permit accurate control of the erbium-doped diode within the operating temperature range of 77 K to 300 K. The circuit's high driving flexibility and static and dynamic performance are a good starting point for a compact, low-cost optoelectronic system for satellites. The experimental validation of the architecture has shown some critical aspects in the "Switched" architecture. In fact, further research on the causes of certain oscillations is required..

Regarding the light emitting diode, the results obtained in the laboratory of the physics department on the tested samples, suggest that the absence of photo- and electroluminescence is due to an inefficiency in the excitation of the electro-emitting centers, but even more likely to the presence of defects along the discontinuities of planar devices with an intrinsic zone thickness of 220nm. It has been hypothesized that the discontinuity between the silicon and the air and other in-depth defects restrict or even prevent the optical activation of the erbium. In the so-called sandwich structure devices manufactured many years ago in Catania, which was developed vertically, photo- and electroluminescence are manifested clearly. Therefore in these devices impurities do not have such a significant impact being the intrinsic silicon area sufficiently distant from impure zones. Other attempts to collect photons emitted by the diode will be carried out with a cryogenic single-photon detector, which can provide significantly higher sensitivity compared to the current detector based on SPAD.

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A | Appendix A

The models of the adopted CMOS technology extracted at 77K are included in this Appendix.

```
--------------------------------------------------------------------------------
//****NMOS 1v8lvt****
simulator lang = spectre
model nmos bsim3v3
//*** Flag Parameter ***
+version = 3.3                  binunit = 2                     mobmod = 1
+capmod = 3                     nqsmod = 0                      minr = 1E-60
+type = n
//*** Geometry Range Parameter ***
+lmin = 1.485E-7                lmax = 1                        wmin = 3.168E-7
+wmax = 1
//*** Process Parameter ***
+tox = 2.8E-9                   xj = 2E-7                       nch = 4.232778E17
//*** dW and dL Parameter ***
+wint = 1.15186E-7              wl = -6.103623E-15              wln = 1
+ww = -1.349498E-14             wwn = 1                         wwl = 1.592066E-22
+lint = -2.829919E-7            ll = 4.5E-15                    lln = 1
+lw = 9.885207E-15              lwn = 1                         lwl = 5.375884E-22
+dwg = -2.633889E-8             dwb = -5.125098E-8              xl = 0
+xw = 0
//*** Vth Related  Parameter ***
+vth0 = 0.433218                k1 = 0.357413                   k2 = -0.016115
+k3 = 24.549813                 k3b = 0                         w0 = 1.250608E-6
+nlx = 4.69278E-7               dvt0 = 2.2                      dvt1 = 0.53
+dvt2 = -0.032                  dvt0w = 0                       dvt1w = 5.3E6
+dvt2w = -0.032                 ngate = 1E30
```

```
//*** Mobility Related Parameter ***
+u0 = 0.205749                  ua = -1.551083E-9           ub = 2.940786E-18
+uc = 1.243524E-10              vsat = 9.032008E4           a0 = 1.030856
+ags = 0.920433                 b0 = -3.196138E-8           b1 = 0
+keta = -0.076875               a1 = 0                      a2 = 1
+rdsw = 15.311436               prwb = 0.75                 prwg = 0
+wr = 1
//*** Subthreshold Related Parameter ***
+voff = -6.95275E-2             nfactor = 6.089091          eta0 = 0.08
+etab = -0.07                   dsub = 0.56                 cit = 0
+cdsc = 2.4E-4                  cdscb = 0                   cdscd = 0
//*** Output Resistance Related Parameter ***
+pclm = 8.807307                pdiblc1 = 2.538032          pdiblc2 = 4.25381E-2
+pdiblcb = 0                    drout = 0.202984            pscbe1 = 2.419161E7
+pscbe2 = 1.5E-10               pvag = 2.791691             delta = 0.01
+alpha0 = 0                     beta0 = 0
//*** NQS Parameter ***
+elm = 0
//*** Capacitance Parameter ***
+xpart = 0                      cgso = 0                    cgdo = 0
+cgbo = 0                       ckappa = 0.6                cf = 0
+clc = 1E-7                     cle = 0.6                   dlc = 0
+dwc = 0                        vfbcv = -1                  cgsl = 0
+cgdl = 0
//*** Souce/Drain Junction Diode Model Parameter ***
+ldif = 0                       hdif = 0                    rsh = 0
+rd = 0                         rs = 0                      rsc = 0
+rdc = 0                        cj = 5E-4                   mj = 0.5
+mjsw = 0.33                    cjsw = 5E-10                cjswg = 5E-10
+mjswg = 0.33                   js = 1E-4                   jsw = 0
+n = 1                          pbsw = 1                    pb = 1
+pbswg = 1
//*** Temperature Coeffient ***
+tnom = -196.15                 ute = -1.5                  kt1 = -0.11
+kt1l = 0                       kt2 = 0.022                 ua1 = 4.31E-9
+ub1 = -7.61E-18                uc1 = -5.6E-11              at = 3.3E4
+prt = 0                        xti = 3
```

```
//*** Stress Effect Related Parameter ***
+saref = 5E-6                  sbref = 5E-6                  wlod = 0
+ku0 = 0                      kvsat = 0                     kvth0 = 0
+tku0 = 0                     llodku0 = 0                   wlodku0 = 0
+llodvth = 0                  wlodvth = 0                   lku0 = 0
+wku0 = 0                     pku0 = 0                      lkvth0 = 0
+wkvth0 = 0                   pkvth0 = 0                    stk2 = 0
+lodk2 = 1                    steta0 = 0                    lodeta0 = 1



--------------------------------------------------------------------------
//****PMOS 1v8lvt****
simulator lang = spectre
model nmos bsim3v3
//*** Flag Parameter ***
+version = 3.3                binunit = 2                   mobmod = 1
+capmod = 3                   nqsmod = 0                    igcmod = 0
+igbmod = 0                   minr = 1E-60                  type = p
//*** Geometry Range Parameter ***
+lmin = 1.485E-7              lmax = 1                      wmin = 3.168E-7
+wmax = 1
//*** Process Parameter ***
+tox = 2.8E-9                 xj = 2E-7                     nch = 1.75E18
//*** dW and dL Parameter ***
+wint = 1.988357E-7           wl = -1.078234E-14            wln = 1
+ww = -8.231988E-14           wwn = 1                       wwl = 9.221978E-21
+lint = 7.286212E-9           ll = 2.014246E-15             lln = 1
+lw = 4.883937E-15            lwn = 1                       lwl = -3.509821E-22
+dwg = -1.98808E-8            dwb = -3.3E-8                 xl = 0
+xw = 0
//*** Vth Related  Parameter ***
+vth0 = -0.75853              k1 = 0.780149                 k2 = -0.03348
+k3 = 27.75359                k3b = 0                       w0 = 1.25E-6
+nlx = 2.878719E-8            dvt0 = 4.409112               dvt1 = 0.265
+dvt2 = -0.032                dvt0w = 8.345703              dvt1w = 2.65E6
+dvt2w = -0.016               ngate = 1E30
```

```
//*** Mobility Related Parameter ***
+u0 = 3.018668E-3              ua = -2.061358E-9            ub = 1.696604E-18
+uc = -1.073745E-10            vsat = 1.114797E5            a0 = 0.247902
+ags = 2.48419E-2              b0 = 1.350542E-7             b1 = 1.998954E-7
+keta = -0.209746              a1 = 0                       a2 = 1
+rdsw = 457.892985             prwb = -1.249708             prwg = -0.473116
+wr = 1
//*** Subthreshold Related Parameter ***
+voff = -0.103613              nfactor = 7.583755           eta0 = 0.083994
+etab = -0.05                  dsub = 0.339017              cit = 0
+cdsc = 3.6E-3                 cdscb = 0                    cdscd = 0
//*** Output Resistance Related Parameter ***
+pclm = 2.116087               pdiblc1 = 0                  pdiblc2 = 1.215669E-4
+pdiblcb = 0                   drout = 1.008                pscbe1 = 2.419161E7
+pscbe2 = 1.5E-10              pvag = 12.733734             delta = 0.01
+alpha0 = 0                    beta0 = 0
//*** Gate Dielectric Tunneling Current ***
+nigc = 1                      aigc = 0.012                 bigc = 2.8E-3
+cigc = 2E-3                   aigbacc = 0.012              bigbacc = 2.8E-3
+cigbacc = 2E-3                nigbacc = 1                  aigbinv = 0.014
+bigbinv = 4E-3                cigbinv = 4E-3               eigbinv = 1.1
+nigbinv = 3                   ntox = 1                     toxref = 1.5E-8
+pigcd = 1                     poxedge = 1                  dlcig = 0
+aigsd = 0.012                 bigsd = 2.8E-3               cigsd = 2E-3
//*** NQS Parameter ***
+elm = 0
//*** Capacitance Parameter ***
+xpart = 0                     cgso = 0                     cgdo = 0
+cgbo = 0                      ckappa = 0.6                 cf = 0
+clc = 1E-7                    cle = 0.6                    dlc = 0
+dwc = 0                       vfbcv = -1                   cgsl = 0
+cgdl = 0
//*** Souce/Drain Junction Diode Model Parameter ***
+ldif = 0                      hdif = 0                     rsh = 0
+rd = 0                        rs = 0                       rsc = 0
+rdc = 0                       cj = 5E-4                    mj = 0.5
+mjsw = 0.33                   cjsw = 5E-10                 cjswg = 5E-10
```

```
+mjswg = 0.33                  js = 1E-4                    jsw = 0
+pbsw = 1                      pb = 1                       pbswg = 1
//*** Temperature Coeffient ***
+tnom = -195.15                ute = -1.5                   kt1 = -0.11
+kt1l = 0                      kt2 = 0.022                  ua1 = 4.31E-9
+ub1 = -7.61E-18               uc1 = -5.6E-11               at = 3.3E4
+prt = 0                       xti = 3
//*** Stress Effect Related Parameter ***
+saref = 5E-6                  sbref = 5E-6                 wlod = 0
+ku0 = 0                       kvsat = 0                    kvth0 = 0
+tku0 = 0                      llodku0 = 0                  wlodku0 = 0
+llodvth = 0                   wlodvth = 0                  lku0 = 0
+wku0 = 0                      pku0 = 0                     lkvth0 = 0
+wkvth0 = 0                    pkvth0 = 0                   stk2 = 0
+lodk2 = 1                     steta0 = 0                   lodeta0 = 1
//*** GIDL Current Parameters ***
+agidl = 0                     bgidl = 2.3E9                cgidl = 0.5
+egidl = 0.8
```

```
//****NMOS 5v0rvt****
simulator lang = spectre
model nmos bsim3v3
//*** Flag Parameter ***
+version = 3.3                 binunit = 2                  mobmod = 1
+capmod = 3                    nqsmod = 0                   minr = 1E-60
+type = n
//*** Geometry Range Parameter ***
+lmin = 7.92E-7                lmax = 1                     wmin = 7.92E-7
+wmax = 1
//*** Process Parameter ***
+tox = 1.7E-8                  xj = 2E-7                    nch = 9.105451E16
//*** dW and dL Parameter ***
+wint = 2.378065E-7            wl = 6.993175E-14            wln = 1
+ww = -7.962465E-14            wwn = 1                      wwl = -1.324177E-19
```

```
+lint = -8.007658E-7          ll = 3.553326E-13          lln = 1
+lw = -4.271859E-13           lwn = 1                    lwl = -1.158698E-20
+dwg = -5.260553E-9           dwb = -3.500977E-8         xl = 0
+xw = 0
//*** Vth Related  Parameter ***
+vth0 = 1.114168              k1 = 1.413977              k2 = -0.227107
+k3 = 0.356031                k3b = 0.473261             w0 = -4.378138E-7
+nlx = -5.502764E-7           dvt0 = 1.98                dvt1 = 0.53
+dvt2 = -0.048                dvt0w = 0                  dvt1w = 5.3E6
+dvt2w = -0.032               ngate = 0
//*** Mobility Related Parameter ***
+u0 = 0.226037                ua = -2.912307E-9          ub = 6.629099E-18
+uc = 1.189319E-10            vsat = 1.788028E5          a0 = 0.738544
+ags = 3.820313E-4            b0 = -2.915256E-7          b1 = 1.064744E-7
+keta = 0.019066              a1 = 0                     a2 = 0.732882
+rdsw = 1.455363E3            prwb = 0.607476            prwg = -4.95747E-2
+wr = 1
//*** Subthreshold Related Parameter ***
+voff = -0.269176             nfactor = 10               eta0 = 6.112947
+etab = -5.852903             dsub = 0.467839            cit = 4.91507E-3
+cdsc = 1                     cdscb = 0                  cdscd = 1
//*** Output Resistance Related Parameter ***
+pclm = 1.583402              pdiblc1 = 2.33671E-2       pdiblc2 = 4.286966E-3
+pdiblcb = 0                  drout = 7.67664E-2         pscbe1 = 9.817917E6
+pscbe2 = 8E-10               pvag = 4.71484E-2          delta = 0.01
+alpha0 = 0                   beta0 = 30
//*** NQS Parameter ***
+elm = 5
//*** Capacitance Parameter ***
+xpart = 0                    cgso = 0                   cgdo = 0
+cgbo = 0                     ckappa = 0.6               cf = 0
+clc = 1E-7                   cle = 0.6                  dlc = 0
+dwc = 0                      vfbcv = -1                 cgsl = 0
+cgdl = 0
//*** Souce/Drain Junction Diode Model Parameter ***
+ldif = 0                     hdif = 0                   rsh = 0
+rd = 0                       rs = 0                     rsc = 0
```

```
+rdc = 0                        cj = 5E-4                       mj = 0.5
+mjsw = 0.33                    cjsw = 5E-10                    cjswg = 5E-10
+mjswg = 0.33                   js = 1E-4                       jsw = 0
+n = 1                          pbsw = 1                        pb = 1
+pbswg = 1
//*** Temperature Coeffient ***
+tnom = -196.15                 ute = -1.5                      kt1 = -0.11
+kt1l = 0                       kt2 = 0.022                     ua1 = 4.31E-9
+ub1 = -7.61E-18                uc1 = -5.6E-11                  at = 3.3E4
+prt = 0                        xti = 3
//*** Stress Effect Related Parameter ***
+saref = 5E-6                   sbref = 5E-6                    wlod = 0
+ku0 = 0                        kvsat = 0                       kvth0 = 0
+tku0 = 0                       llodku0 = 0                     wlodku0 = 0
+llodvth = 0                    wlodvth = 0                     lku0 = 0
+wku0 = 0                       pku0 = 0                        lkvth0 = 0
+wkvth0 = 0                     pkvth0 = 0                      stk2 = 0
+lodk2 = 1                      steta0 = 0                      lodeta0 = 1
```

```
//****PMOS 5v0rvt****
simulator lang = spectre
model pmos bsim3v3
//*** Flag Parameter ***
+version = 3.3                  binunit = 2                     mobmod = 1
+capmod = 3                     nqsmod = 0                      igcmod = 0
+igbmod = 0                     minr = 1E-60                    type = p
//*** Geometry Range Parameter ***
+lmin = 7.92E-7                 lmax = 1                        wmin = 7.92E-7
+wmax = 1
//*** Process Parameter ***
+tox = 1.7E-8                   xj = 2E-7                       nch = 6.710511E16
//*** dW and dL Parameter ***
+wint = 3.496097E-8             wl = 6.063631E-14               wln = 1
+ww = -4.852778E-14             wwn = 1                         wwl = 1.934446E-21
```

```
+lint = -8.134903E-8          ll = 1.095254E-13          lln = 1
+lw = 2.548035E-14            lwn = 1                    lwl = 0
+dwg = 1.527399E-9            dwb = 1.997031E-8          xl = 0
+xw = 0
//*** Vth Related  Parameter ***
+vth0 = -1.088089             k1 = 0.897546              k2 = -6.28486E-2
+k3 = -10.911994              k3b = 0                    w0 = 4.256988E-6
+nlx = -4.455657E-8           dvt0 = 4.317246            dvt1 = 0.671679
+dvt2 = -0.032                dvt0w = 0                  dvt1w = 5.3E6
+dvt2w = -0.032               ngate = 1E30
//*** Mobility Related Parameter ***
+u0 = 4.91936E-2              ua = -8.091586E-11         ub = 9.785326E-18
+uc = -7.791702E-11           vsat = 7.243616E4          a0 = 0.799584
+ags = 0.171037               b0 = 2.036112E-8           b1 = 0
+keta = -2.32619E-2           a1 = 0                     a2 = 0.669458
+rdsw = 1.903462E3            prwb = 7.98554E-2          prwg = -0.071225
+wr = 1
//*** Subthreshold Related Parameter ***
+voff = -9.16204E-2           nfactor = 5.042204         eta0 = 0.028
+etab = -0.07                 dsub = 0.56                cit = 0
+cdsc = 0                     cdscb = 0                  cdscd = 0
//*** Output Resistance Related Parameter ***
+pclm = 1.179103              pdiblc1 = 3.794367E-3      pdiblc2 = 9.801735E-4
+pdiblcb = 0                  drout = 1.10479E-2         pscbe1 = 9.817917E6
+pscbe2 = 8E-10               pvag = -0.632232           delta = 0.01
+alpha0 = 0                   beta0 = 0
//*** Gate Dielectric Tunneling Current ***
+nigc = 1                     aigc = 0.012               bigc = 2.8E-3
+cigc = 2E-3                  aigbacc = 0.012            bigbacc = 2.8E-3
+cigbacc = 2E-3               nigbacc = 1                aigbinv = 0.014
+bigbinv = 4E-3               cigbinv = 4E-3             eigbinv = 1.1
+nigbinv = 3                  ntox = 1                   toxref = 1.5E-8
+pigcd = 1                    poxedge = 1                dlcig = 0
+aigsd = 0.012                bigsd = 2.8E-3             cigsd = 2E-3
//*** NQS Parameter ***
+elm = 0
```

```
//*** Capacitance Parameter ***
+xpart = 0                    cgso = 0                    cgdo = 0
+cgbo = 0                     ckappa = 0.6                cf = 0
+clc = 1E-7                   cle = 0.6                   dlc = 0
+dwc = 0                      vfbcv = -1                  cgsl = 0
+cgdl = 0
//*** Souce/Drain Junction Diode Model Parameter ***
+ldif = 0                     hdif = 0                    rsh = 0
+rd = 0                       rs = 0                      rsc = 0
+rdc = 0                      cj = 5E-4                   mj = 0.5
+mjsw = 0.33                  cjsw = 5E-10                cjswg = 5E-10
+mjswg = 0.33                 js = 1E-4                   jsw = 0
+pbsw = 1                     pb = 1                      pbswg = 1
//*** Temperature Coeffient ***
+tnom = -196                  ute = -1.5                  kt1 = -0.11
+kt1l = 0                     kt2 = 0.022                 ua1 = 4.31E-9
+ub1 = -7.61E-18              uc1 = -5.6E-11              at = 3.3E4
+prt = 0                      xti = 3
//*** Stress Effect Related Parameter ***
+saref = 5E-6                 sbref = 5E-6                wlod = 0
+ku0 = 0                      kvsat = 0                   kvth0 = 0
+tku0 = 0                     llodku0 = 0                 wlodku0 = 0
+llodvth = 0                  wlodvth = 0                 lku0 = 0
+wku0 = 0                     pku0 = 0                    lkvth0 = 0
+wkvth0 = 0                   pkvth0 = 0                  stk2 = 0
+lodk2 = 1                    steta0 = 0                  lodeta0 = 1
//*** GIDL Current Parameters ***
+agidl = 0                    bgidl = 2.3E9               cgidl = 0.5
+egidl = 0.8
--------------------------------------------------------------------------
```

B | Appendix B

Script that permits testing of the shift register.

```
// Pins:
    int Analog0 = 0;
    int Analog1 = 0;
    int Analog2 = 0;
    int Analog3 = 0;
    int Analog4 = 0;
    int Analog5 = 0;

    int DS      = 13; // il pin 1 ha dato dei problemi
    int MR      = 8;
    int SHCP    = 9;
    int STCP    = 10;
    int OE      = 11;

// Timing:
    int half_period = 1; // in ms
    int baudrate = 9600;

// Scorrimento:
    int i = 0;

// Variabili di inizializzazione:
    int j               = 0;
    const int length_v  = 34;

    int SHCP_v  [length_v]  = {0};
    int DS_v    [length_v]  = {0};
```

```
    int STCP_v  [length_v]  = {0};
    int MR_v    [length_v]  = {0};
    int OE_v    [length_v]  = {0};


// put your setup code here, to run once:
void setup() {

  Serial.begin(baudrate);

  pinMode(SHCP, OUTPUT);   // SHCP: shift register clock input
  pinMode(DS,   OUTPUT);   // DS:   serial data input
  pinMode(STCP, OUTPUT);   // STCP: storage register clock input
  pinMode(MR,   OUTPUT);   // MR:   master reset input (active LOW)
  pinMode(OE,   OUTPUT);   // OE:   output enable input (active LOW)

//-- Inizializzazione:
//-- SHCP --
    for(j=1 ; j<length_v; j=j+2)
    {
        SHCP_v[j] = 1;
    }

//-- DS --
    DS_v[4]  = 1;
    DS_v[5]  = 1;
    DS_v[24] = 1;
    DS_v[25] = 1;

//-- STCP --
    STCP_v[26] = 1;
    STCP_v[32] = 1;
    for(j=6 ; j<23; j=j+2)
    {
        STCP_v[j] = 1;
    }
```

```
//-- MR --
    for(j=0 ; j<34; j++)
    {
        MR_v[j] = 1; // Inizializzato tutto a uno alla "Brut Force"
    }
    MR_v[2]  = 0;
    MR_v[3]  = 0;
    MR_v[31] = 0;
    MR_v[32] = 0;

//-- OE --
    OE_v[23] = 1;
    OE_v[24] = 1;
    OE_v[25] = 1;
    OE_v[26] = 1;

}

// put your main code here, to run repeatedly:
void loop() {

  // Ordinati come nel datasheet:
    digitalWrite(SHCP, SHCP_v[i]);
    digitalWrite(DS,   DS_v[i]);
    digitalWrite(STCP, STCP_v[i]);
    digitalWrite(MR,   MR_v[i]);
    digitalWrite(OE,   OE_v[i]);

  // Ritardo di acquisizione per essere sicuri
    delay(half_period-0.25);

  // Acquisizione:
    Analog0 = analogRead(A0);
    Analog1 = analogRead(A1);
    Analog2 = analogRead(A2);
    Analog3 = analogRead(A3);
    Analog4 = analogRead(A4);
```

```
    Analog5 = analogRead(A5);

  // Stampare:
    Serial.print("\n-------");
    Serial.print("\nCounter: ");
    Serial.println(i);
    Serial.print("-------");

    Serial.print("\n\nA0: ");
    Serial.println(Analog0);
    Serial.print("A1: ");
    Serial.println(Analog1);
    Serial.print("A2: ");
    Serial.println(Analog2);
    Serial.print("A3: ");
    Serial.println(Analog3);
    Serial.print("A4: ");
    Serial.println(Analog4);
    Serial.print("A5: ");
    Serial.println(Analog5);

    i++;

  // Finisco di ritardare per avere un ritardo di mezzo periodo:
    delay(0.25);

  // Quando finisce di mandare la stringa comincia da capo:
    if (i==34)
    {
        i=0;
    }

}
```

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