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Executive Summary of the Thesis

Testing Techniques for Photonic Integrated Circuits with Statistical Approach

Laurea Magistrale in Telecommunication Engineering - Ingegneria delle Telecomunicazioni

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Academic year: 2020-2021

1. Testing in Silicon Photonics

The nowadays continuous increase of data hunger reflects on the need for efficient solutions. In the telecom/datacom environment flexible and reconfigurable devices are needed in order to handle this amount of traffic. One technology which can help implement these solutions is integrated photonics. In fact, filters like the one presented in [1], have all the characteristics to implement a Reconfigurable Optical Add Drop Multiplexer (ROADM) node in a flexible optical network scenario.
Being the photonics at a (very) early stage if compared to electronics not every step in the manufacture process is fully optimized and standardized. In fact, despite the chips themselves are cheap, the entire process has some expensive steps. In [2] a precise analysis of the production costs is reported. One interesting figure that emerges is that, together, testing, assembly and packaging represent the 80% of the entire cost of manufacturing a PIC. Furthermore, the testing itself can be the cause of up to almost the 29% of the whole costs [3] as is displayed in Figure 1.

Among the main factors which contribute to

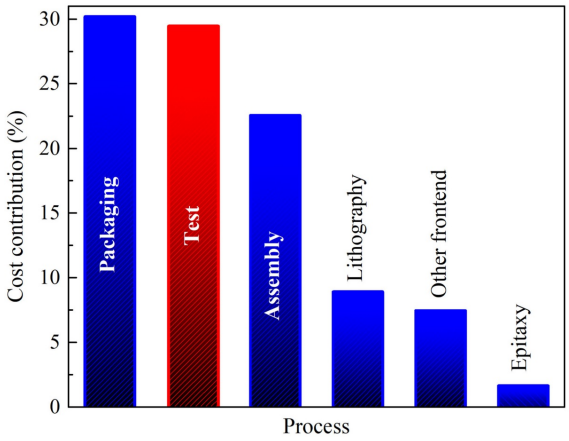

Figure 1: Process cost breakdown (accumulated per process group) with respect to the overall cost of manufacturing of an InP PIC-based module from [3].

the economic impact of testing, the equipment costs and the time costs are the most relevant. Under the denomination of equipment both the expensive specialized groupings of equipment and the large amount this equipment needs to properly perform testing are considered. Another reason for the large time consume in testing is the non-optimized process the DUT has to undergo.
From the depicted picture up to now proposed, it is clear that the testing procedure has to change in order to reduce its impact on the overall cost of the production of PICs. For this reason, in this work, a novel kind of approach to perform the testing procedure on these devices, aiming to save time and economical resources, is proposed.

2. Testing Fundamentals and Techniques

Testing is a complex and outstandingly time consuming process in the manufacture of a PIC. Nevertheless, its importance in the correct development of every integrated circuit is evident. Since the photonics is at a (very) early stage if compared to electronics, a standard is not yet established for testing among the foundries and the manufacture community.
One possible expedient that can be used in order to standardize the testing iter is design for test. It is the earliest of the testing procedure and, so, a very important step because every mistake made at this point will influence all the following process, resulting in an avalanche effect. Design for test means the designer of the PIC, who already should know the testing iter his device will undergo, takes a series of small extra touches in order to make the chip topology the more standard and clear as possible. This kind of accouterments are for instance a smart positioning of the electrical an optical ports (not on the same side), a careful toponomy of each elements in the chip making sure the role of each one will be clear reading the label and standard die orientation through a compass rose.
From the literature two main typologies of testing, in different times of the PIC's production and validation, arise:

- On-Wafer test,
- Bar/Die test.

On-Wafer test is a very important step for testing too. In fact, in the process of manufacture, there is a step in which several (from tens to thousands) of PICs will be on the same wafer. At this point being able to perform the highest number of testing procedure as possible is crucial. The reason is the fact that, this way, a much more efficient and cheap testing can be done, cutting the overall costs. In fact, exploiting a (semi)automatic alignment system and enabling vertical coupling, performing on-wafer testing can provide an efficient (can test hundreds of chips in the same process) and low cost because of the savings in terms of time with respect to test PICs in small groups or individually. Another pro wafer-level testing has is the chance to check the quality of a wafer. This way, if the amount of non-adapt devices is considerable, the tester can just discard the whole wafer, saving the resources for the next (expensive) procedures. Unfortunately, the opportunity of performing on-wafer testing is not for all the integrated photonics technologies and so often is just unavailable.
Bar/Die test mean to detach from the wafer single PICs or small groups and to individually perform testing on them. Usually they are adopted to have extensive characterization of individual building blocks or system-level functionalities of the whole circuit. They are much more complex and costly methods with respect to the on-wafer one, because the procedures have very low automation level. At this stage the lowest number of operations are performed because of the impact they have on the overall costs.

After having treated different stages and kinds of testing procedures, it is important to focus on the characteristics testing needs to have in order to be performed on a large-scale foundry environment.
Testing has to be high speed since one of the most precious resources exploited in the procedure is time. For this reason the process has to be as much automatized as possible and on-wafer. This features may conduct to other equipment costs but in the long run the overall costs will for sure lowered.
Furthermore, testing has to have an high volume of PICs tested together. This feature will reflect

on a considerable time reduction and can be implemented through the wafer-level testing.
Another vital point is the consistency. For consistency the author means the validity and comparability of the measurements in the test process. In fact, in order to have meaningful results, the followed procedure must be repeatable both in the short and long time with small variability of results. Also, the test-station's tares have to be precisely measured and considered.
Eventually flexibility is an important feature too. In fact, if the scenario considered is the one of a real foundry, the testing have to be as more standard and adaptable to all technologies as possible. This will reflect on a reduction of time and equipment resources.
Different testing approaches can be actuated in order to identify the quality of a PIC. Here three are presented:

- System testing,
- Spectral mask-oriented testing,
- Statistical-based testing.

System testing is the most accurate and precise approach, which aims to give a numerical quantification of how well the device can transmit information. The used parameter in this case is the Bit Error Rate (BER). This approach's problems though, are the usual two impairments always present in testing: long time to be performed and expensive equipment. In fact long enough string of bits have to be sent in order to consider the BER meaningful and a particular setup is needed for this experiment. Pieces of this setup includes a BER Tester (BERT) and an Additive White Gaussian Noise (AWGN) generation solution which can cost tens of thousands of dollars.
Spectral mask-oriented testing means the goal of the test process aims to obtain as much information as possible on the frequency response of the device. Usually, the sought quantity for this type of testing is the Mean Squared Error (MSE) of the spectral components of the Device Under Test (DUT) with respect to the ones of a reference "golden" device. Even if the MSE does not give an absolute quantification of the DUT quality like the BER, it still carries a lot of information, especially about the spectrum of the device. The impairments of this direction of testing are the expensive equipment, an Optical Spectrum Analyzer (OSA) is mandatory, and the amount of time to evaluate the entire spectrum and to apply the MSE formula.
The statistical-based testing is the followed approach for this thesis' work. It basically consists in applying to a PIC's environment one of the well-known statistical methods, so that several cost of equipment and time resources can be avoided. The principal obstacle of applying this approach is the correct choice of a suitable statistical method and, then, the way to adapt it to the testing problem.

3. Statistical Method for the Device Under Test

When choosing the statistical approach to follow, two different effective solutions arose: Monte Carlo (MC) and Principal Component Analysis (PCA). Despite both being possible solutions, PCA was preferred. The reason is MC would involve way longer time of execution, since the method itself require an enormous number of iterations and the idea for applying it on this scenario would have needed multiple MC iterations.
For this reason PCA was the chosen statistical method to adjust and apply on the PIC's scenario. The PCA method consists in reducing the environment's complexity by taking in consideration just the main factors which bring independent information. In order to do so, the covariance matrix has to be built considering all the quantities which describe the whole problem. Once obtained, orthogonal eigenvectors and the corresponding eigenvalues have to be found. The eigenvectors which have the highest eigenvalues are the "principal components" to take into account. The decision on the number of principal components to take into consideration is arbitrary and fully depend on the resources the tester has and how well this eigenvectors describe the problem. In order to apply this method to the PIC scenario, it has to be adjusted. In fact, being the eigenvectors purely mathematical results, it is more appropriate to consider real and easy to measure quantities as principal components. In fact, they will still bring information about the device (even if suboptimal with respect to the eigenvectors) and, at the same time, will be less impactful in terms of time since they can be directly measured.

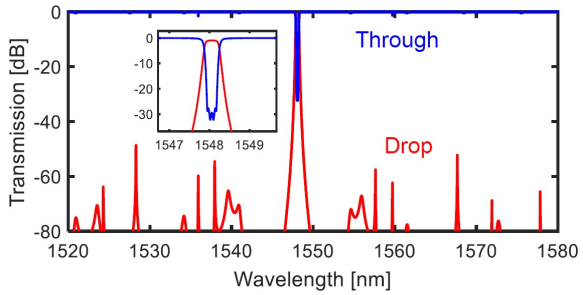

Figure 2: Filter frequency response measured against wavelength. From [1].

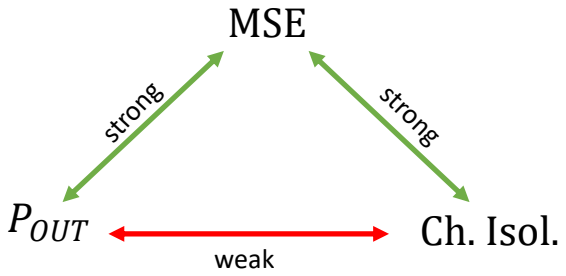

Figure 3: Desired correlation relations between parameters of interest.

For this work, the application of the method was performed on a silicon photonics filter. In particular it is a 4-ports Free Spectral Range (FSR)-free filter. This filter is constituted by a chain of 4 directly-coupled Micro Ring Resonators (MRRs) connected to two bus waveguides through tunable couplers, implemented thanks the use of Mach-Zhender Interferometers (MZIs) (further details about this device can be found in [1]). In Figure 2 its spectrum is shown. This filter is a very in-frequency selective device (3 dB bandwidth of the In-Drop-port is about 40 GHz) which also can be dynamically tuned. These features makes it suitable to be employed in a ROADM context.
The presented filter was modelled through functional-circuital simulations in Matlab focusing on the possibility to apply perturbations on some of the most susceptible parameters. In fact, in order to make the result as more realistic as possible and to determine which kind of disruption harms the most the method, waveguides' phases, couplers' gaps and Round Trip Losses (RTL) were perturbed. These three parameters to perturb were chosen because of their importance in the filter environment and also because of their susceptibility to disruptions during the manufacture process.
For this kind of devices one of the most important and meaningful quantity is the MSE. In fact, this quantity keeps trace of a very large span of useful information about the filter, so that it can be considered as index of the device's quality. In order to effectively apply the statistical method, the principal components have to be found. So, studying the variabilities and correlations upon the study made in [4], the chosen principal components were Output Power (P_{out}) and Channel Isolation at 50 GHz (Ch. Isol.). P_{out} is here considered as the average power measured at the Trough-port when a Drop-port like signal (integral power 14.5 mW) is the input of the filter. It is calculated in the whole frequency span simulated (from -0.1 THz to $+0.1$ THz considering the frequency axis normalized to the central frequency of the filter which is 193.65 THz). The Relative Output Power ($P_{out,r}$) is P_{out} divided by the integral power of the input signal. It will be used to give a clearer interpretation of the measurements. The Ch. Isol. is here considered as the maximum amplitude of the Drop-port frequency response between the one at -50 GHz and the one at $+50$ GHz from the central filter frequency.
The idea for obtaining the same information MSE would give about the DUT's quality was, instead of the longer and expensive procedure to actually measuring it, to exploit the correlation coefficients between the MSE and P_{out}/Ch. Isol. For this work the correlation coefficients are calculated with the Pearson correlation coefficient definition. The best possible scenario is the one reported in Figure 3 in which the correlations between the principal components and MSE are strong and the correlation between the principal components themselves is weak.

4. Numerical Results

As first case, the correlations of interest of the mentioned filter were studied applying only single parameters perturbations. The first perturbed was the phase of the waveguides: the used perturbations were from $-\pi/55 <$ phase perturbation $< +\pi/55$ to $-\pi/5 <$ phase perturbation $< +\pi/5$. After collecting the data of MSE, P_{out} and Ch. Isol. for every filter simulated for this process (44000 filters) it was possible to obtain the values of the correlation

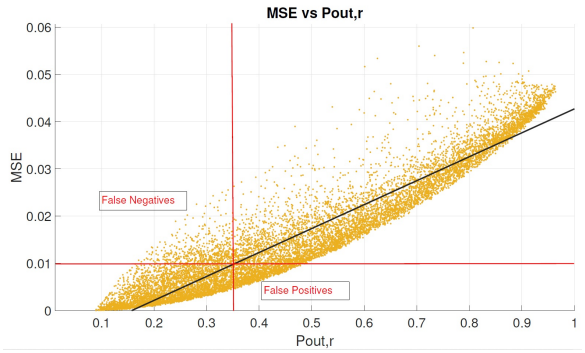

Figure 4: MSE vs $P_{out,r}$ predictions result.

coefficients. For this case the MSE/P_{out} and the MSE/Ch. Isol. correlations are strong (the second especially for the lowest perturbations) while the P_{out}/Ch. Isol. presents low values. This is a good result, since it means the P_{out} and Ch. Isol. bring independent information about the MSE. At this point is possible to make predictions about the quality of the filters tested, thanks to a linear fitting of the MSE/$P_{out,r}$ values and an arbitrary MSE threshold (Figure 4), since their correlation is the strongest. The errors this method makes are labelled as False Positives and False Negatives. The False Positives are the filters this method discard but were actually under the MSE threshold, whether the False Negatives are the ones this method considers good but they actually don't respect the threshold. This two categories have different impacts on the cost. In fact, since the price of manufacturing a chip is much lower than the cost of performing different procedure like testing itself and packaging, the False Positives have a relatively low impact and the real issues are the False Negatives. If the MSE threshold is set to 0.01 the results over 12000 filters with phase perturbations are: False Negatives: 565 (4.71%), False Positives: 1020 (8.50%), total errors: 1585 (13.21%). This results can be further improved by setting a Ch. Isol. threshold too, at the cost of discarding more good chips. For instance, setting a Ch. Isol. threshold at 0.05 will reduce the False Negatives to 85 (0.71%) in this case, resulting in a substantial improvement. Another idea can be setting multiple MSE thresholds in order to better clusterize the products' quality.

This procedure was then performed also with the perturbation of the couplers' gaps. The perturbations used were: -1% < gap's perturbation < +1%, -2% < gap's perturbation < +2%, -5% < gap's perturbation < +5% and -10% < gap's perturbation < +10%. Unfortunately, from these simulations, the only useful correlations emerged from the two weakest perturbation if we consider the MSE and P_{out}/Ch. Isol. correlations. Instead the P_{out}/Ch. Isol. correlation is quite strong for all perturbations (up to 68%). Since the correlation values are the one presented, a linear fitting will conduct to inaccurate decisions.

As third parameter the RTL was perturbed. The values of this perturbations were 0.01 dB/round < RTL < 0.1 dB/round, 0.05 dB/round < RTL < 0.15 dB/round, 0.05 dB/round < RTL < 0.4 dB/round, 0.1 dB/round < RTL < 0.5 dB/round and 0.1 dB/round < RTL < 1dB/round. This time the correlation coefficients between the MSE and P_{out}/Ch. Isol. are strong for the weakest values of RTL (up to 87% and 66%) but unfortunately the values of the P_{out}/Ch. Isol. correlation tend to be quite high too for the first two cases (up to 67%). Like the previous case, a linear fitting for taking decision about the quality of the filter would result in an imprecise solution.

Eventually, the same simulations as before were repeated considering all three kinds of perturbations merged together. In particular, for this case, the phase perturbations distribution was uniform (0 < phase pert. < $\pi/35$), while for the couplers' gaps and RTL the distributions were extracted from [5] and evaluated with different correlation coefficients. The results seemed to be quite insensible to the correlation coefficient between the perturbations so just the 5% one are considered. The found correlations between the principal components and the MSE are quite high (72% and 83%). Unfortunately also the P_{out}/Ch. Isol. correlation is relevant (54%) but, since the other two are strong, decisions about the quality of the filters can be made with a certain accuracy. This time a fitting of the MSE against the Ch. Isol. was performed (Figure 5) since their correlation is the strongest. At this point making predictions is possibile (setting an MSE threshold in 0.015 and the results, over 10000 filters are: False Negatives: 821 (8.21%), False Positives: 80 (0.8%), total errors: 901 (9.01%). This result can be further improved, as already mentioned, by setting a further threshold in the other parameter. For instance if a

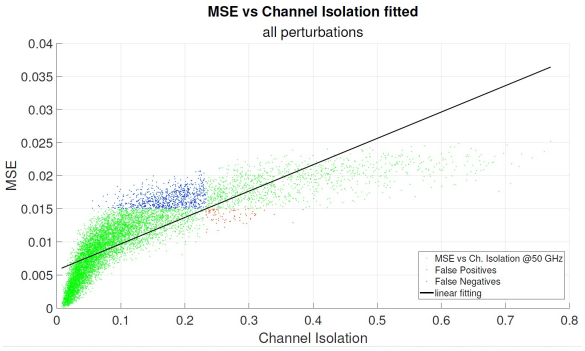

Figure 5: MSE vs. Ch. Isol. linearly fitted.

threshold in $P_{out} = 0.276$ is set the errors become: False Negatives: 178 (1.78%), False Positives: 80 (0.8%), total errors: 258 (2.58%). The cost of this increase in precision is the amount of good filters wasted.

5. Conclusions

In this work a novel method to test PICs was presented. The method, through the exploitation of PCA, circumvents the evaluation of quantities like MSE and BER (which require long time and expensive equipment) and still obtains reliable information about the DUT's quality, resulting in considerable savings of resources. This approach, furthermore, offers the possibility to find out the PIC's quality with a reasonable error probability which can be further improved. This feature contributes to make the method scalable and flexible to the tester needs. The method's efficiency and limitations were tested through simulations of filters with perturbations on their important quantities. The results prove that the method correctly works for the tested filter if the perturbations (especially the couplers' gaps an RTL) are not very prominent. The proposed solution is usable in a wafer-level testing context, resulting in a more efficient and cheap work flow. The discussed approach can be adopted also for other typologies of PICs, adapting the principal components.

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Testing Techniques for Photonic Integrated Circuits with Statistical Approach

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Abstract

A novel method based on a statistical approach for the testing of Photonic Integrated Devices (PIC) is presented. This method aims to strongly cut the time and equipment costs currently present in the testing procedures for this typology of devices, being these the major causes of the testing impact on the total production's cost.

The proposed method exploits the well-known Principal Component Analysis (PCA) statistical approach to obtain information about the overall device quality reducing time and equipment costs.

The effectiveness of the proposed method and its limitations were tested by simulations of a 4-ports Free Spectral Range (FSR)-free silicon photonics filter. In order to perform an interesting validation of the method, different kinds of perturbation were modelled and applied to the simulated filters.

Keywords: Photonics, Testing, PCA, Cost reduction

Sommario

Un metodo innovativo basato su un approccio statistico per il testing di circuiti di fotonica integrata (PICs) è presentato. Questo metodo mira a tagliare fortemente i costi di tempo ed attrezzatura presenti oggigiorno nelle procedure di testing per questa tipologia di dispositivi, essendo queste le cause principali dell'impatto del testing sul costo totale di produzione.

Il metodo proposto sfrutta il ben noto approccio statistico "Analisi delle componenti principali" (PCA) per ottenere informazioni sulla qualità del dispositivo riducendo i costi di tempo ed attrezzatura.

L'efficacia del metodo proposto e i suoi limiti sono stati testati tramite simulazioni di un filtro di silicon photonics a 4 porte Free Spectral Range (FSR)-free su cui diversi tipi di perturbazione sono stati applicati. Al fine di compiere un'interessante validazione del metodo, diversi tipi di perturbazione sono stati modellizzati e applicati ai filtri simulati.

Parole chiave: Fotonica, Testing, PCA, Riduzione dei costi

Introduction

Integrated photonics nowadays is a very promising and fast growing field. Among the various environments, one of the most promising is the telecom/datacom networks. In fact, the perspective of flexible and reconfigurable nodes is a possible way to counteract the increase of traffic recent days are experiencing. To implement this innovative type of network suitable devices are necessary. Integrated photonics can provide fast reconfigurable, cheap, low footprint and very frequency selective tunable devices which can be implemented in this scenario [11].

However, the testing process for this type of devices is as well in development. In fact, the test step in the manufacture of PICs is one of the largest causes of the total cost of producing this type of device. Studies [12] on this argument pointed out that the testing process is responsible for up to the 29% of the total cost of a PIC. The reason behind this heavy impact has to be sought in the early stage of the optical testing, especially if compared with the electric one. For this reason, sub-optimal procedures are often implemented, exploiting expensive equipment machinery and using very long time spans.

The objective of this thesis is to develop a novel statistical approach to apply to the PIC's testing environment in order to save resources in terms

of time and equipment. In particular this method would exploit a well known statistical theory, adjusted and applied to a complex environment like the PIC's one.

This work is divided into chapters, which are organized as follows:

- **Chapter 1** presents an overview of the PIC's testing state of the art focusing on the issues and limitations currently present. Then the thesis' objective is exposed and the original contributions are listed.
- **Chapter 2** presents various methodologies and possible approaches available for testing in a foundry context. In particular the impact on costs of these different options is discussed.
- **Chapter 3** presents the statistical approach chosen for the thesis' work highlighting its features. Furthermore, the filter used for the simulations is described and the simulation approach is depicted.
- **Chapter 4** presents the numerical results. Eventually the results are commented and contextualised.

1 | Testing of Photonics Integrated Circuits

This chapter exposes the meaning of testing, applying this concept in an integrated photonics scenario. It shows the importance testing has in the process of fabrication of a photonic device and the impact it has on the costs. It also tackles the state of the art of testing clarifying which are its issues. Then the objective of the thesis is explained and the original contributions are listed.

The chapter is divided in this sections:

- 1.1 Testing in Photonics,
- 1.2 State of the Art,
- 1.3 Thesis' Objective,
- 1.4 Original Contributions,

1.1. Testing in Photonics

Integrated photonics is nowadays in fast growth due to its several applications like optical signal processing [13], biological application [14],

sensing [15], narrow band filtering [11] etc.

Among these, integrated photonics is a very promising technology for networks. In fact, with the impressing increase of the amount of traffic, integrated photonic offers devices to implement solutions to overcome this hunger of data. In particular the Reconfigurable Optical Add Drop Multiplexer (ROADM) scheme seems to be the most popular and performing way to resolve this traffic problem due to its fast reconfigurability between the nodes and the possibility to implement Dense Wavelength-Division-Multiplexing (DWDM) to better manage the amount of bandwidth needed for this application [16]. In this kind of network PICs are widely employed due to their small footprint, low cost, low power consumption, high speed and multiple choices for reconfiguration. Another key for their success is the possibility to integrate various function on a single device, resulting in savings in occupied volume and production cost [17].

Among the technologies for integrated photonics, the one which had more success is silicon photonics. Silicon photonics devices in fact, exploiting the well affirmed Complementary Metal-Oxide Semiconductor (CMOS) technology, have the enormous advantage of being manufactured in the already existing foundry of electronics. This permits to have a large scale production and a very cheap cost with respect to other integrated photonics technologies [18].

Considering this typology of devices, it is very important the photonics-electronics relationship, in fact they are often complementary and have

to be well mixed to perform at the best. Mainly two types of approach for electronics and photonics integration are available: monolithic integration and multi-chip [19]. Monolithic integration means the electronic and photonic components are fabricated together on a unique chip during a single process flow. This obviously raises the complexity of the process development but, in the meantime, strongly reduces the overall volume and, as will soon depicted, the testing costs. Furthermore monolithic integration doesn't have the parasitic capacities of electrical bondings resulting in grater energy efficiency and bit-rate performances [20].

The other approach is the multi-chip one. Multi-chip basically means that the electronic and photonic components are individually developed and, only after, electrically bonded together. This on one hand means simpler component's fabrication procedures, on the other hand the final device will result more bulky, the costs of testing will increase and parasitic capacities will rise due to the electrical bondings. The final result will be a device with lower performances and efficiency with respect to a monolithically integrated one.

From the foundry to the final user a device has to complete many steps, the one of interest for this thesis is testing. Testing is a process which has the goal to verify fab process tolerances, validate foundry manufacturing, extract building block quantities and study system level behaviour of overall circuits. It is indeed a crucial step in the development of a photonic device.

Since a photonic device is a very complex and multi-physics environ-

ment, different typologies of testing may have to be performed on the same device. In [21] a list of different physical parameters is reported. In particular in [21] is highlighted the importance of measuring and understanding the relationships between the parameters, investigating the dependences between quantities belonging to different fields like mechanics, thermodynamics, optics and electrics. These dependences are crucial to find out and to understand in the testing procedure because the final device must be enough tolerant to unwanted phenomena like physical stress and thermal fluctuations. Another important aspect is testing how and how much the behaviour of the devices changes after changing input parameters like wavelength, applied voltage or optical power depending on the type of device.

Testing has a primary role in the cost of production of photonic devices too. In Figure 1.1 an example of the process cost breakdown of a PIC is shown from [1]. It can be noticed that more than the 80% of the total investments are for packaging, test and assembly. In particular, as reported in [12], testing (immediately after the packaging) is the major contributor to the production cost of the entire photonic chip in the case of a monolithically integrated device. When dealing with a discrete-device single-package it becomes even the most impactful source of cost. The main and most important cause of the rise of the testing cost is the equipment cost. Under equipment cost not only have to be considered the expensive specialized groupings of equipment needed but also the large amount of time resources this equipment has to spend in order to properly do testing [22]. After these economical consideration it seems

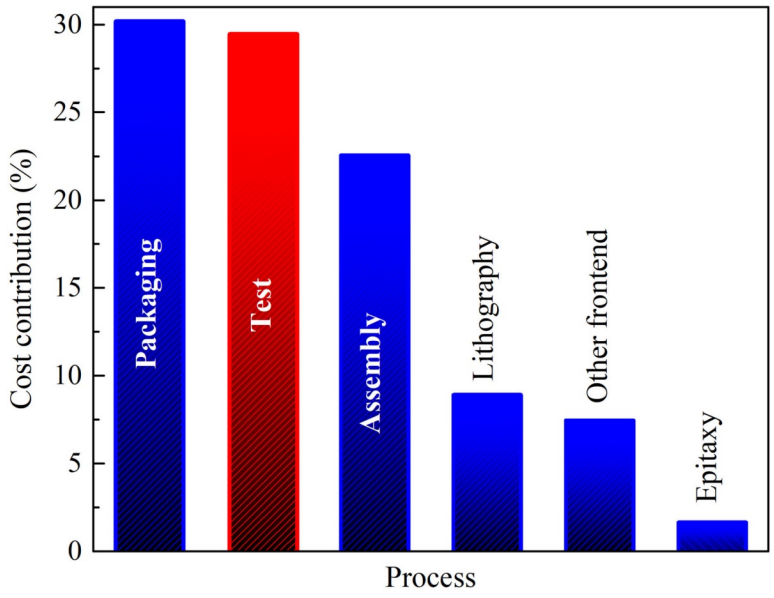


Figure 1.1: Process cost breakdown (accumulated per process group) with respect to the overall cost of manufacturing of an InP PIC-based module from [1]

obvious that the goal of every photonic integrated circuits' manufacturer is to reduce as much as possible the testing costs.

1.2. State of the Art

In the electronic industry, testing has become a mature process supported by methodologies and equipment which was strongly optimized to reduce the costs and the time resources needed to this process. Unfortunately, since integrated photonics is a much more recent technology and cannot benefit of the years of electronics' research, the testing situation is still at a quite early stage. In fact the processes of testing are not standardized over the integrated photonics community, even though some efforts to create a common guide line have been done.

For example in [1] a standardized approach to Photonic Integrated Circuit (PIC) was proposed, so that access to automated testing could be enabled. This work focuses the attention on the costs testing has in a PIC manufacture (up to the 29% of the entire chip's cost) and proposes an innovative way to save as much as possible. The exposed idea is a precise but flexible way to design the PIC, following particular standards based on the kind of test the designer want his product to do, so that when the chip will be tested, an already prepared automatic testing equipment will save precious time reducing the costs.

Up to now different approaches to testing are possible, depending on the device to test and on the tester necessities. Here three of these are briefly introduced, while in the next chapter they will be deeply discussed. System testing is the approach which focuses the most on the device ability to correctly exchange information and its main goal is measuring this efficiency. Spectral mask-oriented testing instead has the direction of evaluating the whole frequency response of the DUT, and focuses on the measurement of parameters which contain information about its discrepancy with a fixed arbitrary standard. Last, the statistics-based approach tries to overcome the expensive drawback of the preceding approaches, cutting the process costs by exploiting an already affirmed statistical method.

A very interesting test system proposed in [2]. This system is a full-automated in line optical test system which performs wafer testing the authors named In-Line Optical Test Systems (ILOTS). It is both able to perform optical and electrical testing on passive and active silicon

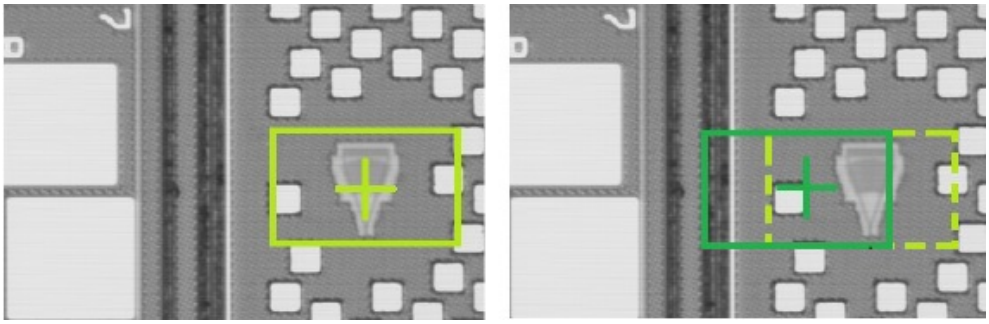


Figure 1.2: Prober pad registration using grating coupler alignment method. From [2].

photonics devices. In particular a nondestructive and repeatable optical coupling method was used by means of vertically diffractive grating couplers. Since the optical alignment is very critical, every input and output coupler was aligned using a suitable alignment algorithm in order to maximize the coupling with the Device Under Test (DUT) as shown in Figure 1.2. Furthermore, to counteract the grating couplers' coupling efficient variability, a four-ports MultiMode Interferometer (MMI) was used, so that the measured results could be determined by linear regression resulting in a reduction of the noise. ILOTS are also able to perform testing and collect data about non-linear optical parameters such as a directional coupler split ratio, phase tuning efficiency of optical modulators thanks to their 1x25 electrical pads and responsivity in photodiods.

For the silicon photonics in particular the most relevant steps have to be done in the wafer-level testing. In the manufacturing of a silicon photonics device, the foundry will, exploiting the CMOS technology, produce large disks called wafers having each up to thousands of chips. This is the perfect moment to do testing because at this point costs can be reduced

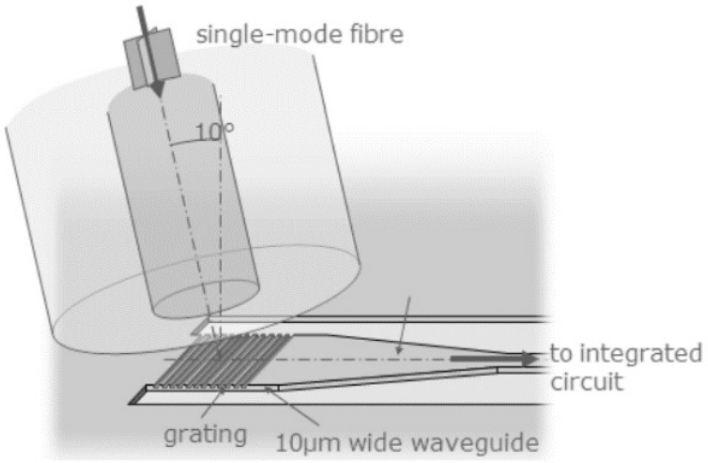
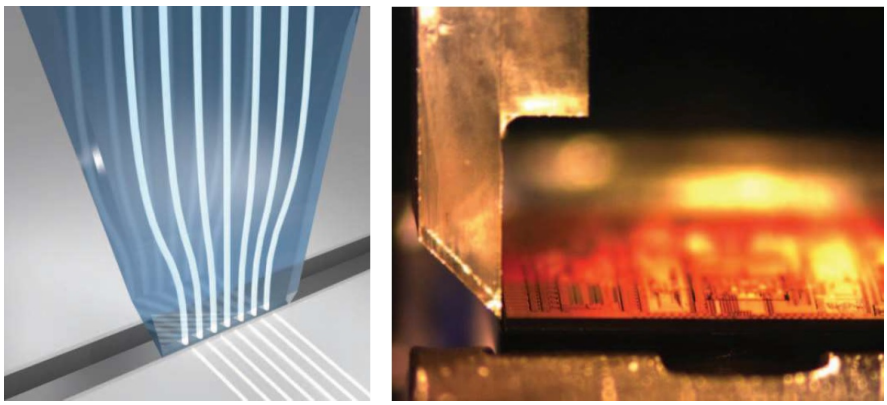


Figure 1.3: Optical coupling scheme with a grating coupler. From [3].

very much. The reasons behind this savings are: the test is much more fast since testing an entire wafer takes less time than dicing every chip and singularly test it and if unfortunately a wafer doesn't meet the specifications, early aborting the process can save packaging resources (which is together with testing one of the most costly part of the manufacture [4]).

Although wafer testing is not always easy. For example to perform it usually chips have to present grating couplers in order to be coupled from above being the devices not diced yet (this type of coupling is schematized in Figure 1.3). Unfortunately this is not optimum because grating couplers need an extremely precise alignment and tend to be loss susceptible. For this reason the optical alignment in wafer-context has to be supported by a suitable algorithm to minimize the coupling loss.

A possible solution to this impairment is presented in [4]. In this work the application of a particular Planar Lightwave Circuit (PLC) as an optical



(a) (b)

Figure 1.4: a) Frontal view of the PLC. b) A PLC photography. Both from [4].

probe has been considered. In order to perform wafer-level testing of PICs with edge-couplers, a vertical probe was introduced into the dicing trenches of silicon wafers. A PLC, shown in Figure 1.4 a) and b), is a silica object which can be designed to have a multitude of channels, is monolithical and enables easy handling and manipulation.

With this approach, the more convenient wafer testing can be performed even with edge couplers in the DUT, meaning that there is no need to design PICs with the more loss-susceptible grating couplers (shown in Figure 1.3) and having developed an algorithm to minimize the loss.

Following the approach discussed in [4], in [5] another probe solution was proposed. In [5] an interesting design of another kind of probe to perform wafer testing with edge-coupler is presented. This probe (Figure 1.5) has on the bottom a planar Total Internal Reflection (TIR) mirror which redirects the beam from the vertical direction to the horizontal one. Once then the beam is reflected, it is focused by an aspheric lens to make

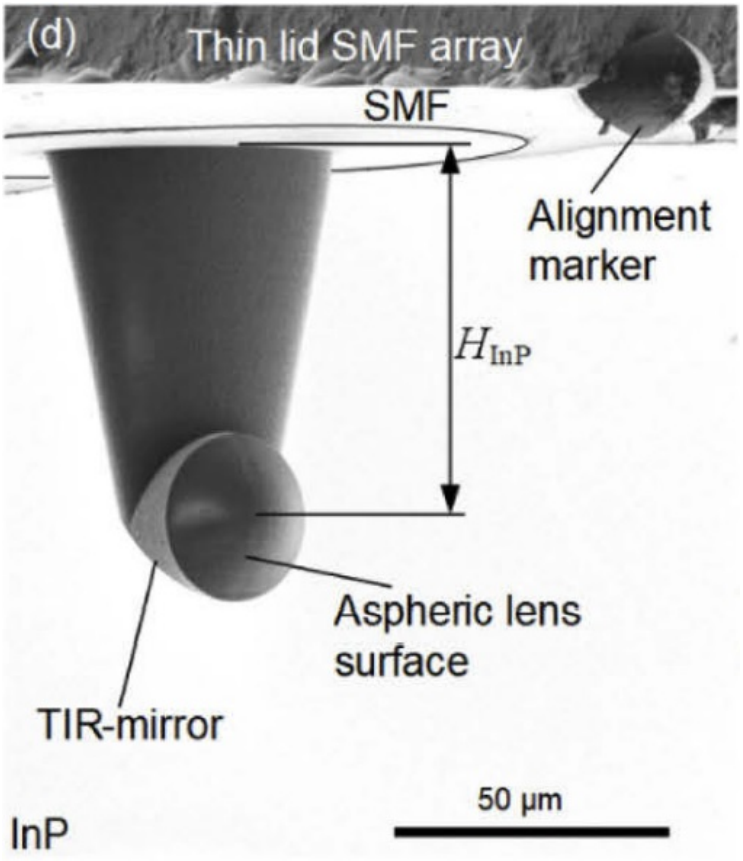


Figure 1.5: Scanning-electron microscope image of the discussed probe for coupling to InP. From [5].

the beam waist diameter at the facet to the right mode-field size, which can propagate inside the chip's waveguide. This technology is suitable for coupling with silicon-nitride on-chip waveguides, InP-based active optical components and silicon photonics on-chip waveguides with respectively 2.7 dB, 1.9 dB and 1.9 dB of coupling loss. It is also remarkable the opportunity the author mention to use an array of this probes to perform testing at multiple PIC ports at the same time.

In general, as presented, the most important problem in photonic devices' testing is the load of resources it needs. The efforts have to be

in the direction of minimize as much as possible these costs through the developing of new low-budget techniques and approaches.

1.3. Thesis' Objective

The goal of this thesis is to develop and implement a method through which the quality of a photonic integrated circuit can be estimated with an innovative approach based over non-expensive measurements.

To get to this goal various kinds of approach have to be compared, as will later on fully explained, in order to find out which one better fits the problem both in terms of precision of results and costs of implementation.

As previously pointed out, the costs in the development of a photonic device are, if not the principal, one of the main players in testing. Since the reason behind the strongly role testing has in the costs is the expensive, in terms of price and in terms of time of elaboration, specialized equipment, the direction will be to find an approach which can, as much as possible, exploits other cheaper methods and/or tools. The focus though will also be on a technique which can be applied over the most wider possible typologies of photonic integrated circuits with the correct trade-off between costs and precision.

This found approach and these results could be very useful on a large scale production of photonic integrated circuits, where the high number of devices to test extremely needs an efficient way to know if their products satisfy the quality standards saving resources.

1.4. Original Contributions

The original contributions contained in this work are listed below:

- Identification of a circuital-functional model to describe an arbitrarily complex PIC.

  A model to describe and simulate a complex PIC was developed. In particular the chance to introduce arbitrary disruptions to its main parameters was actively implemented.

- Application of a statistical method to a photonic integrated circuit test case.

  A method to significantly cut the testing cost of a photonic integrated filter exploiting the Principal Analysis Components (PCA) approach was developed. This technique was developed studying the necessities of testing processes and applied to a specific filter even if its validity could be tested over a wide range of devices.

2 | Testing Fundamentals and Techniques

This chapter deeply investigates the testing procedure in a PIC scenario and different stages in this process are presented. Furthermore, the principal features of the testing procedure are exposed. In the end of the chapter some of the main testing approaches are discussed.

The chapter is divided in the following sections:

- 2.1 Testing's Stages,
- 2.2 Testing's Pillars,
- 2.3 Testing's Approaches.

2.1. Testing's Stages

As already presented, testing is a complex and outstandingly time consuming process in the manufacture of a PIC. Nevertheless, its importance in the correct development of every integrated circuit is evident. Being the photonics at a (very) early stage if compared to electronics, the foundries and the manufacture community have not yet reach a stan-

dard path to follow in the PIC production chain, as is established in electronics. Despite some recent interesting proposal of standardization have been published [1], the procedure is still non-optimized, often steps are overlooked and so automated testing is very hard to perform. The direction of standardization of testing would for sure cut the costs of the overall manufacture, having also an impact on other expensive processes like packaging. This improvement would also increase the yield of production contributing to have a cheaper and larger scale production in foundries.

In order to proceed in the optimization direction, **Design for test** is a suggested path to follow. Design for test is the first and often the most underrated part of the testing procedure. At this point the developer is designing his PIC paying attention to the chip functionalities and optimized layout. It is very important though, in order to have a cheaper, faster and more precise testing result, to keep always present the kind of testing process the PIC will be subjected. With this in mind, the designer has to take small extra touches to facilitate the testing operation the PIC will face, knowing the nature of the device and so the specific operations the PIC will have to go through for the final validation. In order to proper design, a dialog with the testing engineer has to happen, so that the designer can have fully knowledge of the testing needs and, if present, standards to respect. Since this step is at the very beginning of the chip development, its importance has to be further stressed because every sub-optimal design choice will result in higher costs in terms of time and equipment and lower precision for every testing step after, resulting

in a negative avalanche effect. Examples of this simple accouterments, like proper ports naming, standard die orientation through a compass rose and smart ports location, are present in [1], where the focus is on the functional and clever placement of different elements in the device design. In Figure 2.1 a well-designed PIC's layout is shown. It can be noticed that each different I/O ports has a proper naming which tells about its nature and the placement of different kinds of port (electrical and optical) are never on the same side to ease the testing procedures.

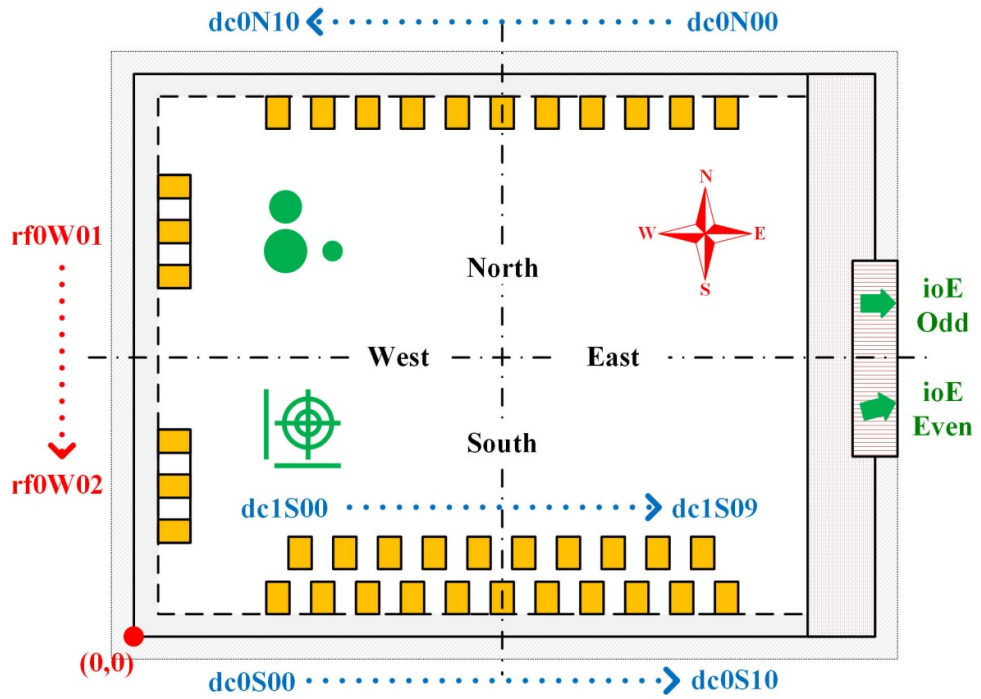


Figure 2.1: Standardized PIC layout setting conventions for edge-coupled circuits, which include die orientation, naming and locations of input-output ports, fiducials, and indication of restricted areas important for assembly and packfrom. From [6].

From the literature two main typologies of testing, in different times of the PIC's production and validation, arise.

- On-Wafer test,
- Bar/Die test.

Both of these steps needs a small introduction and contextualization in order to better understand their roles and importance in the testing chain.

On-Wafer test is a vital moment of the testing procedure. At this point the design is committed and the chips are essentially manufactured by the foundry. Large wafers hosting up to thousands of PICs are produced (a photography is shown in Figure 2.2).

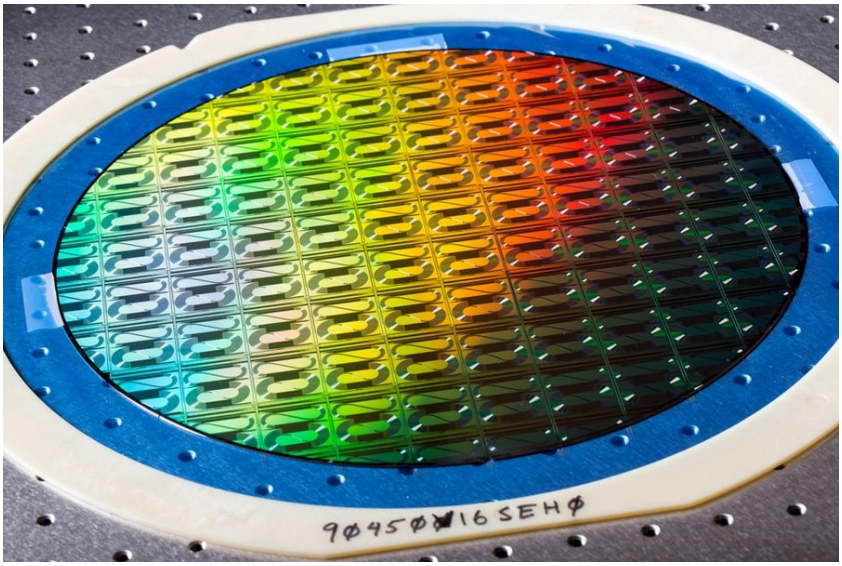


Figure 2.2: A photonic wafer close-up. From [7].

Performing On-Wafer Testing can give the estimation of the yield of a wafer for a particular PIC. In fact it is extremely important, where is possible, to attempt to perform the most possible measurement at this early point of the flow. The reason is that, by having early results

about the PIC's parameters, it is straightforward to identify whether the wafer deserves to go on with the other testing procedures, assembling and packaging or it is better to discard the entire wafer. In fact, as already mentioned, testing, assembly and packaging together contribute to about the 80% of the total cost of the PIC, so sometimes it is just better to discard the whole wafer at this point rather than make it go through all the other expensive procedures and, only after them, discard it.

For this economic reason wafer-level testing is the direction integrated photonics is following, adopting solutions for implementing it in different technologies. Unfortunately in fact is not always straightforward to measure chips on a wafer. First of all today is not possible for all PIC technologies: InP- and GaAs- chips for example, needing cleaved-facets with ultra-low antireflection coating to fully operate, aren't usually able to be wafer-tested. In the future (by 2030 if the roadmap in [22] is respected) for the two mentioned technologies, cleaved facets are to be replaced with by on-wafer etched facets and facet coating by on-wafer coating. Instead silicon photonics' devices can be tested on wafer both optically, with some impairments, and electrically. In Figure 2.3 in-action wafer-level testing is shown.

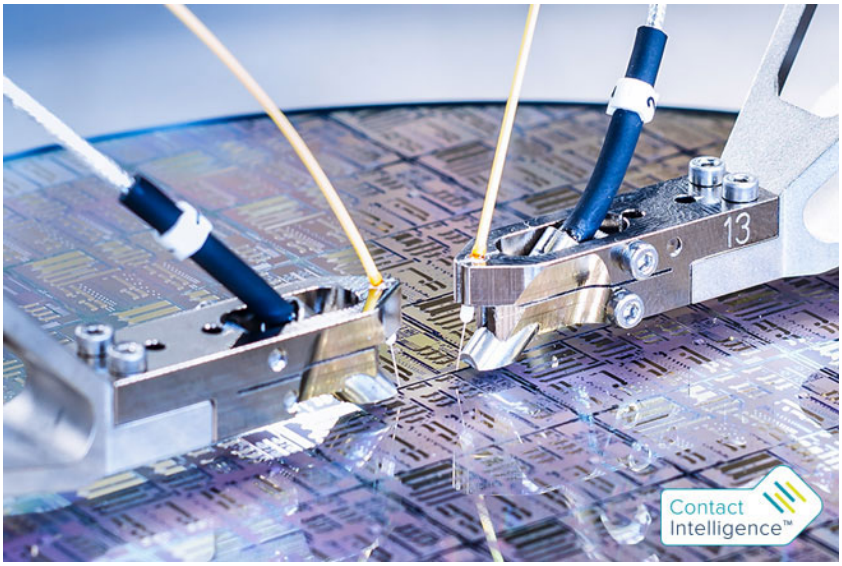


Figure 2.3: Wafer testing close-up. From [8].

The most common method used for optical wafer testing is the employment of grating couplers onto the PIC itself so that vertical coupling could be possible. Unfortunately the usage of grating coupler has the drawback of being a loss susceptible technology and so new techniques were proposed in [4] and [5]. Both of these, through the use of probes inserted into the wafer trenches, permit to use the more robust, fast and repeatable method of edge-coupling even on wafer. In order to perform this type of optical measurement a (semi)automated alignment with high resolution is needed, which implies cost for the development and complexity of this alignment system but ensures great precision and repetibility.

Bar and Die testing mean to detach from the wafer single PICs or small groups and to individually perform testing on them. Usually they are adopted to have extensive characterization of individual building blocks or system-level functionalities of the whole circuit. They are much more

complex and costly methods with respect to the on-wafer one, because the procedures have very low automation level. For this reason foundries tend to leave this kind of testing to end users. For technologies which require integration with other components or for which, due to physical impairments, wafer testing is not possible, electrical and especially optical testing have to be performed with this strategy.

After this considerations is clear that, if possible, especially from a foundry point of view, it is better to minimize the bar/die testing in order to perform more of these measurements directly on the wafer. This is clearly not always possibile but if the total cost of testing needs to be minimized, the direction is the one of wafer-level testing [6].

2.2. Testing's Pillars

After having treated different stages and kinds of testing procedures, it is important to focus on the characteristics testing needs to have in order to be performed on a large-scale foundry environment. First of all it is remarkable to state that the precise necessities of testing depends widely on the kind of PIC, on its technology, on the environmental necessities and on the types of measurement are needed to be performed. Nevertheless, if large-scale foundry testing's necessities are considered, some common features emerge. All these features are listed and discussed in detail below.

One of the most important quality a testing system needs to have is **high speed**. One of the principal causes of the testing's costs is the very

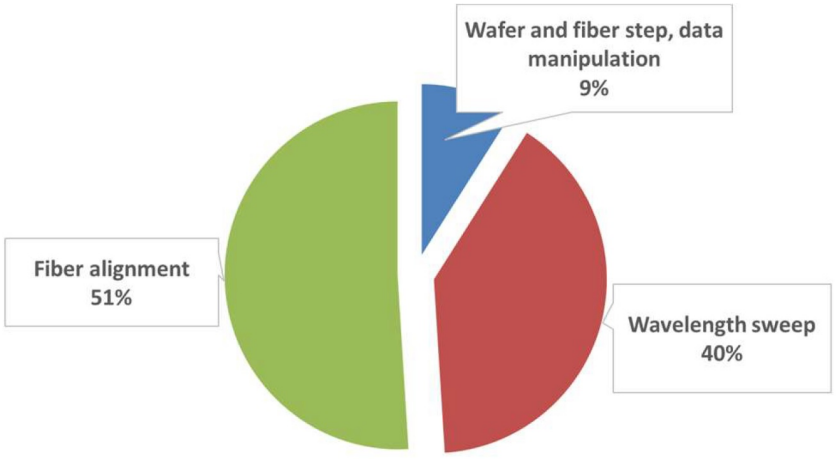


Figure 2.4: Breakdown of the total test time for measuring a test site to extract waveguide loss and grating coupler efficiency. From [3].

large amount of time these procedures need. In particular the most time consuming sub-step is the optical testing. One of the reasons behind the optical testing's time necessity is pointed out in [3].

In this work in fact a test-station for flexible semi-automatic wafer-level testing is presented. The discussed system performs optical testing of an entire wafer using grating couplers to perform vertical coupling. For each PIC, optical alignment has to be performed moving the optical fibers over the wafer thanks to an automated routine alignment method. For each chip, the tunable source has also to change its wavelength over its whole span in order to find out the particular wavelength with peak transmission. This study measured the actual duration of each wafer test and pointed out, reported in Figure 2.4, the breakdown of the total test time.

Even if, as the author emphasizes, these data depend on specific measurement settings as wavelength span and resolution, they can still give an

important indication of the time breakdown of the process. From Figure 2.4 is clear that fiber alignment is the most impactful operation in the optical testing. This information is vital to proceed in the direction of fast testing because the consideration to do is to improve as much as possible the alignment efficiency by the implementation of fast algorithms and automatic alignment structures for wafer testing.

Another crucial aspect testing needs to have is an **high volume** of PIC tested together. The importance of testing in the cost breakdown, which was previously reported in this work, is up to about the 29% of the total costs for the chip production [12]. Therefore, from a foundry point of view, that the number of devices tested together has to be the higher possible so that the process will result cheaper.

In order to follow this direction, wafer-level testing is the most obvious way to proceed. In fact performing the time expensive testing operation on a wafer which contains from several tens to hundreds of PICs (depending on the kind of chip and its dimensions) is much more sustainable than to perform it on bar or die level. For this reason the research and industrial environments of silicon photonics are focusing their efforts in the direction of making wafer testing the more practicable as possibile with the engineering of different opto-mechanics solution like the one presented in [4] and [5]. In general the foundries want to increase as much as possibile the yield of their PIC production to reduce the cost and to raise the revenues of their products so a wafer-level test approach, is necessary, where applicable.

The third vital aspect of testing is **consistency**. For consistency the author means the validity and comparability of the measurements in the test process. In fact, in order to be valuable and meaningful, the extracted data have to be corroborated by a precise sequence which includes the calibration of all the tools and equipment is intended to use and the correct measure of the setup tare. For example is crucial, when measuring the insertion loss of a device, to previously having clear the intrinsic loss the measurement setup has to have meaningful unbiased results. Two important aspects which together contributes to the consistency of a testing process are *short-repeatability* and *long-term reproducibility*.

With short-term repeatability of the measure is intended the standard deviation of all the measure of a set of experiments repeated on the same DUT at small intervals of time one from the other. An example of short-time (30 minutes between experiments) repeated experiment is shown in Figure 2.5 form [3]. In this example 14 dice's coupling efficiencies were measured.

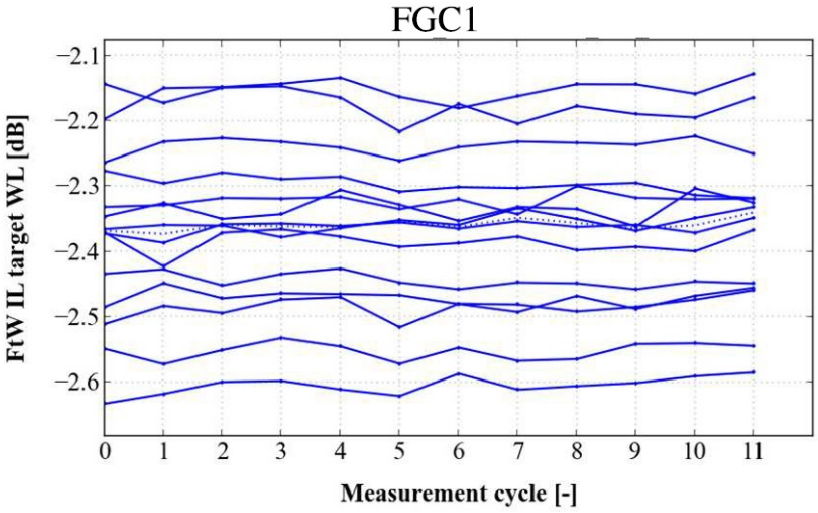


Figure 2.5: Short-time interval measured coupling efficiency on a set of 14 die locations across the reference wafer. From [3].

The average repeatability of these measurements amounts to 0.012 dB which intends that the measurements are consistent in the small-time variation.

With long-time reproducibility of a measure instead is intended the standard deviation of all the measure of a set of experiments repeated on the same DUT at, this time, longer time interval. In the same cited work also long-time (on a 5-months span) repeated experiment was performed, measuring the same quantities as the previous case which is reported in Figure 2.6.

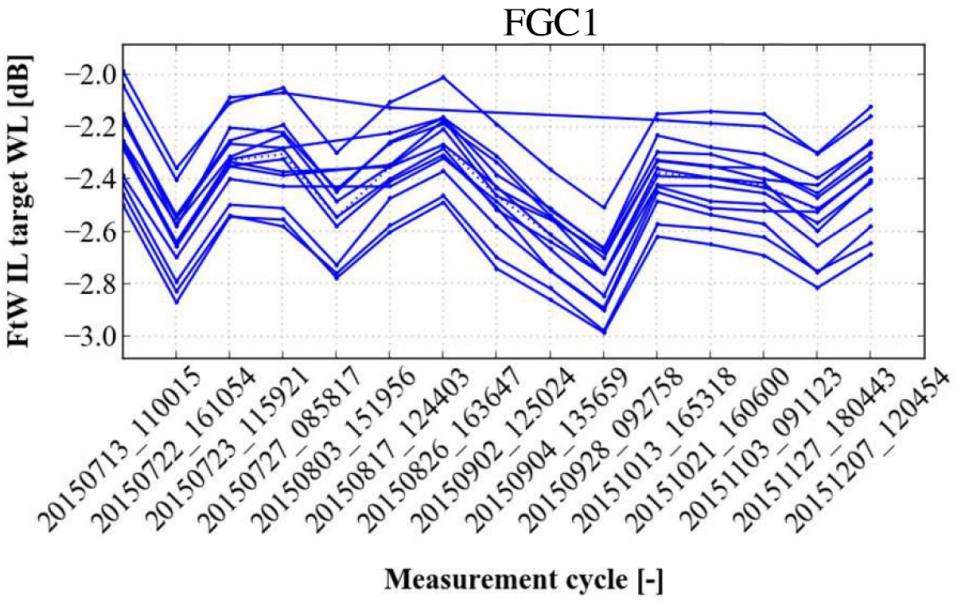


Figure 2.6: Long-time interval measured coupling efficiency on a set of 14 die locations across the reference wafer. From [3].

The average reproducibility of these measurements amounts to 0.14 dB. This value is naturally higher than the short-time repeatability since in a wider time span it is logical to think of various factors which influence the measure. Among these are included the positioning accuracy of the measurement pigtails, the readout accuracy of the power meter and the variation in probe-to-pad resistance.

The last pillar of testing discussed in this work is **flexibility**. If the focus is once again on a foundry context, it is natural to think of various typologies of devices being manufactured. For example filters, photodetectors, delay lines and other PICs can be commissioned to the same foundry. Since this devices have all to be tested, it is clear that performing this procedure in the smartest and cheaper way possible is desirable. In order to reach this goal it is important for the tester to have a flexible

test-station. In fact if, just changing some of the software inputs and modifying minor hardware components, all these kinds of devices could be tested in series it would resolve in having a reduction of the final test cost.

This result could be also eased by a proper communication between the design engineer and the test one, so that the design of the PIC will respect the standards and guide lines the test procedure requires, resulting in time and resource savings.

2.3. Testing's Approaches

The typologies of testing and the features it needs have been discussed up to now. One important choice though, when testing a device, is the kind of approach the tester want to conduce. In order to give the complete picture of these approaches here three different ones are exposed and investigated, showing the advantages and the drawbacks of each and motivating this thesis' chosen one.

The first treated approach is the **system testing**. For system testing is intended the measurement of the functional parameters of the DUT, which define its performance in the field of which it will be inserted to. Usually when considering PICs for telecommunications (one of the most common applications) the main parameter which can identify the quality of the performances of these type of devices (active or passive) is the Bit Error Rate (BER).

The BER is defined as the ratio of the number of incorrect bits N^{ERR}

and the number of total received bits N^{TOT} (Equation (2.1)),

$$BER = \frac{N^{ERR}}{N^{TOT}}. \tag{2.1}$$

This rate is the most important and impactful quantity obtainable because it gives the tester a numerical quantification of the quality of the device in transferring information. In order to have a complete view of the PIC's performance though, just a single measurement is not sufficient. In fact, to have a full characterization of a chip's behaviour, it has to be tested in multiple scenarios where factors like temperature, input power, humidity and other parameters vary so that important dependences on the correlations of different parameters can be pointed out and, if possible, managed. Furthermore, in order for the BER to be meaningful, the total number of bits to transfer has to be significantly high so that the measured BER approaches the true actual BER of the device. This reflects in the use of particularly long sequences of bits: for example in [9] for a BER measurement the total number of bits was 3×10^{10}. These two last listed necessities bring forward to the reader the long time requirements of this type of testing.

BER measurements are performed through the exploitation of a particular set-up. This setup has to include a pattern generator, a transmitter and a receiver, synchronized with the transmitter and able to recognise errors, must be present. A schematic setup is pictured in Figure 2.7.

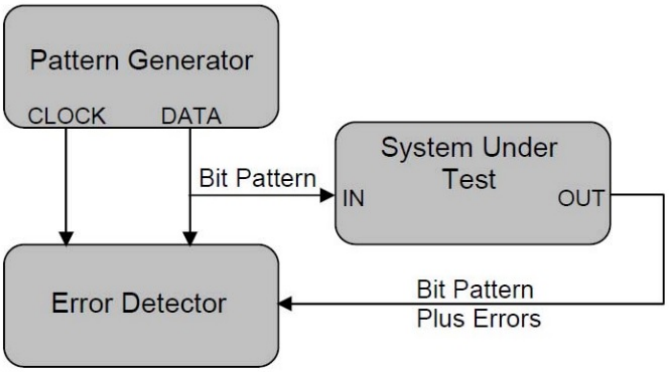


Figure 2.7: Conventional test equipment set-up for BER test. From [9].

Usually, for this type of measurement, the test engineer exploits a stand-alone BER Tester (BERT) and an Additive White Gaussian Noise (AWGN) generation solution. This last is needed to test how the DUT's BER is influenced by the noise it can be subject to when in function. In the BERT a pattern generator and an error detector synchronized by a clock signal have to be present to measure the BER. With that suitable equipment a precise BER measure can be performed. The important drawbacks this technique has are the amount of time needed for data elaboration and the important cost of the devices. In fact a BERT and an AWGN generation solution have a cost that ranges from a few thousand to tens of thousand dollars [23].

The second testing's approach presented is the **spectral mask-oriented testing**. This approach is characterized by the complete identification and evaluation of the spectral components of the DUT. In fact, when dealing with a PIC, usually the frequency response can bring a large amount of information about its quality and precision. When the DUT

is a high selective frequency devices like a laser or a filter, both very common and frequently employed devices, its spectrum is of primary importance. Furthermore, once the optical spectrum is fully extract, several aspects and parameters can be evaluated. Very significant examples of these parameters are the the bandwidth, the channel isolation, the off-band notches, the in-band average output power etc. For instance, if an optical network scenario is considered, the optical filters which will implement the nodes and perform the role of ROADM have to respect important thresholds in their spectral response. In fact they have to be very selective in frequency by means of a very small bandwidth centered in the very precise designed frequency. They also need to isolate as much as possibile off-band while keeping extremely low the in-band losses. One quantity which can be used as an overall quantification of all the spectral quantities, with respect to the ones of a "golden" device used as reference, and, therefore, as global metrics for the device's spectral quality is the Mean Squared Error (MSE).

The MSE is defined as the mean squared variation of the actual device spectrum with respect to the spectrum of a "golden" one used as reference. Usually the average is performed over the whole range of frequencies over which the spectrum was calculated. The precision of this measurement depends on the resolution used for the computation of the frequency response and on the correct choice of the reference filter. The MSE definition is reported in equation form in Equation (2.2),

$$MSE = \sum_{f=f_1}^{f_M} \frac{|H'(f) - H(f)|^2}{M}, \tag{2.2}$$

where f_1 and f_M are the first and the last considered frequencies for the spectrum computation, H'(f) is the reference spectrum, H(f) is the spectrum from which MSE has to be calculated and M is the total number of frequencies which have been chosen to measure the frequency response.

As in the BER computation, it is straight forward that a single extraction of the MSE value is often not enough. In fact, for a complete characterization of the DUT, the measurement has to be repeated multiple times changing the environmental conditions and the input parameters' values. In particular if we think of a dynamic reconfigurable filter used as ROADM (like the one in [10]), not only the measurement of all the ports' frequency responses under different environmental perturbation have to be computed, but also all the possible configuration the filter can have during his work cycle have to be frequency characterized and for each the MSE have to be calculated. It is clear that this kind of approach is very time consuming, especially because the spectrum computation and then the MSE calculus require impactful amounts of time if the frequency resolution (which translates into testing precision) is high.

Another important aspect to take into account for spectral mask-oriented testing is the economic cost of the equipment needed. In fact, for this kind of approach, the usage of an Optical Spectrum Analyser (OSA) is mandatory and the cost for this tool is usually of tens of thousands of dollars.

The last kind of approach is the **statistics-based** one. This approach's idea is to exploit an already existing statistical method and to apply it on a challenging environment, like an arbitrary complex PIC, in order to find alternative solutions to get to the same information the other approaches reach. The hardest part of the application of this approach is the individuation of the statistical method which better fits the problem and of the adjustments to make on it in order to be as useful as possible in the correct estimation of the final goal in the chosen environment. These two steps are strictly linked each other and equally important for the correct workflow of the method.

The emergence of this type of solution to the testing procedure arises from the need of reducing the costs of testing. In fact, due to the hard impairments the other two approaches offer, on a foundry large scale they could be successfully implemented only by paying high costs in terms of equipment and time resources, which contributes to having the testing as the 29% of the impact over all the PIC's manufacture cost impact. Instead, having a statistics approach, which is the one chosen for this thesis work, means trading the very high costs already mentioned of the other testing approaches, with the complexity of choosing and adapting an already present statistical method to the testing of a PIC. Eventually, once found and adjusted the statistical approach (which is part of the next chapter), the resulting method could just be applied on a large scale testing foundry.

3 | Statistical Method for the Device Under Test

In this chapter the choice of the statistical approach for this thesis work is discussed. Then the simulated device which was tested is presented in his main features. Eventually the simulation approach and the PCA's application are treated.

This chapter is divided into the following sections:

- 3.1 Statistical Approach,
- 3.2 Case Study,
- 3.3 Simulation Features,
- 3.4 PCA's Application.

3.1. Statistical Approach

Up to this point it is clear the importance and the impact the testing procedure has on the whole manufacture is massive. Nevertheless, as exposed in the previous chapter, some approaches have different time and cost necessities and so their use have to be carefully evaluated. The

kind of approach, which this thesis focus on, is the statistical one. The reason of this choice can be found in the opportunity of important savings in the testing time and equipment cost, exploiting already established statistical methods.

While choosing the most suitable statistic approach, different methods were evaluated. In fact the idea was to find one method which can, simultaneously, being suitable for the PIC technologies, non require heavy to process mathematical operations, deal with non-hard to extract measurable quantities, being at the same time flexible and adaptable without difficulty to different types of PIC. After having evaluated different methods, two of them were the candidates to this role: PCA [24] and Monte Carlo (MC) [25].

One possible approach which could be adopted is MC. MC is a statistical method which aims to solve a problem through the repeated random sampling. In fact it is commonly used to deal with very hard to manage problems if faced in a deterministic way, but much more handable if solved with its random approach. For its ability to solve very difficult problems it is widely applied in incredibly extensive engineering fields like ocean [26], risk mitigation [27] and financial [28].

If applied to the the testing process, it would need a desired threshold of an overall parameter like MSE and then it would simulate the DUT with random values of a chosen input parameter among the ones of the PIC. After a large number of trials, this process will result in a distribution of acceptable values of the input parameter. Having this one, a second

MC would be performed considering the found distribution and random values for another chosen input parameter. This way on, at the end of the whole procedure, multiple distribution of the selected input parameters would be obtained. From these, it would be possible to extract threshold values for the total input parameters considered in order to respect the overall parameter. In the testing of of a PIC, MC could be an adoptable solution for the statistical approach. The only important obstacle to face is the amount of time it would require. In fact, exploiting multiple random samplings, the time resources employed can be considerable and one of this thesis' goals is to reduce them as much as possible.

PCA, instead, is a very different statistical method which aims to simplify a complex environment described by a multitude of real parameters into a simpler one described by a lower number of new defined parameters (principal components) which bring the most amount of information with them. A trade-off between the number of principal components to consider and the accuracy of the environment description is present, so choices depending on the type of application have to be made.

The first step of this method is the study of the environment and the acquisition of the totality of parameters which contribute to describe it for different iterations so that each parameter can be treated as a random variable. After that, the covariances and variances of all these parameters have to be calculated. The variance is the measure of a random variable dispersion and its definition is reported in Equation (3.1),

$$VAR(X) = \sum_{i=1}^{n} p_{\mathrm{i}} \cdot E[(x_{\mathrm{i}} - E[X])^2]. \tag{3.1}$$

The covariance is defined as the measure of the joint variability of two random variables and its formula is presented in Equation (3.2),

$$COV(X, Y) = \sum_{i=1}^{n} p_{\mathrm{i}} \cdot E[(x_{\mathrm{i}} - E[X]) \cdot (y_{\mathrm{i}} - E[Y])], \tag{3.2}$$

where $X = [X_1, X_2, ..., X_{\mathrm{n}}]$ and $Y = [Y_1, Y_2, ..., Y_{\mathrm{n}}]$ are defined as random variables having n equally probable iterations. Under this assumption the probability mass function is $p_{\mathrm{i}} = \frac{1}{n}$.

This step consists in calculating the covariance matrix. The covariance matrix, shown below, is defined as a square matrix having as elements the covariances between each pair of parameters (Equation 3.3).

$$COV(X_{\mathrm{A}}, X_{\mathrm{B}}, ..., X_{\mathrm{Z}}) = \begin{bmatrix} VAR(X_{\mathrm{A}}) & COV(X_{\mathrm{A}}, X_{\mathrm{B}}) & ... & COV(X_{\mathrm{A}}, X_{\mathrm{Z}}) \\ COV(X_{\mathrm{B}}, X_{\mathrm{A}}) & VAR(X_{\mathrm{B}}) & ... & COV(X_{\mathrm{B}}, X_{\mathrm{Z}}) \\ ... & ... & ... & ... \\ COV(X_{\mathrm{A}}, X_{\mathrm{Z}}) & COV(X_{\mathrm{B}}, X_{\mathrm{Z}}) & ... & VAR(X_{\mathrm{Z}}) \end{bmatrix}$$

where $\mathrm{X_A}$, $\mathrm{X_B}$, ... , $\mathrm{X_Z}$ are the total measured parameters which describe the environment.

Any covariance matrix is also symmetric and positive semi-definite and its main diagonal contains variances, because of the property in Equation (3.3),

$$\begin{aligned} COV(X,X) &= \sum_{i=1}^{n} p_{\mathrm{i}} \cdot E[(x_{\mathrm{i}} - E[X]) \cdot (x_{\mathrm{i}} - E[X])] = \\ &= \sum_{i=1}^{n} p_{\mathrm{i}} \cdot E[(x_{\mathrm{i}} - E[X])^2] = VAR(X). \end{aligned} \tag{3.3}$$

At this point, the eigenvalues and eigenvectors of the covariance matrix have to be calculated. Eigenvalue's and eigenvector's definitions are reported below.

$$COV(X_{\mathrm{A}}, X_{\mathrm{B}}, ..., X_{\mathrm{Z}}) \cdot \begin{bmatrix} Z_{\mathrm{A,\,i}} \\ Z_{\mathrm{B,\,i}} \\ ... \\ Z_{\mathrm{Z,\,i}} \end{bmatrix} = \lambda_{\mathrm{i}} \cdot \begin{bmatrix} Z_{\mathrm{A,\,i}} \\ Z_{\mathrm{B,\,i}} \\ ... \\ Z_{\mathrm{Z,\,i}} \end{bmatrix},$$

where $Z_{\mathrm{i}} = [Z_{\mathrm{A,\,i}}, Z_{\mathrm{B,\,i}}, ..., Z_{\mathrm{Z,\,i}}]$ is the i-th eigenvector and λ_{i} is the corresponding i-th eigenvalue.

Once the totality of eigenvector is found, the precision trade-off comes into play. In fact, in order to apply PCA, the most impactful eigenvectors (i.e. the ones with the highest associated eigenvalues), have to be the one to take in consideration, discarding the rest. These chosen eigenvectors are the ones which carry the largest amount of information about the environment, meaning that considering just them will still describe the environment but with less accuracy. At this point the PCA user have to choose how many eigenvectors he wants to adopt considering that an high eigenvectors number would mean more data to measure and more calculation to perform but, on the other hand, a low number of eigenvectors would mean low precision in the environment description.

Having decided the number of eigenvectors to take in consideration, these are the previously mentioned principal components. These principal components represent, in a Cartesian scenario, the orthogonal set of axis for which the original measured data variance was higher. One thing to keep in mind though is the fact that principal components are not real physical parameters but mathematical linear combinations of the real measurable quantities. This is a very important point since, for the implementation of this method in the presented PIC's environment, there is the need of having real quantities to measure because performing further mathematical operations will negatively impact on the time dedicated to this process. For this reason the classical PCA method was modified: instead of adopting the strictly optimal eigenvalues, found with the presented process, some of the physical quantities which describe the PIC were used as principal components.

After having discussed the PCA statistical approach and the MC one, comparisons can be made. In fact the two methods are intrinsically different and therefore it is natural they have different performances when applied to the PIC environment. For this kind of problem PCA was preferred because, if a careful study of the environment is done, it offers a much more cheap (in term of time and number of computation) and "smarter" solution with respect to MC. In fact MC would still get to the solution but the employed time resources would be way more than PCA and, since time is a very precious resource in the testing procedure, PCA was chosen for this particular situation.

Eventually PCA was chosen as the method to consider and so, from

now on, this section is about its contextualization and adjustments for this scope. Nevertheless, at the end of the section, an idea of how to implement MC is presented, together with the reason PCA was preferred.

3.2. Case Study

In the PIC's field the technologies and the possible kinds of device are various. For this reason the developed technique to test has to be as flexible as possibile, so that it can be easily scaled for the larges amount of typologies of PICs, resulting in savings for the foundry that would hypothetically implement it.

That being said, for this thesis' purpose, the choice of a device to test was compulsory in order to verify the correct working of the developed technique. This choice felt over the device presented in [10]. This PIC is a silicon photonics filter. In particular it is a 4-ports Free Spectral Range (FSR)-free filter. This filter is constituted by a chain of 4 directly-coupled Micro Ring Resonators (MRRs) connected to two bus waveguides through tunable couplers, implemented thanks the use of Mach-Zhender Interferometers (MZIs). A graphical scheme of the filter is presented in Figure 3.1.

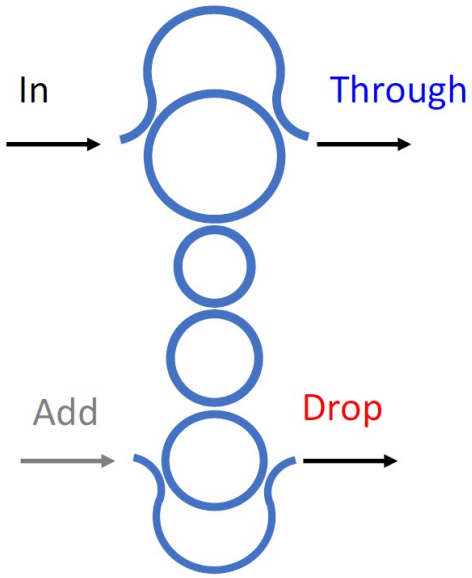


Figure 3.1: Graphical scheme of the filter. From [10].

The radii of the MRRs are $R_1 = 14.371\ \mu m$, $R_2 = 8.240\ \mu m$, $R_3 = 9.964\ \mu m$, $R_4 = 11.976\ \mu m$. The values of the power coupling coefficients are $K_1 = (7.638\%, 7.638\%)$, $K_2 = 0.990\%$, $K_3 = 0.350\%$, $K_4 = 0.85\%$, $K_5 = (6.296\%, 6.296\%)$.

FSR-free means its spectral response, which typically for optical cavities presents a periodicity in frequency of a span (called FSR) does not present periodicity in the bandwidth of interest. In order to obtain this absence of periodicity in the frequency response the MRRs, radii were designed using a Vernier scheme method with non-integer FSRs' ratios [11].

The measured frequency response (plotted against frequency and wavelength) of this filter are reported in Figure 3.2 and Figure 3.3.

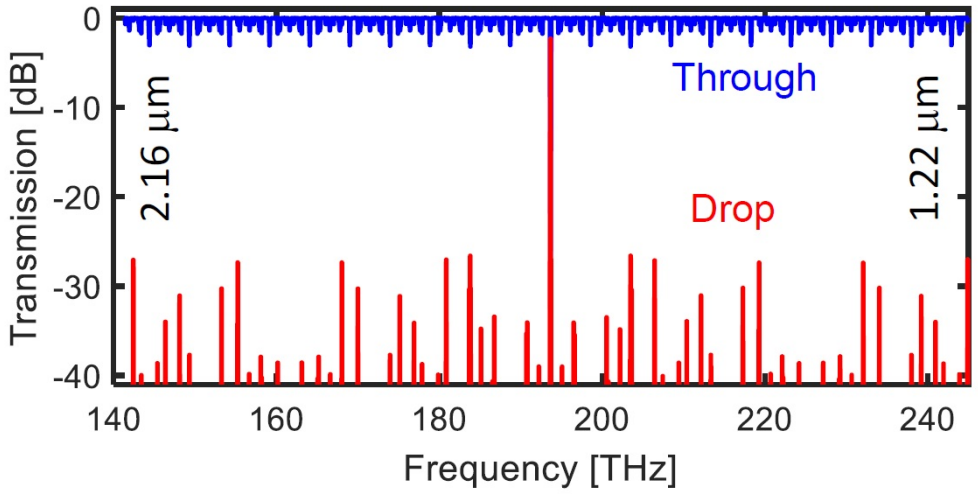


Figure 3.2: Filter frequency response measured against frequency. From [10].

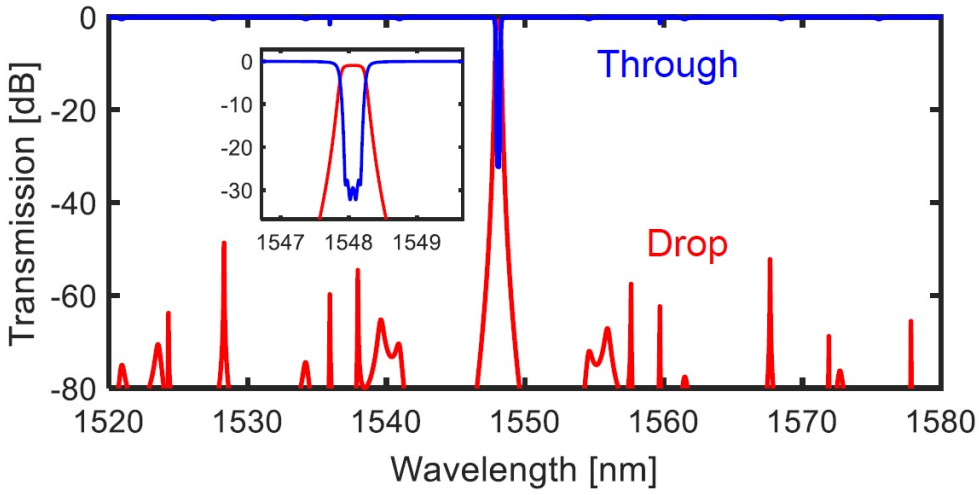


Figure 3.3: Filter frequency response measured against wavelength. From [10].

This filter is a very in-frequency selective device (3 dB bandwidth of the Drop-port is about 40 GHz) which also can be dynamically tuned. In fact, via a set of thermal actuators (all independent and one for each MRR/MZI), the Through- and Drop- port responses can be shifted along

the whole C+L bandwidth. Unfortunately, the presence of multiple actuators, generates the thermal cross-talk phenomenon which basically coincides with the thermal influence by an heaters of the neighbors waveguides. In order to correctly perform the tuning control in a efficient way and, simultaneously, to compensate for detrimental factors which reflects into the change of the optical length of the waveguides, an error minimization algorithm can be adopted. Together with this kind of algorithm it also can be applied the Thermal Eigenvalue Decomposition (TED) method to make it cross-talk-free.

This technique, presented and deeply discussed in [29], offers the possibility, together with a proper algorithm and a chosen parameter to minimize/maximize, to handle in a smart way the unwanted thermal effects happening on the filter, minimizing their impact. In fact, the algorithm controls simultaneously all the actuators and adjusts their input voltages relaying on the TED method, so that the filter frequency response is as much insensitive as possible to thermal unwanted variations which, in part, include thermal cross-talk from neighbours actuators.

The presented features together make this filter suitable for a ROADM implementation in a reconfigurable optical network, which is a very promising technology for the network environment, so it is a device of great interest for the telecom/datacom application.

3.3. Simulation Approach

For this thesis' goal the presented filter was simulated in order to extract the parameters of interest. The functional-circuital simulations were performed thanks to a Matlab script through which the circuit was modelled. These simulations not only took into account the fundamental backbone of the filter's behaviour, but also incorporated effects like cross-talk and the coupler's frequency dependency [19]. Furthermore, the code offers the possibility to arbitrarily perturb three important parameters for this kind of filter: the waveguides' phases, the couplers' gaps and the Round Trip Loss (RTL) of the MRRs.

These three parameters were chosen because of their importance in the filter environment and for their susceptibility to disruptions during the manufacture process. Waveguides' phases are a crucial parameter in this typology of filters. In fact, being employed in DWDM networks, their bandwidth is usually very small and their central frequency has to be equally precise. Nevertheless, it usually happens that phases get perturbed for various reasons: cross-talk from other thermal actuators, unwanted thermal fluctuations or disruptions in the manufacture process. To counteract this phenomena, the presented filter can be controlled by with a suitable algorithm for error minimization (both implemented in the code) which, if used in combination with the presented TED, can also be thermal cross-talk-free. In particular, in the script, an algorithm for the minimization of the average output power at the Through-port, was used. In order to minimize the output power an input signal has to

be sent in the filter. For all the simulations performed in this work the input signal was an broadband flat AWGN noise appropriately shaped into a Drop-port frequency response shape (Figure 3.4) which presents a 3 dB bandwidth of 40 GHz and an integral power of 14.5 mW.

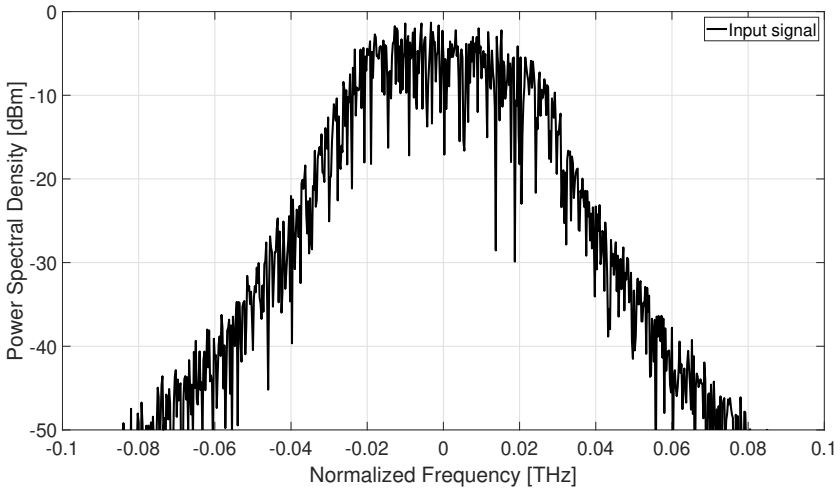


Figure 3.4: Input signal's spectrum.

This kind of input noise was chosen because it maximizes the filter performances as demonstrated in [30]. In a realistic set up, in fact, an AWGN-like noise can be generated in a smart and cheap way by an optical amplifier without an input signal which will result in an Amplified Spontaneous Emission (ASE) noise. Then this noise could be filtered by a Drop-port shaped filter and after that be sent in the actual filter of interest. This input signal was used in all the simulations to have a fair comparison between results.

The resulting work of TED and the minimization algorithm consists in the gradually change (the step can also be customized) of the voltage bias of different heaters, so that the thermal cross-talk effects and other

unwanted dynamics can be countered. Couplers' gap and RTLs are important parameters too and they should be as less perturbed as possible since their change reflects in substantial changes of the spectral response's important feature as the bandwidth. Once again, for the scope this type of filter was designed, the bandwidth is a key parameter because stringent thresholds in the frequency selectivity are present for DWDM standards. For this work's purpose the PCA approach on the filter is applied while perturbing, first one single per time and then together, these three parameters. This way the parameters whose alteration impact the most can be identified and, together with this, the simulations are performed in a more realistic scenario than the one without any perturbation.

The script used for the simulation models the previously described device. In particular it can calculate the frequency response of both Through- and Drop-ports in the frequency span from -0.1 THz to $+0.1$ THz considering the frequency axis normalized to the central frequency of the filter (193.65 THz). An example of the simulated frequency response is depicted in Figure 3.5.

For these simulation the spectra are always considered in the frequency domain in order to be consistent with the mathematical structure from which the model was built [19]. The resolutions among the spectrum is not always the same though. In fact two different resolution were employed: one of 250 MHZ and one of 2 GHz. The highest one was used for the evaluation of the spectra in the proximity of the filter bandwidth (+/- 100 GHz from the central frequency) while the lower for the remaining part's evaluation. The reason behind this choice is the fact that the

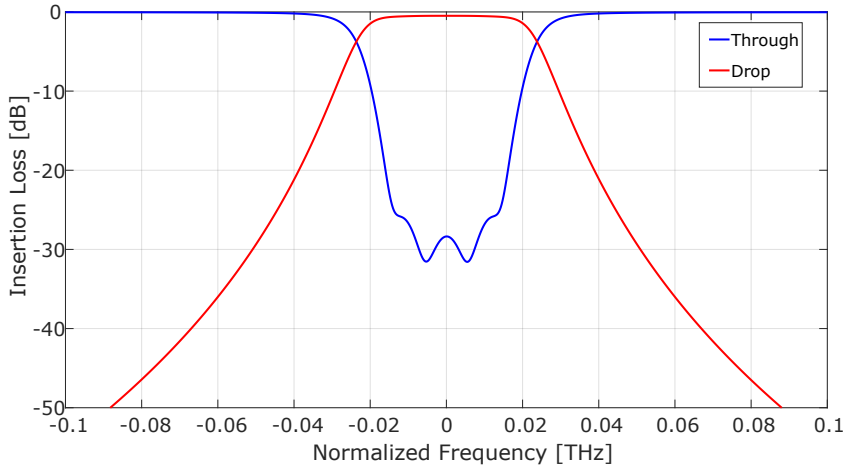


Figure 3.5: Nominal Through- and Drop-ports' frequency response simulated.

behaviour of the filter in the proximity of the bandwidth is more critical than the one far away from it and also to reduce the complexity of the simulation and thus the computation time.

3.4. PCA's Application

In order to successfully apply the PCA method to this scenario, as previously said, some principal components have to be found. The necessities at this point are that these parameters must be cheap to measure and have high variabilities so that they can approximate the PCA's eigenvectors as much as possible. Furthermore, the number of principal components had to be as low as possibile in order to have a reduced number of measurement to do, but at the same time the number has to be high enough not to lose information. Starting from these consideration, a research for the most suitable parameters began. In [30] several parame-

ters' distributions for a similar type of filter were collected and discussed. Starting from this data, a study on the more adapt filter's parameters for the role of principal components was done. The result was the choice, among all the quantities which describe the filter, of the Output Power (P_{out}) and the Channel Isolation at 50 GHz (from now on referred as "Ch. Isol.") both defined below. In fact, beside presenting a good variabilities, these quantities are fast and don't require expensive equipment to be measured (only a power meter, a tunable Dirac's delta and a reference signal are needed).

P_{out} is here considered as the average power measured at the Trough-port when the previously presented input signal is the input of the filter. It is calculated in the whole frequency span simulated. The Relative Output Power ($P_{out,r}$) is P_{out} divided by the integral power of the input signal. It will be used to give a clearer interpretation of the measurements.

The Ch. Isol. is here considered as the maximum amplitude of the Drop-port frequency response between the one at -50 GHz and the one at $+50$ GHz from the central filter frequency. Even if this quantity is usually expressed in dB, for this thesis' aim it will be expressed in linear in order to ease the fitting procedure hereinafter.

The idea for obtaining the same information MSE would give about the DUT's quality was, instead of the longer and expensive procedure to actually measuring it, to exploit the correlation coefficients between the MSE and P_{out}/Ch. Isol. From a Cartesian point of view, this is equal to have two orthogonal directions (the principal components) and to

express the MSE as a linear combination of the two. Since this is not the formal PCA method, P_{out} and Ch. Isol. will not result exactly independent and orthogonal eigenvectors but also their correlation will have to be computed. The best scenario will be that the P_{out} and Ch. Isol. correlation will result weak so that both of these parameter can give different kind of information about the MSE.

For this thesis the correlation coefficients were calculated using the Person correlation coefficients which definition is reported in Equation (3.4),

$$\rho_{X,Y} = \frac{Cov(X,Y)}{\sigma_X \sigma_Y}, \tag{3.4}$$

being $\rho_{X,Y}$ the correlation coefficient, X and Y two random variables, Cov(X,Y) the covariance between X and Y, and σ_X and σ_Y the standard deviation of X and Y.

The correlation relationships between the parameters of interest is the one schematized in Figure 3.6. If the correlation between MSE and one of the considered principal components is strong, the result will be an accurate linear fitting between the two quantities. Having this precise linear fitting would translate filter's quality standards for the MSE in, for instance, $P_{out,r}$ thresholds. After exploiting the strongest correlated with the MSE principal component, the other one, if its correlation with the MSE is enough high and its correlation with the first principal component is sufficiently weak, can be used to refine the prediction.

Different ways of taking decisions about the filter with the help of the

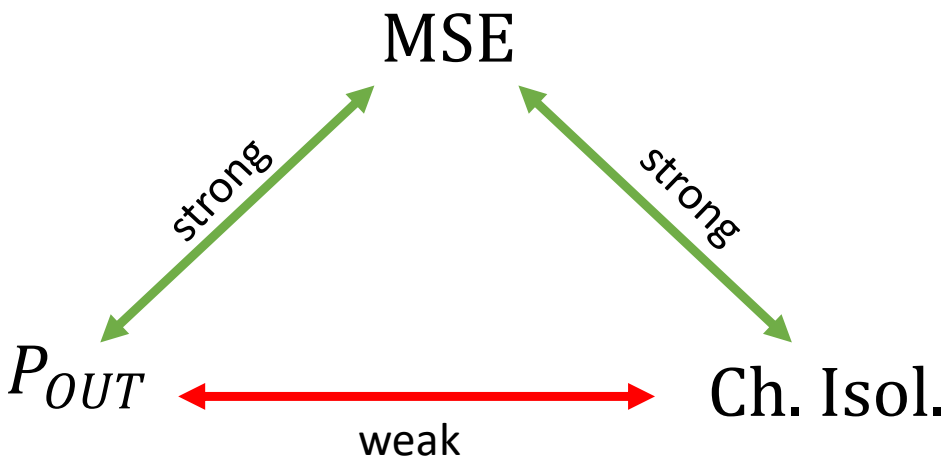


Figure 3.6: Desired correlation relations between parameters of interest.

second principal component will be presented in the next chapter, when numerical results will be presented.

4 | Numerical Results

In this chapter the numerical result obtained through the simulation of the presented filter are exposed. First the results with a singular parameter perturbed are presented, while after the outcomes of simulations with all three kinds of perturbation merged are exposed. Eventually the results are discussed.

This chapter is divided in the following sections:

- 4.1 Singular Parameter Perturbation,
- 4.2 Merging of the Parameters' Perturbations,
- 4.3 Discussion.

4.1. Singular Parameter Perturbation

As first case the correlations of interest of the mentioned filter were studied applying only single parameters perturbations.

4.1.1. Phase Perturbation

Waveguides' phase is the first parameter which was perturbed. Having the phases not impaired is an important point for the correct functioning

of the filter but, unfortunately, phases are easily subject to perturbations often present in this type of devices. In fact the causes of this kind of disturbance are various: it could be due to the heating of the waveguides for external reasons, to crosstalk between thermal actuators and to disruptions in the process of fabrication of the circuit [31] [11]. Several filters with phase perturbations were tested: 4000 filters for each perturbation range.

Figure 4.1 shows an example of phase perturbation distribution. In this first example uniform non-correlated distributions were used, to model the variety of the causes for this kind of perturbation.

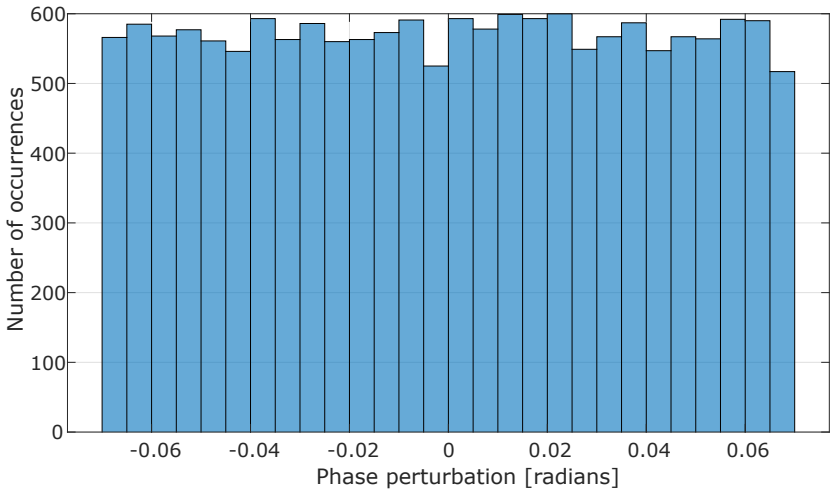


Figure 4.1: Phase perturbation distribution example ($-\pi/45$ <phase perturbation $< +\pi/45$).

In figure 4.2 100 filters frequency responses under the Figure 4.1's perturbations are shown.

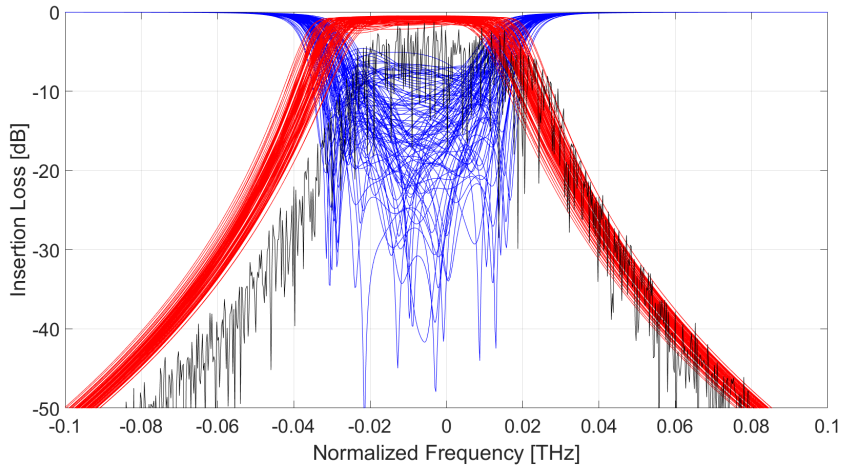


Figure 4.2: Filter frequency response ($-\pi/45$ <phase perturbation < $+\pi/45$).

In order to show a complete view, in figure 4.3 100 filters frequency responses after the application of the TED technique are shown. In figure 4.4 are shown the convergence plots of the TED technique for this particular scenario. The used algorithm's goal for this application was always to minimize as much as possible the previously defined P_{out}.

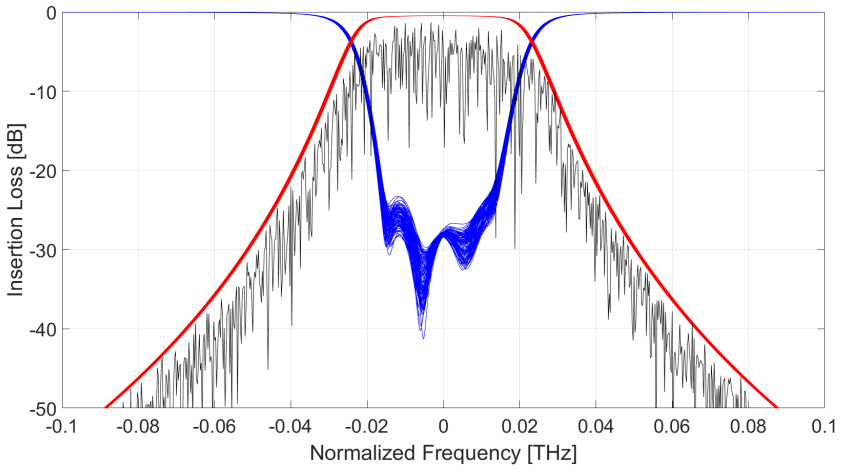


Figure 4.3: Filter frequency responses after TED ($-\pi/45$ <phase perturbation $< +\pi/45$).

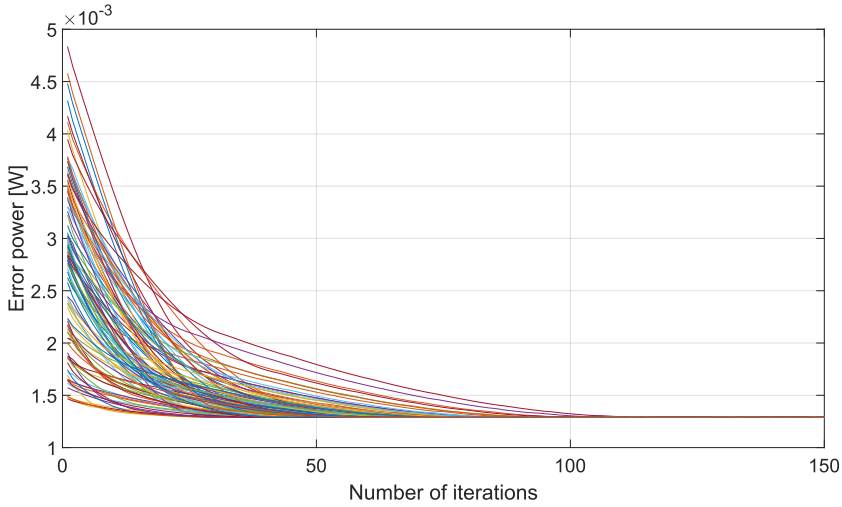


Figure 4.4: P_{out} vs. Number of TED iteration.

The tested perturbations were from $-\pi/55 <$ phase perturbation $< +\pi/55$ to $-\pi/5 <$ phase perturbation $< +\pi/5$. After collecting the data of MSE, P_{out} and Ch. Isol. for every filter simulated for this process (44000 filters) it was possible to plot the values of the found correlations

as can be seen in figure 4.5, 4.6, 4.7 and 4.8.

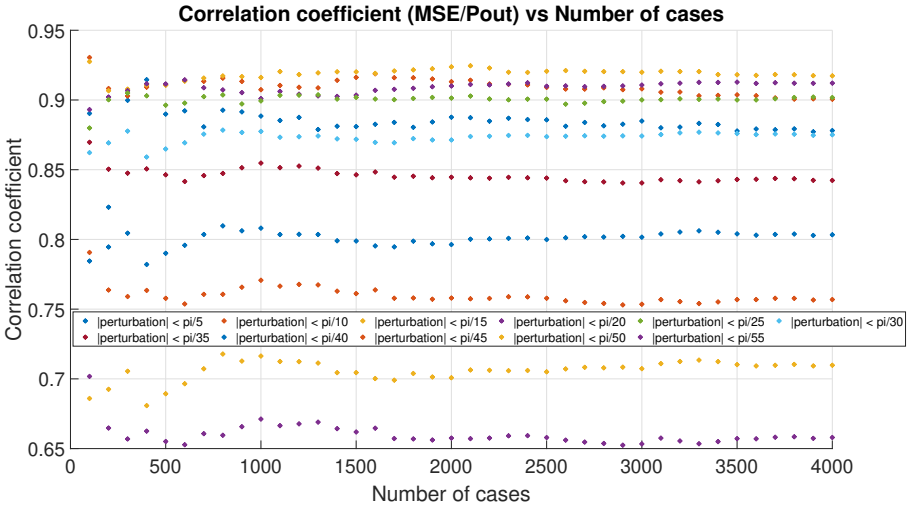


Figure 4.5: MSE/P_{out} correlation coefficients for different phase perturbation values.

As shown in the previous image the trend of the correlation coefficients has an initial transient but then each of them converges to an "asymptotic" value which is the one taken in consideration for our discussion. In fact this value is the more reliable since it is evaluated after a large number of simulations (4000 each) and, for the following correlation coefficients, only this asymptotic value will be taken into account.

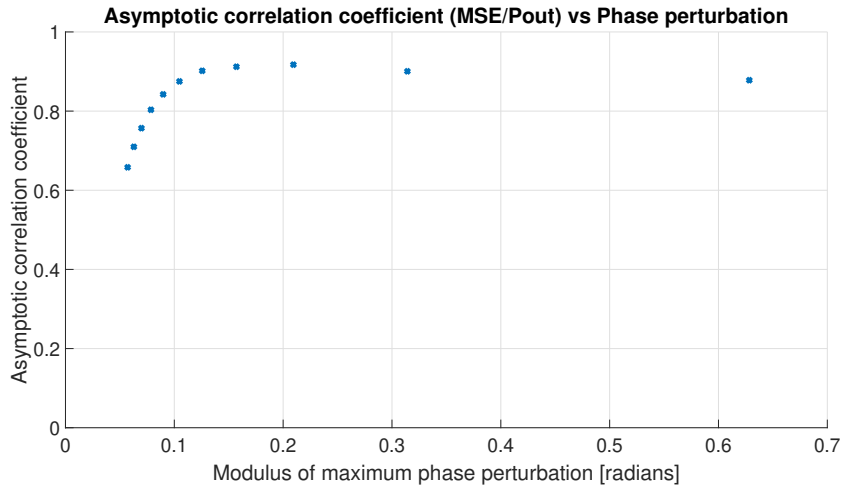


Figure 4.6: MSE/P_{out} asymptotic correlation coefficients for different phase perturbation values.

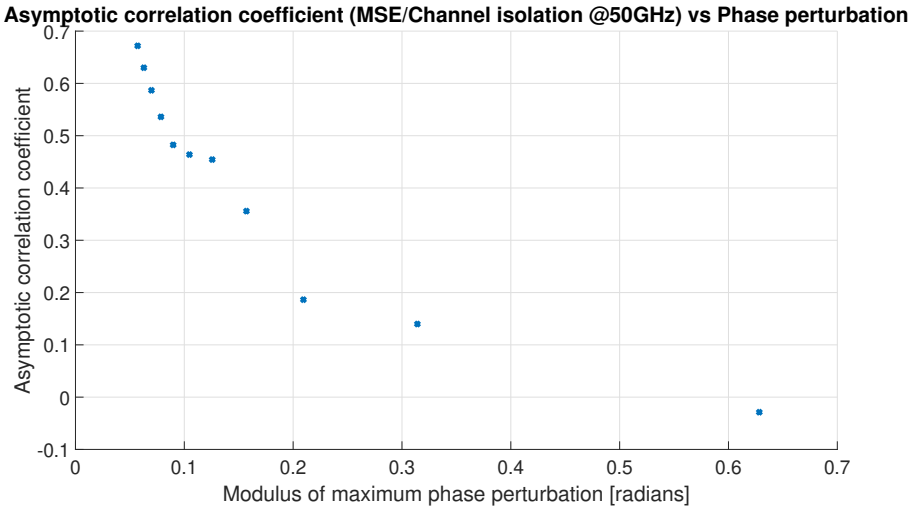


Figure 4.7: MSE/Ch. Isol. correlation asymptotic coefficients for different phase perturbation values.

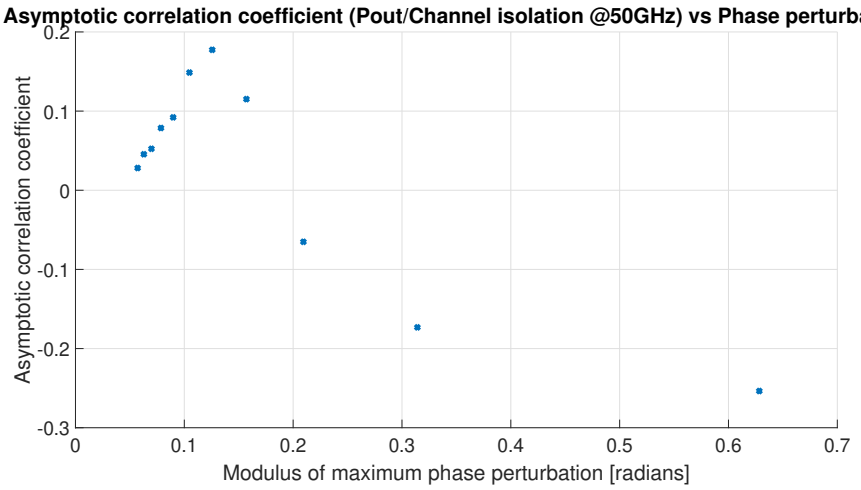


Figure 4.8: P_{out}/Ch. Isol. asymptotic correlation coefficients for different phase perturbation values.

It can be seen from the previous plots that correlation coefficient grows and then "slowly" falls for the MSE/P_{out} (always keeping itself at a quite high value) increasing the modulus of maximum phase perturbation. The MSE/Ch. Isol. correlation coefficient instead starts at about 0.7 but then has a fast decay when the modulus of maximum phase perturbation increases. The P_{out}/Ch. Isol., which it is desirable to be as small as possible, keeps itself at low values for all the perturbations first increasing and then decreasing. When, in the correlation plots above, the correlation coefficient becomes negative it means that the two quantities are inversely proportional, meaning that if the first will increase, the second will decrease.

In Figure 4.9 and 4.10 it is also possible to see the MSE plotted against first the $P_{out,r}$ and after the Ch. Isol. In these figures only the results taken in consideration are the $-\pi/45 <$ phase perturbation $< +\pi/45$,

$-\pi/30 <$ phase perturbation $< +\pi/30$ and $-\pi/15 <$ phase perturbation $< +\pi/15$.

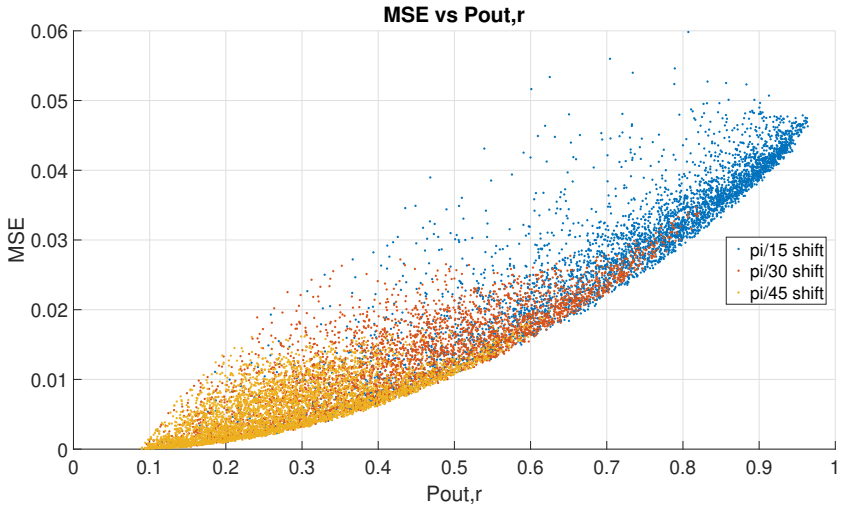


Figure 4.9: MSE vs $P_{out,r}$.

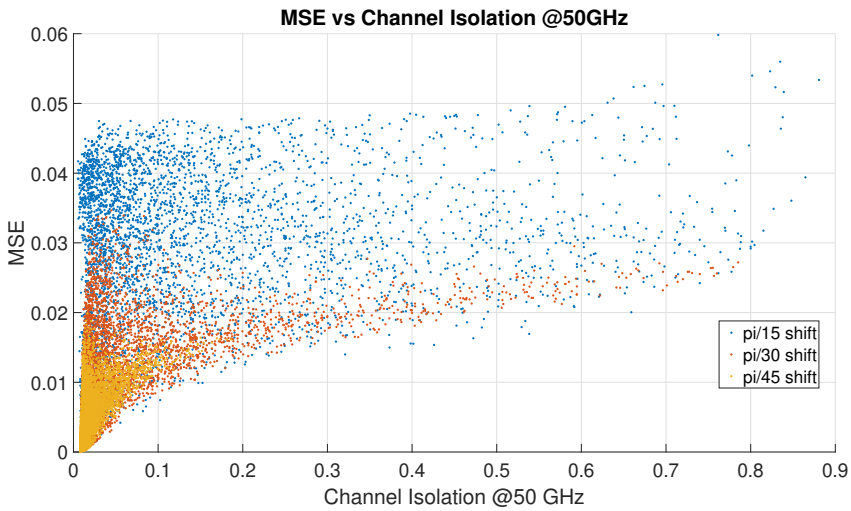


Figure 4.10: MSE vs Ch. Isol.

From the distribution of points of the two previous plots and the collected correlation data presented, the primary principal component to consider

in this case was $P_{out,r}$. So a linear fitting was made as can be seen in Figure 4.11 having this line the following equation:

$$MSE = m \cdot P_{out,r} + q, \tag{4.1}$$

where $m = 0.05069$ and $q = -0.007991$.

Once having a linear fitting it is possible to project the values of $P_{out,r}$ into the MSE ones and so making "predictions". For example let us suppose the foundry wants all its filters with $MSE < 0.01$. Using the presented approach it is possible to split the plane of Figure 4.11 (where every point represents a filter) into four subsections, as can be seen in Figure 4.12, finding the corresponding threshold in $P_{out,r}$ which is 0.35492.

The bottom-right one is for the filters which respect the foundry constraints and this method predicts properly. The top-left one is for the filters which don't respect the foundry constraints and this method predicts properly too. The other two instead are for filters this method fails to predict in the correct way. The chosen names for these groups are (referring to the medical sphere) False Positives and False Negatives. In fact the False Positives are the one this method discard but were actually under the MSE threshold; these filters are unfortunately lost even after when the other principal component will enter the game. The False Negatives are the ones this method takes as good but they don't respect the MSE standard. These last ones are the real issue and they have to be minimized as much as possible.

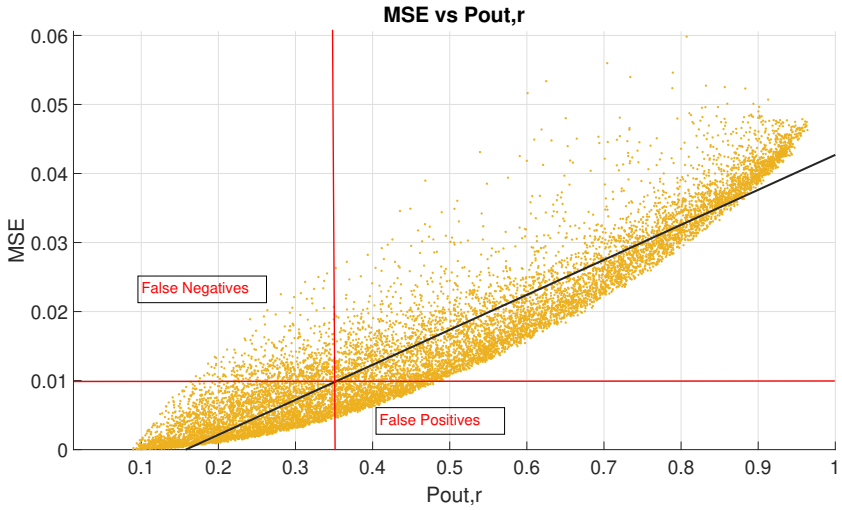


Figure 4.11: MSE vs $P_{out,r}$ linear fitted.

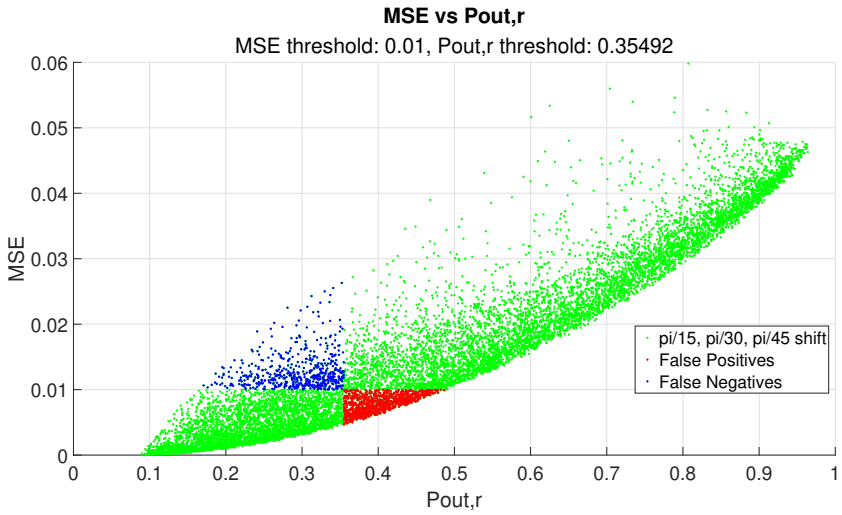


Figure 4.12: MSE vs $P_{out,r}$ predictions result.

In a silicon foundry context the cost of discarding a "good" chip is very low [32] (especially if done during wafer testing) while selling one which does not respect its data sheet could be a real problem. In fact, especially when we are dealing with a large amount of chips like in our case, the cost for the foundry in discarding a single one is very low since the technology

and the materials to produce it are cheap. Instead making an error in the device quality could be a problem.

Up to this point the total number of errors upon 12000 filters are:

False Negatives: 565 (4.71%),

False Positives: 1020 (8.50%),

Total errors: 1585 (13.21%).

To overcome this problem it is possible to take into account in this consideration the other principal component of this testing: in this case the MSE/Ch. Isol. correlation coefficient. In Figure 4.13 the same filters of Figure 4.12 are displayed but, this time, on the horizontal axis there is the Ch. Isol. The goal is to minimize the blue points as much as possible so an idea can be, since a linear fitting is not suitable, to put a threshold in the Ch. Isol. (for example at 0.05) and discard every filter on the right side.

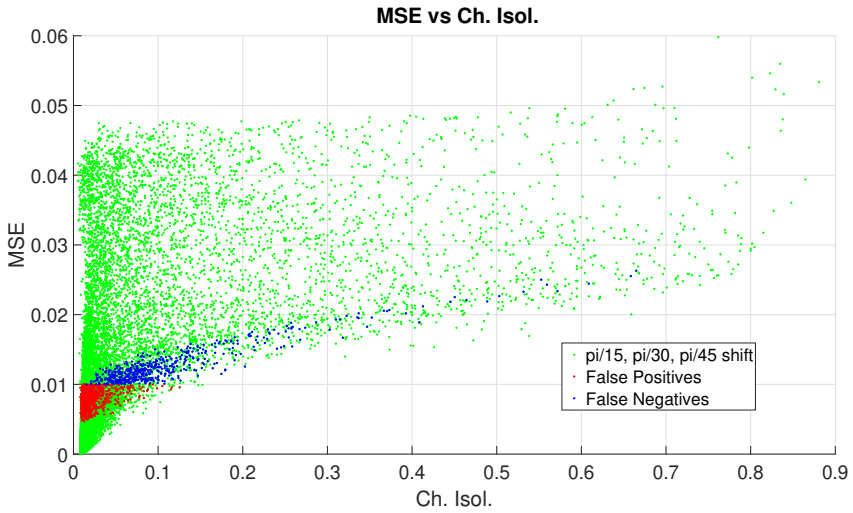


Figure 4.13: MSE vs Ch. Isol. predictions result.

If this is the followed approach, the number of errors upon 12000 filters becomes:

False Negatives: 85 (0.71%),

False Positives: 1020 (8.50%),

Total errors: 1105 (9.21%).

So, essentially, the False Positives fall to a very low number as was the goal. The drawback is, if this further step is done, that a lot of under-MSE-threshold chips will be discarded but is a price to pay in order to have this precision excluding the False Negatives.

Another idea could be setting multiple thresholds in the first and then in the second step of the previous method. This way it will be possible to clusterize the devices into ranges, according to their actual quality, in accordance to their distance to the nominal MSE. The result will be the reduction of the filter waste.

4.1.2. Coupler's gap perturbation

The second perturbed parameter was the coupler's gap distance. Since the used Matlab script only takes as input couplers perturbations, a direct relationship between the Power Coupling Ratio (K) and the gap was found, fitting the data in [11]. Equations (4.2) and (4.3) are the fitting equation used and displayed in Figure 4.14 and 4.15. K_{ext} refers to couplers made with a MZI and a RR and K_{int} refers to couplers made with two RRs. The first fitting is polynomial while the second one is exponential because for the first one there were not enough points to

make it exponential too,

$$K_{\text{ext}} = -1.92 \cdot 10^{-8} \cdot g^3 + 1.85 \cdot 10^{-5} \cdot g^2 - 6.415 \cdot 10^{-3} \cdot g + 0.8201. \tag{4.2}$$

$$K_{\text{int}} = 0.7029 \cdot e^{-0.009838 \cdot g} + 0.2429 \cdot e^{-0.02091 \cdot g}. \tag{4.3}$$

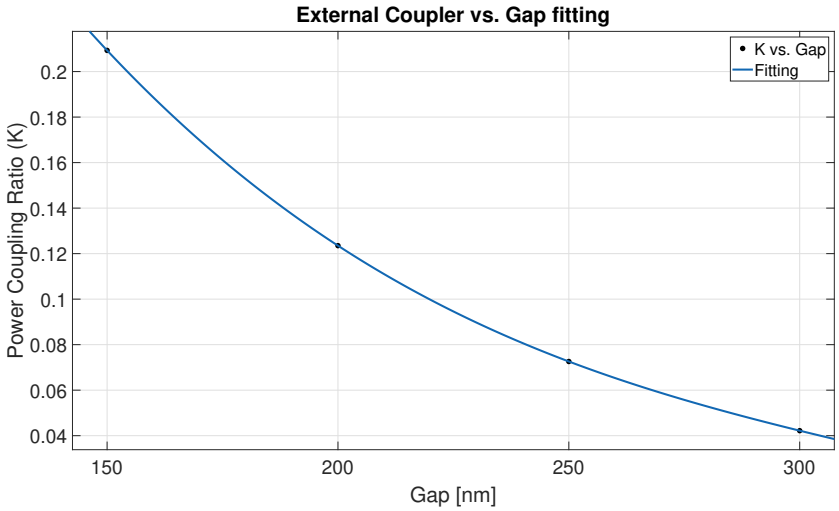


Figure 4.14: external K/gap fitting.

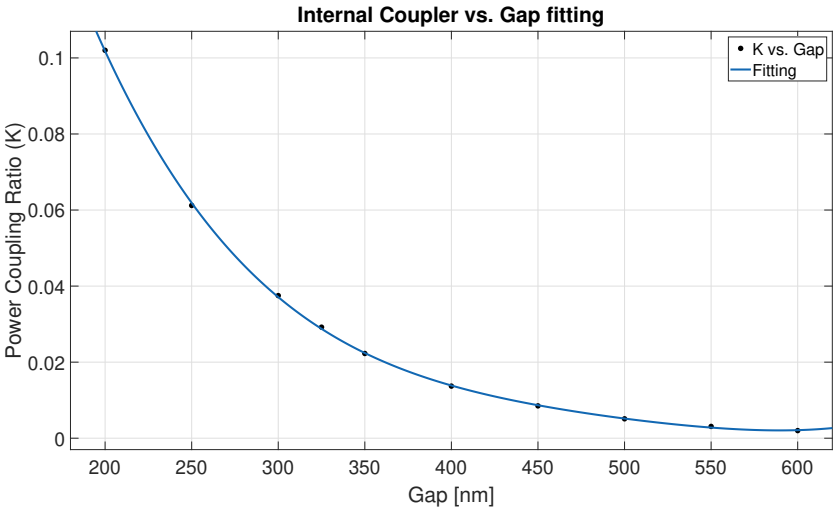


Figure 4.15: internal K/gap fitting.

Then, in analogy with the previous case of phases perturbation, correlation coefficient values were collected for the following gap's perturbation ranges (uniformly distributed): $-1\% <$ gap's perturbation $< +1\%$, $-2\% <$ gap's perturbation $< +2\%$, $-5\% <$ gap's perturbation $< +5\%$ and $-10\% <$ gap's perturbation $< +10\%$.

The results are shown in Figure 16, 17 and 18.

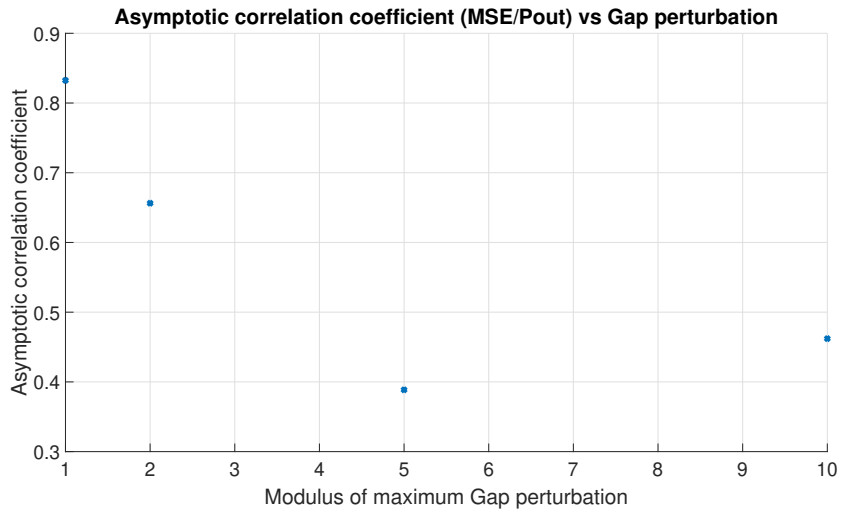


Figure 4.16: MSE/P_{out} asymptotic correlation coefficients for different gap perturbation values.

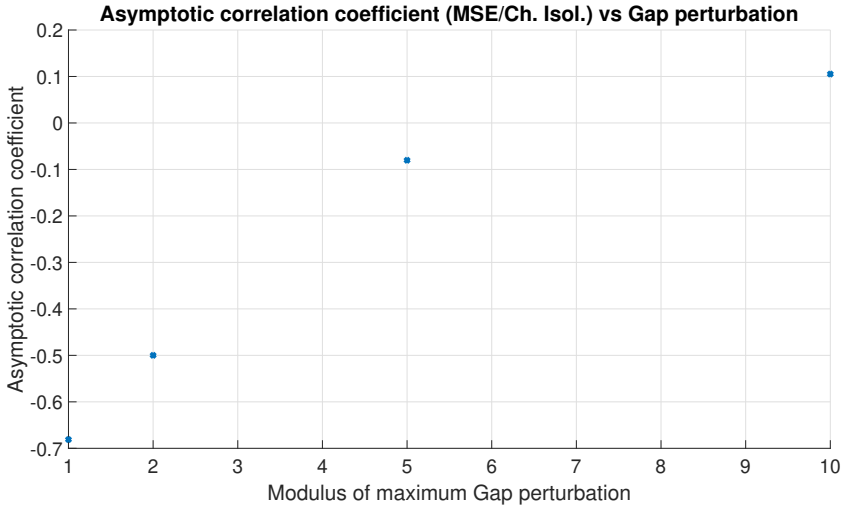


Figure 4.17: MSE/Ch. Isol. asymptotic correlation coefficients for different gap perturbation values.

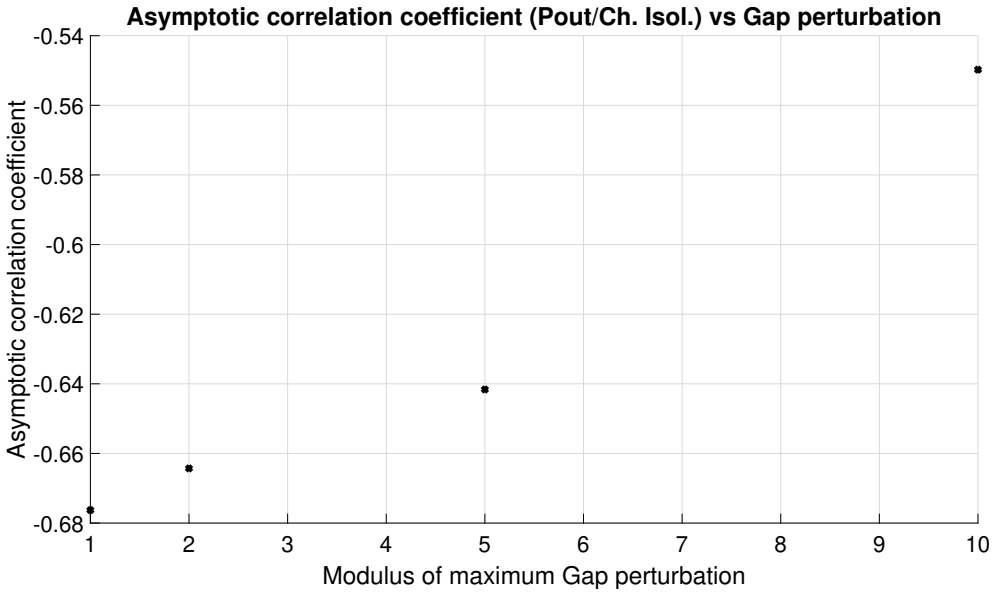


Figure 4.18: P_{out}/Ch. Isol. asymptotic correlation coefficients for different gap perturbation values.

In this case the correlation coefficients found are not as useful as in the phase perturbations' scenario. In fact the only perturbations who leads to acceptable correlation values are the $-1\% <$ gap pert. $< 1\%$ and $-2\% <$ gap pert. $< 2\%$ while, for the other cases, the MSE/P_{out} and the MSE/Ch. Isol. fall to low values. This means this method cannot be applied successfully for this amount of gap perturbations.

In fact, as we can see in Figure 4.19 and 4.20, an accurate linear fitting is not possible to track. It could be may possible if lower perturbation would be chosen.

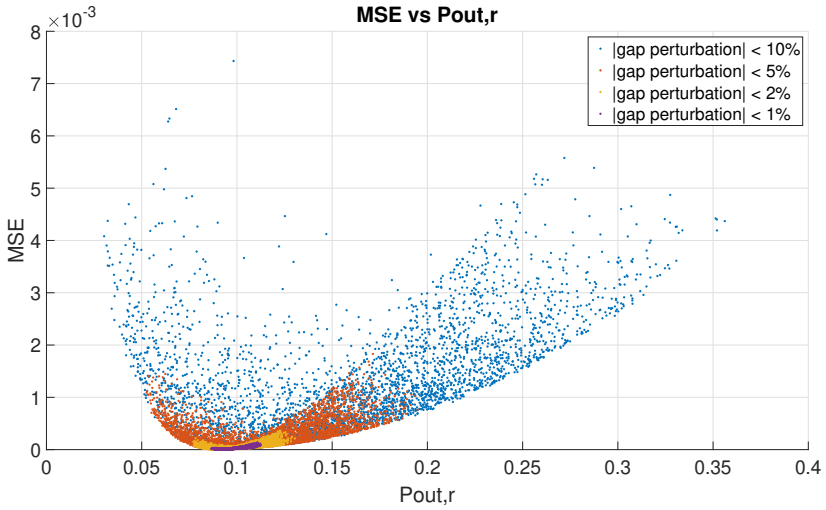


Figure 4.19: MSE vs. $P_{out,r}$.

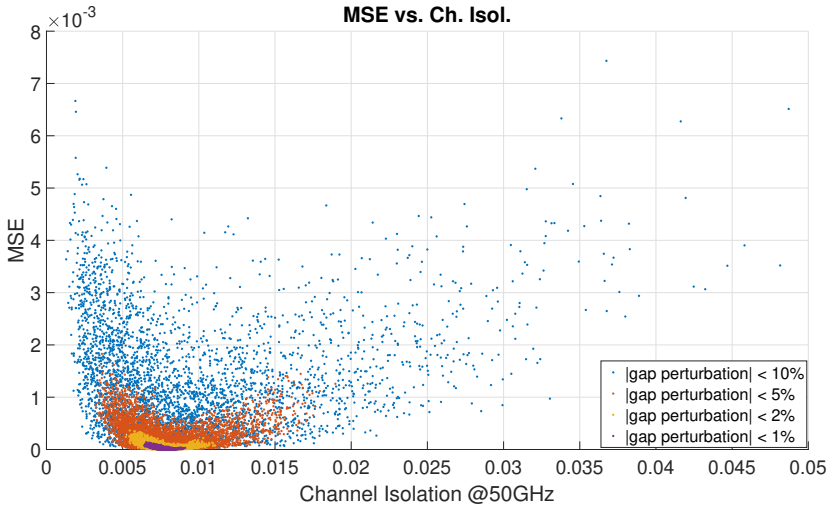


Figure 4.20: MSE vs. Ch. Isol.

4.1.3. Round Trip Loss perturbation

As third parameter to change RTL was chosen. Then, in analogy with the previous case of perturbation, correlation coefficient values were collected for the following RTL ranges (uniformly distributed): 0.01 dB/round <

RTL < 0.1 dB/round, 0.05 dB/round < RTL < 0.15 dB/round, 0.05 dB/round < RTL < 0.4 dB/round, 0.1 dB/round < RTL < 0.5 dB/round and 0.1 dB/round < RTL < 1dB/round.

The correlation coefficients values are displayed in Figure 21, 22 and 23.

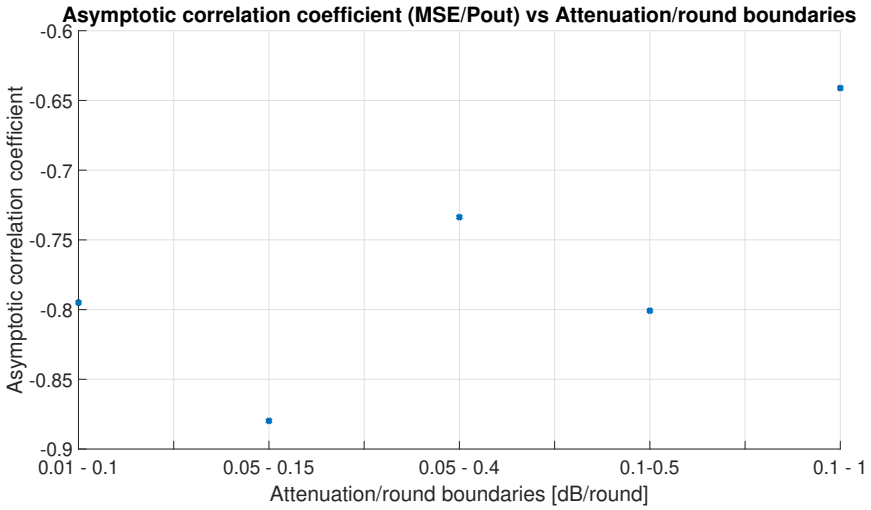


Figure 4.21: MSE/$P_{out,r}$ asymptotic correlation coefficients for different RTL values.

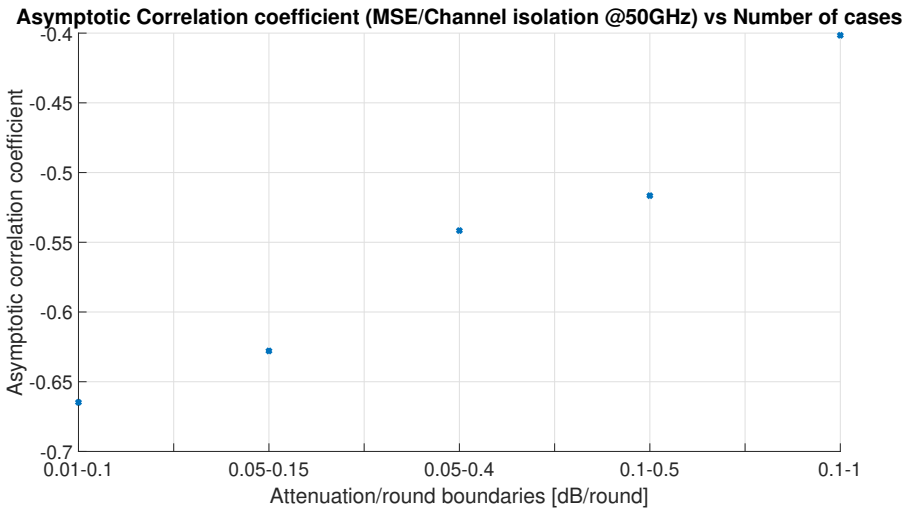


Figure 4.22: MSE/Ch. Isol. asymptotic correlation coefficients for different RTL values.

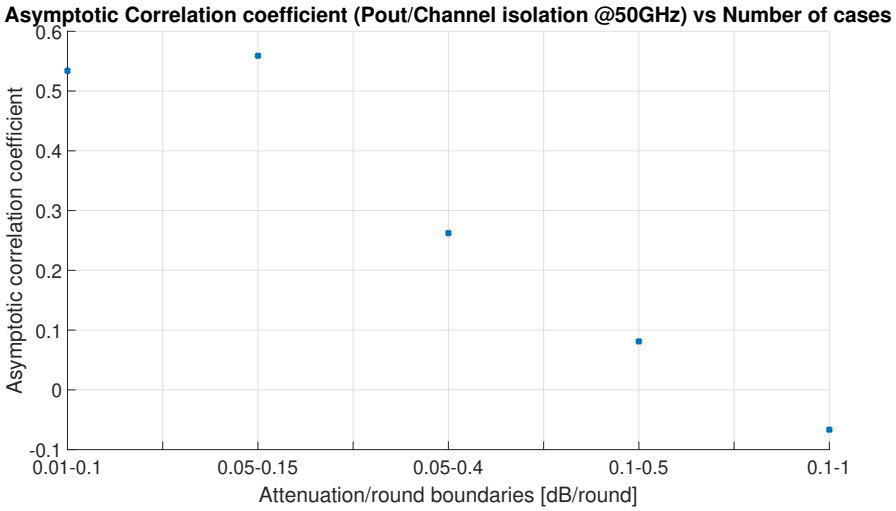


Figure 4.23: $P_{out,r}$/Ch. Isol. asymptotic correlation coefficients for different RTL values.

As can be seen from the previous data, for the first (and lowest) RTL values the MSE/P_{out} correlations are strong even if they are negative and the same can be said for MSE/Ch. Isol. ones. Unfortunately the P_{out}/Ch. Isol. ones are quite strong too for the low RTL values, meaning that P_{out} and Ch. Isol. bring the similar information about MSE. Increasing the values of RTL, the correlation become worse and they are no longer useful.

In Figure 4.25 and 4.26 the filters are plotted in the same way as the other two cases of perturbation were. Still here, considering the whole amount of cases, a linear fitting would be very inaccurate but it should be more useful to do if just the lowest values would be considered.

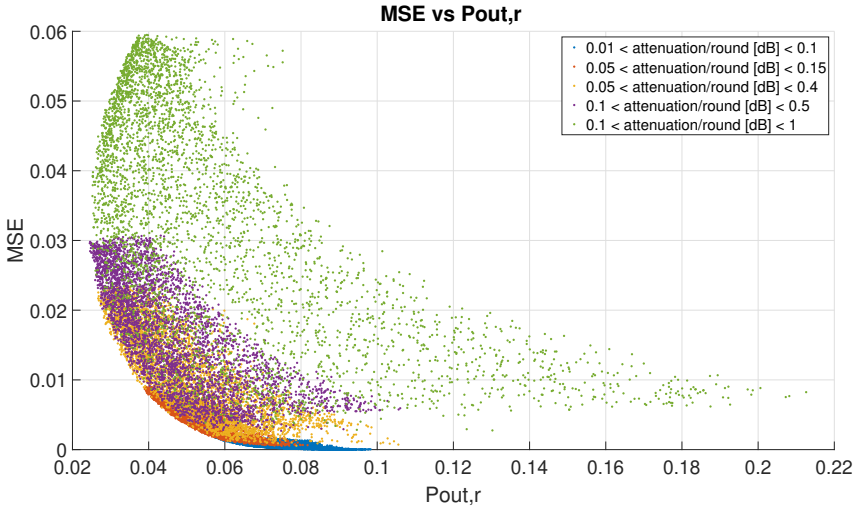


Figure 4.24: MSE vs. $P_{out,r}$.

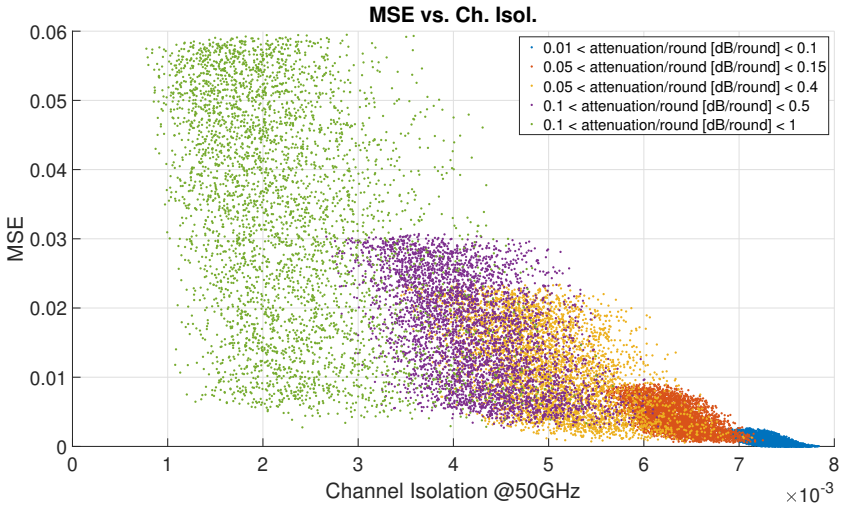


Figure 4.25: MSE vs. Ch. Isol.

4.2. Merging of the Parameters' Perturbations

For this second round of simulations a more complete situation was engineered. In fact now all the three kinds of perturbations separately treated before were applied together to the filter using the distributions for couplers' gap perturbations and RTL previously used in [33] with different values of correlation coefficient $(1\%, 2\%, 5\%, 10\%)$. This time a correlation between these perturbations was introduced because in a real foundry it is reasonable to think of a correlation between the defects present in the chips due to disruptions in the machinery. Instead for the phase perturbations an uniform distribution was used, as can be seen in Figure 4.26, because the reasons behind phase perturbations, as previously stated, could be due to various phenomena like thermal crosstalk, fabrication imperfections and thermal fluctuations.

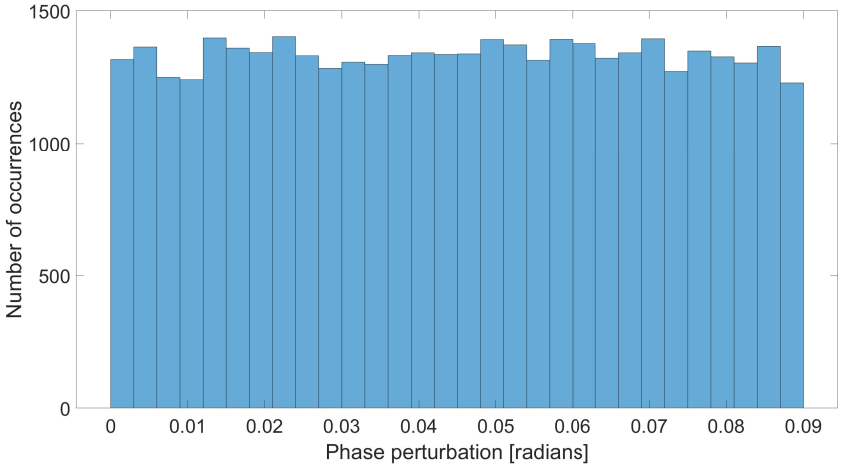


Figure 4.26: Phase perturbations distribution.

The correlation coefficient results can be seen in Figure 5.27, 5.28 and 5.29.

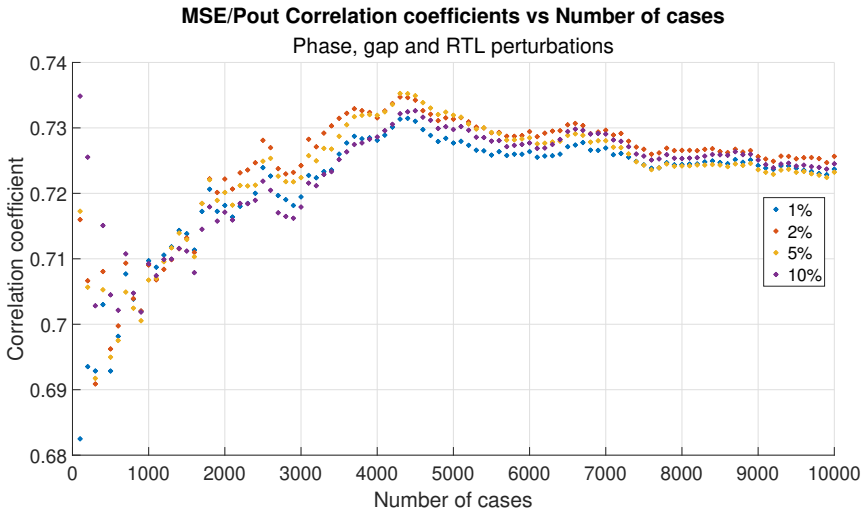


Figure 4.27: MSE/P_{out} correlation coefficients for different correlations in perturbations.

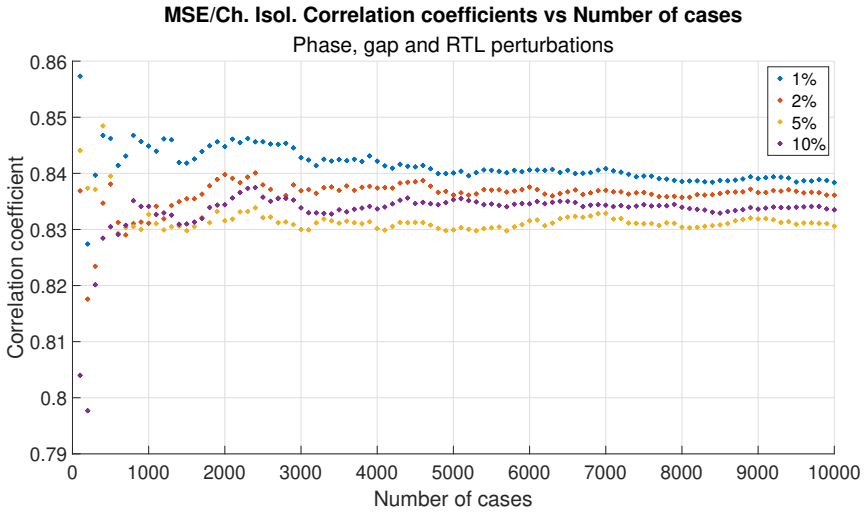


Figure 4.28: MSE/Ch. Isol. correlation coefficients for different correlations in perturbations.

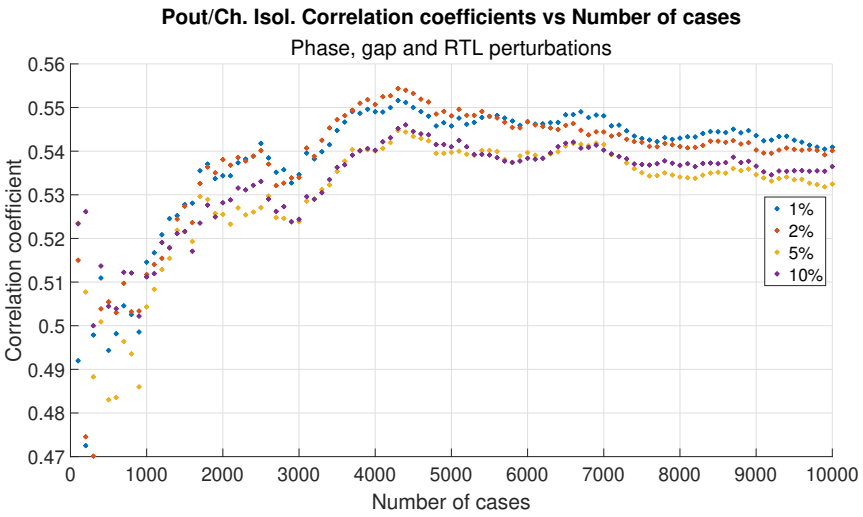


Figure 4.29: P_{out}/Ch. Isol. correlation coefficients for different correlations in perturbations.

From these figures a quite high value for the correlation between MSE and Ch. Isol. can be noticed. Since this correlation is stronger than the MSE/P_{out} one (whose correlation coefficients are quite high too) Ch. Isol. was used as primary parameter. Unfortunately also P_{out}/Ch. Isol. correlation is quite strong but having this high values for MSE/Ch. Isol. makes possible to predict, with an acceptable tolerance, the filters quality.

As can be seen from the previous figures the values of the correlation coefficients of all three kinds change for an almost negligible quantity changing the correlations between the perturbations. For this reason just 5% correlation perturbation results will be discussed.

The same procedure as before was repeated but this time, since the MSE/Ch. Isol. correlation was very high, this was used for a linear fitting and the second correlation was used for a further reduction of False Negatives.

In Figure 4.30 and 4.31 the filters are plotted by means of their MSE against Ch. Isol. (with fitting) and $P_{out,r}$.

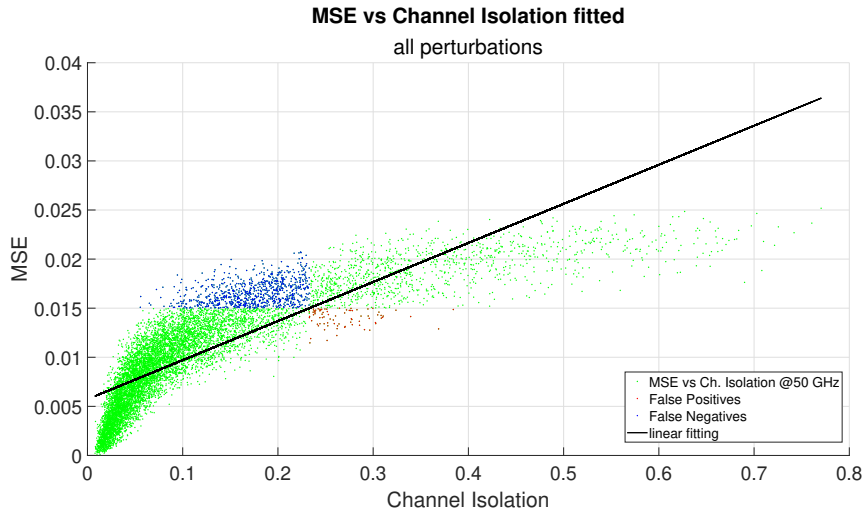


Figure 4.30: MSE vs. Ch. Isol. linearly fitted.

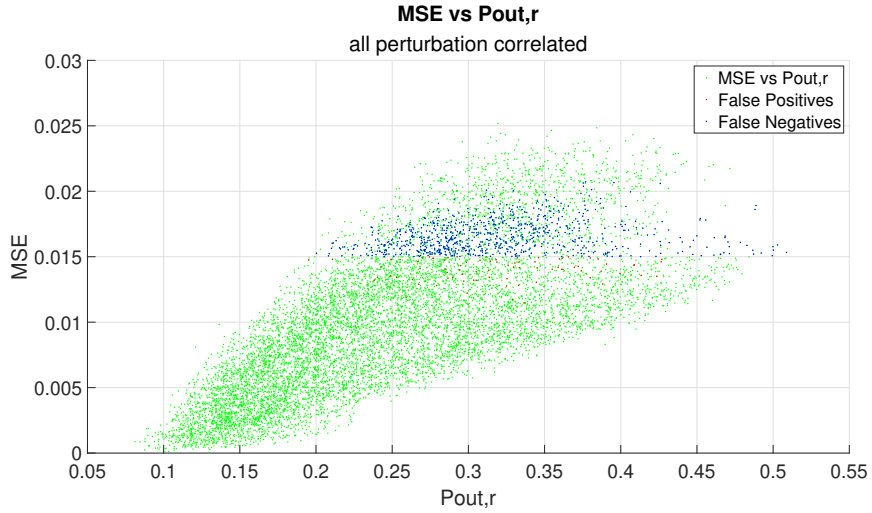


Figure 4.31: MSE vs. $P_{out,r}$.

In analogy with the phase perturbations' case, an MSE threshold was chosen (0.015) and thanks to the linear fitting (Equation (4.4)) a Ch. Isol. threshold can be found too (0.233),

$$MSE = m \cdot Ch.Isol. + q, \tag{4.4}$$

where $m = 0.0398$ and $q = 0.0057$.

At this point making predictions is possibile and the results, over 10000 filters are:

False Negatives: 821 (8.21%),

False Positives: 80 (0.8%),

Total errors: 901 (9.01%).

Like in the previous case here the precision of these predictions can be further improved by also setting one or multiple thresholds in the MSE/$P_{out,r}$ plot.

If we follow this further procedure and set a threshold at $P_{out,r} = 0.276$ the results are:

False Negatives: 178 (1.78%),

False Positives: 80 (0.8%),

Total errors: 258 (2.58%).

Adopting this procedure there is an improvement in the amount of False Negatives cases but all the filters above the $P_{out,r}$ threshold which respected the MSE threshold are wasted. Once again this trade-off can be accepted or not, depending on the needs of the foundry.

4.3. Discussion

The goal of this work was to provide a novel approach to the testing of the PIC environment. In order to overcome the limits and the costs of the nowadays employed testing techniques the developed method had to be fast, flexible and low cost. For low cost are both intended the low time resources and the cheap equipment needed. The proposed method, exploiting the PCA method, can overcome the previously mentioned impairments. In fact the only two parameters to actively measure are (for filters) the P_{out} and the Ch. Isol., both obtainable through a simple and fast power meter measurement.

These two parameters are clearly not mandatory and can depend on the PIC technology and nature. For what concerns photonic integrated filters, the previously mentioned research was performed and these occur to be the most suitable ones for this treatment. If instead the PIC under testing was another typology of device, whose performance is strongly dependent on other factors and quantities a filter does not number in his most important, clearly other principal components would have to be found and the method effectiveness would have to be proven again. Still, this method can be surely applied for filters with these principal components with a good margin of success if they are not severely perturbed.

Furthermore, this approach can be used at the a wafer-level testing stage. In fact, if the correct semi(automated) alignment equipment is present and the vertical coupling is possible (by means of grating couplers or thanks to the probe techniques [4] [5]), these simple optical measures can

be performed on-wafer. This would reflect on a massive saving of time and resources. In fact, as previously discussed, wafer-level testing enables to identify at an early stage the yield of a particular wafer and so, if necessary, discard the entire load in order to contain the costs. Unfortunately, having a (semi)automated equipment supplied with a suitable algorithm for the optical alignment is compulsory in order to perform wafer-level testing. This cost cannot be reduced by this thesis' work.

Looking at the actually obtained results, different considerations have to be made. This proposed method seems to work properly for low perturbations of the three parameters considered. First of all, the singular perturbations cases have to be discussed. Among these the waveguides' phases were the first to be perturbed. As we can see in the last section's extracted correlation coefficients, the MSE/P_{out} correlation is strong for almost all the perturbation values. Instead, unfortunately, the MSE/Ch. Isol. correlation, unless for the first (and weakest) phase perturbations, tend to be weak and, from when the modulus of maximum phase perturbation is $\frac{\pi}{15}$, very weak (< 0.2). For what instead concerns the P_{out}/Ch. Isol. a very weak correlation is present among all the the phase perturbations. This is a symptom of almost orthogonality between the chosen principal components. After having performed the linear fitting predictions can be made about the filter quality. They depend on the designer and foundry necessities, so it is their work to set the suitable thresholds, but the examples provided in the last section resulted in reasonable errors probabilities. An important point to stress is the fact that the probability of having a False Negative case can be arbitrarily reduced at

the cost of discarding a larger number of over-MSE threshold DUTs.

Then the couplers' gaps were perturbed. This time results were not so encouraging. In fact, the MSE/P_{out} correlation is high (> 0.82) for the 1% case but then, even if it is still acceptable for the 2% case ($> 65\%$), falls to low values and tend to be almost useless for this treatment. Almost the same reasoning can be done for the MSE/Ch. Isol. correlation. Instead the P_{out}/Ch. Isol. one keeps itself at considerable values ($-0.68 <$ corr. coeff. < -0.54) meaning that the principal components chosen bring for almost the 54% the same information about the MSE. For this case it was not possible to have a reasonable error probability in the predictions of the filters' quality. Probably, and with less accuracy than the phases cases, a discrete result would have been obtained if weaker perturbations would have been considered.

As last parameter to perturb RTLs were chosen. For this case the MSE/P_{out} correlations are quite strong and the MSE/Ch. Isol. ones have reasonable values. Unfortunately, also in this case, the P_{out}/Ch. Isol. correlation is relevant (especially for the two weaker perturbed cases) meaning that, for this two, which also have the highest values for the other correlations, the principal components have for at least the 52% the same information about the MSE.

For what concerns instead the, more complete, case of all the perturbed parameters merged together, smaller individual perturbations than the previous cases were applied resulting in less distorted filters. The evaluated correlation coefficients for MSE/P_{out} and MSE/Ch. Isol. result

high (especially the second). Unfortunately also the P_{out}/Ch. Isol. correlation is relevant but, since the first two are very high, reasonable error predictions are feasible. In fact the resulting error probabilities for False Negatives and False Positives filters are reasonable and, like in the phase perturbation case, further steps to make this result even more precise can be done at the cost of discarding over threshold filters.

After having discussed the numerical results of this method it is possibile to confirm the effectiveness of the PCA approach applied on testing. This particular method, if adopted in a foundry context can provide, with a certain degree of precision, a fast and cheap solution to the testing today's main problems.

Conclusions

In this work a novel method to perform testing on PICs exploiting a statistical approach is discussed. This method focuses on the reduction of the costs, in terms of both equipment and time needed. In fact, nowadays, testing has a massive impact on the overall PIC cost (up to 29%) and the main factors which contribute to this cost have to be sought in the equipment needed and in the time taken for the various operations [12].

This works adapts a well-known statistical method like PCA to an engineering environment adjusting some of its original aspects in order to make it suitable for a foundry context. For this reason particularly easy and cheap to measure parameters were chosen to estimate the device's quality.

The effectiveness of this method was proven by testing, through circuital-functional simulations, a silicon photonics device [29] which represents the state of the art in terms of reconfigurable filters for the telecom/datacom environment. Furthermore, perturbations of three different kinds were modelled both for deeper investigating the effectiveness of the method with different types of disturbs and for experiment it on a realistic scenario.

A study on the correlation of the chosen principal components was performed, so that, through linear fitting and threshold setting, the overall quality of a PIC can be estimated with a certain uncertainty. Moreover, it is important to point out that the precision of this method can be adjusted depending on the needs of the foundry exploiting the trade-off between accuracy and discarded PICs.

Future developments for the presented method could be the its application to different PICs, which are described by different parameters than the ones of the studied device. For instance photodetectors or active devices could be the next subjects of this method making it even more flexible.

For these other devices the same approach could be followed, identifying the principal components and evaluating correlations among them and the chosen goal parameter in different scenarios, each with particular kinds and amount of perturbations.

Another development for this work's method could be its validation under different kinds of perturbed parameters than the tested ones. For example the waveguides roughness and the chromatic dispersion could be taken into account by simulation models, in order to take an even more complete picture of the methods capabilities and limitations.

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