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SIMULATION AND ANALYSIS OF MODULAR MULTILEVEL CONVERTERS BASED ON ISOMORPHISM AND PERIODIC SMALL-SIGNAL ANALYSIS

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Abstract

The current shift in generation mix towards renewable energy sources, typically interfaced to the grid through power electronics converters, is significantly changing many facets of modern electric power systems, such as planning and operation. In this context, power system simulation is crucial because it enables scholars and power system operators to investigate the fast dynamics of converters, their controls, and interactions with traditional power system elements. However, to do so in a fast and accurate manner, conventional simulation tools need to be updated by implementing advanced techniques specifically tailored for converters.

This thesis focuses on the modular multilevel converter (MMC). Its distinctive feature is the presence of a stack of up to several hundreds of identical submodules (SMs) in each of its arms. On the one hand, this modular structure grants the MMC reduced switching losses and scalability to high voltage and power ratings, thus making it a popular technology in high-voltage direct current systems. On the other hand, the MMC topology and its complex control schemes pose several challenges in standard power system simulators tasks, such as power flow analysis, initialisation, electromagnetic transient simulation, and small-signal analysis. The research activity reported in this thesis was mainly devoted to these last two aspects.

Concerning electromagnetic transient simulation, an MMC simulation paradigm based on sub-circuit isomorphism is proposed. This approach - originally conceived to analyse modular electronic circuits such as RAMs - can be profitably exploited to simulate MMCs, since it exploits the common behaviour of structurally identical SMs by clustering them together. Contrary to other simulation approaches in the literature, this method does not require any simplification of the SM electrical model and minimizes the number of equations to be solved at each time step of the time domain analysis, thereby significantly reducing the computational effort at the expense of a small sacrifice in simulation accuracy.

For what concerns small-signal analysis, the periodic small-signal analysis (PAC) is proposed and applied to MMCs. Despite being adopted for a long time by electronics designers, this technique is still a novelty in the power system field. Being a numerical method directly implemented at the simulator level, PAC requires neither extensive pen-and-paper computations nor simplifications in the model of the system under analysis. In addition, the method can take into account intermodulation and frequency up- and down-conversion of a perturbing signal in the frequency spectrum.

Kewords: *Modular multilevel converters, isomorphic circuits, electromagnetic transients, periodic small-signal analysis.*

Sommario

La presenza sempre più significativa nel parco generativo delle fonti rinnovabili, tipicamente interfacciate alla rete mediante convertitori elettronici di potenza, sta rivoluzionando diversi aspetti dei sistemi elettrici moderni, come la pianificazione e la gestione. In questo contesto, la simulazione è un elemento cruciale, in quanto permette di analizzare non solo le dinamiche veloci associate ai convertitori e ai loro controlli, ma anche le interazioni con componenti di rete tradizionali. Tuttavia, per simulare i convertitori in modo veloce ed accurato, è necessario aggiornare i programmi di analisi circuitale convenzionali sviluppando delle tecniche innovative *ad hoc*.

Questa tesi si focalizza sui convertitori multilivello modulari (o modular multilevel converters (MMCs)). Ogni braccio di questo convertitore è composto da un numero elevato di sotto moduli (SM) identici connessi in cascata. Da un lato, questa struttura modulare garantisce perdite di commutazione ridotte e una flessibile estensione della potenza e tensione nominale dell'MMC a valori elevati. Tali proprietà hanno contribuito ad accrescere la popolarità di questa tecnologia nell'ambito dei sistemi ad alta tensione in corrente continua. Dall'altro lato, la topologia modulare degli MMC e il loro sofisticato schema di controllo complicano l'esecuzione di alcune funzionalità tipicamente disponibili nei simulatori di rete convenzionali, come il calcolo del power flow, l'inizializzazione, la simulazione di transitori elettromagnetici e l'analisi di piccolo segnale. L'attività di ricerca descritta in questa tesi è incentrata principalmente su questi ultimi due aspetti.

Per quanto riguarda la simulazione dei transitori elettromagnetici, in questa tesi è stato impiegato un approccio basato sull'isomorfismo. Questo approccio - concepito originariamente per analizzare i circuiti elettronici modulari come le RAM - permette di simulare efficientemente gli MMC raggruppando in ogni braccio gli SM caratterizzati da un comportamento simile. Contrariamente ad altre soluzioni presenti nella letteratura, questo metodo, sebbene non richieda alcuna semplificazione del modello elettrico

degli SM, permette di minimizzare il numero di equazioni da risolvere ad ogni passo dell'analisi nel dominio del tempo, riducendo così l'onere computazionale con una penalizzazione minima in termini di accuratezza.

Infine, nell'ambito dell'analisi di piccolo segnale, questa tesi propone l'analisi periodica di piccolo segnale (o PAC) e la sfrutta per studiare la stabilità di sistemi elettrici contenenti MMC. Sebbene sia adottata da molto tempo nel campo dell'elettronica, questa tecnica è ancora una novità nei sistemi elettrici. Essendo un metodo numerico realizzato direttamente al livello del simulatore, la PAC non richiede nè laboriosi calcoli "carta e penna", nè la semplificazione della rete da analizzare. Inoltre, il metodo permette di tener conto dell'intermodulazione e di fenomeni di sovra e sotto conversione della frequenza di un piccolo segnale di perturbazione con un determinato spettro.

Parole chiave: *Convertitori multilivello modulari, circuiti isomorfi, transitori elettromagnetici, analisi periodica di piccolo segnale.*

Contents

Introduction

Nowadays, the concept of energy is at the heart of many interconnected challenges that the world is facing. The so-called *global energy challenge* indicates that two actions are essential to ensure sustainable development for all: guaranteeing universal access and use of energy, as well as enforcing proper energy resource management, which limits environmental impact and prevents conflicts and inequalities. The Agenda 2030, an action plan signed in September 2015 by the world leaders, proposed 17 Sustainable Development Goals (SDGs), showing the path to be followed towards sustainable development for the whole world. In particular, energy has a prominent role in the seventh SDG, whose mission is: *"Ensure access to affordable, reliable, sustainable and modern energy for all"*. This goal comprises five targets, one of which promotes a substantial increase in the share of Renewable Energy Sources (RESs) in the global energy mix. The pursuit of this specific target implies that also the electricity sector will keep on changing in the future.

In recent years, the integration of RESs has become more and more evident worldwide. For instance, consider Fig. 1, which shows the percentage share of global electricity generation by energy source in 1973 and 2019. Specifically, the penetration of non-hydro RESs and waste (e.g., geothermal, solar, wind, and biofuels) has increased by $10.2\,\%$ from 1973 to 2019. Among others, this trend is given by the progressive deployment of wind and photovoltaic energy sources reported in Fig. 2, which is fostered by policies and support mechanisms, such as *Feed-In Tariffs* [1]. The aim of these incentives is twofold. The first one is to reduce CO_2 emissions and

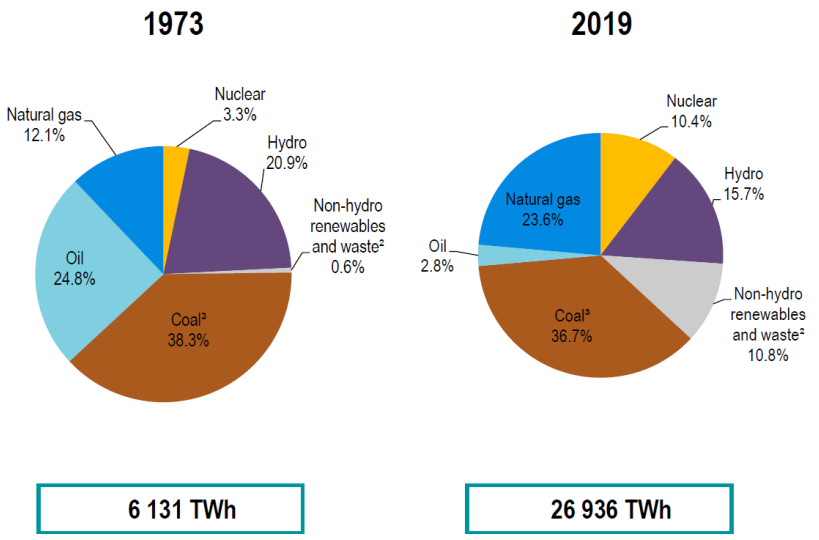

Figure 1: *Share of world electricity generation by source in 1973 and 2019 [2].*

allow countries to be compliant with binding international treaties, such as the well known Paris agreement. The second one is to stimulate the technical and market maturity of RES-fuelled power plants so that in the future they may become profitable even without public subsidies.

Although remarkable, the current rate of penetration of RESs is still insufficient for the years to come. Indeed, compare for instance the projections of the so-called "*Stated Policies Scenario*" and "*Sustainable Development Scenario*" depicted in Fig. 3. The former incorporates today's policy intentions and targets, whereas the latter maps out a way to meet SDGs and other treaties concerning climate change. The fulfilment of these treaties requires more investments in RESs, to the extent that plants based on wind and solar sources will eventually dominate future power systems.

On the one hand, the transition towards this scenario allows reducing the environmental impact of the electricity sector, escaping carbon lock-in, and improving energy security due to a more diversified generation mix. On the other hand, it poses several important challenges, which are pushing modern grids to a turning point.

The energy transition in the electricity sector is a very broad topic. Rather than exploring every nook and cranny of this subject - which would be out of the scope of this thesis - the following sections aim at reviewing some key concepts and highlighting the relevance of the PhD research carried out in this framework.

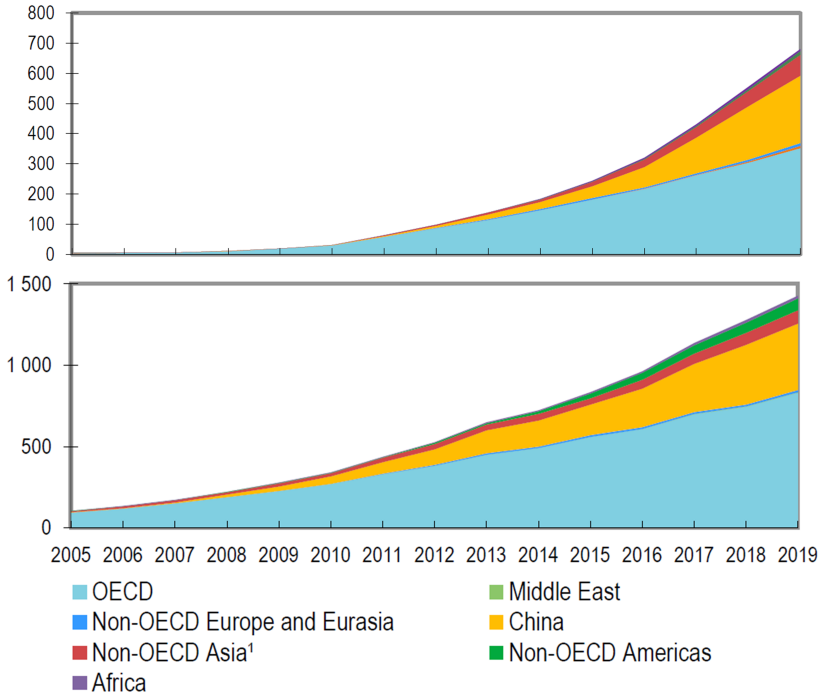

Figure 2: *Solar photovoltaic (upper panel) and wind (lower panel) electricity production [2]. The* OECD *class collects all the countries that belong to the Organisation for Economic Co-operation and Development (e.g., USA, Canada, Australia, most of the European countries). x-axis: year, y-axis: energy production* [TWh].

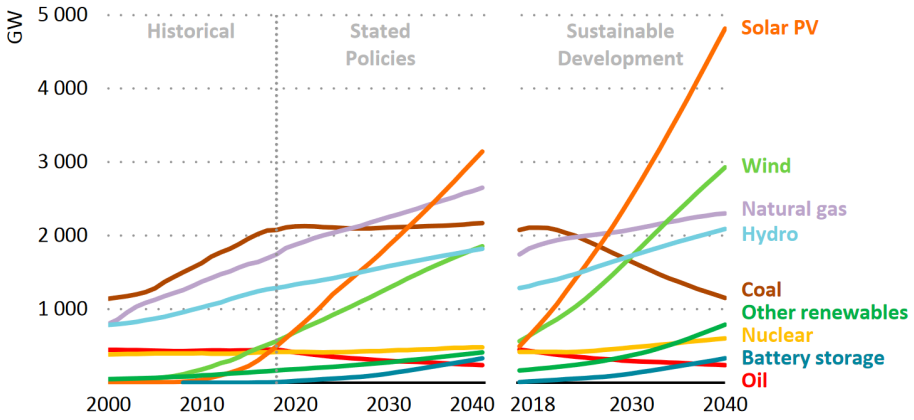

Figure 3: *Global yearly installed power generation capacity by scenario [3].*

Challenges of renewable energy sources in electric power systems

Traditional power systems were originally conceived and progressively developed based on some hypotheses. For example, it was assumed that the electric power would always flow from the transmission to the distribution networks. Indeed, most of the power consumed in the distribution grids would be produced by the synchronous generators connected to the transmission network. Other than producing power, these generators constituted (and still do to date) the backbone of power system stability due to the controls implemented within them, such as frequency and voltage regulation.

The increasing penetration of RESs clashes with this paradigm because it invalidates some hypotheses at the heart of conventional power system planning and operation.[1] To bring the integration of clean energy sources to fruition, several barriers need to be overcome. Massive InteGRATion of power Electronic devices (MIGRATE), a project funded by the European Union in the framework of Horizon 2020 [4], identified them by taking a survey among network operators. Many of the problems identified stem from the fact that the growing deployment of RESs is causing the progressive phase-out of synchronous generators, which in turn has three main implications.

- First, ensuring the balance at all times between power supply and demand becomes more complex. Indeed, while the power production from conventional generators is reliable, that of RES-fuelled generators is typically non-programmable, volatile, and uncertain.
- Second, the decrease in stability services caused by the elimination of synchronous generators (and related controls) is not generally compensated by RES-fuelled power plants. Indeed, an important feature of RESs is that they are interfaced to the grid with power electronic converters, whose control scheme allows them to fulfil specific objectives. These converters are typically controlled to inject the highest possible amount of power (and, thus, maximise their revenues) regardless of grid operating conditions. Therefore, as the penetration of RESs increases, the management of frequency and voltage regulation becomes more challenging.
- Lastly, the phase-out of synchronous generators also implies a reduction in the power system inertia stored in their rotating masses. The

[1] What is stated hereafter does not pertain to hydroelectric power plants, which were part of electricity networks since the very beginning.

inertia, together with the machine and load damping, constitutes a valuable asset for frequency and load angle containment in the immediate aftermath of power mismatches [5]. This decrease, however, is not compensated by RES-fuelled generators because their converters result in a full or partial decoupling between the grid and the generators. Therefore, the presence of a rotating mass in RES-based plants, if any, does not contribute to the overall power system inertia.

To overcome these significant hurdles, several solutions need to be implemented. For instance, in line with the most recent grid codes, RES-based sources need to participate in power system stability services. To do so, their converter control scheme must be changed by including, among others, voltage and frequency regulation [6,7]. In addition, the successful operation of future electric power systems will also depend on other new actors, such as electric vehicles and energy storage systems. On the one hand, electric vehicles are challenging because their daily power consumption pattern is potentially different from that of conventional loads. Moreover, their increasing deployment might put the current distribution grid infrastructure to the test, causing overloads and congestions. On the other hand, they may offer additional stability services with the so-called V2G (vehicle to grid) functionality [8]. For what regards large-size energy storage systems, one of their most attractive features is the capability of coping with the volatility and uncertainty of RESs by either absorbing or injecting power [9].

In the context of electric power systems, non-programmable RESs can be divided into two categories, which are briefly discussed in the following sections: Distributed Energy Resources (DERs) and Concentrated Energy Resources (CERs) [10]. The former are typically associated with small power plants scattered at the distribution level, such as photovoltaic (PV) systems installed on household rooftops. On the contrary, the latter consist of usually remote plants of bigger size, including wind farms and large-scale PV systems, typically connected to the transmission level.

Distributed energy resources

Till several years ago, the share of DERs (also referred to as Distributed Generation (DG) plants) was so limited that they were not considered a threat to power system planning and operation. Specifically, Distribution System Operators (DSOs) managed them with the *Fit and Forget* approach [11]. Every time a connection request of a DG plant was issued, DSOs verified that, at any load condition, this connection would not cause problems to the grid, such as security limit violations of node voltages and cable

thermal ratings. If necessary, DSOs would resort to network reinforcement strategies (*"fit"*), whose costs were borne by the generation plant owners and, in the countries where RES are publicly subsidised, by the end-users. Once installed, the owners of DG plants controlled them to maximise the power injected in the grid (and, in turn, their revenues), regardless of network conditions. Then, as DG plants were of no use for grid control and protection purposes, DSOs would *"forget"* about them in a sense.

The currently increasing penetration of DERs is such that this approach is no longer practical because it would require massive, continuous, and expensive network reinforcement operations to increase the so-called hosting capacity.[2] Another issue is that, due to the growing presence of DG plants, the nature of the distribution system shifts in some periods from passive to active. Therefore, the assumption - based on which grids were conceived and developed - that the power flow in the network is always unidirectional does not hold any longer.

To deal with these problems, the concept of *Smart Grids* emerged in the recent years and gained increasing popularity [12]. These grids consist of an advanced network architecture that exploits an Information and Communication Technology (ICT) layer, which enables the communication among all the users connected to the system (e.g., consumers, producers, DSOs, electric vehicles, smart meters, and energy storage systems). In this new architecture, DG plants are envisaged to contribute to power system stability. Other than allowing the integration of DERs, the current transition from conventional to smart grids will ensure the development of an economically efficient, sustainable power system with limited losses and high levels of quality and security of supply.

Concentrated energy resources and the role of HVDC systems

As in the case of off-shore wind farms or concentrated solar power plants located in the desert, CERs are usually far away from the power system backbone. Thus, they require not only AC/DC converter stations, but also long transmission paths comprising overhead lines or underground cables to connect them to the main grid. In this context, high-voltage alternating current (HVAC) and high-voltage direct current (HVDC) systems rank among the most adopted solutions to integrate these sources.

On the one hand, HVAC systems may require only one conversion stage at the CER point of connection and transformers at both their ends. One of

[2]This term corresponds to the amount of DERs that a grid can accommodate while guaranteeing quality and reliability of supply.

the main drawbacks of this technology is that reactive power losses need to be periodically compensated, thereby resulting in additional costs that increase with the length of the system. In particular, these losses are higher in underground cables than in overhead lines. On the other hand, since HVDC systems resort to DC power transmission, reactive power losses are absent. In addition, HVDC lines are cheaper and have lower power losses than HVAC ones. However, contrary to its HVAC counterpart, this technology requires one AC/DC conversion stage at each end of the system, thus leading to extra cost. In the light of the above, the disadvantages of HVAC systems generally outweigh those of the HVDC ones as longer distances need to be covered. In particular, depending on location, project power and voltage, the breakeven point is typically $600 - 800\,\mathrm{km}$ and $50 - 100\,\mathrm{km}$ for systems employing overhead lines and cables, respectively [13].

For what concerns HVDC systems, the converter stations can implement several technologies, which mainly belong to two categories: line commutated converters (LCCs) (also referred to as current source converters (CSCs)) and voltage source converters (VSCs). The interested reader can refer to [14] for a thorough comparison of the two technologies in terms of operating principle, advantages and disadvantages, which is omitted here for the sake of brevity.

LCC-based technology began to emerge in the 1930s, culminating in the 1950s with the very first commercial HVDC project connecting the Swedish island Gotland to the mainland [13]. This project consisted of a $98\,\mathrm{km}$, $100\,\mathrm{kV}$ submarine cable used to transfer $20\,\mathrm{MW}$ through two DC/AC converter stations using mercury-arc valves. LCC-based systems employing mercury-arc valves dominated the HVDC market until the 1970s, when they started to be replaced by thyristors, which matured as a technology thanks to the advances in the field of semiconductor devices. Since the Gotland project, LCC-based systems witnessed steady development. A true testament to this trend is given by the Hami-Zhengzhou project in China, a thyristor-based HVDC system operating since 2014 at $\pm 800\,\mathrm{kV}$ and exchanging a rated power of $8000\,\mathrm{MW}$ through a $2210\,\mathrm{km}$ line [15].

Compared to LCC-based counterparts, HVDC systems using VSCs are relatively more recent because they were ushered by the gradual development of insulated gate bipolar transistors (IGBTs) in the 1990s. The first project employing this technology, which dates back to 1997, was built in Sweden and consisted of a $3\,\mathrm{MW}$, $\pm 10\,\mathrm{kV}$ HVDC system. Early projects adopted two-level VSCs, which however posed some limits in terms of maximum voltage and power rating incompatible with the increasing size of CERs to be integrated. Over the last decades, the need to attain the higher

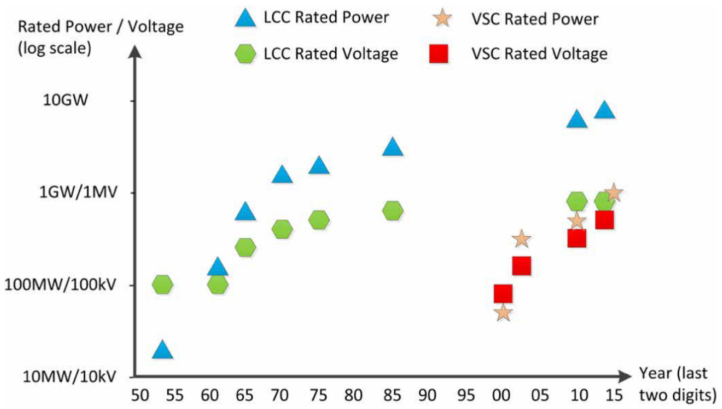

Figure 4: *Evolution of* LCC *and* VSC*-based* HVDC *systems in terms of voltage and power ratings from 1950 to 2015 [13].*

ratings shown in Fig. 4 spurred academia and industry to develop a new family of VSCs, known as *multilevel converters*. Some of the technologies that belong to this group, including the modular multilevel converter (MMC) (which is the main focus of this thesis), are described in the next chapter. The interested reader can refer to Appendix 4.1 of [16] for some examples of HVDC systems based on VSCs.

It is worth pointing out that, regardless of technology, HVDC systems are an ideal candidate also for other applications than just the integration of CERs. For instance, HVDC systems allow connecting asynchronous grids (i.e., networks operating at different nominal frequencies): this is the case of the Minami-Fukumitsu back-to-back HVDC system[3], which connects the eastern and western grid of Japan, operating respectively at 50 and $60\,\mathrm{Hz}$. Even if they operate at the same frequency, HVDC systems can also connect portions of the same AC grid or networks belonging to two different countries. This can be done for several purposes, such as network reinforcement and the provision of ancillary services through the exploitation of the LCCs or VSCs inside the converter stations [17].

Rationale of the PhD research

The previous sections highlighted that future electric power systems will comprise an increasing share of converter-interfaced elements, such as RESs,

[3] A *back-to-back* HVDC system connects two adjacent grids. In this case, the two converter stations are usually located in the same building and the HVDC link (if any) is short. On the contrary, if the HVDC system connects two distant power grids, it is referred to as *point-to-point*.

energy storage systems, electric vehicles, and HVDC systems. To successfully integrate these elements in the current network, power system simulation and analysis are essential.

Indeed, before their actual roll-out in real grids, all converter-interfaced elements (and their internal controls, too) should be tested and validated through simulations by considering a wide range of operating scenarios. The relevance of simulation is not limited to off-line analyses in the network planning phase but extends also to power system operation. For instance, grid operators could resort to real-time simulations to identify the most critical areas of their networks to increase their situational awareness and make informed decisions when contingencies occur, thereby significantly improving the quality and security of supply.

In addition, power system analysis techniques (such as small-signal analysis) may constitute a straightforward approach to detect possible instability issues in converter-dominated grids without resorting to extensive time-domain simulations. Over the last years, this latter aspect has become a hot topic. In fact, the growing presence of converter-interfaced elements is significantly changing power system dynamic behaviour, to the extent that the basic stability terms developed in the literature have been recently revised to consider the fast response of converters [18].

The main issue in this context is that, just as network operation and planning, power system simulation and analysis programs were conceived and further developed based on several assumptions and general practises which did not envisage the massive deployment of converter-interfaced elements. The dynamic phenomena analysed in power systems range from relatively slow electromechanical to fast electromagnetic transients. In conventional power systems, each phenomenon may be studied with different models and tools, aimed at attaining a suitable trade-off between simulation speed and accuracy. For instance, a common approach during the study of transient stability or long-term stability phenomena is to resort to single-phase equivalent models to accelerate the simulations [19]. However, this representation might not be sufficient to capture all the stability issues related to converter-connected elements. Indeed, these components generally require the adoption of electromagnetic transient (EMT) simulations and accurate three-phase models. This, however, has an impact on the overall simulation efficiency. In particular, if large power systems dominated by converters need to be analysed, the computational burden might become unbearable [20, 21].

Although the example above addresses only one issue concerning the analysis of modern power grids, it highlights that the current transition

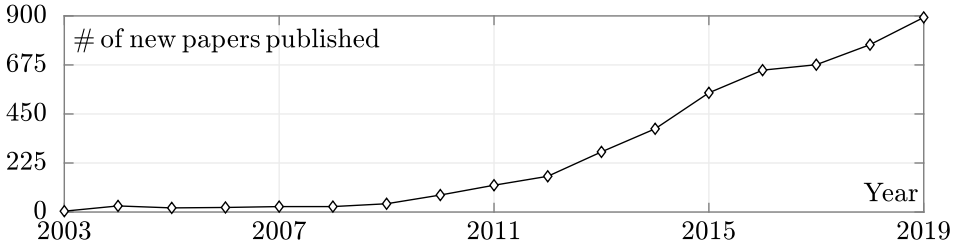

Figure 5: *Number of new scientific articles about* MMC*s published every year since 2003 (source: Scopus).*

in the electricity sector also demands the development of new modelling and simulation approaches suitable for converter-interfaced elements [22], which has been the main research topic of this PhD programme.

Despite being relatively new in the power system field, semiconductor devices inside the converters constitute the basic building blocks of electronics systems. Some of the challenges given by the growing presence of these components have already been addressed in this field by resorting to *ad hoc* innovative heuristics, unique methodologies, and computational techniques [23, 24]. The logical follow-up would be to extend these solutions to electric power systems. However, this is not an easy task, because it requires overcoming a certain reluctance from power system experts and scholars to update the established tools offered by conventional power system simulators, such as PSCAD, EMTP-RV, and DIGSILENT.

The solutions described above may vary based on the converter technology considered. Specifically, the research activity carried out and described in this thesis was aimed at developing circuit simulation and analysis techniques specifically tailored to grids with modular multilevel converters (MMCs). This technology was chosen because it has become a hot topic in the research community over the last few years. This statement is confirmed by Fig. 5, which depicts the number of new scientific articles that have been published on the topic of MMCs every year since 2003 (i.e., when a breakthrough in this field was made). These results have been obtained by querying the Scopus database and using the exact search string "modular multilevel converter" among paper keywords.

As better detailed in the following, the MMC has some key features that contributed to it becoming the technology of choice in VSC-based HVDC systems. However, compared to other VSCs, its simulation and analysis pose additional challenges to conventional power system simulators, some of which are discussed and tackled in the next chapters.

Thesis organization

The remaining chapters of this thesis are structured as follows.

After a brief overview of different multilevel converter technologies proposed in the last decades, Chapter 1 focuses on the modular multilevel converter (MMC) by describing its most relevant properties and a typical control architecture. In Appendix A, additional details are provided on how to modify the control scheme to make it compatible with unbalanced operating conditions. Then, the chapter summarises the main challenges posed by MMCs from a power system simulation and analysis perspective.

Chapter 2 presents the main models available in the literature to simulate MMCs. In addition, the MMC simulation approach based on sub-circuit isomorphism - one of the main aspects of the PhD research - is explained. This approach - originally conceived to analyse modular electronic circuits such as RAMs - can be profitably exploited to simulate MMCs, since it exploits the common behaviour of structurally identical SM by clustering them together. Each model and simulation method is described in terms of the degree of accuracy retained, computational burden incurred, and the most suitable types of analyses that it can carry out.

The isomorphism-based approach is validated in Chapter 3 by simulating an HVDC benchmark system comprising two MMCs in a wide array of scenarios, ranging from normal operating conditions to symmetrical and asymmetrical AC and DC-side faults. Each scenario aims at demonstrating a specific feature of the proposed approach.

In Chapter 4, the focus shifts on MMC small-signal analysis. To begin with, the most popular approaches to small-signal analysis in conventional power systems are introduced. Then, the chapter explains why these approaches are generally incompatible with grids comprising converters (MMCs included) and how they were modified in the literature to address this issue. In this thesis, the periodic small-signal analysis (PAC) is proposed as an alternative: despite being widely adopted for a long time by power electronics designers, this technique - which is implementable directly at the simulator level- still represents an uncharted territory in the power system realm. After a theoretical introduction, the chapter explains how to apply this method to MMCs. To showcase the potentialities of PAC, the same benchmark system considered in the previous chapter is exploited.

Lastly, the main results of this thesis, as well as possible further studies and research directions, are described in the Conclusion.

List of publications

The research activity carried out in the PhD programme and reported in this thesis originated in several conference and journal articles, listed hereafter in order of publication. These works are cited throughout the thesis to support some claims and constitute a source of additional information that could be useful to the interested reader.

- Davide del Giudice, Federico Bizzarri, Daniele Linaro, and Angelo Brambilla. Efficient Isomorphism Based Simulation of Modular Multilevel Converters. In *2019 IEEE Milan PowerTech*, pages 1–5, 2019
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Notation

In this thesis, the following notation is used:

- **Scalars** are denoted by plain italic letters (e.g., x or X).
- **Vectors** are denoted by lowercase, italic, boldface letters (e.g., $\boldsymbol{x}$).
- **Matrices** are denoted by uppercase, italic, boldface letters (e.g., $\boldsymbol{X}$).
- The $\mathrm{diag}(.)$ operator returns the main diagonal elements of a matrix as a vector.
- Depending on their argument, the $\mathrm{Re}(.)$ and $\mathrm{Im}(.)$ operators respectively denote the extraction of the real and imaginary parts of a scalar, vector, or matrix.

CHAPTER 1

Modular multilevel converters: key features, control strategies and main challenges

1.1 Converter technologies for high voltage and power applications

As stated in the Introduction, the increasing share of RESs in electric power systems (most notably, Concentrated Energy Resources) demands the adoption of DC/AC converters with high voltage and power ratings. In principle, this need could be circumvented by installing converters of smaller power ratings that operate in parallel. This solution, however, leads to extra cost and lower efficiency [31]. For this reason, academia and industry focused over the last decades on developing new converter technologies, which belong to the category of multilevel converters. Some of them - including the modular multilevel converter (MMC) - are summarised in this chapter. This short review describes only the three-phase technologies based on VSCs, which have rapidly taken hold also in more recent high-voltage direct current (HVDC) applications. Moreover, since this thesis focuses primarily on the MMC, the following review will not dwell on the details concerning the

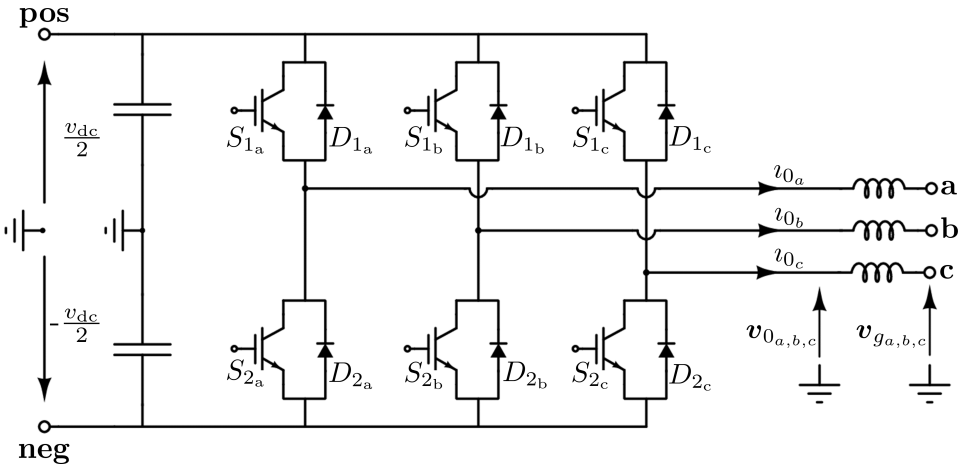


Figure 1.1: *The schematic of a two-level* VSC.

other converter topologies and their control strategies. Indeed, this summary is only meant to provide a logical path aimed at better showcasing the reasons for the increasing popularity of the MMC, its key features, as well as its main similarities and differences with respect to other well-known converter technologies developed in the past. The interested readers can refer to [16, 32–36] for more detailed information on every converter technology described hereafter, as well as other ones that were omitted for the sake of brevity.

1.1.1 Two-level voltage source converters

The two-level voltage source converter is one of the most frequently used VSCs. It is adopted in a wide array of applications with DC-side voltages up to $1800\,\mathrm{V}$, ranging from industrial drives, home appliances, to low-voltage grid-connected converters (such as those used to interface PV plants to the distribution grid).

The schematic in Fig. 1.1 depicts a two-level VSC for a three-phase application. Each leg comprises two semiconductor valves, which constitute the basic building block of this converter (and also of the MMC, as shown in the following). Each valve is typically implemented by a parallel connection of an IGBT and a free-wheeling diode. The mid-points of each leg constitute the AC-side terminals. They are connected to the rest of the grid by a filter, which comprises at least an inductor whose purpose is twofold: limiting current variations during commutations and filtering out high-order

Table 1.1: *Operating states of the two-level* VSC ($k \in \{a, b, c\}$)[1].

Case	S_{1_k}	S_{2_k}	$\imath_{0_k}$	v_{0_k}	$\imath_{0_k}$ flows through:
(a)	ON	OFF	> 0	$\frac{v_{\mathrm{dc}}}{2}$	S_{1_k}
(b)	ON	OFF	< 0	$\frac{v_{\mathrm{dc}}}{2}$	D_{1_k}
(c)	OFF	ON	> 0	$-\frac{v_{\mathrm{dc}}}{2}$	D_{2_k}
(d)	OFF	ON	< 0	$-\frac{v_{\mathrm{dc}}}{2}$	S_{2_k}

harmonics. In addition, a couple of capacitors, connected between each DC pole and ground, maintain the DC-side voltage fairly constant regardless of grid current.

Table 1.1 shows the different operating conditions of the two-level VSC that can be attained by properly regulating the gate signals of the IGBTs (for instance with a strategy based on pulse width modulation (PWM)). During commutations, such signals must comprise dead-times to prevent the creation (even for a short time) of a low-impedance path for the DC-side, which would lead to dangerously high currents. Note that when both gate signals are OFF (condition not reported in the table), the converter behaves as an uncontrolled diode bridge.

It is worth highlighting that the two-level VSC is a bidirectional converter, which means that it can operate as a rectifier (i.e., power flows from AC to DC side) or as an inverter (i.e., the opposite). As it will be explained in the specific case of the modular multilevel converter (MMC), a proper regulation of the AC-side voltage v_{0_k} (also referred to as *output* voltage) allows controlling, among others, active and reactive power flows.

In the case of the two-level VSC technology, as described in Table 1.1, the output AC-side voltage v_{0_k} can assume two values (or *levels*, hence the name of this converter): $\frac{v_{\mathrm{dc}}}{2}$ or $-\frac{v_{\mathrm{dc}}}{2}$. Since one valve at a time is conducting, the remaining one must block the whole DC-side voltage, which is the same value associated with the rate of change of voltage across the valves during a commutation. Through PWM techniques, v_{0_k} is swept between $\frac{v_{\mathrm{dc}}}{2}$ or $-\frac{v_{\mathrm{dc}}}{2}$ continuously, thereby leading to a sinusoidal function with a given harmonic content. As already stated, harmonics higher than the fundamental one are reduced by the AC filter.

Unless its configuration is altered, the current and voltage ratings of the valves (and, most notably, the blocking voltage capability) of this converter are incompatible with HVDC systems, whose pole-to-pole voltage and nominal power are typically in the order of hundreds of kV and MW.

[1]To be precise, the sixth column should be entitled "$\imath_{0_k}$ *mostly* flows through". Indeed, even if a valve is blocked, a fraction of current $\imath_{0_k}$, albeit very small, still flows through it.

To address this issue, the valves in each arm could be modified and comprise multiple semiconductors in series instead of only one. By doing so, the voltage rating of the converter increases because each device needs to block only a fraction of the overall DC-side voltage. If required, parallel connections could also be added to increase the converter current rating. Analogously, the equivalent capacitors on the DC-side could be given by a series connection of capacitors of smaller voltage rating.

For instance, the approach above was used to build the converter stations at the ends of the BorWin1 and Caprivi links. The former is a $200\,\mathrm{km}$, $\pm 150\,\mathrm{kV}$, $400\,\mathrm{MW}$ bipolar HVDC system which began operating in 2009 - the first of its kind to be used for connecting an off-shore wind farm (located in the North Sea and belonging to the German grid) to the mainland [16]. On the contrary, the latter is a $950\,\mathrm{km}$, $350\,\mathrm{kV}$, $300\,\mathrm{MW}$ monopolar HVDC link connecting since 2010 the Namibian and Zambian networks [37].

Although this approach has been exploited in some applications, it is not widely adopted worldwide due to some shortcomings. To begin with, the presence of additional semiconductor devices reduces the converter efficiency and reliability, since semiconductor losses and the chances of having a faulty component increase. In addition, these devices allow improving only the voltage and current converter ratings, but not the quality of the output voltage and current waveforms. Indeed, regardless of the number of additional components, the output voltage v_{0_k} can still assume only the two previously mentioned values (i.e., $\pm\frac{v_{dc}}{2}$). Lastly, the static and dynamic features of the series-connected devices and gate signals are not exactly the same, thereby leading to voltage mismatches. These differences need to be corrected by adopting voltage equalization techniques, which, however, lead to a more complex converter design [33].

In the light of these problems, academia and industry focused their efforts on developing a new family of converters, namely the multilevel converters, which are better suited for high voltage and power applications, and still allow bidirectional operation. In the following, some of the technologies that belong to this group are described.[2] These converters grant more output voltage levels, lower voltage harmonic distortion and voltage stresses, as well as reduced filter requirements.

1.1.2 Diode clamped converters

The first example of multilevel converter technology is the diode clamped converter. The schematic in Fig. 1.2 depicts the three-level version of this

[2]For all the multilevel converters described hereafter, the AC-side voltage v_{0_k} will still be referred to as *output* voltage.

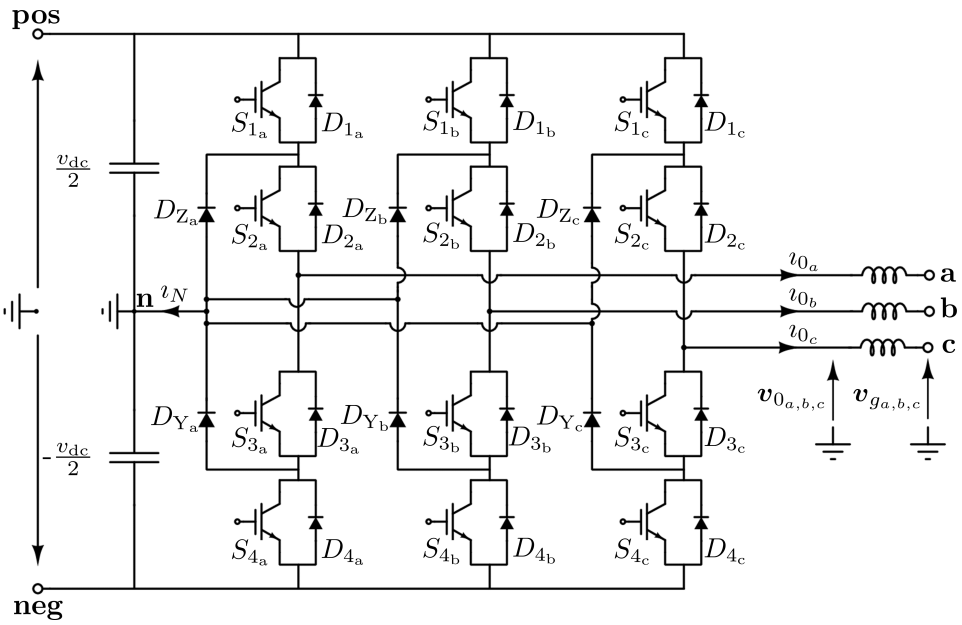


Figure 1.2: *The schematic of a three-level diode clamped converter.*

converter. The phase legs connect each DC and AC-side terminal through two couples of valves. In turn, between each couple of valves there is a path to the so-called clamping diodes (i.e., D_{Z_k} and D_{Y_k}, with k denoting a given phase leg), which are connected to the neutral node **n** that corresponds to the midpoint of the DC link. For this reason, this version is also referred to as neutral-clamped converter.

Table 1.2 summarises the operating states of this converter. Regardless of grid current direction, the output voltage amounts to $\frac{v_{dc}}{2}$ and $-\frac{v_{dc}}{2}$ when only the upper and lower couple of switches are ON, respectively. On the contrary, when only the middle couple of switches (i.e., S_{2_k} and S_{3_k}) is ON, one of the clamping diodes conduct (depending on the sign of i_{0_k}) and the resulting output voltage is null.

To sum up, in this case v_{0_k} can assume three different values. Thus, compared to the two-level VSC, this converter technology grants an improved output voltage waveform quality. In addition, it is characterised by lower switching stresses and a higher voltage rating. To validate this statement, consider for instance case (a) of Table 1.2 and the phase a of the converter in Fig. 1.2. Since both S_{3_a} and S_{4_a} are OFF, both of them need to block a voltage equal to $\frac{v_{\rm dc}}{2}$, so that the overall pole-to-pole voltage is sustained. Analogously, the same voltage (i.e., $\frac{v_{\rm dc}}{2}$) is blocked by any OFF switch in

Table 1.2: *Operating states of the three-level diode clamped* VSC ($k \in \{a, b, c\}$).

Case	S_{1_k}	S_{2_k}	S_{3_k}	S_{4_k}	$\imath_{0_k}$	v_{0_k}	$\imath_{0_k}$ flows through:
(a)	ON	ON	OFF	OFF	> 0	$\frac{v_{\mathrm{dc}}}{2}$	S_{1_k}, S_{2_k}
(b)	ON	ON	OFF	OFF	< 0	$\frac{v_{\mathrm{dc}}}{2}$	D_{1_k}, D_{2_k}
(c)	OFF	OFF	ON	ON	> 0	$-\frac{v_{\mathrm{dc}}}{2}$	D_{3_k}, D_{4_k}
(d)	OFF	OFF	ON	ON	< 0	$-\frac{v_{\mathrm{dc}}}{2}$	S_{3_k}, S_{4_k}
(e)	OFF	ON	ON	OFF	> 0	0	S_{2_k}, D_{Z_k}
(f)	OFF	ON	ON	OFF	< 0	0	S_{3_k}, D_{Y_k}

all the operating states of this converter.[3] Therefore, the voltage rating of the neutral-clamped converter technology is twice that of two-level VSC (whose OFF valves block the whole pole-to-pole voltage v_{dc}).

Figure 1.3 shows the single-phase schematic of a four-level version of this technology.[4] In practical implementations, the number of levels can rise only to a limited extent because the increasingly intricate interconnections of the clamping diodes lead to a complex converter design. Thus, in HVDC applications, the series connection of semiconductor devices is still needed to withstand high voltages.

There are also other shortcomings. The following description refers to the three-level version, but analogous conclusions hold for higher levels. First, the voltage across the two capacitors on the DC-side may differ due to even slight differences in the parameters of the upper and lower valves or due to the neutral current $\imath_N$ flowing through one capacitor during cases (c) and (d). This causes deviations in the neutral-point voltage, which in turn leads to increased voltage stresses on the valves and higher harmonic distortions in the output voltage. To mitigate this issue, *ad hoc* switching strategies need to be adopted. Second, losses in the converter are unevenly distributed, as in some operating conditions the outer and inner valves mostly incur switching and conduction losses, respectively [32].

This converter technology was used in the Eagle Pass project, a $\pm 18\,\mathrm{kV}$, $36\,\mathrm{MW}$ HVDC back-to-back system located in the American-Mexican border [38].

[3] This value also coincides with the voltage change across a given valve during a single commutation.

[4] The topology of the phase legs b and c is the same but it is not reported here because it would lead to an excessively intricate schematic which adds nothing to the description of the converter technology. For the sake of simplicity, the same approach is adopted in the other multilevel VSC schematics in Figs. 1.4 - 1.6.

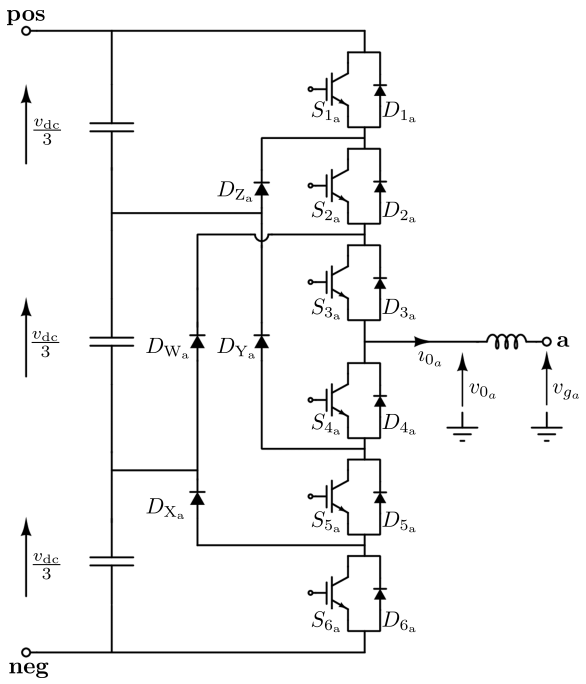


Figure 1.3: *The single-phase schematic of four-level diode clamped converter.*

1.1.3 Active neutral point clamped converters

To better distribute conduction and switching losses in the valves, the active neutral point clamped converter has been proposed [39,40]. Figure 1.4 shows the single-phase schematic of its three-level version: in this case, valves analogous to those used in the original neutral clamped converter replace the clamping diodes. Table 1.3 describes the possible operating states of this converter, while Fig. 1.5 highlights the path taken by the current i_{0_k} in each state.[5]

By comparing Table 1.2 and 1.3, the following remarks can be made. First, in the cases where v_{0_k} amounts to $\frac{v_{\rm dc}}{2}$ ($-\frac{v_{\rm dc}}{2}$), the switch S_{6_k} (S_{5_k}) must be ON to ensure that S_{3_k} and S_{4_k} (S_{1_k} and S_{2_k}) block the same voltage. Second, when adopting the active neutral clamped converter, more cases can be exploited to achieve $v_{0_k} = 0$. For instance, when S_{2_k} and S_{5_k} are ON, the current flows in upper-mid circuit (cases (c) and (d)).

[5]For the sake of simplicity, only the cases where $i_{0_k} > 0$ have been reported. Anyhow, for each of the cases shown, when $i_{0_k} < 0$, the semiconductors flown by current are complementary to those that conduct when i_{0_k} is positive. For instance, in case (a) the current $i_{0_k} < 0$ flows through the diodes D_{1_k} and D_{2_k}, while the same negative current in case (c) flows through D_{2_k} and S_{5_k}.

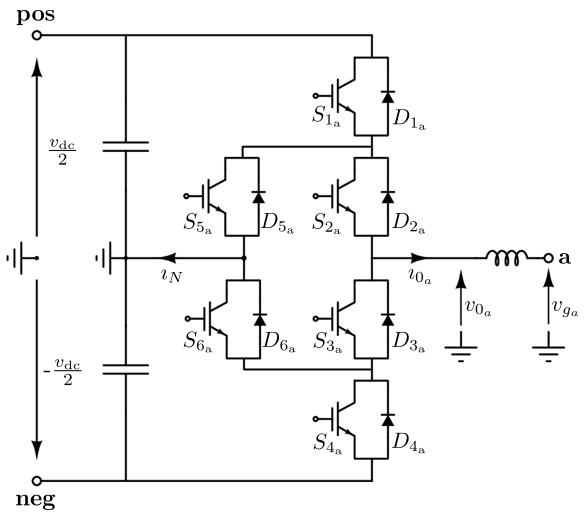


Figure 1.4: *The single-phase schematic of three-level active neutral clamped converter.*

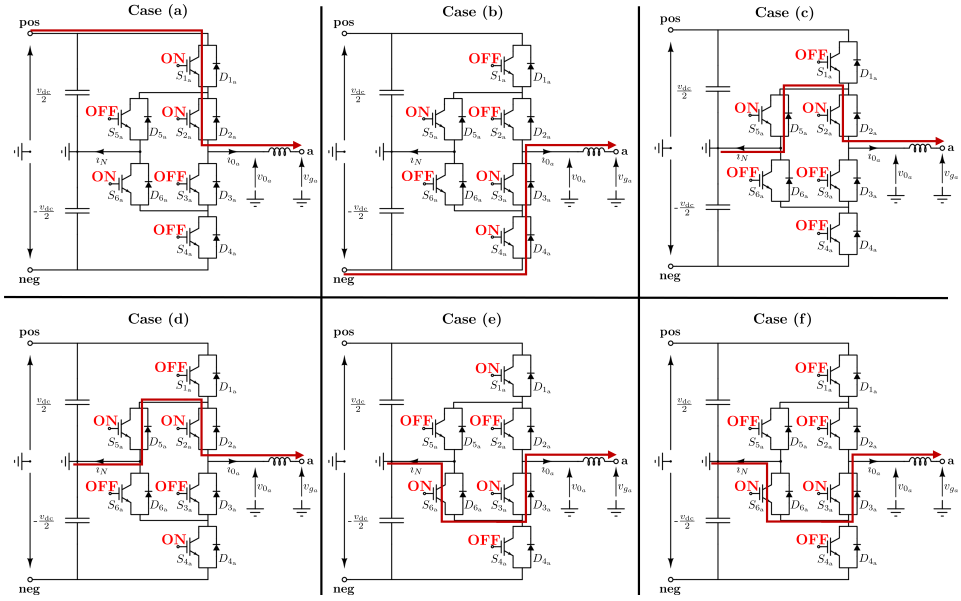


Figure 1.5: *The path taken by the current $\imath_{0_k}$ in each of the cases shown in Table 1.3.*

Table 1.3: *Operating states of the active neutral point clamped* VSC ($k \in \{a, b, c\}$).

Case	S_{1_k}	S_{2_k}	S_{3_k}	S_{4_k}	S_{5_k}	S_{6_k}	$\imath_{0_k}$	v_{0_k}	$\imath_{0_k}$ flows through:
(a)	ON	ON	OFF	OFF	OFF	ON	> 0	$\frac{v_{\mathrm{dc}}}{2}$	S_{1_k}, S_{2_k}
(b)	OFF	OFF	ON	ON	ON	OFF	> 0	$-\frac{v_{\mathrm{dc}}}{2}$	D_{3_k}, D_{4_k}
(c)	OFF	ON	OFF	OFF	ON	OFF	> 0	0	S_{2_k}, D_{5_k}
(d)	OFF	ON	OFF	ON	ON	OFF	> 0	0	S_{2_k}, D_{5_k}
(e)	ON	OFF	ON	OFF	OFF	ON	> 0	0	D_{3_k}, S_{6_k}
(f)	OFF	OFF	ON	OFF	OFF	ON	> 0	0	D_{3_k}, S_{6_k}

To clarify the usefulness of these two cases - which may seem redundant at first glance - consider the following example. Suppose that the converter is operating as in case (b) and that, following a given change, it should move to a working condition where $v_{0_k} = 0$. If case (c) is selected, the S_{4_k} device is subject to switching losses. On the contrary, if case (d) is selected, the same device remains ON and is subject to conduction losses. As a result, this example highlights that the presence of multiple scenarios where $v_{0_k} = 0$ paves to way to more control techniques aimed at distributing the switching and conduction losses of each semiconductor device.

This technology was adopted in the converter stations of the Murray Link [41], a $180\,\mathrm{km}$, $\pm 150\,\mathrm{kV}$, $400\,\mathrm{MW}$ bipolar HVDC system providing an additional connection between the electricity networks of South Australia and Victoria since 2002. In the same year, the same technology was used to implement the Cross-Sound Cable Project, a $40\,\mathrm{km}$, $\pm 150\,\mathrm{kV}$, $330\,\mathrm{MW}$ bipolar HVDC link between New York and New England [42].

1.1.4 Flying capacitor converters

The structure of a three-level flying capacitor converter, whose single-phase schematic is shown in Fig. 1.6(a), is similar to that of the diode clamped converter. The main difference is that a capacitor (referred to as *flying* or *floating* capacitor due to the lack of a direct connection to a common DC-link) replaces the clamping diodes. Each floating capacitor operates around a given voltage, which depends on the number of converter levels.

Table 1.4 lists the operating states of this converter technology. In each operating state, one of the valves must withstand a voltage equal to $\frac{v_{\mathrm{dc}}}{2}$. Thus, the flying capacitor and neutral clamped converter share the same voltage rating requirements. However, in comparison with Table 1.2, this technology comprises more redundant states yielding $v_{0_k} = 0$, all of which involve either the charge or discharge of the floating capacitors. Contrary to the diode-clamped converter, in the flying capacitor converter an adequate

gate signal control strategy allows an even distribution of conduction and switching losses among all valves. For instance, if the output current is positive, the converter can transition from case (a) to either (e) or (g) to obtain $v_{0_k} = 0$. In the former case, S_{1_k} and S_{2_k} will undergo respectively switching and conduction losses. The opposite holds in the latter case. In addition, in this converter technology the DC-side neutral point is not involved in any of the operating states. Thus, contrary to diode clamped converters, neutral point voltage deviations are not an issue.

It is also worth pointing out that the flying capacitor converter has some shortcomings. For example, a charging sequence might be necessary to ensure that the floating capacitors start operating at a given voltage (e.g., $\frac{v_{\mathrm{dc}}}{2}$ in the case of Fig. 1.6(a)). To prevent large inrush currents from damaging the converter, start-up resistors should be inserted at the beginning of converter operation and then shorted once the charging sequence is complete. Another important control requirement - common, as shown in the following, to the modular multilevel converter - pertains to the floating capacitor voltage. During operation, such voltage must not deviate excessively from its per cycle average value (defined in the design stage) to avoid higher voltage stresses on the valves and a more distorted output voltage. To this aim, the sequences (e)-(h) can be exploited to alternate between moments of charge and discharge in the capacitors. Lastly, floating capacitors inevitably exhibit voltage ripples, which affect the quality of the output voltage waveform. Large size capacitors or high switching frequencies can be adopted to limit them: the first solution increases the converter station costs and its footprint, whereas the second leads to higher switching losses.

Figure 1.6(b) shows the single-phase schematic of a four-level version of this technology. The presence of two floating capacitors, which operate around a different voltage, allows implementing an additional output voltage level. However, as for the diode clamped converter technology, also in this case the number of levels can rise only to a limited extent due to an increasingly complex converter design.

1.1.5 Cascaded H-bridge converters

True to their name, cascaded H-bridge converters comprise three phase legs, each of which consists of a cascading connection of N H-bridge modules. Figure 1.7(a) and (b) respectively depict the schematic of the converter and a single H-bridge module (also known as full-bridge cell). Every module comprises four valves, each made up of an IGBT and a free-wheeling diode. The left port of each module is connected to external and separate

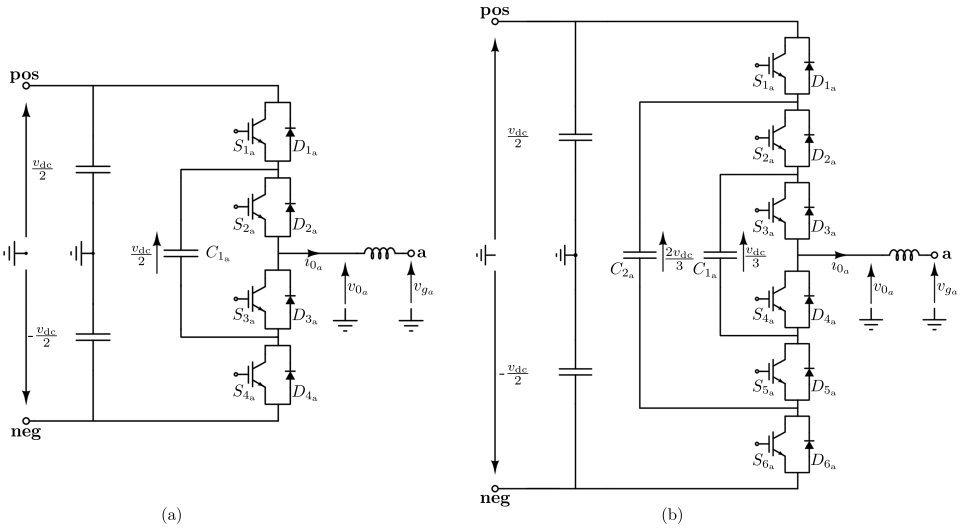


Figure 1.6: *The single-phase schematic of (a) three-level and (b) four-level flying capacitor converter.*

Table 1.4: *Operating states of the three-level flying capacitor* VSC ($k \in \{a, b, c\}$).

Case	S_{1_k}	S_{2_k}	S_{3_k}	S_{4_k}	$\imath_{0_k}$	v_{0_k}	$\imath_{0_k}$ flows through:
(a)	ON	ON	OFF	OFF	> 0	$\frac{v_{\mathrm{dc}}}{2}$	S_{1_k}, S_{2_k} (C_{1_k} bypassed)
(b)	ON	ON	OFF	OFF	< 0	$\frac{v_{\mathrm{dc}}}{2}$	D_{1_k}, D_{2_k} (C_{1_k} bypassed)
(c)	OFF	OFF	ON	ON	> 0	$-\frac{v_{\mathrm{dc}}}{2}$	D_{3_k}, D_{4_k} (C_{1_k} bypassed)
(d)	OFF	OFF	ON	ON	< 0	$-\frac{v_{\mathrm{dc}}}{2}$	S_{3_k}, S_{4_k} (C_{1_k} bypassed)
(e)	OFF	ON	OFF	ON	> 0	0	S_{2_k}, D_{4_k} (C_{1_k} discharging)
(f)	OFF	ON	OFF	ON	< 0	0	D_{2_k}, S_{4_k} (C_{1_k} charging)
(g)	ON	OFF	ON	OFF	> 0	0	S_{1_k}, D_{3_k} (C_{1_k} charging)
(h)	ON	OFF	ON	OFF	< 0	0	D_{1_k}, S_{3_k} (C_{1_k} discharging)

DC sources, which could be given by PV plants or battery energy storage systems. Therefore, this converter technology is an excellent candidate for integrating these elements in high-voltage grids [43, 44]. On the contrary, in motor drives-related applications, the DC sources can be obtained using phase-shifting transformers and multi-pulse diode rectifiers [45, 46]. This solution, however, is expensive and increases the converter footprint.

Based on the operating states listed in Table 1.5, every H-bridge module can synthesize three values of voltage u_{out_k}: positive, negative or null. In addition, the cascaded H-bridge converter can operate in either symmetrical or asymmetrical configuration. In the former case, the DC-side voltage

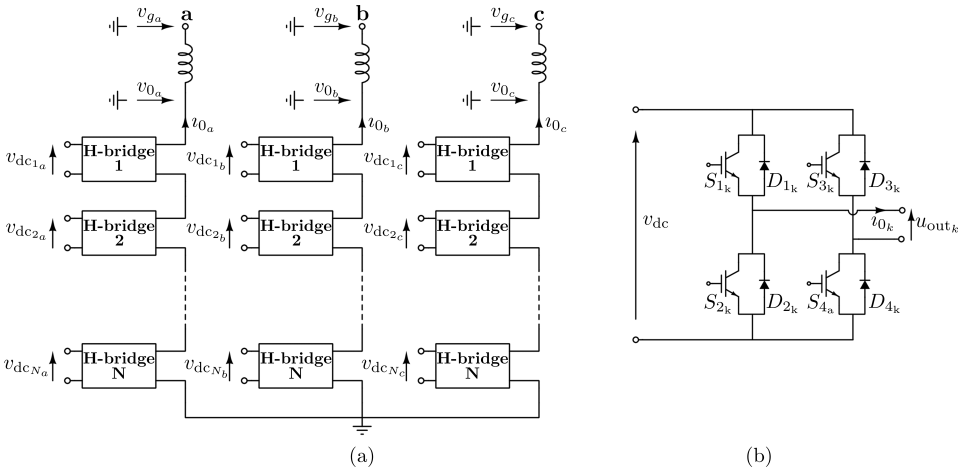


Figure 1.7: *The schematic of (a) cascaded H-bridge converter and (b) H-bridge module of a generic phase k* ($k \in \{a, b, c\}$).

Table 1.5: *Operating states of the H-bridge module in Fig. 1.7(b)* ($k \in \{a, b, c\}$).

Case	S_{1_k}	S_{2_k}	S_{3_k}	S_{4_k}	$\imath_{0_k}$	u_{0_k}	$\imath_{0_k}$ flows through:
(a)	ON	OFF	OFF	ON	> 0	$v_{\rm dc}$	S_{1_k}, S_{4_k}
(b)	ON	OFF	OFF	ON	< 0	$v_{\rm dc}$	D_{1_k}, D_{4_k}
(c)	OFF	ON	ON	OFF	> 0	$-v_{\rm dc}$	D_{2_k}, D_{3_k}
(d)	OFF	ON	ON	OFF	< 0	$-v_{\rm dc}$	S_{2_k}, S_{3_k}
(e)	ON	OFF	ON	OFF	> 0	0	S_{1_k}, D_{3_k}
(f)	ON	OFF	ON	OFF	< 0	0	D_{1_k}, S_{3_k}
(g)	OFF	ON	OFF	ON	> 0	0	D_{2_k}, S_{4_k}
(h)	OFF	ON	OFF	ON	< 0	0	S_{2_k}, D_{4_k}

across each module is the same (e.g., $v_{\rm dc}$). For instance, consider Table 1.6(a), which reports the values assumed by v_{0_k} when $N = 2$ and a symmetrical configuration is adopted. In this case, the number of levels of the output voltage v_{0_k} is equal to $2 \cdot N + 1 = 2 \cdot 2 + 1 = 5$. By increasing N it is possible to obtain a high-quality output voltage waveform with minimum filter requirements. Moreover, if the sum of DC-side voltages across the modules of each leg remains fixed, the voltage rating (as well as the voltage stress) of the valves decreases with the number of modules. As a result, the converter can operate at high voltage and power through the adoption of low-cost, low-voltage IGBT technology. This is in sharp contrast with the previously mentioned converter technologies, which need to resort to series-connected semiconductor devices to withstand high volt-

Table 1.6: *Operating states of the H-bridge converter in symmetrical (a) and asymmetrical (b) configuration ($N = 2$) ($k \in \{a, b, c\}$).*

(a)

Case	$u_{\mathrm{out}_{k_1}}$	$u_{\mathrm{out}_{k_2}}$	v_{0_k}
(a)	$-v_{\mathrm{dc}}$	$-v_{\mathrm{dc}}$	$-2v_{\mathrm{dc}}$
(b)	$-v_{\mathrm{dc}}$	0	$-v_{\mathrm{dc}}$
(c)	0	$-v_{\mathrm{dc}}$	$-v_{\mathrm{dc}}$
(d)	0	0	0
(e)	v_{dc}	$-v_{\mathrm{dc}}$	0
(f)	$-v_{\mathrm{dc}}$	v_{dc}	0
(g)	v_{dc}	0	v_{dc}
(h)	0	v_{dc}	v_{dc}
(i)	v_{dc}	v_{dc}	$2v_{\mathrm{dc}}$

(b)

Case	$u_{\mathrm{out}_{k_1}}$	$u_{\mathrm{out}_{k_2}}$	v_{0_k}
(a)	$-v_{\mathrm{dc}}$	$-2v_{\mathrm{dc}}$	$-3v_{\mathrm{dc}}$
(b)	0	$-2v_{\mathrm{dc}}$	$-2v_{\mathrm{dc}}$
(c)	$-v_{\mathrm{dc}}$	0	$-v_{\mathrm{dc}}$
(d)	v_{dc}	$-2v_{\mathrm{dc}}$	$-v_{\mathrm{dc}}$
(e)	0	0	0
(f)	v_{dc}	0	v_{dc}
(g)	$-v_{\mathrm{dc}}$	$2v_{\mathrm{dc}}$	v_{dc}
(h)	0	$2v_{\mathrm{dc}}$	$2v_{\mathrm{dc}}$
(i)	v_{dc}	$2v_{\mathrm{dc}}$	$3v_{\mathrm{dc}}$

ages. Other than being cost-effective and easy to implement, the modular structure of this converter enables fault-tolerant operation by adding redundant modules: if a module is damaged, it can be bypassed and another one in the same leg, which was previously idle, can be activated.

On the contrary, in the case of asymmetrical configuration, the DC-side voltage in each module can be a multiple of another. For instance, Table 1.6(b) describes the operating states obtained when $N = 2$ and the DC-side voltage of one module is twice the other. As the table shows, the asymmetrical configuration leads to more output voltage levels and, thus, a higher power quality. However, this implies that each module may have a different voltage rating and that the redundancy in the operating states reduces (and, with it, the flexibility for switching pattern design).

1.2 Modular multilevel converter

1.2.1 Topology, key features, fields of application

The modular multilevel converter (MMC), whose schematic is shown in Fig. 1.8, was first proposed in [47, 48]. In a three-phase configuration, the converter comprises three legs and a filter (R_T,L_T) used to reduce the harmonic distortion in the output voltage. In turn, every leg includes an upper and lower arm, each consisting of a string of up to several hundreds of series-connected identical SMs and a filter (R_S,L_S). This filter does not only smooth current variations during switching of SM capacitors and DC-side faults, but also limits - as shown later - circulating currents.

The SMs can implement different topologies. Among others, the works

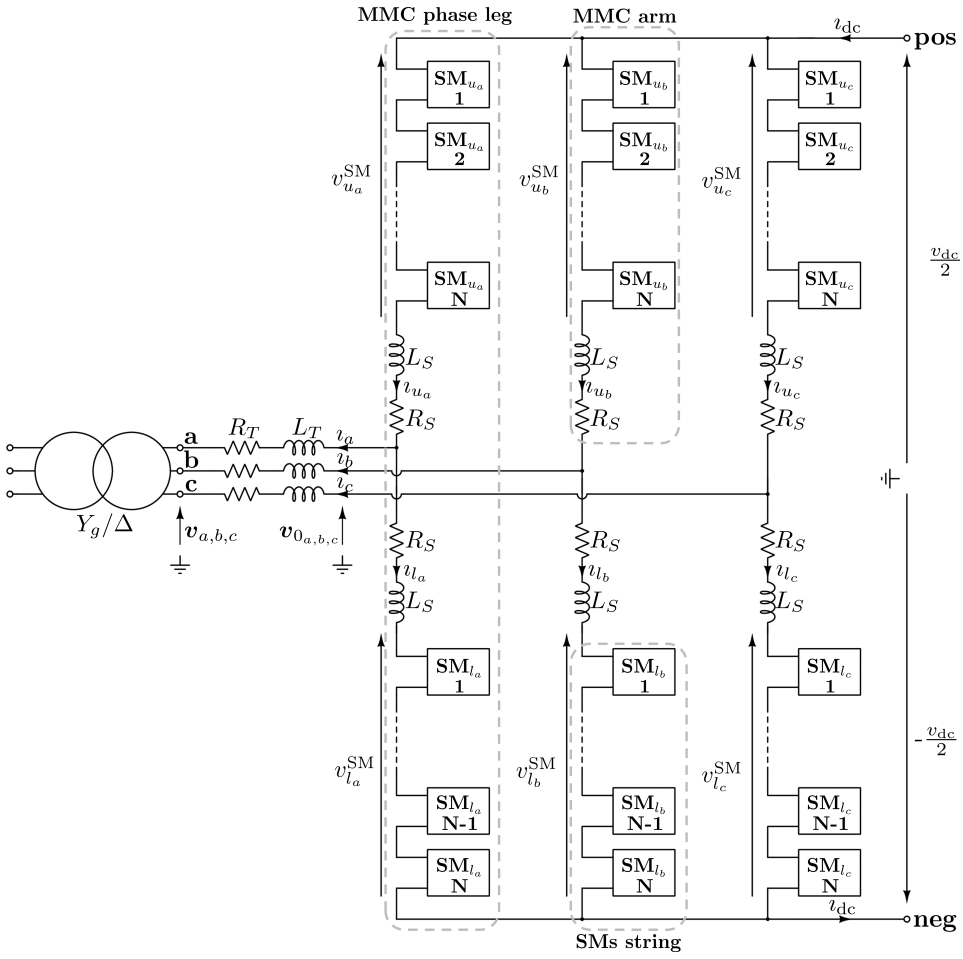


Figure 1.8: *The schematic of an* MMC *comprising a generic number* N *of* SM*s per arm.*

in [49, 50] present several ones developed over the years, some of which are based on the multilevel converters reviewed in the previous section. This chapter describes the most common ones, namely the half-bridge and full-bridge SMs. Specifically, for reasons explained in the following, this thesis focuses primarily on the former topology. In any case, contrary to the cascaded H-bridge converter, none of the SMs is connected to an external DC source. Indeed, depending on the topology chosen, each SM comprises at least one local capacitor, whose voltage is exploited to synthesize the output voltage waveform.

Consider for instance the case of the half-bridge submodule, shown in Fig. 1.9(a). It comprises the following operating conditions, listed also in

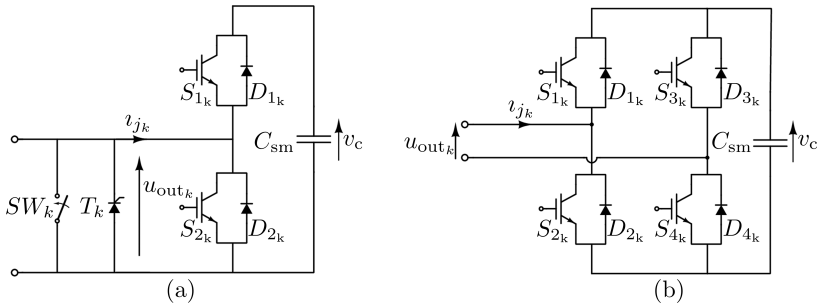


Figure 1.9: *The schematic of the half-bridge (a) and full-bridge (b) submodules. In the right figure, the bypass switch and thyristors were not included for simplicity.*

Table 1.7:

- **Inserted SM (cases (a) and (b))**: when only S_{1_k} is switched on, the SM impresses at its pins the capacitor voltage and is either charged or discharged based on the sign of the arm current (e.g., i_{u_a}). Thus, the capacitor $C_{\rm sm}$ is effectively inserted into its corresponding MMC arm.

- **Bypassed SM (cases (c) and (d))**: the voltage at the SM terminals is basically null, regardless of arm current. Since in this case only S_{2_k} is ON, most of the arm current circulates through the lower valve: only a negligible current flows through $C_{\rm sm}$, which is therefore bypassed.

- **Blocked SM (cases (e) and (f))**: attained by switching off both S_{1_k} and S_{2_k}. In this working condition, the voltage $u_{{\rm out}_k}$ depends on the current direction because the SM behaves as an uncontrolled diode bridge. This configuration is such that the capacitor $C_{\rm sm}$ can only charge (case (e)) but not discharge. Indeed, in case (f), when the SM current is negative, the capacitor is bypassed. The SM enters this operating mode either during converter start-up or when faults occur.

  In the first scenario, case (e) is exploited to charge, if needed, the SM capacitors up to their rated value at the beginning of MMC operation. As with flying capacitor converters, a start-up resistor is often added to limit inrush currents when the start-up sequence begins and then shorted to minimise losses once the standard system operation starts.

  In the second scenario, the blocked condition in case (f) prevents the discharge of SM capacitors during DC-side faults, which would otherwise further aggravate fault currents. In this scenario, the presence of the thyristor T has a beneficial effect. Indeed, in case of a DC-side

fault, the thyristor can receive a firing signal from the MMC control scheme. This is done because, compared to the free-wheeling diodes inside the valves, the thyristors can withstand the higher surge current observed during DC-side faults. As a result, most of this current would flow through the thyristors, thereby protecting the free-wheeling diodes.

It is worth pointing out that this SM topology is incapable of limiting DC fault currents. Indeed, after blocking the SMs, the DC-side fault must be managed either by opening *ad hoc* DC breakers or those at the AC-side of the converter (and then isolating the fault using off-load isolators in the DC grid). Since the former solution is still at an early stage of development, the second option is typically adopted (besides, alternating current is easier to interrupt due to the presence of zero-crossing points). This aspect is troublesome if DC faults occur in multi-terminal direct current (MTDC) systems. Indeed, the remaining part of the DC grid must be able to cope momentarily with one converter being out of service after its AC-breakers have been opened.

- **SM failure (not listed in the table)**: it arises when both its IGBTs are mistakenly ON or a fault within the SM occurs. In this case, the normally open bypass switch SW grants the MMC high reliability and fail-safe functionality - a feature common to the cascaded H-bridge converter. When the MMC control scheme detects a damaged SM, its bypass switch closes, thus shorting the faulty SM. At the same time, a redundant SM, which was idle until then, is connected to the SMs string by opening its switch, thereby replacing the faulty one. By doing so, standard MMC operation quickly resumes without needing to put the converter out of service.

To explain how the output voltage level is synthesized during the normal operation of MMCs, consider the set of equations in Eq. (1.1), which relate the output voltage v_{0_k} and current $\imath_k$ with the variables on the DC-side ($k \in \{a, b, c\}$).

$$\begin{aligned} v_{0_k} &= -R_S\, \imath_{u_k} - L_S \frac{d\imath_{u_k}}{dt} - v_{u_k}^{\mathrm{SM}} + \frac{v_{\mathrm{dc}}}{2} \\ v_{0_k} &= R_S\, \imath_{l_k} + L_S \frac{d\imath_{l_k}}{dt} + v_{l_k}^{\mathrm{SM}} - \frac{v_{\mathrm{dc}}}{2} \\ \imath_k &= \imath_{u_k} - \imath_{l_k} \end{aligned} \tag{1.1}$$

[6] If both S_{1_k} and S_{2_k} are OFF and the hyphotheses in the rows of case (e) and (f) are not respected, none of the diode conducts.

Table 1.7: *Operating states of the half-bridge submodule.*[6]

Case	S_{1_k}	S_{2_k}	$\imath_k$	u_{out_k}	$\imath_k$ flows through:
(a)	ON	OFF	> 0	v_c	D_{1_k} (C_{sm} is charging)
(b)	ON	OFF	< 0	v_c	S_{1_k} (C_{sm} is discharging)
(c)	OFF	ON	> 0	0	S_{2_k} (C_{sm} is bypassed)
(d)	OFF	ON	< 0	0	D_{2_k} (C_{sm} is bypassed)
(e)	OFF	OFF	> 0	v_c	D_{1_k} (C_{sm} is charging) (hp: $u_{\mathrm{out}_k} > v_c$)
(f)	OFF	OFF	< 0	0	D_{2_k} (C_{sm} is bypassed) (hp: $u_{\mathrm{out}_k} < 0$)

A proper rearrangement of the equations above allows recasting v_{0_k} as

$$v_{0_k} = \underbrace{\frac{1}{2}\left(v_{l_k}^{\mathrm{SM}} - v_{u_k}^{\mathrm{SM}}\right)}_{u_k} - \frac{1}{2}R_S\,\imath_k - \frac{1}{2}L_S\,\frac{d\imath_k}{dt}\,, \tag{1.2}$$

where u_k, as described later in Section 1.3.3, is a variable regulated by the MMC control scheme. By neglecting momentarily the voltage drop across the resistor R_S and inductor L_S, the following holds. Assume for simplicity that the voltage across each capacitor is constant[7] and equal to $v_{\mathrm{c}} = \frac{v_{\mathrm{dc}}}{2N}$, with N being the number of SMs in each arm.[8] If $N = 4$, the output voltage levels that can be obtained with the MMC through Eq. (1.2) are those shown in Table 1.8. These operating states - which correspond to given values of u_k - are cyclically repeated during operation, thereby leading to a stair-case waveform that aims at approximating a sinusoid. Note that, for each operating state, the number of inserted SMs in one phase leg is such that the overall voltage across them amounts to the pole-to-pole voltage v_{dc}. In other words, $v_{l_k}^{\mathrm{SM}} + v_{u_k}^{\mathrm{SM}} = v_{\mathrm{dc}}$[9]. If this condition were not met, R_S and L_S would withstand dangerously high voltages. As a result, the normal operation of MMC involves SMs moving from inserted to bypassed working condition and vice versa. As previously stated for other converter technologies, it is worth emphasising that, during the transition between these working modes, the gate signals of the IGBTs must comprise adequate dead times to prevent the creation of low-impedance paths involving the SM capacitors.

[7] This hypothesis will be removed when describing capacitor voltage balancing algorithms.

[8] Possible redundant SMs left idle by closing their bypass switch are not included in this count.

[9] As shown in the following, this property, which holds only if all SM capacitor voltages are perfectly balanced, is at the basis of the Average Value Model (AVM) of the MMC.

Table 1.8: *Example of operating states of the* MMC *when* $N = 4$ *and half-bridge* SM*s are adopted. Only a single-phase leg* k *is examined.*

Case	SMs inserted in the k-th upper arm	SMs inserted in the k-th lower arm	v_{0_k}
(a)	4	0	$-\frac{v_{\mathrm{dc}}}{2}$
(b)	3	1	$-\frac{v_{\mathrm{dc}}}{4}$
(c)	2	2	0
(d)	1	3	$\frac{v_{\mathrm{dc}}}{4}$
(e)	0	4	$\frac{v_{\mathrm{dc}}}{2}$

The example in Table 1.8 suggests that, when using half-bridge SMs, the MMC can generate $N + 1$ output voltage levels. Contrary to the diode clamped and flying capacitor converter technologies, the number of SMs in each arm can be easily extended, thus increasing the converter power quality to the point that v_{0_k} strongly resembles a sinusoidal wave. As a result, since filter requirements on the AC side are minimum, R_T and L_T could just be given by the leakage resistance and inductance of the transformer used to connect the MMC to the grid, without needing the installation of an *ad hoc* filter. In addition, since in typical applications each arm comprises up to several hundreds of identical SMs, their valves could be switched on and off with a low frequency (e.g., that of the AC grid) to minimise switching losses. Lastly, by increasing the number of levels, each valve incurs lower voltage stresses. Thus, as the cascaded H-bridge converter, the MMC is scalable to high voltage and power applications, although its SMs consist of low-cost, low-voltage rating semiconductor devices.[10]

Together with the fail-safe functionality, the abovementioned features have contributed to making the MMC a popular converter technology in many applications, ranging from medium-voltage motor drives, power quality improvement, off-shore wind farm integration, to HVDC and MTDC systems. Examples of HVDC systems based on the MMC technology include the Trans Bay Cable [51] and Inelfe [52] projects. The former is the first MMC-based HVDC system ever built: it began operating in 2010 and consists of an $85\,\mathrm{km}$, $200\,\mathrm{kV}$, $500\,\mathrm{MW}$ monopolar HVDC link providing additional power to the city of San Francisco. The latter project comprises two $65\,\mathrm{km}$, $320\,\mathrm{kV}$, $1000\,\mathrm{MW}$ monopolar HVDC links connecting France and Spain since 2015. The BorWin2 project - a $200\,\mathrm{km}$, $300\,\mathrm{kV}$, $800\,\mathrm{MW}$

[10] Since they are easily scalable to high voltages, MMCs may not necessarily be connected to the grid with the Y_g/Δ transformer shown in Fig. 1.8. For this reason, the next figures that depict the MMC omit this component. In Chapter 3.2, however, this transformer is still considered because of its usefulness for MMC control and protection purposes. This aspect is better detailed in Appendix A.

Table 1.9: *Operating states of the full-bridge submodule.*[11]

Case	S_{1_k}	S_{2_k}	S_{3_k}	S_{4_k}	$\imath_k$	u_{out_k}	$\imath_k$ flows through:
(a)	ON	OFF	OFF	ON	> 0	v_{c}	D_{1_k},D_{4_k} (C_{sm} is charging)
(b)	ON	OFF	OFF	ON	< 0	v_{c}	S_{1_k},S_{4_k} (C_{sm} is discharging)
(c)	OFF	ON	ON	OFF	> 0	$-v_{\mathrm{c}}$	S_{2_k},S_{3_k} (C_{sm} is discharging)
(d)	OFF	ON	ON	OFF	< 0	$-v_{\mathrm{c}}$	D_{2_k},D_{3_k} (C_{sm} is charging)
(e)	ON	OFF	ON	OFF	> 0	0	D_{1_k},S_{3_k} (C_{sm} is bypassed)
(f)	ON	OFF	ON	OFF	< 0	0	S_{1_k},D_{3_k} (C_{sm} is bypassed)
(g)	OFF	ON	OFF	ON	> 0	0	S_{2_k},D_{4_k} (C_{sm} is bypassed)
(h)	OFF	ON	OFF	ON	< 0	0	D_{2_k},S_{4_k} (C_{sm} is bypassed)
(i)	OFF	OFF	OFF	OFF	> 0	v_{c}	D_{1_k},D_{4_k} (C_{sm} is charging) (hp: $u_{\mathrm{out}_k} > v_{\mathrm{c}}$)
(j)	OFF	OFF	OFF	OFF	< 0	$-v_{\mathrm{c}}$	D_{2_k},D_{3_k} (C_{sm} is discharging) (hp: $u_{\mathrm{out}_k} + v_{\mathrm{c}} > 0$)

symmetrical monopole HVDC link - is an example of MMC-based HVDC system for off-shore wind farm integration. As the Borwin1 project cited in Section 1.1.1, it is located in the North Sea and is connected to the German grid. Lastly, the Zhoushan project in China, built in 2014, is one of the few MMC-based MTDC projects installed so far. Made up of a $134\,\mathrm{km}$, $200\,\mathrm{kV}$, $800\,\mathrm{MW}$ five-terminal system, its purpose is to guarantee the distribution of power among different islands in the Zhoushan region.

As previously mentioned, one issue regarding MMCs based on half-bridge SMs is their incapability of limiting DC-side fault currents. The adoption of full-bridge cell SMs, whose schematic and operating states are reported in Fig. 1.9(b) and Table 1.9, allows solving this problem. Compared to its half-bridge counterpart, this SM model offers more operating states, thus granting grant more flexibility to the MMC modulation strategy. The most important feature of this SM, though, is its capability of limiting DC-side fault currents. By blocking the SMs in each arm, it is possible to obtain SM string voltages $v_{u_k}^{\mathrm{SM}}$ and $v_{l_k}^{\mathrm{SM}}$ in opposition to that at the AC side [53]. So doing, the diodes in each SM do not conduct and block the DC-side current. As a result, the faulty part of the system can be isolated by opening fast-acting switches directly on the DC side. This is in contrast with half-bridge SMs, which require the intervention of AC-side breakers (unless *ad hoc* DC-side breakers are used) to manage this kind of faults.

This advantage, however, is generally outweighed by the fact that with

[11] If all IGBTs are OFF and the hyphotheses in the rows of case (i) and (j) are not respected, no diode conducts.

this SM topology higher costs and converter losses are incurred. Indeed, with respect to half-bridge SMs, full-bridge cells have twice the number of semiconductor devices and ON valves during normal operation. Moreover, for HVDC grids to be developed in the future, additional DC breakers are most likely needed [16]. In the light of the above, this thesis focuses on MMCs based on half-bridge SMs.

1.3 The MMC control strategy

Just like any other converter technology, the MMC is not exempt from shortcomings. Except from the general challenges listed in Section 1.4, one of the main issues of the MMC is that its control strategy is more complex than that of other converter architectures, since it needs to process a large number of gate signals and regulate different aspects at the same time. These aspects include, for instance, the so-called circulating current and the capacitor voltage of the SMs in each arm. Over the years, industry and academia proposed several *circulating current suppression strategies* (Section 1.3.4.1) and *capacitor voltage balancing controls* (Section 1.3.4.3) to regulate these variables both during *balanced* and *unbalanced* operating conditions.

This section explains the MMC control structure illustrated in Fig. 1.10. In particular, the focus is on half-bridge SMs and balanced operating conditions (i.e., three-phase quantities have the same magnitude and are 120° out of phase with each other clockwise).[12] The control of every converter - be it for instance an MMC, a diode clamped or a flying capacitor converter - typically comprises three main parts: *upper level controls*, *lower level controls*, and *protections*.

Upper level controls (Section 1.3.3) determine the voltage needed at the AC-side point of connection of the converter to fulfil specific objectives, given by *internal settings or external dispatching orders*. The regulations that belong to this category, contrary to *lower level controls* and *protections*, practically remain the same regardless of converter technology. In the case of the MMC, the *upper level controls* provide as output a given value of $\boldsymbol{u}_{a,b,c}^{\mathrm{ref}}$, which corresponds to the vector of the reference values of the variable u_k $(k \in \{a, b, c\})$, first introduced in Eq. (1.2).

The *lower level controls* of the MMC (Section 1.3.4) translate the previously obtained reference voltages $\boldsymbol{u}_{a,b,c}^{\mathrm{ref}}$ into a specific gate signal sequence

[12] As better specified in Appendix A, this implies that all three-phase variables are characterised exclusively by a positive sequence component. The appendix explains how the controls described hereafter change in case of unbalanced conditions with a null zero sequence component.

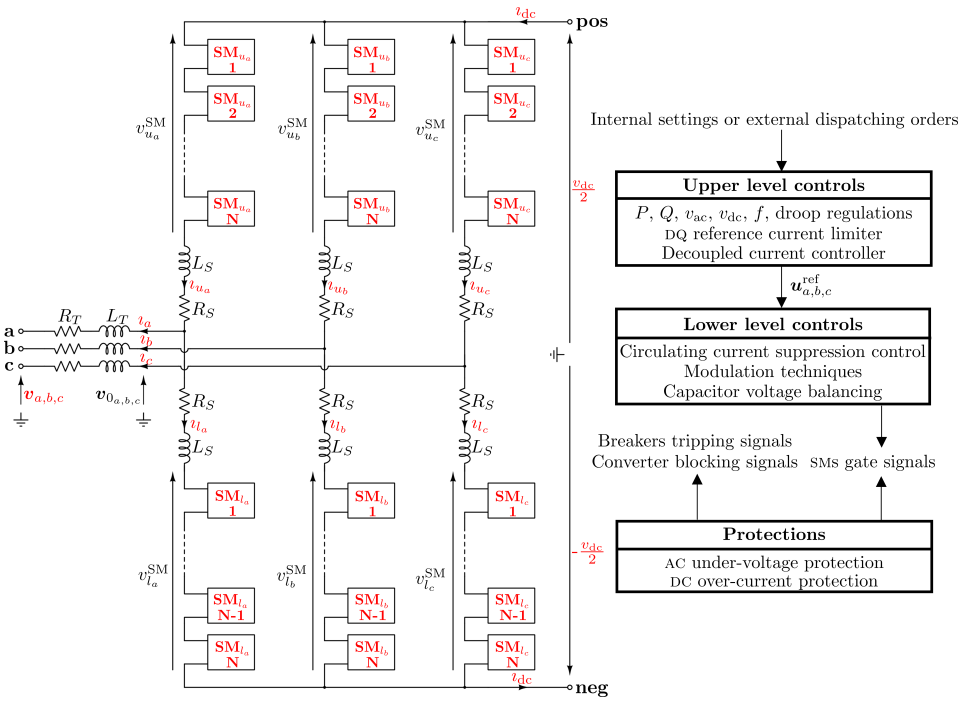


Figure 1.10: *The synthetic control scheme of an* MMC*. The electrical variables shown in red represent those measured and used as input for the* MMC *control scheme. For each* SM*, the v_c voltage shown in Fig. 1.9(a) is the measured variable.*

for the SMs, which satisfies additional desiderata (i.e., *circulating current suppression* and *capacitor voltage balancing*). The gate signals could be modified at any time by the MMC *protections* (Section 1.3.5), which could order the tripping of the converter breakers and the blocking of all SMs if abnormal operating conditions are detected.

To implement the previously described tasks, measurements are needed. The variables shown in red in Fig. 1.10 are measured and in some cases filtered to suppress high-order harmonics and contribute to the overall stability of the MMC. For each SM, the measured variable is the capacitor voltage v_c depicted in Fig. 1.9(a).

The literature provides several methods to implement the controls shown in Fig. 1.10. For the sake of brevity, major emphasis is put only on those adopted in this thesis. The works in [54–56] review some of the many other control techniques available in the literature.

1.3.1 Park transformation

A common converter regulation strategy relies on *vector current control*, which uses a rotating reference frame, synchronized with the grid voltage $\boldsymbol{v}_{a,b,c}$ through a *phase-locked loop (*PLL*)*. The rotating reference frame is related to the Park transformation, described in Eq. (1.3). It converts any set of three-phase variables (i.e., the ABC-frame given by the variables x_a, x_b, and x_c) into another set of three quantities, namely the direct, quadrature, and homopolar components (i.e., the DQ0-frame given by the variables x_d, x_q, and x_0). On the contrary, the inverse Park transformation, shown in Eq. (1.4), performs the opposite conversion. In the following figures, Eq. (1.3) and Eq. (1.4) are also referred to as "*abc/dq*" and "*dq/abc*" transformations, respectively.

$$\begin{bmatrix} x_d(t) \\ x_q(t) \\ x_0(t) \end{bmatrix} = \sqrt{\frac{2}{3}} \overbrace{\begin{bmatrix} \cos(\theta(t)) & \cos\left(\theta(t)-\frac{2\pi}{3}\right) & \cos\left(\theta(t)+\frac{2\pi}{3}\right) \\ -\sin(\theta(t)) & -\sin\left(\theta(t)-\frac{2\pi}{3}\right) & -\sin\left(\theta(t)+\frac{2\pi}{3}\right) \\ \sqrt{1/2} & \sqrt{1/2} & \sqrt{1/2} \end{bmatrix}}^{\boldsymbol{\Gamma}(\theta(t))} \begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} \tag{1.3}$$

$$\begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} = \sqrt{\frac{2}{3}} \overbrace{\begin{bmatrix} \cos(\theta(t)) & -\sin(\theta(t)) & \sqrt{1/2} \\ \cos\left(\theta(t)-\frac{2\pi}{3}\right) & -\sin\left(\theta(t)-\frac{2\pi}{3}\right) & \sqrt{1/2} \\ \cos\left(\theta(t)+\frac{2\pi}{3}\right) & -\sin\left(\theta(t)+\frac{2\pi}{3}\right) & \sqrt{1/2} \end{bmatrix}}^{\boldsymbol{\Gamma}^{-1}(\theta(t))=\boldsymbol{\Gamma}^{\mathrm{T}}(\theta(t))} \begin{bmatrix} x_d(t) \\ x_q(t) \\ x_0(t) \end{bmatrix} \tag{1.4}$$

Before discussing the advantages of resorting to the Park transformation and explaining the PLL, it is worth introducing some variables and concepts that recur throughout this section and Appendix A. The first variable is the *space phasor* (or *space vector*) $\bar{x}(t)$ [57], defined as

$$\bar{x}(t) \equiv \sqrt{\frac{2}{3}} \left(x_a(t) + x_b(t) e^{\mathrm{j}\frac{2}{3}\pi} + x_c(t) e^{-\mathrm{j}\frac{2}{3}\pi} \right) . \tag{1.5}$$

In the specific case of the Park transformation, Eq. (1.5) can be recast as shown in Eq. (1.6). For the sake of brevity, the following equations usually omit the time dependence of their variables. Moreover, in the derivation process, the terms x_a, x_b, and x_c have been replaced with their equivalent expressions given by Eq. (1.4), thereby leading to the A, B, and C terms

listed in Eq. (1.7). These terms are gradually simplified by resorting to Euler's formula and basic algebra.

$$\begin{aligned}\bar{x} &= \sqrt{\frac{2}{3}}\left(x_a + x_b e^{\mathbb{j}\frac{2\pi}{3}} + x_c e^{-\mathbb{j}\frac{2\pi}{3}}\right) = \\ &= \sqrt{\frac{2}{3}}\left(A + B + C\right) = \\ &= \left(x_d + \mathbb{j}x_q\right) e^{\mathbb{j}\theta}\,.\end{aligned} \tag{1.6}$$

$$\begin{aligned}A =& \sqrt{\frac{2}{3}}x_d\left[\cos(\theta) + \cos\left(\theta - \frac{2\pi}{3}\right)e^{\mathbb{j}\frac{2\pi}{3}} + \cos\left(\theta + \frac{2\pi}{3}\right)e^{-\mathbb{j}\frac{2\pi}{3}}\right] = \\ =& \frac{x_d}{2}\sqrt{\frac{2}{3}}\left\{e^{\mathbb{j}\theta} + e^{-\mathbb{j}\theta} + \left[e^{\mathbb{j}\left(\theta-\frac{2\pi}{3}\right)} + e^{-\mathbb{j}\left(\theta-\frac{2\pi}{3}\right)}\right]e^{\mathbb{j}\frac{2\pi}{3}} + \right. \\ & \left.\left[e^{\mathbb{j}\left(\theta+\frac{2\pi}{3}\right)} + e^{-\mathbb{j}\left(\theta+\frac{2\pi}{3}\right)}\right]e^{-\mathbb{j}\frac{2\pi}{3}}\right\} = \\ =& \frac{x_d}{2}\sqrt{\frac{2}{3}}\left[3e^{\mathbb{j}\theta}\underbrace{+e^{-\mathbb{j}\theta} + e^{-\mathbb{j}\left(\theta-\frac{4\pi}{3}\right)} + e^{-\mathbb{j}\left(\theta+\frac{4\pi}{3}\right)}}_{\equiv 0}\right] = \sqrt{\frac{3}{2}}x_d e^{\mathbb{j}\theta}\end{aligned}$$

$$\begin{aligned}B =& -\sqrt{\frac{2}{3}}x_q\left[\sin(\theta) + \sin\left(\theta - \frac{2\pi}{3}\right)e^{\mathbb{j}\frac{2\pi}{3}} + \sin\left(\theta + \frac{2\pi}{3}\right)e^{-\mathbb{j}\frac{2\pi}{3}}\right] = \\ =& \mathbb{j}\frac{x_q}{2}\sqrt{\frac{2}{3}}\left\{e^{\mathbb{j}\theta} - e^{-\mathbb{j}\theta} + \left[e^{\mathbb{j}\left(\theta-\frac{2\pi}{3}\right)} - e^{-\mathbb{j}\left(\theta-\frac{2\pi}{3}\right)}\right]e^{\mathbb{j}\frac{2\pi}{3}} + \right. \\ & \left.\left[e^{\mathbb{j}\left(\theta+\frac{2\pi}{3}\right)} - e^{-\mathbb{j}\left(\theta+\frac{2\pi}{3}\right)}\right]e^{-\mathbb{j}\frac{2\pi}{3}}\right\} = \\ =& \mathbb{j}\frac{x_q}{2}\sqrt{\frac{2}{3}}\left[3e^{\mathbb{j}\theta}\underbrace{-e^{-\mathbb{j}\theta} - e^{-\mathbb{j}\left(\theta-\frac{4\pi}{3}\right)} - e^{-\mathbb{j}\left(\theta+\frac{4\pi}{3}\right)}}_{\equiv 0}\right] = \mathbb{j}\sqrt{\frac{3}{2}}x_q e^{\mathbb{j}\theta}\end{aligned} \tag{1.7}$$

$$C = \sqrt{\frac{2}{3}}\sqrt{\frac{1}{2}}x_0\underbrace{\left(1 + e^{\mathbb{j}\frac{2\pi}{3}} + e^{-\mathbb{j}\frac{2\pi}{3}}\right)}_{\equiv 0} = 0$$

Based on Eq. (1.4) and Eq. (1.6), the variables in the ABC-frame (x_a, x_b, and x_c) can also be derived from their corresponding space phasor $\bar{x}$ and homopolar component x_0 as

$$\begin{aligned} x_a &= \sqrt{\tfrac{2}{3}}\mathrm{Re}\{\bar{x}\} + \sqrt{\tfrac{1}{3}}x_0 \\ x_b &= \sqrt{\tfrac{2}{3}}\mathrm{Re}\{\bar{x}e^{-\mathbb{j}\frac{2\pi}{3}}\} + \sqrt{\tfrac{1}{3}}x_0 \\ x_c &= \sqrt{\tfrac{2}{3}}\mathrm{Re}\{\bar{x}e^{\mathbb{j}\frac{2\pi}{3}}\} + \sqrt{\tfrac{1}{3}}x_0\,. \end{aligned} \tag{1.8}$$

Consider now a three-phase element characterised by a set of voltages (v_a, v_b, and v_c) and currents ($\imath_a$, $\imath_b$, and $\imath_c$). Its instantaneous power $p(t)$ can be computed as shown in Eq. (1.9) by exploiting the corresponding space phasors (i.e., $\bar{v}$ and $\bar{\imath}$) and homopolar components (i.e., v_0 and $\imath_0$). For the sake of brevity, the mathematical steps required to obtain the final solution are omitted. The interested reader can find similar computations in [57].

$$\begin{aligned} p(t) &= v_a\imath_a + v_b\imath_b + v_c\imath_c = \\ &= \sum_{\alpha\in\{0,\pm\frac{2\pi}{3}\}} \left[\left(\sqrt{\frac{2}{3}}\mathrm{Re}\{\bar{v}e^{\mathbb{j}\alpha}\}+\sqrt{\frac{1}{3}}v_0\right)\left(\sqrt{\frac{2}{3}}\mathrm{Re}\{\bar{\imath}e^{\mathbb{j}\alpha}\}+\sqrt{\frac{1}{3}}\imath_0\right)\right] = \\ &= \ \ldots = \underbrace{\mathrm{Re}\{\bar{v}\bar{\imath}^*\}}_{P} + \underbrace{v_0\imath_0}_{P_0}\,. \end{aligned} \tag{1.9}$$

The P and P_0 terms in Eq. (1.9) are respectively the real and homopolar power. Based on Eq. (1.6), the former can also be computed by substituting the space phasors of voltage and current with their corresponding direct and quadrature components, thereby leading to the first equation of Eq. (1.10). The other two equations allow computing the reactive power Q and complex power S.

$$\begin{aligned} P &= \mathrm{Re}\{\bar{v}\bar{\imath}^*\} = \mathrm{Re}\left\{(v_d+\mathbb{j}v_q)e^{\mathbb{j}\theta}(\imath_d-\mathbb{j}\imath_q)e^{-\mathbb{j}\theta}\right\} = v_d\imath_d+v_q\imath_q \\ Q &= \mathrm{Im}\{\bar{v}\bar{\imath}^*\} = \mathrm{Im}\left\{(v_d+\mathbb{j}v_q)e^{\mathbb{j}\theta}(\imath_d-\mathbb{j}\imath_q)e^{-\mathbb{j}\theta}\right\} = v_q\imath_d-v_d\imath_q \\ S &= \bar{v}\bar{\imath}^* = P+\mathbb{j}Q\,. \end{aligned} \tag{1.10}$$

In the light of the above, $p = v_a\imath_a+v_b\imath_b+v_c\imath_c = P+P_0 = v_d\imath_d+v_q\imath_q+v_0\imath_0$. Based on this property, the Park transformation shown in Eq. (1.3) is said to be *power invariant*.[13]

[13] An alternative Park transformation, known as *amplitude invariant*, is shown in [58], where the matrix in $\mathbf{\Gamma}$ is multiplied by $\frac{2}{3}$ instead of $\sqrt{\frac{2}{3}}$. On the one hand, during balanced operating conditions, the *amplitude invariant* Park transformation leads to DQ0-frame variables having the same amplitude as those in the ABC-frame. However, the powers computed in the two frames differ. On the other hand, in the *power invariant* Park transformation, the DQ0-frame variables are $\sqrt{\frac{3}{2}}$ times those in the ABC-frame, but the powers in the two frames coincide. The interested reader can refer to [58] for a detailed comparison of these transformations.

1.3.2 Phase-locked loop PLL

The Park transformation has the great advantage of converting a *balanced* set of three-phase waveforms in the reference ABC-frame into a *constant* point in the DQ0-frame. This property holds only if $\dot{\theta}(t) = \omega(t)$, with ω being the angular frequency of the ABC-frame. In other words, the DQ0-frame is synchronized with the three-phase quantities used for the Park transformation (i.e., $\boldsymbol{v}_{a,b,c}$ in the case of the MMC control strategy).

To clarify this statement, consider for example the following set of three-phase voltages, representative of a power system in balanced operating conditions.

$$\begin{aligned} v_a(t) &= v\ \cos\left(\delta(t)\right) \\ v_b(t) &= v\ \cos\left(\delta(t) - \tfrac{2}{3}\pi\right) \\ v_c(t) &= v\ \cos\left(\delta(t) + \tfrac{2}{3}\pi\right)\ . \end{aligned} \tag{1.11}$$

If the Park transformation in Eq. (1.3) is applied to the variables above, two main features can be observed. First, the corresponding homopolar component v_0 is null (and so is the homopolar component of any other variable, assuming balanced operating conditions). Thus, $P_0 = v_0 v_0 = 0$. Second, the direct and quadrature components v_d and v_q are constant only if $\dot{\theta}(t) = \dot{\delta}(t) = \omega(t)$ (i.e., the DQ0 and ABC frames are synchronized).[14] The same holds for other three-phase variables expressed in the DQ0-frame. As shown in the following, the absence of time-dependence is a useful feature, which justifies the adoption of Park transformation in typical converter regulation strategies.

To achieve synchronization, this thesis adopts a phase-locked loop (PLL), which exploits the AC-side voltage $\boldsymbol{v}_{a,b,c}$ at the point of connection of the converter. Figure 1.11 depicts the simplest structure of the PLL[15]. The control is such that the quadrature component of the grid voltage v_q, measured at the point of connection of the converter, stays close to zero. To do so, any value of v_q different from zero is considered as an error ε and constitutes the input of a PI regulator. In turn, the regulator outputs the angular frequency variation $\Delta\omega$ needed to ensure synchronization between the rotating reference and three-phase frames. This variation, summed to the nominal grid angular frequency ω_0, is integrated, thereby deriving the angle θ needed for the Park transformation.

It is worth pointing out that the PLL, as well as other controls listed in Fig. 1.10, rely on the per-unit conversion of the inputs (i.e., voltages, cur-

[14] In particular, it can be demonstrated through Eq. (1.3) that v_q is null if $\theta(t) = \delta(t)$.

[15] The PLL described in the following is typically adopted in energy conversion systems such as power electronic converters [59, 60]. Its design is different from that of other PLLs adopted in electronic applications.

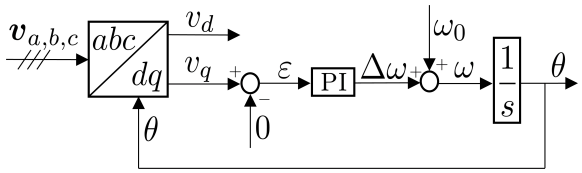


Figure 1.11: *The schematic of a* PLL *used in energy conversion systems.*

rents and powers). In other words, all values are normalized to a base value. By doing so, provided that the converter ratings do not change significantly, the control parameters can be flexibly re-used. Another advantage of this per-unit control is that all the limit values (associated with security constraints, such as maximum AC-side current) remain the same regardless of converter ratings [61].

1.3.3 Upper level controls

Regardless of converter technology, VSCs are entrusted with different tasks, such as P-Q and DC-AC voltage control. These tasks are included in the *upper level controls*: each of them is associated with some setpoints, which derive from default internal settings or external ones sent by a transmission system operator in the form of a dispatching order.

To explain how these controls are implemented, recall that the active and reactive power P and Q associated with the MMC can be computed as shown in Eq. (1.11). The direct and quadrature components of voltages and currents (v_d, v_q, $\imath_d$, and $\imath_q$) are associated with the variables $\boldsymbol{v}_{a,b,c}$ and $\boldsymbol{\imath}_{a,b,c}$ depicted in Fig. 1.10 (note that their direction is such that a positive value of P denotes active power flowing from the DC to the AC-side). At steady-state, the presence of the PLL is such at $v_q = 0$. Thus, $P = v_d\imath_d$ and $Q = -v_d\imath_q$. In addition, assuming that the converter is connected to an almost infinitely stiff AC grid[16], the voltage v_d is fairly constant, so the only variables that can be regulated are the direct and quadrature current at the AC-side terminals of the converter.

Therefore, the name of vector current control derives from the fact that it regulates $\imath_d$ and $\imath_q$ to fulfil specific active and reactive power setpoint values, respectively. As explained in [57], these currents can also be used to control respectively the DC and AC-side voltage. On the contrary, the homopolar component of the line current $\imath_0$ is not regulated under the assump-

[16]According to [57], an infinitely stiff AC grid can be modelled with a balanced and sinusoidal three-phase voltage source of constant amplitude and frequency. This implies that the voltage at the point of connection of the converter in normal operating conditions basically remains the same regardless of power fluctuations.

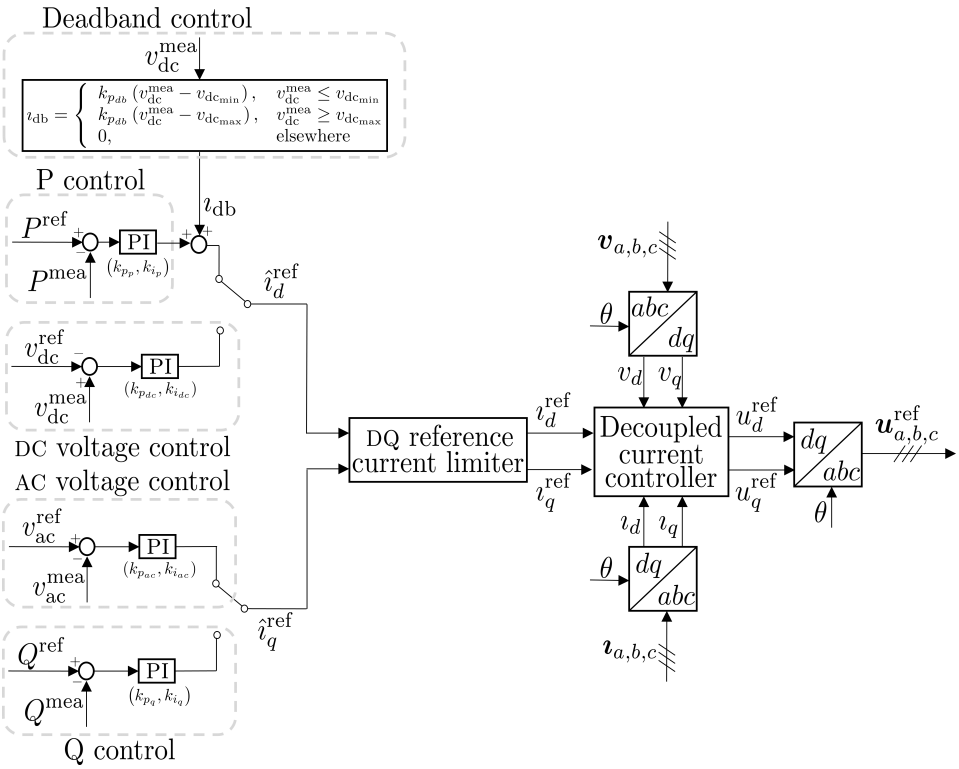


Figure 1.12: *The schematic of the upper level controls. These control are typically compatible with any* VSC *technology. Other control functions not used in this thesis, such as frequency control, $P - v_{dc}$, and $Q - v_{ac}$ droop regulations were omitted for brevity.*

tion of balanced operating conditions. Indeed, in this case, the homopolar component of any three-phase set of variables is null.[17]

In the light of the above, the *upper level controls* can be represented with the control structure shown in Fig. 1.12. Based on *internal settings or external dispatching orders* (see Fig. 1.10), the converter regulates either P or v_{dc} and Q or v_{ac}, so that specific setpoints are fulfilled. Each setpoint value is compared with its measured counterpart at the converter terminals; any difference between the two quantities is an input for a PI controller, which outputs a reference current - either on the direct ($\hat{\imath}_d^{\mathrm{ref}}$) or quadrature ($\hat{\imath}_q^{\mathrm{ref}}$) axis, depending on the control considered. In the specific case of active

[17] As stated in [61], the control of $\imath_0$ can be in general avoided by connecting the AC-side of the MMC to the secondary winding of a Y_g/Δ transformer. Since in the delta (Δ) windings no path to ground is available for the currents, the three-phase line currents are such that $\imath_a + \imath_b + \imath_c = 0$. According to Eq. (1.3), this implies that $\imath_0$ is null. This aspect is considered once again in Appendix A.

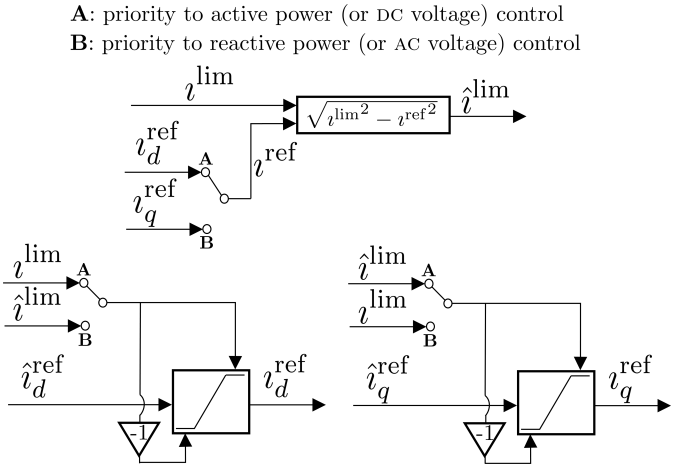


Figure 1.13: *The schematic of the* DQ *reference current limiter.*

power regulation, the reference current $\hat{\imath}_d^{\mathrm{ref}}$ also depends on an additional control, referred to in [61] as *deadband control*. In a nutshell, the purpose of this block is to limit $\hat{\imath}_d^{\mathrm{ref}}$ so that the DC-side voltage $v_{\mathrm{dc}}^{\mathrm{mea}}$ does not vary excessively from its nominal value. Section 3.2.2 includes some comments on the usefulness of this control in a specific simulated scenario.

Then, the reference values $\hat{\imath}_d^{\mathrm{ref}}$ and $\hat{\imath}_q^{\mathrm{ref}}$ are processed through the DQ *reference current limiter*, illustrated in Fig. 1.13, which ensures that $|\hat{\imath}_d^{\mathrm{ref}} + \mathbb{j}\hat{\imath}_q^{\mathrm{ref}}|$ is within a given value. If not, the actual reference values are somehow limited, by giving priority to either $\hat{\imath}_d^{\mathrm{ref}}$ or $\hat{\imath}_q^{\mathrm{ref}}$ (see case **A** and **B** in Fig. 1.13). As a consequence, the AC-side current of the MMC is always limited (even during three-phase AC-faults and without needing to block the MMC), thereby preventing the breach of the converter current ratings.

The direct-quadrature reference currents $\imath_d^{\mathrm{ref}}$ and $\imath_q^{\mathrm{ref}}$ exiting the DQ *reference current limiter* - together with $v_d, v_q, \imath_d$ and $\imath_q$ - are the inputs of the *decoupled current controller*, whose schematic is shown in Fig. 1.14(b). To explain its operating principle, consider once again the MMC schematic in Fig. 1.8. The grid voltage v_k $(k \in \{a, b, c\})$ amounts to:

$$v_k = -R_T\, \imath_k - L_T\, \frac{d\imath_k}{dt} - v_{0_k} \tag{1.12}$$

By exploiting Eq. (1.2), the previous equation can be recast as follows:

$$v_k = \underbrace{\frac{1}{2}\left(v_{l_k}^{\mathrm{SM}} - v_{u_k}^{\mathrm{SM}}\right)}_{u_k} - \left(R_T + \frac{R_S}{2}\right) \imath_k - \left(L_T + \frac{L_S}{2}\right) \frac{d\imath_k}{dt}\,, \tag{1.13}$$

where u_k is the voltage controlled by the converter (i.e., the output of the *upper level controls* in Fig. 1.12). By resorting to Eq. (1.6), the previous equation can be analysed as shown in Eq. (1.14) with space phasors, denoted by an upper bar.

$$\bar{v} = \bar{u_k} - \left(R_T + \frac{R_S}{2}\right) \bar{\imath} - \left(L_T + \frac{L_S}{2}\right) \frac{d\bar{\imath}}{dt}$$

$$\begin{aligned}(v_d + \mathbb{j} v_q)\, e^{\mathbb{j}\theta} = (u_d + \mathbb{j} u_q)\, e^{\mathbb{j}\theta} - \left(R_T + \frac{R_S}{2}\right) (\imath_d + \mathbb{j}\imath_q)\, e^{\mathbb{j}\theta} + \\ - \left(L_T + \frac{L_S}{2}\right) \frac{d}{dt}\left[(\imath_d + \mathbb{j}\imath_q)\, e^{\mathbb{j}\theta}\right]\end{aligned} \tag{1.14}$$

$$\begin{aligned}(v_d + \mathbb{j} v_q)\, e^{\mathbb{j}\theta} = (u_d + \mathbb{j} u_q)\, e^{\mathbb{j}\theta} - \left(R_T + \frac{R_S}{2}\right) (\imath_d + \mathbb{j}\imath_q)\, e^{\mathbb{j}\theta} + \\ - \mathbb{j}\omega \left(L_T + \frac{L_S}{2}\right) (\imath_d + \mathbb{j}\imath_q)\, e^{\mathbb{j}\theta} - \left(L_T + \frac{L_S}{2}\right) \frac{d}{dt} (\imath_d + \mathbb{j}\imath_q)\, e^{\mathbb{j}\theta}\end{aligned}$$

The mathematical steps shown in the previous equation lead to two terms associated with $\left(L_T + \frac{L_S}{2}\right)$. This is due to the fact that in the term $\frac{d}{dt}\left[(\imath_d + \mathbb{j}\imath_q)\, e^{\mathbb{j}\theta}\right]$ not only θ, but also $\imath_d$ and $\imath_q$ are generally time-varying.

By analysing separately the real and imaginary part of Eq. (1.14), the following system of equations can be obtained.

$$\begin{cases} v_d = u_d - \left(R_T + \frac{R_S}{2}\right) \imath_d - \left(L_T + \frac{L_T}{2}\right) \frac{d\imath_d}{dt} + \omega \left(L_T + \frac{L_T}{2}\right) \imath_q \\ v_q = u_q - \left(R_T + \frac{R_S}{2}\right) \imath_q - \left(L_T + \frac{L_T}{2}\right) \frac{d\imath_q}{dt} - \omega \left(L_T + \frac{L_T}{2}\right) \imath_d \end{cases} \tag{1.15}$$

By applying the Laplace transformation, the equations in Eq. (1.16) can be derived [57]. Such equations give shape to the diagram block in Fig. 1.14(a), which depicts the physical relationship between the converter voltage and its output current.

$$\begin{cases} v_d = u_d - \left[R_T + \frac{R_S}{2} + s\left(L_T + \frac{L_S}{2}\right)\right] \imath_d + \omega \left(L_T + \frac{L_S}{2}\right) \imath_q \\ v_q = u_q - \left[R_T + \frac{R_S}{2} + s\left(L_T + \frac{L_S}{2}\right)\right] \imath_q - \omega \left(L_T + \frac{L_S}{2}\right) \imath_d \end{cases} \tag{1.16}$$

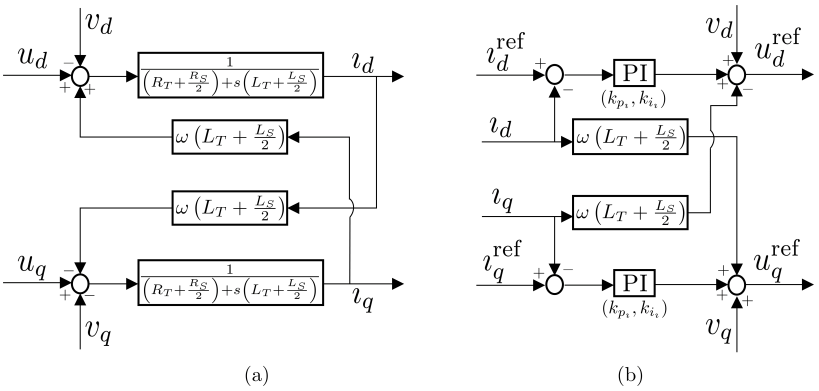


Figure 1.14: *Diagram block depicting the physical relationships among the direct-quadrature converter voltages and currents (a) and the decoupled current control of the* MMC *(b).*

It is worth pointing out that the terms $-v_d + \omega\left(L_T + \frac{L_S}{2}\right)\imath_q$ and $-v_q - \omega\left(L_T + \frac{L_S}{2}\right)\imath_d$ are considered from the control point of view as disturbances that are compensated in the *decoupled current control*, as reported in Fig. 1.14(b). In this case, the reference and measured direct and quadrature currents are compared and their difference is used as an input for PI controllers. The resulting output, which includes a compensation of the previously mentioned disturbances [57], is associated with the converter reference voltages. Once computed, the direct and quadrature-axis reference voltage components are converted back to ABC-frame through the inverse Park transformation (recall that, in balanced conditions, homopolar quantities are null).

1.3.4 Lower level controls

In the *upper level controls*, the voltages u_k^{ref} have been determined. However, in the specific case of the MMC, the ultimate goal of the control strategy is to compute the reference voltages of $v_{l_k}^{\text{SM}}$ and $v_{u_k}^{\text{SM}}$ associated with the SM strings in each arm. In turn, these voltages correspond to a given gate signal sequence for the IGBTs in each SM, whose identification is the main objective of the *lower level controls*. These controls include a *circulating current suppression strategy*, a *modulation technique*, and a *capacitor voltage balancing control*, all of which are explained in the following subsections.

1.3.4.1 Circulating current suppression control

It is worth noting that since $u_k^{\text{ref}} = \frac{1}{2}\left(v_{l_k}^{\text{SM,ref}} - v_{u_k}^{\text{SM,ref}}\right)$, there are in principle many combinations of the upper and lower SM string voltages in each arm that lead to the same value of u_k^{ref}. However, as explained in this subsection, there is only an optimal combination that yields the minimization of the so-called circulating currents. The next paragraphs explain what circulating currents are, how they originate, and why they should be limited.

To begin with, consider once again Fig. 1.8. Each arm current ($\imath_{u_k}$, $\imath_{l_k}$) can be regarded as the sum of two components - namely the grid current $\imath_k$ and a current $\imath_{z_k}$ - that lead to the following expressions

$$\begin{aligned} \imath_{u_k} &= \frac{1}{2}\imath_k + \imath_{z_k} \\ \imath_{l_k} &= -\frac{1}{2}\imath_k + \imath_{z_k}\,. \end{aligned} \tag{1.17}$$

The equations above result in the currents $\imath_k$ and $\imath_{z_k}$ being equal to

$$\begin{aligned} \imath_k &= \imath_{u_k} - \imath_{l_k} \\ \imath_{z_k} &= \frac{1}{2}\left(\imath_{u_k} + \imath_{l_k}\right)\,. \end{aligned} \tag{1.18}$$

By exploiting Eq. (1.17), the DC-side current $\imath_{\text{dc}}$ (assumed hereafter to be constant) is related to the $\imath_{z_k}$ component of the arm currents as follows

$$\begin{aligned} \imath_{\text{dc}} &= \imath_{u_a} + \imath_{u_b} + \imath_{u_c} = \\ &= \frac{1}{2}\underbrace{\left(\imath_a + \imath_b + \imath_c\right)}_{=0 \text{ (balanced system)}} + \imath_{z_a} + \imath_{z_b} + \imath_{z_c} = \\ &= \imath_{z_a} + \imath_{z_b} + \imath_{z_c}\,. \end{aligned} \tag{1.19}$$

In ideal conditions, $\imath_{\text{dc}}$ would be equally shared among each phase leg so that $\imath_{z_a} = \imath_{z_b} = \imath_{z_c} = \frac{\imath_{\text{dc}}}{3}$. In practical applications, however, this is not true. The mathematical steps in Eq. (1.20) - obtained by considering any mesh given by a phase leg and the DC-side terminals - show that the currents $\imath_{z_k}$ are linked not only to the DC-side current, but also to the voltage balance among the DC side and the SMs strings in each arm.

$$
\begin{aligned}
&v_{l_k}^{SM} + v_{u_k}^{SM} + R_S\left(\imath_{u_k} + \imath_{l_k}\right) + L_S\frac{d}{dt}\left(\imath_{u_k} + \imath_{l_k}\right) - v_{\mathrm{dc}} = 0 \\
&v_{l_k}^{SM} + v_{u_k}^{SM} + 2R_S\,\imath_{z_k} + 2L_S\frac{d\imath_{z_k}}{dt} - v_{\mathrm{dc}} = 0 \\
&R_S\,\imath_{z_k} + L_S\frac{d\imath_{z_k}}{dt} = \frac{1}{2}\left[v_{\mathrm{dc}} - \left(v_{l_k}^{\mathrm{SM}} + v_{u_k}^{\mathrm{SM}}\right)\right]
\end{aligned}
\tag{1.20}
$$

Assuming momentarily that $R_S \approx 0$, the current $\imath_{z_k}$ varies whenever the sum between the voltages of the upper and lower SMs strings in the k-th arm does not coincide with the pole-to-pole voltage v_{dc} (i.e., $v_{\mathrm{dc}} \neq v_{l_k}^{\mathrm{SM}} + v_{u_k}^{\mathrm{SM}}$). During normal operation, the current and the number of inserted SMs (i.e., the only ones whose capacitor voltage varies based on the sign of the current) in each arm continuously change over time. This inevitably leads to an uneven distribution of the capacitor voltages in the SMs of each arm, which hinders the attainment of the abovementioned voltage match. As a result, even if $\imath_{\mathrm{dc}}$ is constant, it is not true that $\imath_{z_a} = \imath_{z_b} = \imath_{z_c} = \frac{\imath_{\mathrm{dc}}}{3}$.

In the light of the above, the $\imath_{z_k}$ component of arm currents can be rewritten as

$$
\imath_{z_k} = \frac{\imath_{\mathrm{dc}}}{3} + \imath_{circ_k}\,, \tag{1.21}
$$

where $\imath_{circ_k}$ is the circulating current, caused by the voltage unbalances among the DC side and SM strings. As can be inferred from Eq. (1.17), the presence of circulating currents in $\imath_{z_k}$ leads to an increase in the RMS of the arm currents $\imath_{u_k}$ and $\imath_{l_k}$, which results in increased converter losses and the need of choosing SMs with higher current ratings.

To avoid these issues, circulating current suppression schemes, either based on passive or active filters, should be adopted [62]. The former solution consists of additional filters that are physically installed in the MMC arms. For instance, as can be inferred from Eq. (1.20), the circulating current variation could be limited by adopting a higher inductance L_S. This solution, however, is expensive and not the most effective in terms of circulating current suppression. An alternative, more efficient solution relies on the adoption of parallel resonant filters, which allows the suppression of circulating currents without requiring an increase in the arm inductance [62]. On the contrary, active filters comprise an additional control used to regulate the gate signals of the MMC SMs. Since it is implemented on software, this kind of control does not bring additional hardware costs.

Considering the latter approach, circulating currents could be suppressed with the control outlined in [63] and shown in Fig. 1.15. As demonstrated

in [64], in balanced operating conditions, the circulating currents have a main negative sequence component at twice the fundamental frequency, which is eliminated as follows. First, the $\imath_{z_k}$ component of the arm current is computed by Eq. (1.17). Then, a Park transformation at twice the fundamental frequency (i.e., -2ω, which is related to the angle -2θ in Fig. 1.15) is performed to obtain direct and quadrature components.[18] Any non-zero value is considered as an error and used as input for PI regulators. The quantities $2\omega L_S \imath_{z_d}$ and $2\omega L_S \imath_{z_q}$ are added as in [63] for compensation purposes (analogously to the decoupled current control), thereby leading to the reference values u_{z_d} and u_{z_q}. These quantities are then brought back to the three-phase frame and exploited to compute $v_{u_k}^{\mathrm{SM,ref}}$ and $v_{l_k}^{\mathrm{SM,ref}}$. To explain how these values are determined, consider the following equations. In the derivation process, Eq. (1.2) and Eq. (1.17) have been exploited.

$$\begin{aligned}
&v_{0_k} + R_S\, \imath_{u_k} + L_S \frac{d\, \imath_{u_k}}{dt} + v_{u_k}^{\mathrm{SM}} - \frac{v_{\mathrm{dc}}}{2} = 0 \\
&\underbrace{\frac{v_{l_k}^{\mathrm{SM}} - v_{u_k}^{SM}}{2}}_{u_k} + R_S \underbrace{\left(\imath_{u_k} - \frac{\imath_k}{2}\right)}_{\imath_{z_k}} + L_S \frac{d}{dt} \underbrace{\left(\imath_{u_k} - \frac{\imath_k}{2}\right)}_{\imath_{z_k}} + v_{u_k}^{\mathrm{SM}} - \frac{v_{\mathrm{dc}}}{2} = 0 \\
&v_{u_k}^{\mathrm{SM}} = -u_k - \underbrace{\left(R_S\, \imath_{z_k} + L_S \frac{d\, \imath_{z_k}}{dt}\right)}_{u_{z_k}} + \frac{v_{\mathrm{dc}}}{2}
\end{aligned} \tag{1.22}$$

Analogous computations hold for $v_{l_k}^{\mathrm{SM}}$. While u_k is regulated by the *upper level controls*, u_{z_k} is controlled by the *circulating current suppression strategy*. Similarly to Eq. (1.22), Fig. 1.15 shows that the output of this control is combined with u_k and the DC-voltage to obtain $v_{u_k}^{\mathrm{SM,ref}}$ and $v_{l_k}^{\mathrm{SM,ref}}$, which are computed as

$$\begin{aligned}
v_{u_k}^{\mathrm{SM,ref}} &= -u_k^{\mathrm{ref}} - u_{z_k}^{\mathrm{ref}} + \frac{v_{\mathrm{dc}}}{2} \\
v_{l_k}^{\mathrm{SM,ref}} &= -u_k^{\mathrm{ref}} + u_{z_k}^{\mathrm{ref}} + \frac{v_{\mathrm{dc}}}{2}\,.
\end{aligned} \tag{1.23}$$

[18] As better specified in Appendix A, a negative sequence component is associated with a set of three-phase quantities $\boldsymbol{x}_{a,b,c}$ equal in magnitude but phased out of 120° counterclockwise (instead of clockwise, as in balanced operating conditions). Assuming that the angular frequency of this set is equal to $\omega(t)$, it can be demonstrated that constant direct and quadrature Park components $\boldsymbol{x}_{d,q}$ can be obtained by applying Eq. (1.3) to $\boldsymbol{x}_{a,b,c}$ and letting $\dot{\theta}(t) = -\omega(t)$. When dealing with the suppression of the MMC circulating currents, this is reflected by the minus sign next to 2θ in Fig. 1.15 (as stated in Section 1.3.2, $\theta(t)$ is related to $+\omega(t)$).

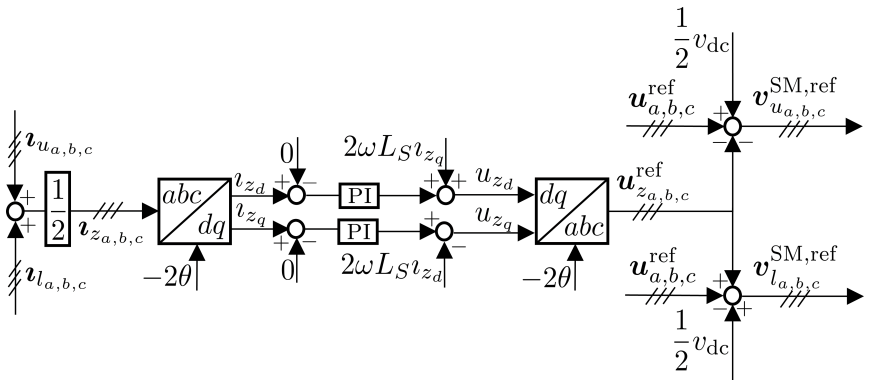


Figure 1.15: *The schematic of the* MMC *circulating current suppression control.*

1.3.4.2 Modulation techniques

The objective of *modulation techniques* is to determine, based on the voltage reference values $v_{l_k}^{\mathrm{SM,ref}}$ and $v_{u_k}^{\mathrm{SM,ref}}$, the number of inserted and bypassed SMs in each arm. Over the years, academia and industry have developed a plethora of different modulation techniques. Some of them operate at high switching frequencies, whereas in others the switching frequency is close to the nominal one of the grid. The works in [54, 55] provide an extensive review of different modulation strategies.

In this thesis, the Nearest Level Modulation (NLM) is adopted. It is a technique that operates at low switching frequencies and it is suited for MMCs with a high number of SMs. To explain how it works, consider an MMC made up of N SMs in each arm, whose capacitor voltages are assumed to be more or less the same (i.e., $\frac{v_{\mathrm{dc}}}{N}$). Each SM in one arm, if inserted, contributes to a fraction of the overall voltage at the SMs string. As a result, a given reference voltage value $v_{j_k}^{\mathrm{SM,ref}}$ ($j \in \{u, l\}$, $k \in \{a, b, c\}$) corresponds to a specific number of inserted $N_{j,k}^{\mathrm{in}}$ and bypassed $N_{j,k}^{\mathrm{by}}$ SMs equal to

$$\begin{aligned} N_{j_k}^{\mathrm{in}} &= round\left(\frac{v_{j_k}^{\mathrm{SM,ref}}}{v_{\mathrm{dc}}}\right) \\ N_{j_k}^{\mathrm{by}} &= N - N_{j_k}^{\mathrm{in}}\,. \end{aligned} \tag{1.24}$$

Around the threshold crossings in Fig. 1.16 (i.e., whenever $N_{j_k}^{\mathrm{in}}$ changes value), the number of inserted and bypassed SMs in one arm changes. As described in the next section, the specific SMs that need to be inserted or bypassed are chosen based on *capacitor voltage balancing algorithms*.

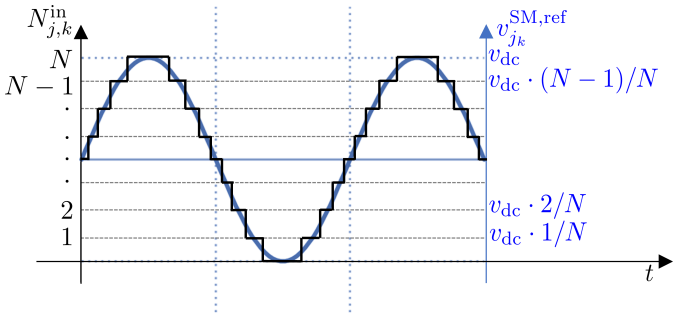


Figure 1.16: *The operating principle of the* NLM.

It should be specified that formulas in Eq. (1.24) are valid only in normal operating conditions. Indeed, as described in Section 1.3.5, the number of inserted and bypassed SMs is also influenced by the MMC protections, which drive the SMs to the blocked status if faults in the AC or DC side are detected.

1.3.4.3 Capacitor voltage balancing algorithms

As previously stated, the normal operation of MMCs leads to an uneven distribution of the SM capacitor voltages. As in the flying capacitor converter, *Capacitor voltage Balancing Algorithms (*CBA*s)* are necessary to address this issue. One of the simplest ways of controlling the capacitor voltages is outlined in [65] and can be described as follows.

Suppose that, at a given time instant, the modulation imposes a change in the number of inserted SMs in one arm (e.g., $\hat{N}$). In the light of the operating states highlighted in Table 1.8, the capacitor voltages of the inserted SMs either increase or decrease based on the sign of the current, while that of the bypassed SMs is practically unaltered. This happens because, as previously stated, only a negligible fraction of the arm current (i.e., the leakage current of the S_{1_k} IGBT in Fig. 1.9(a)) flows through them. Bearing this in mind, the CBA sorts the capacitor voltages v_c and, if the arm current is positive (i.e., capacitors charge), it inserts the first $\hat{N}$ SMs having the lowest capacitor voltages. On the contrary, if the arm current is negative (i.e., capacitors discharge), the $\hat{N}$ SMs having the highest capacitor voltage are selected. On the contrary, the remaning SMs are bypassed.

Albeit conceptually simple, this approach leads to high switching losses. Indeed, at every threshold crossing in the modulation block, the gate signals of many SMs would continuously change to make them shift from inserted to bypassed operating conditions and vice versa. To mitigate this issue, the

Table 1.10: *Capacitor voltage balancing algorithm: criteria for inserting or bypassing a half-bridge* SM.

Required action	$\imath_{\mathrm{arm}} > 0$	$\imath_{\mathrm{arm}} < 0$
Insert a new SM	Insert the bypassed SM with the lowest v_{c}	Insert the bypassed SM with the highest v_{c}
Bypass a new SM	Bypass the inserted SM with the highest v_{c}	Bypass the inserted SM with the lowest v_{c}

CBA could instead alter the state of just one SM at a time, as described in Table 1.10. However, if the number of SMs in each arm is high, this solution might lead to unsatisfactory voltage ripples across each SM capacitor. To solve this problem, a trade-off between the two solutions can be adopted. In this thesis, the CBA was modified to act on a higher number of SMs (that is, 20) at each crossing. Through MMC simulations, it was observed that this solution improves voltage balancing and circulating current suppression.

All of these solutions, however, require the knowledge of not only the arm currents, but also of the capacitor voltage of every SM in the MMC. In practical applications, this leads to a high number of measurements and reliability issues. Although this aspect is neglected in this work, it is worth pointing out that some "sensorless" capacitor balancing algorithms were proposed in the literature [66].

1.3.5 Protections

Protections are needed to prevent abnormal operating conditions, such as AC and DC faults, from damaging the converter. Figure 1.17 depicts a simplified schematic that implements the protection mechanism of MMCs based on half-bridge SMs: regardless of the event, after a given time delay, the protections send a blocking signal to all the SMs (i.e., all their gate signals are OFF) and a tripping signal to the breakers at the AC side of the converter.

The proposed control scheme allows detecting faults on the AC side (e.g., three-phase to ground and single-line to ground faults) by comparing the voltages at the point of connection of the converter with a limit value. An analogous concept, based on DC-side currents, is used to detect faults at the DC terminals (e.g., pole-to-pole converter faults).

1.4 Challenges

As stated in the previous chapter, the increasing penetration of RES (and their converters) is introducing a series of challenges, which affect not only

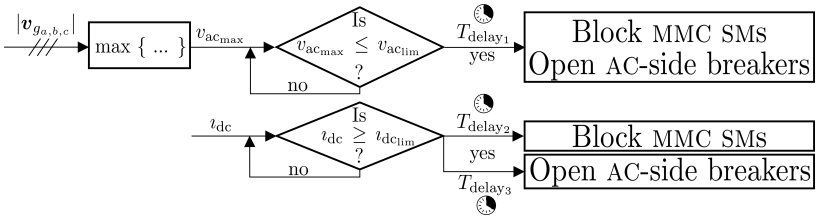


Figure 1.17: *The simplified schematic of the* MMC AC *under-voltage and* DC *over-current protections.*

the electricity network management and planning, but also the simulation environment - which is the main focus of this thesis. The following subsections describe in short some core tasks typically performed by power system simulators and how they have been lately put to the test due to, among others, the increasing adoption of MMCs - most notably in HVDC systems. The next chapters provide a more in-depth discussion about some of the aspects briefly described hereafter.

1.4.1 Power Flow

This analysis derives the steady-state solution of AC systems, which is an input needed for the other tasks mentioned in this list [58]. The power flow (PF) techniques adopted in conventional grids have become pretty established. Indeed, modern simulation tools can derive the power flow solution (PFS) of AC grids described by a single-phase equivalent model and composed of hundreds of thousands of buses and tens of thousands of synchronous generators within reasonable CPU times. However, this simulation paradigm has been recently modified to make these tools compatible with mixed AC/DC systems. This change has been triggered by the increasing penetration of HVDC and MTDC systems, most of which are foreseen to rely on MMCs. These new systems connect portions of the same AC grid or separated, possibly asynchronous, large AC networks. So far, the size of DC grids in these mixed systems is somewhat limited. However, even this feature is changing in the following years due to upcoming projects, where the HVDC and MTDC systems will form the new backbone of future transmission systems [67].

According to the literature, PF algorithms for mixed AC/DC power systems belong to two main classes: *sequential* [68–72] and *unified* methods [73–76]. Both of them rely on an iterative approach. On the one hand, sequential methods derive, at each iteration the PFS of the AC sub-systems

and then that of the DC ones. While doing so, these methods regard AC/DC converters as boundary elements between AC and DC networks. On the other hand, unified methods compute at each iteration the PFS of the whole mixed AC/DC system, without solving the AC and DC grids separately. Both methods have their pros and cons. For instance, unified approaches are more numerically efficient and less prone to convergence issues than sequential ones. On the other hand, sequential methods are easier to implement in existing AC PF programs. Indeed, the already developed routines for deriving the PFS of the AC sub-systems can be kept, and only the algorithms for computing the PFS of the DC sub-systems and handling the AC/DC converters need to be added.

Concerning this topic, a unified PF algorithm was developed during this PhD programme, which can accurately and efficiently derive the PFS of large and complex mixed AC/DC systems made up of any combination of multiple DC and possibly non-synchronized AC grids [27]. The algorithm relies on power system partitioning, a version of the two-level Newton method, and the modified nodal analysis formulation. The proposed approach is compatible with several converter control functions (e.g., P, Q, v_{ac}, and v_{dc} regulations) and can take converter losses into account through *ad hoc* models.

1.4.2 Initialization

This task, which is a prerequisite for the next ones shown in this list, receives as input the results of the power flow (i.e., bus voltages and current flows along the lines) and determines the internal states of several components needed for the subsequent simulations to begin at steady-state. In other words, no transient behaviour should be observed. In the case of synchronous generators, for example, the initialization algorithm entails the computation of their mechanical power and no-load voltage.

While this task has become a standard practice for traditional power components, it is still a relatively new topic for the MMC, whose complex model and control structure hinder its initialization process [77,78]. Indeed, its state variables cannot be easily determined not only due to the high number of SMs (and, thus, of gate signals and state variables) in each arm, but also because of its advanced control structure, which typically relies on closed-loop schemes.

A way of circumventing the need for a full-fledged initialization is to resort to *initialization transients*. In other words, simulations could start from an operating point that does not exactly correspond to steady-state

operation. As a consequence, the state variables of the power system will undergo a transient until the steady-state operation is finally reached. Until then, no disturbance or any other network event should be examined, because they might lead to unexpected network behaviour. Albeit conceptually simple, this solution requires the user to wait a given time before obtaining desired simulation results. Due to the high computational burden of the MMC during time-domain simulations (see the next bullet point), one should avoid initialization transients as much as possible.

1.4.3 Electromagnetic transient simulation

A topic of interest in the power system field is the analysis of electromagnetic and electromechanical phenomena, which act on different time scales. To analyse them, engineers typically resort to EMT and root mean square (RMS) simulations, respectively. The former grants a high degree of detail, because it adopts the differential algebraic equations (DAEs) modelling each power system device. However, this comes at the cost of a high computational burden, especially when dealing with large electricity networks.

This aspect is further worsened by the presence of MMCs. Indeed, their modularity is both a blessing and a curse. On the one hand, this feature is the main root cause of the popularity of MMCs, since it grants them low switching losses, minimum filter requirements, and scalability to high voltage and power ratings. On the other hand, it poses a significant challenge in terms of EMT. Indeed, the multitude of cascaded SMs in each arm implies that many electrical nodes and semiconductor devices must be evaluated simultaneously during simulation, thereby leading to a high computational burden if conventional EMT simulation tools are adopted. To address this issue, scholars proposed several MMC simulation approaches, most of which rely on the adoption of more simplified SM models [55,79]. Despite paving the way towards compact equivalent MMC arm representations and higher simulation efficiency, these simplified models neglect the switching dynamics within each SM. As a result, these approaches are not suited for thorough simulations of AC/DC networks, which may require the implementation of detailed transistor-level representations of converter submodules.

This PhD thesis focuses on the implementation of a different MMC simulation paradigm based on sub-circuit isomorphism [25,29]. This technique was originally adopted to analyse electronic circuits made up of many structurally identical cells, such as RAMs. If applied to MMCs, this approach exploits the common behaviour shown by the SMs of each arm by dynami-

cally grouping them based on their current working conditions. While simulating, this paradigm selects only a single element for each group. By doing so, the number of nodes and semiconductor devices to be evaluated reduces significantly, thereby leading to simulations that are much faster than those obtained with conventional EMT solvers but just as accurate. Since this approach has general validity, it can be applied to any SM model. Thus, depending on the degree of detail required, the user can flexibly choose a bi-value resistor representation, a more detailed one to analyse switching phenomena within the SMs, or even define a brand new, custom model.

1.4.4 Stability analysis

The small-signal analysis is a useful tool to investigate system stability. For example, it allows establishing if the current operating point of the system is stable or not, and assessing how system stability changes by varying some parameters (e.g., regulators gains).

Many of the methods implemented in the literature to perform this analysis in conventional power systems rely on the fact that the steady-state operating condition of the grid corresponds to an equilibrium point in the DQ0-frame. This holds if this working condition is characterised only by the presence of positive sequence components and the absence of harmonics, which is generally true for traditional networks.

However, the increasing presence of converters (most notably, MMCs) in modern power systems poses some challenges in this context because they might introduce harmonics and negative sequence components. Thus, the steady-state operation of the network no longer translates into an equilibrium point in the DQ0-frame, but rather into a periodic orbit [80]. In the light of the above, conventional approaches to small-signal analysis need to be updated so that they become compatible also with converter-based grids. By doing so, these analyses can be profitably exploited in the design phase of the MMCs to identify the source of possible instability issues and oscillation phenomena [81].

To this aim, scholars have extended some of the conventional approaches to small-signal analysis by resorting to dynamic phasors [82–86] or harmonic state-space (HSS) analysis [87–91]. However, the main disadvantage of both solutions is that the derivation of small-signal models (e.g., admittances) requires either lengthy EMT simulations or some simplifying assumptions (e.g., the DC-side of the MMC is connected to an infinite DC bus[19]) and extensive pen-and-paper computations, which need to be re-

[19] An infinite DC-bus superposes a constant pole-to-pole voltage regardless of grid operating conditions.

peated from scratch whenever new MMC controls need to be analysed.

In this thesis, the MMC admittances are derived with a novel method in the power system field based on the periodic small-signal analysis (PAC) [30, 92]. The term "periodic" means that the small-signal model is time-varying and derived over one period of the large-signal solution of the MMC (in general $1/50$ or $1/60\,\mathrm{Hz}$), obtained in turn through the shooting method (SHM) [93]. Compared to some of the previously mentioned approaches, the main advantage of this method is that it can compute the MMC admittance numerically without needing to explicitly write a small-signal model, putting forward simplifying assumptions or relying on cumbersome EMT simulations. Indeed, this method is directly implemented at the simulator level. To obtain an analytical representation of the MMC admittances, the user can resort to vector fitting (VF) algorithms [94, 95]. Versatility is one of the strong points of the PAC analysis: if a new aspect of the system (e.g., controls or parameters) under analysis changes, the new admittances can be computed simply by running once again the simulations, starting the PAC and, finally, using VF algorithms.

CHAPTER 2

Modular multilevel converter models and simulation approaches

"Remember that all models are wrong; the practical question is how wrong do they have to be not to be useful": this aphorism, generally attributed to the statistician George Box, states that a perfect understanding and description of the complexities of reality is within no one's grasp [96]. Thus, every scientific model has some approximations, whose importance depends on the application where the model is adopted. A good part of engineering revolves around deciding the appropriate level of modelling and knowing under what conditions the chosen model will fail.

The models used to describe MMCs are no exception. As already stated, power system simulators can perform different tasks, such as power flow, stability analyses, RMS, and EMT simulations. For each application, some MMC models are more suitable than others because they reach an optimal trade-off between simulation accuracy and efficiency. For instance, the main focus in PF analyses is the steady-state operation of the grid. MMC models capable of describing and capturing very fast dynamics are not the best choice for this kind of task, since such dynamics are not of interest in PF analyses. Thus, the adoption of these models leads to no substantial

improvement in terms of PF results but rather increases the computational burden. On the contrary, when it comes for instance to EMT simulations, the user should refrain from using too simple models, such as those employed for PF analyses. Since they typically neglect some dynamics to boost simulation speed, their adoption might introduce mathematical artefacts, and lead to misguided conclusions about the actual transient behaviour of the whole power system.

This chapter focuses on models and techniques for the simulation of MMCs based on half-bridge SMs and used in HVDC applications. To begin with, Section 2.1 presents the challenges related to MMCs in this context. The same section describes the main MMC models available in the literature and compares them in terms of fields of applicability and limitations. Then, Section 2.2 explores the topic of isomorphism-based simulation techniques. After describing their original development in FAST-SPICE simulators, the section explains how these approaches can be exploited to efficiently simulate MMCs - one of the main topics of this PhD thesis.

2.1 Literature review of MMC models for transient simulations

The increasing penetration of power electronics converters in electricity networks makes it imperative to ensure that their performance is satisfactory in a wide range of operating conditions. To do so, component, system, and network level studies are commonly carried out during simulations [55, 97]. This practice holds for every converter technology (e.g., diode clamped, flying capacitor, and modular multilevel converter).

Component level studies mainly focus on the early design stage of the converter and the performances of its semiconductors (e.g., voltage and current stresses, conduction and switching losses, and electromagnetic compatibility issues). To carry out such analyses, detailed semiconductor models and small integration time steps are needed because the time of investigation ranges from nano to milliseconds.

On the contrary, the goal of system level studies is evaluating the interactions between the converter and the associated AC power system, whose extension is in this case limited to a few generators and loads. These analyses involve dynamics that can last from milliseconds to several seconds, and allow the validation of, among others, converter controls, filters, and protections.

Finally, network level studies aim at investigating how the converter behaves in a large AC network and affects the electromechanical transients and the steady-state operation of the whole system. As a result, the time in-

terval of interest ranges between seconds and several minutes. Such studies address, for instance, power flow and stability analyses.

It is clear that the most detailed converter and semiconductor models could be adopted in principle for all the abovementioned studies. However, this would result in a high computational burden, especially if simulations last up to several minutes as in network level studies. Indeed, power electronics systems are usually simulated using EMT-type solvers, which rely on the nodal admittance method and adopt a sufficiently short and often fixed integration time step [98, 99]. For instance, in the case of the MMC, the presence of a multitude of SMs in each arm has several implications. First, thousands of IGBTs and diodes must be considered[1], which results in the MMC being described by a rather big nodal admittance matrix $\boldsymbol{G}$. Second, due to the non-linear nature of semiconductor devices, repetitive re-triangularizations of the matrix are required to determine the power system solution at each time step [55, 100]. Third, frequent interpolations are necessary to track the exact switching instants of the semiconductor devices (i.e., the exact moment when they shift from conduction to interdiction operating mode) [101, 102].

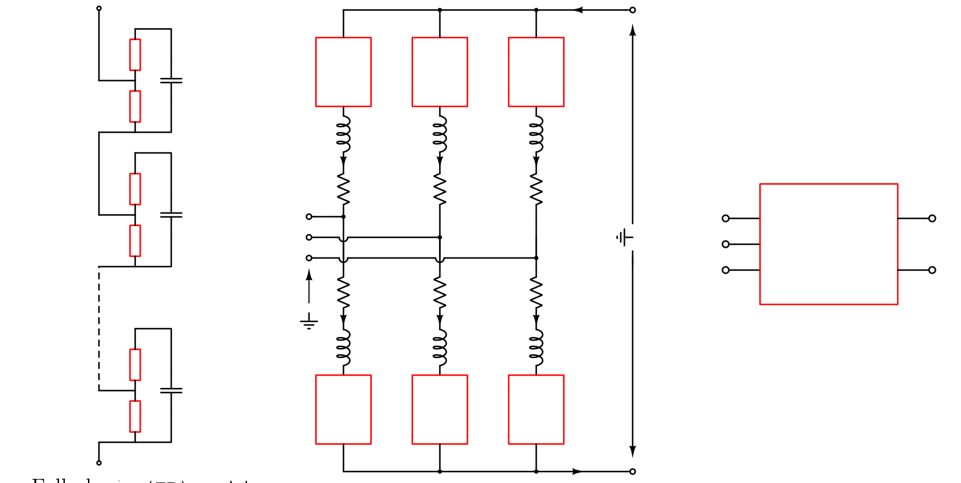
Other converter technologies used in HVDC applications, such as the two-level and the diode clamped converters, suffer from the same problems. In fact, as stated in the previous chapter, each phase leg of these converters comprises stacks of semiconductor devices connected in series to reach voltage ratings compatible with those of the HVDC systems where they are installed. If simulations must retain the behaviour of every single device, the number of variables and equations to be considered increases significantly also for these converters.

To overcome the above simulation efficiency issues, equivalent models need to be adopted. For instance, in the case of the two-level and diode clamped converters, a straightforward way to reduce the computational burden is to merge the series-connected IGBTs and diodes in each leg into an equivalent semiconductor device. This can be done because the components in each stack are associated with the same gate signals, which means that their behaviour is practically the same.[2]

However, when dealing with the simulation of MMCs (and also of cascaded H-bridge converters, which have a similar topology), the above approach is not applicable. Indeed, although the SMs in each arm are con-

[1] Each half-bridge SMs comprises 4 semiconductor devices (i.e., 2 IBGTs and 2 diodes). Considering the MMC in Fig. 1.8, which has N SMs per arm, the total number of these components amounts to $24N = N \times 6 \times 4$ (N SMs per arm, 6 arms, 4 semiconductor devices per SM). For instance, if $N = 200$, this number equals 4800.

[2] If the behaviour of each semiconductor device inside a stack is not of interest, minor differences in their static and dynamic features can be neglected. This justifies that their behaviour is approximately the same.



Full physics (FP) model
Full detailed (FD) model
Bi-value resistor (BVR) model

Thévenin equivalent model (TEM)
Switching function model (SFM)

Average value model (AVM)

Figure 2.1: *The* MMC *models grouped and listed in decreasing order of complexity. The red boxes highlight the sections of the* MMC *that are subject to simplification for each group of models.*

nected in series, their gate signals are different. Thus, the behaviour of each SM is different from one another, which prevents their semiconductor devices from being directly merged into an equivalent circuit.

The increasing popularity of MMCs in HVDC applications has spurred the development of several models, grouped in Fig. 2.1 in decreasing order of complexity and described in detail in the following subsections, which aim at overcoming this simulation issue by implementing different trade-offs between simulation speed and accuracy. Each of them is more suitable than others for component, system, or network level studies. In short, the full physics (FP), full detailed (FD), and bi-value resistor (BVR) models consist of different representations of the semiconductor devices inside each SM that, however, do not alter the overall MMC topology. On the contrary, the Thévenin Equivalent Model (TEM) and Switching Function Model (SFM) lead to a more compact representation of the SMs strings in each MMC arm. Lastly, by using the Average Value Model (AVM), the whole MMC topology is significantly simplified.

As a disclaimer, there is a plethora of MMC representations in the literature: some of them are named differently but present only minor differences, whereas others share the same name but yield different features. Therefore, it is rather difficult to establish a classification of MMC models

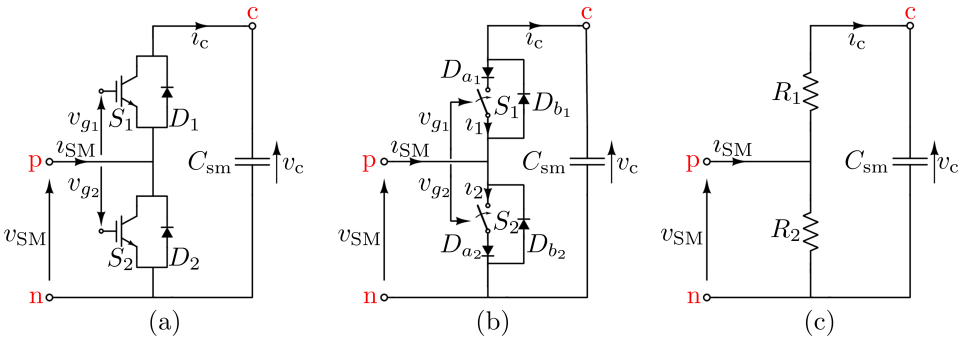


Figure 2.2: *The* SM *schematic of the* FP *(a),* FD *(b), and* BVR *(c) models. The voltages* v_{g_1} *and* v_{g_2} *denote the gate signals of the* IGBT*s. The bypass switch and thyristors of Fig. 1.9(a) were not included in these representations for the sake of simplicity.*

coherent with the whole literature. The main purpose of this review is to outline some core concepts that will allow a better understanding of the key features of the isomorphism-based MMC simulation approach (presented in Section 3) and its main differences with respect to other already developed methods.

2.1.1 Full Physics (FP) model

All the MMC representations described in this chapter stem from the full physics (FP) model, which represents SMs as shown in Fig. 2.2(a). This model retains the highest accuracy, because it describes the semiconductor devices in each SM through detailed, non-linear dynamic representations based either on built-in or macro models [103–106]. In the former case, diodes and IGBTs are described by a set of DAEs implemented in the simulator through dedicated software code, which typically grants better numerical robustness and efficiency. On the contrary, macro models exploit discrete elements already existing in the simulator, such as non-linear controlled sources, diodes, and transistors. These elements are suitably connected to form a sub-circuit whose behaviour at its pins replicates that of the real semiconductor devices.

The FP model is the most suitable one for component level studies. Other than allowing accurate analyses of switching characteristics (e.g., turn-on and turn-off characteristic, transient recovery voltage) and parasitics of the IGBTs and diodes, this model is the only one capable of assessing both conduction and switching losses.

These features, however, come at the cost of a high computational bur-

den due to the multitude of SMs in each arm. In particular, simulation times become even more prohibitive if simulators based on a fixed integration time step ΔT are adopted to analyse fast switching transients inside the SMs. Indeed, values of ΔT in the order of nanoseconds must be employed throughout the whole simulation to observe the behaviour of semiconductors during commutations. This level of modelling is typically not available in power system simulation packages.[3] For this purpose, circuit simulation programs are usually used [61].

If details during switching transients are not of interest, more simplified SMs circuits based on the FD or BVR models can be adopted.

2.1.2 Full Detailed (FD) model

Compared to its FP counterpart, the full detailed (FD) model replaces each valve inside the SMs with an ideal controlled switch and two non-ideal diodes (one in series, the other in anti-parallel) modelled with a $v-i$ driving point characteristic, based either on the semiconductors data sheets or *ad-hoc* measurements. To further reduce the computational burden during simulations, piece-wise linear representations could be adopted instead of smooth driving point characteristics [108].

Figure 2.2(b) depicts the FD SM model. The IGBT gate signals control the open/closed configuration of the corresponding ideal switches (e.g., if the IGBT S_1 is ON, the ideal switch of the same name is closed and open otherwise). The schematic might include a snubber circuit that acts as a surrogate of the dynamic behaviour exhibited by IGBTs and diodes during switching, which otherwise would be lost. In [79], for instance, the snubber circuit is used to mimic the reverse recovery condition. It is worth pointing out that in the real design, however, snubbers play a different role, which is protecting and improving the performance of semiconductor devices (e.g., by limiting peaks and rate of change of current and voltage across them during commutations) [109].

Since in this model switching transients are not of interest, higher integration time steps ΔT can be adopted. In the case of the FP model, each gate signal comprises rising and falling fronts, together with dead-times to prevent cross-conductions. On the contrary, with the FD model, the adoption of values of ΔT higher than nanoseconds implies that these features are no longer relevant. Therefore, gate signal control can be simplified. However, this means that converter losses (most notably, switching losses) cannot be accurately analyzed. On the contrary, conduction losses can still

[3] The standard libraries of simulators such as PSCAD, EMTDC, and EMTP-RV adopt simplified semiconductor models, whose ON and OFF states are associated with bi-value resistors [107].

be evaluated, provided that the $v-\imath$ driving point characteristic of the non-ideal diodes closely matches that of the real semiconductor devices.[4]

This model is the most accurate among those usually available in power system simulators and can be used as a benchmark to validate simpler MMC models. Moreover, it allows analysing converter start-up, normal and abnormal operating conditions (e.g., AC and DC-side faults, as well as those within a single SM), and testing the effectiveness of MMC protection and control systems.

2.1.3 Bi-value resistor (BVR) model

The bi-value resistor (BVR) model [61], depicted in Fig. 2.2(c), reduces the operation of the pairs of semiconductor devices S_1-D_1 and S_2-D_2 to that of two time-varying resistors R_1 and R_2, whose resistance is either small ($\sim \mathrm{m}\Omega$) or high ($\sim \mathrm{M}\Omega$) if one of the elements in each pair is conducting or not, respectively [111]. These values may derive from manufacturers data sheets, and depend on the gate signals and the SM current and voltage.

Figure 2.3 shows a pseudo-code that determines the possible values of R_1 and R_2 at a given time t if a fixed time step ΔT is used.[5] In the inserted and bypassed operating modes, based on the sign of the current $\imath_{SM}$, either the IGBT in the ON-state or its free-wheeling diode conducts. Thus, R_1 and R_2 are easy to determine. On the contrary, in the blocked state these values are less straightforward to derive, since the SM behaves as an uncontrolled diode bridge. In this case, depending on the current and the voltages of the SM and its capacitor, the diode D_1, D_2, or none of them conducts.

The BVR representation inherits the accuracy limitations and fields of application of the FD one. It has a reduced computational burden because it neglects any switching dynamic whatsoever inside the SMs. However, it is important to note that the adoption of the BVR model does not completely solve the MMC-related simulation issues. To better clarify this statement, consider the schematic in Fig. 2.4, which depicts a string of N SMs inside an MMC arm when the BVR model is adopted. Overall, the number of nodes in one arm amounts to $2N + 1$, where N is in the order of hundreds in HVDC applications. Despite the adoption of simplified SM models such as the BVR one, the presence of 6 MMC arms and the multitude of SMs in each of them still results in a big MMC nodal admittance matrix $\boldsymbol{G}$. As

[4] The interested reader can refer to [110] for conduction and switching losses estimation methods of VSCs used in HVDC applications, such as MMCs.

[5] It is worth pointing out that the pseudo-code in Fig. 2.3, taken from Table I of [79], does not describe every SM operating condition. Indeed, the case of SM failure (i.e., both IGBTs are mistakenly ON or an internal fault occurs) is not included.

Values of R_1 and R_2 of a generic SM at time t
if S_1 **is ON** && S_2 **is OFF (i.e., SM inserted state)**
$R_1 = R_{\mathrm{ON}}, R_2 = R_{\mathrm{OFF}}$
else if S_1 **is OFF** && S_2 **is ON (i.e., SM bypassed state)**
$R_1 = R_{\mathrm{OFF}}, R_2 = R_{\mathrm{ON}}$
else if S_1 && S_2 **are OFF(i.e., SM blocked state)**
if $\imath_{\mathrm{SM}}(t) > 0$ && $v_{\mathrm{SM}}(t - \Delta T) > v_c(t - \Delta T)$ **(i.e.,** D_1 **conducts)**
$R_1 = R_{\mathrm{ON}}, R_2 = R_{\mathrm{OFF}}$
else if $\imath_{\mathrm{SM}}(t) < 0$ && $v_{\mathrm{SM}}(t - \Delta T) < 0$ **(i.e.,** D_2 **conducts)**
$R_1 = R_{\mathrm{OFF}}, R_2 = R_{\mathrm{ON}}$
else (i.e., no diode is conducting)
$R_1 = R_{\mathrm{OFF}}, R_2 = R_{\mathrm{OFF}}$
end
end

Figure 2.3: *A pseudo-code that determines the values of R_1 and R_2 of a generic* SM *at a given time t with the* BVR *representation. The different "if/else" statements in the code retrace the operating states listed in Table 1.7.*

already stated, the matrix needs to be LU-factorized at a large number of time steps to solve the circuit. The computational effort of this operation has an almost quadratic dependence on the size of $\boldsymbol{G}$ [112, 113], which constitutes the main bottleneck for the simulations of MMCs. This issue can only be partially mitigated by exploiting the fact that the matrix is sparse [61]. In the light of the above, MMC simulations based on FD, FP, and BVR models are characterised by a CPU time that varies super-linearly with the number of SMs per arm[6], which results in a low simulation efficiency.

To overcome this problem, other MMC representations are needed. In this regard, as shown in the following, the BVR model paves the way to a more efficient MMC representation, where the stack of cascading SMs in each arm can be grouped compactly through a linear, time-varying Thévenin equivalent circuit.

2.1.4 Thévenin equivalent model (TEM)

The model proposed in [100], hereafter referred to in this thesis as Thévenin Equivalent Model (TEM), is based on an idealized representation of switches as bi-value resistors. It grants a significant reduction of the computational burden when simulating grids comprising MMCs because it replaces the string of cascaded SMs in each arm with an equivalent circuit.

[6]For instance, this trend is visible in the CPU results of the "Model 1" row in Table II of [79], which adopts the FD representation.

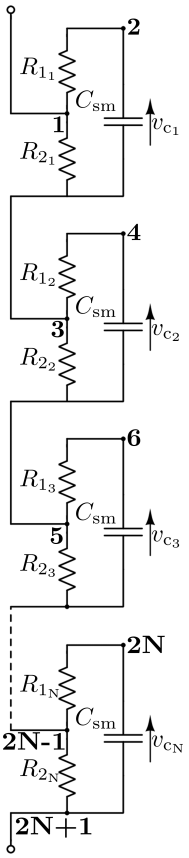


Figure 2.4: *Schematic of a string of N* SM*s inside one* MMC *arm when the* BVR *model is adopted. The labels in bold denote nodes numbering.*

To achieve this boost in simulation efficiency, the model in [100] relies on the adoption of a fixed integration time step ΔT and the trapezoidal integration rule. By doing so, the differential constitutive equation of the capacitor in each SM (see Fig. 2.5(a)) can be substituted through the mathematical steps shown in Eq. (2.1) with an (algebraic) Thévenin equivalent, also known in the literature as *companion model*. The resulting circuit comprises a resistor $R_{\mathrm{c_{eq}}}$ in series with a voltage source $v_{\mathrm{c_{eq}}}$, whose value at a given time t depends on the capacitor voltage and current at the previous time step (i.e., $i_{\mathrm{c}}\left(t-\Delta T\right)$ and $v_{\mathrm{c}}\left(t-\Delta T\right)$).

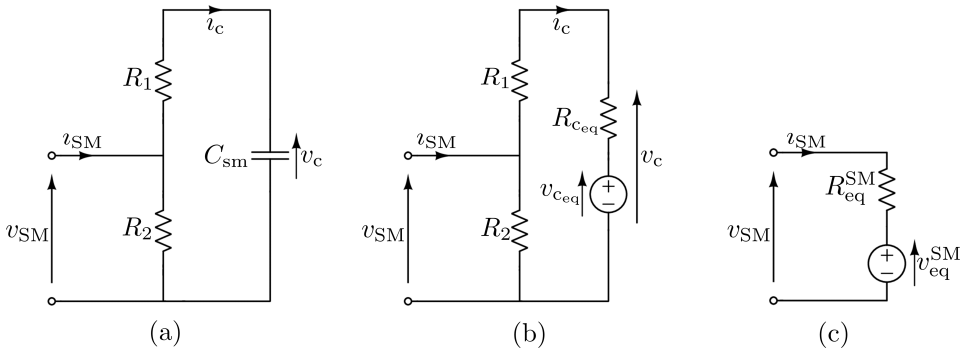


Figure 2.5: *Simplification process of the* SM *schematic based on the* TEM.

$$
\begin{aligned}
i_{\mathrm{c}} &= C_{\mathrm{sm}} \frac{dv_{\mathrm{c}}}{dt} \\
\int_{t-\Delta T}^{t} dv_{\mathrm{c}} &= \int_{t-\Delta T}^{t} \frac{1}{C_{\mathrm{sm}}} i_{\mathrm{c}}\, dt \\
v_{\mathrm{c}}(t) - v_{\mathrm{c}}\left(t-\Delta T\right) &\approx \underbrace{\frac{\Delta T}{2C_{\mathrm{sm}}}\left(i_{\mathrm{c}}(t) + i_{\mathrm{c}}\left(t-\Delta T\right)\right)}_{\text{Trapezoidal integration rule}} \\
v_{\mathrm{c}}(t) &= \underbrace{\frac{\Delta T}{2C_{\mathrm{sm}}}}_{R_{\mathrm{c_{eq}}}} i_{\mathrm{c}}(t) + \underbrace{v_{\mathrm{c}}\left(t-\Delta T\right) + \frac{\Delta T}{2C_{\mathrm{sm}}} i_{\mathrm{c}}\left(t-\Delta T\right)}_{v_{\mathrm{c_{eq}}}}.
\end{aligned}
\tag{2.1}
$$

In the light of the above, the half-bridge SM circuit in Fig. 2.5(a) can be redrawn as that shown in Fig. 2.5(b). By deriving the Thévenin equivalent circuit at the pins of each SM, this circuit can be further simplified, thereby leading to that in Fig. 2.5(c). Simple calculations demonstrate that the equivalent resistance $R_{\mathrm{eq}}^{\mathrm{SM}}$ and voltage source $v_{\mathrm{eq}}^{\mathrm{SM}}$ amount to

$$
\begin{aligned}
R_{\mathrm{eq}}^{\mathrm{SM}} &= \frac{R_2\left(R_1 + R_{\mathrm{c_{eq}}}\right)}{R_1 + R_2 + R_{\mathrm{c_{eq}}}} \\
v_{\mathrm{eq}}^{\mathrm{SM}} &= v_{\mathrm{c_{eq}}} \frac{R_2}{R_1 + R_2 + R_{\mathrm{c_{eq}}}}.
\end{aligned}
\tag{2.2}
$$

The steps carried out so far were aimed at simplifying the structure of a single SM. To simplify that of a cascaded SM string (referred to in [100] as Multi-Valve (MV)), the model exploits the fact that the N SMs in each arm

are connected in series and, thus, flown by the same current. Therefore, as shown in Eq. (2.3), the terms $R_{\mathrm{eq}}^{\mathrm{SM}}$ and $v_{\mathrm{eq}}^{\mathrm{SM}}$ of each SM in a given arm can be summed, thereby leading to

$$\begin{aligned} R_{\mathrm{eq}}^{\mathrm{MV}} &= \sum_{n=1}^{N} R_{\mathrm{eq_n}}^{\mathrm{SM}} \\ v_{\mathrm{eq}}^{\mathrm{MV}} &= \sum_{n=1}^{N} v_{\mathrm{eq_n}}^{\mathrm{SM}} . \end{aligned} \tag{2.3}$$

Equations (2.1)-(2.3) lead to each arm being simplified step by step as outlined in Fig. 2.6(a-c). Thus, the TEM is advantageous because it grants a more compact representation of each arm: regardless of the number N of SMs in each arm, the SM string in Fig. 2.6(c) is characterised by three nodes. This number could be reduced to two by transforming the Thévenin equivalent circuit in Fig. 2.6(c) into a Norton one, as shown in Fig. 2.6(d). In contrast, the original schematic in Fig. 2.6(a) - obtained with the BVR model and no further simplifications - comprises $2N + 1$ nodes.

Therefore, by resorting to the TEM, the generic MMC schematic in Fig. 1.8 becomes the one in Fig. 2.7. During each time step, the derivation of this equivalent circuit requires to follow two steps for the upper and lower arms of every phase leg. First, the pseudo-code of Fig. 2.3 must be executed to determine the values of R_1 and R_2 of each SM. Then, the values of $R_{\mathrm{eq}}^{\mathrm{MV}}$ and $v_{\mathrm{eq}}^{\mathrm{MV}}$ of every arm are computed with Eqs. (2.1)-(2.3).

It is important to underline a marked difference between the BVR-based representation and the TEM. In the first case, a big matrix is re-factorized at each time step to determine every state and algebraic variable of the system, including those internal to the MMC. On the contrary, the TEM relies on Eqs. (2.1)-(2.3) to simplify the MMC circuit and obtain a smaller nodal admittance matrix. After deriving the network solution at a given time step, other equations (shown in the following) allow keeping track of the individual evolution of each SM, which otherwise would be lost due to the simplification process.

The difference highlighted above has some implications. To begin with, the TEM allows validating all MMC protections and controls, including Capacitor voltage Balancing Algorithms (CBAs). Although the representation in Fig. 2.7 loses the individual behaviour of each SM, their capacitor voltages (i.e., the inputs of CBAs) can still be recorded over time through Eq. (2.4). These equations, which are hard-coded in the simulator and hold for a generic SM, can be derived by analysing Fig. 2.5(b) and exploiting

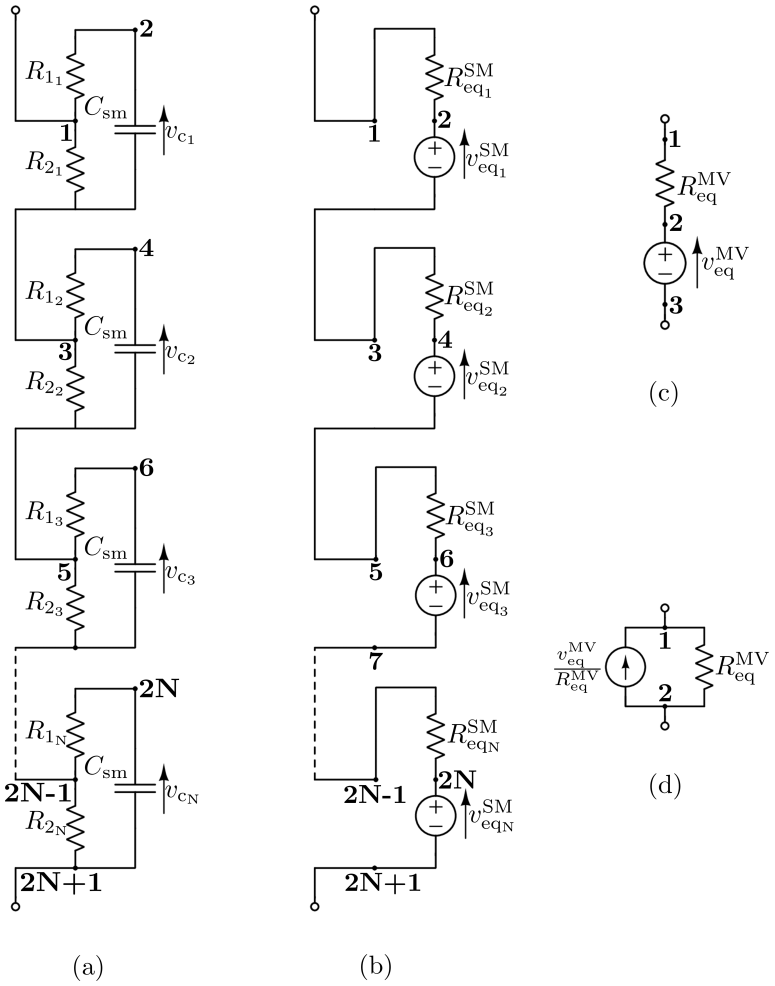


Figure 2.6: *The simplification process of the* MMC *arm schematic based on the* TEM. *The labels in bold denote nodes numbering.*

Eq. (2.1).

$$\begin{aligned} i_{\mathrm{c}}(t) &= \frac{R_2 i_{\mathrm{SM}}(t) - v_{\mathrm{c_{eq}}}(t - \Delta T)}{R_1 + R_2 + R_{\mathrm{c_{eq}}}} \\ v_{\mathrm{c}}(t) &= R_{\mathrm{c_{eq}}} i_{\mathrm{c}}(t) + v_{\mathrm{c_{eq}}} \end{aligned} \tag{2.4}$$

The second implication is that the CPU time related to the TEM is not quadratically dependent on the number of SMs per arm N, but rather just linearly-dependent. As already stated, the TEM leads to an MMC equivalent circuit whose number of nodes is independent of N. This results in

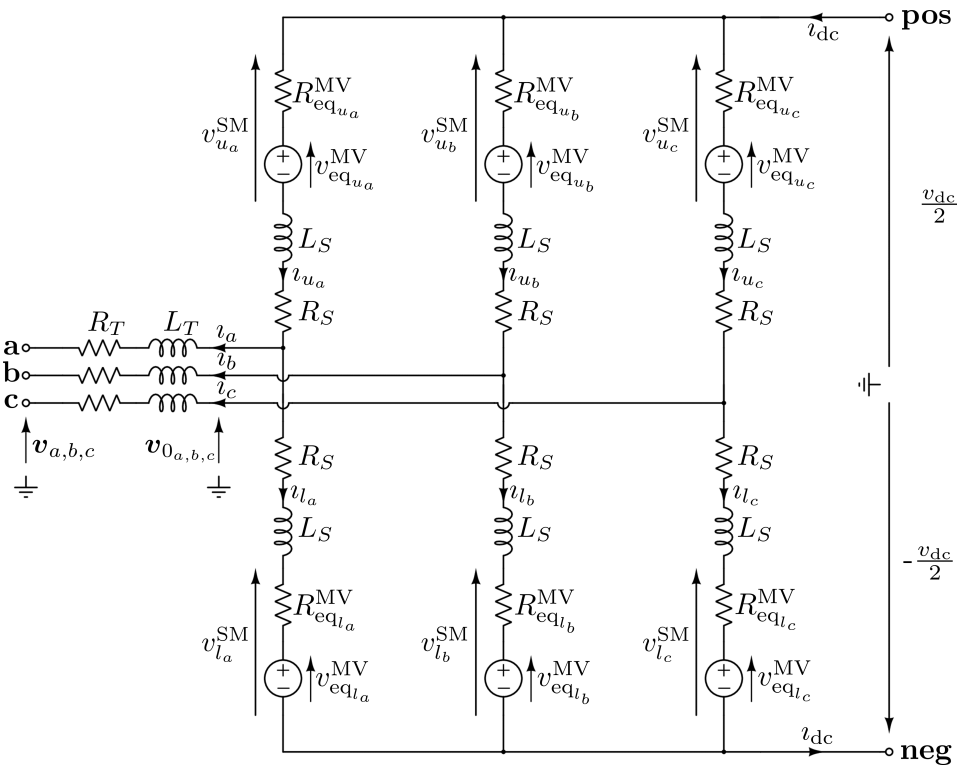


Figure 2.7: *Simplified* MMC *schematic based on the* TEM.

a constant computational burden associated with matrix re-factorizations. However, this does not explain the linear dependency on N of the CPU time. Such a trend is due to different reasons. First, as N increases, so does the switching activity of the MMC, that is, the number of threshold crossings per period shown in Fig. 1.16. If simulators based on a fixed time step ΔT are adopted, this parameter must be reduced accordingly to better detect these crossings, thereby leading to proportionally higher simulation times. Nonetheless, even if a fixed and sufficiently low ΔT is used during a set of simulations characterised by different values of N, a linear increase in CPU time would still be witnessed. This is because of the presence of Capacitor voltage Balancing Algorithms (CBAs), which require sorting the SM capacitor voltages. Since these algorithms are run at every threshold crossing, the number of times they are executed (and, thus, their computational overhead) rises linearly with N.[7]

[7]For instance, this trend is visible in the curve labelled "EIM" in Fig. 14 of [55] and the "Model 2" row in Table II of [79], associated with a TEM similar to that shown in this section. Both of them adopt a fixed time step

To sum up, in comparison with the BVR representation, the TEM enhances simulation efficiency while maintaining accuracy. In addition, this model lends itself to parallel computation [114, 115]: at every time step, Eqs. (2.1)-(2.4) could be solved for each arm in separate threads. In the light of the above, the TEM is an excellent candidate for real-time simulation of MMCs through CPUs and Field-Programmable Gate Arrays (FPGAs) - a topic that has become increasingly popular over the past few years [116–119].

Like the BVR model, the TEM allows studying both normal and all abnormal operating conditions (e.g., AC and DC-side faults) except for the failure of SMs (i.e., both gate signals are ON or an internal fault occurs). This is because the TEM relies on the BVR representation, which cannot replicate this behaviour.[8] On the contrary, the blocked condition of SMs can still be correctly analysed with the TEM because the pseudo-code in Fig. 2.3 takes this operating state into account.[9]

Lastly, it is important to note that the simplifications attained with the TEM are possible because the SMs based on the BVR model are linear and time-varying. Only in this case the stack of SMs in each arm can be grouped compactly through a linear, time-varying Thévenin equivalent circuit. The same approach cannot be applied to SMs based on the FD and FP models because of their non-linearities. In fact, the Thévenin equivalent exists only for linear time-varying circuits. In contrast, as described in Section 2.2, a key feature of the isomorphism-based approach is its capability of increasing the MMC simulation efficiency regardless of the SM model adopted, be it linear or not.

2.1.5 Switching function model (SFM)

The MMC Switching Function Models (SFMs) further simplify the operation of SMs: instead of bi-value resistors, ideal switches are used to model the semiconductor devices in each SM valve. As a result, by referring to

$\Delta T = 10$ µs regardless of the number of SMs.

[8] This problem is addressed in [120] as follows. If a SM string in one arm contains a faulty SM, its equivalent circuit is made up of three parts. In the middle, the faulty SM (based on the FD or FP models) is connected. The remaining two parts comprise a Thévenin equivalent circuit, which group the SMs (based on the BVR model) above and below the faulty one. The interested reader can refer to Fig. 4 of [120] (and its related text) for more information about the implementation of this circuit. The paper also improves the simulation speed of the TEM by adopting a different sorting algorithm and integration rule to generate the companion model of the SM capacitors.

[9] An issue of the pseudo-code in Fig. 2.3 is that it requires an iterative approach such as that outlined in Fig. 5 of [79] to track the time instants when diodes D_1 and D_2 begin or stop conducting during SM blocked operation to avoid numerical oscillations. To circumvent this need, the authors of [121] resort to a different equivalent circuit from that shown in Fig. 2.7 to simulate the blocking state. By doing so, a simpler pseudo-code can be adopted.

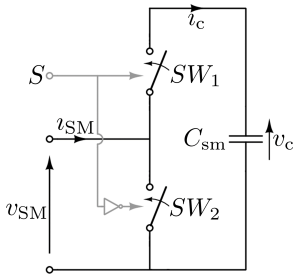


Figure 2.8: SM *representation based on the* SFM.

Fig. 2.8, the voltage and current of a SM and its corresponding capacitor are related to one another by the following equations

$$\begin{aligned} i_{\mathrm{c}} &= S\, i_{\mathrm{SM}} \\ v_{\mathrm{SM}} &= S\, v_{\mathrm{c}}\,, \end{aligned} \tag{2.5}$$

where S is the SM binary switching function provided by the modulation technique described in Section 1.3.4.2, which gives the name to this model. The variable S is equal to 1 when the SM is inserted (i.e., SW_1 and SW_2 are closed and open, respectively) and 0 when bypassed (i.e., SW_1 and SW_2 are open and closed, respectively). These equations refer to the normal operating conditions of the SMs. As shown in the following, *ad hoc* equivalent circuits are adopted to mimic the behaviour of each arm during blocked conditions, while the failure of SMs is not covered.

Another variable often used in SFMs is the *arm* switching function s, which is defined as

$$s = \frac{1}{N}\sum_{n=1}^{N} S_n\,, \tag{2.6}$$

where S_n is the binary function associated with the $n-th$ SM and N is the overall number of SMs in one arm. During normal operating conditions, s ranges between 0 and 1 (i.e., all SMs are bypassed and inserted, respectively). In particular, s changes in a discrete manner at each crossing of the modulation scheme (i.e., whenever the voltage reference waveform crosses one of the thresholds in Fig. 1.16).

There are different versions of the SFM. The simplest one, referred to in this work as *type 1* SFM, assumes that all SM capacitor voltages are always perfectly balanced [79, 122, 123], that is

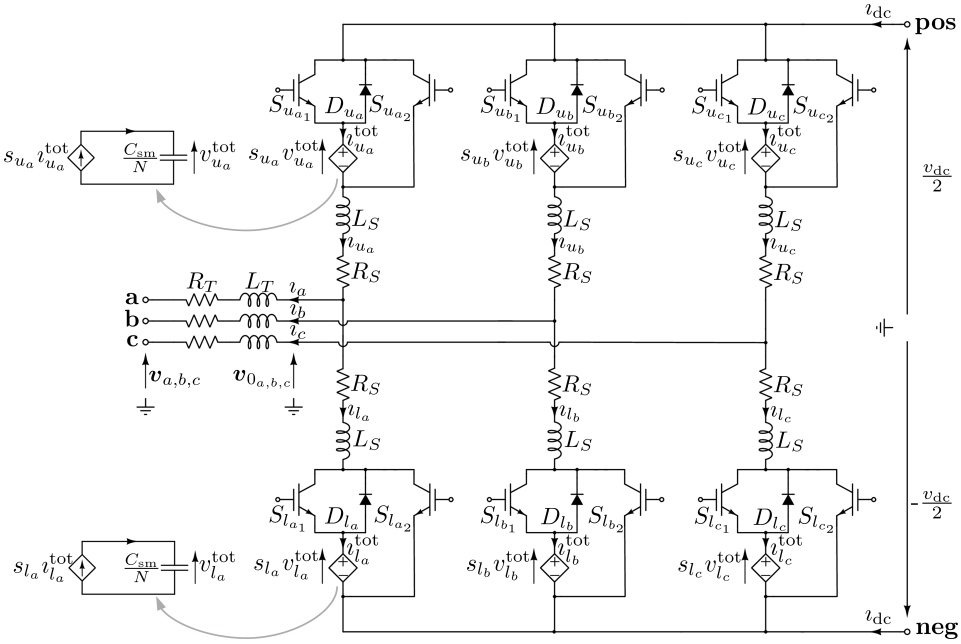


Figure 2.9: *Type 1* SFM *of the* MMC. *For the sake of simplicity, the figure depicts the capacitor and controlled current sources associated with the upper and lower arm of phase a only. Analogous circuits are actually included in the other phase legs of the* MMC.

$$v_{\rm c_1} = v_{\rm c_2} = ... = \frac{1}{N}\sum_{n=1}^{N} v_{\rm c_n} = \frac{v_{\rm c}^{\rm tot}}{N}\,. \tag{2.7}$$

The accuracy of this assumption increases by including more SMs in each arm and reducing capacitor voltage ripples [79].

In this case, as shown in Fig. 2.9, each SM string is replaced with an equivalent circuit, whose diodes and IGBTs are described by a simple representation based on an ON-state and OFF-state resistance [107]. The behaviour of the equivalent circuit can be explained by selecting, for instance, the upper arm of phase a (whose variables and components are denoted by the subscript $_{u_a}$) - analogous considerations apply to the other arms.

In normal operating conditions, the IGBTs $S_{u_{a_1}}$ and $S_{u_{a_2}}$ are respectively ON and OFF. Thus, the current $\imath_{u_a}$ flows through a voltage controlled source (i.e., $i_{u_a}^{\rm tot} = \imath_{u_a}$) and, depending on its sign, through either $S_{u_{a_1}}$ or D_{u_a}. The voltage across the source amounts to $s_{u_a} v_{u_a}^{\rm tot}$, with s_{u_a} and $v_{u_a}^{\rm tot}$ being respectively the arm switching function and the voltage of a capacitor $\frac{C_{\rm sm}}{N}$

(this value is justified later). In turn, this latter component is connected in series with a controlled current source $s_{u_a} \imath_{u_a}^{\mathrm{tot}}$.

The controlled sources are a ploy to simulate the behaviour of all SMs in one arm by merging all their capacitors into a single one. On the one hand, the controlled current sources mirror the charge and discharge of the SM capacitors. On the other hand, the controlled voltage sources mimic the fact that, as the insertion indices vary, so does the voltage $s_{u_a} v_{u_a}^{\mathrm{tot}}$ across the SM strings because the number of SMs inserted into the arms changes.

To prove that the value of the capacitor $\frac{C_{\mathrm{sm}}}{N}$ is correct, it is useful to compute the equivalent capacitance $C_{u_{a_{\mathrm{eq}}}}$ seen from the upper arm of phase a, which can be derived as

$$\imath_{c_{u_a}} = s_{u_a} \imath_{u_a} = \frac{C_{\mathrm{sm}}}{N} \frac{dv_{u_a}^{\mathrm{tot}}}{dt} \rightarrow \imath_{u_a} = \underbrace{\frac{C_{\mathrm{sm}}}{s_{u_a} N}}_{C_{u_{a_{\mathrm{eq}}}}} \frac{dv_{u_a}^{\mathrm{tot}}}{dt} . \tag{2.8}$$

For instance, suppose that at a given time instant all N SMs in the upper arm of phase a are ON (i.e., $S = 1$ for each of them) so that $s_{u_a} = 1$. Thus, the equivalent capacitance amounts to $C_{u_{a_{\mathrm{eq}}}} = \frac{C_{\mathrm{sm}}}{N}$. Indeed, if all SM are inserted, also all their capacitances are in series. Therefore, the equivalent capacitance is obtained by dividing C_{sm} (i.e., that of a single SM) by N. The above considerations justify the adoption in the first place of capacitors $\frac{C_{\mathrm{sm}}}{N}$ in Fig. 2.9. During normal operation, s_{u_a} and, thus, the equivalent capacitance $C_{u_{a_{\mathrm{eq}}}}$ vary at each threshold crossing of the modulation technique adopted in the MMC control scheme. If $s_{u_a} = 0$, $s_{u_a} v_{u_a}^{\mathrm{tot}}$ and $s_{u_a} \imath_{u_a}^{\mathrm{tot}}$ are null because all SMs are bypassed and their capacitors cannot charge.

If the MMC enters the blocked operating condition, all the capacitors inside the SMs can charge but not discharge. To simulate this behaviour, the IGBTs $S_{u_{a_1}}$ and $S_{u_{a_2}}$ are respectively OFF and ON. If $\imath_{u_a}$ is positive, the diode D_{u_a} conducts. Therefore, $\imath_{u_a}^{\mathrm{tot}} = \imath_{u_a} > 0$ and all SMs capacitors are charging by letting $s_{u_a} = 1$. Otherwise, the IGBT $S_{u_{a_2}}$ conducts and all capacitors neither charge nor discharge because $\imath_{u_a}^{\mathrm{tot}} = 0$.

This model can be used to analyse all the protections and controls except for Capacitor voltage Balancing Algorithms (CBAs), which are absent in this case because a perfect voltage balance is assumed. Moreover, since the individual behaviour of each SM is lost, faults inside one SM cannot be studied.[10] Normal and other abnormal operating conditions can still be analysed with the SFM. To take into account the resistance of the SMs replaced by

[10]This issue could be solved by using the model shown in [124]: the user can adopt several SM models (half-bridge, full-bridge, etc.) and decide during simulation to represent each arm with a SFM or a more detailed one. However, when the former model is adopted, the individual behaviour of each SM is once again lost.

ideal switches (and, thus, conduction losses), the ON-state resistance of the IBGTs and diodes in Fig. 2.9 could be increased accordingly.[11]

It is important to point out that, in comparison with the TEM, the computational burden of this SFM is basically constant regardless of the number of SMs in one arm.[12] This feature results from the fact that (i) the equivalent circuit is the same independently from the number of SMs in each arm (i.e., the MMC nodal admittance matrix has a constant size) and (ii) the linear overhead resulting from capacitor voltage sorting - incurred when adopting the TEM - is in this case absent because no CBA is adopted.

The schematic illustrated in Fig. 2.10 shows a slightly different version of the SFM, referred to as *type 2* SFM. It retains the individual behaviour of each SM capacitor [55, 122, 125]. In fact, as shown in the grey boxes in Fig. 2.10 for the upper and lower arm of phase a (analogous computations are carried out for the other phase legs), the time evolution of each capacitor voltage is recorded, starting from an initial value $v_{\mathrm{c}_{j,k}}^{\mathrm{init}}$ $(j \in \{u, l\})$. As a consequence, contrary to the scheme depicted in Fig. 2.9, this SFM version also allows testing different CBAs. However, the adoption of such a model leads to CPU times that increase linearly with the number of SMs, because the previously mentioned overhead due to voltage sorting algorithms is reintroduced.[13]

Another model, which is used in Section 4.4, is shown in Fig. 2.11 and referred as to *type 3* SFM. With respect to Fig. 2.9, the only difference is that the variable controlling the dependent sources is no longer the arm switching function s, but rather the modulation index m. For each arm $(j \in \{u, l\}$ and $k \in \{a, b, c\})$, this variable is defined as

$$m_{j_k} = \min\left(\max\left(0, \frac{v_{j_k}^{\mathrm{SM,ref}} N}{v_{\mathrm{dc}}}\right), 1\right) \tag{2.9}$$

In case of blocked operating conditions, m_{j_k} is equal to 1.

While the arm switching function s changes in a discrete manner at each threshold crossing, the modulation index m, despite still being bounded between 0 and 1, varies continuously. This implies that the voltages of the SM strings in each arm vary smoothly as well. Another consequence is that, contrary to the *type 1* SFM, this model does not allow examining the efficiency of modulation techniques such as the Nearest Level Modu-

[11] Alternatively, resistors can be added to each arm of the equivalent MMC circuit, as shown in Fig.7 of [79].

[12] For instance, the CPU results of the "Model 3" row in Table II of [79] and the "Continuous model" column of Table IV in [123], which adopt a SFM representation analogous to that shown in Fig. 2.9, confirm this tendency.

[13] For example, this trend is visible in the curve labelled "SFM" in Fig. 14 of [55], associated with a SFM similar to that shown in Fig. 2.10.

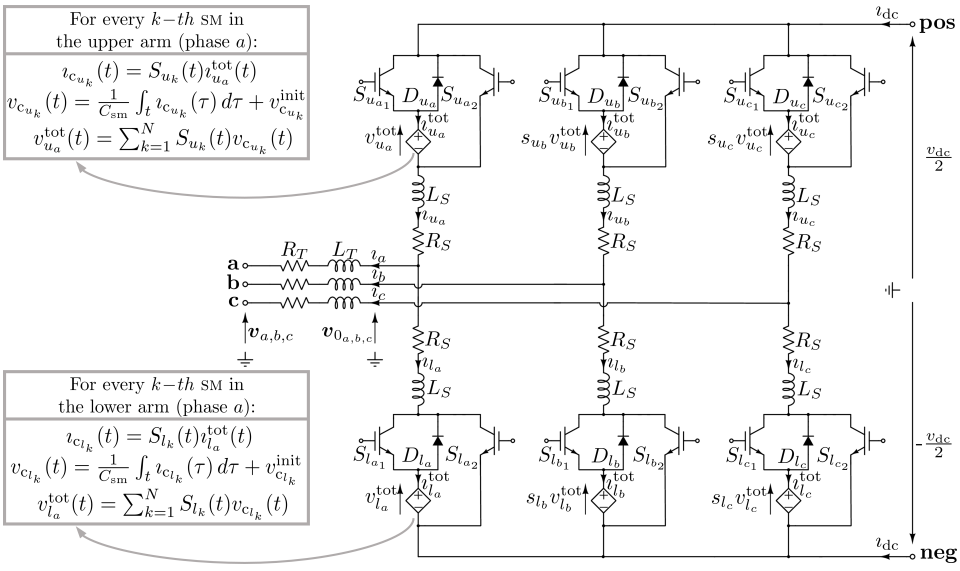


Figure 2.10: *Type 2* SFM *of the* MMC. *For the sake of simplicity, the grey boxes associated to the upper and lower arms of the phase legs* b *and* c *are not shown.*

lation (NLM). On the other hand, the computational burden incurred while simulating this MMC model is lower.

It is worth pointing out that the *type 3* SFM described here is referred to in [122] as *Average*. Perhaps this is because, despite sharing a similar topology with the *type 1* and *type 2* SFMs, in this model the concept of switching function is completely lost. Thus, based on the work in [122], this model would need to be placed in the next section, which deals with the Average Value Models (AVMs) of MMCs. After reading the next section, however, the reader might notice that the *type 3* SFM shares similar traits with both the AVMs and the other SFMs representations. Yet again, as mentioned at the beginning of this chapter, it is difficult to establish a classification of MMC models coherent with the whole literature.

2.1.6 Average value model (AVM)

Average Value Models (AVMs) can be clustered in two types, which in this thesis are referred to as discrete and continuous [55, 61, 79, 108]. In general, both model types neglect the individual behaviour of each SM and significantly simplify the MMC topology through the adoption of controlled voltage and current sources. These representations owe their name to the fact that they disregard voltage and current ripples given by SMs commuta-

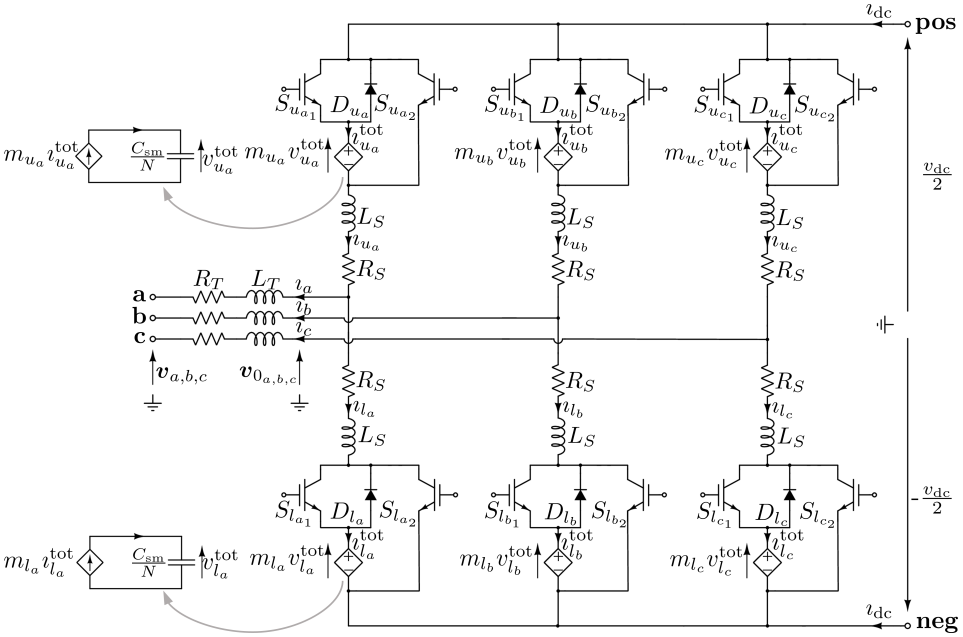


Figure 2.11: *Type 3* SFM *of the* MMC. *For the sake of simplicity, the figure depicts the capacitor and controlled current sources associated to the upper and lower arm of phase a only. Analogous circuits are actually included in the other phase legs of the* MMC.

tions, thereby leading to waveforms that are in a sense an *average* of those obtained with more detailed models (e.g., the FD one).

The AVM relies on two assumptions. First, the SM capacitor voltages are always perfectly balanced. Second, considering once again Fig. 1.8, the voltages of the upper and lower arm SMs strings in each phase leg are such that $v_{l_k}^{\rm SM} + v_{u_k}^{\rm SM} = v_{\rm dc}$. According to Eq. (1.20) and supposing that $R_S \approx 0$, this implies that the current $\imath_{{\rm z}_k}$ does not vary. Since $\imath_{{\rm z}_k} = \frac{\imath_{\rm dc}}{3} + \imath_{{\rm circ}_k}$, the assumptions above result in the suppression of the circulating current $\imath_{{\rm circ}_k}$. Thus, no control scheme like that shown in Fig. 1.15 needs to be adopted.

Figure 2.12 depicts the structure of a discrete AVM. Compared to the original circuit in Fig. 1.8, here the MMC is divided into two parts, one in the AC and the other in the DC side. In the former, the SMs strings in each arm are replaced with controlled voltage sources, which derive from the MMC control scheme in the following way. As shown in Fig. 1.12, the MMC upper level control determines the value of the voltage $u_k = \frac{1}{2}\left(v_{l_k}^{\rm SM} - v_{u_k}^{\rm SM}\right)$ (see Eq. (1.2)), which corresponds to a given reference voltage across the upper and lower SMs strings $v_{u_k}^{\rm SM,ref}$ and $v_{l_k}^{\rm SM,ref}$. In real applications, these

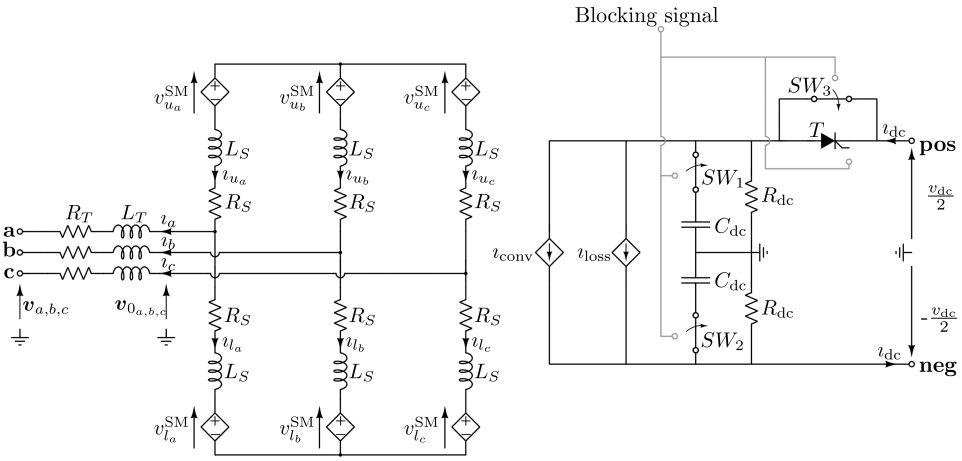


Figure 2.12: *Discrete* AVM *of the* MMC.

values would be the output of a circulating current suppression scheme (see Fig. 1.15). However, as previously mentioned, this control is not considered in the AVM. Therefore, a different approach is adopted. By exploiting the fact that $u_k = \frac{1}{2}\left(v_{l_k}^{\mathrm{SM}} - v_{u_k}^{\mathrm{SM}}\right)$ and $v_{l_k}^{\mathrm{SM}} + v_{u_k}^{\mathrm{SM}} = v_{\mathrm{dc}}$, the terms $v_{u_k}^{\mathrm{SM,ref}}$ and $v_{l_k}^{\mathrm{SM,ref}}$ can be derived as

$$\begin{aligned} v_{u_k}^{\mathrm{SM,ref}} &= -u_k^{\mathrm{ref}} + \frac{v_{\mathrm{dc}}}{2} \\ v_{l_k}^{\mathrm{SM,ref}} &= +u_k^{\mathrm{ref}} + \frac{v_{\mathrm{dc}}}{2}\,. \end{aligned} \tag{2.10}$$

These reference values are the input of a modulation block, which converts them into specific insertion indices for each MMC arm and, in turn, voltage values for the controlled voltage sources in Fig. 2.12. To better clarify this statement, suppose that the number of SMs in each arm is N and that at a given time the modulation block commands the insertion of $\hat{N}$ SMs in one arm. Since SM capacitor voltages are assumed to be perfectly balanced, the voltage of the SM string in that arm amounts to $\hat{N}\frac{v_{\mathrm{dc}}}{N}$, which is mirrored by its corresponding voltage controlled source. During operation, these voltages change whenever the values of $v_{u_k}^{\mathrm{SM,ref}}$ or $v_{l_k}^{\mathrm{SM,ref}}$ cross a threshold in the modulation scheme. During each crossing, the voltages will vary of a quantity equal to $\pm\frac{v_{\mathrm{dc}}}{N}$, hence the name *discrete* AVM.

For what concerns the DC-side of Fig. 2.12, the controlled current sources implement the following power balance between the AC and DC side of the converter

$$\sum_{k\in\{a,b,c\}} u_k \imath_k = v_{\mathrm{dc}} \imath_{\mathrm{dc}} - P_{\mathrm{loss}}\,, \tag{2.11}$$

where P_{loss} are the converter losses. The current controlled sources $\imath_{\mathrm{conv}}$ and $\imath_{\mathrm{loss}}$ can be obtained as follows by isolating the $\imath_{\mathrm{dc}}$ term

$$\imath_{\mathrm{dc}} = \underbrace{\frac{\sum_{k\in\{a,b,c\}} u_k \imath_k}{v_{\mathrm{dc}}}}_{\imath_{\mathrm{conv}}} + \underbrace{\frac{P_{\mathrm{loss}}}{v_{\mathrm{dc}}}}_{\imath_{\mathrm{loss}}}\,. \tag{2.12}$$

The literature proposes several approaches to model converter losses [69, 110]. In [61], for instance, $P_{\mathrm{loss}} = R\imath_{\mathrm{conv}}^2$, with R associated with switching and conduction losses. By doing so, the losses considered are only those dependent on the DC-side current. As shown in Fig. 2.12, two resistors R_{dc} could be connected in parallel to the controlled current sources to consider also losses depending on the pole-to-pole DC-side voltage.

The couple of capacitors C_{dc} in Fig. 2.12 represent those of the inserted SMs in each arm. The value of their capacitance can be obtained by using the energy conservation principle. In other words, the sum of the energy stored inside the inserted SM capacitors in each of the six MMC arms must be equal to that associated with the two capacitors C_{dc}, each of which sustains the pole-to-ground voltage $\frac{v_{\mathrm{dc}}}{2}$. This results in the following equality:

$$6\sum_{i=1}^{N} \frac{1}{2} C_{\mathrm{sm}} v_{c_i}^2 = \frac{1}{2} C_{\mathrm{dc}} \left(\frac{v_{\mathrm{dc}}}{2}\right)^2 + \frac{1}{2} C_{\mathrm{dc}} \left(\frac{v_{\mathrm{dc}}}{2}\right)^2 = \frac{1}{4} C_{\mathrm{dc}} v_{\mathrm{dc}}^2\,, \tag{2.13}$$

where C_{sm} and v_{c} are the capacitance and the voltage of each SM capacitor. Under the assumption of perfectly balanced SM capacitor voltages, $v_{\mathrm{c}} = \frac{v_{\mathrm{dc}}}{N}$. Therefore, C_{dc} can be derived as[14]

$$6\sum_{i=1}^{N} \frac{1}{2} C_{\mathrm{sm}} v_{c_i}^2 = \frac{1}{2} 6NC_{\mathrm{sm}} \left(\frac{v_{\mathrm{dc}}}{N}\right)^2 = \frac{1}{4} \underbrace{\frac{12C_{\mathrm{sm}}}{N}}_{C_{\mathrm{dc}}} v_{\mathrm{dc}}^2\,. \tag{2.14}$$

What described so far relates to the normal operating conditions of the MMC. On the contrary, if the converter enters the blocked state (e.g., following a DC-side fault), the switches SW_1, SW_2, SW_3 and the thyristor

[14] It is worth pointing out that the underlying assumption in Eq. (2.13) and Eq. (2.14) is that the number of inserted SMs in every arm is N. In reality, however, this number is actually different for each arm and varies over time. As a result, C_{dc} is time-varying [28]. The same concept holds for R_{dc} and the computation of P_{loss}. Albeit detrimental to simulation accuracy, the approximations above only serve the purpose of reducing the computational burden.

T play an essential role. As stated in Section 1.3.5, when a fault is detected, the MMC protections react by blocking the converter (i.e., all the SMs gate signals are OFF) and opening the AC-side breakers after a given delay. The components above are introduced to mimic the MMC behaviour during these occurrences. As already mentioned, when the SMs are blocked, their capacitors cannot discharge. In Fig. 2.12 this is simulated by opening the switches SW_1 and SW_2 in series with the capacitors C_{dc}[15]. In addition, to force the direction of $\imath_{\mathrm{dc}}$ from the AC to the DC side, the switch SW_3 is opened and the thyristor T receives a firing signal.

Due to its reduced computational burden and the resulting possibility of adopting higher integration time steps, the discrete AVM is suitable for network level studies aimed at analysing the dynamic behaviour and stability of large grids made up of multiple MMCs. Moreover, this model allows tuning high-level control parameters (e.g., the PI regulators in Fig. 1.12) and testing several modulation schemes. However, due to its underlying assumptions, the model cannot assess the effectiveness of different Capacitor voltage Balancing Algorithms (CBAs) and circulating current suppression strategies. In addition, compared to more detailed representations, the model shown in Fig. 2.12 is less accurate when DC-side faults are simulated [79, 108]. The interested reader can refer to [126] for a more accurate AVM that can also simulate the start-up sequence of MMC.

For what regards the continuous AVM, its schematic is depicted in Fig. 2.13. Compared to its discrete counterpart, the MMC DC-side is the same, while the AC one is further simplified. Based on Eq. (1.2), the upper and lower arms of each MMC leg are replaced by a controlled voltage source (which mirrors the value of u_k^{ref} given by the outer level controls in Fig. 1.12), a resistor $\frac{1}{2}R_S$, and an inductor $\frac{1}{2}L_S$. Contrary to the previous model, the continuous AVM does not allow testing different modulation techniques because it disregards insertion indexes. Thus, the voltages across the controlled sources do not change with discrete steps but rather vary *continuously* - hence the name of the model. Except for this aspect and a lower computational burden, the continuous AVM inherits the same pros and cons of the discrete version.

Lastly, other than being the lowest among the proposed MMC models, the CPU-time related to the discrete and continuous AVMs is practically independent of the number of SMs in each arm N. In fact, in both models the size of the MMC nodal admittance matrix is fixed because, no matter the

[15] Note that this, however, precludes the possibility of analysing capacitor charging, which can still occur in the SM blocked condition (e.g., during the start-up sequence). This problem was addressed in [126] by developing an alternative and more accurate AVM.

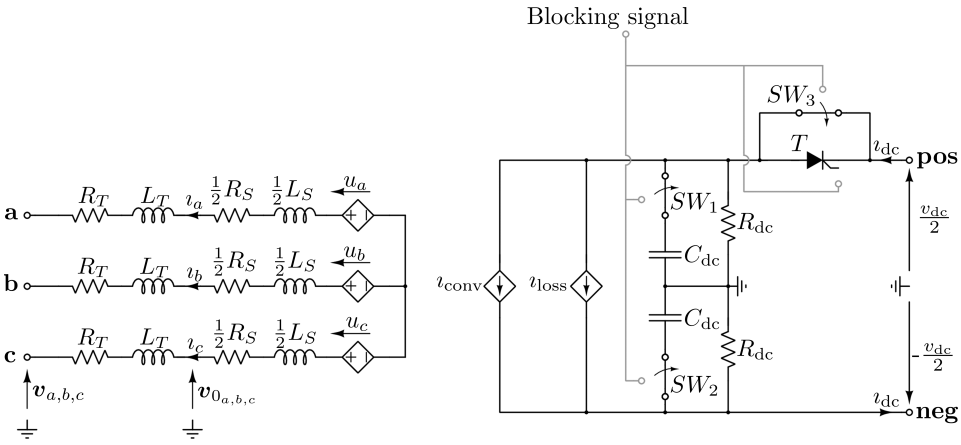


Figure 2.13: *Continuous* AVM *of the* MMC.

value of N, the equivalent MMC circuit remains the same. Moreover, the linear overhead incurred from capacitor voltage sorting in CBAs is avoided since AVMs do not adopt them.

2.2 Isomorphism-based simulation techniques

Over the last decades, academia and industry proposed several general-purpose circuit simulators. In particular, the Electro-Magnetic Transient Program (EMTP) and the Simulation Program with Integrated Circuit Emphasis (SPICE) rank among the most adopted ones. The former, originally developed in 1968 by the Bonneville Power Administration, is widely used to simulate electro-mechanical components in electric power systems. Specifically, EMTP relies on a fixed integration time step and describes any semiconductor device included in the system with simplified models [127]. On the contrary, SPICE is a program developed by the University of Berkeley. As its acronym suggests, it is specifically tailored for transistor-level electrical simulation of electronic Integrated Circuits (ICs). However, it is not suited for electro-mechanical simulations. Contrary to EMTP, SPICE uses a variable integration time step and the most accurate models of semiconductor devices to allow a detailed analysis of their behaviour also during commutations [112].

Ever since its first version in 1975, SPICE provided engineers with continuously improving means for analysing and verifying the design of their ICs before their actual fabrication in silicon. To achieve high simulation accuracy, the SPICE simulation engine was originally conceived by intro-

ducing some restrictions. Among others, these included: no component model approximations, adoption of the same integration step for the whole simulated system, and global convergence to the solution at every time step.

Over time, the gradual improvements in the SPICE software engine in terms of speed and capacity (i.e., number of components that it can manage) were mainly due to the adoption of more efficient time-integration schemes, as well as non-linear and linear solvers. Note that these enhancements focused exclusively on the numerical algorithms used, rather than on the exploitation of possible features of the simulated objects. This is because SPICE was conceived as a general-purpose simulation software, which could accurately simulate any electronic circuit, be it standard or unconventional. Thus, all the improvements in the simulation software had to be compatible with every component model.

This development strategy, however, eventually clashed with the increasing integration level and downscaling of electronic devices in ICs. Indeed, other than requiring the adoption of complex semiconductor models, the SPICE simulation paradigm implies that a matrix of a given size N (describing the linearised simulated circuit, with N being the number of its circuit equations) has to be LU-factorized every time step. As already stated, this operation leads to a computational burden that varies almost quadratically with N[16], which constitutes one of the main numerical bottlenecks in the simulation of large networks such as those mentioned above.

To analyse and design relatively recent and more complex ICs, a paradigm shift in the SPICE simulation approach was necessary. This has led to the emergence of a novel family of accelerated transistor-level simulators (i.e., "FAST-SPICE" simulators), which resort to innovative heuristics, unique methodologies, and computational techniques [23, 24]. These approaches implement different trade-offs between simulation speed and accuracy to attain a significant gain in simulation efficiency and capacity compared to SPICE. For example, instead of adopting a common integration time step and solving the entire network at each time step, FAST-SPICE exploits multirate simulation and network partitioning to accelerate the simulations.

This section focuses on isomorphism-based simulation, a technique originally introduced in FAST-SPICE to analyse ICs made up of topologically identical cells, such as RAMs. Section 2.2.1 presents this technique from a general perspective. Then, Section 2.2.2 explains how to use it to efficiently simulate MMCs. Lastly, Section 2.2.3 summarises the main features of this simulation approach and its fields of applications compared to the

[16]This trend is attained with algorithms that exploit circuit sparsity. Otherwise, the trend evolves as $\mathcal{O}(\frac{N^3}{3})$.

MMC models presented in the previous section.

2.2.1 Principles of isomorphism

Among others, FAST-SPICE simulators can efficiently simulate memory circuits, such a RAMs. These circuits can be regarded as a combination of arrays comprising at least hundreds of thousands of basically identical cells. Since RAMs are a typical component in relatively modern ICs, their fast and accurate simulation is of prominent importance.

The multitude of cells in RAMs leads to an unbearable computational burden if the traditional SPICE simulator is adopted. Indeed, its standard simulation approach requires the entire system to be "flattened": in the case of memory circuits, this means that all its internal cells are included in the netlist and simulated concurrently, thereby leading to a network with a high number of nodes and equations to be evaluated. On the one hand, circuit flattening is in principle the only viable option to track the evolution of each cell over time. On the other hand, it causes an almost quadratic increase in simulation time as circuit complexity grows [113]. It is also worth pointing out that in a memory circuit only a minor fraction of its cells is active during a read/write cycle [23]. The idle ones (whose state and algebraic variables are basically unaltered) do not strictly require to be simulated. Thus, circuit flattening inevitably results in some wasted effort.

As previously mentioned, the progressive enhancements in SPICE simulation speed and capacity were mainly due to the adoption of more efficient numerical algorithms, rather than from the exploitation of the key features of some simulated components. On the contrary, in FAST-SPICE simulators, this latter aspect is at the heart of some approaches aimed at significantly accelerating simulations at the expense of a slightly reduced accuracy.

For instance, some methods - hereafter referred to as *isomorphism-based techniques* - were originally adopted to efficiently simulate memory circuits by exploiting the presence of cells with identical topology and a limited number of operating states (e.g., cells in "*read/write*" or "*idle*" mode). During simulation, these methods group in classes the cells with similar behaviour. Then, instead of simulating each cell individually (as in the case of circuit flattening), the approaches simulate only one cell per class. As a result, the number of variables and equations necessary to solve the circuit reduces significantly by avoiding the simulation of similar cells. Despite this, the dynamic evolution of each one of them over time is still retained. Indeed, for each class, the dynamic evolution of one cell is replicated to those of the same group. Therefore, the computational burden is reduced

without sacrificing accuracy and losing any information about the cells.

To provide the reader with more information about the operating principle of isomorphism, the following paragraphs summarize the key features of the simulation strategies outlined in [128, 129]. Since the proposed methodologies have general validity and applicability, the description written hereafter focuses on generic sub-circuits (SCs). These SCs could represent different network components, such as cells in memory circuits or, as shown in the following, SMs in one arm of an MMC.

The approaches presented in [128, 129] efficiently simulate intrinsically modular circuits by resorting to static and dynamic circuit partitioning. Static partitioning, carried out at the beginning of the simulation, identifies SCs characterized by the same topology (i.e., the way internal components are connected) and nature of components (i.e., constitutive equations), and regards them as stand-alone modules during simulations.

On the other hand, dynamic partitioning is performed while simulating and groups all the static isomorphic SCs with common dynamics in a single equivalent entity. The electrical variables monitored during a working period to establish whether or not some SCs can be merged in a single equivalent entity are the input electrical quantities, the load conditions, and the state variables (e.g., capacitor voltages and inductor currents). Through dynamic partitioning, rather than simulating each SC individually, only separate, equivalent entities are simulated. The evolution of their state and algebraic variables is replicated for all the dynamic isomorphic SCs described by the same entity, without repeating the intensive computations for every SC.

When dealing with dynamic partitioning, one must bear in mind that the behaviour of each SC may change. Thus, during some simulation time intervals some SCs can be merged because their behaviour is similar, while during others previously merged SCs must be split because their dynamics have become so different that some of those cannot be represented by a common equivalent entity any longer. As a consequence, proper *isomorphism indicators* must be adopted to merge (or split) SCs based on their convergent (or divergent) dynamics [128, 129]. To explain at a high level how such indicators are used, assume for instance that the generic $\mathcal{S}_j$ subcircuit (SC) belonging to the $\mathcal{C}^k$ class of equivalent entities can be described by the following set of differential algebraic equations (DAEs)

$$\begin{cases} \dot{\boldsymbol{x}}_{k,j} = \boldsymbol{f}_k(\boldsymbol{x}_{k,j}, \boldsymbol{y}_{k,j}, t) \\ 0 \;\; = \boldsymbol{g}_k(\boldsymbol{x}_{k,j}, \boldsymbol{y}_{k,j}, t) \;, \end{cases} \tag{2.15}$$

where $\boldsymbol{x}_{k,j} \in \mathbb{R}^{N_k}$ and $\boldsymbol{y}_{k,j} \in \mathbb{R}^{M_k}$ are the state and the algebraic variables

vectors of $\mathcal{S}_j$.

Each class of isomorphic modules can be associated with a $(N_k + M_k)-$ dimensional hyper-sphere of a given radius. A SC enters (leaves) the $\mathcal{C}^k$ class if its $N_k + M_k$ state and algebraic variables are within (outside) this hyper-sphere. Since the behaviour of the SCs may change during simulation, such check must be repeated at each time step. A generic $\mathcal{S}_j$ SC belongs to the $\mathcal{C}^k$ class at a given time t only if the following constraints hold [128]

$$\begin{cases} |\boldsymbol{x}_{k,j}(t) - \hat{\boldsymbol{x}}_k(t)| \leq \boldsymbol{\alpha}_{\mathrm{R}_k} |\hat{\boldsymbol{x}}_k(t)| + \boldsymbol{\alpha}_{\mathrm{A}_k} \\ \left|\boldsymbol{y}_{k,j}(t) - \hat{\boldsymbol{y}}_k(t)\right| \leq \boldsymbol{\beta}_{\mathrm{R}_k} |\hat{\boldsymbol{y}}_k(t)| + \boldsymbol{\beta}_{\mathrm{A}_k} . \end{cases} \tag{2.16}$$

In Eq. (2.16), $\hat{\boldsymbol{x}}_k(t)$ and $\hat{\boldsymbol{y}}_k(t)$ are the reference state and algebraic variables vectors of the equivalent module of the $\mathcal{C}^k$ class at time t. For instance, these vectors could be computed as the average value of the state and algebraic variables of all the SCs belonging to the same $\mathcal{C}^k$ class at each time instant. In addition, $\boldsymbol{\alpha}_{\mathrm{A}_k}$, $\boldsymbol{\alpha}_{\mathrm{R}_k}$, $\boldsymbol{\beta}_{\mathrm{A}_k}$ and $\boldsymbol{\beta}_{\mathrm{R}_k}$ are the isomorphism indicators of the $\mathcal{C}^k$ class. Such parameters, whose role is analogous to that of absolute and relative tolerances in DAEs variable-step size solvers, determine the radius of the hyper-sphere of each class [98,130]. Adopting larger hyper-spheres makes an SC more likely to be simulated by an equivalent class with other SCs rather than being simulated alone, thereby speeding up the simulation process. As a consequence, the merging and splitting procedure becomes less strict and simulation accuracy may decrease. When a SC $\mathcal{S}_j$ leaves a given class, say $\mathcal{C}^k$, it can be simulated alone or it may enter another class, say $\mathcal{C}^l$, of dynamic isomorphic SCs.

2.2.2 Isomorphic simulation of MMCs

As in the case of RAMs, also the MMC has an intrinsically modular structure, and its SMs are associated with a limited number of operating states (which will be duly described in the following). Therefore, this converter technology lends itself to isomorphism-based simulation. In this thesis, the general approach described in Section 2.2.1 is exploited to efficiently simulate MMCs based on half-bridge SMs. To the best of the author knowledge, such an approach has never been used before in this context (except for [25, 29], co-written by the author during the PhD programme).

As previously stated, an isomorphism-based simulation consists of two phases: static and dynamic partitioning. The former is performed at the beginning of the simulation. In the case of the MMC, the cascaded SMs of each upper and lower arm of the three-phase converter legs are identified

as static isomorphic SCs, since their topology and nature of components is the same. In general, if the SMs in one MMC arm are characterised by discrepancies in their parameters (e.g., the capacitance C_{sm}), their constitutive equations are inevitably different. As a result, the SMs in one stack are not isomorphic from a "*static*" point of view. In the light of the above, it is not possible to select just one of them as a "stand-alone module": indeed, multiple static isomorphic SMs need to be considered. In the following, it is assumed that there is no discrepancy in the parameters of each SM.

Then, dynamic partitioning is carried out repeatedly during simulation: in each arm, the SMs (i.e., static isomorphic sub-circuits) showing common, redundant behaviours are dynamically grouped in four main different equivalent entities (or classes).[17] While simulating, each SM is moved from a class to another based on gate and blocking signals. Indeed, SMs sharing the same gate and blocking signals potentially belong to the same class.

In turn, such classes can be dynamically divided into sub-classes if, based on Eq. (2.16), the isomorphism indicators require gathering the SMs of a given class in more than a single group. By considering the most general FP model in Fig. 2.2(a), the four main classes of SMs can be described by the following list.

- The *capacitor-inserted* ($\mathcal{C}^{\mathrm{in}}$) class represents the SMs whose S_1 and S_2 IGBTs are ON and OFF, respectively. Based on the sign of the current $\imath_{\mathrm{SM}}$, the generic capacitor C_{sm} is either charging or discharging.
- The *capacitor-bypassed* ($\mathcal{C}^{\mathrm{by}}$) class describes the SMs whose S_1 IGBT is OFF and S_2 IGBT is ON. In this configuration, the capacitor C_{sm} is said to be bypassed because only a negligible fraction of $\imath_{\mathrm{SM}}$ (leakage current of the IGBT) flows through it.
- The *blocked* ($\mathcal{C}^{\mathrm{bl}}$) class represents the SMs whose IGBTs are both OFF. This class is relevant during system start-up, or when an external fault occurs and the MMC is blocked.
- Lastly, the *switching* ($\mathcal{C}^{\mathrm{sw}}$) class contains all the SMs moving from one class to the other (i.e., from $\mathcal{C}^{\mathrm{in}}$ to $\mathcal{C}^{\mathrm{by}}$ and vice versa, as well as from $\mathcal{C}^{\mathrm{in}}$ or $\mathcal{C}^{\mathrm{by}}$ to $\mathcal{C}^{\mathrm{bl}}$ and vice versa). In this class, the gate signals are time-varying and include dead-times to prevent cross-conduction. During normal operating conditions, the switching class contains two major sub-classes. One sub-class refers to the SMs switching from the inserted to the bypassed class, whereas the other sub-class refers to

[17] Since the current flowing in every MMC arm is different, each of them requires the creation of separate isomorphic classes.

the SMs switching in the opposite direction. Considering the former, for instance, the gate signal v_{g_1} (see Fig. 2.14) goes from ON to OFF, while the opposite holds for v_{g_2}. The number of SMs in this class depends on the algorithm used to control the gate signals of each SM and the MMC current working condition (i.e., presence or absence of faults). Let us consider for instance normal operating conditions (i.e., the $\mathcal{C}^{\mathrm{bl}}$ class is empty). If the control system switches just one SM per arm at a time, the $\mathcal{C}^{\mathrm{sw}}$ class consists of no more than just one SM, which leaves this class and enters the $\mathcal{C}^{\mathrm{in}}$ or $\mathcal{C}^{\mathrm{by}}$ classes as soon as the switching transient is exhausted [131][18]. Furthermore, if the BVR model of SMs is used, the switching process is instantaneous (besides, as stated in Section 2.1.3, any switching dynamic whatsoever inside the SMs is disregarded). Thus, the $\mathcal{C}^{\mathrm{sw}}$ class is empty and all the SMs instantaneously jump from and to the $\mathcal{C}^{\mathrm{in}}$ and $\mathcal{C}^{\mathrm{by}}$ classes.

Note that the amount of SMs in each class changes over time. Thus, dynamic partitioning is performed continuously while simulating. In normal operating conditions, for instance, by taking into account the nearest-level modulation, the number of inserted and bypassed SMs will be time-varying. If faults occur, the SMs will move to the $\mathcal{C}^{\mathrm{bl}}$ class.

The isomorphic simulation of MMCs does not depend on the model used to describe their submodules (SMs). Designers can adopt any of the models reported in Fig. 2.2 or even define their own SM model. This is a strong point of the proposed approach if one just notes that, from a theoretical standpoint, non-linearities and dynamic elements prevent collapsing SMs in an equivalent time-varying Thévenin equivalent as in [100], which is only compatible with the BVR SM model.

For the sake of generality, and to provide the reader with more details, the following description focuses on an MMC whose SMs are described through the full physics (FP) model. In this case, as stated in Section 2.1.1, the SMs include semiconductor devices described by detailed, non-linear dynamic models (i.e., built-in or macro-models). Under the assumptions of isomorphism and if the previously described classes are not split into subclasses, the string of SMs in one arm can be replaced with the equivalent circuit in Fig. 2.14.

There are six equivalent circuits of this kind, one for each arm of the three-phase MMC, as shown in Fig. 2.15. By referring to the circuit of

[18]The $\mathcal{C}^{\mathrm{sw}}$ class collects SMs whose semiconductors (if any) are undergoing a transient, mainly triggered by time-varying signals. Whenever such SMs reach a new "steady-state" working condition, they move to other classes. For instance, if in a SM v_{g_1} reaches its "on" (constant) value and $v_{\mathrm{g}_\mathrm{c}}$ its "off" (constant) value and the dynamic behaviour of semiconductors has come to an end, said SM moves to the $\mathcal{C}^{\mathrm{by}}$ class. This means that $\mathcal{C}^{\mathrm{sw}}$ is the bridging class that governs transitions to the other ones.

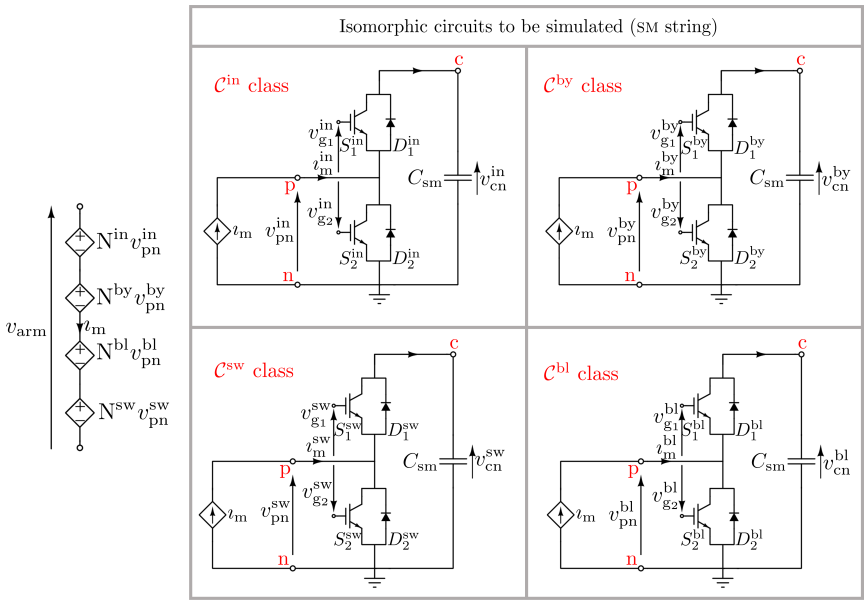


Figure 2.14: *The equivalent circuit of a* SM *string in one* MMC *arm obtained by adopting the* FP SM *model and the isomorphism-based approach. Each isomorphic class is represented by an individual* SM.

Fig. 2.14, the SM representing those in $\mathcal{C}^{\text{in}}$ class is driven by the $\imath_{\text{m}}$ arm current, which is mirrored by the current controlled current source. The $v_{\text{pn}}^{\text{in}}$ voltage is multiplied by the N^{in} (time-varying) number of SMs in the class and added to build the v_{arm} voltage using a voltage controlled voltage source. Similar electrical considerations hold for the SMs of the other classes. It is important to underline that the v_{g_1} and v_{g_2} gate signals of the IGBTs in the $\mathcal{C}^{\text{in}}$, $\mathcal{C}^{\text{by}}$ and $\mathcal{C}^{\text{bl}}$ classes are constant during the entire simulation, whereas they are time-varying in the $\mathcal{C}^{\text{sw}}$ class[19]. Thus, switching phenomena, power dissipation and current conduction by IGBTs or diodes are correctly simulated (that is, provided that the FP model of SMs and a sufficiently low integration time step are used).

In the light of the above, the constitutive equation of the equivalent cir-

[19]The gate signals of the SMs in the $\mathcal{C}^{\text{bl}}$ class are always zero, while those of the $\mathcal{C}^{\text{sw}}$ class are both equal to zero only during dead-time. To distinguish the two kinds of SMs during dead-time, a blocking signal is added to each SM, which is active only when a given SM enters the blocked condition.

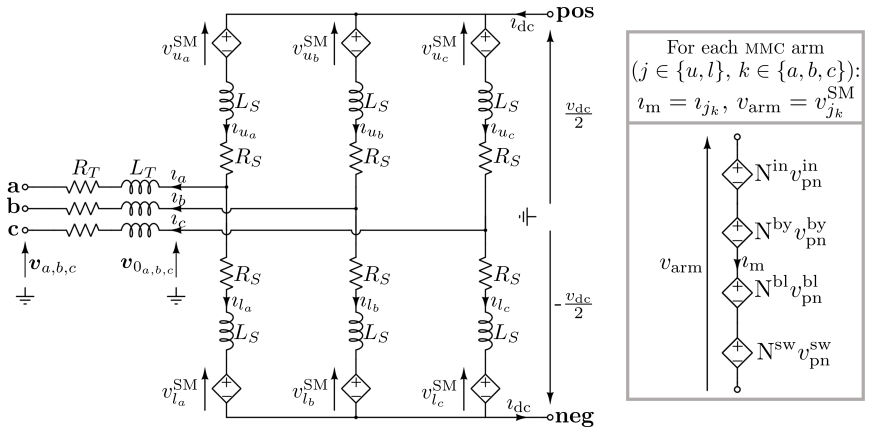


Figure 2.15: *The resulting* MMC *schematic when the isomorphism-based simulation approach is adopted.*

cuit representing the stack of SMs in one MMC arm can be formalised as

$$
\begin{aligned}
& v_{\mathrm{arm}} = v^{\mathrm{in}} + v^{\mathrm{by}} + v^{\mathrm{bl}} + v^{\mathrm{sw}} \\
& v^{\mathrm{in}} = N^{\mathrm{in}} v^{\mathrm{in}}_{\mathrm{pn}} = N^{\mathrm{in}} v^{\mathrm{in}}_{\mathrm{pc}} + \sum_{j=1}^{N^{\mathrm{in}}} v^{\mathrm{in}}_{\mathrm{cn}_j} \\
& v^{\mathrm{by}} = N^{\mathrm{by}} v^{\mathrm{by}}_{\mathrm{pn}} \\
& v^{\mathrm{bl}} = N^{\mathrm{bl}} (v^{\mathrm{bl}}_{\mathrm{pc}} + v^{\mathrm{bl}}_{\mathrm{cn}}) \\
& v^{\mathrm{sw}} = N^{\mathrm{sw}} (v^{\mathrm{sw}}_{\mathrm{pc}} + v^{\mathrm{sw}}_{\mathrm{cn}}) \\
& \imath_{\mathrm{m}} = \imath^{\mathrm{in}}_{\mathrm{m}} = \imath^{\mathrm{by}}_{\mathrm{m}} = \imath^{\mathrm{bl}}_{\mathrm{m}} = \imath^{\mathrm{sw}}_{\mathrm{m}} \\
& \boldsymbol{f}^{\mathrm{in}} \left(\dot{v}^{\mathrm{in}}_{\mathrm{pc}}, v^{\mathrm{in}}_{\mathrm{pc}}, v^{\mathrm{in}}_{\mathrm{g}_1}, v^{\mathrm{in}}_{\mathrm{g}_2}, \dot{v}^{\mathrm{in}}_{\mathrm{cn}}, v^{\mathrm{in}}_{\mathrm{cn}}, \imath^{\mathrm{in}}_{\mathrm{m}} \right) = 0 \\
& \boldsymbol{f}^{\mathrm{by}} \left(\dot{v}^{\mathrm{by}}_{\mathrm{pc}}, v^{\mathrm{by}}_{\mathrm{pc}}, v^{\mathrm{by}}_{\mathrm{g}_1}, v^{\mathrm{by}}_{\mathrm{g}_2}, \dot{v}^{\mathrm{by}}_{\mathrm{cn}}, v^{\mathrm{by}}_{\mathrm{cn}}, \imath^{\mathrm{by}}_{\mathrm{m}} \right) = 0 \\
& \boldsymbol{f}^{\mathrm{bl}} \left(\dot{v}^{\mathrm{bl}}_{\mathrm{pc}}, v^{\mathrm{bl}}_{\mathrm{pc}}, v^{\mathrm{bl}}_{\mathrm{g}_1}, v^{\mathrm{bl}}_{\mathrm{g}_2}, \dot{v}^{\mathrm{bl}}_{\mathrm{cn}}, v^{\mathrm{bl}}_{\mathrm{cn}}, \imath^{\mathrm{bl}}_{\mathrm{m}} \right) = 0 \\
& \boldsymbol{f}^{\mathrm{sw}} \left(\dot{v}^{\mathrm{sw}}_{\mathrm{pc}}, v^{\mathrm{sw}}_{\mathrm{pc}}, v^{\mathrm{sw}}_{\mathrm{g}_1}, v^{\mathrm{sw}}_{\mathrm{g}_2}, \dot{v}^{\mathrm{sw}}_{\mathrm{cn}}, v^{\mathrm{sw}}_{\mathrm{cn}}, \imath^{\mathrm{sw}}_{\mathrm{m}} \right) = 0 \,,
\end{aligned}
\tag{2.17}
$$

where the $^{\mathrm{in,\,by,\,sw,\,bl}}$ superscripts refer to a given class of isomorphic SMs.

The $\boldsymbol{f}^{\cdot}(\,\cdot\,)$ vector-valued multivariate functions are a condensed way of representing the model of the diodes and IGBTs of each class of isomorphic SMs and their interconnections. Note that time derivatives, denoted by dots above the variables, appear among the arguments of these functions (i.e., the dynamical models of the diodes and IGBTs are employed [104–106]).

Each one of the last four equations of Eq. (2.17) is a specialization of Eq. (2.15). To give a handy example of what happens by further specializing one of these equations, we expand $\boldsymbol{f}^{\mathrm{sw}}(\,\cdot\,)$ when the full detailed (FD) model is adopted (see Fig. 2.2(b)). In this case, by letting $\imath_{\mathrm{SM}} = \imath_{\mathrm{m}}$ we have

$$C_{\mathrm{sm}}\dot{v}_{\mathrm{c}}^{\mathrm{sw}} = I_o\left(e^{\kappa_d v_{\mathrm{pc}}^{\mathrm{sw}}} - 1\right) - \imath_1^{\mathrm{sw}} \tag{2.18}$$

$$\imath_{\mathrm{m}}^{\mathrm{sw}} - I_o\left(e^{\kappa_d v_{\mathrm{pc}}^{\mathrm{sw}}} - e^{-\kappa_d\left(v_{\mathrm{pc}}^{\mathrm{sw}}+v_{\mathrm{cn}}^{\mathrm{sw}}\right)}\right) + \imath_1^{\mathrm{sw}} - \imath_2^{\mathrm{sw}} = 0 \tag{2.19}$$

$$\imath_2^{\mathrm{sw}} - \chi(v_{\mathrm{g}_2}^{\mathrm{sw}})I_o\left(e^{\kappa_d\left(v_{\mathrm{pc}}^{\mathrm{sw}}+v_{\mathrm{cn}}^{\mathrm{sw}}\right)} - 1\right) = 0 \tag{2.20}$$

$$\imath_1^{\mathrm{sw}} - \chi(v_{\mathrm{g}_1}^{\mathrm{sw}})I_o\left(e^{-\kappa_d v_{\mathrm{pc}}^{\mathrm{sw}}} - 1\right) = 0\,, \tag{2.21}$$

where $\kappa_d = \frac{q}{\eta k_B T}$, being q the electron charge, η the emission coefficient, k_B the Boltzmann constant, and T the junction temperature. In this example, to keep notation simple, the I_o saturation current is assumed identical in all diodes and charge equations were dropped [103]. The $\chi(\,\cdot\,)$ function assumes values from the two-element set $\{0, 1\}$ according to its argument (i.e., the gate driving voltages, in this case). The charging of the SM capacitor is governed by Eq. (2.18). Equation (2.19) expresses the $\imath_{\mathrm{m}}^{\mathrm{sw}}$ submodule current as the sum of the currents flowing in the two switches and the antiparallel diodes. Equations (2.20) and (2.21) implement the characteristic of the two switches. These equations become more complicated if the FP SM model is used.

Having in mind Eq. (2.15), which collects the DAEs governing the generic class $\mathcal{C}^k$, for the j-th SM belonging to the $\mathcal{C}^{\mathrm{sw}}$ class, the state variable $v_{\mathrm{c}}^{\mathrm{sw}}$ in Eq. (2.18) matches with $\boldsymbol{x}_{k,j}$ ($N_k = 1$), while the $(v_{\mathrm{sm}}^{\mathrm{sw}}, v_{\mathrm{cn}}^{\mathrm{sw}}, v_{\mathrm{g}_2}^{\mathrm{sw}}, v_{\mathrm{g}_1}^{\mathrm{sw}}, \imath_1^{\mathrm{sw}}, \imath_2^{\mathrm{sw}}, \imath_{\mathrm{m}}^{\mathrm{sw}})$ algebraic variables in Eqs. (2.19)-(2.21) match with $\boldsymbol{y}_{k,j}$ ($M_k = 7$). Note that $\boldsymbol{f}_k(\,\cdot\,)$ reduces to the right hand side of Eq. (2.18), whereas $\boldsymbol{g}_k(\,\cdot\,)$ is a vector-valued function collecting the left hand side of Eqs. (2.19)-(2.21).

When it comes to isomorphism-based MMC simulation, Eq. (2.16), which governs clustering and class building, becomes in the case of a SM belonging to the $\mathcal{C}^{\mathrm{sw}}$ class

$$\begin{aligned}
|v_{\mathrm{cn}}^{\mathrm{sw}}(t) - \hat{v}_{\mathrm{cn}}^{\mathrm{sw}}(t)| &\leq \alpha_{\mathrm{R}_{\mathrm{cn}}^{\mathrm{sw}}}\,|\hat{v}_{\mathrm{cn}}^{\mathrm{sw}}(t)| + \alpha_{\mathrm{A}_{\mathrm{cn}}^{\mathrm{sw}}} \\
\left|v_{\mathrm{g}_1}^{\mathrm{sw}}(t) - \hat{v}_{\mathrm{g}_1}^{\mathrm{sw}}(t)\right| &\leq \beta_{\mathrm{R}_{\mathrm{g}_1}^{\mathrm{sw}}}\left|\hat{v}_{\mathrm{g}_1}^{\mathrm{sw}}(t)\right| + \beta_{\mathrm{A}_{\mathrm{g}_1}^{\mathrm{sw}}} \\
\left|v_{\mathrm{g}_2}^{\mathrm{sw}}(t) - \hat{v}_{\mathrm{g}_2}^{\mathrm{sw}}(t)\right| &\leq \beta_{\mathrm{R}_{\mathrm{g}_2}^{\mathrm{sw}}}\left|\hat{v}_{\mathrm{g}_2}^{\mathrm{sw}}(t)\right| + \beta_{\mathrm{A}_{\mathrm{g}_2}^{\mathrm{sw}}} \\
|\imath_{\mathrm{m}}^{\mathrm{sw}}(t) - \hat{\imath}_{\mathrm{m}}^{\mathrm{sw}}(t)| &\leq \beta_{\mathrm{R}_{\mathrm{m}}^{\mathrm{sw}}}\,|\hat{\imath}_{\mathrm{m}}^{\mathrm{sw}}(t)| + \beta_{\mathrm{A}_{\mathrm{m}}^{\mathrm{sw}}}\,,
\end{aligned}$$

where, being $\zeta \in \{v_{\mathrm{cn}}^{\mathrm{sw}}, v_{\mathrm{g}_1}^{\mathrm{sw}}, v_{\mathrm{g}_2}^{\mathrm{sw}}, \imath_{\mathrm{m}}^{\mathrm{sw}}\}$, $\hat{\zeta}(t) = \dfrac{1}{N^{\mathrm{sw}}}\displaystyle\sum_{j=0}^{N^{\mathrm{sw}}}\zeta_j(t)$ is the average

value of ζ, $\alpha_{\mathrm{R}_{\mathrm{cn}}^{\mathrm{sw}}}$ ($\beta_{\mathrm{R}_{\mathrm{g}_1}^{\mathrm{sw}}}$, $\beta_{\mathrm{R}_{\mathrm{g}_2}^{\mathrm{sw}}}$ $\beta_{\mathrm{R}_{m}^{\mathrm{sw}}}$) and $\alpha_{\mathrm{A}_{\mathrm{cn}}^{\mathrm{sw}}}$ ($\beta_{\mathrm{A}_{\mathrm{g}_1}^{\mathrm{sw}}}$, $\beta_{\mathrm{A}_{\mathrm{g}_2}^{\mathrm{sw}}}$ $\beta_{\mathrm{R}_{\mathrm{m}}^{\mathrm{sw}}}$) define the relative and the absolute error, respectively, with respect to $\hat{v}_{\mathrm{cn}}^{\mathrm{sw}}$ ($\hat{v}_{\mathrm{g}_1}^{\mathrm{sw}}$, $\hat{v}_{\mathrm{g}_2}^{\mathrm{sw}}$ $\hat{\imath}_{\mathrm{m}}^{\mathrm{sw}}$). The $\beta_{\mathrm{R}_{\mathrm{m}}^{\mathrm{sw}}}$ and $\beta_{\mathrm{A}_{\mathrm{m}}^{\mathrm{sw}}}$ thresholds can be chosen very close to similar constants (10^{-6}) governing the accuracy of the DAE solver that computes the solution of the circuit since the modules in $\mathcal{C}^{\mathrm{sw}}$ share by construction the same $\imath_{\mathrm{m}} \equiv \imath_{\mathrm{m}}^{\mathrm{sw}}$ current. This leads to a good clustering level of $\mathcal{C}^{\mathrm{sw}}$.

To give more insight into the use of isomorphic indicators consider for instance the SMs populating the $\mathcal{C}^{\mathrm{in}}$ class. It is reasonable to accept that a negligible current ($\mu\mathrm{A}/\mathrm{mA}$ saturation current against kA arm current) flows through the S_2 IGBT and the D_2 diode. This assumption is justified by the fact that, once the switching transient is completed, in the $\mathcal{C}^{\mathrm{in}}$ SMs the current $\imath_{\mathrm{m}} \equiv \imath_{\mathrm{m}}^{\mathrm{in}}$ mostly flows through the capacitor C_{sm} and the S_1 IGBT (or the D_1 diode, based on the sign of the current). If this negligible current satisfies the constraint in Eq. (2.16) independently from the $v_{\mathrm{pc}}^{\mathrm{in}}$ and $v_{\mathrm{cn}}^{\mathrm{in}}$ voltages, the $\mathcal{C}^{\mathrm{in}}$ class collects all the N^{in} arm SMs that are in this *inserted* working condition. Thus, the voltage *variation* of the capacitor C_{sm} and the voltage $v_{\mathrm{pc}}^{\mathrm{in}}$ (across the p and c nodes) are the same for all the SMs of such class. Note that the voltage of each capacitor can be significantly different but this marginally affects the current flowing through the SMs of each arm (fraction of mA versus kA). Thus, the isomorphic behaviour of each SM in the arm is not affected. Consequently, one can relax the $\alpha_{\mathrm{R}_{\mathrm{cn}}}$ and $\alpha_{\mathrm{A}_{\mathrm{cn}}}$ tolerances of the $\mathcal{C}^{\mathrm{in}}$ class.

Importantly, this simulation paradigm can continuously keep track of the SM capacitor voltages, which is an input required by the MMC control scheme to perform Capacitor voltage Balancing Algorithms (CBAs). To do so, the capacitor voltage variation of a given class is replicated to all the capacitors of the SMs belonging to the same class. In other words, the voltage variation is summed to the voltage that the capacitor of each SM of the same class had at the beginning of a new dynamic clustering, similarly to what is done in [125] and Section 3.2.3 of [55] .

2.2.3 Main features and fields of application of the isomorphism-based simulation of MMCs

As shown in Fig. 2.1 and its related text, as well as in the summary of Table 2.1, the MMC models and simulation approaches developed in the literature implement different trade-offs between simulation speed and accuracy by simplifying the SMs model and/or the overall MMC structure. For example, the Thévenin Equivalent Model (TEM) relies on the BVR model of SMs, while the Switching Function Model (SFM) resorts to an idealized repre-

sentation of the semiconductor devices in each valve as ideal switches.

On the contrary, the isomorphism-based approach allows increasing the simulation efficiency of MMCs regardless of the SM model adopted because it leads to a compact representation of the SM strings. Indeed, for each of them, only a single element of a given group of isomorphic SMs (i.e., a class) is simulated and its electrical evolution is replicated to all the SMs in the same class. In the best-case scenario depicted in Fig. 2.14, each SM string comprises only four classes. Thus, since the number of nodes and model equations to be considered reduces significantly, the simulations are much faster than those obtained with conventional EMT solvers but just as accurate. This approach can also simulate the highly detailed FP model of SMs within reasonable CPU times.

In addition, similarly to the Thévenin Equivalent Model and the discrete Switching Function Model, the MMC computational burden increases linearly with the number of SMs per arm N, instead of (almost) quadratically. As stated in Section 2.1.4, this happens because the switching activity of the MMC (i.e., number of threshold crossings per period in Fig. 1.16) rises with N, which requires a proportional reduction of the integration time step. The slope associated with this linear trend depends on the integration time step adopted (fixed or variable) and the SM model chosen (i.e., in general, the more complex the model, the steeper the linear trend). Even if a sufficiently low integration time step were used for an entire set of simulations with different values of N, linearly varying CPU times would still be observed due to the increasingly frequent execution of Capacitor voltage Balancing Algorithms (CBAs) as N rises.

Lastly, contrary to the AVM, no simplification whatsoever (e.g., perfectly balanced voltage, no circulating current) is introduced to the operation of MMC when the isomorphism-based method is used. As a result, the proposed approach can correctly simulate MMCs during both normal and abnormal operating conditions, and validate all their protections and controls, including CBAs. If the FP SM model is adopted, the method also allows evaluating both conduction and switching losses of semiconductor devices with a high degree of accuracy.

All the abovementioned features are highlighted and validated in the next chapter, where the isomorphism-based approach is used to simulate two MMCs in an HVDC system in different operating conditions.

Table 2.1: *Summary table of the* MMC *models or simulation approaches described in this chapter. For ease of reference, some of the acronyms used are listed hereafter: full physics* (FP)*, full detailed* (FD)*, bi-value resistor* (BVR)*, Circulating Current Suppression Strategy* (CCSS)*, Capacitor voltage Balancing Algorithm* (CBA)*, Nearest Level Modulation* (NLM)*. In the last column, N corresponds to the number of submodules* (SMs) *in each arm.*

MMC model or simulation approach	SM models allowed	Lower level controls analyzable			Individual SM behaviour is retained	Compatible with component level studies	CPU time trend as N increases
		CCSS	CBA	NLM (or others)			
Conventional approach	All: FP, FD, BVR, custom models, etc.	Yes	Yes	Yes	Yes	Yes (with FP or equally detailed SM models)	$\sim$ Quadratic
TEM	BVR	Yes	Yes	Yes	Yes	No	$\sim$ Linear
SFM type 1	SM valves as ideal switches	Yes	No	Yes	No	No	$\sim$ Constant
SFM type 2		Yes	Yes	Yes	Yes	No	$\sim$ Linear
SFM type 3	Average behaviour: SM model neglected	Yes	No	No	No	No	$\sim$ Constant
AVM discrete		No	No	Yes	No	No	$\sim$ Linear
AVM continuous		No	No	No	No	No	$\sim$ Constant
Isomorphism-based approach	All: FP, FD, BVR, custom models, etc.	Yes	Yes	Yes	Yes (approximately)	Yes (with FP or equally detailed SM models)	$\sim$ Linear

CHAPTER 3

Validation of the isomorphism-based approach

3.1 Simulation setting

To demonstrate and highlight the features of the isomorphism-based simulation approach described in the previous chapter, the DCS1 HVDC CIGRE test system, shown in Fig. 3.1 and presented in [61], was selected as a benchmark and simulated in different operating conditions. It is worth pointing out that, however, the simulation setting described in [61] lacks some details. For example, it does not specify the exact *lower level controls* adopted and refrains from using the full physics model of SMs (which, as previously stated, is not simulated in programmes such as EMTP-RV and PSCAD). In addition, the MMC control strategy described in [61] can only deal with balanced working conditions.

To fill in the gap given by missing data and make the MMC control strategy compatible also with unbalanced operating conditions (e.g., single-line to ground faults), the simulation setting has been improved. This section briefly describes how each component in Fig. 3.1 has been implemented and simulated.

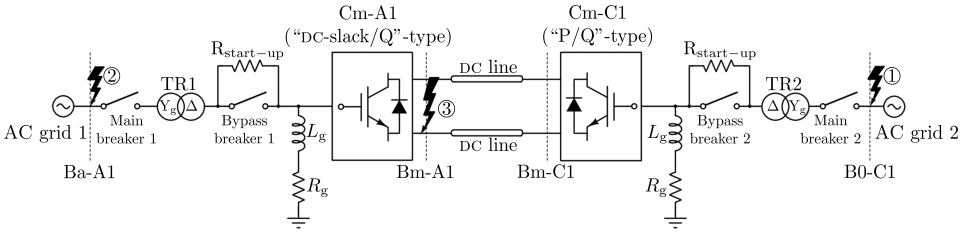


Figure 3.1: *The block schematic of the* CIGRE DCS1 HVDC *test system [61]. Dashed lines indicate busses. Lightning bolts and circled numbers next to those respectively indicate faults and the order in which they are considered in this chapter.*

Table 3.1: *Parameters of the* AC *grids 1 and 2 in Fig. 3.1.*

Parameter	AC grid 1	AC grid 2	Comment
V_{nom}	380 kV	145 kV	Nominal line-to-line RMS voltage
S_{sc}	30 GVA	30 GVA	Short circuit power
$X/R = \tan(\varphi)$	10	10	X/R ratio

3.1.1 AC grids and transformers

The AC grids 1 and 2 in Fig. 3.1 comprise a three-phase voltage source ($v_a(t)$, $v_b(t)$, and $v_c(t)$) connected in series with an impedance (R_{grid}, X_{grid}) as shown in Fig. 3.2. Based on the data listed in Table 3.1, the parameters of the two AC grids are computed as

$$\begin{aligned}
Z_{\text{grid}} &= \frac{V_{\text{nom}}^2}{S_{\text{sc}}} \\
R_{\text{grid}} &= Z_{\text{grid}} \cos(\varphi) \\
L_{\text{grid}} &= \frac{Z_{\text{grid}} \tan(\varphi)}{2\pi f_0} \\
v_a(t) &= \sqrt{\frac{2}{3}} V_{\text{nom}} \cos\left(2\pi f_0 t\right) \\
v_b(t) &= \sqrt{\frac{2}{3}} V_{\text{nom}} \cos\left(2\pi f_0 t - \frac{2\pi}{3}\right) \\
v_c(t) &= \sqrt{\frac{2}{3}} V_{\text{nom}} \cos\left(2\pi f_0 t + \frac{2\pi}{3}\right) ,
\end{aligned} \tag{3.1}$$

As stated in Section 1.2.1, since the filter requirements of the MMC are minimum, the filter (R_T, L_T) in Fig. 1.8 could just be given by the leakage resistance and inductance of the transformer used to connect the converter

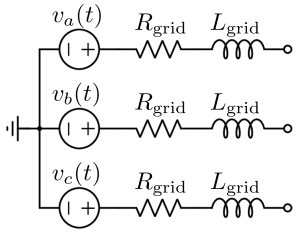


Figure 3.2: *Schematic of the* AC *grids 1 and 2 in Fig. 3.1.*

Table 3.2: *Parameters of the Y_g/Δ transformers TR1 and TR2 in Fig. 3.1.*

Parameter	TR1	TR2	Comment
S_{nom}	800 MVA	800 MVA	Nominal power
$V_{\text{Y}_{\text{nom}}}$	380 kV	145 kV	Nominal line-to-line RMS voltage (Y-side)
$V_{\Delta_{\text{nom}}}$	245 kV	245 kV	Nominal line-to-line RMS voltage (Δ-side)
R_{T}	0.363 Ω	0.363 Ω	Leakage resistance (connected to the Δ-side)
L_{T}	35 mH	35 mH	Leakage inductance (connected to the Δ-side)

to the grid, without requiring the installation of an *ad hoc* filter. This is exactly the case of the MMCs simulated in Fig. 3.1. Indeed, Table 3.2, which describes the parameters of the Y_g/Δ transformers TR1 and TR2 in Fig. 3.1, also includes R_T and L_T as variables. The resistance $R_g = 5\,\text{k}\Omega$ and inductance $L_g = 5\,\text{kH}$ are added to provide a voltage reference at the ungrounded side (i.e., the Δ-side) of the transformers [121]. Their value is such that only a negligible current flows through them, thereby ensuring that the zero sequence current at the AC-side of the two MMCs is basically always null. This holds provided that, as assumed in this chapter, asymmetric faults never occur at the Δ-side of TR1 and TR2.

Section 3.1.5 explains the role of the start-up resistors ($R_{\text{start}_{\text{up}}} = 10\,\text{k}\Omega$), bypass breakers, and main breakers in Fig. 3.1.

3.1.2 DC line

The modelling of DC lines is a key aspect of steady-state and transient simulations involving HVDC and MTDC systems. The simplest approach models lines with cascaded π sections characterised by constant parameters. By doing so, however, the frequency dependency of the line resistance and inductance due to skin effect is neglected. In turn, this might lead to simulation results significantly different from the correct ones: conclusions drawn *tout court* from them about the system dynamics and stability would be misguided [28]. In the light of the above, a more sophisticated line model has been adopted.

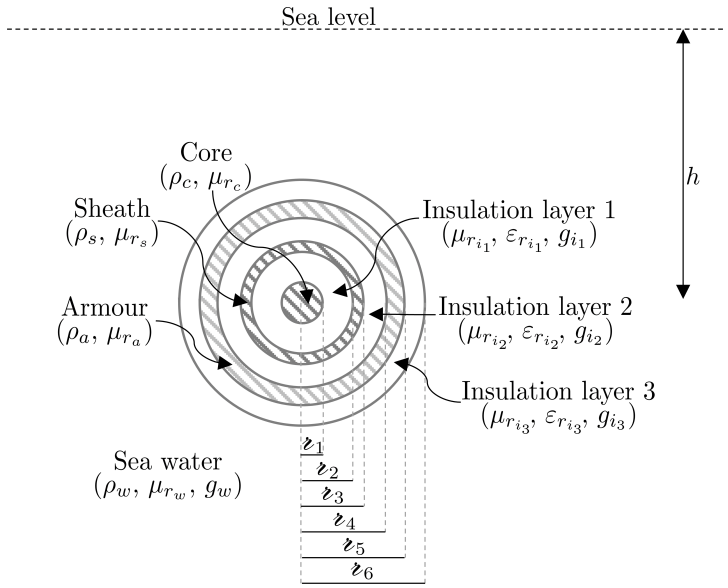


Figure 3.3: *Cross section of the submarine cable adopted for the* DC *lines in Fig. 3.1. Regardless of subscript, the terms r, ρ, g, μ_r, and ε_r respectively refer to the radius, conductivity, leakage conductance, relative permeability, and relative permittivity of the conducting/insulating layers inside the cable. The variables h and g correspond respectively to the depth of the cable (central point) below the sea level and the sea water per-unit length conductance.*

3.1.2.1 Line geometry and derivation of its impedance and admittance

Before describing the model of the DC lines adopted, this section details how to derive their impedance and admittance matrices starting from geometric and other technical data. Most of the papers concerning MMC studies either briefly mention this aspect or take it for granted. Indeed, some popular simulation programmes, such as EMTP and PSCAD, compute these matrices automatically by resorting to the "*Cable Constants*" subroutine developed by Ametani in 1976 [101]. Since then, this subroutine has been improved by adding new formulas, either accurate or approximate, that take into account several line topologies.

The following paragraphs, particularly aimed at readers who are not familiar with EMTP and PSCAD, briefly explain the operating principle of this subroutine by considering as an example the DC lines in Fig. 3.1. These lines are submarine cables comprising different conducting (i.e., core, sheath, and armour) and insulating layers, sketched in Fig. 3.3. Table 3.3 lists the specifics of these layers.

The voltages and currents of the core, sheath and armour (denoted re-

Table 3.3: *Detailed characteristics of the* DC *lines used in this thesis. The listed values, which derive from [61, 132], refer to the cross section of the cable in Fig. 3.3.*

Parameter	Value
r_1	$25.125\,\mathrm{mm}$
r_2	$45.125\,\mathrm{mm}$
r_3	$47.125\,\mathrm{mm}$
r_4	$50.225\,\mathrm{mm}$
r_5	$55.725\,\mathrm{mm}$
r_6	$60.725\,\mathrm{mm}$
h	$51.5\,\mathrm{m}$
g_w	$1.65\,\mathrm{S/mm}$
$\varepsilon_{r_{i_1}} = \varepsilon_{r_{i_2}} = \varepsilon_{r_{i_3}}$	2.3

Parameter	Value
ρ_c	$2.20 \cdot 10^{-8}\,\Omega\mathrm{m}$
ρ_s	$27.40 \cdot 10^{-8}\,\Omega\mathrm{m}$
ρ_a	$18.15 \cdot 10^{-8}\,\Omega\mathrm{m}$
ρ_w	$0.20\,\Omega\mathrm{m}$
g_{i_1}	$0.055\,\mu\mathrm{S/km}$
$g_{i_2} = g_{i_3}$	$1.3\,\mu\mathrm{S/km}$
$\mu_{r_c} = \mu_{r_s} = \mu_{r_{i_1}} = = \mu_{r_{i_2}} = \mu_{r_{i_3}}$	1
μ_{r_a}	10

spectively with the subscripts $_c$, $_s$, and $_a$) at a given distance x along the cable are linked to one another as

$$\frac{d}{dx}\begin{bmatrix} v_c \\ v_s \\ v_a \end{bmatrix} = \underbrace{\begin{bmatrix} z_{\mathrm{cc}} & z_{\mathrm{cs}} & z_{\mathrm{ca}} \\ z_{\mathrm{sc}} & z_{\mathrm{ss}} & z_{\mathrm{sa}} \\ z_{\mathrm{ac}} & z_{\mathrm{as}} & z_{\mathrm{aa}} \end{bmatrix}}_{\boldsymbol{Z}} \begin{bmatrix} \imath_c \\ \imath_s \\ \imath_a \end{bmatrix}, \quad \frac{d}{dx}\begin{bmatrix} \imath_c \\ \imath_s \\ \imath_a \end{bmatrix} = \underbrace{\begin{bmatrix} y_{\mathrm{cc}} & y_{\mathrm{cs}} & y_{\mathrm{ca}} \\ y_{\mathrm{sc}} & y_{\mathrm{ss}} & y_{\mathrm{sa}} \\ y_{\mathrm{ac}} & y_{\mathrm{as}} & y_{\mathrm{aa}} \end{bmatrix}}_{\boldsymbol{Y}} \begin{bmatrix} v_c \\ v_s \\ v_a \end{bmatrix}, \tag{3.2}$$

where $\boldsymbol{Z}$ and $\boldsymbol{Y}$ are the cable impedance and admittance matrices expressed in per-unit length. Equations (3.4) and (3.5) report the formulas of every self and mutual impedance and admittance: these computations can be easily adapted to a varying number of conducting and insulating layers [133]. To retrieve the entries of the matrices $\boldsymbol{Z}$ and $\boldsymbol{Y}$, either accurate [133] or approximate [134] formulas can be used. The latter, adopted in Eq. (3.5), are generally used for simulation purposes because they grant higher stability and speed of solution [101].[1]

The term γ in the expression of z_{11} in Eq. (3.5) corresponds to Euler's constant, while ω is the angular frequency considered. The variable m_i ($i \in \{c, s, a, w\}$) is the inverse depth of penetration, defined as

$$m_i = \sqrt{\frac{\mathbb{j}\mu_0\mu_{r_i}}{\rho_i}}\,, i \in \{c, s, a, w\}\,. \tag{3.3}$$

[1]For the sake of simplicity, the mutual coupling between the two DC lines in Fig. 3.1 is neglected. Among others, this aspect is thoroughly detailed and taken into account in [101, 133].

$$
\begin{aligned}
z_{\mathrm{cc}} &= z_1 + z_2 + z_3 - 2z_4 + z_5 + z_6 + z_7 - 2z_8 + z_9 + z_{10} + z_{11} \\
z_{\mathrm{ss}} &= z_5 + z_6 + z_7 - 2z_8 + z_9 + z_{10} + z_{11} \\
z_{\mathrm{aa}} &= z_9 + z_{10} + z_{11} \\
z_{\mathrm{cs}} &= z_{\mathrm{sc}} = -z_4 + z_5 + z_6 + z_7 - 2z_8 + z_9 + z_{10} + z_{11} \\
z_{\mathrm{ca}} &= z_{\mathrm{ac}} = z_{\mathrm{sa}} = z_{\mathrm{as}} = -z_8 + z_9 + z_{10} + z_{11} \\
y_{\mathrm{cc}} &= y_1 \\
y_{\mathrm{ss}} &= y_1 + y_2 \\
y_{\mathrm{aa}} &= y_2 + g_w \\
y_{\mathrm{cs}} &= y_{\mathrm{sc}} = -y_1 \\
y_{\mathrm{sa}} &= y_{\mathrm{as}} = -y_2 \\
y_{\mathrm{ca}} &= y_{\mathrm{ac}} = 0
\end{aligned}
\tag{3.4}
$$

$$
\begin{aligned}
z_1 &= \tfrac{\rho_c m_c}{2\pi \imath_1} \coth\left(0.777 m_c \imath_1\right) + \tfrac{0.356\rho_c}{\pi \imath_1^2} \\
z_2 &= \mathbb{j} \tfrac{\omega \mu_0 \mu_{r_{i_1}}}{2\pi} \ln\left(\tfrac{\imath_2}{\imath_1}\right) \\
z_3 &= \tfrac{\rho_s m_s}{2\pi \imath_2} \coth\left(m_s(\imath_3 - \imath_2)\right) - \tfrac{\rho_s}{2\pi \imath_2(\imath_2 + \imath_3)} \\
z_4 &= \tfrac{\rho_s m_s}{\pi(\imath_3 + \imath_2)} \operatorname{csch}\left(m_s(\imath_3 - \imath_2)\right) \\
z_5 &= \tfrac{\rho_s m_s}{2\pi \imath_3} \coth\left(m_s(\imath_3 - \imath_2)\right) + \tfrac{\rho_s}{2\pi \imath_3(\imath_3 + \imath_2)} \\
z_6 &= \mathbb{j} \tfrac{\omega \mu_0 \mu_{r_{i_2}}}{2\pi} \ln\left(\tfrac{\imath_4}{\imath_3}\right) \\
z_7 &= \tfrac{\rho_a m_a}{2\pi \imath_4} \coth(m_a(\imath_5 - \imath_4)) - \tfrac{\rho_a}{2\pi \imath_4(\imath_5 + \imath_4)} \\
z_8 &= \tfrac{\rho_a m_a}{\pi(\imath_5 + \imath_4)} \operatorname{csch}\left(m_a(\imath_5 - \imath_4)\right) \\
z_9 &= \tfrac{\rho_a m_a}{2\pi \imath_5} \coth\left(m_a(\imath_5 - \imath_4)\right) + \tfrac{\rho_a}{2\pi \imath_5(\imath_5 + \imath_3)} \\
z_{10} &= \mathbb{j} \tfrac{\omega \mu_0 \mu_{r_{i_3}}}{2\pi} \ln\left(\tfrac{\imath_6}{\imath_5}\right) \\
z_{11} &= \mathbb{j} \tfrac{\omega \mu_0 \mu_{r_w}}{2\pi} \left(-\ln\left(\tfrac{\gamma m_w \imath_6}{2}\right) + \tfrac{1}{2} - \tfrac{4}{3} m_4 h\right) \\
y_1 &= g_{i_1} + \mathbb{j}\omega c_{i_1} = g_{i_1} + \mathbb{j} \tfrac{\omega 2\pi \varepsilon_0 \varepsilon_{r_{i_1}}}{\ln\left(\frac{\imath_2}{\imath_1}\right)} \\
y_2 &= g_{i_2} + \mathbb{j}\omega c_{i_2} = g_{i_2} + \mathbb{j} \tfrac{\omega 2\pi \varepsilon_0 \varepsilon_{r_{i_2}}}{\ln\left(\frac{\imath_4}{\imath_3}\right)} \\
y_3 &= g_{i_3} + \mathbb{j}\omega c_{i_3} = g_{i_3} + \mathbb{j} \tfrac{\omega 2\pi \varepsilon_0 \varepsilon_{r_{i_3}}}{\ln\left(\frac{\imath_6}{\imath_5}\right)}
\end{aligned}
\tag{3.5}
$$

By resorting to Kron reduction, a single value of impedance z_{cable} can be obtained, which includes the interaction between the core and the passive conducting layers (i.e., sheath and armour). In other words, the analytical representation of the submarine cable with any number of conducting layers

reduces to that of an equivalent conductor. To do so, it is assumed that both the armour and sheath are at ground potential along the entire length of the cable, so that $v_s = v_a = 0$.[2] As a result, z_{cable} can be derived through the following mathematical steps.

$$\begin{aligned} \frac{d}{dx}\begin{bmatrix} v_c \\ 0 \\ 0 \end{bmatrix} &= \underbrace{\begin{bmatrix} z_{\text{cc}} & z_{\text{cs}} & z_{\text{ca}} \\ z_{\text{sc}} & z_{\text{ss}} & z_{\text{sa}} \\ z_{\text{ac}} & z_{\text{as}} & z_{\text{aa}} \end{bmatrix}}_{\boldsymbol{Z}} \begin{bmatrix} \imath_c \\ \imath_s \\ \imath_a \end{bmatrix} \\ \frac{d}{dx} v_c &= \underbrace{\left(z_{\text{cc}} - \begin{bmatrix} z_{\text{cs}} & z_{\text{ca}} \end{bmatrix} \begin{bmatrix} z_{\text{ss}} & z_{\text{sa}} \\ z_{\text{as}} & z_{\text{aa}} \end{bmatrix}^{-1} \begin{bmatrix} z_{\text{sc}} \\ z_{\text{ca}} \end{bmatrix} \right)}_{z_{\text{cable}}} \imath_c \end{aligned} \tag{3.6}$$

The same approach can be used to derive a single value of admittance y_{cable}, which in this case coincides with y_{cc}.

By sweeping ω in Eq. (3.5) across a given interval, the cable resistance, inductance, conductance and capacitance as a generic function of frequency are computed as

$$\begin{aligned} r(\omega) &= \text{Re}\{z_{\text{cable}}(\omega)\} \\ l(\omega) &= \tfrac{1}{\omega}\text{Im}\{z_{\text{cable}}(\omega)\} \\ g(\omega) &= \text{Re}\{y_{\text{cable}}(\omega)\} \\ c(\omega) &= \tfrac{1}{\omega}\text{Im}\{y_{\text{cable}}(\omega)\}\,. \end{aligned} \tag{3.7}$$

Based on the approach outlined above, the data in Fig. 3.3, and Table 3.3, the frequency behaviour of $r(\omega)$, $l(\omega)$, given by the dashed black lines in Fig. 3.4 is obtained. Both parameters exhibit a strong frequency dependency due to skin effect, based on which the line resistance and inductance respectively increase and decrease with frequency. On the contrary, due to the admittance formulas used in Eq. (3.5), the per-unit length line conductance and capacitance have no frequency dependency (indeed, here it is assumed that $g(\omega) = g = 0.055\ \frac{\mu\text{S}}{\text{km}}$ and $c(\omega) = c \approx 0.2185\ \frac{\mu\text{S}}{\text{km}}\,, \forall\omega$). This assumption is usually put forward in power system studies [135].

3.1.2.2 Vector fitting (VF)

As shown in the next section, the vector fitting (VF) method is used to build a cable model that takes into account the frequency dependency of the line

[2] In reality, this is not true, since these two layers are typically grounded only at their ends. However, this assumption is deemed acceptable for converter control studies [135].

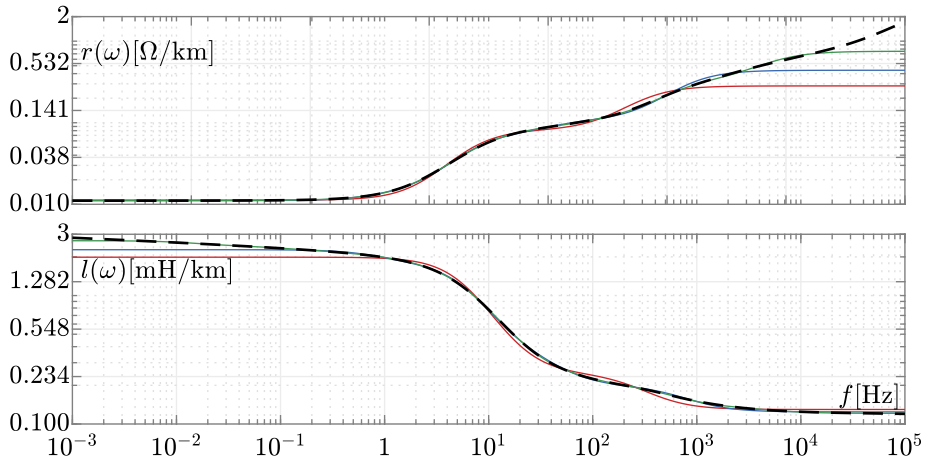


Figure 3.4: *Per-unit length cable resistances $r(\omega)$ and inductances $l(\omega)$. The dashed black lines refer to the theoretical values computed with Eqs. (3.4) and (3.5), based on the data in Table 3.3. On the contrary, the red, blue, and green solid lines correspond to the values obtained by applying the* VF *method to $z_{\mathrm{cable}}(\omega)$ and using an approximation order respectively equal to* 3*,* 5*, and* 10 *(see Section 3.1.2.3).*

resistance and inductance [135].

This method allows describing a measured or calculated frequency domain response $f(s)$ through a rational transfer function. Despite being originally adopted to build frequency-dependent models of cables and transformers [95], a wide array of applications has made use of this method over the years. For example, the authors in [136] use VF and measured data to derive a black-box model of a dynamic load. In [137], the VF method automatically identifies the electrical components of a circuit. VF was also recently used to model the transfer function of a grid-following inverter [138]. In the next chapter, this method is used for a similar purpose.

In short, VF approximates $f(s)$ through the partial fraction expansion

$$f(s) = \sum_{n=1}^{N} \frac{c_n}{s - a_n} + d + sh \ , \tag{3.8}$$

where N is the order of approximation, while a_n and c_n are respectively the poles and residues of the transfer function. The terms d and h, corresponding to a constant gain and a frequency-proportional term, are optional, as their presence depends on the fitted frequency response. VF estimates the parameters above by initially guessing the approximation order N and sequentially solving two stages.

The first stage derives the poles a_n by adopting an iterative procedure that relies on their initial estimate (typically logarithmically spaced over the frequency range of interest) and a scaling function. In each iteration, poles are relocated until a convergence criterion is attained. Should this criterion not be satisfied after a given number of iterations, the algorithm increases the approximation order N and repeats the first stage. Then, the second stage solves (3.8) as a least-squares problem. Besides, since the frequency response $f(s)$ is evaluated at several frequency points, Eq. (3.8) leads to an over-determined system of equations, where $f(s)$ and the poles a_n are known parameters, whereas c_n, d, and h are the unknowns.

The performance of the VF method depends on different factors, such as the initial poles estimate and the approximation order, as well as the adoption of a weighting function, which can improve the fitting results in a given frequency interval or minimize the relative fitting error rather than its absolute value. The interested reader can refer to [94, 95, 139] for more details about the VF algorithm and some of its further enhancements over time. A software package to perform VF can be downloaded at [140].

3.1.2.3 Frequency-dependent cable model

Over the years, scholars proposed several line models that allow taking into account the frequency dependency of line parameters (i.e., resistance and inductance, in the case of this work). Some of them are described in [61]. The Universal Line Model (ULM), thoroughly detailed in [141, 142], ranks among the most popular and accurate ones. However, other than being relatively more complex to implement, an additional drawback is the presence of delay blocks associated with propagation delays. These blocks make this model incompatible with state-space representations that could be used for stability analyses of HVDC systems.

To address this issue[3], the model described in [135] and shown in Fig. 3.5 is adopted. It comprises a cascaded connection of n_p identical π sections[4], whose transverse parameters are equal to $G = g\frac{\ell}{n_p}$ and $C = c\frac{\ell}{n_p}$ (with ℓ being the DC line length). In classic π sections, the longitudinal line parameters are associated with a single resistive-inductive branch. On the contrary, the model in Fig. 3.5 comprises n_b parallel $R - L$ branches for each section. As for G and C, the value of each resistance R_n $(n \in \{1, 2, ..., n_b\})$ amounts to $r_n\frac{\ell}{n_p}$, with r_n being the corresponding per-unit lenght value (analogous calculations hold for the inductances L_n and their per-unit length

[3] As explained in Section 4.4, this issue is more relevant for the studies performed in Chapter 4.

[4] This cascaded connection approximates the effect of the hyperbolic correction factors in the computation of lumped line parameters. For further information, refer to [143, 144].

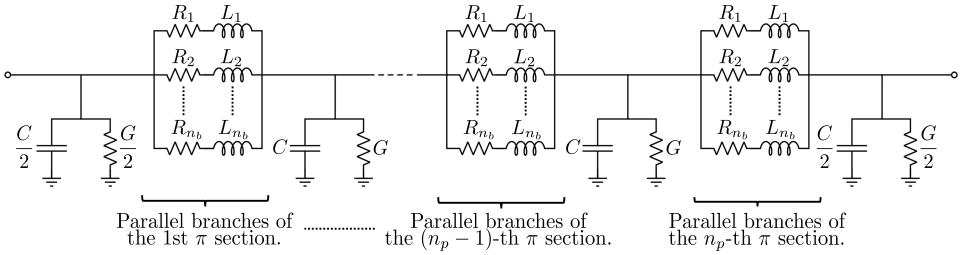


Figure 3.5: *Cable modelling approach adopted in this thesis.*

counterparts l_n). The VF method is employed to determine the values of r_n and l_n of each branch by fitting $z_{\text{cable}}(\omega)^{-1}$ as

$$z_{\text{cable}}(\omega)^{-1} = \sum_{n=1}^{n_b} \frac{c_n}{s - a_n}\,, \tag{3.9}$$

where the constant and proportional terms d and h (see Eq. (3.8)) are omitted. Since the parallel connection of $R - L$ branches leads to a per-unit length series admittance $z_{\text{cable}_{\text{fit}}}(\omega)^{-1}$ equal to

$$z_{\text{cable}_{\text{fit}}}(\omega)^{-1} = \sum_{n=1}^{n_b} \frac{1}{l_n s + r_n}\,, \tag{3.10}$$

it is straightforward to derive that $l_n = c_n^{-1}$ and $r_n = -a_n c_n^{-1}$.

The red, blue, and green curves in Fig. 3.4 show the fitted series resistances and inductances obtained by setting a value of n_b respectively equal to 3, 5, and 10. On the one hand, the higher n_b, the more accurate the fitting procedure becomes. On the other hand, it increases the number of components in each line, thereby leading to a higher computational burden. In this work, n_b was set to 5: as observed during simulations, this results in a good compromise between CPU time and simulation accuracy.[5] The resulting line parameters are listed in Table 3.4.

3.1.3 MMC parameters

As previously stated, the MMC control strategy described in [61] and Section 1.3 can only deal with balanced voltages and currents. This control

[5]By looking at Fig. 3.4, the adoption of $n_b = 5$ implies that the fitted resistance $r(\omega)$ (blue line) differs from the true one (black dashed line) at frequencies higher than about 600 Hz. In the following simulations, the frequency of interest of the electrical variables at the DC side does not exceed this value, which makes $n_b = 5$ acceptable. On the contrary, the fitted inductance $l(\omega)$ differs from the real one at frequencies lower than about 0.1 Hz. This is not an issue during simulations because at these frequencies inductance is less relevant than resistance, which is accurately fitted in the same frequency range.

Table 3.4: *Parameters of the cable model shown in Fig. 3.5 and adopted in this thesis.*

Parameter	Value	Parameter	Value
ℓ	$200\,\mathrm{km}$	g	$0.055\,\mu\mathrm{S/km}$
$n_p = n_b$	5	c	$0.2185\,\mu\mathrm{S/km}$
r_1	$2.1945\,\Omega/\mathrm{km}$	l_1	$0.2896\,\mathrm{mH/km}$
r_2	$0.1849\,\Omega/\mathrm{km}$	l_2	$0.2876\,\mathrm{mH/km}$
r_3	$0.2350\,\Omega/\mathrm{km}$	l_3	$1.4167\,\mathrm{mH/km}$
r_4	$0.0370\,\Omega/\mathrm{km}$	l_4	$4.3104\,\mathrm{mH/km}$
r_5	$0.0190\,\Omega/\mathrm{km}$	l_5	$5.4657\,\mathrm{mH/km}$

Table 3.5: *Parameters of the* MMC*s Cm-A1 and Cm-C1 in Fig. 3.1. Both of them share the same topology shown in Fig. 1.8.*

Parameter	Value	Comment
S_{nom}	$800\,\mathrm{MVA}$	Nominal power
$V_{\mathrm{dc_{nom}}}$	$400\,\mathrm{kV}$	Nominal pole-to-pole DC-side voltage
$V_{\mathrm{ac_{nom}}}$	$245\,\mathrm{kV}$	Nominal line-to-line RMS AC-side voltage
f_{nom}	$50\,\mathrm{Hz}$	Nominal frequency
N	200	Number of SMs per arm
R_{T}	$0.363\,\Omega$	Grid resistance (see Table 3.2)
L_{T}	$35\,\mathrm{mH}$	Grid inductance (see Table 3.2)
R_{S}	$1.31\,\mathrm{m}\Omega$	Arm resistance
L_{S}	$29\,\mathrm{mH}$	Arm inductance

strategy was modified as described in Appendix A to make it compatible also with unbalanced operating conditions. The Cm-A1 and Cm-C1 MMCs in Fig. 3.1 share the same topology depicted in Fig. 1.8, but their controls are different. Indeed, the former and the latter MMCs are defined respectively as of "DC-slack/Q" and "P/Q" type. By referring to the *upper level controls* in Fig. A.2, this means that the Cm-A1 MMC controls the DC-side voltage and reactive power, while the Cm-C1 MMC regulates active and reactive power. Regardless of the specific control strategy adopted, the general parameters of these two MMCs are listed in Tables 3.5 and 3.6. Section 3.1.5 defines the reference values (i.e., P^{ref}, Q^{ref}, and $v_{\mathrm{dc}}^{\mathrm{ref}}$) used in Fig. A.2 to control the two MMCs.

[6]The parameter $\imath^{\mathrm{lim}}$ is expressed in per-unit. Thus, it is very high: this means that no reference current is ever limited in practice. In Section 3.2.1, a value of $\imath^{\mathrm{lim}} = 1.1$ is adopted in one simulation to show the usefulness of the *reference current limiter* when faults occur and the accuracy of the isomorphism-based simulation method.

Table 3.6: *General control parameters of the Cm-A1 and Cm-C1* MMC*s used in this thesis.*

Parameter	Value	Comment
$H(s)$	$16.4\frac{s^2+(754)^2}{s^2+452s+(444)^2}\frac{s+92.4}{s}$	Parameters of the notch filters (NF) (Eq. (A.13)) and $H(s)$ regulator of the PLL in Fig. A.1
ω_0	$314\,\mathrm{rad/s}$	
w_c	$628\,\mathrm{rad/s}$	
Q_f	10	
k_{p_p}	0	Parameters of the PI regulators and *deadband control* used in the *upper level controls* in Fig. A.2
k_{i_p}	33	
$k_{p_{dc}}$	8	
$k_{i_{dc}}$	272	
k_{p_q}	0	
k_{i_q}	33	
$k_{p_{ac}}$	0.2	
$k_{i_{ac}}$	30	
$k_{p_{db}}$	10	
$v_{\mathrm{dc}_{\min}}$	$380\,\mathrm{kV}$	
$v_{\mathrm{dc}_{\max}}$	$420\,\mathrm{kV}$	
$\imath^{\lim}$	10	Parameters of the *reference current limiter* in Fig. 1.13[6]
Priority	**A**	
$k_{p_\imath}$	0.48	Parameters of the PI regulators in the *decoupled current control* in Fig. A.3(b)
$k_{i_\imath}$	149	
k_p	0.001	Parameters of the proportional-resonant (PR) filters (Eq. (A.17)) used in the *circulating current suppression control* in Fig. A.4
k_r	1	
w_c	2	
w_r	$628\,\mathrm{rad/s}$	
$v_{\mathrm{ac}_{\mathrm{lim}}}$	$24.5\,\mathrm{kV}$	Parameters of the MMC AC under-voltage and DC over-current protections in Fig. 1.17
T_{delay_1}	$20\,\mathrm{ms}$	
$\imath_{\mathrm{dc}_{\mathrm{lim}}}$	$6\,\mathrm{kA}$	
T_{delay_2}	$40\,\mu\mathrm{s}$	
T_{delay_3}	$50\,\mathrm{ms}$	

3.1.4 Details concerning full-physics, full-detailed, and bi-value resistor submodule models

Hereafter are given some details about the full physics (FP), full detailed (FD), and bi-value resistor (BVR) models of SMs used during simulations. Regardless of the model, the capacitance of each SM equals $C_{\mathrm{sm}} = 10\,\mathrm{mF}$.

For what concerns the FP SM model in Fig. 2.2(a), the following holds. Assuming that both Cm-A1 and Cm-C1 MMCs comprise 200 SMs per arm and they operate at a maximum pole-to-pole voltage of $480\,\mathrm{kV}$, the aver-

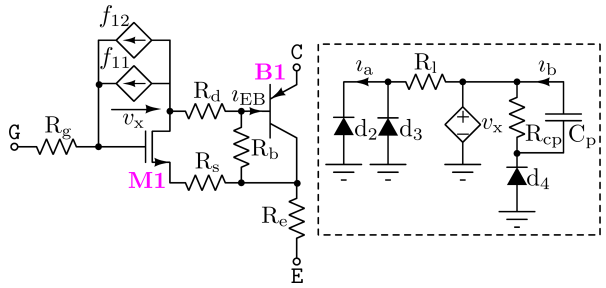


Figure 3.6: *The schematic of the sub-circuit implementing the model of the* ST3000GXH31A IGBT *adopted in Fig. 2.2(a). The* B1 BJT *is a* PNP *type, so its emitter corresponds to the collector terminal of the* IGBT *model.*

age working voltage across each SM capacitor should be no greater than $^{480\,\mathrm{kV}}/_{200} = 2.4\,\mathrm{kV}$. This value is compatible with the D2700U45X122 diode by Infineon and the ST3000GXH31A IGBT by Toshiba ($v_{\mathrm{ces}} = 4.5\,\mathrm{kV}$, $i_{\mathrm{dc}} = 3\,\mathrm{kA}$), both adopted in this model.

As specified in Section 2.1.1, the semiconductor devices in the FP SM model can be represented through detailed, non-linear dynamic representations based on built-in or macro models [103–106]. The ST3000GXH31A IGBT macro model disclosed by the manufacturer - whose schematic is depicted in Fig. 3.6 - is adopted. In brief, the collector-emitter current is conducted by the PNP-type B1 BJT. The BJT is turned on/off by the M1 MOSFET that can conduct a fraction of the total $\imath_{\mathrm{EB}}$ current. The modelling equations of the BJT and MOSFET (LEVEL2) can be found in [103]. The circuit in the dashed-box and the f_{12}, f_{11} controlled sources implement the non-linear charge characteristic of the gate, whose behaviour is governed by the D2, D3, and D4 diodes [103]. This non-linear charge characteristic is the main actor in determining the switching losses of the SM and the current flowing through the gate driver. The gate driver is *ideal* (i.e., it does not introduce any limitation in its branch current). The gate signal of each IGBT in every SM is given by a voltage-dependent source connected directly to the terminal G in Fig. 3.6 (note that the gate includes an internal resistance $\mathrm{R_g}$). The value of this source depends on the MMC *Capacitor voltage Balancing Algorithm (*CBA*)* and protection scheme (see Sections 1.3.4.3 and 1.3.5). In addition, the gate signals are shifted by $100\,\mathrm{ns}$ to avoid cross conduction, and their rising/falling fronts last $100\,\mathrm{ns}$.

When the FD model in Fig. 2.2(b) is adopted, the switches S_1 and S_2 are modelled as bi-value resistors, whose ON and OFF-state are associated with $1\,\mu\Omega$ and $1\,\mathrm{M}\Omega$ resistors, respectively (i.e., basically an *ideal* switch). The

diode model is analogous to the static one used in [103].

Lastly, as regards the BVR SM model in Fig. 2.2(c), the R_1 and R_2 resistances amount to $1.361\mathrm{m}\Omega$ or $1\mathrm{M}\Omega$ if their corresponding valves are ON or OFF, respectively [61]. Both the FD and BVR models neglect the rising/-falling fronts and dead-times of the gate signals.

3.1.5 Simulated scenarios

All the simulations described in the following sections were carried out with PAN simulator [145, 146] on a $1.8\,\mathrm{GHz}$ Intel i7, $14\,\mathrm{MByte}$ processor, whose RAM allocation never exceeded $100\,\mathrm{MByte}$.

By referring to Fig. 3.1, every simulation is structured as follows:

- The simulation starts with a start-up sequence. The SM capacitors are pre-charged to the value $v_{\mathrm{dc_{nom}}}/N$, the main breakers 1 and 2 are closed, and the start-up resistors are inserted (i.e., the bypass breakers 1 and 2 are opened). The active power and DC-side voltage setpoints (i.e., P^{ref} and $v_{\mathrm{dc}}^{\mathrm{ref}}$) of the Cm-C1 and Cm-A1 MMCs are respectively 0 and $400\,\mathrm{kV}$. The reactive power setpoint of both MMCs is null.

  One might argue that the start-up sequence is unnecessary if SM capacitors are already pre-charged. However, as mentioned in Section 1.4.2, it is important to recall that the initialization of MMCs is a complicated task and at a relatively early stage of development (consider for instance [77], which addresses this topic). At the time of writing, PAN simulator could not find an exact steady-state operating point of the system in Fig. 3.1 from the power flow results. In the light of the above, the start-up sequence serves as an *initialization transient*, which allows the state and algebraic variables of the system (MMCs included) to reach steady-state operation before some changes are applied (i.e., at $t = 0.15\,\mathrm{s}$). This ploy, however, comes at the expense of a higher simulation time. Note that this is a recurring problem also in other power system simulators.[7]

[7] Consider for instance [108], which simulates with EMTP-RV a grid similar to that in Fig. 3.1. Also in this case, the presence of MMCs and their controls causes initialization problems. Section IV.A of [108] and 4.10 of [147] explain how to deal with this issue using EMTP-RV. In a nutshell, all MMCs are connected in parallel to ideal voltage sources, which mirror their reference active and reactive power exchange. When computing the power flow solution, the MMCs are disregarded, and the ideal voltage sources (modelled either as PQ or PV busses [148]) are considered in their stead. Then, power system initialization is carried out: together with the AC grids, the ideal voltage sources are initialized (i.e., their magnitude and phase are automatically calculated). The only elements not initialized are the MMCs and their controls. When electromagnetic transient simulations start, the ideal voltage sources are still connected to the main grid, while the MMCs are not. After some time steps, these sources are disconnected and the MMCs are finally connected. Of course, such a strategy inevitably leads to initialization transients.

- At $t = 0.06\,\mathrm{s}$, both bypass breakers are closed (i.e., start-up resistors are short-circuited). Set-points are unaltered.
- At $t = 0.15\,\mathrm{s}$, the active power setpoint of the Cm-C1 is set to $-400\,\mathrm{MW}$ (i.e., power is injected from the AC-side to the HVDC link). The other setpoints remain unaltered.
- If tested, AC or DC faults (whose location is given by lightning bolts in Fig. 3.1) are applied at $t = 0.6\,\mathrm{s}$.

3.2 Simulation results

The isomorphism-based approach has three main properties, which are described in Section 2.2.3 and summarized hereafter. First, regardless of the SM model adopted, it can simulate MMCs in different operating conditions almost as accurately as conventional simulation paradigms that represent each SM individually. Second, by adopting the full physics (FP) model of SMs, the isomorphism-based approach allows examining internal variables (such as losses and semiconductor currents) in great detail and with a reasonable CPU time. Other approaches cannot do the same because they either adopt simpler SM models or lead to prohibitive simulation times. Third, the computational burden associated with isomorphism-based simulations increases almost linearly with the number of SMs per arm. On the contrary, in conventional simulation approaches, this trend is almost quadratic.

The following sections aim at demonstrating all of these features. Hereafter, several faults are studied as a pretext to showcase the compatibility of the isomorphism-based approach with a wide range of MMC operating conditions.

3.2.1 Analysis of simulation accuracy

To assess the accuracy of the isomorphism-based method, the scenarios considered in the following compare two simulation, hereafter referred to as **Iso** and **Conv**. The former relies on the isomorphism-based method, whereas the latter considers each SM individually (i.e., without using the proposed isomorphic simulation technique), and it is thus defined as *conventional*. Contrary to its **Iso** counterpart, this method leads to a high computational burden because it does not reduce the number of electrical nodes and variables.

The simulations shown in this subsection rely on the FD model of SMs and a fixed integration time step of $h = 4\,\mu\mathrm{s}$ instead of a variable one. This

choice stems from the fact that, due to its low computational efficiency, simulations based on the **Conv** approach last several days. If a variable h were used, CPU times would increase even more (the implications of using a variable or fixed h are detailed in Section 3.2.3).

The first scenario considered is a three-phase fault occurring in AC grid 2 (whose exact location is given by the ① mark in Fig. 3.1). The left and right column panels of Fig. 3.7 respectively report the simulation results obtained with the **Iso** and **Conv** approaches.[8] The results are in agreement with those in Chapter 6 of [61]. Before the fault, the *circulating current suppression strategy* and Capacitor voltage Balancing Algorithm (CBA) attenuate efficiently high-order harmonics in the arm currents and limit capacitor voltage deviations in the SMs. When the fault occurs, the AC-side currents of the Cm-C1 MMC increase and drop to zero after about $20\,\mathrm{ms}$, which is the time required by the protection system in Fig. 1.17 to open the main breaker 2 when under-voltages at the AC side are detected. Concurrently, the Cm-C1 MMC SMs become blocked, and its active power setpoint is disregarded: at steady-state, this corresponds to a null current at the AC-side of the Cm-A1 MMC and in the DC link. Indeed, Fig. 3.7 shows that both sets of currents go to zero to achieve a null power exchange.

By comparing the results obtained with the **Iso** and **Conv** approaches, the reader can notice that the capacitor voltage of a given SM in Cm-A1 MMC (bottom panel) is slightly different. Before the fault occurs, it seems that the SM is inserted and bypassed (i.e., its capacitor voltage practically remains constant) at different time instants in the two approaches. This happens for two main reasons: first, voltage deviations may be due to even slight differences in the simulation approaches and models adopted. Second, if the switching thresholds in the Nearest Level Modulation are not identically crossed in the **Iso** and **Conv** scenarios, time inaccuracy contributes to varying the voltage of the submodule capacitor even further. In turn, such deviations affect the behaviour of the voltage balancing and circulating current controller, thereby resulting in distinct switching sequences of the MMC in the two scenarios. This peculiarity was already reported in other papers dealing with MMC accelerated simulation models [120, 149]. In practical implementation terms, this has similar effects to electrical noise.

Despite these issues, the key features of the MMCs, such as maximum capacitor voltage ripple, pole-to-pole voltage, AC side current, and arm current in the two approaches are very similar. To provide the reader with an

[8] For the sake of readability, simulation results are shown between $0.5\,\mathrm{s}$ and $0.8\,\mathrm{s}$. The results in Fig. 3.15 show some electrical variables before $0.6\,\mathrm{s}$ (i.e., before any of the faults analyzed in this section occurs).

indication of the accuracy of the isomorphism-based approach, the fourth panel of Fig. 3.7 (left column) includes a number, which corresponds to the maximum Relative Squared Error (RSE) [150] obtained among the variables shown in all the panels. While computing the RSE, the results of the **Conv** approach are taken as reference, as it introduces no simplification.[9] This indicator is computed also for every other scenario.

Figures 3.8 and 3.9 depict the simulation results obtained by repeating the previous fault and changing the number of SMs in each arm N to 128 and 64, respectively. Except for an increased ripple in the DC-side voltage and current (given by a decrease in N, which coincides with the number of levels used in the modulation technique), the trend of the variables is analogous to that of Fig. 3.7. In addition, the comparison between the **Iso** and **Conv** approaches confirms that high simulation accuracy is still retained.

To further prove the accuracy of the isomorphism-based approach and show the usefulness of the *reference current limiter*, the fault in AC grid 2 was simulated again. In this case, the parameters $\imath^{\mathrm{lim}}$ and $T_{\mathrm{delay_1}}$ (see Table 3.6) were set to 1.1 and $1\mathrm{s}$, respectively. The increase in $T_{\mathrm{delay_1}}$ implies that MMCs withstand AC-side faults for an extended period before protections activate. Figure 3.10 shows the simulation results obtained in this case. Compared to Fig. 3.7, the change in $\imath^{\mathrm{lim}}$ makes the reference current limiter effective in preventing the fault current (see $\imath_{\mathrm{CmC1}}$) from rising excessively, which limits the converter contribution to faults in AC grids.

Lastly, Fig. 3.11 depicts the simulation results of a single-line to ground fault at AC grid 1 (see the ② mark in Fig. 3.1 for its exact location). The parameter $T_{\mathrm{delay_1}}$ was kept to $1\,\mathrm{s}$ to make the MMCs withstand the fault for longer. One can notice that the AC currents of the Cm-C1 MMC are still balanced, while those of the Cm-A1 MMC lose symmetry but quickly recover it after a transient. This is due to the presence of the *negative sequence control* in Fig. A.2, which regulates the d, q components of the negative sequence MMC AC-side current to zero. However, as shown in the third and fourth panels of Fig. 3.11 and reported in [151], the adoption of this control comes at the expense of significant DC-side voltage and current ripples when unbalances arise.

In conclusion, the results shown in Figs. 3.10 and 3.11 still confirm the accuracy of the isomorphism-based approach.

[9] This error was not computed for the last panel (i.e., SM capacitor voltage) because the **Iso** and **Conv** approaches might lead to different SM switching sequences. Thus, their comparison would be unfair.

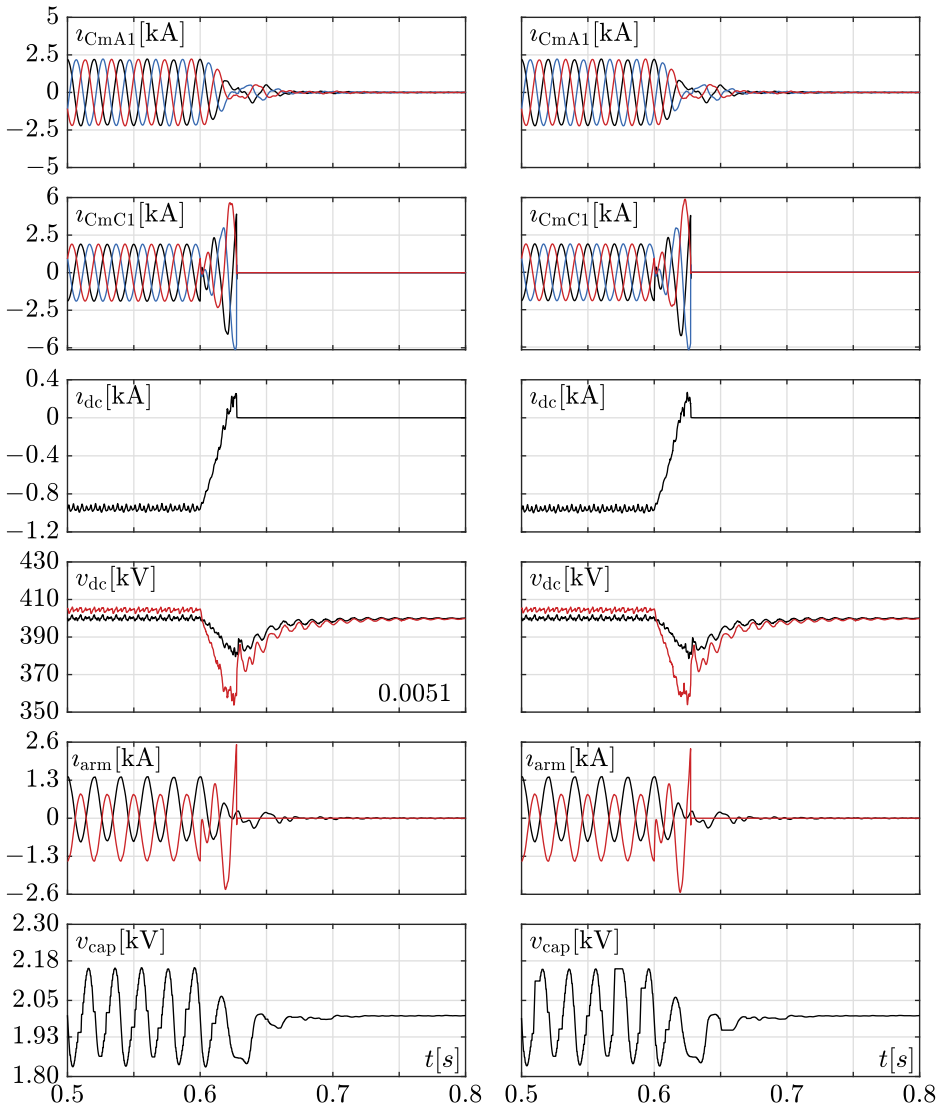


Figure 3.7: *Simulation results of a three-phase fault occurring in* AC *grid 2 at* 0.6 s*, obtained with the* ***Iso*** *(left column panels) and* ***Conv*** *(right column panels) approaches. From top: Panel 1 ($\imath_{\mathrm{CmA1}}$): three-phase* AC *currents of Cm-A1* MMC*. Panel 2 ($\imath_{\mathrm{CmC1}}$): three-phase* AC *currents of Cm-C1* MMC*. Panel 3 ($\imath_{\mathrm{dc}}$):* DC *current of Cm-C1* MMC*. Panel 4 (v_{dc}): pole-to-pole* DC *voltages at Bm-A1 (black) and Bm-C1 (red). Panel 5 ($\imath_{\mathrm{arm}}$): upper arm current in the phase a of* MMC*s Cm-A1 (black) and Cm-C1 (red). Panel 6 (v_{cap}): capacitor voltage of the most upward* SM *in the upper arm (phase a) of Cm-A1* MMC*. The number in the fourth panel of the left column corresponds to* RSE *of the variable plotted in the same panel. This number is obtained by comparing the results of* ***Iso*** *and* ***Conv*** *approaches, using the latter as reference (see Section 3.2.1).*

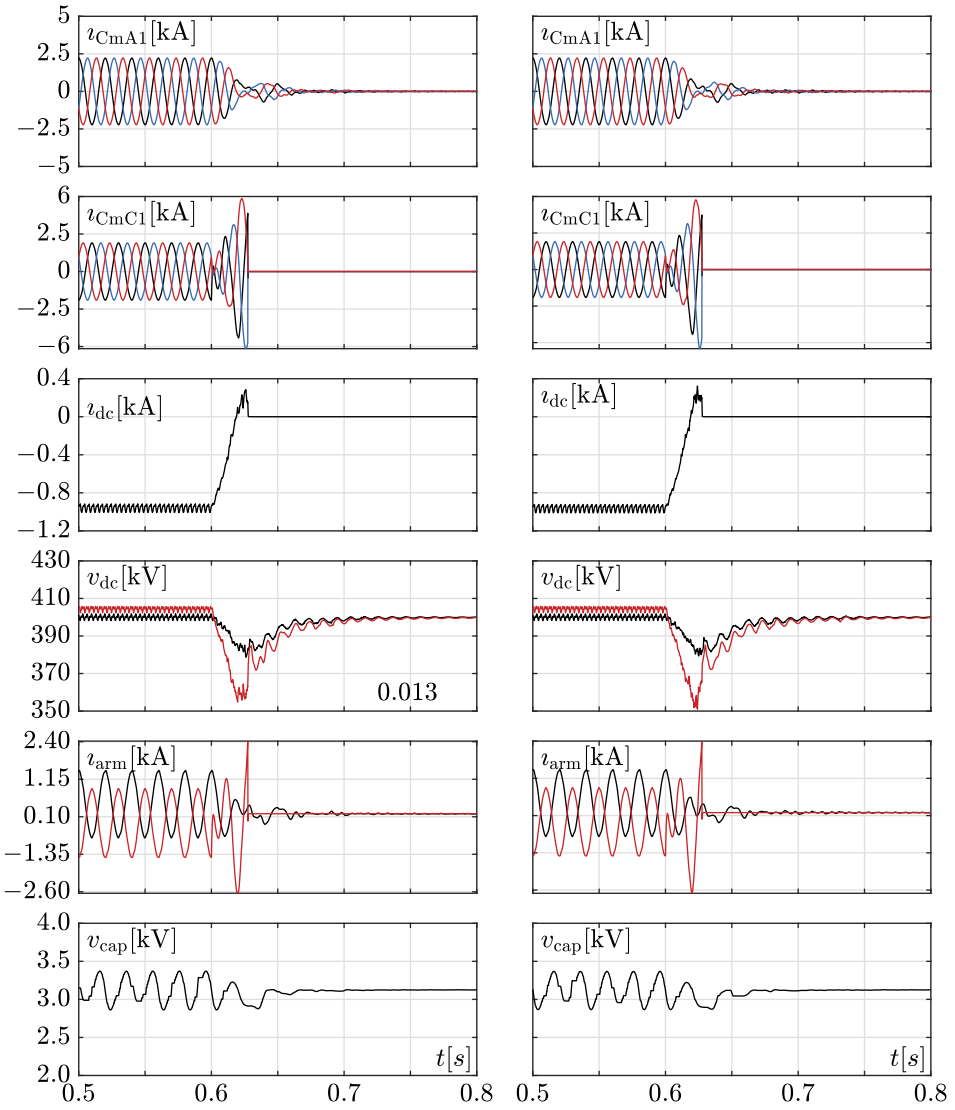


Figure 3.8: *Simulation results of a three-phase fault occurring in* AC *grid 2 at* 0.6 s*, obtained with the* ***Iso*** *(left column panels) and* ***Conv*** *(right column panels) approaches. Contrary to Fig. 3.7, in this case the number of* SMs *per arm in both* MMCs *is set to 128. Labels in panels have the same meaning as those in Fig. 3.7.*

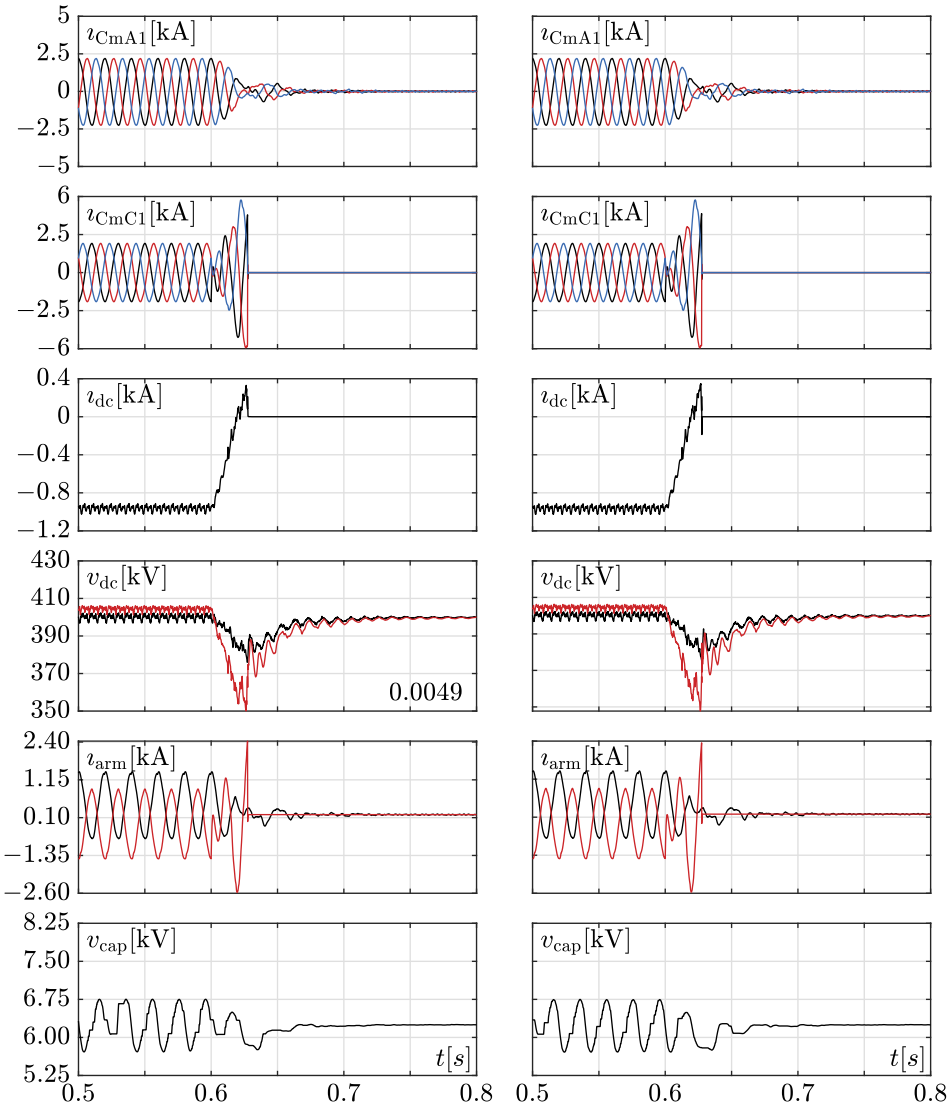


Figure 3.9: *Simulation results of a three-phase fault occurring in* AC *grid 2 at* 0.6 s*, obtained with the* ***Iso*** *(left column panels) and* ***Conv*** *(right column panels) approaches. Contrary to Fig. 3.7, in this case the number of* SM*s per arm in both* MMC*s is set to 64. Labels in panels have the same meaning as those in Fig. 3.7.*

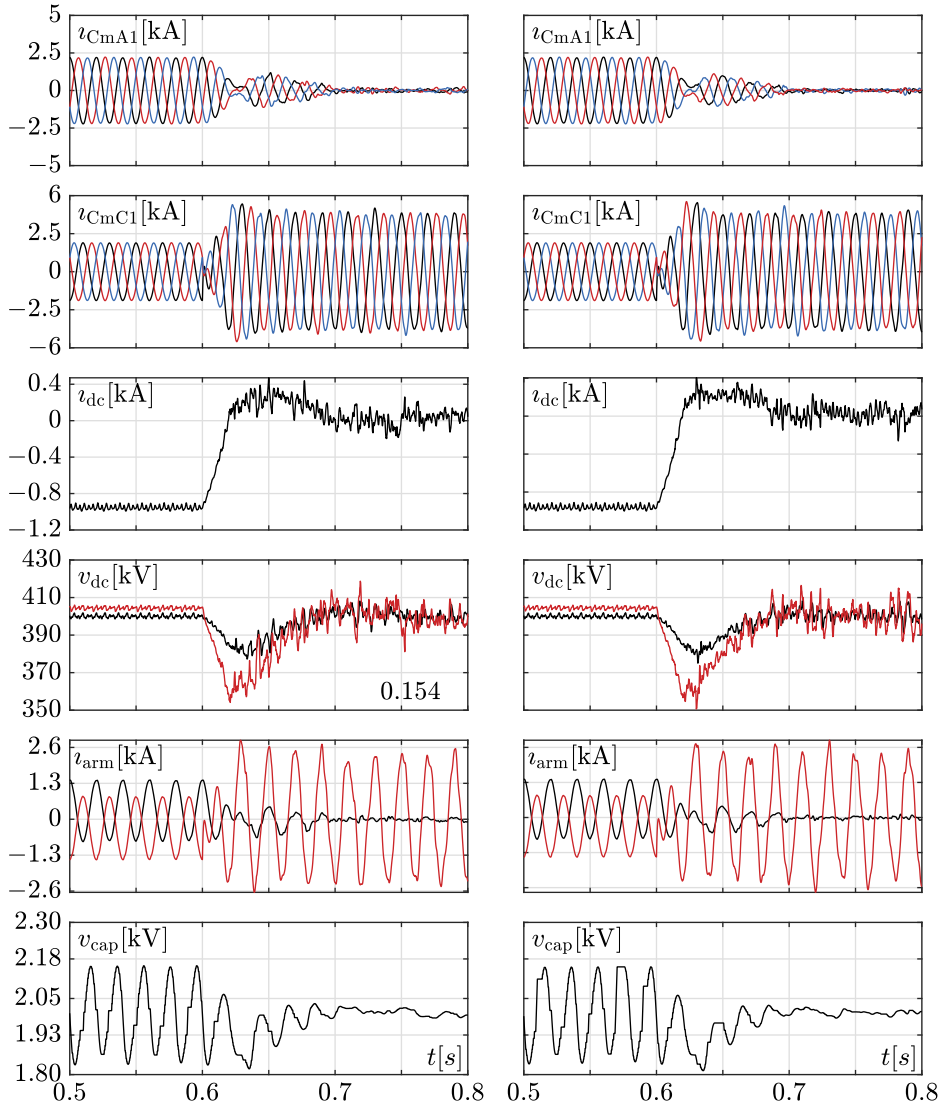


Figure 3.10: *Simulation results of a three-phase fault occurring at* AC *grid 2 at* 0.6 s*, obtained with the* ***Iso*** *(left column panels) and* ***Conv*** *(right column panels) approaches. Contrary to Fig. 3.7, in this case the parameter* i^{lim} *of the reference current limiter (see Fig. 1.13) is set to* 1.1*. Moreover, the fault is withstood for the whole simulation time. The number of* SM*s per arm in both* MMC*s remains the same (i.e., 200). Labels in panels have the same meaning as those in Fig. 3.7.*

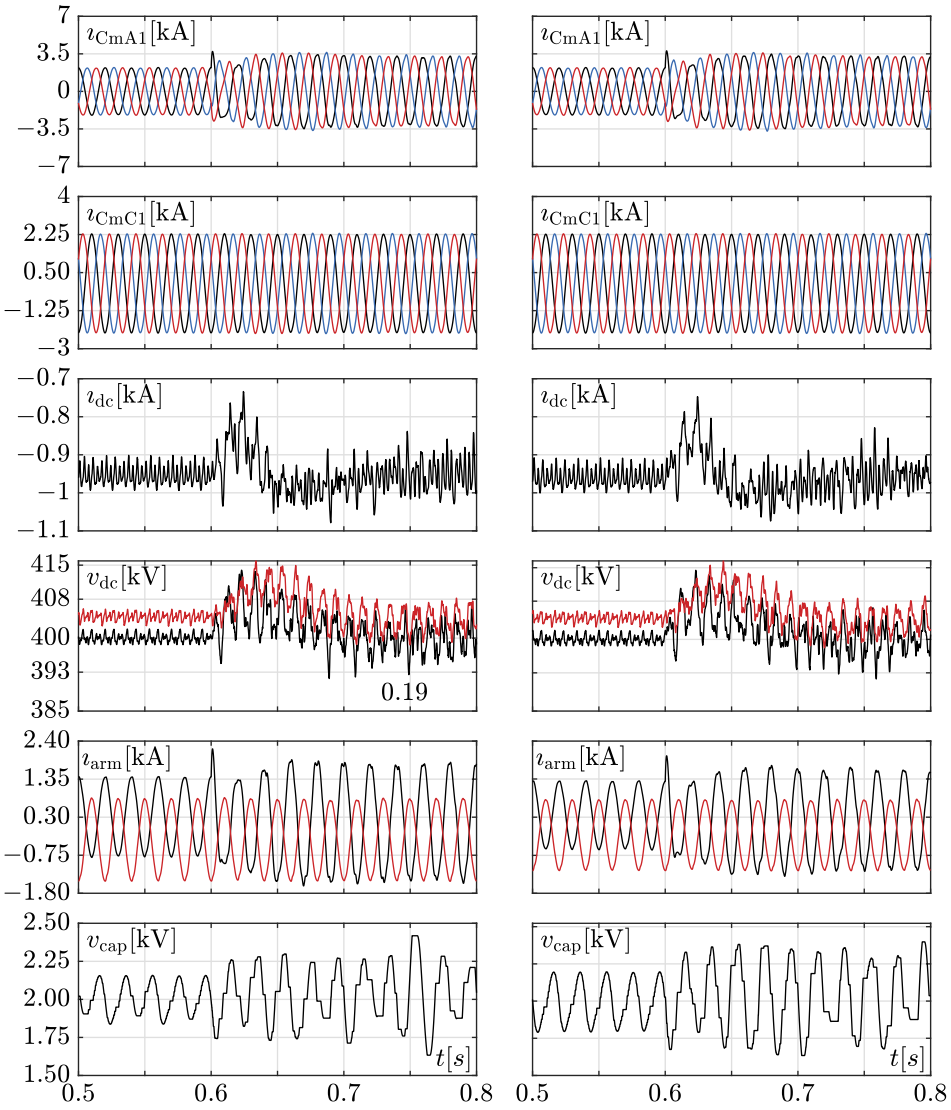


Figure 3.11: *Simulation results of a single-line to ground fault occuring in* AC *grid 1 at* 0.6 s*, obtained with the* ***Iso*** *(left column panels) and* ***Conv*** *(right column panels) approaches. The fault is withstood for the whole simulation time. Labels in panels have the same meaning as those in Fig. 3.7.*

3.2.2 Analysis of submodules variables

The case studies considered so far rely on the FD model of SMs and a fixed integration time step. However, it is worth recalling that an advantage of the isomorphism-based method is its compatibility with SM models of any degree of complexity. For instance, if the FP model is adopted, it is possible to analyze specific SM features, such as switching losses and IGBT currents during gate signal commutations.

To prove it, this section considers a three-phase to ground fault at AC grid 1 (denoted by the ② mark in Fig. 3.1). Specifically, this scenario adopts the FP SM model and an integration scheme based on variable time step h, with absolute and relative error tolerances on the electrical variables of 10^{-3} and 10^{-6}, respectively. The time step integration scheme relies on the implicit linear multi-step method by Gear up to order six or the trapezoidal method, used in several other EMT simulators such as EMTP-RV and PSCAD. These integration methods are thoroughly described in [98, 130, 152]. In this case, a fixed value of h was avoided because it would have been inefficient. Indeed, values of h in the order of ns are necessary to observe SM variables during gate signal commutations, which would lead to relatively high CPU times. On the contrary, with a variable time-step integration scheme, the simulation algorithm adjusts h acccording to circuit dynamics through the estimation of the local truncation error (ℓte), based on an optimal trade-off between accuracy and efficiency [98, 130].

Figure 3.12 reports the simulation results. Mirroring the case of Fig. 3.7, the AC-side currents of converter Cm-A1 start increasing right after the fault occurs. After $20\,\mathrm{ms}$, they drop to zero because the main breaker 1 is opened by the MMC under-voltage protection. At the same time, the SMs of the Cm-A1 MMC enter the blocked condition. The AC-side currents of the Cm-C1 MMC drop smoothly with some magnitude oscillations, and so does the HVDC link current. Contrary to Fig. 3.7, this is due to the presence of the *Deadband control* in Fig. A.2, which progressively lowers the absolute value of the reference current $\hat{\imath}_d^{p,\mathrm{ref}}$ of Cm-C1 MMC to achieve a null power exchange when the pole-to-pole voltage v_{dc} reaches $470\,\mathrm{kV}$, without requiring a blocking signal. The absence of this control would have resulted in a relentless increase in v_{dc} and, eventually, instability. Indeed, the power coming from converter Cm-C1 cannot be transferred to AC grid 1 because the Cm-A1 MMC is blocked. Thus, its SM capacitors inevitably absorb it, causing the previously mentioned increase in v_{dc}. In the light of the above, the *Deadband control* guarantees overall system stability, without the need for any communication between the converters [28].

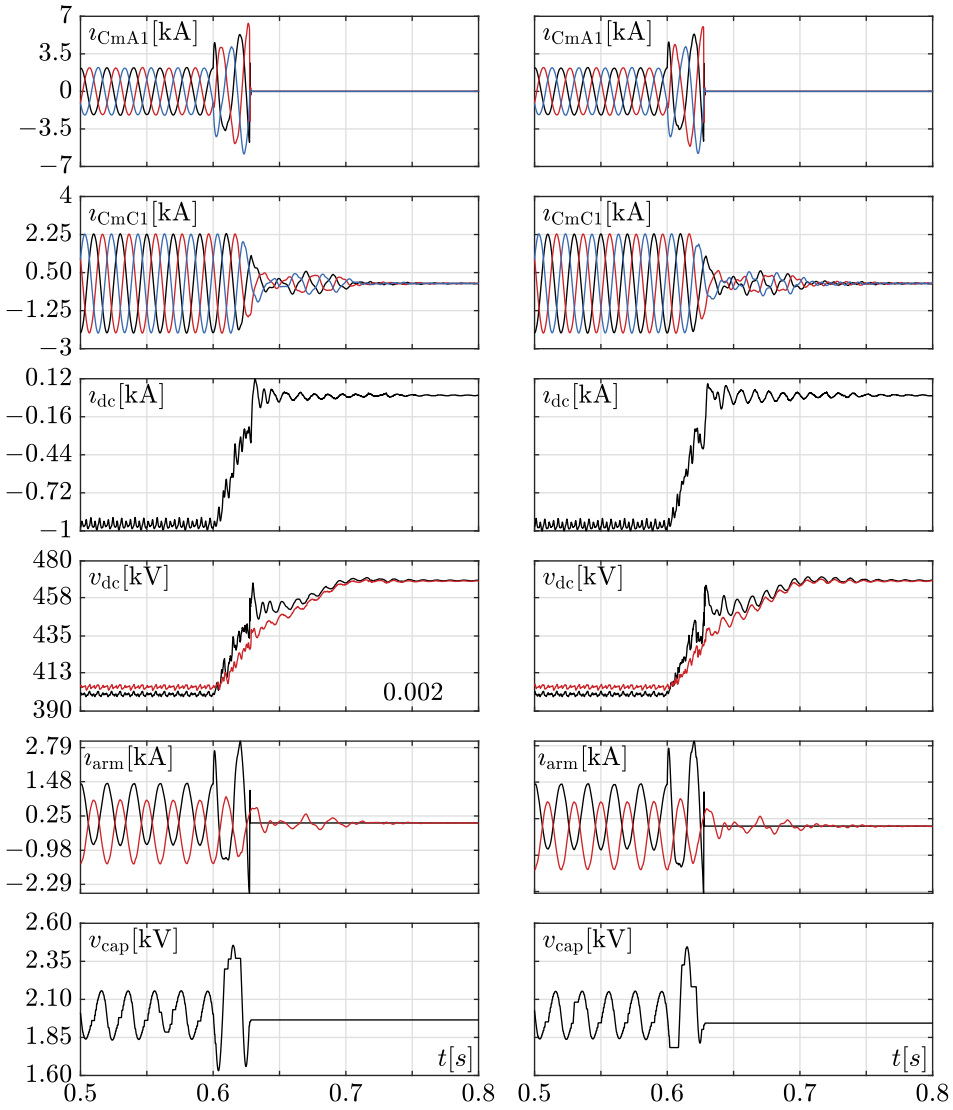


Figure 3.12: *Simulation results of a three-phase fault occurring in* AC *grid 1 at* 0.6 s*, obtained with the* ***Iso*** *(left column panels) and* ***Conv*** *(right column panels) approaches and the* FP *model of* SMs*. Labels in panels have the same meaning as those in Fig. 3.7.*

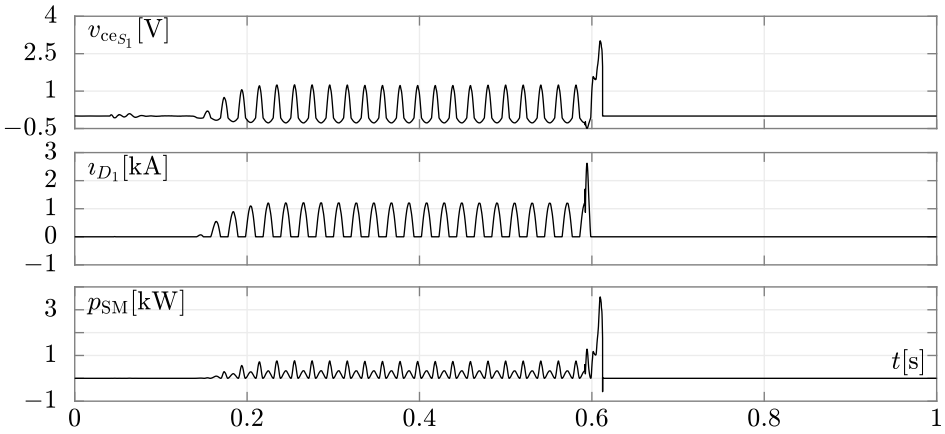


Figure 3.13: *From top: Panel 1:* S_1 IGBT *collector-emitter voltage. Panel 2:* D_1 *diode current. Panel 3:* SM *power losses. Results refer to a* SM *of the upper arm (phase a) of Cm-A1* MMC *in the* $\mathcal{C}^{\mathrm{in}}$ *class, considering the scenario simulated in Fig. 3.12.*

Since the isomorphism-based method is used, the details of the SMs inside each class are available. For instance, Fig. 3.13 depicts some variables of the equivalent SM of the upper arm (phase *a*) of Cm-A1 MMC associated with the $\mathcal{C}^{\mathrm{in}}$ class (see Fig. 2.14). Results refer to the previous case study. The variables shown are the collector-emitter voltage of S_1^{in} IGBT, the D_1^{in} diode current, and the SM power losses. When positive, the arm current flows through the S_1^{in} IGBT and its collector-emitter voltage is positive. On the contrary, when the arm current is negative, the IGBT does not conduct. Indeed, the arm current flows through the D_1^{in} antiparallel diode, thereby leading to a negative collector-emitter voltage.

According to Section 2.1, component level studies involve the analysis of voltage and current stresses, as well as conduction and switching losses inside SMs. They constitute a useful tool for, among others, the selection of the semiconductor devices employed in each SM. These highly detailed analyses can be carried out by resorting to the full physics (FP) model and the isomorphism-based method. For example, Fig. 3.14 reports some electrical variables of a single SM in the time interval between a single switching-off of the S_1 IGBT and the subsequent switching-on of the S_2 IGBT. The simulated scenario remains the same as before.

Panel B of Fig. 3.14 reports the v_{g_1} gate-emitter voltage of the S_1 IGBT at turn-off. The fall time amounts to $100\,\mathrm{ns}$. The corresponding gate voltage of the M1 MOSFET of the IGBT model in Fig. 3.6 is reported in Panel D. The inset of the same panel highlights the so-called Miller plateau, caused

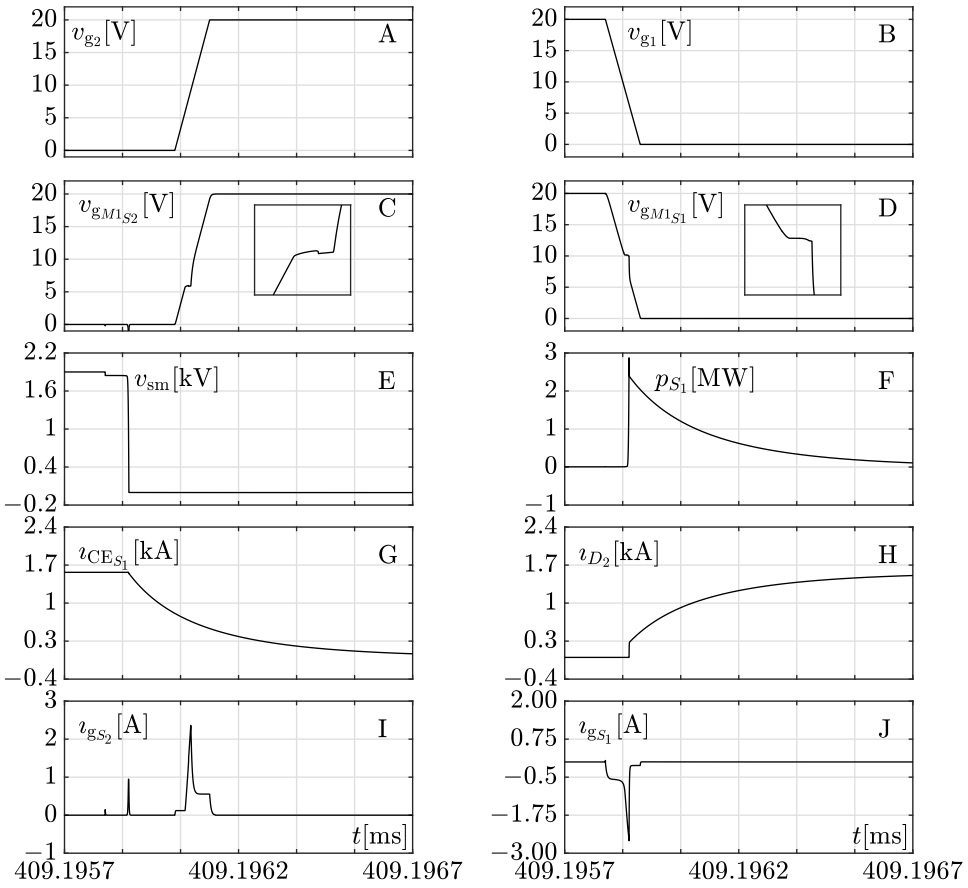


Figure 3.14: *Main waveforms during switching of a submodule described by a full physics model. Simulation results are obtained by adopting the isomorphism-based approach (**Iso**). Devices and circuit nodes to which waveforms refer to are those in Fig. 2.2(a) and Fig. 3.6. Panel* A*: the v_{g_2} gate-emitter voltage (turn-on) of the S_2* IGBT*. Panel* B*: the v_{g_1} gate-emitter voltage (turn-off) of the S_1* IGBT*. Panel* C*: voltage at the gate of the* M1 MOSFET *in Fig. 3.6 of the S_2* IGBT *model. Panel* D*: voltage at the gate of the* M1 MOSFET *in Fig. 3.6 of the S_1* IGBT *model. The Miller Plateau, given by the homonymous effect and highlighted in the insets of Panel* C *and* D*, is clearly visible. Panel* E*: the v_{sm}^{SW} voltage. Panel* F*: the instantaneous power dissipated by the S_1* IGBT*. Panel* G*: the collector-emitter current of the S_1* IGBT*. Panel* H*: the current through the D_2 diode. Panel* I*: the gate current of the S_2* IGBT*. Panel* J*: the gate current of the S_1* IGBT*. x-axis: time* [ms].

by the homonymous effect. The IGBT collector-emitter voltage starts to increase only when the Miller effect takes place (see Panel E, which depicts the SM voltage drop). The collector-emitter current of the IGBT is $1566\,\mathrm{A}$ (Panel G), which leads to a peak in the instantaneous switching losses of $2.77\,\mathrm{MW}$ (Panel F). The fall of the collector-emitter current of the IGBT is evident, and so is its current switching toward the D_2 diode (Panel H). Panel J shows the current of the S_1 IGBT ideal gate driver. After $100\,\mathrm{ns}$ from the falling edge of the gate driving waveform of the S_1 IGBT, there is the rising edge of the gate driving waveform of the S_2 IGBT, which also lasts $100\,\mathrm{ns}$ (Panel A). The inset of Panel B (i.e., the gate voltage of the M2 MOSFET) shows again the Miller effect. It is important to note that this kind of detail is not available in popular simulators such as PSCAD and EMTP-RV, whose MMC models rely only on simplified SM representations.

3.2.3 Analysis of simulation speed

As already mentioned, conventional simulation approaches, which consider each SM individually, lead to an almost quadratic increase in CPU time as the number N of SMs in each arm (and, thus, circuit complexity) grows. This behaviour is evident in the blue curve of Fig. 12 in [120] and the "Model 1" row of Table II in [79], which adopt the full detailed (FD) model of SMs and do not resort to further circuit simplifications. An analogous trend (but with different slopes) would be observed if the bi-value resistor (BVR) or full physics (FP) SM models were used. On the contrary, this trend becomes almost linear by exploiting the isomorphism-based approach.

To showcase this feature, the test system of Fig. 3.1 was considered once again by simulating a DC pole-to-pole fault at bus Bm-A1 (i.e., the ③ mark in Fig. 3.1). Analogously to Section 3.2.1, the FD SM model and a fixed integration time step of $h = 4\,\mu\mathrm{s}$ were adopted. Figure 3.15 depicts some simulation results obtained with the **Iso** approach for the entire simulation time (i.e., $1\,\mathrm{s}$). An inset of these results between 0.55 and $0.70\,\mathrm{s}$ is compared in Fig. 3.16 to those derived with the **Conv** approach. In this case, the DC overcurrent protection blocks the SM of both MMCs immediately after the fault (see T_{delay_2} in Table 3.6) so that their capacitor voltage can only increase but not decrease. Then, at about $0.65\,\mathrm{s}$, the MMC protection scheme opens the main breakers 1 and 2. It is important to underline that the DC line model adopted heavily influences the evolution of the HVDC link current $\imath_{\mathrm{dc}}$ after the fault. Indeed, if a simple cable model based on constant line parameters were adopted, its behaviour would have changed drastically.

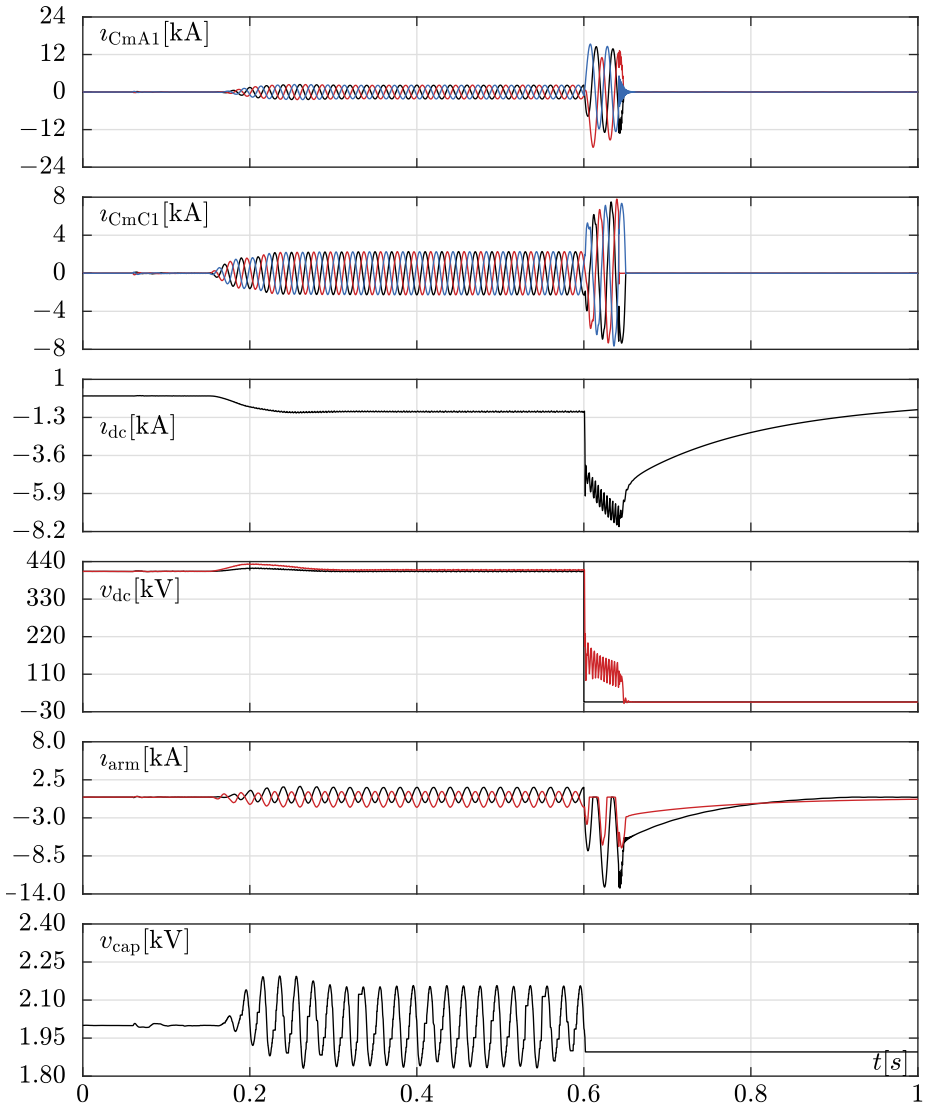


Figure 3.15: *Simulation results of a* DC *pole-to-pole fault at bus Bm-A1 occurring at* 0.6 s*, obtained with the proposed isomorphism-based approach (**Iso**) and shown for the whole simulation time (i.e.,* 1 s*). Labels in panels have the same meaning as those in Fig. 3.7.*

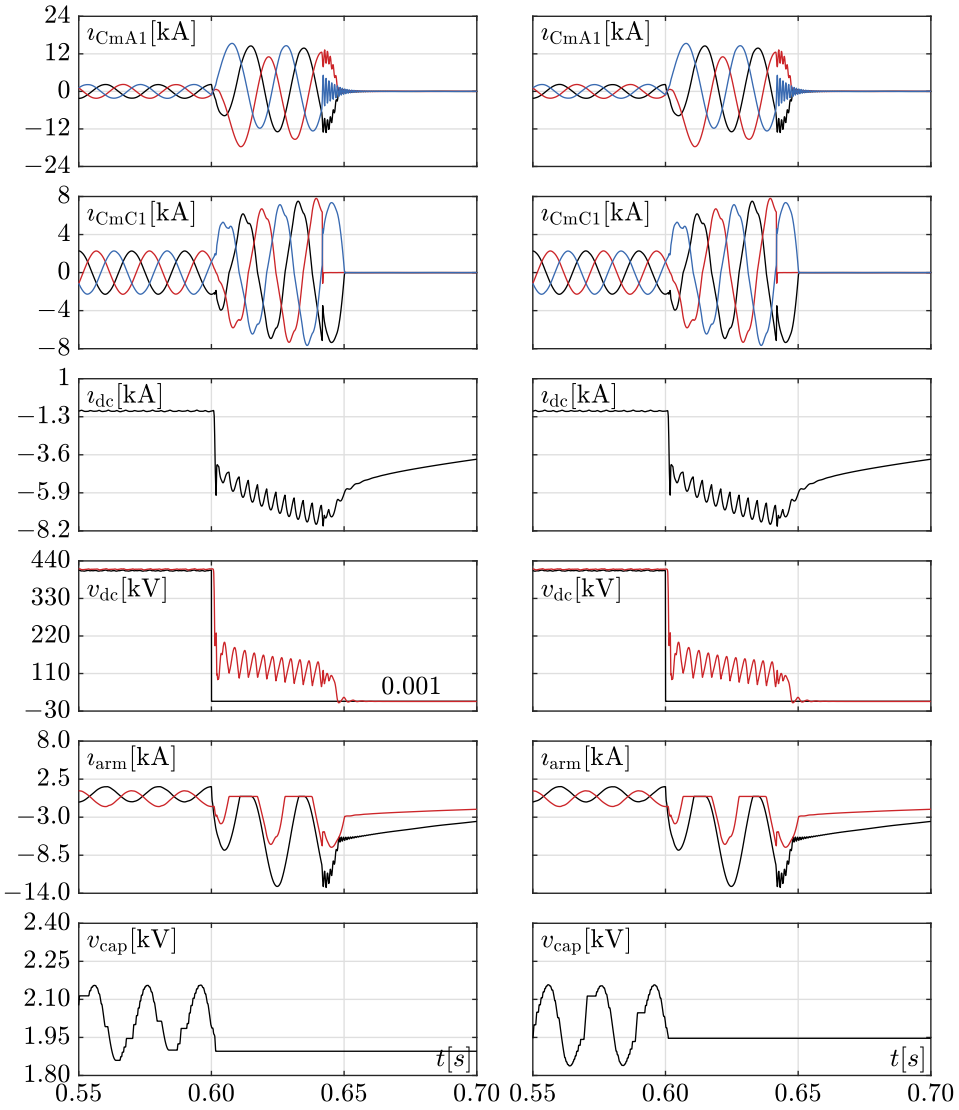


Figure 3.16: *Simulation results of a* DC *pole-to-pole fault at bus Bm-A1 occurring at* 0.6 s*, obtained with the* ***Iso*** *(left column panels) and* ***Conv*** *(right column panels) approaches and the* FP *model of* SM*s. The results in the left column panels are an inset of those in Fig. 3.15. Labels in panels have the same meaning as those in Fig. 3.7.*

The same simulation was repeated by varying N from 20 to 200 in both MMCs. Moreover, to demonstrate that the proposed isomorphism-based method allows the user to freely choose any SM model, different representations (i.e., FP, FD, and BVR) were considered while simulating.[10]

As done in most EMT simulators (e.g., EMTP-RV and PSCAD), a fixed h integration time step was adopted during most of the simulations. This integration scheme disregards the local truncation error (ℓte) introduced in computing the solution, whose accuracy is neither checked nor estimated [98, 99]. Thus, even though at each time point the Kirchhoff voltage and current laws are satisfied, the solution computed with the integration method (typically the implicit Euler or trapezoidal methods, see for example the EMTP-RV manual [98, 130]) might be affected by a large ℓte. On the contrary, variable time step integration schemes estimate the ℓte and, if too large, reduce h. Therefore, simulation accuracy is enhanced [98, 130] at the expense of simulation time, which increases because the solution may be computed at more time points.

Another aspect worth highlighting is how variable and fixed time step integration schemes deal with threshold crossings in the MMC Nearest Level Modulation (NLM). In the former case, if adequate absolute and relative tolerances are adopted, the time instants when these crossings occur are computed in the most accurate way. In the latter case, however, an error (known as *time jitter*) is introduced. Indeed, these time instants are tweaked and made to coincide with multiples of h (which is in this case fixed). As h increases, so does the time jitter. Since threshold crossings coincide with a given SM possibly changing its configuration (e.g., SM inserted or bypassed), this leads to a voltage drifting of each SM capacitor. For instance, if the time jitter is such that an inserted SM is shifted to the bypassed status later than it would be if a smaller time-step h was used, its capacitor voltage starts deviating (drifting) from its *true* value. In turn, this also affects leg voltage mismatch and, thus, circulating currents. Moreover, it is interesting to note that simulators such as EMTP-RV and PSCAD often introduce a time-lag of one integration time step h, which may worsen accuracy.[11]

[10] The change in the number of SMs per arm implies that the average working voltage across each SM capacitor (see Section 3.1.4) varies as well. Thus, for each simulation based on the FP-based SM representation, the semiconductor models of the IGBTs in each SM were suitably adapted to withstand the correct voltage values.

[11] In general, time-lags could be added for two reasons. First, to include delays associated with measurements and controls (this practice is not considered here). Second, to manage algebraic loops, which inevitably arise also due to the presence of closed loops in the MMC control strategy. These loops are a recurring, problematic aspect of several (circuit) simulators such as EMTP-RV, PSCAD, and SIMULINK. For instance, the Transient Analysis of Control Systems (TACS) solution engine of EMTP-RV deals with algebraic loops by adopting delay blocks that decouple different parts of the simulated system [153]. On the one hand, these blocks boost simulation speed, as algebraic loops no longer need to be solved at each time step. On the other hand, they introduce a numerical artefact that can compromise simulation accuracy and even system stability. On the contrary, algebraic loops are

Figure 3.17: CPU *time in [*s*] (shaded grey area) required to simulate the grid in Fig. 3.1 for* 1 s *(with a* DC *fault at* 0.6 s*) with the isomorphism-based method and different numbers of* MMC SM*s* N.

SM model	Integration time step h	Number of SMs per arm N 20	50	80	110	140	170	200
FD	variable	1206	2568	3623	4086	5095	5870	7097
FP	fixed	103	167	226	316	430	484	548
FD	fixed	116	176	262	333	450	508	578
BVR	fixed	50	86	132	180	246	278	312
Fixed time step h		60 µs	30 µs	18 µs	13 µs	9 µs	8 µs	7 µs

If $N = 200$, there are at least $200 \times 2 \times 2 \times 3 = 2400$ commutations per working period (200 SMs per arm, 2 commutations (ON/OFF) per period, 2 arms, 3 legs), corresponding to one commutation every $\hat{t} \approx 8.33\,\mu\text{s}$. This simple observation suggests that simulators based on a fixed h have to use a time step smaller than $\hat{t}$. Furthermore, if switching power losses have to be examined in thorough detail, h would need to be further reduced to two orders of magnitudes (thus setting an upper bound of $200\,\text{ns}$ in the simulations considered here) to accurately simulate also gate driving signals. Since a lower time step implies a higher computational burden, this may lead to numerical inefficiency [79, 108]. On the contrary, with a variable time step integration scheme, h is shortened to accurately identify threshold crossings and then possibly increased between subsequent ones to boost CPU times. In summary, selecting a suitable fixed value of h is a delicate choice that depends on the degree of simulation accuracy required.

Figure 3.18 and Table 3.17 report the CPU times required to perform the previously mentioned simulations. The times in the last row of Table 3.17 correspond to the values of h used in the simulations based on a fixed time step. In each case, h was set to be as large as possible to minimize CPU times but small enough to correctly identify threshold crossings in the NLM, which would have otherwise lead to inaccurate results. Since the analysis of IGBT gate driving signals and switching losses was not the focus of this section, time steps in the order of ns were not adopted.

The comparison among the first and the other rows of Table 3.17 highlights how the adoption of a fixed h instead of a variable one largely reduces simulation times, thereby boosting the simulation efficiency of the isomorphism-based method. Indeed, with a fixed h, the simulator com-

not an issue for the simulator used in this work [145, 146], which resorts to the Modified Nodal Analysis and differential algebraic equation (DAE) formulations to solve circuits [98, 99]. Thus, time-lags are not necessary.

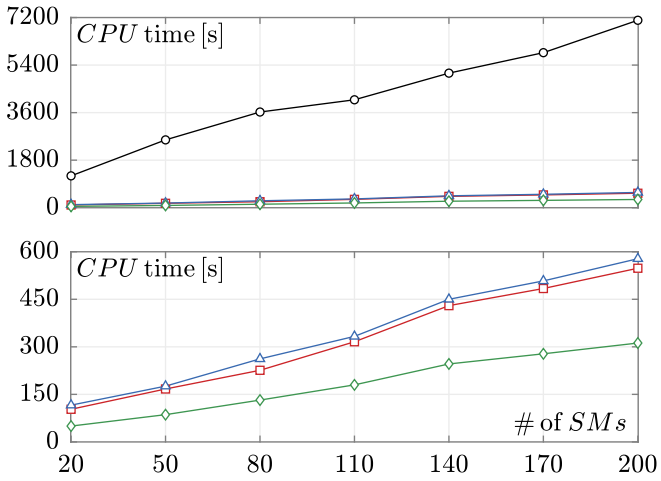


Figure 3.18: *Plot of the simulation times shown in Table 3.17. The black, red, blue, and green lines refer respectively to the cases "*FD*-variable h", "*FP*-fixed h", "*FD*-fixed h", and "*BVR*-variable h".*

putes the solution at a fewer time points than with a variable h.

What is stated so far, however, does not explain why the CPU times of the "FD-fixed h" case are higher than that of the "FP-fixed h" one (i.e., second and third rows of Table 3.17). Indeed, since the former SM model is less complex than the latter, one might be inclined to expect the opposite. The reason for this lies in the ideal commutations of switches in the FD model, which introduce more "time-discontinuities" in the solution than in the FP one (i.e., a much more dynamic variation of the solution from a time point to the next one is observed). This leads to more iterations with the Newton method to compute the solution at each time point and, thus, a higher CPU time. On the contrary, with a variable h, if too many Newton iterations are performed, the method is stopped, and h is shortened. In summary, the total CPU time depends on both h and the number of Newton iterations performed every time step.

It is worth pointing out that, as N increases, the results based on a fixed h become one or two orders of magnitude lower than those shown for instance in the "Model 1" row of Table II in [79], corresponding to the **Conv** approach based on the FD SM model. What is more, regardless of the SM model adopted, the CPU times become comparable to those shown in "Model 2" row of Table II in [79], based on the Thévenin Equivalent Model (TEM) described in Section 2.1.4 (which, thus, is only compatible with the BVR SM model). Of course, a rigorous comparison would require

simulations to be carried out with the same simulation engine and hardware.

In addition, the traces in Fig. 3.18 confirm that, by resorting to the isomorphism-based approach, the CPU time increases almost linearly with the number of SMs per arm N, with different slopes based on the SM model and the kind of integration time step employed.

Lastly, as mentioned in Section 2.1.1, simulations based on FP models are typically not considered in power system simulators because they lead to prohibitively high simulation times [61]. However, when the isomorphism-based approach is adopted, the increase in simulation time becomes tolerable. Indeed, Table 3.17 shows that the simulation times with a fixed h in the FP (and FD) case are only about twice those in the BVR one. The reason for this boost in simulation speed can be explained as follows. The IGBT sub-circuit in Fig. 3.6 contains K nodes. If the FP model and the **Conv** approach is adopted, simulating an MMC with $N = 200$ SMs per arm implies considering more than $6 \times 200 \times 2 \times K = 2400 \times K$ nodes.[12] On the contrary, with the **Iso** approach, this number reduces significantly because the SMs in each arm are not represented individually. Indeed, their evolution is derived by simulating a limited number of isomorphic classes. Assuming that only 4 isomorphic classes are simulated on average in each MMC arm, only (at least) $6 \times 4 \times 2 \times K = 48 \times K$ nodes need to be considered to implement an MMC, regardless of N. Since the number of nodes is reduced, so is the number of equations to be considered and the size of the nodal admittance matrix to be inverted at each time step. This ultimately leads to a boost in simulation time. The above holds also if the isomorphism-based method is applied when FD and BVR models of SMs are used, with the already discussed differences in terms of the computational burden.

[12]Note that the B1 BJT, the M1 MOSFET, and diodes in Fig. 3.6 add some "internal" nodes (i.e., extra nodes hidden to the user and automatically added by the simulator to handle the DAEs modelling the semiconductors). In the above counting, these nodes and those by controllers and drivers are neglected.

CHAPTER 4

Periodic small-signal analysis applied to modular multilevel converters

The small-signal analysis is a useful tool to establish if the operating point of a power system is stable or not, and to study how stability changes by varying some parameters, such as the regulator gains inside the control scheme of a synchronous generator. In general, grid stability can be assessed by deriving the "eigenvalues of the system", viz. the eigenvalues at the power flow solution of the Jacobian matrix of the differential algebraic equations (DAEs) governing the system dynamics. In some cases, however, power system designers limit themselves to study the equivalent admittances (or impedances)[1] measured or computed at some points of the grid. For instance, the presence of peaks in some frequency ranges could be an indication of possible resonance issues.

As better detailed in the following, in the case of conventional grids (i.e., those without converter-interfaced elements), three main approaches can be adopted to perform small-signal analysis. Their common trait is the reliance on two assumptions. While these hypotheses are typically valid in traditional power systems, they may not hold in modern grids due to, among

[1] The following sections indistinctly refer to either one of the two terms.

others, the presence of converters. To address this issue, over the years two out of the three methods mentioned above were updated and extended to modern power systems.

After a brief discussion of the previously mentioned aspects, in this chapter the so-called periodic small-signal analysis (PAC) is proposed as an extension to the remaining approach, thereby filling the gap in this context. This chapter explains the theoretical basis of this technique and how to apply it to analyse the small-signal behaviour of MMCs. To showcase the key features of PAC, the same benchmark system considered in Chapter 3 is exploited.

4.1 Small-signal approaches in conventional power systems

To begin with, it is worth pointing out that, by resorting to the Park transformation, the ABC-frame power system variables at steady-state operation correspond to a constant *equilibrium point* in the DQ0-frame. More precisely, this holds if two conditions are fulfilled. The first assumption is that the steady-state operation of the grid must have no harmonics. This implies that the ABC-frame variables are characterised only by a fundamental component at $50\,\mathrm{Hz}$ (or $60\,\mathrm{Hz}$, depending on the case considered), which is mirrored by the angle $\theta(t)$ used in the Park transformation in Eq. (1.3) to synchronize the DQ0 and ABC frames. On the contrary, if harmonics were present in the ABC frame, they would also appear in the DQ0 one. The second hypothesis is that the ABC-frame variables must comprise only positive-sequence components. Indeed, as explained in Section A.1, even if harmonics are absent in the ABC frame, the presence of negative-sequence components leads to the emergence of direct and quadrature components rotating at twice the fundamental frequency instead of constant ones [151].

These two assumptions, which typically hold in conventional power system operation, constitute the cornerstone of the approaches to small-signal analysis briefly reviewed hereafter.

4.1.1 Approach A

This approach (described extensively in power system textbooks [58]) requires formulating analytically the power system under study as

$$\begin{cases} \dot{\boldsymbol{x}}(t) = \boldsymbol{f}(\boldsymbol{x}(t), \boldsymbol{u}(t)) \\ \boldsymbol{y}(t) = \boldsymbol{g}(\boldsymbol{x}(t), \boldsymbol{u}(t)) \,, \end{cases} \tag{4.1}$$

with $\boldsymbol{x}$, $\boldsymbol{u}$, and $\boldsymbol{y}$ being respectively the vectors of the state, input, and output variables of the system. As already stated, if these variables are

expressed in the DQ0-frame, the steady-state operation of the system corresponds to an *equilibrium* point $(\hat{\boldsymbol{x}}, \hat{\boldsymbol{u}})$ such that

$$\begin{cases} \mathbb{0} = \boldsymbol{f}(\hat{\boldsymbol{x}}, \hat{\boldsymbol{u}}) \\ \hat{\boldsymbol{y}} = \boldsymbol{g}(\hat{\boldsymbol{x}}, \hat{\boldsymbol{u}})\,. \end{cases} \tag{4.2}$$

Small-signal analysis requires determining how small perturbations (denoted in this section by the letter δ) affect the steady-state operation of the system. To do so, Eq. (4.1) can be linearized around the previously identified equilibrium point, which can be progressively simplified as

$$\begin{cases} \dot{\hat{\boldsymbol{x}}} + \delta\dot{\boldsymbol{x}} = \boldsymbol{f}(\hat{\boldsymbol{x}} + \delta\boldsymbol{x}, \hat{\boldsymbol{u}} + \delta\boldsymbol{u}) \\ \hat{\boldsymbol{y}} + \delta\boldsymbol{y} = \boldsymbol{g}(\hat{\boldsymbol{x}} + \delta\boldsymbol{x}, \hat{\boldsymbol{u}} + \delta\boldsymbol{u}) \end{cases}, \tag{4.3}$$

$$\begin{cases} \underbrace{\dot{\hat{\boldsymbol{x}}}}_{\triangleq\mathbb{0}} + \delta\dot{\boldsymbol{x}} = \underbrace{\boldsymbol{f}(\hat{\boldsymbol{x}}, \hat{\boldsymbol{u}})}_{\triangleq\mathbb{0}} + \left.\dfrac{\partial \boldsymbol{f}(\boldsymbol{x}, \boldsymbol{u})}{\partial \boldsymbol{x}}\right|_{\substack{\boldsymbol{x}=\hat{\boldsymbol{x}} \\ \boldsymbol{u}=\hat{\boldsymbol{u}}}} \delta\boldsymbol{x} + \left.\dfrac{\partial \boldsymbol{f}(\boldsymbol{x}, \boldsymbol{u})}{\partial \boldsymbol{u}}\right|_{\substack{\boldsymbol{x}=\hat{\boldsymbol{x}} \\ \boldsymbol{u}=\hat{\boldsymbol{u}}}} \delta\boldsymbol{u} \\ \hat{\boldsymbol{y}} + \delta\boldsymbol{y} = \cancel{\boldsymbol{g}(\hat{\boldsymbol{x}}, \hat{\boldsymbol{u}})} + \left.\dfrac{\partial \boldsymbol{g}(\boldsymbol{x}, \boldsymbol{u})}{\partial \boldsymbol{x}}\right|_{\substack{\boldsymbol{x}=\hat{\boldsymbol{x}} \\ \boldsymbol{u}=\hat{\boldsymbol{u}}}} \delta x + \left.\dfrac{\partial \boldsymbol{g}(\boldsymbol{x}, \boldsymbol{u})}{\partial \boldsymbol{u}}\right|_{\substack{\boldsymbol{x}=\hat{\boldsymbol{x}} \\ \boldsymbol{u}=\hat{\boldsymbol{u}}}} \delta\boldsymbol{u}\,, \end{cases} \tag{4.4}$$

$$\begin{cases} \delta\dot{\boldsymbol{x}} = \boldsymbol{A}\delta\boldsymbol{x} + \boldsymbol{B}\delta\boldsymbol{u} \\ \delta\boldsymbol{y} = \boldsymbol{C}\delta\boldsymbol{x} + \boldsymbol{D}\delta\boldsymbol{u}\,. \end{cases} \tag{4.5}$$

This linearization process yields a *linear time-invariant system*. Through this state-space representation, the relationships (i.e., transfer functions) between the vectors of small-signal input and output variables can be derived with Laplace transform as

$$\delta\boldsymbol{y}(s) = \underbrace{\left[\boldsymbol{C}(s\mathbb{1} - \boldsymbol{A})^{-1}\boldsymbol{B} + \boldsymbol{D}\right]}_{\boldsymbol{H}} \delta\boldsymbol{u}(s)\,, \tag{4.6}$$

where $\mathbb{1}$ is the identity matrix (whose size depends on that of the system under study), while $\boldsymbol{H}$ collects a matrix of transfer functions, which can be used for stability analyses. Moreover, the knowledge of the matrices in Eq. (4.5) (denoted in bold) makes it possible to perform modal analysis, which includes the calculation of the eigenvalues and eigenvectors of the linearized system.

Equation (4.5) also allows computing relationships between a single input and output. For instance, considering as an input a small-signal voltage variation at a given point of a grid and its corresponding small-signal current variation as output, the relationship between those variables corresponds to an admittance.[2] In addition, by letting $s = \mathbb{j}\omega$, the behaviour of

[2] As stated at the beginning, all the variables involved must be expressed in the DQ0-frame.

the real and imaginary part of this admittance can be expressed as a function of frequency (i.e., the frequency response is obtained).

On the one hand, this approach is the most ideal for parametric analyses. For instance, since Eq. (4.5) is derived analytically, eigenvalue sensitivity analysis can be performed straightforwardly. This analysis allows evaluating the influence of several parameters (e.g., regulator gains) on the system eigenvalues and, thus, overall stability. On the other hand, the analytical derivation of Eq. (4.5) may be cumbersome and require extensive pen-and-paper computations, especially in the case of large-scale networks. This issue can only be partially mitigated by resorting to simplified grid models, which must still retain the key dynamic features of the network. In any case, these extensive computations must be inevitably repeated whenever even the slightest variations are applied in the network.

4.1.2 Approach B

In this case, frequency responses (e.g., admittances) are numerically computed as follows [154, 155]. First of all, an electromagnetic transient (EMT) simulation of the unperturbed power system is performed for enough time to reach steady-state (i.e., grid initialization is complete[3]). Then, starting from scratch or the initialized grid, a small-signal perturbation with a given spectrum (i.e., the *input*) is injected into the network. Through another EMT simulation, the small-signal variation of a variable of interest (i.e., the *output*) is calculated by comparing its steady-state behaviour in the current and previous simulation. Lastly, the frequency response is computed as the ratio between the Fast Fourier Transforms (FFTs) of the output and the input.

Frequency response is a well-understood concept for *linear time-invariant systems*. While small-signal injection ensures the extraction of a linearized model, the time-invariance property depends on the system model and the variables used as perturbation and output. As previously mentioned, in conventional power systems the time invariance property is attained by adopting DQ0-frame variables as inputs and outputs.

On the one hand, the method proposed here is more straightforward than approach A, since it resorts to simple EMT simulations instead of pen-and-paper computations. In addition, contrary to approach A, it can be applied even if the network under study comprises parts described by black-box models (i.e., an analytical model is not available). On the other hand, sufficiently small time steps and tolerances must be adopted during EMT simula-

[3] As stated in Section 1.4.2, through initialization the internal states of dynamic elements (i.e., those described by DAEs, such as synchronous generators) are computed so that subsequent simulations begin at steady-state. In other words, no transient behaviour should be observed.

tions to accurately compute the frequency responses. However, this results in a high computational burden, which increases with the number of frequency responses to be determined. This problem is further aggravated if the power system under analysis requires a long time to reach steady-state.[4]

4.1.3 Approach C

This last approach relies on a three-step numerical algorithm that is directly implemented at the simulator level.[5] The first step computes the power flow (PF) solution of the grid under study, while the second one initialises its dynamic elements. As a result, provided that the power system components are modelled and simulated in the DQ0-frame, an *equilibrium point* of the network is identified. In the third step, the simulator linearises the power system equations (e.g., obtained with the modified nodal analysis (MNA)) around this point, thereby obtaining a formulation analogous to that in Eq. (4.5). By exploiting this linearised model and sweeping the frequency of the small-signal perturbation in a given range, the simulator can derive the small-signal solution of the system (and, thus, also frequency responses) by resorting to methods that are more computationally efficient than approach B. In addition, the availability of the linearised model paves the way for analyses similar to those enabled by approach A, without needing to resort to extensive pen-and-paper computations and possibly simplifying the power system under study.

4.2 Small-signal approaches in modern power systems

In the light of their increasing adoption in modern power systems, the small-signal analysis constitutes a useful tool during the MMC design phase to identify the source of possible instability issues and oscillation phenomena. However, the non-linear switching nature of MMCs (and, in general, of all kinds of converters) introduces harmonics in the network and may lead to the emergence of negative-sequence components, which can also be given by single-phase loads (e.g., single-phase induction motors, computers, and other electronics loads, and incandescent) connected to the distribution grid [26]. Thus, the steady-state operation of modern networks no longer translates into an equilibrium point in the DQ0-frame but rather into

[4] As described in the following, this issue can be solved by adopting *ad hoc* techniques aimed at determining the periodic steady-state behaviour of any circuit, such as the *shooting method*. However, at the time of writing and to the best of the author knowledge, this method is not adopted in conventional power system simulators.

[5] Several simulators, such as EMTP-RV and POWERFACTORY [156] implement this algorithm and refer to it as *frequency scan* (or *sweep*). The same term, however, is adopted in other papers to indicate approach B [154]. To avoid ambiguity, this nomenclature is avoided in this thesis.

a *periodic orbit* [80]. As a consequence, since the two hypotheses they rely on are no longer valid, the small-signal stability approaches described in the previous sections cannot be employed in modern power systems.

In principle, this issue could be circumvented by (over-)simplifying the complex model of the MMC (and also that of other converters and grid components, if necessary) till reducing the network under study to a set of quite simple linear time-invariant state equations in the DQ0-frame, whose small-signal response (and, thus, admittances) can still be analysed with the previously mentioned approaches. This is for instance done in [81], [157]. It is worth pointing out that this process is not effortless, especially when dealing with MMCs. Indeed, the topology and control scheme of the MMC is more complicated than that of, for example, conventional two-level VSCs [158]. For instance, the circulating current flowing in each arm and the capacitor voltage ripple of every SM in the MMC require *ad hoc* controls [159] as the steady-state harmonic content of these two variables leads to the converter having a multi-frequency response [88]. Moreover, the MMC cross-coupling behaviour causes the interaction of its internal variables at different frequencies [160]. Hence, the simplification process of the MMC model demands a careful evaluation to prevent erroneous estimates.

In the light of the above, unless simplifications are adopted, the previously described methods to small-signal stability need to be updated and made compatible with grids comprising converters, such as MMCs. To address this issue, scholars have introduced the concepts of dynamic phasors [82–86, 161] and HSS analysis [87–91]. The former, which has been used to update approaches A and B, can be seen as an extension of the Fourier series coefficients to the case of nearly periodic systems and allows obtaining small-signal models amenable to linearization and eigenvalue analysis. On the contrary, the latter approach, which has been proposed as an extension of approach A only, derives small-signal models easily expandable to any harmonic order.

These updated approaches, however, still suffer from the drawbacks mentioned in Sections 4.1.1 and 4.1.2. For instance, in the former approach, the main disadvantage is that the derivation of small-signal models still requires extensive pen-and-paper computations and some simplifying assumptions (e.g., the DC-side of the MMC is connected to an infinite DC-bus[6]). In addition, when new MMC controls need to be analysed, these lengthy computations must be started from scratch.

To the best of the author knowledge, approach C has not been updated in the literature yet. To fill in this gap, the PAC is proposed and described in

[6] An infinite DC-bus superposes a constant pole-to-pole voltage regardless of grid operating conditions.

the following section. It is a numerical tool, directly implementable at the simulator level, which computes the small-signal response of a system in periodic steady-state operating conditions [92]. The term "periodic" means that the small-signal model is time-varying and derived over one period of the large-signal solution of the MMC (in general $1/50$ or $1/60\,\mathrm{Hz}$), which is in turn obtained through the SHM [93]. This technique is compatible with any power system formulation, such as those in the DQ0 or ABC frames (or a mixture of both). Despite being widely adopted for a long time by power electronics designers, this method is still a novelty in the power system realm. The complete absence of the PAC in the numerical tools offered by popular commercial simulators, such as DIGSILENT and EMTP, at least supports this statement.

The main advantage of this method is that it can compute the MMC impedance numerically, without needing to explictily write a small-signal model and putting forward simplifying assumptions or resorting to extensive EMT simulations. To obtain an analytical representation of the MMC admittance, the user can resort to VF algorithms [94, 95]. Versatility is one of the strong point of the PAC-based analysis: if a new aspect of the system (e.g., controls or parameters) under study changes, the new admittance can be computed simply by running once again the simulations, starting the PAC and, finally, using VF algorithms. As shown in the following, the method is also able to take into account intermodulation and up-conversion/down-conversion of a perturbing signal in the frequency spectrum. For example, it is able to compute how a low frequency (e.g. $1\,\mathrm{Hz}$) perturbation in the HVDC link can be up-converted to $(50+1)\,\mathrm{Hz}$ in the AC system. These results cannot be obtained with the ones described in Sections 4.1.1-4.1.3.

4.3 Shooting method (SHM) and Periodic Small-Signal Analysis (PAC)

This section focuses on describing in detail the operating principle of the periodic small-signal analysis (PAC) [30, 92]. This technique can be regarded as an extension of the standard small-signal analysis (AC). Indeed, while the latter calculates the small-signal response of a circuit in the neighbourhood of an *equilibrium point* (like the approach in Section 4.1.1), the former allows studying how the same small-signal input affects the steady-state solution of periodically working circuits and systems (i.e., an *orbit*, so no longer an *equilibrium point*). As AC analysis is used to obtain linearised models of non-linear (sub)systems in the neighbourhood of an equilibrium point, PAC can do the same but in the neighbourhood of a limit cycle.

Indeed, PAC yields a periodic linear time-varying version of the original system. By driving this dynamical system with different small-signal single tones and computing the Fourier transform of the corresponding output signals, it is possible to derive a set of transfer functions which are equivalent to those derived by resorting to the AC analysis in the stationary case. These transfer functions can be used as a linearised version of the original (sub)system in the frequency domain and are useful in the design phase to study, for instance, the stability of the overall system in which the linearised one operates. In the framework of this thesis, the MMC is an eligible candidate for PAC-based analyses because of its periodic steady-state behaviour.

The equations describing the behaviour of any power system and circuit component (MMCs included) can be automatically derived with the Modified Nodal Analysis (MNA) [98, 99]. Several simulation programmes such as PAN (see Section 3.1.5) exploit this analysis to solve power systems and circuits in the time domain [98, 99]. When it comes to generic electr(on)ic circuits or systems, the MNA requires solving a set of non-linear differential algebraic equations (DAEs) [162, 163] at each time step. In principle, if these DAEs are of index-1 [164], it is possible to identify a state-space form with a minimal set of variables leading to a system of ordinary differential equations (ODEs). In general, this cannot be done in the explicit form if, for instance, the algebraic constraints are highly non-linear. However, this formulation exists theoretically, and, when the explicit form exists, it can be profitably used to reduce complexity in deriving results.

To illustrate how PAC works, consider the following non-linear and time-varying index-1 DAE describing the dynamics of a periodically forced circuit such as the MMC (with period $T = {}^{1}/_{f_o} = {}^{2\pi}/_{\omega_o}$)

$$\frac{d}{dt}\boldsymbol{q}(t, \boldsymbol{y}(t)) + \boldsymbol{j}(t, \boldsymbol{y}(t)) = \mathbb{0} \,, \tag{4.7}$$

where t is the time variable and $\boldsymbol{y}(t)$ is a vector that collects all the N state and algebraic variables. For the sake of brevity, the time-dependency of $\boldsymbol{y}(t)$ is often omitted when writing the following equations of this chapter. The DAEs of the circuit are compactly described by the $\boldsymbol{q}(t, \boldsymbol{y})$, $\boldsymbol{j}(t, \boldsymbol{y})$, and $\mathbb{0}$ vectors $\in \mathbb{R}^N$ (with N being also the number of differential and algebraic equations). Equation (4.7) reduces to an ODE if the N equations in Eq. (4.7) are linearly independent and it is not possible to linearly combine them to obtain one or more null entries in $\boldsymbol{q}(t, \boldsymbol{y})$.[7]

If the circuit steady-state is periodic, an orbit $\boldsymbol{y}_s(t) = \boldsymbol{y}_s(t + T) \in \mathbb{R}^N$ (i.e., the *large-signal solution*) exists that solves Eq. (4.7). In the specific

[7] Without loss of generality, this is assumed to be the case, since Eq. (4.7) is supposed to be an index-1 DAE.

case of the MMC, $\boldsymbol{y}_s(t)$ represents the periodic solution of the converter at both the AC and DC sides during steady-state operation.

Assume now that a small additive perturbation, obtained by combining the effects of M small-signal inputs collected in $\boldsymbol{\eta}(t) \in \mathbb{R}^M$, acts on Eq. (4.7) as

$$\frac{d}{dt}\boldsymbol{q}(t,\boldsymbol{y}) + \boldsymbol{j}(t,\boldsymbol{y}) = \boldsymbol{\Lambda}\boldsymbol{\eta}(t) \;, \tag{4.8}$$

where $\boldsymbol{\Lambda} \in \mathbb{R}^{N\times M}$ is a constant matrix.

As previously stated, the purpose of PAC is to determine the influence of small-signal periodic perturbations on the steady-state periodic behaviour of the system. Considering Eq. (4.8), this requires evaluating how $\boldsymbol{\eta}(t)$ affects $\boldsymbol{y}(t)$ at steady-state. To do so, assume that the effects of $\boldsymbol{\eta}(t)$ translate into writing the solution of the original non-linear circuit as $\boldsymbol{y}(t) = \boldsymbol{y}_s(t) + \boldsymbol{y}_\eta(t)$. In other words, the effects of the small-signal perturbation $\boldsymbol{y}_\eta(t)$ *superimpose* to the large-signal (unperturbed) periodic solution $\boldsymbol{y}_s(t)$. Thus, Eq. (4.8) can be linearized along $\boldsymbol{y}_s(t)$, thereby obtaining

$$\begin{aligned}
&\frac{d}{dt}\boldsymbol{q}(t,\boldsymbol{y}_s+\boldsymbol{y}_n) + \boldsymbol{j}(t,\boldsymbol{y}_s+\boldsymbol{y}_n) = \boldsymbol{\Lambda}\boldsymbol{\eta}(t) \\
&\underbrace{\frac{d}{dt}\boldsymbol{q}(t,\boldsymbol{y}_s)+\boldsymbol{j}(t,\boldsymbol{y}_s)}_{\triangleq\mathbb{0}} + \frac{d}{dt}\left[\left.\frac{\partial\boldsymbol{q}(t,\boldsymbol{y})}{\partial\boldsymbol{y}}\right|_{\boldsymbol{y}=\boldsymbol{y}_s}\boldsymbol{y}_\eta\right] + \left.\frac{\partial\boldsymbol{j}(t,\boldsymbol{y})}{\partial\boldsymbol{y}}\right|_{\boldsymbol{y}=\boldsymbol{y}_s}\boldsymbol{y}_\eta = \boldsymbol{\Lambda}\boldsymbol{\eta}(t) \\
&\frac{d}{dt}\left[\underbrace{\left.\frac{\partial\boldsymbol{q}(t,\boldsymbol{y})}{\partial\boldsymbol{y}}\right|_{\boldsymbol{y}=\boldsymbol{y}_s}}_{\boldsymbol{C}(t)}\boldsymbol{y}_\eta\right] + \underbrace{\left.\frac{\partial\boldsymbol{j}(t,\boldsymbol{y})}{\partial\boldsymbol{y}}\right|_{\boldsymbol{y}=\boldsymbol{y}_s}}_{\boldsymbol{G}(t)}\boldsymbol{y}_\eta = \boldsymbol{\Lambda}\boldsymbol{\eta}(t) \;,
\end{aligned} \tag{4.9}$$

where the matrices $\boldsymbol{C}(t)$ and $\boldsymbol{G}(t)$ are characterized by T-periodic entries. In the light of the above, $\boldsymbol{y}_\eta(t)$ can be expressed as a function of $\boldsymbol{\eta}(t)$ only if $\boldsymbol{C}(t)$ and $\boldsymbol{G}(t)$ are known. Assuming that the functions $\boldsymbol{q}(t,\boldsymbol{y})$ and $\boldsymbol{j}(t,\boldsymbol{y})$ are automatically available in the simulation programme by adopting the MNA, this implies that the knowledge of $\boldsymbol{y}_s(t)$ (i.e., the value at which the partial derivatives of $\boldsymbol{q}(t,\boldsymbol{y})$ and $\boldsymbol{j}(t,\boldsymbol{y})$ are evaluated) is a prerequisite.

Sections 4.3.1 and 4.3.2 detail how $\boldsymbol{y}_s(t)$ and $\boldsymbol{y}_\eta(t)$ can be derived. In brief, $\boldsymbol{y}_s(t)$ is obtained with the shooting method (SHM), which was first developed in [165, 166] and also recently used in [20, 163].[8] The $\boldsymbol{y}_\eta(t)$ small-signal solution is computed by resorting to the so-called *fundamental matrix*, which derives as a byproduct of the SHM.

[8]The literature describes several techniques to obtain $\boldsymbol{y}_s(t)$ [167]. Among them, the SHM is the only available method whenever the circuit is switching or described by an Analog Mixed Signal (AMS) model. In these cases, it is necessary to resort to an extension toward hybrid dynamical systems of the SHM [168, 169].

4.3.1 Shooting method and derivation of the large-signal solution

To easily describe the operating principle of the SHM, suppose that in the index-1 DAE in Eq. (4.7) $\boldsymbol{q}(t, \boldsymbol{y}(t)) = \boldsymbol{Q}\boldsymbol{y}(t)$, and $\boldsymbol{Q}$ is a non-singular matrix. So doing, Eq. (4.7) reduces to an ODE and can be recast as

$$\begin{aligned} \boldsymbol{Q}\tfrac{d}{dt}\boldsymbol{y}(t) + \boldsymbol{j}(t, \boldsymbol{y}) &= \mathbb{0} \\ \tfrac{d}{dt}\boldsymbol{y}(t) &= -\boldsymbol{Q}^{-1}\boldsymbol{j}(t, \boldsymbol{y}) \\ \dot{\boldsymbol{y}}(t) &= \boldsymbol{f}(t, \boldsymbol{y}) \end{aligned} \tag{4.10}$$

where $\boldsymbol{f}(t, \boldsymbol{y}) = -\boldsymbol{Q}^{-1}\boldsymbol{j}(t, \boldsymbol{y})$ is the vector field.[9] The SHM can efficiently locate the steady-state periodic solution of Eq. (4.10) by solving an appropriate Boundary Value Problem (BVP) imposing the condition

$$\boldsymbol{y}(t_0 + T) = \boldsymbol{y}(t_0) = \boldsymbol{y}_0 \,. \tag{4.11}$$

In Eq. (4.11), t_0 is an arbitrary initial time and T is the period of the system.

The name of the shooting method stems from the analogy with *target shooting*. For instance, consider a gunner who wants to shoot an object with a cannonball by regulating the tilt angle α of a cannon. At each hit, he observes where the cannonball lands: if it misses the target, the gunner evaluates the sensitivity of the solution (i.e., the arrival position p of the cannonball) to the tilt angle and modifies the latter accordingly. Eventually, after a series of attempts, the cannonball will hit the target. In a nutshell, the gunner resorts to an iterative process, whose key elements are α and p.

As better detailed in the following, the SHM adopts an analogous approach, where $\boldsymbol{y}(t_0)$ and $\boldsymbol{y}(t_0 + T)$ are the corresponding counterparts of α and p. To explain the method in the simplest terms, assume for the sake of simplicity that (i) $\boldsymbol{f}(t, \boldsymbol{y})$ is continuously differentiable in its definition domain and (ii) the circuit described by Eq. (4.10) is non-autonomous and driven by one or more $\hat{T}$-periodic input signals. These input signals give a time reference, and we assume that the period T in Eq. (4.11) coincides with $\hat{T}$. Therefore, the only unknown in the BVP to be derived with the SHM is the vector $\boldsymbol{y}(t_0)$ (and not also T).

For reasons that will soon become clearer, the BVP can be solved by extending Eq. (4.10) with the so-called *variational system* [170], thereby

[9] The reader can refer to [168] for details concerning the extension of the SHM to index-1 DAEs.

obtaining the following system of equations

$$\begin{cases} \dot{\boldsymbol{y}}(t) = \boldsymbol{f}(t, \boldsymbol{y}) \\ \boldsymbol{y}(t_0) = \boldsymbol{y}_0 \\ \dot{\boldsymbol{\Phi}}(t, t_0) = \boldsymbol{J}(t, \boldsymbol{y})\boldsymbol{\Phi}(t, t_0) \\ \boldsymbol{\Phi}(t_0, t_0) = \mathbb{1} \ , \end{cases} \tag{4.12}$$

where $\boldsymbol{J}(t, \boldsymbol{y}) \in \mathbb{R}^{N \times N}$ is the time-varying Jacobian matrix of $\boldsymbol{f}(t, \boldsymbol{y})$, and $\mathbb{1}$ is the $(N \times N)$ identity matrix. On the contrary, $\boldsymbol{\Phi}(t, t_0) \in \mathbb{R}^{N \times N}$ is the *fundamental matrix*. By definition, this matrix is the solution of the variational system (see the last two equations in Eq. (4.12)) associated to Eq. (4.10) and provides the sensitivity of $\boldsymbol{y}(t)$ with respect to the initial condition $\boldsymbol{y}_0$ [170]. As a matter of fact, the following holds

$$\begin{aligned} \frac{\partial}{\partial \boldsymbol{y}_0} \frac{d\boldsymbol{y}}{dt} &= \frac{\partial}{\partial \boldsymbol{y}_0} \boldsymbol{f}(t, \boldsymbol{y}) \\ \frac{d}{dt} \underbrace{\frac{\partial \boldsymbol{y}}{\partial \boldsymbol{y}_0}}_{\boldsymbol{\Phi}(t,t_0)} &= \underbrace{\frac{\partial \boldsymbol{f}(t, \boldsymbol{y})}{\partial \boldsymbol{y}}}_{\boldsymbol{J}(t,\boldsymbol{y})} \underbrace{\frac{\partial \boldsymbol{y}}{\partial \boldsymbol{y}_0}}_{\boldsymbol{\Phi}(t,t_0)} \\ \dot{\boldsymbol{\Phi}}(t, t_0) &= \boldsymbol{J}(t, \boldsymbol{y})\boldsymbol{\Phi}(t, t_0) \end{aligned} \tag{4.13}$$

The SHM finds a value of $\boldsymbol{y}_0$ satisfying Eq. (4.11) by resorting to an iterative process that includes the following steps, sketched also in Fig. 4.1:

(a) At first, a guess of the initial condition $\boldsymbol{y}_0$ is made.

(b) Starting from $\boldsymbol{y}(t_0) = \boldsymbol{y}_0$ and $\boldsymbol{\Phi}(t_0, t_0) = \mathbb{1}$, a time-domain analysis of the system in Eq. (4.12) is performed from t_0 to $T + t_0$. By doing so, $\boldsymbol{y}(t)$ and $\boldsymbol{\Phi}(t, t_0)$ are computed at possibly unevenly spaced time instants, depending on the integration scheme adopted. In any case, $\boldsymbol{y}(T + t_0)$ and $\boldsymbol{\Phi}(T + t_0, t_0)$ are also determined.

(c) Any difference between $\boldsymbol{y}(T + t_0)$ and $\boldsymbol{y}(t_0)$ - referred to as residual $\boldsymbol{r}$ - implies that there is an error in the guess of the initial condition. This error is exploited to update this guess through Newton's method. To better clarify this statement, consider the generic $\boldsymbol{y}_0^k$ guess, with k being used hereafter as a superscript to denote every variable of interest at the k-th iteration of the SHM. The corresponding residual $\boldsymbol{r}$ can be written as

$$\boldsymbol{r}(\boldsymbol{y}_0^k) = \boldsymbol{y}^k(T + t_0) - \boldsymbol{y}_0^k \, . \tag{4.14}$$

The exact solution $\hat{\boldsymbol{y}}$ of the BVP (i.e., the one granting a null residual) is related to the possibly wrong guess at the k-th iteration as $\hat{\boldsymbol{y}} = \boldsymbol{y}_0^k + \boldsymbol{\varepsilon}^k$, the latter term being the error in the guess of $\boldsymbol{y}_0^k$. An estimation of $\boldsymbol{\varepsilon}^k$ can be derived through the following first order Taylor expansion

$$\begin{aligned}
&\boldsymbol{r}(\hat{\boldsymbol{y}}) = \mathbb{0} \\
&\boldsymbol{r}(\boldsymbol{y}_0^k + \boldsymbol{\varepsilon}^k) = \mathbf{0} \\
&\boldsymbol{r}(\boldsymbol{y}_0^k) + \left.\frac{\partial \boldsymbol{r}(\boldsymbol{y}_0^k)}{\partial \boldsymbol{y}_0^k}\right|_{\boldsymbol{y}_0^k} \boldsymbol{\varepsilon}^k = \mathbb{0} \\
&\boldsymbol{r}(\boldsymbol{y}_0^k) + \underbrace{\left.\frac{\partial \left(\boldsymbol{y}^k(T+t_0) - \boldsymbol{y}_0^k\right)}{\partial \boldsymbol{y}_0^k}\right|_{\boldsymbol{y}_0^k}}_{\boldsymbol{\Phi}^k(T+t_0,t_0)-\mathbb{1}} \boldsymbol{\varepsilon}^k = \mathbb{0} \\
&\rightarrow \boldsymbol{\varepsilon}^k = \left(\mathbb{1} - \boldsymbol{\Phi}^k(T+t_0,t_0)\right)^{-1} \boldsymbol{r}(\boldsymbol{y}_0^k)
\end{aligned} \tag{4.15}$$

and exploited to update the initial guess at the $(k+1)$-th iteration as

$$\begin{aligned}
\boldsymbol{y}_0^{k+1} &= \boldsymbol{y}_0^k + \boldsymbol{\varepsilon}^k = \\
&= \boldsymbol{y}_0^k + \left(\mathbb{1} - \boldsymbol{\Phi}^k(T+t_0,t_0)\right)^{-1} \boldsymbol{r}(\boldsymbol{y}_0^k)\,.
\end{aligned} \tag{4.16}$$

(d) Steps (b) and (c) are repeated until the residual is below an accepted tolerance (see ⊛ in Fig. 4.1). Note that, while $\boldsymbol{y}(t_0)$ changes at each iteration because it is corrected in the previous one through Eq. (4.16), $\boldsymbol{\Phi}(t_0,t_0)$ always equals the identity matrix by definition.

When the convergence criterion is satisfied at, say, the K-th iteration, $\boldsymbol{y}_0^{\mathrm{K}}$ is such that the BVP in Eq. (4.11) is solved (i.e., $\boldsymbol{y}_0^{\mathrm{K}} \approx \hat{\boldsymbol{y}}$). Based on step (b), this also implies that the SHM provides at the last iteration $\boldsymbol{y}(t)$ and $\boldsymbol{\Phi}(t,t_0)$ computed *along the periodic orbit* from t_0 to $T + t_0$. The former result entails that the SHM allows deriving the large-signal periodic solution $\boldsymbol{y}_s(t) = \boldsymbol{y}_s(t+T)$ of Eq. (4.7). In addition, the following section proves that the second result can be profitably exploited to compute the small-signal solution $\boldsymbol{y}_\eta(t)$ of Eq. (4.8).

The algorithm outlined above constitutes a basic version of the SHM. It would become more complicated by removing the simplifying assumptions put forward earlier. For instance, if $\boldsymbol{f}(t,\boldsymbol{y})$ were not continuously differentiable in its definition domain, the so-called *saltation matrices* must be adopted to correctly compute the evolution of the fundamental matrix from t_0 to $T + t_0$ whenever discontinuities in the state variables or the vector

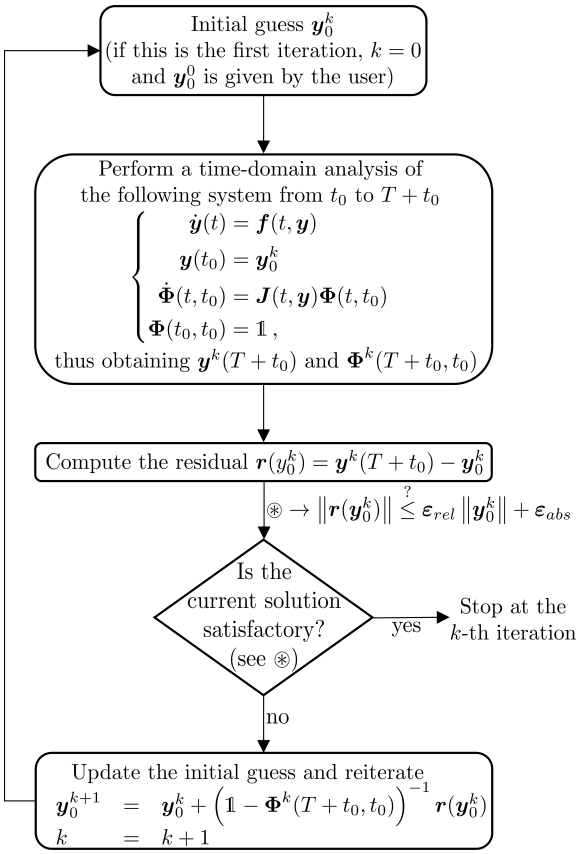


Figure 4.1: *The operating principle of the shooting method.*

field occur [145, 169, 171].[10] In addition, if the system in Eq. (4.10) were autonomous, it would lack a time reference and the unknowns of the BVP would also include the period T. In this case, minimising only the residual $\boldsymbol{r}$ through the iterative approach in Fig. 4.1 is insufficient, because it leads to an underdetermined problem. To address this issue, it is necessary to add a non-linear algebraic equation depending on $\boldsymbol{y}_0$ and T, known as *phase condition*, which guarantees a unique solution of the BVP [145, 170, 173].

4.3.2 PAC and derivation of the small-signal solution

This section describes how to compute the $\boldsymbol{y}_\eta(t)$ solution of Eq. (4.9). The small-signal perturbation $\boldsymbol{\eta}(t)$ can be generally given by any periodic func-

[10] The dynamical systems that require the introduction of saltation matrices are referred to in the literatures as *hybrid* and may present discontinuities in the vector field and/or the state variables [172].

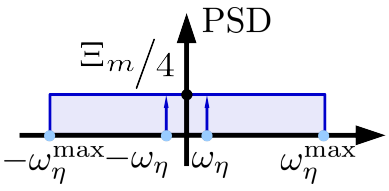


Figure 4.2: *Sketch of the Power Spectral Density (*PSD*) of the m-th component of $\boldsymbol{\eta}(t)$.*

tion. Here it is assumed that $\boldsymbol{\eta}(t) = \boldsymbol{\Xi}\sin(^{2\pi t}/_{T_\eta} + \boldsymbol{\psi})$, where $\boldsymbol{\Xi}$ is an $\boldsymbol{M}$ real-element vector, $\boldsymbol{\psi}$ is the phase of each sinusoid (which could be different from zero), and $T_\eta \in [T_\eta^{\min}, T_\eta^{\max}]$. As depicted in Fig. 4.2, these interval extremes define the bandwidth of the perturbation under analysis. By varying T_η in the selected interval, a set of small-signal solutions $\boldsymbol{y}_\eta(t; T_\eta)$ that satisfy Eq. (4.9) can be obtained. In the following, $T_\eta = \nu T$, with $\nu \in \mathbb{Z}$.[11]

According to the previous section, one of the byproducts of the SHM is the state transition matrix $\boldsymbol{\Phi}(t, t_0)$ of the circuit, computed along its periodic solution $\boldsymbol{y}_s(t)$. This matrix is known only for a finite set of samples corresponding to possibly unevenly spaced time instants t_h ($h = 0, ..., H$), such that $t_H = T$. By resorting to Lagrange's formula [170], the matrix $\boldsymbol{\Phi}(t, t_0)$ can be used to derive each $\boldsymbol{y}_\eta(t; T_\eta)$ solution of Eq. (4.9) as

$$\boldsymbol{y}_\eta(t) = \boldsymbol{\Phi}(t, t_0) \int_{t_0}^{t} \boldsymbol{\Phi}^{-1}(\tau, t_0)\boldsymbol{\Lambda}\boldsymbol{\eta}(\tau)d\tau \ . \tag{4.17}$$

This equation might be solved for each value of ν with numerical integration methods and other techniques that reduce computational burden [174].[12] Hereafter, a different approach is adopted, which aims at finding a closed-form solution of Eq. (4.17). This approach relies on the *Floquet-Lyapunov factorization* [175], according to which the fundamental matrix $\boldsymbol{\Phi}(t, t_0)$ can be decomposed as

$$\boldsymbol{\Phi}(t, t_0) = \boldsymbol{L}_F(t, t_0)e^{\boldsymbol{F}(t-t_0)} \ , \tag{4.18}$$

[11] In other words, the values of T_η analysed are only integer multiples of T, so that $\boldsymbol{\eta}(t) = \boldsymbol{\eta}(t + T_\eta) = \boldsymbol{\eta}(t + \nu T)$. This is a more practical approach but can be easily generalized for $\nu = \frac{\nu_N}{\nu_D} \in \mathbb{Q}$. In this case, $\boldsymbol{y}_\eta(t)$ would be computed in the time interval $[t_0, t_0 + \nu_D T_\eta] \equiv [t_0, t_0 + \nu_N T]$.

[12] It is worth specifying that the upper extreme of the integral in Eq. (4.17) is $t = T_\eta + t_0$. Since T_η is a multiple of T, the computation of the integral requires the knowledge of $\boldsymbol{\Phi}(t, t_0)$ in a wider time interval than $[t_0, T + t_0]$, which corresponds to the one where $\boldsymbol{\Phi}(t, t_0)$ is originally determined through the SHM (see Section 4.3.1). To overcome this issue, the composition property of $\boldsymbol{\Phi}(t, t_0)$ can be used: it allows one to compute the fundamental matrix at any time t as $\boldsymbol{\Phi}(t, t_0) = \boldsymbol{\Phi}(t, \hat{t}\,)\boldsymbol{\Phi}(\hat{t}, t_0)$, being $t_0 \leq \hat{t} \leq t$ [170]. The interested reader can refer to [20, 165] for more information about how this property can be profitably exploited.

known as *Floquet normal form*. In Eq. (4.18), the matrix $\boldsymbol{L}_F(t,t_0)$ is such that $\boldsymbol{L}_F(t+T,t_0+T)=\boldsymbol{L}_F(t,t_0)$ and $\boldsymbol{L}_F(T+t_0,t_0)=\boldsymbol{L}_F(t_0,t_0)=\mathbb{1}_N$ (being $\mathbb{1}_N$ the $N\times N$ identity matrix). On the contrary, $\boldsymbol{F}$ is one of the infinitely many solutions of the equation $\mathrm{e}^{\boldsymbol{F}T}=\boldsymbol{\Psi}$, with $\boldsymbol{\Psi}=\boldsymbol{\Phi}(t_0+T,t_0)$ (also known as *monodromy matrix*). Since $\boldsymbol{\Phi}(t,t_0)$ is known at $t=T$, so is $\boldsymbol{\Psi}$. Assuming that the monodromy matrix can be diagonalized as $\boldsymbol{\Psi}=\boldsymbol{V}\boldsymbol{\Delta}\boldsymbol{V}^{-1}$ (this is generally the case when dealing with well-posed circuits), one can write

$$\boldsymbol{F}=\tfrac{1}{T}\boldsymbol{V}\log(\boldsymbol{\Delta})\boldsymbol{V}^{-1}\,, \tag{4.19}$$

$$\begin{aligned}\boldsymbol{\Phi}(t,t_0) &= \boldsymbol{L}_F(t,t_0)\mathrm{e}^{\boldsymbol{F}(t-t_0)}=\\ &= \boldsymbol{L}_F(t,t_0)\mathrm{e}^{\frac{1}{T}\boldsymbol{V}\log(\boldsymbol{\Delta})\boldsymbol{V}^{-1}(t-t_0)}=\\ &= \boldsymbol{L}_F(t,t_0)\boldsymbol{V}\mathrm{e}^{\log(\boldsymbol{\Delta})\frac{t-t_0}{T}}\boldsymbol{V}^{-1}=\\ &= \boldsymbol{L}_F(t,t_0)\boldsymbol{V}\mathrm{e}^{\log\left(\boldsymbol{\Delta}^{\frac{t-t_0}{T}}\right)}\boldsymbol{V}^{-1}=\\ &= \boldsymbol{L}_F(t,t_0)\boldsymbol{V}\boldsymbol{\Delta}^{\frac{t-t_0}{T}}\boldsymbol{V}^{-1}\,.\end{aligned} \tag{4.20}$$

The matrix $\boldsymbol{L}_F(t,t_0)$ can be easily derived from Eq. (4.20). Hence, Eq. (4.17) can be rewritten as follows

$$\begin{aligned}\boldsymbol{y}_\eta(t) &= \boldsymbol{\Phi}(t,t_0)\int_{t_0}^{t}\boldsymbol{\Phi}^{-1}(\tau,t_0)\boldsymbol{\Lambda}\boldsymbol{\eta}(\tau)d\tau=\\ &= \boldsymbol{L}_F(t,t_0)\boldsymbol{V}\boldsymbol{\Delta}^{\frac{t-t_0}{T}}\boldsymbol{V}^{-1}\int_{t_0}^{t}\left(\boldsymbol{L}_F(\tau,t_0)\boldsymbol{V}\boldsymbol{\Delta}^{\frac{\tau-t_0}{T}}\boldsymbol{V}^{-1}\right)^{-1}\boldsymbol{\Lambda}\boldsymbol{\eta}(\tau)d\tau=\\ &= \boldsymbol{L}_F(t,t_0)\boldsymbol{V}\int_{t_0}^{t}\boldsymbol{\Delta}^{\frac{t-\tau}{T}}\boldsymbol{L}_F(\tau,t_0)^{-1}\boldsymbol{V}^{-1}\boldsymbol{\Lambda}\boldsymbol{\eta}(\tau)d\tau=\\ &= \boldsymbol{L}_F(t,t_0)\boldsymbol{V}\int_{t_0}^{t}\boldsymbol{\Delta}^{\frac{t-\tau}{T}}\left(\boldsymbol{L}_F(\tau,t_0)\boldsymbol{V}\right)^{-1}\boldsymbol{\Lambda}\boldsymbol{\eta}(\tau)d\tau\,.\end{aligned} \tag{4.21}$$

The periodicity of the matrix $\boldsymbol{L}_F(t,t_0)$ translates also into that of the matrix $(\boldsymbol{L}_F(\tau,t_0)\boldsymbol{V})^{-1}$ in the last equation of Eq. (4.21), which can be expressed through the Fourier decomposition of each of its entries as

$$(\boldsymbol{L}_F(\tau,t_0)\boldsymbol{V})^{-1}=\sum_{r=0}^{\infty}\boldsymbol{C}_r\underbrace{\mathrm{diag}\begin{pmatrix}\mathrm{e}^{\mathbb{j}\frac{2\pi rt}{T}} & \cdots & \mathrm{e}^{\mathbb{j}\frac{2\pi rt}{T}}\end{pmatrix}}_{\boldsymbol{E}_r(t)}\,, \tag{4.22}$$

where $\boldsymbol{C}_r$ is an $N\times N$ complex elements matrix, and $\boldsymbol{E}_r(t)$ is an $N\times N$ elements diagonal matrix. As a consequence, Eq. (4.21) can be finally transformed into

$$\boldsymbol{y}_\eta(t) = \boldsymbol{L}_F(t,t_0)\boldsymbol{V}\sum_{r=0}^{\infty}\boldsymbol{C}_r\boldsymbol{B}_r(t)\ . \tag{4.23}$$

$\boldsymbol{B}_r(t)$ is a diagonal matrix whose (k,k)-element ($k=1,...,N$) is

$$\left(B_r(t)\right)_{k,k} = \int_{t_0}^{t}\Delta_{k,k}^{-\frac{t-\tau}{T}}\ \mathrm{e}^{\mathbb{j}\frac{2\pi r t}{T}}\left(\boldsymbol{\Lambda}\boldsymbol{\eta}(\tau)\right)_k d\tau\ . \tag{4.24}$$

This compact representation is possible because the $\boldsymbol{\Delta}^{-\frac{t-\tau}{T}}$ and $\boldsymbol{E}_r(t)$ matrices are diagonal. Note that the upper limit of the summation terms in Eqs. 4.22 and 4.23 implies that in principle all the harmonics of $\boldsymbol{y}_\eta(t)$ are considered. In practice, this upper limit is truncated to a custom number of terms R, and the integral in Eq. (4.24) may be solved in closed-form as [171]

$$\left(B_r(t)\right)_{k,k} = \left(\frac{\mathrm{e}^{-\mathbb{j}\psi_k}\left(\mathrm{e}^{\mathbb{j}2\pi t\left(r/T-1/T_\eta\right)} - \left|\Delta_{k,k}\right|^{(t-t_0)/T}\mathrm{e}^{\mathrm{j}\arg\Delta_{k,k}(t-t_0)/T+\mathrm{j}2\pi t_0\left(r/T-1/T_\eta\right)}\right)}{2\pi T + T_\eta\left(\arg\Delta_{k,k} - 2\pi r - \mathbb{j}\log\left|\Delta_{k,k}\right|\right)} + \right.$$
$$\left. + \frac{\mathrm{e}^{\mathbb{j}\psi_k}\left(\mathrm{e}^{\mathbb{j}2\pi t\left(r/T+1/T_\eta\right)} - \left|\Delta_{k,k}\right|^{(t-t_0)/T}\mathrm{e}^{\mathrm{j}\arg\Delta_{k,k}(t-t_0)/T+\mathrm{j}2\pi t_0\left(r/T+1/T_\eta\right)}\right)}{2\pi T - T_\eta\left(\arg\Delta_{k,k} - 2\pi r - \mathbb{j}\log\left|\Delta_{k,k}\right|\right)}\right)\left(-\frac{TT_\eta(\boldsymbol{\Lambda\Xi})_k}{2}\right)\ . \tag{4.25}$$

4.3.3 Frequency folding and derivation of generic transfer matrices

It is worth pointing out that, since Eq. (4.9) is a set of linear time-varying periodic DAEs, the spectrum of $\boldsymbol{y}_\eta(t;T_\eta)$ contains frequencies of the form $2\pi k f_o \pm {}^{2\pi}/_{T_\eta}$, with f_0 being the fundamental frequency of the large-signal solution $\boldsymbol{y}_s(t)$. In other words, *frequency is folded* at kf_o harmonics of $\boldsymbol{y}_s(t)$ [176].

By resorting to Fourier transforms, it is possible to relate the elements of the vectors $\boldsymbol{y}_\eta(t;T_\eta)$ and $\boldsymbol{\eta}(t;T_\eta)$ to one another with suitable $H_{qm}^{(k)}(\omega)$ *transfer functions*. In particular, $H_{qm}^{(k)}(\omega)$ represents the transfer function from the m-th component of $\boldsymbol{\eta}(t)$ to the q-th component of $\boldsymbol{y}_\eta(t)$ centered at $\pm 2\pi k f_o$. Figure 4.3 depicts as an example the generic PSD of $|H_{qm}^{(k)}(\omega)|^2$ centered at different $2\pi k f_o$ frequencies.

As a result, the relationship among the small-signal perturbation and the corresponding system response can be expressed as

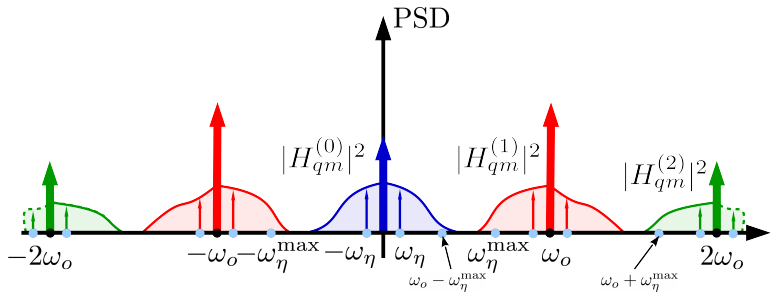


Figure 4.3: *Sketch of the* PSD *of the $|H_{qm}^{(k)}|^2$ transfer functions from the m-th component of $\boldsymbol{\eta}(t)$ to the q-th component of $\boldsymbol{y}_\eta(t)$ centered at $\pm 2\pi k f_o$. The value ω_η is related to the period of the small-signal perturbation in Fig. 4.2 as $\omega_\eta = {}^{2\pi}/_{T_\eta}$.*

$$\hat{\boldsymbol{y}}_\eta(\omega) = \sum_k \underbrace{\begin{bmatrix} H_{11}^{(k)}(\omega) & \dots & H_{1M}^{(k)}(\omega) \\ \vdots & \ddots & \\ H_{N1}^{(k)}(\omega) & & H_{NM}^{(k)}(\omega) \end{bmatrix}}_{\boldsymbol{H}^{(k)}(\omega)} \hat{\boldsymbol{\eta}}(\omega) \ , \tag{4.25}$$

where the $\hat{}$ symbol denotes the Fourier transform.[13]

What stated so far, however, does not justify the presence of the summation in Eq. (4.25). Indeed, by referring to Fig. 4.3, if one is interested in analysing what happens around the generic $2\pi p f_o$ harmonic, the $\boldsymbol{H}^{(k)}(\omega)$ contributions with $k \neq p$ can be ignored because their corresponding PSDs do not overlap. In the most general case, however, overlaps do may occur: this is exemplified by Fig. 4.4 (see the superposition of $H_{qm}^{(0)}(\omega)$ with $H_{qm}^{(1)}(\omega)$, and of $H_{qm}^{(1)}(\omega)$ with $H_{qm}^{(2)}(\omega)$).

Based on the above, a rigorous approach requires combining the effects of each transfer function whenever overlaps are observed. This implicitly reflects on the summation index in Eq. (4.25). In practice, the $\boldsymbol{H}^{(k)}(\omega)$ contributions with $k \neq p$ may be disregarded only if they are negligible with respect to $\boldsymbol{H}^{(p)}(\omega)$.

[13] If one is interested in the transfer functions relating a subset of the elements of $\boldsymbol{\eta}(t)$ to a subset of the elements of $\boldsymbol{y}_\eta(t)$ (or a linear combination of them) it is sufficient to properly select and combine a subset of the elements of each $\boldsymbol{H}^{(k)}(\omega)$ matrix.

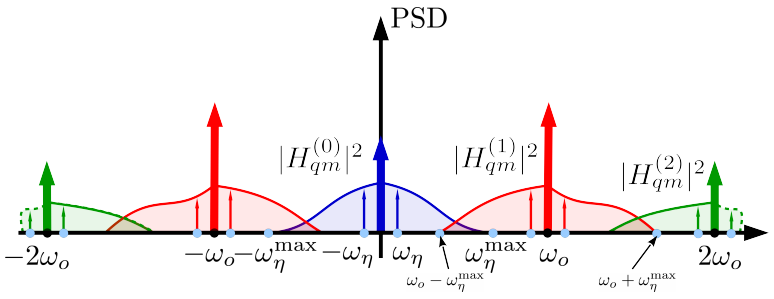


Figure 4.4: *Sketch of the* PSD *of the* $|H_{qm}^{(k)}|^2$ *transfer functions from the* m*-th component of* $\boldsymbol{\eta}(t)$ *to the* q*-th component of* $\boldsymbol{y}_\eta(t)$ *centered at* $\pm 2\pi k f_o$*. The value* ω_η *is related to the period of the small-signal perturbation in Fig. 4.2 as* $\omega_\eta = {}^{2\pi}/_{T_\eta}$*. Contrary to Fig. 4.3, in this case the* PSD*s centered at* $\pm 2\pi k f_0$ *overlap in some frequency ranges.*

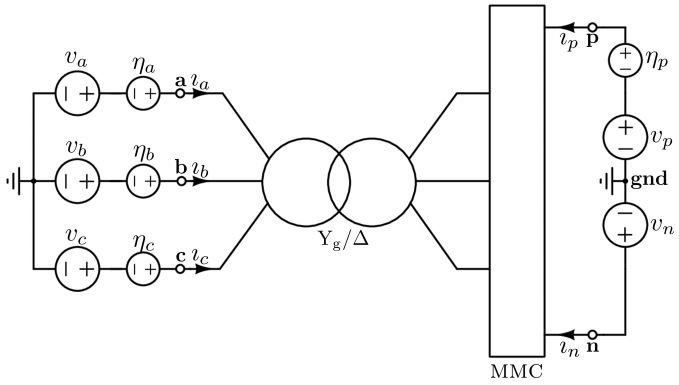


Figure 4.5: MMC *representation as a 5-terminal component.*

4.3.4 PAC and derivation of MMC admittance matrix

The general approach outlined in the previous section can be adopted to derive the transfer functions that relate to one another any subset of the small-signal responses $\boldsymbol{y}_\eta(t)$ and perturbations $\boldsymbol{\eta}(t)$ (hereafter also referred to as *outputs* and *inputs*, respectively). In particular, the PAC-based analysis grants the user absolute freedom in choosing input and output variables to describe a given circuit or power system component.

To explain how PAC is applied to MMCs (and which variables to use as inputs and outputs to describe them), consider the simple circuit schematic in Fig. 4.5 and neglect momentarily the η_a, η_b, η_c, and η_p voltage sources. In this case the MMC, which includes a Y_g/Δ transformer, is treated as a 5-terminal component whose AC and DC sides are connected to voltage sources.

By analysing Fig. 4.5, it is possible to derive that $\imath_p + \imath_n = 0$. On the contrary, since the three-phase voltage sources on the AC-side are connected to ground, $\imath_a + \imath_b + \imath_c \neq 0$. This implies that four currents ($\imath_a$, $\imath_b$, and $\imath_c$ at the AC side; one between $\imath_p$ and $\imath_n$ at the DC side) are necessary to describe the behaviour of the MMC. Analogously, four voltages (υ_a, υ_b, and υ_c, as well as one between υ_p and υ_n) can be chosen to control the converter.

In this thesis, the sets of voltages and currents chosen are $(\upsilon_a, \upsilon_b, \upsilon_c, \upsilon_p)$ and $(\imath_a, \imath_b, \imath_c, \imath_p)$. The former and latter set collect respectively the inputs and outputs of the MMC. Indeed, the η_a, η_b, η_c, and η_p voltage sources in Fig. 4.5 constitute the small-signal perturbations added to study how they affect the periodic behaviour of the circuit (specifically, the small-signal response of $\imath_a$, $\imath_b$, $\imath_c$, and $\imath_p$).

Through PAC, a matrix of transfer functions can be obtained in the form

$$\begin{bmatrix} \hat{\imath}_{a_\eta} \\ \hat{\imath}_{b_\eta} \\ \hat{\imath}_{c_\eta} \\ \hat{\imath}_{p_\eta} \end{bmatrix} = \sum_k \underbrace{\begin{bmatrix} Y_{aa}^{(k)} & Y_{ab}^{(k)} & Y_{ac}^{(k)} & Y_{ap}^{(k)} \\ Y_{ba}^{(k)} & Y_{bb}^{(k)} & Y_{bc}^{(k)} & Y_{bp}^{(k)} \\ Y_{ca}^{(k)} & Y_{cb}^{(k)} & Y_{cc}^{(k)} & Y_{cp}^{(k)} \\ Y_{pa}^{(k)} & Y_{pb}^{(k)} & Y_{pc}^{(k)} & Y_{pp}^{(k)} \end{bmatrix}}_{\boldsymbol{Y}^{(k)}} \begin{bmatrix} \hat{\eta}_a \\ \hat{\eta}_b \\ \hat{\eta}_c \\ \hat{\eta}_p \end{bmatrix}, \tag{4.26}$$

where $\boldsymbol{Y}$ is used instead of $\boldsymbol{H}$ (see Eq. (4.25)) since the entries are admittances (from hereon, for the sake of brevity, the frequency-dependency of each entry of the matrix is omitted).[14] [15] This represents the small-signal model of the MMC in this specific configuration and PAC provides the entries of this matrix in numerical form. To obtain an approximate formulation of each entry in $\boldsymbol{Y}$ in closed-form, one may resort to the vector fitting (VF) method already described in Section 3.1.2.2.

[14] To be precise, the term "admittance" is loosely adopted here. Indeed, from a rigorous standpoint, admittances relate voltages and currents at the same frequency: this is exactly what is mirrored by the entries of the matrix $\boldsymbol{Y}^{(k)}$ with $k = 0$. On the contrary, when $k \neq 0$, the small-signal input (i.e., voltage) and its corresponding output (i.e., voltage) refer to different frequency ranges. Thus, the entries of the matrix in this case are not exactly admittances.

[15] The size of the matrix in Eq. (4.26) would become 3×3 if the small-signal perturbations and responses were injected and examined at the Δ side of the transformer (if any) used to connect the MMC to the grid. This is because in the Δ side the property $\imath_a + \imath_b + \imath_c = 0$ is valid. Anyhow, regardless of the point of injection of the perturbations, the application of PAC remains straightforward. This note is made since [89,91] derived impedance models of a three-phase, four-wire MMC, whose DC and AC sides were grounded to provide a circulation path for the zero-sequence current. This path does not exist in reality, as MMCs are three-phase, three-wire systems. Thus, to force the zero-sequence current on the MMC AC side to zero in order to carry out the analysis, [89] introduced a fictitious zero-sequence voltage compensation. On the contrary, PAC requires no additions of this sort.

4.4 Numerical results

To prove that PAC can be profitably used to analyse MMCs, this section employs three test systems of increasing complexity, hereafter referred to as case (a), (b), and (c). These cases are outlined in Fig. 4.6(a-c): the latter is the same as Fig. 3.1, but it is shown again for ease of reference. Unless otherwise stated, in each test case it is assumed that simulations start with the Cm-C1 MMC injecting $400\,\mathrm{MW}$ in the DC grid and the main and bypass breakers being closed and opened, respectively.

The grid corresponding to case (c) in Fig. 4.6(c) presents two main differences from that presented in Section 3.1. First, since this chapter focuses on steady-state operation, faults are not considered. Second, instead of simulating MMCs with the isomorphism-based approach, the *type 3 Switching Function Model (*SFM*)* introduced in Section 2.1.5 is adopted.

As shown in Table 2.1, the only *lower level controls* analysable with this MMC model are circulating current suppression strategies. On the contrary, Capacitor voltage Balancing Algorithms (CBAs) and Nearest Level Modulation (NLM) (or other modulation techniques) cannot be studied. These two controls can be interpreted as discrete-time dynamical systems. Indeed, their dynamical evolution occurs only at a discrete set of possibly unevenly spaced time instants (for instance, consider the case when an SM changes its operating condition at the threshold crossing of the NLM). The presence of these events makes the overall circuit a hybrid system. By definition, this class of systems comprises dynamical continuous/discrete-time evolution processes interacting with logical/decisional ones [177]. As well known in the literature, to determine the steady-state working period T of hybrid systems is a complex task: discrete-time events may lead to the appearance of quasi-periodic or even chaotic dynamical evolutions[16], thereby jeopardising the existence of a periodic steady-state in the first place.[17]

In the light of the above, this section adopts the *type 3* SFM because it provides the highest level of detail without introducing discrete-time events. However, this implies that the impact of CBAs and NLM on the shape of the MMC transfer functions computed in the following cannot be assessed.

In the test systems in Fig. 4.6(a-b) the additional simplification is that an infinite DC bus replaces the Cm-A1 MMC and the corresponding AC grid.

[16] A simple example of a *hybrid* system is the buck-boost converter. In [178], the authors installed this converter in a simple test system and analyzed how chaotic behaviour could be triggered by varying some parameters.

[17] This is one of the reasons why the initialization transient described in Section 3.1.5 is necessary when using the isomorphism-based simulation approach. Indeed, this approach includes CBAs and NLM, thus making the grid in Fig. 3.1 a hybrid system. Therefore, despite being in principle a viable solution to initialise power systems, the SHM cannot be employed in this case to start simulations from an exact steady-state operating point.

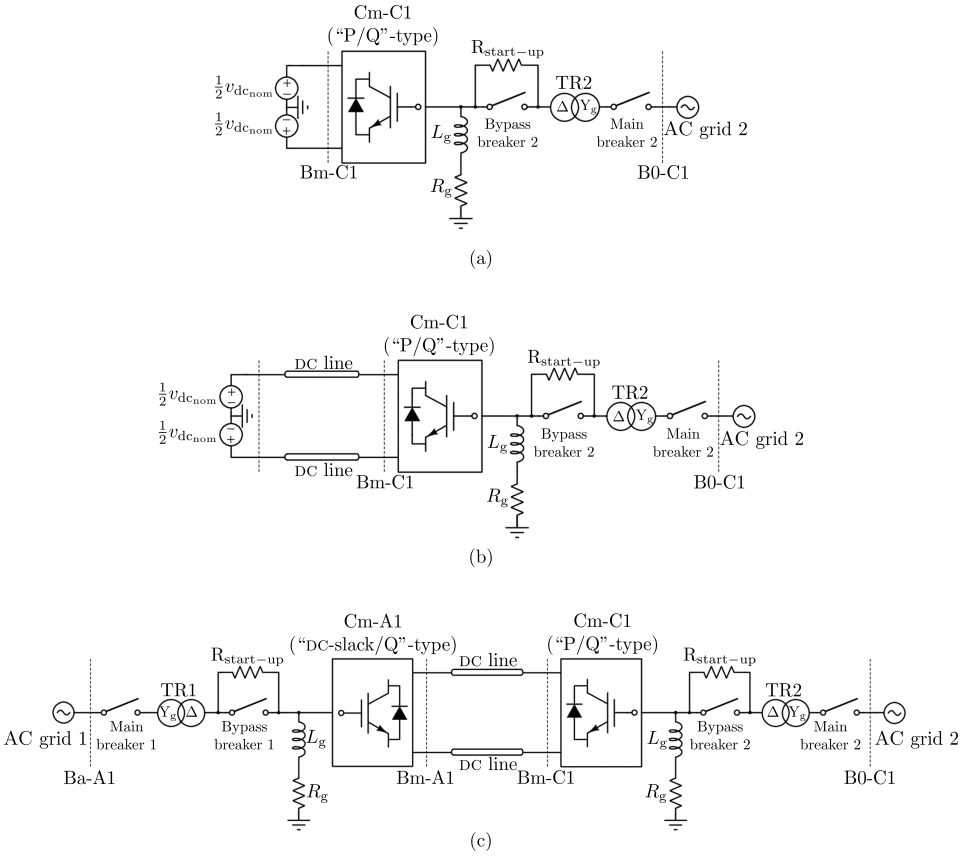


Figure 4.6: *The block schematic of the three test systems (i.e., case (a), (b), and (c)) considered in this section. Dashed lines indicate busses. The meaning of each component is described in Section 3.1.*

This bus, given by two voltage sources $\frac{1}{2}v_{\mathrm{dc_{nom}}}$, superposes a constant pole-to-pole voltage, regardless of grid operating conditions. In Fig. 4.6(a), the infinite DC bus and DC-side of Cm-C1 MMC are connected directly, while in Fig. 4.6(b) two DC lines are placed between them. As mentioned in Section 3.1.2.3, the DC line model in Fig. 3.5 was selected instead of the Universal Line Model (ULM) because the latter includes delay blocks. Albeit necessary to simulate propagation delays, these blocks are incompatible with a simple time-domain implementation of the SHM.

Except for the differences mentioned above, all the other circuit models and parameters adopted are the same as those described in Section 3.1. Rather than investigating the HVDC systems in use (and, for instance, improve their stability by implementing more advanced controls), the main

objective of this section is deriving specific transfer functions of the MMCs through PAC and commenting on possible interesting electrical aspects enlightened by those.

4.4.1 Analysis of AC-side MMC self- and mutual admittances

One of the already mentioned issues related to HSS and dynamic phasor-based modelling is that the derivation of MMC small-signal models requires extensive pen-and-paper computations and the introduction of simplifying hypotheses. For instance, a common assumption is that the DC-side voltage of the MMC under analysis is always constant, as if an infinite DC-bus was connected at its terminals [84, 87, 179].

The purpose of this section is twofold. First, it proves that the previous assumption might not always be valid, since the computed equivalent AC-side MMC small-signal admittance depends on what is connected to its DC-side. Second, it showcases the flexibility of PAC-based analyses, which can be easily carried out regardless of what exists beyond the DC-side of the MMC, without needing any simplifying assumption.

In line with these aims, PAC was first used to analyse the Cm-C1 MMC. For all the case studies in Fig. 4.6(a-c), the η_a, η_b, and η_c small-signal sources were connected in series to the $v_a(t)$, $v_b(t)$, and $v_b(t)$ voltage generators of AC grid 2 (see Fig. 3.2). The period T_η of these perturbations was varied in the interval $\left[\frac{1}{0.1}, \frac{1}{350}\right]$ s. The small-signal responses of the $\imath_a$, $\imath_b$, and $\imath_c$ currents were measured right where the corresponding perturbating signals are connected.

Figure 4.7 depicts some results obtained with PAC for each case study. For the sake of brevity, only some entries of the $\boldsymbol{Y}^{(0)}$ matrix in Eq. (4.26) are presented. Specifically, this section focuses on the admittances $Y_{aa}^{(0)}$ and $Y_{ba}^{(0)}$ of the Cm-C1 MMC.[18] In each panel, the solid black, solid magenta, and dashed green lines respectively refer to cases (a), (b), and (c).

Based on these results, it is evident that the computed admittances obtained in cases (b) and (c) overlap, which suggests that the adoption of the real Cm-A1 MMC - or, in its stead, of an infinite DC bus in series with an HVDC link - leads to almost identical results in terms of $Y_{aa}^{(0)}$ and $Y_{ba}^{(0)}$. On the contrary, the results of case (a) are different from the previous ones, mostly in the frequency range from 0 to $100\,\mathrm{Hz}$. This implies that simplifying the DC-side of an MMC by directly connecting it to an infinite DC bus is not always an adequate choice when computing the AC-side MMC small-signal admittance.

[18] The next sections analyse also other entries of the same matrix or centered at $2\pi k f_0$ (with $k \neq 0$).

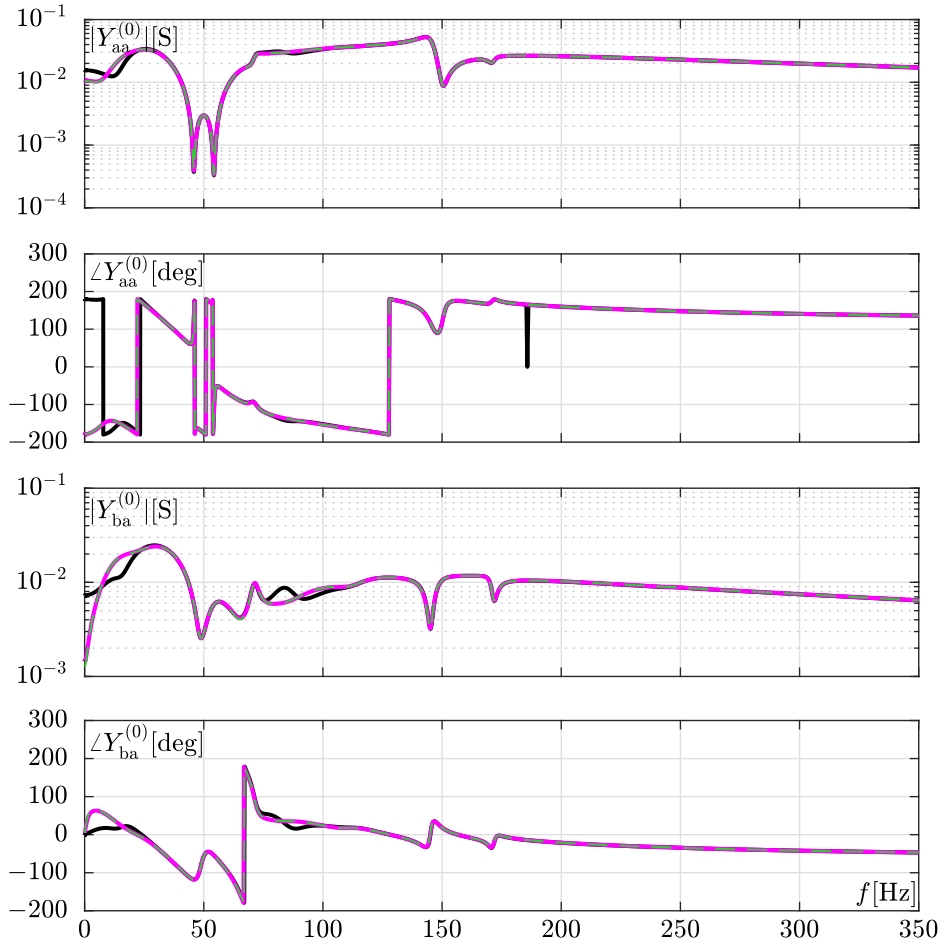


Figure 4.7: *The magnitude and phase of the $Y_{qm}^{(0)}$ admittance entries of the $\boldsymbol{Y}^{(0)}$ matrix in Eq. (4.26), associated with the Cm-C1* MMC. *The sets plotted with solid black, solid magenta, and dashed green lines respectively refer to the power system configuration shown in in Fig. 4.6(a-c). By from top to bottom: panel 1: magnitude of $Y_{aa}^{(0)}$; panel 2: phase of $Y_{aa}^{(0)}$; panel 3: magnitude of $Y_{ba}^{(0)}$; panel 4: phase of $Y_{ba}^{(0)}$.*

4.4.2 Analysis of interactions between MMCs

This section highlights another feature of PAC-based analyses, which is their capability of evaluating how two AC grids connected with an HVDC system interact with each other in case of small-signal perturbations.[19].

To prove this statement, the test system in Fig. 4.6(c) is considered again.

[19]This analysis can be extended to multiple AC grids connected through a multi-terminal direct current (MTDC) network.

Figure 4.8 shows the magnitude and phase of four admittances obtained with PAC: $Y^{(0)}_{a^{\text{AC}\,1}a^{\text{AC}\,2}}$, $Y^{(0)}_{b^{\text{AC}\,1}a^{\text{AC}\,2}}$, $Y^{(0)}_{a^{\text{AC}\,2}a^{\text{AC}\,1}}$, and $Y^{(0)}_{b^{\text{AC}\,2}a^{\text{AC}\,1}}$. The second and first letters in the subscript of each admittance respectively correspond to the phases where the small-signal disturbance and its current are injected and measured. The $_{\text{AC}\,1}$ and $_{\text{AC}\,2}$ symbols to refer to the grid where the small signal is injected/measured.

These traces indicate a small coupling between the AC1 and AC2 systems. The mutual interaction between the two grids is similar (although not identical), as indicated by comparable admittance magnitude values.

It is worth pointing out that the analysis shown above could have not been done just as easily with the previously mentioned MMC small-signal modelling approaches, since they lead to calculations that become already complex and lengthy when considering a single MMC connected to an infinite DC bus.

4.4.3 Analysis of DC-side MMC self-admittance

Other than the already discussed small-signal sources η_a, η_b and η_c, the PAC-based MMC analysis requires the introduction of a small-signal perturbation η_p connected to the DC-side (see Section 4). Assuming that the objective is still the analysis of the admittances of the Cm-C1 MMC in Fig. 4.6, the following holds. In case (a), η_p was connected between the bus Bm-C1 and the infinite DC-bus. On the contrary, in cases (b) and (c) η_p was placed between the bus Bm-C1 and the upper DC line.

The resulting real and imaginary parts of the $Y^{(0)}_{pp}$ admittances obtained with PAC in the three cases are shown in Fig. 4.9. At low frequencies, the admittance is mostly of resistive/capacitive type (i.e., negative imaginary part) in all cases. It is also worth pointing out that the real part of three admittances is never negative, which is a general indication of the fact that Cm-C1 MMC is not prone to DC side instabilities. Recent works [28, 180, 181] considered this aspect and highlighted the importance of accurate cable modelling when studying DC side stability [135]. The frequency-dependence of the resistance and inductance due to skin effect improves stability margins. Indeed, although the capacitive part of the admittance of the MMC may fall in some frequency ranges due to resonance phenomena, the cable resistance and inductance are respectively sufficiently high and low to prevent the negative resistance of the MMC from manifesting.

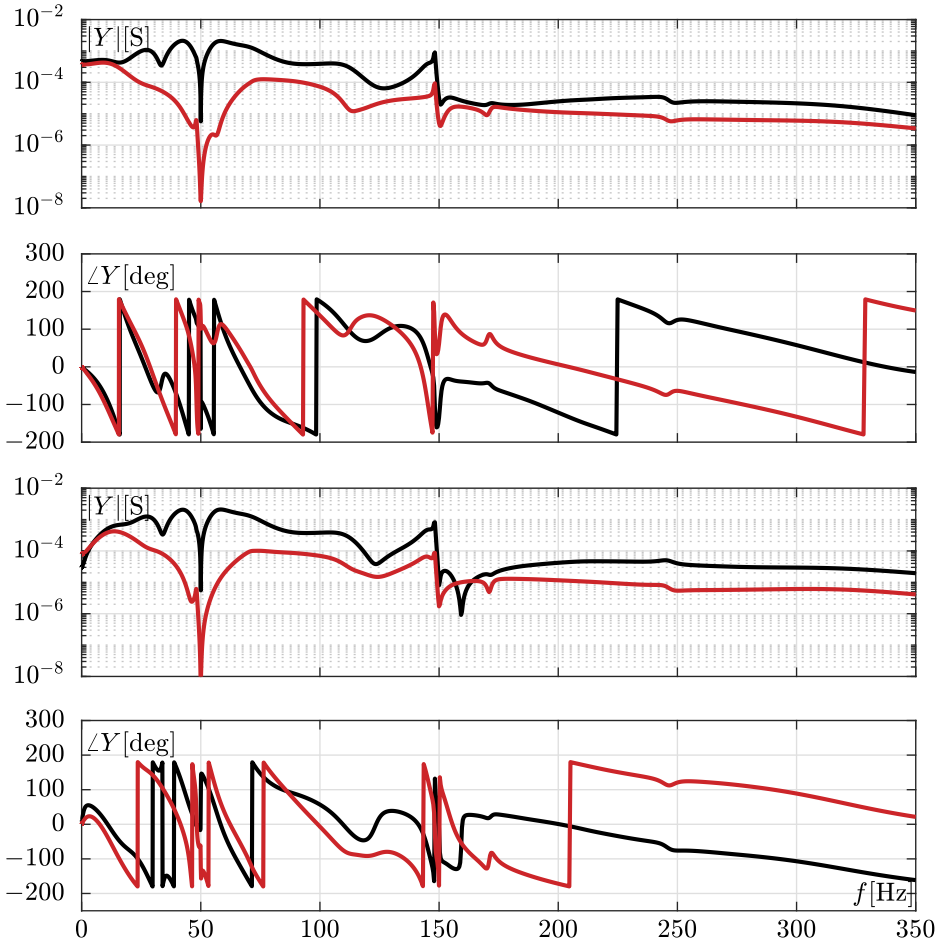


Figure 4.8: *Panel are listed from top. Panel 1: moduli of* $Y^{(0)}_{a^{AC1}a^{AC2}}$ *(black) and* $Y^{(0)}_{b^{AC1}a^{AC2}}$ *(red). Panel 2: phases of* $Y^{(0)}_{a^{AC1}a^{AC2}}$ *(black) and* $Y^{(0)}_{b^{AC1}a^{AC2}}$ *(red). Panel 3: moduli of* $Y^{(0)}_{a^{AC2}a^{AC1}}$ *(black) and* $Y^{(0)}_{b^{AC2}a^{AC1}}$ *(red). Panel 4: phases of* $Y^{(0)}_{a^{AC2}a^{AC1}}$ *(black) and* $Y^{(0)}_{b^{AC2}a^{AC1}}$ *(red).*

4.4.4 Stability analysis through vector fitting

Once the admittances of the MMC have been derived numerically, they can be represented in closed-form with the VF algorithm, which then allows performing several stability analyses. To showcase this feature, this section investigates as an example instabilities triggered by the insertion of inductor-based Fault Current Limiters (FCLs) at each pole of the DC side of Cm-C1 MMC in case (c).

As their name suggests, FCLs can be inserted in the DC network to limit

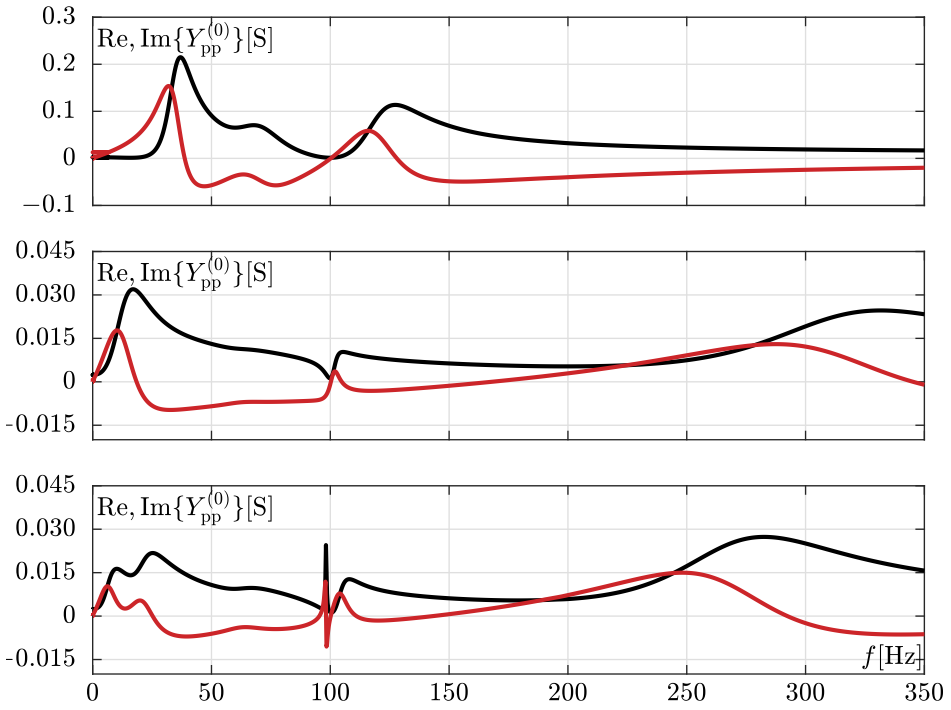


Figure 4.9: *The real (black) and imaginary (red) components of the $Y_{pp}^{(0)}$ admittances of the (a), (b) and (c) case studies (see Fig. 4.6(a-c)). Real and imaginary parts of $Y_{pp}^{(0)}$ are displayed in panels from top to bottom for the (a), (b) and (c) cases.*

the rate of rise of DC short circuit currents. One of the many ways to implement them is through the insertion of inductors [61]. Despite being the simplest solution, the main shortcoming of inductor-based FCLs is that they may trigger instabilities during normal operating conditions. For instance, this issue was recently reported in [28, 157, 181]. While in [28, 181] the authors showed that a too large inductance leads to instabilities, the authors of [157] came to the opposite conclusion (i.e., instability is triggered by too small inductance values). It thus seems that an interval of inductance values exists in which the insertion of a reactor limits the DC short circuit current without causing instability phenomena.

In any case, the important aspect is that the analysis described hereafter is performed after deriving an analytical model of the Cm-C1 MMC by applying VF to the numerical results provided by the PAC analysis. In principle, if this model is sufficiently simple, it allows designers to perform conventional pen-and-paper analyses or based on programming languages such as MATLAB or Python. In this work, a parametric stability analysis is

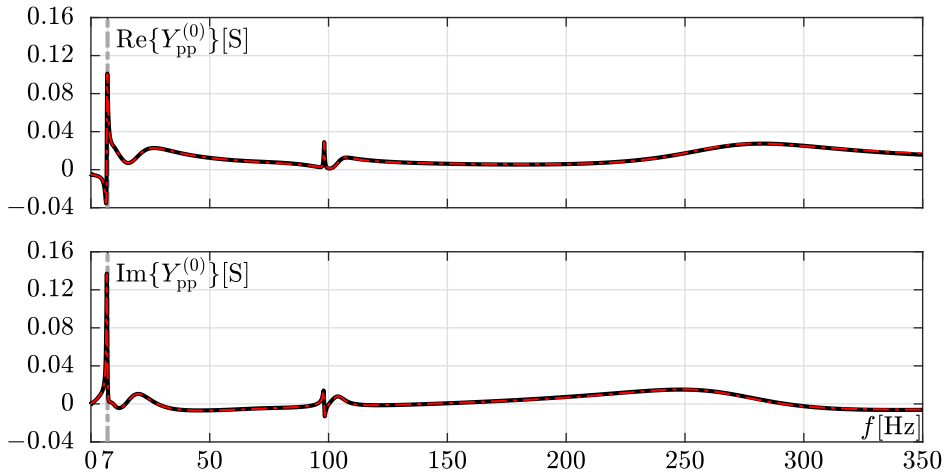


Figure 4.10: *The real and imaginary parts of $Y_{pp}^{(0)}$ of the modified system in Fig. 4.6(c). Black traces refer respectively to the real and imaginary part of Y_{pp}^{0} obtained numerically with* PAC*, while the dashed red lines correspond to the results obtained with* VF*.*

carried out with simple MATLAB scripts by sweeping the inductance of the FCLs connected to the Cm-C1 MMC across a given range.

To this end, the $Y_{pp}^{(0)}$ admittance of the case (c) was computed again by resorting to PAC and a modified version of the system in Fig. 4.6(c). In this version, the power setpoint of Cm-C1 MMC was varied with $6\,\mathrm{s}$-long steps of $-100\,\mathrm{MW}$, reaching a final value of $-800\,\mathrm{MW}$. Moreover, the integral and proportional gains of the PI regulators k_{i_i} and k_{p_i} of the MMC *decoupled current control* were respectively reduced to 30 and 0.16. Lastly, the *deadband control* in Fig. A.2 was deactivated by setting the parameter $k_{p_{db}}$ to zero.[20] The reader can refer to Table 3.6 for the original values of these parameters.

Figure 4.10 illustrates the real and imaginary parts of $Y_{pp}^{(0)}$, obtained with PAC and VF, when the MMC reference power reaches $-800\mathrm{MW}$. The real part of $Y_{pp}^{(0)}$ has a negative peak at about $7\,\mathrm{Hz}$: this negative impedance is a consequence of power flowing from the DC-side to the AC side (i.e., reference power is negative). The VF process required 15 poles for the closed-form results to match the numerical ones obtained with PAC.

If an inductor is connected at each pole of the DC side of Cm-C1 MMC,

[20]These amendments, albeit debatable from a design standpoint, were implemented to reduce stability margins and trigger instability by adding inductor-based FCLs of plausible inductance.

the equivalent DC side admittance $Y^{(0)}_{pp_{new}}$ becomes:

$$Y^{(0)}_{pp_{new}} = \frac{Y^{(0)}_{pp}\frac{1}{sL_{dc}}}{Y^{(0)}_{pp} + \frac{1}{sL_{dc}}} = \frac{Y^{(0)}_{pp}}{1 + sL_{dc}Y^{(0)}_{pp}}, \tag{4.27}$$

where L_{dc} is the inductance of the FCL. The expression in Eq. (4.27) is equivalent to the closed-loop transfer function of a feedback system, where $Y^{(0)}_{pp}$ and sL_{dc} lie respectively in the forward and feedback paths. The root locus of the system allows studying how the poles vary with respect to L_{dc}. The expected result is that, as L_{dc} increases, some poles move to the right half of the s-plane, thus making the system unstable. Note that this analysis can be carried out only because the VF provides the analytic expression of $Y^{(0)}_{pp}$ used in Eq. (4.27).

The top panels of Fig. 4.11 show the root locus of the system in Eq. (4.27). The markers in the top right panel indicate how a pole varies when L_{dc} is equal to $50, 75, 100$, and $125\,\mathrm{mH}$. These markers show that the system is surely unstable for $L_{dc} \geq 100\,\mathrm{mH}$, since at least one pole lies in the right half of the s-plane. The bottom panels of Fig. 4.11 depict the Nyquist diagram of the open-loop transfer function in Eq. (4.27) for $L_{dc} = 100\,\mathrm{mH}$. The point (-1,0) is encircled, confirming system instability.[21]

To verify these predictions, a time-domain simulation of the modified test system was performed by considering the previously mentioned inductance values. The corresponding results are shown in Fig. 4.12. As expected , when L_{dc} is equal to $100\,\mathrm{mH}$ or $125\,\mathrm{mH}$, instability occurs. Indeed, in both cases, the DC-side voltage diverges when the reference power reaches $-800\,\mathrm{MW}$. On the contrary, the power exchange is bounded between two extremes (see the lower panel for $t \geq 42\,\mathrm{s}$) due to the presence of the *reference current limiter* in the MMC control scheme.

4.4.5 From baseband to the second harmonic

Another interesting feature of PAC is its capability of analysing the effects of frequency up-conversion (folding) of the small-signal perturbations. Considering case (a), this section analyses $Y^{(2)}_{pa}$, that is, the effects of the frequency folding of the small-signal η_a at $2f_0$ (i.e., in the right-side band of the second harmonic) on the small-signal current flowing through η_p in the infinite DC bus. Due to the periodic working mode of the MMC

[21] For the sake of completeness, PAC and VF were used for each power reference step shown in Fig. 4.12. Then, the corresponding Nyquist plots (not reported here for space reasons) obtained by letting $L_{dc} = 100\,\mathrm{mH}$ were examined to verify that the point $(-1, 0)$ in the Nyquist plot is encircled (i.e., instability occurs) only when the reference power reaches $-800\,\mathrm{MW}$. The same was done for the case $L_{dc} = 125\,\mathrm{mH}$.

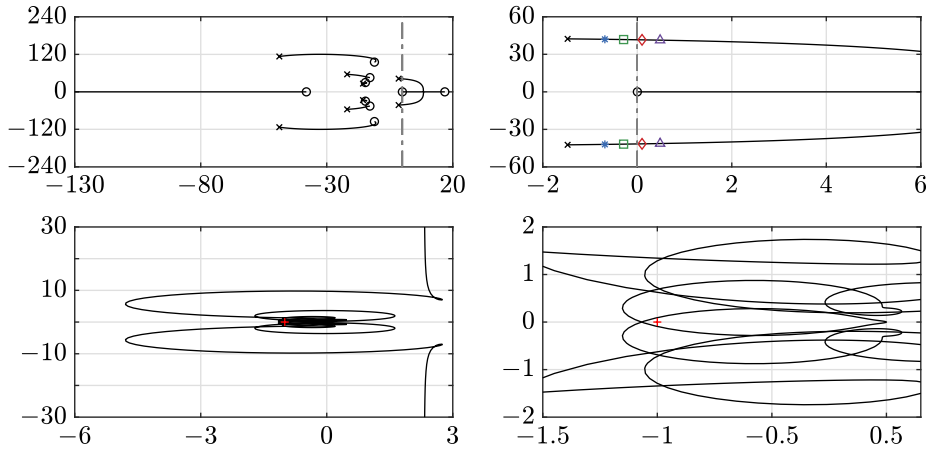


Figure 4.11: *Upper panels: root locus of Eq. (4.27) as a function of L_{dc} (left) and its inset (right) (stable poles that lie further away in the left half plane are not shown). In the inset, the $*$, $\square$, $\diamond$, and $\triangle$ markers indicate the value of some poles in the root locus when L_{dc} is respectively equal to $50, 75, 100$, and $125\,\mathrm{mH}$. Lower panels: Nyquist diagram of $\mathbb{j}\omega L_{dc} Y^0_{pp}$ when $L_{dc} = 100\,\mathrm{mH}$ (left) and its inset (right). The $+$ marker denotes the point $(-1, 0)$. x-axis: real part; y-axis: imaginary part.*

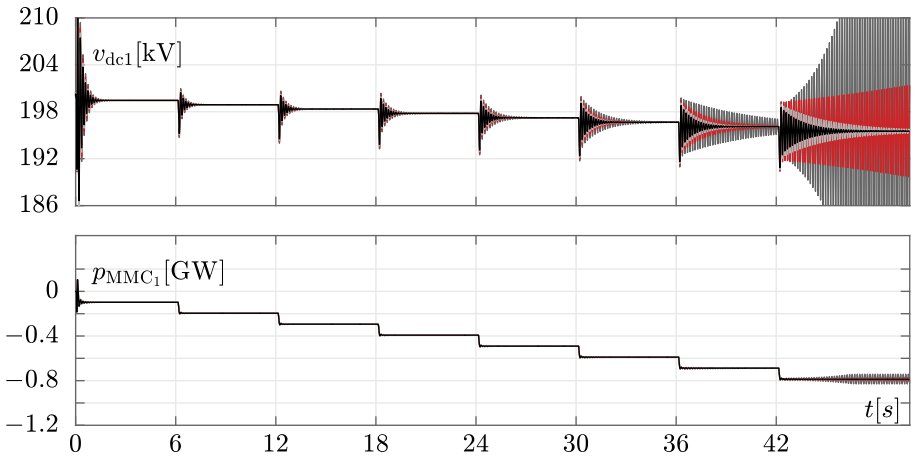


Figure 4.12: *Simulation results of the modified system in Fig. 4.6(c), obtained by inserting an inductance L_{dc} at each pole of the* DC *side of Cm-C1* MMC*. Upper panel: Cm-C1* MMC *positive pole to ground voltage. Lower panel: Cm-C1* MMC *active power exchange. In the first* $150\,\mathrm{ms}$ *of simulation the entire system undergoes a turn-on phase. In both panels, the black, grey, red, and dark grey lines correspond to simulations results obtained with a value of L_{dc} respectively equal to 50, 75, 100, and* $125\,\mathrm{mH}$.

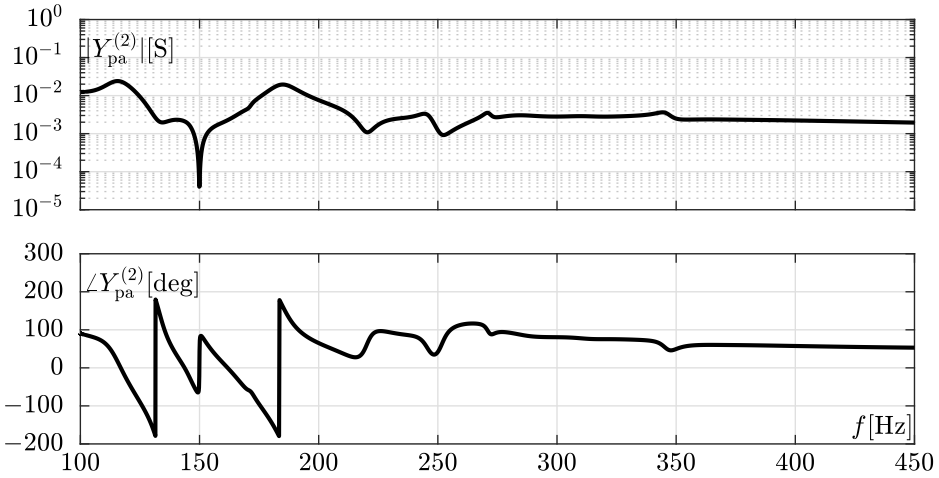


Figure 4.13: *The module and phase of the $Y^{(2)}_{pa}$ admittance of the power system configuration in Fig. 4.6(c). Upper panel: module of $Y^{(2)}_{pa}$. Lower panel: phase of $Y^{(2)}_{pa}$. The superscript $^{(2)}$ indicates frequency up-conversion at the second harmonic.*

and its circulating currents, a second harmonic component may be present in the DC line current. Figure 4.13 depicts the admittance $Y^{(2)}_{pa}$ obtained in this case. It is worth recalling that the frequencies on the f-axis must be read as $2f_0 + {}^1\!/_{T_\eta} = 100\,\mathrm{Hz} + {}^1\!/_{T_\eta}$. For example, a small-signal perturbation at ${}^1\!/_{T_\eta} = 1\,\mathrm{Hz}$ of the η_a source in the AC1 grid thus folds at $100\,\mathrm{Hz} + 1\,\mathrm{Hz}$ in the frequency axis.

4.4.6 Unbalanced operating conditions

As already stated, versatility is one of the strongest points of PAC. For instance, if the effect of new controls or system parameters needs to be assessed, simulations are simply repeated after editing the circuit under analysis. Then, PAC is used again to derive the new entries of the MMC admittance, without needing to perform extensive pen-and-paper calculations. The same holds when investigating unbalanced operating conditions.

To validate this statement, the AC1 grid of case (a) was modified. In general, the AC systems in the simulated grids comprise three-phase balanced voltage sources in series with an impedance (see Fig. 3.2). In this case, however, the voltage source $v_a(t)$ was slightly changed as shown by the black line in the top panel of Fig. 4.14 to generate unbalanced operating conditions. The bottom panel of the same figure reports the resulting phase currents when the reference power of the Cm-C1 MMC is $400\,\mathrm{MW}$.

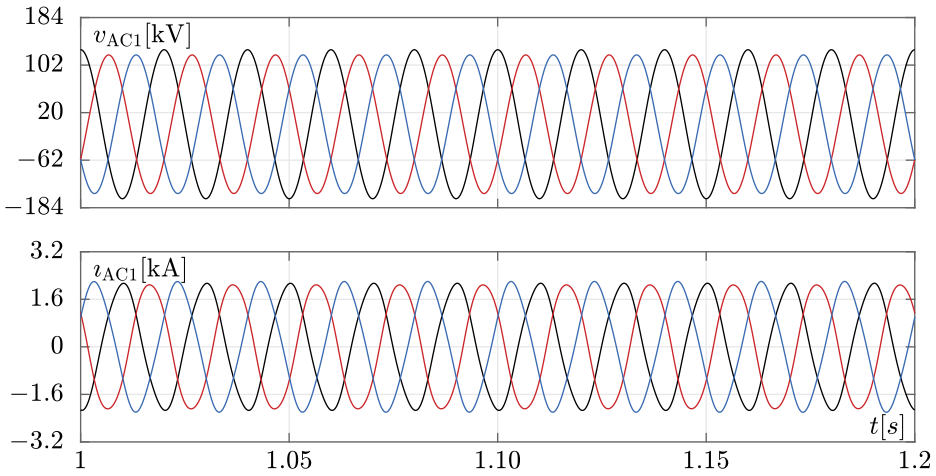


Figure 4.14: *Phase voltages (upper panel) and currents (lower panel) of the* AC1 *grid in Fig. 4.6(c) in unbalanced operating conditions. In both panels, the black, blue, and red lines refer respectively to phases a, b, and c.*

As an example, Fig. 4.15 compares the $Y_{pa}^{(0)}$ admittance obtained during balanced and unbalanced operating conditions. By looking at the upper panel, one can notice that the module of $Y_{pa}^{(0)}$ is similar in both cases. This indicates that the large-signal voltage unbalance acts on the HVDC link current in an almost linear way: for example, by doubling the magnitude of the former, the ripple of the latter doubles as well.

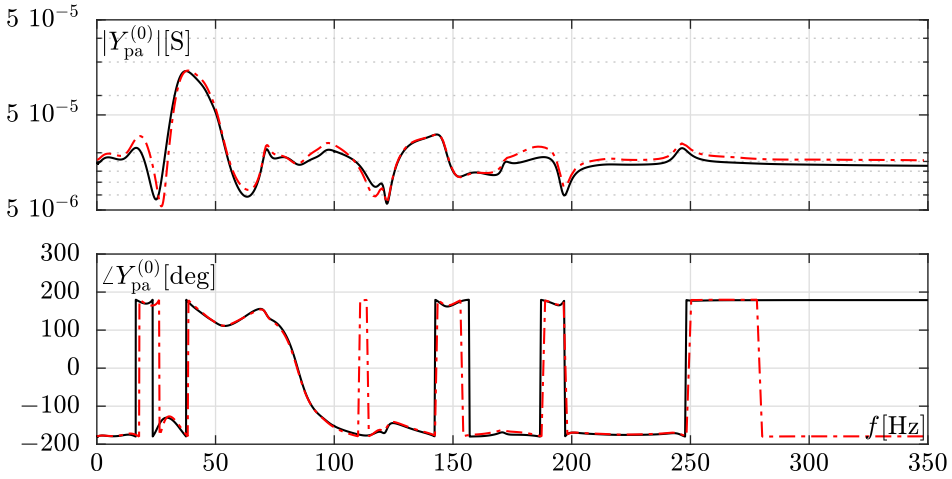


Figure 4.15: *The module and phase of the $Y_{pa}^{(0)}$ admittance of the power system configuration shown in Fig. 4.6(c) in balanced (black solid line) and unbalanced (red dashed line) operating conditions. Upper panel: module of $Y_{pa}^{(0)}$. Lower panel: phase of $Y_{pa}^{(0)}$.*

Conclusion

The research presented in this thesis focused on circuit simulation and analysis techniques specifically tailored for modular multilevel converters (MMCs), which have lately become a hot topic in the research community. In particular, the research was mainly devoted to (i) the development of a fast and accurate EMT simulation technique for MMCs based on isomorphism and (ii) the application of the periodic small-signal analysis (PAC) to high-voltage direct current (HVDC) systems comprising MMCs.

Electromagnetic transient simulation of MMCs based on isomorphism

The key features of the isomorphism-based MMC simulation approach can be summarised as follows. First, the method is compatible with any submodule (SM) model, ranging from the simple bi-value resistor (BVR) to the detailed full physics (FP) one. Second, this approach minimizes the number of SMs to be simulated, thereby significantly boosting simulation speed without sacrificing accuracy. Thus, the approach allows performing detailed simulations in a reasonable CPU time. Lastly, regardless of the SM model adopted, the computational burden of the proposed method increases only linearly with the number of SMs in each MMC arm. This is in sharp contrast with conventional simulation approaches, where this trend evolves almost quadratically. It is worth highlighting that this feature is attained without simplifying neither the SMs model nor that of the entire MMC, as instead is done in several accelerated simulation models in the literature.

To support these claims, a modified version of the Cigré DCS1 test

system (comprising two MMCs connected with an HVDC link) was simulated by considering SM models of different degrees of detail and several operating scenarios (i.e., normal operating conditions, symmetrical and asymmetrical AC and DC-side faults). In each case, the conventional and isomorphism-based simulation approaches were compared to verify the accuracy and speed of the latter.

The case study above proved that the isomorphism-based method is ideal for EMT simulation of MMCs during component and system studies, which typically require detailed SM models. In the case of network level studies, which involve large AC networks, other MMC models might be preferred because they reduce the computational burden and the focus would no longer be the analysis of specific converter features. However, it is worth pointing out that, depending on the version considered, these simplified models neglect some converter controls (e.g., circulating current control, modulation techniques, capacitor voltage balancing) and some internal dynamics. The simulation results obtained with these models approximately adhere to those of more detailed ones provided that these missing elements, if considered, do not lead to significant deviations in the system behaviour. This check can only be performed by using detailed, yet efficient MMC models and simulation approaches such as that proposed in this thesis.

For what concerns possible future studies concerning the topic of isomorphism, the proposed technique has general validity and can be profitably exploited in grids comprising structurally identical elements with sufficiently similar behaviour. For instance, future research might be aimed at exploiting it to efficiently simulate wind farms, which connect multiple wind power plants usually characterised by the same model. A commonly adopted solution in the literature and power system simulators to reduce the computational burden is to aggregate these plants dynamically. Despite leading to a reduced computational burden, this process is not accurate, as it produces significantly different values of damping to the modes close to the second, fifth, and seventh harmonics of the power system frequency [182]. This issue may not arise when resorting to the isomorphism-based method.

Also photovoltaic parks lend themselves to isomorphism-based simulation. Indeed, these systems comprise structurally identical photovoltaic panels that, however, may not always operate in the same way due to shading and other mismatches [183]. On the one hand, the simulation of each panel individually would result in an excessive computational burden - especially when detailed panel models are used. On the other hand, despite reducing simulation time, aggregate models typically do not retain the individual behaviour of each panel, which may be of interest, for example,

when investigating extreme operating conditions [184]. In this context, the isomorphism-based method should boost simulation efficiency, while allowing the analysis of specific contingencies affecting one or more panels, such as hot spots.

Periodic small-signal analysis applied to MMCs

For what concerns PAC, this numerical method has several advantages compared to other alternatives to small-signal analysis compatible with power systems comprising MMCs, based on dynamic phasors or harmonic state-space analysis. First, being a numerical technique directly implementable at the simulator level, PAC requires neither extensive pen-and-paper computations nor simplifications in the model of the system under study, MMCs included. Second, it does not rely on computationally intensive EMT simulation to derive the small-signal response of the system, but rather conveniently exploits the fundamental matrix - a byproduct of the shooting method (SHM). Lastly, the method can take into account intermodulation and frequency up- and down-conversion of a perturbing signal in the frequency spectrum. For example, it can compute how a low frequency (e.g., $1\,\mathrm{Hz}$) small-signal perturbation in the HVDC link can be up-converted to $50 + 1\,\mathrm{Hz}$ in the AC system.

PAC is still a relatively new approach in the power system realm and requires further study. For instance, a possible follow-up research direction could be devoted to better interpreting the PAC results associated with frequency folding and understanding in which cases they might be relevant for power system stability. Another field of investigation may be related to the adoption of PAC to detect stability issues in HVDC systems connected to wind farms, such as subsynchronous resonances. This topic was the main focus of a recent report [185].

MMC initialization: a still open challenge

As a last remark, according to Section 3.1.5, the initialization of detailed MMC models for EMT simulations is a complicated task that, at the time of writing, has been addressed only by a few papers in the literature. The incapability of performing it implies that initialization transients are necessary for MMC-based systems to reach steady-state operation before simulating events in the network. Due to the high computational burden required to simulate MMCs, this practice should be avoided as much as possible. In principle, the shooting method (SHM) described in Section 4.3.1 could be used to address this issue. However, as mentioned in Section 4.4, the main

issue in this context is that detailed MMC models include Capacitor voltage Balancing Algorithms (CBAs) and Nearest Level Modulation (NLM) (or other modulation techniques). The presence of these controls results in MMC-based grids being hybrid dynamical systems. Thus, despite representing a generally viable solution to initialize power systems, the SHM cannot be straightforwardly employed in this case because the determination of the steady-state working period T of such systems is a challenging aspect. This issue could be tackled in future research work.

APPENDIX $\mathcal{A}$

Modular multilevel converter control strategy in unbalanced operating conditions

Section 1.3 describes a typical MMC control architecture (shown in Fig. 1.10) adopted in balanced operating conditions (i.e., the three-phase quantities of any electrical variable in the system have equal magnitude but are 120° out of phase with each other clockwise). In some cases, however, the converter may witness abnormal operating conditions, such as single-phase to ground or phase-to-phase faults (i.e., asymmetrical faults), which lead to voltage and current unbalances in the three phases. For instance, in the immediate aftermath of a solid single-phase to ground fault[1], the voltage of the faulted phase at the point of the fault is null, while that of the other phases is not.

The increasing penetration of MMCs (and other converters) in modern electric power systems requires them to be able to cope with the above-mentioned faults, preferably until they are somehow cleared by the network operator. According to [148], single-phase to ground faults have the lowest fault current magnitude but also the highest rate of occurrence. On the con-

[1]Regardless of the case considered, a *solid* (or *bolted*) fault is such that its fault impedance is null [148].

trary, three-phase faults, despite being the most dangerous, occur the least frequently. This simple observation suggests the importance of developing control schemes also compatible with unbalanced operating conditions.

This appendix describes the MMC control strategy used in this work to cope with such occurrences. Compared to its counterpart in Fig. 1.10, the main differences - detailed in the following sections - relate to the *upper level controls*, the *circulating current suppression control*, and the PLL. On the contrary, the remaining controls and measured variables used in the control strategy (i.e., those shown in red in Fig. 1.10) remain the same.

A.1 Space vector and power in unbalanced operating conditions

To begin with, consider the generic unbalanced three-phase set of variables

$$\begin{aligned} x_a(t) &= X_a \cos(\delta(t) + \alpha_a) \\ x_b(t) &= X_b \cos(\delta(t) + \alpha_b) \\ x_c(t) &= X_c \cos(\delta(t) + \alpha_c) \ . \end{aligned} \tag{A.1}$$

The unbalance in this three-phase set may be given by the fact that the magnitudes X_a, X_b, and X_c could be different, and that the angles α_a, α_b, and α_c may not be 120° out of phase with each other clockwise. By resorting to the so-called *sequence transformation* described in Eq. (A.2) (also referred to as *Fortescue transformation*), this three-phase set can be regarded as shown in Eq. (A.3) as the superposition of three components - namely the positive, negative, and zero sequences [57, 148, 186].[2]

$$\begin{bmatrix} x^p(t) \\ x^n(t) \\ x^0(t) \end{bmatrix} = \overbrace{\sqrt{\frac{1}{3}} \begin{bmatrix} 1 & e^{\mathbb{j}\frac{2\pi}{3}} & e^{-\mathbb{j}\frac{2\pi}{3}} \\ 1 & e^{-\mathbb{j}\frac{2\pi}{3}} & e^{-\mathbb{j}\frac{2\pi}{3}} \\ 1 & 1 & 1 \end{bmatrix}}^{\boldsymbol{F}} \begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} \tag{A.2}$$

$$\begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} = \underbrace{\begin{bmatrix} \frac{X^p}{\sqrt{3}} \cos(\delta(t)+\alpha^p) \\ \frac{X^p}{\sqrt{3}} \cos\left(\delta(t)+\alpha^p-\frac{2\pi}{3}\right) \\ \frac{X^p}{\sqrt{3}} \cos\left(\delta(t)+\alpha^p+\frac{2\pi}{3}\right) \end{bmatrix}}_{\text{Positive sequence}} + \underbrace{\begin{bmatrix} \frac{X^n}{\sqrt{3}} \cos(\delta(t)+\alpha^n) \\ \frac{X^n}{\sqrt{3}} \cos\left(\delta(t)+\alpha^n+\frac{2\pi}{3}\right) \\ \frac{X^n}{\sqrt{3}} \cos\left(\delta(t)+\alpha^n-\frac{2\pi}{3}\right) \end{bmatrix}}_{\text{Negative sequence}} + \underbrace{\begin{bmatrix} \frac{x^0(t)}{\sqrt{3}} \\ \frac{x^0(t)}{\sqrt{3}} \\ \frac{x^0(t)}{\sqrt{3}} \end{bmatrix}}_{\text{Zero sequence}} \tag{A.3}$$

[2] The inverse Fortescue transformation, used to obtain Eq. (A.3), can be derived by exploiting the orthogonality of the matrix in $\boldsymbol{F}$ (i.e., $\boldsymbol{F}^{-1} = \boldsymbol{F}^T$). In sinusoidal steady-state operation, $x^p(t) = X^p \cos(\delta(t) + \alpha^p)$ and $x^n(t) = X^n \cos(\delta(t) + \alpha^n)$.

The positive and negative sequences are associated with all the three-phase variables that are equal in magnitude but are 120° out of phase with each other clockwise and counterclockwise, respectively. On the contrary, the zero sequence mirrors all the three-phase variables that are always equal. During balanced operating conditions, only the positive sequence exists. The other two sequences arise when unbalances occur.

The three-phase variables associated with the positive and negative sequences are related to the positive and quadrature Park components $x_d^p(t)$, $x_q^p(t)$, $x_d^n(t)$, and $x_q^n(t)$, defined as shown in Eqs. (A.4) and (A.5).[3] These terms are generally time-varying but become constant if a value of $\theta(t)$ such that $\frac{d\theta}{dt} = \frac{d\delta}{dt} = \omega$ is adopted (e.g., a PLL synchronizes the DQ0 and ABC frames). However, it is important to notice that the two equations rely on two distinct Park transformations: one adopts $\mathbf{\Gamma}(\theta(t))$, while the other $\mathbf{\Gamma}(-\theta(t))$. This difference is given by the fact that the three-phase variables associated with the positive and negative sequences rotate in opposite directions. Indeed, if the Park transformations $\mathbf{\Gamma}(\theta(t))$ and $\mathbf{\Gamma}(-\theta(t))$ were used respectively for the negative and positive sequences, direct and quadrature components rotating at twice the fundamental frequency would be obtained instead of constant ones [151].

$$\begin{bmatrix} x_d^p(t) \\ x_q^p(t) \\ 0 \end{bmatrix} = \mathbf{\Gamma}(\theta(t)) \begin{bmatrix} \frac{X^p}{\sqrt{3}} \cos(\delta(t) + \alpha^p) \\ \frac{X^p}{\sqrt{3}} \cos\left(\delta(t) + \alpha^p - \frac{2}{3}\pi\right) \\ \frac{X^p}{\sqrt{3}} \cos\left(\delta(t) + \alpha^p + \frac{2}{3}\pi\right) \end{bmatrix} \tag{A.4}$$

$$\begin{bmatrix} x_d^n(t) \\ x_q^n(t) \\ 0 \end{bmatrix} = \mathbf{\Gamma}(-\theta(t)) \begin{bmatrix} \frac{X^n}{\sqrt{3}} \cos(\delta(t) + \alpha^n) \\ \frac{X^n}{\sqrt{3}} \cos\left(\delta(t) + \alpha^n + \frac{2}{3}\pi\right) \\ \frac{X^n}{\sqrt{3}} \cos\left(\delta(t) + \alpha^n - \frac{2}{3}\pi\right) \end{bmatrix} \tag{A.5}$$

In the light of the above, the expression of $x_a(t)$, $x_b(t)$, and $x_c(t)$ can be recast as follows by resorting to inverse Park transformations.

$$\begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} = \mathbf{\Gamma}^{-1}(\theta(t)) \begin{bmatrix} x_d^p(t) \\ x_q^p(t) \\ 0 \end{bmatrix} + \mathbf{\Gamma}^{-1}(-\theta(t)) \begin{bmatrix} x_d^n(t) \\ x_q^n(t) \\ 0 \end{bmatrix} + \begin{bmatrix} \frac{1}{\sqrt{3}} x^0(t) \\ \frac{1}{\sqrt{3}} x^0(t) \\ \frac{1}{\sqrt{3}} x^0(t) \end{bmatrix} \tag{A.6}$$

Starting from its general definition in Eq. (1.5), the so-called *space vector* $\bar{x}(t)$ corresponding to the three-phase set in Eq. (A.1) can be written

[3] The homopolar components in Eqs. (A.4) and (A.5) are null because the sum of the three-phase variables in the positive and negative sequences is null, too.

as reported in Eq. (A.7). The terms A, B, C, D, and E are derived in Eqs. (A.8) and (A.9). Hereafter, the time dependency of some variables is omitted for brevity.

$$\begin{aligned}\bar{x}(t) &= \sqrt{\frac{2}{3}}\left(x_a(t) + x_b(t)e^{\mathbb{j}\frac{2\pi}{3}} + x_c(t)e^{-\mathbb{j}\frac{2\pi}{3}}\right) = \\ &= \sqrt{\frac{2}{3}}\left(A+B+C+D+E\right) = \\ &= \left(x_d^p + \mathbb{j}x_q^p\right)e^{\mathbb{j}\theta} + \left(x_d^n + \mathbb{j}x_q^n\right)e^{-\mathbb{j}\theta}\,.\end{aligned} \tag{A.7}$$

$$\begin{aligned}A &= \sqrt{\frac{2}{3}}x_d^p\left[\cos(\theta) + \cos\left(\theta-\frac{2\pi}{3}\right)e^{\mathbb{j}\frac{2\pi}{3}} + \cos\left(\theta+\frac{2\pi}{3}\right)e^{-\mathbb{j}\frac{2\pi}{3}}\right] = \\ &= \frac{x_d^p}{2}\sqrt{\frac{2}{3}}\left\{e^{\mathbb{j}\theta} + e^{-\mathbb{j}\theta} + \left[e^{\mathbb{j}\left(\theta-\frac{2\pi}{3}\right)} + e^{-\mathbb{j}\left(\theta-\frac{2\pi}{3}\right)}\right]e^{\mathbb{j}\frac{2\pi}{3}} + \right. \\ &\quad \left.\left[e^{\mathbb{j}\left(\theta+\frac{2\pi}{3}\right)} + e^{-\mathbb{j}\left(\theta+\frac{2\pi}{3}\right)}\right]e^{-\mathbb{j}\frac{2\pi}{3}}\right\} = \\ &= \frac{x_d^p}{2}\sqrt{\frac{2}{3}}\left[3e^{\mathbb{j}\theta}\underbrace{+e^{-\mathbb{j}\theta} + e^{-\mathbb{j}\left(\theta-\frac{4\pi}{3}\right)} + e^{-\mathbb{j}\left(\theta+\frac{4\pi}{3}\right)}}_{\equiv 0}\right] = \sqrt{\frac{3}{2}}x_d^p e^{\mathbb{j}\theta}\end{aligned}$$

$$\begin{aligned}B &= -\sqrt{\frac{2}{3}}x_q^p\left[\sin(\theta) + \sin\left(\theta-\frac{2\pi}{3}\right)e^{\mathbb{j}\frac{2\pi}{3}} + \sin\left(\theta+\frac{2\pi}{3}\right)e^{-\mathbb{j}\frac{2\pi}{3}}\right] = \\ &= \mathbb{j}\frac{x_q^p}{2}\sqrt{\frac{2}{3}}\left\{e^{\mathbb{j}\theta} - e^{-\mathbb{j}\theta} + \left[e^{\mathbb{j}\left(\theta-\frac{2\pi}{3}\right)} - e^{-\mathbb{j}\left(\theta-\frac{2\pi}{3}\right)}\right]e^{\mathbb{j}\frac{2\pi}{3}} + \right. \\ &\quad \left.\left[e^{\mathbb{j}\left(\theta+\frac{2\pi}{3}\right)} - e^{-\mathbb{j}\left(\theta+\frac{2\pi}{3}\right)}\right]e^{-\mathbb{j}\frac{2\pi}{3}}\right\} = \\ &= \mathbb{j}\frac{x_q^p}{2}\sqrt{\frac{2}{3}}\left[3e^{\mathbb{j}\theta}\underbrace{-e^{-\mathbb{j}\theta} - e^{-\mathbb{j}\left(\theta-\frac{4\pi}{3}\right)} - e^{-\mathbb{j}\left(\theta+\frac{4\pi}{3}\right)}}_{\equiv 0}\right] = \mathbb{j}\sqrt{\frac{3}{2}}x_q^p e^{\mathbb{j}\theta}\end{aligned} \tag{A.8}$$

$$\begin{aligned}C &= \sqrt{\frac{2}{3}}x_d^n\left[\cos(-\theta) + \cos\left(-\theta+\frac{2\pi}{3}\right)e^{\mathbb{j}\frac{2\pi}{3}} + \cos\left(-\theta+\frac{2\pi}{3}\right)e^{-\mathbb{j}\frac{2\pi}{3}}\right] = \\ &= \frac{x_d^n}{2}\sqrt{\frac{2}{3}}\left\{e^{\mathbb{j}\theta} + e^{-\mathbb{j}\theta} + \left[e^{\mathbb{j}\left(\theta+\frac{2\pi}{3}\right)} + e^{-\mathbb{j}\left(\theta+\frac{2\pi}{3}\right)}\right]e^{\mathbb{j}\frac{2\pi}{3}} + \right. \\ &\quad \left.\left[e^{\mathbb{j}\left(\theta-\frac{2\pi}{3}\right)} + e^{-\mathbb{j}\left(\theta-\frac{2\pi}{3}\right)}\right]e^{-\mathbb{j}\frac{2\pi}{3}}\right\} = \\ &= \frac{x_d^n}{2}\sqrt{\frac{2}{3}}\left[3e^{-\mathbb{j}\theta}\underbrace{+e^{\mathbb{j}\theta} + e^{\mathbb{j}\left(\theta+\frac{4\pi}{3}\right)} + e^{\mathbb{j}\left(\theta-\frac{4\pi}{3}\right)}}_{\equiv 0}\right] = \sqrt{\frac{3}{2}}x_d^n e^{-\mathbb{j}\theta}\end{aligned}$$

$$
\begin{aligned}
D &= -\sqrt{\frac{2}{3}}x_q^n\left[\sin(-\theta)+\sin\left(-\theta-\frac{2\pi}{3}\right)e^{\mathbb{j}\frac{2\pi}{3}}+\sin\left(-\theta+\frac{2\pi}{3}\right)e^{-\mathbb{j}\frac{2\pi}{3}}\right]= \\
&= \mathbb{j}\frac{x_q^n}{2}\sqrt{\frac{2}{3}}\left\{-e^{\mathbb{j}\theta}+e^{-\mathbb{j}\theta}-\left[e^{\mathbb{j}\left(\theta-\frac{2\pi}{3}\right)}-e^{-\mathbb{j}\left(\theta-\frac{2\pi}{3}\right)}\right]e^{\mathbb{j}\frac{2\pi}{3}}+\right. \\
&\quad \left.-\left[e^{\mathbb{j}\left(\theta+\frac{2\pi}{3}\right)}-e^{-\mathbb{j}\left(\theta+\frac{2\pi}{3}\right)}\right]e^{-\mathbb{j}\frac{2\pi}{3}}\right\}= \\
&= \mathbb{j}\frac{x_q^n}{2}\sqrt{\frac{2}{3}}\left[3e^{-\mathbb{j}\theta}\underbrace{-e^{\mathbb{j}\theta}-e^{\mathbb{j}\left(\theta-\frac{4\pi}{3}\right)}-e^{\mathbb{j}\left(\theta+\frac{4\pi}{3}\right)}}_{\equiv 0}\right]=\mathbb{j}\sqrt{\frac{3}{2}}x_q^n e^{-\mathbb{j}\theta} \\
E &= x^0\underbrace{\left(1+e^{\mathbb{j}\frac{2\pi}{3}}+e^{-\mathbb{j}\frac{2\pi}{3}}\right)}_{\equiv 0}=0
\end{aligned}
\tag{A.9}
$$

Analogously to Eq. (1.8), based on the Park inverse transformation and Eqs. (A.3) and (A.7), the variables in the ABC-frame (x_a, x_b, and x_c) can also be derived from their corresponding space phasor $\bar{x}$ and zero sequence component x^0 as

$$
\begin{aligned}
x_a &= \sqrt{\tfrac{2}{3}}\mathrm{Re}\{\bar{x}\}+\sqrt{\tfrac{1}{3}}x^0 \\
x_b &= \sqrt{\tfrac{2}{3}}\mathrm{Re}\{\bar{x}e^{-\mathbb{j}\frac{2\pi}{3}}\}+\sqrt{\tfrac{1}{3}}x^0 \\
x_c &= \sqrt{\tfrac{2}{3}}\mathrm{Re}\{\bar{x}e^{\mathbb{j}\frac{2\pi}{3}}\}+\sqrt{\tfrac{1}{3}}x^0\,.
\end{aligned}
\tag{A.10}
$$

Consider now a three-phase element characterised by a set of (possibly unbalanced) voltages (v_a, v_b, and v_c) and currents ($\imath_a$, $\imath_b$, and $\imath_c$). Its instanteous power $p(t)$ can be computed as shown in Eq. (A.11) by exploiting the corresponding space phasors (i.e., $\bar{v}$ and $\bar{\imath}$) and zero sequence components (i.e., v^0 and $\imath^0$). For the sake of brevity, the mathematical steps required to obtain the final solution are omitted. The interested reader can find similar computations in [57].

$$
\begin{aligned}
p(t) &= v_a\imath_a+v_b\imath_b+v_c\imath_c= \\
&= \sum_{\alpha\in\{0,\pm\frac{2\pi}{3}\}}\left[\left(\sqrt{\frac{2}{3}}\mathrm{Re}\{\bar{v}e^{\mathbb{j}\alpha}\}+\sqrt{\frac{1}{3}}v^0\right)\left(\sqrt{\frac{2}{3}}\mathrm{Re}\{\bar{\imath}e^{\mathbb{j}\alpha}\}+\sqrt{\frac{1}{3}}\imath^0\right)\right]= \\
&= \ldots=\underbrace{\mathrm{Re}\{\bar{v}\bar{\imath}^*\}}_{P}+\underbrace{v^0\imath^0}_{P^0}\,.
\end{aligned}
\tag{A.11}
$$

Appendix A. Modular multilevel converter control strategy in unbalanced operating conditions

The computations above are analogous to those shown in Eq. (1.9) (except for the fact that here homopolar components are disregarded and replaced by zero sequence components[4]). However, the presence of possible unbalances leads to specialised formulas of the real, reactive, and complex powers different from those in Eq. (1.10). Indeed, the following holds.

$$
\begin{aligned}
P &= \mathrm{Re}\{\overline{v}\overline{\imath}^{*}\} = \\
&= \mathrm{Re}\Big\{\Big[\big(v_d^p + \mathbb{j} v_q^p\big)e^{\mathbb{j}\theta} + \big(v_d^n + \mathbb{j} v_q^n\big)e^{-\mathbb{j}\theta}\Big]\Big[\big(\imath_d^p + \mathbb{j}\,\imath_q^p\big)e^{\mathbb{j}\theta} + \big(\imath_d^n + \mathbb{j}\,\imath_q^n\big)e^{-\mathbb{j}\theta}\Big]^{*}\Big\} = \\
&= \ldots = v_d^p\imath_d^p + v_q^p\imath_q^p + v_d^n\imath_d^n + v_q^n\imath_q^n + \\
&\quad + \big(v_d^p\imath_d^n + v_q^p\imath_q^n + v_d^n\imath_d^p + v_q^n\imath_q^p\big)\cos(2\theta) + \\
&\quad + \big(v_q^n\imath_d^p - v_d^n\imath_q^p - v_q^p\imath_d^n + v_d^p\imath_q^n\big)\sin(2\theta) = \\
&= P_k + P_{c_2}\cos(2\theta) + P_{s_2}\sin(2\theta)
\end{aligned}
$$

$$
\begin{aligned}
Q &= \mathrm{Im}\{\overline{v}\overline{\imath}^{*}\} = \\
&= \mathrm{Im}\Big\{\Big[\big(v_d^p + \mathbb{j} v_q^p\big)e^{\mathbb{j}\theta} + \big(v_d^n + \mathbb{j} v_q^n\big)e^{-\mathbb{j}\theta}\Big]\Big[\big(\imath_d^p + \mathbb{j}\,\imath_q^p\big)e^{\mathbb{j}\theta} + \big(\imath_d^n + \mathbb{j}\,\imath_q^n\big)e^{-\mathbb{j}\theta}\Big]^{*}\Big\} = \\
&= \ldots = v_q^p\imath_d^p - v_d^p\imath_q^p + v_q^n\imath_d^n - v_d^n\imath_q^n + \\
&\quad + \big(v_q^p\imath_d^n - v_d^p\imath_q^n + v_q^n\imath_d^p - v_d^n\imath_q^p\big)\cos(2\theta) + \\
&\quad + \big(v_d^p\imath_d^n + v_q^p\imath_q^n - v_d^n\imath_d^p - v_q^n\imath_q^p\big)\sin(2\theta) = \\
&= Q_k + Q_{c_2}\cos(2\theta) + Q_{s_2}\sin(2\theta)
\end{aligned}
\tag{A.12}
$$

$$
S = \overline{v}\overline{\imath}^{*} = P + \mathbb{j}Q\,.
$$

If unbalances are absent (i.e., v_d^n, v_q^n, $\imath_d^n$, and $\imath_q^n$ are null), the formulas of active and reactive power in Eq. (A.12) become analogous to those shown in Eq. (1.10), which involve exclusively the products among the direct and quadrature components of the positive sequence. Indeed, in this case, $P = P_k = v_d^p\imath_d^p + v_q^p\imath_q^p$ and $Q = Q_k = v_q^p\imath_d^p - v_d^p\imath_q^p$. On the contrary, if unbalances occur, the terms P_k and Q_k also include terms associated with the negative sequence. Moreover, the active and reactive power terms P_{c_2}, P_{s_2}, Q_{c_2}, and Q_{s_2} appear. These variables cause periodic power fluctuations, whose frequency is twice the nominal one of the grid (i.e., 2θ[5]).

[4] The comparison of Eqs. (1.3) and (A.2) highlights that homopolar and zero sequence components share the same value and meaning: they are different from zero only if the sum of variables $x_a(t)$, $x_b(t)$, and $x_c(t)$ is not.

[5] It is assumed that $\frac{d\theta}{dt} = \omega$, meaning that a PLL ensures the synchronization of the ABC and DQ0 frames.

A.2 Phase-locked loop (PLL) in unbalanced operating conditions

As already stated, the components x_d^p, x_q^p, x_d^n, and x_q^n of a possibly unbalanced three-phase set of variables are in general time-varying. However, if the Park transformation uses a value of θ such that $\frac{d\theta}{dt} = \frac{d\delta}{dt} = \omega$ (i.e., the DQ0 and ABC frames are synchronized), these components become constant. This is accomplished by the PLL shown in Fig. A.1, which exploits the three-phase voltages v_a, v_b, and v_c depicted in Fig. 1.10.

Compared to its counterpart in Fig. 1.11, the PLL described here exhibits two main differences: the adoption of two Park transformations (i.e., $\mathbf{\Gamma}(\theta)$ and $\mathbf{\Gamma}(-\theta)$) and four notch filters, labelled as "NF" in Fig. A.1. As already mentioned, if $\mathbf{\Gamma}(\theta)$ and $\mathbf{\Gamma}(-\theta)$ were used respectively for the negative and positive sequences, direct and quadrature components rotating at twice the fundamental frequency would be obtained instead of constant ones. This is exactly the case of the PLL in Fig. A.1, since the set of voltages v_a, v_b, and v_c is generally unbalanced and therefore includes both positive and negative sequences (see Eq. (A.3)). For instance, when $\mathbf{\Gamma}(\theta)$ is applied to this set, two pair of outputs are obtained. The first pair comprises the voltages v_d^p and v_q^p, which are constant if frame synchronization is attained. The second pair, which is undesired, is given by the voltages v_d^n and v_q^n rotating at twice the fundamental frequency.[6] Analogous conclusions hold when $\mathbf{\Gamma}(-\theta)$ is applied. To eliminate these unwanted terms, notch filters are adopted. Their transfer function $F_{\mathrm{nf}}(s)$ is

$$F_{\mathrm{nf}}(s) = \frac{s^2 + \omega_c^2}{s^2 + \frac{\omega_c}{Q_f} s + \omega_c^2}, \tag{A.13}$$

where ω_c and Q_f are respectively the natural resonant frequency and the quality factor of the filter. $F_{\mathrm{nf}}(s)$ is such that it attenuates the frequency components of the input signal centred around ω_c and spanning a frequency interval whose width is inversely proportional to Q_f. In the case of the PLL presented here, ω_c is twice the nominal angular frequency of the system, while the value of Q_f is selected to cope with slight frequency deviations due to power mismatches. Contrary to Fig. 1.11, in Fig. A.1 the PI regulator is replaced with a transfer function $H(s)$, which is designed to adequately attenuate the error ε at twice the nominal frequency and, thus, eliminate distortions in θ [151].

The variables v_d^p, v_q^p, v_d^n, and v_q^n are used for control purposes in the

[6] Zero sequence or homopolar components are not considered as outputs.

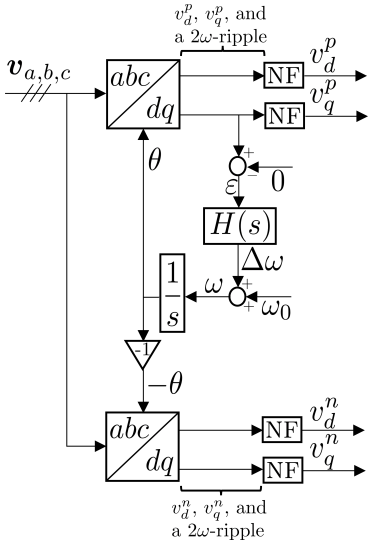


Figure A.1: *The schematic of a* PLL *used in unbalanced operating conditions. The label "*NF*" stands for notch filter.*

upper level controls. An analogous structure to that shown in Fig. A.1 is used to derive the terms i_d^p, i_q^p, i_d^n, and i_q^n from the line currents i_a, i_b, and i_c.

A.3 Upper level controls in unbalanced operating conditions

The upper level controls proposed in this section, based on [65, 151, 187] and illustrated in Fig. A.2, rely on a *double synchronous reference frame* [187]. The first frame - associated with the positive sequence and, thus, balanced operating conditions - is entrusted with the same controls (i.e., P, Q, $v_{\rm ac}$, and $v_{\rm dc}$ regulations) shown in Fig. 1.12. On the contrary, the second frame, related to the negative sequence, fulfils other desiderata that become relevant when unbalances arise.

As already stated, the d, q components associated with the negative sequence are absent during balanced operating conditions. If so, assuming steady-state and that $v_q^p = 0$ due to the presence of the PLL, the active and reactive power formulas in Eq. (A.12) become analogous to those obtained in Section 1.3.3 (i.e., $P = P_k = v_d^p i_d^p$ and $Q = Q_k = -v_d^p i_q^p$). Assuming once again an almost infinitely stiff AC grid, the voltage v_d^p is fairly constant. Therefore, the only variables that can be regulated for active and reactive power control are the i_d^p and i_q^p currents at the AC-side terminals of the converter. Similarly, the same variables could be used to control the DC

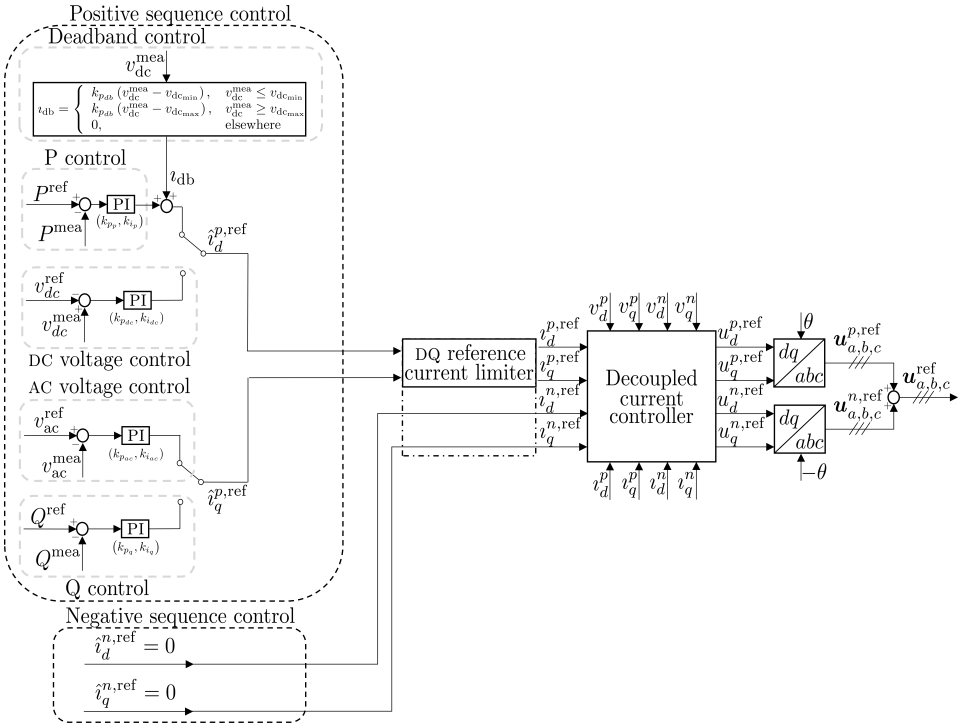


Figure A.2: *The schematic of the upper level controls in unbalanced operating conditions. Other control functions, such as frequency control, $P - v_{dc}$ and $Q - v_{ac}$ droop regulations have been omitted.*

and AC-side voltages, respectively.

In case of unbalances, the d, q components associated with the negative sequence are different from zero. Analogously to the positive sequence, the variables controlled in the negative sequence reference frame are the currents $\imath_d^n$ and $\imath_q^n$. Contrary to their positive sequence counterparts, these variables are regulated for other purposes. Two possible control strategies (analysed in [151, 187]), are briefly summarised hereafter.

The simplest one, adopted in this thesis, suppresses negative sequence currents and imposes $\hat{\imath}_d^{n,\text{ref}} = \hat{\imath}_q^{n,\text{ref}} = 0$. This implies that, if unbalances occur on the AC-side of the MMC, the control aims at ensuring that the line currents $\imath_a$, $\imath_b$, $\imath_c$ remain balanced. The advantage in doing so is that fault current stresses on the converter switches are reduced [151]. Indeed, if no countermeasure were adopted, the line current in the faulted phases would be higher than that of the healthy phases. Thus, current stresses would be

unevenly distributed among the three phases.[7] In addition, since at steady-state $\imath_d^n = \imath_q^n = 0$, another consequence of this control strategy is that the steady-state expressions of P_k and Q_k remain unchanged (i.e., $P_k = v_d^p \imath_d^p$ and $Q_k = -v_d^p \imath_q^p$). However, this does not prevent the emergence of the power terms P_{c_2}, P_{s_2}, Q_{c_2}, and Q_{s_2} in Eq. (A.12). These terms result in active and reactive power fluctuations. In turn, as stated in [151], higher DC-side voltage ripples are incurred.[8]

To address this issue, another possibility could be to control $\imath_d^n$ and $\imath_q^n$ to let $P_{c_2} = P_{s_2} = 0$ and also reduce DC-side voltage ripples. The works in [151, 187] analyzed this strategy. Albeit successful in meeting the above targets, this control leads to unbalanced line currents and, thus, unevenly distributed current stresses among the phases.

Other negative sequence current control strategies are described in [187]. In any case, regardless of the strategy considered, none of them is flawless. Besides, the degrees of freedom in the control scheme (i.e., $\imath_d^n$ and $\imath_q^n$) is lower than the number of possible control objectives. Therefore, no solution fits all the requirements.

Another advantage of resorting to a negative sequence current control such that $\hat{\imath}_d^{n,\mathrm{ref}} = \hat{\imath}_q^{n,\mathrm{ref}} = 0$ is that the same reference current limiter shown in Fig. 1.13 can be adopted. Indeed, in this case only $\hat{\imath}_d^{p,\mathrm{ref}}$ and $\hat{\imath}_q^{p,\mathrm{ref}}$ might need to be limited, since $\hat{\imath}_d^{n,\mathrm{ref}} = \hat{\imath}_q^{n,\mathrm{ref}} = \imath_d^{n,\mathrm{ref}} = \imath_q^{n,\mathrm{ref}} = 0$. On the contrary, if other negative sequence control strategies were adopted, $\hat{\imath}_d^{n,\mathrm{ref}}$ and $\hat{\imath}_q^{n,\mathrm{ref}}$ may be different from zero. Therefore, the reference current limiter scheme would need to be changed and accept also them as inputs (as succinctly sketched in the dashed box around the *reference current limiter block* in Fig. A.2). However, this would require the adoption of more advanced reference current limiters. The interested reader can refer to [188, 189] for some implementation examples.

After being (possibly) limited, the reference currents $\imath_d^{p,\mathrm{ref}}$, $\imath_q^{p,\mathrm{ref}}$, $\imath_d^{n,\mathrm{ref}}$, and $\imath_q^{n,\mathrm{ref}}$ - together with the d, q positive and negative sequence components of the grid voltages and currents - constitute the inputs of the *decoupled current controller* depicted in Fig. A.3(b). To explain its operating principle, an analogous approach to that described when deriving Eqs. (1.12) and (1.16) is followed. Since the only difference lies in the formula of the space phasor (compare Eqs. (1.6) and (A.7)), the following paragraphs do not dwell

[7] The interested reader can refer to Figs. 6(a) and 7(a) of [151], which respectively show the line currents of a converter after a single-line to ground fault without and with the negative sequence current suppression scheme.

[8] This is because active power is exchanged with the DC-side of the MMC and determines the DC-side voltage level. As a consequence, if the active power contains a 2ω ripple, so does the DC-side voltage. These ripples can be minimised by nullifying P_{c_2} and P_{s_2}.

on the details to avoid excessive repetitions. Starting from Eq. (1.13), the space phasor $\bar{v}$ of the grid voltage can be defined (and gradually recast) as

$$\bar{v} = -\left(R_T + \frac{R_S}{2}\right)\bar{\imath} - \left(L_T + \frac{L_S}{2}\right)\frac{d\bar{\imath}}{dt} + \bar{u_k}$$

$$\begin{aligned}\left(v_d^p + \mathbb{j}v_q^p\right)e^{\mathbb{j}\theta} + \left(v_d^n + \mathbb{j}v_q^n\right)e^{-\mathbb{j}\theta} = \left(u_d^p + \mathbb{j}u_q^p\right)e^{\mathbb{j}\theta} + \left(u_d^n + \mathbb{j}u_q^n\right)e^{-\mathbb{j}\theta} + \\ - \left(R_T + \frac{R_S}{2}\right)\left[\left(\imath_d^p + \mathbb{j}\imath_q^p\right)e^{\mathbb{j}\theta} + \left(\imath_d^n + \mathbb{j}\imath_q^n\right)e^{-\mathbb{j}\theta}\right] + \\ - \left(L_T + \frac{L_S}{2}\right)\frac{d}{dt}\left[\left(\imath_d^p + \mathbb{j}\imath_q^p\right)e^{\mathbb{j}\theta} + \left(\imath_d^n + \mathbb{j}\imath_q^n\right)e^{-\mathbb{j}\theta}\right]\end{aligned} \tag{A.14}$$

$$\begin{aligned}\left(v_d^p + \mathbb{j}v_q^p\right)e^{\mathbb{j}\theta} + \left(v_d^n + \mathbb{j}v_q^n\right)e^{-\mathbb{j}\theta} = \left(u_d^p + \mathbb{j}u_q^p\right)e^{\mathbb{j}\theta} + \left(u_d^n + \mathbb{j}u_q^n\right)e^{-\mathbb{j}\theta} + \\ - \left(R_T + \frac{R_S}{2}\right)\left[\left(\imath_d^p + \mathbb{j}\imath_q^p\right)e^{\mathbb{j}\theta} + \left(\imath_d^n + \mathbb{j}\imath_q^n\right)e^{-\mathbb{j}\theta}\right] + \\ -\mathbb{j}\omega\left(L_T + \frac{L_S}{2}\right)\left(\imath_d^p + \mathbb{j}\imath_q^p\right)e^{\mathbb{j}\theta} + \mathbb{j}\omega\left(L_T + \frac{L_S}{2}\right)\left(\imath_d^n + \mathbb{j}\imath_q^n\right)e^{-\mathbb{j}\theta} + \\ - \left(L_T + \frac{L_S}{2}\right)\frac{d}{dt}\left(\imath_d^p + \mathbb{j}\imath_q^p\right)e^{\mathbb{j}\theta} - \left(L_T + \frac{L_S}{2}\right)\frac{d}{dt}\left(\imath_d^n + \mathbb{j}\imath_q^n\right)e^{-\mathbb{j}\theta}\end{aligned}$$

By analysing separately the real and imaginary part of Eq. (A.14), the system of equations reported in Eq. (A.15) can be obtained.

$$\begin{cases} v_d^p = u_d^p - \left(R_T + \frac{R_S}{2}\right)\imath_d^p - \omega\left(L_T + \frac{L_T}{2}\right)\frac{d\imath_d^p}{dt} + \omega\left(L_T + \frac{L_T}{2}\right)\imath_q^p \\ v_q^p = u_q^p - \left(R_T + \frac{R_S}{2}\right)\imath_q^p - \omega\left(L_T + \frac{L_T}{2}\right)\frac{d\imath_q^p}{dt} - \omega\left(L_T + \frac{L_T}{2}\right)\imath_d^p \\ v_d^n = u_d^n - \left(R_T + \frac{R_S}{2}\right)\imath_d^n - \omega\left(L_T + \frac{L_T}{2}\right)\frac{d\imath_d^n}{dt} - \omega\left(L_T + \frac{L_T}{2}\right)\imath_q^n \\ v_q^n = u_q^n - \left(R_T + \frac{R_S}{2}\right)\imath_q^n - \omega\left(L_T + \frac{L_T}{2}\right)\frac{d\imath_q^n}{dt} + \omega\left(L_T + \frac{L_T}{2}\right)\imath_d^n \end{cases} \tag{A.15}$$

By applying a Laplace transformation, the equations in Eq. (A.16) can be obtained. Such equations give shape to the diagram block shown in Fig. 1.14(a), which depicts the physical relationship between the converter voltage and its output current in the positive and negative sequence. The *decoupled current control* in Fig. A.3(b) follows an analogous approach to derive $u_d^{p,\mathrm{ref}}$, $u_q^{p,\mathrm{ref}}$, $u_d^{n,\mathrm{ref}}$, and $u_q^{n,\mathrm{ref}}$. As illustrated in Fig. A.2, these components are converted back to the ABC-frame through two inverse Park transformations and then summed up.

$$\begin{cases} v_d^p = u_d^p - \left[R_T + \frac{R_S}{2} + s\left(L_T + \frac{L_S}{2}\right)\right] \imath_d^p + \omega\left(L_T + \frac{L_S}{2}\right) \imath_q^p \\ v_q^p = u_q^p - \left[R_T + \frac{R_S}{2} + s\left(L_T + \frac{L_S}{2}\right)\right] \imath_q^p - \omega\left(L_T + \frac{L_S}{2}\right) \imath_d^p \\ v_d^n = u_d^n - \left[R_T + \frac{R_S}{2} + s\left(L_T + \frac{L_S}{2}\right)\right] \imath_d^n - \omega\left(L_T + \frac{L_S}{2}\right) \imath_q^n \\ v_q^n = u_q^n - \left[R_T + \frac{R_S}{2} + s\left(L_T + \frac{L_S}{2}\right)\right] \imath_q^n + \omega\left(L_T + \frac{L_S}{2}\right) \imath_d^n \end{cases} \tag{A.16}$$

It is worth pointing out that zero sequence (and, by extension, homopolar) components are disregarded in the presented MMC control strategy [57, 151]. For instance, the zero sequence current $\imath^0$ is not regulated in the *upper level controls*. As stated in [61], the control of $\imath^0$ can be in general avoided by connecting the AC-side of the MMC to the secondary winding of a Y_g/Δ transformer, as shown in Fig. 1.8. Since in the delta (Δ) windings no path to ground is available for the currents, the three-phase line currents are such that $\imath_a + \imath_b + \imath_c = 0$. According to Eq. (A.2), this implies that $\imath^0$ is null (i.e., the zero sequence current is blocked). However, note that this holds assuming that unbalanced faults occur only in the Y-side of the grid. Otherwise, $\imath^0$ would be inevitably different from zero, thereby requiring an *ad-hoc* control scheme that involves the zero sequence of the voltage u^0. For the sake of simplicity, the assumption above is always respected in the faults simulated in Chapter 3.2.

A.4 Circulating current suppression control in unbalanced operating conditions

As stated at the beginning of this appendix, the only *lower level control* that needs to be changed to make the control strategy compatible with unbalanced operating conditions is the *circulating current suppression control*. As demonstrated in [64], in balanced operating conditions, the circulating currents $\imath_{circ}$ flowing through the three phases of the converter have a main negative sequence component rotating at twice the fundamental frequency 2ω, suppressed by the scheme in Fig. 1.15. However, when unbalances occur, [190] shows that $\imath_{circ}$ also includes significant positive and zero sequence components rotating at 2ω.

In the light of the above, the *circulating current suppression control* needs to be modified. The most straightforward way to do so would be to replicate the control structure shown in Fig. 1.15 so that also the positive and zero sequences of $\imath_{circ}$ rotating at 2ω are suppressed. However, this would result in an excessively complex control scheme, characterised by an increased number of PI regulators and direct and inverse Park transfor-

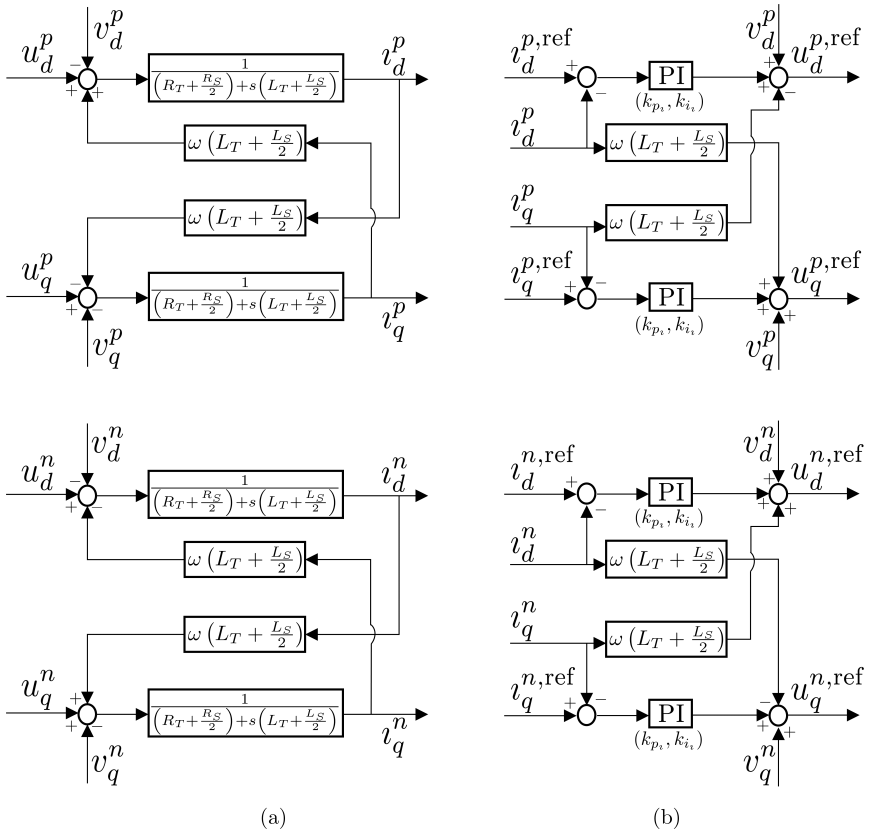


Figure A.3: *Diagram block depicting the physical relationships among the d, q components of the positive and negative sequences of the converter voltages and currents (a) and the decoupled current control of the* MMC *in unbalanced operating conditions (b).*

mations. In this work, a different control scheme, based on [190, 191] and shown in Fig. A.4, is adopted.[9]

The operating principle of this circulating current suppression strategy can be described as follows. The current $\imath_{z_k} = \frac{1}{2}\left(\imath_{u_a} + \imath_{l_k}\right)$ (recall that $k \in \{a, b, c\}$) is compared with $\frac{\imath_{\mathrm{dc}}}{3}$. As can be inferred from Eq. (1.21), any difference between the two terms is associated with the circulating current $\imath_{circ_k}$ and constitutes the input of a non-ideal proportional-resonant filter, labelled as "PR" in Fig. A.4. Its transfer function is

[9]The interested reader is invited to read [56] for an extensive review of other methods for circulating current control in unbalanced operating conditions.

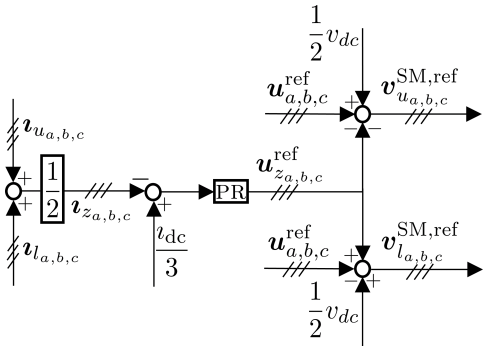


Figure A.4: *The* MMC *circulating current suppression control used for unbalanced operating conditions. The label "*PR*" stands for proportional-resonant filter.*

$$F_{\text{pr}}(s) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega_r^2}, \tag{A.17}$$

where k_p , k_r , ω_r , and ω_c are respectively the proportional gain, resonant gain, resonant frequency, and cut-off frequency of the filter. Around ω_r, the filter provides a high gain which largely depends on k_r. On the contrary, the proportional gain k_p results in a vertical shift in the Bode plot of the magnitude of $F_{\text{pr}}(s)$ for every frequency value. In this thesis, the resonant frequency of the filter amounts to $\omega_r = 2\omega_0$, with ω_0 being the nominal frequency of the grid. By doing so, the main component of $\imath_{circ}$ (i.e., that rotating at twice the angular frequency) can be successfully tracked and suppressed. The tuning of the cut-off frequency ω_c stems from a compromise between the tracking error of the input signal and the filter sensitivity to frequency deviations. Indeed, the higher ω_c, the wider the frequency interval around ω_r characterised by a high gain. On the one hand, this might lead to other frequency components of $\imath_{circ}$ than ω_r from being amplified and regulated. On the other hand, it might still allow tracking the input signal despite slight frequency variations, due to which circulating currents would rotate at a frequency different from $2\omega_0 = \omega_r$.

The filters provide as output a reference voltage $\boldsymbol{u}^{\text{ref}}_{z_{a,b,c}}$. Analogously to Fig. 1.15 and based on Eq. (1.23), these values are combined with the voltages $\boldsymbol{u}^{\text{ref}}_{a,b,c}$ and $\frac{1}{2}v_{\text{dc}}$ to obtain $\boldsymbol{v}^{\text{SM,ref}}_{u_{a,b,c}}$ and $\boldsymbol{v}^{\text{SM,ref}}_{l_{a,b,c}}$.

One of the key features of this control strategy is its compactness. Indeed, it suppresses circulating currents by exploiting just one non-ideal proportional-resonant filter for each phase, without requiring any direct and inverse Park transformation.

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