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POWER SEQUENCING APPROACH TO FAULT ISOLATION IN MVDC SYSTEMS

Tesi di Laurea Specialistica di:

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Master of Science in Electrical Engineering

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Master Graduation Thesis by:

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Abstract

Protection of multi-branch Medium-Voltage DC distribution systems is one of the biggest challenges in the development of this kind of system, especially regarding interruption of high DC currents during ground faults. The strong influence of components of the system on fault behavior is part of this challenge.

The move toward DC power distribution for many power applications (electric ships, offshore wind farms, power in underground cable in-feeds of city centers or industrial systems, ...) makes facing these problems a necessity.

We show that medium-voltage DC power buses can be protected against short circuit faults by coordinating the action of a converter that supplies power to the bus with the action of contactors that are used to reconfigure the bus connections. Following a fault, the bus is de-energized (rather than attempting to interrupt a large fault current), one or more contactors are reconfigured, and the DC bus is then reenergized. For a typical industrial DC bus, we show that it is possible to execute this de-energize-reconfigure-re-energize process 10 times faster than a traditional AC bus can be protected and reconfigured.

We show how the de-energizing and reconfiguration times depend: on characteristics of the DC bus; on short circuit fault conditions; on the distance to the fault; on the output capacitance and inductance of the main converter. We also show how to size each hold-up capacitance so as to permit unfaulted circuits to ride through the process uninterrupted.

Our results provide essential guidelines for design of fault protection for DC power systems using power sequencing and they illustrate how to achieve specified reaction times of the protection scheme.

Sommario

L’aumento di prestazioni e di efficienza, e la diminuzione dei costi dei convertitori ha spinto la riscoperta e la diffusione dei sistemi di distribuzione in corrente continua. Mentre la distribuzione di energia in corrente continua in bassa tensione sta diventando sempre più comune per centri di telecomunicazione e centri di dati, lo sviluppo di sistemi di distribuzione DC in media tensione è parzialmente ostacolato dalla mancanza di opportune strategie e attrezzature per la protezione di questi circuiti. Infatti, la protezione contro guasti a terra e da corto circuito in sistemi di distribuzione DC in media tensione è generalmente percepita come un’importante sfida in quanto comporta l’interruzione di grandi correnti continue. In questa tesi, si mostra come sia possibile controllare i convertitori per attuare una strategia di protezione del sistema DC in modo che non sia necessario impiegare apparecchiature per la protezione dai guasti utilizzate tradizionalmente, quali gli interruttori. Questo consente di eliminare i vari problemi legati all’estinzione di archi elettrici per il mancato passaggio periodico dallo zero della corrente continua.

L’approccio proposto fa affidamento su una sequenza di controllo e sulla riconfigurazione della rete di distribuzione DC. Questo studio è stato applicato nell’ambito della progettazione di una rete di distribuzione in corrente continua per navi militari americane.

Il sistema studiato è articolato nel seguente modo:

Il convertitore DC/DC principale (Main converter) alimenta un bus di distribuzione DC composto da più rami. I contattori SW1, SW2, e SW3 possono essere chiusi per fornire potenza ai vari rami o possono essere aperti per isolare i singoli rami, ma non sono in grado di interrompere correnti di guasto. Quando avviene un guasto a terra o di linea, i carichi sui rami sani sono isolati per mezzo di un diodo in ingresso e sono in

grado di assorbire energia dai condensatori di sostenimento ($C_{hold\text{-}up}$). Per cui i convertitori dei rami sani sono in grado di fornire energia al loro carico per un tempo dipendente dalla taglia dei condensatori di sostenimento. Nel processo sono coinvolti i seguenti elementi: Il controllo del convertitore, il condensatore in uscita (C_{out}) e l'induttanza (L_{out}) del convertitore principale, i diodi in ingresso, i condensatori a valle e i contattori di ogni ramo. In Figura A è mostrato lo schema adottato nelle simulazioni.

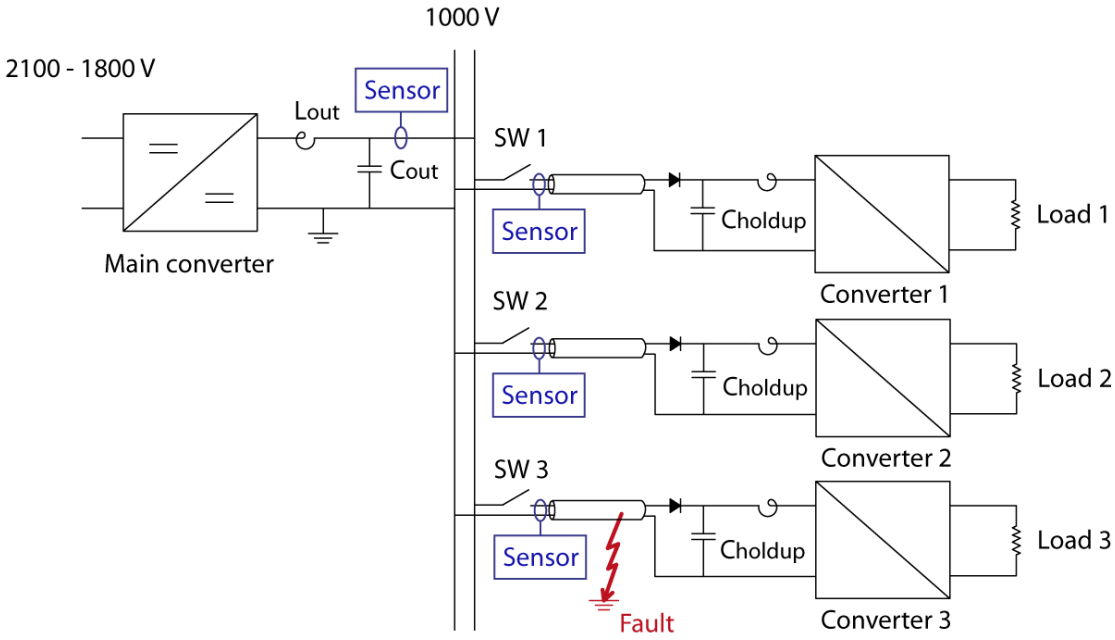

Figura A - Schema del bus DC utilizzato

Nel momento in cui viene individuato un guasto, il bus DC viene de-energizzato spegnendo il convertitore principale che alimenta il bus o controllando il suo duty-cycle. In seguito uno o più contattori vengono aperti per riconfigurare la rete e il bus DC può essere rienergizzato riattivando il convertitore principale. Questo sistema di protezione, in grado di agire in pochi millisecondi, consente l'isolamento del ramo guasto e la rialimentazione dell'intero bus in modo che i rami sani non si accorgano che il bus principale è stato disalimentato e riconfigurato. In Figura B è mostrato il funzionamento della sequenza di controllo.

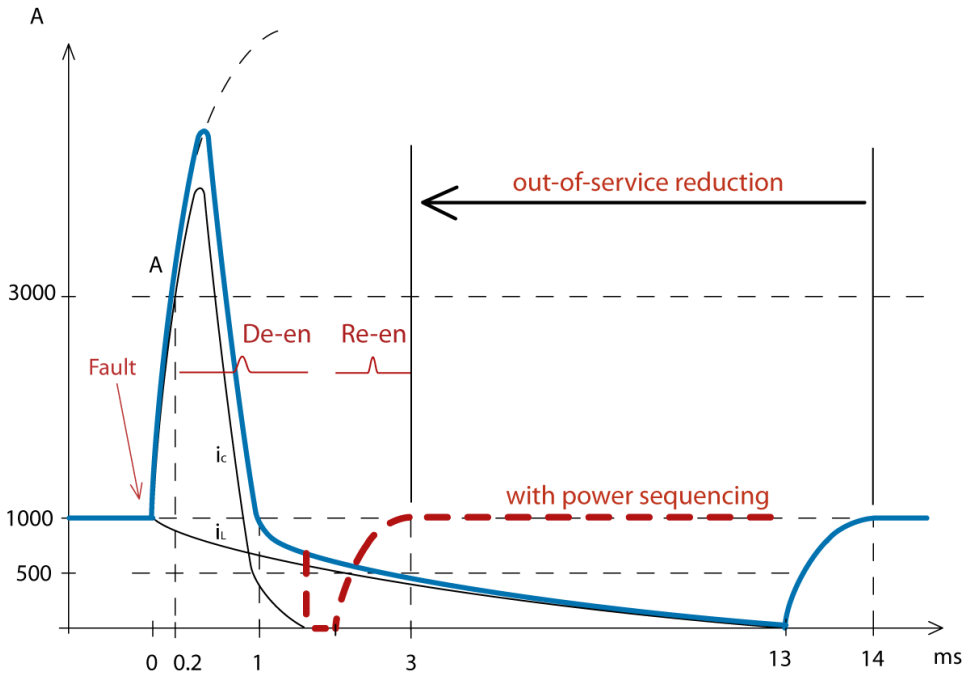

Figura B - Comportamento del sistema quando la sequenza di controllo interviene

Questa tesi ha l'obiettivo di fornire i seguenti contributi:

Prima di tutto, una profonda analisi del sistema mostra il comportamento del bus DC al presentarsi di un guasto a terra o di linea. Questo consente di capire come i transitori del guasto dipendono dalle caratteristiche del bus, dalle sorgenti e dai carichi connessi.

In secondo luogo, viene mostrato come operano la strategia di protezione introdotta e i componenti che prendono parte al processo.

Terzo: la sequenza di controllo utilizzata per risolvere i guasti è fortemente influenzata dai parametri di sistema. Perciò, viene illustrato come ottenere specifici tempi di reazione dello schema di protezione e per quale intervallo di variazione dei parametri si è in grado di ottenere le migliori prestazioni.

Infine, i risultati forniscono linee guida per la progettazione di protezioni contro guasti per sistemi elettrici in corrente continua utilizzando la sequenza di controllo presentata.

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Introduction

The increased performance, higher efficiency, and decreased cost of power electronic converters have spurred a rediscovery and proliferation of DC distribution systems.

DC power distribution at the low voltage level is becoming common for data centers [1]. Less common are DC distribution systems at the medium voltage level, and these are partially hindered by lack of appropriate circuit protection strategies and equipment [2]-[4]. In fact, protection of medium voltage DC distribution systems against short circuit faults is widely perceived to be a significant challenge because it can entail interrupting of large DC currents [5].

In this thesis, we show how electronic power converters can be controlled to effect the circuit protection strategy so that traditional circuit protection elements are not needed. Thus we avoid the widely cited problem of arc extinction in the absence of periodic zero crossings of the current.

Although many techniques have been proposed to induce an oscillating current zero, and thereby to allow physical interruption of DC currents using apparatus similar to AC circuit breakers, these approaches introduce additional complexity [6] and are not as effective at rapid limiting of fault currents. Expensive, fast-acting, solid state circuit breakers [7] can more quickly interrupt fault currents, but even these may be unnecessary considering new approaches that rely on controlling the converter duty cycle [8] to limit and quench fault currents, and this is our focus.

Our new approach relies on a controlled sequencing of power conversion and network configuration. When a fault is detected the bus is de-energized by turning off the main converter, one or more contactors are reconfigured, and the DC bus is reenergized. A

protection system acting within a few milliseconds allows the isolation of the faulty branch and the re-energizing of the entire bus such that the healthy branches are not aware that the main bus has been brought down and reconfigured [9]. Figure 1 shows how the controlled power sequencing works.

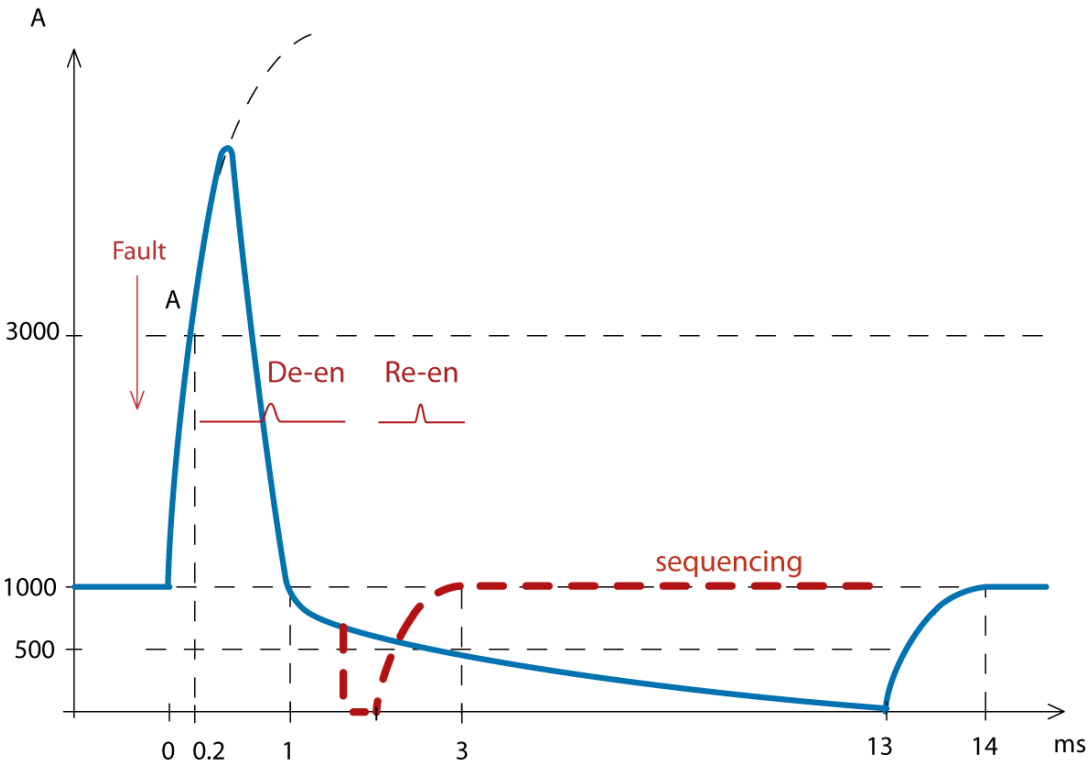

Figure 1 - System behavior when the power sequencing is acting

Figure 2 shows the scheme that has been explored in simulations. A main DC/DC converter supplies power to a DC distribution bus that supplies many branch circuits. The switches SW1, SW2, and SW3 can be closed to supply power to the branch circuits, or they can be opened to isolate a branch circuit, but they are not capable of interrupting fault currents. When a fault happens, the loads on healthy lines are isolated by the input diodes while they draw power from the hold-up capacitors. Therefore, healthy load converters on healthy lines are able to supply power to each load for a time depending on the size of the hold-up capacitors. The converter control,

the output capacitor (C_{OUT}) and inductance (L_{OUT}) of the main converter, input diodes, downstream input capacitors and branch switches are all involved in this process.

Chapter one discusses challenges and opportunities of using DC systems and approaches to face fault isolation. Chapter two illustrates a new approach for protection against fault in DC and the description of the system utilized in our study.

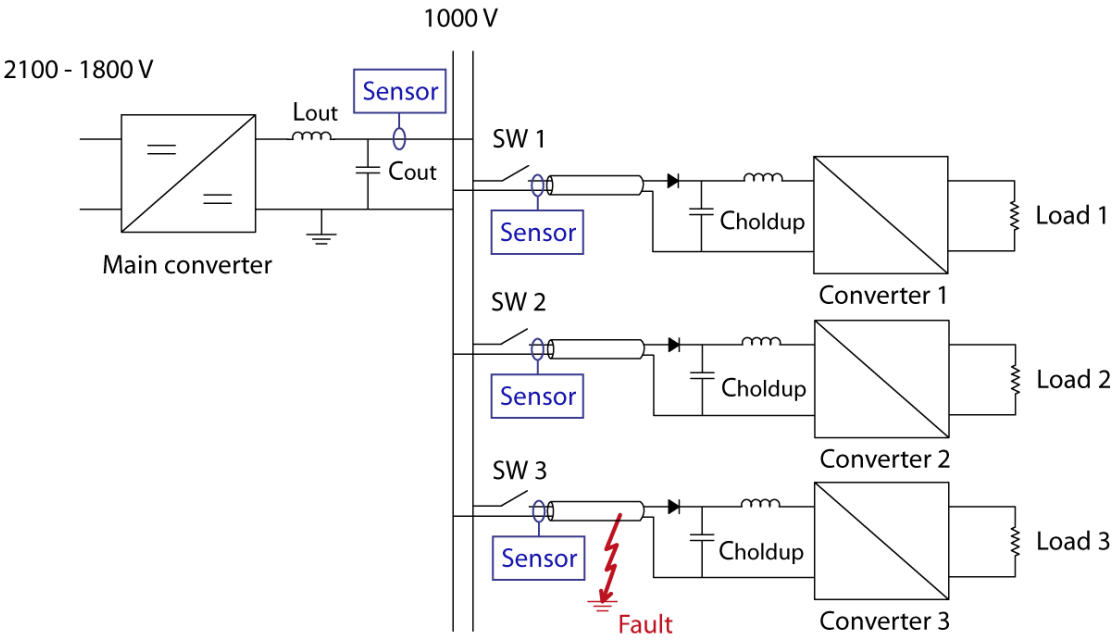

Figure 2 – Scheme of the DC bus used

In chapter three, we analyze dynamics of short circuit and ground faults on a DC bus. Chapter four shows how the introduced approach works, and analyzes the influence of system components on the protection system and its performances. Chapter five gives important considerations on contactors for the reconfiguration after a fault and hold-up capacitors.

This thesis attempts to make the following contributions:

First of all, a deep analysis of the system shows the system behavior when a short circuit fault happens. That allows us to understand how transients depend on the DC bus characteristics, and on sources and loads connected.

Secondly, we show how the introduced approach operates, and the components that take part in the process.

Thirdly, the controlled power sequencing is strongly affected from the system parameters. Therefore, we illustrate how to achieve specified reaction times of the protection scheme, and for which range of parameters we are able to obtain the best performances.

Finally, our results provide essential guidelines for design of fault protection for DC power systems using the presented power sequencing.

1. DC systems: Challenges and Opportunities

For many years power distribution focused the attention far away from direct current. In fact, the impossibility to easily step up and down the voltage caused the abandonment of DC distribution for the most of applications. With the advent of power electronic and a strong improvement of semiconductor devices, direct current is becoming interesting for a lot of electrical applications in each voltage level. That is because DC has advantages in term of efficiency, reliability, stability, and active power control. Despite many advantages, DC distribution systems are not widely accepted because of the lack of proper protections. This thesis offers a solution for protecting DC systems against ground and line faults.

1.1 Historical reasons for the abandonment of DC distribution systems

With the advent of Alternating Current power in 1887, direct current became less and less used. Direct current could not easily be changed to higher or lower voltages. This meant that separate electrical lines had to be installed in order to supply power to appliances that used different voltages. When Tesla introduced a system for alternating current generators, transformers, motors, wires, and lights, AC became the new standard for electric power distribution. That is because alternating current could be transmitted over long distances at high voltages, at lower current for lower voltage drops, and then conveniently stepped down to low voltages for use in homes and factories. The possibility to easily change the voltage level made AC systems successful [10]-[11].

The discovery of new technologies in the field of power electronic has introduced new semiconductor based components (e.g. diodes, thyristors, …) that allows

converters to completely manage the direct current. Power electronic converters composed by these semiconductor components enable to easily step up and down the voltage.

The increased performance, higher efficiency, and decreased cost of power electronic converters have spurred a rediscovery and proliferation of DC distribution systems for many electrical applications.

1.2 DC is returning for several power applications

Low Voltage and Medium Voltage DC distribution is receiving more attention after the development of Voltage Source Converters (VSC) and successful implementation of the VSC based Multi-Terminal HVDC system [12]. Some successful applications are:

1- Optimal acquisition of wind power from offshore wind farms

2- DC transmission in interconnection systems

3- Premium quality power providing in underground cable in-feeds of city centers or industrial systems

Optimal acquisition of power in wind farm requires the speed of each individual turbine-generator to converge to the optimum speed corresponding to the local wind velocity. The DC grid interconnects multiple Voltage Source Converters (VSCs), rectifying the generator powers that come in diverse frequencies and magnitudes to a common DC voltage for their aggregation [13]. Moreover, HVDC transmission systems have a number of advantages for large off shore wind farms, including fully controlled power flow, transmission distance using DC not affected by cable charging currents, and fewer cable required [14]-[15].

The introduction of DC transmission in interconnection systems allows the de-coupling of the Inter-Area System Dynamics. Through de-coupling, any transient disturbance will be restricted to the area of origin. Dynamic controls of DC transmission not only have the capability to de-couple the inter-area modes but also, at the same time, provide damping to local modes within each area [16].

The property of VSC-HVDC to control the active and reactive power independent of each other allows the modulation of both when disturbances occur in the system. Control strategies allow VSC-HVDC to damp power oscillations or enhance the transient stability and provide voltage support at the same time, in an effective and robust way. The voltage-source converter can solve the PQ-related problem due to its ability to mitigate or filter voltage dips from the grid and, at the same time, transferring active power to the customer. This capacity allows DC systems to be used to provide high-quality power to industrial customers or to provide power in underground cable in-feeds of city centers [17].

Another example of employment of DC distribution systems are power delivery architectures for Telco and Data Centers at 400V DC. DC distribution offers higher efficiency by eliminating the inverter (DC/AC conversion stage) in the UPS, the AC/DC converter, as well as the transformer. By decreasing the number of conversion stages the DC configuration is able to improve power delivery efficiency. For data center distribution systems, a 7% input power saving is possible. The power delivery efficiency improvements alone may not justify the change to DC distribution system by itself. However, the combination of high efficiency with the other advantages of 400 Vdc distribution, including higher reliability, simplified implementation due to lack of phasing requirements and harmonic mitigation, and reduced component cost, makes the use of 400Vdc distribution advantageous.

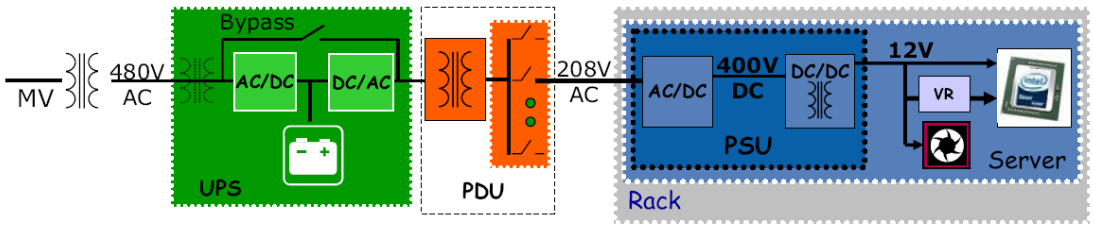

Figure 3 - Conventional 480Vac distribution in the United States

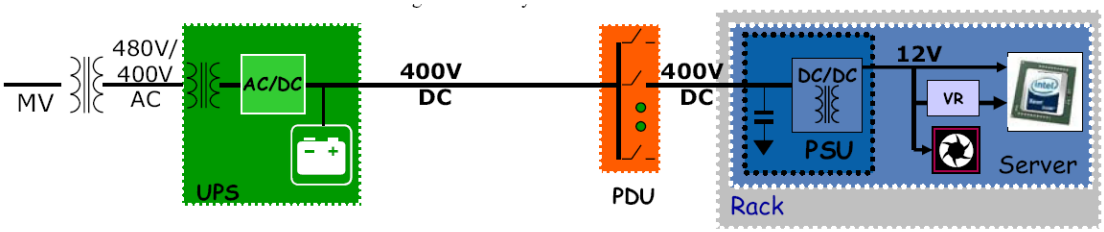

Figure 4 - Facility-level 400Vdc

Figure 3 and Figure 4 show the reduction of stages between an AC power delivery system and a facility level 400V DC power delivery system [1],[18]-[20].

1.2.1 US Navy ZONAL MVDC system for war ships

A multi-zonal MVDC architecture has been identified by the US Navy as one of the possible architectures for the shipboard power distribution [12].

The zonal electrical system architecture eliminates all switchboard feeder cables transitioning watertight bulkheads, except the port and starboard cableways [21].

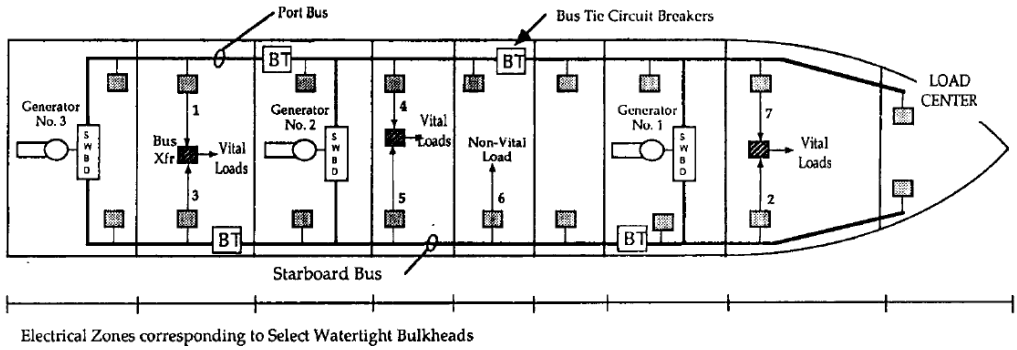

Figure 5 - Zonal electrical distribution system onboard a typical surface combatant

The ever-increasing high-power loads on ships, which need highly reliable and very high-quality power supply, made conventional AC systems very hard to maintain. The

system envisioned by the Navy is illustrated in Figure 6. Two or more generators supply power to the DC distribution bus through power electronic converters, which rectify AC to DC and regulate the DC bus voltage. Lower voltage buses are served through dc-dc converters that isolate the loads in the zone from the rest of the system, and thus, any fault and disturbance within a zone can be confined within that zone. The DC bus also simplifies the cabling for power distribution, as more power can be transferred on a cable with DC than AC [22].

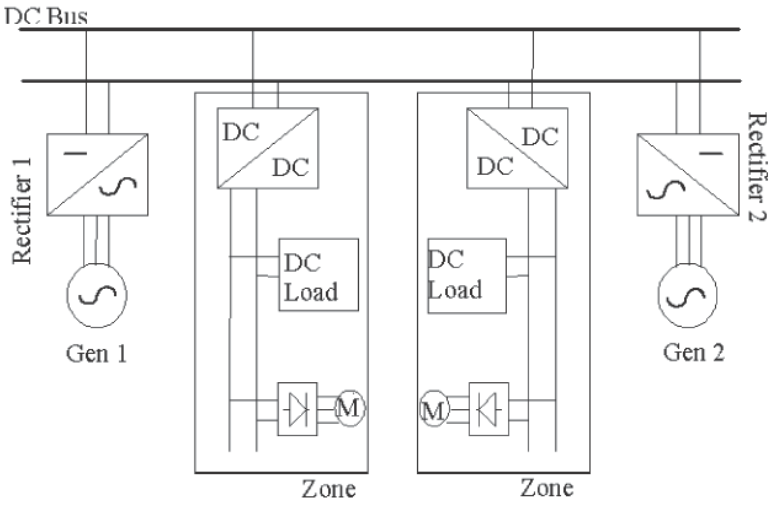

Figure 6 - DC shipboard distribution system

Additional benefits provided by a zonal electrical system architecture include enhancement of ship producibility, ease of future ship modernization, and component commonality with other ship classes.

1.2.2 Advantages and disadvantages of DC systems

As shown in most of the applications mentioned before, DC distribution has many advantages compared with AC distribution.

First of all the enhancement of efficiency and reliability by reducing conversion stages. In fact, DC links allow the employment of energy storage elements without the use of UPS composed by AC/DC converter and inverter. Secondly, DC distribution

does not have problems related to alternating current, such as phasing requirements, frequency synchronization, harmonic mitigation, etc. Thirdly, DC systems have the ability to rapidly control the transmitted active power, and to independently exchange reactive power between transmission systems, and consequently, DC power transmission allows a de-coupling of two interconnected areas. Moreover, DC distribution enhances power transferred on a cable, and decreases the number of conductors.

1.3 Fault protection in DC systems

In spite of many advantages, DC distribution systems are partially hindered by lack of appropriate circuit protection strategies and equipment [2]-[4]. In fact, protection of DC distribution systems against short circuit and ground faults, especially at the Medium-Voltage level, is widely perceived to be a significant challenge because it can entail interrupting of large DC currents [5].

1.3.1 Ground and line fault in DC systems

Direct current presents different problems in comparison to alternate current. That is because of different phenomena associated with the interruption of high currents and the arc extinction. While alternating current has a natural crossing through zero every semi-period, this crossing does not exist for direct current (Figure 7). In AC systems the arc extinction happens when the current crosses zero during the opening of the circuit (Figure 8). In DC circuits, the current has to decrease down to null to guarantee arc extinction (forcing the current passage through zero).

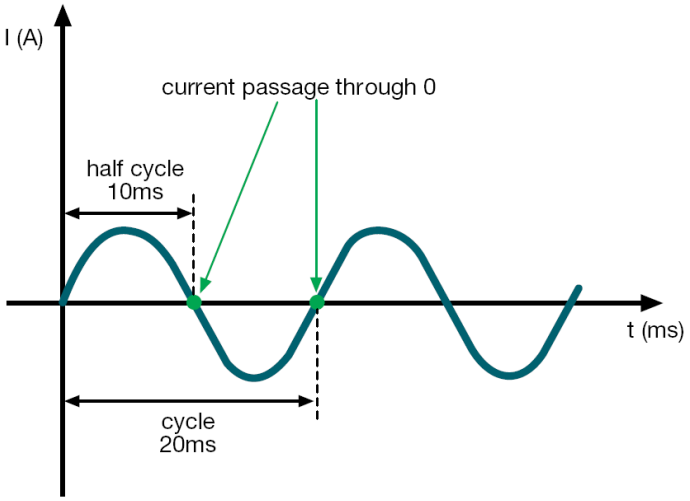

Figure 7 - Point where is possible to extinguish the alternating current

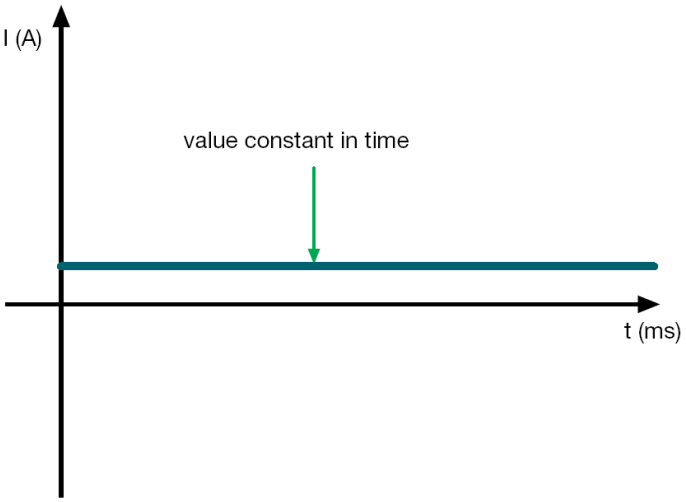

Figure 8 - Non-existence of a natural zero-crossing in the direct current

Figure 9 illustrates a DC circuit that has to be opened by a circuit breaker. The resistance R and the inductance L represent equivalent parameters of the circuit. The following expression describes the voltage balance of the DC circuit: V is the rated voltage of the supply source, i is the current that has to be interrupted, and V_a is the arc voltage.

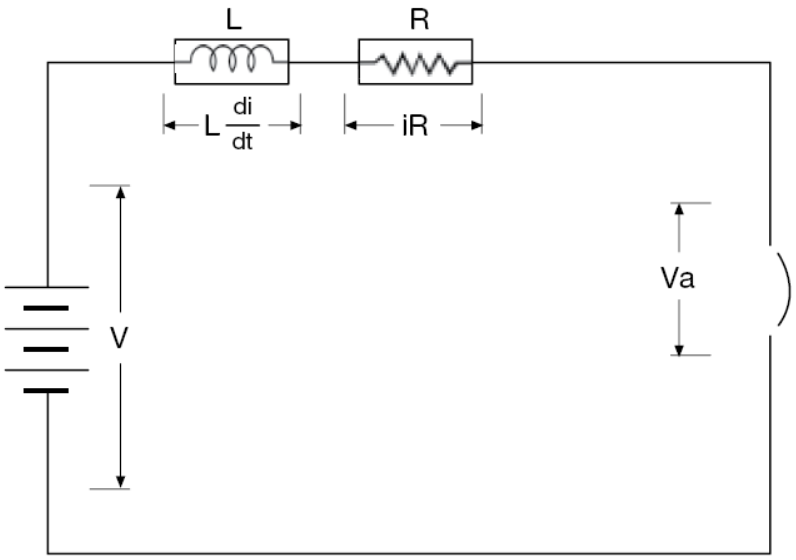

Figure 9 - Equivalent circuit of a DC line

$$V = L\frac{di}{dt} + Ri + V_a \qquad (1)$$

The formula can be written also as:

$$L\frac{di}{dt} = V - Ri - V_a \qquad (2)$$

To guarantee arc extinction, it is necessary that:

$$\frac{di}{dt} < 0 \qquad (3)$$

This relationship shall be verified when the arc voltage (*Va*) is so high that the first part of the formula (2) becomes negative. It is possible to conclude that the extinction time of a direct current is proportional to the time constant of the circuit $\tau = L/R$ and to the extinction constant. The extinction constant is a parameter depending on the arc characteristic and on the circuit supply voltage.

Figure 10 shows an oscillogram of the opening of a short circuit by means of a circuit breaker. *Ip* is the short circuit making current, *Icn* is the prospective short circuit current, *Va* the maximum arc voltage, *Vn* the network voltage, *T* the time constant, t_o

the instant of beginning of short circuit, t_s the instant of beginning of separation of the circuit breaker contacts, t_a the instant of quenching of the fault current.

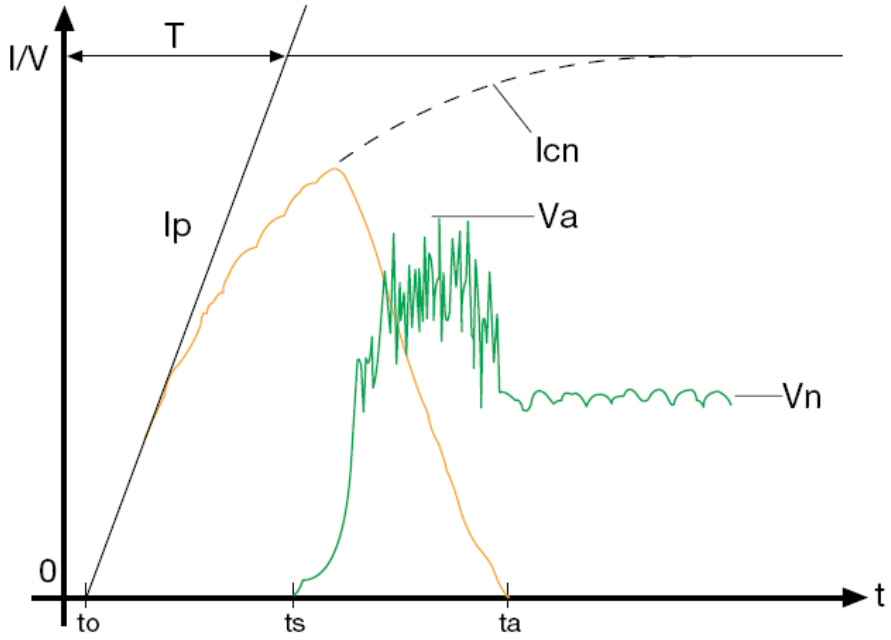

Figure 10 - Oscillogram of the opening of a short circuit with a circuit breaker

When a short-circuit occurs in correspondence to the instant t_o, the current starts rising according t_o the time constant of the circuit. The circuit breaker contacts begin to separate, thus an arc starts from the instant t_s. The current keeps on rising for a short period after the beginning of contacts opening, then decreases depending on the increasing value of the arc resistance progressively introduced in the circuit. As can be seen in the graph, the arc voltage remains higher than the supply voltage of the circuit during the interruption. In correspondence of t_a, the current is completely quenched. As the graph in Figure 10 shows, the short-circuit current represented by the orange line is extinguished without abrupt interruptions which could cause high voltage peaks. As a consequence, to obtain a gradual extinction, it is necessary to cool and extend the arc with arc eliminating equipment, so that increasing arc resistance is inserted in the circuit (with the consequent increase of the arc voltage V_a). This

extinction involves energetic phenomena which depend on the voltage level of the system (V_n) and require circuit breakers to be connected in series to optimize performance during short circuit conditions. The higher the number of contacts opening the circuit, the higher the breaking capacity of the circuit breaker [23].

Thus, one of the solutions to the problem of opening direct currents is the employment of traditional circuit breakers with the addition of specific devices to extinguish arcs. There are many kinds of arc eliminating equipment for circuit breakers. One of the most used is the arc chute that extinguishes the arc by fragmenting it. When contacts of the circuit breaker open, a magnetic device blows the arc through the arc chute, the arc is fragmented in many parts, and is finally extinguished. Figure 11shows an example of DC circuit breaker with arc chute on the top.

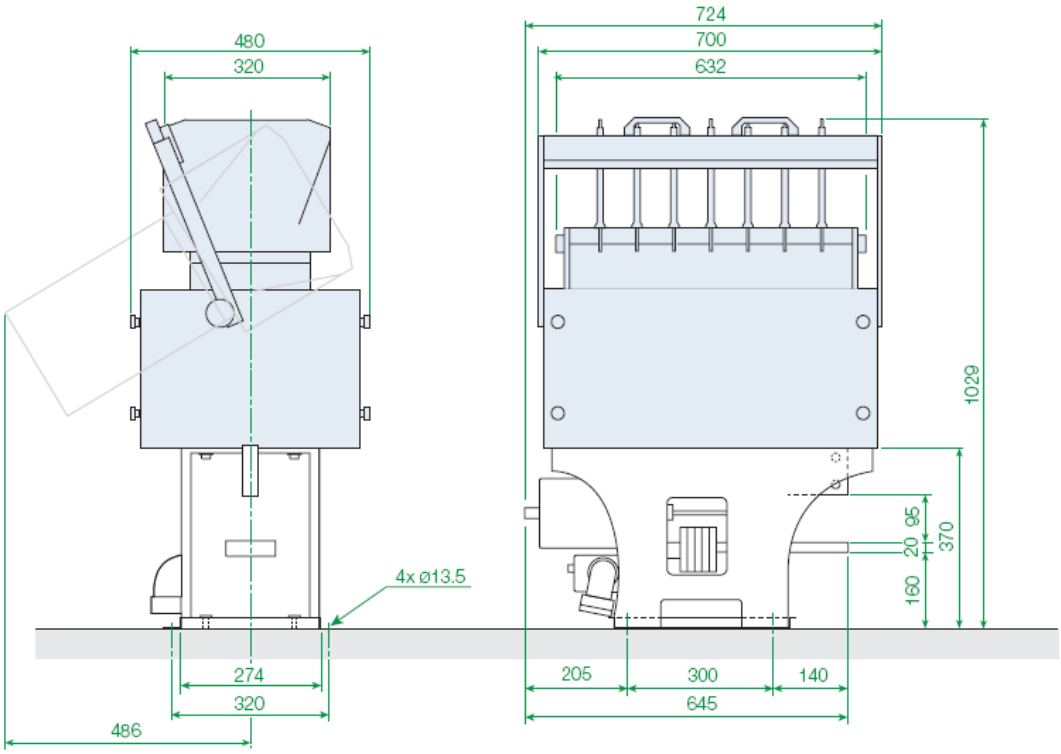

Figure 11 - Example of arc chute over a DC circuit breaker (Grey section)

Figure 12 shows the position of circuit breakers on a DC shipboard electrical system to protect bus and components against faults.

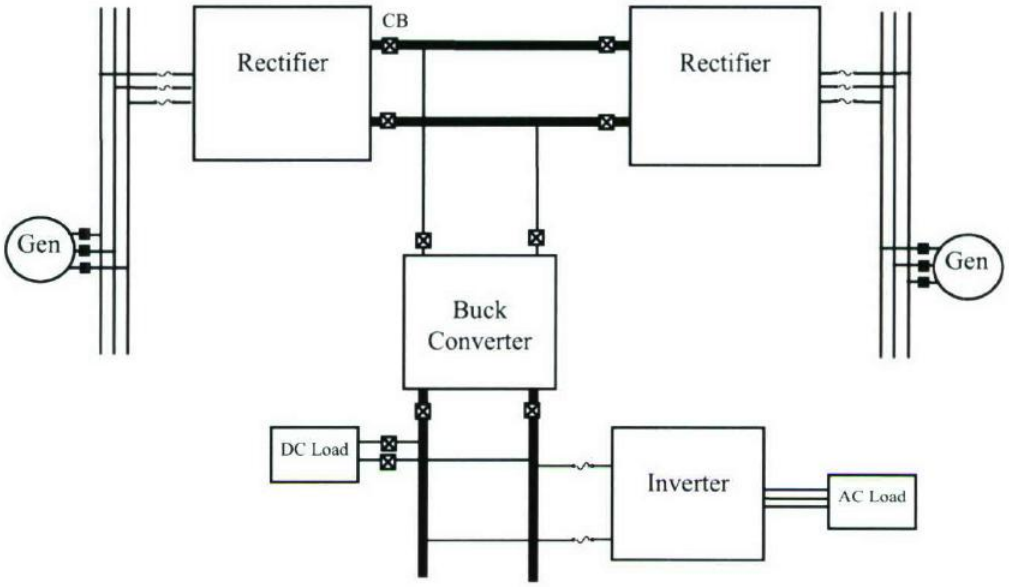

Figure 12 - Circuit breaker needed on a DC shipboard electrical system to protect components against faults

This solution is widely employed in DC systems such as DC electric traction, but circuit breakers and their arc eliminating equipments need a lot of space and weight, and are very expensive.

In the following paragraph, we have shortly analyzed different solutions to solve the fault protection problem without employing circuit breakers.

1.3.2 Approaches for protection against fault in DC distribution systems

Other solutions to solve the protection of DC systems are current oscillating equipments to turn off thyristors of the upstream rectifier, the use of the rectifier as a crowbar in order to open the circuit by means of the AC side circuit breaker, the employment of solid state based circuit breakers, and the use of converters composed by turn-off switches that allow to limit and interrupt the current flow.

Many techniques have been proposed in the literature to induce an oscillating current to lead the current to zero, and thereby interrupt the current. These methods typically

involve opening or closing of selective switches and charging or discharging of capacitors. The main drawback of all such methods is that they involve additional devices in series to the system component that needs to be protected. Also, these devices are slow and bulky and may require extra charging circuits and power supplies [24]-[25].

Currently, commonly used approaches to isolate faults on the DC bus involves the use of VSC as a crowbar. The crowbar shorts the input and thus protects the converter from high currents, and the fault current is then interrupted by the AC circuit breaker on the source side. Despite this is an interesting solution, shorting of the AC side by means of switches of the bridge provides high current stress on switches during the fault. The possibility to use this method only with a converter having an AC side limits this fault protection method.

Another interesting solution is the employment of solid state based circuit breakers (SSCBs). These are composed by a solid state switch, such as an IGBT or IGCT thyristor or ETO thyristor, and a snubber circuit that can be composed by a combination of resistances, capacitors, and metal oxide varistors (MOVs). Thanks to recent developments, SSCBs offer the possibility of interrupting fault currents very fast. A SSCB can be placed at DC terminals of the VSC or on the downstream side of a dc-dc converter to interrupt the fault current as shown in Figure 13, and isolate the fault [24],[26]-[27]. The development of such devices is becoming more and more interesting, but some drawbacks make the employment of SSCB disputable. First of all this kind of circuit breaker is limited by the maximum current that the solid state device can stand. Secondly, the resistance of solid state devices is much larger than the resistance of a mechanical circuit breaker. This imply more losses during the on-state.

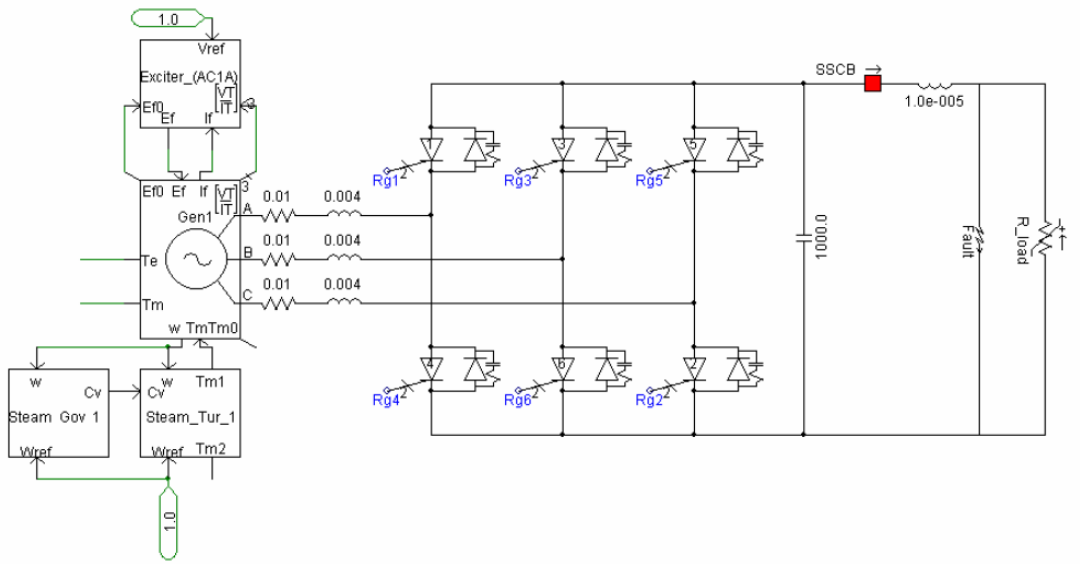

Figure 13 - Protection against faults using solid state circuit breaker

New approaches rely on controlling the converter duty cycle to limit and quench fault currents [28]. Converters composed by switches with turn-off capability, such as dc-dc buck converters, can also perform the fault current interruption when properly designed. After fault identification on the downstream side, the protection action taken by the relay is the turning off of converter switches. The action of hard turn off of switches interrupts the current from the primary side immediately, but the current on the load side does not cease immediately. The energy stored in the output inductor is freewheeled through the freewheeling diode of the converter. When this energy is completely dissipated, the fault is completely interrupted.

Summary

The advent of power electronic allows DC distribution systems to manage the voltage level, and consequently it makes it possible to distribute power with the opportune voltage level. In fact, with this improvement, DC distribution is becoming interesting for a lot of electrical applications. However, the challenge of the protection against ground and line fault is still unresolved.

2. A new approach for protection against fault in DC

Finding a new solution for the protection of DC systems against ground and line fault is the purpose of our work. For this reason, we investigated the feasibility of a protection method that does not involve the employment of circuit breakers. This is possible if we can turn off the main converter that feeds the DC bus, and to reconfigure the bus through contactors or sectionalizers already present on the DC system. Looking at the DC system in Figure 14, we can see where the elimination of circuit breakers is possible, and which elements of the system assume an important function in the protection against fault.

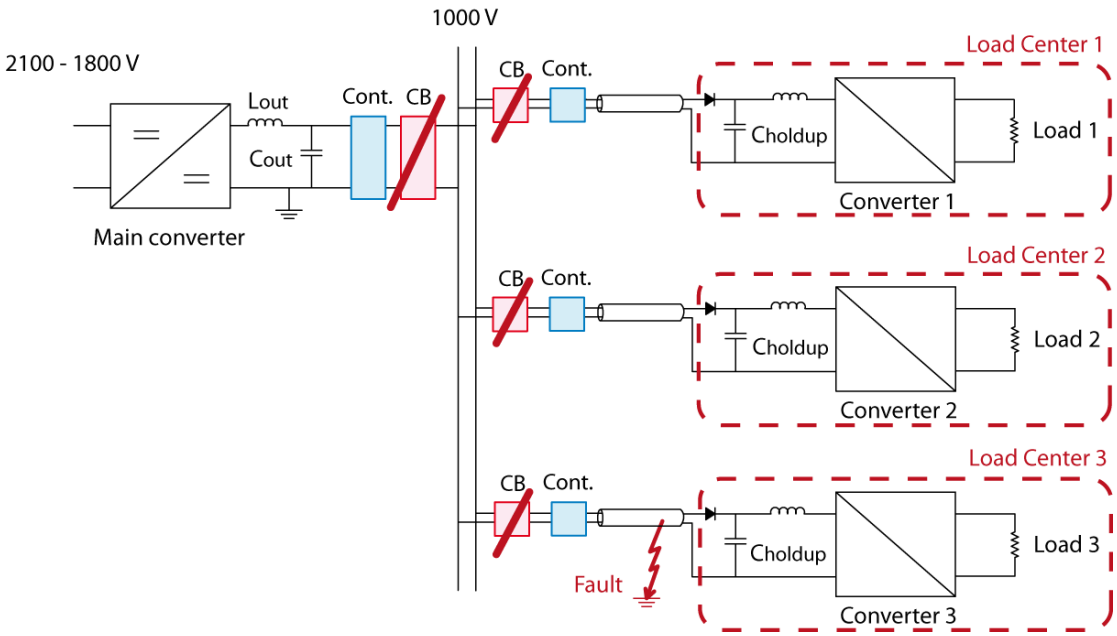

Figure 14 - Elimination of circuit breakers and holding of contactors in a DC system

First of all, the elimination of circuit breakers is possible both in the upstream side and in the downstream side of the DC bus. A necessary condition is that branches and loads of the bus are on the downstream side of a main converter. In this way, the protection of bus and loads is assured from the main converter.

Other elements that play an important role in the bus protection are diodes at the head of each load center. A load center can be represented by a converter that feeds one or more loads, and a capacitor at the input of the converter able to supply energy in case that the bus is brought down. We call these capacitors hold-up capacitors. The diode at the head of a load center allows each load center to be isolated from the main bus when the bus is brought down by a ground or a line fault on the upstream side. In fact, when the diode anode voltage goes under the cathode voltage and the current goes to zero, the diode is like an open circuit and the load center is isolated. Contactors or sectionalizers that are already part of the DC system can be used to reconfigure the bus in order to physically and permanently isolate a faulted branch.

The main advantage of our protection method is that it does not need additional devices to protect the system, but it uses components that already are in the DC system. Addition of diodes and hold-up capacitors are not required to protect the DC bus, but rather to enable the ride-through capability for load centers. Contactors or sectionalizers in a DC system are usually slow devices, because they do not need to open fault currents. Consequently, switching from traditional contactors to other type of contactor can be a necessity. Traditional contactors or sectionalizers have a opening time that can vary between 60ms and 1s. Last version of DC contactors have an opening time smaller than 15ms. Figure 15 shows a comparison between the opening time of different typologies of contactors, such as solid state devices and hybrid contactors.

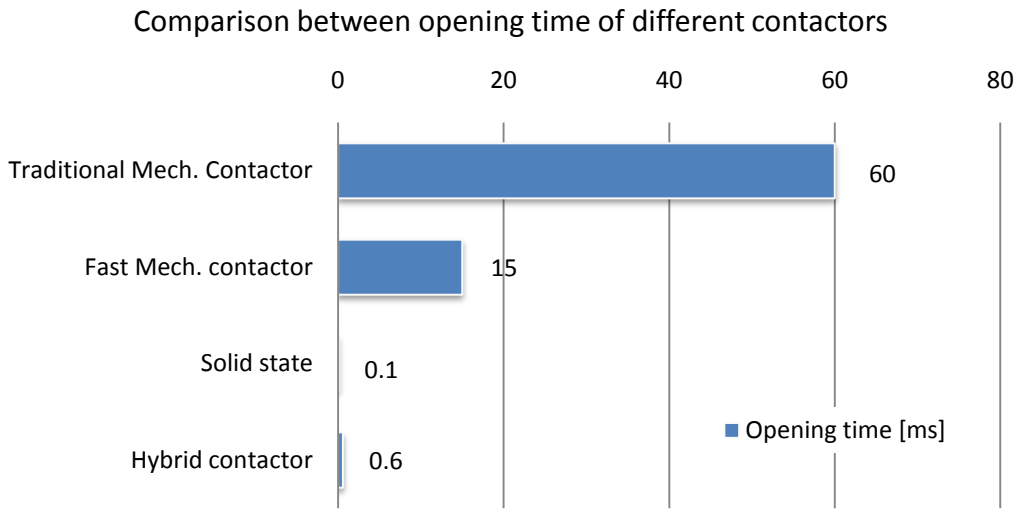

Figure 15 - Comparison between opening time of different kind of contactors

In chapter 5, more details about these kinds of devices are illustrated.

2.1 Controlled Power Sequencing

In this thesis a new approach that consists in a controlled power sequencing is presented. In order to redutc the out-of-service time and to allow unfaulted branches to ride-through the process, we introduced a power sequencing that acts on the main converter, and contactors of faulted branches.

Once the fault on one of the branch of the bus is individuated, the following power sequencing starts:

1) Turning off of the main converter
2) Opening of contactors when the fault current go down under the current nominal value
3) Bus reconfiguration and bus re-energizing

Figure 16 shows an overview of the protection process: the solid line shows the fault current dynamic after the individuation of the fault and the shutting off of the main

converter; and, the dashed curve shows the effect of the controlled power sequencing on the protection process [9].

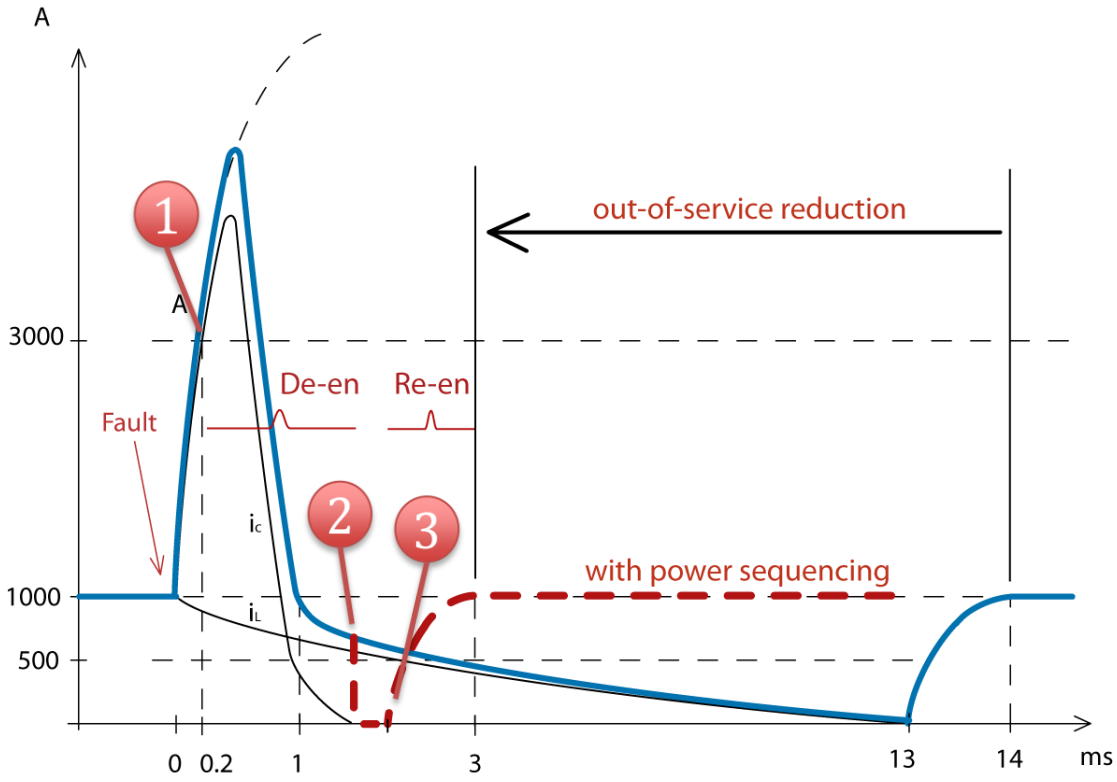

Figure 16 – Overview of the protection process action

In Chapter 4, more details about the controlled power sequencing and its performance are presented.

2.2 DC system description

The considered DC system is attributed to a DC shipboard electric system. Length of the system, cable parameters, voltage and power level are chosen following the development direction of new generation war ships. For this reason, we followed some guidelines proposed by a study by North Carolina State University in 2007: "Collaborative protection and control schemes for shipboard electrical system". In order to better concentrate our attention on the fault protection study, we analyzed a simplified DC distribution system that can be extended to a DC shipboard electric system or to a part of it.

2.2.1 DC zonal shipboard electrical system

The zonal power distribution system proposed by a study for one of the Navy war ship consists of two main power distribution buses running longitudinally along the port and starboard side of the ship. Each longitudinal bus consists of multiple cables and is separated by the maximum deck and athwartship distance to provide optimum survivability of the system. The ship is then subdivided into electrical zones, each zone having two power distribution load centers. Each power distribution load center is connected to the main power distribution buses via a connection box.

The zonal architecture eliminates the distribution sections and associated circuit breakers for the distribution switchboards. These distribution sections are replaced by smaller load centers, two load centers within each of the seven electrical zones [21].

Figure 17 and Figure 18 show the difference between the conventional and the zonal electrical distribution system of a war ship.

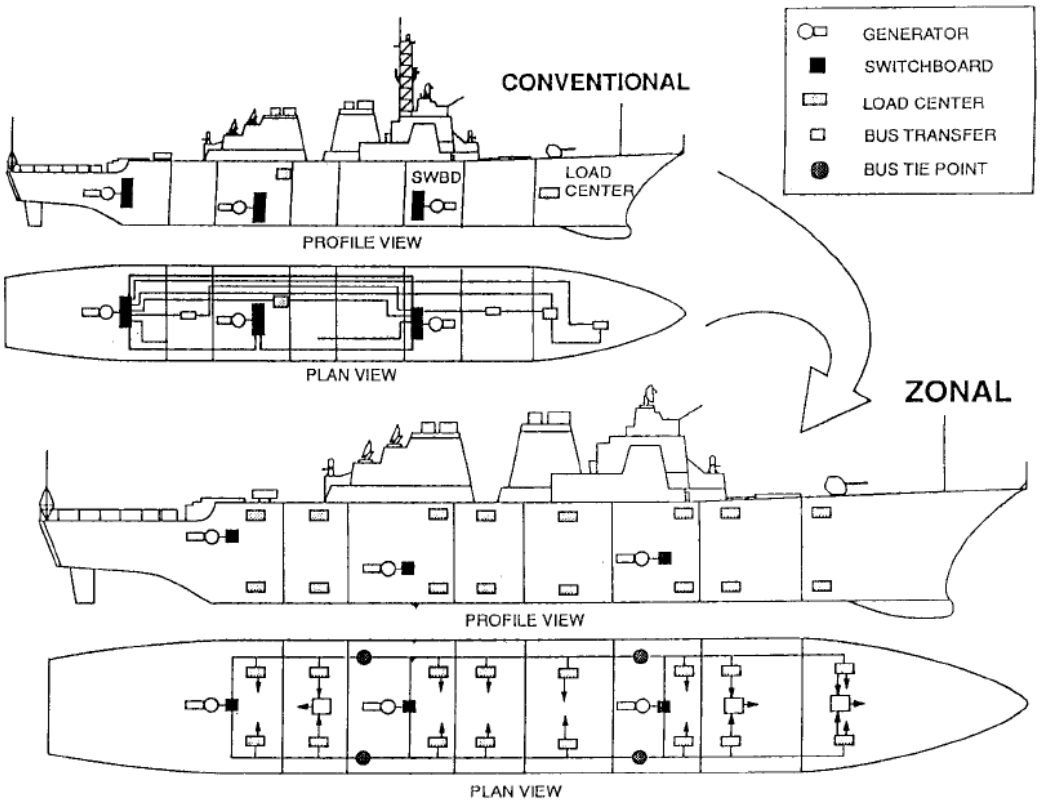

Figure 17 - Comparison between conventional and zonal architectures

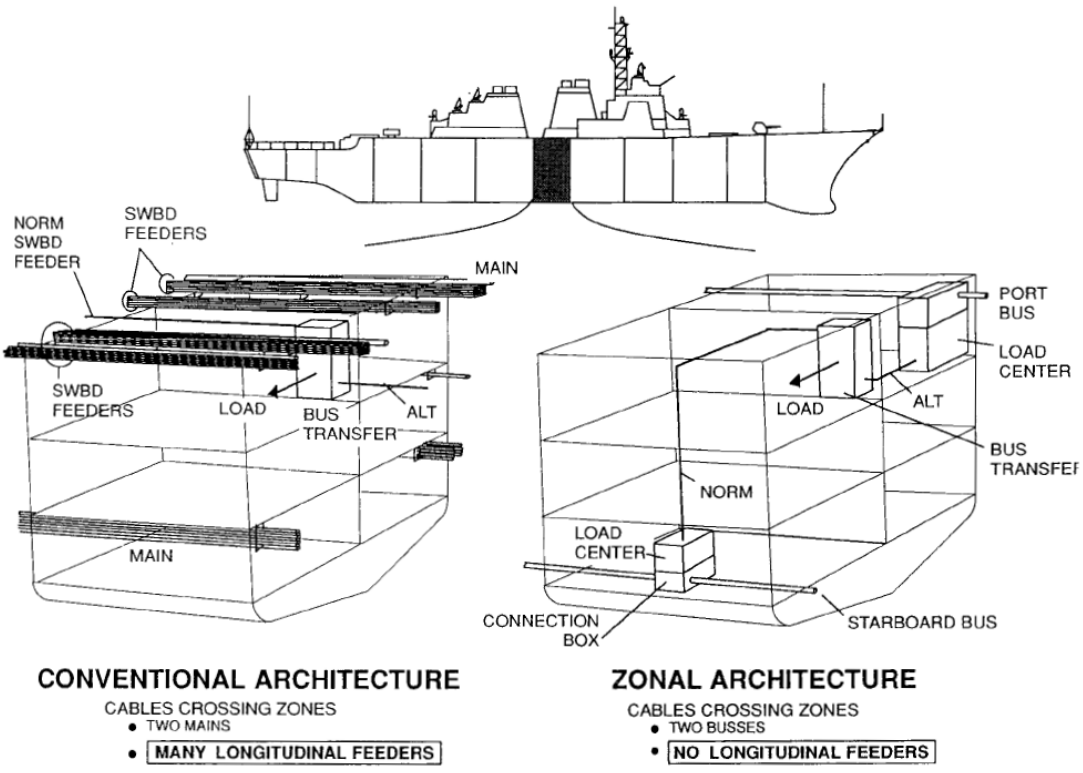

Figure 18 - Construction module comparisons for conventional and zonal electrical distribution systems

From the “Collaborative protection and control schemes for shipboard electrical system” study, we can consider the DC ship electrical system as composed by three main zones, as shown in Figure 19 [29].

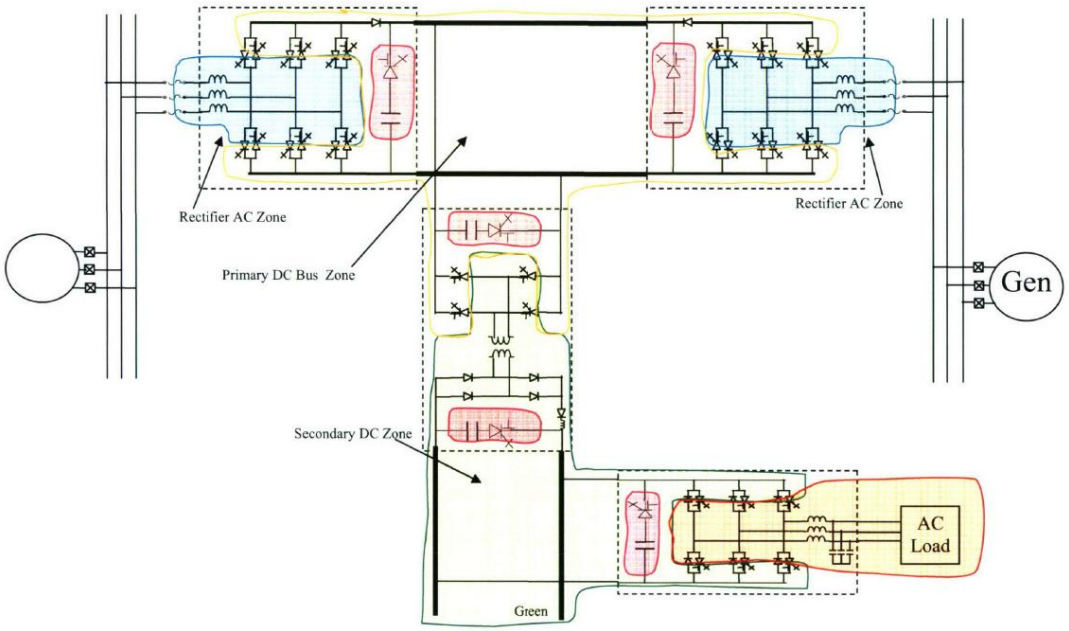

Figure 19 - Protection zones in a DC shipboard electrical system

Primary DC Bus Zones

The primary DC bus supplies power to all the load zones and therefore it is the most critical component for protection as it is also the one that is exposed to the most of the damages. Note that since switches in converters will be doing the fault interruption, the protection zone is defined by switches of converters that are connected to the bus, rectifiers, and buck converters. The zone therefore includes not only the bus but also the DC rail of rectifiers and buck converters, as illustrated in Figure 2001.

Secondary DC Bus Zone

This zone is defined by the buck converter and includes the secondary DC bus, load side buck converter rails, and source side inverter rails. The secondary DC bus supplies power to all the loads within the zone; either directly to the DC loads or via

inverters to AC loads. Therefore, the secondary DC bus is the second most critical component for protection. Different load zones on a ship are typically separated by watertight bulkhead compartments of the ship, and therefore, the faults occurring in a load zone are localized to that zone.

Rectifier AC Zone

The rectifiers are connected to the AC source bus supplied by generators. The AC source side of the rectifier, which includes the rectifier input filter elements, need to be protected, and the rectifier switches cannot be used for this purpose. Since the system uses mainly cables for power distribution, any fault in this protection zone, or any other part of the system, will be permanent rather than temporary. Thus, there is no need for fast reclosing capability that the circuit breaker (CB) can provide. A solution can be using fuses at the input terminal of the rectifier to protect this AC source zone of the rectifier. Note that the generators have usually their own protection zones defined by their CBs as illustrated in Figure 2001.

2.2.2 The DC system explored by simulations

Our system takes place either in the secondary DC bus zone or in the primary DC bus zone. While the standard of the voltage level for the primary DC bus is +/- 5kV, the secondary DC bus has a voltage level between 800V and 1000V [30]-[31].

We decided to develop a DC system with a voltage level of 1000V and a power level of 1MW. This model fits completely the characteristics of the secondary DC bus of the ship, but with some adjustments it can be applied to the +/- 5kV primary DC bus.

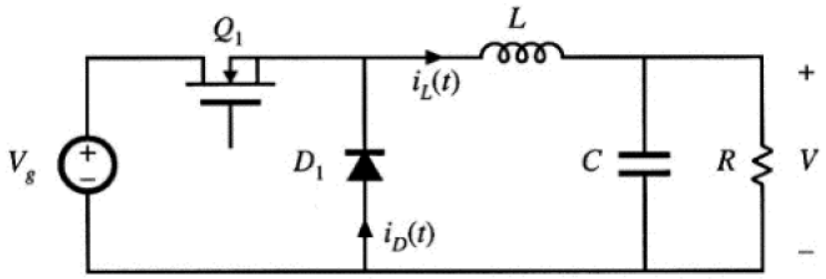

Figure 20 - Example of a buck converter

A buck converter as main converter that feeds the bus has been considered (Figure 20). The primary side has a voltage level of 1800-2100 V and the downstream side has a voltage level of 1000V. In order to have a more general case, we have considered the downstream side of the main converter grounded. It means that the negative conductor of the DC bus is grounded as illustrated in Figure 21.

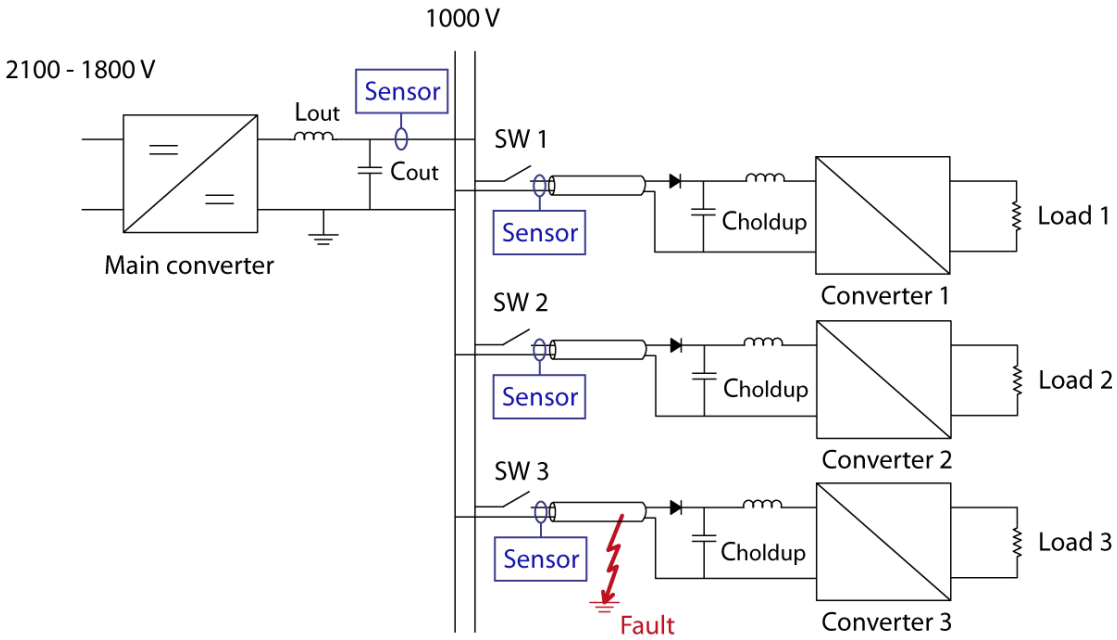

Figure 21 - Model used to study the DC system

The design of the inductance and the capacitor of the buck converter is interesting for the analysis that we have done. In fact, having inductance and capacitance value closed to those of a real DC/DC converter is important in order to have a reliable model.

Considering a maximum current ripple of 2.5%, having a DC system with a nominal current of 1kA, and the following values of input and output voltages:

V_g = 2100 V, Buck input voltage

V = 1000V, Buck output voltage

$\Delta i_L = 25A$, maximum current ripple

As shown in [32], the inductance of the buck converter can be found as:

$$L = \frac{V_g - V}{2\Delta i_L} \frac{V}{V_g} \frac{1}{f_{sw}} \quad (4)$$

After the determination of the buck inductance, determining the value of the output capacitor is possible:

$$C = \frac{1}{(2\pi \cdot f_C)^2 \cdot L} \quad (5)$$

Different choices can be done about switching frequency (f_{sw}) and cutoff frequency (f_C). Table 1 shows values of inductance and capacitor of the converter with a cutoff frequency 1/50 and 1/10 of the switching frequency.

Table 1 - Inductance and capacitor of the main converter depending on the switching frequency

	fc = 1/50 fsw			fc = 1/10 fsw		
fsw	fc	L [uH]	C [uF]	fc	L [uH]	C [uF]
1000	20	8889	7124	100	8889	285
4000	80	2222	1781	400	2222	71
10000	200	889	712	1000	889	28
25000	500	340	280	2500	340	12
40000	800	222	178	4000	222	7
60000	1200	148	119	6000	148	5
100000	2000	89	71	10000	89	3

For our model, we decided to consider a switching frequency of 25kH and a cutoff frequency equal to 1/50 of the switching frequency. Table 2 shows values of inductance and capacitor chosen for the converter during the analysis.

Table 2 – Characteristics of the main converter

fsw	L [uH]	C [uF]
25000	340	280

The DC bus composed by different branches is represented by π distributed parameter lines. We have considered the following cable parameters from technical documents for the considered voltage and power level [33]:

Table 3 – Characteristics of the DC link cable

R [mOhm/m]	L [µH/m]	C [nF/m]
0.193	0.3051	0.55

We have considered a range of lengths between 3 and 100 meters as length of cables of the DC bus. These dimensions are compatible with the dimensions of a common war ship or a zone of a war ship.

Loads on each branch of the DC bus are considered in two ways. They are represented as a resistive load during simulations of the fault dynamics on the entire system, because of memory availability on the computer used for simulations. Regarding analysis on the supplying of power by means of hold-up capacitors, a constant power load model has been used to represent converters that feed loads. In the first case, the modellization of the branch converter as a constant power load is not required because the fault time is much smaller than the time of load variations in normal operation conditions. In the second one, considering the load as a constant power load is a

necessity because it reflects the proper energy extraction by means of a controlled converter.

Another important consideration is the definition of the nominal current I_n. We define as nominal current the rated current of the DC bus that corresponds to the rated current of the main converter that feeds the bus.

2.3 Illustration of the work

The developed work is composed of a short circuit fault analysis, a parametric study, and considerations on two important component of the system: contactors and hold-up capacitors.

The action on the main converter and the hard turning off of switches interrupt the current from the upstream side immediately, but the current on the downstream side of the converter does not cease immediately because of the discharge of inductance and capacitor of the converter. In order to understand the behavior of the system when a short circuit fault happens, we observed current fault dynamics, carrying out an analysis of fault and fault current through simulations.

The proposed protection method is strongly dependent on parameters and configurations of the system. This involves an high variation of the protection scheme performances depending on the kind of converter, DC bus configuration, load, fault condition. For this reason we made an accurate model with SimPowerSystems Application Library of Simulink®, and we carried out simulations with different converters, DC bus configurations, and fault conditions. This allows us to obtain a parametric study for the fault protection method.

Contactors at the head of each branch of the DC bus and hold-up capacitors, which store energy to supply loads when the bus is down, are critical elements of the system and they influence performances of the protection scheme. In order to have a more clear illustration of the proposed approach, we did some considerations about these two components.

3. Fault dynamics analysis

The first step for the formulation of a new protection strategy for a system is observing how such a system behaves when a fault happens. For this reason, we run a in-depth analysis of transients due to a short circuit both through an analytical analysis, and through simulations with a Simulink ® test bench.

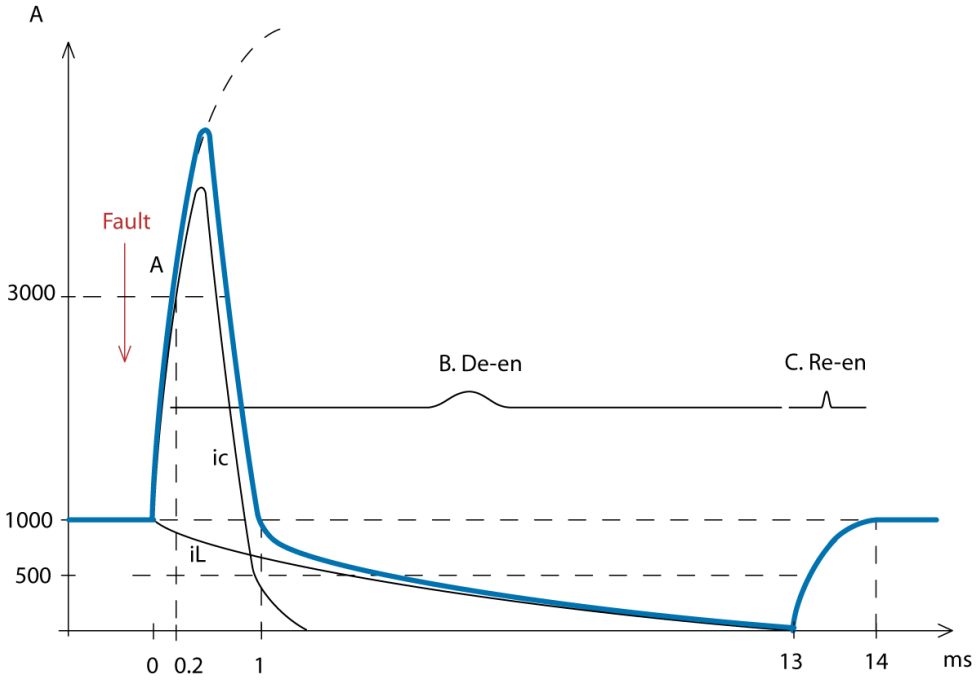

Figure 22 - Shot circuit fault analysis on a DC bus

When a ground fault happens ($t=0$) on a branch of the DC bus, the fault dynamic is divided in three main parts (Figure 22).

A. *Current rising*. When a short circuit or ground fault happens, the current begins to rise due to the low impedance of the fault. When the current reaches a certain value, the rising of the current through the main converter can be stopped by sending an off-signal to the converter control. The valves of the converter are able to extinguish the current within a converter cycle. While the flux of energy supplied by the converter is stopped, the energy stored in the

output inductance and capacitor of the converter keeps feeding the fault. Thus, the fault current keeps rising.

B. *De-energizing process.* Once the main converter is shut off, the output inductance and capacitor discharge their energy on the faulty bus with a time constant depending on system elements involved: the output inductance, the output capacitance, cable parameters, the impedance and distance of the fault from the main converter.

C. *Re-energizing process.* Once the current is definitely brought to zero, the switch SW3 can isolate the faulty branch, and the main bus has to re-energize the entire DC bus to come back to the operation state. Loads, bus cables, the main converter, and possible storage elements take part at this process.

3.1 Current rising

How the current rises when a short circuit fault happens is important with regard to the fault individuation. Many solutions about fault individuation have been studied in

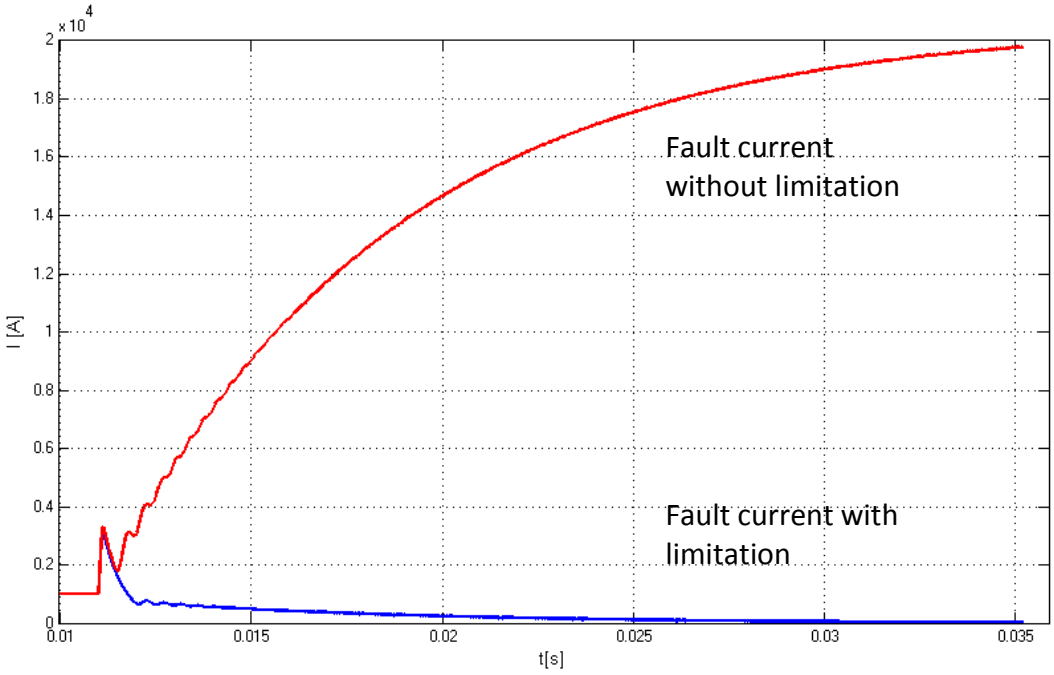

Figure 23 – Comparison between a fault current in a DC system with and without the possibility of limiting the converter current

the literature [34]. In this analysis, a maximum current threshold method has been chosen. We fixed the maximum current threshold at 3 times the nominal current of the main converter.

Figure 23 shows the comparison between a fault current in a DC system with the possibility of limiting or nullifying the converter current and a fault current in a system where the fault current must be limited by a Circuit breaker. In the first case the current has an initial peak. After that the current decreases slowly, but with value less than the nominal value of the current. The current in the second case is much larger and needs a circuit breaker with arc eliminating equipment to bring the current down to zero.

3.2 De-energizing process analysis

The new converter generations are able to limit the current requested from a DC bus and to instantaneously interrupt the current flow from the upstream to the downstream side of the converter. They cannot stop the output inductance and the output capacitor from supplying a ground fault on one of the branches. We did an analytical analysis of the discharging process by investigating the dominant transient after the main converter valve was turned off. In this case, we have the superposition of two main transient events as we can see from Figure 22. The first current impulse (i_C) depends on the size of the output capacitor and the fault impedance. The short time constant is due to the small value of the fault resistance ($\tau_1 = R*C_{out}$). The second slower-decaying current (i_L) depends on the size of the output inductor ($\tau_2 = L_{out}/R$).

Figure 24 shows a simplified equivalent circuit that represents the downstream side of the main converter, the DC bus and the fault resistance.

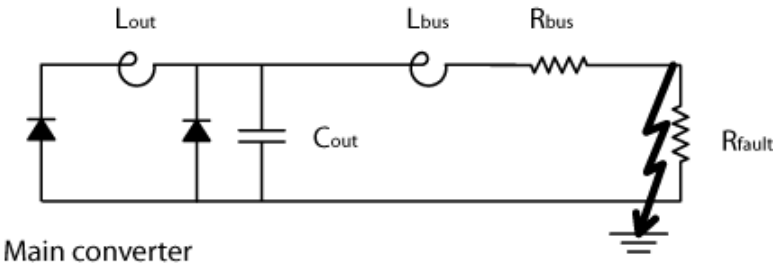

Figure 24 - Equivalent circuit of the downstream side of the main converter and the faulted DC bus

In this analysis, the main converter, the DC bus, and the fault have the following characteristics (Table 4, Table 5).

Table 4 - Parameters of the main converter

Switching Frequency [Hz]	L_{out} [uH]	C_{out} [uF]
25000	340	280

Table 5 - Line parameters and fault resistance

R [mOhm/m]	L [µH/m]	Rfault [Ohm]
0.193	0.3051	0.02

Under these conditions and with a fault distance of 100 meters, the two following time constants result from the analytical analysis of the system:

$$\tau_1 = R \cdot C = 11us$$

$$\tau_2 = \frac{L}{R} = 8.6ms$$

$$t(10\%) = 2.3 \cdot \tau_2 = 20ms$$

Table 6 shows the variation of the de-energizing time depending on the distance of the fault from the main converter.

Table 6 - De-energizing time dependence on the distance of the fault from the main converter

distance [m]	R [Ohm]	C [uF]	L [uH]	τ1 [ms]	τ2 [ms]	t (10%) [ms]
100	0.0393	280	370	0.011	9.4	**21.7**
90	0.03737	280	367	0.010	9.8	**22.6**
80	0.03544	280	364	0.010	10.3	**23.6**
70	0.03351	280	361	0.009	10.8	**24.8**
60	0.03158	280	358	0.009	11.3	**26.1**
50	0.02965	280	355	0.008	12.0	**27.5**
40	0.02772	280	352	0.008	12.7	**29.2**
30	0.02579	280	349	0.007	13.5	**31.1**
20	0.02386	280	346	0.007	14.5	**33.4**
10	0.02193	280	343	0.006	15.6	**36.0**
3	0.020579	280	340.9	0.006	16.6	**38.1**

Table 7 illustrates the variation of the de-energizing time for different value of output inductance.

Table 7 - De-energizing time variation for different value of output inductance

distance [m]	R [Ohm]	C [uF]	L [uH]	τ1 [ms]	τ2 [ms]	t(10%) [ms]
100	0.0393	**5**	**5**	0.0002	0.1	0.3
100	0.0393	**10**	**10**	0.0004	0.3	0.6
100	0.0393	**50**	**50**	0.0020	1.3	2.9
100	0.0393	**100**	**100**	0.0039	2.5	5.9
100	0.0393	**200**	**200**	0.0079	5.1	11.7
100	0.0393	**300**	**300**	0.0118	7.6	17.6
100	0.0393	**400**	**400**	0.0157	10.2	23.4
100	0.0393	**600**	**600**	0.0236	15.3	35.1
100	0.0393	**1000**	**1000**	0.0393	25.4	58.5

The time to reach 10% of the nominal current value has been considered as a good approximation of the null value. Thus, the time to reach the complete discharge is about 25 ms for considered system.

In order to have a more accurate model, we did a transient analysis through Simulink® simulations, by inserting a π distributed line between the main converter and the ground fault with the following values:

Table 8 - π distributed line parameters

R [mOhm/m]	L [µH/m]	C [nF/m]
0.193	0.3051	0.55

In Figure 25, the de-energizing transient is shown. We can notice the superposition of the two main transients: the first one due to the output capacitor and the second one due to the output inductance.

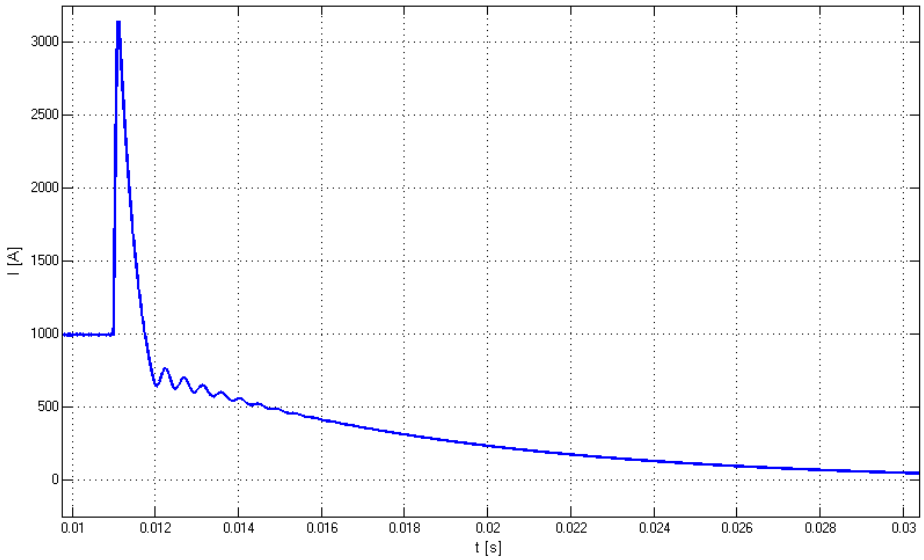

Figure 25 – Example of De-energizing process of a DC bus

The DC bus length variation, which is the distance from converter to fault, and the maximum current threshold are parameters we have considered.

The result from the transient analysis of the DC bus discharge is that there is a large dependence between discharge time and the distance of the fault from the main converter. Considered distances are from 3 to 100 meters. Figure 26 shows an inverse relationship where as the distance of the fault increases, the de-energizing time of the DC bus decreases. The four different curves represent the time to go down to the 100%, the 50%, the 25%, and the 10% of the nominal current value, respectively.

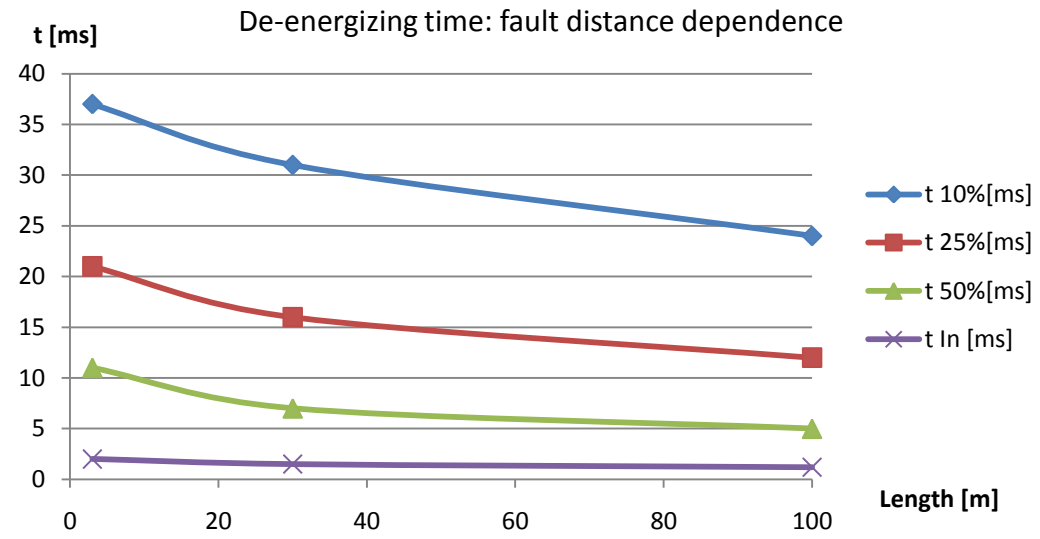

Figure 26 – De-energizing time dependence on the bus length

The maximum current value (Trip current) at which the main converter is shut off affects the discharge time because the current going through the output inductance is higher and the energy that the DC bus has to dissipate is greater (6).

$$W = L \int_0^I i(t)di(t) \qquad (6)$$

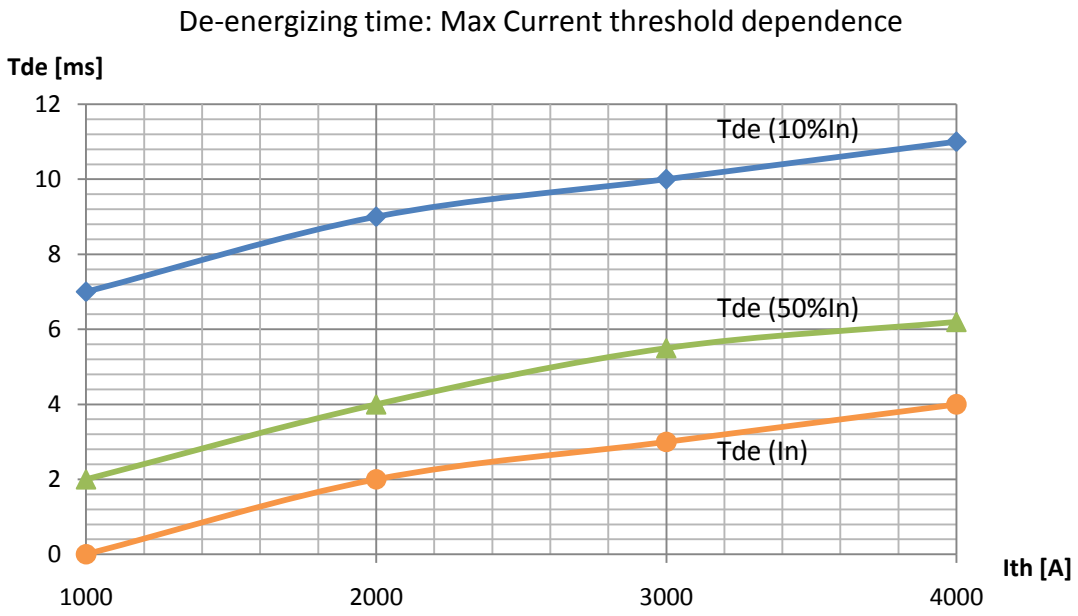

Figure 27 – De-energizing time dependence on the max current threshold (Trip current)

Looking at the literature, we assume that the current limit is about three times the rated current [32],[35]. The graph of Figure 27 shows the time to reach the rated current as 50% and 10% of the rated current, respectively.

Due to the amount of the energy stored in the output inductance of the main converter and the small equivalent resistance of the cable and of the ground fault, the de-energizing time is strongly influenced by the size of the output inductance.

Figure 28 illustrate the fault current behavior for 3 different output inductance (100 µH, 340 µH, 1000 µH). The last part of the transient (t > 0.012s) is influenced by the

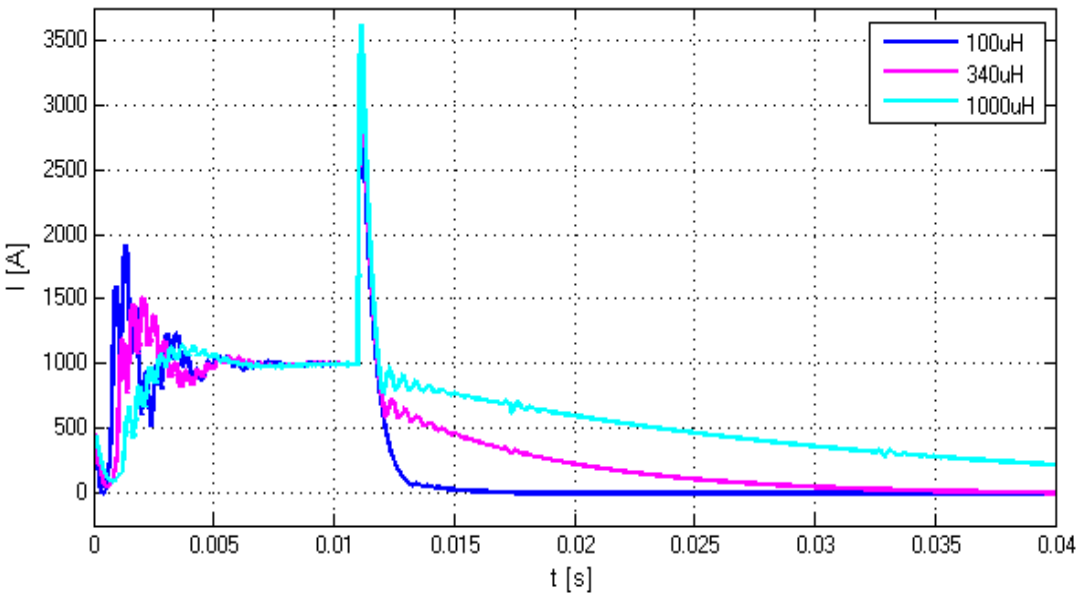

Figure 28 – Fault current behavior for different value of output inductance (100-340-1000 uF)

inductance of the converter.

Figure 29 shows that the time has a linear dependence on the inductance as confirmed by the transient theory. The time to reach the 10% of the nominal value of the current is very interesting for our study and it is considered as good approximation of the null value of the fault current.

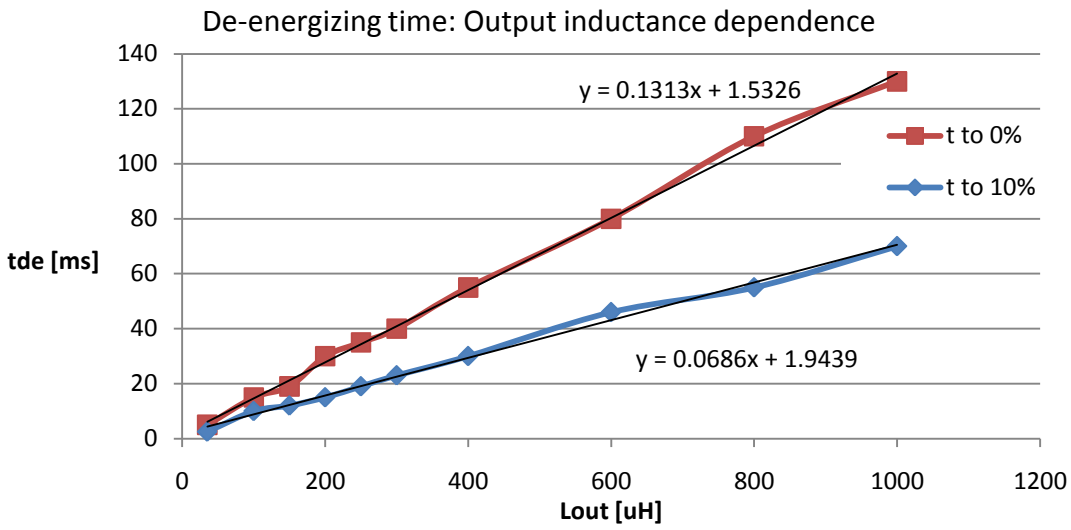

Figure 29 – De-energizing time dependence on output inductance of the main converter

The short circuit current is characterized by a current peak due to the fast discharge of the output capacitor of the main converter on a small equivalent resistance. The simulations of the considered system shows a parallel relationship where as the capacitor size increases, so does the de-energizing time of the DC bus. Figure 30 illustrates how the current peak depends also on the distance of the fault from the main converter.

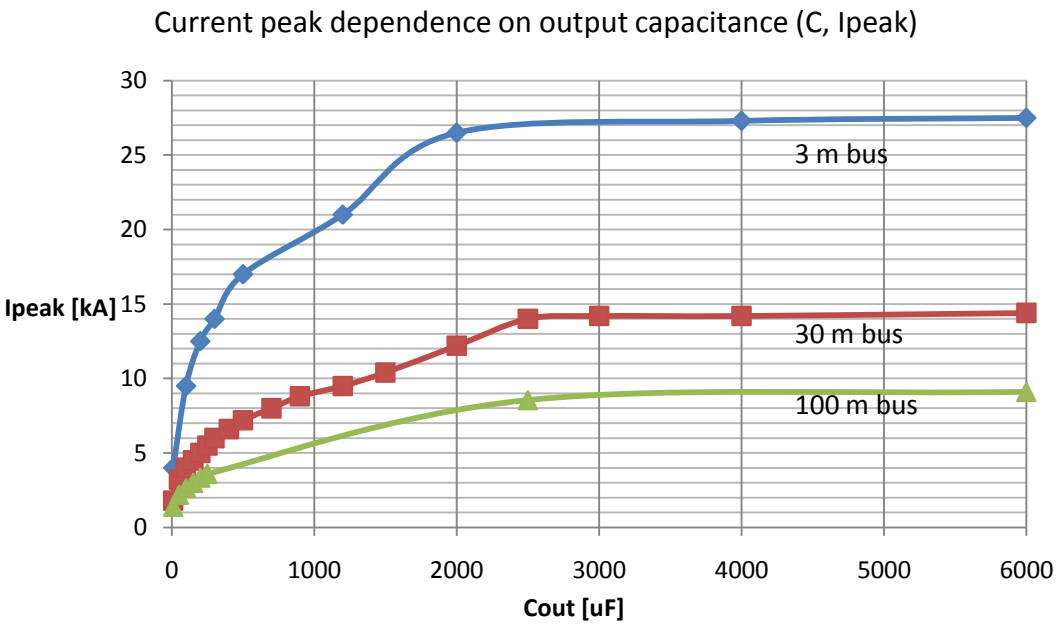

Figure 30 – Current peak dependence on output capacitance of the main converter

Summary

The analysis shows that the parameters of the system that influence the de-energizing time are: the bus length or the distance of the fault from the main converter, the current flowing in the output inductance of the main converter when the protection process intervenes, the main converter output inductance and output capacitor size. The value of the current peak depends mainly on the output capacitor size and on the proximity of the fault to the main converter. The equivalent resistance of the short circuit fault also influence the de-energizing process, but we decided to carry out the transient analysis considering the fault equivalent resistance closed to 0.02 Ω, and able to cause a short circuit current of 50kA. This resistance is small enough for such a system.

From these results, we can see that although the fault current spends between 2 and 60 ms to go to zero, the current needs only 0.5-4 ms to go down under the nominal value and 2-6 ms to decrease under 50% of the nominal value.

3.3 Re-energizing process analysis

In order to provide the ride through capability for healthy branches, the time to re-energize the entire bus must be short. Figure 31 shows an example of the voltage behavior during the re-energizing process of the DC bus.

The output capacitor of the main converter, the input capacitors of converters that feed healthy branches, and possible storage elements (such as hold-up capacitors) take part in this process. In fact, these elements have to be recharged by the main converter if they have been discharged through the fault, or by supplying downstream loads.

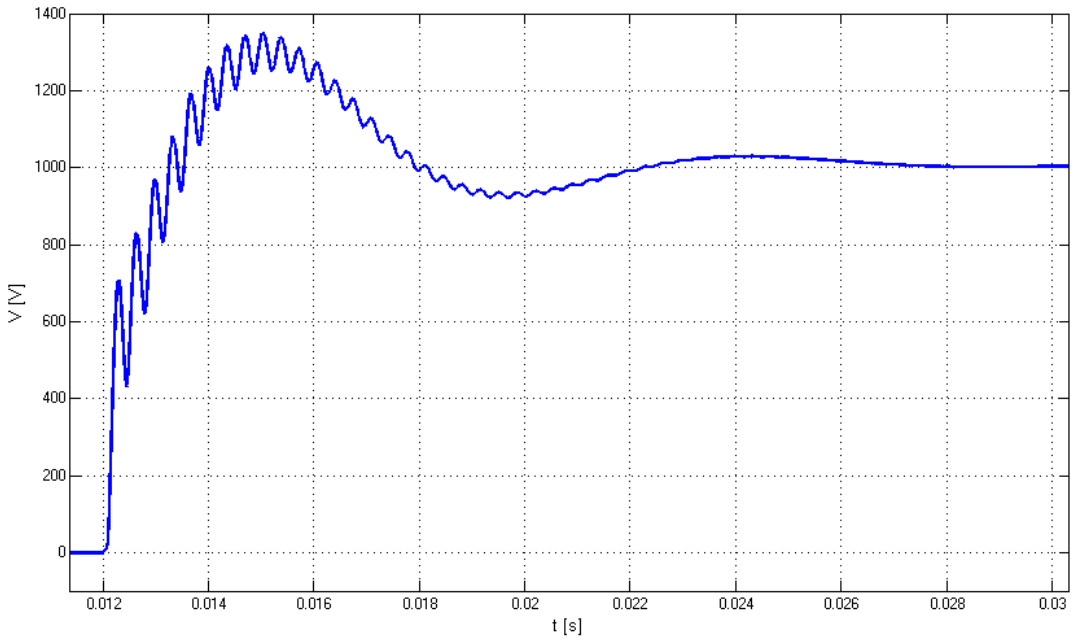

Figure 31 – Voltage behavior during the re-energizing process [REDO with control]

For this reason, the bus charging process for different lengths and different voltages on healthy branches' converter input capacitors and hold-up capacitors has been studied. Figure 32 illustrates the voltage trend graph that shows the re-energizing process of two different unfaulted branches after the turning on of the main converter (t = 0.012 s). The different voltage level on the two hold-up capacitor is due either to the different size of capacitors or to the difference between loads.

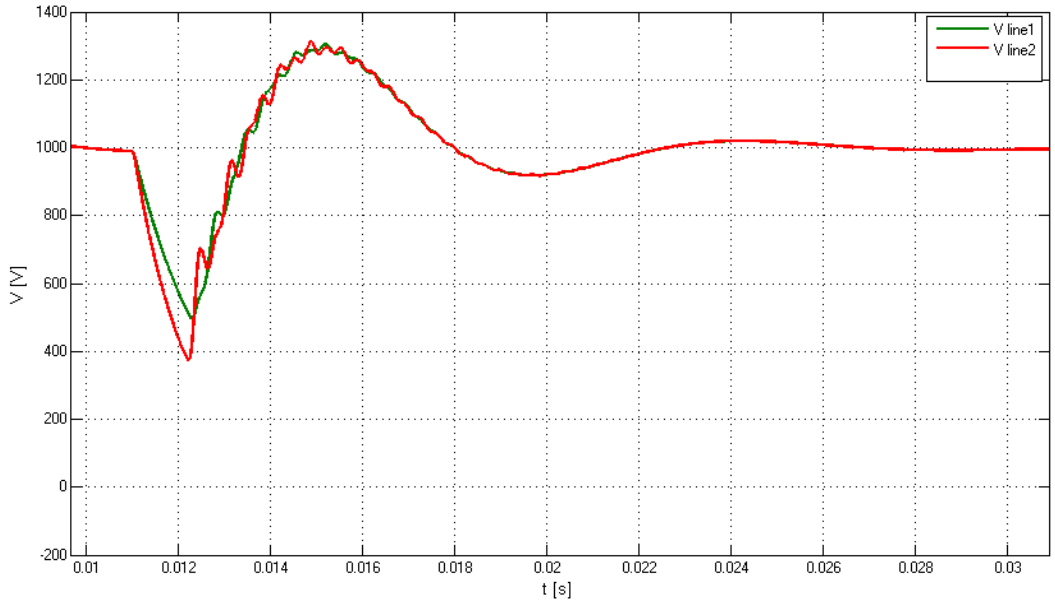

Figure 32 – Example of the re-energizing process of two different lines

In Figure 33, the re-energizing time for different voltage levels on the hold-up capacitors is shown.

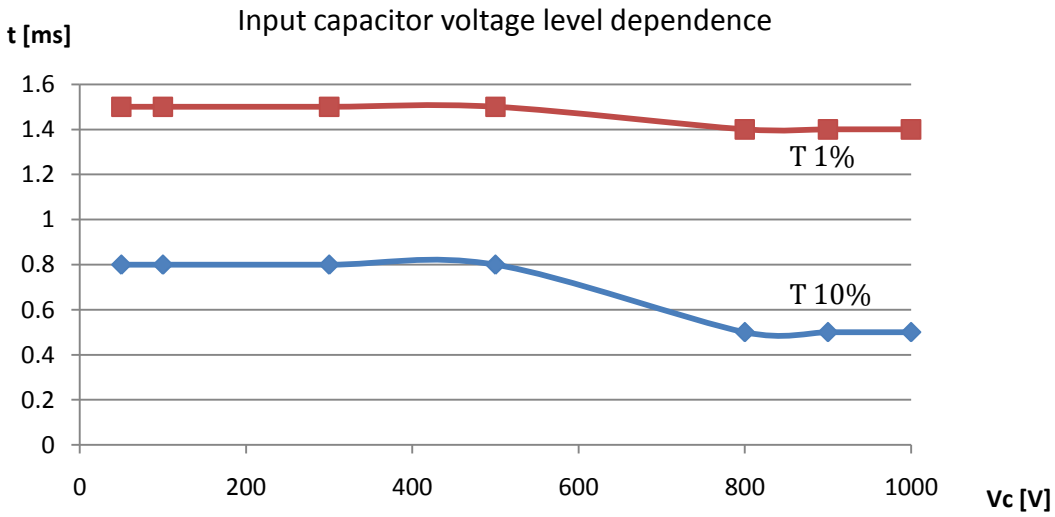

Figure 33 – Re-energizing time dependence on the input capacitor voltage level

The first trend indicates the re-energizing time to reach the rated voltage with 10% accuracy and the second one with 1% accuracy.

Summary

The time that the system needs to re-energize the DC bus does not depend from the DC bus length very much because of the small influence of the resistance and inductance of the cable compared with the equivalent impedance of loads. Simulations show how the charging rapidity of storage elements depends strongly on the main converter overload capability, and on the level of discharge of each capacitor on the load side (input capacitors of the converter of loads, hold-up capacitors, etc.). The influence of hold-up capacitors and other storage elements has been studied in chapter 5.

4. Parametric study and performances of the protection method

In this thesis a new approach is presented that consists in a controlled power sequencing. The analysis carried out in the previous chapter shows that the de-energizing time, after the turning off of the main converter, is strongly dependent on system components. Although the complete de-energizing happens between 2 and 60 ms, the fault current go down under the nominal current value in only 0.5-4 ms. A look at the fault current behavior shows the possibility to shorten the de-energizing time by opening some contactors (SW1, SW2, SW3) at the head of each branch of the DC bus as shown in Figure 34.

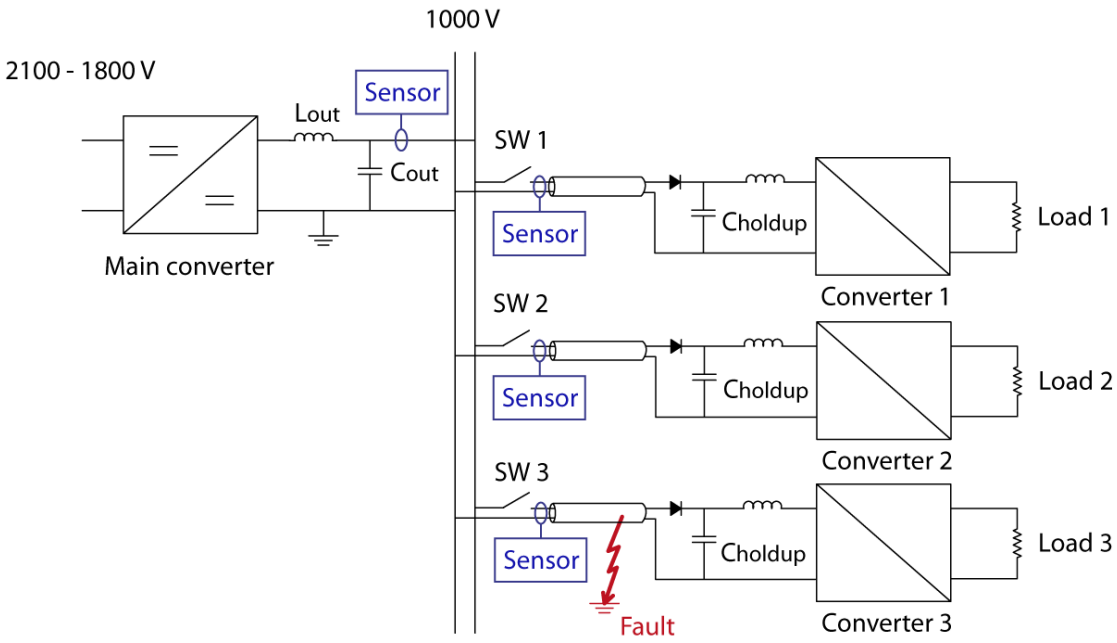

Figure 34 – DC bus scheme – Location of contactors that isolate faulted branches and reconfigure the bus

The low value of the fault current after 0.5-4 ms enables the use of contactors instead of the employment of circuit breakers because opening of the entire fault current is avoided by the power sequencing. Once the fault is eliminated and the faulty branch is disconnected the main converter can be turned on and the DC bus re-energized.

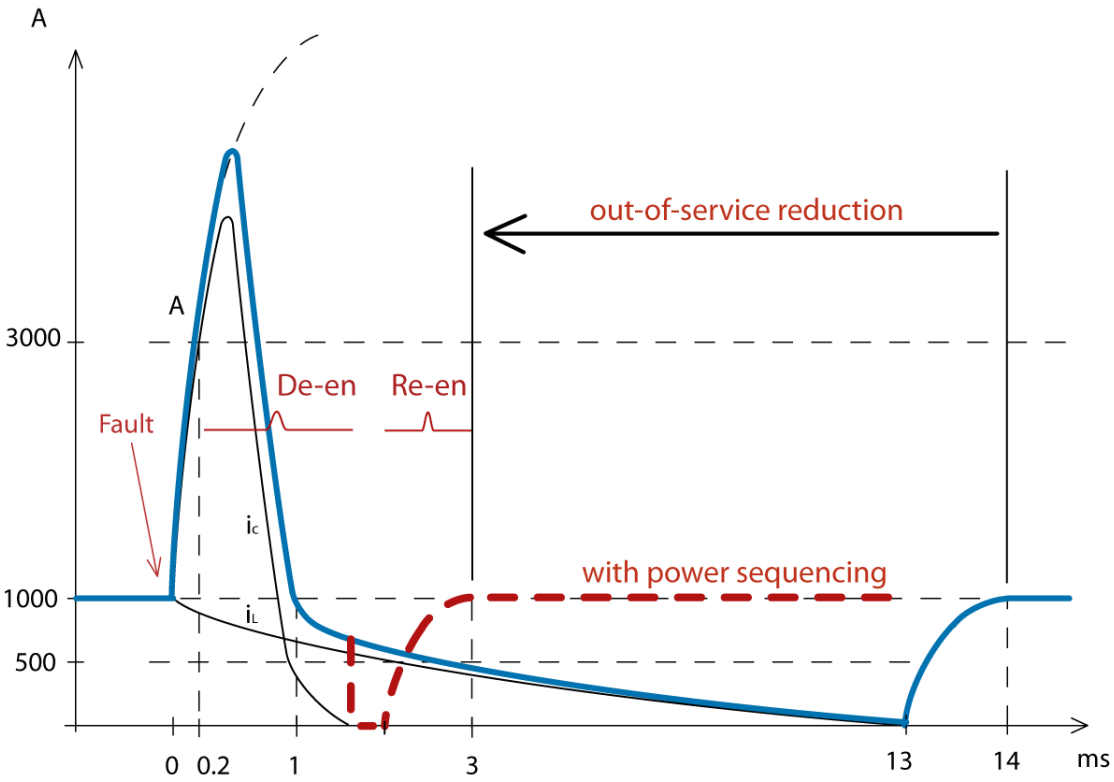

Figure 35 – Controlled power sequencing effect on the DC bus protection process

Figure 35 shows an overview of the protection process: the solid line shows the fault current dynamic after the individuation of the fault and the shutting off of the main converter; and, the dashed curve shows the effect of the controlled power sequencing on the protection process.

The shortening of the de-energizing time and a fast DC bus reconfiguration allows the unfaulted branches of the bus to ride-through the process uninterrupted if the system is equipped with hold-up capacitor on the upstream side of the downstream converters that supply energy to loads.

Figure 36 shows the comparison between the protection scheme before and after the introduction of the controlled power sequencing (CPS). Moreover, Figure 36 shows the influence of the type of contactor that we use to isolate the faulted branch on the protection process with the controlled power sequencing.

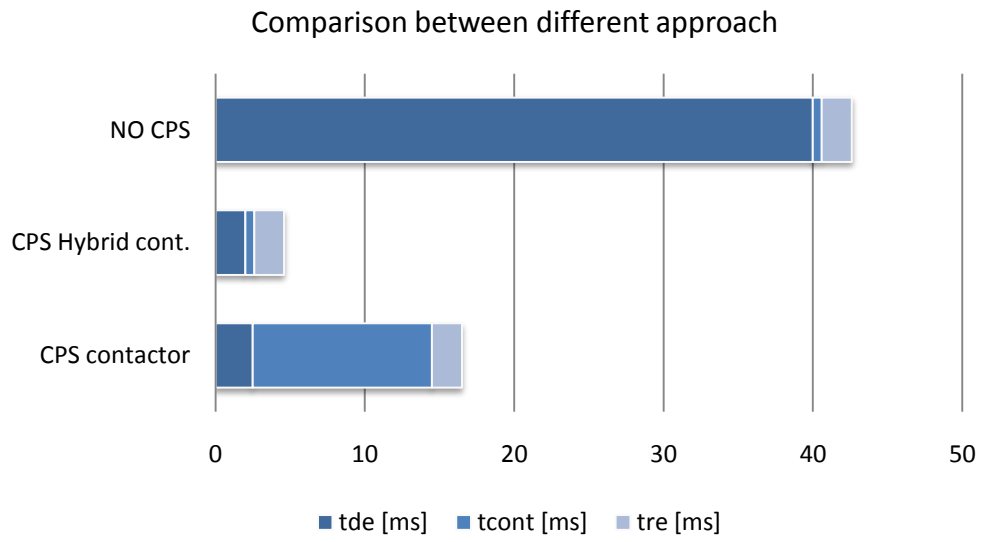

Figure 36 – Comparison between protection scheme without and with the power sequencing and between different type of contactor to isolate the faulty line

The decision to adopt the controlled power sequencing to protect the DC bus from short circuit and ground fault lead to new considerations about the influence of components of the system on the fault protection process.

4.1 Influence of the system components on performances of the protection system

Components of the system influence performances of the fault protection process by changing the current peak of the fault current, the time that the fault current needs to go down under the nominal value, and the amount of energy to interrupt by mean of a contactor that isolates the faulty branch.

The considered components in our study are:

1. Output capacitor of the main converter (C_{out})

2. Output inductance of the main converter (L_{out})

3. Contactors used to isolate the faulted line

4. Overload capacity of the main converter (I_{MAX}/I_n)

5. Cable length and Fault impedance

4.1.1 Output capacitor of the main converter influence

The output capacitor of the main converter, as already demonstrated in chapter 3, is one of the most critical components of the system because of the size of the main converter and the amount of energy that can be stored in the capacitor. Sometimes, this kind of capacitor are used also as energy storage or as bus interface capacitors, besides as voltage smoothing. In these cases, when the capacitance and the stored energy exceed a specific value, considerations on the protection of these elements are necessary, depending on the type of capacitor and the allowed peak current. For example, electrolytic capacitors need a protection against reverse voltage. In case of use of electrolytic capacitors, we added a diode in parallel to each capacitor to prevent damages to the capacitor.

In the matter of protection system, the time that the fault current needs to go down under the nominal current value depends on the size of the output capacitor. In fact, the duration of the current peak depends on the amount of energy to dissipate and thus on the size of the output capacitor.

The time that the output capacitor needs to discharge on the faulty line corresponds to the minimum time at which we can shorten the de-energizing process by isolating the faulty branch by means of contactors. For this reason, we did a transient analysis of the capacitor discharge on a faulty line for different sizes of capacitor and for different distances of the fault from the main converter capacitor.

Figure 37 shows the dependence of the current peak duration on the size of the output capacitor. There is a parallel relationship between the current peak duration and the size of the capacitor.

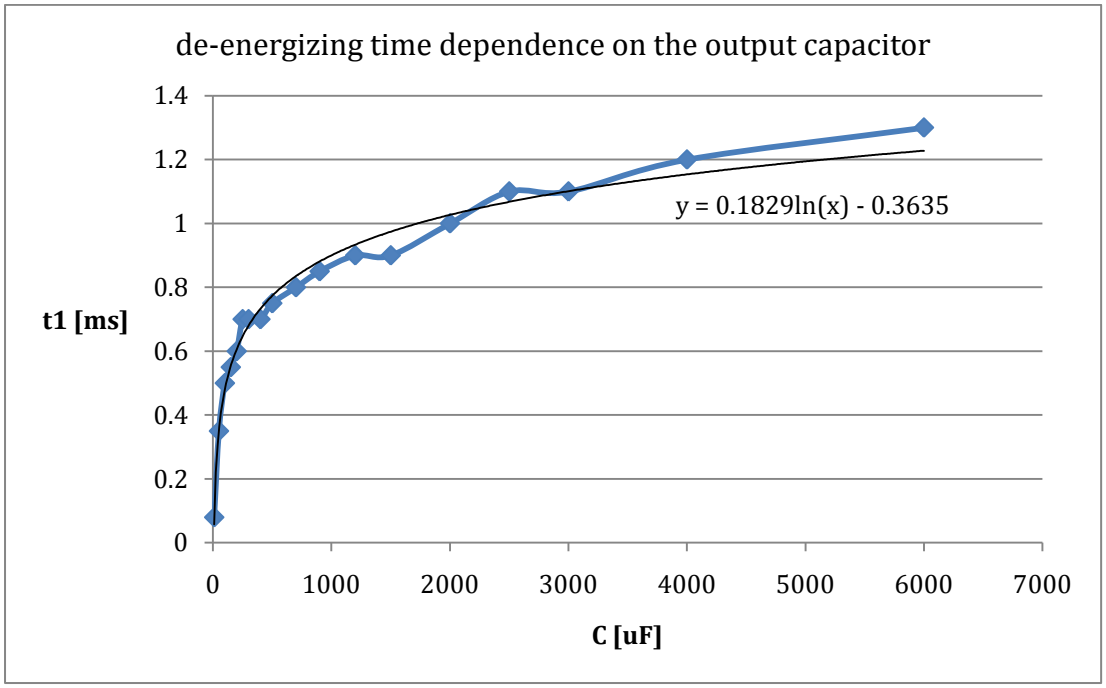

Figure 37 – Current peak duration dependence on output capacitor

4.1.2 Output inductance of the main converter influence

The output inductor of the converter has two main characteristics: it limits the current variation, and it contain a large amount of energy.

Regarding the influence of the inductor on performances of the protection process, we have to face the tradeoff between employing a large inductor that limits the current increasing during the first instants of the fault, and limiting the inductance and the respective amount of energy to dissipate.

The absence of delay (between the fault individuation and the turning off of the converter) due to the control action allows the use of a smaller inductance.

The rate of the current is given by the following relationship:

$$\frac{dI(t)}{dt} = \frac{V_L}{L_{OUT}} \qquad (7)$$

Table 9 shows the current rising rate dependence on the output capacitance of the main converter. If the control time remains in the order of µ-seconds a wide range of inductance is usable.

Table 9 - Relationship between output inductance and current rising rate

L [µH]	W [J]	di/dt [A/µs]
5	2.5	200
10	5	100
50	25	20
100	50	10
200	100	5
300	150	3.3
400	200	2.5
600	300	1.7
1000	500	1

These results illustrate clear references for the choice of the switching frequency of the converter and for the design of the converter controller. For example, with a switching frequency between 25 and 40 kHz the response time acting on the duty cycle is between 40µs and 25µs respectively. The response time acting directly on the gate signal of the switches of the converter is dependent only on the control loop rapidity.

The output inductance is usually imposed by the limiting of the converter ripple. In case this limitation conflicts with previous inductance limits, other solutions are usable. For example putting two or more converter in parallel allows the reduction of output inductances by maintaining the same output ripple.

4.1.3 Contactors for the DC bus reconfiguration

The time that contactors needs to open faulty branches (Opening time) takes part in the duration of the protection process. In Chapter 5, we made considerations about some kind of contactors, solid state switching devices, and hybrid contactors.

Choosing hybrid contactors as a solution for our system, we can observe that the time (t_1) to de-energize and to reconfigure the DC bus became:

$$t_1 = t_{de} + t_{cont} \tag{8}$$

Where t_{de} is the de-energizing time and t_{cont} is the time that the contactor or hybrid contactor needs to open faulted circuit.

While commercial DC contactors for this kind of system need between 12ms and 20ms to open a circuit, the hybrid contactor shown in chapter 5 has a opening time of 0.6ms. If the contactors on each branch of the bus are sized for the nominal current I_n of the system, the best performances of the protection scheme are achievable. That means that an oversizing of contactors is necessary. If the oversizing of contactors is not possible (The contactors are sized for the rated current of the single branch of the bus), the protection process keeps working with a longer de-energizing time.

4.1.4 Overload capacity of the main converter

The overload capability of the main converter allows the DC bus to draw more power than the nominal power. This capability allows capacitor or other storage elements to be recharged more quickly than they are discharged. In fact, they discharge by feeding loads while the bus is down and they have to supply power until the power start coming from the main converter. Being the energy used to supply loads equal to the energy the main converter has to replace (except losses), the recharge of capacitor can be faster that their discharge only if the recharge power is bigger than the nominal one.

$$E_{charge} = E_{discharge}$$

$$P_{charge} \cdot t_{charge} = P_{discharge} \cdot t_{discharge}$$

$$t_{charge} = \frac{P_{discharge}}{P_{charge}} \cdot t_{discharge}$$

Under the hypothesis to have the same voltage during the discharge and the recharge:

$$t_{charge} = \frac{I_n}{I_{MAX}} \cdot t_{discharge} \quad (9)$$

Where I_n is the nominal current and I_{MAX} is the overload current allowed by the main converter.

The discharging time corresponds at the time that loads need to be supplied by hold-up capacitors. Thus, the charging time is part of the discharging time:

$$t_{discharge} = t_{hold-up} = t_{de} + t_{cont} + t_{charge} = t_1 + t_{charge}$$

$$t_{charge} = \frac{t_{de} + t_{cont}}{\left(\frac{I_{MAX}}{I_n} - 1\right)} \quad (10)$$

$$t_{hold-up} = \frac{t_{de} + t_{cont}}{\left(1 - \frac{I_n}{I_{MAX}}\right)} \quad (11)$$

Table 10 shows some example of hold-up time and charge time for different overload capability of the main convert ($t_1 = t_{de} + t_{cont}$).

Table 10 - Hold-up time and charge time dependence on the overload capability of the main converter

Imax/In	t_1 [ms]	thold-up [ms]	tch [ms]
1.2	1.6	9.6	8.0
1.3	1.6	6.9	5.3
1.4	1.6	5.6	4.0
1.5	1.6	4.8	3.2
1.6	1.6	4.3	2.7
1.7	1.6	3.9	2.3
1.8	1.6	3.6	2.0
1.9	1.6	3.4	1.8
2	1.6	3.2	1.6
3	1.6	2.4	0.8
4	1.6	2.1	0.5

4.1.5 Cable length, fault distance and impedance

The cable length and the distance of the fault from the main converter influence not only the de-energizing process without the power sequencing, as shown in Chapter 3.

The duration of the current peak due to the discharge of the output capacitor is also influenced, and thus, also the performance of the protection strategy.

Figure 38 shows the dependence of the current peak duration (t_{de}) on the distance of the fault from the main converter. There is a parallel relationship between the current peak duration and the fault distance.

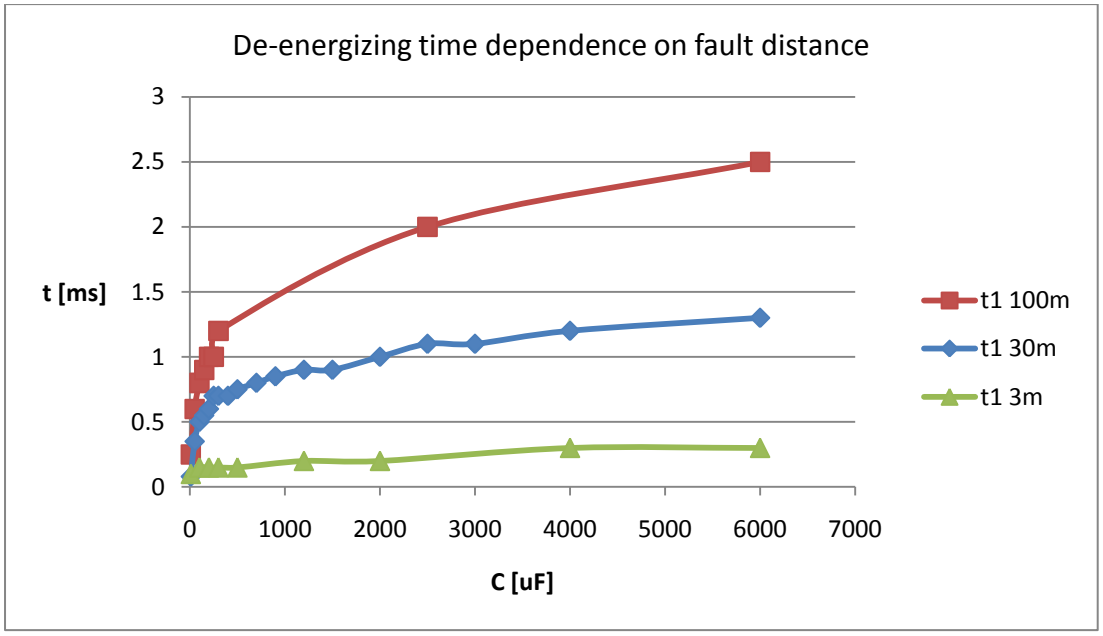

Figure 38 - De-energizing time dependence on the fault distance from the main converter

The impedance of the contact due to a short circuit or a ground fault influence both the fault current and the duration of the protection process. For most of simulations, we adopt as a fault impedance an equivalent resistance of the short circuit fault:

$$R_f = 0.02\ \Omega$$

This equivalent resistance can cause a short circuit current of 50 kA, that is big enough for such a system, and it allows us to carry out Simulink simulations without memory and time problems.

The variation of the fault impedance influence slightly the performance of the protection process, as shown in Figure 39 for bus length of 100 meters. In fact, the duration of the current peak, that corresponds to the de-energizing time for the power sequencing, varies between 0.2 and 1 ms.

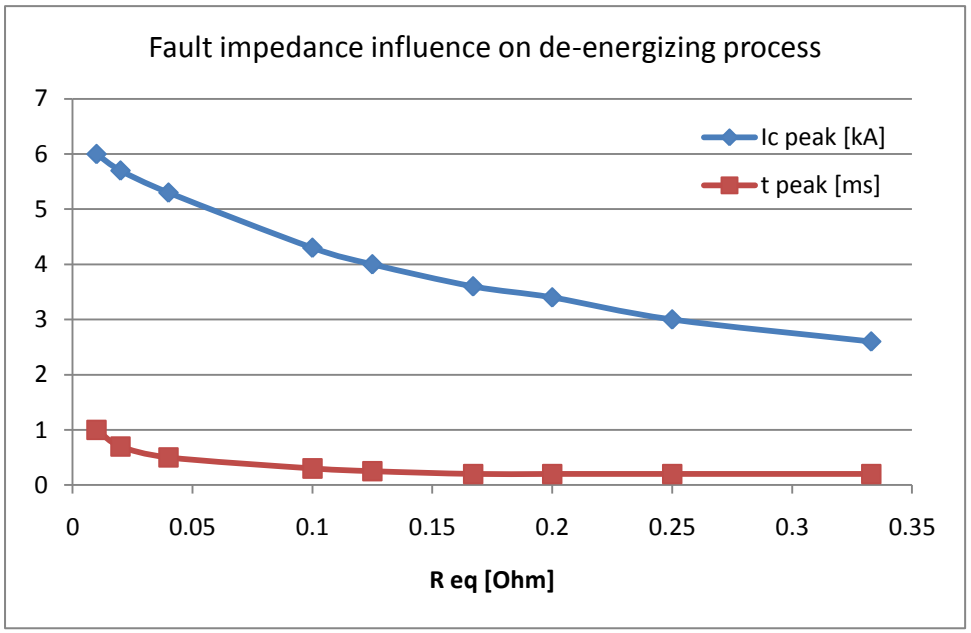

Figure 39 – Fault impedance influence on the de-energizing process

For small fault impedance, the consideration done before are valid. For big fault impedance the fault becomes less dangerous and the protection process is advantaged.

4.2 Influence of the de-energizing time on the whole process

Components and characteristics observed above influence directly the de-energizing time of the DC bus and indirectly the duration of the entire process including the reconfiguration and the re-energizing of the DC bus. The longer is the time to eliminate the fault, the longer is the time in which hold-up capacitors have to supply loads of unfaulted branches, and the longer will be the time that the main converter needs to recharge the discharged output capacitor and hold-up capacitors.

The entire process time includes the time necessary to eliminate the fault (t_{de} + t_{cont}) and to re-energize the DC bus (t_{re}).

$$t_2 = t_{de} + t_{cont} + t_{re} \quad (12)$$

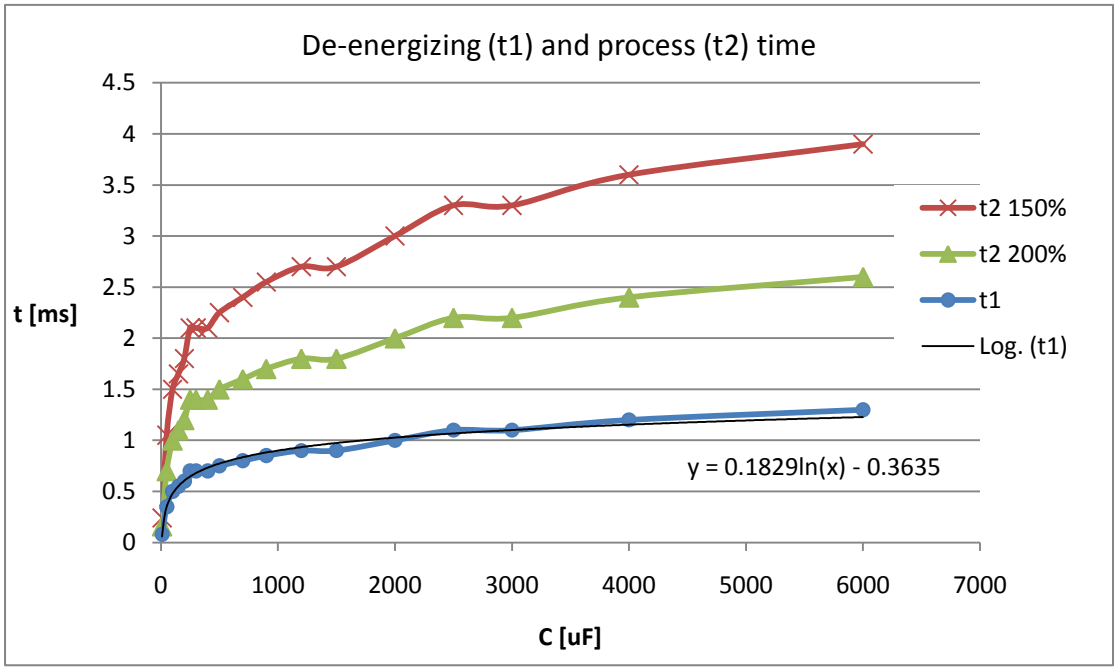

Figure 40 - System response dependence from the size of the output capacitor

A good approximation on the re-energizing time is the time to recharge the storage elements (capacitors and hold-up capacitors). Figure 40 shows how the time to isolate the faulted line (t_{de} + t_{cont}) and the entire process time (t_2) depend on the size of the output capacitor and the overload capability of the main converter (150% *Pn*, 200% *Pn*), for a cable length of 30 meters.

4.3 Simulation of the 1MW DC bus with the controlled power sequencing

We have studied the performance of the protection system, and how the performance depends on system parameters, using a 1 MW – 1kV system as our reference. Converters and bus parameters used in Simulink simulations are presented in Chapter 2.

Simulations of a multi-branches DC bus supplied by a 1 MW – 1kV main converter show how the protection process operates and the capability for unfaulted lines to ride through the process uninterrupted.

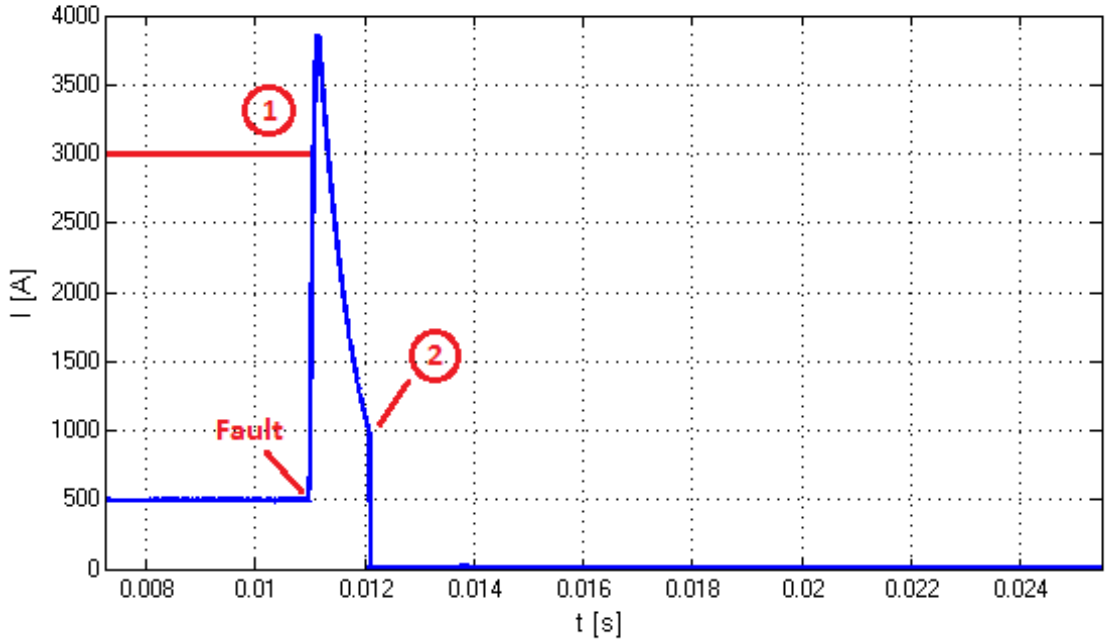

Figure 41 - Current of the faulty branch

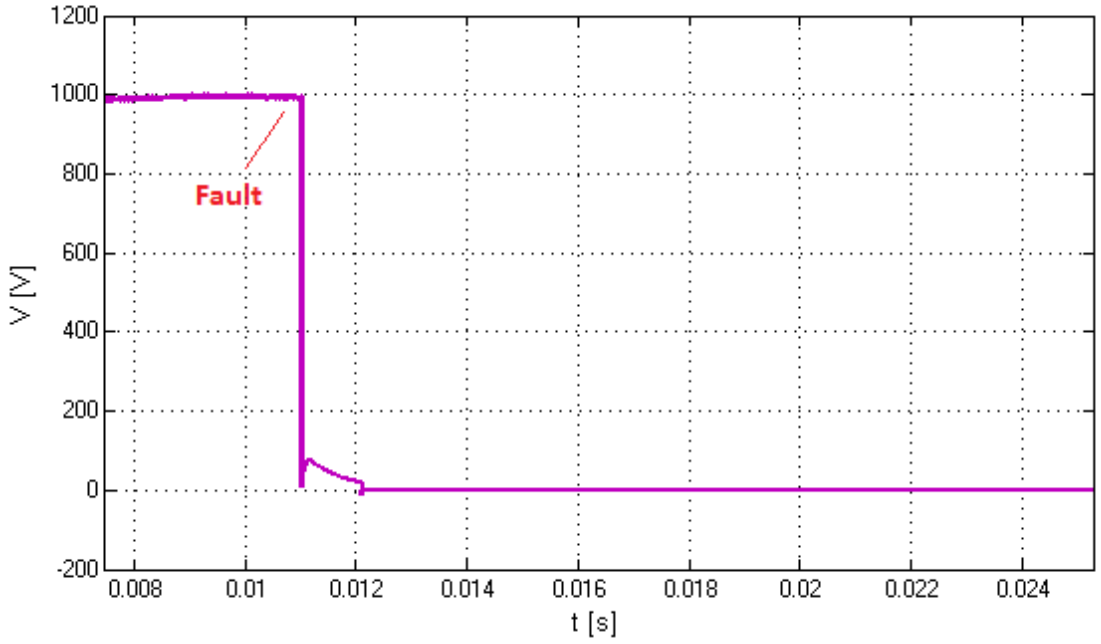

Figure 42 - Voltage of the faulty branch

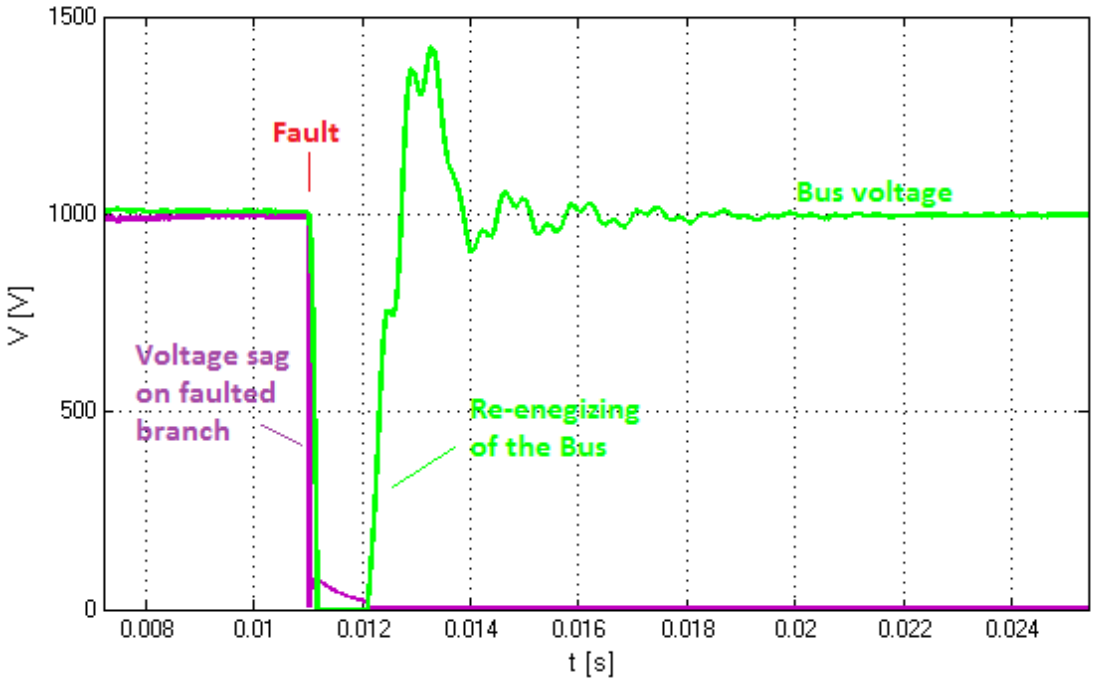

Figure 43 - Voltage of the faulted branch and voltage of the main Bus

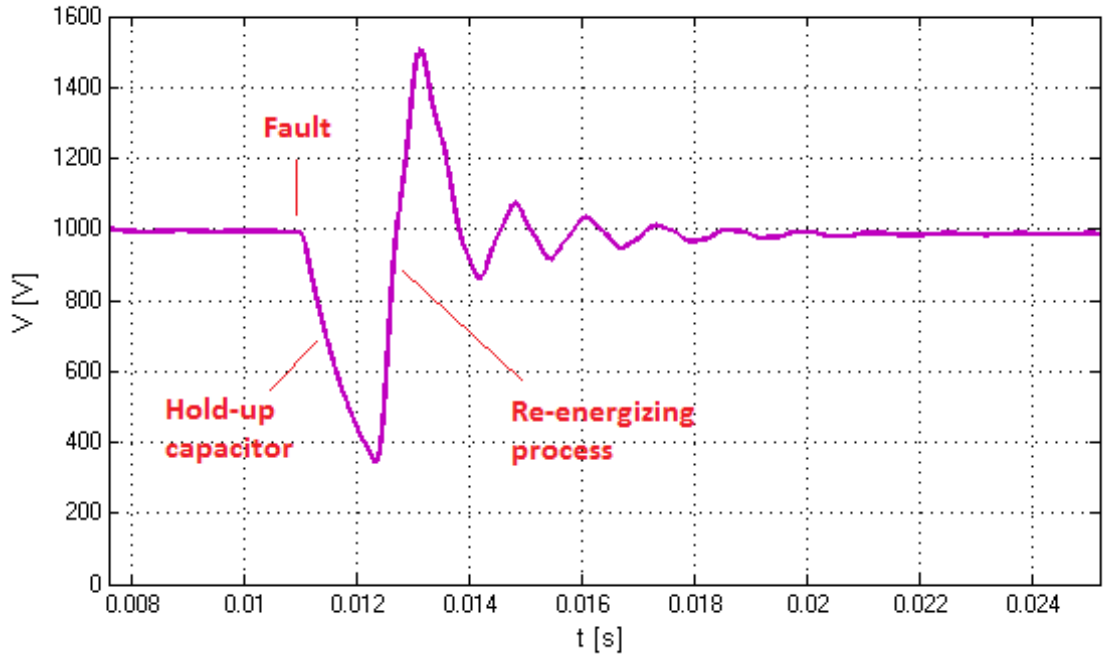

Figure 44 - Voltage of the healthy branch

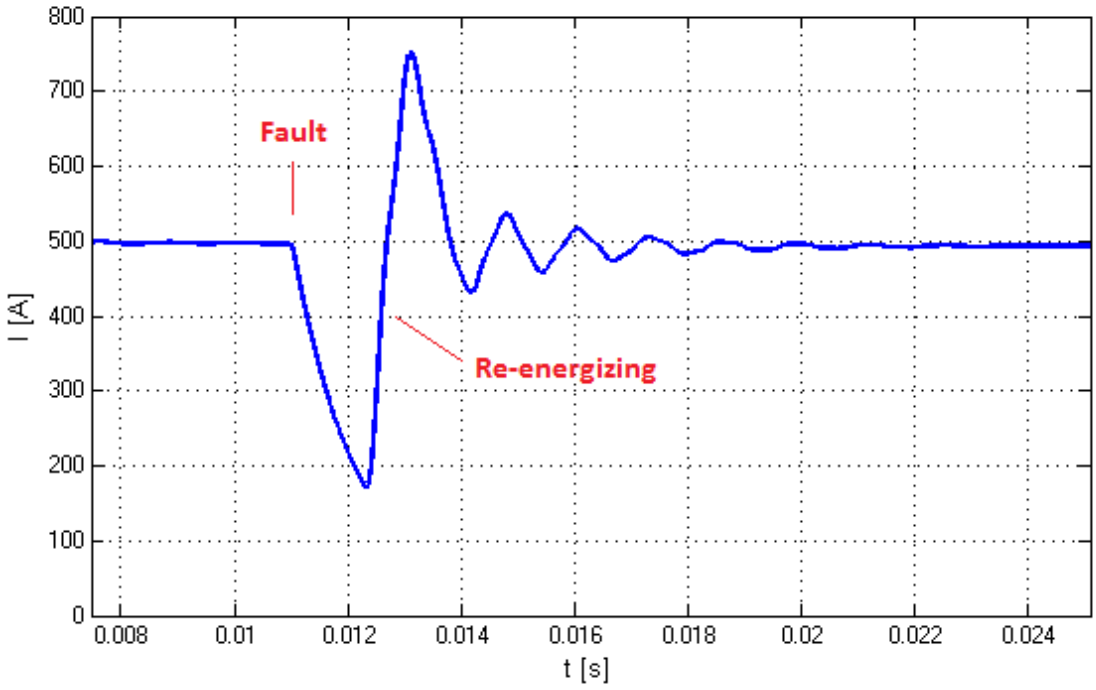

Figure 45 - Current of one of the unfaulted branch

Figure 41 and Figure 45 show the behaviors of currents in the faulty branch and in one of the unfaulted branches respectively. A line-to-ground fault happens at t = 0.011s. After detecting the fault at time *point 1* the control turns off the main converter and, at time *point 2*, it isolates the faulted circuit by means of SW3 as soon as the current falls under the rated opening current of the contactor. Figure 42 shows the voltage on the faulty line, while Figure 43 illustrate the comparison between the voltage of the faulted branch and the voltage of the main bus. Figure 44 shows that the voltage at a load served by a healthy line does not drop immediately but with a time depending on the size of the hold-up capacitor and the power demand of the load. As soon the fault is eliminated, the re-energizing process begins (t = 0.0125s). For simplicity regarding system stability and amount of memory available on the computer, we ran simulations regarding the whole process by supplying resistive loads on healthy lines. For simulations regarding the feeding of loads from hold-up

capacitor, we used constant power load models to simulate controlled DC/DC converters that supply loads.

Summary

From this parametric study we are able to understand which are the most influent components on the performances of the protection strategy:

- Output capacitor of the main converter
- Type of contactors
- Overload capacity of the main converter
- Fault distance from the main converter.

Figure 46 shows a comparison between eliminating a fault by using the controlled power sequencing, by simply controlling the main converter, and by utilizing traditional circuit breakers.

Providing important information for the design of the fault protection by using the proposed power sequencing is another purpose of this chapter. In fact, we showed how to achieve specified reaction times of the protection scheme for a wide range of converters and bus configurations.

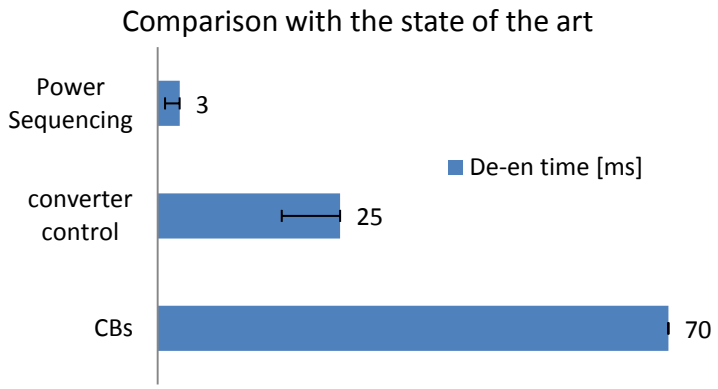

Figure 46 - Comparison with the state of the art

5. Contactors and Hold-up capacitors

Contactors and hold-up capacitors are elements that take an important place in the protection system design, and in the trade-off between cost and performances. For this reason we are going to discuss the choice of these components.

5.1 Contactors

Contactors or switch disconnectors were used to isolate sections of the DC bus when the current was already interrupted by circuit breakers. Although these contactors were already part of the DC system, they usually are very slow components compared to circuit breakers and other protection devices because they operate without current and they don't need to open a fault current. With the introduction of the new approach to protect a DC bus, contactors assume a new function and they participate at the protection process. For this reason, the opening time of contactors weighs upon the complete protection cycle. More than one technology can be used to carry out this task, everyone with its advantages and disadvantages. In the next paragraphs we presented three different solutions: mechanical contactors, solid state switches, hybrid contactors.

5.1.1 Mechanical contactors

In the wide range of mechanical contactors, we have considered the fastest that are usually used in the field of electric traction vehicles that work in DC in many countries. They are particularly suitable for propulsion main circuit (line contactor, pre-charging contactor, main converter isolating contactor). We take as example the Secheron SEC contactor that has the following characteristics:

- Operation voltage rated 900V to 4000V DC
- Rated thermal current up to 1300 A

- Designed for heavy operational frequencies
- Opening time τ = 15 ms

In this case, we have a very robust device with the capacity to endure to overvoltage and overcurrent, and to tolerate high fault current for a limited duration of time [36].

The main disadvantage of mechanical contactors stay in the opening time. An opening time of 15 ms is excellent for normal tasks in a DC system, but it is problematic in the controlled power sequencing cycle. As a matter of fact, a 15 ms opening time can lead the entire cycle duration from 3-6 ms to 21-50 ms. Figure 47 illustrates an example of mechanical contactor that can be used for our applications, dimensions are showed in mm.

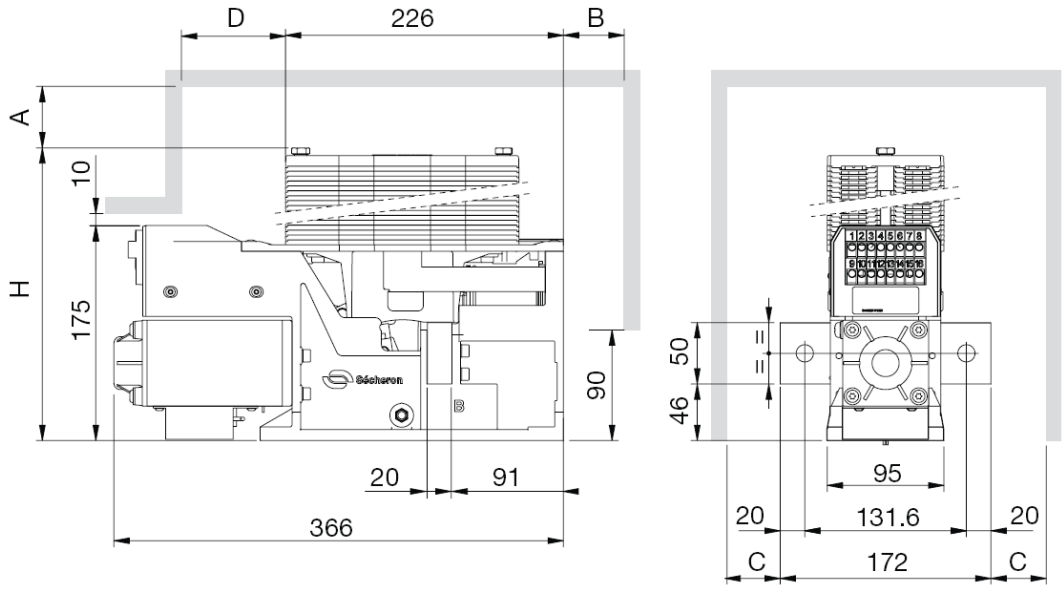

Figure 47 - SEC contactor, dimensions in mm

5.1.2 Solid state switches

The main reason we consider solid state switches is because of the extreme high operation speed compared with moving contacts. The combination of a solid state switch with a snubber allows to open a circuit operating at the nominal current in 10-

100 μs. The total extinguishing depends also on the kind of snubber we use to limit the voltage on the switch, but it remains fast enough. The two main drawbacks of employing solid state switches to isolate faulted branches of the bus are:

- Conduction losses during normal operations (e.g. feeding loads at the nominal current), that are much larger than conduction losses in a contactor;
- Incapability to withstand to high fault currents for a short time.

There is also a further problem due to the safety isolation function of a normal contactor that a solid state switch cannot have. This last problem can be easily resolved by adding some additional device, such as a switch disconnector, with the only task to separate physically the faulted line.

Example of solid states switch that can be used for such application are IGBTs and gate turn-off thyristors (GTO, ETO, IGCT) [27].

5.1.3 Hybrid contactors

The hybrid contactor is a solution that gets into the trade-off between opening speed, physical withstand and losses.

Figure 48 shows the limitations of mechanic contact opening time regarding the semiconductor commutation performances.

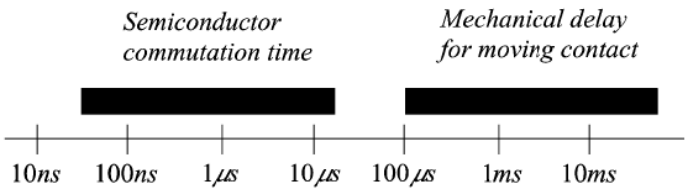

Figure 48 - Typical reaction time for semiconductors and mechanical contactors

Classical mechanical contactors have a very small contact resistance (a few micro-Ohms) in the closed position, and represent a galvanic separation in the open state. However, these devices have a long reaction time due to the need of blowing the arc

in a arc chute. Arc occurrence leads to contact erosion and, consequently, a short lifetime and high maintenance costs. On the other hand, power semiconductors device provide a fast acting arcless interruption with high reliability and reduced maintenance, but they suffer from high on-state losses and a low thermal capability of the silicon wafers. As a result, large transient overcurrents or high-rated currents are not permitted even if effective cooling is implemented.

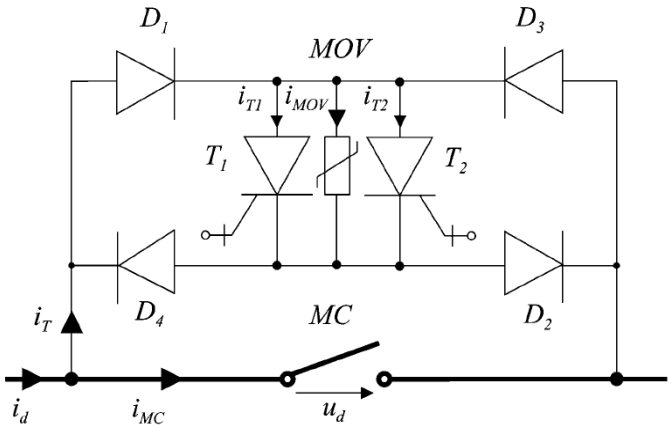

Figure 49 - Basic configuration of a hybrid contactor

The integration of both mechanical contactor and static switch allows a combination of the former's current carrying function and the latter's high-speed arcless interrupting characteristic. In order to keep the benefits of static interruption, an ultra-fast contact opening is required [37]. Figure 49 shows an example of hybrid contactor. It consist of a mechanical contact and a bidirectional static cell with two high power IGCTs connected in parallel, four diodes in a rectifier scheme, and a metal-oxide varistor (MOV) element. The diode bridge configuration allows this contactor to be used for both current directions in DC systems. In case of short circuit individuation, the opening signal acts on the moving contacts, and, at the same time, as a turn-on signal for IGCTs. Contact separation occurs after a reaction time Tm.

Then, a small arc discharge is drawn between the contacts after separation and an arc voltage appears. This arc voltage acts as a commutation voltage in the circuit

comprising the diodes D_1 and D_2, and also the two IGCTs T_1 and T_2. The current is rapidly and totally directed to the power electronic path. After the time T_{cond}, when the distance of between contacts is sufficient (total recovery of the dielectric strength), the IGCTs interrupt the fault current upon receiving a turn-off signal. Energy remaining in the circuit is absorbed by the MOV during the time T_a. Figure 50 illustrates the opening sequence of an hybrid contactor. With this solution, the time T_{lim} from the short-circuit detection to current limitation is less than 300 µs.

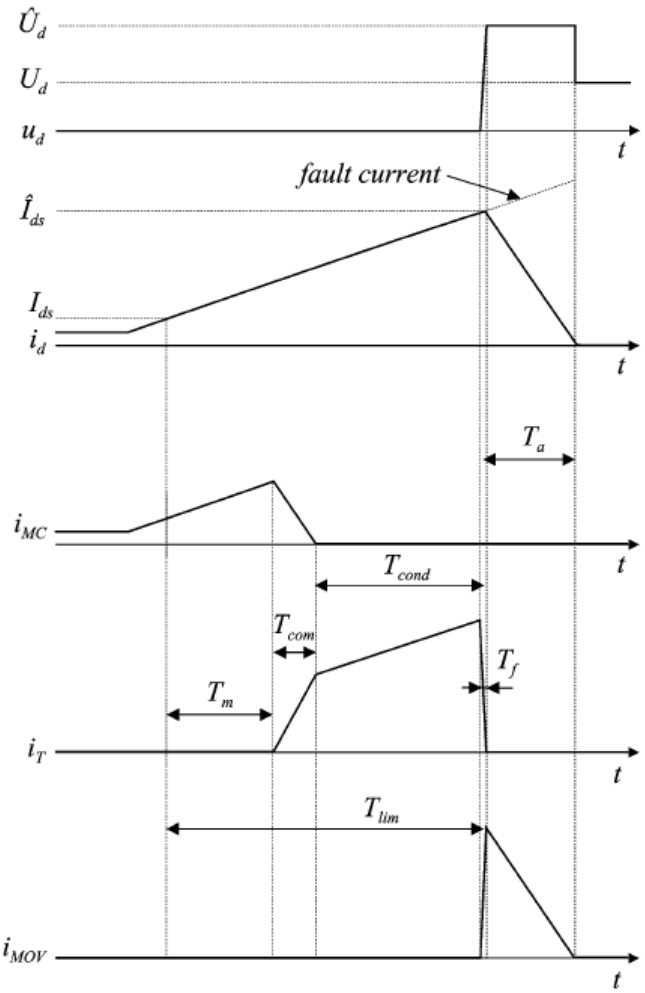

Figure 50 - Main waveforms during the opening sequence of the IGCT hybrid breaker

5.1.4 Summary

As already stated, the opening time weighs on the de-energizing and on the whole protection process. Figure 51 shows the comparison of the three type of contactor we have considered.

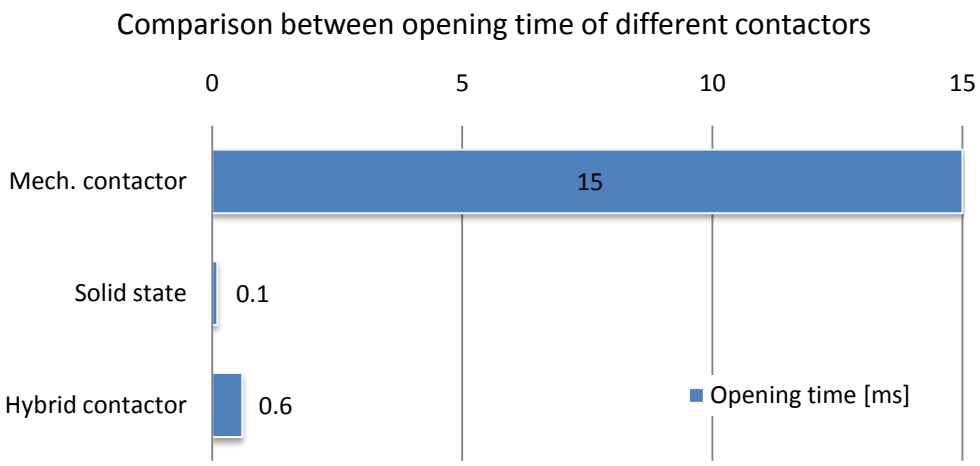

Figure 51 - Opening time of different type of contactor

Mechanical contactors are commonly used, but they need a considerable time to open a faulted circuit. They can be bought for 2000-3000$. Solid state based contactors are very fast but they are strongly limited by their on-state behavior. An IGBT for such a system can be bought for 300$, without considering the cost of the snubber. A good compromise is reached by the hybrid contactor which has good opening speed and good on-state performances.

5.2 Hold-up capacitors

Another important challenge in DC system protection is introduced by storage elements directly connected to the DC bus, such as hold-up shunt capacitors. On one hand shunt capacitors allow energy storage and bus voltage smoothing, on the other hand, under fault conditions, these capacitors discharge a high amount of energy in extremely short time, into the fault through the bus. This high discharge rate may cause electromagnetic as well thermal and mechanical damage to the system components. Typically RL snubbers are provided to divert the energy and reduce the discharge rate, thereby reducing the damage caused by shorting of the shunt capacitors during faults. The main drawback of using snubbers for capacitor protection is that energy stored in the capacitor is dissipated, and thus wasted, in the snubbers. The dissipation requires high thermally rated snubber components, making them bulky. Another drawback of dissipating shunt capacitor energy is the delay caused by the recharge of these capacitors during restart operation of the DC bus.

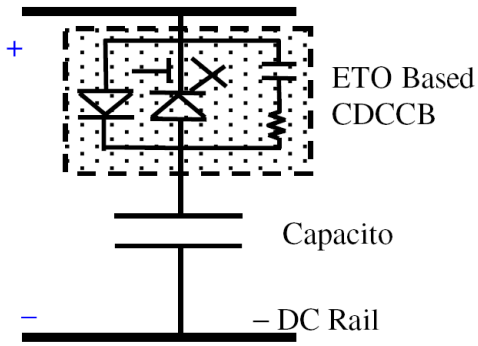

Figure 52 - ETO based device scheme

One solution is protecting shunt capacitors by means of a solid state switch based device able to isolate the capacitor. One example is a Emitter Turn Off (ETO) thyristor based device, located between the capacitor and the positive DC bus rail (Figure 52). This device is able to turn off the capacitor current and isolate the shunt

capacitor in less than 10 μs up to a current of 4kA and DC bus voltage of 4kV [24],[27].

Another solution is to insert hold-up shunt capacitors in the upstream side of each converter. In this way the capacitor discharge is controlled by converter switches and can be limited by the converter control. For this reason we position hold-up capacitor in the upstream side of each converter of our system as shown in Figure 2 and Figure 53.

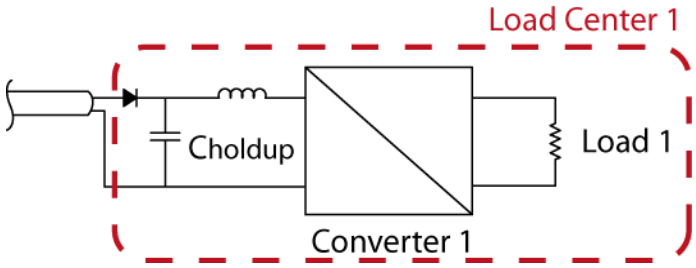

Figure 53 – Position of the hold-up capacitor in a load zone

5.2.1 Sizing of hold-up capacitors

The previous chapter illustrates how performances of the protection system depends on system components and give foundations for design of hold-up capacitors that allows the unfaulted circuits to ride through the process uninterrupted.

The size of this kind of capacitors is strongly dependent on the energy that the system needs to ride through. This energy depends most of all on:

1) Time in which the bus is down, that is composed by de-energizing time, opening time, re-energizing time
2) Power demand of loads
3) Overload capability of the main capacitor

As seen in 4.1.4 the time in which the capacitor has to supply energy to the load $t_{hold\text{-}up}$ is given by the following expression:

$$t_{hold-up} = \frac{t_{de} + t_{cont}}{\left(1 - \frac{I_n}{I_{MAX}}\right)} \quad (13)$$

Where t_{de} is the de-energizing time, t_{cont} is the time that the contactor need to remove the faulted line, I_n the nominal current and I_{MAX} the maximum current the converter can deliver. The energy supplied from the capacitor E_C will be:

$$E_C = P_{load} \cdot t_{hod-up} \quad (14)$$

Where P_{load} is the power absorbed by the load or by the converter between the hold-up capacitor and the load. The capacitance of the storage element will be:

$$C_{hold-up} = \frac{2 \cdot P_{load} \cdot t_{hold-up}}{V_n^2 \cdot 0.7} \quad (15)$$

V_n is the nominal voltage of the converter and 0.7 is factor to maintain a safety margin as illustrated later in 5.2.2.2.

For example for a branch with a converter that supply a 10kW load or a 50kW load:

Table 11 – Size of hold-up capacitors depending on the overload capability of the main converter

Imax/In	thold-up [ms]	Chold-up 10kW [µF]	Chold-up 50kW [µF]
1.2	9.6	274	1371
1.3	6.9	198	990
1.4	5.6	160	800
1.5	4.8	137	686
1.6	4.3	122	610
1.7	3.9	111	555
1.8	3.6	103	514
1.9	3.4	97	483
2	3.2	91	457
3	2.4	69	343
4	2.1	61	305

Being the hold-up time related to the overload capability of the main converter, there is a trade-off between the request of high performance of the main converter and size of the capacitors.

5.2.2 Characteristics of hold-up capacitors and Cycle efficiency

5.2.2.1 Modeling of capacitors for power electronics applications

Electrical characteristics at the terminals of an actual capacitor are quite different from those of an ideal capacitor. Several resistive components appear in the current path of the device, depending on the kind of capacitors, giving rise to an equivalent series resistance (ESR). The simplest model for the device is therefore the one in Figure 54 [38].

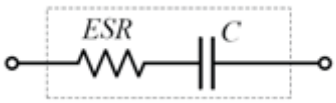

Figure 54 - Single R-C model for an actual capacitor

Deeper investigation on the physical structure of the device, taking into account the distributed nature of the resistance and capacitance of the porous electrode, suggests a more refined model made up of cascaded R-C pairs, as shown in Figure 55. Such a model can be experimentally verified by executing spectroscopic analysis of the terminal impedance. Results are schematically shown in Figure 56 and can be synthesized as follows:

- At very low frequency (less than about 1 Hz), the impedance is reasonably well described by a simple R-C series network with constant values of both capacitance (the DC-capacitance) and resistance (the DC-ESR).
- At relatively high frequency (above about 100 Hz), the capacitance is reduced to a very small fraction of its DC value, and the component behavior is

essentially resistive, with a “high frequency” ESR that is smaller than the DC-ESR.

- At intermediate frequency, both ESR and equivalent capacitance increase with decreasing frequency, giving rise to the distinctive 45 degree-slope region in the complex impedance plane.

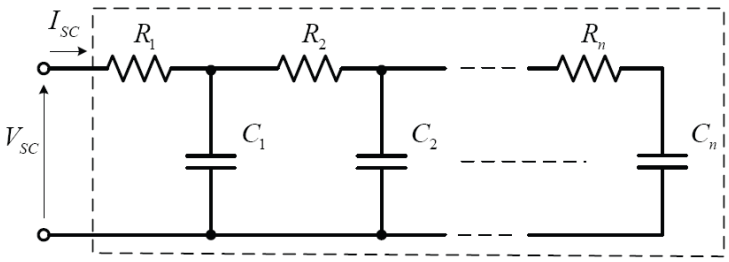

Figure 55 - Cascaded R-C model for an actual capacitor

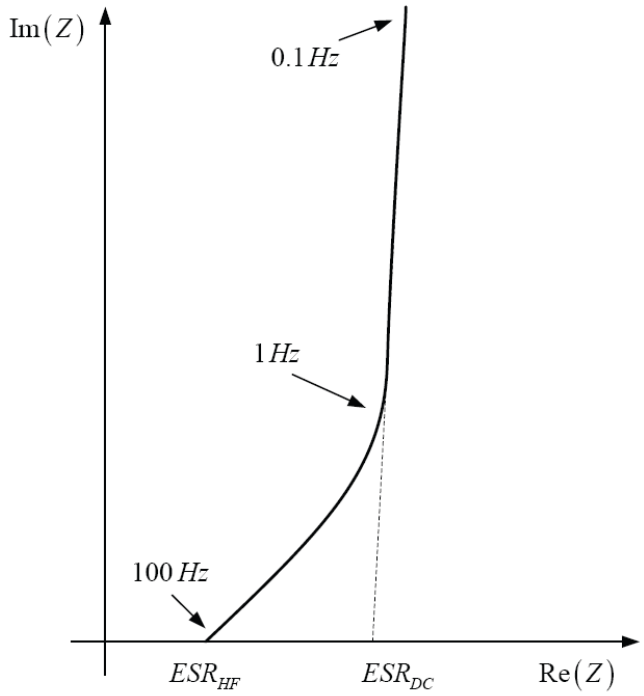

Figure 56 - Schematic representation of Nyquist impedance plot of a typical capacitor cell

We are actually interested in a low frequency use of capacitors, thus, the simple R-C series is reasonably adequate.

5.2.2.2 Evaluation of losses in hold-up capacitors

Electrical resistivity of electrodes in a capacitor is not zero; also, losses are generated in the electrolyte. A general expression for the losses is quite involved and depends on the actual voltage distribution inside the device. According to the previous paragraph, an equivalent series resistance (ESR) is associated to the capacitor; such a resistance is assumed to be constant with voltage and frequency.

The amount of energy dissipated into the ESR of the shunt capacitors is expressed as:

$$E_{loss} = \int_0^T I_C^2 \cdot ESR_C \cdot dt \tag{16}$$

The efficiency of the energy extraction from the hold-up capacitor can be calculate as:

$$\eta = \frac{E_{dis}}{E_{dis} + E_{loss}} \tag{17}$$

We considerate some different type of capacitors, such as:

1) Polypropylene Film Capacitors (*NEW! – Digikey*)
2) Snap-in capacitors (*Tecate Group*)
3) Aluminum capacitors (*Tecate Group*)
4) Double layer super capacitors (*Maxwell Technologies*)

Table 12 - Evaluation of losses and efficiency for different kind of capacitor

	Film	Snap-in	Aluminum	Double layer
Nominal voltage [V]	1200	450	200	125
Series	1	3	3	10
ESR [Ohm]	0.0034	0.6	2.49	0.018
TOT ESR [Ohm]	0.0034	1.8	7.47	0.18
Capacity max [uF]	470	330	100	6.30E+07
TOT Capacity [uF]	470	110	33.3	6300000
Power Losses (100A) [W]	34	18000	74700	1800
Power (100A) [W]	100000	100000	100000	100000
Efficiency	0.99	0.85	0.57	0.98

These type of capacitors have different characteristics. That concerned the evaluation of losses are the different ESR of each capacitor as shown in Table 12.

Being the considered operation time the same for losses and power supplied by capacitors, the efficiency can be found as following:

$$\eta = \frac{P_{dis}}{P_{dis} + P_{loss}} \tag{18}$$

Where P_{dis} is the power supplied to loads and P_{loss} is the power lost during the energy extraction from capacitors.

It comes out that the energy extraction efficiency is between 60% and 99%, depending on the type of capacitor that we use as a hold-up capacitor. The energy extraction efficiency can be improved by reducing the ESR of the capacitor by putting more capacitors in parallel.

Another reason to put more capacitors in parallel is the enhancing of the capacitor available energy, and thus, the capacitor battery capacity. In fact, the available energy in a capacitor is around 80-90% because a converter can't operate when the input voltage go down under a specific threshold. If we look at a converter as a constant power load, if the input voltage goes down the current goes up. The point in which the voltage starts going rapidly down and the current rapidly up is around the 10-20% of the charge of the capacitor. Figure 57 shows the behavior of voltage and current of the capacitor during the feeding of the converter. Around 90% of the capacitor charge the voltage starts going down faster and the current starts going up rapidly.

We fix 30% of the capacitor charge as a threshold with a safety margin to assure the reliability of energy extraction from hold-up capacitors.

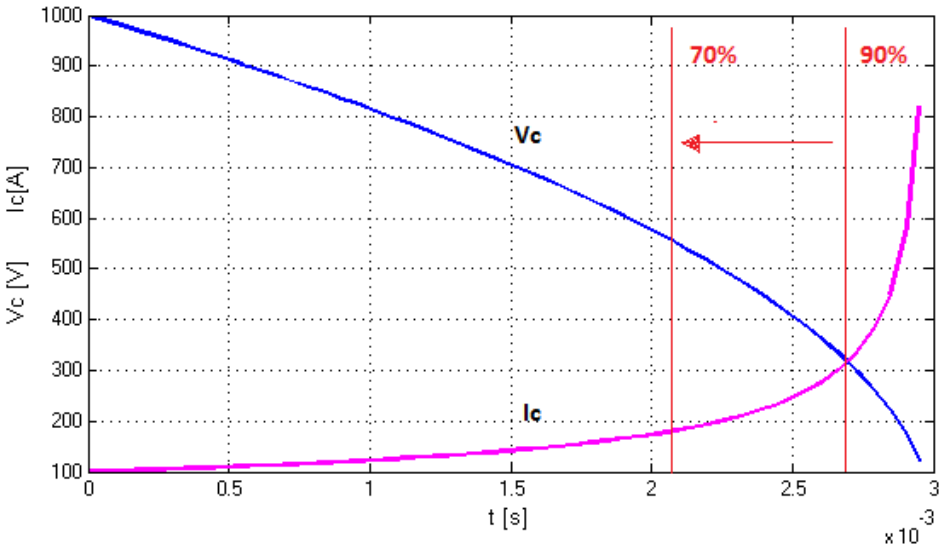

Figure 57 - Hold-up capacitor discharge by feeding a constant power converter

Conclusion

A solution for protecting DC systems against ground and line faults has been presented. We demonstrated how it is possible to replace traditional circuit breaker in a MVDC system with a controlled power sequencing and a reconfiguration of the bus. For a typical industrial DC bus, we showed that is possible to execute this de-energize-reconfigure-re-energize process 10 times faster than a traditional AC bus can be protected and reconfigured.

Fault dynamic and bus de-energizing process on a 1kV-1MW DC distribution system were analyzed utilizing Simulink simulations.

We explained how the de-energizing and reconfiguration time depend mainly on the output capacitance of the main converter, on the distance of the fault from the main converter, and on the overload capability of the main converter. Moreover, we gave some considerations about the influence of the performances of different kind of contactors on the protection process. Finally, we showed how to size each hold-up capacitor so as to permit loads on unfaulted circuits to ride through the process uninterrupted.

We illustrated how to achieve specified reaction times of the protection scheme, and for which range of parameters we are able to obtain the best performances.

Our study provides essential guidelines for design of fault protection for DC power systems using the presented controlled power sequencing.

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Appendix

Simulink Scheme used to simulate the line fault on branch 1 of the DC bus.