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Electronical instrumentation for impedance measurement on biosamples

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Abstract

In the last years electronical systems entered with great importance in the measurement of biological quantities, granting access to information from electrical cellular characteristics: it is in fact possible to measure capacitance or conductance that are dependent on the health state of cells and can be used to perform drug testing. In addition, lab-on-a-chip systems are attracting a growing attention for the possibility of parallelization and portability of biological assays, but they require sensitive and compact electronic measurement systems to be developed, in order to realize instruments that can be utilized also by people outside a biological laboratory, reaching what is called point-of-care diagnostic.
To support on-chip electrobiological measurements, during this research, the development of highly sensitive, economical and compact instruments to detect impedance of biological samples has been explored.
A first part of the research dealt with discrete systems development, with the focus of obtaining high sensitivity, while keeping the system compact, low-cost and low-power.These constraints have been considered while designing an handheld impedance based cell counter, that has been used to replace fluorescence-based detection in a dielectrophoretic separation experiment.
The need for increased flexibility and compactness, then, lead to the design of a fully integrated chip for impedance measurement with two phases lock-in to obtain magnitude and phase information about the impedance. The challenges in this kind of design are to obtain good performances even with standard, low-voltage and low-cost technology; the design techniques used to solve them are presented in this work.
Finally a new circuital topology will be explored to increase the impedance measurement bandwidth over the usual range of operational-amplifier based transimpedance amplifiers. Exploiting modulation and demodulation, together with feedback we can achieve bandwidth bigger than $100MHz$ with good linearity.

Riassunto

Negli ultimi anni i sistemi elettronici sono entrati con molta importanza nelle misure di quantitá biologiche, fornendo accesso ad informazioni derivate dalle caratteristiche elettriche delle cellule: é infatti possibile misurare capacitá o conduttanze che sono dipendenti dallo stato di salute delle cellule e che possono essere usate per effettuare screening farmacologici. Inoltre i sistemi lab-on-chip stanno attraendo sempre maggiore attenzione dal momento che offrono parallelizzabilitá e portabilitá degli esami biologici, ma richiedono sistemi di misura elettronici ad elevata sensibilitá e compattezza per realizzare strumenti utilizzabili anche da persone al di fuori di un laboratorio e realizzare ció che si chiama diagnostica point-of-care.
Per supportare misure elettrobiologiche su chip, durante questa ricerca, é stato esplorato lo sviluppo di strumenti per la misura di impedenza che fossero sensibili, economici, compatti ed adattabili a campioni biologici.
La prima parte della ricerca si é occupata di sviluppare elettronica a componenti discreti, con l'obiettivo di ottenere un'elevata sensibilitá, mantenendo il sistema compatto, a basso costo e bassa potenza. Questi vincoli sono stati presi in considerazione nella realizzazione di un contatore di cellule portatile e basato sulla misura di impedenza, che é stato utilizzato per sostituire strumenti basati su fluorescenza in un esperimento di rilevamento seguente una separazione dielettrica delle cellule.
La necessitá di maggiore flessibilitá e compattezza, ha quindi spinto al progetto di un chip totalmente integrato per misure di impedenza con lock-in a due fasi per ottenere contemporaneamente le informazioni su modulo e fase dell'impedenza misurata. Le difficoltá di questo tipo di progetto, riguardanti la difficoltá di realizzare sistemi complessi con tecnologie standard e a basso costo, sono state risolte con particolari topologie circuitali che sono presentate in questo lavoro.
Infine verrá presentata una nuova topologia circuitale mirata ad aumentare l'intervallo di frequenze ove é possibile la misura di impedenza oltre il limite imposto dalla struttura a transimpedenza basata su amplificatori operazionali. Sfruttando la tecnica di modulazione e demodulazione, unita alla retroazione,

é stato possibile estendere la banda oltre i $100MHz$, mantenendo un'ottima linearitá.

Chapter 1

Introduction

In this chapter some example of application of impedance measurement on biosamples will be presented together with the description of the most used techniques to detect it, with a particular attention to the ones that can be used for wide range impedance detection.

1.1 Impedance Biosensors

Many processes that happen in biological samples modify the electrical behavior of the sample itself and can be investigated using electrical measurement techniques. The electrical measurement has the advantage over the classical optical observation to require an instrumentation that is generally less sophisticate, bulky and expensive; moreover, the integrated electronic technology allows the realization of inexpensive arrays of electrodes that can perform multiple parallel measurement, thus reducing biological investigation time and opening the possibility to realize hand-held instrumentation for blood analysis, cell culture, smell measurement and DNA sequence detection.
Most of the interest in this field is in affinity biosensors that are sensors in which an immobilized biological receptor molecule reversibly detects binding with a ligand [1]. The transduction of the reaction to an electrical signal can be detected using different detection schemes: a direct one is electrochemical while some indirect ones are optical, calorimetric or piezoelectric. In our case the main focus will be on the first one.
Various electrical measurements can be performed on biosamples to study their characteristics, including cyclic voltammetry, amperometry and impedance spectroscopy. The first one is the application to the sample of a triangular voltage waveform with contemporary current reading. The result of this measurement can be plotted on an I/V graph from which it is possible to reveal

the presence of ions and their concentration, by analyzing the voltage and the amplitude of current peaks [2]: when the voltage of the electrode is near to the oxidation or reduction potential of one molecule present in the solution, it causes a neat current flow that reveals information both on the nature and on the concentration of the molecule itself. This is going to be exploited for instance to detect dopamine release by stem cells to monitor their differentiation in an innovative european project [3].
With amperometry it is possible to detect current variations over time that can, for instance, be used to gain insight on the flow of ions in cell membrane ion channels [4]. This is both a means to study the electrophysiology of the cell and a recommended test for screening new drugs [5].
Finally with impedance spectroscopy it is possible to characterize the linear electrical behavior of the system under test to measure variations in conductivity or dielectric constant due to morphological changes. This technique can be used for example to probe the system during electrode functionalization or to directtly read [6]. In the first case impedance measurement can monitor the thickness and the goodness of the functionalization layer, while in the second it is directly used to read the sensor. The second use is the most promising for biological and medical application and many projects to exploit it are active: in the European project Bioelectronic Olfactory Neuron Device (BOND), the goal of a bionic nose is pursued by mounting mammalian olfactory receptors on nanoelectrodes [7]; flow cytometry integrated on a microfluidic device will be presented on chapter 2, and also DNA hybridization can be sensed with this technique [8].

1.1.1 Electrical models

One important aspect of electrical measurement on biological samples is that they generally must be performed in liquid environment to preserve the functionality of the involved elements (enzymes, antibodies, cells...). In most cases, the medium used for this goal is Phosphate Buffered Saline (PBS), a water-based solution containing salts that help maintaining a constant pH, while in some case the medium also contains nutrients, drugs or other chemicals. The presence of the liquid during the measurement must be correctly modeled: in this way it is possible both to study the interface using electrical measurements and to remove its effect when the system under test is not the interface itself. A complete model of the interface should take into account various phenomena happening between ions dissolved in liquid and the metal and can be found in [9], in any case simpler models can be used in specific situations.
One of the dominant phenomena appearing at the liquid to metal interface is the formation of a double layer of charges that can be modeled as a ca-

pacitance, commonly known as double layer capacitance (C_{dl}). For PBS, the specific capacitance lies in the range of $10 \sim 20\ \mu F/cm^2$. Other processes happening at the interface, known as faradaic ones, include the charge transport across it and their simplest model is a resistance in parallel with the double layer capacitance.
Furthermore the liquid itself must be electrically modeled. For what concerns pure water, its electrical model is fully described by its relative permittivity, that is roughly 80, up to a frequency of $17GHz$ [10]. If ions are added to it, ion mass transport results in electrical conductivity depending on concentration and mobility. For instance PBS has a resistivity of $\approx 66\Omega cm$. Since the permittivity is just slightly influenced by the presence of ions, we can calculate the time constant associated with a volume of liquid as $\rho\epsilon$, corresponding for PBS to a cut-off frequeuncy of $300MHz$; below this frequency the fluid can be considered a resistance.
A typical impedance spectrum of two electrodes immersed in PBS is shown in fig. 1.1 and it shows at low frequency a capacitive behavior due to the double layer capacitance, whose value is proportional to the area of the electrodes, at medium frequencies a resistive plateau due to ionic resistance of the liquid medium and at higher frequency, the total impedance is shunted by a capacitance that can be either the parasitic capacitance of the connections to the electrodes or the physical capacitance of the electrodes separated by water.

The impact of the presence of a cell inside the liquid can be modeled as in figure 1.2; this model, one of the simplest and largely accepted, is called single shell [10] as it assumes the cell to be a sphere of the insulating membrane containing the cytoplasm. The thickness of the membrane is around $4nm$ and the specific capacitance associated with it is $\approx 1\mu F/cm^2$. The inner part of the cell, instead can be modeled with an RC parallel impedance with a characteristic frequency similar to the one of the solution. At low frequencies, the cell is seen as an insulating sphere increasing the total impedance of the medium. At higher frequencies, instead, the membrane capacitance is shorted, opening the possibility to investigate the electrical properties of the medium inside the cell.

Another interesting element to model electrically is binding of proteins near to the metal to liquid interface. This has been modeled in [11] by mapping the carbon atoms in protein structure and their electrostatic interaction; the resulting global model is an RC equivalent. For particular molecules like rhodopsin or acetylcholinesterase the impedance variations between the native and the complexed states are in the order of 10% to 30%. A similar behavior is present in DNA where the hybridized state increases the total impedance of the molecule layer [12]

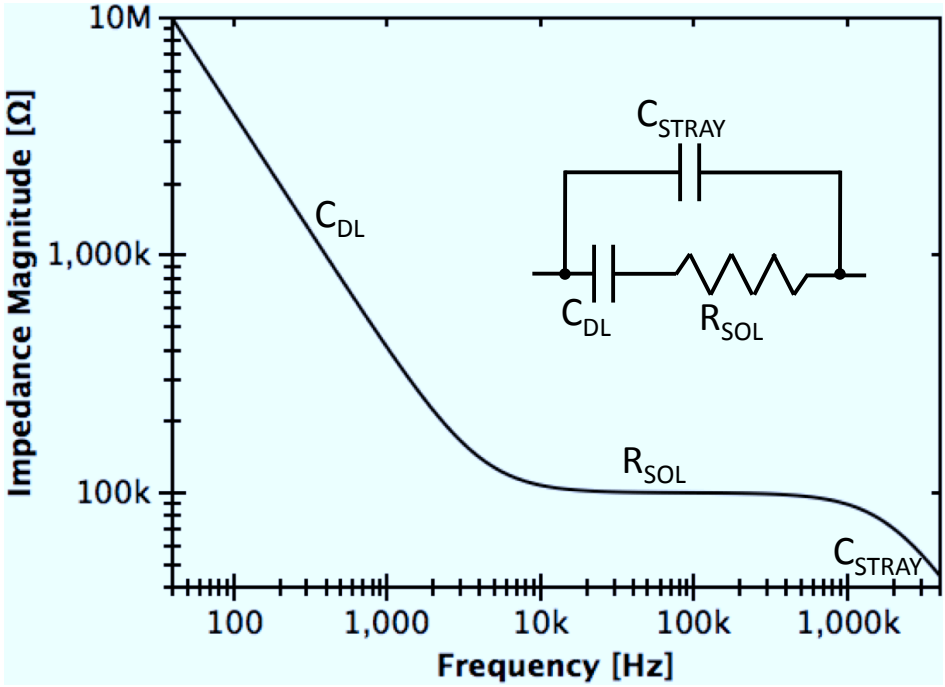

Figure 1.1: Typical impedance spectrum of two electrodes in liquid, showing three principal regions: at low frequency, the impedance is dominated by the double layer capacitance, at intermediate frequency

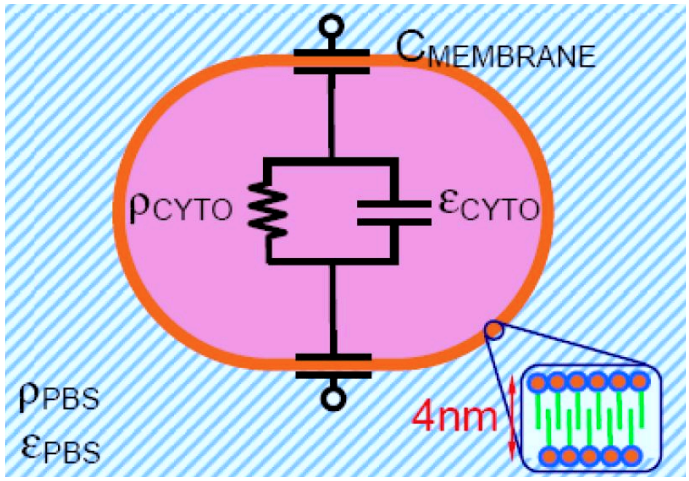

Figure 1.2: Single-shell equivalent model of a cell suspended in buffer solution. The cell membrane is formed by a bilayer of self-assembling lipid molecules.

1.2 Impedance measurement techniques

The measurement of impedance can be performed using different techniques. In all of them the sample under test is excited using a signal that is small enough to maintain its linear electrical behavior. Here we briefly present the main used ones together with their advantages and challenges.

Lock-in techniques With this techniques a frequency sweep is needed to obtain the impedance information over a range of frequencies and for each frequency the unknown impedance is excited using a sinusoidal signal multiplying the output with two sinusoids at the same frequency and with 0° and 90° phase difference; the result of the multiplication is low-pass filtered to obtain real and imaginary part. These can be related to the unknown impedance depending on the excitation scheme.
Most frequently used excitation schemes are presented in fig. 1.3 and include the Wheatstone bridge, ratiometric reading and transimpedance amplification. Wheatstone bridge is mostly useful when we are interested in measuring the variation of impedance over a reference impedance Z_{R2} since all the variations affecting both Z_X and Z_{R2} are directly canceled out. The main problem of this technique instead is the need for many different reference impedance to maintain a good sensitivity over a wide dynamic range (sensitivity is maximized when $Z_X \approx Z_{R1}$); furthermore its accuracy is limited by the presence of parasitic capacitances due to connections and this effect becomes dominant in microsystems where the interesting signal is small. The ratiometric scheme is useful due to its simple realization, but suffers from the same problems of the Wheatstone bridge and it cannot compensate unwanted variations of the impedance to be measured. The transimpedance scheme is useful because it allows precise control of the voltage applied to the device under test and it measures the input impedance independently from the stray capacitance due to connections. Furthermore this scheme allows also other type of measurement such as cyclic voltammetry or amperometry without changing the experimental setup. The main drawback of this technique is that the measurement bandwidth is limited by the maximum achievable gain-bandwidth product of the operational amplifier and from the input capacitance.

Fourier Transform This technique applies a known signal to the device under test, containing a wide spectrum of frequencies (most used signals are white noise, pulses or steps, but also more complex signals like chirps can be used) and derives the impedance from the ratio between the Fourier transform of the read current signal and the Fourier transform of the

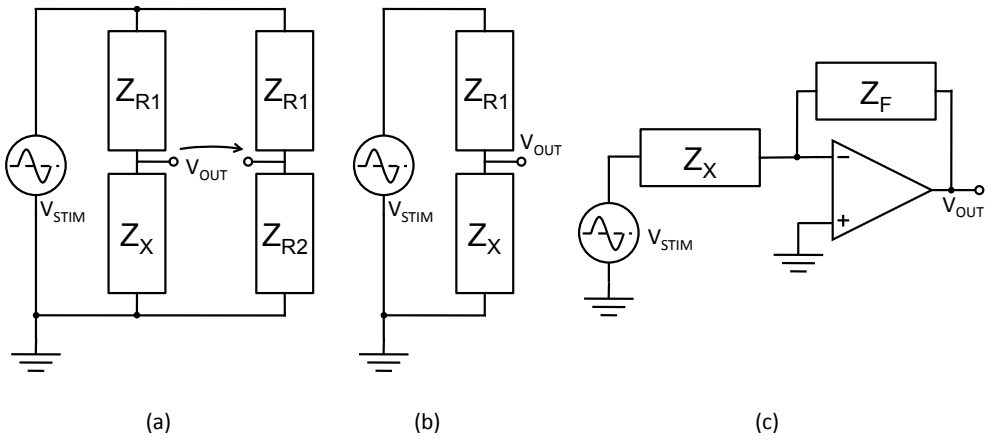

Figure 1.3: Circuits for excitation of the impedance to be measured Z_X. (a): Wheatstone bridge, (b): Ratiometric, (c): Transimpedance

stimulation signal. The excitation schemes are similar to the ones used for lock-in measurement. The main advantage of this method is that it can derive all the impedance spectrum from a single measurement, while the main disadvantages are that the limited power that can be delivered to the device under test is spread over all the frequency range, so at each frequency the signal to noise ratio is not optimal. Another disadvantage is that in case of non linear behavior of the device under test a phenomenon of cross-talk between frequencies can occur. Furthermore a great processing power is needed to extract the impedance from time domain measurements and this can limit time resolution respect to lock-in based techniques.

Charge Based This technique is mostly used to measure capacitances and has great success in CMOS technology. It is based on charging the input capacitance to a known voltage level and then discharging it, measuring the total mean current. Knowing the mean current and the reset rate it is possible to measure the input capacitance. Recent developments of this technique rely on the integration of the input charge on a known capacitance whose final voltage is directly proportional to the input capacitance value. This method is commonly used in commercial chip for capacitance measurement, but has the limitations that it is limited to capacitive input with no leakage current and it measures the capacitance at low frequency (ideally DC) not allowing impedance spectroscopy, nevertheless it has been used also in biological measurement

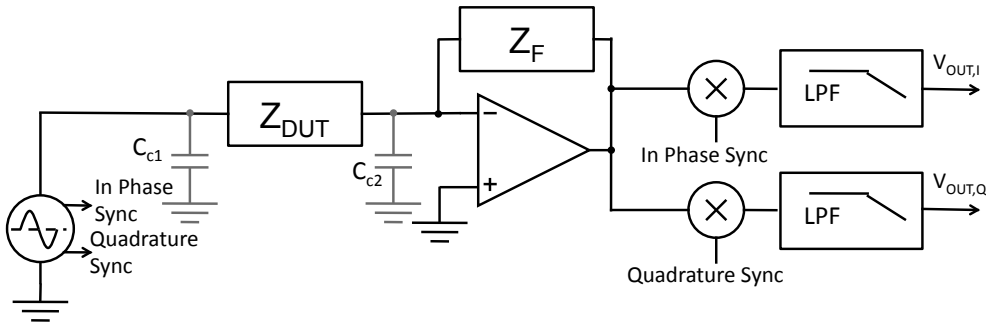

Figure 1.4: Impedance measurement scheme using transimpedance and lock-in amplifier

for DNA hybridization detection [8].

Resonant Methods With this techniques, the device under test is used as an element of the tank of an oscillator, so it influences the oscillating frequency. If the final resonator has a high quality factor, the sensitivity of this kind of measurement is really high. The problems with this measurement scheme is that it is suitable just for reactive impedances, it can measure the impedance only at the resonant frequency (that is usually in the *MHz* range, and is not suitable to characterize slow effects happening in biological environments), making impedance spectroscopy difficult to be realized. Furthermore the resonant frequency is usually in the *MHz* range and is not suitable to characterize slow effects happening in biological environments such as the formation of the double layer capacitance (see fig. 1.1). One more problem with this techniques is that parasitic capacitances associated with connections are seen as the device capacitance, worsening measurement accuracy, and this case transimpedance amplifiers cannot be used to solve it.

The technique that has been used in most of the circuits presented in this thesis is that one of the lock-in following a transimpedance amplifier (fig. 1.4). It is implemented using a sinusoidal voltage generator that drives the sensor, a transimpedance amplifier that reads the current flowing into it, two multipliers to move into the baseband the information about the impedance and finally two low-pass filters used to eliminate high frequency spurs arising from multiplication and to obtain a narrow noise bandwidth [13]. The feedback impedance Z_f can be chosen in order to maximize dynamic range and minimize noise. Note that in this scheme connection capacitances aren't limiting the accuracy of the measurement: capacitance C_{C1} is driven by the low-impedance voltage source used for stimulation and the voltage across C_{C2}

is fixed by the feedback of the transimpedance amplifier.

The DC component output voltage of the two channels can be expressed as:

$$V_{out,I} = -\frac{V_{stim}}{2}\frac{|Z_f|}{|Z_{DUT}|}cos(\angle Z_{DUT} - \angle Z_f) \tag{1.1a}$$

$$V_{out,Q} = -\frac{V_{stim}}{2}\frac{|Z_f|}{|Z_{DUT}|}sin(\angle Z_{DUT} - \angle Z_f) \tag{1.1b}$$

where $V_{out,I}$ and $V_{out,Q}$ are the output voltages of the two signal path, V_{stim} is the stimulation voltage amplitude, Z_f is the chosen feedback impedance, Z_{DUT} is the unknown impedance and the multiplier has been assumed to have a conversion gain of 1. From the measurement of the output voltages and knowing the feedback impedance it is possible to measure Z_{DUT}:

$$|Z_{DUT}| = \frac{V_{stim}}{2\sqrt{V_{out,I}^2 + V_{out,Q}^2}}|Z_f| \tag{1.2a}$$

$$\angle Z_{DUT} = arctg\left(\frac{V_{out,Q}}{V_{out,I}}\right) - \angle Z_f \tag{1.2b}$$

The noise in lock-in technique can be limited using a narrow final low-pass filter that allows the integration of the noise just around the measurement frequency. In addition most of the electronic components used for this technique must handle signals at the measurement frequency and only the final stage has a meaningful amplitude in DC, so the $1/f$ noise associated with them can be efficiently filtered out.

1.3 The need for miniaturization

The techniques for impedance measurement described so far are largely known and implemented in commercial instruments that nowadays are used by biologists for their study. In any case, for specific applications where the signal to noise ratio is important and the characteristics of the sensors are known, the performance of these instruments can be largely improved using custom designed electronics and integrated circuits.
In particular, one of the main source of noise when measuring currents or impedances at relatively high frequency is the series voltage noise of the transimpedance amplifier that generates a noise current in the input capacitance. The only ways to reduce this noise are: reduce the magnitude of the input noise, reduce the measurement frequency or reduce the input capacitance.

The first option must be surely pursued, but realizing amplifiers with less than $1nV/\sqrt{Hz}$ is a really challenging task and produces an increment on the input capacitance and consequently a worse noise and bandwidth performance. When measuring impedance spectrum, then, the measurement frequency must be spanned over a range, so also high frequencies must be considered. The only option remaining is the reduction of the input capacitance. Since the input capacitance in most cases is dominated by the connections, reducing the distance between the sample and the instrument positively affects noise performance. This is becoming also more important since device size is going from the microscale to the nanoscale to improve sensitivity. For this reason the integration of reading electronics on silicon is a recent challenge in the scientific community.
Of course the measurement instrumentation can be placed closer to the sample if it is compact, and the best performances can be achieved if the sample can be placed directly on the pad of a custom silicon integrated circuit.
Integration of the measurement system also allows the realization of smart substrates for the acquisition of multiple signals, improving measurement time and accuracy due to the use of redundant data [14]. These can be used to realize portable systems designed for replacement of laboratory analysis usable in point of care applications to speedup diagnosis. A further reduction in device size can lead to the realization of implantable systems that can be used for instance in real-time monitoring of vital parameters important for specific diseases like glychaemia for diabetics.

1.4 Scope and Organization of the Thesis

The scope of the thesis is the project and realization of electronical instrumentation for impedance measurement on micrometric biological samples. The activities done for this purpose comprehend design of integrated circuits, printed circuit boards, VHDL code for FPGAs and Visual Basic code for measurement control. These activities has been done for various instruments facing different applications and described in the following thesis chapters:

Chapter 2 Describes the design and realization of a compact instrument for cell counting applications in a microfluidic system, based on impedance measurement.

Chapter 3 Presents a custom designed instrument, based on an instrument on chip, for 2 phases impedance spectroscopy measurements with sensitivity better than $1aF/\sqrt{Hz}$.

Chapter 4 Presents a novel architecture for high frequency (up to 100 MHz) impedance measurements in a CMOS chip, based on the demodulation of the input signal, subsequent amplification and remodulation before closing a feedback loop.

Chapter 2

Cell Counting System

2.1 Motivation

Massive, cross-disciplinary scientific and technological efforts are devoted to the development of microfluidic systems allowing the implementation of biochemical analytical and diagnostic assays in miniaturized, portable lab-on-a-chip devices [15]. Unfortunately, very often the portability (and thus the diffusion) of these revolutionary bio-medical devices is significantly limited by dimension and complexity of the instrumentation required for their operation, in particular for liquid driving (pumps), sample preparation (centrifuges) and detection (microscopes).
Since a direct electrical read-out enables automatic, multichannel, high throughput, label free and quantitative single cell screening [16], we decided to explore the feasibility of a hand-held instrument addressing the need for miniaturization and portability. For these two characteristics, we choose to realize an instrument that is entirely powered and operated using the widespread USB standard. The whole system has been designed to read the impedance from two channels at the same time to detect cells flowing in two different microchannels.

2.2 Impedance sensing specifications

The system described in this chapter has been designed to be coupled to a specific microfluidic platform to integrate dielectrophoretic cell sorting with impedance-based counting. In any case the same design steps can be replicated to adapt instrumentation and electrodes to different microfluidic technologies, detection targets and systems.
The original dielectrophoretic system scheme [17] is shown in fig. 2.1 and consists in a microchannel where pressure driven cells immersed in PBS are

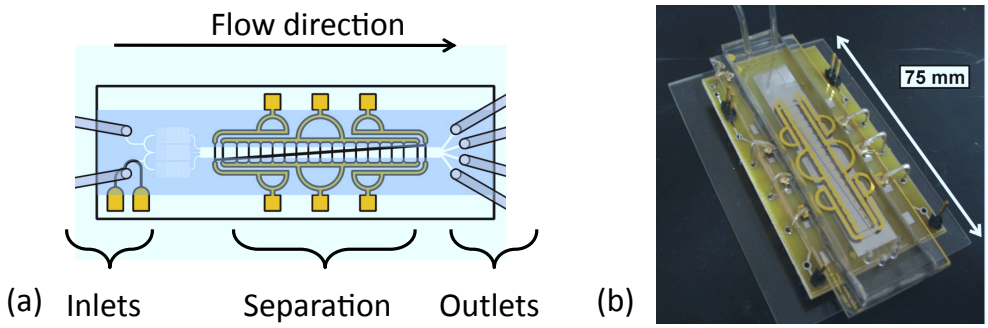

Figure 2.1: (a) Schematic of the device used for dielectrophoresis: cells diluted in PBS are inserted through the inlets and driven by hydrodynamic pressure, in the separation region, a dielectrophoretic force dependent on their electrical properties is applied to them using specific electrodes and can be directed in different outlets. (b) Photograph of a realized microfluidic device for dielectrophoretic separation.

separated depending on their electrical properties into different outlets. The electrical part of the system comprises different electrodes that are excited at frequencies around the *MHz*. Depending on the driving frequency different cells experiment different separations along the channel. The classical way to sense that separation is to mark the cells with fluorescent labels and then, using a microscope, to detect their position at the end of the channel. This method requires initial labeling and a fluorescence microscope, thus increasing measurement complexity and instrumentation cost. The goal of the project presented in this chapter is to design a system that can improve these two aspects.

The technology used to build the microfluidic system is soft molded PDMS (poly(dimethyl-siloxane)) on glass that allows fast prototyping and low-cost fabrication [18]. In this case only coplanar electrodes can be realized so parallel plate electrodes on two sides of the microfluidic channel, that are ideal from the sensitivity point of view, are not feasible. For ease of alignment reasons, the transversal configuration has been preferred over the longitudinal one. Channel dimensions are designed to minimize the pressure needed to move the fluid, together with the probability of two $15\mu m$ diameter cells to overlap along it, resulting in a cross section of $20\mu m \times 40\mu m$ (fig. 2.2a). The shape of the electrodes has been chosen to maximize intrinsic sensor sensitivity for cells of the same size [19]. In particular a big electrode size has been chosen to extend the possible measurement frequency: in fact, as illustrated in fig. 2.2b, the simplest small-signal equivalent of the electrode-solution interface is given by the series of the double layer capacitance and the solution resistance and

it goes in parallel with the unavoidable stray capacitance due to the connections. Since the electrical model of a cell passing between the electrodes at frequencies lower than some MHz is an insulating sphere that reduces channel conductivity [10], the range of frequencies where we have maximum sensitivity is where the total impedance is dominated by the solution resistance and is extended for big double layer capacitances. The value of double layer capacitance can be estimated from the area of the electrode in contact with the solution, considering a specific capacitance of $0.1 - 0.2pF/\mu m^2$ for standard PBS.
The impedance estimated using lumped parameters is shown in dashed lines in fig. 2.2c. The measured impedance instead is shown as a solid line in the same figure. The simple model (fig. 2.2b) is correct for low and high frequencies, while it underestimates the impedance for intermediate frequencies (transition region); this is because it doesn't take into account the finite height of the channel that creates a strong vertical confinement of the electric field, as confirmed by simulations using Finite Elements Methods (FEM).
Also the sensitivity of the sensor has been simulated using FEM, resulting in a variation of impedance that depends on the height of the cell on the channel (cells flowing closer to the electrodes are easier to detect), on its size and on electrodes gap. The latest one has been designed to maximize relative resistance variation when $10\mu m$ diameter cells pass over it, resulting in minimum variations on the order of 1% [19]. The absolute value of channel resistance can be correctly modeled using FEM, that gives a value of $\approx 50k\Omega$ when filled with PBS.
The detection bandwidth requirements depend on the speed of the cells crossing the sensing volume. In order to reach counting rates comparable with the throughput of state-of-art fluorescent cell sorters (thousands of cells per second) a sub-ms temporal resolution is needed. Thus selectable impedance sampling rate must reach $5 - 20kSa/s$.

2.3 Electrical design

In order to detect resistance variations of the channel impedance, a lock-in measurement scheme has been chosen. The system, presented in fig. 2.3, is composed by a signal generator that imposes a sinusoidal voltage across the electrodes inside the microfluidic channel, followed by a transimpedance amplifier that converts the current flowing in the device into a voltage. The signal is then multiplied by a synchronous square waveform coming from the generator in order to obtain the information about its in-phase component, proportional to the resistive part of the sensor impedace. The choice of the

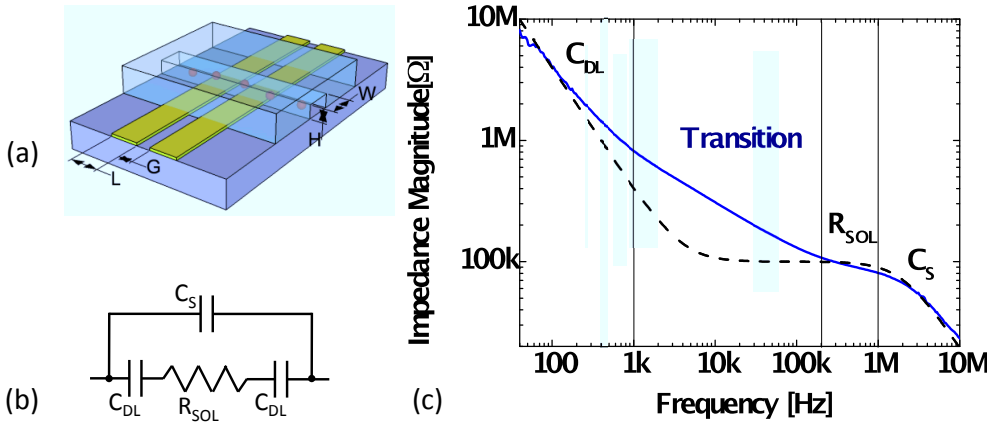

Figure 2.2: (a): Coplanar electrode configuration at the bottom of a microfluidic channel for impedimetric flow cytometry: $L = 200\mu m$, $G = 12\mu m$, $W = 40\mu m$ and $H = 20\mu m$. (b): Equivalent impedance model comprising the double layer capacitance ($C_{DL} \approx 800pF$), the solution resistance ($R_{SOL} \approx 100k\Omega$) and a stray capacitance ($C_S \approx 1pF$). (c) Simulation of the modeled spectrum (dashed) and its measurement on the realized electrodes (solid). The preferable operating frequency range is $10kHz - 1MHz$, where the modulation of the resistive part of the impedance is easier to detect.

square waveform multiplier has been done because of its ease of implementation and immunity to $1/f$ noise. The signal from the multiplier is then converted into the digital domain and elaborated using an FPGA that low-pass filters it and extracts the informations regarding the peaks due to the fast changes in channel resistance. Finally data is transferred to a laptop PC to be visualized, stored and analyzed.

For the correct design of the analog circuit, we first introduce the main equations governing the circuit transfer functions: the voltage output of the multiplier, when low-pass filtered is:

$$V_{OUT,lock-in} = -V_{gen}\frac{R_f}{R_{SOL}}\frac{2}{\pi} \tag{2.1}$$

where V_{gen} is the output voltage of the generator, R_f is the feedback resistor of the transimpedance amplifier, R_{SOL} is the unknown resistance of the microfluidic channel and the factor $2/\pi$ is the transfer gain of the square waveform multiplier inside the lock-in. Since we expect to measure small resistance variations (ΔR_{SOL}) over a reasonably high nominal value, we can linearize (2.1) obtaining:

$$\Delta V_{OUT,lock-in} = V_{gen}\frac{R_f}{R_{SOL}^2}\frac{2}{\pi}\Delta R_{SOL} \tag{2.2}$$

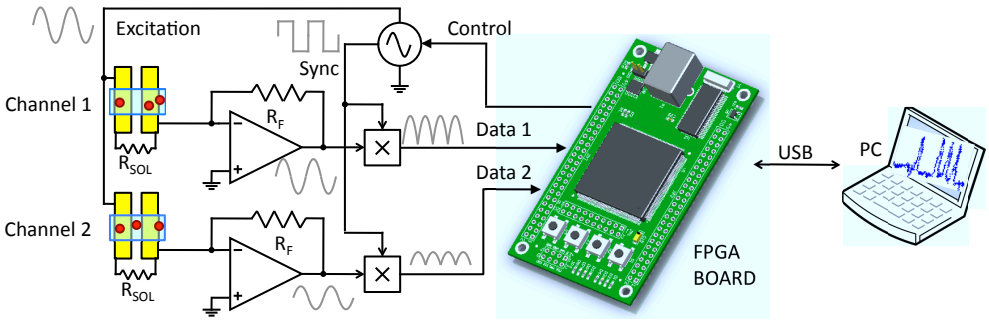

Figure 2.3: Block diagram of the 2 channels lock-in based impedance measurement system showing its basic blocks: the signal generator, the transimpedance amplifier, the synchronized square waveform multiplier and the USB connected FPGA board for digital data handling and experiment control.

Using this relation, fixing the maximum voltage applicable to the electrodes and the minimum resistance variation that the instrument must detect, we can determine the specification on the maximum acceptable noise of the instrument. For instance, for a channel resistance of $100k\Omega$ and an applied voltage of $1V_{PP}$, the rms noise voltage needed for 10Ω resolution is $10\mu V_{rms}$. If we want a lock-in low-pass filter bandwidth of $BW = 5kHz$ (suitable for $10kSa/s$ sampling rate), the total noise density at the output of the system (assumed white around the measurement frequency) must be smaller than:

$$S_V < \sigma \frac{V_{OUT,lock-in}}{\sqrt{2BW}} = \frac{10\mu V}{\sqrt{2 \times 5kHz}} = 100 \frac{nV}{\sqrt{Hz}} \tag{2.3}$$

This is a reasonable target that will be used in the design of the single blocks described in the following paragraphs.

2.3.1 Generation path

The signal gereration path has been designed taking into account the need for (i) sufficient SNR, greater than $80dB$ for an accurate detection of 0.1% resistance variations, (ii) flexible frequency selection in the $10kHz - 1MHz$ range, in order to adapt to various electrodes and channel geometries (iii) low impedance output with configurable amplitude from tens of mV up to a few Volts peak-to-peak (iv) a single supply voltage, compatible with the USB standard and battery operation ($< 5V$).
The architecture chosen for signal generation is based on a *Direct Digital Synthesizer* (DDS) followed by a fully differential transimpedance amplifier (fig. 2.4). The DDS is chosen for its versatility in frequency selection and its ease of

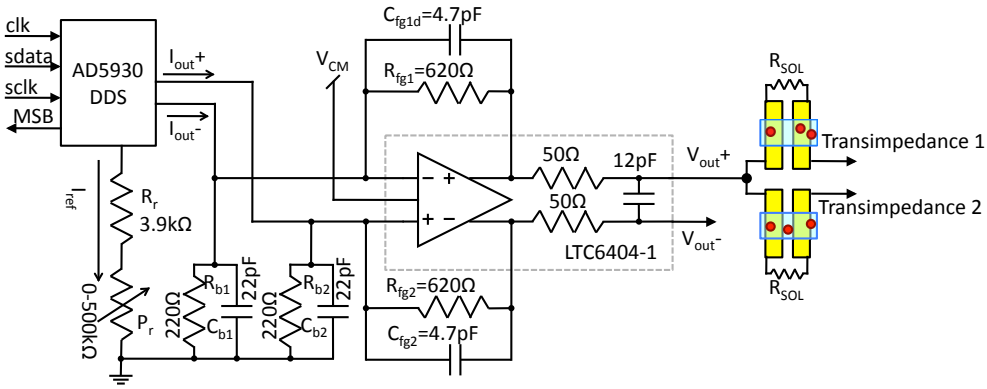

Figure 2.4: Schematic of the signal generation path: the DDS, controlled by the FPGA, is followed by a fully differential output buffer, based on an operational amplifier, configured as a transimpedance amplifier, that sets the output mean value and allows differential driving of sensing electrodes.

integration in a digital system, while the transimpedance amplifier is needed due to the current output of the DDS: voltage output DDSs in commerce don't allow free choice of output mean value; in addition this solution allows differential driving of electrodes that is a commonly used technique for dealing with low frequency channel impedance variations due to temperature or buffer solution ions concentration [29]. In our case, anyway, a simple high pass filtering of the signal output from the lock-in was enough to clearly detect the cell flow. The chosen DDS (AD5930) has a sampling rate sufficient to generate few MHz sinusoids with at least 10 sampling points and features a most significant bit output suitable for lock-in synchronization. The amplitude modulation has been managed by changing the reference current for the DDS over two orders of magnitude using a potentiometer.

Transimpedance resistances (R_{fg1} and R_{fg2}) has been chosen in order to obtain maximum output peak voltage greater than $1V$, while R_{b1} and R_{b2} are needed for setting DDS output voltage inside its compliance range. Capacitances C_b and C_f are chosen to low-pass filter the output and, in this configuration, a gain-bandwidth product of the operational amplifier of $320MHz$ is required for 45° phase margin.

The total output noise is due both to the DDS and to the output buffer. The expected output noise of the DDS (usually not explicitly reported in the datasheets) can be estimated from the Signal to Noise Ratio (SNR). This parameter is defined as the ratio between the maximum amplitude of the signal and the total spurious signals (noise and harmonics of the main frequency) calculated on the Nyquist bandwidth. By assuming the noise from DDS as a

white noise, we are overestimating it in regions where harmonics aren't present, like in our case where the bandwidth of interest is a narrow interval around the fundamental tone.
Taking into account noise from DDS, from the output buffer and from passive components, we can calculate the total output noise spectral density as:

$$S_{v,gen} = \\ = \sqrt{\left(\frac{V_{DDS,p}}{\sqrt{2}\,SNR_{DDS}}\right)^2 \frac{2}{f_{ck}} + \left(I_{n,AD} + \frac{4kT}{R_b} + \frac{4kT}{R_{fg}}\right) R_{fg}^2 + V_{n,AD}^2 \left(1 + \frac{R_{fg}}{R_b}\right)^2} \tag{2.4}$$

Where $V_{DDS,p}$ is the peak voltage of the generated sinusoid, SNR_{DDS} is the signal to noise ratio of the DDS as reported on the datasheet, f_{ck} is DDS clock frequency, $I_{n,AD}$ and $V_{n,AD}$ are the current and noise voltage of the fully differential operational amplifier and R_a and R_b are the input and feedback resistances of the output buffer (see fig. 2.4).

2.3.2 Readout path

The basic requirements for the current-reading front-end are proper bandwidth to perform measurements up to $1MHz$, a single supply voltage smaller than $5V$ (to have compatibility with USB standard), stability with an input capacitance as big as $10pF$ and it should be as low-noise as possible. The topology chosen to perform current amplification is the classical transimpedance amplifier (fig. 2.5) with a feedback resistor and a capacitor to stabilize the configuration.

In this topology we need to chose the operational amplifier, the feedback resistor and the feedback capacitance. The analysis of the loop gain of this configuration, under the hypothesis of single pole behavior of the operational amplifier, shows two poles, one of which is due to the operational amplifier and the other one due to feedback and input impedances, and one zero due to feedback impedance at the frequency of $1/(2\pi R_{ft} C_{ft})$. The zero comes after the second pole if the voltage partition due to C_{ft} and C_{IN} is smaller than the one due to R_{ft} and R_{SOL}, which is usually the case. In this condition, the stability of the transimpedance amplifier is guaranteed with more than 45° of phase margin if the closed loop bandwidth is bigger than the frequency of the zero, and in this case the unitary loop gain frequency is $GBWP_{OAT} \times (C_{ft} + C_{IN})/C_{ft}$. To have higher phase margin, the design has been done with a factor of 10 margin between the closed loop bandwidth and the frequency of the zero. Note that the frequency of the zero is also the frequency of the first pole of the ideal gain, so it must be kept at at least $5MHz$

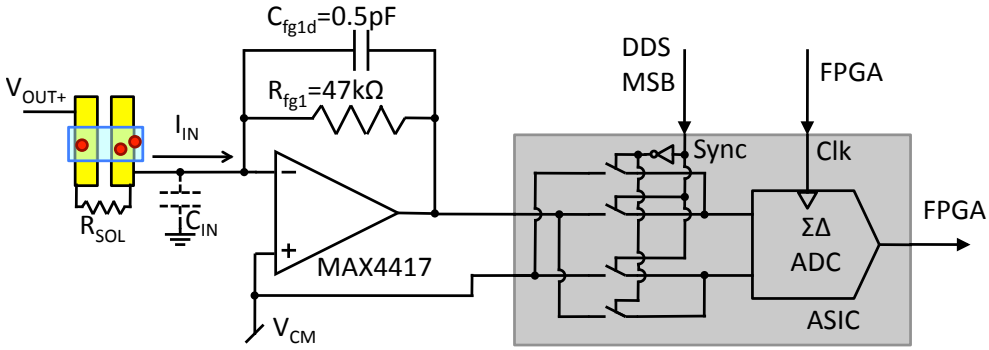

Figure 2.5: Schematic of the current reading path showing the low-noise transimpedance amplifier, the square waveform multiplier synchronized with the generated signal and the analog to digital converter. This structure is replicated twice to handle data from two channels.

to correctly amplify also high frequency signals.
Transimpedance design also took into account noise performances. The total output noise spectral density, including the contribution due to channel resistance is:

$$S_{v,OUT,T}(f) = \\ = \sqrt{4kTR_{ft} + I_{n,OAT}^2 R_{ft}^2 + V_{n,OAT}^2 \left|1 + \frac{R_{ft}}{R_{SOL}}(1 + j2\pi f R_{SOL} C_{IN})\right|^2 + \frac{4kT}{R_{SOL}} R_{ft}^2} \tag{2.5}$$

where $I_{n,OAT}$ and $V_{n,OAT}$ are respectively the current and voltage noise spectral densities of the operational amplifier, f is the frequency and $j = \sqrt{-1}$. The noise performance of the amplifier has been evaluated calculating the relative excess noise introduced by the electronic system respect to the intrinsic current noise of the sensor:

$$S_{v,OUT,S} = \sqrt{\frac{4kT}{R_{SOL}}} R_{ft} \tag{2.6}$$

Using these equations we screened commercially available operational amplifiers suitable for this block, determining for each one: (i) minimum C_{ft} in order to obtain a closed loop frequency of $50MHz$, (ii) maximum R_{ft} that gives an ideal gain pole of $5MHz$, (iii) the total relative excess noise introduced by the electronics. The configuration introducing less noise is reported in fig. 2.5, while figure 2.6 reports measurements on transfer function and output noise from the realized system, that show good agreement with the expected ones: the bandwidth of the amplifier is slightly bigger than the designed because

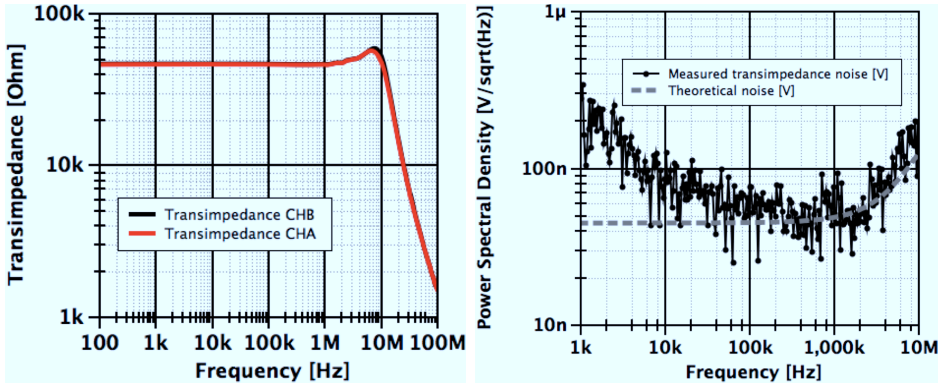

Figure 2.6: Transfer function (left) and output noise (right) of the realized transimpedance amplifier.

we did not use a phisical $500fF$ feedback capacitance, relying on the resistor parasitic one, and the output noise is compatible with an input capacitance of $3pF$.

The signal from the transimpedance amplifier is fed to a custom designed chip for lock-in multiplication and analog to digital conversion, with an input referred noise smaller than $40nV/\sqrt{Hz}$. The lock-in multiplication is obtained using pass transistors that invert the differential input signal synchronously with the most significant bit coming from the DDS (see fig. 2.5). The analog to digital conversion is obtained using a 2^{nd} order $\Sigma\Delta$ ADC clocked at $10MHz$. The whole reading structure is replicated twice to sense the resistance on two microfluidic channels contemporarily.

2.3.3 Digital signal elaboration

After the analog to digital conversion, all data processing can be done inside a digital processor. The basic operations that must be performed in the digital domain are: low-pass filtering and decimation of $\Sigma\Delta$ data to remove shaped quantization noise and reduce sampling rate, high pass filtering of data to remove low frequency impedance drifts due to temperature and ion concentration variations, peak detection and data transfer. These operations must be performed in real-time, so a dedicated system is required.

Low pass filtering of data can exploit the short length (1 bit) of the data from the converter to realize a Finite Impulse Response filter with no multipliers. The details of the realization of the filter together with the decimator are given in the next chapter.

The subsequent high-pass filter is designed to reduce at minimum the needed

computing power, in fact a fine tuning of the transition frequency is not required. For that, all the operations made with data were reduced to divisions by power of 2 (shifting of data) and additions. The high-pass filter is obtained subtracting the low-passed signal from the signal itself. Time domain equation of the filter is:

$$Y_{LPF}(n) = \frac{X(n)}{2^k} - \frac{Y_{LPF}(n-1)}{2^k} + Y_{LPF}(n-1) \tag{2.7}$$

where $X(n)$ is the input signal, $Y_{LPF}(N)$ is the output of the filter and k is a natural number that sets the bandwidth of the filter. The relation between k and the $-3dB$ bandwidth of the low-pass filter can be approximated for high values of k as:

$$BW_{-3dB} \approx \frac{2^{-k}}{2\,\pi\,T_{ck}} \tag{2.8}$$

where T_{ck} is the sampling period after the first filtering and decimation stage. That means that with a $\Sigma\Delta$ sampling frequency of $10MHz$, a decimation factor of 1000 and a k of 7, the pole of the transfer function is around $10Hz$, suitable to eliminate temperature drifts.
After high-pass filtering, the signal passes through a finite state machine to detect the impedance peaks due to cells passing over the electrodes. It works using a user-selectable threshold with hysteresis and stores data about peaks amplitude, duration and time of occurrence to allow reduction of data to be sent to the computer and easy analysis on peak characteristics.
The platform used to realize the digital blocks of the system is an Opal Kelly xem3001v2 FPGA extension module, featuring a Xilinx Spartan 3 FPGA, a PLL for clock generation and circuitry for USB communication.

2.4 Electrical validation

The realized prototype is shown in fig. 2.7 and is a sandwich of two $6cm \times 9cm$ boards, realized to match with the microfluidic system shown in the lower part of the same figure. After a first characterization of the performance of the single analog blocks, the system has been tested using a dummy impedance modulator simulating biological conditions: a fast analog switch (ADG333) has been used to short a 200Ω resistor in series with a $27k\Omega$ one, producing a resistance variation of 0.75%. The solid state switch is driven by a custom waveform generator in which various sequences of pulses can be loaded.
Using this simple and reliable setup, the sequences of the peaks detected with our system have been compared with the generated ones regarding mean and standard deviation of their duration, showing good agreement for a count rate

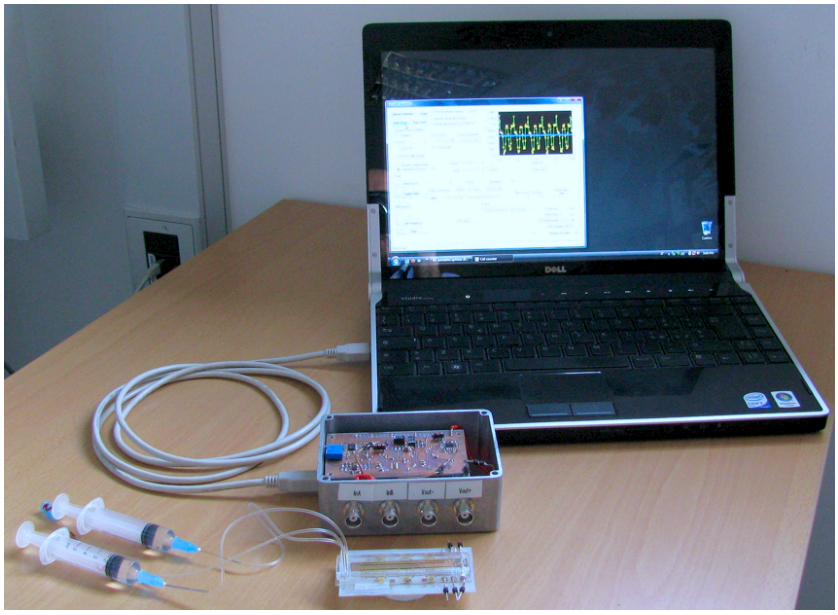

Figure 2.7: Assembled cell counter prototype connected to a laptop for data acquisition and real-time visualization.

of 100 events per second (fig. 2.8a): starting with pulses with mean duration of $2ms$ and standard deviation of $500\mu s$, after all the acquisition chain, we obtain a mean of $2ms$ and a standard deviation of $430\mu s$. Increasing the event rate to 1000 events per seconds, the read distribution is broadened from $50\mu s$ to $88\mu s$ (fig. 2.8b) due to the low-pass filter of the lock-in instrument: peak duration in that case has a mean of $200\mu s$ and the time constant of the filter was $63\mu s$, for a sampling rate of $10kSa/s$.
In this configuration, we also compared our instrument with a state-of-art bench top lock-in connected to a commercial stand-alone transimpedance amplifier (Zurich Instruments HF2LI and Femto DHPCA-100) for a count rate of 2000 events per second. The comparison is presented in fig. 2.8c-d, and shows similar SNR for the two instruments in the same conditions: applied voltage of $200mV$ at $100kHz$ and reading at $20kSa/s$ with a low-pass filtering bandwidth of $5kHz$. In fig. (fig. 2.8e) it is also possible to see the read high-passed voltage output from the realized lock-in together with the threshold used for peak detection algorithm and the error free peak detected by the embedded FPGA (fig. 2.8f).

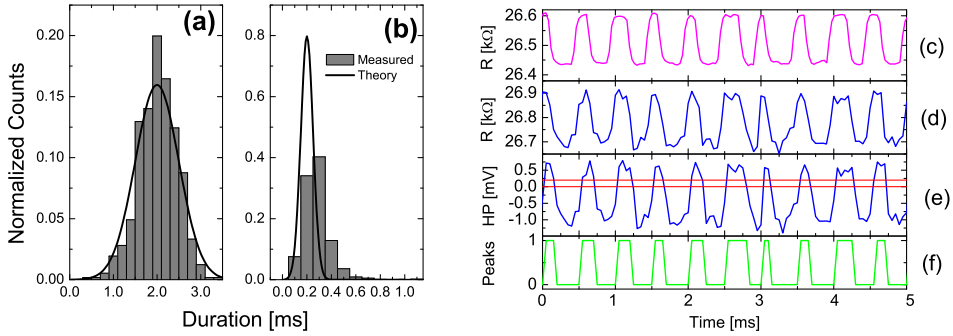

Figure 2.8: On the left side: comparison between the distribution of read peak durations and generated one, with gaussian distribution at 100 peaks per second (a) and 1000 peaks per second (b). On the right side: impedance variation measured at a sample rate of $20kSa/s$ with a bench top instrument (c), compared with our instrument (d); read voltage and threshold measured with our instrument (e) and detected peaks (f)

2.5 Biological measurements

The system has also been tested in a working microfluidic environment to count yeast cells (*Saccharomyces Cerevisiae*, strain B4743) suspended in diluted PBS (conductivity $0.35S/m$, corresponding to a channel resistance of $100k\Omega$). In the experiment the maximum count rate was limited by many factors: to correctly detect cells on the electrodes, they must stay on the high electric field zone between the electrodes ($30\mu m$ wide according to FEM simulations) for more than one sampling period, so, setting the sampling frequency at $2kHz$ and setting 2 samples per cell as the minimum requirement, lead us to a cell velocity of $30\mu m/ms$, corresponding to a flow-rate of $1.2\mu l/min$. Since the maximum concentration that doesn't lead to stiction on the channel is $10^6 cells/ml$, the average count rate is limited to $20cells/s$.
In these conditions, applying a sinusoid of $650mV$ at $100kHz$, clear peaks are visible in the high-pass filtered ($10Hz$) output voltage read from the embedded lock-in (fig. 2.9) and can be detected using the threshold algorithm described previously.
A statistical analysis on the recorded peaks (fig. 2.10)shows:

- A mean peak duration around $1.5ms$ that is in agreement with imposed cell speed in the microchannel
- Counting rate of $20cells/s$ that is in agreement with flow-rate and concentration
- Mean relative resistance peak height in the order of 0.2%, that is in

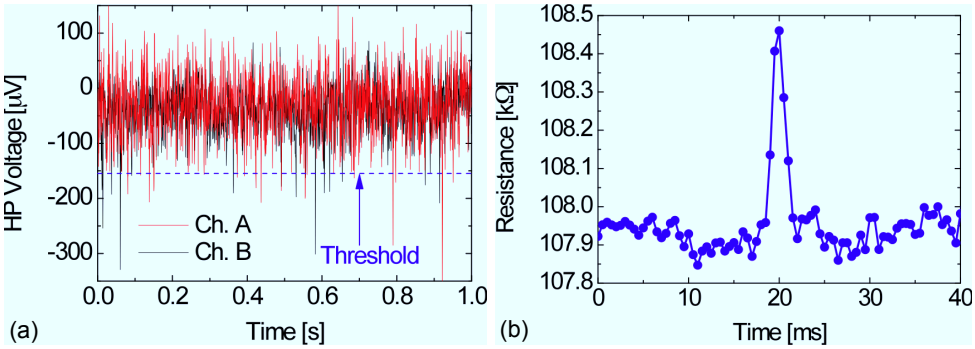

Figure 2.9: (a): Dual channel automatic threshold detection of yeast cells flowing in diluted PBS at 20 cells/s. (b): Detail of a single resistive peak (0.5% amplitude, $2.5ms$ duration) due to cell passing on the electrodes, sampled at $2kSa/s$ with an applied signal of $650mV$ at $100kHz$.

agreement with a mean cell diameter of $5\mu m$

- Wide distribution of peak heights due to wide distribution of cell diameters as shown in the inset of fig. 2.10 (a similar measurement on certified $10\mu m$ polystyrene beads shows far less peak height spreading).

The final experiment performed to validate instrument performance involved both dielectrophoretic separation and classical fluorescence cell detection. With dielectrophoresis it has been possible, by applying a voltage signal at a proper frequency and amplitude, to move the cells flowing in the microfluidic system between two different outlets (High or Low) with electrodes for cell counting at the end of each outlet. The setup can be also monitored using a fluorescence microscope.
Figure 2.11 shows the comparison between the relative count of the consolidated optical measurement and the results from our system for four different dielectrophoretic frequencies and for the two channels. It is possible to see that with no dielectrophoretic separation, almost all the cells go into the High outlet, for a dielectrophoretic frequency of $500kHz$ almost all the cells go to the Low outlet, and for the other frequencies intermediate results are obtained. As can be seen, with both methods the relative count is similar, meaning that the signals for dielectrophoresis, as expected, don't interfere with the lock-in measurement. Note that the dimensions of the setup with the new instrument is considerably shrinked and no fluorescent labeling is needed for electrical measurements.

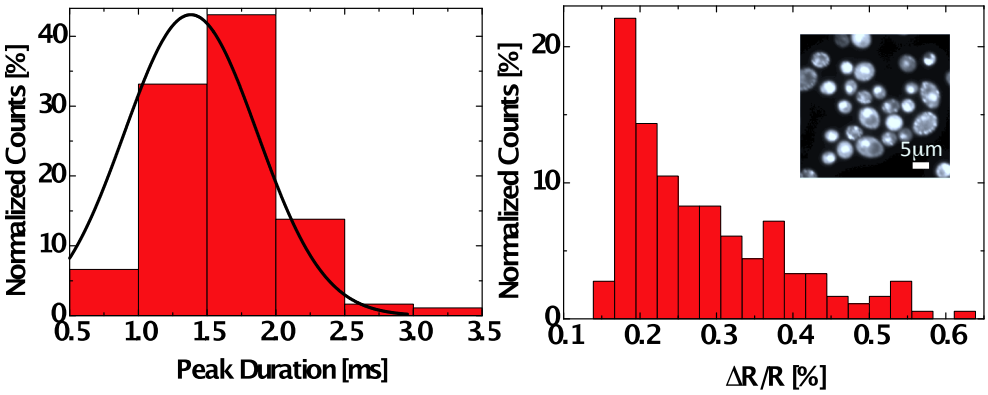

Figure 2.10: Statistical distributions of peaks regarding duration (left) and amplitude (right). In the inset is shown a microscope photograph of the counted yeast cells showing their distribution in size.

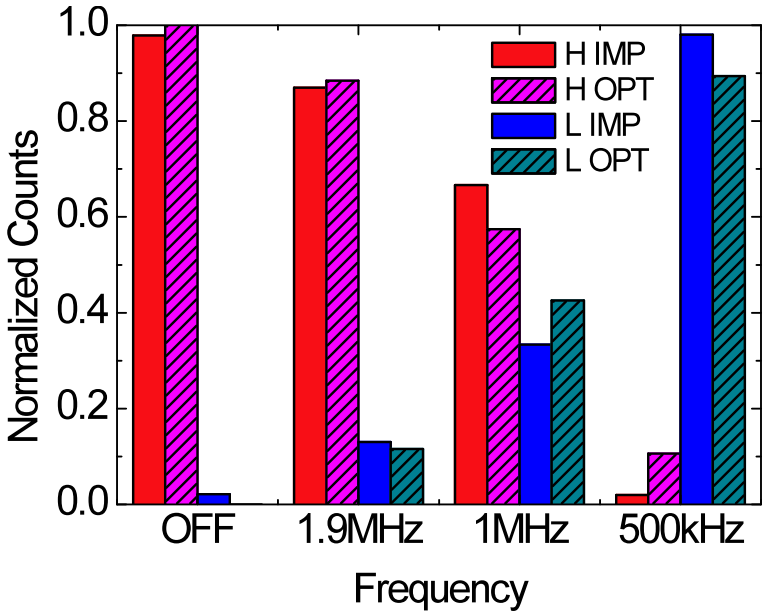

Figure 2.11: Performance comparison between counts obtained with our prototype and with optical detection for four different dielectrophoretic movements.

2.6 Conclusions

In this chapter we have presented the design and experimental characterization of a credit card sized dual-channel impedance detection system able to reach a throughput of 2000 counts per second. It operates up to $1MHz$ with a resolution of 0.1%. It implements real-time peak-detection simultaneously on the two channels exploiting an embedded FPGA that enables it use as a basic tool for an automated platform for high-throughput quantitative cell monitoring, analysis and closed-loop sorting. The combination of real-time digital processing and custom CMOS lock-in and data conversion enables unprecedented compactness and versatility for this kind of instrumentation especially if compared with standard fluorescence-based methods. The compatibility of impedance based cell-counting with concomitant dielectrophoresis has also been demonstrated.

Chapter 3

Portable Impedance Measurement System

In this chapter we will present the design of a compact system for impedance measurement in the kHz-MHz range, designed to address micro- and nano-scale bio-sensing applications such as flow cytometry or affinity biosensing. The core of the system is a CMOS integrated circuit performing low-noise analog current amplification and 2 phases lock-in multiplication that has been surrounded with the circuitry needed to use it as a complete hand-held instrument

3.1 Motivation

The system presented in this chapter can be considered as an evolution of the instrument presented in the previous one: in that case impedance sensing was obtained using commercially available integrated silicon chips that realized a transimpedance amplifier, and the system was used to detect the real part of the impedance using a single phase lock-in designed for the application. In this case the goal is to realize a fully integrated chip to sense both the in-phase and the in-quadrature part of the impedance.
The integration of the full instrument in a silicon chip is beneficial on many aspects of the measurement including noise, bandwidth and cost: reducing the length of connections between the instrument and the impedance to be detected, it is possible to reduce the noise introduced by the electronic instrumentation and to increase its bandwidth, furthermore, using a small-sized instrument, many parallel measurements on electrode arrays are possible, increasing throughput of biological screening.
Two phases lock-in, in addition, opens the possibility to investigate more details about the system under test: for instance in a metal-electrolyte junction

it is possible to measure both the double layer capacitance and the solution resistance, approaching the realization of a complete system for electrical characterization.
The basic blocks that have been integrated on silicon in this instrument are the front-end, the lock-in and an analog to digital converter, leaving outside the circuitry to source the stimulation sinusoidal signal and the final low-pass filter. In this way it is possible to change the bandwidth of the final filter according to the requirements in terms of measurement speed and total noise by changing the parameters of a digital filter; the front-end is designed to minimize noise, and all the off-chip connections, apart from the current sensing input, are either robust digital signals or power supplies that can easily be transferred without needing careful choice of the connections.
The proposed system, due to its high sensitivity and wide bandwidth, can be profitably exploited in a wide range of applications in the nanotechnology field, where the reduced size of the sample increases the impedance value beyond the possibility of standard instrumentation.

3.2 Front-end design

The front-end of this instrument has been designed in order to be able to measure impedances that are mainly capacitive, with maximum value of some tens of pF with parallel resistance in the order of the $G\Omega$ or more. One of the main objectives in the project of the front-end is the reduction of noise together with the achievement of wide bandwidth. For more flexibility, the front-end must have the capability to operate with leakage currents in the nanoampere range, as common in some biological experiments [20]. For these reasons we choose to implement a transimpedance amplifier with capacitive feedback, in fact this topology gives constant gain versus frequency when the input impedance is capacitive, doesn't introduce any noise due to the feedback element and has wider bandwidth respect to the resistive feedback if stability has to be guaranteed. The circuital scheme of the front-end is given in fig. 3.2 and is based on a previous work [21]. The feedback capacitor has been chosen to be small to increase sensitivity, but big enough to have sufficient bandwidth and matching on different realized chips, resulting in a value of $100fF$. The designed operational amplifier for this block has a gain-bandwidth product of $100MHz$ and the resulting overall bandwidth is in the order of $10MHz$ when the total input capacitance is in the order of $1pF$. The noise of this stage is dominated by the series noise of the operational amplifier that has been minimized using an high transconductance input stage with resistive load. Further details can be found in [21].

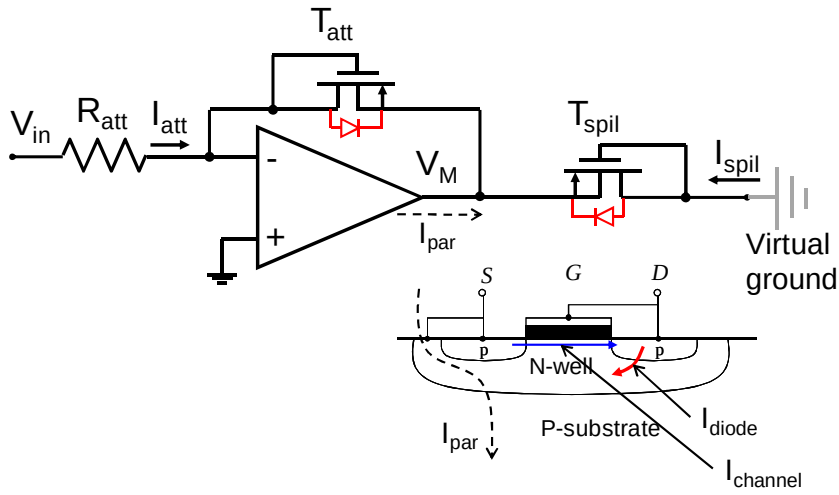

Figure 3.1: High valued resistors realization. Since the voltage applied to T_{att} and T_{spill} is the same, the ratio between the currents flowing into them depends only on their aspect ratio and so it is possible to obtain current division and high value equivalent resistors. Note that the bulk-source connection allows the system to manage the current in one direction using the active PMOS and in the other direction using the Drain-Nwell junction.

The main drawback of choosing an integrator as the front-end for our instrument is that it needs a reset network to prevent saturation. A simple switch in parallel with the feedback capacitance, active when the output voltage reaches a threshold can ensure a measurement time of $100\mu s$ if the threshold is set to $1V$, the feedback capacitance to 100 fF and the DC input current is $1nA$. Of course it can change with different DUTs or threshold voltages, but in typical applications is less than $10ms$ and is not enough to get accurate impedance measurement. Furthermore the discharge of the feedback capacitor introduces charge on the virtual ground that can damage the input sample. So, to enable unlimited measurement time, we implemented a continuous time reset network.

The simplest continuous-time reset network is a resistor, but its use in integrated technology poses some problems: first of all noise is reduced using high value resistors and to become negligible respect to operational amplifier series noise should be in the $G\Omega$ range, but such high value resistors occupy unacceptable large area of the silicon chip and add an high parasitic capacitance. These aspects have been solved using specific circuit techniques. The realization of high valued resistors has been done using the scheme presented in Fig. 3.1. In that scheme the current flowing into resistor R_{att} gets divided using the two transistors T_{att} and T_{spil} that share the same drain to source voltage

since they are connected between one common node and two virtual grounds. In this way all the current flowing into R_{att} flows into T_{att} and gets divided by the ratio between the form factors of the two transistors. Using this technique it is possible to obtain an equivalent resistor of $45M\Omega$, integrating a resistance R_{att} of $300k\Omega$ and using a division factor of 150. In this scheme the source of the PMOS has been shorted with the bulk on the n-well, enabling the circuit to handle both forward and reverse polarity current: when the input voltage is positive, the current flows into the drain-bulk parasitic diode and can still be divided making the ratio of the drain areas of T_{att} and T_{spill} equal to their form factor ratio. This scheme is also beneficial regarding the noise of R_{att}: its thermal noise gets divided by the square of the division factor so for our $45M\Omega$ equivalent resistor, we obtain an equivalent noise equal to that one of a $6.5G\Omega$. This noise is achieved if the total current is smaller than the pA, for higher currents the dominant noise source is the shot noise of T_{spil} which is equal to $2qI_{spil}$ since it is designed to be in the sub-threshold region.

The realization of the discharge network using a resistor poses a second problem. In fact the low frequency pole in this case is fixed by the choice of the capacitor and equivalent resistor values. With the cited values we obtain a low-frequency pole at $f_{MIN} = 1/(2\pi 100fF 45M\Omega) \approx 35kHz$, posing a strict limit on impedance measurement frequency. To extend the bandwidth of the front-end toward lower frequencies, we added a filter in the DC current feedback path that activates it at low frequencies and disables it for frequencies lower than the natural $R_{DC}C_f$ pole (see Fig. 3.2). The transfer function of the filter is sketched in the upper right part of the figure and it is possible to see that at low frequencies its high gain imposes a low level voltage at the node A and consequently forces the current to flow into R_{dc}. At high frequencies, instead the loop gain of the DC path is smaller than 1, leaving all the signal current i_s to flow in the feedback capacitor. The frequency at which the input signal starts to be integrated is where the DC loop gain is 1 and can be expressed as:

$$f_m = \frac{1}{2\pi R_{dc} C_i \gamma} \tag{3.1}$$

where γ is the attenuation of the H(s) filter at high frequency and is a free parameter that can be used to move the lower measurement limit. Since f_m is intended to be in the hundred of Hz range to extend the minimum measurement limit, all the singularities in the filter must be well before that frequency to ensure stability. For that reason the resistances used in its realization must be well bigger than the $G\Omega$ and have been realized using the current division technique described earlier in this paragraph. In particular, by cascading four current dividers, an equivalent resistor of $5T\Omega$ has been obtained using a physical resistor of only $100k\Omega$.

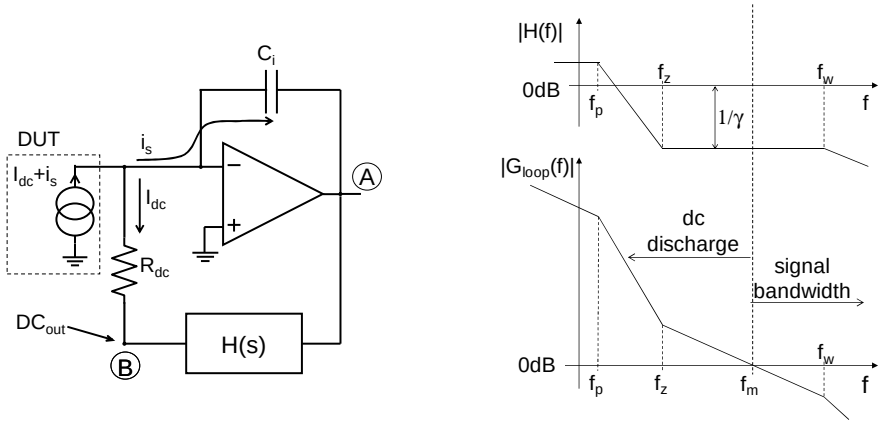

Figure 3.2: Realization scheme of the discharge netword (left) and transfer functions (right) of the H(s) amplifier (top) and of the loop gain (bottom)

The realized front-end has a bandwidth of $10MHz$ with an input capacitance of $1pF$, an input referred noise of $3fA/\sqrt{Hz}$ with a pole at $100kHz$ with the same input capacitance (corresponding to an output voltage of $40nV/\sqrt{Hz}$ at frequency higher than $100kHz$), and an ideal transimpedance gain that, corresponding to a capacitance, depends on frequency and has a magnitude of $1/(2\pi f 100fF)$ and a phase shift of 90°.

3.3 Integrated lock-in design

To obtain a compact instrument that can be easily utilized also in lab-on-a-chip applications, we choose to integrate in the silicon chip also the lock-in functionality and an analog to digital converter. In this way the chip has two digital outputs proportional to the real and imaginary part of the input impedance that can be directly processed using configurable digital electronics.

3.3.1 Multiplier

The first element that must be chosen when we want to integrate a lock-in instrument is the multiplier. In literature, many active multiplier structures in CMOS technology are reported [22], exploiting the non-linear characteristic of a MOS transistor, but all of them have strong limitations regarding low-frequency noise. In fact, since they are used as down-converters the output signal is in DC and the flicker noise of the drain current of the transistor used for multiplication is directly summed to it, so, to make it negligible respect to the noise of the front-end unacceptably large transistors are needed.

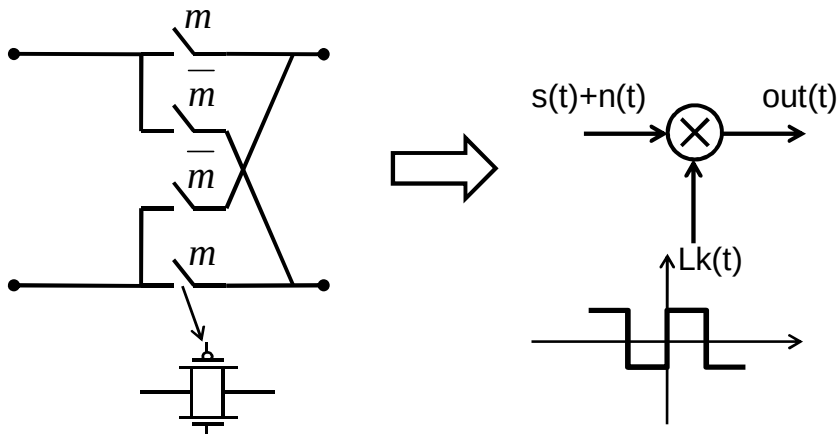

Figure 3.3: Scheme of the passive multiplier showing its equivalence to a square waveform multiplication. The realization of this multiplier is far easier than an active multiplier since it uses just four CMOS transmission gates

To avoid that, we chose to use simple passive multipliers as shown in figure 3.3. This kind of multiplier, being unpolarized, is almost flicker-noise free and has the great advantage of having a really compact implementation in CMOS technology. The main drawback of this scheme is that it cannot perform the multiplication of the input signal with a sinusoid, but multiplies it by a square waveform with values of ± 1. That results, in frequency domain, in a convolution of the input signal with a Lk signal whose spectrum is a series of deltas:

$$Lk(f) = \frac{2}{i\pi} \sum_{j=-\infty}^{\infty} \frac{1}{2j+1} \delta\left(f - (2j+1)f_m\right) \tag{3.2}$$

where f_m is the lock-in signal frequency and i is $\sqrt{-1}$. Considering a sinusoidal input signal that can be written as

$$S_{IN} = A_{IN} \left(\frac{\delta\left(f - f_m\right) - \delta\left(f + f_m\right)}{2i} \cos(\phi) + \frac{\delta\left(f - f_m\right) + \delta\left(f + f_m\right)}{2} \sin(\phi) \right) \tag{3.3}$$

where ϕ is the phase of the sinusoid and A_{IN} is its amplitude, the result of the convolution has a DC component that is equal to:

$$Out = \frac{2}{\pi} A_{IN} \cos(\phi) \tag{3.4}$$

That is equivalent, from the signal point of view and if we are able to correctly filter out all the undesired harmonics, to a sinusoidal multiplier with a

downconversion gain of $2/\pi$ that is more than acceptable since the input signal has already been amplified by the preamplifier. One problem with the square waveform multiplier can come when we consider noise, in fact the presence of multiple harmonics in the multiplier signal spectrum downconverts into the baseband more noise than just that one present around the measurement frequency. To quantify this noise increment we must know the output spectrum of the previous stage: in case of white noise the total downconverted spectrum can be written as:

$$Sn_{out}^2 = Sn_{in}^2 \left(\frac{2}{\pi}\right)^2 \sum_{j=-\infty}^{\infty} \left(\frac{1}{2j+1}\right)^2 = Sn_{in}^2 \tag{3.5}$$

where Sn_{in}^2 is the noise spectrum of the input signal; meaning that if the input noise is white, its spectral density is maintained after the multiplication, remembering that the signal has a loss of $2/\pi$ resulting in an acceptable increase of the equivalent input noise of $\sqrt{\pi/2} - 1 \approx 25\%$. In our case, since the preamplifier is an integrator, its output spectrum is decreasing with frequency and that results in even better performance of the passive multiplier. In the case of resistive feedback, instead, the typical output noise spectrum is increasing with frequency and can lead to a degradation in signal to noise ratio due to square waveform multiplication that is in the order of the square root of the ratio between the measurement frequency and the bandwidth of the preamplifier.

3.3.2 Analog to digital conversion

A second element that must be dimensioned in the lock-in scheme is the low-pass filter that must eliminate undesired noise and harmonics after multiplication. The bandwidth of the filter sets both sensitivity and time resolution of the measurement: a smaller bandwidth increases sensitivity, but decreases sampling rate. Since we want to realize a general purpose instrument in which the bandwidth can vary from 1Hz up to some kHz, it is very difficult to realize analog filters covering the desired frequency interval with good noise and linearity characteristics, for that we decided to realize the filter after the analog to digital conversion. Placing the analog to digital converter directly after the multiplier poses two design constraints:

1. the sampling frequency of the converter must be higher than the bandwidth of the preamplifier to avoid aliasing of high frequency noise or a low frequency anti-aliasing filter must be placed before the converter

2. a high sensitivity is needed to exploit all the sensitivity given by the front-end: a resolution better than 20 bit is needed at 1kHz if we don't want

to be limited by the converter regarding noise (considering an output voltage noise of $40nV/\sqrt{Hz}$ from the preamplifier and a full scale range of $3V$)

These requirements can be met using a $\Sigma\Delta$ analog to digital converter [23] since it can have high sampling rate to avoid aliasing and has high sensitivity due to noise shaping. The architecture chosen for this converter is a second order, switched capacitors $\Sigma\Delta$. The choice of the second order is a compromise between architectural complexity and stability on one hand and noise shaping slope and immunity to pattern noise on the other: for our application a high slope is not required since the oversampling ratio is big, but since we want to limit pattern noise we didn't choose a first order structure. The switched capacitor topology instead has been chosen to obtain good independence on clock jitter and duty cycle variations. The design of the converter has been driven by noise considerations on three main terms: i) shaped quantization noise, ii) residual quantization noise, iii) electronic noise.
The shaped quantization noise present in the signal bandwidth can be calculated, under the hypothesis of uncorrelated quantization noise [23] (reasonable in second order $\Sigma\Delta$ converters) as:

$$N_q = \frac{1}{3} V_{FS}^2 \frac{32\pi^4 \Delta_f^2}{5 f_s^2} \tag{3.6}$$

where V_{FS} is the full scale range of the converter, f_s is the sampling frequency and Δ_f is the bandwidth of the low-pass filter that follows the converter. As can be seen the quantization noise rapidly becomes negligible as the oversampling ratio $\frac{f_s}{\Delta_f}$ increases, so its impact is bigger when we want to measure a wide bandwidth signal. In our case, using a sampling frequency of $10MHz$ a full scale voltage of $3V$ and a maximum low-pass filter bandwidth of $5kHz$, the residual quantization noise is around $(242nV_{rms})^2$ which is lower than the noise of the front-end: $(40nV/\sqrt{Hz})^2 \left(\frac{2}{\pi}\right)^2 5kHz \approx (1.8\mu V_{rms})^2$. For lower input frequencies, the noise from the front-end is decreasing as $\sqrt{\Delta_f}$ while the quantization noise decreases as $\Delta_f^{5/2}$, resulting in a quantization noise that is always negligible.
The residual, unshaped quantization noise comes from using non-ideal integrators in the realization of the converter and this contribution to final noise can be expressed as [23]:

$$N_l = \left[\frac{1}{12}\frac{V_{FS}^2}{4}\frac{1}{f_s/2}\right]\left[\frac{1}{(1+A_1A_2)^2}\right]\Delta_f \tag{3.7}$$

with the first term between brackets being the 1bit quantization noise power spread over the Nyquist frequency $f_s/2$ and the A_1 and A_2 the DC gains of

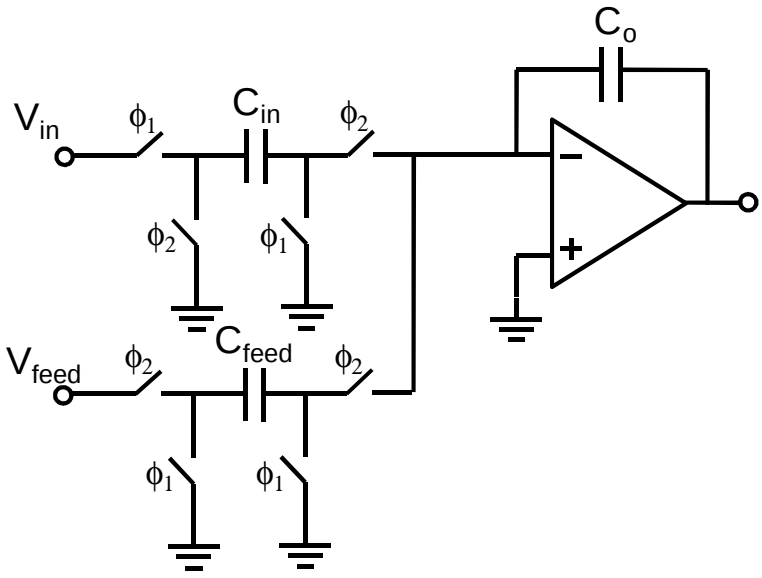

Figure 3.4: Schematic of a typical integrator used in switched capacitor ΣΔ converters with input and feedback branches

the real integrators of the first and second stage respectively. To have an unshaped quantization noise density negligible respect to the noise density of the front-end we must have:

$$\frac{(40nV)^2}{Hz} >> \frac{1}{12}\frac{V_{FS}^2}{4}\frac{1}{f_s/2}\frac{1}{(1+A_1A_2)^2} \tag{3.8}$$

that means that with a sampling frequency of $10MHz$, the geometrical mean of the DC gains of the two stages must be greater than 70.
To evaluate the noise added by the electronic components, we must know the structure of the input stage of the converter. A simplified schematic of the switched capacitor input stage is shown in figure 3.4. The contributions to front-end noise come both from the switched capacitors and from the noise of the operational amplifier. The switched capacitor contribution to noise has an rms value of $4kT/C$ for each capacitor each time it is switched. The input capacitor (C_{in}) directly has its noise at the input of the converter, while the feedback capacitor (C_{feed}) must be reported to the input with a gain of C_{feed}/C_{in}. The total noise power can be spread over the entire Nyquist frequency, resulting in a white power spectral density with value:

$$N_{SC} = 2\left(\frac{4kT}{C_{in}} + \frac{4kT}{C_{feed}}\left(\frac{C_{feed}}{C_{in}}\right)^2\right)\frac{2}{f_s} \tag{3.9}$$

where the 2 reflects the fact that each capacitor is sampled twice every clock period (it is charged during half of the period and then discharged during the other half), k is the Boltzman constant, T the absolute temperature, C_{in} and C_f are the input and feedback capacitances respectively (see fig. 3.4). From equation 3.9 it is possible to see that the noise can be minimized reducing C_{feed}, but this isn't generally done because it would affect the stability of the converter so usually C_{in} and C_{feed} are equally sized with $C_{in} = C_{feed} = C_a$ [24]. With this condition, if we want the noise of the converter to be smaller than the minimum noise of the front-end, we must have:

$$4\frac{kT}{C_{in}}\frac{2}{f_s} << 4\frac{4}{\pi^2}\frac{(40nV)^2}{Hz} \tag{3.10}$$

where the 4 in the right hand side is given by the particular structure adopted that adds a gain of 2 on the converter. Considering a sampling frequency of $10MHz$, the minimum input capacitance value is $1.3pF$. The chosen value is of $4pF$.
For what concerns the noise of the operational amplifier it is directly related to the input of the converter and therefore must be sized to be smaller than the minimum output noise from the preamplifier. For what concerns the white noise this is straightforward by the correct sizing of the transconductance of the input differential pair of the operational amplifier, while flicker noise has been managed using the chopping technique.
The complete schematic of the 2^{nd} order $\Sigma\Delta$ converter is shown in fig. 3.5; its structure is fully differential to exploit efficiently the dynamic range available in $0.35\mu m$ CMOS technology and the input is alternatively switched between the positive and negative input to obtain a gain of 2 in the signal path without increasing the noise. The first operational amplifier as said before is chopped both at its input and at its output to reduce low frequency noise. The chopping frequency has been chosen to be higher than the flicker noise corner frequency but lower than the operational amplifier first pole. In this way it is possible to neglect the additional flicker noise but at the same time the gain of the operational amplifier is not reduced by the chopping technique [25].

The clocking signals of the converter are internally generated following a four phase non-overlapping scheme in which are present the two main phases ϕ_1 and ϕ_2 and two delayed phases used to make the charge injected into the capacitances insensitive to the input voltage by opening input referred switches when the sensitive nodes are already at high impedance [26].
The input switches can be also used to perform the lock-in square waveform multiplication: for that purpose it is necessary to invert the polarity of the input voltage of the converter according with a synchronization signal and since the input switches already connect each input node with V_{IN+} and V_{IN-}

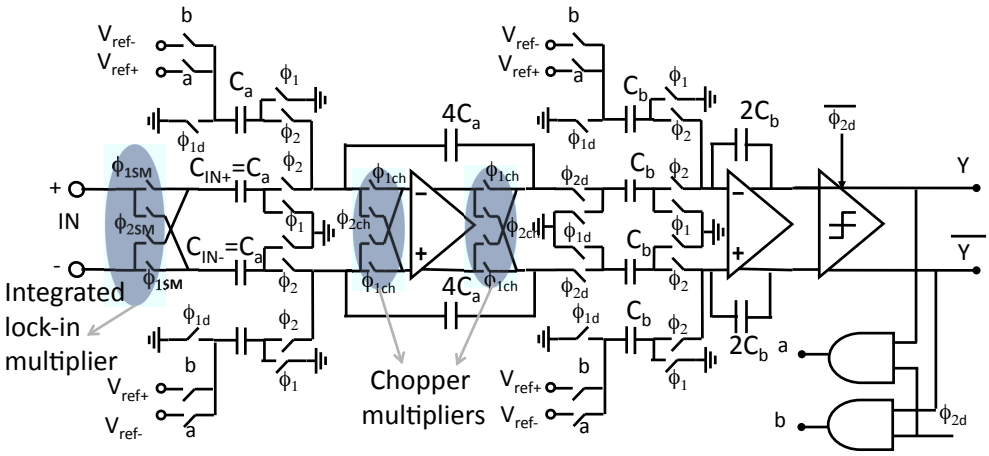

Figure 3.5: Complete schematic of the ΣΔ converter. Chopping switches for first stage operational amplifier and input lock-in multiplier are highlighted.

twice every clock period, the inversion of polarity can be achieved just with the correct handling of digital signals going to the input switches. The circuit that performs this operation is shown in figure 3.6; it takes the delayed versions of ϕ_1 and ϕ_2 and feeds them to the input switches when the synchronization signal is 0 and inverted when it is 1. To avoid switching when the converter is integrating and the related charge injection, multiplier switches are activated when both ϕ_1 and ϕ_2 are 0, delaying the multiplication signal until the next phase switching by means of a flip-flop and a NOR gate.

The conversion circuitry, has been replicated twice to obtain the measurement of the in-phase and of the in-quadrature part of the impedance. The two realizations share the same front-end, a buffer needed to charge the converter input capacitances, and the circuitry to generate the signals related to the phases of the converter. The front-end, the buffer and the two ΣΔ converters have been integrated in standard $0.35\mu m$ CMOS technology. The outputs of the realized chip are two one-bit streams whose baseband value is proportional to the in-phase and in-quadrature part of the admittance. Due to noise shaping in the 2^{nd} order ΣΔ converter, the spectrum of the quantization noise in these signals has a slope that increases as f^2. For that reason, to obtain optimum signal to noise ratio, the low-pass filter that follows the converter must be at least of the 3^{rd} order [27]. The third order filter, together with the decimator, has been implemented off-chip to reduce the number of connections with the outer world and an FPGA has been chosen as the computing element; that grants high throughput and fast information processing.

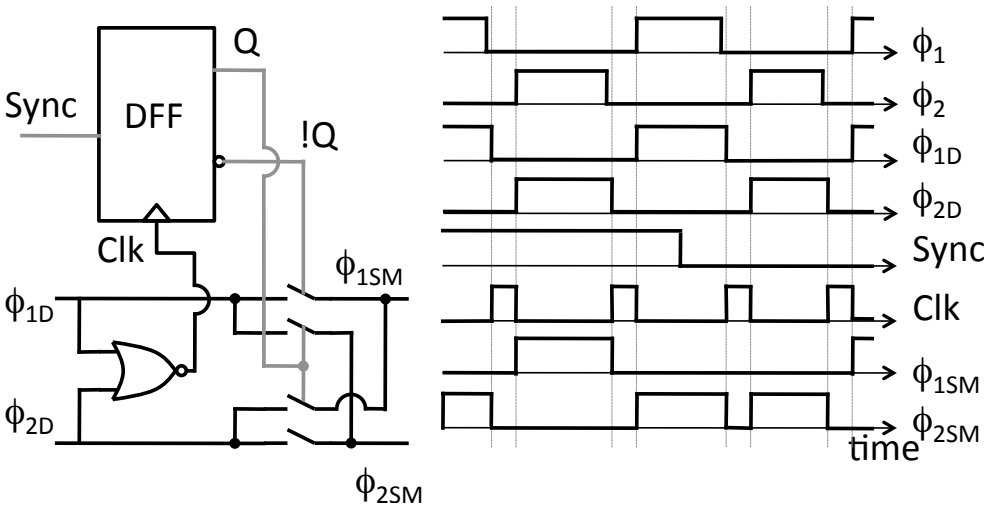

Figure 3.6: Schematic of the input switches phase generation circuit that enables the square waveform lock-in multiplication.

A 3^{rd} order filter suitable for N times decimation is the convolution of three first order filters, each with a bandwidth that is smaller than $f_s/2N$ where f_s is the original sampling frequency, in this way we can consider Shannon's theorem to be satisfied and aliasing is avoided. A simple moving average filter on N samples is a single pole filter whose $-3dB$ bandwidth is $BW \approx f_s/2.25N$ so we can implement a 3^{rd} order filter cascading three moving average filters of length N. The resulting $-3dB$ bandwidth is $f_s/(N \times 3.8)$ (coming from the numerical solution of the z-transform transfer function where the z variable is substituted with $e^{i2\pi f T_{CK}}$).
Since the total length of the final filter is 3N and the decimation factor is N we need to process in parallel three output samples using the coefficients $C1$, $C2$ and $C3$ shown in fig. 3.7. The function describing the coefficients can be divided into three parts: in $P1$ it is a parabola with positive derivative and upper concavity, in $P2$ it is a parabola with negative concavity and in $P3$ it is a parabola with negative derivative and upper concavity. The value of the coefficients in these three parts can be expressed recursively as [28]:

$$C(n)|_{P1} = C(n-1)|_{P1} + n \qquad \forall n \neq 0,\ C(0)|_{P1} = 0 \tag{3.11a}$$
$$C(n)|_{P2} = C(n-1)|_{P2} + N - 2n \quad \forall n \neq 0,\ C(0)|_{P2} = C(N)|_{P1} \tag{3.11b}$$
$$C(n)|_{P3} = C(n-1)|_{P3} - N + n \qquad \forall n \neq 0,\ C(0)|_{P3} = C(N)|_{P2} \tag{3.11c}$$

From this recursive definition it is easy to implement the filter in an FPGA using one counter, three adders and three registers, as shown in the right part

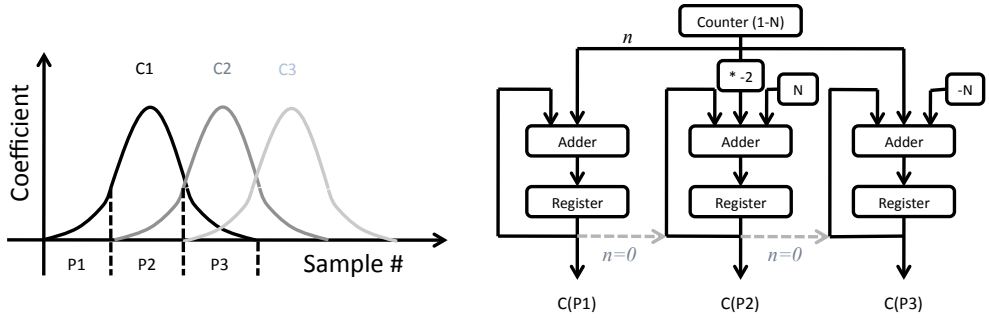

Figure 3.7: Third order filter and decimator coefficients and generation scheme that can be efficiently implemented

of fig 3.7. This solution is efficient from the point of view of memory usage, since no coefficients must be stored inside the FPGA, but they are computed every time. Once the coefficients are generated, the implementation of the filter is straightforward because the input signal is 1 bit wide and its multiplication with the coefficients of the filter is just a multiplication by 0 or 1.

The bandwidth of the filter can be easily tuned increasing the maximum value of the counter, paying attention to have enough word length in the signals that store coefficients and filtering results. In our case we choose a coefficient word length of $40bit$ leading to a maximum decimation factor of around 10000 and a minimum bandwidth of $f_s/10000/3.8$ where the factor 3.8 is the $-3dB$ bandwidth of the cascade of three first order moving average filters. So, for a sampling frequency of $10MHz$, the minimum sampling rate after the filter is $1kHz$ and its $-3dB$ bandwidth is $262Hz$. Bandwidth and sampling rate can be further reduced once data is transferred to a PC with the custom designed software using a simple moving average filter, that is sufficient since the shaped quantization noise is already removed by the first filter.

3.4 Generation Path

The next section of the compact impedance measurement system that has been designed is the circuitry to source the excitation sinusoid. The main characteristics that this block must have are:

- Easily selectable frequency in the range from a few Hz to some MHz
- Amplitude control from few mV up to some hundreds of mV
- Low noise spectral density around the generated frequency

- Availability of synchronization signals both at 0° and at 90° with the generated signal

The need for tunable frequency suggests the use of a DDS (Direct Digital Synthesizer) that easily allows the generation of sinusoids over many decades of frequency. Since commercially available DDS don't provide in phase and in quadrature synchronization signals, we chose to implement the DDS inside the FPGA and use a DAC to generate the output sinusoid; in this way we have direct access inside the FPGA to the phase of the generated sinusoid (apart from analog delays) and we can generate in-phase and in-quadrature synchronization signals. The DDS and the DAC are clocked at $50MHz$ enabling a theoretical maximum generated frequency of $25MHz$ and the phase accumulator of DDS is $31bit$ wide for a minimum frequency and resolution smaller than $25mHz$. After the DAC that has a differential current output, we placed a difference amplifier to convert the current into an output voltage with fixed mean value, to limit the bandwidth to some MHz and to drive the output load. The generation path has been designed with an analog bandwidth of $10MHz$ so that it is possible to generate sinusoids up to some MHz with limited phase delay but at the same time we can filter high frequency noise from digital circuitry. The selection of the generated amplitude follows three different strategies: the modulation of the reference current of the DAC, a digital division of the signal fed to the DAC and an analog division of the signal at the output of the buffer. With these three techniques it is possible to obtain a output range from $1mV$ up to $1V$ with good noise and distortion characteristics. The complete design of the sourcing circuit is shown in fig. 3.8.

3.5 Electrical Measurements

All the presented sections of the measurement system have been realized and fit in a $9cm \times 12cm \times 5cm$ box (fig 3.9). For digital processing we used an OpalKelly xem3001v2 extension module that features a Xilinx Spartan3 FPGA, PLL, and circuitry for USB communication. The custom code for DDS source and $\Sigma\Delta$ filtering has been written in VHDL and measurement handling code has been written in Visual Basic. The whole system is USB powered and has external connectors just for the connection of the unknown impedance.

To validate the realized instrument, we performed measurements on test impedances and compared the results with the ones given by a commercial state-of-the-art LCR meter (Agilent E4980A). This comparison when measuring a $22pF$ capacitor in series with a $1M\Omega$ resistor, both shunted with a $1.5pF$

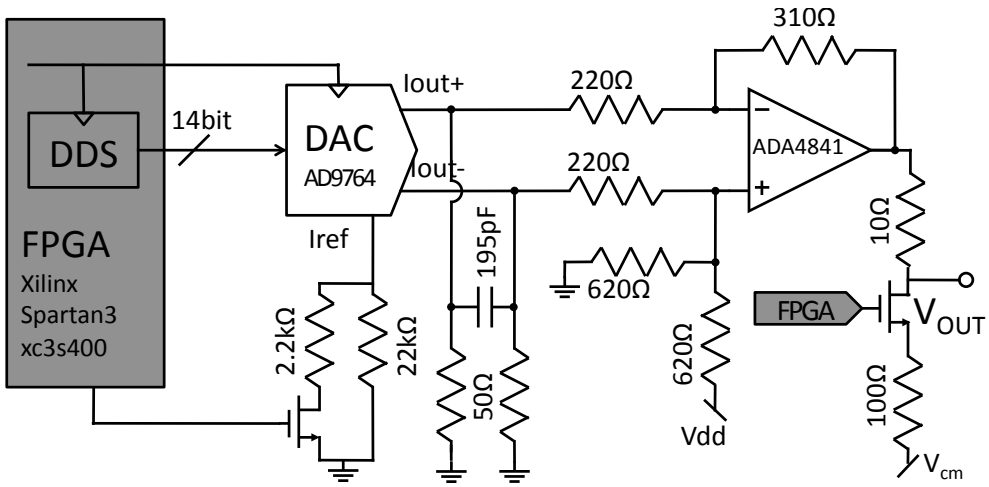

Figure 3.8: Schematic of the circuit that generates the sinusoid for impedance measurement including the FPGA implemented DDS, the output buffer and the amplitude selection circuits.

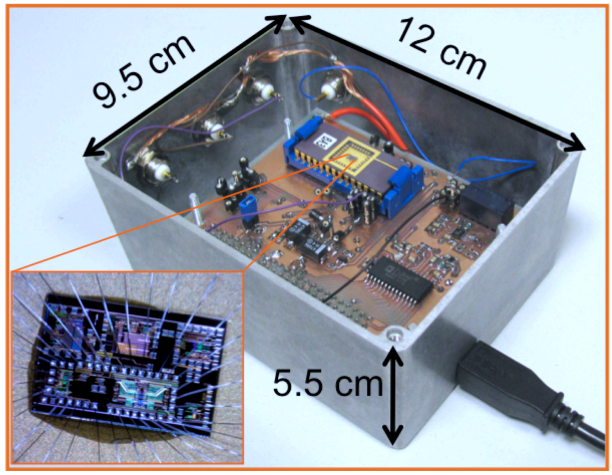

Figure 3.9: Picture of the complete Impedance Measurement System. In the inset a photograph of the realized CMOS chip is shown

capacitor are shown in figure 3.10 in the range from $1kHz$ up to $2MHz$. For this measurement we made a software compensation of the pole from the front-end, but no compensation was made for the low-frequency pole due to the DC discharging network and that causes the small increase in low-frequency measured impedance. From this figure we can see that the measurement without calibration is not greatly accurate, but in general in biological measurements, this is not needed since they rely on differential measurement, where noise performance is more important than accuracy. For what concerns the noise, we made the same comparison between our instrument and the commercial LCR meter while measuring a ΔC of $10fF$ over a $1.3pF$ mean value. The modulation has been obtained shorting a big capacitance in series with the small one using a MOS switch driven by an external digital signal running at $10Hz$. The results of this measurement are shown in fig. 3.11 for two different stimulation amplitudes. It is possible to see that with an excitation amplitude of $100mV$ the $10fF$ steps are clearly visible with both instruments, but with our instrument is around $140aF$, almost 10 times better than the commercial instrument. Furthermore, if we reduce the stimulation amplitude to $10mV$, the steps are still clearly visible with our instrument but are completely surrounded by noise using the commercial LCR.

The realized instrument has also been compared with two commercially available integrated circuits to measure capacitances: Irvine Sensors MS3110 and Analog Devices AD7745. These two circuits relay on the charge based capacitance measurement and can only measure capacitive devices, furthermore, they are less flexible in impedance measurements because they don't allow selection of applied voltage and of measurement frequency; nevertheless they are the only ones that can measure such high impedances and it makes sense to compare with our instrument with them since many biosensors are based on capacitive detection. Other circuits, like Analog Devices AD5933, that have a structure similar to the proposed circuit, cannot be compared, since they have a maximum input impedance range in the order of $10M\Omega$.

To compare noise performance of our circuit to the commercial ones, we used a figure of merit (FOM) obtained multiplying the noise spectral density in capacitance measurement (expressed in $aF/\sqrt{Hz}$) by the applied voltage: in fact for any measurement method, it is possible to obtain less equivalent noise, increasing the excitation voltage.

The results of the comparison are presented in Table 3.1 and show an improvement of our chip of more than a factor of 10, due to carefully designed front-end. One drawback of our system is that it is not fully integrated, since the generation part is realized off chip. In any case this is not a major problem since even for arrays of sensors the generation part can be shared between all the electrodes and even long connections don't affect measurement capability

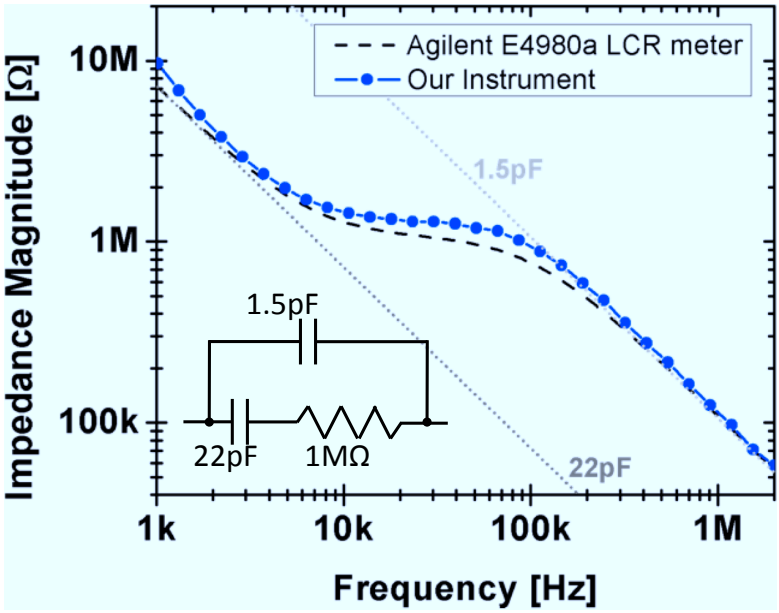

Figure 3.10: Comparison of the inpedance magnitude measured with the realized instrument and with a commercial LCR meter, when measuring the test impedance shown in the inset.

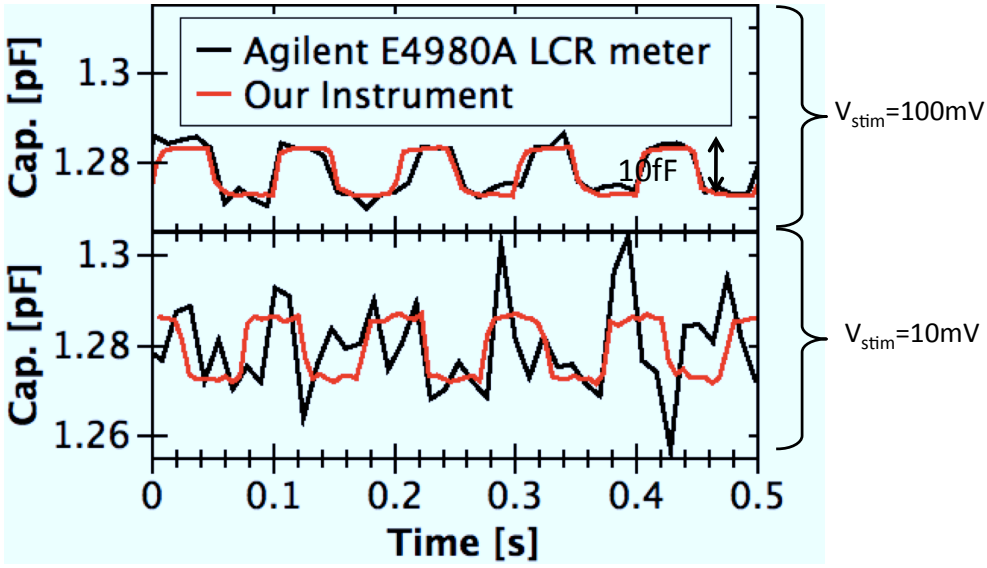

Figure 3.11: Comparison of noise performance on impedance time tracking between the realized instrument and a commercial LCR meter

as long as the source output buffer can drive their capacitive load.

Table 3.1: Comparison between the realized instrument and commercially available IC for capacitance measurement.

	Noise $[aFrms]$	Applied Voltage $[mV]$	Bandwidth $[kHz]$	FOM $[aF/\sqrt{Hz} * V]$
Our Instrument	350	100	2.5	0.7
Irvine Sensors MS3110	200	2250	2.5	9
Analog Devices AD7745	40	1650	0.087	7.1

Chapter 4

Wide bandwidth system

In this chapter we will present the concept and the design consideration that lead us to the project of an impedance measurement system suitable for wide bandwidth measurement. The idea behind this system is to avoid the use of a wide bandwidth operational amplifier using a demodulation and modulation scheme that allows to maintain a really high loop gain even when measuring the impedance at high frequencies.

4.1 Motivation and concept

In the previous chapters we have shown examples of impedance measurement systems based on a transimpedance amplifier and a lock-in. Although that scheme is quite easy to implement, it cannot be used to measure the impedance at frequencies higher than some MHz: assuming a capacitive feedback with a value of $100fF$ and a parasitic capacitance of $1pF$, we would need an operational amplifier with a gain bandwidth product of $10GHz$ to have a loop gain of 10 at $100MHz$. Although this is possible using current feedback topologies and BJT technology, this performance cannot be obtained in standard CMOS technology and furthermore in this case at the maximum frequency, the very limited loop gain doesn't allow accurate measurement.
Increasing the measurement frequency at some tens of MHz can be beneficial on the application point of view since at frequencies higher than some MHz the capacitance associated to the cell membrane is shorted enabling the investigation of the electrical properties of the cytoplasm [29].
Another application of high frequency impedance measurement is the support to AFM measurement in liquid. The addition of local impedance measurement to topography in AFM measurements adds useful information on electrical properties of the sample such as the dielectric constant or the conductivity.

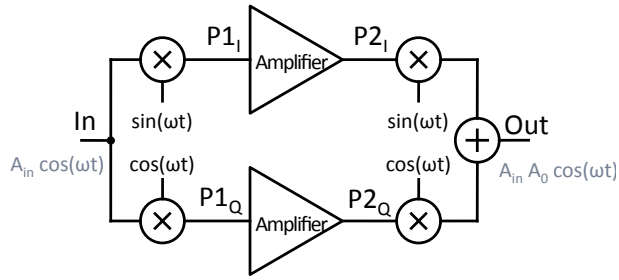

Figure 4.1: Ideal scheme of the proposed amplifier: the input signal that is mainly at the measurement frequency is multiplied with a sine and a cosine at the same frequency, amplified in the baseband and finally remodulated by the sine and cosine and summed. The resulting signal has the same frequency and phase as the input signal, but is amplified by the DC gain of the amplifier.

For example, the local low-frequency dielectric constant of thin insulating films can be measured performing capacitance measurements at different AFM tip-sample distances. The use of an appropriate model allows the extraction of the local capacitance given by the tip apex, removing the effect of the prevailing stray capacitances [30]. These measurements cannot be done on biological samples in liquid environment because the presence of ions electrically connect all the surface of the sample to the AFM tip. The locality of the impedance measurement can be recovered measuring at high frequency, tipically from tens to hundreds of *MHz* depending on ion concentration. At these frequencies the ions have no time to move following the electric field and the liquid behaves as an insulator, allowing the extraction of the local properties of the sample probed by the AFM tip.
For these reasons, we are exploring a new scheme of measurement that can reach higher frequencies but that can still be integrated on chip to take advantage from the reduction of parasitics.
The idea behind this new scheme is to realize an amplifier that, instead of amplifying all the frequencies from DC to the highest frequency of interest, is just able to amplify the frequency we are interested in and to close a feedback loop just at that frequency. This can be obtained multiplying the input signal by two sinusoid in quadrature, amplifying the resulting signal in the baseband and then remodulating it with a second multiplication (see fig. 4.1).

In this case, assuming a gain of 1 of the multipliers and a sinusoid with amplitude 1, the signals, with an input signal at the same frequency of the stimulating signals ($In = A_{in}sin[\omega t + \phi]$), we have:

$$P1_I = \frac{A_{in}}{2}cos(\phi) - A_{in}cos(2\omega t + \phi) \tag{4.1a}$$

$$P1_Q = \frac{A_{in}}{2} sin(\phi) + A_{in} sin(2\omega t + \phi) \tag{4.1b}$$

and if we assume the amplifier to have a gain A_0 in DC and great attenuation at 2ω, we can write:

$$P2_I = \frac{A_{in} A_0}{2} cos(\phi) \tag{4.2a}$$

$$P2_Q = \frac{A_{in} A_0}{2} sin(\phi) \tag{4.2b}$$

by multiplying $P1_I$ and $P2_Q$ respectively for the sine and the cosine and adding the results we obtain an output of:

$$Out = \frac{A_{in} A_0}{2} sin(\omega t + \phi) \tag{4.3}$$

that is a signal at the same frequency and phase of the input signal, amplified by $A_0/2$. That means that we close a feedback loop around this block to obtain an amplification that is independent on the gain of this stage.
The main advantage of this scheme is that the only components that are needed with wide bandwidth are the multipliers that in general can have a bandwidth greater than operational amplifiers in the same technology.

4.2 Circuit implementation

The simple scheme proposed in the previous paragraph cannot be efficiently implemented in CMOS since the required multipliers and also the amplifier generally suffer from high flicker noise if used in the baseband. The standard technique to reduce this problem is to modulate the input signal so that the signal of interest doesn't fall in DC. In our case one problem of using this technique is that the chopping multiplier should be placed directly in the delicate input node and that causes spikes due to charge injection during switching. This effect has been reduced placing a wide bandwidth buffer with moderate gain at the input. In that way the input node is shielded from spikes arising from chopping and furthermore, all the noise coming from the multiplier and the following amplifier are divided by the gain of this buffer. Low frequency noise of this buffer is not important because it will be modulated by the first multiplier and then filtered out. The same buffer is also used to convert the input signal from single-ended to fully differential, to increase linearity and range performances of the following stages.
Another problem that we have when using chopped amplifiers is that their gain is limited, since it is related to the gain of a standard amplifier at the chopping frequency. For that we decided to use a first chopped amplifier followed by a

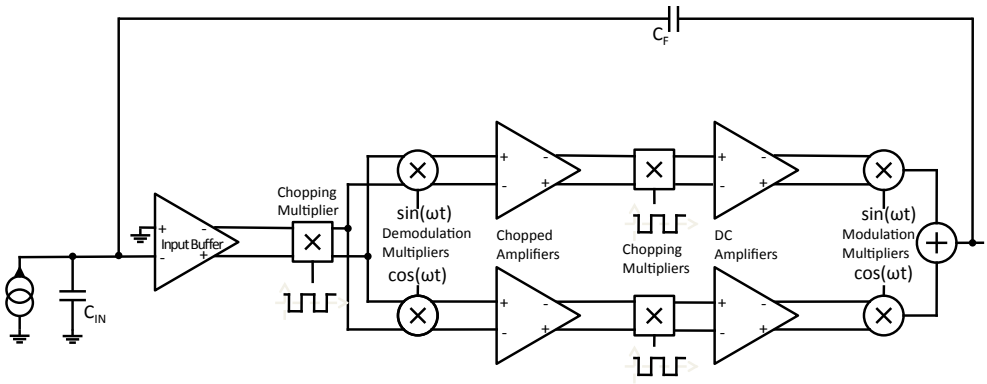

Figure 4.2: Complete block schematic of the demodulation-modulation instrument showing the input buffer, the chopping amplifier that reduces low frequency noise, the two demodulator amplifiers for in-phase and in-quadrature demodulation, the chopped amplifier, the second square-waveform chopping multiplier, the DC filter, the final remodulation multiplier and adder, and the feedback capacitor. For loop gain considerations, the input impedance has been modeled as a capacitance.

DC amplifier. In this way the noise from the second amplifier, dominated by flicker noise, is divided by the gain of the first one. The resulting scheme is shown in fig 4.2.

4.2.1 Loop gain

To calculate the loop gain we can cut the loop at the negative input of the input buffer and apply a signal $X(f)$. To simplify the analysis, we now assume the chopper off. In this case the loop voltage at the negative input of the buffer can be written as:

$$\begin{aligned} V_{-}(f) = \frac{C_f}{C_{IN}+C_f}\Bigg\{ & \\ & \left[\left[X(f)G_1(f)K_{m1} * \frac{\delta(f-f_0)-\delta(f+f_0)}{2i}\right]G_A(f)K_{m2}\right] \\ & \qquad * \frac{\delta(f-f_0)-\delta(f+f_0)}{2i} \\ & + \left[\left[X(f)G_1(f)K_{m1} * \frac{\delta(f-f_0)+\delta(f+f_0)}{2}\right]G_A(f)K_{m2}\right] \\ & \qquad * \frac{\delta(f-f_0)+\delta(f+f_0)}{2}\Bigg\} \\ = X(f)\frac{C_f}{C_{IN}+C_f}\frac{K_{m1}K_{m2}}{2}G_1(f)\left[G_A(f-f_0)+G_A(f+f_0)\right] & \quad (4.4) \end{aligned}$$

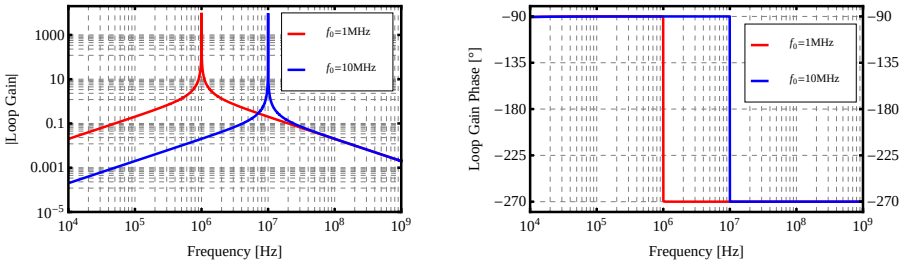

Figure 4.3: Qualitative Bode diagram of the demodulation-modulation amplifier for two different measurement frequency f_0. The loop gain has a maximum value at f_0 and the value of the maximum is independent from the chosen frequency.

where C_f is the feedback capacitance, C_{IN} is the total input capacitance, K_{m1} and K_{m2} are the gains of the first and second multipliers, $G_1(f)$ is the transfer function of the input buffer, $G_A(f) = G_{CH}(f)G_F(f)$ is the transfer function of the amplifiers working in DC, $f_0 = \omega_0/2\pi$ is the frequency of the excitation sinusoids, $*$ stands for convolution and δ is the Dirac delta function. From this equation we can see that it is possible to define a loop gain as $V_-(f)/X(f)$ and that this gain is the product of the feedback attenuation, of the gains of the two multipliers, of the gain of the input buffer and of the sum of the gain of the DC components moved by $\pm f_0$. If G_A can be approximated as a single pole gain $G_A(f) = \frac{A_0}{1+if/f_A}$, we can write the loop gain as:

$$G_{LOOP}(f) = \frac{C_f}{C_{IN}+C_f}\frac{K_{m1}K_{m2}}{2}G_1(f)\frac{2A_0\left(1+i\frac{f}{f_0}\right)}{1+\frac{i2f}{f_A}+\frac{f_0^2-f^2}{f_A^2}} \tag{4.5}$$

A qualitative Bode diagram of this loop gain for two different f_0 is shown in figure 4.3. It is possible to note that at f_0, under the hypothesis of $f_0 \gg f_A$, the loop gain magnitude can be approximated as:

$$|G_{LOOP}(f_0)| \approx \frac{C_f}{C_{IN}+C_f}\frac{K_{m1}K_{m2}}{2}|G_1(f_0)|A_0 \tag{4.6}$$

that is independent on the measurement frequency as long as we are inside the bandwidth of the first buffer. That means that it is possible to have an accurate measurement up to the bandwidth of the buffer. To study the stability of the proposed structure, we draw the Nyquist plot of the system (fig 4.4). When the measurement frequency f_0 is lower than the bandwidth of the buffer, the Nyquist diagram is an ellipse that crosses the unitary module

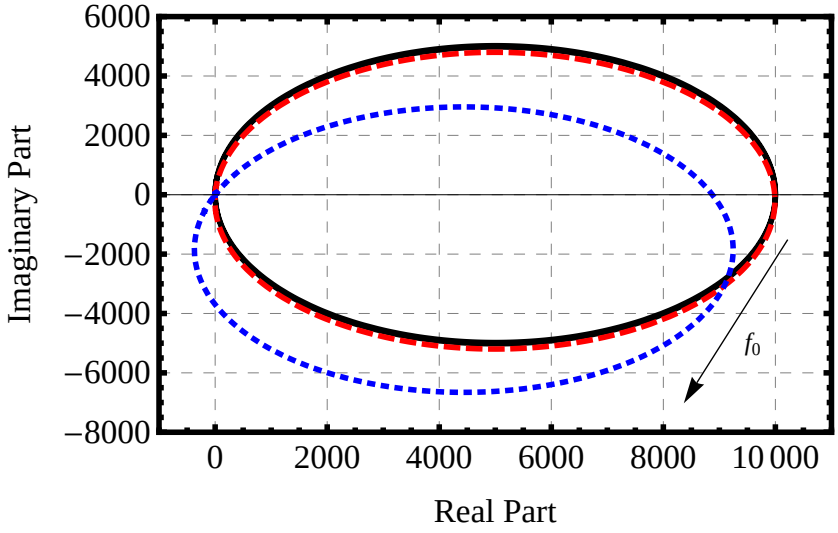

Figure 4.4: Nyquist diagram of the system for different measurement frequencies, when the input buffer is considered as a single pole amplifier. As the measurement frequency f_0 approaches the pole of the buffer, the diagram rotate clockwise. The stability limit is when the introduced phase offset reaches 90°.

circle one first time with a phase close to 90°, has a maximum value at f_0 that is purely real and then crosses a second time the unitary module circle with a phase of −90°. In this case, the diagram doesn't turn around $(-1, 0i)$, so the Nyquist stability criterion is satisfied and closed loop system is stable. When f_0 is increased, the poles of the input buffer introduce a phase offset that can be considered constant: the whole part of the Nyquist diagram where the modulus of the loop gain is bigger than 1 is a narrow frequency range around f_0 for which the phase of the input buffer can be considered constant. In any case, Nyquist stability criterion remains satisfied until the introduced phase shift is smaller than 90°. Under the hypothesis of $f_0 \gg A_0 f_A$ and $A_0 \gg 1$, the frequency interval where $|G_{LOOP}|$ is greater than 1 is $2A_0 f_A$ so it is twice the gain-bandwidth product of the amplifier working in DC. The closed loop transfer function of the system can be expressed as:

$$G_{CL}(f) = G_{ID} \frac{1}{1 - \frac{1}{G_{LOOP}}} \tag{4.7}$$

where the ideal gain G_{ID} is

$$G_{ID}(f) = -\frac{1}{i2\pi f C_f} \tag{4.8}$$

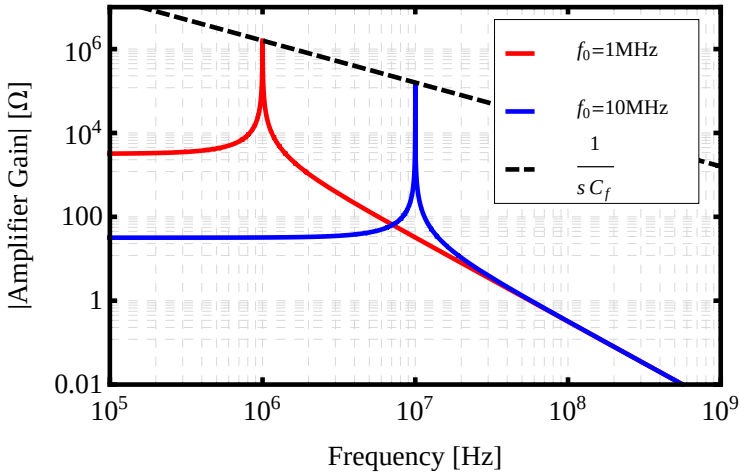

Figure 4.5: Real gain of the modulation-demodulation scheme for two excitation frequencies: note that it approaches the ideal gain $1/sC_f$ only in the proximity of the excitation frequency.

substituting the expression of G_{LOOP} (eq. 4.5) and G_{ID} into 4.7 we obtain:

$$G_{CL}(f) = \left[-\frac{1}{i2\pi f C_f}\right]\left[\frac{G_{MAX}\left(1+i\frac{f}{f_A}\right)}{\frac{1}{2}+G_{MAX}(f_0)+\frac{f_0^2}{2f_A^2}+i\frac{f}{f_A}(1+G_{MAX})+i^2\frac{f^2}{2f_A^2}}\right] \tag{4.9}$$

where $G_{MAX} = |G_{LOOP}(F_0)|$ and is plotted in fig. 4.5 for two different measurement frequencies. The first term between square brackets is the ideal gain of an integrator with C_f as the feedback capacitor, while the second one is a resonant filter with amplitude at the resonance approximatively equal to 1 if $G_{MAX} \gg 1$ and a $-3dB$ bandwidth equal to $F_A * G_{MAX}$. That means that for a narrow frequency around the measurement frequency, the gain of the system is equal to the gain of an integrator, while for all the other frequencies the gain is far smaller. So far, we have studied the circuit taking the output after the final adder. In this way it is possible to amplify the current input using the feedback capacitor, so the output in this point is linear independently from the characteristics of the other amplifying blocks. One drawback in taking the output in this point is that the signal is still at high frequency and to obtain informations about magnitude and phase of the input current, we still need an external lock-in. The need for an external instrument can be avoided, taking as the output signals, the outputs of the DC amplifiers: in fact, following

ideal gain equation, for an input signal $I_{IN}(t) = I_0 sin(2\pi f_m t + \phi)$, the output voltage is:

$$\begin{aligned} V_{OUT}(t) &= -\frac{I_0}{2\pi f_m C_f} cos(2\pi f_m t + \phi) \\ &= -\frac{I_0}{2\pi f_m C_f} \left(cos(2\pi f_m t)cos(\phi) - sin(2\pi f_m t)sin(\phi)\right) \\ &= K_{m2} V_{out,DC,Q} cos(2\pi f_m t) + K_{m2} V_{out,DC,I} sin(2\pi f_m t) \end{aligned} \quad (4.10)$$

where the last line is the characteristic equation of the last multipliers and adder. From this equation we can observe that the output signals of the DC amplifiers are:

$$V_{out,DC,I} = -\frac{I_0 sin(\phi)}{K_{m2} 2\pi f_m C_f} \quad (4.11a)$$

$$V_{out,DC,Q} = \frac{I_0 cos(\phi)}{K_{m2} 2\pi f_m C_f} \quad (4.11b)$$

so they are proportional to the imaginary and real part of the input current. The drawback of using these DC outputs is that noise and non-linearity of the final multipliers, being present in the feedback path, are directly affecting the measurement.

4.2.2 Non-idealities

To define the design objectives of the blocks of this system we analyzed the impact of some non-idealities that can affect them.
First effects of non-idealities analyzed is mismatch on multiplier-driving signals. Assuming that they are at the same frequency, they can be different because they have different amplitude or different phase from the ideal ones. These two effects can also take into account gain or bandwidth of the amplifiers or multipliers that aren't the nominal ones. In presence of these non-idealities, assuming the low-pass filter of the system to be ideal (it doesn't alter frequencies lower than the measurement frequency and it completely blocks higher ones) and neglecting the effect of the chopping amplifier, it is possible to write the output voltage when the input is a sinusoidal voltage $V_{IN}(t) = A_{IN} sin(\omega_{IN} t + \phi_{IN})$ and the multipliers run at ω_m:

$$V_{OUT}(t) = A_{IN} k_1 sin(\omega_{IN} t + \phi_{IN} + \theta_1) + A_{IN} k_2 sin((2\omega_m - \omega_{IN})t - \phi_{IN} + \theta_2) \quad (4.12)$$

where the left part of the right side of the equation is the usual gain of an amplifier, whereas the right part is present because of the time-variance of

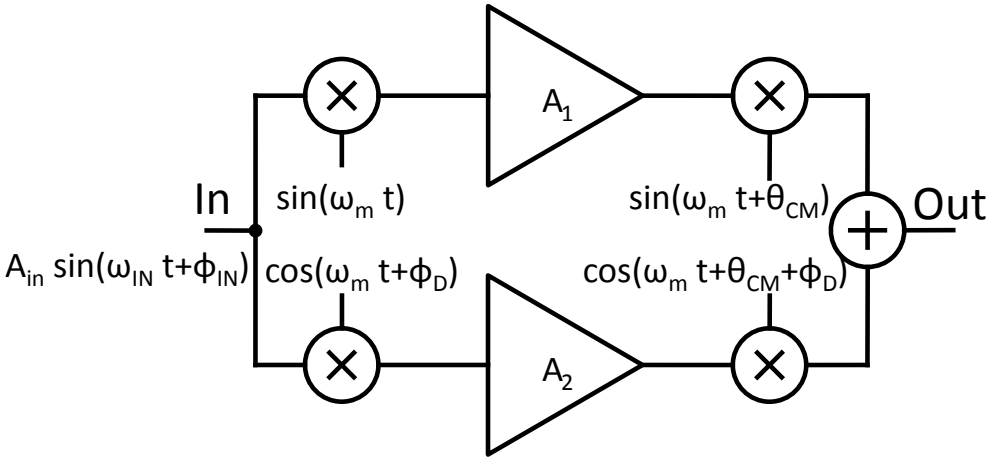

Figure 4.6: Non-idealities considered in the amplifying path: different gain for the two paths (A_1 and A_2), demodulation phase different from modulation phase (θ_{CM}) and in-quadrature path with phase difference not equal to 90° (ϕ_d).

the system and of a non perfect cancelation of the unwanted terms after the modulation multiplication and in fact isn't at the same frequency as the input. The terms in eqn. 4.12 are:

$$\begin{aligned} k_1 &= \frac{A_1 + A_2}{4} \\ \theta_1 &= \theta_{CM} \\ k_2 &= \frac{|m|}{4} \\ \theta_2 &= \theta_{CM} + \angle m \\ m &= A_1 - A_2 cos(2\phi_d) - iA_2 sin(2\phi_d) \end{aligned} \tag{4.13}$$

where A_1 is the total gain of the in-phase branch, including multipliers transfer gain, A_2 is the total gain of the in-quadrature branch, θ_{CM} is the phase shift from demodulator to modulator multipliers driving signals, ϕ_d is the phase deviation of the cosine from the ideal 90° from the sine. All these non-idealities are presented in fig. 4.6.

It is important to note than when the input frequency is ω_{IN}, the output is at ω_{IN} and at $2\omega_m - \omega_{IN}$, and these are also the frequencies present when the input frequency is at $2\omega_m - \omega_{IN}$, so when we close a feedback loop around the amplifier, to calculate the steady state output, we just need to balance the input and output of the amplifier at these two frequencies. Note also that even if the system is not time-invariant, it keeps its linearity, since the output of the sum of two inputs is the sum of the output of the two inputs taken separately.

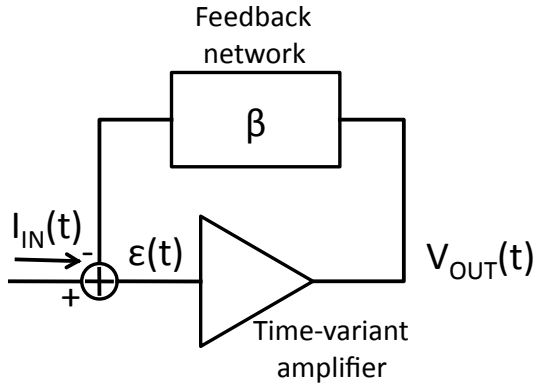

Figure 4.7: Structure of the feedback system: when the input signal is at ω_{IN}, in steady state, due to time variance of the amplifier, the error signal ϵ and the output have components at ω_{IN} and $2\omega_m - \omega_{IN}$.

Since we expect these the effects of the non-idealities to be small, we can consider them separately.
The easiest non-ideality that we can consider is the phase difference between the signals driving the demodulator multiplier and the modulator one. In that case $A_1 = A_2$ and $\phi_d = 0$, so $k2 = 0$ and equation 4.12 is just that one of a normal amplifier with added phase shift of θ_{CM}. This effect must be taken into account to guarantee the stability of the system.
More effort must be done instead to evaluate the impact of non-balanced gain in the structure. The idea we followed to compute it is that when an input signal at frequency ω_{IN} is input to the feedback system (fig. 4.7), we expect only signals at ω_{IN} and at $2\omega_m - \omega_{IN}$ to be present in the system in steady state. In this case we can write the error signal as:

$$\epsilon(t) = m \times sin(\omega_{IN}t + \phi_m) + n \times sin((2\omega_m - \omega_{IN})t + \phi_n) \tag{4.14}$$

With this input, following equation 4.12 and noting that in case of amplitude mismatch only, $\theta_1 = \theta_2 = 0$, we can write the output voltage as:

$$\begin{aligned} V_{OUT}(t) = m\,k_1\,sin(\omega_{IN}t + \phi_{IN}) + m\,k_2\,sin((2\omega_m - \omega_{IN})t - \phi_{IN}) + \\ + n\,k_2\,sin(\omega_{IN}t + \phi_{IN}) + n\,k_1\,sin((2\omega_m - \omega_{IN})t - \phi_{IN}) \end{aligned} \tag{4.15}$$

Since the feedback network can be considered linear, the two components do not influence each other in the feedback path and can be considered indepen-

dently; the steady state equation then becomes:

$$A_{IN}sin(\omega_{IN}t+\phi_{IN})-\beta V_{OUT} = m\times sin(\omega_{IN}t+\phi_m)+n\times sin((2\omega_m-\omega_{IN})t+\phi_n) \tag{4.16}$$

Combining equations 4.18 and 4.16, and separating the terms at the two frequencies it is possible to calculate the parameters of the error signal:

$$\begin{aligned} \phi_n &= \phi_{IN} \\ \phi_m &= -\phi_n \\ \begin{bmatrix} m \\ n \end{bmatrix} &= \begin{bmatrix} 1+k1\beta & k2\beta \\ k2\beta & 1+k1\beta \end{bmatrix}^{-1} \begin{bmatrix} A_{IN} \\ 0 \end{bmatrix} \end{aligned} \tag{4.17}$$

using equations 4.13 and 4.18, for $A_2 = \gamma A_1$ and assuming $\omega_{IN} = \omega_m = \omega$, we obtain the output voltage:

$$V_{OUT} = A_{IN}\frac{A_1\left[(1+\gamma+A_1\beta\gamma)sin(\omega t+\phi_{IN})+(1-\gamma)sin(\omega t-\phi_{IN})\right]}{4+2A_1\beta(1+\gamma)+(A_1\beta)^2\gamma} \tag{4.18}$$

Where the first term between square brackets is the gain of a linear amplifier and approaches $1/\beta$ if $A_1\beta \gg 1$, while the second term is a phase dependent error due to time variance of the system. As usual, the feedback mechanism tends to attenuate the effect of the unwanted term and the maximum relative error in the output amplitude due to mismatch in amplifying paths is:

$$err_{gain} = \frac{1-\gamma}{1+\gamma+A_1\beta\gamma} \tag{4.19}$$

that can be made negligible with high loop gain. Substituting the numbers on this equation, we can see that assuming a nominal loop gain of 10^4 and an error due to gain difference smaller than 10^{-5}, the gain of the two paths should be within 10%.

A similar approach can be adopted to analyze the case in which the in phase and the in quadrature paths aren't precisely 90° out of phase. In this case we can assume $A_1 = A_2$ and $\theta_{CM} = 0$. Imposing the balance of the components at ω_{IN} and at $2\omega_m - \omega_{IN}$, we can calculate the output voltage in steady state when the input and stimulating frequency are equal that is, like in the previous case, the sum of one component depending on ϕ_{IN} and another one depending on $-\phi_{IN}$:

$$V_{OUT} = A_{IN}\,A_1\frac{sin(\omega t+\phi_{IN})(2+cos^2(\phi_d)A_1\beta)+2cos(\omega t-\phi_{IN}-\phi_d)sin(\phi_d)}{4+4A_1\beta+A_1^2\beta^2cos^2(\phi_d)} \tag{4.20}$$

also in this case it is possible to calculate the maximum relative variation of the gain from the time invariant system as:

$$err_{phase} = \frac{2\,sin(\phi_d)}{2 + cos^2(\phi_d)A_1\beta} \tag{4.21}$$

and also this can be reduced increasing the loop gain of the amplifier and with a loop gain of 10^4 and a desired error smaller than 10^{-5}, the phase difference on the two channels must be $90° \pm 2.8°$.

Summing up the different effects that are present due to different path on the gain path we have:

- A phase shift present due to phase difference on the demodulation and modulation amplifiers or to limited bandwidth of the multipliers that must be considered to ensure stability
- Phase dependent errors due to mismatches on the two amplifying paths that can be reduced increasing the loop gain.

4.2.3 DC current handling

A fundamental problem arising from the utilization of the scheme in fig. 4.2 is that the presence of a DC component in the input current is not correctly handled and causes input voltage to exit from linear range. This is due both to the fact that the amplification of the modulation-demodulation structure is ideally zero for DC inputs and that the feedback capacitor isolates the output from the input in DC. For these reasons a separate feedback is needed.
One delicate point in the design is that the input node voltage is controlled by two different feedback networks and, to avoid saturation due to offsets, the loop gain must not be high for the two paths at the same frequency: this poses a limit on the minimum allowable measurement frequency.
Another limit on the lower measurement frequency comes from the particular input impedances of the two considered blocks: the high frequency path at the measurement frequency has a capacitive input impedance with a value of $C_f \times G_{loop}(f_m)$, while the DC path must have an impedance that is low at low frequencies, but increases at higher ones, to make the current flow in the high frequency path. The parallel of the two input impedances is then equivalent to a capacitor in parallel with the series of a resistor and an inductor; that has a resonation frequency $1/(2\pi\sqrt{L_{eq}\,C_{eq}})$ for which the total input impedance increases and the current flowing in the high frequency path is bigger than the input one. To limit the effect of this resonation, the frequency $1/(2\pi\sqrt{L_{eq}C_f G_{loop}})$ must be kept as low as possible. This can be achieved increasing the loop gain of the high frequency path (higher C_{eq}) and reducing

the bandwidth of the DC path (higher L_{eq} for a given DC resistance). The first technique has been adopted and a loop gain that is around 10^6 has been achieved while the second is a key point in the design of the DC network.
The easiest solution to the DC current problem is to realize a resistive feedback, active at low frequencies with relatively low input impedance. The problem with this solution comes if we try to dimension it: if we want to share the input stage with the high frequency path and have a residual offset smaller than $1mV$ at the input of the demodulation amplifier (corresponding to a signal at $100kHz$ at the output of the chopped amplifier smaller than $100mV$), the gain of the amplifier must be bigger than 10000 (corresponding to an output of $3V$ when the input is $300\mu V$). Since we must ensure the stability of the loop and two poles are present in the loop gain (one due to the input capacitance and feedback resistor and the other due to the operational amplifier), we must have that the second pole is higher than the frequency at which the absolute value of the loop gain is 1. Imposing this condition for the minimum input capacitance of $1pF$ and choosing a feedback resistor of $10M\Omega$ results in the need of an operational amplifier with a gain-bandwidth product greater than $1GHZ$ that is not easily achievable.
The requirements on the operational amplifier bandwidth can be relaxed if we introduce a zero in the loop at low frequency. A structure that can accomplish this task has already been presented in paragraph 3.2, is reported in fig. 4.8 as the loop filter and has both a gain greater than 10000 in DC and a zero at $20Hz$. In this way the condition on the stability just requires that the unitary frequency of the loop gain must be after the introduced zero. If we use a physical resistor to close the feedback, this conditions requires a resistor value smaller than $160M\Omega$ that can be satisfied.
The problem that arises if we want to use a physical resistor is that the smaller it is, the more current noise it introduces in the system and, to make it smaller than the one due to the high frequency path for frequency higher than $100kHz$ ($5nV/\sqrt{Hz}$ on a $10pF$ capacitor in typical conditions), the resistor value must be greater than $16M\Omega$ one. Such big resistors occupy huge area in silicon, have big parasitic capacitances and limit the maximum current that can be handled by the instrument.
One way to solve these problems is to divide the current of a smaller resistor to obtain a bigger equivalent one. A technique that can be used is to force the current to flow in a non-linear device before re-linearizing it with a similar one but with smaller area. One example of this technique has been presented in paragraph 3.2 and uses the MOS transistors in transdiode configuration as the non-linear device. In this case the transistors introduce a pole in the loop gain whose frequency can go from DC to $1/(2\pi g_m C_{IN})$ (g_m being the transconductance of the MOS). For C_{IN} of $1pF$ and a DC current of $10nA$ the

pole is higher than $50kHz$ and the DC path must be active at this frequency for stability reasons, limiting the effective frequency range that can be measured with the modulation and demodulation path.
Another solution is to use transistor with fixed gate voltage as the current division devices. In this case both a PMOS and an NMOS are needed to handle the input current in both directions and a parallel capacitor is needed to compensate the input pole with a zero and ensure stability. The total impedance used for current division is named Z_{NL} in fig. 4.8 and on small signal is the parallel of a transconductance g_{mNL} and a capacitance C_{NL}; it is replicated M times in the feedback of the current division block. Using this scheme, the pole due to the input capacitance on the global loop gain is always in DC (the transistors act as current sources) and the bandwidth of the DC loop can be reduced. The limit on the minimum frequency for which the feedback is active is the frequency of the zero introduced by the loop filter and is around $20Hz$. Imposing the loop gain to be higher than one at that frequency with an input capacitance of $50pF$ results in a maximum equivalent resistor $M \times R_{ATT}$ of $2.6M\Omega$. This requisite can be satisfied together with the one on noise chosing $R_{ATT} = 200k\Omega$ and $M = 10$.
The maximum DC current that can be handled with this network is limited by the stability of the current division circuit: for big currents the zero from the feedback capacitance and the transconductance of the transistors is after the transition frequency of the internal loop gain. For the designed feedback capacitance $M \times C_{NL} = 1pF$, and the gain bandwidth product of the used amplifier of $15MHz$, the current limit on the input is $250nA$. The upper limit on the bandwidth of the current that is handled by the feedback network depends on the input capacitance and for a minimum value of $1pF$ is $1.4kHz$, leaving wide frequency range for measurement with the high frequency path.

4.2.4 First stage amplifier

The first stage amplifier is a wide bandwidth amplifier that is used to decouple the virtual ground node from the interferences introduced by following multipliers and also to reduce the effect of their noise. Key requirements for this block are its bandwidth that must be at least greater than $100MHz$ that is the maximum designed operating frequency and its white noise that must be kept small. A great voltage gain is not needed in this stage if the following are designed to introduce small noise. The choice of the topology of this amplifier followed the general rule of thumb that simple wideband is granted by simple topologies, so a PMOS differential stage with resistive load has been used. This stage has good performances in terms of noise, that is generally dominated by transistor series noise, wide bandwidth due to relatively low output

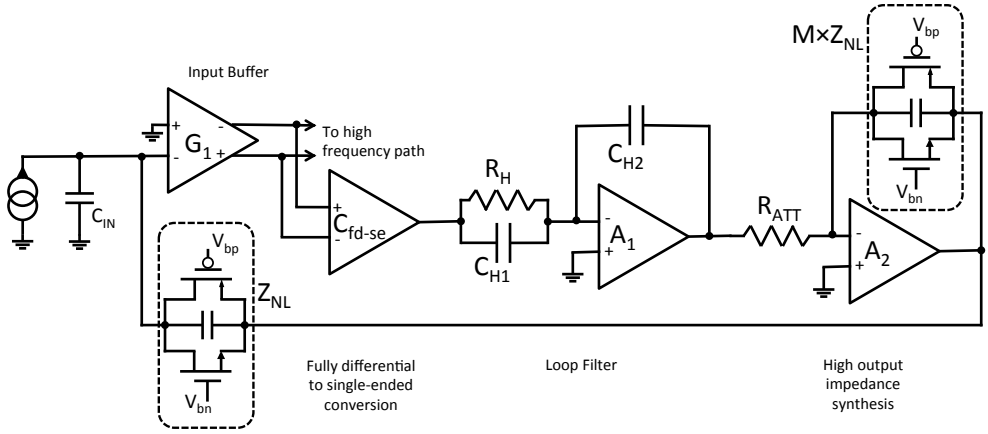

Figure 4.8: Scheme of the designed DC current feedback: the DC loop shares the same input amplifier as the high frequency path, then converts the fully differential signal to single-ended, adds a loop filter to achieve high gain at low frequency and attenuation at higher ones, and uses an high impedance to remove the input DC current. Such high impedance is realized dividing the current of a physical resistor with non-linear impedances.

resistance and can convert the single ended input voltage in a differential signal suitable to drive following multipliers. The current of the stage has been chosen of $5mA$ to have a white noise of less than $2nV/\sqrt{Hz}$) with an input capacitance of $1pF$. The resistances have been chosen to set the common mode of the output halfway between the rails (suitable for subsequent multipliers) and resulted in a value of 500Ω, that place a pole at a frequency of $300MHz$ with an output capacitance as big as $1pF$, that the capacitances of the drain of the amplifier and of the gate of the demodulation multiplier. The resulting gain is around 7, that is high enough to attenuate following stages noise.

4.2.5 Chopping multiplier

As shown in fig. 4.2, to reduce the low-frequency noise of the demodulation multiplier, the first block placed after the input amplifier is a chopping multiplier that has the input at the measurement frequency ($2\pi\omega_{IN}$) and moves it at $2\pi(\omega_{IN} \pm \omega_{CH})$ where $2\pi\omega_{CH}$ is the chopping frequency. In this way, after demodulation, the input signal isn't in DC but at the chopping frequency and lies in a spectral region where the $1/f$ noise isn't dominant. Obviously the chopping multipliers must have limited low-frequency noise and this suggests the use of square waveform, switch-based multipliers.
The design constraints that must be met by these multipliers are: they must introduce a pole with the input capacitance of the following stage above $100MHz$

(we designed it for a pole at $200MHz$, considering the input capacitance of the following stage to be $200fF$) and they must inject as low charge as possible during switching. For this reason each switch has been realized using a transmission gate with nominally matched capacitances for PMOS and NMOS, even if the input voltage is a small signal centered between the rails.
The designed multiplier has transistors with minimum length to have minimum resistance and charge injection, and PMOS have width of $30\mu m$, while NMOS $35\mu m$ to match their injected charge. The resulting equivalent resistance is of $3.8k\Omega$.
Also chopping multipliers after amplification have been realized with the same topology, but in that case the signal is around the chopping frequency (in the order of $100kHz$), so they don't have to be designed to guarantee the maximum bandwidth. In this case instead the input voltage is greater and we choose the PMOS and the NMOS to have similar transconductance, resulting in a W/L of $30\mu m/0.35\mu m$ for PMOS and $10\mu m/0.35\mu m$ for NMOS.

4.2.6 Demodulation and modulation multipliers

These multipliers are the key element of the proposed structure since they realize the frequency shift needed to have high gain over a wide range of frequency. The down-conversion and up-conversion multipliers are designed to have different characteristics: the down-conversion mixer must have:

Small input capacitance Because its input capacitance together with the resistance of the switching multiplier introduce a pole whose phase at the measurement frequency reduce the phase margin of the system, the target capacitance is in the order of $200fF$ with the previously mentioned resistances of the switching multiplier

Small offset Because its offset is amplified by the following stage before being filtered and can push it out of it linear range: assuming a gain of 100 of the following stage, the maximum allowed offset is smaller than $10mV$.

Low noise Since it comes after the first stage that hasn't high gain.

Small attenuation Since its attenuation negatively affect noise performance of the following stages.

Other aspects such as linearity and output dynamic range aren't fundamental, since the input of this multiplier is expected to be small, and also output bandwidth can be limited since the output signal is shifted at low frequency.
On the other end, the key characteristics of the up-conversion mixers are:

Wide output bandwidth At least greater than $100MHz$ since the output pole introduces a phase shift in the feedback loop.

Good linearity Since its output signal can be big and the generated harmonics fall outside from the feedback bandwidth and aren't compensated by the loop gain. Furthermore, if the inputs of the two in phase multipliers are considered the output voltage, this multiplier is in the feedback path and all of its non-linearity is directly present in the output.

Wide output voltage range Needed to obtain high dynamic range. Ideally a rail-to-rail output would be desirable, but $500mV$ can be acceptable.

To limit mismatches on the signal driving down and up -conversion mixers and to limit the number of signals driving our circuit, we choose to use the same signals to drive both the multipliers, and consequently we adopted the same architecture for both of the multipliers, tuning the required characteristics by changing the sizes of the various transistors.
The core of the designed multiplier is a MOS transistor (M_M) biased in the linear region (fig. 4.9a) [31]: in this case the current flowing between drain and source is:

$$I_{DS} = \mu_n C_{OX} \frac{W}{L} (v_b \times v_a + (V_{GS} - V_T) v_b) \tag{4.22}$$

and has two terms: one that depends on the product of the two inputs and the other one that is proportional to the drain to source voltage. If we are able to read this current while we apply both drain to source voltage and gate to source voltage, by subtracting the unwanted part of the current, we can obtain a current that is proportional to the product of the two voltage inputs.
One circuit that allows us to impose the drain and source voltages while reading the current flowing in the transistor is presented in figure 4.9b. It is composed by the current mirror M_2 and M_3 and by the follower M_1 and M_2. The follower is used to impose the voltage to the source and drain of the transistors, while the mirror replies the current in the output branch. Proper bias of the structure is obtained using a PMOS for current bias and an $R \parallel C$ biased with M_b that, increasing the drain voltage of M_1, assures its operation in the saturation region (fig. 4.9c).
The subtraction of the unwanted component of the drain current is obtained replicating the structure with another MOS in the ohmic region and with gate driven by a signal voltage equal to v_a but with opposite sign. The subtraction of the two currents is obtained using two output resistances and a following differential amplifier for the down-conversion mixer, while for the up-conversion mixer it is obtained using one output resistor and an additional current mirror.

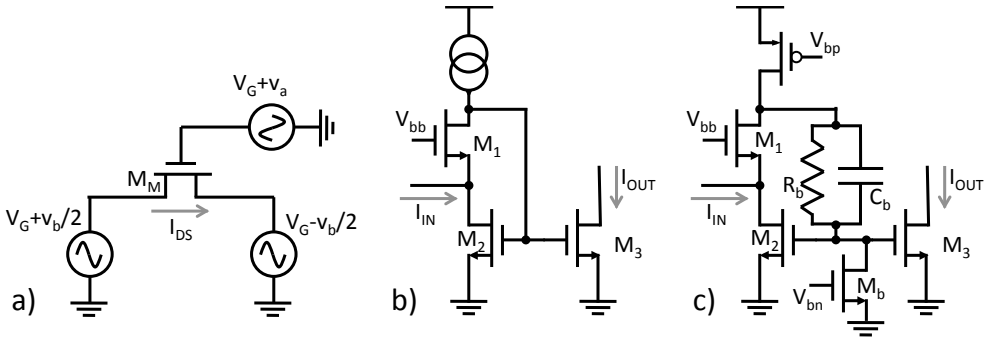

Figure 4.9: a) Central element of the designed multiplier b) Principle schematic of the circuit used to impose the drain and source voltages to the central MOS and contemporary read its current c) Full schematic of b) with current biases and bias network $C_b \parallel R_b$ used to extend DC input range.

This solution is required to obtain a single-ended output from the differential inputs and assures the wide bandwidth necessary for this multiplier.
The design of these blocks required numerous simulation in terms of gain, bandwidth, noise and mismatch that resulted in the final dimensions shown in table 4.1. With these sizes the down-conversion mixer has a gain of 0.96 with a differential signal of $200mV$ on the external input, an output voltage noise of $34nV/\sqrt{Hz}$ with a corner frequency of $12kHz$. The total current consumption is of $12mA$ and the capacitance of the input coming from the previous stage is of $186fF$. The capacitance that must be driven by the external input is of $3.2pF$, but it doesn't pose problems for the stability of the system. The simulated offset, due to both process and mismatch variations, has a standard deviation of $5.7mV$ and can cause problems with the next stages; for this reason the down converter mixer has two resistances at the output nodes that can be driven externally to compensate the offset up to $15mV$.
The up-conversion mixer shares the same external excitation voltages of the down-conversion one and has smaller current-mirroring components because it must have wider bandwidth. The gain obtained with this multiplier is 0.5 with a maximum output peak voltage of $250mV$ and a total harmonic distortion smaller than 5%.

4.2.7 Chopped amplifier

After the down-conversion mixer the input signal is translated at the chopping frequency and can be amplified using a CMOS amplifier without paying too much the flicker noise. One critical aspect of this circuit is that the offset of

Table 4.1: Nominal values of the components of the designed mixers

	Down-Conversion	Up-Conversion
M_M	$40\mu m/1\mu m$	$15\mu m/0.35\mu m$
M_1	$600\mu m/0.7\mu m$	$600\mu m/0.7\mu m$
M_2	$110\mu m/2\mu m$	$25\mu m/0.35\mu m$
M_3	$200\mu m/2\mu m$	$50\mu m/0.35\mu m$
M_4	$33\mu m/7\mu m$	$3.3\mu m/0.7\mu m$
I_{TOT}	$12mA$	$19mA$
R_b	$10k\Omega$	$10k\Omega$
C_b	$300fF$	$300fF$

the previous multiplier, instead, is in DC and, when it is amplified, it must not saturate the amplifier, and this poses a maximum limit to the acceptable gain. Having a simulated offset of $5mV$ of standard variation, the maximum gain must be in the order of 100. Bandwidth requirements for this amplifier aren't very stringent, but the first pole must be well after the chopping frequency (in the order of $100kHz$) so that the input signal is correctly amplified without phase shift, allowing the subsequent chopping multiplier to be driven with the same signal as the previous one.
A simple structure that can meet the stated requirements is a 5 transistor amplifier (fig. 4.10a). With this structure a gain of 100 with a bandwidth of $17MHz$ and a noise density at $100kHz$ of $8nV/\sqrt{Hz}$ has been achieved. The output common mode voltage is kept at the correct value using the switched capacitor network shown in fig. 4.10b, that reads the output mean voltage and modulates the tail current of M_5 to keep it at V^*_{cm}. V^*_{bn} is the nominal voltage needed for M_5 to carry the nominal current of $250\mu A$ and ϕ_1 and ϕ_2 are two non-overlapping phases.

4.2.8 DC amplifiers

The main objectives of the DC amplifiers (one for the in-phase channel and the other for the in-quadrature one) are to have an high gain at the measurement frequency and to place the dominant pole in the loop gain before the other singularities that can make the system unstable. A good topology for these characteristics is the integrator: it has really high gain in DC, limited only by the gain of the operational amplifier and then there is a wide frequency range with a slope of $-20dB/decade$ that can be placed changing the values of R and C. In our case a fully differential integrator is preferable since we have fully

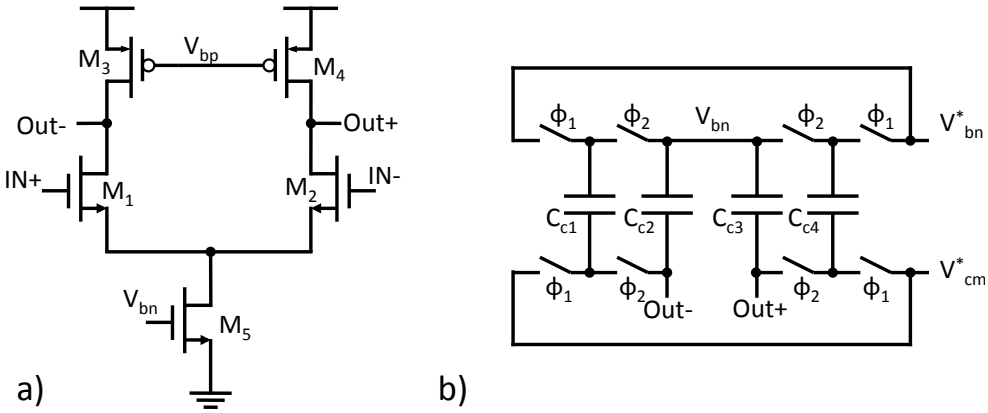

Figure 4.10: a) Schematic of the fully differential amplifier that amplifies the chopped signal b) Schematic of the common mode feedback network for the amplifier.

differential blocks before and after the amplifier. For this purpose a common mode feedback network is needed and in this case has been realized using continuous time elements because high frequency spikes due to capacitance switching won't be filtered after this block. The schematic of the amplifier and the common mode feedback network are shown in fig. 4.11. The gain obtained with this configuration is around 10^7 and becomes unitary at a frequency of $10Hz$, resulting in a frequency range where the system has loop gain greater than one that is wide:

$$BW = \beta\, 2\, G_{input}\, \frac{2}{\pi}\, \frac{G_{M1}}{2}\, G_{CH}\, \frac{2}{\pi}\, GBWP_{lpf}\, \frac{G_{M2}}{2} \approx 680Hz \tag{4.23}$$

Where β is the partition loss of the input capacitance and has been considered 1/100 in this calculation (corresponding to an input capacitance of $10pF$), G_{input} is the gain of the input buffer (7 in this design), the two factors $2/\pi$ are the gains of the chopping multipliers, G_{M1} is the gain of the first multiplier (0.96), G_{CH} is the gain of the chopping amplifier (100), $GBWP_{lpf}$ is the gain bandwidth product of the loop filter ($100Hz$) and G_{M2} is the transfer gain of the final multiplier (0.5). To obtain this frequency response, the feedback capacitance has been chosen to be $10pF$ and the input resistance must be $1.6G\Omega$. Such high value of resistance has been obtained exploiting the current division technique shown in par. 3.2, realizing a physical resistor of $1M\Omega$ and two attenuating stage with a division factor of 40.
The common mode output voltage is managed reading its value using a resistive partition, comparing it with the desired value and acting on the positive input of the two integrators. The stability of this feedback loop is guaranteed

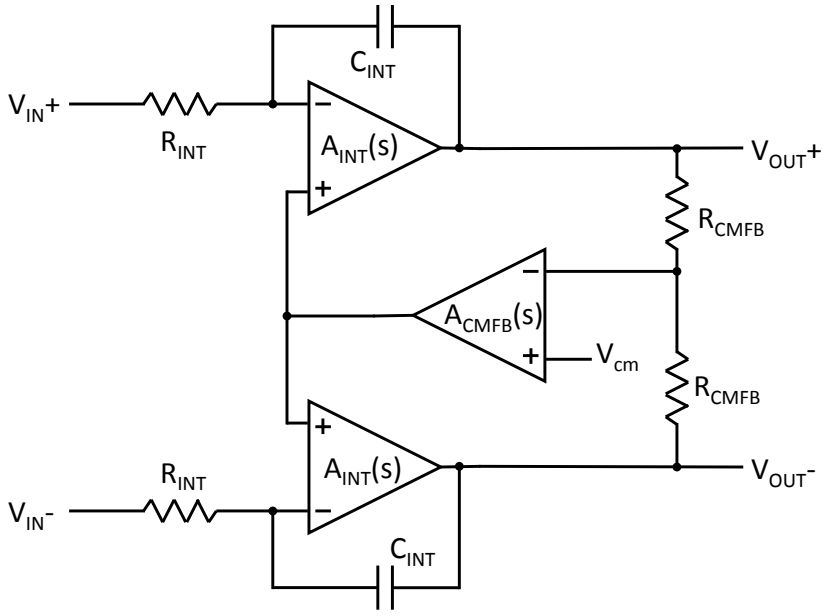

Figure 4.11: Schematic of the fully differential integrator used as the loop filter for the designed instrument. The output common mode voltage is read using a resistive partition and controlled modifying the positive input node of the two single-ended integrators.

choosing a gain-bandwidth product of the operational amplifier smaller than the closed loop frequency of the integrators: in this way, when the second pole of the integrators becomes active, the loop gain of the common mode feedback is already smaller than one.

4.3 Simulation techniques

The simulation of this kind of system requires the use of different simulation techniques to minimize the time required to verify the design considerations. Standard linear blocks like the operational amplifiers, buffers and in general all the blocks that do not shift the input signal in frequency, have been simulated calculating the DC bias condition and the AC parameters that were sufficient to verify gain, bandwidth, noise, dynamic range and bias.
Non-linear blocks like the multipliers cannot be simulated in this way: their behavior depends strongly on time-variant signals on their input and parameters like their transfer gain, bandwidth and noise must be simulated taking into account them. This can be done simulating these blocks in time and waiting until a steady state is reached. Although for some simple blocks this is feasible there are techniques that are way more efficient for this purpose. One of them is the Periodic Steady State analysis (PSS) [32] in which only one period of the fundamental frequency is simulated in time and initial conditions are computed using Newton method in order to have them as similar as possible as the final conditions after one period. With this technique a smaller number of periods can be simulated before obtaining the steady state condition. Once the steady state has been computed, perturbation methods can be used to calculate the effects of small signals and this has been exploited to compute multipliers noise.
Also the whole system performances cannot be simulated using AC parameters and during the various stages of the project they have been simulated either in time-domain or using PSS. Time domain simulations are quite expensive in terms of time because the steady state is reached with a time that is inversely proportional to the closed loop bandwidth of the system (in the order of tens of milliseconds) while all the internal signals run at the measurement frequency that can be as fast as $100MHz$. Nevertheless time domain simulations are more robust in terms of numerical errors and always converge, furthermore in case of instability, they are more likely to show which are the critical components. PSS simulations instead, converge more rapidly to the steady state solution and for that are useful to test the performances of a working design in multiple conditions, but they can cause convergence problems or even converge to an unstable operating point. The first problem can be solved either by loosen-

ing convergence parameters or by simulating the system for some time with a transient analysis before running the PSS. The second problem instead can only be solved using higher initial transient simulation time. Another problem arising from PSS analysis is that in our circuit, besides the measurement frequency, other tones are present: the chopping frequency and the frequency for the common mode feedback of the chopped amplifier. These two frequencies can be up to a factor of one thousand smaller than the measurement frequency so the PSS analysis, that must simulate the system in time for at least one period of the slowest signal, cannot be really efficient. One way to avoid this is to turn off chopping and common mode feedback (substituting the latter with a continuous time network), in this way the efficiency of the PSS is regained, but the simulated system is not precisely the realized one.
The designed instrument, due to its particular structure, needed various level of simulations: firs of all it has been simulated with all the ideal components to test the viability of the basic idea behind it, then the instrument has been redesigned with elements with realizable characteristics. Then all blocks were designed and tested both alone and inside the complete architecture to highlight the critical aspects of each one of them, and finally the whole instrument realization has been tested in various configurations.
The ability of the circuit to amplify currents with frequency up to $100MHz$ over imposed on DC currents up to $10nA$ with both polarities, with different phases respect to the excitation signals has been simulated obtaining outputs that agree with the proposed theory of operation. The high gain of the feedback loop at the measurement frequency results in a gain at the center of the bandwidth that is really close to the ideal gain $1/(i\,2\,\pi\,f_m C_f)$.

4.4 Experimental results

The designed chip has been realized in a $1.1mm \times 1.65mm$ CMOS $0.35\mu m$ chip (fig. 4.12) and its full experimental characterization is ongoing. Nevertheless the results of the first measurement confirm its functionality. The system has been initially tested applying at its input the equivalent of a capacitance step: this has been achieved using a physical capacitance of $100fF$ integrated on the chip as a test impedance and modulating the input voltage sinusoid, with a square waveform, obtaining an amplitude variation between $0V$ and $5mV$. This test has been made with various measurement frequencies, ranging from few kHz up to $20MHz$. The results with the maximum frequency are shown in fig. 4.13, where input and high-frequency output voltage of the system are plotted. From these measurement we can observe that the total input impedance is in the order of $800fF$ and this can be due to an additional par-

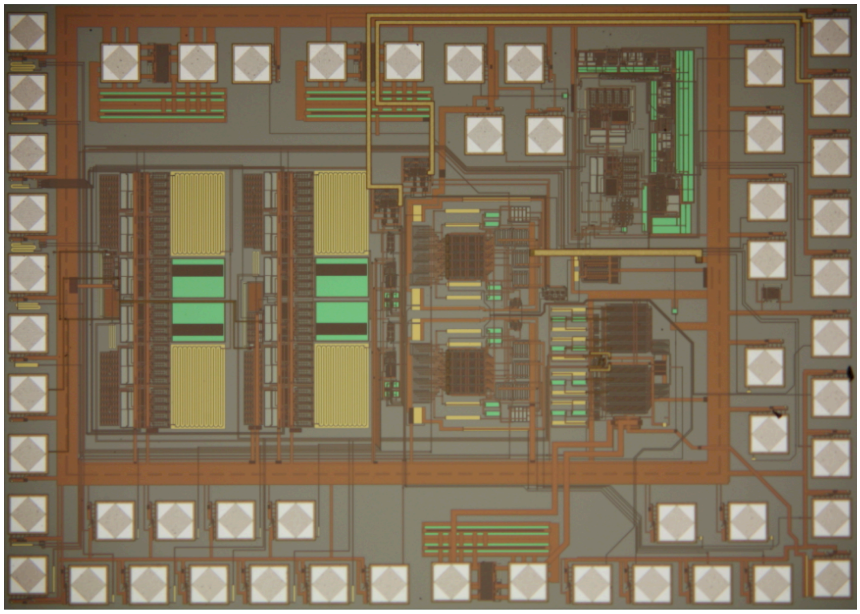

Figure 4.12: Photograph of the realized chip that occupies an area of $1.8mm^2$, dominated by the DC filters.

asitic capacitance of $700fF$ on the input pad; this is a reasonable value since the input pad leading to the integrated capacitance is close to the input pad for the external impedance. On the left part of fig. 4.13 it is also possible to see that the time constant of the system is around $10ms$ and therefore is related to the bandwidth of the system around the measurement frequency. The measured value is smaller than the designed, but it is constant for different measurement frequencies, confirming the theoretical considerations that lead to the design of the circuit.
Further measurements with un-modulated input signal confirmed steady state operation in a measurement frequency range between $2kHz$ and $120MHz$. At higher frequencies the total phase delay of the high frequency components inside the loop causes the system instability. The frequency range has also a lower limited due to the instability caused by the interaction between the high-frequency path and the DC handling circuit, as theoretically predicted. Test performed on the DC handling circuit shown its functionality up to a DC current of $300nA$ in both directions.

In the same experimental conditions, also the output of the differential amplifier driving the final multipliers have been measured (fig. 4.14). As expected and according to simulations, these two outputs evolve with the same time

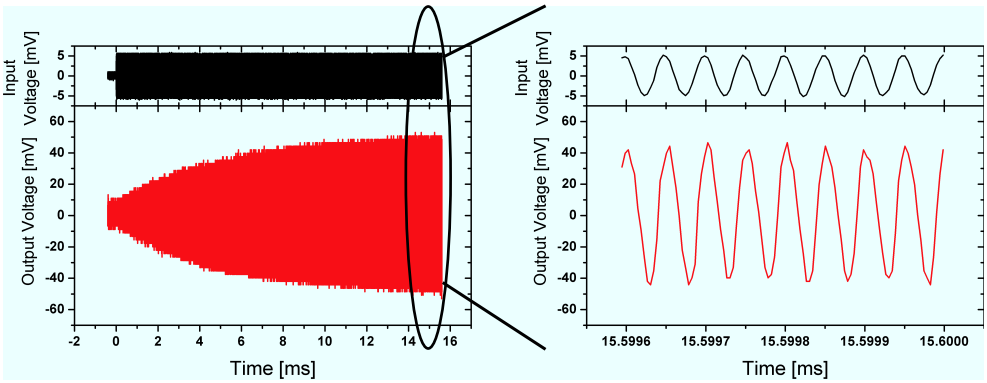

Figure 4.13: Output and input voltage of the system when stimulated with a step modulated at $20MHz$. In this case the total input impedance can be estimated as a capacitance of $800fF$. On the left part of the figure it is possible to see that the system reaches its steady state with a time constant of about $10ms$, related to the bandwidth of the system around the measurement frequency. On the right part, a zoom on the previous figure shows the phase relation between the input and the output. As expected it is around $0°$.

constant as the high-frequency output and they can be used to have a quantitative estimation of the real and imaginary part of the impedance that is measured. Although they suffer from the problems arising from having an active device on the feedback branch of the system, the measurement of their value is very simple and doesn't require the instrumentation needed to demodulate the high-frequency output.

The realized instrument has been used to measure a test impedance over its operating frequency range. The test impedance has been realized with discrete components and is the series of a $15pF$ capacitor and a $100k\Omega$ resistor having a parallel parasitic capacitance of $500fF$. In fig. 4.15 are presented the results of the magnitude and phase of the measured impedance. They have been derived from oscilloscope read of the magnitude and phase of the high-frequency output respect to the input signal and assuming an ideal transimpedance gain of $-\frac{1}{2\pi f 100fF}$. Good agreement between experimental results and theoretical expectations can be observed.

4.5 Conclusions

In this chapter the design of an instrument for impedance measurement based on a novel topology has been presented. The central part of the instrument is an amplifier based on demodulation and remodulation: the input signal is multiplied with a sinusoid to translate it to a lower frequency where it is enlarged

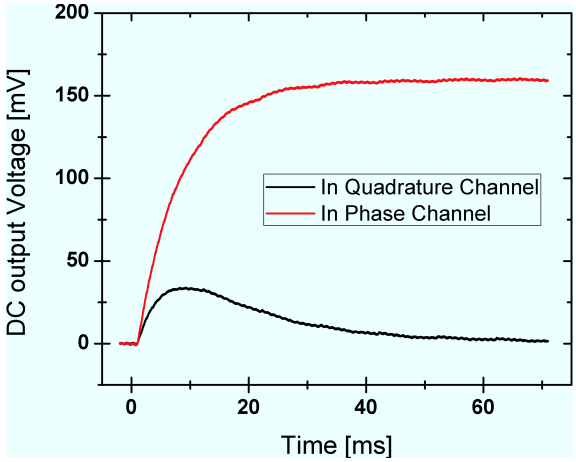

Figure 4.14: Output voltages of the amplifiers driving the final multiplier in the same experimental conditions of fig. 4.13. As can be seen in response to a sinusoidal step in phase with the stimulation voltage, the system reacts increasing the driving voltage of the in phase multiplier.

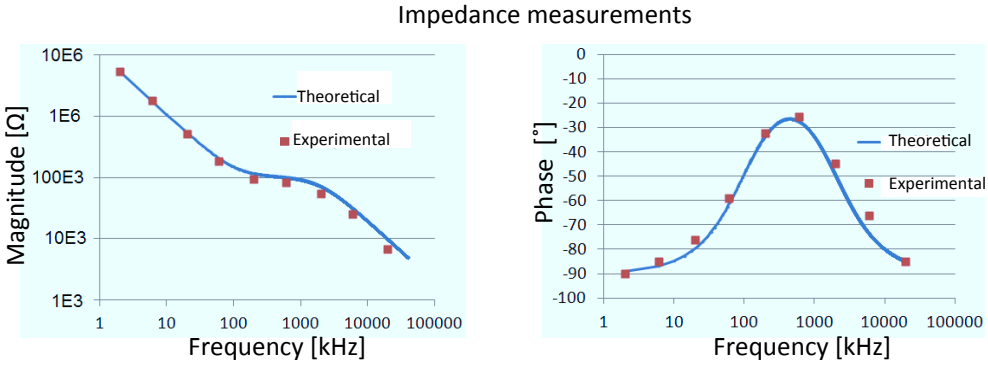

Figure 4.15: Measurement of the impedance of a calibrator realized with the parallel of a capacitance of $0.5pF$ and a resistance of $100k\Omega$ in series with a $15pF$ capacitance, in the frequency range from $1kHz$ and $20MHz$. On the left side is presented the comparison between the expected theoretical value of the magnitude of the impedance and its measurement, while on the right side is presented the comparison of the two phases. The errors in the measurement fall inside the tolerance of the used passive devices.

using a classical amplifier before being remodulated. This structure is used as the amplifying block of a feedback system and has the advantage over classical structures to have a loop gain that is almost independent on frequency. In this way it is possible to obtain accurate impedance measurement also at high input frequencies.
The development of the instrument started from the definition of the characteristics of the blocks that constitutes it and went on solving the various problems arising from their implementation in CMOS technology. For instance chopping technique has been added to cope with low-frequency noise of the amplifying part and a specific DC current handling block has been designed.
The work presented in this chapter resulted in the design of a CMOS integrated chip that has been realized occupying an area of $1.1mm \times 1.65mm$ (fig. 4.12) and proved its functionality in preliminary tests, confirming design considerations. The testing of the chip showed the criticality of the offsets in the high-frequency path that can be amplified and can lead to saturation of the low-frequency blocks. At the moment they must be compensated manually in order to obtain a functional system. Paying attention to these aspects, the system has proved its functionality in the frequency range between $2kHz$ and $120MHz$, thus extending the bandwidth of the previously realized systems by almost two order of magnitude.

Conclusions

In this thesis work many concepts regarding impedance measurements in biological samples have been investigated and different circuital solutions to address specific problems have been presented.
First of all a fully functional instrument for cell counting, based on impedance measurement technique, has been realized and experimentally characterized. Careful electrode design, together with the choice of low noise electronic components, supported by on board computing lead to the realization of an instrument that is in line with state-of-the-art instrumentation regarding sensitivity and counting rate, while drastically reducing device dimensions.
The need for a more flexible instrument, able to measure magnitude and phase of the impedance, lead to the design of a fully integrated silicon chip featuring a low-noise front-end amplifier and the circuitry to perform two phases lock-in multiplication and analog to digital conversion. The chip, surrounded with a signal generator and an FPGA module for control, digital filtering and communication with a PC, resulted in an instrument with excellent noise characteristics.
In this work it has also been presented a novel instrumentation topology, suited to extend the bandwidth of the impedance measurement toward frequencies that are higher than the ones achievable with the standard transimpedance one. This can be achieved demodulating the input signal, amplifying it, remodulating it and then closing a feedback loop. Thanks to the feedback it is possible to obtain linear amplification, while the demodulation and remodulation technique leads to high loop gain ideally at any frequency. The solutions to integration problems of this system have been presented and a functional prototype has been realized. The upper bandwidth limit of this chip has been found to be $120MHz$, almost two order of magnitude better than what achieved with the standard topology.

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