POLITECNICO DI MILANO
Dipartimento di Elettronica e Informazione
DOTTORATO DI RICERCA IN INGEGNERIA DELL'INFORMAZIONE

ELECTRICAL CHARACTERIZATION AND PHYSICAL MODELING OF UNIPOLAR/BIPOLAR RESISTIVE SWITCHING MATERIALS

Doctoral dissertation of:

Ing. Federico NARDI

Advisor:
Prof. Daniele Ielmini

Tutor
Prof. Angelo Geraci

Supervisor of the Doctoral Program:
Prof. Carlo Fiorini

2011 – XXIV

Abstract

≪Nam Sibyllam quidem Cumis ego ipse oculis meis vidi in ampulla pendere, et cum illi pueri dicerent: Σιβυλλα τι Θελεις; respondebat illa: αποΘανειν Θελω.≫

For Ezra Pound, il miglior fabbro.

Thomas Stearn Eliot 1922, THE WASTE LAND

In recent years the technology has marked the deepest changes in our lives and culture. The impressive development of new electronic devices is by far the fastest progress that human kind has ever experienced. The continuous demand of new portable, low-cost, low-power devices has forced a huge effort in $R\&D$, pushing the limits of the current technology. The demand of memory supports represents an excellent example of such rush toward the limits of our technology. Flash memory, representing the main stream memory technology, experienced an impressive development being, at the time of writing, at the 25 nm node. The foresee of the intrinsic limit of Flash scalability, is also driving a tremendous amount of research in completely new memory technologies. This research is yielding to an exciting activity directed to a deeper physical understanding and, at the same time, to a fast technology development.

This Doctoral Dissertation will be focused on Nickel Oxide-based and Hafnium Oxide-based Resistive-switching RAM (RRAM). The work describes working principles, physical/numerical modeling, reliability issues and innovative memory structures of RRAM technology. Experimental characterization has been a crucial step in this task, being the starting point of physical understanding and thus modeling.

The first Chapter briefly describes the non-volatile memory market scenario, explaining the Flash technology basics showing its limits and presenting a few solutions that have been proposed. A first introduction

on RRAM technology will be discussed, presenting the basic working principle and making clear already how the research is all but close to a complete understanding of RRAM dynamics and behavior.

The second Chapter will give a deep insight into the different kind of memory structures that have been electrically tested. The basic mechanisms for program operation in RRAM devices will be described from a more electrical point of view, showing the feasibility of growth/dissolution control of the conductive filament, helping us in unveiling its real nature.

The third chapter will focus on physical and numerical modeling of unipolar/bipolar resistive switching, starting from the experimental results obtained on NiO-based and HfO-based devices. We will also introduce the concept of universal reset for unipolar/bipolar RRAM and the innovative concept of complementary switching, a new operation mode in non-polar RRAM.

The fourth Chapter will focus on scaling. In particular will be described a possible approach to scale down the reset current, which is probably the biggest issue in RRAM, exploiting 1T1R devices. By the use of CAFM technique we will try to direct manipulate single conductive filament thus exploring program performances of future ultra-scaled devices.

The fifth Chapter will be completely devoted to reliability issues. We will start with the study of the feasibility of a RRAM multilevel cell (MLC). Data retention will be then discussed from a statistical point of view. We will show prediction of our models, illustrating how a trade-off between reset current and data retention is necessary. The aspect of pulsed program in RRAM will be presented showing the presence of a trade-off between reset current and the onset of set-reset instability. We will conclude showing Random Telegraph Signal Noise (RTN) affecting high resistive states, and we will describe a physics-based model based on these evidences.

In the last Chapter a completely new approach to RRAM technology will be presented. We will report our results obtained on the synthesis and the characterization of self assembled Ni-NiO core-shell nanowires (NW) for cross-bar memory implementation. This work is particularly interesting in future prospectives since the so-called bottom-up approach could lead to a very aggressive scaling at a relatively low-cost.

Riassunto

Negli ultimi anni l'evoluzione della tecnologia ha tracciato profondi cambiamenti nella nostra vita e cultura. L'impressionante sviluppo di nuovi dispositivi elettronici rappresenta di gran lunga il più veloce progresso che l'umanità abbia mai sperimentato. La continua domanda di dispositivi portatili, a basso costo e a basso consumo energetico ha richiesto un enorme sforzo da parte del settore $R\&D$, spingendo sempre più avanti i limiti delle attuali tecnologie. La domanda di supporti di memoria rappresenta un ottimo esempio di tale corsa verso i limiti della nostra tecnologia. Le memorie Flash, che rappresentano attualmente la principale tecnologia di memoria, hanno registrato un impressionante sviluppo trovandosi, al momento in cui si sta scrivendo, al nodo 25 nm. La previsione del raggiungimento dei limiti intrinseci di scalabilità delle memorie Flash è da stimolo per una vasta attività di ricerca verso tecnologie di memoria completamente nuove. Questa ricerca sta dando vita ad entusiasmanti attività rivolte ad una più profonda comprensione fisica e allo stesso tempo ad un rapido sviluppo tecnologico.

Questa Tesi di Dottorato sarà focalizzata su memorie a switching resistivo (RRAM) basate su ossido di Nickel e ossido di Afnio. Il lavoro analizza principi di funzionamento, modellistica fisica/numerica, problemi di affidabilità e strutture di memoria innovative della tecnologia RRAM. La parte di caratterizzazione sperimentale è stata fondamentale in questo attività di ricerca, essendo il punto di partenza della comprensione fisica e quindi della modellistica.

Il primo capitolo descrive brevemente lo scenario del mercato delle memorie non volatili, spiegando i funzionamenti di base della tecnologia Flash, mostrandone i limiti e presentando alcune possibili soluzioni architetturali a questi problemi. Sarà presentata anche una prima introduzione sulla tecnologia RRAM, discutendo i principi di funzionamento di base e chiarendo come la ricerca si stia spingendo verso una completa comprensione delle dinamiche e del comportamento di tale tecnologia.

Il secondo capitolo darà una visione approfondita dei diversi tipi di struttura di memoria che sono stati testati elettricamente. I meccanismi

di base per la programmazione dei dispositivi RRAM saranno descritti da un punto di vista più elettrico, mostrando la possibilità di crescere/dissolvere in maniera controllata il filamento conduttivo al fine di cercare di svelarne la vera natura.

Il terzo capitolo si concentrerà sulla modellistica fisica e numerica dello switching resistivo unipolare/bipolare a partire dai dati sperimentali ottenuti su dispositivi basati su NiO e HfO. Sarà anche introdotto il concetto di reset universale per RRAM unipolari/ bipolari e l'innovativo concetto di switching complementare, un nuovo metodo di programmazione per RRAM non polari.

Il quarto capitolo si concentrerà sullo scaling. In particolare sarà descritto un possibile metodo per ridurre la corrente di reset, che rappresenta probabilmente il problema più grande nella tecnologia RRAM, sfruttando dispositivi 1T1R. Tramite l'utilizzo di tecniche CAFM si cercherà di manipolare direttamente il singolo filamento conduttivo così da esplorare le prestazioni della programmazione in futuri dispositivi ultra-scalati.

Il quinto capitolo sarà completamente dedicato ai problemi di affidabilità. Inizieremo con lo studio della fattibilità della realizzazione di una cella RRAM multilivello (MLC). Sarà poi discussa la ritenzione del dato da un punto di vista statistico. Dopo aver mostrato le previsioni dei modelli realizzati, sarà evidenziato come un trade-off tra corrente di reset e ritenzione del dato sia necessario. Verrà analizzata la programmazione impulsata di dispositivi RRAM mostrando la presenza di un trade-off tra la corrente reset e l'insorgere di instabilità di set-reset. Il capitolo si concluderà mostrando come il Random Telegraph Signal Noise (RTN) interessi gli stati alto resistivi, introducendo un modello fisico basato su queste evidenze.

Nell'ultimo capitolo sarà presentato un approccio completamente nuovo alla tecnologia RRAM. Saranno riportati i risultati ottenuti sulla sintesi e caratterizzazione di Ni-NiO core-shell nanowires autoassemblanti per l'implementazione in strutture di memoria cross-bar. Questo lavoro è particolarmente interessante in prospettive del futuro sviluppo del cosiddetto approccio litografico bottom-up il quale potrebbe portare ad uno scaling molto aggressivo a relativamente a bassi costi.

Contents

Chapter 1

RRAM technology: state of the art

Apri la mente a quel ch'io ti paleso
e fermalvi entro; che non fa scienza,
senza lo ritenere, avere inteso.

Dante, Paradiso V 40-42

The ever increasing demand for high density and low cost storage devices has lead the tremendous development of today's non-volatile market leader Flash technology. Besides that, new technologies are emerging as interesting solutions in post-Flash scenario. In this chapter, after a brief introduction of non-volatile memory market, a first overview to post-Flash technology will be done.

1.1 Non-Volatile Memory: An Introduction

The fast adoption of electronic low-volume portable devices with low power consumption and high performances is pushing up the demand of non-volatile solid-state memories. Smart phones, music players, tablets and Solid State Disks (SSDs) are only few examples of the ubiquitousness and the ever increasing role played by non-volatile memory (NVM) in changing our lifestyle. From a simple concept in the early 80's, Flash

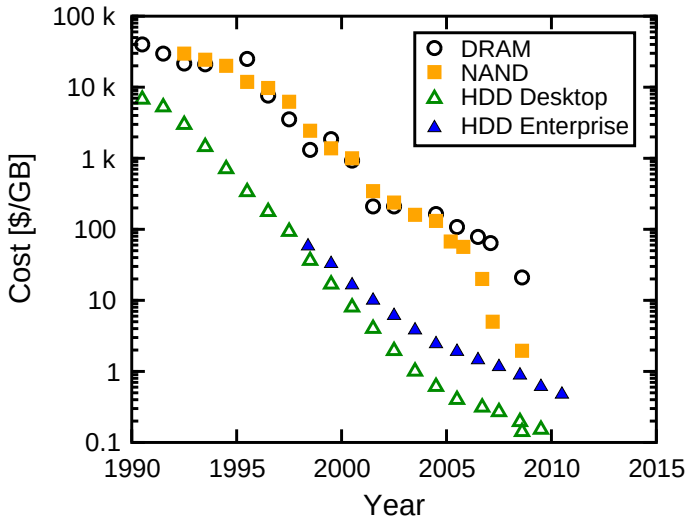

Figure 1.1: Cost per GigaByte (GB) of Desktop and Enterprise hard disk drives (HDD) compared to the cost reduction trend in DRAM and NAND memory (recompiled from [2])

memory, the actual market leader of NVMs, grew up and generated close to $23 billion in worldwide revenue in 2007 [1], representing one of the many success stories in the semiconductor industry.

This incredible growth was essentially driven by the Moore's Law that lead to dramatic reductions in unit cost over the past few decades for the entire semiconductor industry. This enables NVM to fulfill the requirement for products of ever higher density while continuously pulling down market prices. As can be seen in Fig. 1.1, the cost of Flash memory has fallen from $10 000 per gigabyte of the mid 90's, approaching $1 per gigabyte in 2010 [2]. This continuous reduction of the memory price enabled creation of new markets that in turn largely repaid the efforts devoted for the manufacturing of memory chips with increased performances and functionality. All these improvements were made possible by the innovation of the industry along different fronts, first of all the great advances in lithography which is fundamental for the area scaling. A great contribution was also provided by innovative self-aligned technologies, the introduction of NAND memory to reduce memory cell size, the introduction of multi-level cell technology and wafer size increasing from 150 mm in 1987 to 300 mm in recent years [1].

Despite their still high cost per bit with respect to magnetic hard disk drives, semiconductor memories resulted the winning solution in all the consumer products requiring light weight, low size, low power

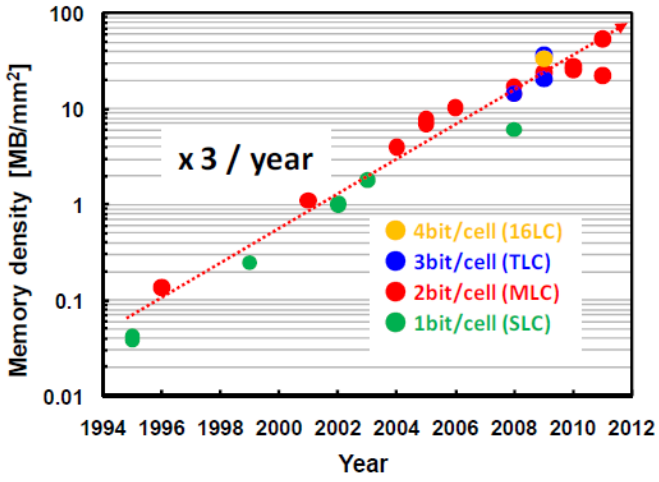

Figure 1.2: Observed trend in NAND Flash memory capacities presented at ISSCC in the past 12 years (data from ISSCC 2011 documentation).

consumption and high reliability.

In this frame, Fig. 1.2 reports the significant developments in NAND flash memory over the past few years, as extracted from the works presented at the ISSCC 2011. Continuous scaling of the memory cell has resulted in an exponential increase of the memory density per chip. Note that in 2010, the reduction in process feature sizes, coupled with advanced multi-level cell (MLC) techniques have yielded a 32 Gb/chip capacity in a 32 nm technology with 2 bit/cell operation.

However, in order to guarantee an ever increase in memory density and and ever decrease in memory costs, something more than the mere scaling of feature size will be necessary, due to the intrinsic physical limits that Flash technology will face in the next years [3].

In the last decade several emerging memory technologies have been proposed as possible alternatives to Flash memory. Such technologies may be classified into two big categories, that is evolutionary memories, that essentially rely on the continuation of the existing ones, and completely new storing concepts. In the following sections, the traditional Flash memory cell, its working principle and the main scaling limitations will be briefly described, then the main direction in the non-volatile panorama will be presented and discussed. A particular attention will be devoted to Resistive-switching Random Access Memory (RRAM) technology and its fundamentals, as it will be the main topic of this Doctoral dissertation.

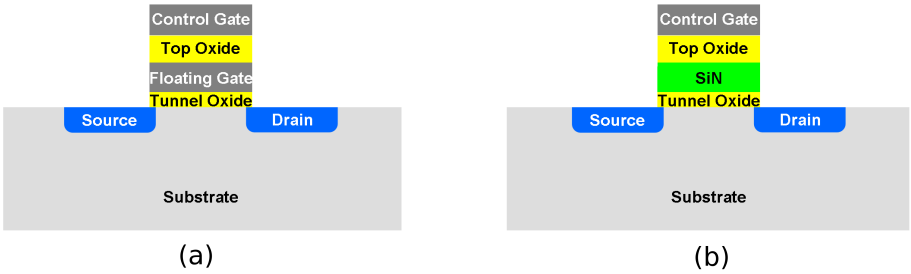

Figure 1.3: (a) Schematic view of a Flash memory cell: The charge is stored in the floating gate (FG) by applying the proper voltage to the control gate (CG); Tunnel and control dielectric are also shown. (b) Schematic view of a TANOS memory: The trapping layer is a discrete traps one, limiting the SILC effect; Also the tunnel and control dielectric are made of stack of different materials to improve memory performance.

1.2 Mainstream FLASH memory

The outstanding improvements in Flash technology have been achieved by the practical scaling methodologies allowed by the CMOS technology and by the simple structure of the floating-gate cell today representing the mainstream non-volatile storage element. Flash memory essentially consists in a MOSFET transistor with tunable threshold voltage. A basic scheme is depicted in Fig. 1.3a. Respect to a conventional transistor, the structure presents a floating gate (FG), in which it is possible to store charge, typically electrons.

There are two kinds of Flash memories, NOR and NAND. In NOR memory architectures, each cell in a two-dimensional array is directly connected to its word-line and bit-line input lines, whereas in NAND memory architectures, small blocks of cells are connected in series between a high input signal and ground.

Thus, due to its smaller unit cell size and being in perspective well suitable for the exploitation of new enhanced optical lithographic techniques [1], NAND Flash can inherently be packed more densely than NOR Flash, attaining the minimum cell area of $4F^2$ respect to the $10F^2$ occupied by the NOR counterpart.

The sensing mechanism consists in applying a positive bias to the control gate (CG) and subsequently reading of the resulting current that can be high or low as a function of threshold-voltage (V_T), hence function of the stored charge in the FG. On the other hand, the programming mechanism consists of a controlled shift of the threshold voltage, achieved by injecting or removing charge in the floating gate. This

operation can exploit Channel Hot Electrons injection (CHE) or Fowler-Nordheim tunneling (FN) mechanism [4]. The former approach needs a relatively high drain to source current and is used in NOR Flash, where each cell has its drain contact connected to the bit-line. FN programming is instead employed in NAND Flash, where the drain contact is not available, and provides slower single bit operation; however, the much smaller value of the tunneling current allows for parallel programming of several cells in the same array and largely enhances the overall write throughput. As a consequence, NOR memory are mainly used for applications such as embedded logic that require fast access to data that is modified only occasionally. In contrast, NAND memory is a high-density, block-based architecture with slower random access which is mainly used for mass storage applications. In both NOR and NAND architectures, the erase operation is achieved by means of FN tunneling from the FG to the channel.

As already mentioned, the success of Flash technology has been guaranteed by the complete compatibility with the CMOS technology, and Flash cell has been profitably scaled in a similar way as conventional transistors. However, major scaling challenges mine Flash scalability for next generations, originating from both physical scaling constraints (lithography and the cell layout design) and severe reliability issues [1,2,5]. Among them we can cite [6]: (i) oxide traps, contributing threshold-voltage (V_T) instability issues such as stress-induced leakage current (SILC) [7, 8], trapping/detrapping [9] and random telegraph-signal noise (RTN) [10], (ii) edge field-enhancement and discrete-dopant effects, which collaborate with oxide-trap effects to enhance the V_T spread in the array, (iii) few-electron effects [11] and (iv) cell-cell electrostatic coupling in the array [12].

To address some of these problems, such as SILC and electrostatic interference, many alternative cell devices have been proposed, mainly involving the replacement of the floating polysilicon gate by some type of charge trapping layer, for example silicon nitride SiN. The discrete nature of storage nodes prevents complete leakage of charge through SILC spots, while electrostatic coupling among adjacent cells is strongly inhibited due to the lack of significant capacitive coupling between thin trapping layers. This thus seems to guarantee the possibility of decreasing the thickness of the gate dielectric stack and, therefore, the program/erase (P/E) biases. Several discrete traps concepts have been proposed: MNOS - *Metal-Nitride-Ox-Silicon*, SONOS - *Si-Ox-Nitride-Ox-Si* and TANOS - *TaN-Alumina-Nitride-Ox-Si*. In all these technologies, the working principle is similar to the conventional Flash memory: the trapped charge in the storage layer modifies the threshold voltage,

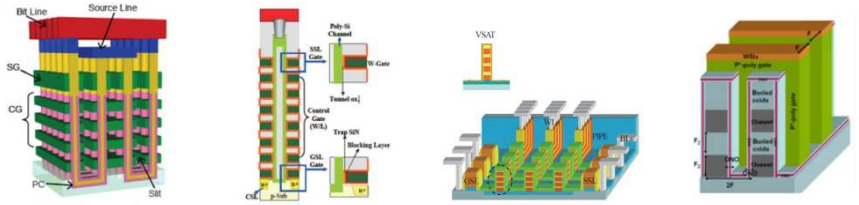

Figure 1.4: Pictorial view of different 3D NAND Flash architectures: (a) P-BiCS [15] (b) TCAT [16] (c) VSAT [17] (d) VG [18].

hence the current, of the transistor. Among these alternatives, TANOS memory, featuring a high-k top dielectric and a metal gate to prevent erase saturation, seems to be the most promising one [2]. The structure of a TANOS cell (TaN gate, Al_2O_3 top dielectric, SiN trapping layer and thin bottom SiO_2) is schematically depicted in Fig. 1.3b.

1.3 Evolutionary scenario and paradigm shift

The impressive performance growth rate of the traditional system memory and storage hierarchy that we are experiencing in the memory market since the last 30 years is facing serious problems and main challenges in the design of large-scale, high-performance systems. The gap between the performance of disks and the rest of the system - which is already five orders of magnitude - continues to widen rapidly [13, 14]. In addition, the energy consumption, the space usage and cost of the memory and storage systems pose major doubts on the feasibility of even higher performing, although low-cost, devices. Naturally, the continuous challenge toward lower costs and higher performances has driven a strong innovation in the existing technologies but it has also led to the development of alternative memory technologies as well, in anticipation of scaling limitations of existing Flash memory [1].

In the previous section we gave a brief overview of the major scaling issues of Flash memory. To overcome these obstacles and maintain the historic growth rate we have experienced so far two possible strategy may apply to Flash technology. A further progress and advance in current solid-state knowledge represents the most conservative approach, and it is currently tried with alternative structures as TANOS or SONOS devices implementing also the possibility of storing more than one bit on a single cell. Anyway exploiting the idea of using a Multiple Level

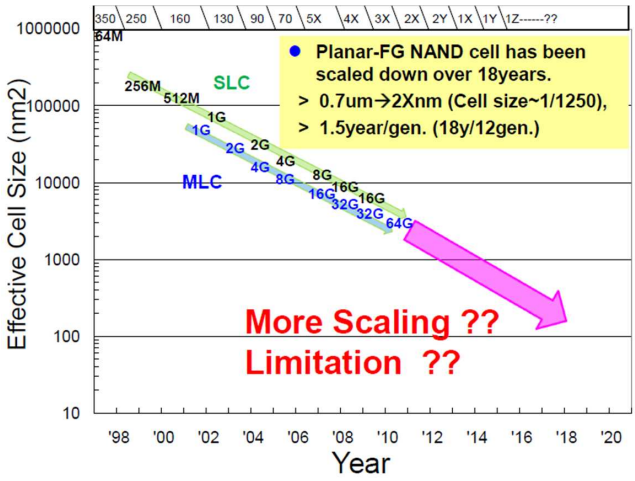

Figure 1.5: Road map for NAND scaling in which Planar FG NAND would convert to 3D NAND (data from IMW 2011 documentation).

Cell (MLC) requires maintaining a minimum of few electrons per bit, and managing the increasing complexities for beyond 4bits/cell. A second approach aims to a better optimization of the areal efficiency of the integrated memories stacking several layer of circuits on the same wafer [15–19] (see Fig. 1.4). 3D stacking of NAND Flash transistor is being aggressively pursued by several laboratories using a variety of approaches and is showing promise of lowering the cost per bit and extending the effective density of NAND Flash beyond the 16nm generation (see Fig. 1.5). However this $3D$ integration is faced by hard challenges of design, fabrication, bonding, test, reliability, yield issues and overall cost. On the other hand entirely new approaches must be developed changing completely the paradigm so far established.

Possible candidates to become the next leading class of memory are the RRAM devices. The basic building blocks of this NVM are a storage element and a selection device that is used to address it inside a memory array. The latter is also necessary for the reading and programming operations. The extreme simplicity of the cell structure, a switching active layer material interposed between two metal electrodes, may allow a brute-force lithographic scaling, where the Flash technology cannot follow. Of course this impressive reduction of device dimension is not cost-free in term of reliability. As recently underlined in [14] we should foresee a stronger importance of correction algorithms that supply to the more controllable ultra-scaled devices.

1.4 RRAM technology

Among the candidates for NVM applications RRAM represents a very promising competitor in the challenge for the post-Flash scenario. The first report about it is dated 1960s [20], but only recently this technology is attracting a serious interest both in academy and industry.

The basic principle of this kind of memory is the so called resistive-switching, i.e. the peculiar property of an active layer material of changing its resistivity after the application of an external voltage or current. Starting from a high resistive value, typical of insulators, the material can switch to a low resistive value, typical of metals. This change in conduction is reversible and the two resistance states can be easily used to store a bit of information.

RRAM devices include a wide range of different materials and switching modes where the physics mechanisms driving these phenomena have not been fully understood. To clarify this complex zoology, a useful taxonomy has been provided by Waser and Aono [21], introducing a classification of nine different basic switching mechanisms and devices: (i) Nanomechanical Memory, (ii) Molecular Memory, (iii) Phase Change Memory, (iv) Thermochemical Memory, (v) Valence Change Memory, (vi) Electrochemical Metallization Memory, (vii) Electrostatic/Electronic Effects Memory, (viii) Magnetoresistive Memory and (ix) Ferroelectric Memory. Devices from (iii) to (vii) are the most promising NVMs for future post-Flash replacement where the resistive-switching effect can be obtained by the application of electrical stimuli able to generate thermal, chemical, electronic/electrostatic effects inside the active layer material. More precisely, the physical mechanism for switching resistance states in the Phase Change Memory is purely thermal and for the Electrostatic/Electronic Effects Memory the switching mechanism is purely electronic. However, the physical switching mechanisms for the Thermal Chemical Memory (TCM), the Valence Change Memory Cell (VCM), and the Electrochemical Metallization Cell (ECM) are all based on reduction/oxidation (Redox)-related chemical effects. Due to similarity of their physical mechanisms they are also known with the name of Redox RAM.

The Doctoral Dissertation here reported is focused on the electrical characterization, physical/numerical modeling and performances optimization of TCM and VCM cells. A preliminary introduction to this two kind of RRAM technology is here reported.

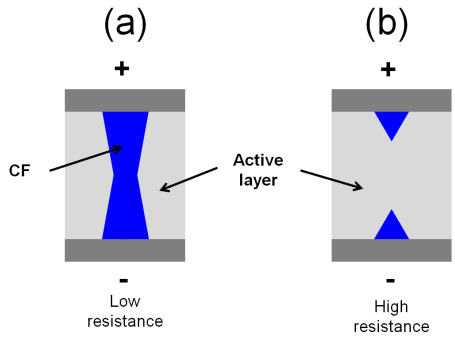

Figure 1.6: Schematic representation of a TCM cell in the low resistive state (a) and in the high resistive state (b). The same polarity is applied for the creation and dissolution of the CF.

1.4.1 Thermo-chemical memory (TCM)

A TMC cell is a RRAM device where the resistance switching is due to thermally-induced chemical reactions, typically reduction and oxidation [22, 23]. These reactions are typically localized at one spot in the active switching material, which will be referred to as the conductive filament (CF) [24, 25]. The CF is initially obtained through a soft breakdown process, which causes a local reduction of the metal oxide and results in the formation of a metallic-rich CF with low resistance (see Fig. 1.6a). Next, the CF can be oxidized by application of a voltage and the consequent release of a Joule heat accelerating diffusion and chemical reaction [26]. Now the composition in the oxidized part of the CF is closer to the metal oxide, thus showing a high resistance (see Fig. 1.6b).

The localized nature of switching in TMC cells can be supported by the fact that the set-state resistance is generally independent from the device area, since R is controlled by the CF area and conductivity [26,27]. This has significant implications in terms of reduction of the switching current and scaling of the cell size in a real array [26].

The most important signature of this switching mode is its unipolar nature, where both set and reset processes are achieved by the application of electrical pulses with the same (e.g. positive) polarity. This allows a straightforward implementation of a crossbar array architecture through TCM devices, with a relatively simple periphery circuitry and unipolar rectifying diodes as select elements [28].

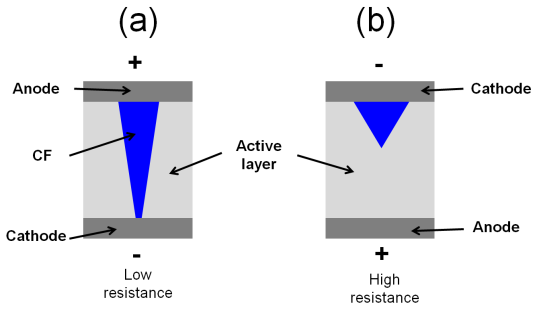

Figure 1.7: Schematic representation of a VCM cell in the low resistive state (a) and in the high resistive state (b). Different polarity is applied for the creation and dissolution of the CF.

1.4.2 Valence-change memory (VCM)

In a VCM cell the resistive-switching requires a change of bias polarity between the set and the reset operations. This is thus referred to as bipolar switching. The switching phenomenon in VCMs can be explained by a physical mechanism similar to TCMs, however involving a significant thermally- and voltage-assisted ion migration [21].

After the creation of the CF, again obtained through a soft breakdown process, it is dissolved by migration of ions toward the electrodes, namely positive ions (e.g. metallic ions or oxygen vacancies) drift toward the cathode and negative ions (oxygen ions) drift toward the anode (see Fig. 1.7b). The CF is recovered by migration of the ions back to the previous position (see Fig. 1.7a). This allows a low-resistance connection between the electrodes by a continuous metal-rich (or oxygen-vacancy rich) CF. The vertical migration of ions, instead of the mostly-radial diffusion of conductive species in the TCM, thus forms the basis for the bipolar switching process in VCMs.

Several transition metal oxides have been shown to display bipolar VCM switching. Examples are ZrO_x [29], $SrTiO_x$ [30], Nb_2O_5 [31], TiO_x [32] and HfO_x [33]. The preliminary forming operation is generally required to initiate the resistance switching, but the reset and set parameters generally vary depending on the materials and the cell structures. Moreover in some VCM devices is possible to observe the uniform switching of the active layer material instead of the filamentary switching. This cells are based on complex oxides such as PrCaMnO (PCMO) and other perovskites [34]. In this case the memory show an area-dependent switching, where the both high resistance and low resistance state are inversely proportional to the device area, contrary

to TCM. Ion migration in these materials is probably uniform, leading to an increase of the oxygen concentration to the anode side and a resulting oxidation. The formation of an interface layer with a high potential barrier for electrons causes the increase of resistance in the uniform switching VCM. This kind of VCM is attracting a growing interest since the reset current can be reduced linearly with the device area, in contrast to filamentary switching RRAM where the reset current is area independent. However, the deposition and control of complex ternary/quaternary oxides is generally not straightforward and the reliability issues and mechanisms are still not clear, thus these devices appear to be not yet sufficiently mature as compared to filamentary TCMs and VCMs.

1.5 Conductive filament experimental evidences

As it will be explained in more detail in Chapter 2, the materials used as active layers in the memory devices object of this Doctoral Dissertation are simple transition metal oxides. A wide spread consensus exists in literature about the link between resistive-switching phenomenon and

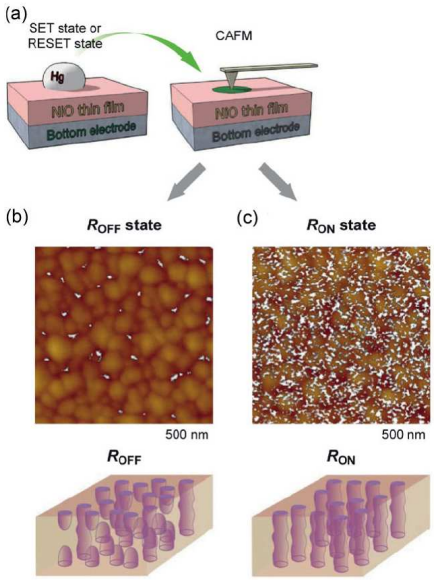

Figure 1.8: a) A drop of Hg is used as top electrode. Once the cell is programmed, removing the Hg allows to analyze the NiO film via C-AFM. b) and c) show respectively the distribution of the conductivity for OFF and On states. Fig. from [25]

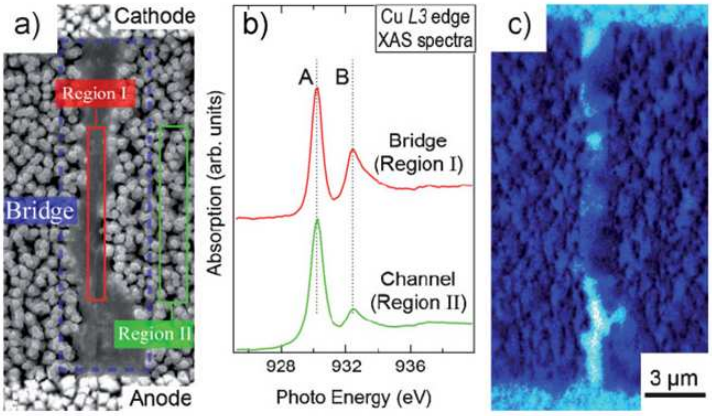

Figure 1.9: (a) SEM image of the planar-type $Pt/CuO/Pt$ resistance-switching device. Top and bottom regions in the image correspond to the anode and cathode parts, respectively. The central lighting-shaped structure is the bridge structure formed in the CuO channel. (b) XAS spectra of $CuL3$ absorption edge for bridge structure (Region I) and CuO channel (Region II) structures. The reduction component at 932.6 eV (B) is enhanced at the bridge structure. (c) Division of two PEEM images taken in the same region as the SEM image and obtained with a photon energy of 930.3 eV (CuO derived component A) and 932.6 eV (reduction component B), respectively. The bright regions in the bridge structure correspond to the reduced region of the CuO channel [35].

the creation/dissolution of a CF in these kind of materials.

Anyway due to the very localized nature of the CF, and to its reduced diameter (estimated to be around 10 - 100 nm [21,36,37]), it is very hard to analyze its composition. Several researches attempted the task, trying to solve several doubts and debates. In particular there is not yet a clear evidence of the formation of a single CF or multiple CFs, neither the exact position of the filament.

Son and Shin have used a Hg drop top electrode to switch a NiO film [25]. They removed the metal afterward and analyzed the surface of the oxide layer using a conducting AFM. Data are shown in Fig. 1.8 It is worth to note two main aspects in this experiment. First of all, the granularity of the high conductive spots on the oxide layer, suggesting the formation and rupture of several filaments. Moreover, it was shown that the CFs generally form at the grain boundaries of the NiO layer.

Moreover Deleruyelle et al. [38] demonstrated resistive switching at the nanoscale on a NiO layer using conductive AFM tip as top electrode. Filamentary conduction was clearly evidenced through the creation of multiple highly conductive regions.

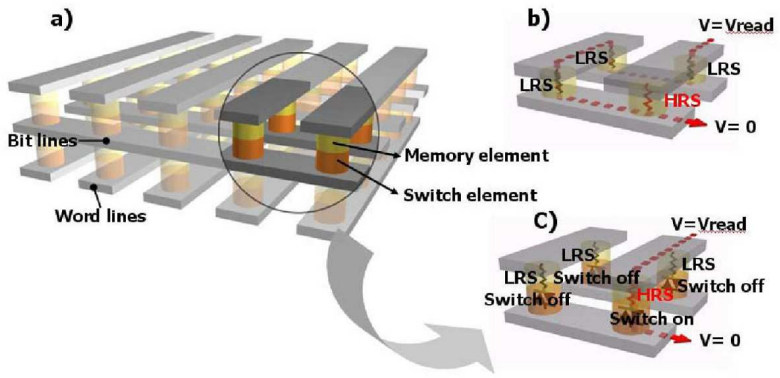

Figure 1.10: Double stack, cross-point RRAM array (a), demonstrated by Samsung in 2007 [39]. In order to prevent reading interferences (b) it is necessary to have a rectifying element, e.g. a diode (c).

On the other hand, Yasuhara et al. [35] studied lateral cells showing the formation of a single percolative path through CuO, in a $Pt/CuO/Pt$ structure. Fig. 1.9 shows their analysis, revealing that the CF is constituted by reduced Cu.

1.6 Architectures and scaling perspectives

RRAM technology has attracted a strong interest in particular for its intrinsic scalability potentials. The particular simplicity of the cell, as a matter of fact a simple capacitor, is extremely suited for extreme scaling. However several issues arise. Directly connected with cell area scaling is the high program current needed for the dissolution of the CF. This topic will be discussed throughly in Chapter 2 and 4, showing a solution to the problem by the use of the so called 1-transistor/1-resistor structure (1T1R). Basically, each cell is addressed by a selector, which can be a MOSFET for NiO-based cell. The transistor has two aims. First, it provides a current compliance during the creation of the CF, which reduces the amount of current that the cell will drain at the subsequent dissolution of the CF. Second, it provides an easy and high reliable way to address a single cell in the array [40]. However two main concerns arise about the 1T1R structure, namely the scaling of the selector device and the feasibility of a multi-stacked array due to the high temperature process for MOSFET manufacture. To solve both the issue it has been proposed by many authors a different approach based on diode/1-resistor structure (1D1R), where the selector is substituted by a diode and the

cells are arranged in a cross-point array. Each bit line and word line are addressed by a simple MOSFET, thus significantly reducing the number of the transistor, and the diode prevents cross-talk and leakage current between adjacent cells. This approach would lead to a minimum of $4F^2$ cell size, maximizing the wafer yield. Particularly interesting is the structure proposed by Lee et al. (Samsung) in 2007 [39], who demonstrated a two-stack cross-point array, using $p{-}CuO_x/n{-}InZnO_x$ as selector diode. Fig.1.10 shows the structure of the device, illustrating how the diode prevents the read disturb during the read operation (b and c). The bottleneck of this approach is the current density that the diode can drive, and that could be lower than what the cell requires for program operations in a high scaled cell.

Chapter 2

Electrical characterization and conductive filament control

Tyger! Tyger! burning bright
In the forest of the night,
What immortal hand or eye
Dare frame thy fearful symmetry?

William Blake (1757-1827), THE TYGER

This chapter gives a deeper insight into memory structures and program operations of RRAM devices object of this Doctoral Dissertation. The nature of the resistive-switching is investigated unveiling the nature of the conductive filament.

2.1 Materials, device structure and electrical characterization

The memory devices object of this Doctoral Dissertation belong to the group of TCM and VCM already presented in Chapter 1. Two kind of binary oxide materials have been used as active switching layer in the RRAM cell: Nickel-Oxide NiO and Hafnium-Oxide HfO.

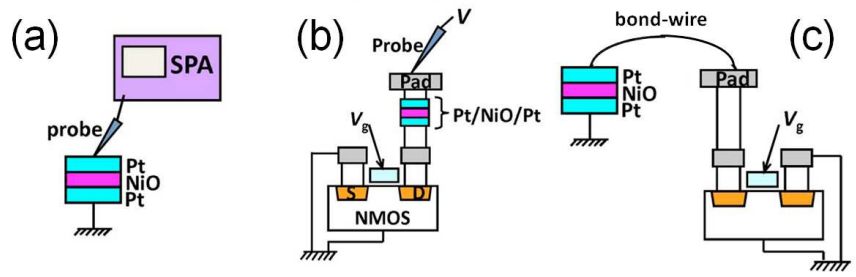

Figure 2.1: Qualitative sketches of the three types of analytical cells object of the electrical characterization in this Doctoral Dissertation, namely MIM (a), 1T1R (c) wire-bonded 1T1R structures

In order to access a deeper comprehension of the physical mechanisms involved in the resistive-switching phenomenon, the electrical characterization dealt only with single analytical cells. As already mentioned in Chapter 1, the simplest RRAM cell is the so called Metal-Insulator-Metal (MIM) structure reported in Fig. 2.1a. This memory device consists of an active switching layer interposed between two metal electrodes. A more complex memory cell is the 1-transistor/1-resistor structure (1T1R) obtained by the integration of a MIM device with a MOS field effect transistor (see Fig. 2.1b). The cell structure presents a memory element (1R) and also a selection element (1T). As it will be presented in Chapter 4, the presence of a MOSFET device is fundamental for RRAM power scaling. Note that in this case the structure could still be compatible with a diode-selected crossbar array with maximum cell density. In fact, MOSFET devices are always present in the memory array for decoding/selecting wordlines and bitlines, thus may be actively control the programming operation in the selected cell in the array. An analogous version is the wire-bonded 1T1R structure in which the MIM device and the MOSFET device are bonded together by Au wires (see 2.1c).

As a useful example of electrical characterization, in Fig. 2.2 the three typical program operations for a unipolar MIM device are shown. The resistive-switching is obtained by the application of current/voltage-controlled sweeps (DC). In a real memory array of course all the program operations are performed by voltage pulses. Anyway DC operation is usually chosen as the first attempt to show the feasibility of resistive-switching in a RRAM memory device.

The first operation which the cell is subjected to is the forming operation (Fig. 2.2a). As can be seen, by the application of a current

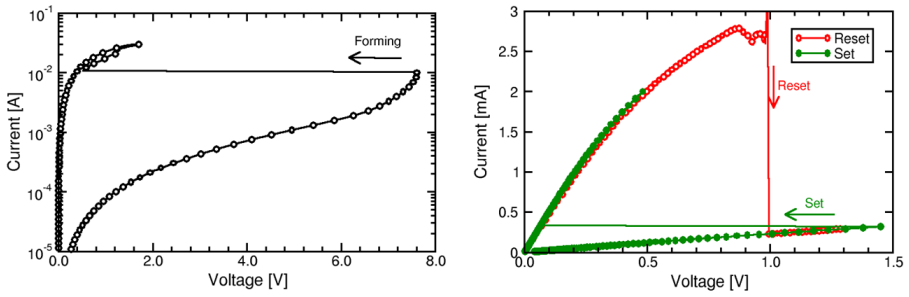

Figure 2.2: $I - V$ curves for a typical forming (a) and set/reset (b) operations. Note that in this case the forming/set process is current-driven, while the reset is voltage-driven.

sweep, the device shows a sudden voltage decrease at a relatively high current marking the transition from a pristine high resistive state to a low resistive state by the creation of the CF through the oxide layer. This operation is a one-time process, i.e. the cell will never restore the pre-forming resistance during its working life-time. A subsequent voltage ramp will cause the transition from the low resistive state to the high resistive state by the dissolution of the CF (Fig. 2.2b). This is the so called reset operation. The cell now exhibits a high resistance (lower than the pre-forming anyway). Again, the application of a current sweep will change the cell state to a low resistive one. This is the set operation, operatively similar to the forming operation (Fig. 2.2b).

It is noteworthy that the use of a current sweep (also with the use of a protection resistor) is necessary during forming/set operation in order to limit high current flowing through the cell during the switch to the low resistive state and avoid subsequent degradation of the device.

Another way to control the flowing current during the creation of the CF is the use of a voltage sweep combined with a current compliance. This can be done by the use of a special functionality in the Semiconductor Parameter Analyzer, general purpose tool used for the electrical characterization of semiconductor devices. However the response of the electronic loop in controlling the increase of current takes hundreds of μs. This time can be quite big compared to the usual ns regime for set/forming operation in RRAM devices thus leading to a non perfect control of the maximum current flowing into the cell [41].

This problem can be overtake by the use of 1T1R or wire-bonded 1T1R structures where the maximum current can be directly biased by the polarization of the gate terminal. In these cases the possible draw-

back could be now the presence of an additional parasitic capacitance C_p in parallel to the RRAM cell which can lead to unwanted and unexpected phenomena during program operations, i.e. current overshoots [41, 42]. This is avoided in the integrated 1T1R structure, which limits C_p largely below 1 pF.

2.2 CF control

While set transition is generally abrupt, leading directly to the full set state, the reset operation in some kind of devices allows a gradual change of resistance. R_{set} can be fine tuned to higher resistances by careful control of stop voltage (V_{stop}) during reset operation by the use of voltage sweeps. Fig. 2.3 shows the measured $I-V$ curves during multiple reset sweeps in a NiO RRAM: the first sweep applied to the set state results in a resistance R increase by about 10%. The application of successive voltage sweeps with higher V_{stop} lead to an additional and controllable increase of cell resistance. This program algorithm for reset operation (which from now will be called partial reset) is very useful toward a multilevel cell (MLC) approach in RRAM technology. In fact, thanks to the large resistive window ($R_{set} \approx 100\ \Omega$ for the full-set state and $R_{reset} \approx 10^9\ \Omega$ for the full reset state) different values of resistance can be selected thus storing more than one logic bit on the same memory element leading to a dramatic increase of storage information density.

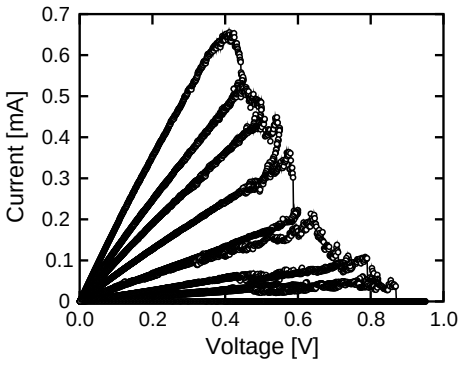

Figure 2.3: Measured $I-V$ characteristics showing MLC operation of a NiO RRAM: starting from the set state, the programmed R can be tightly controlled by the final V_{stop} within a reset sweep.

Even if set transition is generally abrupt, in some cases it is possible obtain the control of the growth of the CF by limiting the maximum current flowing through the cell. This can be done by the use of 1T1R

structure presented in Section 2.1 introducing the partial set program algorithm.

Fig. 2.4 shows measured $I - V$ characteristics for a 1T1R NiO-based structure, during forming, reset and set operations [43]. Note that the select transistor is differently biased depending on the specific programming step. In this particular case, forming and set operations are performed under a relatively low V_G, it e.g. $V_G = 0.8$ V yielding about 200 μA in Fig. 2.4. This allowed to limit the maximum current supplied to the memory element at the CF formation, thus limiting the area of the CF (A_{CF}). On the other hand, reset is done at a relatively high V_G, to allow delivery of a maximum current at minimum voltage drop across the select MOSFET. Limiting the equivalent MOSFET resistance is particularly important to avoid an excessive increase of cell voltage upon reset, that could induce an unwanted set and a consequent reset-set instability (RSI) [44, 45]. On the other hand, a large V_G may result in electrical stress and a possible breakdown of the thin layer of gate oxide (1.6 nm). For this reason, V_G is fixed to a maximum value of 1.4 V during reset.

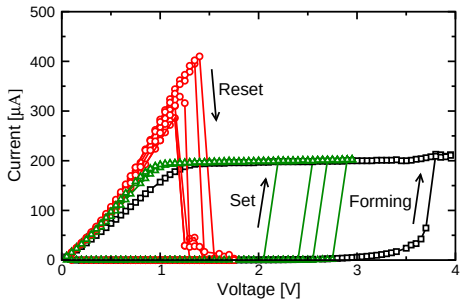

Figure 2.4: Forming, reset and set $I - V$ characteristics for 1T1R devices. A low $V_G = 0.8$ V, resulting in a low I_D and a small A_{CF}, is used for the forming and set operations, while a high $V_G = 1.4$ V is used during reset operation to minimize V_{reset}.

Fig. 2.5 shows the measured R after set as a function of drain current I_D used in the set operation. R increases for decreasing I_D due to the decreasing size of the CF. The slope is around -1 in the log-log plot: This is due to R in the set state being inversely proportional to A_{CF}. In turn, the filament area is supposed to be close to the area A_{EF} of the electronic filament generated at the very first stage of the set process, i.e. threshold switching [46]. Thus, the current I_D determines an electronic filament with size $A_{EF} \propto I_D$, where the NiO chemical composition is modified to yield the CF, e.g. by increasing the oxygen vacancy concentration or

increasing the Ni content [47]. This can be expressed as

$$R \propto {A_{CF}}^{-1} \sim A_{EF}^{-1} \propto {I_D}^{-1}. \tag{2.1}$$

Data in Fig. 2.5 indicate that a good control of R can be achieved through a proper choice of I_D. This can be used for programming the cell into intermediate states between set and reset. Different states thus correspond to different cross section of the CF. This flexibility is a key for the development of multilevel programming in NiO-based RRAMs.

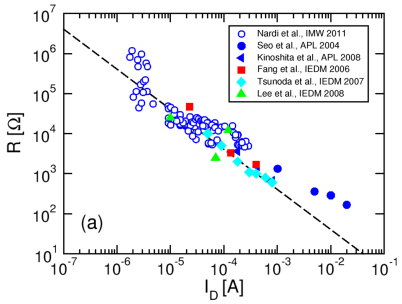

Figure 2.5: Measured R after set operation as a function of I_D for our 1T1R structures. Data from 1T1R and stand-alone cells with other active materials are shown for comparison [42, 48–51].

2.3 CF conduction model

Up to now a metallic-type filament was assumed. However, this is not entirely true in NiO, where a continuous change between metallic and semiconductorlike behaviors is observed. Fig. 2.6 shows the measured resistance as a function of $1/kT$ (Arrhenius plot) for different conductive states in NiO. The programmed resistances were obtained by the partial reset method discussed in section 2.2. The temperature dependence of resistance can provide a useful insight into the conduction mechanism in the CF. In particular, the resistance for a metallic filament increases linearly with temperature, according to [52]

$$R = R_{0m} \left(1 + \alpha \left(T - T_0\right)\right) \tag{2.2}$$

where T_0 is the room temperature, R_{0m} is the metallic resistance at T_0 and α is the temperature coefficient of resistance. On the other

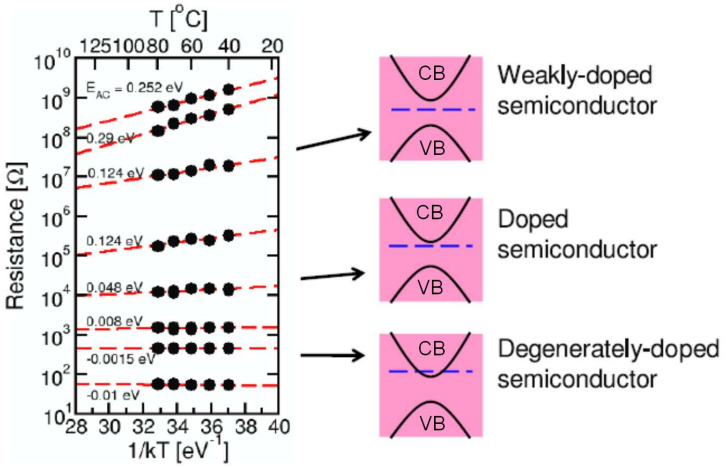

Figure 2.6: Arrhenius plot of resistances for different CF states (left) and corresponding schematic band structures (right). Low resistance states display a metallic conductivity behavior, where resistance increases with T, as revealed by the negative apparent activation energy. This suggests that the Fermi level is pinned in the conduction (or valence) band as for a degenerately doped semiconductor. For increasing resistance, the CF behavior becomes increasingly semiconductor-like, showing an increasing activation energy. The corresponding physical picture is a semiconductor with a different Fermi level with respect to the band edge.

hand, semiconductor-like filaments display an exponential decrease of resistance for increasing temperature, according to

$$R = R_{0s} e^{\left(\frac{E_{AC}}{kT}\right)} \tag{2.3}$$

where R_{0s} is the extrapolated resistance at infinite T, k is the Boltzmann constant and E_{AC} is the activation energy for conduction, which reflects the difference between the band edge relevant for carrier transport and the Fermi level. Eq. 2.3 can describe carrier generation in the conduction/valence bands for n-or p-type semiconductors, respectively. The same T dependence of conductivity is expected also for PooleFrenkel (PF) conduction in semiconductors with high-defect concentrations or disordered structures, due to the exponentially enhanced carrier emission probability at increasing T [53]. Note that the resistance in Fig. 2.6 and Eq. 2.3 refers to very low voltage, where an ohmic voltage is observed even for PF conduction. Data in Fig. 2.6 show that low resistance CFs display a metallic-type conductivity while for increasing resistance there is a transition to semiconductor-like transport. The activation energy increases for increasing R, from 0 to about 0.3 eV. Note

that resistance values above 10^8 Ω may not refer to the CF, but to the parallel resistance due to the background leakage in the surrounding dielectric, as described in more detail later. Based on the exponential relationship in Eq. 2.3, the large increase of activation energy indicates that the major role in the change of resistance is played by the shift of Fermi level with respect to the conduction band. This may be attributed to a variable concentration of oxygen vacancies, as suggested by ab initio studies in NiO [54], or to doping by substitutional metallic elements, introducing metal-metal wrong bonds. In this regard, it is worth noting that O excess in NiO leads to p-doping. Therefore, assuming that Ni excess leads to n-type conductivity in NiO, the most plausible picture for the variable Fermi level is Ni local doping in the CF. According to this model, the right-hand part of Fig. 2.6 displays a possible interpretation of the observed different T dependence of conductivity: the semiconductor behavior at relatively high R suggests a variable E_{AC}, possibly due to a change in the position of the Fermi level as a result of a variable concentration of defects (vacancies and wrong bonds) playing the role of dopants. For low R, due to the increasing defect concentration, the filament turns into a degenerately doped semiconductor, where the Fermi level is very close or even above the conduction band edge. In this case, the carrier concentration is practically constant, while the drift mobility degrades for increasing temperature. The mobility degradation thus accounts for the observed metallic character of conductivity. Note that a similar transition from negative to positive temperature coefficient (or, equivalently, from positive to negative activation energy) of resistance is usually observed in the drain current of bulk [55, 56] and SOI MOS transistor [57] for increasing gate voltage. This insulator metal transition is similarly explained by the shift of Fermi level induced by the external gate voltage. This CF model allows us to explain the whole range of observed R, E_{AC} and T dependences only invoking a different defect/doping concentration and a variable size of the CF.

Moreover the extracted E_{AC} allows to estimate the effective CF area A_{CF} by the formula

$$R = \rho_0 \frac{t_{NiO}}{A_{CF}} e^{\left(\frac{E_{AC}}{kT}\right)} \tag{2.4}$$

where k is the Boltzmann constant and $\rho_0 = 100$ μΩcm [58] is the pre-exponential constant for resistivity. The NiO layer thickness t_{NiO} was used to identify the CF length in Eq. 2.4. Fig. 2.7 shows the extracted CF diameter $\phi = (4A/\pi)^{1/2}$ obtained from Eq. 2.4 using the piecewise-linear fitting of E_{AC} in Fig. 2.7(a), where $E_{AC} = 0$ was assumed for metallic states ($R < R_{metal}$) while $E_{AC} = E_{AC0} log(R/R_{metal})$ with $E_{AC0} = 0.0178$ eV was assumed for semiconductor-like states (R

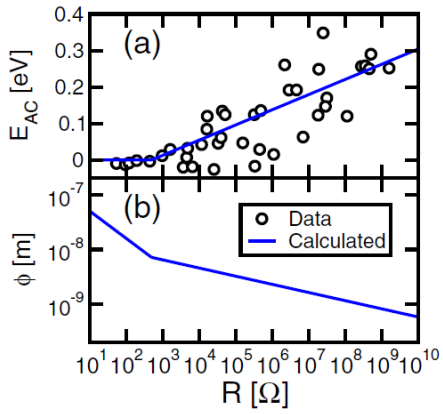

Figure 2.7: Measured E_{AC} with its piecewise linear fit (a) ans calculated CF diameter ϕ (b) from Eq. 2.4 as a function of R.

$> R_{metal}$). The resulting CF diameter ϕ changes only by a factor 20 in the investigated R window, from 20 nm at R = 100 Ω to about 1 nm at 3×10^8 Ω. Note again that ϕ should be viewed as an effective value for the CF size, taking into account the possible irregular shape of CFs, possibly including multiple branches and nonuniform cross section. Also, conduction may be largely nonuniform at relatively large resistivity as a result of percolation effects. In this case, the extracted effective area could yield an estimate for the conduction path in the percolation process.

Due to this chemical disorder resulting from nonstoichiometry combined with the possible structural disorder associated with the CF location at grain boundaries [59], it may not be possible to account for conduction characteristics just based on the standard drift-diffusion model. In fact, disordered or highly defective polycrystalline semiconductors typically display PF conduction [53]. This should result in a marked nonlinear behavior in the voltage dependence of the current for semiconductor-like CFs. To confirm this point, Fig. 2.8a shows the measured $I - V$ curves for CFs at variable resistance, namely the pristine (before forming) state, the set state (R of about 100 Ω) and four intermediate states with R = 44 kΩ, 100 kΩ, 1 MΩ and 27 MΩ. Increasing R of these intermediate states, the $I - V$ curves become increasingly nonlinear, which is consistent with a PF transport at defects (e.g. vacancies and wrong bonds). To confirm the PF behavior of conduction, Fig. 2.8b shows the same characteristics, where the measured current is plotted as a function of the square root of the applied voltage. This allows us to highlight the

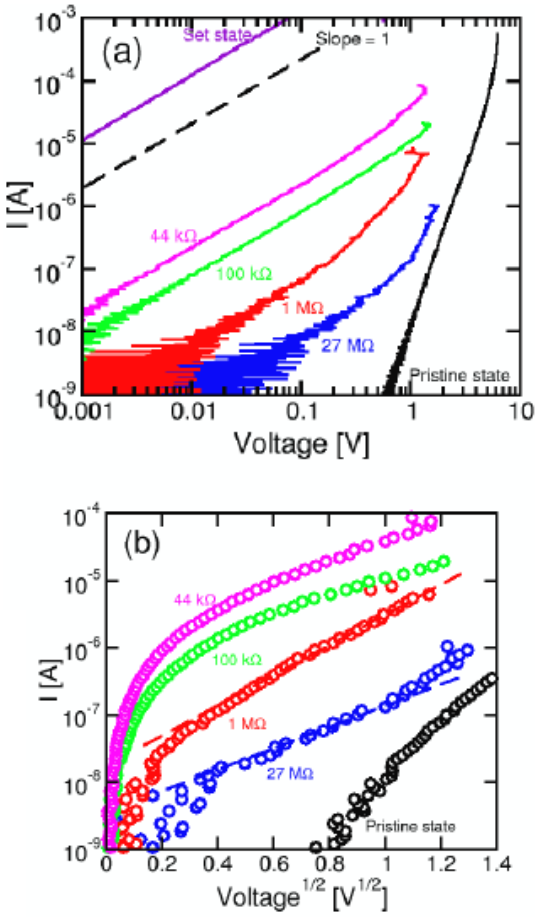

Figure 2.8: Measured IV curves for CFs with variable resistance, on a bilogarithmic scale (a) and on a logarithmic scale of current as a function of the square root of the voltage (b). An increasing nonlinearity (i.e. deviation from the slope 1 in the loglog plot) is shown in (a) for increasing R, consistent with PF conduction at defects in the CF. The linear fitting in (b) confirms the PF behavior for R = 1 and 27 MΩ.

PF conduction law

$$I = I_0 e^{\beta V^{\frac{1}{2}}} \tag{2.5}$$

where I_0 and β are constants dictating the amplitude of the current and the slope in the $log\,(I) - V^{1/2}$ plot, respectively. The slope factor is given by

$$\beta = \frac{q^{\frac{3}{2}}}{(\pi \epsilon t_{NiO} k^2 T^2)^{\frac{1}{2}}} \tag{2.6}$$

where ϵ is the dielectric constant. In Fig. 2.8b, the states with R =

1 and 27 MΩ clearly show a PF behavior at sufficiently high voltage, whereas at low voltage they show an ohmic behavior due to the onset of a diffusion regime [53]. For R = 1 MΩ, the extracted slope factor is $\beta = 5.1\ V^{-1/2}$, which corresponds to a dielectric constant $\epsilon = 13.3\ \epsilon_0$. Values for R = 27 MΩ are $\beta = 3.7\ V^{-1/2}$ and $\epsilon = 24.9\ \epsilon_0$. The change in relative permittivity with resistance might result from the different defect concentration in the CF.

Chapter 3

Program operation modeling

There are two possible outcomes:
if the result confirms the hypothesis,
then you've made a measurement.
If the result is contrary to the hypothesis,
then you've made a discovery.

Enrico Fermi (1901-1954)

This chapter is dedicated to the analytical and numerical modeling of program operations for both unipolar (NiO-based) and bipolar (HfO-based) devices. Complementary switching and universal reset for unipolar/bipolar RRAM will be also presented.

3.1 NiO unipolar modeling

As already mentioned in Chapter 1, NiO-based memories are unipolar devices belonging to the category of TCM cells. Electrical characterization experiments were conducted on these devices. By the analysis and interpretation of these results we were able to give a deeper insight into the physical mechanisms of unipolar resistive-switching for both reset and set operation.

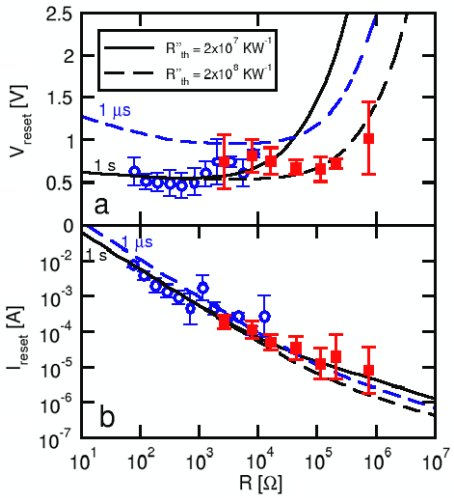

Figure 3.1: Measured and calculated V_{reset} (a) and I_{reset} (b) as a function of resistance in the set state. The resistance states were obtained by partial reset operation (open symbols) or partial set operation (filled symbols). Calculations are shown for both DC (1 s reset time) and pulsed operations (1 μs reset time).

3.1.1 Analytical reset model

Fig. 3.1 shows the measured reset voltage (a) and current (b) as a function of initial resistance in the set state. The initial resistance was controlled through the partial reset operation (open symbols) or the partial set operation (filled symbols) previously discussed in Section 2.2. The reset voltage for partial set states was corrected for a series resistance of 3 kΩ due to a parasitic resistance in the 1T1R structure [43]. To a first approximation, the reset voltage V_{reset} is roughly constant along more than four orders of magnitude of initial resistance. Consequently, the reset current I_{reset} is inversely proportional to R, since $I_{reset} = V_{reset}/R$. Data for partial reset and partial set align almost perfectly on the same trend, suggesting that the CF properties (size and density of defects/dopants) negligibly depend on the formation method. These results can be understood by the Joule heating model for thermochemical reset [58]. In this model, the CF is described as a metallic phase (e.g. Ni mixed with electrode elements in NiO) and the reset transition is explained as a radial diffusion and oxidation of the metallic elements constituing the CF. According to this model, the onset of reset is achieved once a critical reset temperature T_{reset} is reached at one point along the filament. T_{reset} corresponds to that particular temperature at which the reaction-diffusion process of oxidation proceeds with the same

timescale of the experiment, e.g. of the order of seconds for DC measurements. The reset condition can thus be obtained by the relationship between maximum temperature along the filament and applied voltage V, namely [52]:

$$T = T_0 + \frac{R_{th}}{R} V^2 \tag{3.1}$$

where T_0 is the room temperature and R_{th} is the effective thermal resistance of the CF. According to Eq. 3.1, the reset voltage can be written as $V_{reset} = (R\Delta T_{reset}/R_{th})^{1/2}$, where ΔT_{reset} is the critical temperature increase for the onset of oxidation. The ratio R/R_{th} is approximately constant due to the Wiedemann-Franz law for metals, linking thermal and electrical conductivity, thus V_{reset} is approximately constant and $I_{reset} = V_{reset}/R$ is inversely proportional to R, as shown by the data.

This first-order model for thermal reset cannot, however, account for the detailed behavior of V_{reset} and I_{reset} reported in Fig. 3.1. The reset voltage in fact displays a shallow U shape, where voltage first decreases, then increases for increasing R. This is also reflected in the bent I_{reset} behavior in the log-log plot of Fig. 3.1b, which also agrees with other reports from the literature [60]. To account for this subtle R dependence of reset parameters, size-dependent heating and diffusion effects should be taken into account.

The effective thermal resistance of the CF includes in fact two contributions: the heat loss along the filament ($R_{th}^{'}$) and the one occurring out from the surface of the filament through the surrounding NiO ($R_{th}^{''}$) [58].

The first contribution to thermal resistance $R_{th}^{'}$ can be evaluated in terms of the CF thermal conductivity k_{th}, area A_{CF} and length, corresponding to the NiO layer thickness t_{NiO}, yielding [52]:

$$R_{th}^{'} = \frac{1}{8k_{th}} \frac{t_{NiO}}{A_{CF}} \tag{3.2}$$

where the factor 1/8 is obtained assuming a parabolic temperature profile along the CF and is due to heat diffusing in the two directions along the CF [52].

To evaluate the out-of-filament thermal resistance $R_{th}^{''}$, an analytical approach is not adequate for the complex geometry of heat diffusion from a non-uniformly heated cylindrical CF. To study the impact of CF size on heat loss processes, we used 3D numerical simulations of electrical conduction and Joule heating which will be discussed later in detail in Section 3.1.2. To evaluate the overall equivalent thermal resistance, a constant voltage V = 0.2 V was applied to a cylindrical filament with metallic conductivity and variable area A_{CF}, embedded in an NiO film with infinite electrical resistivity. The NiO thermal

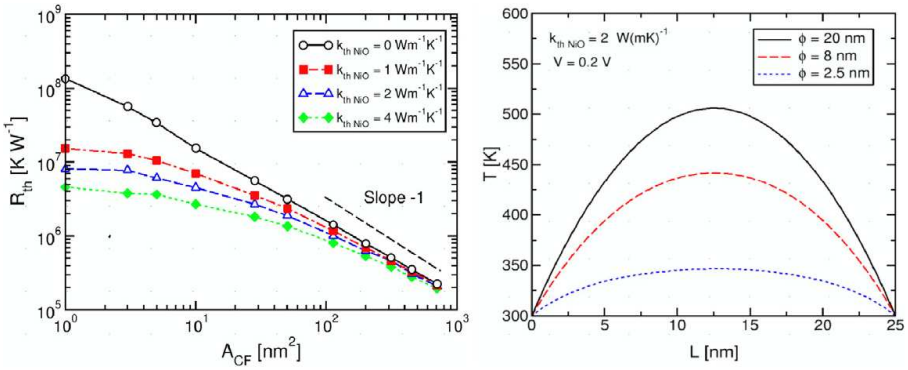

Figure 3.2: Calculated effective thermal resistance as a function of CF area A_{CF} for various thermal conductivities of NiO (a) and temperature profile for $k_{th,NiO} = 2\ Wm^{-1}K^{-1}$ and increasing CF diameter (b).

conductivity $k_{th,NiO}$ was changed between 0 (perfect thermal insulator) and 4 $Wm^{-1}K^{-1}$, to study the size dependence of R'_{th} and R''_{th}. The effective thermal resistance was evaluated from the formula $R_{th} = R(T - T_0)/V^2$, which can be obtained from Eq. 3.1, and using the values of R and T (maximum temperature along the filament) extracted from simulation results.

Fig. 3.2a shows the extracted R_{th} as a function of A_{CF} for different values of $k_{th,NiO}$. R'_{th} can be obtained from simulation results for $k_{th,NiO} = 0$, since in this case only the filament contributes to heat loss. The results show that R'_{th} decreases with A_{CF} with a slope -1 on the log-log plot, indicating $R'_{th} \propto A_{CF}^{-1}$, in agreement with Eq. 3.2. For other values of $k_{th,NiO}$, R_{th} can be approximated by the parallel composition of R'_{th} and R''_{th}, namely $R_{th} = R'_{th}R''_{th}/(R'_{th} + R''_{th})$. For relatively large A_{CF}, R_{th} is approximately equal to R'_{th}, thus indicating that out-of-filament heat conduction can be neglected, while R_{th} is dominated by R''_{th} for small A_{CF}. As expected, R''_{th} decreases for increasing $k_{th,NiO}$, while the dependence on A_{CF} becomes more shallow with respect to R'_{th}. This is because R''_{th} describes heat loss from the surface of the filament, instead of through the filament volume. This also explains why out-of-filament heat loss arises for small filaments, where the surface/volume ratio becomes increasingly important. Fig. 3.2b shows the calculated temperature profile for $k_{th,NiO} = 2\ Wm^{-1}K^{-1}$ and three different filament diameters, namely 2.5, 8 and 20 nm. Calculations indicate that, for a given applied voltage, heating decreases for decreasing size of the filament: this is because R is inversely proportional to A_{CF}, while R_{th} has a weaker size dependence, thus R_{th}/R in Eq. 3.1

decreases for decreasing size of the filament. Therefore T decreases for a given applied voltage, or, conversely, a higher voltage must be applied to achieve the critical temperature T_{reset} needed for the onset of filament oxidation. This accounts for the increase of V_{reset} for increasing R (or decreasing filament size) in Fig. 3.1a. Also note in Fig. 3.2b the change of temperature profile, from a pure parabolic behavior, as expected from ideal heat conduction through the filament [52], to an almost uniform temperature, which is a signature of dominating out of filament heat loss [61]. In conclusion this phenomenon can be referred as a sort of size-dependent Joule heating.

Fig. 3.1a also shows that V_{reset} increases for decreasing resistance below about 0.5 $k\Omega$. This cannot be attributed to size-dependent Joule heating effects, since the R_{th}/R ratio in Eq. 3.1 remains constant based on the simulation results in Fig. 3.2a. The V_{reset} increase at large filament sizes shows instead the increase of T_{reset} for the onset of diffusion in large filaments. Assuming that filament oxidation is due to diffusion of nickel atoms or ions, as suggested by results for Ni film growth by oxidation [62], the reaction-diffusion kinetics can be described by the following radial diffusion equation for conductive species [63]

$$\frac{\partial n}{\partial t} = \frac{1}{r}\frac{\partial}{\partial r}\left(rD\frac{\partial n}{\partial r}\right) \tag{3.3}$$

where n (cm^{-3}) is the concentration of conductive species, D ($cm^2 s^{-1}$) is the diffusion coefficient given by the Arrhenius law D = $D_0 exp(-E_A/kT)$, t is time and r is the radial coordinate.

Assuming an initial delta-like distribution of dopants, the solution to Eq. 3.3 is given by

$$n\left(r,t\right) = \frac{N}{4\pi Dt}e^{-\frac{r^2}{4Dt}} \tag{3.4}$$

where N is the integral of dopant concentration within a plane perpendicular to the filament axis, namely $N = \int n\left(r,t\right) 2\pi r dr$. Eq. 3.4 describes a Gaussian distribution which broadens for increasing time t. The standard deviation of the distribution increases according to $\sigma(t) = (2Dt)^{1/2}$, while the peak concentration decreases with time according to $n\left(0,t\right) = N\left(4\pi Dt\right)^{-1} = N\left(2\pi\sigma^2\right)^{-1}$. Defining an initial Gaussian spread $\sigma_0 = \sigma(t_0)$, corresponding to the programmed CF size, and a filament dissolution time $t_{1/2}$, corresponding to the time for a decrease of the peak concentration $n\left(0,t\right)$ by a factor of two, we obtain $n\left(0,t_{1/2}\right)/n\left(0,t_0\right) = \sigma_0^2/\left(2Dt_{1/2}\right) = 1/2$, which yields a time for the reset transition given by

$$t_{reset,u} = t_{1/2} - t_0 = \frac{\sigma_0^2}{2D} \propto A_{CF} \tag{3.5}$$

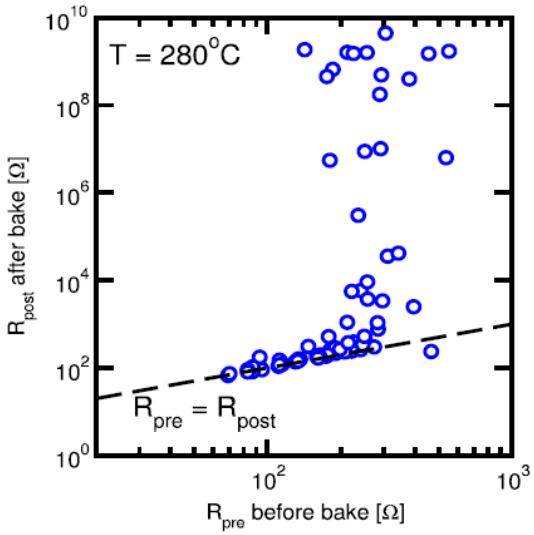

Figure 3.3: Resistance R_{post} measured after annealing as a function of resistance R_{pre} measured before annealing. Annealing was carried out at 280°C for 1 h.

Eq. 3.5 indicates that the reset time increases with the square of the initial size of the CF, or with its area. Equivalently, for a given reset time, T_{reset} and V_{reset} must increase for increasing size of the CF. In conclusion this phenomenon can be referred as a sort of size-dependent diffusion/oxidation process. For a further confirmation of the size-dependent reset effect, we performed annealing experiments on RRAM cells in the set state with different initial resistances, corresponding to different CF size. Fig. 3.3 shows the correlation plot of resistance measured after and before annealing, R_{post} and R_{pre}, respectively, at 280°C for 1 h. Data show that states with a relatively low R_{pre} maintained their resistance at the end of the annealing experiment, indicating a stronger stability against CF oxidation. On the other hand, states with $R_{pre} > 200$ Ω, corresponding to small CFs, show a larger probability for resistance degradation (this consideration will be deepened in Section 5.2).

Fig. 3.1 shows V_{reset} (a) and I_{reset} (b) obtained from calculations including the effects of size-dependent Joule heating and size-dependent diffusion/oxidation. The initial size of the filament was obtained from previous estimations taking into account the variable activation energy of resistance (see Section 2.3). Calculations were obtained from Eq. 3.1, where R_{th} was evaluated as the parallel of R'_{th} and R''_{th}, the latter being

assumed constant. T_{reset} was estimated by the Arrhenius formula

$$T_{reset} = \frac{E_A}{klog\left(\frac{D_0 t_{reset,u}}{\phi^2}\right)} \tag{3.6}$$

where $E_A = 1.4$ eV is the activation energy for filament oxidation [64], D_0 is a constant and T_{reset} was assumed equal to either 1 s, corresponding to DC operation, or 1 μs, corresponding to pulsed operation [47]. Size-dependent diffusion/oxidation is taken into account in Eq. 3.6 by the term $(\phi/\phi_0)^2$ in the logarithm, as a result of the area dependence of T_{reset} in Eq. 3.5. Size-dependent heating was taken into account by the presence of a thermal resistance R''_{th}. The best agreement with the high-R part of V_{reset} data is obtained for $R''_{th} = 2 \times 10^8 KW^{-1}$, which, after comparison with calculations in Fig. 3.2a, suggests that the thermal conductivity of NiO, responsible for R''_{th}, may be smaller than $k_{th,NiO} = 1Wm^{-1}K^{-1}$. The reset current was calculated according to $I_{reset} = V_{reset}/\mathrm{R}$. Both calculated V_{reset} and I_{reset} display good agreement with data, supporting our explanation for the observed resistance-dependent reset behavior. Note that the calculated V_{reset} and I_{reset} for pulsed operation ($t_{reset} = 1$ μs) are about a factor of two higher than those required for DC operation. This is in good agreement with experimental results, showing an approximately twofold increase of V_{reset} from the 1 s to the 1 μs timescale [47]. This is relevant from the application viewpoint, since an RRAM device must be operated in the pulsed mode in the ns-μs time range to maximize program/erase data throughput.

3.1.2 Numerical reset model

The numerical implementation of the change in resistance during reset needs a physics-based model for the conduction in the CF. This CF conduction model, based on transport in a localized region with high concentration n_D of defects, has been already described in Section 2.3. These defects are seen as dopants controlling the local conductivity according to the empirical behavior in Fig. 3.4a.

For high defect concentration, σ linearly increases with n_D to describe the enhanced metallic conductivity for increased defect density. In this n_D range, σ decreases with T according to the metallic behavior, namely $\sigma = \sigma_0[1 + \alpha(T - T_0)]^{-1}$, where R_0 and α are constants and T_0 is room temperature. The T-dependence of metallic conductivity, which is shown in Fig. 3.4b, is reflected by the measured and calculated $I - V$ curves in Fig. 3.5 where the resistance increases before the reset due to Joule heating within the CF [52].

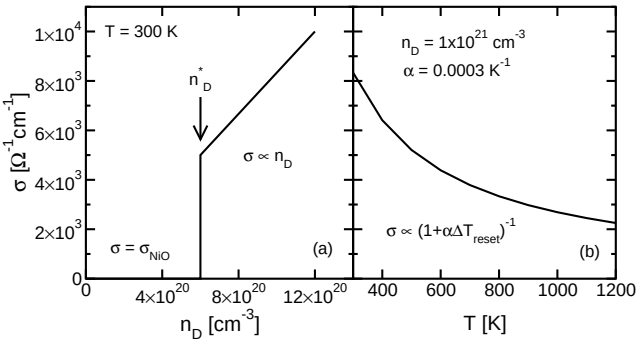

Figure 3.4: Conductivity σ as a function of defect density n_D for $T = 300K$ (a) and as a function of T for $n_D = 10^{21} cm^{-3}$ (b). The non-linear behavior of r describes percolation conductivity with an abrupt transition across a threshold concentration.

Below a threshold value $n_D^* = 6 \times 10^{20} cm^{-3}$ of the defect density, σ drops to the extremely-low NiO conductivity, $\sigma_{NiO} = 0.1\Omega^{-1} cm^{-1}$. This threshold density n_D^* may be viewed as a percolation threshold, below which σ sharply decreases [65]. This effect relates to the deepening of the Fermi level for decreasing n_D, as supported by the observed increase of the activation energy of $\sigma$for partially dissolved CFs (see Section 2.3). To describe the CF dissolution, the model calculates the temperature profile as a result of Joule heating, based on the steady-state Fourier equation

$$\nabla (k_{th} \nabla T) = -P''' = -\sigma F^2 \tag{3.7}$$

where k_{th} is the CF thermal conductivity, P''' is the Joule power density and F is the electric field. Defect diffusion is modeled by time-dependent Fick's law given by

$$\nabla (D \nabla n_D) = \frac{dn_D}{dt} \tag{3.8}$$

where D is the diffusivity given by $D = D_0 exp(-E_A/kT)$, where D_0 is a pre-exponential constant and E_A is the activation energy, where E_A = 1.5 eV and $D_0 = 10^{-3}$ cm^2 s^{-1}. Note that Joule heating accelerates the isotropic diffusion of defects through the exponential T-dependence of the diffusivity. Defect diffusion in the hottest region along the CF results in a drop of defect density around the middle of the CF. When the defect density decreases below the percolation threshold, the conductivity undergoes an abrupt reduction to the NiO value, causing a reduction of the current that collapses to the NiO leakage level. This leads in turn to a collapse of the local temperature, thus inhibiting defect diffusion from the CF. Fourier and diffusion equations were solved using a 3D partial differential equation (PDE) numerical solver.

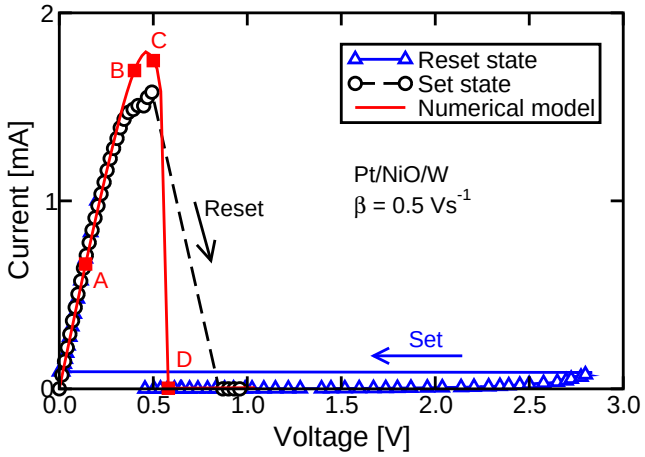

Figure 3.5: Measured $I-V$ curves for the set and reset states of a $Pt/NiO/W$ RRAM plug size device. The figure also shows the calculated reset characteristic. The four points AD indicate the bias points for simulations in Fig. 3.6.

Fig. 3.5 shows a typical $I-V$ curve obtained from simulations when a triangular voltage pulse is applied to the cell, with ramp rate $\beta = dV/dt = 0.5\ Vs^{-1}$. The calculated $I-V$ curve agrees well with the experimental data, reproducing the transition from low to high resistance. Fig. 3.6 shows the calculated profiles of T (a), n_D (b) and σ (c) along the linear and radial coordinates of the CF, for the four bias points A, B, C and D indicated in Fig. 3.5, corresponding to voltages 0.14, 0.4, 0.5 and 0.58 V, respectively. The voltage increase causes a temperature increase due to Joule heating as shown in Fig. 3.6a. The local temperature increase and the defect gradient strongly enhance diffusion at the CF surface around the middle of the filament, as shown in Fig. 3.6b. In fact, the top and bottom electrodes act as thermal sinks where the temperature is virtually fixed at T_0. The drop of n_D eventually results in the disconnection of the CF, as shown by the abrupt drop of σ at bias point D in Fig. 3.6c. According to the simulation results, diffusion effects only become significant in the timescale of the experiment when the temperature approaches a critical diffusion temperature, due to the Arrhenius law linking diffusion and local temperature. This is consistent with the observed abrupt drop of the current along the $I-V$ curve during reset in experimental $I-V$ curves as shown in Fig. 3.5. Note that the experimental curve shows a finite slope in the negative differential resistance region of the reset transition, this is due to a series resistance $R_S = 220\ \Omega$ in our experimental setup, while $R_S = 0\ \Omega$ was assumed in

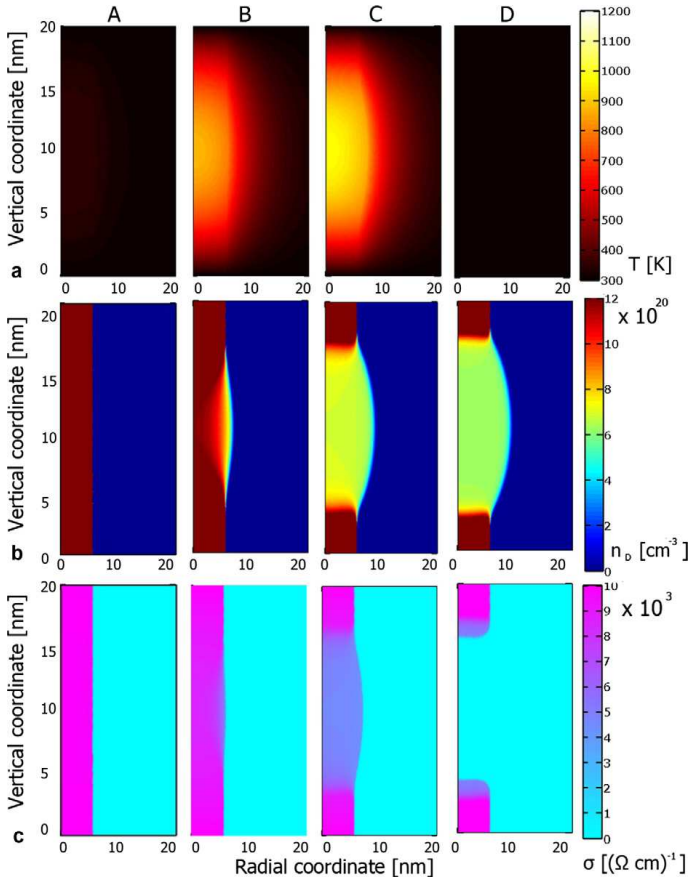

Figure 3.6: Maps of calculated T (a), n_D (b) and σ(c), for the four bias points (A)−(D) along the reset transition in Fig. 3.5. Note the abrupt CF disconnection due to the percolation threshold in Fig. 3.4a

the simulations.

Fig. 3.7 shows measured and calculated V_{reset} as a function of triangular pulse ramp rate $\beta = dV/dt$ for an initial set-state resistance R = 200 Ω. V_{reset} was taken in correspondence of the maximum current in the $I-V$ curves during reset. Results at high ramp rate ($\beta > 3\times10^2\ Vs^{-1}$) were obtained applying a triangular pulse and monitoring the voltage across the RRAM to identify V_{reset}, as indicated in the inset. V_{reset} at low β were instead obtained in the quasi-static mode. The increase of V_{reset} for increasing β is due to the temperature and time dependence of the diffusion kinetic [47]: For increasing β, less time is spent at each voltage (hence temperature) along the measurement sweep, thus an increasing voltage is needed to complete the CF dissolution process. Note

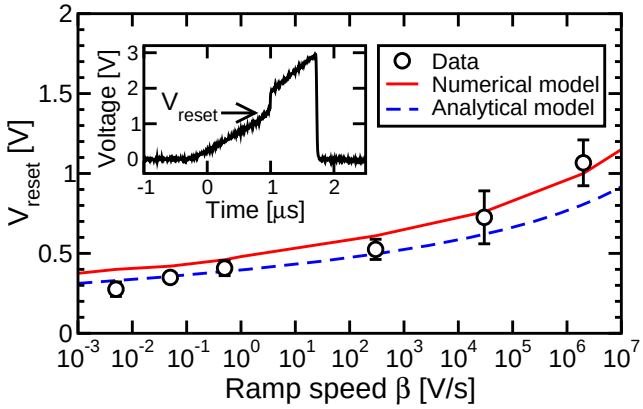

Figure 3.7: Measured and calculated V_{reset} as a function of the sweep rate $\beta = dV/dt$. Calculations from the numerical and the analytical models are compared.

that the time-temperature relationship is dictated by the activation energy: a good agreement in the β-dependence of V_{reset} thus indicates that a realistic value of $E_A = 1.5$ eV was assumed in the calculations [47,58]. The figure also shows results from a previous analytical model for the reset transition, showing a good agreement with experimental and numerical results [47]. Note that V_{reset} according to the numerical model is higher than the analytical results by about 20%. This is mainly due to the temperature profile within the CF, resulting in a typically large difference between the core and the surface temperatures for relatively large CFs at small resistances. On the other hand, the analytical model only assumes a constant temperature within the CF. Therefore, to heat the CF surface to the critical diffusion temperature, the core temperature needs to be higher, thus requiring a higher Joule power dissipation with respect to the analytical estimation.

Since the size dependence of reset parameters is a critical point for model validation, we simulated the reset transition as a function of the initial CF size, hence initial resistance. Fig. 3.8 shows results from both numerical and analytical models for the calculated core temperature at reset T_{reset} (a), V_{reset} (b) and I_{reset} (c) as a function of the initial resistance R, which is related to the CF cross-section A_{CF} according to $R \propto A_{CF}^{-1}$. Correspondingly the CF radius ranges from 25 to 0.25 nm for a 10-100 kΩ resistance range. For increasing R, hence decreasing A_{CF}, T_{reset} decreases in Fig. 3.8a, since the average n_D gradient guiding the diffusion process increases for decreasing CF size [64]. Correspondingly, V_{reset} decreases for small R in Fig. 3.8b. However, at larger $R > 1k\Omega$ (CF radius $< 2.5nm$), V_{reset} increases although the corresponding T_{reset}

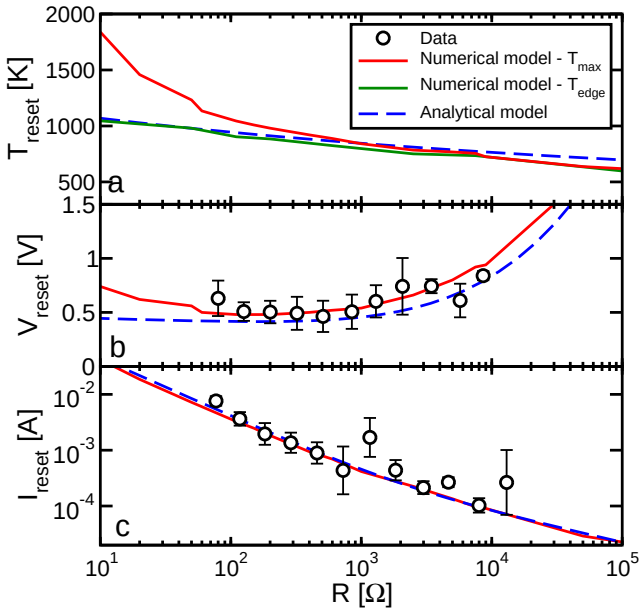

Figure 3.8: Measured and calculated T_{reset} (a), V_{reset} (b) and I_{reset} (c) as a function of the initial set-state resistance R. Calculations from the numerical and the analytical models are compared.

still decreases. As already explained in Section 3.1.1, this is due to the parasitic thermal conductance of the metal oxide surrounding the CF that provides an alternative, parallel path for heat loss [58]. Since the out-of-filament heat loss becomes increasingly important with the surface-volume ratio, CFs with small cross section and high resistance are increasingly affected. In such narrow filaments, the critical T_{reset} can thus be reached only at higher V_{reset}. Both numerical and analytical calculations display the same V_{reset} behavior, in good agreement with reported data from [63]. Fig. 3.8(c) shows the calculated I_{reset}, obtained as $I_{reset} = V_{reset}/R$ and reference data from [14]. I_{reset} decreases with R according to I_{reset}/R^{-1}, due to the almost constant V_{reset} in Fig. 3.8b. These results confirms the need for a reduction of the filament size to achieve low reset current in the 1 - 10 μA range [63, 66].

In Fig. 3.9 we anticipate some data retention results that will be deeply discussed in Chapter 5 in order to show the validity of the model also for retention simulations.

Experiments were conducted by constant-T annealing between 250 and 323°C, and τ_R was defined as the time for a R increase by a factor 10 [63]. Data refer to different statistical percentiles from 50% to 90%.

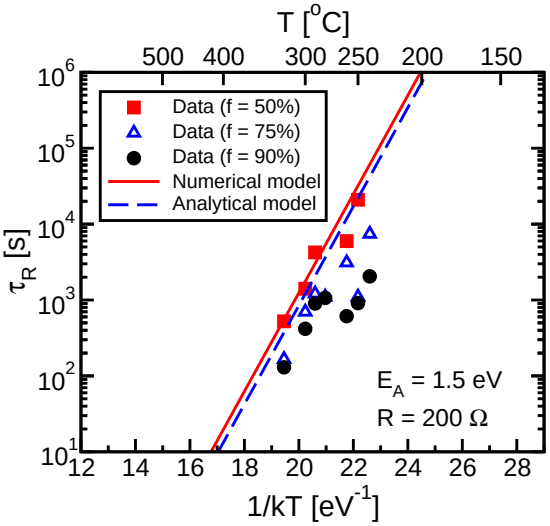

Figure 3.9: Arrhenius plot of measured and calculated τ_R. Different f values refer to percentiles in the measured statistical sample

To calculate τ_R, we used the same thermally- activated diffusion model as for reset, where a constant and uniform T was used instead of a temperature profile due to Joule heating. Simulated τ_R was defined as the time needed to reduce the peak concentration to n_D^*. Results from an analytical model, assuming an initial Gaussian defect profile along the radial coordinate, are also shown [63]. The calculations account very well for the measured τ_R, although analytical calculations show a lower τ_R, due to the initial pre-diffused condition.

Fig. 3.10 shows the calculated n_D (a) and σ (b) for increasing annealing times $t = 0$, 250 and 540 s at $323°C$. A comparison with Fig. 3.6 allows to clarify the impact of the temperature profile in providing localized (reset in Fig. 3.6) or uniform (data loss in Fig. 3.10) dissolution of the CF. In the retention case the filament dissolves uniformly along the CF length because of the uniform temperature, although diffusion in strongly localized at the CF surface where the n_D gradient is maximum. A single set of parameters D_0 and E_a were used in reset and retention simulation, allowing for a unified modeling of RRAM operation and reliability.

3.1.3 Analytical Set Modeling

The set transition can be viewed as a soft breakdown phenomenon that causes the formation of the CF. This process is critical since it determines

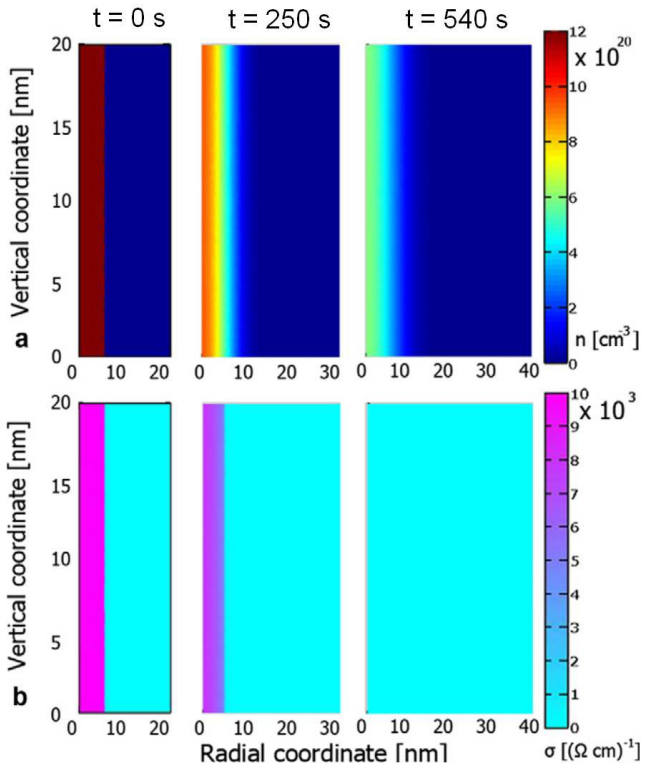

Figure 3.10: Calculated profiles of n_D (a) and σ (b), corresponding to three different stages, namely $t = 0$, 250 and 540 s, of the annealing simulation at $323°C$.

most of the characteristics of the switching behavior of the cell. In fact, the set operation determines the resistance of the set state, which in turn controls the reset current (see Chapter 4). Given its importance, a good understanding and modeling of this process is necessary to develop and improve RRAM devices and arrays. To this purpose, the kinetics of the set transition is critical.

To understand the relationship between V_{set}, I_{set} and R, we make use of the filament model reported in Section 2.3. The resistance R of the semiconductive filament can be described by the following PF equation [53]

$$R = \frac{kT\tau_0 t_{NiO}}{q^2 A_{CF} N_T \Delta z^2} e^{\frac{E_{AC}}{kT}} \tag{3.9}$$

where τ_0 is the attempt-to-escape characteristic time for the carrier from the localized state, t_{NiO} is the thickness of the NiO layer corresponding to the CF length, N_T is the density of dopants, A_{CF} is the CF area and

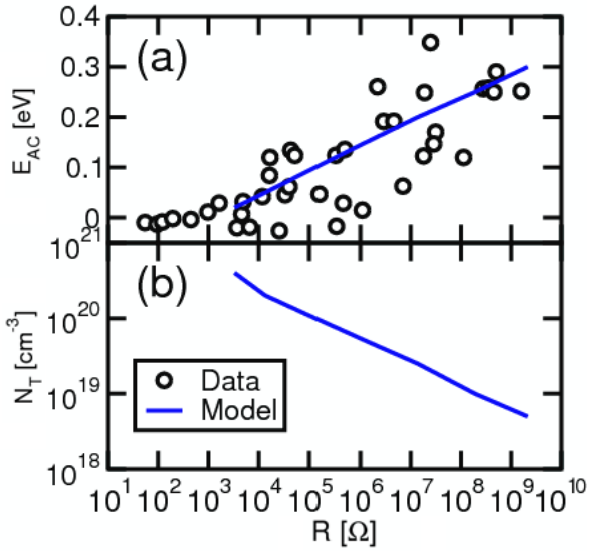

Figure 3.11: Measured and calculated correlation between R and E_{AC} (a) and the corresponding defect concentration N_T as a function of R (b).

Δz is the distance between positively charged defects, modulating the band edge and dictating the potential energy barrier for PF transport [53].

Fig. 3.11a shows calculations according to Eq. 3.9, using $\tau_0 = 0.5$ x 10^{-14} s, $t_{NiO} = 30$ nm, A = 10 nm^2 and the variable defect concentration N_T shown in Fig. 3.11b. The concentration of defects and the corresponding E_{AC} were independently changed, according to the qualitative picture in figure 7, where the transition from weak to strong doping results in a shift of the Fermi level, hence in a decrease of the activation energy toward 0, i.e. the metallic state. With these assumptions, Eq. 3.9 can provide a close prediction of the dependence between activation energy and resistance in NiO CFs. Note that the NiO thickness used in the calculations ($t_{NiO} = 30$ nm) differs from the experimental value of 25 nm, although the main conclusions regarding the relationship between resistance, activation energy and set parameters remain unaffected.

To describe the set process and related parameters V_{set} and I_{set}, we rely on the interpretation of the set transition based on threshold switching [67]. Time-resolved experiments have revealed the signature of threshold switching in the set transition of NiO RRAM devices [46]. Threshold switching is an electronic process of conductivity enhancement from a high resistance OFF state to a low resistance ON state [20].

The conductivity change is completely reversible, i.e. the OFF state can be recovered once the voltage is reduced below a specific holding value, which is the minimum voltage capable of sustaining the excited carrier distribution responsible for the ON state. Set experiments in NiO revealed that either a stable set transition from high to low resistance occurred, or the transition to the low resistance state showed recovery of the high R state [46]. This was interpreted by the cell voltage after switching decreasing below the holding voltage, that is the minimum voltage able to sustain the ON state [46]. It is important to note that previous works have found clear evidence for threshold switching in NiO. Oxygen-rich NiO films were found to be unable to display resistance switching although they showed threshold switching at sufficiently high voltage [48]. On the other hand, threshold switching was found to take place in NiO films with thin bottom electrodes [68] and in NiO films at high operating temperatures [69], which was explained by excessive T along the CF during its formation, thus resulting in a sudden formation-destruction dynamics due to thermally activated reset. Threshold switching might thus be a systematic precursor in the CF formation mechanism, with the stable set transition resulting from the extremely high local T and high current density, especially in the presence of set current overshoots due to relatively large parasitic capacitances [41, 46].

To account for set parameters, we thus used a threshold switching model based on conduction by a PF mechanism and carrier excitation due to high-field energy gain [70]. According to this model, carriers moving along a trap chain (represented by a high-R, low-N_T CF) gain kinetic energy at high field based on the following differential equation

$$\frac{d\left(E_F - E_{F0}\right)}{dz} = qF - \frac{qn_T}{J}\frac{E_F - E_{F0}}{\tau_{rel}} \tag{3.10}$$

where E_F and E_{F0} are the quasi-Fermi and the equilibrium Fermi levels, respectively, F is the electric field, τ_{rel} is the characteristic time for carrier energy relaxation, J is the current density and n_T is the concentration of trapped carriers [38]. The two terms on the right-hand side represent the field-driven energy gain and the energy relaxation effects, balancing each other at a characteristic excess energy $E_F - E_{F0}$. Since the carrier conductivity exponentially depends on the difference between the quasi-Fermi level (representative of the electron population probability being 1/2) and the band edge, even a minor increase of E_F results in a huge increase in conductivity. The non-uniform profile of E_F results in a collapse of electric field along the CF, leading to a negative differential resistance and in a corresponding instability at the basis of the sudden

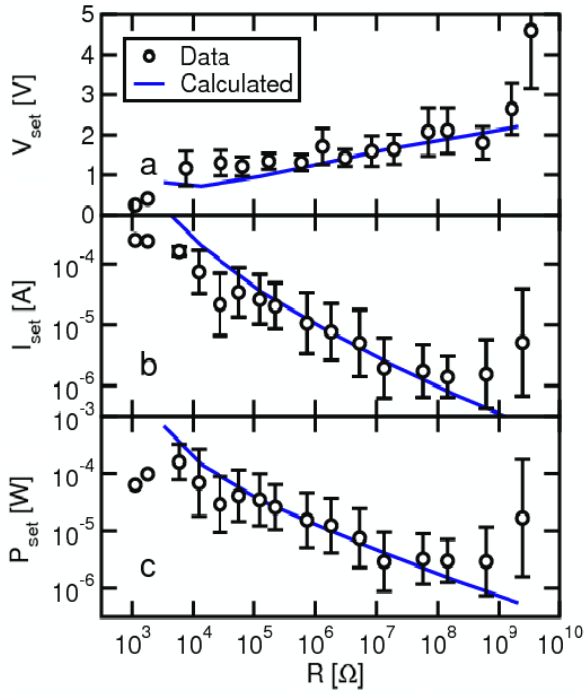

Figure 3.12: Measured and calculated V_{set} (a), I_{set} (b) and their respective product P_{set} (c) as a function of R.

transition to the high conductivity ON state [38]. An approximated close formula for the threshold switching power density P_T''', which is the product between threshold field and current density, is obtained assuming a critical condition for threshold switching $E_F = E_{F0} + kT$, that is a conductivity enhancement by a factor e. This leads to [70]

$$P_T''' = \frac{\gamma_T N_T (kT)^2}{\tau_{rel} \left(E'_C - E_{F0}\right)} \tag{3.11}$$

where $\gamma_T \approx 1$ is a constant and E'_C is the minimum energy of the conduction band.

Fig. 3.12 shows the measured and calculated V_{set} (a), I_{set} (b) and $P_{set} = V_{set} I_{set}$ (c), as a function of resistance. Measurements were done in DC conditions and the set transition was operated under constant current. Note that these parameters mark the onset (starting point in the OFF state) for the set transition, and thus can be fully accounted for by the threshold switching model. On the other hand, threshold switching cannot account for the material transformation (i.e. Joule

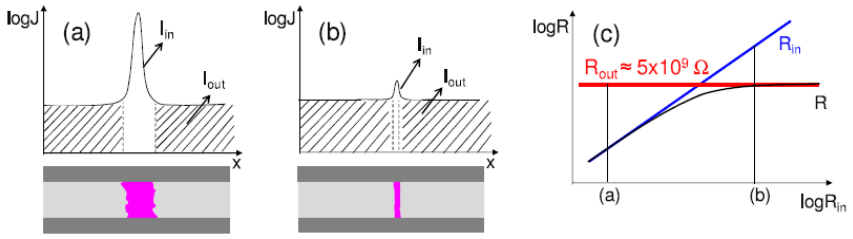

Figure 3.13: Schematic for the current density profile along the device area, for a strong (a) and weak CF (b). The overall resistance is dominated by the filament R_{in} or by the out-of-filament resistance R_{out} for strong and weak filaments, respectively (c).

heating, chemical reduction and/or oxidation, defect generation) that may take place after threshold switching. The P_{set} behavior can be explained based on Eq. 3.11 and given the increase of E_{AC} with R in Fig. 3.11a and the decrease of N_T with R in Fig. 3.11b. For decreasing R, the concentration of trapped carriers that need to be excited for conductivity enhancement increases, resulting in an increase of the power density at switching. The V_{set} and I_{set} behaviors are a consequence of the P_{set} dependence on R and of the $I-V$ curve. In fact, P_{set} from Fig. 3.12c approximately decreases as $R^{-0.5}$. Thus within a linear approximation of $I-V$ characteristics, we can write

$$V_{set}I_{set} = RI_{set}^2 = P_{set} \propto R^{-0.5} \tag{3.12}$$

which yields $I_{set} \propto R^{-0.75}$ and $V = IR \propto R^{0.25}$. These results qualitatively explain the smooth V_{set} increase with R and the large decrease of I_{set} for increasing R in Fig. 3.12a and b. The calculation results in the figures were obtained by accurate calculations using a numerical model, thus accounting for the nonlinear I-V curves. These results confirm that the threshold switching model can account for the R dependence of set parameters, and thus may be valuably used for predicting set transition parameters depending on the high-R state parameters (e.g. R, E_A, N_T).

The behavior of set parameters in the high-R regime, Fig. 3.12, deserves further analysis. Here, the set voltage dramatically increases at extremely high R close to 1 GΩ. Correspondingly, I_{set} and P_{set} strongly increase in the same resistance range. This can be understood by the schematics in Fig. 3.13. For a large filament with low R (a), the measured resistance R is dominated by the resistance of the CF R_{in}, while the resistance R_{out} of the remaining area of the device can be neglected. Conversely, a small filament may have $R_{in} \gg R_{out}$ (b). Thus the fil-

ament current cannot be distinguished from the uniform current flowing through the sample. The out-of-filament resistance R_{out} is approximately given by the pristine device, thus $R_{out} = 5$ x 10^9 Ω in our samples. The overall measured resistance is shown in Fig. 3.13c: for $R_{in} \gg R_{out}$, V_{set} continues to increase according to the threshold switching model discussed above. However, the measured R remains clamped at R_{out}. The steep V_{set} increase in Fig. 3.12 is thus due to the saturation of resistance to R_{out}, although another switching mechanism could also come into play at higher voltages. For similar reasons, one may expect a steep decrease of I_{set} at the saturated R_{out}. However, in this resistance regime I_{set} is dominated by out-of-filament current I_{out}, as clarified by Fig. 3.13. Thus, the current strongly increases at the increasing V_{set} due to the relatively steep voltage dependence of the current for the pristine state. This effect can account for the increase of I_{set}, hence of P_{set} , at high resistance in Fig. 3.12.

3.2 HfO bipolar modeling

The electrical characterization experiments conducted on HfO-based memories reveal the importance of field-driven migration in the resistive-switching mechanisms for bipolar VMC cells (see Chapter 1). Of course the same basic temperature-activated nature of the reset process is shared between unipolar- and bipolar-switching RRAM devices but the radial diffusion model of the previous Section 3.1.1 strictly applies to unipolar switching only.

3.2.1 Analytical Reset Modeling

In the case of bipolar switching ion migration contributes to the dissolution process in addition to pure diffusion [21, 71]. This is schematically shown in Fig. 3.14, depicting the potential profiles for ion migration along the CF with and without an applied bias. Migrating species may consist of positive metallic ions, negative oxygen ions, or positive oxygen vacancies. Migration may be described by ion hopping among localized states, characterized by an effective energy barrier E_A, which we will assume equal to the activation energy for diffusion used in the previous section [71, 72]. The application of a bias results in a barrier lowering for hopping; thus, the ion hopping rate r_{ion} can be given by [58]

$$r_{ion} = r_0 e^{-\frac{E_A - q\alpha V}{kT}} \tag{3.13}$$

where r_0 is a pre-exponential factor and α is a coefficient controlling the barrier lowering effect. As shown in Fig. 3.14, αV gives the barrier

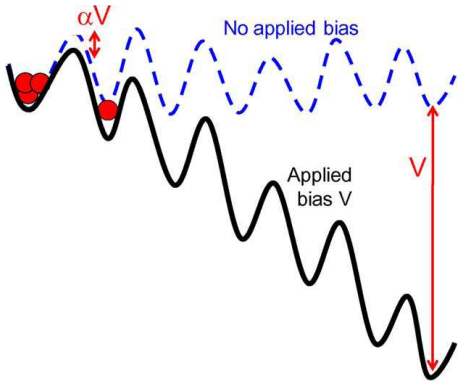

Figure 3.14: Schematic illustration of the potential profile for ion hopping along the CF with and without an applied bias. Ions diffuse randomly when the applied voltage is zero. The barrier lowering αqV induces ion migration in the direction of the electrostatic force in the presence of an applied voltage V.

lowering in the direction of the field for a positive ion [58]. Therefore, α may be approximated by $\Delta z/2L_{CF}$, where Δz is the distance among ion hopping states and L_{CF} is the length of the filament. The latter may be assumed equal to the thickness of the oxide layer, in case of a CF with approximately uniform conductivity and cross section. Evidence for migration controlling set and reset in a bipolar-switching device comes from the fact that the polarity must be necessarily reversed for repeatable switching. Note that, although the electric field plays a key role in the ion migration owing to the barrier lowering effect in Fig. 3.14, the temperature dependence is nonetheless very important, given the Arrhenius model for ion migration in Eq. 3.13 [71, 72]. Based on Eq. 3.13, the reset time $t_{reset,b}$ for bipolar switching can thus be obtained by a generalization of Eq. 3.5, where a voltage-dependent activation energy is used to describe ion migration in the direction of the electrostatic force, namely

$$t_{reset,b} = \frac{\phi^2}{D} = \frac{\phi^2}{D_0} e^{\frac{E_A - q\alpha V}{kT}} \tag{3.14}$$

where the voltage-induced barrier lowering has been included in the Arrhenius law. Using the Joule heating formula and $t_{reset,b} = \tau$, Eq. 3.14 yields a second-order equation in V, which can be solved to obtain a closed formula for the reset voltage V_{reset} [73]. Note that the approximation in Eq. 3.14 is physically consistent with the fact that, for decreasing V toward zero, the unipolar-switching formula of the previous section is recovered. In addition, the CF dissolution requires that its cross section is reduced to zero, thus justifying the dependence of

$t_{reset,b}$ on the diameter ϕ (instead, e.g., of the CF length L_{CF}) in Eq. 3.14.

3.2.2 Numerical Reset Modeling

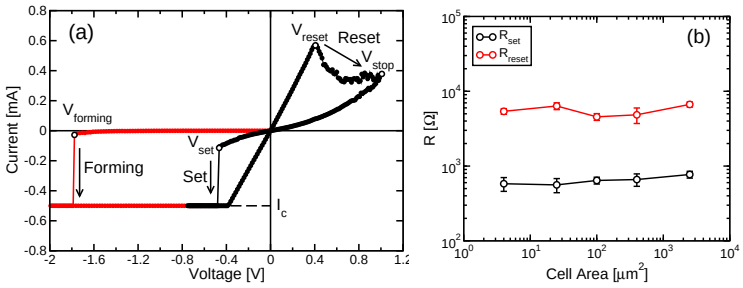

Figure 3.15: Measured $I-V$ curves in our $TiN-HfO_x-TiN$ bipolar RRAM, showing forming, set and reset. Note the analog reset under positive voltage (a). Measured R for set/reset states as a function of device area. The lack of area dependence supports filamentary switching (b).

Fig. 3.15a shows measured $I-V$ curves under forming/set (V $<$ 0) and reset (V $>$ 0). The $I-V$ curve shows analog reset, i.e. R starts increasing at $V_{reset} = 0.4$ V, then saturates around 1 V. The filamentary nature of set/reset is demonstrated in Fig. 3.15b, showing that R for set/reset states does not depend on device area. Further evidence comes from Fig. 3.16, showing R after set/reset as a function of compliance current I_C during set, compared to other unipolar/bipolar RRAMs [43]: R scales with ${I_C}^{-1}$, due to self-limited filament growth during set (see Section 2.2). These results support filamentary switching in our HfO_x RRAM.

Analog reset was characterized for set states S1, S2, S3 and S4 with different R (between 0.25 and 1.7 kΩ) obtained by different I_C in Fig. 3.16 (partial set algorithm). Fig. 3.17a shows measured $I-V$ curves for reset, indicating an almost constant reset voltage $V_{reset} = 0.4$ V for the onset of the reset transition. For comparison, reset transition was studied in reset states, obtained by interrupting the reset sweep at increasing stopping voltage V_{stop} [74, 75] (partial reset algorithm). Fig. 3.17b shows $I-V$ curves of reset states R1, R2, R3 and R4 starting from S2. In contrast to Fig. 3.17a, V_{reset} increases from 0.4 to 0.9 V for increasing R. Fig. 3.18a summarizes the V_{reset} dependence on R: Set/reset states show different V_{reset} for the same R, suggesting that set and reset states with equal R have different structure/shape of the conductive filament (CF). A pictorial view of different nature of the CF

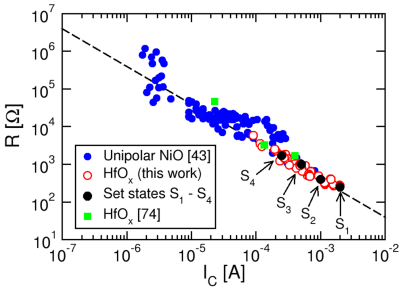

Figure 3.16: Measured R in the set state as a function of compliance current I_C, namely the maximum current during set. Literature data are from [43, 74].

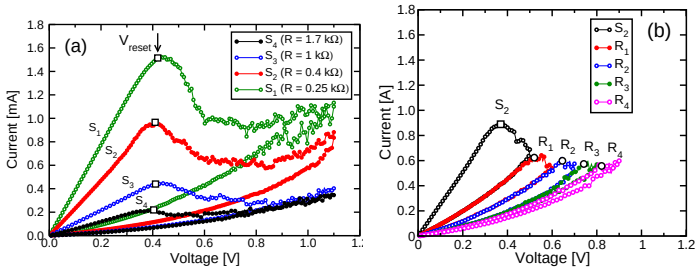

Figure 3.17: Measured $I - V$ curves for set states S1, S2, S3 and S4 in Fig. [**?**]. V_{reset} remains almost constant irrespective of R (a) Measured $I - V$ curves for set (initial) state S2 and reset states R1, R2, R3 and R4 obtained by reset at increasing V_{stop} (b).

is given in Fig. 3.18b where for reset and set states we have respectively a variable gap region or a variable A_{CF}.

To account for analog-reset characteristics and to explain the different CF nature in set/reset states, we developed a switching model based on ion migration. Similar to the one proposed in Section 3.1.2, the CF is assumed to consist of a sub-oxide phase with locally-enhanced density n_D of dopants, namely excess Hf or O-vacancies. The flux j_D [$\mathrm{cm^{-2}s^{-1}}$] of ionized dopants during set/reset is given by the drift-diffusion equation

$$j_D = -D\nabla n_D + \mu n_D F \tag{3.15}$$

where D [$\mathrm{cm^2s^{-1}}$] is the ion diffusivity, μ [$\mathrm{cm^2V^{-1}s^{-1}}$] is the ion mobility and F is the electric field. Thermally-activated diffusion according to the Arrhenius law $D = D_0 exp(-E_A/kT)$ was assumed, where $D_0 = 2$

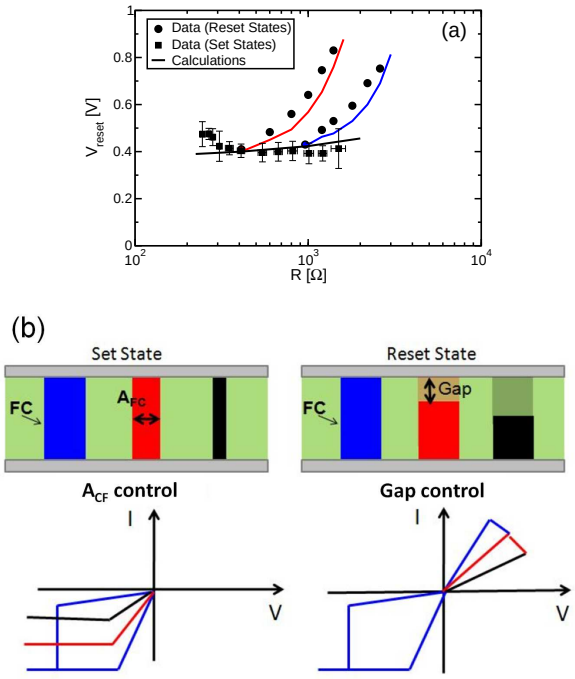

Figure 3.18: Measured and calculated V_{reset} as a function of R (a) and sketches evidencing the different nature (b) for set and reset states.

x 10^7 m^2/s is the diffusivity pre-factor and $E_A = 1$ eV is the activation energy [76, 77]. The latter dictated both diffusion and migration (i.e. drift), as these obeyed the Einstein relation $D = \mu kT/q$.

Eq. 3.15 is solved with (i) Poisson equation $\nabla j = 0$ for the electrical current density j, (ii) Ohm law $j = \sigma F$ where the electrical conductivity σ increased with doping according to Fig. 3.19a, and (iii) steady-state Fourier equation $\nabla\cdot(k_{th}\nabla T)$=-j$\cdot F$, where k_{th} is the thermal conductivity, which increased with n_D according to Fig. 3.19b.

Fig. 3.20a shows the measured and calculated $I - V$ curves during reset for set states S2 and S3 in Fig. 3.17a. These states were simulated by cylindrical CFs with diameter $\phi = 14$ and 9 nm, respectively, with uniform $n_D = 12 \times 10^{21}$ cm^{-3}. Reset starts at $V_{reset} = 0.4$ V, then R gradually increases up to about one decade.

Reset $I - V$ curves were calculated for set states in Fig. 3.21a, corresponding to different ϕ, and reset states in Fig. 3.21b, corresponding to different V_{stop} along the reset sweep. The resulting V_{reset} are summarized in Fig. 3.20a: V_{reset} remains constant for set states, while it increases with R for reset states, in agreement with data.

Fig. 3.22 describes the reset dynamics in the model, showing the 2D

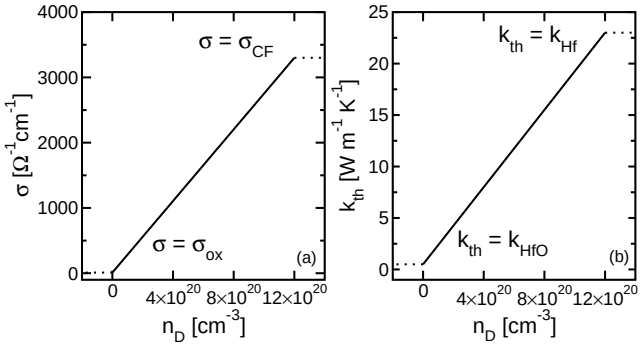

Figure 3.19: Electrical (a) and thermal conductivity (b) as a function of dopant density n_D in the numerical model.

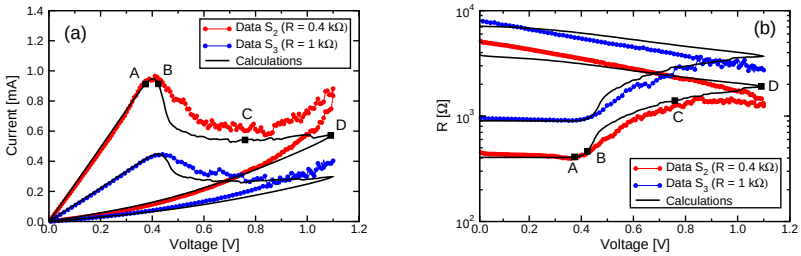

Figure 3.20: Measured and calculated $I-V$ (a) and $R-V$ (b) curves for set states S2 and S3

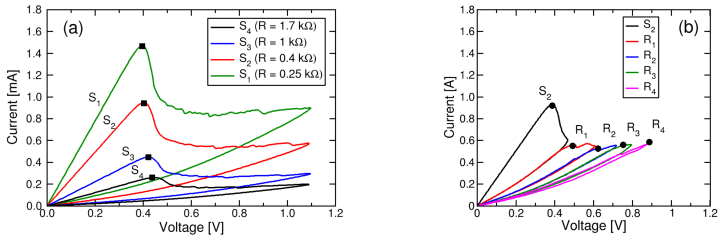

Figure 3.21: Calculated $I-V$ curves for set states (a) and reset states (b) with different initial R. V_{reset} remains almost constant in the first case while increases in the latter.

maps of n_D, T and potential V (from top to bottom, respectively) at bias points A, B, C and D along the reset sweep of S2 in Fig. 3.20a. Fig. 3.23 shows the corresponding profiles along the symmetry axis. Dopants migrate to the negative (bottom) electrode, thus leaving a depleted gap of increasing length Δ (shaded area in Fig. 3.23). Analog reset can be

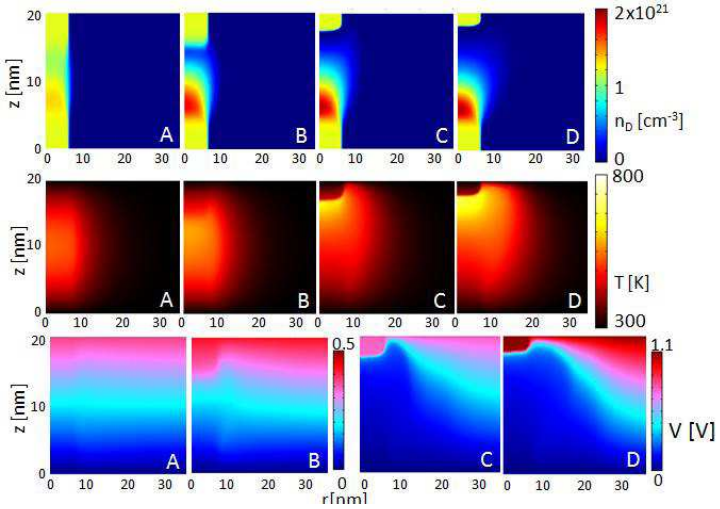

Figure 3.22: Calculated map of dopant density n_D (top), T (middle) and potential V (bottom), for bias points A, B, C and D along the reset sweep of S2 in Fig. 3.20a.

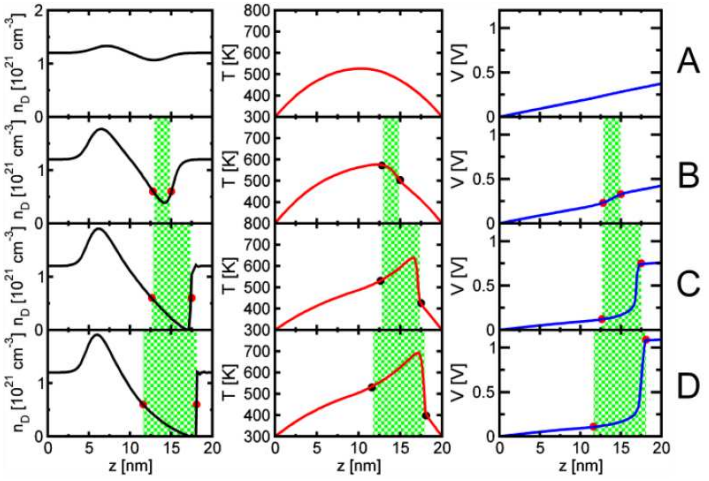

Figure 3.23: Profiles of n_D, T and V obtained from simulation results in Fig. 3.22 in correspondence of the cylindrical axis of the CF. The depleted gap, defined for n_D < 6x10^{20} cm^{-3}, is marked as a shaded area.

described as follows: After the onset of reset, the decrease of σ in the gap locally enhances F = $|dV/dz|$ and $j{\cdot}F$, hence T. However, the T increase in the gap is hindered by k_{th} decreasing less than σ as a function of n_D in Fig. 3.19. Therefore, the gap formation results in poorer heating

efficiency, thus inhibiting further depletion by ion migration. The Δ-dependent Joule heating also accounts for the V_{reset} increase with R for reset states (Fig. 3.17) as opposed to the constant V_{reset} of set states due to the fixed R_{th}/R in cylindrical CFs [76].

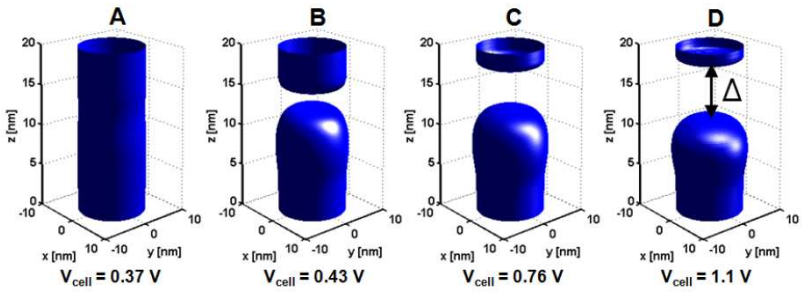

Figure 3.24: CF shape represented by the contour plots of n_D for reset states A through D, showing the increasing size of the depleted gap Δ

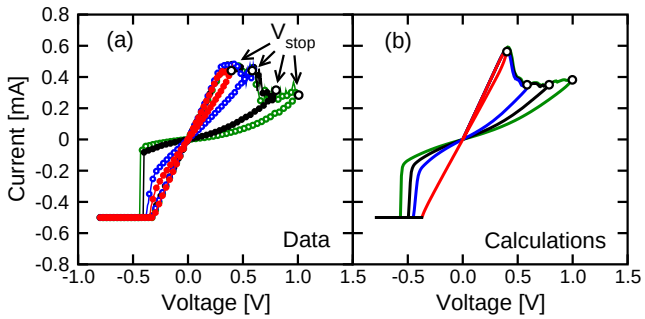

Figure 3.25: Measured (a) and calculated (b) $I-V$ curves for reset (V > 0) and set (V < 0). The set voltage V_{set} increases with the stopping voltage V_{stop} used in the reset sweep, hence with R.

Fig. 3.24 shows contour plots of n_D at simulated points A-D, showing a Δ increase up to about 6 nm in D. The increasing gap can be experimentally evidenced by the set voltage V_{set}: The measured $I-V$ curves in Fig. 3.25a show that V_{set} increases in reset states for increasing R [75]. The calculated $I-V$ curves (Fig. 3.25b) are in good agreement with data, supporting the gap-based interpretation of reset states and the ion migration model for describing set/reset states and processes.

Fig. 3.26 shows measured (a) and calculated $I-V$ curves (b) for increasing sweep rate $\beta = dV/dt$. The model can account for the increase of V_{reset} at increasing β due to the tradeoff between transition time

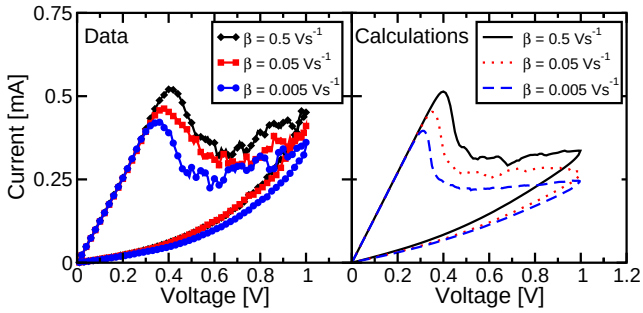

Figure 3.26: Measured (a) and calculated (b) $I-V$ curves showing reset for variable sweep rate $\beta = dV/dt$. V_{reset} increases with β due to the time-temperature tradeoff in the Arrhenius law for ion migration.

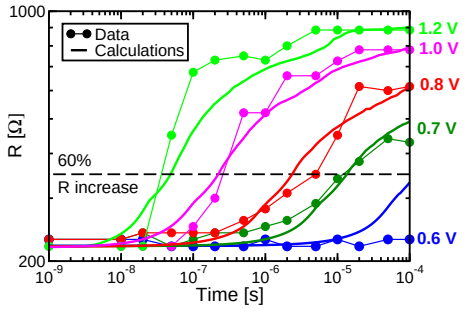

Figure 3.27: Measured and calculated R as a function of reset pulsed-width for increasing pulse voltage V_p. The reset time is defined at a 60% increase of resistance.

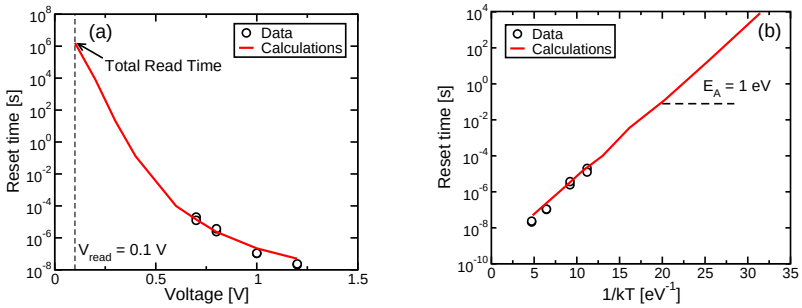

Figure 3.28: Measured and calculated reset time as a function of V_p (a) and 1/kT (b). The model allows extrapolations at low V_p (hence low T) for program/read disturb predictions.

and temperature (i.e. applied voltage) in the Arrhenius-driven reset process [47, 76].

To investigate pulsed reset, we performed time-resolved experiments to monitor R after the application of voltage pulses of width t_p = 10 ns - 100 μs. Fig. 3.27 shows measured and calculated R as a function of t_p for increasing voltage V_p. Calculations agree with data, supporting our model for simulating ns-μs reset. Fig. 3.28 shows measured/calculated t_{reset}, defined as the time for a 60% increase of R, as a function of V_p (a) and 1/kT (b), i.e. the Arrhenius plot. Model-based extrapolations to low V_p are shown, allowing for read-disturb predictions in the set state.

3.3 Universal reset for unipolar/bipolar RRAM

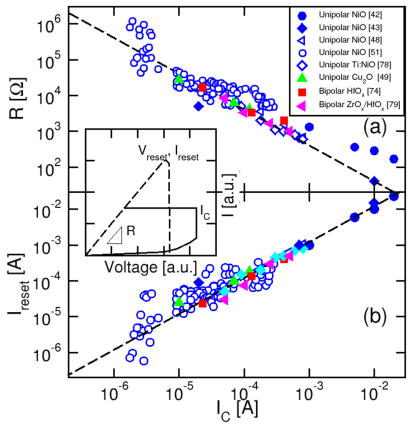

Figure 3.29: Measured (a) set-state resistance R and (b) I_{reset} as a function of I_C. Data are shown for several unipolar and bipolar RRAM devices with different active materials, including NiO [42,43,48,51,78], Cu_2O [49], HfO_x [74], and ZrO_x/HfO_x [79]. The inset shows the schematic $I-V$ curves for (solid) unipolar set and (dashed) reset transitions, defining parameters I_C, V_{reset}, I_{reset}, and R.

Despite the wide range of materials and switching polarity, all the data in Fig. 3.29 fall along the same trend. In particular, R in Fig. 3.29a is inversely proportional to I_C according to the empirical law

$$R = \frac{V_0}{I_C} \tag{3.16}$$

where V_0 is about 0.4 V, while I_{reset} in Fig. 3.29b is proportional to I_C with a ratio I_{reset}/I_C of about 1.2. The dashed lines in the figure correspond to the two empirical laws of constant V_0 [Fig. 3.29a] and constant I_{reset}/I_C ratio [Fig. 3.29b]. From Eq. 3.16, one can estimate the reset voltage V_{reset} from the product R$I_{reset} \approx V_0 I_{reset}/I_C \approx$1.2 x

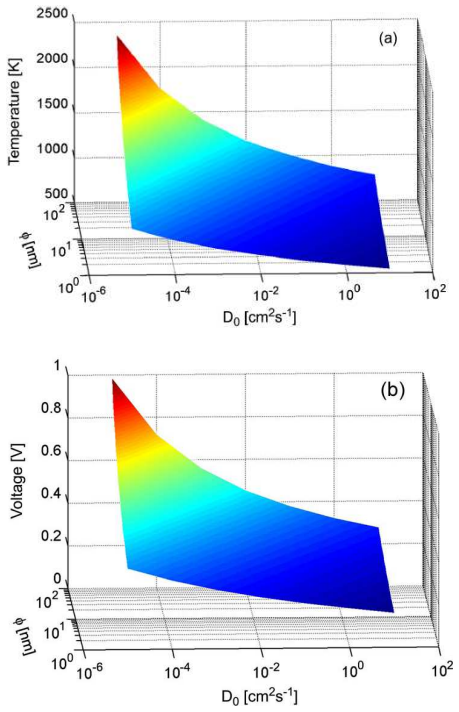

Figure 3.30: Calculated (a) T_{reset} and (b) V_{reset} from (3) and (5), respectively, as a function of parameters D_0 and ϕ for unipolar-switching devices

0.4 $\approx$ 0.5 V. This indicates that the universal reset characteristic in the figure is due to an approximately constant V_{reset}, irrespective of the unipolar/bipolar-switching mode and of the oxide material used in the RRAM device.

Fig. 3.30a shows T_{reset} calculated by Eq. 3.6 as a function of D_0 and ϕ. These two parameters were changed in a broad range of six orders of magnitude (D_0 between 10^{-5} and 10 cm^2s^{-1}) and two orders of magnitude (ϕ between 1 and 100 nm), respectively. E_A was kept equal to 1.4 eV, close to the measured activation energy from reset and retention experiments in NiO [47, 64]. This value is also comparable to the calculated energy barrier for Ni vacancy diffusion in NiO [80], thus supporting the key role of diffusion as the limiting step in the reset process. A characteristic time $t_{reset,u} = 10^{-2}$ s was used, corresponding to DC measurements. Due to the logarithmic dependence on D_0 and ϕ in Eq. 3.6, the calculated T_{reset} remains within a narrow range between 500 K and 2500 K, despite the large range assumed for D_0 and ϕ. From these results, T_{reset} may display only a weak dependence on host and CF materials, due to the logarithmic dependence on D_0 in Fig. 3.30a.

Similarly, different CF sizes may result in a relatively small change of T_{reset}.

Note that assuming an initial delta-like distribution of dopants in Eq. 3.4 means that the low-resistance state is assumed to be due to a single CF. In the case of multiple filaments being responsible for the low-resistance state in the memory, similar results would be obtained. In fact, assuming that R is due to N identical CFs instead of a single CF, the individual area of multiple CFs is N times smaller than the single-CF case. As a result, the reset temperature T'_{reset} for N parallel CFs becomes

$$T'_{reset} = \frac{E_A}{klog\frac{ND_0\tau}{\phi^2}} \tag{3.17}$$

which is clearly smaller than T_{reset} in Eq. 3.6. However, due to the logarithmic dependence on N, the reset temperature remains almost unchanged with respect to the calculations in Fig. 3.30a.

From the estimated T_{reset} it is possible calculate the reset voltage V_{reset} by inverting Eq. 3.1. For a metallic CF at T_{reset}, the ratio between R and R_{th} can be given by the Wiedemann-Franz (WF) law for the ratio between thermal conductivity k_{th} and electrical conductivity σ, yielding [52]

$$\frac{R}{R_{th}} = \frac{8k_{th}}{\sigma} = 8LT_{reset} \tag{3.18}$$

where L = 2.48 x 10^{-8} $V^{-2}K^{-2}$ is the Lorenz constant. The factor 8 in Eq. 3.18 comes from the steady-state solution of the Fourier equation during reset in the CF and is due to the uniform Joule dissipation and the heat conduction toward the top and bottom heat sinks. Fig. 3.30b shows these results as a function of D_0 and ϕ. Both parameters were chosen in the same range as in Fig. 3.1a. Again, despite the large range of D_0 and ϕ, the reset voltage varies within a relatively small range from 0.2 to 1 V. This demonstrates that the unipolar reset model based on thermally activated CF dissolution can account for the weak dependence of V_{reset} on CF and host materials in the RRAM, consistently with data in Fig. 3.29.

Eq. 3.18 assumes that Joule heating dissipated during reset mainly flows along the CF toward the top and bottom heat sinks. On the other hand, assuming that R_{th} includes a non-negligible contribution of heat loss through the metal-oxide region surrounding the CF, the ratio R/R_{th} may be larger than that in Eq. eq:wf, thus leading to a larger V_{reset}. Similarly, assuming that heat conduction includes a significant phonon contribution [52], larger values for R/R_{th} and, consequently, for V_{reset} may be obtained.

Eq. 3.18 assumes that the CF has a metallic conduction characteristic, where both electrical and thermal conductions are controlled by electrons. This assumption is strictly valid only for relatively small R below 1 kΩ, since CFs with higher R typically display a semiconductor-like conduction [64]. However, it should be noted that the activation energy for conduction E_{AC}, describing the semiconductor-like transport, is smaller than 0.1 eV for R below 100 kΩ, which represents the majority of data in Fig. 3.29. In addition, at high voltage close to the reset point, the carrier concentration in the semiconductor-like CF is highly enhanced, due to the following: 1) the field-induced barrier lowering, which decreases E_{AC} as in the PooleFrenkel effect, and 2) the temperature-induced emission of carriers to the conduction/valence bands. These multiplication effects result in charge carriers providing the main contribution to thermal and electrical conductions close to the reset point, thus supporting the WF law for calculating the resistance ratio in Eq. 3.18.

Note also that the thermally activated reset model in Eq. 3.6 is experimentally supported by the evidence for the temperature dependence of reset parameters on the sample temperature T_0. For instance, it was shown that the reset power in unipolar NiO decreases for increasing T_0 as a result of the smaller temperature increase $\Delta T = T_{reset} - T_0$ to reach the critical oxidation temperature [81]. Similar results were obtained for bipolar switching: For increasing T_0, V_{reset} was shown to decrease in bipolar HfO_2 [82], and the reset time at a given pulse voltage was shown to decrease in bipolar ZnO [83]. These evidences support the thermally activated CF dissolution model for both unipolar and bipolar switchings in RRAM operation.

3.4 Complementary Switching

Complementary resistive switch (CRS) has been recently proposed as a promising memory element able to solve the sneak-path problem for future RRAM crossbar arrays [84]. Fig. 3.31 schematically shows the structure of the CRS (a) and the $I-V$ characteristics (b) that can be obtained biasing this device with positive/negative voltage sweeps. From the architectural point of view the CRS basically consists of a stack of two conductive-bridging RRAM (CBRAM) cells antiserially-connected. The result is a memory device with one inert top electrode (TE) and bottom electrode (BE), e.g. Pt, and two solid-electrolyte switching layers separated by a common active electrode, e.g. Cu. The two binary logic states necessary to store a bit of information corresponds to the conductive filament (CF) shunting either (1) the top switching layer,

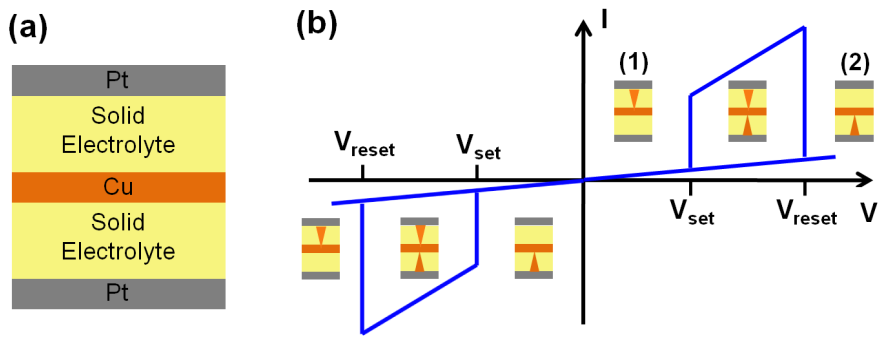

Figure 3.31: Schematic structure (a) and $I-V$ characteristics (b) of the conventional CRS based on an anti-serial connection of two CBRAMs [84]. Sketches of CF's evolution during voltage sweep are also shown

or (2) the bottom switching layer (see sketches in Fig. 3.31b). It is noteworthy that the overall device, at the end of a program operation shows always a high resistance thus avoiding the presence of leaky paths during the successive reading operation [84]. To switch the memory element from the high resistive state (1) to the high resistive state (2) of Fig. 3.31b a positive voltage sweep must be applied to the top electrode. This program operation causes first of all (i) a set process, i.e. formation of a CF in the bottom layer by Cu^+ migration toward the bottom electrode, and then (ii) a reset process, i.e. consumption of the CF in the top layer by Cu^+ migration back to the Cu common electrode. In this way we succeeded in moving the CF from the up layer, i.e. state (1), to the bottom layer, i.e. state (2). In the same way a negative bias can be applied to switch the cell from state (2) to state (1) in Fig. 3.31b. The reading operation is performed applying a positive TE voltage above the set voltage V_{set} [84]. The fabrication of a CRS was also shown for $Pt/ZrO_x/HfO_x/metal/HfO_x/ZrO_x/Pt$ and $Pt/ZrO_x/HfO_x/ZrO_x/Pt$ stacks, indicating that not only CBRAMs but also oxide-RRAMs can be used for the realization of this kind of memory element [79].

The CRS shown in Fig. 3.31a or the ones proposed in [79] require a complex stacking of metal-oxide/metal layers thus resulting in a delicate fabrication process and in the fast degradation of the common active internal electrode [79, 84]. The integration complexity may be reduced by the introduction of complementary switching (CS), a new program operation that can be performed in single-stack nonpolar-RRAM devices. CS can be obtained thanks to the natural asymmetry of reset state, where

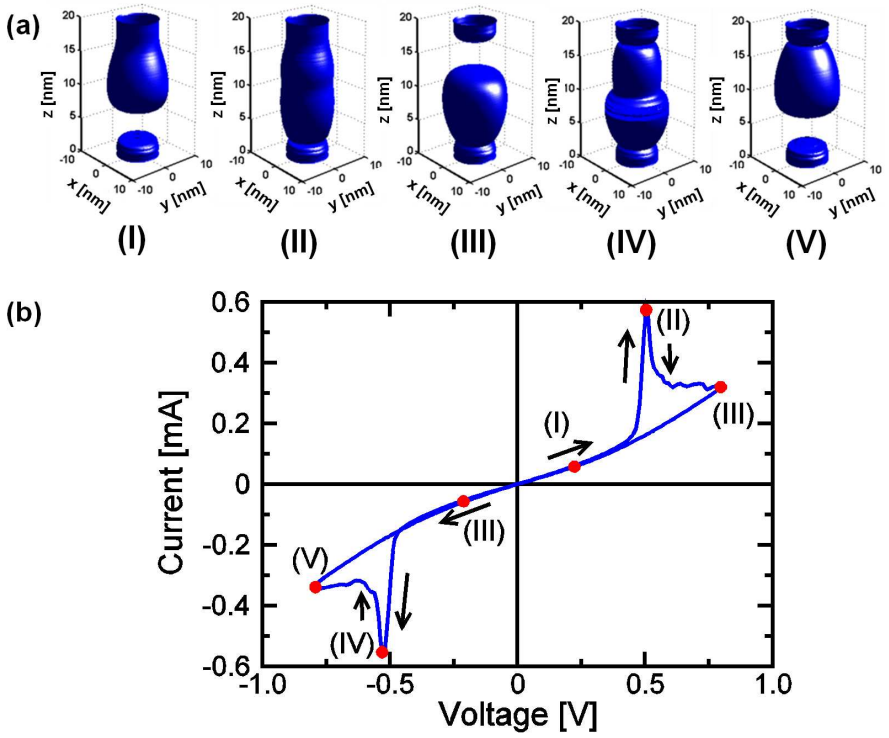

Figure 3.32: Calculated CF shape (a) and corresponding $I-V$ characteristics (b) for applied positive (I-III) and negative (III-V) ramped voltage. The broken CF (I) reforms as the gap is refilled by migrating positive ions (II), then a new gap is opened at the positive TE (III). Similarly, under $V<0$ the gap is refilled (IV), then reopened at the BE [state (V), same as (I)]. The $I-V$ curves evidence set (I→ II) and reset (II→III) transitions under positive voltage, then set (III→IV) and reset (IV→V) transitions under negative voltage.

a depleted gap can be selectively created close to the BE or the TE by the application of a positive or negative voltage respectively. Fig. 3.32a shows the evolution of calculated CF shape obtained by simulations with a numerical model for unipolar/bipolar switching [76]. The initial shape (I) is obtained by the application of a negative reset inducing a depletion of conductive defects (e.g. excess Hf or O-vacancies in HfO_x) close to the BE. An applied positive voltage causes defects migration toward the BE, resulting first of all in CF reconnection (II), followed by depletion of the CF at the TE side (III). In the same way, a negative TE voltage can be applied to state (III) resulting first of all again in CF reconnection (IV), and then in gap formation (V). Anyway this time the depleted region is close to the BE thus leading to state (V) analogous to

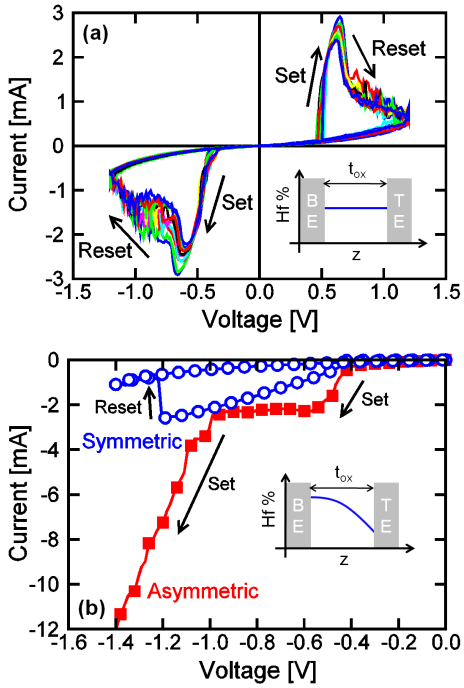

Figure 3.33: Measured $I-V$ curves for symmetric RRAM, demonstrating complementary switching (CS) in single-stack nonpolar-RRAM, (a) and asymmetric RRAM (Hf-rich close to the BE, see inset) (b). The necessity of a symmetric structure for CS is evidenced.

the initial state (I). It is noteworthy that each program sequence ends up with a reset operation which leaves the memory element always in a high resistive state. In this way, like in CRS, we are able to avoid the presence of leaky paths during the successive reading operation. Using the same numerical model for unipolar/bipolar switching [76] used to represent the evolution of CF under CS programming in Fig. 3.32a, it is possible to obtain the calculated $I-V$ curves shown in Fig. 3.32b. It is here evidenced the intrinsically symmetric set/reset switching between low resistive states (II, IV) and high resistive states (I→V, III) under positive and negative voltage.

The experimental validation of CS in a single-stack nonpolar-RRAM device is shown in Fig. 3.33a. This oxide-RRAM structure is a simple $TiN-HfO_x-TiN$ stack with 5 nm-thick HfO_x as active layer material. The uniform Hf concentration profile (see inset in Fig. 3.33a) allowed for a fully symmetric nonpolar-RRAM device. As a result, CS operation is possible and the voltage levels for both set ($V_{set} \approx 0.5$ V) and reset ($V_{reset} \approx 0.7$ V) show only a minor asymmetry while chang-

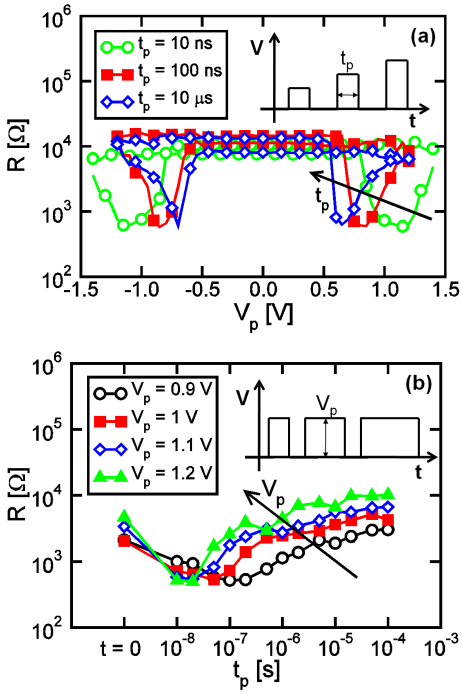

Figure 3.34: Measured R as a function of the pulse voltage V_p for increasing pulse-width t_p (a) and as a function of the pulse-width t_p for increasing pulse voltage V_p (b).

ing the polarity of the applied bias. To further support our physical interpretation of CS, we performed electrical characterization also on asymmetric RRAM devices, i.e. with non-uniform Hf concentration profile (see inset in Fig. 3.33b). Due to this asymmetry the typical nonpolar behavior is impossible, thus CS operation is not expected. In fact, during the application of a negative bias, these particular devices are able to perform set process but they are not able to switch again to a high resistive state (see red curve in Fig. 3.33b). Reset is prevented by virtually-unlimited ion supply at the BE side, thus inhibiting the achievement of state (c) in Fig. 5.11a-b. These experiments conducted on devices with different Hf concentration profile suggest the necessity of symmetric structures, i.e. nonpolar-RRAM devices, being CS itself an inherently symmetric program operation.

In order to access the performances of CS under pulse programming, we applied trains of pulses of increasing voltage V_p at fixed pulse width t_p. Fig. 3.34a shows the cell resistance R measured after each pulse, evidencing the change from high-R, to low-R and again to high-R for each of the pulsed polarity used. These results are in complete agreement

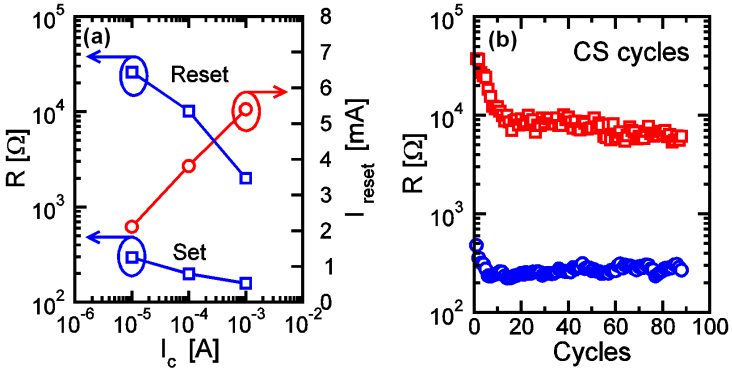

Figure 3.35: Set/reset R and I_{reset} as a function of forming I_C (a) and CS cycling characteristics for $I_C = 10$ μA (b). The window is degraded after about 15 cycles.

with data shown for voltage sweeps in Fig. 3.33b. For decreasing t_p we can observe a shift toward higher values for the threshold voltages of set and reset operations. Fig. 3.34b shows measurements from other pulsed-CS experiments where R is measured at fixed V_p and increasing t_p. For high V_p the set transition is fast, i.e. < 10 ns, not detectable with our experimental setup. Anyway the trends for the time necessary to set and reset operations are clear, both decreasing for increasing V_p.

The use of CS in high-density crossbar arrays necessitates a high R window. In fact, the read current I_{on} must be at least 2-3 times higher than the off-leakage $(N-1)I_{off}$, where N is the number of bit-lines/wordlines and I_{off} is the current measured using a $V/2$ or $V/3$ program scheme [85]. From here the necessity to improve the ratio I_{on}/I_{off} in order to obtain the maximum N. We succeeded in improving this ratio by I_{off} reduction, limiting the CF size by I_C control during forming operation. Fig. 3.35a shows CS data for $I_C = 10$, 100 μA and 1 mA: R window increases and reset current I_{reset} decreases for decreasing I_C due to the decreasing CF size [43]. However, Fig. 3.35b shows that R window degrades after about 15 cycles. This can be attributed to the absence of any form of current compliance during CS which leads to the lost of CF control due to unlimited growth during set operation. Another way for I_{on}/I_{off} optimization might be the choice of a proper material, as shown by nonpolar-RRAM devices reported in [86–90] which show R window up to more than 10^7. Besides material engineering, architectural solutions can be implemented, e.g. replication of small array units with maximum I_{on}/I_{off} on the chip area and/or stacking in $3D$ structures.

The introduction of CS should be interpreted more than a new pro-

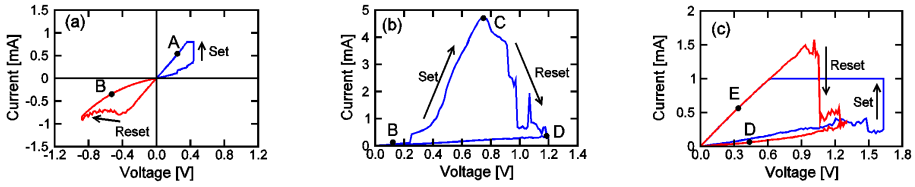

Figure 3.36: $I - V$ curves displaying BS (a), CS transition step with positive set/reset (b) and US (c). States A→E refer to the description in Fig. 3.37.

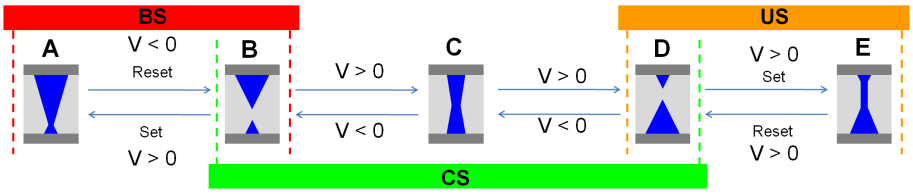

Figure 3.37: Schematic explanation of the transition from BS to US through CS. States A through E are highlighted in the $I - V$ curves of Fig. 3.36.

gram operation for RRAM or a promising solution for the development of future high density architectures. The physical interpretation of this new phenomenon can shed light into the frequently-observed and not clearly understood coexistence of bipolar switching (BS) and unipolar switching (US) in the same RRAM device [91]. Fig. 3.36 shows $I - V$ curves of BS, CS and US operated in sequence on the same RRAM device. The evolution of the CF during each of this phases is shown in Fig. 3.37, giving a pictorial view of the temperature- and field-accelerated ion migration mechanisms that govern each type of switching. In the BS regime (Fig. 3.36a), the CF switches between a continuous CF (A) after positive set and a depleted CF (B) after negative reset. Note that in this type of switching a current compliance must be used to control the growth of the CF. The application of a positive sweep to state B, without current compliance and with stop voltage above the usual BS set threshold ($V_{set} \approx 0.45$ V), results in CS (Fig. 3.36b). In accordance with the applied field, ions migrate from the TE side (B) resulting first in CF reconnection/growth (C) and then in CF depletion at the TE side (D). The use of a positive voltage above CS values ($V \approx 1.2$ V) combined with current compliance, leads to set under US mode (Fig. 3.36c), with gap filling (D → E) and depletion (E → D).

Note that in this last case the gap is refilled by ion displacement opposite to the applied electric field. This may be explained by electro-

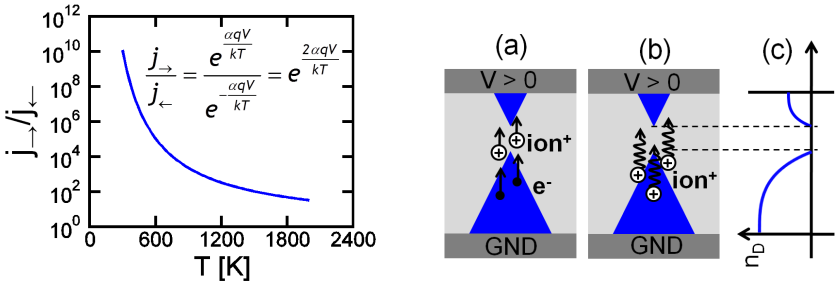

Figure 3.38: Calculated ratio between migration rates in the forward direction $j_{\rightarrow} \propto e^{(\alpha qV/kT)}$ and reverse direction $j_{\leftarrow} \propto e^{(-\alpha qV/kT)}$ as a function of T. Mechanisms for unipolar set D → E in Figs. 3.36 and 3.37, namely electromigration (a) and high-T diffusion (b) driven by the gradient of dopant concentration n_D (c).

migration due to momentum-transfer from electrons to ions (Fig. 3.4a), and/or gradient-driven diffusion of ions (Fig. 3.4b-c), due to relatively large set voltage (V_{set} = 1.65 V in Fig. 3.36c while V_{set} = 0.45 V in Fig. 3.36a). A high V_{set} (hence T) promotes isotropic ion-migration, as shown by the calculated ratio of forward/reverse migration rates in Fig. 3.4. The ratio decreases with T, supporting the role of diffusion-driven CF growth in US instead of field-driven migration. This scenario is confirmed by endurance data in Fig. 3.39: US displays the minimum endurance (250 cycles) due to the high V_{set} (hence high local T), as opposed to high endurance in migration-driven BS (7000 cycles) and CS (1000 cycles).

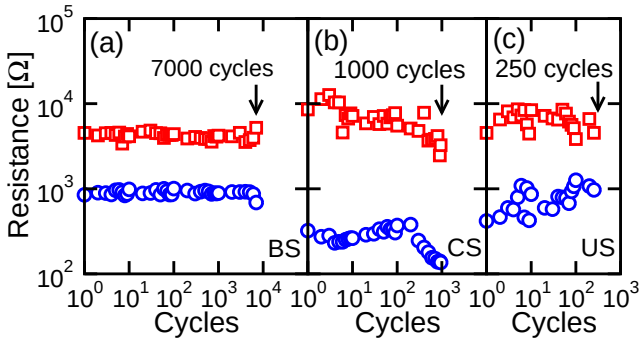

Figure 3.39: Measured DC cycling endurance for BS (a), CS (b) and US (c). Endurance is minimum for US due to the high V_{set}, hence high T at switching. BS displays the best endurance due to low voltage, T and ionic displacement.

Chapter 4

Program power control

Physics is like sex.
Sure, it may give some practical results,
but thats not why we do it.

Richard Feynman (1918-1965)

One of the main issues with RRAM devices is the high current required for the program operation. In this chapter we show how to control power dissipation exploiting the 1T1R structure. Moreover we will try to access program performances of single conductive filament by CAFM technique.

4.1 Reset current scaling

One of the advantages that make RRAM devices very attractive is the possibility to achieve high density cross-point arrays, leading to a strong reduction of costs per bit. However, this structure requires a selector device, in series to the memory cell, that address the single bit. The unipolar behavior of NiO-based RRAM memory enables diodes to be used as selectors. This is an evident advantage in terms of costs respect to MOS transistors. However the need for a high I_{reset} limits the dimension of the select-diode in the cross-bar array [93]. Therefore, reducing I_{reset} is mandatory for the development of a cross-bar structure.

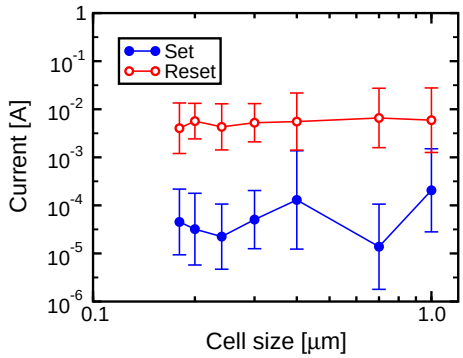

Figure 4.1: Measured current for set and reset operations as a function of cell size in NiO memory devices [92]

Fig. 4.1 shows measured set current I_{set} and reset current I_{reset} as a function of cell size in unipolar NiO memory devices [92]. Both I_{set} and I_{reset} do not scale with the BE size, due to the localized nature of set and reset at a CF. In particular, all the current in the set state flows along the low-resistance CF, which is negligibly small as compared to the typical cell area, ranging from 1 μm to 0.18 μm (see Fig. 4.1). As we have demonstrated in Chapter 2, the CF size was estimated in fact by electrical characterization in the range of few tens of nm at most [64].

Note that data in Fig. 4.1 were obtained from RRAM cells without selector, where the set operation was performed at constant current, i.e. the current was nominally limited to the value achieved at the set transition. However, due to parasitic capacitances and to the finite response time of the measurement system in readjusting the voltage after switching, the set transition was presumably affected by a significant current overshoot [42,94]. Thus, no specific control of the CF formation process was put in place in Fig. 4.1, which explains the large I_{reset}.

The absence of cell-area dependence in Fig. 4.1 can be understood by a simple Joule heating model for unipolar reset operation already presented in Section 3.1. Reset transition is the result of thermally-activated diffusion and oxidation processes taking place at the CF, thus reset is primarily controlled by Joule heating. For a given transition time, determined for instance by the voltage sweep rate $\beta = dV/dt$ in the experiment [67], reset occurs at a critical temperature T_{reset} given by the following steady-state equation

$$T_{reset} = T_0 + R_{th} R I_{reset}^2 \tag{4.1}$$

where T_0 is the initial temperature of the CF, R_{th} is its equivalent ther-

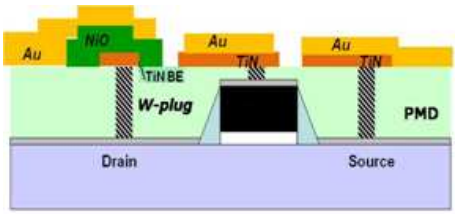

Figure 4.2: Schematic representation of the 1T1R cell structure fabricated for the experimental results presented in this chapter.

mal resistance and $P = RI_{reset}^2$ is the dissipated Joule power during the process [47, 95]. Eq. 4.1 can be rewritten as

$$I_{reset} = (T_{reset} - T_0)^{1/2}(RR_{th})^{-1/2} \tag{4.2}$$

To a first order approximation, both R_{th} and R are inversely proportional to the CF area A_{CF}, thus from Eq. 4.2 we obtain:

$$I_{reset} \propto A_{CF}. \tag{4.3}$$

This suggests that I_{reset} can be efficiently reduced by properly decreasing A_{CF} [58]. This can be achieved reducing the available current that flows through the cell during the set operation [42, 48, 96]. I_{reset} reduction below 100 μA was in fact demonstrated in 1T1R structures where the drain current I_D supplied by the select transistor was properly limited for a control of A_{CF} [42, 96].

In order to study I_{reset} scalability, we measured 1T1R devices as schematically shown in Fig. 4.2. The n-MOSFET was made by a 130 nm process, with a channel length $L = 1\mu m$, width $W = 10\mu m$ and a gate oxide thickness of 1.6 nm. The memory element, i.e. a NiO-based RRAM, was integrated on the drain and consisted of a stack of a 90 nm-width W-contact plug obtained by PVD and dry-etch patterning, a 30 nm-thick TiN bottom electrode with area $0.24\mu m^2$, an electron beam evaporated polycrystalline cubic NiO [97]. The NiO thickness was 35 nm, and NiO was capped by an Au top electrode obtained by lift-off technique.

Fig. 4.3a shows the measured I_D of the integrated series MOSFET as a function of drain-source voltage V_{DS} for increasing gate voltage V_G, from 0 to 2.6 V. Fig. 4.3b shows the measured $I_D - V_G$ curve for a fixed $V_{DS} = 1$ V. I_D displays a relatively large on-off swing from about 0.1 μA to about 300 μA, allowing for a good control of the current during the set operation.

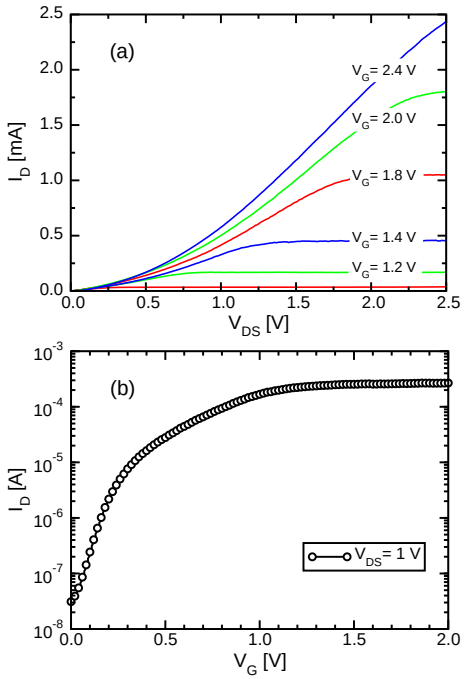

Figure 4.3: Measured $I-V$ characteristics of the isolated select transistor (1T device) with W/L = 10 μm / 1 μm and a gate oxide thickness of 1.6 nm. The $I_D - V_{DS}$ curves (a) are measured at various V_G and indicate a superlinear behavior at low currents, possibly due to a parasitic series resistance R_S. The I_D-V_G curve is measured at V_{DS} = 1 V and indicates a good control of I_D over a swing of about 4 decades.

Fig. 4.4a shows the measured R after set as a function of drain current I_D used in the set operation. R increases for decreasing I_D due to the decreasing size of the CF (see Section 2.2).

Data in Fig. 4.4 indicate that a good control of R can be achieved through a proper choice of I_D. This can be used for programming the cell into intermediate states between set and reset. Different states thus correspond to different cross section of the CF. This flexibility is a key for the development of multilevel programming in NiO-based RRAMs. At the same time, size-dependent reliability of the CF should be carefully taken into account, since it will be demonstrated in Chapter 5 that small size CFs are more prone to early data loss [64], pulsed set-reset instability [66] and random telegraph signal noise (RTN) [98].

Fig. 4.4b shows the measured I_{reset}, i.e. the maximum current reached during a DC reset sweep, as a function of I_D. I_{reset} increases linearly with I_D during the set operation, which can be understood by

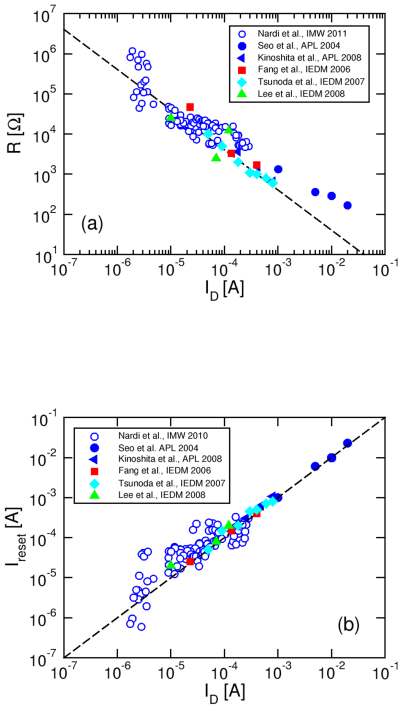

Figure 4.4: Measured R after set operation (a) and measured I_{reset} (b) as a function of I_D for our 1T1R structures. Data from 1T1R and stand-alone cells with other active materials are shown for comparison [42, 48–51].

Eq. (4.3). Data show that I_{reset} can be reduced below 10 μA: This unprecedented low reset current is obtained through careful control of the CF size thanks to the extremely low parasitic capacitance in the integrated 1T1R device. Both Figs. 4.4a and b display literature data for RRAM cells with different active materials. The good consistency of our data with other material systems demonstrate that current-controlled set features an almost universal dependence of filament size (expressed by R) and critical temperature (expressed by I_{reset}) on I_D. Different materials include NiO_x [42,48], CuO [49], Ti-doped NiO [51] and HfO_2 [50].

Fig. 4.5 shows measured $I-V$ characteristics displaying reset transitions with sub-10 μA reset current. I_{reset} scales for increasing resistance obtained from set operation. This behavior is also visible in Fig. 4.6 for a wide range of resistance values. The figure also shows data for I_{reset} as a function of R for states obtained by partial reset operation

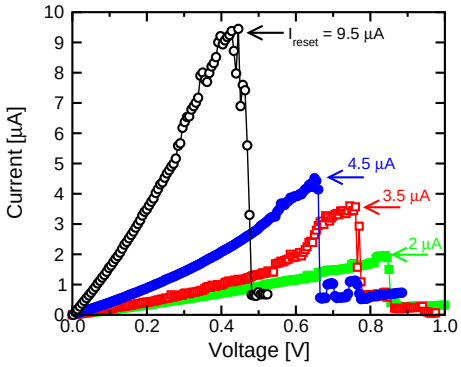

Figure 4.5: Measured $I-V$ characteristics for reset operation demonstrating the feasibility of a sub-10 μA reset current.

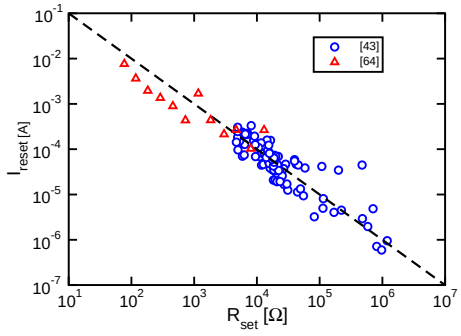

Figure 4.6: Measured R as a function of I_{reset} from Figs. 4.4a and b. The figure also shows data obtained from partial reset in isolated RRAM cells [64]. The two sets of data indicate a good consistency with each other.

in isolated RRAM cells [64]. The consistency between the two sets of data suggests that the filament nature and morphology for a given R may be similar, irrespective of the electrical operation used to achieve the RRAM state. On the other hand, as we will see in Chapter 5, large set resistance may degrade reliability in terms of diffusion-limited data retention [64] and random telegraph noise [98]. Both these reliability issues critically depend in fact on the size of the conductive filament, hence on the programmed cell resistance.

Fig. 4.7 shows measured currents and voltages for set and reset operations. Set current I_{set} decreases and set voltage V_{set} increases in agreement with recently reported data for isolated NiO memory cells [99]. The increase of set voltage with R is due to the increase of activation energy for conduction E_{AC} in the reset state, which results in an increase

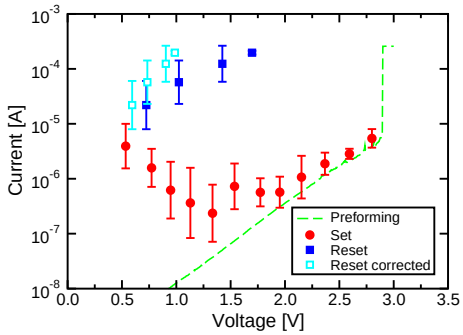

Figure 4.7: Correlation plot of current and voltage for the set (filled red circles) and the reset (open blue squares) operations. Reset data corrected for the parasitic and the MOSFET series resistances, thus revealing the "true" voltage drop at the memory cell, are also shown. Set data are grouped in two different regimes, namely group A and B.

of the threshold voltage for electrical threshold switching initiating the set transition [70]. The increase of E_{AC} with R is also responsible for the decrease of the set current $I_{set} \propto exp(-E_{AC}/kT)$ [70]. Note that the exponential drop of I_{set} is stronger than the almost linear dependence of V_{set} on E_{AC}, thus resulting in a decrease of $P_{set} = V_{set}I_{set}$ with R [99]. This behavior is highlighted in the scatter plot of Fig. 4.7 for data within group A. On the other hand, states with higher values of R (group B) display an increase of both I_{set} and V_{set} with R. Note that the increase of set voltage and currents follows the virgin-state $I-V$ characteristic measured before forming. This can be understood by the CF current becoming more and more negligible compared to the uniform current through the insulating layer of active material. Thus I_{set} is no more controlled by the CF properties (*i.e.* size and E_{AC}), rather contains the uniform current through the NiO layer. The reset current I_{reset} follows Eq. 4.2, while the reset voltage V_{reset} increases for decreasing resistance in the set state. This contradicts previous data showing an almost constant V_{reset} for variable R [63]. This can be understood by the additional voltage drop at the MOSFET and, more importantly, on the series resistance R_S causing the superlinear $I-V$ behavior in Fig. 4.3. In fact, R_S results in a voltage drop during reset transition causing a larger V_{reset}:

$$V_{reset} = V'_{reset}\left(1 + \frac{R_S}{R}\right), \tag{4.4}$$

where V'_{reset} is the "true" voltage across the cell at reset. The effective V'_{reset} was extracted eliminating the additional voltage drop at R_S. The

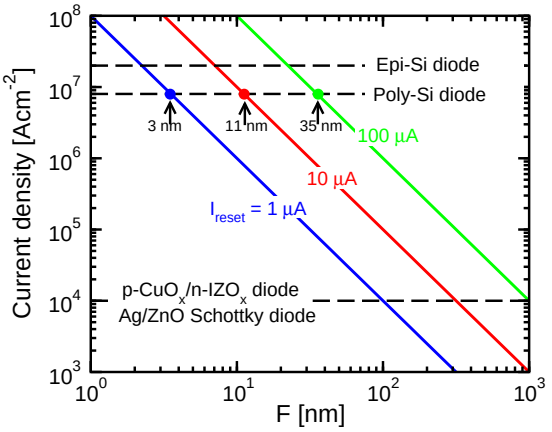

Figure 4.8: Calculated reset current density j_{fwd}=I_{reset}/F^2 as a function of technology node F, for I_{reset} 1, 10 and 100 μA. j_{fwd} values for different diode technologies are also reported [40, 100].

corrected V_{reset} is also reported in Fig. 4.7, showing a smaller increase of reset voltage for decreasing resistance. A similar increase is consistent with previous data [63, 74] and can be explained by the higher temperature needed to reset relatively large CFs [63, 64].

Achieving sub-10 μA current in reset operation is mandatory for future development of cross-bar array structures. In fact I_{reset} directly impacts the area of the select diode for a given current density j_{fwd} under forward bias [93]. The maximum value of j_{fwd} is fixed for a given diode technology, depending on physical parameters such as carrier mobility and conduction band offset between the two materials in the diode junction. Fig. 4.8 shows the calculated $j_{fwd} = I_{reset}/F^2$ as a function of technology node F, defined as the minimum feature size controlling the half pitch in the crossbar array. The current density is calculated for three values of reset current, namely I_{reset} = 1, 10 and 100 μA. The experimental j_{fwd} values for different diode technologies are also reported, including epitaxial Si p-n junction [100], poly-Si p-n junction [101], oxide hetero-junction diode [50] and Ag-ZnO Schottky diode [40]. The reference values for the forward current density were taken at a voltage of 2 V across the diode. Considering a I_{reset} of 10 μA, our prediction indicates that poly-Si-based diodes allow scaling to F = 11 nm. On the other hand, oxide-based hetero-junction diodes, which are an ideal solution for 3D-stackable cross-bar structures and back-end of line (BEOL) processing [50], cannot go below F = 50 nm due to their smaller j_{fwd}. For smaller reset current, the required diode

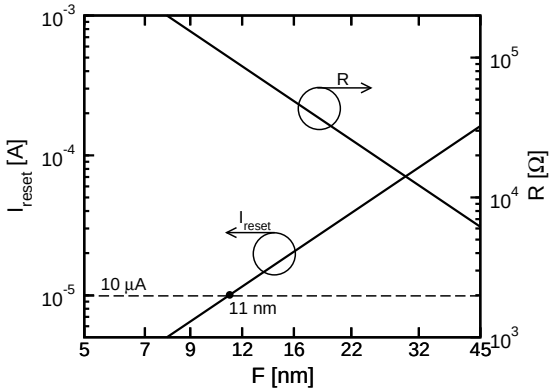

Figure 4.9: Calculated I_{reset}=$j_{fwd}F^2$ and R=V_{reset}/I_{reset} (V_{reset} is assumed 1 V) as a function of F.

area decreases, thus allowing to extend the scaling capability of crossbar memory.

Fig. 4.9 shows calculated values of I_{reset} and $R = V_{reset}/I_{reset}$, assuming V_{reset} = 1 V and a polysilicon-diode forward current density. These results indicate that for a chosen diode technology, *i.e.* a fixed j_{fwd}, I_{reset} must be continuously scaled to allow scaling to a smaller node in a cross-bar array structure. It is also clear that a low I_{reset} requires a high R in the set state. However, it should be noted that large set-state resistances limit the maximum read current, hence speed. Improving the read current may be obtained by read voltage increase, which however may lead to read disturb and even unwanted reset. Thus, extreme I_{reset} scaling may require improvement of sense amplifier circuits for efficient reading, or a tradeoff with read time. Finally, it is clear from our study that BEOL diode solutions, such as oxide-based heterojunction diodes or Schottky diodes, allow for limited scaling due to their relatively small forward current. Possible improvement of the diode current may result from material engineering in the diode structure, for instance with the aim of decreasing the conduction band offset in the heterojunction or suppressing the series resistance due to grain boundaries or interfaces. Alternatively, higher bias voltage may be used during reset, as already suggested in the case of bipolar-transistor selected phase change memory [102].

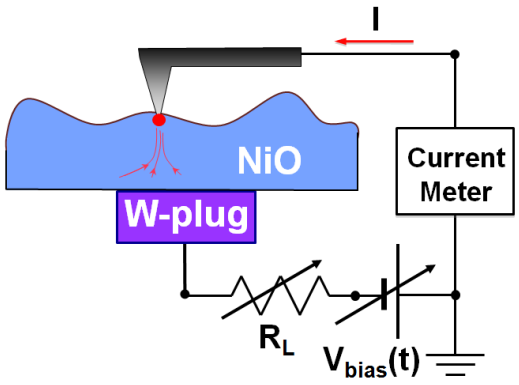

Figure 4.10: Schematic illustration of the CAFM experimental setup used in this work. A load resistance $R_L = 10$ MΩ was used to limit the maximum current during forming.

4.2 Conductive Atomic Force Microscopy

In order to access the direct manipulation of single CFs we used particular memory devices in which the active layer is not covered by the top electrode. NiO films were deposited on patterned substrate consisting of a vertical W bottom electrode (BE) with an area of 1 μm^2, surrounded by a thick (300 nm) insulating SiO_2 [103]. A polycrystalline, 15-nm thick film of NiO was deposited by atomic layer deposition (ALD) at 300°C. Details about sample preparation and film microstructure were reported elsewhere [26, 38].

Fig. 4.10 sketches the experimental setup used for CAFM measurements and enabling both topography and current mapping. For local electrical characterization, a voltage sweep was applied to the CAFM tip, while the current was measured by a Veeco Dimension 3100 with a Nanoscope V controller. Conductive tips coated with boron-doped diamond and Pt-Ir coated were used throughout this work. Only positive voltages were applied to the CAFM tip to avoid anodic oxidation of the sample surface [104].

Both forming, namely the formation of a CF by electrical breakdown in an originally high-resistivity NiO film, and reset, consisting of CF deactivation through electrically-induced diffusion and oxidation [21,26], were made possible under the same voltage tip polarity thanks to the unipolar character of switching in our NiO films [103]. A load resistance $R_L \approx 10$ MΩ was used during forming transition to limit the maximum current and avoid CF overgrowth [42, 66]. No load resistance was used

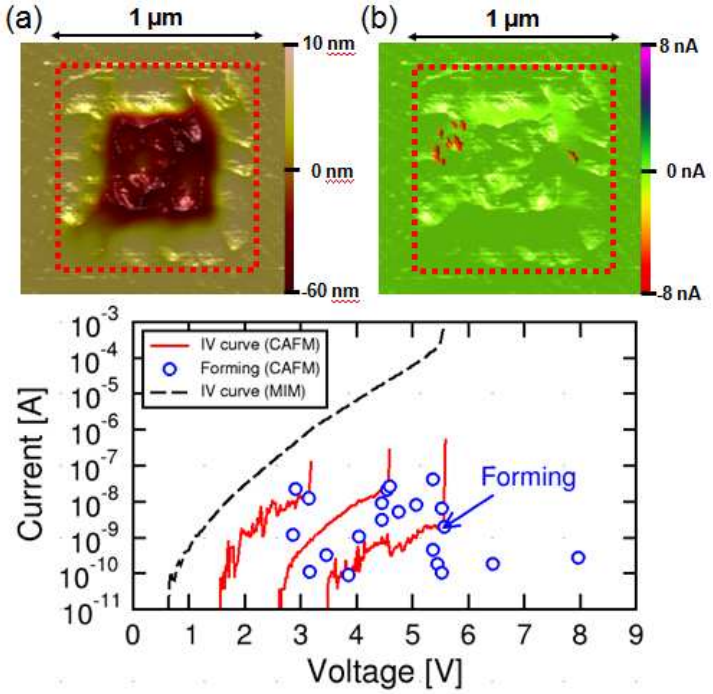

Figure 4.11: (a) Topography map obtained by CAFM scanning of the NiO surface, evidencing the enhanced roughness in the plug region due to W roughness. (b) Topography/current map after forming, showing surface topography with a light/dark scale and low/high currents as green/red colour scale. Red spots reveal electrically-formed nanoscale CFs. (c) Measured $I-V$ characteristics for CAFM forming (red lines) and scatter plot of forming points at V_{form}, I_{form} (blue circles), compared with $I-V$ characteristic of μm-scale MIM device (black dashed line).

during reset. Measurements were carried out in contact mode under atmospheric conditions.

Figs. 4.11a and b show topography and topography/current mappings, respectively, obtained from tip scanning across an area of 1.2 x 1.2 μm^2 above the W-plug region. The latter is marked as an inner square with 1 μm side in the figures. The roughness in the W-plug region is significantly higher than the surrounding area, due to the relatively rough W-plug as opposed to the flat SiO_2 layer underneath the NiO film [38]. Following the topographic scanning shown in Fig. 4.11a, CFs were formed by applying voltage sweeps on the CAFM tip positioned over randomly chosen spots within the W-plug area. Fig. 4.11b shows the current and topography maps collected after forming at some selected locations in the W-plug region: The topography shows no sig-

nificant changes with respect to the pre-forming state in Fig. 4.11a, indicating that neither the CAFM topography scanning nor the forming operations did not modify the surface topology of NiO. On the other hand, the current map reveals clear conductive spikes indicative of formed CFs, highlighted by the red marks in the figure. Three current-voltage characteristics measured during forming are shown in Fig. 4.11c as red lines. In these $I-V$ curves, the forming event appears as a step-like current increase at a voltage V_{form} and current I_{form}. The figure also shows collected V_{form} and I_{form} for several forming operations as a scatter plot. V_{form} displays a large spread between about 3 and 8 V, while I_{form} is between 10^{-10} and 10^{-7}A. The large variability of forming parameters can be understood by the localized nature of switching, thus being strongly impacted by (i) nanoscale variability in the local thickness due to the W-plug surface roughness, (ii) nanoscale variability in the chemical composition of the NiO film and (iii) defects, such as dislocations [105] and grain boundaries [105]. The latter defects may explain the most part of the variability considering the polycrystalline microstructure of our NiO films [97] and the possible segregation of Ni atoms at grain boundaries [106], thus enhancing the local tendency to switching.

To gain more insight into the amplitude and variability of V_{form} in Fig. 4.11c, CAFM data were compared with $I-V$ characteristics measured on micrometric pad-size MIM devices during forming. The MIM devices were identical to samples used for CAFM except for a 30 nm thick Pt top electrode connected with a large area (40 μm) pad, enabling electrical measurements with conventional probes with tip size of several μm. Based on data in Fig. 4.11c, the current measured by CAFM appears much smaller than the one obtained on MIM capacitor by 1 to 7 orders of magnitude, with an average around 4. From such a large variability of current ratio, it is clear that CAFM current cannot be understood only in terms of different tip/electrode areas, but is strongly influenced by localization effects due to roughness, composition variability and defects [104, 105].

The forming voltage measured on large-area MIM devices is also larger than V_{form} obtained by CAFM experiments: This result contradicts the area-scaling behavior of breakdown voltage, since V_{form} is expected to increase with decreasing area, due to the decreasing probability of finding a weak spot to initiate the breakdown process [107]. The reverse area dependence of V_{form} can be understood in terms of electric field localization in CAFM measurements, due to current crowding close to the tip electrode. Figs. 4.12a and 4.12b show the calculated maps of electric field in two MIM capacitors with different diameters of

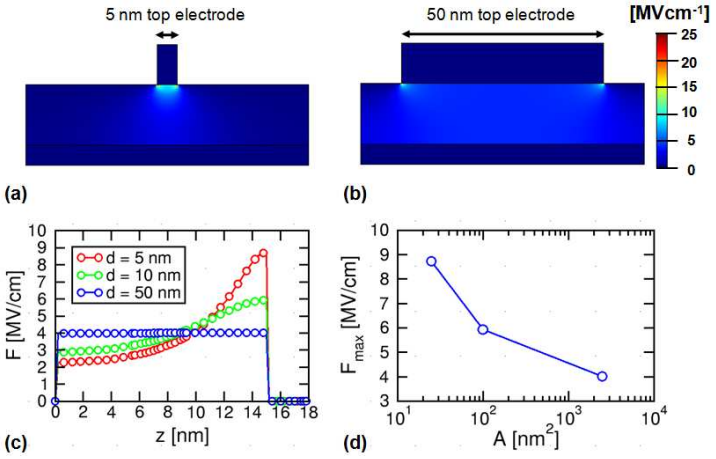

Figure 4.12: Calculated maps of electric field in MIM capacitors with different diameters of the top electrode, namely $\phi = 5$ (a) and 50 nm (b), under a bias voltage of 6 V. (c) Calculated electric field F along the revolution axis of MIM capacitors for $\phi = 5$, 10 and 50 nm diameters of top electrode and (d) calculated maximum electric field F_{max} as a function of top-electrode area.

the top electrode, namely $\phi = 5$ (a) and 50 nm (b), under an applied voltage of 6 V. The MIM structure with the smallest top electrode was used to represent the CAFM experiment with a sub-10 nm tip. A significant electric field enhancement is seen for $\phi = 5$ nm, as a result of the smaller top electrode and the consequent current crowding close to the tip. Fig. 4.12c shows the corresponding electric field F along the revolution axis of the MIM capacitor, calculated for $\phi = 5$, 10 and 50 nm. The maximum electric field increases by a factor two from $\phi =$ 50 nm to 5 nm, which can be taken as a reference for the contact area between the film surface and the CAFM tip. The field enhancement effect is summarized in Fig. 4.12d, showing the calculated maximum electric field F_{max} as a function of the top electrode area. These results indicate that field enhancement should be taken into account when comparing $I-V$ characteristics measured at the nanoscale by CAFM, since both Poole-Frenkel transport, responsible for conduction in NiO before forming [81], and dielectric breakdown, which is responsible for forming process, are field-driven phenomena. Calculations in Fig. 4.12 indicate that, assuming a CAFM tip around 5 nm in size, V_{form} voltages measured by CAFM should be multiplied by a factor of the order of 2 for a comparison with MIM data at equal electric field. This explains the non-Poissonian area scaling of forming voltage from micrometric MIM capacitors to nanoscale switching by CAFM. These results also suggest

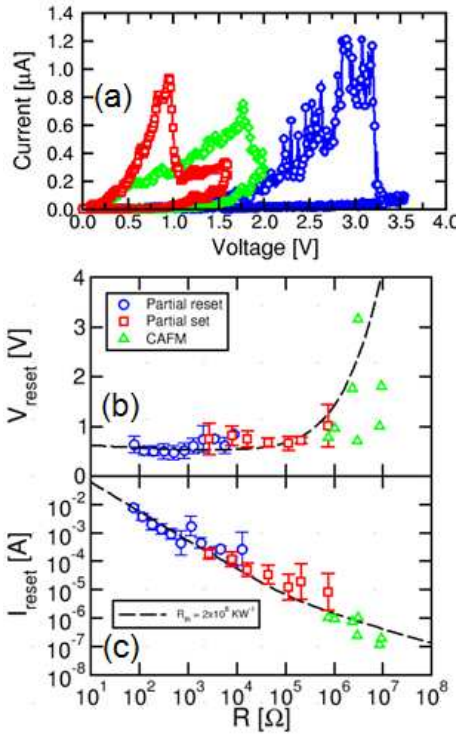

Figure 4.13: (a) $I - V$ reset characteristics measured at three different CFs. (b) Measured V_{reset} and (b) I_{reset} as a function of resistance R (green triangles). CAFM results are compared to data for μm-scale MIM devices obtained by partial reset (blue circles) and partial set (red squares) [108]. Data are in agreement with the results of analytical Joule-heating model [108].

that memory cell based on corner/tip geometries to localize the electric field [24] might be used to efficiently reduce the forming voltage.

After forming, CFs were submitted to a second voltage sweep for reset, namely disruption by thermally-induced oxidation and diffusion. No load resistance was used, since no current limitation is needed during reset. Fig. 4.13a shows $I - V$ characteristics measured on three different CFs and clearly demonstrating local reset at a variable voltage V_{reset}. Figs. 4.13b and 4.13c show measured V_{reset} and reset current I_{reset}, respectively, as a function of the initial CF resistance. Data for micrometer-size MIM capacitors are also shown in Figs. 4.13b and 4.13c, corresponding to CFs controlled by either partial reset, where CFs with different sizes are obtained after set and after reset at variable voltages, or partial set, where the maximum current during set is limited by a saturated MOS transistor in series with the cell [108]. In both cases,

V_{reset} ranges from 0.5 to 1.2 V, while I_{reset} follows an inversely-linear dependence on R according to $I_{reset} = V_{reset}$/R. With respect to MIM devices, where a maximum resistance of about 10^6 Ω could be obtained by partial set, CAFM results show relatively high resistance up to 2 x 10^7 Ω thus leading to a I_{reset} well below 1 μA. Such high resistance values cannot be explained only by the self-limiting process of CF formation due to the small available current during set [42]. In fact, the self-limited set is described by the empirical law [66, 73]

$$R = V_C/I_C \tag{4.5}$$

where R is the CF resistance after set, $V_C = 0.4$ V is the voltage across the cell at the end of the set process and I_C is the compliance current, namely the maximum current during set. Based on Eq. 4.5, we obtain a maximum CF resistance $R_{max} = R_L x V_C/(V_{max} - V_C) \approx 420$ kΩ , where $R_L = 10$ MΩ and $V_max = 10$ V is the maximum voltage during the forming sweep. The measured set-state resistance after forming is significantly larger than R_{max}: This might be explained by the CF size being limited by the top electrode during CAFM forming. It should be reminded in fact that the CF effective size is generally viewed as the size of the percolation bottleneck within a modified oxide region, where the concentration of conductive dopants (e.g. Ni excess atoms and/or O vacancies in NiO) is higher than in the pristine oxide due to the breakdown process during the forming event [65, 76]. The nanoscale CAFM tip might thus lead to a relatively-small modified area, resulting in a lower probability of finding a low resistivity percolation bridge and in an overall high CF resistance. Tip size-limitation might thus result in a degraded forming efficiency, leading to a slower kinetic of CF growth. This would translate into a relatively high V_C in Eq. 4.5, causing a relatively high R after CAFM formig with respect to usual MIM devices. For instance, assuming R = 3 MΩ as a reference CF resistance in Fig. 4.13, Eq. 4.5 yields $V_C = V_max$ R/(R+R_L) ≈ 2.3 V, thus far higher than the usual V_C values found in the literature [73]. Figs. 4.13b and 4.13c also show calculated V_{reset} and $I_{reset} = V_{reset}$/R according to an analytical Joule-heating model for diffusion and oxidation of conductive dopants in the CF region [108, 109]. The heat loss from the CF is described by two parallel thermal resistances, a CF thermal resistance R'_{th}, which is proportional to R and accounts for heat flow along the CF, and a parasitic R''_{th}, which instead models heat conduction out of the CF and through the surrounding NiO [108]. The best agreement between data and calculations in Fig. 4.13c was found for R''_{th} around 2x10^8 kW^{-1}. The large spread in measured V_{reset} may be due to the statistical variability of thermal resistances (R'_{th} and R''_{th}) and diffusion-kinetic parameters,

such as the activation energy for atomic diffusion [110]. These results support electrode area reduction as an efficient method to reduce the CF size and I_{reset} through size-dependent forming. In conclusion, electrical formation and dissolution of nanoscale filaments by CAFM has been demonstrated in NiO. The comparison of switching parameters from CAFM experiments and micrometer-size MIM capacitors allows to highlight the role of defect variability and of electric field localization due to the small CAFM contact-area in the forming operation. Reset measurements indicate unusually high CF resistance after forming, which is attributed to an effective limitation of CF size by the small CAFM tip. Reset currents below 1 μA are in line with the expected dependence on CF size, thus supporting CF area scaling as a powerful method for I_{reset} reduction scaling.

Chapter 5

Reliability and scaling

VLADIMIR: You have a message from Mr.Godot.
BOY: Yes, sir.
VLADIMIR: He won't come this evening.
BOY: No, sir.
VLADIMIR: But he'll come tomorrow.
BOY: Yes, sir.
VLADIMIR: Without fail.
BOY: Yes, sir.
[*Silence.*]

Samuel Beckett (1906-1989), WAITING FOR GODOT

In this chapter the attention will be focused on RRAM reliability issues. The feasibility of multilevel RRAM cell will be explored and the results on statistical analysis on data retention will be presented. A fundamental trade-off between reset current scaling, data retention, set-reset instabilities and RTN noise will be shown evidencing its importance for the future development of RRAM technology.

5.1 Multilevel feasibility

In Section 2.2 it has been shown the possibility to obtain intermediate resistive states between full-set and full-reset state by the application

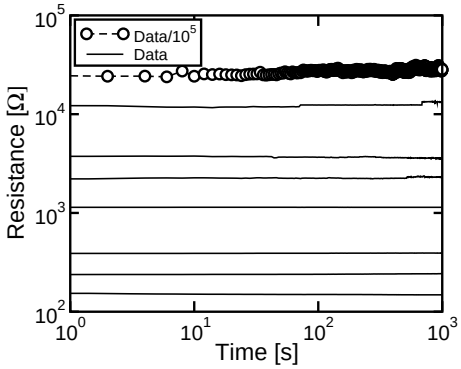

Figure 5.1: Measured R as a function of time at room temperature. Stable R is demonstrated for all MLC states between 10^2 Ω and 10^4 Ω. Data for the full reset state ($R_{reset} > 10^9$ Ω) are scaled by a factor 10^5 for clarity.

of a partial reset or a partial set algorithm. Thanks to this program algorithm it is possible to store more than one logic bit on a single RRAM device thus dramatically increasing the memory density of the entire array. Anyway an important parameter to take under control for the feasibility of a MLC is the stability over time of the program resistance, i.e. the ability of the memory element to maintain a certain resistive state. Using the MLC algorithm described above, we programmed RRAM cells in different resistance states, including set/reset states and intermediate MLC states considering in the resistive window from 10^2 Ω to 10^4 Ω. The resistance stability for these states was then studied at room temperature. Fig. 5.1 shows the measured R as a function of time for several MLC states at increasing resistance. No significant change of resistance could be found in a time scale of about 3 decades, for all states reported in the figure. Time evolution of the resistance can be fit by a power law:

$$R \propto \left(\frac{t}{t_0}\right)^{\nu}, \tag{5.1}$$

in analogy with resistance drift phenomena in amorphous semiconductors resulting from structural relaxation [111].

Fig. 5.2 shows the extracted power-law time exponent ν as a function of resistance. In the considered MLC range between 0.1 and 5 kΩ, the time exponent ν remains below 0.015. The projected increase of resistance along 17 decades of time, from a verify time of 300 ns to a data retention time of 10 years, i.e. $\approx 3\text{x}10^{10}$ s, can thus be obtained as $10^{17*0.015} \approx 1.8$, i.e only +80%. This allows closely-spaced levels, e.g. $R_1 = R_{set} = 100$ Ω, $R_2 = 300$ Ω, $R_3 = 1$ $k\Omega$ and $R_4 = R_{reset}$.

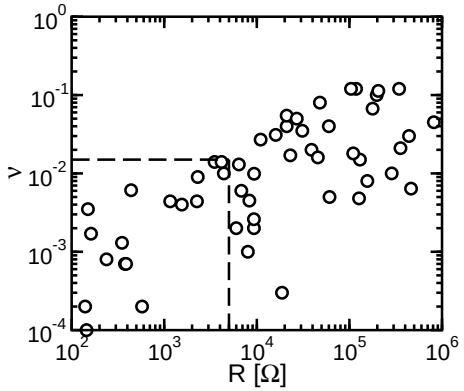

Figure 5.2: Time exponent ν as a function of the cell R. ν was obtained fitting the $R - t$ curves by the power law in Eq. 5.1.

5.2 Data retention

Although decreasing CF size results in a smaller I_{reset} [42,96,112], it also raises a concern in terms of CF stability. In fact, T-activated diffusion and oxidation of small CF can result in data loss at relatively low T/short times. This is in agreement with previous results for bipolar CuO-based RRAMs, showing that the set state obtained with relatively high current limit and displaying relatively low resistance was less sensitive to elevated-temperature bake [49]. A similar report on $Cu : MoO_x/GdO_x$ capacitors showed that the set states with high resistance were affected by a shorter retention time [113]. To assess data-loss effects for variable size of the CF, we performed high-T annealing experiments on RRAM cells. To handle the large spread of retention behavior in our samples, we performed the annealing at a fixed time and temperature on a large set of samples, usually including 50 cells programmed at approximately the same initial resistance. The resistance of the cells was measured at room temperature before and after bake, and after each bake the cells were set again and subjected to a new bake experiment for a different time and/or temperature. Sufficiently long annealing times were used in our bake experiments, to ensure that a steady-state, constant temperature throughout the annealing chamber and the samples was reached during the experiment. Fig. 5.3 shows the correlation plot of the post-bake resistance R_{pre} as a function of pre-bake resistance R_{post}, for an annealing temperature T = 280°C. The dashed line indicating $R_{pre} = R_{post}$ and corresponding to negligible effects of the annealing on resistance is also shown for reference. From the figure, one may note that

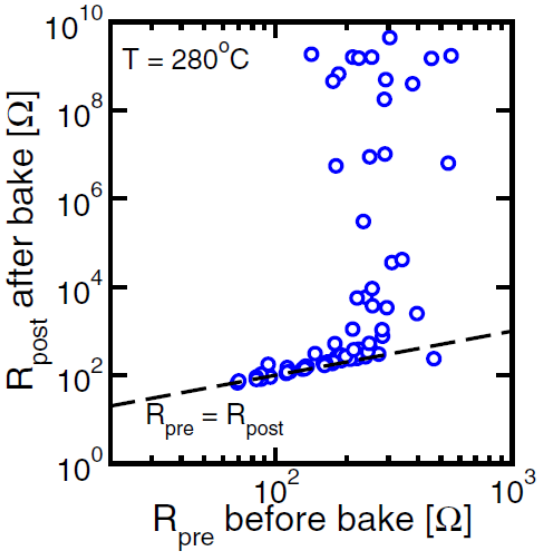

Figure 5.3: Correlation plot of R measured before (R_{pre}) and after (R_{post}) bake.

R_{post} is generally larger than R_{pre}, as a result of bake-induced oxidation and dissolution of the CF. Most importantly, cells with relatively large R are weaker against thermal reset, as indicated by the larger tendency to move to a high R_{post}. This demonstrates the size-dependent data loss effects in our samples, thus posing a reliability issue for scaled RRAMs with small CF.

Fig. 5.4 shows cumulative distributions of measured R before annealing (initial) and after bake experiments for increasing annealing times at 300°C. Cells were programmed at an initial R between 0.2 and 1 kΩ. Annealing results in a shift to higher resistance, usually close to the reset state. This indicates a sharp transition between the set and reset state, also consistent with the generally small voltage range where the reset transition takes place on the $I-V$ curve. The amount of cells belonging to the moving tail increases for increasing time. This behavior is similar to the previously observed data-loss process in phase change memories, and can be explained by the relatively large retention time distribution and by the sharp transition from set to reset state as the CF is thermally dissolved [114]. From the cumulative distributions in Fig. 5.4, the average evolution of resistance with time can be obtained, similarly to the established procedure in Flash memories [115]. The cumulative distributions were analyzed at a constant percentile f (e.g. see the horizontal line corresponding to f = 90% in Fig. 5.4). In cor-

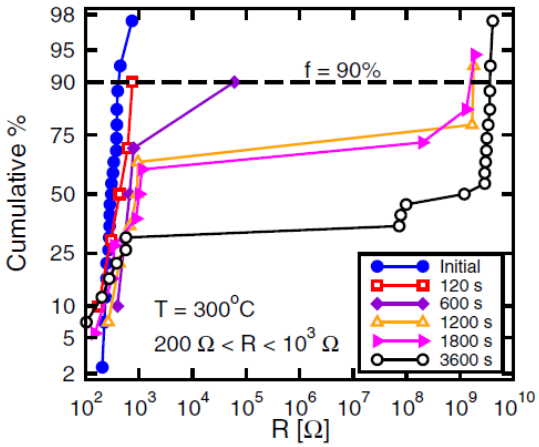

Figure 5.4: Cumulative distributions of R for increasing annealing times at 300°C, starting from a set state resistance between 0.2 and 1 $k\Omega$.

respondence of the intersections between the cumulative distributions and the horizontal line at constant f, resistances values were extracted and plotted as a function of the corresponding annealing time. Fig. 5.5 shows the resulting R as a function of time for increasing percentile f = 25, 50, 75 and 90%, obtained from the cumulative distributions in Fig. 5.4. The results indicate relatively abrupt transitions from the set to the reset state, where the transition time increases for decreasing f. This is clearly the consequence of the ordering procedure inherent to the cumulative distribution plot. Note in particular that no resistance transition could be detected for f = 25% within the experimental time range considered.

From Fig. 5.5, one can define a retention time τ_R as the time for a 10x increase of R (10 kΩ in the figure). Fig. 5.6b shows the Arrhenius plot of retention times τ_R at variable f from 25% to 90%. The measured retention time τ_R obeys an Arrhenius law with an activation energy for retention E_{AR} = 1.21 eV for f = 50%, in good agreement with previous results (1.4 eV) of voltage-driven reset studies [47]. Extrapolation indicates a 10-years-retention T of 110°C for f = 50%. However, τ_R decreases at low f, confirming that statistical studies are mandatory for RRAM reliability assessments. From a careful inspection of the figure, one may notice that more data points are available at large f as compared to small f: This is due to the already mentioned shift of τ_R to longer times for decreasing f, hence away from the statistical tail of moving cells. Longer experimental time would obviously result in more point

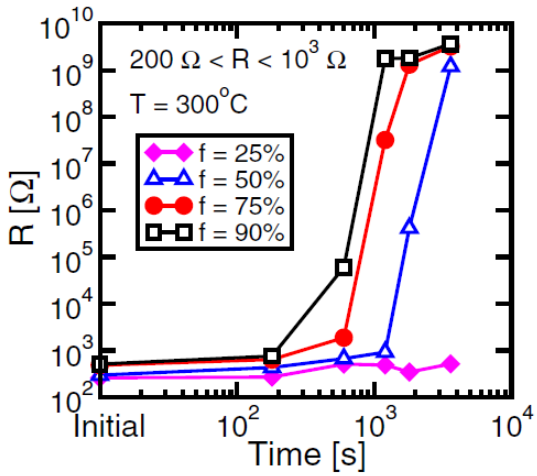

Figure 5.5: Time evolution at constant percentile f, from Fig. 5.4.

for τ_R at smaller percentiles.

Fig. 5.6b shows the Arrhenius plots for three different ranges of R at f = 90%. Data show that τ_R decreases for increasing R, hence decreasing CF size, at a given temperature. Although τ_R is reported for f = 90%, similar results may be expected for smaller f, e.g. 50%, due to the similar behavior at different f in the Arrhenius plot of Fig. [**?**]a. The results in Fig. 5.6b demonstrate that smaller CFs result in a shorter τ_R. The extracted activation energy E_{AR} in the figure is between 0.64 and 1 eV, with no clear dependence on initial resistance. Note however that the extracted E_{AR} may be affected by a measurement spread due to the variability of data loss in memory cells. More data along an extensive temperature range are needed for a better and more reliable evaluation of the activation energy as a function of the cell resistance.

5.3 Retention-reset tradeoff

To explain the size dependence of reliability, we modeled data loss assuming that CF oxidation is limited by a diffusion of metallic atoms from the CF [62]. According to this model, nickel atoms diffuse from the Ni-rich CF toward the surrounding stoichiometric or oxygen-rich film, where Ni gets oxidized. The diffusion of metallic species was simulated by a 3-D finite-difference model for increasing initial CF size, and τ_R was evaluated as the time for a decrease of the metallic concentration by a factor of 10 or 100. Fig. 5.7a shows the calculated τ_R as a func-

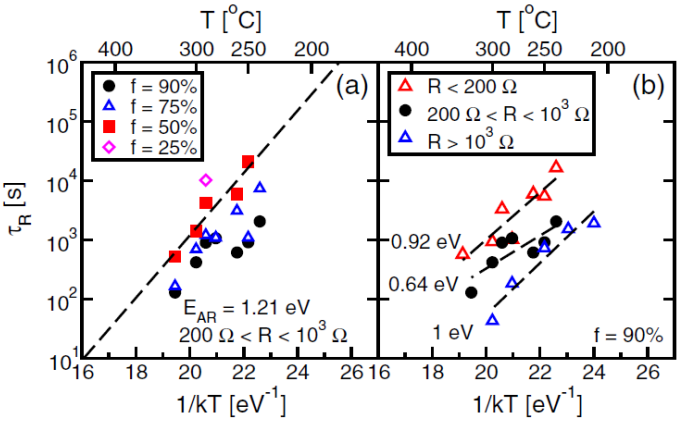

Figure 5.6: (a) Arrhenius plot of the measured R for different percentiles, namely, f = 25%, 50%, 75%, and 90%, within a fixed resistance range 0.2 < R < 1 kΩ and (b) Arrhenius plot of measured τ_R for three different resistance ranges, namely, R < 0.2 kΩ, 0.2 < R < 1 kΩ, and R > 1 kΩ, at f = 90%. The retention time was extracted by the method shown in Fig. 5.5. The temperature in the x-axis represents the bake temperature in the annealing experiments.

tion of ϕ, showing that the retention time increases as ϕ^2. From these results, we can describe both the temperature dependence (Arrhenius model) and the ϕ^2 geometry dependence by

$$\tau_R = \tau_{r0} \left(\frac{\phi}{\phi_0} \right)^2 e^{\left(\frac{E_{AR}}{kT} \right)}, \tag{5.2}$$

where τ_R and ϕ_0 are constants. The Meyer-Neldel effect, i.e., the τ_{R0} dependence on E_{AR} [116], was not considered for simplicity. Fig. 5.7b shows the experimental τ_R at 250°C [from interpolation of data in Fig. 5.6b] and calculation results by 5.2. In these calculations, we used the extracted ϕ from Fig. [**?**]b and parameter values E_{AR} = 1 eV, τ_{R0} = 1.4 x 10^7 s, and ϕ_0 = 5 nm. Calculations agree very well with data, supporting our physical interpretation of the data-loss process. Extrapolations at 85°C are also shown in comparison with the ten-year criterion for nonvolatile storage.

These results suggest that the CF size ϕ should be maximized (i.e., R minimized) for best data retention. This, however, impacts programming, since a smaller resistance results in a larger reset current [112]. To solve this intrinsic tradeoff between reset and data retention, physics based material engineering to improve E_{AR} could be a viable solution. For instance, replacing or alloying Ni with metallic elements with a

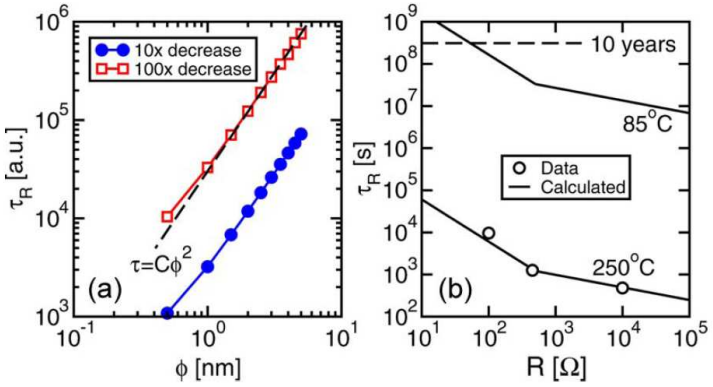

Figure 5.7: (a) Calculated retention time as a function of CF diameter from reaction.diffusion simulations and (b) measured and calculated τ_R as a function of programmed resistance. Experimental values are taken from interpolations in Fig. 5.6b. Calculations are shown for annealing temperatures T = 250°C (same as reported data) and 85°C for reliability assessment of RRAM.

higher activation energy for diffusion in NiO might improve the data retention at low T while preserving the necessary fast reset at high T.

5.4 Pulsed operated set-reset instability

Pulsed operated set/reset experiments were conducted on the structure shown in Fig. 5.8a The RRAM element (Fig. 5.8b) is a MIM device with a 25 nm-thick NiO layer sandwiched between a Pt top electrode and a W-plug bottom electrode with diameter from 0.18 to 1 μm [26] like the one used in Section 4.1. The MOSFET had W/L = 10 μm /1 μm and gain G = dI_D/dV_G = 650 μA/V (Fig. 5.8c). The RRAM and MOSFET chips were carefully wire-bonded by Au wires to minimize parasitic capacitance and resistance (see Section 2.1).

Fig. 5.9a shows the measured $I-V$ curves under DC operation. The set transition from high to low resistance R is carried out under a relatively low V_G, yielding a maximum MOSFET current I_D = 3 μA. The resulting set state has R $\approx$ 370 kΩ and a relatively low reset current I_{reset} = 6 μA. The small I_{reset} is obtained thanks to the small size of the CF, which results from a low I_D during set. To calculate the minimum cell size corresponding to such a low I_{reset}, we refer to calculations in Fig. 5.9b. Here, the maximum I_{reset} is shown as a function of F, assuming that the individual RRAM cell in the crossbar array is selected by a polysilicon diode with a maximum current density of $J_{fwd} = 8MAcm^{-2}$

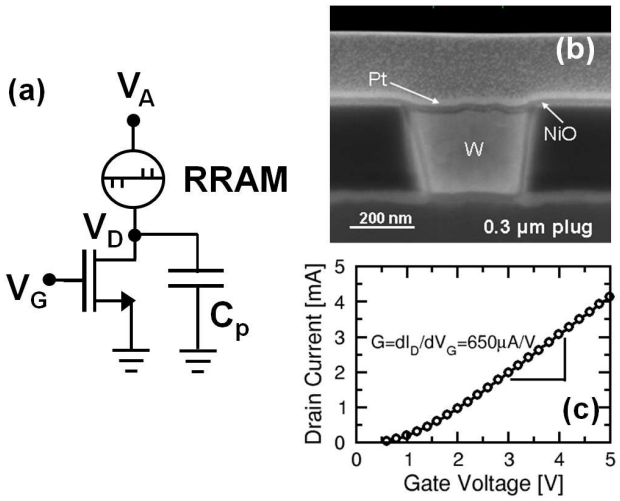

Figure 5.8: Schematic for the 1T1R structure used in this work (a), cross section of a RRAM element used in 1T1R structures (b) and measured $I_D - V_G$ characteristic for the MOSFET used in 1T1R structures (c).

at 2 V [101]. The reset current as a function of the cell size is obtained as $I_{reset} = J_{fwd}F^2$, assuming a square shape of the cell and select diode and a voltage drop of 2 V across the diode during reset. A low I_{reset} of 6 μA would thus results in a minimum feature size F of approximately 9 nm. However, it is known that the reset voltage and current increase in the pulsed operation regime of RRAM, due to the thermo-chemical nature of the reset transition [47].

The reduction of I_{reset} and the scaling projection through Fig. 5.9b thus require that the reset current is evaluated under a pulsed operation. To study the reduction of I_{reset} under pulsed reset operation, we prepared the cell in a set state with a relatively high R corresponding to a narrow CF through the NiO film [42, 43]. Set was performed by the application of a DC voltage sweep across the 1T1R while biasing the MOSFET to low V_G, hence low I_D. Fig. 5.10a shows the RRAM resistance R measured after set as a function of I_D. Two different set behaviors are highlighted: Cells A follow the usual law $R = V_0 I_D^{-1}$ with $V_0 = 0.4$ V, which can be explained by the common dependence of R and I_D on CF area A_{CF}, namely $R \propto A_{CF}^{-1} \propto I_D^{-1}$ [117]. On the other hand, cells B display a constant low $R < 1k\Omega$, irrespective of I_D.

To understand the lack of resistance control in cells B, Fig. 5.10b compares the set characteristics of cells A and B of Fig. 5.10a. In the figure, the current is shown as a function of the overall voltage across

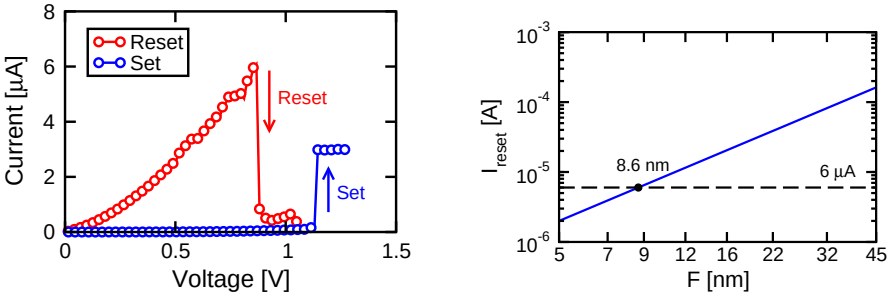

Figure 5.9: Measured (a) DC set/reset characteristics obtained with the 1T1R structure in Fig 5.8a.Calculated (b) $I_{reset} = J_{fwd} * F^2$, that is the reset current that can be supplied by a polysilicon diode selector, as a function of F. $J_{fwd} = 8MAcm^{-2}$ of a poly-Si diode [101] was assumed.

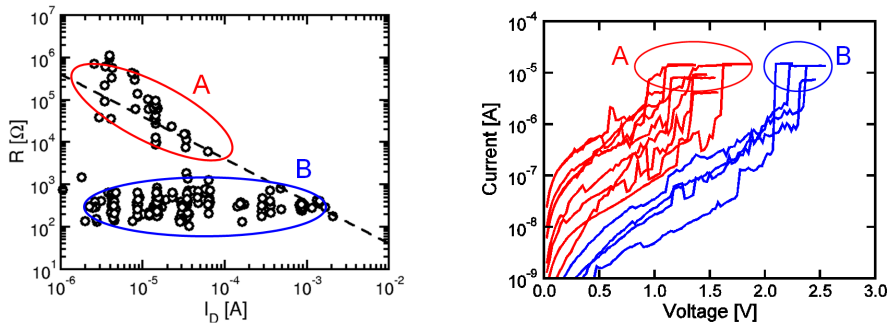

Figure 5.10: Measured R (a) as a function of I_D supplied by the MOSFET during set. Data show two different set regimes, namely A and B. The theoretical behavior $R = V_0 I_D^{-1}$ with $V_0 \approx 0.4$ V is also shown. Measured $I - V$ characteristics (b) for cells A and B in (a). Group B displays higher reset-state resistance and larger V_{set}, leading to a current overshoot and a low set R in (b).

the 1T1R, where the compliance current of about 12 μA corresponds to the I_D of the saturated MOSFET. Cells A have a relatively low reset-state resistance and a low set voltage V_{set}. On the other hand, cells B evidence a relatively high reset-state resistance (R > 100 MΩ) and a high set voltage $V_{set} > 2$ V. The high V_{set} for high reset-state resistance can be understood by the threshold switching model for set transition, where the threshold switching voltage increases with R due to the increasing activation energy for conduction [108].

The high V_{set} of cells B can lead to a current overshoot during the set transition, due to the finite parasitic capacitance C_p in the wire-bonded 1T1R structure in Fig. 5.8a [41, 42, 46, 78]. To explain the current overshoot effect, Fig. 5.11 show the calculated voltage across the cell (a), cell current (b) and local temperature T (c) during set,

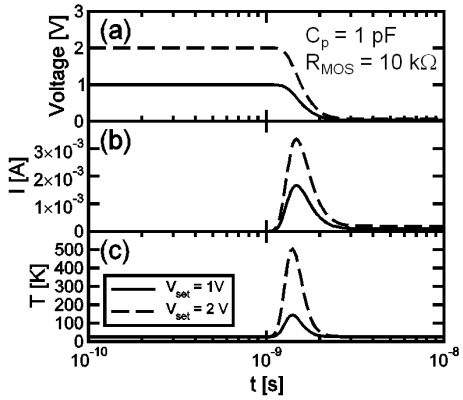

Figure 5.11: Calculated voltage (a), current (b) and CF temperature (c) as a function of time during set at $V_{set} = 1$ and 2 V, qualitatively describing the behaviors A and B, respectively, in Figs. 5.10a and 5.10b

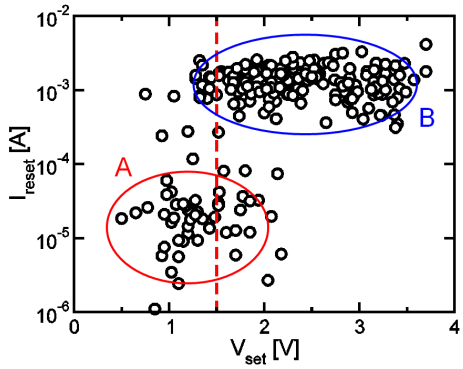

Figure 5.12: Correlation plot of measured I_{reset} and V_{set} for cells A and B in Fig. 5.10a. Small V_{set} ¡ 1.5 V ensures ideal CF size control through minimum overshoot effects.

assuming a set switching time of 0.5 ns [46] and a parasitic capacitance of 1 pF. Both the current and the local temperature displays overshoots at the switching time, which may be critical for high V_{set} due to the sudden transition to the low-R state. The overshoot effect can cause uncontrolled set with low set state R [42, 78].

To minimize overshoot effects, V_{set} should be kept below 1.5 V as shown by the correlation between I_{reset} and V_{set} in Fig. 5.12. These results demonstrate the need for a controlled reset to ensure low V_{set}, thus minimizing overshoot effects during set. Cells A showing controlled set with a relatively high R were then subjected to a reset operation to

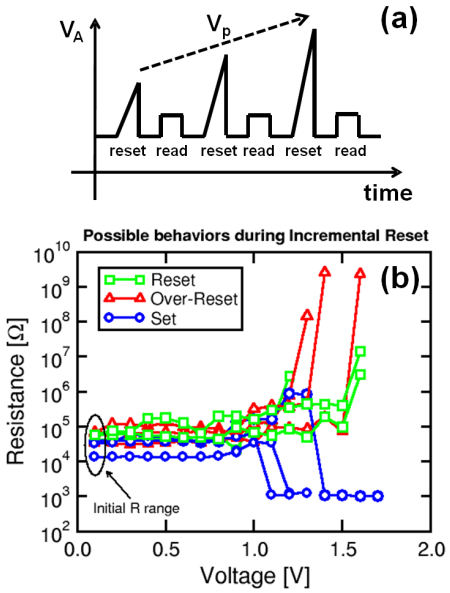

Figure 5.13: Schematic for the incremental reset (IR) pulsed operation (a) and measured R during IR cycles as a function of V_p for $t_s = 10^{-5}$ s (b). Reset, over-reset and set behaviors are shown.

study the minimum reset current in the pulsed regime. Only cells with a relatively large initial resistance between 10^4 and 10^5 Ω were selected, corresponding to a I_{reset} approximately between 4 and 40 μA in the DC regime [117].

To reset the cells, we used the incremental reset (IR) algorithm proposed in Fig. 5.13a. This consists of a sequence of triangular pulses with fixed time ts and increasing amplitude V_p. Three pulse-widths were used, namely ts = 10^{-1}, 10^{-5} and 2x10^{-7} s. The reset pulse was applied with gate voltage $V_G = 5$ V, corresponding to a MOSFET series resistance $R_{MOS} = 0.5$ kΩ. After each reset pulse, the cell resistance was read, until a state with R$\geq 10^6\Omega$ was achieved. IR allows to carefully control the reset process to avoid overshoot-induced B-type cells in Fig. 5.10a [118]. Fig. 5.13b shows the measured R after repeated IR cycles as a function of V_p, for $t_s = 10^{-5}$ s. Cells display three different behaviors, namely (a) reset to R $\approx 10^6\Omega$, (b) over-reset to R $\gg 10^6$ Ω, and (c) set to about 10^3 Ω.

Fig. 5.14 shows the $I - V$ curves for $t_s = 10^{-5}$ s, measured during the final reset cycle in the IR scheme by an active probe at the drain of the select transistor in Fig. 5.8a: Reset (a) shows a direct transition to

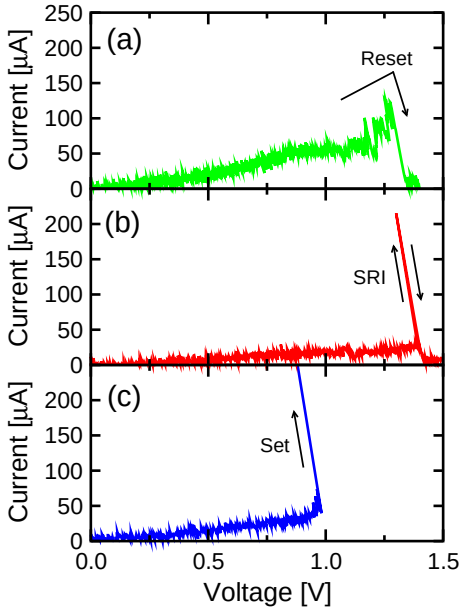

Figure 5.14: Experimental I-V curves extracted probing electrical potential V_D in Fig. 5.8a. The cell voltage was obtained as V = $V_A V_D$, while the cell current was calculated by I = V_D/R_{MOS}. Reset (a), SRI-induced over-reset (b) and set (c) for $t_s = 10^{-5}$ s are shown

R just above 10^6 Ω at low I_{reset}, while over-reset (b) displays a set-reset instability (SRI), that is a set transition to low R followed by a reset transition to a reset state with R $\gg 10^6$ Ω. Finally, set transition not followed by reset is shown in (c). SRI and set can be explained by the competition between reset and set phenomena in small, semiconductor-like CFs with relatively large R. For increasing R, in fact, CF may have disordered shape and doping, where electric-field localization result in threshold switching which triggers the set transition [46, 108]. On the other hand, low-R CFs with homogeneous metallic conductivity may limit field non-uniformity and favor Joule-heating-induced reset.

SRI and set transitions can be serious reliability issues: In fact, SRI in a crossbar array can lead to over-set failure, where the excessive I_{reset} after set cannot be supplied by the scaled select diode (see Fig. 5.9b), thus leaving the cell in an unrecoverable low-R set state. Fig. 5.15a shows the measured probabilities for having one of the three different transitions (a-b-c) in Fig. 5.14 as a function of ts: Reset probability decreases for decreasing ts, thus making fast, controlled and low-current reset increasingly difficult. Fig. 5.15b confirms that V_{reset} increases for

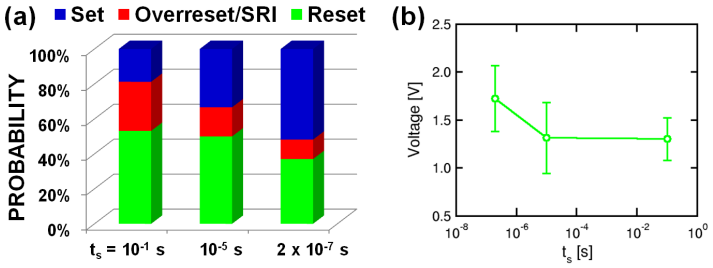

Figure 5.15: Probabilities for set, SRI-induced over-reset and reset as a function of t_s (a) and measured V_{reset} as a function of t_s (b).

decreasing ts. Given the results in Fig. 5.15, stable and low-current reset may be possible at relatively long ts [44].

5.5 RTN Model

We observed *Random Telegraph Signal Noise* (RTN) in RRAM devices affecting states with high resistance. The reported measurements were performed on devices that consist of MIM structure, with W as BE, Pt as TE, and NiO insulator. The BE area was about 0.04 μ m^2, and the NiO film was deposited by atomic layer deposition (ALD) with a thickness t_{NiO} of 20 nm. These devices show a low resistance state of about 10^2 Ω and a high resistance state of about 10^8 Ω. Intermediate states, with resistance between the set and reset values correspond to different CF sizes and were obtained by the electrical algorithm, i. e. partial reset, described in the Section 2.2, starting from a full set state and increasing gradually the resistance up to the desired state.

As can be seen in Fig. 5.16, intermediate states (10^2 Ω < R < 10^7 Ω) display a characteristic two-level random fluctuation of current with time. The figure reports the measured resistance R=V/ I as a function of V, where I is the measured current under a voltage V across the cell. Several resistance states are shown in the figure, from $R = 3$ $k\Omega$ to about 3 $M\Omega$. The resistance clearly displays a fluctuation between two levels, with a difference $\Delta R = R - R'$ between the high level R and the low level R'. The relative resistance change $\Delta R/R$ increases with R from about 2×10^{-3} for metallic CFs to about 0.5 for semiconductor-like conduction. RTN below $\Delta R/R = 10^{-3}$ could not be detected due to limitations in our setup. We developed a model for resistance-dependent RTN in intermediate states, as schematically shown in Fig. 5.17.

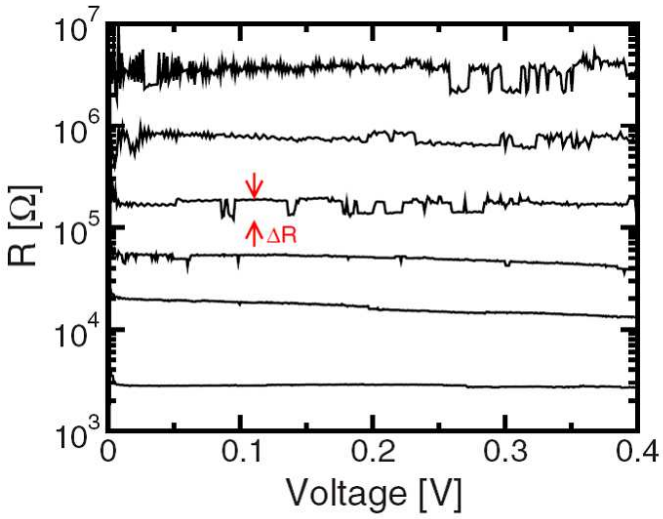

Figure 5.16: Measured resistance as a function of applied voltage, for different states with increasing programmed resistance. RTN characterized by a difference ΔR between two metastable states is shown.

The model assumes a cylindrical CF with diameter ϕ, area $A = \pi\phi^2/4$ and length equal to the NiO thickness t_{NiO}. In the model, ΔR is due to a change in the effective CF area and resistivity , induced by a fluctuating defect with variable charge (e.g., negative or neutral) close to the CF surface. The defect could be an oxygen ion or oxygen vacancy fluctuating between two equal-energy states, or a trap responsible for carrier capture/emission at the surrounding dielectric close to the CF surface. The latter model is generally applied to account for RTN fluctuations in MOSFET channels [119] and nanowires. The fraction of the effective area where conduction is affected by the bistable charged defect depends on the nature of the CF. In the case of metallic conduction, the defect charge may be efficiently screened by free carriers [Fig. 5.18(a)], whereas a longer interaction range in expected for semiconductor-like CFs [Fig. 5.18(b)].

To estimate the affected area in the CF cross section, we use the Debye length λ_D given by

$$\lambda_D = \sqrt{\frac{\epsilon kT}{q^2 n}}, \tag{5.3}$$

where ϵ is the static dielectric constant, k is the Boltzmann constant, T is the temperature, q is the electron charge, and n is the free carrier

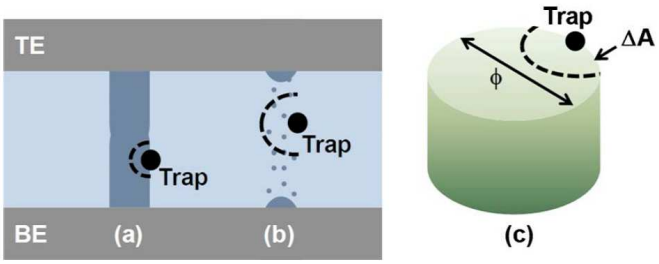

Figure 5.17: Schematic for the resistance change induced by a metastable defect at the CF surface. Metallic (a) and semiconductor-like (b) CFs are subjected to different interaction cross sections, as a result of the different screening length. The unscreened area ΔA affected by the fluctuating defect and the CF diameter are shown in (c).

concentration. The latter can be estimated as the density of carriers contributing to the electric current, i.e., carriers which are thermally excited from the Fermi level to the nearest band edge, namely [120]:

$$n = n_0 e^{-E_{AC}/kT}, \tag{5.4}$$

where n_0 is the effective density of states at the relevant mobility band edge. From λ_D, the interaction area affected by the metastable defect is obtained as the area of the intersection between the CF section and the sphere with radius λ_D, as shown in Fig. 5.17c. This was estimated as the half circle with area $\Delta A = \pi\lambda_D^2/2$, which is a good approximation for $\lambda_D \ll \phi$ and was found to never exceed an error of 40% in ΔR. To compute the resistance change, we refer to a CF sector of length u_{CF}, where the defect charge affects conduction. The low resistance R', corresponding to neutral defect state, is given by $\rho u_{CF}/A$. The high resistance R, corresponding to negatively charged defect, can be estimated as the parallel of a screened (unaffected) resistance R_s and an unscreened resistance R_u, given by

$$\begin{aligned} R_S &= \frac{\rho u_{CF}}{A - \Delta A} \\ R_u &= \frac{\alpha \rho u_{CF}}{\Delta A} \end{aligned} \tag{5.5}$$

respectively, where α is a factor describing the resistivity increase due to the electrostatic repulsion ($\alpha > 1$). Note that Eq. 5.5 holds only for $\Delta A < A$ (partial screening). For $\Delta A > A$ (no screening), R is given by R_u in Eq. 5.5, replacing ΔA by A. Neglecting the series resistance outside the CF block of thickness u_{CF}, the relative resistance change is

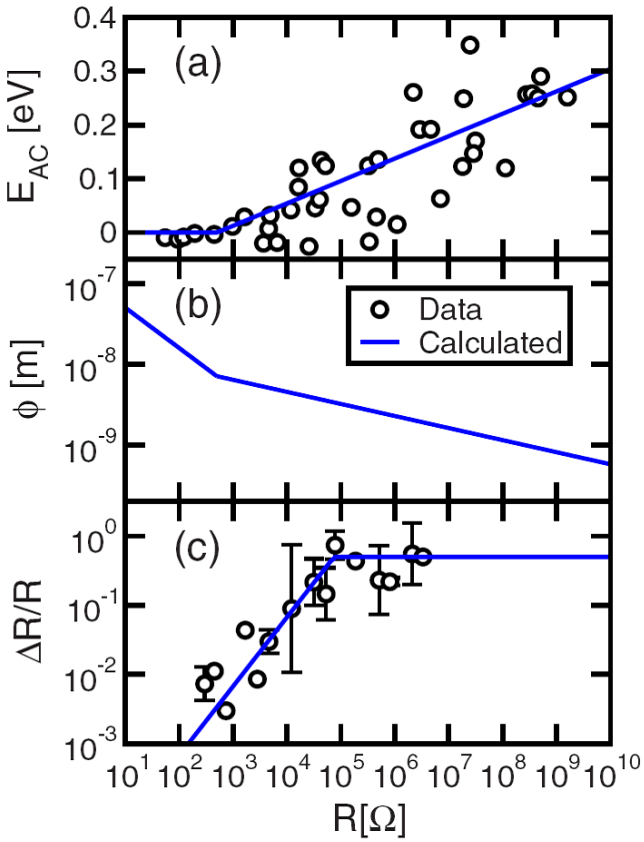

Figure 5.18: Measured activation energy for conduction E_{AC} (a), extracted CF diameter ϕ (b) and measured and calculated relative change of resistance by RTN (c). The CF diameter is extracted by Eq. 5.7, where the piecewise linear regression of E_{AC} in (a) was used. Calculations in (c) are based on Eq. 5.6.

thus given by

$$\frac{\Delta R}{R} = \frac{R - R'}{R} = \frac{\Delta A}{A}\left(1 - \frac{1}{\alpha}\right), \tag{5.6}$$

which, for no screening, yields the special case $\Delta R/R = 1 - 1/\alpha$. The increase in the relative RTN amplitude with resistance can thus be understood by the increasing unscreened area ΔA and by the decreasing A in Eq.5.6.

To use the model in Eq. 5.6, we evaluated the CF area from the measured resistance as reported in Section 2.3. As already explained,

the resistance can be expressed by the Arrhenius law as following

$$R = \rho \frac{t_{NiO}}{A} = \rho_0 \frac{4 t_{NiO}}{\pi \phi^2 e^{E_{AC}/kT}}, \tag{5.7}$$

where ρ_0 is the pre-exponential factor for resistivity. The Meyer-Neldel effect, i.e., the ρ_0 dependence on E_{AC}, was not taken into account in Eq. 5.7 [121]. To extract ϕ from Eq. 5.7, we used a piecewise-linear regression law for E_{AC}, shown in Fig. 5.18a, where E_{AC} increases linearly with $\log R$ in the semiconductor regime, while $E_{AC} = 0$ in the metal CF regime. As an estimate for the pre-exponential factor ρ_0, we assumed $\rho_0 = 100$ $\mu\Omega$cm, which roughly corresponds to the average between reported values for metallic Ni nanowires in the literature. A resistivity of 31 $\mu\Omega$cm was found for large Ni nanowire (ϕ between 50 and 100 nm [122]), while a larger value of 250 $\mu\Omega$cm was found for small Ni nanowires (ϕ between 12 and 16 nm [123]).

Fig.5.18b shows the extracted CF diameter ϕ as a function of R. The two different slopes correspond to metallic and semiconductor CF regimes in Fig. 5.18a. The CF diameter decreases for increasing R by only a factor 20 despite the huge resistance window from 10^2 to $10^8\Omega$. Similar to phase-change materials, the large resistance window is mostly due to a change in from metallic drift conduction to thermally activated hopping in the semiconductor state [120].

Fig. 5.18c shows the measured $\Delta R/R$ as a function of R, and calculations from Eq. 5.5. The CF area was computed from ϕ in Fig. 5.18b, and using a resistivity increase by a factor $\alpha = 2$, a density of states $n_0 = 10^{20}$ cm^{-3} at the mobility edge and $\epsilon = 12\epsilon_0$ (Ref. [124]). The different slopes of $\Delta R/R$ below and above 10^5 Ω correspond to partial and no screening regimes, respectively, in good agreement with the experimental behavior. The slope of $\Delta R/R$ does not change instead at the transition between metallic and semiconductor regimes at R = 0.5 $k\Omega$. This is because both λ_D and ϕ scale with $e^{E_{AC}/2kT}$, according to Eqs. 5.3, 5.4 and 5.7, respectively. Due to the proportionality of $\Delta R/R$ to $(\lambda_D/\phi)^2$ in Eq. 5.6, the dependence on E_{AC} cancels out, and $\Delta R/R$ maintains a proportionality to R in both resistance ranges despite the different trends of E_{AC}.

Note that our explanation, based on a change of geometry and resistivity in the CF, may represent an oversimplification for semiconductor (high R) case, where the local fluctuating charge may cause a more radical redistribution of hopping current in the CF. For instance, the reduction in resistivity along the main CF may cause the current to flow through an alternative hopping path with lower resistance [125]. This also includes the case of a fluctuating defect (e.g., oxygen ion or va-

cancy) affecting the percolation path of the hopping conduction, similar to previous explanations of post-breakdown gate current noise in silicon dioxide [126]. The parameter α should thus be viewed as an effective correction factor describing both current modulation and redistribution. Another significant simplification in the model consists in the rough distinction between screened and unscreened areas in the CF cross section, whereas a gradual screening effect would instead be more realistic.

Chapter 6

Metal-oxide nanowires crossbar memory

The imagination of nature is far,
far greater than the imagination of man.

Richard Feynman (1918-1965)

In this last chapter an innovative memory structure will be presented, that exploits the so-called bottom-up approach. Nickel nanowires have been synthesized and magnetically assembled. Oxidation of the nanowires cause the growth of a thin NiO shell wrapped around the nickel core. Crossbar structures were then assembled. Each cross point has still a MIM structure, and potentially works as a planar cell. Here we demonstrate the feasibility of this device and characterize the switching behaviour of the junction.

To date, RRAM devices have mostly been developed by a top-down approach, in which the active oxide layer is sandwiched between two metal electrodes defined by lithography or nanoimprint techniques [127, 128]. However, a bottom-up approach based on the synthesis and assembly of functional nanoparticles, such as nanowires (NWs) and nanodots, may provide a valuable tool to fabricate relatively complex architectures with unprecedented miniaturization, approaching the 10-nm scale [129]. Previous studies have demonstrated self-assembly of func-

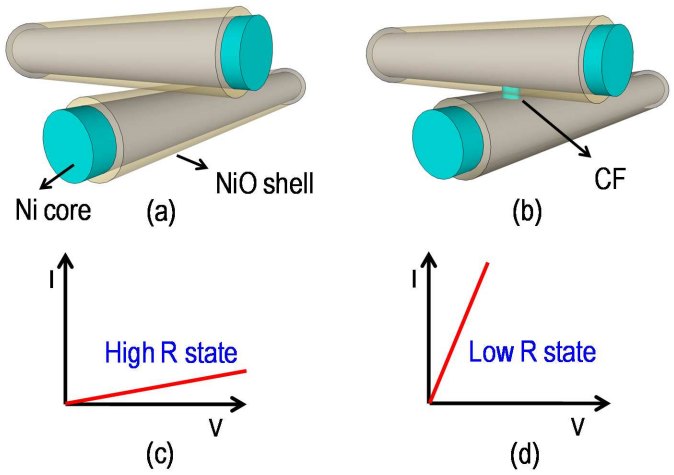

Figure 6.1: Schematic illustration of the crossbar memory structure formed from two NiO-Ni core-shell NWs, in high- (a) and low-resistance states (b), differing by the presence of a CF, and the consequent IV curves (c,d). Ni cores act as wordline/bitline interconnects, while the NiO shell is the active switching layer.

tional active NWs for address decoders [129], logic gates [130] and memory devices [131, 132]. In particular, resistance switching was demonstrated at the junction between a Si NW with an amorphous Si shell and an Ag electrode, which acted as an ion reservoir for field-induced formation of a CF across the quasi-insulating NWshell [132]. In a similar approach, resistance switching was demonstrated in ultradense crossbar arrays of carbon nanotubes (CNTs) with a thin amorphous carbon interlayer between perpendicular CNTs. NiO NWs bridging two electrical contacts were shown to repeatedly switch between two electrical states [133, 134]. A key challenge is the development of fully bottom-up crossbar arrays, in which memory elements are located at the crossing of perpendicular metallic lines [135, 136]. The demonstration of resistance switching in crossbar junctions of two functional NWs may be a key step toward the development of high-density bottom-up RRAM crossbar arrays.

6.1 Fabrication

We studied resistance switching in coreshell NWs for crossbar RRAM arrays. Fig. 6.1a shows the memory concept, which consists of a crossbar junction between two coreshell NWs, with an Ni core and an NiO shell. The Ni core serves as the metallic interconnect, while the NiO shell

plays the role of the active switching layer. In a perpendicular crossbar structure of the two metal-oxide coreshell NWs, metallic CFs can be formed through the insulator shells in response to the application of voltage pulses (Fig. 6.1b). High- and low-resistance binary states thus correspond to the presence of a continuous or broken CF, respectively (Fig.6.1c and d) [22].

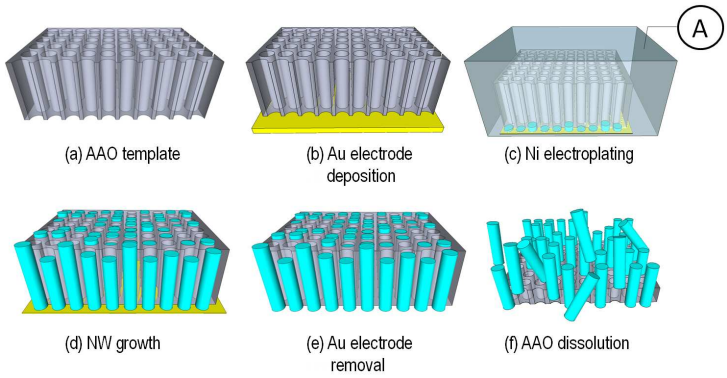

Figure 6.2: Schematic illustration of Ni NW synthesis. An AAO template (a) was first coated on one side with sputtered Au (b), then used as a cathode in an electroplating chamber (c) for Ni NW growth within the pores (d). After growth completion, the Au electrode was first removed by etching (e) then the AAO was dissolved in $NaOH$ (f), which left free-standing Ni NWs in solution.

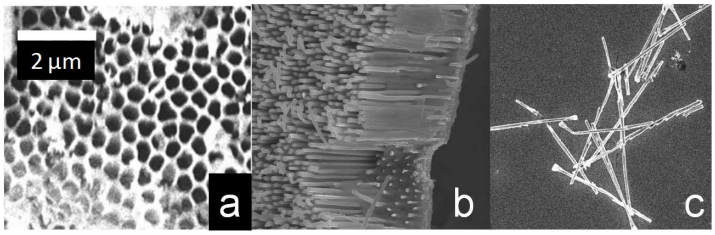

Figure 6.3: Top view of the AAO template (a), of Ni NW after growth and before AAO dissolution (b), and NWs after AAO dissolution (c).

The NWs used in the crossbar structure were fabricated using an electrochemical procedure, as described in Fig. 6.2. NWs were grown by electrochemical synthesis in an anodized aluminum oxide (AAO) template with self-assembled nanopores of controllable size (N = 200 nm in our samples, see Fig. 6.3a) [137]. An Au film of 50 nm thickness was deposited on one side of the template to provide an electrical contact during the electrochemical growth. After the growth of the Ni NWs

within the AAO pores, the AAO and electrodes were dissolved, thus providing free-standing NWs ready for assembly. The NWs display a regular size of N = 200 nm with variable lengths of around a few tens of micrometers. NWs were then deposited onto a Si wafer with a thermally grown SiO_2 film of 150 nm thickness, which featured prepatterned evaporated metal pads of 50 μm^2 for electrical contact.

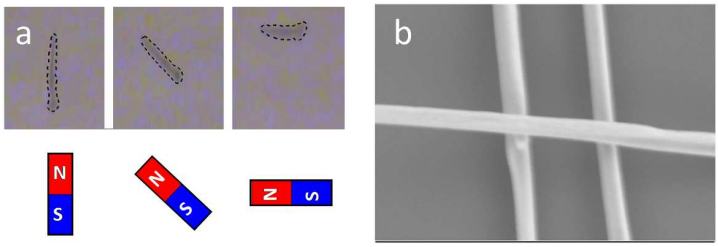

Figure 6.4: Optical micrographs of a single NW in acetone under magnetic field with different orientations (a) and crossbar NW structure resulting from the two-layer-assembly methodology (b).

NWs were aligned on the substrate by exploiting their ferromagnetic behavior, as demonstrated in Fig. 6.4a: NW orientation promptly changes according to the direction of an external magnetic field. This reorientiation allowed the deposition of two NW layers with perpendicular orientation. Two oxidation steps were applied to form the coreshell structure by thermal growth of a surface NiO layer on the NW. The first (bottom) NW layer was oxidized in air at 300°C for 3 hours [138], while the second (top) NW layer was oxidized by spontaneous room-temperature annealing in air, to avoid over-oxidation of the bottom coreshell NWs. Fig. 6.4b shows the resulting two-layer NW crossbar structure.

Fig. 6.5a shows high-resolution transmission electron microscopy (HRTEM) images for an Ni-NiO core-shell NW within the first layer. The NiO shell has an amorphous structure with a thickness of around 15 nm and a large surface roughness of about ±5 nm, due to nonuniform oxidation rate at the surface. The Ni core is polycrystalline with the face-centred cubic (fcc) structure, as revealed by the electron diffraction in the inset. Electron energy-loss spectroscopy (EELS) analysis on the coreshell NWs, shown in Fig. 6.5b, indicates a nonuniform, nonstoichiometric composition for the NWs of Ni_xO, with x > 1 in agreement with previous results for thermal oxidation of deposited Ni [78].

Fig. 6.6 shows schematic pictures and scanning electron microscopy (SEM) images of the complete structures developed in this study. We in-

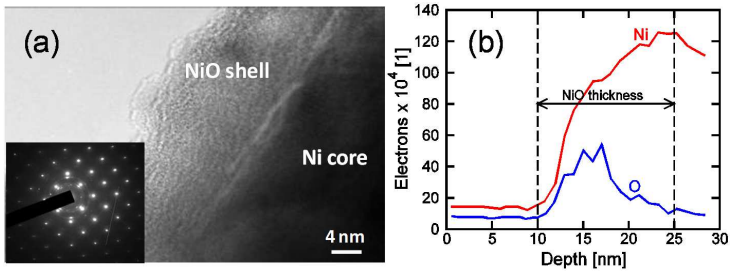

Figure 6.5: TEM image of a coreshell NW after oxidation in air for 1.5 hours at 300°C (a) and EELS profile along the radial direction of the NW (b). The electron diffraction spectrum in the inset indicates an fcc structure for the Ni core.

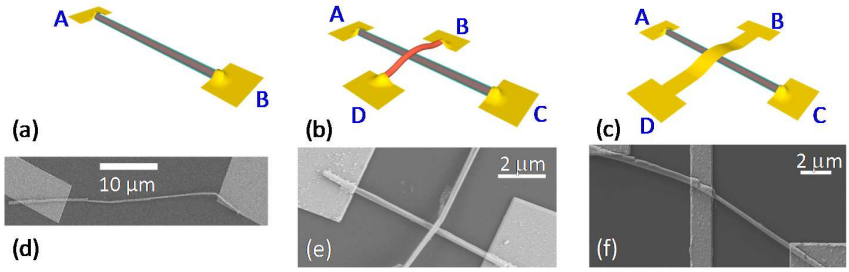

Figure 6.6: Schematic (ac) and SEM images (df) of the device structures investigated in this study. The structures include single coreshell NWs (a,d), a full bottom-up crossbar between two perpendicular coreshell NWs (b,e) and a hybrid bottom-up/ top-down crossbar structures between a coreshell NW and an Au strip (c,f).

vestigated isolated coreshell NWs (a, d), a full bottom-up crossbar junction between two coreshell NWs (b, e), and a hybrid bottom-up/top-down crossbar junction between a coreshell NW and a metallic strip defined by electron-beam lithography (EBL) on top of the NW (c, f). To electrically test the nanostructures, contact metallic lines were deposited by evaporation (200-nm thick Au with a Cr adhesion layer) and patterned using EBL.

6.2 Electrical characterization

Fig. 6.7 a shows the measured currentvoltage (IV) characteristics for the single core-shell NW structure in Fig. 6.6a and d. After an initial electroforming operation, which was needed to first initialize the CF for subsequent switching, the device displayed unipolar changes of resistance between a high (about 10 MΩ) and a low value (about 1 kΩ). Switching

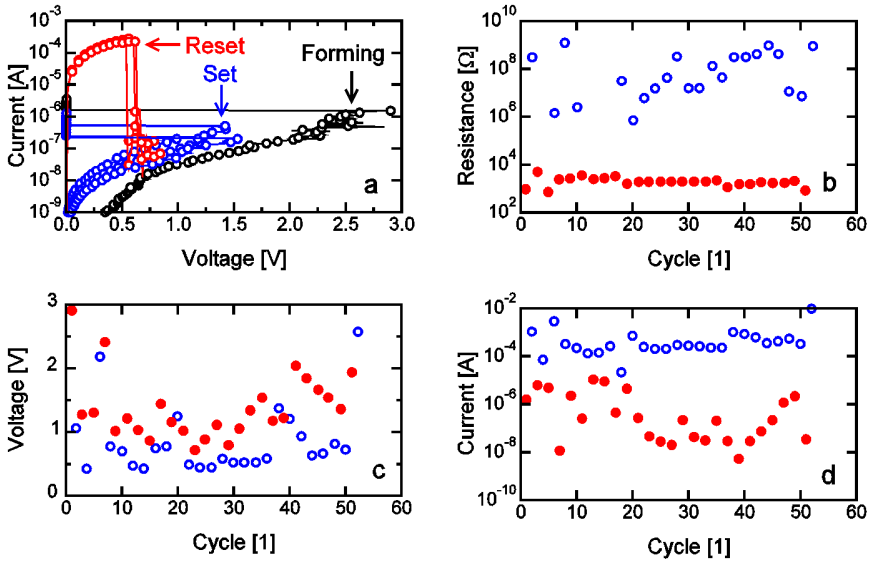

Figure 6.7: Measured switching characteristics for a single core-shell NW shown in Fig. 6.6d, showing $I-V$ curves for set/reset transistions (a), set/reset resistance as a function of the number of programming cycles (b), and set/reset voltage (c) and current (d) as a function of cycles.

from high to low resistance (set transition) occurred above 1 V, while the reverse (reset) transition occurred at a lower voltage of about 0.5 V. Fig. 6.7b shows the measured resistance for the two memory states as a function of the number of set/reset cycles. After about 50 set/reset cycles, the cell remained in a low-resistance state and resistance switching could not be repeated anymore, possibly due to irreversible dielectric breakdown of the NiO shell. Fig. 6.7c and d show the measured set/reset voltages and currents, respectively. Note that resistance switching displayed a unipolar switching behavior, in that both set and reset transitions occurred under the same bias polarity. This behavior can be explained by thermochemical reduction (set transition) and oxidation (reset transition), which are induced by the dissipation of local Joule heating in the filament region [108]. The switching mode, cycling lifetime, and set/reset parameters in Fig. 6.7 are in agreement with previous data for large, planar large NiO devices [108], which suggests that resistance switching is indeed due to the reversible metal-insulator transition in the thin active NiO shell of the NW. This result might explain why we achieved low switching voltages (set below 2 V, reset around 0.5 V) instead of the relatively high set voltage of around 10 V which was previously reported for NiO NWs [134]. In the latter case,

in fact, the threshold electric field for metal-insulator transition had to be developed across the whole length of the NiO NW, instead of the thin NiO shell in our coreshell NW. The location of resistance switching in the coreshell NW is believed to be the NiO shell at the extreme Au contact pads A or B in Fig. 6.6a.

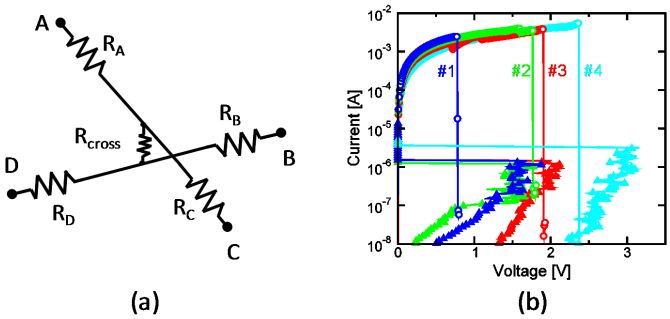

Figure 6.8: Resistance network model for the NW-NW crossbar structure (a) and measured IV curves showing set/reset switching across AB for four sequential cycles (b), for the sample in Fig. fig:crossb and e.

	State	R_{AC}	R_{BD}	R_{AB}
(a)	Initial	$> 10M\Omega$	$> 10M\Omega$	$> 10M\Omega$
(b)	AC, BD forming	180Ω	326Ω	$> 10M\Omega$
(c)	AB forming	180Ω	326Ω	265Ω
(d)	AB reset	182Ω	351Ω	$16M\Omega$

Table 6.1: Measured resistances for the NW-NW crossbar in Fig. 6.8, in the initial state (a), after forming across A_C and B_D (b), after forming across A_B (c) and after reset across A_B (d). High R states are highlighted in gray.

For minimum area occupation in a real memory chip, the crossbar structure in Fig. 6.6b and e is best suited. In fact, a crossbar array with core-shell NWs with 20 nm cell-cell pitch between adjacent NWs, corresponding to the 10-nm technology generation, would yield a memory density of one bit per 400 nm^2, which corresponds to 0.25 Tb cm^{-2}.

For a functional crossbar memory structure, however, switching must be located at the $Ni/NiO/Ni$ junction between the two coreshell NWs rather than at the $Au-$NW junction. To demonstrate switching at the crossing of NWs, we monitored all resistances between the crossbar terminals A, B, C, and D in Fig. 6.6b after electroforming, set, and reset transitions, and compared the measured results with the electrical network model of the crossbar junction in Fig. 6.8a. Here, the crossbar

structure is described by four resistances R_A, R_B, R_C, and R_D, each including the resistance of i) a Au contact electrode, ii) the NiO shell at the contact junction, and iii) the Ni core from the respective electrode to the crossing point, and by the resistance R_{cross}, which describes the NiO shell at the NWNW crossbar junction. Table 1 shows the measured resistances R_{AC}, R_{BD}, and R_{AB} measured before and after electroforming, set, and reset processes in the crossbar structure. All resistances were initially high with values above 10 MΩ (state 1 in Table 6.1), due to the presence of insulating NiO shells at both the AuNW and NWNW junctions. The AuNW junctions at contacts A and C were electroformed by applying a voltage of about 5 V across the two contacts, while contacts B and D were left floating to avoid any disturb to the NWNW junction. Similarly, electroforming of NiO layers at B and D contacts was carried out with electrically floating A and C contacts. After these preliminary electroforming steps, NW resistances R_{AC} and R_{BD} were found to be below 1 kΩ, while R_{AB} remained high due to the high value of R_{cross} at the NW NW junction (state 2 in Table 6.1). The latter was electroformed by applying a high voltage across contacts A and B, which resulted in a change of R_{AB} (hence R_{cross}) to a low value (state 3 in Table 6.1). The low resistance of about 265 Ω is mostly due to the metallic-type CF that is formed at the NW-NWjunction, as schematically shown in Fig. 6.1b. A high R_{cross} value of 16 MΩ was restored by the reset operation across contacts A and B (state 4 in Table 6.1). Note that reset affected only the NiO shell at the NWNW crossing and not at the AuNW junctions, since values of R_{AB} and R_{CD} remained low in state 4. Set was then carried out by applying a high voltage across contacts A and B, which resulted in resistance values similar to those of state 3 in Table 6.1. This procedure fully demonstrated, selective electroforming, set, and reset transitions of the NiO shell at the NWNW crosspoint junction, and thus provides proof of concept for a full bottom-up scheme for NW-based crossbar memory. Fig. 6.8b shows IV curves measured across contacts A and B for repeated set and reset states. The reset current of a few milliamperes and the set voltage of 1.52 V is consistent with data for planar NiO RRAMs [108]. Note that the reset current (above 2 mA in Fig. 6.8b) is higher than that of the single NW device (below 1 mA for most data points in Fig. 6.7d). This result can be attributed to the relatively large set voltage (above 1.5 V in Fig. 6.8b) in the NWNW switching device. In fact, a high set voltage is known to result in a current overshoot during the set transient, which causes CF overgrowth and a correspondingly high reset current [78, 108]. The latter can be suitably controlled by limiting the supply current during the set operation using the select transistor in the memory array. The cy-

cling endurance in our NWNW device was only four cycles, possibly due to unstable switching at the cross-point contact between the two NWs and/or to thermally induced mechanical failure of the contacts. SEM analysis of the devices after cycling suggests, in fact, that detachment and/or loss of NWs occurred after repeated electrical switching. This degradation might be improved by sealing the crossbar structure for a better mechanical stability. Another potential concern may arise from the relatively large series resistance in the metallic core, particularly at smaller NW sizes. By assuming a NW core with a diameter of 10 nm, which is consistent with the 10-nmgeneration node and an array size of 512 x 512, one obtains a series resistance of around 50 kΩ. By assuming a read voltage of 0.1 V, the read current in the set state would thus be around 0.1/50 mA = 2 μA, which is fully manageable using a dedicated read circuit.

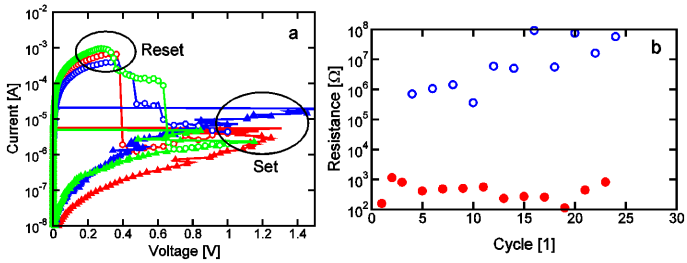

Figure 6.9: Measured IV curves during set/reset processes for the crossbar structure in 6.1c and f (a), and measured resistance after repeated set/reset cycles (b).

To take advantage of the high cycling lifetime of the single NW device in Fig. 6.6a and d, while maintaining the high potential memory density of the crossbar structure, we developed a crossbar device made using a hybrid bottom-up/top-down approach, as shown in Fig. 6.6c and f. This structure is similar to the NW-NW crossbar, where one NW is replaced by a metallic strip patterned by EBL [132]. Fig. 6.9 shows the measured $I-V$ curves for set and reset and the corresponding measured resistance as a function of the number of set/reset cycles for the nanostructure in Fig. 6.6c and f. The device lifetime was improved to 24 cycles, i.e., compatible with the single-NW device in Fig. 6.7. The switching location was confirmed to be at the NWstrip junction, rather than at the NWcontact junction, by using a characterization procedure similar to that described in the scheme in Fig. 6.8 and Table 6.1. Such a hybrid approach to NW crossbar arrays may provide a useful trade-off between inherent scaling capability of the bottom-up approach and an improved switching stability.

Summary of results

The science of today
is the technology of tomorrow.

Edward Teller (1908-2003)

A short summary of results and several concluding remarks are reported in the following.

Oxide based resistive switching memories represent a strong candidate for next generation solid state non-volatile memory technology. In particular, the extreme ease of fabrication, the relative low operating voltages and high write/erase speed suggest that this technology may became a valid alternative to Flash memories.

The working principle of RRAM is based on the capability of the material to switch reversibly between two different resistance values. The build-up of a thin conductive filament is responsible of the low resistance that characterizes the so-called set state. There are several experimental evidences that support this hypothesis, but still the actual nature of the conductive filament is unknown.

By the use of particular program algorithm we characterized carefully both set and reset states, showing in particular that there is a continuous transition between the set state, that is characterized by a metallic conduction, to the reset state that is, on the contrary, semiconductor-like with a certain activation energy for conduction. This change in resistance can be related to a modulation of defect doping and a consequent shift in the Fermi level. Thanks to this characterization we were able to extract an important microscopic parameter, namely the effective diameter of the conductive filament.

Starting from electrical characterization on NiO (unipolar) RRAM we developed physical models for the set (formation) and the reset (rupture) of conductive filaments, and their dependence on filament size/resistance. A Joule heating thermal model for reset accounts for

the reset voltage and current as a function of filament size, taking into account size-dependent heat conduction mechanisms and size-dependent diffusion/oxidation effects. Set transition is modeled by threshold switching while the resistance-dependent set voltage and current are well reproduced by a change in doping concentration and activation energy. The unipolar reset switching model was extended to the case of HfO (bipolar) RRAM by considering field driven ion migration. The physical comprehension of these switching mechanisms lead us to evidence a universal unipolar/bipolar reset model with negligible dependence on materials.

Physical-based numerical models for reset and retention of unipolar/bipolar RRAM have been presented. These models have been validated on electrical characterization results and can be used for numerical simulations of programming, reliability and scaling predictions.

For the first time we demonstrated complementary switching in single-stack nonpolar-RRAM devices, based on simulations and DC/pulsed experiments in symmetric HfO-based RRAM. The introduction of this new operation mode, which intrinsically solves the sneak-path problem in cross-bar arrays, seems to be very promising for the development of future high-density memory. Finally, complementary switching allowed us to explain the coexistence of unipolar and bipolar through vertical ion displacement by field-driven migration and electromigration/diffusion.

Reset current reduction has been accessed by the control of the dimension of the conductive filament. This can be done limiting the current drained by the cell during its growth, by mean of an integrated MOSFET. We characterized 1T1R structures, showing that there is a linear relationship between the current compliance imposed by the MOSFET during set, and the reset current. By the use of CAFM techniques we were able to direct manipulate single conductive filaments showing reset currents below 1 μA. These results are in line with the expected dependence on the size of the conductive filament thus supporting area scaling as a powerful method for program power reduction which is crucial for device scaling itself. In particular, since unipolar-RRAM may be utilized in cross-point array with dedicated selector diode, reset scaling is necessary to assure that the integrated diode may carry sufficient current.

We statistically studied data retention issues, showing that the time to failure for the set state (the reset state is on the contrary stable) depends on temperature with an Arrhenius-like behavior, and on the initial resistance, i.e. the diameter of the conductive filament and the activation energy. As can be qualitatively expected the failure time decreases for increasing resistances. This fact in turn yield to an intrinsic

trade-off between retention time and reset current, since the lower is the resistance, the higher is the current drained by the cell during reset.

Power reduction was addressed in in unipolar RRAMs by the use of pulsed program operation. Minimum reset current requires controlled set to avoid overshoot effects. Set-reset instability and set due to threshold switching in semiconductor-like conductive filament affect both DC and pulsed reset and appear as main issues in preventing low-current, stable and fast reset. This issue may be suppressed by careful set algorithms or material engineering aimed at obtaining metallic-like filaments with sufficiently high resistance.

To better assess reliability issues, we showed data and discussed RTN affecting the reset state. We developed a simple model based on trapping/detrapping of a single localized state that is able to reproduce data of relative resistance fluctuation as a function of the resistance. RTN however may hardly cause read mistakes or other issues.

The last part of this thesis was instead dedicated to the description of the synthesis and characterization of a novel device, based on the self-assembly of Ni-NiO core-shell nanowires. The assembly of complex architectures, starting from simple nanometric building blocks, possesses strong potentials since it may lead to the production of large arrays without lithographic limits. Here we demonstrated the working principle of a NiO RRAM constituted by the two NWs in a cross-bar structure. The contact point of the two NWs has in fact a $Ni/NiO/Ni$ stack. For the first time we showed resistive switching at the crosspoint of two nanowires. Set and reset parameters were shown to be compatible with typical values for planar structures. The missing encapsulation of these devices are probably responsible for their low endurance, that was evidenced during the characterization. Eventually we showed that better endurance can be achieved with hybrid devices made by a single core-shell NW, crossed by an EBL deposited metal strip.

List of Figures

Bibliography

[1] S. K. Lai, "Flash memories: successes and challenges," *IBM J. Res. Develop.*, vol. 52, pp. 529–535, 2008.

[2] G. W. Burr, B. N. Kurdi, J. C. Scott, C. H. Lam, K. Gopalakrishnan, and R. S. Shenoy, "Overview of candidate device technologies for storage-class memory," *IBM J. Res. Develop.*, vol. 52, pp. 449–464, 2008.

[3] *International Technology Roadmap for Semiconductors (ITRS)*, 2010.

[4] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash memory cells - an overview," *Proc. IEEE*, vol. 85, pp. 1248 – 1271, 1997.

[5] S. K. Lai, "Non-volatile memory technologies: The quest for ever lower cost," in *IEDM Tech. Dig.*, 2008, pp. 11–16.

[6] D. Ielmini, "Overview of modeling approaches for scaled non volatile memories," in *SISPAD*, 2009, p. 9.

[7] D. Ielmini, A. S. Spinelli, A. L. Lacaita, and A. Modelli, "A new two-trap tunneling model for the anomalous SILC in flash memories," *Microelectron. Eng.*, vol. 59, pp. 189–195, 2001.

[8] ——, "A statistical model for SILC in Flash memories," *IEEE Trans. Electron Devices*, vol. 49, pp. 1955–1961, 2002.

[9] N. Mielke, H. Belgal, I. Kalastirsky, P. Kalavade, A. Kurtz, M. Qingru, N. Righos, and W. Jie, "Flash EEPROM threshold instabilities due to charge trapping during program/erase cycling," *IEEE Trans. Dev. Mater. Reliab.*, vol. 4, pp. 335–344, 2004.

[10] A. Ghetti, M. Bonanomi, C. M. Compagnoni, A. S. Spinelli, A. L. Lacaita, and A. Visconti, "Physical modeling of single-trap RTS statistical distribution in flash memories," in *IRPS*, 2008, pp. 610–615.

[11] C. M. A. S. Spinelli, R. Gusmeroli, S. Beltrami, A. Ghetti, and A. Visconti, "Ultimate accuracy for the NAND Flash program algorithm due to the electron injection statistics," *IEEE Trans. Electron Devices*, vol. 55, pp. 2695–27 026, 2008.

[12] J.-D. Lee, S.-H. Hur, and J.-D. Choi, "Effects of floating-gate interference on NAND Flash memory cell operation," *IEEE Electron Device Lett.*, vol. 23, pp. 264–266, 2002.

[13] R. F. F. andW.W.Wilcke, "Storage-class memory: The next storage system technology," *IBM J. Res. Develop.*, vol. 52, pp. 439–446, 2008.

[14] A. Fazio, "Future directions of non-volatile memory in compute applications," in *IEDM Tech. Dig.*, 2009, pp. 641–644.

[15] T. Maeda, K. Itagaki, T. Hishida, R. Katsumata, M. Kito, Y. Fukuzumi, M. Kido, H. Tanaka, Y. Komori, M. Ishiduki, J. Matsunami, T. Fujiwara, H. Aochi, and Y. Iwata, "Multi-stacked 1G cell/layer pipe-shaped BICs Flash memory," in *Symp. on VLSI Tech. Dig*, 2009, pp. 22–23.

[16] J. Jang, H.-S. Kim, W. Cho, H. Cho, J. Kim, S. I. Shim, Y. Jang, J.-H. Jeong, B.-K. Son, D. W. Kim, K. Kim, J.-J. Shim, J. S. Lim, K.-H. Kim, S. Y. Yi, J.-Y. Lim, D. Chung, H.-C. Moon, S. Hwang, J.-W. Lee, Y.-H. Son, U.-I. Chung, and W.-S. Lee, "Vertical cell array using TCAT (Terabit cell array transistor) technology for ultra high density NAND Flash memory," in *Symp. on VLSI Tech. Dig*, 2009, pp. 192–193.

[17] J. Kim, A. J. Hong, S. M. Kim, E. B. Song, J. H. Park, J. Han, S. Choi, D. Jang, J.-T. Moon, and K. L. Wang, "Novel vertical-stacked-arraytransistor (VSAT) for ultra-high-density and cost-effective NAND Flash memory devices and SSD (solid state drive)," in *Symp. on VLSI Tech. Dig*, 2009, pp. 186–187.

[18] W. Kim, S. Choi, J. Sung, T. Lee, C. Park, H. Ko, J. Jung, I. Yoo, and Y. Park, "Multi-layered vertical gate NAND Flash overcoming stacking limit for terabit density storage," in *Symp. on VLSI Tech. Dig*, 2009, pp. 188–189.

[19] H. Tanaka, M. Kido, K. Yahashi, M. Oomura, R. Katsumata, M. Kito, Y. Fukuzumi, M. Sato, Y. Nagata, Y. Matsuoka,

Y. Iwata, H. Aochi, and A. Nitayama, "Bit cost scalable technology with punch and plug process for ultra high density flash memory," in *Symp. on VLSI Tech. Dig.*, 2007, pp. 14–15.

[20] S. R. Ovshinsky, "Reversible electrical switching phenomena in disordered structures," *Phys. Rev. Lett.*, vol. 21, p. 1450, 1968.

[21] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nature Mater.*, vol. 6, pp. 833–840, 2007.

[22] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories nanoionic mechanisms, prospects, and challenges," *Advanced Materials*, vol. 21, no. 25–26, p. 2632, 2009.

[23] L. Zhang, R. Huang, M. Zhu, S. Qin, Y. Kuang, D. Gao, C. Shi, and Y. Wang, "Unipolar TaO_x-based resistive change memory realized with electrode engineering," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 966–968, 2010.

[24] J. Park, M. Jo, J. Lee, S. Jung, S. Kim, W. Lee, J. Shin, and H. Hwang, "New set/reset scheme for excellent uniformity in bipolar resistive memory," *IEEE Electron Device Letters*, vol. 32, p. 63, 2011.

[25] J. Y. Son and Y.-H. Shin, "Direct observation of conducting filaments on resistive switching of *nio* thin films," *Appl. Phys. Lett.*, vol. 92, p. 222106, 2008.

[26] D. Ielmini, S. Spiga, F. Nardi, C. Cagli, A. Lamperti, E. Cianci, and M. Fanciulli, "Scaling analysis of submicrometer nickel-oxide-based resistive switching memory devices," *Journal of Applied Physics,*, vol. 109, p. 034506, 2011.

[27] J. Park, M. Jo, B. E.M., J. Yoon, D.-J. Seong, J. Lee, W. Lee, and H. Hwang, "Investigation of state stability of low-resistance state in resistive memory," *IEEE Electron Device Letters*, vol. 31, pp. 485–487, 2010.

[28] I. Baek, D. Kim, M. Lee, H.-J. Kim, E. Yim, M. Lee, J. Lee, S. Ahn, J. Seo, S. Lee, J. Park, Y. Cha, S. Park, H. Kim, I. Yoo, U. Chung, J. Moon, and B. Ryu, "Multi-layer cross-point binary oxide resistive memory (OxRRAM) for post-NAND storage application," in *IEDM Tech. Dig.*, 2005, pp. 750–753.

[29] B. Sun, Y. X. Liu, L. F. Liu, N. Xu, Y. Wang, X. Y. Liu, R. Q. Han, and J. F. Kang, "Highly uniform resistive switching characteristics of TiN/ZrO_2/Pt memory devices," *J. Appl. Phys.*, vol. 105, p. 061630, 2009.

[30] X. B. Yan, Y. D. Xia, H. N. Xu, X. Gao, H. T. Li, R. Li, J. Yin, and Z. G. Liu, "Effects of the electroforming polarity on bipolar resistive switching characteristics of $SrTiO_{3-\sigma}$ films," *J. Appl. Phys.*, vol. 97, p. 112101, 2010.

[31] H. Sim, D. Choi, D. Lee, S. Seo, M.-J. Lee, I.-K. Yoo, and H. Hwang, "Resistance-switching characteristics of polycrystalline Nb_2O_5 for nonvolatile memory application," *IEEE ELECTRON DEVICE LETTERS,*, vol. 26, pp. 292–294, 2005.

[32] W.-G. Kim and S.-W. Rhee, "Effect of the top electrode material on the resistive switching of TiO_2 thin film," *Microelectronic Engineering*, vol. 87, pp. 98–103, 2010.

[33] X. A. Tran, H. Y. Yu, Y. C. Yeo, L. Wu, W. J. Liu, Z. R. Wang, Z. Fang, K. L. Pey, X. W. Sun, A. Y. Du, B. Y. Nguyen, and M. F. Li, "A high-yield HfO_x-based unipolar resistive RAM employing ni electrode compatible with si-diode selector for crossbar integration," *IEEE Electron Device Letters*, vol. 32, pp. 396–398, 2011.

[34] S.-L. Li, D.S.Shang, J. Li, J. L.Gang, and D. Zheng, "Resistive switching properties in oxygen-deficient $Pr_0.7Ca_0.3MnO_3$ junctions with active al top electrodes," *J. Appl. Phys. 105*, p. 033710, 2009.

[35] R. Yasuhara, K. Fujiwara, K. Horiba, M. Kotsugi, F. Guo, H. Kumigashira, M. Oshima, and H. Tagaki, "Observation of inhomogeneous chemical states associated with resistance changes of *pt/cuo/pt* structures by photoemission electron microscopy," *XV International Workshop on Oxide Electronics*, 2008.

[36] Y.-S. Shin, "Non-volatile memory technologies for beyond 2010," in *Symp. VLSI Circ. Tech. Dig.*, 2005, pp. 156–159.

[37] U. Russo, D. Ielmini, A. Redaelli, and A. L. Lacaita, "Modeling of programming and read perfomances in phase-change memories - Part I: Cell optimization and scaling," *IEEE Trans. Electron Devices*, vol. 55, pp. 506–514, 2008.

[38] D. Deleruyelle, C. Dumas, M. Carmona, C. Muller, S. Spiga, and M. Fanciulli, "Direct observation at nanoscale of resistance switching in NiO layers by conductive-Atomic Force Microscopy," *Applied Physics Express*, vol. 4, p. 051101, 2011.

[39] M.-J. Lee, Y. Park, B.-S. Kang, S.-E. Ahn, C. Lee, K. Kim, W. Xianyu, and G. Stefanovich, "2-stack 1D-1R cross-point structure with oxide diodes as switch elements for high density resistance RAM applications," in *IEDM Tech. Dig.*, 2007, pp. 771–774.

[40] G. Tallarida, N. Huby, B. Kutrzeba-Kotowska, S. Spiga, M. Arcari, G. Csaba, P. Lugli, A. Redaelli, and R. Bez, "Low temperature rectifying junctions for crossbar non-volatile memory devices," in *IEEE IMW Tech. Dig.*, 2009.

[41] S. Tirano, L. Perniola, J. Buckley, J. Cluzel, J. V., C. Muller, D. Deleruyelle, B. De Salvo, and G. Reimbold, "Accurate analysis of parasitic current overshoot during forming operation in rrams," *Microelectron. Eng.*, vol. 88, pp. 1129–1132, July 2011.

[42] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, and Y. Sugiyama, "Reduction in the reset current in a resistive random access memory consisting of NiO_x brought about by reducing a parasitic capacitance," *Applied Physics Letters*, vol. 93, p. 033506, 2008.

[43] F. Nardi, D. Ielmini, C. Cagli, S. Spiga, M. Fanciulli, L. Goux, and D. J. Wouters, "Sub-10μA reset in NiO-based resistive switching memory (RRAM) cells," in *IEEE IMW Tech. Dig.*, 2010.

[44] D. Ielmini, "Reset-set instability in unipolar resistive switching memory," *IEEE Electron Device Lett.*, vol. 31, pp. 552–554, 2010.

[45] D.-K. Kim, dong Seok Suh, and J. Park, "Pulse-programming instabilities of unipolar-type NiO_x," *IEEE Electron Device Lett.*, vol. 31, pp. 600–602, 2010.

[46] D. Ielmini, C. Cagli, and F. Nardi, "Resistance transition in metal oxides induced by electronic threshold switching," *Appl. Phys. Lett.*, vol. 94, p. 063511, 2009.

[47] C. Cagli, F. Nardi, and D. Ielmini, "Modeling of set/reset operations in NiO-based resistive-switching memory RRAM devices," *IEEE Trans. Electron Devices*, vol. 56, pp. 1712–1720, 2009.

[48] S. Seo, M. J. Lee, D. H. Seo, E. J. Jeoung, D.-S. Suh, Y. S. Joung, I. K. Yoo, I. R. Hwang, S. H. Kim, I. S. Byun, J.-S. Kim, J. S. Choi, , and B. H. Park, "Reproducible resistance switching in polycrystalline NiO films," *Appl. Phys. Lett.*, vol. 85, p. 5655, 2005.

[49] T. N. Fang, S. Kaza, S. Haddad, A. Chen, Y. C. Wu, Z. Lan, S. Avanzino, D. Liao, C. Gopalan, S. Choi, S. Mahdavi, M. Buynoski, Y. Lin, C. Marrian, C. Bill, M. VanBuskirk, and M. Taguchi, "Erase mechanism for copper oxide resistive switching memory cells with nickel electrode," in *IEDM Tech. Dig.*, 2006, pp. 789–792.

[50] M.-J. Lee, Y. Park, B.-S. Kang, S.-E. Ahn, C. Lee, K. Kim, W. Xianyu, G. Stefanovich, J.-H. Lee, S.-J. Chung, Y.-H. Kim, C.-S. Lee, J.-B. Park, I.-G. Baek, and I.-K. Yoo, "2-stack 1D-1R cross-point structure with oxide diodes as switch elements for high density resistance RAM applications," in *IEDM Tech. Dig.*, 2007, pp. 771–774.

[51] K. Tsunoda, K. Kinoshita, H. Noshiro, Y. Yamazaki, T. Iizuka, Y. Ito, A. Takahashi, A. Okano, Y. Sato, T. Fukano, M. Aoki, and Y. Sugiyama, "Low power and high speed switching of Ti-doped NiO ReRAM under the unipolar voltage source of less than 3 V," in *IEDM Tech. Dig.*, 2007, pp. 767–770.

[52] U. Russo, D. Ielmini, C. Cagli, and A. L. Lacaita, "Filament conduction and reset mechanism in NiO-based resistive-switching memory (RRAM) devices," *IEEE Trans. Electron Devices*, vol. 56, pp. 186–192, 2009.

[53] D. Ielmini and Y. Zhang, "Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices," *J. Appl. Phys.*, vol. 102, p. 054517, 2007.

[54] H. D. Lee, B. M. Kope, and Y. Nishi, "Model of metallic filament formation and rupture in NiO for unipolar switching," *Phys. Rev. B*, vol. 81, p. 193202, 2010.

[55] F. P. Heiman and H. S. Miller, "Temperature dependence of n-type MOS transistor," *IEEE Trans. Electron Devices*, vol. 12, p. 142, 1965.

[56] K. Kanda, K. Nose, K. Kawaguchi, and T. Sakurai, "Design impact of positive temperature dependence on drain current in sub-1

V CMOS VLSIs," *IEEE J. Solid-State Circuits*, vol. 36, p. 1559, 2001.

[57] G. Groeseneken, J.-P. Colinge, H. E. Maes, J. C. Alderman, and S. Holt, "Temperature dependence of n-type MOS transistor," *IEEE Electron Device Lett.*, vol. 11, p. 329, 1990.

[58] U. Russo, D. Kalamanathan, D. Ielmini, A. L. Lacaita, and M. Kozicki, "Study of multilevel programming in programmable metallization cell (PMC) memory," *IEEE Trans. Electron Devices*, vol. 56, no. 5, pp. 1040–1047, 2009.

[59] J.-B. Yun, S. Kim, S. Seo, M.-J. Lee, D.-C. Kim, S.-E. Ahn, Y. Park, J. Kim, and H. Shin, "Fractal dimension of conducting paths in nickel oxide NiO thin films during resistance switching," *IEEE Trans. Nanotechnol.*, vol. 9, p. 131, 2010.

[60] S.-M. Lee, D. G. Cahill, and T. H. Allen, "Scaling behaviors of reset voltages and currents in unipolar resistance switching," *Appl. Phys. Lett.*, vol. 93, p. 212105, 2008.

[61] E. Pop, "The role of electrical and thermal contact resistance for Joule breakdown of single-wall carbon nanotubes," *Nanotechnology*, vol. 19, p. 295202, 2008.

[62] S. A. Makhlouf, "Electrical properties of nio films obtained by high-temperature oxidation of nickel," *Thin Solid Films*, vol. 516, pp. 3112–3116, 2008.

[63] D. Ielmini, F. Nardi, C. Cagli, and A. L. Lacaita, "Trade-off between data retention and reset in NiO RRAMs," in *Proc. IRPS*, 2010, pp. 620–6.

[64] ——, "Size-dependent retention time in NiO-based resistive switching memories," *IEEE Electron Device Lett.*, vol. 31, pp. 353–355, 2010.

[65] S. C. Chae, J. S. Lee, S. Kim, S. B. Lee, S. H. Chang, C. Liu, B. Kahng, H. Shin, D.-W. Kim, C. U. Jung, S. Seo, M.-J. Lee, and T. W. Noh, "Random circuit breaker network model for unipolar resistance switching," *Adv. Mater.*, vol. 20, no. 6, pp. 1154–1159, 2008.

[66] F. Nardi, D. Ielmini, C. Cagli, S. Spiga, M. Fanciulli, L. Goux, and D. J. Wouters, "Control of filament size and reduction of reset

current below 10 10μA in NiO resistance switching memories," *Solid State Electronics*, vol. 58, pp. 42–47, 2010.

[67] C. Cagli, D. Ielmini, F. Nardi, and A. L. Lacaita, "Evidence for threshold switching in the set process of NiO-based RRAM and physical modeling for set, reset, retention and disturb prediction," in *IEDM Tech. Dig.*, 2008, pp. 301–304.

[68] S. H. Chang, S. C. Chae, S. B. Lee, C. Liu, T. W. Noh, J. S. Lee, B. Kahng, J. H. Jang, M. Y. Kim, D.-W. Kim, , and C. U. Jung, "Random circuit breaker network model for unipolar resistance switching," *Appl. Phys. Lett.*, vol. 92, no. 18, p. 183507, 2008.

[69] S. H. Chang, J. S. Lee, S. C. Chae, S. B. Lee, C. Liu, B. Kahng, D.-W. Kim, , and T. W. Noh, "Random circuit breaker network model for unipolar resistance switching," *Phys. Rev. Lett.*, vol. 102, p. 026801, 2009.

[70] D. Ielmini, "Threshold switching mechanism by high-field energy gain in the hopping transport of chalcogenide glasses," *Phys. Rev. B*, vol. 78, p. 035308, 2008.

[71] S. Yu and H.-S. P. Wong, "A phenomenological model for the reset mechanism of metal oxide RRAM," *Electron Device Letters, IEEE*, vol. 31, no. 12, pp. 1455–1457, 2010.

[72] D. Kamalanathan, U. Russo, D. Ielmini, and M. N. Kozicki, "Voltage-driven on–off transition and tradeoff with program and erase current in programmable metallization cell (PMC) memory," *IEEE Electron Device Lett.*, vol. 30, pp. 553–555, 2009.

[73] D. Ielmini, F. Nardi, and C. Cagli, "Universal reset characteristics of unipolar and bipolar metal-oxide RRAM," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3246–3253, 2011.

[74] H. Y. Lee, P. S. Chen, T. Y. Wu, Y. S. Chen, C. C. Wang, P. J. Tzeng, C. H. Lin, F. Chen, C. H. Lien, and M. J. Tsai, "Low power and high speed bipolar switching with a thin reactive Ti buffer layer in robust HfO_2 based RRAM," in *IEDM Tech. Dig.*, 2008, pp. 1–4.

[75] S.-L. Li, D.S.Shang, J. Li, J. L.Gang, and D. Zheng, "Investigating the switching dynamics and multilevel capability of bipolar metal oxide resistive switching memory," *Appl. Phys. Lett.*, vol. 98, p. 103514, 2011.

[76] S. Larentis, C. Cagli, F. Nardi, and D. Ielmini, "Filament diffusion model for simulating reset and retention processes in RRAM," in *INFOS*, 2011.

[77] S. Menzel, M. Waters, A. Marchewka, U. Böttger, R. Dittmann, and R. Waser, "Origin of the ultra-nonlinear switching kinetics in oxide-based resistive switches," *Adv. Funct. Mater.*, pp. 1 – 6, 2011.

[78] L. Goux, J. G. Lisoni, X. P. Wang, M. Jurczak, and D. J. Wouters, "Optimized Ni oxidation in 80 nm contact holes for integration of forming-free and low-power Ni/NiO/Ni memory cells," *IEEE Trans. Electron Devices*, vol. 56, p. 2363, 2009.

[79] J. Lee, J. Shin, D. Lee, W. Lee, S. Jung, M. Jo, J. Park, K. P. Biju, S. Kim, S. Park, and H. Hwang, "Diode-less nano-scale ZrO_x/HfO_x RRAM device with excellent switching uniformity and reliability for high-density cross-point memory applications," in *IEDM Tech. Dig.*, 2010, pp. 452–455.

[80] T. Karakasidis and M. Meyer, "Grain-boundary diffusion of cation vacancies in nickel oxide: A molecular-dynamics study," *Phys. Rev. B*, vol. 55, no. 20, pp. 13 853–13 864, May 1997.

[81] U. Russo, D. Ielmini, C. Cagli, A. L. Lacaita, S. Spiga, C. Wiemer, M. Perego, and M. Fanciulli, "Conductive-filament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM," in *IEDM Tech. Dig.*, 2007, pp. 775–778.

[82] Z. Fang, H. Y. Yu, W. J. Liu, Z. R. Wang, X. A. Tran, B. Gao, and J. F. Kang, "Temperature instability of resistive switching on HfO_2-based RRAM devices," *IEEE Electron Device Lett.*, vol. 31, pp. 476–478, 2010.

[83] B. Gao, B. Sun, H. Zhang, L. Liu, X. Liu, R. Han, J. Kang, and B. Yu, "Unified physical model of bipolar oxide-based resistive switching memory," *IEEE Electron Device Lett.*, vol. 30, pp. 1326–1328, 2009.

[84] E. Linn, R. Rosezin, C. Kgeler, and R. Waser, "Complementary resistive switches for passive nanocrossbar memories," *Nature Materials*, vol. 9, pp. 403–306, 2010.

[85] Y.-C. Chen, C. F. Chen, C. T. Chen, J. Y. Yu, S. Wu, S. L. Lung, R. Liu, and C.-Y. Lu, "An access-transistor-free (0R/1R) non-volatile resistance random access memory (RRAM) using a novel

threshold switching, self-rectifying chalcogenide device," in *IEDM Tech. Dig. IEEE International*, 2003, pp. 905–908.

[86] Y. Wang, Q. Liu, S. Long, W. Wang, Q. Wang, M. Zhang, S. Zhang, Y. Li, Q. Zuo, J. Yang, and M. Liu, "Investigation of resistive switching in Cu-doped HfO_2 thin film for multilevel non-volatile memory applications," *Nanotechnology*, vol. 21, p. 045202, 2010.

[87] V. Jousseaume, A. Fantini, J. F. Nodin, C. Guedj, A. Persico, J. Buckley, S. Tirano, P. Lorenzi, R. Vignon, H. Feldis, S. Minoret, H. Grampeix, A. Roule, S. Favier, E. Martinez, P. Calka, N. Rochat, G. Auvert, J. P. Barnes, P. Gonon, C. Vallée, L. Perniola, and B. D. Salvo, "Comparative study of non-polar switching behaviors of NiO- and HfO_2-based Oxide Resistive-RAMs," in *IMW*, 2010, pp. 62–65.

[88] W. Guan, S. Long, Q. Liu, M. Liu, and W. Wang, "Nonpolar nonvolatile resistive switching in Cu doped ZrO_2," *Electron Device Letters, IEEE*, vol. 25, no. 5, pp. 434–437, 2008.

[89] H.-H. Huang, W.-C. Shih, and C.-H. Lai, "Nonpolar resistive switching in the Pt/MgO/Pt nonvolatile memory device," *Applied Physics Letters*, vol. 96, p. 193505, 2010.

[90] X. Liu, Z. Ji, D. Tu, L. Shang, J. Liu, M. Liu, and C. Xie, "Organic nonpolar nonvolatile resistive switching in poly(3,4-ethylenedioxythiophene): Polystyrenesulfonate thin film," *Organic Electronics*, vol. 10, pp. 1191–1194, 2009.

[91] L. Goux, J. G. Lisoni, M. Jurczak, D. J. Wouters, L. Courtade, and C. Muller, "Coexistence of the bipolar and unipolar resistive-switching modes in NiO cells made by thermal oxidation of Ni layers," *Journal of Applied Physics*, vol. 107, p. 024512, 2010.

[92] A. Demolliens, C. Muller, D. Deleruyelle, S. Spiga, E. Cianci, M. Fanciulli, F. Nardi, C. Cagli, and D. Ielmini, "Reliability of NiO-based resistive switching memory (RRAM) elements with pillar W bottom electrode," in *IEEE IMW Tech. Dig.*, 2009.

[93] B. S. Kang, S.-E. Ahn, M.-J. Lee, G. Stefanovich, K. H. Kim, W. X. Xianyu, C. B. Lee, Y. Park, I. G. Baek, and B. H. Park, "High-current-density $CuO_x/InZnO_x$ thin-film diodes for cross-point memory applications," *Advanced Materials*, vol. 20, pp. 3066–3069, 2008.

[94] D. Ielmini, D. Mantegazza, A. L. Lacaita, A. Pirovano, and F. Pellizzer, "Parasitic reset in the programming transient of PCMs," *IEEE Electron Device Letters*, vol. 26, pp. 799–801, 2005.

[95] U. Russo, D. Ielmini, and A. L. Lacaita, "A physics-based crystallization model for retention in phase-change memories," in *Proc. IRPS*, 2007, pp. 547–553.

[96] Y. Sato, K. Tsunoda, K. Kinoshita, H. Noshiro, M. Aoki, and Y. Sugiyama, "Sub-$100-\mu$A reset current of nickel oxide resistive memory through control of filamentary conductance by current limit of MOSFET," *IEEE Trans. Electron Devices*, vol. 55, pp. 1185–1191, 2008.

[97] S. Spiga, A. Lamperti, C. Wiemer, M. Perego, E. Cianci, G. Tallarida, H. Lu, M. Alia, F. G. Volpe, and M. Fanciulli, "Study of the interfaces in resistive switching NiO thin films deposited by both ALD and e-beam coupled with different electrodes (Si, Ni, Pt, W, TiN)," *Microelectron. Eng*, vol. 85, pp. 2425–2429, 2008.

[98] D. Ielmini, F. Nardi, and C. Cagli, "Resistance-dependent amplitude of random telegraph signal noise in resistive switching memories," *Appl. Phys. Lett.*, vol. 96, p. 053503, 2010.

[99] D. Ielmini, M. Boniardi, A. L. Lacaita, A.Redaelli, and A. Pirovano, "Unified mechanisms for structural relaxation and crystallization in phase-change memory devices," *Microelectron. Eng.*, vol. 86, pp. 1942–1945, 2009.

[100] J. Oh, J. Park, Y. Lim, H. Lim, Y. Oh, J. Kim, J. Shin, Y. Song, K. Ryoo, D. Lim, S. Park, J. Kim, J. Kim, J. Yu, F. Yeung, C. Jeong, J. Kong, D. Kang, G. Koh, G. Jeong, H. Jeong, and K. Kim, "Full integration of highly manufacturable 512mb pram based on 90 nm technology," in *IEDM Tech. Dig.*, 2006, pp. 1 – 4.

[101] Y. Sasago, M. Kinoshita, T. Morikawa, K. Kurotsuchi, S. Hanzawa, T. Mine, A. Shima, H. Fujisaki, Y. Kume, H. Moriya, N. Takaura, and K. Torii, "Cross-point phase change memory with $4F^2$ cell size driven by low-contact resistivity poly-si diode," in *Symp. VLSI Tech. Dig.*, 2009, pp. 24–25.

[102] A. Redaelli, A. Pirovano, I. Tortorelli, F. Ottogalli, A. Ghetti, L. Laurin, and A. Benvenuti, "Impact of the current density increase on reliability in scaled BJT-selected PCM for high-density applications," in *Proc. IRPS*, 2010.

[103] C. Dumas, D. Deleruyelle, A. Demolliens, C. Muller, S. Spiga, E. Cianci, M. Fanciulli, I. Tortorelli, and R. Bez, "Resistive switching characteristics of NiO films deposited on top of W or Cu pillar bottom electrodes," *Thin Solid Films*, vol. 519, pp. 3798–3803, 2011.

[104] M. Lanza, M. Porti, M. Nafría, X. Aymerich, E. Whittaker, and B. Hamilton, "UHV CAFM characterization of high-k dielectrics: Effect of the technique resolution on the pre- and post-breakdown electrical measurements," *Microelectronics Reliability*, vol. 50, pp. 1312–1315, 2010.

[105] C. Szot, W. Speier, G. Bihlmayer, and R. Waser, "Switching the electrical resistance of individual dislocations in single-crystalline $SrTiO_3$," *Nature Materials*, vol. 5, p. 312, 2006.

[106] G.-S. Park, X.-S. Li, D.-C. Kim, R.-J. Jung, M.-J. Lee, and S. Seo, "Observation of electric-field induced Ni filament channels in polycrystalline NiO_x film," *Appl. Phys. Lett.*, vol. 91, p. 222103, 2007.

[107] M. A. Alam, B. E. Weir, and P. J. Silverman, "A study of soft and hard breakdown-part I: Analysis of statistical percolation conductance," *IEEE Trans. Electron Devices*, vol. 49, p. 232, 2002.

[108] D. Ielmini, F. Nardi, and C. Cagli, "Physical models of size-dependent nanofilament formation and rupture in NiO resistive switching memories," *Nanotechnology*, vol. 22, no. 25, p. 254022, 2011.

[109] M. Bocquet, D. Deleruyelle, C. Muller, and J.-M. Portal, "Self-consistent physical modeling of set/reset operations in unipolar resistive-switching memories," *Appl. Phys. Lett.*, vol. 98, p. 263507, 2011.

[110] D. Ielmini, F. Nardi, and C. Cagli, "Universal reset characteristics of unipolar and bipolar metal-oxide rram," *Electron Devices, IEEE Transactions on*, vol. 58, no. 10, pp. 3246 –3253, oct. 2011.

[111] D. Ielmini, D. Sharma, S. Lavizzari, and A. L. Lacaita, "Reliability impact of chalcogenide-structure relaxation in phase-change memory (PCM) cells – Part I: Experimental Study," *IEEE Trans. Electron Devices*, vol. 56, pp. 1070–1077, 2009.

[112] U. Russo, D. Ielmini, C. Cagli, and A. L. Lacaita, "Self-accelerated thermal dissolution model for reset programming in NiO-based re-

sistive switching memory (RRAM) devices," *IEEE Trans. Electron Devices*, vol. 56, no. 2, pp. 193–200, 2009.

[113] J. Park, J. Yoon, M. Jo, D.-J. Seong, J. Lee, W. Lee, J. Shin, E.-M. Bourin, and H. Hwang, "Effect of filament resistance on retention characteristics of ReRAM," in *as discussed at 2009 IEEE SISC, Arlington, VA*, 2009.

[114] D. Mantegazza, D. Ielmini, E. Varesi, A. Pirovano, and A. L. Lacaita, "Statistical analysis and modeling of programming and retention in PCM arrays," in *IEDM Tech. Dig.*, 2007, paper 46.6.

[115] D. Ielmini, A. S. Spinelli, A. L. Lacaita, and A. Modelli, "Equivalent cell approach for extraction of the SILC distribution in Flash EEPROM cells," *IEEE Electron Device Lett.*, vol. 23, pp. 40–42, Jan. 2002.

[116] D. Ielmini and M. Boniardi, "Common signature of many-body thermal excitation in structural relaxation and crystallization of chalcogenide glasses," *Appl. Phys. Lett.*, vol. 94, p. 091906, 2009.

[117] D. Ielmini, F. Nardi, A. Vigani, E. Cianci, and S. Spiga, "Read-disturb limited reliability of multilevel NiO-based resistive-switching memory," in *IEEE SISC*, 2009.

[118] M. Yin, P. Zhou, H. B. Lv, J. Xu, Y. L. Song, X. F. Fu, T. A. Tang, B. A. Chen, and Y. Y. Lin, "Improvement of resistive switching in Cu_xO using new reset mode," *Electron Device Letters, IEEE*, vol. 29, pp. 681–683, 2008.

[119] K. S. Ralls, W. J. Skocpol, L. D. Jackel, R. E. Howard, L. A. Fetter, R. W. Epworth, and D. M. Tennant, "Discrete resistance switching in submicrometer silicon inversion layers: Individual interface traps and lowfrequency 1/f noise," *Phys. Rev. Lett.*, vol. 52, pp. 228–231, 1984.

[120] D. Ielmini and Y. Zhang, "Evidence for trap-limited transport in the subthreshold conduction regime of chalcogenide glasses," *Appl. Phys. Lett.*, vol. 90, p. 192102, 2007.

[121] R. S. Crandall, "Defect relaxation in amorphous silicon: Stretched exponential, the Meyer-Neldel rule, and the Staebler-Wronski effect," *Phys. Rev. B*, vol. 43, pp. 4057–4070, 1991.

[122] T. Ohgai, L. Gravier, X. Hoffer, M. Lindeberg, K. Hjort, R. Spohr, and J.-P. Ansermet, "Template synthesis and magnetoresistance property of ni and co single nanowires electrodeposited into nanopores with a wide range of aspect ratios," *Journal of Physics D: Applied Physics*, vol. 36, no. 24, pp. 3109–3114, 2003. [Online]. Available: http://stacks.iop.org/0022-3727/36/3109

[123] D. N. Davydov, J. Haruyama, D. Routkevitch, B. W. Statt, D. Ellis, M. Moskovits, and J. M. Xu, "Nonlithographic nanowire-array tunnel device: Fabrication, zero-bias anomalies, and Coulomb blockade," *Phys. Rev. B*, vol. 57, no. 21, pp. 13 550–13 553, Jun 1998.

[124] K. V. Rao and A. Smakula, "Dielectric properties of cobalt oxide, nickel oxide, and their mixed crystals," *J. Appl. Phys.*, vol. 36, pp. 2031–2039, 1991.

[125] D. Fugazza, D. Ielmini, S. Lavizzari, and A. L. Lacaita, "Distributed-Poole-Frenkel modeling of anomalous resistance scaling and fluctuations in phase-change memory (PCM) devices," in *IEDM Tech. Dig.*, 2009, pp. 723–726.

[126] T. P. Chen, M. S. Tse, X. Zeng, and S. Fung, "On the switching behaviour of post-breakdown conduction in ultra-thin SiO_2 films," *Semicond. Sci. Technol.*, vol. 16, pp. 793–799, 2001.

[127] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Lett.*, vol. 10, p. 1297, 2010.

[128] M. Meier, C. Nauenheim, S. Gilles, D. Mayer, C. Kugeler, and R. Waser, "Nanoimprint for future non-volatile memory and logic devices," *Microelectron. Eng.*, vol. 85, pp. 870 – 872, 2008.

[129] W. Lu and C. M. Lieber, "Nanoelectronics from the bottom up," *Nat. Mater.*, vol. 6, p. 841, 2007.

[130] Y. Huang, X. Duan, Y. Cui, L. J. Lauhon, K.-H. Kim, and C. M. Lieber, "Logic gates and computation from assembled nanowire building blocks," *Science*, vol. 294, p. 1313, 2001.

[131] X. Duan, Y. Huang, and C. M. Lieber, "Nonvolatile memory and programmable logic from molecule-gated nanowires," *Nano Lett.*, vol. 2, p. 487, 2002.

[132] Y. Dong, G. Yu, M. C. McAlpine, W. Lu, and C. M. Lieber, "Si/a-Si core/shell nanowires as nonvolatile crossbar switches," *Nano Lett.*, vol. 8, p. 386, 2008.

[133] S. I. Kim, J. H. Lee, Y. W. Chang, S. S. Hwang, and K.-H. Yoo, "Reversible resistive switching behaviors in NiO nanowires," *Applied Physics Letters*, vol. 93, p. 033503, 2008.

[134] K. Oka, T. Yanagida, K. Nagashima, T. Kawai, J.-S. Kim, and B. H. Park, "Nonvolatile bipolar resistive memory switching in single crystalline NiO heterostructured nanowires," *J. Am. Chem. Soc*, vol. 132, p. 6634, 2010.

[135] N. A. Melosh, A. Boukai, F. Diana, B. Gerardot, A. Badolato, P. M. Petroff, and J. R. Heath, "Ultrahigh-density nanowire lattices and circuits," *Science*, vol. 300, p. 112, 2003.

[136] G. Y. Jung, S. Ganapathiappan, D. A. A. Ohlberg, D. L. Olynick, Y. Chen, W. M. Tong, and R. S. Williams, "Fabrication of a 34 x 34 crossbar structure at 50 nm half-pitch by UV-based nanoimprint lithography," *Nano Lett.*, vol. 4, p. 1225, 2004.

[137] X. Zhao, J.-L. Sun, and J.-L. Zhu, "Field-induced semiconductor-metal transition in individual NiONi schottky nanojunction," *Appl. Phys. Lett.*, vol. 93, p. 152107, 2008.

[138] L. Courtade, C. Turquat, C. Muller, J. G. Lisoni, L. Goux, D. J. Wouters, D. Goguenheim, P. Roussel, and L. Ortega, "Oxidation kinetics of Ni metallic films: Formation of NiO-based resistive switching structures," *Thin Solid Films*, vol. 516, pp. 4083–4092, 2008.

List of publications

C. Cagli, F. Nardi and D. Ielmini "Modeling of Set/Reset Operations in NiO-Based Resistive-Switching Memory Devices", IEEE Trans. Electron Devices, VOL. 56, NO. 8, August 2009.

D. Ielmini, C. Cagli and F. Nardi "Resistance transition in metal oxides induced by electronic threshold switching", Applied Physics Letters 94, 063511, (2009).

D. Ielmini, F. Nardi, C. Cagli and A. L. Lacaita "Size-dependent retention time in NiO-based resistive switching memories", IEEE Electron Device Letters, VOL. 31, NO. 4, APRIL 2010.

D. Ielmini, F. Nardi and C. Cagli "Resistance-dependent amplitude of random telegraph-signal noise in resistive switching memories", Applied Physics Letters 96, 053503 (2010).

F. Nardi, D. Ielmini, C. Cagli, S. Spiga, M. Fanciulli, L. Goux and D. J. Wouters "Control of filament size and reduction of reset current below 10 μA in NiO resistance switching memories", Solid State Electronics, Volume 58, Issue 1, April 2011, Pages 42-47.

D. Ielmini, F. Nardi and C. Cagli "Physical models of size-dependent nanofilament formation and rupture in NiO resistive switching memories", Nanotechnology 22, 254022 (2011).

D. Ielmini, S. Spiga, F. Nardi, C. Cagli, A. Lamperti, E. Cianci and M. Fanciulli "Scaling analysis of submicrometer nickel-oxide-based resistive switching memory devices", Journal of Applied Physics, 109, 034506 (2011).

F. Nardi, C. Cagli, S. Spiga and D. Ielmini "Reset instability in pulsed-operated unipolar resistive switching memory", IEEE Electron Device Letters, VOL. 32, NO. 6, JUNE 2011.

S. Larentis, C. Cagli, F. Nardi and D. Ielmini "Filament diffusion model for simulating reset and retention processes in RRAM", Microelectronic Engineering, 2011, Volume 88, Issue 7, July 2011, Pages 1119-1123.

D. Ielmini, F. Nardi and C. Cagli "Universal reset characteristics of unipolar and bipolar metal-oxide RRAM", IEEE Transaction on Electron Devices, 2011, (in press).

C. Cagli, F. Nardi, B. Harteneck, Z. Tan, Y. Zhang and D. Ielmini "Resistive-switching crossbar memory based on Ni-NiO core-shell nanowires", Small, (in press).

C. Cagli, D. Ielmini, F. Nardi and A. L. Lacaita "Evidence for threshold switching in the set process of NiO-based RRAM and physical modeling for set, reset, retention and disturb prediction", IEEE International Electron Device Meeting (IEDM) 2008, S. Francisco, CA (USA).

A. Demolliens, Ch. Muller, D. Deleruyelle, S. Spiga, E. Cianci, M. Fanciulli, F. Nardi, C. Cagli and D. Ielmini "Reliability of NiO-based resistive switching memory (ReRAM) elements with pillar W bottom electrode", IEEE International Memory Workshop (IMW) 2009, Monterey, CA (USA).

D. Ielmini, F. Nardi, A. Vigani, E. Cianci and S. Spiga "Read-disturb limited reliability of multilevel NiO-based resistive-switching memory", Semiconductor Interface Specialists Conference (SISC) 2009, Arlington, VA (USA).

D. Ielmini, F. Nardi, C. Cagli and A. L. Lacaita "Trade-off between data retention and reset in NiO RRAMs", SIEEE International Reliability Physics Symposium (IRPS) 2010, Anaheim, CA (USA).

D. Ielmini, F. Nardi, C. Cagli and A. L. Lacaita "Size-dependent temperature instability in NiO-based resistive switching memory", MRS Spring Meeting 2010, S. Francisco, CA (USA).

F. Nardi, D. Ielmini, C. Cagli, S. Spiga, M. Fanciulli, L.Goux, D. J. Wouters "Sub-10 μA reset in NiO-based resistive switching memory (RRAM) cells", IEEE International Memory Workshop (IMW) 2010, Seoul (Korea).

D. Ielmini, C. Cagli, F. Nardi, A. L. Lacaita "Resistance-dependent switching in NiO-based filamentary RRAM devices", International

Symposium on Integrated Functionalities (ISIF) 2010, San Juan, Puerto Rico.

D. Ielmini, F. Nardi, C. Cagli "Universal switching and noise characteristics of nanofilaments in metal-oxide RRAMs", Semiconductor Interface Specialists Conference (SISC) 2010, San Diego, CA (USA).

C. Cagli, B. Harteneck, F. Nardi, Z. Tan, Y. Zhang, and D. Ielmini "Size-dependent temperature instability in NiO-based resistive switching memory", MRS 04/2011 San Francisco, CA (USA). .

F. Nardi, C. Cagli, S. Spiga, D. Ielmini "Reset current reduction and set-reset instabilities in unipolar NiO RRAM", IEEE International Memory Workshop (IMW) 2011, Monterey, CA (USA).

S. Larentis, C. Cagli, F. Nardi and D. Ielmini "Filament diffusion model for simulating reset and retention processes in RRAM", Insulating Films on Semiconductors (INFOS) 2011, Grenoble, France.

C. Cagli, F. Nardi, B. Harteneck, Z. Tan,Y. Zhang and D. Ielmini "Nanowire-based RRAM crossbar memory with metallic core-oxide shell nanostructure", European Solid-State Device Research Conference (ESSDERC) 2001, Helsinki, Finland.

F. Nardi, S. Balatti, S. Larentis and D. Ielmini "Complementary switching in metal oxides: toward diode-less crossbar RRAMs", IEEE International Electron Device Meeting (IEDM) 2011, Washington, DC (USA), accepted.

Ringraziamenti

Prima di tutti voglio ringraziare il mio Prof. Daniele Ielmini che in questi quattro anni (contando anche l'anno passato assieme durante la tesi laurea) è stato la mia guida nello straordinario mondo della ricerca scientifica. Mondo in cui spero di continuare a lavorare ed essere in grado di mettere in pratica tutti gli insegnamenti che ho ricevuto.

In secondo luogo ringrazio tutti i miei colleghi di laboratorio. E' una lista lunghissima... Quanta gente è passata in questi anni! In ordine sparso ringrazio: Mirko, Tiziano, Michele, Simone, Angelo, Deepak, Fugaz, Mattia, Carmine, Mack, Salvo, Simone, Nicola, Giovanni, Seol, Stefano, Carlo e tutti gli altri che sicuramente ho dimenticato. E' stato un piacere lavorare con voi!

Un rigranziamento speciale va al Bonf, uno dei pilastri del laboratorio. Grazie a lui ho iniziato a dedicarmi all'attività della corsa anche se senza molto successo... il maestro rimarrà sempre irraggiungibile! Oltre che un ottimo collega è stato davvero un amico prezioso in tutto questo tempo. Ti ringrazio.

Vista la così bella compagnia avrei voluto continuare a lavorare in questo fantastico laboratorio del Politecnico di Milano ma purtroppo gli eventi mi hanno portato altrove. Infatti sto scrivendo queste ultime righe dalla Silicon Valley dove domani mattina inizierò una nuova avventura.

Certamente devo ringraziare la piccola comunità di amici all'estero che ho conosciuto in Francia a Marseille e negli US a Berkeley. Anche qui in ordine sparso: Damien, Stefano, Hannes, Magalì, Christophe, Inigo, Marc, Bob, Irene, Anni, Julian e tutti gli altri. Insomma anche qui tantissime persone.

Che dire di tutti i miei amici storici? Luca, Vì, Cele, Seba, Stefania, Tia, Delo, Lore, Nello... Siamo cresciuti assieme ed hanno saputo dimostrarmi amicizia ed affetto incredibili. Mi sono sempre stati vicini soprattutto nei momenti di difficoltà e di lontananza... A loro devo il

superamento di queste difficoltà che mi hanno inaspettatamente portato ad una delle più belle cose della mia vita: grazie Manu.

Infine, un ringraziamento a parte e speciale va ai miei genitori. Quello che sono lo devo a loro e spero potranno essere sempre orgogliosi di me e che potrò ripagarli di tutti gli sforzi che hanno fatto per crescermi. Anche se lontano vi sarò sempre vicino.

POLITECNICO DI MILANO
Dipartimento di Elettronica e Informazione
Piazza Leonardo da Vinci, 32 I 20133 – Milano