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CRYOGENIC ELECTRONIC CIRCUITS OPERATING AT 1 KELVIN FOR CHARACTERIZATION OF QUANTUM DEVICES

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Contents

Abstract

In this PhD thesis we studied, designed, realized and tested custom instrumentation for cryogenic measurement, in particular measurement on quantum dot for quantum computing. This kind of investigation has huge application on cryptography, advanced physical simulation and single electron devices.

In *chapter 1* after a short introduction on quantum computing we'll present quantum dot devices their application, showing their capability to study single electron effects. We underline the conditions of temperature and magnetic field required for good quantum measurement in *chapter 2* and we show the experimental set-up to perform quantum dot measurement in 300mK and 12T magnetic field environment. The information are extracted by measuring the current signal passing thought the dot. This current reflects about the single energy levels into the 0-dimensional quantum dot. But this complicated set-up reduces the accessibility of detection electronics which can be placed only several meters far away from the sample; this requires the presence of a long cable between quantum dot and electronic and so a big input capacitance for electronics that can reach up to 1nF; we show that this huge capacitance reduces the measurement's performance both resolution and bandwidth. In *chapter 3* we show a characterization at 4 Kelvin of a cmos technology $0.35\mu m$ by Ams. In fact the only way to reduce the input capacitance, improving the performances of measurements, is attaching the electronics near the sample inside the cryostat, which provides the low temperature and high magnetic field to the sample. A integrated technology is necessary for dimensional reasons, inside the cryostat the temperature can reach up to 1-5 kelvin or below; at this low temperature jFet and bipolar transistors don't work due to freeze-out effect while cmos technology based on drift current and degenerated doped silicon can even work but the foundries do not provide models for such a low temperature; so a complete characterization is necessary. This characterization shows that transistor can work up to 4 Kelvin with higher threshold voltage and higher mobility but only if their dimensional ratio W/L is below a certain value (35 for Nmos 70 for Pmos) otherwise more complex phenomenon (hysteresis and kink effects) happen making the transistor unusable. In *chapter 4* we design,

realized and tested a hybrid transimpedance amplifier in which the operational amplifier is split in two parts; one is a single transistor stage at cryogenic temperature and the other is a commercial room temperature opamp. In this way is possible to reduce the input capacitance. The tests show a bandwidth of 10kHz and a noise of $1.3pA_{rms}$. In *chapter 5* we design and tested a cryogenic transimpedance with a whole cryogenic operational amplifier, to overtake the high input offset voltage of single transistor stage and obtain a transimpedance less affected by disturbs and by long connection cables. We obtain a 30kHz bandwidth with $2.8pA_{rms}$. In *chapter 6* we improve the performances by using a non-conventional structure, based on internal feedback operational amplifier instead standard two-stage structures. We reach up to 100kHz bandwidth and $40pA_{rms}$ resolution. Finally we'll present a conclusion of the work of this PhD thesis.

Chapter 1

Quantum dot for quantum computing

Quantum computing is a very challenging field of investigation; his purpose is to built quantum computer, taking advantage of peculiarities of quantum mechanics; in particular superposition and entanglement by using a quantum magnitude as fundamental unit called qubit correspondent to classical bit. It has be proven that quantum computing could perform problems that seems intractable with a standard computer [1]. But managing quantum element controlling them and maintaining their quantum properties for a reasonable time it's hard to achieve. One of the most used synthesis of quantum circuit is based on quantum dots; in fact the confinement in quantum dot (see appendix C) permits to manage also single electron [2] and use their quantum magnitude, like position to implement a quantistic elaboration. But they require a low temperature to permit to quantum mechanism to take part; and also a dedicated and sophisticated electronics is required. Here we'll present the main feature or quantum computation and the structure of quantum dot's in next chapter we'll going into design a dedicated electronics.

1.1 Principles of quantum information

Quantum computation use quantum magnitude to elaborate information and solve a specific task. But quantum information is quite different from standard one, in particular it must obey to the following limits:

No Coping Quantum information can not be copied because it can not be read with fidelity [3].

Transfer Quantum information can be transfered only it the original is destroyed [4]

Measurement Measuring the information destroy part of it.

Probabilistic In general the measuring process is probabilistic-depend

Indetermination Some observable can not be known simultaneously.

there limits belong to the characteristic of quantum mechanics. A quantum magnitude, like for example, the position of one electron is view like a wave called wave-function which magnitude in one point reflects the probability of the electron to be in that point; the measure of the position provokes a collapse of the wave-function in one point. Although the measure destroys part of the information, the precision during the processing is infinite, there are no problems of underflow or overflow or, in other words, a quantum algorithm is always stable except to input and output. With quantum computing is moreover possible to generate random numbers instead of pseudo-random of standard computation.

1.2 Qubit

Feynman [5] in 1985 starts to discuss the question of using quantum physic element to compute unsolvable problem with standard computation. In standard computation the basic unit of information is bit; in quantum computing is called *qubit*; while a bit can only be 0 or 1 a qubit is a linear superposition of two state called $|0\rangle$ or $|1\rangle$. A quantum computer is similar to a probabilistic computer; where to each state corresponds a probability ${}^1P$ and ${}^0P$ whose sum has to be unitary. Similarly the state of a qubit can be represented by two complex number c_0 and c_1 and corresponds to a vector in a C^2 Hilbert Space[1].

$$qubit \Rightarrow a|0\rangle + b|1\rangle \tag{1.1}$$

$|a|^2$ and $|b|^2$ are the probability that the qubit is in state $|0\rangle$ or $|1\rangle$ as consequence must be verified the relationship $|a|^2+|b|^2 = 1$. This status vector can also be represented by the coordinates of the vector (a b) while using as bases the vector (1 0), corresponding to $|0\rangle$, and (0 1) corresponding to $|1\rangle$. So a qubit carries the information of two real number (real and imaginary part) in contrast with single bit carried by a binary digit.

A quantum processor is composed by N qubit, the status of these N qubit is a linear superposition of the 2^N basis vector:

[1] A Hilbert space is a space of complex number in n dimension

$$\begin{aligned} &|0\rangle \otimes |0\rangle \otimes \cdots |0\rangle \\ &|0\rangle \otimes |0\rangle \otimes \cdots |1\rangle \\ &\quad \vdots \\ &|1\rangle \otimes |1\rangle \otimes \cdots |1\rangle \end{aligned} \tag{1.2}$$

and so can be represented by a 2^N-dimensional vector[2] in the C^{2^N} Hilbert space (a_1 a_2 a_3 ... a_i ... a_{2^N}); N qubit carries 2^N complex number in respect to the integer range $(0..2^N - 1)$ carried by N bit. The probability that the quantum computer has to be in ith state is $|a_i|^2$ this reflects the interpretation of the wave-function of an electron. Must always be verified the relationship.

$$\sum_{i=1}^{2^N} |a_i|^2 = 1 \tag{1.3}$$

Although we might think that qubit carries exponential information in comparison with bit it is important to remember than when we measure the state of a qubit the wave-function collapses into a single classical state. So the status of a unmeasured quantum computer with N qubit is indexable by 2^N complex coefficient but once measured all coefficient collapses into 0 or 1, and so the final status is representable with an integer from 0 to $2^N - 1$, like classical bit:

$$|a_1\rangle \otimes |a_2\rangle \otimes \cdots |a_{2^N}\rangle \equiv |a_1 a_2 \cdots a_{2^N}\rangle \overset{Measuring}{\rightarrow} |b_1 b_2 \cdots b_{2^N}\rangle \Rightarrow [0\ to\ 2^N - 1] \tag{1.4}$$

In which a_i is a complex number while b_i is a bit.

1.3 Elaboration with qubit

Once presented qubit the next step is explain how to implement functions working with qubit. As a quantized magnitude, qubit respond to Schrödinger equation $i\hbar\frac{d}{dt}|\Psi(t)\rangle = H|\Psi(t)\rangle$, if we call Ψ_f the final state and Ψ_0 the initial state, the synthesis of a general function f is equivalent to searching a operator U that satisfies the following equation:

$$|\Psi_f\rangle = exp\left(-\frac{i}{\hbar}\int H dt\right)|\Psi_0\rangle = U|\Psi_0\rangle \tag{1.5}$$

[2]In a classical computer with N bit the numbers of possibility state are 2^N

In which H is the Hamiltonian, the equation 1.5 has solution as long as the operator U is unitary and this happens only if the function f that simulate U is reversible [6], as example AND function is not reversible because starting from the results is not possible to calculate the input values; only reversible function can be synthesize in quantum systems.

Now it's possible to appreciate and understand the powerful of parallelism in quantum computing elaboration, in fact considering the following superposition of n qubits:

$$\frac{1}{\sqrt[n]{2}} \sum_{i_1,i_2,...,i_n=0}^{1} |i_1, i_2, ..., i_n\rangle \tag{1.6}$$

This is the uniform superposition because all states have the same probability, now if we apply the function f due to the linearity of equation 1.5 we obtain:

$$\frac{1}{\sqrt[n]{2}} \sum_{i_1,i_2,...,i_n=0}^{1} f\left(|i_1, i_2, ..., i_n\rangle\right) \tag{1.7}$$

so in one step we had applied the function f to all the 2^n combinations; this is a great improvement due to parallelism, but this not lead directly to a exponential improvement in computational power because as yet noted, when is needed to extract the information from the quantum system is required to measure the system and this leads the collapse of the wave-function, this causes the lost of the parallelism. The parallelism shows his power when joined with another feature of quantum system that is *interference*, the basic idea is to provoke destructive interference of wave function in that states that are not in out interest and focus on states interested to remain. The combination of parallelism and interference gives to quantum computation his great improvement versus standard computation.

1.3.1 Quantum gate

Once show the overview of quantum elaboration we're going into detail showing how quantum algorithms works and which requirement are needed to do so, in fact according to Loss and Di Vincenzo [7] it's possible to find five requirement for a usable quantum computing system:

Well defined qubit Identify usable physical quantum magnitude as qubit.

Initialization of qubits This is related to the capability to control qubits for set-up a particular elaboration.

Relatively long decoherence times Decoherence time must be at least longer than gate operation time.

A qubit-specitic read-out capability This is related to the capability to read a qubit stored in someway.

A universal set of quantum gates Capability to implement a complex functions on qubit.

Probably the most obscure points are: what is decoherence and what is a universal set of quantum gate. A quantum gate is the equivalent of gate in standard digital elaboration; it's a system with can elaborate qubit applying on them a function.

An example of simple quantum gate is NOT gate, in a similar way than standard gate it swap the coefficient of $|0\rangle$ e $|1\rangle$ of a general qubit $|i\rangle$. It's possible to denote $|0\rangle$ as the vector (1 0) and $|1\rangle$ as (0 1) and, in general, a qubit $|i\rangle$ with $(a\ b)$ in which a is the projection of $|i\rangle$ on basis $|0\rangle$ and b on basis $|1\rangle$, using this formulation a NOT gate can be represented as a 2x2 matrix:

$$NOT = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$$

and the output of NOT gate, when in the input there is the qubit $\mathbf{x}$=$(a\ b)$ is NOT matrix right-multiplied $\mathbf{x}$. Since for all qubit, both in input and in output of a quantum gate, must be verified the relationship:

$$\sum_{i=1}^{2^n} |a_i|^2 = 1 \tag{1.8}$$

matrix characterizing a quantum gate must be a unitary matrix or rather the condition $U(U^*)^T = I$ must be satisfied.

1.3.2 CNOT and 2-qubit gates

A system composed with 2 qubit is characterized by 4 complex number for each base $|00\rangle$,$|01\rangle$, $|10\rangle$,$|11\rangle$. A 2 qubit quantum gate matrix is a 4x4 matrix, in general a gate working on N qubit has 2^N x 2^N matrix dimensions. A very important quantum gate is Controlled NOT gate (CNOT), it's a 2-bit input gate which compute the function $(a, b) \rightarrow (a, a \otimes b)$ where a and b the input qubit and $\otimes$ is the standard XOR function. CNOT can be represented by the matrix 4x4:

$$CNOT = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix}$$

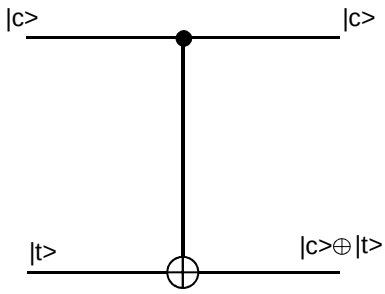

Figure 1.1: Representation of CNOT quantum gates, if the control qubit $|c\rangle$ is $|1\rangle$ the target qubit ($|t\rangle$) is inverted, otherwise remains unaltered

this gates on a standard bit applies a NOT on the second bit (called target) if the first bit (control) is 1 otherwise keep the same value it corresponds to XOR classical gate. This gate is also represented graphically like in figure 1.1.

Can be curious that control bit is an input but also an output, this is because XOR function is not reversible but only reversible function can be transformed into quantum gates (refer to section 1.3), but is easy to transform a irreversible function into reversible function by writing down in output the input qubits instead of erasing them.

Quantum gate can perform more complicated function than standard computation gates, like the following gate that applies a general rotation to a qubit:

$$G_{\theta,\phi} = \begin{pmatrix} cos(\theta) & sin(\theta)e^{i\phi} \\ -sin(\theta)e^{-i\phi} & cos(\theta) \end{pmatrix}$$

Another very useful quantum gate is Hadamard gate it's a 1 qubit gate:

$$H = \begin{pmatrix} 1/\sqrt{2} & 1/\sqrt{2} \\ 1/\sqrt{2} & -1/\sqrt{2} \end{pmatrix}$$

When Hadamard gate is applied on $|0\rangle$ or $|1\rangle$ qubit his result is $1/\sqrt{2}\,(|0\rangle \pm |1\rangle)$ it's a random qubit because each state has the same probability to being measured, so with quantum computation it's possible not only to simulate standard computation but also probabilistic standard gate. Once defines the quantum gate it's possible, by succession of gates to perform the synthesis of algorithms in order to compute the requested function, in section A.3 will be shown some example like shor's algorithm for factorization of integers.

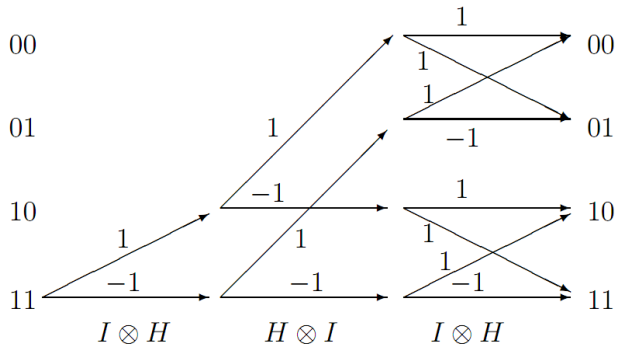

Figure 1.2: Interference on quantum algorithm: Applying the operator H thrice on a initial state $|11\rangle$. Final state $|11\rangle$ and $|00\rangle$ have probability 0.5 while $|01\rangle$ and $|10\rangle$ have probability zero, due to constructive and destructive interferences

1.4 Improvement from quantum computing

After presenting the principles of quantum computing is possible to go ahead with synthesis of quantum algorithm as show in appendix A where it's proved that quantum computing is able to solve algorithm that seems hard or impossible to do efficiently with classical machines [8]; thanks to superposition and interference. In figure 1.2 we can represent quantum computing elaboration from another point of view, we start with two qubit in state $|11\rangle$ then the Hadamantard gate is applied thrice; the arrows represent all the possible final and intermediate transition, the numbers near the arrow represent the coefficient of the transition (1 is $1/\sqrt{2}$ and -1 is $-1/\sqrt{2}$). The probability to arrive in a final state is calculated by multiplying all the coefficient in a path and adding those of parallel paths; notice that the final states $|10\rangle$ and $|01\rangle$ have a weight 0.

If on the other hand we use a stochastic matrices[3] R instead of the quantum gate H; every arrow has 0.5 coefficient and every final state has a 0.25 probability to happen. Quantum computation is not powerful because it has exponential parallelism, with n particles the vertical axis will run over 2^n possible classical state, in fact this is also true in the diagram of stochastic computation on n bits. There are two difference between quantum gates and stochastic gates: stochastic gates have only real positive number while quantum gates has positive and negative number; the other difference is that the quantum gates are unitary gate and so preserve the L_2 norm of vectors, while stochastic gate preserve L_1 norm. Negative number are important because

[3] A stochastic matrix is a matrix in which every columns are probability distributions and so every element is a positive real

permits to the different path to cancel each other as we can see in algorithm presented in appendix A; in the algorithms interference has a central role in quantum computing, because it cancels the "bad" answers; in probabilistic case the cases this do not happens.

Probabilistic has the power of exponentiality but not interference, on the other way optical computation has interference but doesn't exhibit exponentiality. It's only quantum computation which combines the two features of exponentiality and interference.

1.5 Limit of quantum computing

After presenting the improvements of the science of quantum computing, we show the limit of the quantum model, in particular quantum computation can not solve problems that are unsolvable with classical computing but can solve problem with polynomial cost instead exponential cost, so more efficiently; this is due to the fact that a classical computer can compute the coefficients of the superposition and simulate it; this will take a exponential time but at the end a classical computer can solve anything which can be done quantumly. The only difference between classical and quantum computation lies in the computational cost.

Also the parallelism of the function is not a exponential advantage; in classical computation in one step we can know a value of a bit; into quantum world we can call the function with the following unitary transformation:

$$|i\rangle|0\rangle \rightarrow |i\rangle|f(i)\rangle \tag{1.9}$$

in this way with only one step we have all possible value of function $i \rightarrow f(i)$, but this not correspond to exponential advantage, due to measurement information destruction; moreover it has been demonstrated that in N qubit lies only log(N) bit of information [9], and also Bennett et al. [10] demonstrated that to apply a OR gate on N qubit we need $O(\sqrt{N})$ call to function.

We can conclude that if the acquisition of the input is the bottle neck in classical computation, quantum algorithm has quadratic advantage over classical algorithm; this is the case of search in a unsorted database quantum algorithm by Groover [11] that need $O(\sqrt{N})$ queries instead of N of classical algorithm (see appendix A). If the bottle neck is the processing, like in case of factorization of integers then quantum algorithm can have exponential advantage.

Quantum computing does not achieve better performances in term of precision respect to standard computing, but it solve problem with polynomial cost that today are still not computable in reasonable time. Other application for

quantum computing can involve the solution of class NP problem [12] or the simulation of physical systems [13]. We suppose that in all computation step there were no errors; but this can not be possible, in appendix A is presented the effect of error on quantum computing.

1.6 Quantum dot

In this section we present the quantum dot used for spin-based quantum computing. Electron spin is a good quantum number, because, given an operator O his eigenvectors remain an eigenvector of O with the same eigenvalue as time evolves; and is one of most used method to implement a qubit [14]. Has been developed other method: in2001 IBM built a computer with 7 qubit using nuclear spin of a single molecule, also hybrid quantum computing has been proved [15] by entanglement between photon and spin qubit, allowing to use different carrier for qubit and adapting it to different needed.

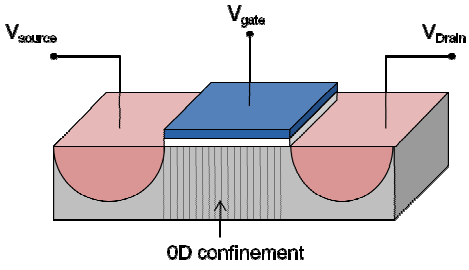

Figure 1.3: Mos structure for a quantum dot, the small dimensions of channel lead a discrete energy spectrum due to quantistic confinement. Measuring the current flowing in it is possible to extract information to single electron behavior

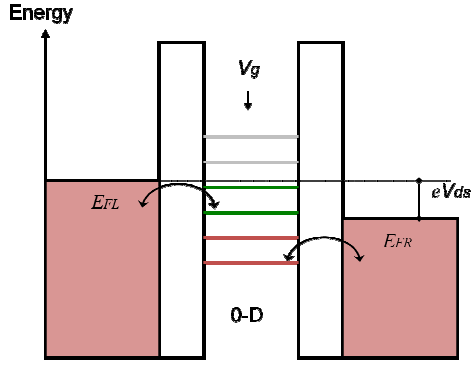

Figure 1.4: Energy spectrum of Mos structure, drain and source has standard behavior while the channel has discrete energy level, and is separated by high barrier from source and drain

Now we start analyze quantum dot spin-based method [16]; mainly because it's based on well know mos transistor structure common in cmos technology. Different materials have been used, in particular GaAs [17] and silicon [2]. A qubit is implemented as a electron spin in a semiconductor; spin up is $|1\rangle$ and spin down is $|0\rangle$, for studying spin is important to detect the status of just one electron, for this purpose quantum dot satisfy the requirement because the

three dimensional quantic confinement leads a discrete energy level behavior in the spectrum of energy (see appendix C). The energy level in quantum dot can host one electrons. The base structure of this kind of quantum dot is a well-known Mosfet showed in figure 1.3 and the consequent energy level spectrum is in figure 1.4, source and drain can be assumed as metal due to his doping; while the channel has discrete levels due to confinement.

Between the dot and the leads there are barriers and electrons can tunnel in it with a certain probability. The gate voltage is capacitive coupled with energy in the dot levels in quantum dots, when we apply a voltage V_{DS} between drain and source in energy diagram we misalign the Fermi level in source and drain by a quantity $-eV_{DS}$ in this case if a level is present in this window (the green levels in fig. 1.4)it's possible to obtain a flux of electron from drain to source due to electrons goes from source to the dot and then they tunnel to the drain (fig. 1.5 b); when raising the V_{GATE} the energy level $\mu(n)$ goes below Γ_D and the current blocks because there are no energy levels inside the bias window and one more electron is blocked inside the quantum dot.

When we fix V_{DS} is a small value that only one energy level of dot can lies in bias window and sweep V_{GATE}; we obtain a peaked current corresponding to the energy diagram of the dot(Fig 1.5 c). This phenomenon is called Coulomb blockade [18] because the Columbian repulsion of the new electron blocked into quantum dot blocks the current until the next level is sufficiently tied down.

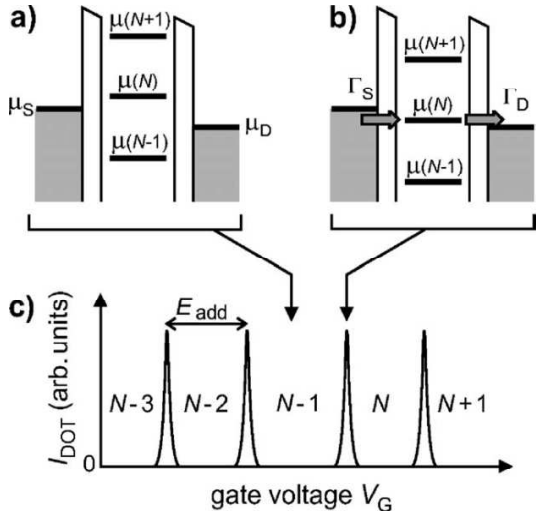

Figure 1.5: In case a) There are no current since there are no available energy level between source and drain fermi energy levels. In case b) There are a current flowing from source to drain thought the level $\mu(N)$. In c there is a typical I-V to each energy level corresponds one peak

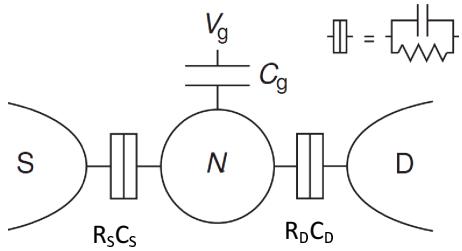

Figure 1.6: Equivalent scheme of a quantum dot; the leads are coupled to quantum dot via two impedance R_DC_D and R_SC_S and gate terminal is capacitive coupled to the dot via the capacitance C_G

The circuital model for the quantum dot is presented in fig. 1.6. The dot is coupled to the gate by capacitance C_G and with reservoir (source and drain) also with a resistor that model the tunnel between lead and dot. The total capacitance view by dot is $C = C_D + C_S + C_G$ and the total energy in dot is:

$$U(N) = \frac{[|e|(N - N_0) + C_S V_S + C_D V_D + C_G V_G]^2}{2C} + \sum_{n=1}^{N} E_n(B) \qquad (1.10)$$

where $N_0\|e\|$ is the term compensating the positive charge due to donors in structure and B is magnetic field. We calculate the electrochemical potential $\mu(E)$:

$$\mu(N) = U(N) - U(N-1) = \left(N - N_0 - \frac{1}{2}\right) E_C - \frac{E_C}{|e|}(C_S V_S + C_D V_D + C_G V_G) + E_N \qquad (1.11)$$

where $E_C = e^2/C$ is the charging energy, the electrochemical potential is the energy needed to add en electron on dot. We also define the addition energy $E_{ADD} = \mu(N+1) + \mu(N) = E_c + \Delta E$ as the charging energy plus the energy spacing between levels. By keeping V_{DS} sufficiently low to contain only one level at once the distance between peaks in fig. 1.5 correspond to E_{ADD} the addition energy requested to capture one more electron inside the dot.

1.6.1 High bias

When the voltage bias V_{DS} is big enough that more than one energy level are at the same time inside the window between source and drain energy levels, different levels can participate to the transport of electrons. If N-1 electrons are in the dot and the ground state N (GS(N)) is inside the bias window and the bias is increased that also the excited level N (ES(N)) can enter in the window. As result there are two path for electrons and the current increases;

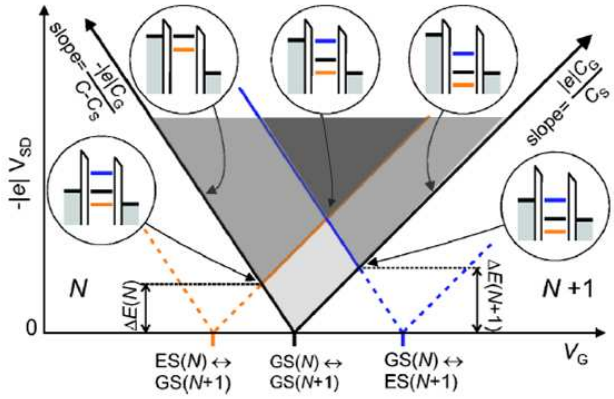

Figure 1.7: Graph of current in quantum dot in function of bias voltage V_{DS} and gate voltage V_G depending on how many levels there are in bias windows; there can be different path for electron tunneling from source to drain, resulting in increase in current (gray scale).

in fig. 1.7 there is the current in function of V_{DS} and V_G; the slopes of the V shaped figure are the point in which changing gate voltage and source voltage, the energy level of the dot remains in the same value; the slope becomes equal to $\delta V_S/\Delta V_G = C_G/(C - C_S)$. The 2D measurement of the current in function of the voltages is called *stability diagram* of the quantum dot. Different information can be extracted from it like ratio of capacitance from slopes and ΔE_N and ΔE_{N+1} from the points in which the lines of excited level touches the V-shape. Outside the V-shape the current is zero and this is called Coulomb blockade region.

In fig. 1.8 there is a measurement of a stability diagram, taking using the model in fig. 1.6 the negative slope of the diamond is equal to $-C_G/C_D$ the positive is $C_G/(C_S+C_G)$ by summing the inverse of these two slope we obtain $C_D + C_S + C_G/C_G = 1/\beta$ that is the inverse of the conversion factor between energies in quantum dot and gate voltages $\Delta E = e\beta\Delta V$ once calculated is easy to convert voltages in stability diagram into energies.

1.7 Spin in quantum dot

In this section we present the methods to get information about spin of electron in a quantum dot. Pauli's exclusion principle avoids that two electrons with same spin occupy the same orbital; but in each state two electron can be hosted only if they have opposite spin. The spin level degeneration can be broken via zeeman effect allowing to fix the spin on a certain energy levels.

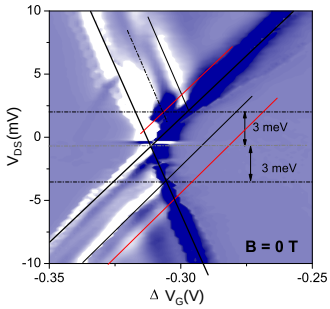

Figure 1.8: Measurement of a stability diagram, from slopes can be extracted the factor $\beta = C_G/(C_G + C_S + C_D)$ to convert voltages into energy by the relationship $\Delta E = e\beta\Delta V$. In Z coordinate is plotted the differential conductance dI/dV

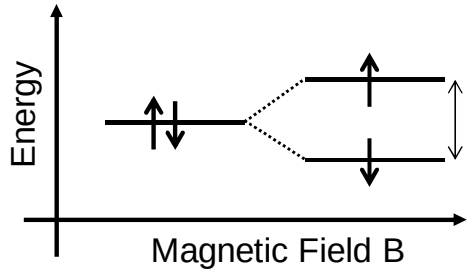

Figure 1.9: Zeeman Effect, under a magnetic Field B the energy levels can spit each other and the spin degeneration has broken; each level has a well defined spin.

1.7.1 Zeeman Effect

Zeeman effect is the separation of energy levels due to magnetic field. In particular under magnetic field the Hamiltonian of the system becomes:

$$H = H_0 + V(M) = H_0 + \left(-\vec{\mu}\cdot\vec{B}\right) = H_0 - \left(\frac{-\mu_B g\vec{J}}{\hbar}\right)\cdot\vec{B} \tag{1.12}$$

H_0 is the impertubated Hamiltonian, μ_B is magneton's Bohr, g is a constant called g-factor $\vec{J}$ is the angular momentum that is the sum of orbital angular momentum $\vec{L}$ and spin angular momentum $\vec{S}$ $\vec{J} = \vec{L} + \vec{S}$ in which the orbital angular momentum is usually negligible respect to spin. The new available energy states can be calculated from the eigenvalues of:

$$H\psi(x) = E\psi(x) \tag{1.13}$$

and result $E = \mu_B g m_j B$ we called m_j the magnetic quantum number ($\pm 1/2$). Intuitively under a magnetic field there is a preferred direction for spin that direction has less energy than the opposite; in fig. 1.9 there are the representation of zeeman effect, the level splits in two each with a specific spin. The g-factor is a well fixed constant that depends on material, in silicon his values is 1.998 in GaAs is -0.4.

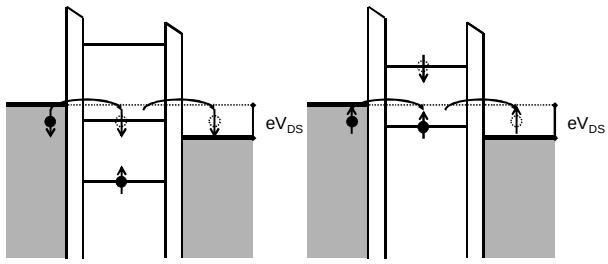

Figure 1.10: Spin filter, in a quantum dot under a magnetic field it's possible to use Zeeman Effect to filter the spin of carriers, if only one level is involved in conductance, it's possible to choose which spin direction to filter by changing the gate voltage until the other level is inside the bias windows.

Spin Filter

Quantum dot can act as a spin filter thanks to zeeman effect(fig. 1.10), because if the bias voltage is so little that only one of the two splitted energy level can enter in it, the conduction involves only this level and so only electron having a spin compatible. By tuning the gate voltage is possible to change the level inside the window and so change the spin of the electron involved in conduction.

1.7.2 Spin and Pauli's exclusion principle

Spin behavior in a quantum dot must observes Pauli's exclusion principle. According to Pauli's principle any orbital can be occupied by at most two electron with opposite spin. When we add a electron to a dot, by raising the gate voltage the new electron can move to an empty orbital or to an already occupied orbital: in first case the electron will occupy the level whatever will be his spin (except if the zeeman effect has happen), if the electron goes to an already occupied orbital he must have the opposite spin than the present electron.

1.7.3 Two electron spin state

Consider a ground state with two electrons, for the Pauli's principle they have opposite spin and so the total spin quantum number S is 0 when this happen the state is called singlet state, their wave-functions are antisymmetric and $|S\rangle = (|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle)/\sqrt{2}$. The excited states are the spin triplets (S=1), where the antisymmetry of the total two-electron wave-function requires one electron to occupy a higher orbital. The three triplet states are degenerated at zero magnetic field, but acquire different values under magnetic field because

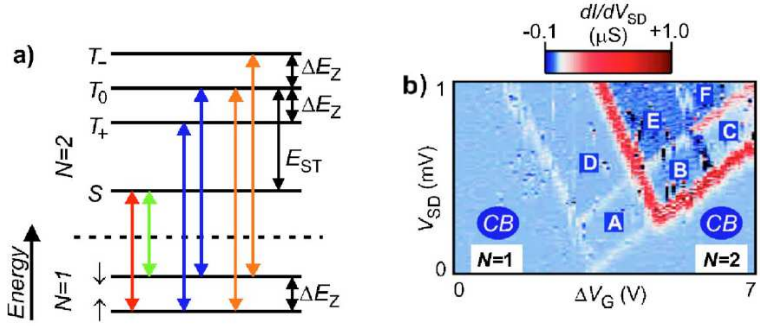

Figure 1.11: (a) Energy diagram of transition N=1 to N=2 under Zeeman splitting: two more exited energy level appears; the transition $\uparrow \leftrightarrow T_-$ and $\downarrow \leftrightarrow T_+$ are suppressed by spin blockade since they need more than S=1/2 of spin change (b) measure of stability diagram under Zeeman more region appears correspondently to new exited levels.

their spin z components differs: $S_z = 1$ for $|T_+\rangle = |\uparrow\uparrow\rangle$, $S_z = 0$ for $|T_0\rangle = (|\uparrow\downarrow\rangle + |\uparrow\downarrow\rangle)/\sqrt{2}$, and $S_z = -1$ for $|T_-\rangle = |\downarrow\downarrow\rangle$ so their zeeman effect is different T_- increase his energy under magnetic field, T_0 remains constant, T_+ decrease. In fig. 1.11 there is the energy level for a single electron (N=1) and two electron (N=2) for a quantum dot under a splitting Zeeman ΔE_Z the level T_+ is split down from his 0T position T_0 and T_- is split up; E_{ST} is the energy difference between singlet state and triplet state.

1.8 Double quantum dot system

In section 1.3.1 we present the request for a quantum computer, one of this is the availability of a universal set of quantum gate, according to [19] it's possible to implement a universal set of quantum gate with 2 qubit gate; so double dot systems are needed to implement a 2 qubit gate. The dot can be implement in different in series or in parallel, when in parallel the resulting current is the sum of the current flowing in each dot, while in series a strong cooperation of dot is fundamental to permit conduction. The equivalent scheme two series quantum dots is shown in fig. 1.12, a conduction is possible only if electron flows from a lead to both dots, that are couplet capacitively to the correspondent gate voltage by C_{G1-2} and to the leads by C_{D-S} also the dots talk each other thought the capacitance C_m. The resistances model the tunnel conductivity. The diagram V_{G1} V_{G2} versus current I_D has different behavior depending on C_m.

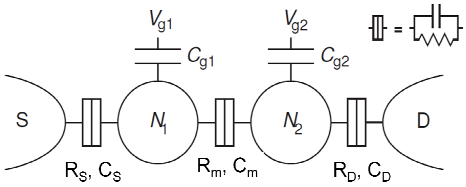

Figure 1.12: Model of a series double dot: for conduction each electron must pass through both dot, tunneling is modeled as resistors

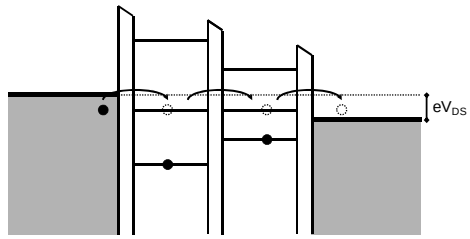

Figure 1.13: Energy spectrum in a series double dot, there are conduction only if two level of both dots are in the bias window and are aligned

1.8.1 Small bias in double dot

Double dot systems are quite complex than the single dot, we start analyzing the case we have a bias smaller than the distance between levels, in this case only one level at once can be in the bias window, suppose $C_m = 0$ so each gate voltage control only the energy levels of his own dot. We can only have current if in both dots there are one level in bias window (fig. 1.13). In fig. 1.14 *a*) there is the so called charge stability diagram, it's a current 2D diagram in function of V_{G1} and V_{G2}, the orthogonal lines identify the region where a dot has an aligned energy level in bias windows; the crosses are the region in which both dots have an aligned level and so they are single point that allow conduction; changing the number of electron in dot 1 or changing his gate voltage don't lead modification on dot 2.

When C_m is increased the lines losses her orthogonality as every change on one dot affects also the other dot; the crosses are split in two 3-way cross called triple point (Fig. 1.14 b), as consequence the square becomes hexagon, in triple point the energy levels are in resonance and conduction happens. Referring to figure 1.12 it's possible to calculate the electrochemical potential for dot 1 defined as follow:

$$\begin{aligned}\mu_1(N_1,N_2) &\equiv U(N_1,N_2) - U(N_1-1,N_2) = \\ &= \left(N_1 - \frac{1}{2}\right) E_{C1} + N_2 E_{Cm} - \frac{E_C 1}{|e|}\left(C_S V_S + C_{11} V_{G1} + C_{12} V_{G2}\right) + \\ &+ \frac{E_{Cm}}{|e|}\left(C_D V_D + C_{22} V_{G2} + C_{21} V_{G1}\right)\end{aligned} \tag{1.14}$$

where C_{ij} is the capacitance between gate j and dot i, E_{Ci} is the charging energy of the individual dot i, E_{Cm} is the electrostatic coupling energy defined

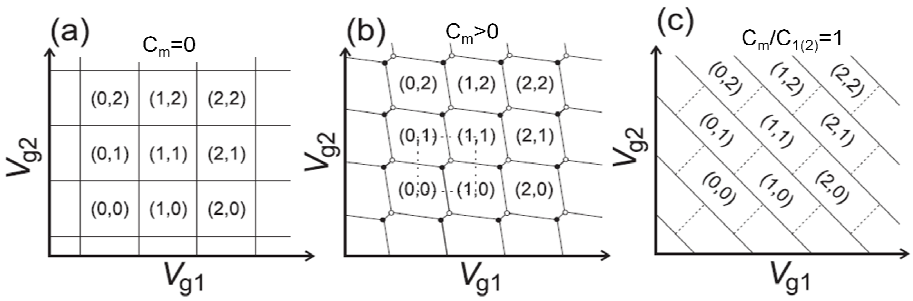

Figure 1.14: $V_{G1} - V_{G2}$ Graph for double dot: (a) case with no inter-coupling between dot; the current happens only in square crosses. (b) case medium intercoupling: two triple point appear instead of single cross. (c) case with dominant inter-coupling between dots: electrons are shared between dots only the gain and the losing of electron are noticeable not inter-dots changing.

as the changing in energy of one dot when the other gains one electron. From the measured diagram in fig. 1.14 it's possible to calculate the capacitances of double dot system. When the inter-dot capacitance C_m is the dominant term in total dot capacitance, the interaction between dots is very easy and the electron is no more localized into one dot but becomes distributed, according to his wave-function, into both dots, the continuous straight line in fig. 1.14 c, are the point in which the double dot structure gain or lose one electron, they are -45° degrees because each gate acts in same way on structure; the dotted lines identify the inter-dot electron managing, in this case is less marked as electrons are shared between dots.

High bias

In the previous section the voltage V_{DS} has been neglected, but in a real measure using a small bias can reduce the amplitude current reducing the SNR. When the voltage bias is increased the bias window E_{DS} can be comparable to energy spacing; as consequence resonance condition is not more punctual but there is region in V_{G1} V_{G2} diagram that allow conduction. In particular triple point in fig. 1.14 b, becomes the triangles in fig 1.15 there is a magnification of couple of triple points the triangles appears when increasing bias, to obtain conduction the energy level of dot must be aligned [4] but can be aligned in all points of bias windows, this corresponds to marked edge of triangles; if an excited level enter into bias window, in triangles appears another conduction

[4]Is not possible for an electron in a dot to tunnel in other dot with lower energy level also if energetically favorable due to the conservation of energy, a phonon can take the excess of energy but is less probable a phonon interaction

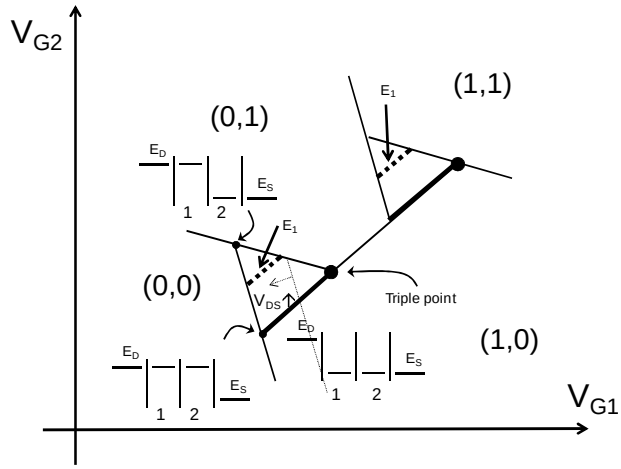

Figure 1.15: Current diagram in function of gate voltages. When the bias voltage is increased the triple point becomes triangles, the current flow in the marked side of triangle and in dotted side if an excited level enter into bias window.

line (E_1 in fig.1.15) by the analysis of graph is possible to calculate the capacitances [20]. There are also second order effect like inelastic process that allow conduction if the level of dot are misaligned, due to emission of a phonon or photon [21]; this cause a weak current in all triangle's area.

1.8.2 Spin Blockade

Spin blockade or Pauli spin blockade is a rectification of current due to electron spin, it can be used to measure a spin. We take a double dot structure and we apply the gate voltage waveform that allow this cycled state: $(0,1) \rightarrow (0,2) \rightarrow (1,1) \rightarrow (0,1)$; the second dot acquires a second electron, it transfers to first dot and than to lead. The electron entering from drain on second dot must have the opposite spin respect to already present electron for Pauli exclusion than he goes to source thought the first dot. During this gate operations the drain voltage is swept from negative to positive voltages. In case of positive voltages an electron goes from source to first dot with an certain spin, once in the dot can form a singlet(1,1) or triplet(1,1) state with the electron in dot 2, during inter-dot interaction the total orbital moment must be preserved so singlet state (1,1) can becomes singlet state (0,2) while triplet state(1,1) becomes triplet state (0,2); but triplet (0,2) is at higher energy respect singlet (0,2) so the current in case of triplet state will stop, this is the spin blockade effect (Fig. 1.16).

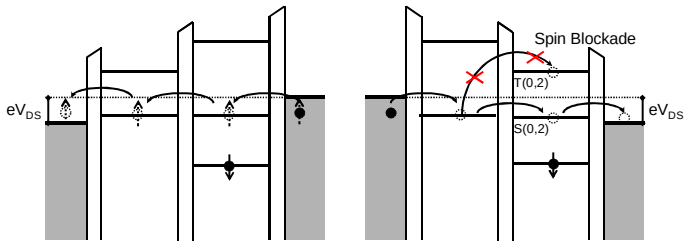

Figure 1.16: Spin blockade effect: drain voltage is continuously changed, for negative bias (left figure) there is a spin filter effect but the current never stop. For positive bias, if the entering electron does a triplet state the current blocks because triplet state (0,2) is at higher energy than singlet state and is higher than bias

1.9 Measurement on quantum dots

Once presented the structure and the analyzing method for one and double dot system, we continue presenting two example of measurement on quantum dot; one is the read of spin in quantum dot obtained with two different techniques and a co-tunnelling current measurement it's a second order effect due to Heisenberg uncertainly principle.

1.9.1 Reading a spin

Qubit measurement is one of the requisite for the synthesis of quantum computer in 1.3.1, this are done on GaAs by charge sensing [22], and also in silicon with a current inhibition analysis. One of these it the one propose in [23] using a spin selective coulomb blockade region.

It's is based on a quantum dot and a donor near the dot, the electron can move by tunnel between dot and donor but only if it is in the dot can participate to conduction. A magnetic field is applied to spit energy level od donor according to zeeman effect; the quantum dot is tuned in way that if one electron is in it there is current otherwise coulomb blockade leads zero current. The measurement process is composed by 3 main phases: load, read, empty (fig. 1.18). In load phase the gate voltage is at -5mV and this result that level into donor are below the level of dot, so one electron goes to the donor; in the second phase the gate voltage is swept from up to down levels of dot interact with levels of donor when the lower donor level is aligned with dot level. When the dot level is in the middle of donor levels two situation can overcome: if the electron in donor is spin down no conduction is allowed because he can't pass to dot, if he's spin up he can pass temporary to dot due to inelastic process and and lead a finite drain current until another inelastic interaction moves

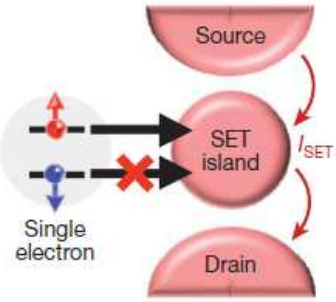

Figure 1.17: Structure for measure a spin, an electron from donor (single electron) can move into set island only if he has a spin up. His presence is detected by measuring the drain current.

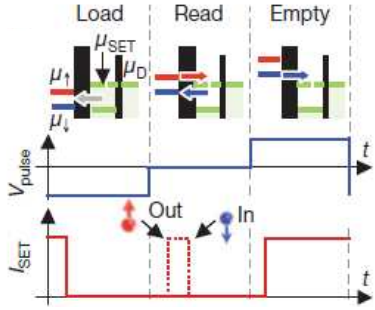

Figure 1.18: Measurement of spin: in load phase donor is loaded with one electron, in read phase the electron pass to the dot and than returns to donor only if he has spin up otherwise remain in donor, in empty phase the electron leaves donor.

again electron into donor at lower energy. We saw a current pulse when spin up and zero current for spin down. The relaxation processes are not so fast due they depends on inelastic process they need another particle to overcome, they can be detected by measuring the current. With this method a fidelity of more than 90% has been achieved [23].

Charge sensing

Quantum dot based on charge sensing are characterized by a quantum dot that do not participate directly to main conduction, but affects electro-statically a near conduction channel [24].

In figure 1.19 there is the double dot structure is defined by gate L, R, T, M and they are tuned by P_L and P_R. The presence of electron in one dot affect the current in I_{QPC} by measuring the difference with left current and right current is possible (I_{QPC}) to calculate the current inside dot; I_{QPC} is also affected by the charge changing in one of dots, this is reflected in fig 1.14 b because not only the triple point but also the edge of hexagons is visible (fig. 1.20).

In charge sensing technique there are some limitation, we must be able to detect a small current signal on a big current baseline and moreover the structure requires a fine tuning of dot barriers obtained with a lot of gates; while in standard technique with only 2 gate it's possible to manage up 3 dots structures [25].

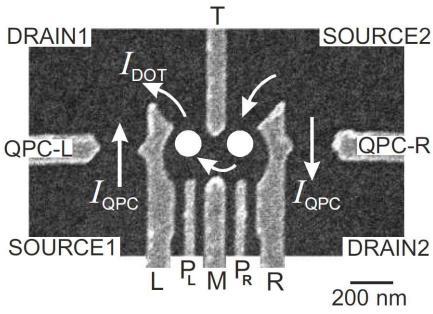

Figure 1.19: Double dot structure for charge sensing: the currents from drain 1(2) to source 1(2) is affected by status of dot 1 (2). Gate T in combination with L(R) define the coupling between dot and lead, M define the coupling between dots, $P_L(P_R)$ tunes the electrostatic potential of dot 1(2).

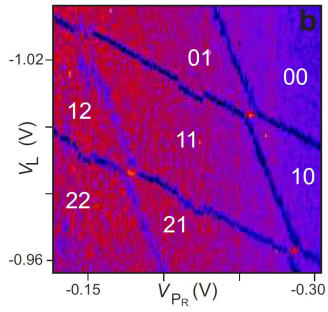

Figure 1.20: Measurement of charge stability diagram: with charge sensing is also visible the edge of the hexagon not only the triple point because every change in charge inside dots leads a change in current

1.9.2 Cotunneling

Co-tunneling is a very interesting measure on quantum dot already done on GaAs structure [26] but not on silicon; we take a single quantum dot and we measure the stability diagram. Inside the coulomb blockade region of N=1 we saw a little current step (fig. 1.21); in this region should not be current because no energy level are in the bias windows only excited level (N=1) may be present but as his correspond ground level N=1 is full, it is not accessible. In fig. 1.21 there are the stability diagram of single dot structure, in A region both ground state and excited state are responsible of conduction, in C region neither ground or excited level can conduce because they are outside the bias window. In B region ground state is full of an electron and excited state although is inside the bias window should not conduce because it's unaccessible; but he does thanks to Heisenberg principle.

The Heisenberg uncertainty principle is a fundamental limit on quantum physics, certain observable can not measured simultaneously with infinite accuracy, but the product of his accuracy must be higher than a certain constant, a typical example is position and speed of an electron. There are also a Energy-Time version of the principle that is:

$$\Delta E \Delta t \geq h \tag{1.15}$$

in which h is Plank constant, so for very small time energy are undetermined.

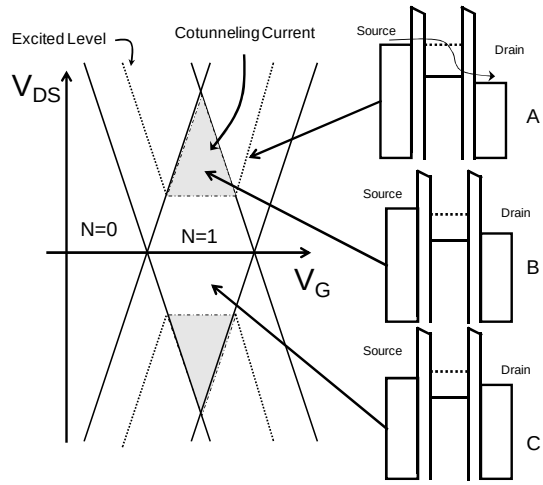

Figure 1.21: Co-tunneling Current: In the gray region there are a small increase in current due to co-tunneling effect, this happens when only an excited level is inside the bias windows, as his ground state it's full, he should be accessible; but thanks to Heisenberg indetermination time-energy some electrons can pass through it.

So let concentrate in region C in fig. 1.21, for very small time the electron on ground state has an uncertain energy and may be possible that he jumps on drain also if thermal energy do not allow it, then one electron can go from source to excited state now available and then to drain, this until an electron goes fall into ground state. The Heisenberg process cannot create energy, in fact in our system the energy is conserved between initial and final state but not in the middle. In figure 1.22 there are a measure of co-tunneling current on quantum dot in GaAs.

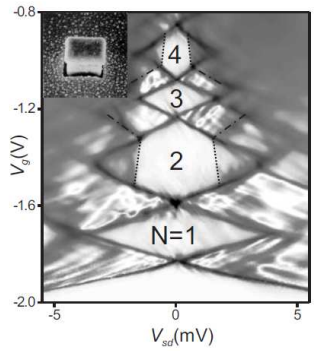

Figure 1.22: Measure of co-tunneling effect in GaAs quantum dot. [26]

1.10 Conclusion

In this chapter was presented the quantum computing principles showing possible improvement. Than we presented the quantum dot structure that are one of the most used structures to implement a quantum gate, showing the typical measurement. In the next chapter we'll present a set-up for measurement on quantum dot, and we will proceed with the design of a low-noise electronic amplifier for measurement on quantum dot.

Chapter 2

Electrical measurement on quantum devices

In this chapter we'll present our design of set-up for studying quantum dots. We start presenting the conditions to make possible to measure of quantum dot, then we present the specification in terms of resolution and bandwidth for current measurement, we continue with the design of a high performance instrument optimized for our setup and adaptable to different measurement operating at room temperature. The analysis of quantum dots concerns the measure of the current in a mos structure, we proceed with the design of a transimpedance amplifier that translate current signals into voltage signals read in our system thought a commercial acquisition system by national instrument.

2.1 Cryomagnet

The advance of using quantum dot is the capability to obtain a current that strictly depends on properties of just one electron; this thanks to discretization of energy spectrum of the channel in a ultra-scaled mosfet structure. The thermal energy kT must be smaller than energy spacing on quantum dot and zeeman effect whose the spacing is $\Delta E = \mu_B g B$ where $\mu B = 9.27 \cdot 10^{-24} j T^{-1}$ is Bohr's magneton and g is a constant that in Silicon is 1.998, for a magnetic field of 10T the energy spacing is 1.16meV, at 300K the thermal energy is 25meV it's many times bigger. For example in these condition it's impossible to see any kind of quantum effect because the electrons are able to jump to higher level. Concluding it's mandatory for these kind of investigation the use of a cryomagnet allowing both cryogenic temperature (below 1K) and also high magnetic field (over 10 T).

We use a ^3He cryomagnet from cryogenics, a simplified scheme is in figure

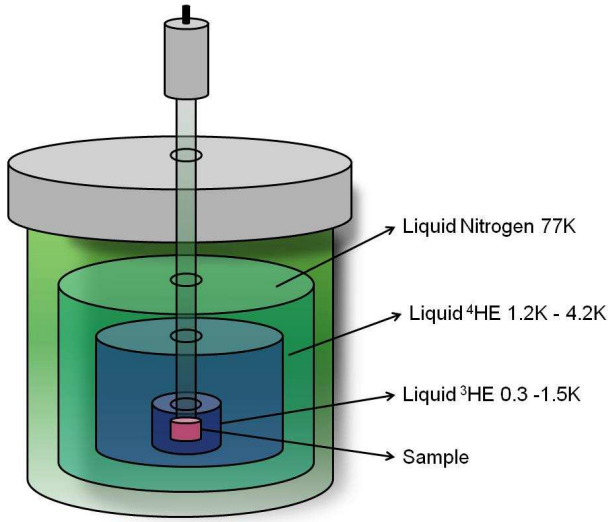

Figure 2.1: Simplified scheme of cryostat, there are different region: Nitrogen liquid, Helium 4 liquid and Helium 3 liquid; the sample can reach up 0.3K and 12 T

2.1. The sample is kept at 0.3K surrounded by different zones isolated by vacuum, an external donut shape region fulled by nitrogen liquid is used for block irradiation from external environment, the region of liquid Helium 4 is used to isolate the internal zone from 77K irradiation, to keep the superconductivity of magnet and it is used also to liquefy the Helium 3. The 0.3K is reached when Liquid Helium 3 is de-pressurized. The sample is inside the helium 3 zone attached on a probe that provide electric connections. The entire system is very complicate and quite big, the height of the structure is about 2 meters so also the cable between the sample and the read-out electronics are quite long about 4 meters, reducing the performance of the electronic instrumentation as shown in section 2.2.

2.2 Transimpedence amplifier

A transimpedance amplifier is the most used circuit to detect a current because thanks to feedback it's be able to fix very precisely the voltage bias on device under test and measure the current without the need to charge the capacitance of wires that may affected the measurement in other topologies like measuring voltage across a series resistor. In figure 2.2 there is a transimpedence amplifier's schematic; the input current flow thought the feedback resistor, if the gain of opamp is bigger than 1, the negative feedback brings

the inverting terminal of operational amplifier almost at zero voltage like non inverting terminal, so the output voltage becomes $-R_F I_{IN}$ proportional to input current; this voltage can be then digitalized and elaborated in a computer. The capacitance C_{in} is between ground and virtual ground and ideally not affect the measurement.

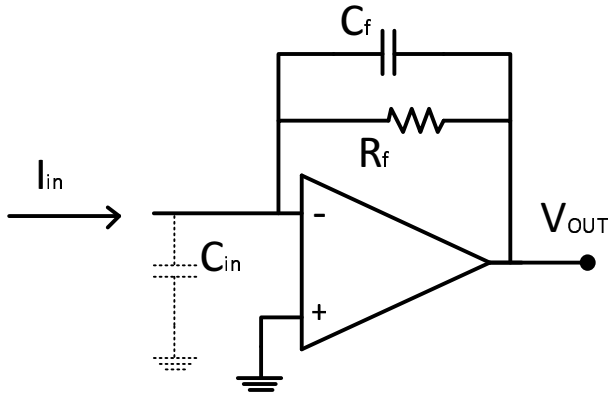

Figure 2.2: Simple transimpedance amplifier, the input current flows on feedback resistor and the output voltage results $V_{OUT} = -R_f I_{IN}$.

We proceed showing the main project guidelines, the main trade-off encountered and the expected performances.

2.2.1 Resolution

The values of capacitance and resistor in feedback net affects the resolution, bandwidth, maximum current of the system. The resolution reflects the minimum signal detectable and it depends on electrical noises. In figure 2.3 are reported the main noise sources. The opamp's noise is modeled by two noise sources, a current and a voltage source (also called respectively parallel and series noise). The thermal noise of resistor noise is modeled by ideally a voltage source with power density 4kTR; capacitor is ideally a noiseless device. The effect of each noise source on output voltage can be analyzed separately by superposition principle. The output noise results:

$$V_{out} = E_i * R_f + E_v * \left(1 + \frac{R_f}{\frac{1}{sC_{in}}}\right) + E_r \tag{2.1}$$

If we suppose that noise sources are totally uncorrelated the total noise spectral density of voltage is the sum of the single power spectral density:

$$S^2_{Vout}(f) = S^2_i \cdot R^2_f + S^2_v \cdot \left(1 + 4\pi^2 f^2 R^2_f C^2_{in}\right) + 4kTR_f \tag{2.2}$$

in which S_i^2 is the variance of parallel noise while S_v^2 is the variance of series noise, k is Boltzmann constant and T is the temperature. The RMS of output voltage can be calculated by square root of integral over the frequency of equation 2.2 it's possible to see that for high bandwidth the main source of rms noise is $4\pi^2 S_v^2 R_f^2 C_{in}^2 f^3/3$.

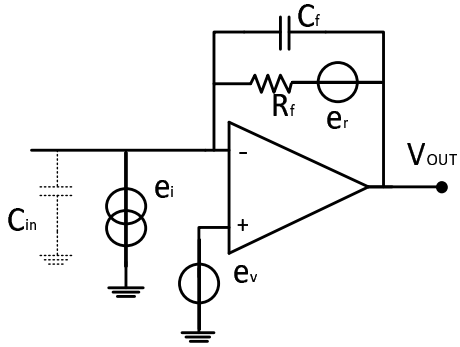

Figure 2.3: The impact of noise can be modeled as two noise sources from opamp and one noise sources for resistance, should be present also a current noise source on non inverting terminal of op-amp but as it's a low impedance node his impact is zero.

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2.2.2 Bandwidth

Over a certain current signal frequency the feedback capacitance cut-off the resistance reducing the transimpedance gain, in particular at the frequency ($f = 1/2\pi R_f C_f$) the resistance and capacitance have the same impedance magnitude beyond this frequency (called signal pole) the amplitude of output signal reduces. Moreover in all measurement frequencies the loop gain must be higher than 1 otherwise the feedback does is no more active and system might be instable or slower than expected. The bandwidth of closed loop is determined by the frequency in which the system has still a sufficient negative feedback, as convention we can take the point in which the loop gain is 1 and take this as limit. Supposing to have a single-pole operational amplifier and referring to fig. 2.2 the loop gain results:

$$\begin{aligned} G_{loop} &= A(s) \cdot \frac{1/sC_{in}}{1/sC_{in} + Z_f} \;;\; A(s) = \frac{A_0}{1 + s\tau_0} \;;\; Z_f = \frac{R_f}{1 + sR_f C_f} \\ G_{loop} &= \frac{A_0}{1 + s\tau_0} \cdot \frac{1 + sR_f C_f}{1 + sR_f \left(C_f + C_{in}\right)} \end{aligned} \tag{2.3}$$

The loop gain has two poles and one zero: one pole is the opamp dominant pole ($f_0 = 1/\left(2\pi\tau_0\right)$), usually it's a very low frequency about 1-100Hz, at higher

frequency the feedback net add two more singularities one zero $(1/(1/2\pi))$and one pole, the pole is a smaller frequency than the zero. A typical graph for g_{loop} (loop gain)is in figure 2.4. According to Bode stability criterion a

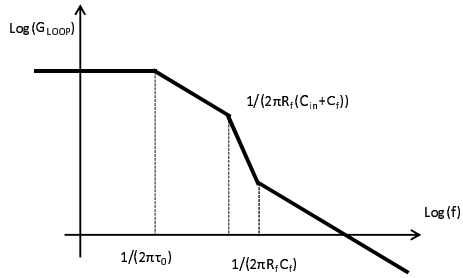

Figure 2.4: Typical graph of transimpedance g_{loop}, the first pole is due to operational amplifier, the two more singularities are due to feedback net. The bode stability criterion affirm that stability is reached if the graph cut the 0dB x-axis with -20dB/dec

feedback system is stable if the phase at gain 1 is at least 45° in other words if the loop gain diagram cross the 0dB x-axis, correspondent to magnitude of gain=1, with a slope of -20dB/dec like in figure 2.4 for a not so high value of $1/(2\pi R_f C_f)$.

2.2.3 Offset

The offset voltage (V_{os}) of a operational amplifier is defined as the input voltage to be applied to opamp in order to obtain a zero voltage at output; this is a value that depends both on asymmetries in opamp due to topologies and to aleatory dispersion of device's parameters. Offset can be model like a voltage source with value V_{os} (figure 2.5) on one of two input terminal of opamp.

In our measurement if the impedance of device under test is bigger than feedback resistor the impact on output voltage is to add a shift of output voltage by V_{os}, as consequence current measurements have a static error of $I_{os} = V_{os}/R_f$. But there is a second effect that might be worst, the voltage of input node is at a voltage V_{os}, so the voltage on the device under test is changed, offset could theoretical be read and keep in count but his temperature variation are unpredictable. Offset set approximatively the minimum voltage applicable on device under test, when analyzing a quantum dot V_{DS} corresponds to bias voltage and bias voltage fix the energy resolution of two spectral energy lines, two lines that are separated less than $\Delta E = eV_{DS}$ are not well detectable. Concluding the offset voltage of opamp limit the energy resolution, typical value of offset voltage for cmos opamp are 1mV while with bipolar technology it's possible to arrive up $100\mu V$. Some operational ampli-

fier are able to measure and reject their own offset, reaching up to $10\mu V$ of precision.

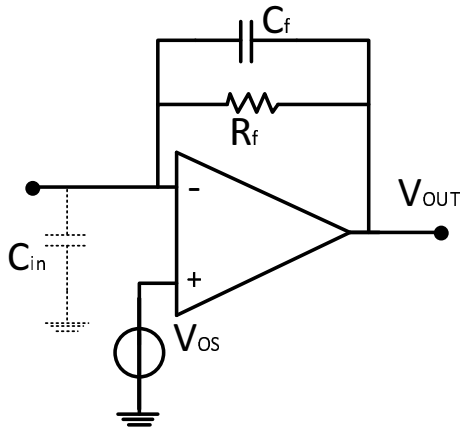

Figure 2.5: The offset voltage on a transimpedance amplifier is modeled by a voltage source on the non-inverting terminal of opamp; it causes a offset current and an error on voltage bias applied on device under test (DUT)

2.3 Design of multi-gain system

As we see in section 1.6, there are different measures to do on quantum dots with different characteristics, in particular stability diagram are essentially a DC measurement. Stability diagram can be composed up to 100 thousand points if we want a maximum measurement time of 3 hours we have to fix the bandwidth for a single measurement at 10Hz. The required resolution should be around 5fA to be able to detect also small secondary effect on quantum dots. On the other side measuring of reading spin [23] requires very fast current measurement down to few μs (corresponding to a bandwidth[1] of 160kHz). From the first requirement we can design the feedback resistor by force that thermal noise of resistor, integrated over 10 Hz, returns a input noise of 5fA, we obtain:

$$I_{RMS}^2 = \frac{4kT}{R_f}\Delta f \Rightarrow R_f = \frac{4kT * \Delta f}{(5fA)^2} = 6.6G\Omega \tag{2.4}$$

we choose $10G\Omega$ for be conservative (we are neglecting the opamp noise); now we can calculate the requested C_f from second requirement (bandwidth

[1]Each measurement costs about 5 $\tau = \frac{1}{2\pi f_b}$ in which f_b is the bandwidth and τ the time constant

at least 160kHz) and result $C_f = 1/(2\pi R_f 160kHz) = 0.1fF$ this is a value extremely low, impossible to obtain with realistic components due to parasitics and moreover if could be possible the requested gain-bandwidth product for opamp will be:

$$G_{loop}(160kHz) = 1 \rightarrow GBWP \cdot \frac{C_f}{C_f + C_{in}} = 160kHz \rightarrow GBWP = 1.6THz \tag{2.5}$$

this is many order of magnitude higher than actual technology can do, in equation 2.5 the input capacitance was valued into 1nF compatible with dimension of input wire.

According to this simple calculation, it's impossible to satisfy both requirement on resolution and bandwidth with a single transimpedance amplifier. The requirements belong to different type of measurement so it's possible to design different amplifiers each optimized for a specific measure (fast or sensible). As the principal design parameter is resistance value, we can design a single transimpedance amplifier with different feedback resistor chosen by switch like in fig. 2.6.

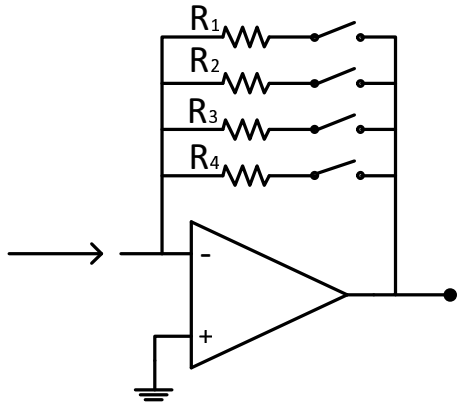

Figure 2.6: Using a different feedback resistors is possible to adapt the request in speed and resolution to different kind of measurement.

The $10G\Omega$ stage satisfy the accuracy requested in stability diagrams while a stage with $R_f = 1M\Omega$ can reach a 160kHz bandwidth, supposing a reasonable 1pF of feedback capacitance needed for stability reasons. Finally we choose our set of feedback resistor: $10G\Omega$, $1G\Omega$, $100M\Omega$, $10M\Omega$ and $1M\Omega$.

Now we analyze the effect of parasitics added by the switch; the residual On resistance is not critical up it's smaller than $1M\Omega$, also the switching speed is not a problem. The effect of parasitic capacitance (around few pF) on the switch is shown in figure 2.7, when the switch is in ON state C_a and C_b are

summed and has almost no effect because they are charged by opamp output[2] (fig. 2.6); while C_c is shorted and has no effect.

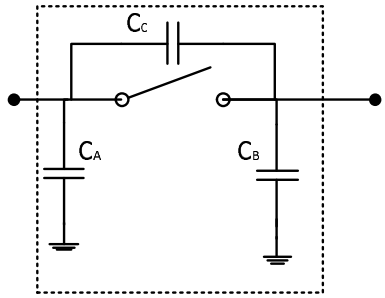

Figure 2.7: Model of a switch considering the parasitic capacitance, we neglect the parasitic resistance because it's not critical in our design.

When the switch is off C_b again is charged by opamp output, but C_a at high frequency short the OFF resistance on input node, since it's a virtual ground this is not a problem on signal, but occurs to be sure that the modification on G_{loop} not affected the amplifier stability. Capacitance C_c has a dangerous effect, it shorts the open switch at high frequency and since the feedback resistances has quite high values his happen for small frequencies; supposing for example $C_c = 1pF$ the $10G\Omega$ stage becomes active from 16Hz always independent from which stage is active. This affect dramatically the flatness of the transfer function and this is not acceptable.

The solution is to use one opamp for each transimpedance stage connected to input current and output voltage as in figure 2.8. In this case each parasitic capacitor on switches see a low impedance nodes so singularities associated with it are pushed at higher frequency[3]

Using different transimpedance has another advantage, it keep possible to use different opamp for different stages to adapt the characteristics to each stage in order to optimize the performances.

2.3.1 Speed and stability

A transimpedance amplifier can be analyzed as in the inset of fig. 2.9 in which the block A correspond to opamp amplifier and block β is the feedback net.

[2]Also if the switch is swapped with his correspondent feedback resistor the $C_a + C_b$ capacitance increase a little the input capacitance but it's not dramatic as there already have a 1nF input capacitance

[3]Approximately a pole due to a capacitance is at frequency $1/2\pi RC$, in which R is the equivalent resistance on capacitance, if is low the pole are at high frequency

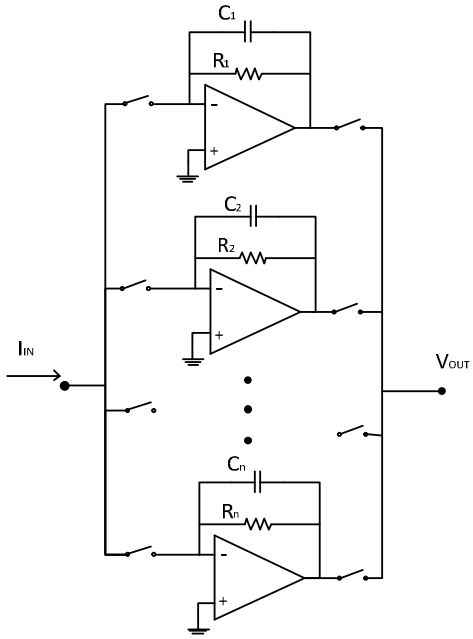

Figure 2.8: Parallel transimpedance stages, in this case the parasitic of switches are always on low impedance node and doesn't affect the circuit. This is the topology chosen for our circuit.

The loop gain it's $A \cdot \beta = A/\left(1/\beta\right)$ and correspond in a log scale to the area between $A(s)$ curve and $1/\beta(s)$ curve in fig. 2.9.

In figure 2.9 there is the plot of $A(s)$ and $1/\beta$ curves, the bandwidth of the feedback is the point $G_{loop} = 1$ corresponding to in the point f_T where curves cross each others the circuit is stable if the cross between $A(s)$ and $1/\beta(s)$ happens with a -20dB/dec as differential slope. In fig. 2.9 this correspond to have a f_t far enough from f_f and f_{o2} because his phase component may reduce the phase margin. A decade of distance is enough to keep the phase contribute below 5°. So we design $10f_f = f_t$ $f_t = GBWP \cdot C_f/C_{in}$ and $f_f = 1/(2\pi R_f C_f)$, by merge these equation it's possible to calculate the condition on gain bandwidth product:

$$10 \cdot \frac{1}{2\pi R_f C_f} = GBWP\frac{C_f}{C_{in}} \Rightarrow GBWP = 10\frac{C_{in}}{2\pi R_f C_f^2} \tag{2.6}$$

as already mentioned the presence of C_f reduce drastically the requested GBWP and fixes the high frequency loop gain. Of course C_f limit the signal bandwidth f_f that can be raised by reducing R_f but so increasing the noise and reducing the gain; it's important to find the good trade-off between design parameters.

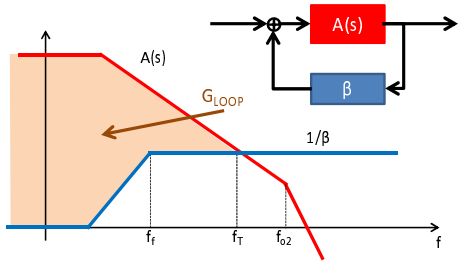

Figure 2.9: Transfer functions of a A and the inverse of β, blocks in a feedback loop, the loop gain it's the area between the curves, the point in which the curves cross it the frequency in which $G_{LOOP} = 1$. A is a double-pole opamp, while β is the feedback net of a transimpedance amplifier.

2.3.2 Noise requirement

Let switch now to see the noise design project. Starting with equation 2.2, we can divide the spectral density of opamp's series noise S_v^2 in two contributes: a white noise e_b^2 constant with f and a flicker noise e_a^2/f predominant at low frequencies, the same happens for parallel noise $S_i^2 = I_b^2 + I_a^2/f$. Substituting into equation 2.2, we obtain:

$$S_{Vout}^2 = \frac{I_a^2}{f} \cdot R_f^2 + I_b^2 \cdot R_f^2 + 4kTR_f + e_b^2 + \frac{e_a^2}{f} + 4\pi^2 e_a^2 R_f^2 C_{in}^2 f + 4\pi^2 f^2 R_f^2 C_{in}^2 e_b^2 \tag{2.7}$$

in figure 2.10 there is an example of output noise spectra; there are 4 main contributes: a flicker noise due to opamp's flicker noises, a white component due to resistance, series and parallel opamp thermal noise, a f component due to flicker series noise and input capacitance and a f^2 component due to white series noise and input capacitance. The resolution in term of V_{rms}can be calculated by integrating the noise spectral density over the bandwidth and extracting the square root.

2.3.3 Opamp dimensioning

For high sensibility stage we choose a $10G\Omega$ resistor to satisfy the noise requirement (5fA over 10Hz bandwidth) with a maximum input current of 1nA on a 10V supply; using higher feedback resistor may reduce the maximum input current too much. The equivalent input noise spectra with a $10G\Omega$ resistor is:

$$\sqrt{\frac{4kT}{R_f}} = 1.28f\frac{A}{\sqrt{Hz}} \tag{2.8}$$

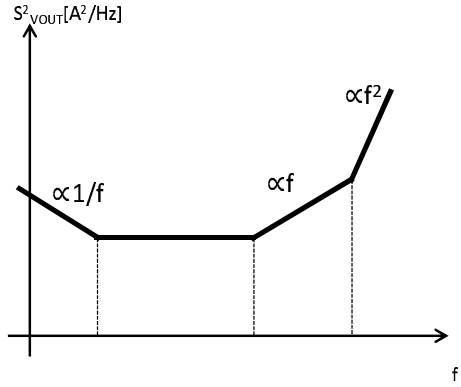

Figure 2.10: Example for noise spectral density for a transimpedance amplifier, one over f noise is due to series noise from opamp, white noise is to also to resistor and f noise and f^2 is the series noise of opamp that becomes differentiated on input capacitance.

we have to choose an opamp that add less noise then resistance noise, series white noise add a contribute in input noise e_b/R_f, to be negligible respect resistance noise e_b must be smaller than $12.8\mu V/\sqrt{Hz}$ this is a easy condition to satisfy even with cmos opamp, while parallel noise has a direct impact on input node and must be below $1.28fA/\sqrt{Hz}$ this is quite impossible with bipolar opamp. For these reason we choose a AD8625 JFET opamp from Analog Device, with parallel white noises $e_i = 0.4fA/\sqrt{(Hz)}$ and series $e_b = 17nV/\sqrt{(Hz)}$. To maximize the bandwidth we choose do not put a physical feedback capacitor but enjoying at least 200fF parasitic in surface mount device, so the signal bandwidth results about $1/(2\pi * 10G\Omega * 200fF) = 80Hz$; the requested GBWP for the stability of the transimpedance, according to equation 2.6 is greater than 4MHz, that is available[4] in AD8627 (5MHz).

Following the same design procedures we design the second stage with a resistor of $1G\Omega$ increasing the bandwidth up to 160Hz in this transimpedance amplifier the series noise became more critical and we choose a different opamp AD8066 with lower $e_b = 7nV/\sqrt{Hz}$. The third transimpedance ($100M\Omega$) use the same Opamp AD8066 reaching 1.6kHz. The forth transimpedance use a $10M\Omega$ as feedback resistor and reaches 16kHz bandwidth obtained with an high speed 210MHz opamp by Texas instruments THS4631 and with a feedback capacitor added for stability reasons. It has a higher parallel noise than previous opamp but this is less critical than series noise which has has higher density at high frequency (last two term in eq. 2.7); in this transimpedance we obtain a $53pA_{RMS}$ over 16kHz. For the transimpedance with the highest

[4]We need a 4MHz opamp in order to detect a 80Hz signal this is due to big input capacitance

bandwidth the series noise becomes very critical, let consider only the last term in equation 2.7 the correspondent input noise rms integrated on band B becomes:

$$A_{rms} = \sqrt{\int_0^B \frac{4\pi^2 \cdot e_b^2 \cdot R_f^2 \cdot C_{in}^2 \cdot f^2}{R_f^2} df} = \sqrt{2}\pi C_{in} e_b B^{\frac{3}{2}} \tag{2.9}$$

For this reason the feedback resistor can be reduced allowing a raising on bandwidth without decrease the SNR, but very critical is series noise. According to the requirement we choose a bipolar amplifier by Texas THS4021 because it can satisfy the requested bandwidth (for 160kHz signal bandwidth and using a 1pF feedback capacitor the requested Gain-bandwidth product is 1.6GHz), with a $1.5nV/\sqrt{Hz}$ very low series noise, the noise is dominated by current white noise and f^2 noise. Giving $980pA_{RMS}$ over 160kHz with 1nF as input capacitor.

2.3.4 Low offset stage

In section 2.2.3 we presented the effect of offset voltage of opamp on measure of quantum dots. As seen it affects both the offset on output signal and also the bias on quantum dot which can hardly be smaller than offset voltage[5]; we choose to insert in our system also a low-offset opamp stage for that kind measures in which the bias voltage on quantum dot has to be below 1mV, a typical offset in FET opamp. There are different particular ways to reduce the offset of an opamp amplifier[27], in our case we choose the MAX4238 by maxim semiconductor that uses a autozeroing offset amplifier. It's claimed with $0.1\mu V$ maximum voltage. Unfortunately it has some restriction: a low supply voltage (5V), low GBWP (1MHz) and relatively high noise ($30nV/\sqrt{Hz}$). As low offset is useful for low bias voltage, and a low bias reduce the current, we optimize his performances of high-sensitivity, designing a $1G\Omega$ feedback resistor with a 1pF as feedback capacitor. Considering a 1nF as input capacitor we obtain a bandwidth of 160Hz with rms input noise at full bandwidth of 400fA.

In table 2.1 there are a syntesis of the simulated performances of our six transimpence amplifier.

[5]Although a calibration could theoretical resolve the offset problem, but it's hard to prevent his temperature variations

Stage	R_f	I_{max} ($V_{DD} = 10V$)	Bandwidth	Input noise rms at FB
1	$10G\Omega$	1nA	80 Hz	90fA
2	$1G\Omega$	10nA	160 Hz	230fA
3	$100M\Omega$	100nA	1.6kHz	2.25pA
4	$10M\Omega$	$1\mu A$	16kHz	54pA
5	$1M\Omega$	$10\mu A$	160kHz	980pA
6	$1G\Omega$	$2.5nA$	160 Hz	400fA

Table 2.1: Multi Stage Transimpedence amplifier characteristics

2.4 Post-elaboration

DC filtering

Once translated the current signal into voltage signal, we have to elaborate the signal in order to maximize the signal-to-noise ratio without significant losses in bandwidth. Referring to figure 2.11, at higher frequency than signal bandwidth, over $f_s = 1/(2\pi R_f C_f)$ the feedback resistor becomes shorted by feedback capacitor; as consequence both e_i noise and e_r noise have no effect because they circulate into capacitance instead of resistor and the voltage output remains fixed to zero. But this don't cancel e_v contribute, on the contrary it becomes amplified by a factor $(1 + C_{in}/C_f)$ that can reach 1000, so we have a significant noise in frequencies that we are not interested in, in fact our signal stop at f_s. For this reason we decide to insert a optional low-pass filter in order to reduce the high frequency noise. It can be useful to maximize the S/N.

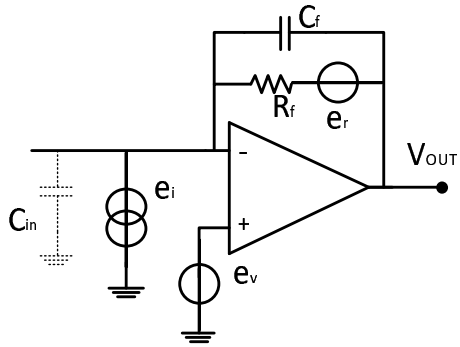

Figure 2.11: Noise sources in a transimpedence amplifier, at high frequency C_f shorts R_f, this nullify the impact of e_i and E_r but e_v become amplified by $1 + C_{in}/C_f$.

The cut-off frequency has been choose at 40Hz to reject the power line disturbs and the order is two to be effective also for power density noise pro-

portional to frequency (like in transimpedance amplifier)

AC filtering

If we have a small high frequency current signal over a big dc current, like in case of charge sensing measurement (sez 1.9.1), may be hard to detect the small signal due to limited dynamic range of ADC; moreover to detect high frequency signal we had to use a small feedback resistance and so the amplitude of this signal is quite small and the quantization noise of an ADC may cover significantly the information. To solve this problem we add a parallel path for signal which include a high-pass filter and a voltage amplifier, in this way the dc voltage is rejected and the signal is amplified to permit a optimization of ADC performances.

In figure 2.12 there is the complete schematic for signal path, after the multi-stage transimpedance we have a signal with bandwidth up to 160kHz and minimum noise of $40nV/\sqrt{Hz}$ due to the thermal noise of resistance in $1M\Omega$ stage[6]. We put three different signal path: V_{DC} is unchanged to the output for measure in which the transimpedance characteristics are exhaustive, the V_{LPF} path has a Sallen-Key double-pole low-pass filter when the noise band can be reduce to improve SNR, the poles are butterworth pole at 50Hz in order to maximize the flat response of filter. The third path is an V_{AC} path, equipped with a 10Hz high-pass pole and a voltage amplifier by 101, this path can be used to reject a high DC component and magnify the high frequency signal over it. We use a THS4631 opamp by Texas instrument that has sufficient GBWP for a 160kHz signal and has a lower noise ($7nV/\sqrt{Hz}$) than minimum noise from transimpedance stages $40nV/\sqrt{Hz}$ and also it has a low offset $250\mu V$ important on high gain voltage amplifier.

Our system allows to apply a voltage on input node by changing the voltage on non-inverting terminal of opamp; this is useful when for example we want to apply to the device under test a $V_{bias} = V_{DC} + V_{AC} * sin(\omega t)$, in this case it's easy applying the DC component on V_{DUT} and the ac component on quantum dot's second terminal avoiding the use of other summing stages. It's problematic applying an AC signal on non-invering terminal of opamp because in this case C_{IN} requires a current that comes from the feedback leading a big spurious signal. Moreover high frequency noise on V_{DUT} reduces dramatically the SNR since it works like e_v noise sources in figure 2.3 for this reason we insert a simple RC low-pass filter on V_{DUT}.

[6]The high sensibility stages have less input noise but high output noise of high bandwidth stages, in fact the output noise density of resistor is $4kTR_f$ increasing with the value of resistor

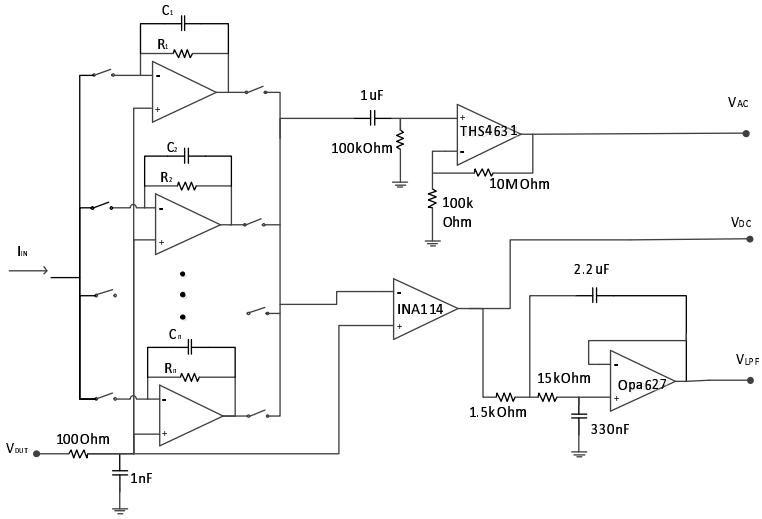

Figure 2.12: Complete schematic for signal path of room temeperature detection eletronics, different output can used to follow different requirement of different measurement on quantum dots.

Of course when apply a voltage on V_{DUT} the output voltage of transimpedance amplifier changes and becomes $V_{OUT} = V_{DUT} - R_F I_{IN}$, to restore the ideal characteristic the INA amplifier subtracts V_{DUT} and V_{OUT} to restore in output $V_{INA} = R_F I_{IN}$. Since V_{DUT} is almost a DC voltage, on AC path is rejected so no INA is needed in this path.

2.4.1 Stage selector

We have twelve switches, driven with 6 signal, one for two switches. As there are no requirement on speed of commutation we decide to use relais because that have less parasitic, less current leakage and less shot noise than solid state switches. We use a single-side stable relais G6H-DPDT-12VDC by Omron, they are a dual package driven with 12V signal. The state of our system is managed by MC14017B a decade counter by On semiconductor, it has six output connected to relay control, only one of these output is high and every clock edge the high value is shifted to next output so using a button as clock is possible change the input amplifier. As the output current of counter (2.5mA) is no enough to drive a relay (12mA), we use a current buffer with a Bipolar transistor in saturation or off region. In figure 2.13 there is the schematic of control part of only one relay.

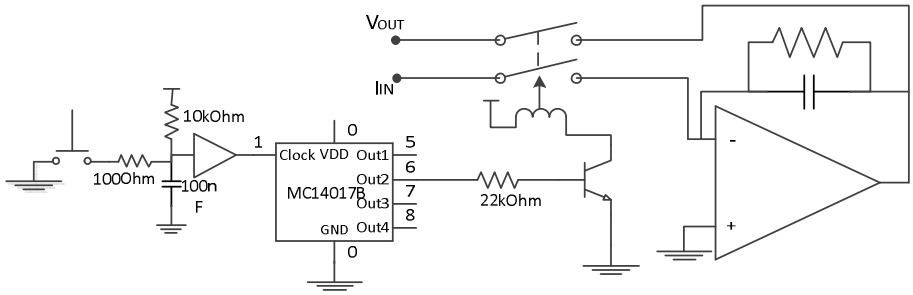

Figure 2.13: Schematic for control part of room temeperature detection eletronics, the status is stored in decade counter MC14017B by On Semiconductor, and it's changed when the button is pushed. A bjt provide the needed current for relay's coil.

2.5 Measurement of 300K system

2.5.1 Transfer function

We present now the measurements of characterization of our system. In figure 2.15 there are the transfer function of the first five stages. We see a reduction of bandwidth of about factor 2 except for stage 1 in which the reduction arrives to factor 6; the poles are 12Hz, 130Hz, 718Hz, 6.34kHz, 60kHz. This is due to unexpected crosstalk parasitic capacitance in relay, in particular the parasitic capacitance between input transimpedence node and output transimpedence, works as well as a feedback capacitor, reducing the bandwidth, this is a un-

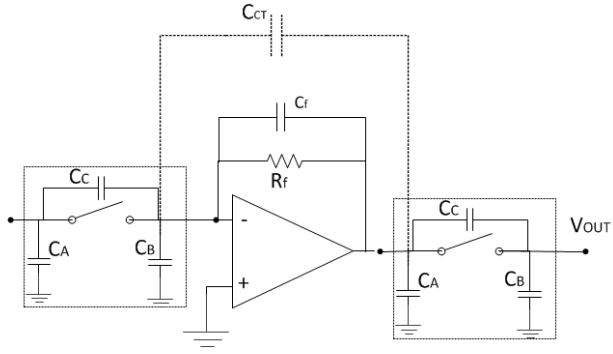

Figure 2.14: Schematic for control part of room temeperature detection eletronics, the status is stored in decade counter MC14017B by On Semiconductor, and it's changed when the button is pushed changing the pair of switches to be closed. A bjt provide the needed current for relay's coil.

characterized capacitance in datasheet that we are able to estimate in 1pF; in stage 1 his effect is more significant because there was no physical capacitance

but only parasitic capacitance estimate in 200fF. Despite the reduction of bandwidth the specification for stage 1 satisfy the resolution specification but not for stage 5 since was required 160kHz bandwidth; we could change the relay or lowering the value of feedback resistor eventually increasing a few the feedback capacitance to avoid the instability.

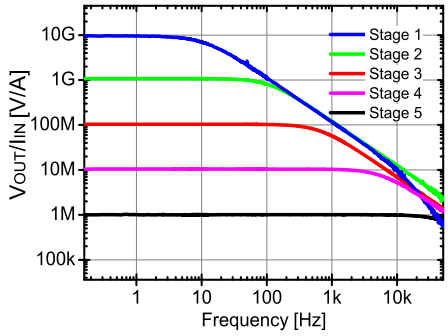

Figure 2.15: Transfer function of first five stage of multistage transimpedence amplifier, there are a band reduction due to crosstalk capacitance C_{CT}between two relais in same package.

2.5.2 Noise

In figure 2.16 there are the input noise spectral density for each amplifier; amplifier 5 has a strong 1/f and white noise but considering his maximum bandwidth it's not the dominant term because series noise will dominate in whole bandwidth. The other stages confirm the design project; in stage 2 and stage 3 it's possible to see also the f dependent noise, stage 1 has a few more white noise due probably to insulation resistance on input node. To reduce white noise of stage 5, it's possible to change opamp and use a fet opamp, in this case the best alternative is opa657 by texas instrument (GBWP=1.6GHz); but using fets the series noise is raised a lot, in opa 657 is $5nV/\sqrt{Hz}$, since it's the dominant term at full bandwidth, in this stage we decide to avoid this way.

The stage 5 has showed a high offset voltage about 100mV, for this reason was hard to measure his noise with DC coupling so we decide to measure his noise thought the AC path, in fact below 1Hz it's clear the high-pass effect. The high output offset of stage 5 is due to high bias current of opamp in bipolar technology, although it's possible to compensate this effect by using in both input terminal of opamp the same resistor to cancel the output offset, in our case this would have a destructive effect because will change the voltage

on input node and so the bias voltage on quantum dot modifying totally our measurement meaning; having a high offset in output voltage and keeping a small offset on bias voltage is a preferable situation. A way to reduce output offset is reducing the feedback resistor; this is the solution we choose since solve also the problem related to the reduction of bandwidth due to relay capacitor. We put a $100k\Omega$ resistor and a $5pF$ capacitor on feedback to raise the bandwidth up to 300kHz and ensure stability; the increment of white noise due to resistance is negligible respect the white current noise of opamp.

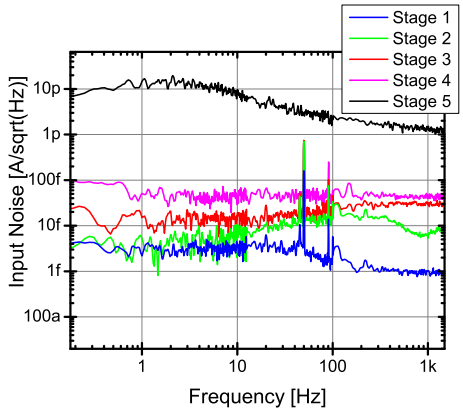

Figure 2.16: Noise of first five amplifiers of multistage transimpedence amplifier, amplifier 5 has a bigger 1/f noise but it is not the dominant term, while other amplifiers has almost the white noise due to feedback resistor, stage 1 has more noise due probably the parasitic isolation resistance of input node.

2.5.3 Low offset stage

The low offset stage (stage 6) is based on a auto-zero operational amplifier, max4238 by maxim semiconductor they claimed a $0.1\mu V$ offset. Periodically the low-offset operational amplifier read his own offset and subtracts it, so not only offset is drastically reduced, but also his drift and his temperature dependence has been canceled out because are periodically corrected. But the autozeroing has the inconvenient that introduce disturbs related to the different internal configuration.

A low-offset operational amplifier permits the use of a very small bias on quantum dot, useful for distinguish two close energy levels, since only energy level inside the bias window participate to conduction. The frequency response of low offset stage confirms our results. The measure of input noise has be done by applying a resistor (in our case $47M\Omega$) as device under test input and sweeping a voltage on it, the input voltage that allows zero current is the offset

voltage. In figures 2.17 and 2.18 there are the transfer function, and the input voltage versus input current. The transfer function confirm the little band reduction due to relay parasitic capacitance, obtaining a 70Hz bandwidth. The input noise results $-33\mu V$; it's due to offset of our measurement instrument, semiconductor parameter analyzer 4200 by keithley.

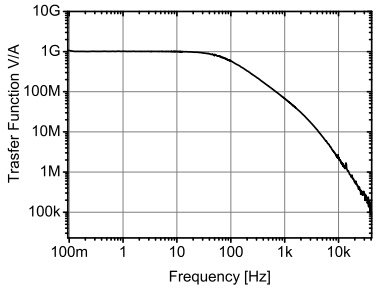

Figure 2.17: Transfer function of low offset stage of multistage transimpedance amplifier confirm a bandwidth of about 70Hz.

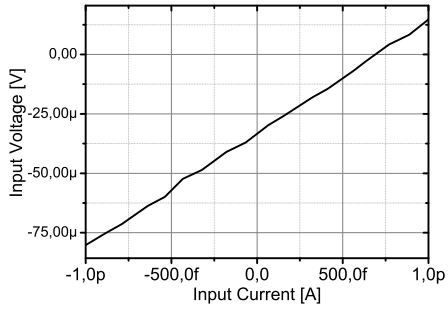

Figure 2.18: Measure of input offset voltage by measuring the voltage on input node through a resistor when zero current flows in it

2.6 Conclusion

The measurements confirm that our system satisfy the specification for measurement on quantum dot, we are able to detect 5fA of current with a bandwidth of 10Hz, and on the other hand measure up to 150kHz with input rms noise of 980pA. We mounted out circuit in a 19-inch Rack (figure 2.19) suitable for multi-instrument setup. It's supplied by two batteries +12V -12V, to avoid 50Hz related disturbs, absorbing 90mA on +12V and 55mA on -12V. The asymmetric supply current is due to the control net supplied with only +12V.

2.6.1 Limit and improvement

We have already seen some limits of our multistage amplifier, the bandwidth is a little less than the original design due to unexpected parasitic crosstalk capacitance on relay. Using different package for switches can solve the problem, but at cost of more supply current that now is 100mA. Current can be reduced by using a latch relay instead of static relay, latch relays need current only when have to commute and are without consumption in static regime; in

Figure 2.19: Photo of the multistage system, mounted on a rack. The terminal are easy accessible by bnc cable.

this case in necessary to change the control net. However the most important limit in our amplifier performances is input capacitance, it limits the noise because at high frequency the input noise in rms is:

$$A_{RMS} = \frac{2\pi}{3} e_v C_{in} B^{\frac{3}{2}} \tag{2.10}$$

the opamp series noise e_v is limited by technology and can hardy be below $1nV/\sqrt{Hz}$, B is bandwidth. The only way to reduce the noise is reducing the input capacitance.

We see that for stability reason the signal bandwidth has to be below $f_t = GBWP \cdot C_f/C_{in}$ (figure 2.9). The signal bandwidth is $1/(2\pi R_f C_f)$ substituting C_f and supposing that signal frequency may arrive up to f_t we obtain a maximum signal bandwidth of:

$$F_s^2 = \frac{GBWP}{2\pi R_f C_{in}} \tag{2.11}$$

Since GBWP is limited on few GHz and R_f cannot be reduced for noise requirement, the only way to increase the bandwidth is again reducing the input capacitance.

But in our setup (section 2.1) it's not possible reduce safely the input capacitance, the cryomagnet is unaccessible to discrete electronics; we decided to develop an integrated system working *inside* the cryomagnet in order to reduce the dimension of input wire and so reduce noise and increase bandwidth.Inside the cryomagnet the temperature are low to reduce significantly the input capacitance the electronics must be able to work into 1-4K range. In next chapter we see the effect on a standard cmos technology when used at cryogenic temperature and how to take advantage of it.

Chapter 3

Cmos Technology Characterization at 4.2K

In the last chapter we described that the most limiting parameter when detecting a current coming from a ultra-scaled mosfet quantum dot is input capacitance; which is due to the long wire between the sample, kept at cryogenic temperature and room temperature electronics. Our purpose is to develop an integrated amplifier able to work even at cryogenic temperature, in this way can be attached in the cryostat near the sample reducing drastically the input capacitance. In order to design and realize the blocks composing the integrated cmos transimpedance amplifier working at a temperature of few Kelvin, it is necessary first of all characterize all the integrated components that are likely to be employed into the amplifier stage at the liquid Helium temperature, $T_{Liquid-He} = 4.2K$.

3.1 Electronic devices at cryogenic temperature

Since the development of integrated circuits, the effect of temperature has been intensively studied [28]. In particular, cryogenic operation of silicon devices has been studied for spatial applications [29], in which the low temperature is forced by external environment. Low temperature gives some improvement on performance; in fact low temperature reduce the thermal noise and the dark current in detectors [30] and improve the stability on oscillators [31], increasing the mobility of electrons and holes.

Semiconductors are material in which the free charges are produced by thermal excitation. The doping of a semiconductor consists on replace the semiconductor atom with other element in whose the thermal excitation is more convenient. When we reduce the temperature, it's more difficult to

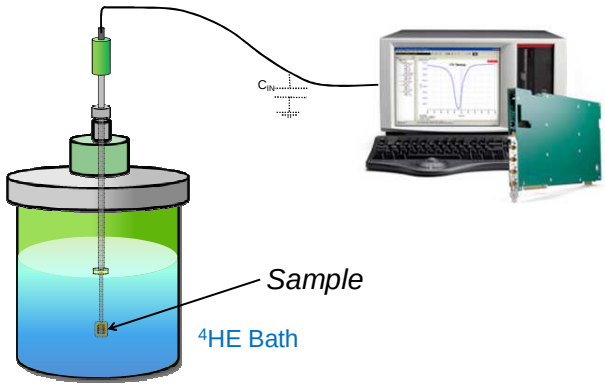

Figure 3.1: Experimental setup for device characterization at cryogenic temperature. A sample holder and a silicon diode are mounted on a probe to make measurement and monitoring the temperature, there are a constant temperature gradient inside the dewar that allows measurement in function of the temperaure.

separate one electron from is own atom, at 0 Kelvin are no free charges, the semiconductor becomes an insulator.

Due to the freeze-out effect a suitable technology for temperature around 4K is cmos [32]. In bipolar technology the conduction is ensured by diffusion which is strictly dependent on temperature; while in cmos electrons move thanks to drift less affected by temperature than diffusion. There are others special technology used at 4K like GaAs HEMT (High Electron Mobility Transistor) [33].

3.1.1 Setup for cryogenic characterization

In this section, we focus on the description of the experimental bench we made up at the very beginning of this work, used for device characterization within the temperature range $4.2K \leq T_{MEAS} \leq 300K$ and we provide a very basic explanation of the measurements performed. Consider the quite simple experimental setup, represented in figure 3.1: it consists of a Keithley semiconductor parameter analyzer which has been used to characterize the (I-V) curves of the devices available in our technology (Nmos, Pmos, resistors and capacitors); and also a network analyzer to measure the frequency response. Then in order to perform the measurements at different temperature, we equipped the lab with a liquid helium (He) dewar. With a long steel rod we were able to test the devices fixed on a sample holder either at $T_{He} = 4.2K$ and within a temperature range between T_{ROOM} and T_{He}, by sliding the rod down into the dewar closer and closer to the helium surface until its contact. To correctly establish the temperature experienced by the sample itself, a silicon diode probe (tem-

perature range: $1.40K \leq T \leq 500K$) was fixed to the sample holder, close to the DUT. Such experimental setup has been adopted to track the temperature dependence of the remarkable parameters of the examined components. The adoption of such temperature probe has been useful to keep the temperature controlled, in particular in presence of mosfet transistors with large W/L ratios and hence with large drain current, or power dissipation, that might affect the temperature stability of the environment close to the DUT. We made standard I-V characteristic, trans-characteristic and noise measurements on mosfet transistors with different geometry, standard I-V curves on integrated poly-silicon resistors, and capacitance measurements at different temperature under T_{ROOM}.

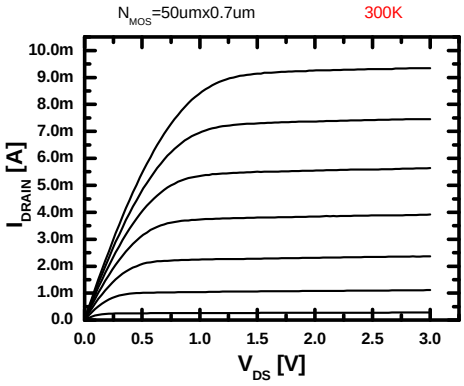

Figure 3.2: Characteristic of Nmos $50\mu m/0.7\mu m$ at 300K.

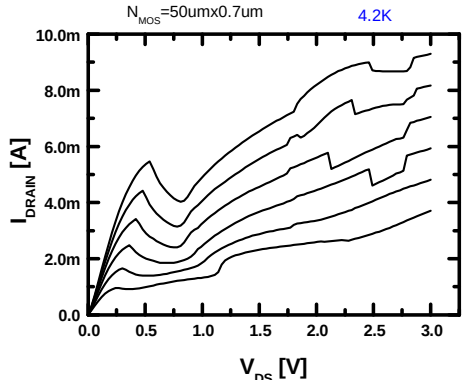

Figure 3.3: Characteristic of Nmos $50\mu m/0.7\mu m$ at 4.2K there are strong effect that compromise transistor working due to low temperature.

3.2 Mosfet transistor at 4.2K

In this section we present the characterization of simple mosfet transistors at 4K. In figure 3.2 and 3.3 there are the characteristic curves of the nmos $50\mu m/0.7\mu m$ at 300K and at 4K. At low temperature appear some strange effects, when the drain-source voltage reaches the pinch-off point the current starts decreasing for a while and than increase; this make the device unusable for analog application that are based on the flatness of saturation region. In the characteristic curve we can distinguish two kind of effects: the reduction of current in pinch-off zone and the increase at high V_{ds}; these effects are

already known in literature [34], [35], [30], [36] and they are called respectively *Hysteresis* and *Kink* effect (fig. 3.5).

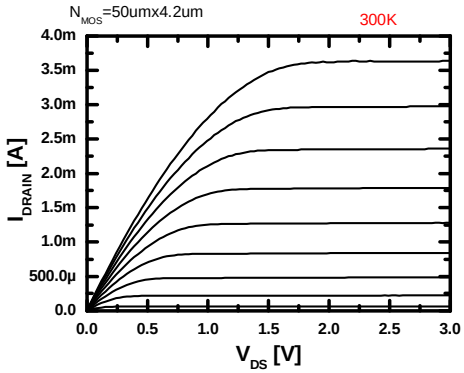

Figure 3.4: Characteristic of nmos $50\mu m/4.2\mu m$ at 300K.

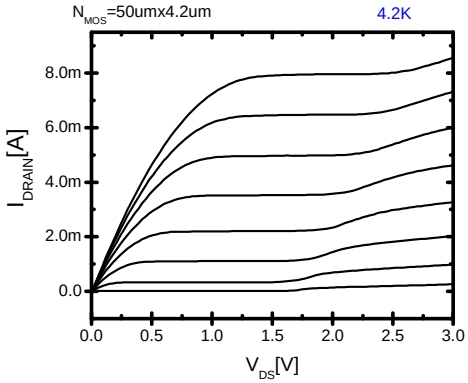

Figure 3.5: Characteristic of nmos $50\mu m/4.2\mu m$ at 4.2K, Hysteresis-like effect disappears and kink is reduced. There is a huge region in which transistor works good.

The increase of current at high drain voltage is the so called kink effect (fig. 3.5), typical in SOI technology. It's due to high impedance of bulk, a hole current flowing through bulk provoke a changing in voltage of bulk itself, this affect the source-bulk junction increasing the current. The reduction of current in pinch-off in literature is known as hysteresis effect (fig. 3.3) because the peak of current is present only from small to high voltage while from up to down it disappears [30]. In our measurement we have the peaked behavior in both direction, probably because our technology is a low-voltage 3.3V and the voltage don't reaches the value to activate the cancellation of the peak.

This hysteresis effect is due to the forced formation of a depletion layer caused by the avalanche-generated majoritar substrate current [34]. At 4.2K the thermal generation/recombination is very slow and no depletion layer is expected however it was shown that the depletion layer width and charge density can be modified by a mechanism based on impact ionization and recombination of shallow (dopant) levels in the bulk. this process is induced by a hole current (in nmos) flowing from the pinch-off region towards the substrate back contact; the hole current originates from the avalanche ionization at the pinch-off end of channel. The holes can interact in three ways while traveling through the bulk: can drift, can impact an neutral acceptor and free a additional hole or can recombines with an ionized acceptor. Dependending on

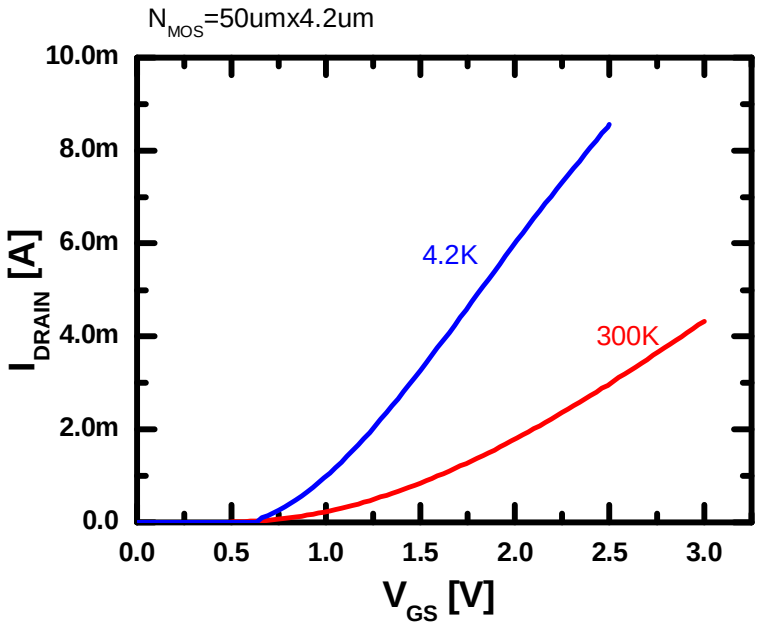

Figure 3.6: Transcharacteristic of nmos $50\mu m/4.2\mu m$ at $V_{DS} = 3V$, the mobility is increased and also the threshold voltage (table 3.2).

the local electric field and charge densities an equilibrium space charge will be established after some time, the time constant for this forced depletion later formation is in first instance inversely proportional to the mentioned substrate current [36].

However kink effect and hysteresis have an impact strictly dependent on dimension, for small W/L the impact of hysteresis can be negligible, and also kink effect reduces. In figure 3.5 there is the characteristic of a $50\mu m/4.2\mu m$, in this transistor there is no effect of reducing current (Hysteresis) and also kink effect is reduced; so this transistor behave like a room temperature transistor even at 4K in non-kink region. In figure 3.6 there is the transcharacteristic of nmos $50\mu m/4.2\mu m$, we can see the improvement in term of mobility thanks to less frequency impact with phonon.

We characterized transistor both nmos and pmos with different dimension, summarized in table 3.1 in which the cell "working at 4K" means that hysteresis and kink are negligible.

Looking at the table we can conclude that hysteresis and kink appear only in transistor big W/L ratio, in particular nmos with W/L above 35 and pmos with W/L above 71. Both working Nmos and Pmos have been investigated in terms of their remarkable electrical-parameters, that is threshold voltage

Name	$W[\mu m]$	$L[\mu m]$	W/L	Working at 4.2K
$Nmos_1$	50	0.35	142.8	No
$Nmos_2$	50	0.7	71.4	No
$Nmos_3$	50	1.4	35.7	Yes
$Nmos_4$	50	4.2	11.9	Yes
$Nmos_5$	20	7	2.86	Yes
$Nmos_6$	0.4	0.35	1.14	Yes
$Pmos_1$	220	0.6	366.6	No
$Pmos_2$	50	0.35	142.8	No
$Pmos_3$	50	0.7	71.4	Yes
$Pmos_4$	50	1.4	35.7	Yes
$Pmos_5$	50	4.2	11.9	Yes
$Pmos_6$	80	14	5.7	Yes
$Pmos_7$	0.4	0.35	1.14	Yes
$Pmos_8$	1	14	0.07	Yes

Table 3.1: Geometric dimensions of measured mosfets. Not all the measured devices have shown a correct operation at low temperature, as reported within this table

V_{TH}, the gain factor k_p, k_n and the early factor λ, drain current I_D and transconductance g_m. The very basic equations describing the mosfet operation will be recalled within this paragraph, equation 3.1 describes the saturation current as:

$$I_D = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{3.1}$$

in which V_{TH} is the threshold voltage and $(\mu C_{OX}) = k$. The transconductance g_m can be derived from Eq.3.1 neglecting the Early factor ($\lambda = 0$) as:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{OX}\left(\frac{W}{L}\right)(V_{GS} - V_{TH}) = \frac{2I_D}{V_{OV}} \tag{3.2}$$

in which $V_{OV} = V_{GS} - V_{TH}$ is the overdrive voltage.

We decide to use a simple model for transistor (equation 3.1), it would be possible develop a more complicated model like bsim3v3 [37] including also kink effect; but this will be useless because kink has to be avoided because reduce drastically the output impedance of the mosfet, moreover it need different design approaches. On the other hand using simple model once extracted the parameter it possible to design and realize a cryogenic circuit able to work at 4K, with the same design method than for room temperature.

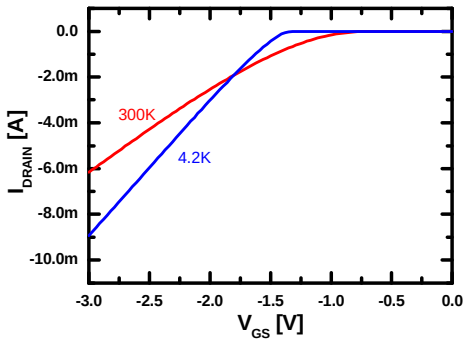

Figure 3.7: Transcharacteristic of pmos $50\mu m/0.7\mu m$ at 4.2K, there is an improvement of mobility but also a huge increase of threshold voltage that becomes about -1.3V

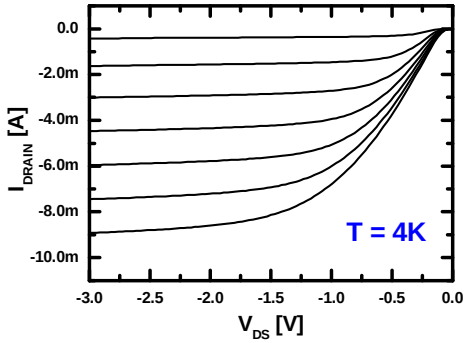

Figure 3.8: Characteristic of pmos $50\mu m/0.7\mu m$ at 4.2K, the kink effect respect nmos at 4.2K (figure 3.5) is reduced thanks to the less multiplication factor M for holes respect to electrons.

Figures 3.8 and 3.7 show the characteristic and trans-characteristic of pmos $50\mu m/0.7\mu m$. The curves has an acceptable mosfet behavior although the threshold is increased. This is an effect well known in literature [30]; it's due to the high impedance of bulk that seems a insulator and so the gate-channel capacitance reduces. These cryogenic phenomenons have similar impact on nmos and pmos, in pmos there are less kink effect due to the smaller multiplication factor M for holes respect electrons.

In table 3.2 there are a summary with all working transistor both N and P with the extracted K_N or K_P and V_{TH}; we can see an increment on gain factor k, and on threshold voltage, in case of pmos it almost is half of maximum voltage permitted by technology 3.3V. Another important information that we extract from measurement is the fact that gain factor k at 4K is strongly dependent on geometry, this means that is not possible to extract a single k parameter and use it to design a whole integrated circuit with transistor different in size. For these reason we will use only one size for pmos and one for nmos to synthesize a whole amplifier.

3.2.1 Gate and Junction capacitance

In a mosfet the gate capacitance is essentially the capacitance between the gate polysilicon (or metal) and bulk. In a nmos if the gate voltage is below zero the holes that are majority in bulk accumulate in the gate interface, and the thickness of gate oxide is the effective thickness of capacitance, but if we reduce the temperature the bulk becomes almost an insulator due to freeze-

Type	$\frac{W[\mu m]}{L[\mu m]}$	$K_N(\lvert K_P\rvert)^{300K}$	$K_N(K_P)^{4.2K}$	$\lvert V_{TH}\rvert[V]^{300K}$	$\lvert V_{TH}\rvert^{4.2K}[V]$
N	50/1.4	74.7	4000	0.46	0.88
N	50/4.2	93.3	1500	0.44	0.67
N	20/7	119.2	879	0.47	0.64
N	0.4/0.35	57.9	277	0.45	0.67
P	50/0.7	32.9	220	0.71	1.33
P	50/1.4	40.1	397	0.725	1.36
P	50/4.2	44.73	467	0.74	1.4
P	80/14	48.87	354	0.67	1.4
P	0.4/0.35	42.12	123	0.70	1.37
P	1/14	33	175	0.73	1.45

Table 3.2: Extracted parameter for mosfet at 300K and 4.2K, k_p and k_n are expressed in module in A/V^2

out of carriers so the holes have difficulty to accumulate on the interface and the effective thickness increase and as consequence the gate capacitance at cryogenic temperature reduces (figure 3.9). On the other hand if gate voltage is positive the electrons accumulate under the gate leading almost to the same capacitance (now called strong inversion capacitance). The electrons come from source and drain where are the majority carriers. Thanks to the high doping level of source and drain region, they maintain free electrons also at cryogenic temperature allowing the formation of the conductive channel below the gate contact. In figure 3.9 there is a measure taken from [38] that shows how accumulation capacitance($V_{GS} < 0$) reduce drastically from 300K to 4.2K while strong inversion capacitance ($V_{GS} > 0$) still remain almost constant.

For junction capacitance the dielectric is the space charge region between n and p region, the thickness of it is due to the equilibrium between drift and diffusion, at cryogenic temperature the diffusion of carrier is inhibited and so the drift take place and enhance the space charge carriers (figure 3.10) as result the equivalent dielectric become thicker and junction capacitance decrease.

3.2.2 Coupling

One of the most improvement in integrated circuits is the capability to obtain an high matching between mosfet pair. In table 3.2 we can calculate the dispersion at room temperature of both on k parameter and threshold voltage V_{TH} resulting about 10%. The dispersion on k is mainly due to different effective geometries, for V_{TH} also process parameter may overcome; by common centroid topology it's possible to reach coupling between two idential mosfet

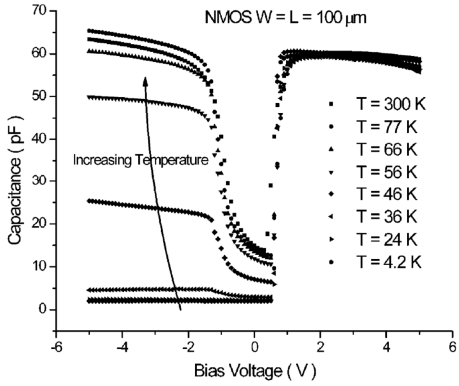

Figure 3.9: Gate capacitance versus gate voltage in a nmos $100\mu m$ x $100\mu m$, the accumulation capacitance (negative gate voltages) reduces from 300K to 4.2K, while strong inversion capacitance (positive voltages) still remain the same [38].

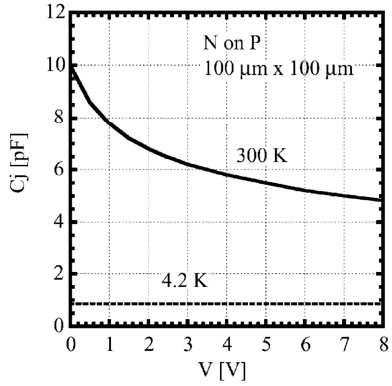

Figure 3.10: Junction capacitance on diode reduces at low temperature because the diffusion of carrier is inhibited and so the space charge region is enhanced by drift reducing the capacitance [38].

in the range of 1%.

May be natural to think that when lowering the temperature the coupling between two transistor, does not change; but let refer to figure 3.11. The right mosfet is in transdiode configuration and can read the current I_{IN} generating a specific V_{GS}. The gate-source voltages for both transistor are the same and using transistor with the same W/L, the current I_{IN} is mirrored in left transistor; this is a current mirror a fundamental block for integrated circuits.

When the input current is reduced in way that the overdrive voltage of input transistor becomes similar to thermal voltage $kT/q = 25mV$ at 300K, a sub-threshold effect take over, and the current becomes driven by diffusion into the channel following the red curve in figure 3.12, the current become exponential with gate voltage (the linear behavior in logarithmic scale). But the diffusion is deeply reduced at cryogenic temperature, as see in figure 3.12, the 4K curve has a higher slope in sub-threshold region than 300K curve. So in sub-threshold region the current is very sensitive to voltage changing. If this small current flow in the input transistor of current mirror (figure 3.11); the output current is driven by gate voltage of so small difference in ΔV_{TH} between transistors may provoke huge difference in current ΔI_D. Has been proved [39] that coupling of current mirror at 4K may reach 6% in comparison with 1% at room temperature. If more coupling is required the cryogenic

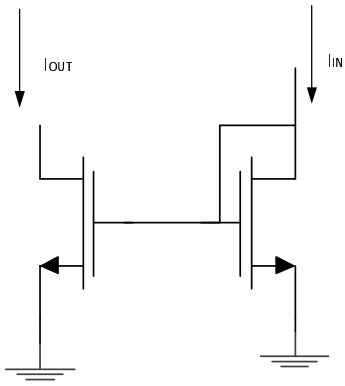

Figure 3.11: Current mirror; as the gate to source voltage is the same for both transitor, the input current is mirrored in output branch, with a error about 1% obtained a good matching of mosfet layout.

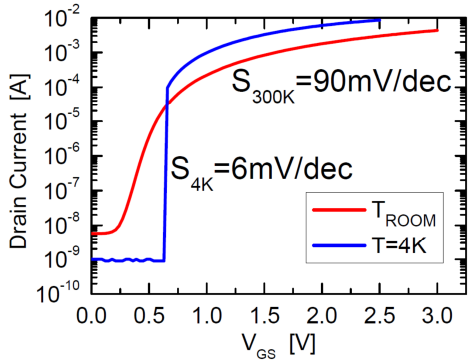

Figure 3.12: Measure of transcharacteristic of a nmos $50\mu m/4.2\mu m$, we see the inhibition of sub-threshold current.

transistor should always avoid the sub-threshold region.

3.2.3 Noise

The noise of a mosfet transistor is composed by two terms; a flicker and a thermal noise, according to well-known noise model [40]:

$$\begin{aligned} \frac{S^2_{Thermal}}{\Delta f} &= \frac{2}{3} 4kTg_m \\ \frac{S^2_{Flicker}}{\Delta f} &= \frac{1}{C_{ox}WL} \cdot \frac{K_F I_d^{AF}}{f} \end{aligned} \tag{3.3}$$

in which k is Boltzmann constant, T is temperature, g_m is the transconductance, C_{ox}, K_F and A_F are technology parameter, W and L are the gate dimension of transistor. At cryogenic temperature the thermal noise reduces drastically, while flicker noise does not have an explicit temperature dependence. In figure 3.13 there is the noise spectrum in function of temperature from 300K to 4K. We can take note of increasing of flicker noise while thermal noise is beyond the measurable frequency range in our setup (3.1) becomes unmeasurable due to the limit bandwidth and to huge presence of disturbs. However as the thermal noise is a thermodynamic process we may be confident that it follow equation 3.3 also at 4K. On the other hand flicker noise is due to

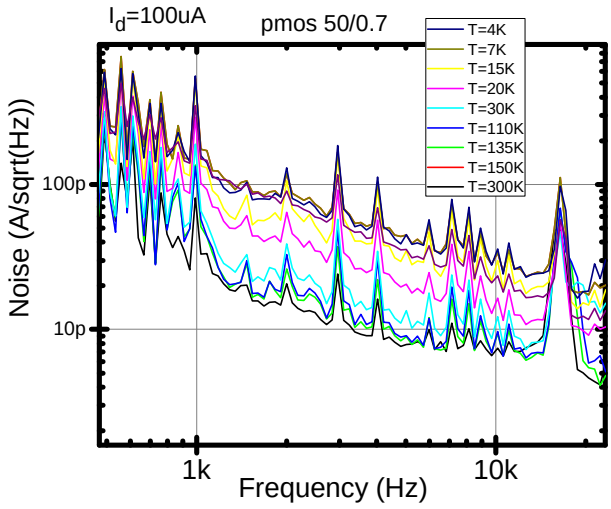

Figure 3.13: Noise spectral density of pmos $50\mu m/p.7\mu m$ at constant $I_d = 100\mu A$, the flicker noise raise of value 31.28 in spectral power from 300K to 4.2K.

the capture and release of carriers by traps into gate oxide. Since at 4K the carrier mobility is improved, the number of carriers request for a given current is less than at room temperature. Consequently, the effect of the capture/release of a single carrier has a bigger effect on the current increasing the noise [41]. The increment factor is 5.6 and so $({}^{4k}K_F) = 5.6^2 \cdot ({}^{RT}K_F) = 31.28({}^{RT}K_F)$ in which ${}^{RT}K_F$ is the K_F parameter at room temperature.

3.2.4 Guard Ring

Both the hysteresis effect and kink effect of mosfet transistor at 4K are mainly due to the impedance of bulk; if we reduce the bulk impedance these effects should be reduced. In figure 3.14 there is the characteristic of pmos $50\mu m/0.35\mu m$ in which the bulk is connected by a contact at about $5\mu m$ distance hysteresis and kink are present and affect dramatically the mosfet behavior. In figure 3.15 there is the same mosfet with a guard ring around it; both hysteresis and kink effects disappear totally, thanks to smaller resistance of bulk even at 4K. Guard ring so can deeply reduce the impact of kink and hysteresis effect typical in 4K temperature.

3.3 Integrated Resistors

We report here the data related to the measured integrated polysilicon resistors, that is the I-V curves at room temperature and at the liquid helium

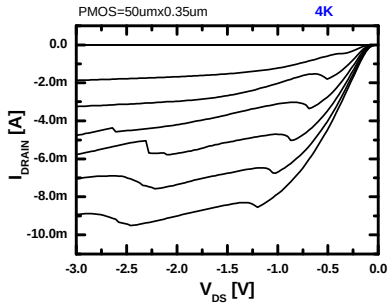

Figure 3.14: Characteristic of pmos $50\mu m/0.35\mu m$ with contact bulk at $5\mu m$ distance.

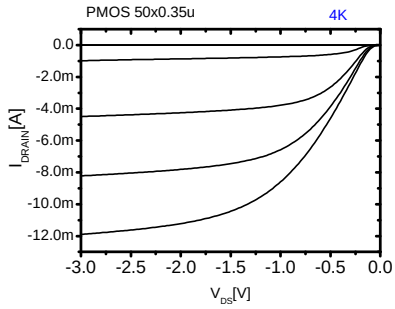

Figure 3.15: Characteristic of pmos $50\mu m/0.35\mu m$ with guard ring. Hysteresis and Kink effects disappear

temperature. We will also focus on the linearity issue at low temperature. In Figures 3.16 and 3.17 we report such I-V curves: it is worth noting that the low temperature causes a increasing R value in both cases by a factor 2.4 . Moreover the $R = 1M\Omega$ resistor in Fig. 3.16 keeps almost constant its R value at low temperature within the whole voltage range, while some of $R = 50k\Omega$ in Fig. 3.17 show a marked non-linearity at $T = 4.2K$, in particular tight polysilicon resistor show more non linearity . Such behavior may be divided into two main zones: a low-field and a high-field zone. Within the latter the dissipated power is high and this results into a resistor self-heating, producing as a consequence, an increasing conductivity and hence a decreasing resistance. The low-field in the former zone is not enough for self-heating to take place, resulting into a higher R. Some extracted parameters are collected in table 3.3. The high-field values of R are 2%, 27% and 4.7% of their corresponding low-field values, respectively; the non-linearity is thus negligible for high values of resistance or resistors with width greater than $10\mu m$.

3.4 Integrated Capacitors

The characterization at low temperature compared to the T_{ROOM} data has been made on an integrated capacitor as well. In particular the selected polysilicon capacitor is characterized by a nominal $C = 85pF$; by applying a $V_{AC} = 0.5V$ at $f_1 = 100kHz$ and $f_2 = 1kHz$. Data are reported in figure 3.18 within the range $4.2K \leq T \leq 300K$. It is apparent that the C value being almost constant over the whole temperature range, except for T very close to the He/sample contact at which C slightly decreases. However such C decrease is just two units pF and can be thus neglected. This prove that at

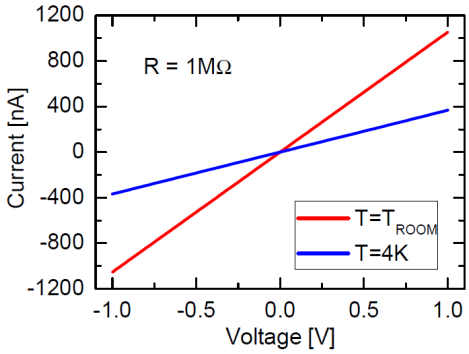

Figure 3.16: Integrated polysilicon resistor, $R = 1M\Omega$, $W = 1\mu m$, $L = 613\mu m$

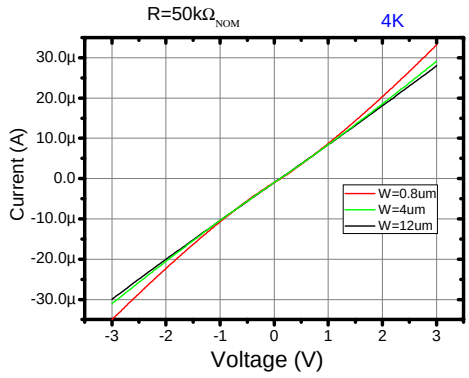

Figure 3.17: IV of three polysilicon resistor with same nominal value $50k\Omega$ but different width $0.8\mu m$,$4\mu m$ and $12\mu m$. Non-linear behavior at $T = 4.2K$ is reduced over a $10\mu m$ width.

4K the polysilicon still remains full of charges.

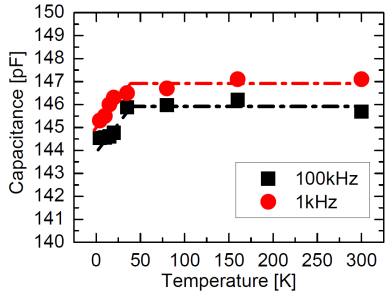

Figure 3.18: Capacitor measurement from 300K to 4.2K: capacitance keeps almost constant within the whole temperature range. There is a parallel parasitic capacitance due to wires which contributes to the measured value.

3.5 Conclusion

In this chapter was presented the characterization of cmos technology at 4 Kelvin, this because foundry do not provides valid model under 300 Kelvin. Our aim is to develop electronics circuit able to work at 4 Kelvin to be use inside a cryostat, reducing the input capacitance and improving the performances of measurement. In next chapter we will see how to join the charac-

$R_{NOMINAL}$	$1M\Omega$ (Fig. 3.16)	$50k\Omega$ (Fig. 3.17)	$50k\Omega$ (Fig. 3.17)
$W[\mu m]$	1	0.8	12
$L[\mu m]$	613	25	491
R^{300K}_{Meas}	$950k\Omega$	$49.994k\Omega$	$49.675k\Omega$
$R^{4.2K}_{Meas}$ (LF)	$2.75M\Omega$	$105.062k\Omega$	$106.38k\Omega$
$R^{4.2K}_{Meas}$ (HF)	$2.69M\Omega$	$77.841k\Omega$	$101.39k\Omega$
$R^{300K}_{Meas}\left[\frac{k\Omega}{\square}\right]$	1.63	1.38	1.2
$R^{4.2K}_{Meas}\left[\frac{k\Omega}{\square}\right]$	4.4	3.360	2.602

Table 3.3: Integrated resistor geometry and parameters measured at room temperature and at $T = 4.2K$ divided into Low-Field (LF) and High-Field(HF) behavior.

terization done here for cryogenic circuits synthesis.

Chapter 4

Cryogenic Cmos Amplifiers

In the previous chapter we presented the results of the characterization of a cmos technology at 4 Kelvin. Now we'll present the synthesis of an amplifier attached near the sample inside the cryostat, to reduce the impact of input capacitance as told in chapter 2. We'll describe the state of art of cryogenic amplifier and then the design, realization and characterization of our cryogenic amplifier making notice the advantages and disadvantage respecting room temperature system.

4.1 State of the art

The state of the art on cryogenic amplifier can be identified with the work cited in [42]. It is based on two stages amplifier chain (figure 4.1), one current amplifier at low temperature based on an HEMT (High Electron Mobility Transistor) and a transimpedance amplifier AC coupled at room temperature. The bandwidth is from 1.2kHz up to 2MHz, with a noise floor of $130fA/\sqrt{Hz}$ equivalent to $180pA_{RMS}$. This circuit has some disadvantage: it's a open loop system and the gain is dependent on the parameters of an active devices (Hemt) that can vary a lot; moreover biasing of HEMT requires an AC coupling, making impossible DC measurement like those for stability diagram of quantum dots.

Another example of cryogenic circuit is in figure [43], is a transimpedance amplifier in which they cool the feedback resistor to achieve less thermal noise; but the input capacitance it's not reduced and limits performances at high frequency.

Hemt transistors are used in wide kind of cryogenic amplifier working up to 4K for RF measurement like [44] and [45]. But also cmos has good diffusion like in [46] in which a cryogenic ADC in cmos technology is developed but also

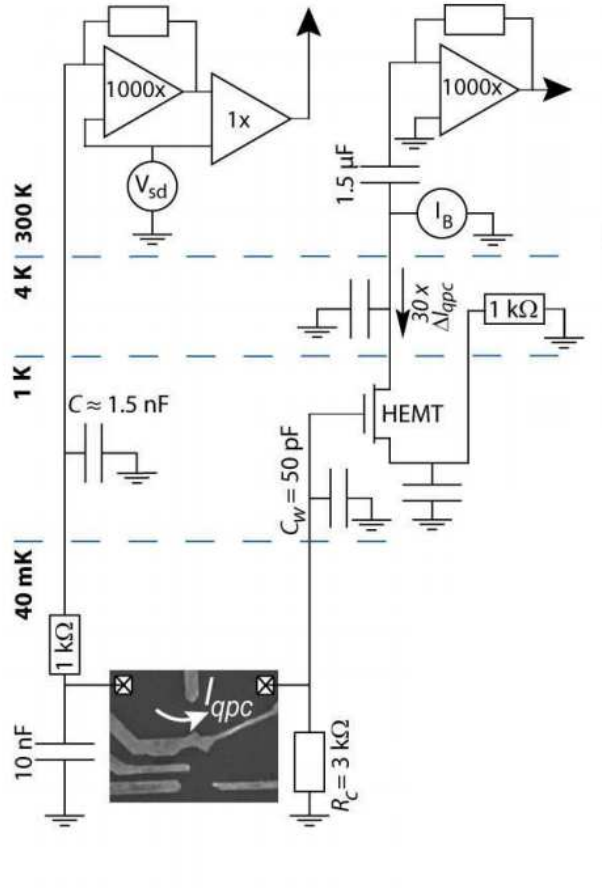

Figure 4.1: Schematic of in [42], the current on quantum dot is amplified with gain 30 by the $3k\Omega$ resistor and Hemt. Then the current is read by a room temperature transimpedance amplifier ac coupled.

other components have been developed [47] [29]

4.2 Multi temperature Cryogenic amplifier

Once presented in the third chapter the characterization of cmos technology $0.35\mu m$, it's now possible to use the extracted parameters (resumed in table 4.1) to enjoy the advantage of cryogenic temperature. Our aim is reduce the input capacitance by reducing the length of the wires and so their parasitic capacitances, the main scheme is shown in figure 4.2; a classic transimpedance amplifier (figure 2.2) in which the opamp is split in two blocks one is at low temperature region G_1 and the other at room temperature G_2; G_1 should have

	$K_n(K_p)$	V_{TH}	λ
Nmos $50\mu m/1.4\mu m$	$4mA/V^2$	0.88V	$0.0102V^{-1}$
Pmos $50\mu m/0.7\mu m$	$-220\mu A/V^2$	-1.3V	$0.059V^{-1}$

Table 4.1: Resume of mosfet parameters at 4.2K extracted in chapter 3.

has sufficient gain to reduce the impact of noise sources coming from G_2, while G_2 provides the gain required by the feedback structure.

The parameter extracted for cmos transistor are valid only on a specific geometry otherwise the parameters have huge differences. For this reason the design of the amplifier stage at cryogenic temperature may be hard, it's simpler use a single transistor amplifier stage for G_1 but it suffers of a limited gain[1] compensated by high temperature stage G_2. In order to reduce input capacitance, the feedback capacitor and resistor must be placed in 1.5K region.

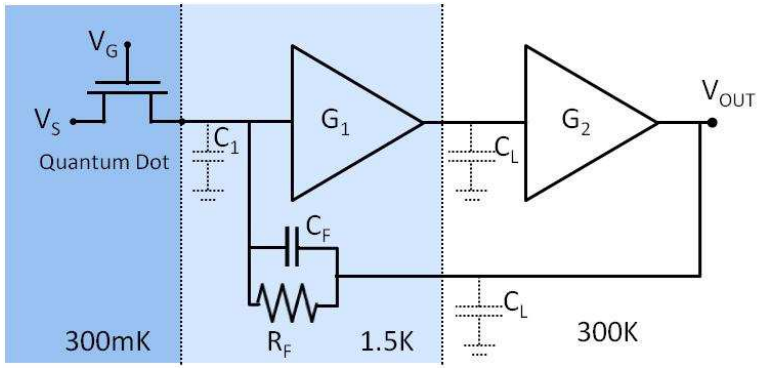

Figure 4.2: A multi-temperature cryogenic transimpedence amplifier, the opamp is composed by two stage: one at 1.5K (G_1) and the other at 300K (G_2), in this way the input parasitic capacitance is reduced as the input current wire does not reach 300K region. Gain of G_1 should be high enough to reduce the noise of G_2 which provides the requested gain for feedback.

The most common single transistor voltage amplifier is common source amplifier, see figure 4.3: the input voltage signal is applied on the gate of a mosfet in which the source is at fixed voltage (typical V_{dd} for Pmos and ground for Nmos) and the drain it connected to a load resistor. A small voltage signal δv_{gs} on gate of transistor modify the gate to source voltage, the drain current

[1]The maximum gain of a single transistor stage is $g_m R_o$, the R_o at cryogenic temperature is reduced because λ is increased and $R_o = 1/(I_d\lambda)$

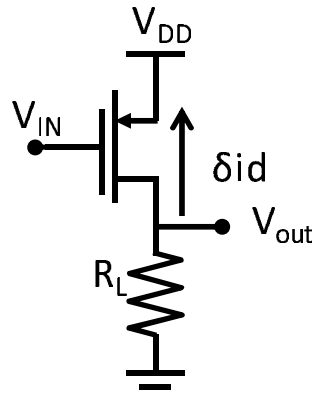

Figure 4.3: Common source stage, the input voltage signal induce a current signal on mosfet $i_d = g_m v_{gs}$ than this current flows on resistance R_l leading a output voltage $v_{out} = -i_d R_l = -g_m R_l \cdot v_{in}$.

variation signal may be calculated:

$$\delta i_d = \delta\left(\frac{1}{2}|k_p|\frac{W}{L}(|V_{gs}| - |V_{th}|)^2\right) = |k_p|\frac{W}{L}(|V_{gs}| - |V_{th}|)\cdot\delta v_{gs} = g_m \delta v_{gs} \quad (4.1)$$

in which capitol V_{gs} is the bias voltage on gate, V_{th} is the threshold voltage $K_p W/L$ is the gain factor of transistor and g_m is his transconductance. The voltage gain between input and output result $G = \delta v_{out}/\delta v_{in} = -g_m R_l$ as much the gain is high as the impact of noise of room temperature electronics is reduced, the same analysis is valid also for Nmos-based common source stage.

The stage in figure 4.3 it's a good candidate for block G_1 in figure 4.2 because it's composed by only one transistor and his input noise is lower than a differential input stage at fixed power consumption because only one transistor in involved in noise spectra; the choice of Pmos instead Nmos it's motivated by observing that white noise scales in temperature and we expect a dominance of flicker noise that is lower in Pmos respect Nmos. The schematic of our multi-stage transimpedance amplifier is in figure 4.4; the output node of common source stage correspond to the node between G_1 and G_2 in figure 4.2, this is the node that connects the cryogenic and the room temperature stages; it's a long wire and we aspect on it a parasitic capacitance of about $C_l = 1nF$. The pole of common source stage (G_1) is $1/(2\pi R_l C_l)$ is at low frequency because C_l is a large capacitance and R_l should be high to obtain enough gain, this frequency f_l will be at low frequency and may affect the stability because in G_{LOOP} is present another low frequency pole due to G_2 composed by a commercial operation amplifier. We have to push the f_l pole towards higher frequency to

obtain a stable, high frequency amplifier; this concept will be clarified later.

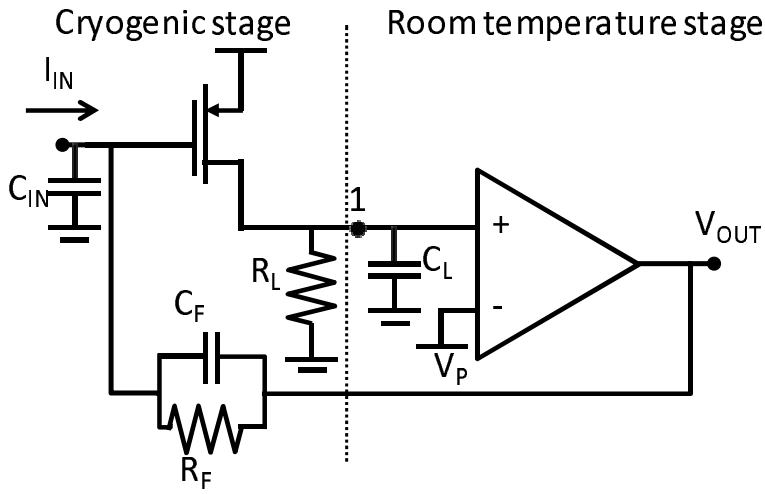

Figure 4.4: A multi-temperature cryogenic amplifier, a transimpedence amplifier uses two gain stages: one at 4K and one at 300. The low temperature stage is a common source while at room temperature a opamp is used to provide the requested gain for feedback, in this way the input parasitic capacitance is reduced as the input current wire does not reach 300K region so its have less parasitic capacitance.

The solution we propose for increasing the frequency of f_l is to use a room temperature cascode transistor (figure 4.5) in this way the impedance of the node 1 is reduced because it's connected to source of cascode mosfet; but the signal current can flow on it without being affected and than on the load resistor. The pole introduced by C_1 is pulled at high frequency because his equivalent resistor is $1/g_{mc}$ that can be reduced without modifying the gain determined by $G = g_m R_l$; on the other hand in G_{loop} another pole due to R_l is added but in this case the parasitic capacitance on it it's lower because the wire can be small. The signal between the cryogenic and room temperature stages is no longer a voltage signal (which requires a high impedance for obtain sufficient gain) but it's a current signal, in particular equivalent to the voltage on gate on transistor of G_1 multiplied by his transconductance g_m. The translation of current signal in voltage signal happens on non inverting terminal through resistance R_L. So the gain is the same $G = -g_m R_l$.

So the cascode decouples the big capacitance C_1 due to the long wire connecting cryogenic e room temperature circuits and the gain resistance R_l; does't it possible to use the same trick to masks the input capacitance in room temperature amplifier (described in chapter 2), the answer is no because in standard transimpedance amplifier a input cascode leaves on the Dut an uncontrolled bias voltage equivalent to V_{gs} of cascodes plus the gate bias. In

figure 4.5 In our circuit this is not a problem as long as the input cryogenic mosfet remains in saturation region.

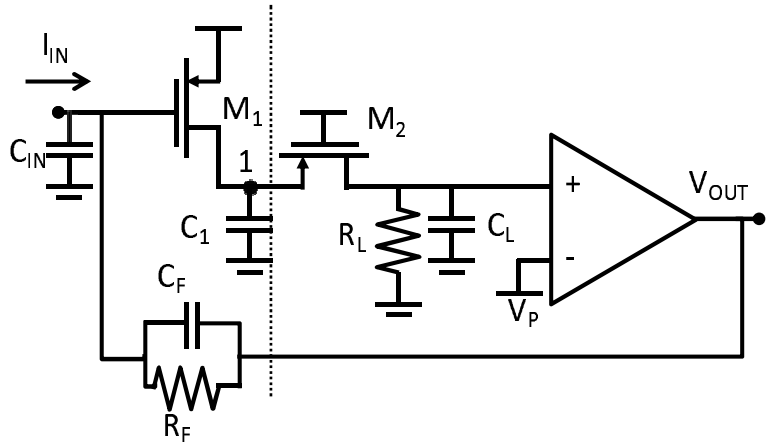

Figure 4.5: Using a cascode transistor between cryogenic stage and room temperature stage may increase the pole frequency introduced by C_1 decoupling it from load resistance R_l

The cryogenic stage G_1 is formed by only one Pmos, the room temperature stage G_2 is composed one resistor one transistor and one commercial opamp. The current bias of the cryogenic Pmos is determined by V_p by the relationship:

$$I_d = \frac{V_p}{R_L} \tag{4.2}$$

The bias current fixes the transconductance of first cryogenic mosfet according to the relationship:

$$g_m = k_p \frac{W}{L} \left(|V_{gs}| - |V_{th}| \right) = \sqrt{2k_p \frac{W}{L} I_d} \tag{4.3}$$

4.2.1 Input noise

We remember now that the most important improvement in use cryogenic circuits is reducing the input capacitance which limits the resolution in room temperature system (chapter 2). Now we'll calculate the equivalent input noise to prove the increased sensibility. In figure 4.6 there is the schematic in which we add noise sources, as told in section 2.2.1 the opamp can be modeled by two noise sources a voltage and a current source; called respectively series and parallel noise[2]

[2]Actually the required sources are three because we need two current noise sources on both terminals of opamp but the source on inverting input has no effects on noise.

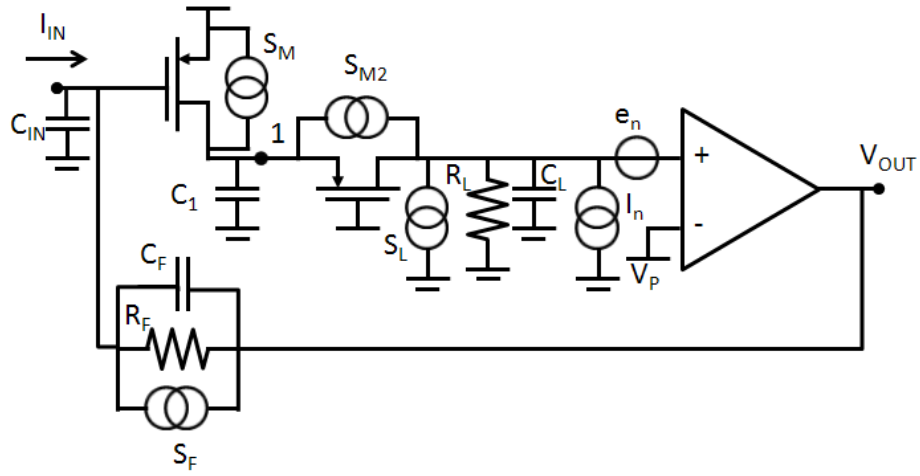

Figure 4.6: Schematic of multi-temperature cryogenic amplifier with noise sources. It's possible to join all contribute from G_1 and G_2 stages into a single equivalent voltage noise source S_g placed in input of G_1.

First of all we calculate the input noise of block composed by G_1 and G_2 called S_G neglecting the feedback $R_f C_f$ and then we'll calculate the total noise considering feedback and only S_G as total noise of G_1 and G_2 . The noise S_G can be calculated by valuate for every noise sources the output contribute and summing their power and then calculating the equivalent input voltage noise source S_G:

$$\begin{aligned} S_G^2 &= S_m^2 + \frac{4kT}{R_l}\frac{1}{g_m^2} + \frac{2}{3}4kTg_{m2}\left(\frac{1/g_{m2}}{1/g_{m2}+1/sC_1}\right)^2 \cdot \frac{1}{g_m^2} + \frac{I_n^2}{g_m^2} + \frac{e_n^2}{g_m^2 R_l^2} \\ S_m^2 &= \frac{2}{3}\frac{4kT^*}{g_m} + \frac{A_m}{f} \\ e_n^2 &= e_b^2 + \frac{A_v}{f} \end{aligned} \tag{4.4}$$

In which S_m is the noise due to cryogenic mosfet both flicker and thermal, g_m is the transconductance of cryogenic mosfet, I_n is the current noise of room temperature opamp, e_n is the voltage noise of room temperature opamp composed by white noise e_b and flicker noise A_v/f, g_{m2} it the transconductance of cascode mosfet, T is room temperature while T^* is the temperature for cryogenic part (4.2K).

Then the feedback net is added and the entire noise of G stage can be modeled with only S_G; the noise of the entire system can be calculated considering the noise from feedback resistor and the noise of G stage calculated

in equation 4.4; we neglect the current noise of cryogenic Pmos, negligible in cmos technology, related to the shot noise due to gate leakage. The total input noise of our cryogenic transimpedance amplifier is:

$$S_i^2 = \frac{4kT}{R_f} + s^2 C_{in}^2 S_G^2 + \frac{S_G^2}{R_f^2} \tag{4.5}$$

rearranging the equation 4.4 and substituting in equation 4.5 we can identify in S_i^2 5 different behavior in frequency:

1 over f components $\left(\frac{A_m}{R_f^2} + \frac{A_v}{g_m^2 R_l^2 R_f^2}\right)\frac{1}{f}$

White components $\frac{4kT^*}{R_f} + \frac{2}{3}\frac{4kT^*}{g_m R_f^2} + \frac{4kT}{R_l R_f^2}\frac{1}{g_m^2} + \frac{I_n^2}{g_m^2 R_f^2} + \frac{e_b^2}{g_m^2 R_l^2 R_f^2}$

F components $4\pi^2 f\left(A_m C_{in}^2 + \frac{A_v C_{in}^2}{g_m^2 R_l^2}\right)$

F square components $4\pi^2 f^2 C_{in}^2\left(\frac{2}{3}\frac{4kT^*}{g_m} + \frac{4kT}{R_l}\frac{1}{g_m^2} + \frac{I_n^2}{g_m^2} + \frac{e_b^2}{g_m^2 R_l^2}\right)$

Cascode noise $\left(s^2 C_{in}^2 + \frac{1}{R_f^2}\right)\left(\frac{2}{3}\frac{4kT}{g_{m2} g_m^2}\frac{s^2 C_1^2}{\left(1+s\frac{C_1}{g_{m2}}\right)^2}\right)$

starting from the specification introduced in chapter 2: $10fA_{RMS}$ over 10Hz bandwidth, we are able to determine the maximum acceptable white noise density by the relationship:

$$S_{max} = \frac{10fA}{\sqrt{10Hz}} = 3.16f\frac{A}{\sqrt{Hz}} \tag{4.6}$$

and considering only the first term of white component because the others can be neglected if $G_1 = g_m R_l$ is sufficiently higher than 1 and assuming $R_f >> 1/g_m$; we can design the feedback resistor by:

$$R_f = \frac{4kT}{\left(3.16f\frac{A}{\sqrt{Hz}}\right)^2} = 22.6M\Omega \tag{4.7}$$

for a room temperature system described in chapter 2 the required feedback resistor was $10G\Omega$, in this case thanks to thermal noise reduction due to cryogenic temperature the requested resistor reduced to $22M\Omega$ with same resolution but with benefits in term of bandwidth and maximum current allowable. By tuning g_{m2} is possible to reduce the impact of cascode noise, and with $g_m R_l$ and the we can find the minimum noise sufficient high can help to find the minimum of noise; the root mean square of noise is obtainable by square root of S_i^2 over the bandwidth of signal. So before determining the resolution we had to calculate the bandwidth of the signal in our amplifier.

4.2.2 Stability

The loop gain of our system determine the bandwidth and also the stability performances it can be easily calculated by cut the loop for example in output node and see the transfer function of a signal crossing the loop neglecting C_{1-2}, referring to figure 4.5 the results is:

$$G_{loop} = \frac{-A_0}{1+s\tau_0}\frac{1+sR_fC_f}{1+sR_f\left(C_{in}+C_f\right)}\frac{g_m}{1+\frac{sC_1}{g_{m2}}}\frac{R_l}{1+sR_lC_l} \tag{4.8}$$

in which we suppose the opamp to be at single pole with dc gain of A_0 and pole with time constant τ_0, the capacitance of output node is charged ideally by opamp output and can be neglected; pole due to C_1 capacitance is pulled at high frequency by cascode transistor M_2, in fact the source of M_2 reduces the impedance of node 1, this is the long wire coming from cryogenic section and has a huge capacitance.

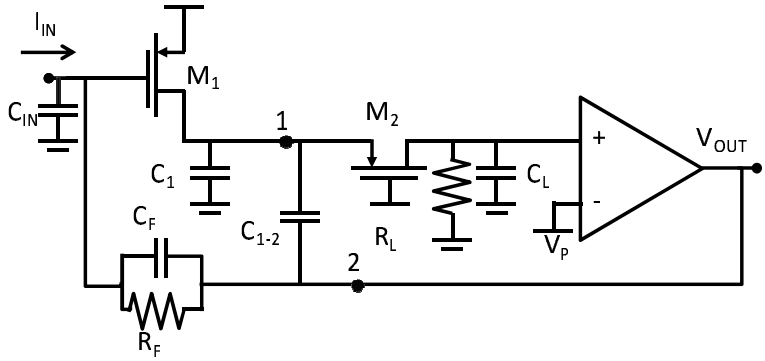

Figure 4.7: Schematic for loop gain calculation; the a crosstalk capacitance reduces the stability because it adds a right half plane zeros due to the inverted parallel path.

But in our calculus we use only parasitic capacitance to ground, but a better modeling considers also the coupling capacitance between wires 1 and 2. In figure 4.7 we consider also a coupling capacitor C_{1-2} between node 1 and output node, the effect of wire on cryogenic transistor's source is neglected because it's a supply node so is like ground for parasitic capacitance. The G_{loop}

considering also C_{1-2} is quite complex and results:

$$G_{loop} = -g_m \frac{A_0}{1+s\tau_0} \cdot \frac{R_l}{1+sR_lC_l} \cdot \frac{1}{1+s\frac{C_1}{g_{m2}}} \cdot \frac{T(s)}{(1+sR_f(C_{in}+C_f))\left(1+s\frac{C_{1-2}+C_1}{g_{m2}}\right)}$$

$$\begin{aligned} T(s) = 1 &+ s\left(\frac{C_1+C_{1-2}}{g_{m2}} + R_fC_f - \frac{C_{1-2}}{g_m}\right) + \\ &+ s^2\left(\frac{R_fC_f}{g_{m2}}(C_{1-2}+C_1) - \frac{C_{1-2}C_1}{g_{m2}g_m} - \frac{C_{1-2}R_f(C_{in}+C_f)}{g_m}\right) - \\ &- s^3R_f(C_{in}+C_f)\frac{C_{1-2}C_1}{g_{m2}g_m} \end{aligned} \tag{4.9}$$

If we consider frequencies in which $sR_fC_f >> 1$ and $s^2(C_{1-2}C_f)/(g_{m2}g_m) << 1$ the G_{loop} can be approximed with:

$$G_{loop} = g_mR_lA(s)\frac{-C_f}{C_{in}+C_f}\frac{1-s\frac{C_{1-2}(C_f+C_{in})}{g_mC_f}}{1+s\frac{C_1+C_{1-2}}{g_{m2}}} \tag{4.10}$$

so in this case appears a zero in right half plane, considering $C_{1-2} = 100pF$ $g_m = 1.2mA/V$ $C_{in} = 50pF$ and $C_f = 500fF$ the zero is at frequency of 19kHz. This is a right half plane zero so after his frequency the phase of loop gain loses 90°; this effect has negative influence on stability because the main parameter describing the stability is phase margin defined as the phase of G_{loop} at frequency f_t in which $|G_{loop}| = 1$. It has to be bigger than 45° for a stable amplifier. The signal bandwidth is 14kHz due to C_f and R_f assuming that f_t is a decade far from signal bandwidth so at 140kHz the phase and considering only right half plane zero and dominant pole from opamp, at f_t is around 7° insufficient for stability, moreover the increased slope on magnitude due to right half plane zero can push the cut-off frequency f_t at higher frequency where non dominant pole may affect further on the phase margin.

Looking at relationship in 4.10 the zero can be carried at higher frequency only by increasing C_f, reducing the signal bandwidth, or by increasing the bias current but this is not possible due to dissipation limit. The current bias should increase of 100 factor to obtain a zero in 100kHz range, is very hard to do so, due power consumption.

The sign of the zero is caused by the different sign between nominal and parasitic signal paths at 4K. The voltage signal from node 2 to node 1 goes with sign plus when passing through capacitance C_{1-2} and C_1 and with a minus sign when passing through cryogenic Pmos; so it's not possible eliminating it by changing the room temperature stage because always we will have this

different behavior; we had to change the cryogenic stage in way to obtain a positive sign into from signal path.

4.3 Source follower

Our idea to solve the sign question in cryogenic stage is to use, instead of common-source stage, a source follower stage, as show in figure 4.8. A Pmos is biased through a current source at room temperature; in this way there is a positive gain between input signal and output signal in cryogenic stage. We expect a negative half plane zero which increase the phase by 90° instead reducing it. The loop gain result:

$$G_{loop} = \frac{-A_0}{1+s\tau_0} \frac{1 + s\left(R_f C_f + C_{1-2}/g_m\right) + s^2 R_f C_{1-2}\left(C_{in}+C_f\right)/g_m}{\left(1 + s\frac{C_{1-2}+C_1}{g_m}\right)\cdot\left(1 + sR_f\left(C_{in}+C_f\right)\right)} \quad (4.11)$$

In this case the cascode is not useful because the node 1 is yet low impedance thanks to cryogenic Pmos transistor, so the pole associated with it is a high frequency even in presence of big capacitance C_1.

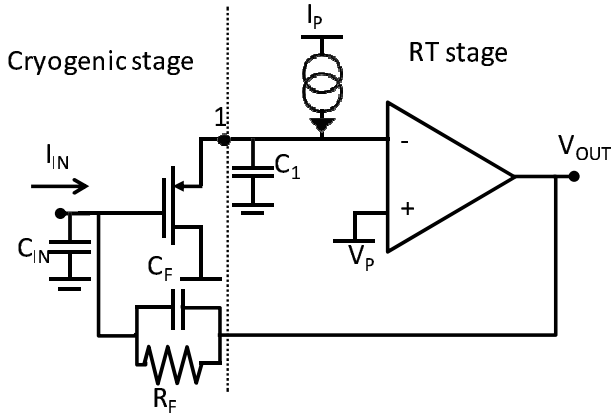

Figure 4.8: A cryogenic transimpedance amplifier using a source follower instead of a common source, in this way the sign of signal path in cryogenic stage is positive. The zero introduced by parasitic capacitance improves the stability.

From the numerator in equation 4.11 we see that our circuit has two zeros with negative real part and considering the values estimated before $R_f = 22\Omega$ $g_m = 1.2mA/V$, $C1-2 = 100pF$, $C_{in} = 50pF$ and $C_f = 0.5pF$ the zeros result complex conjugated because it's verified the following relationship:

$$R_f C_f^2 - \frac{C_{1-2}C_{in}}{g_m} < 0 \quad (4.12)$$

and their module results 17kHz, the pole instead are at $f_{p1} = 1/(2\pi\tau_0)$, $f_{p2} = 1/(R_f(C_{in} + C_f)) = 144Hz$ and $f_{p3} = g_m/(2\pi(C_1 + C_{1-2})) = 188kHz$. The G_{loop} graph is shown in figure 4.9 we supposed a single pole opamp whose pole is the lowest, the cut-off frequency is:

$$f_t = \frac{A_0}{2\pi\tau_0} \cdot \frac{C_{1-2}}{C_{1-2} + C_1} = \frac{GBWP_{op}}{11} \tag{4.13}$$

in which $GBWP_{op}$ is the gain bandwidth product of room temperature opamp. The phase contribute due to first two poles is in this configuration compensated by the zeros phase contributes. If the third pole is more than one decade far from f_t it can be neglected and the phase margin can be arrive up to 90° due to the remaining pole. So using a source follower the signal path and the parasitic path from C_{1-2} have the same sign and as consequence the zero interconnected with multi-path has real part negative and improves stability.

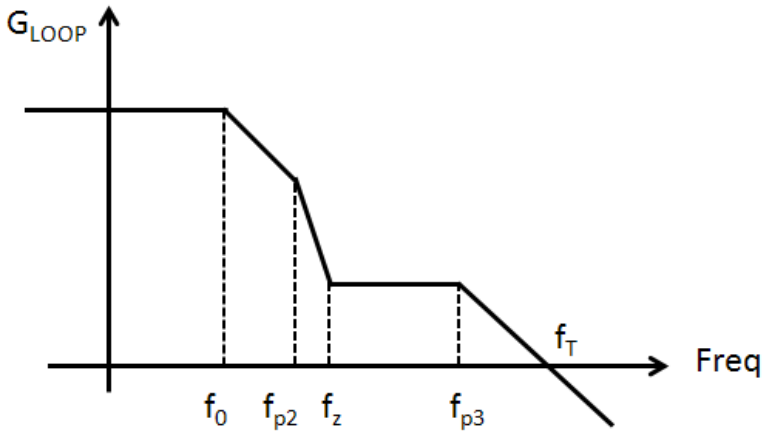

Figure 4.9: Graph of G_{loop} with source follower the first pole is due to opamp the second to resistor, in this case the zeros are on left half plane and improves stability. If the forth pole is one decade higher than f_t can be neglected and the phase margin reaches 90°.

In order to have a good feedback system in all frequencies up to f_t the gain of flat region of G_{loop} should be at least 10, as consequence f_t should be ten times far from f_{p3} so at 1.88MHz and according the equation 4.13, the requested gain bandwidth for room temperature opamp is about 20MHz, and it should be unitary gain stable to avoid the presence of poles near f_t.

But using a follower instead a common source amplifier reduces the gain: in a follower the gain is 1 at maximum where in a common-source stage the gain can be higher than 1, we have to demonstrate convenience of using a follower by analyzing the input noise. Otherwise use a multi-stage amplifier

has no improvement respect to room temperature system described in chapter 2.

4.3.1 Input noise

In figure 4.10 there is the schematic of our system in which the G_1 stage is implemented by a source follower and with the associated noise sources. As already said in this case the wire connecting the cryogenic and room temperature stage (node 1) is a low impedance due to source of cryogenic mosfet, we do not need a cascode which in common-source case had a significant contribute to noise.

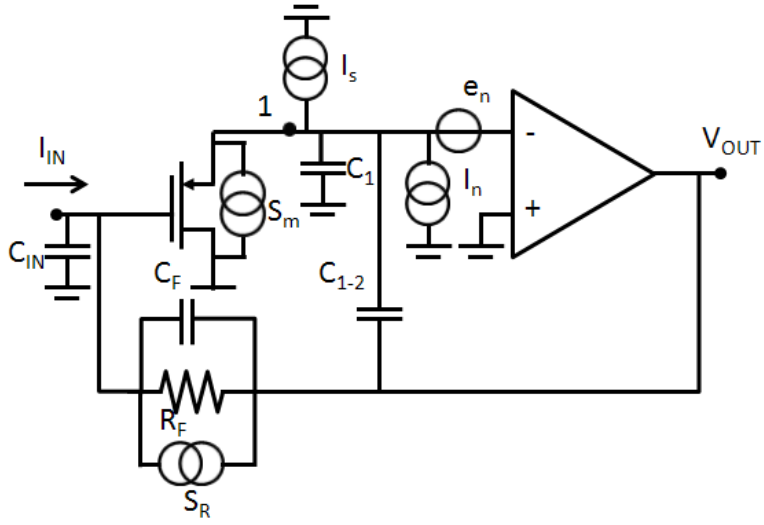

Figure 4.10: Noise sources in source follower based cryogenic amplifier. In this case we can eliminate the cascode avoiding his noise contribute.

The input noise of G stage is, like before, calculated by first calculating the contributes of every single noise sources in output than summing their power and referring the total noise in input all without considering the feedback. Once calculated the input total noise spectrum for G stage S_G, it's possible to add the feedback and calculate the total input noise of transimpedance amplifier. The noise of stage G_1 and G_2 results:

$$S_G^2 = \frac{2}{3}\frac{4kT^*}{g_m} + \frac{A_m}{f} + \frac{I_s^2}{g_m^2} + \frac{I_n^2}{g_m^2} + e_n^2\left(1 + s^2\frac{(C_{1-2}+C_1)}{g_m}\right) \tag{4.14}$$

in which the first two term are the thermal and flicker noise of cryogenic mosfet, the third is the noise associated with current generator, the others are the noise

due to room temperature opamp; e_n is composed by thermal and flicker noise as defined in equation 4.4. Now we can consider only the noise source S_G for G stage, add the feedback and calculate the input noise density:

$$S_i^2 = \frac{4kT^*}{R_f} + \left(\frac{1}{R_f^2} + s^2 C_{in}^2\right) S_G^2 \tag{4.15}$$

substituting 4.14 and 4.4 into 4.15 we obtain different component than can be resumed as:

1 over f components $\left(\frac{A_m}{R_f^2} + \frac{A_v}{R_f^2}\right)\frac{1}{f}$

white components $\frac{4kT^*}{R_f} + \frac{2}{3}\frac{4kT^*}{g_m R_f^2} + \frac{I_s^2}{g_m^2 R_f^2} + \frac{I_n^2}{g_m^2 R_f^2} + \frac{e_b^2}{R_f^2}$

f components $4\pi^2 f\left(A_m C_{in}^2 + A_v C_{in}^2 + \frac{(C_1+C_{1-2})^2 A_v}{g_m^2 R_f^2}\right)$

f square components $4\pi^2 f^2\left(C_{in}^2\frac{2}{3}\frac{4kT^*}{g_m} + C_{in}^2\frac{I_n^2}{g_m^2} + C_{in}^2\frac{I_s^2}{g_m^2} + C_{in}^2 e_b^2 + \frac{e_b^2(C_1+C_{1-2})^2}{g_m^2 R_f^2}\right)$

f third component $16\pi^4 f^3 \frac{A_v*(C_1+C_{1-2})^2 C_{in}^2}{g_m^2}$

f forth component $16\pi^4 f^4 \frac{C_{in}^2(C_1+C_{1-2})^2 e_b^2}{g_m^2}$

Focusing on white noise the contribute from feedback resistor is $3.16fA/\sqrt{Hz}$ with $R_f = 22M\Omega$; to make negligible the opamp noise it must be have the following conditions: $I_n << 90pA/\sqrt{Hz}$ and $e_n << 80nA/\sqrt{(}Hz)$ easily achievable with low noise opamp, also the current source must is $I_s << 90pA/\sqrt{Hz}$. In f square component the first term is dominant if $I_s, I_n << 530fA/\sqrt{Hz}$ and $e_b << \sqrt{8}kT * /3g_m = 0.33nV/\sqrt{Hz}$ it's hard to satisfy so it's probable that in f square component the series noise from opamp will dominate. Supposing $A_m » A_v$ because the opamp can be choose in Jfet technology that has lower flicker noise compared to cryogenic mosfet; and considering that $g_m R_f = 29 \cdot 10^3 >> 1$ the input noise spectra can be approximated with:

$$\begin{aligned} S_i^2 =& \frac{A_m}{f R_f^2} + \frac{4kT^*}{R_f} + 4\pi^2 C_{in}^2 A_m f + e_b^2 C_{in}^2 4\pi^2 f^2 + \\ &+ \frac{16\pi^4 A_v C_{tot}^2 C_{in}^2}{g_m^2} f^3 + \frac{C_{in}^2 {C_{tot}}^2 e_b^2}{g_m^2} 16\pi^4 f^4 \end{aligned} \tag{4.16}$$

in which $C_{tot} = C_1 + C_{1-2}$, according to models the A_m coefficient of a Pmos $50\mu m/0.7\mu m$ at 300 Kelvin with a bias of $I_d = 100\mu A$ is $4 \cdot 10^{-13} V^2$ and

considering the characterization done in chapter 3 we aspect that when the temperature reduces up to 4K, A_m results $A_m = 1.25 \cdot 10^{-11}$. The total input noise in term of root mean square depends on bandwidth of integration. In next section we determine those of our amplifier.

4.3.2 Bandwidth

The ideal gain of our transimpedance amplifier can be calculated by considering a ideal loop gain, so a infinite dc gain of opamp, the inputs terminal of room temperature opamp are exactly at the same voltage and the node 1 becomes a virtual ground, the ideal transfer function results:

$$G_{id} = \frac{-R_f}{\left(1 + \left(R_f C_f + \frac{C_{1-2}}{G_m}\right) s + \frac{R_f C_{1-2} C_{in}}{g_m} s^2\right)} \tag{4.17}$$

so in the ideal transfer there are a couple of poles complex conjugated. This may be affected the performances because a complex poles may introduce overshoot and response with damped oscillation. We impose a limit for overshoot in 10% so from system theory result that the damper factor, defined as ratio between real part and module of poles must be 0.7; analyzing the equation 4.17 system the damping factor results:

$$\xi = \frac{C_f}{2} \sqrt{\frac{g_m R_f}{C_{1-2} C_{in}}} \tag{4.18}$$

As $R_f = 22M\Omega$ for noise requirement, $C_{1-2} = 100pF$ and $C_{in} = 50pF$ for setup requirements, $I_m = 100\mu A$ for power dissipation; using a Pmos 50/0.7 the damping factor is 0.7 if the feedback capacitor is $C_f = 500fF$. The signal bandwidth result $\approx 1/(2\pi R_f C_f)$ =14kHz and this is not increasable by reducing C_f for two reasons first of all the parasitic capacitance on resistor can dominate, but also because with a lower C_f the response of amplifier would have higher overshoot instead to be faster.

4.4 Design of cryogenic amplifier

Once chose the topology and proved his functionality we are now ready to realized our amplifier. In figure 4.11 there is the complete schematic of the cryogenic amplifier realized; the current source it realized by a the drain of a bipolar transistor with a resistance on emitter, the bias current for cryogenic mosfet is defined by $I_d = (V_{dd} - 0.7V - V_B)/R_e$.

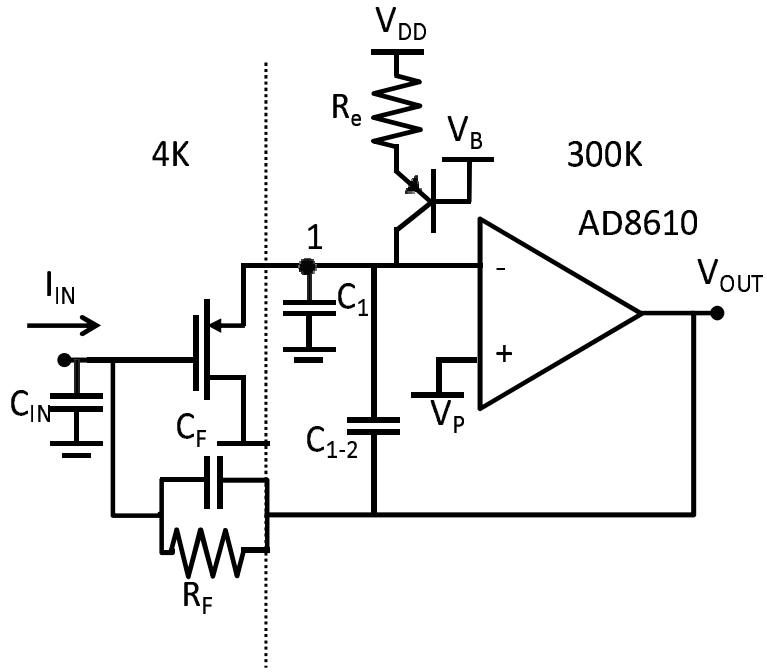

Figure 4.11: The complete schematic of the realized cryogenic amplifier, we use a bipolar to implement the current supply. The voltage V_p tune the V_{ds} voltage of cryogenic opamp.

We chose a commercial opamp by analog Device AD8610; it has a gain-bandwidth product of 25MHz stable unitary gain, satisfying our requirement of 22 MHz. It also has $6nV/\sqrt{Hz}$ and $1fA/\sqrt{Hz}$ of noise source.

Our system have been tested at room temperature and at 4.2Kelvin, in figure 4.12 there is the characteristic I-V at room temperature and at low temperature, the changed slope is due to the increased resistance due to temperature dependent. In figure 4.13 there is the noise density spectrum, at room temperature is thermal noise from resistance that dominates $\sqrt{4kT/R} = 40fA/\sqrt{Hz}$ and pole is at $1/(2\pi R_f C_f) = 16kHz$ in which $R_f = 10M\Omega$ and $C_f = 1pF$. At cryogenic temperature the thermal noises reduce drastically while flicker noise increases as expected according to discussion in section 3.2.3 the pole moves to 8kHz. The total noise is $1.3pA_{RMS}$ in about 10kHz bandwidth.

4.5 Conclusion

In this chapter we have designed, realized and tested a cryogenic amplifier, composed by two section. One at cryogenic temperature with a single transistor source follower stage; and the other at room temperature composed by

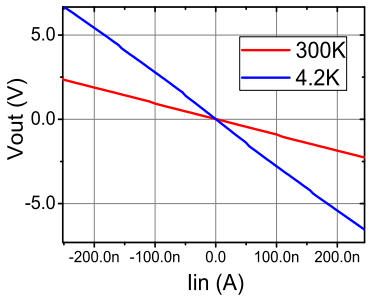

Figure 4.12: Characteristic of cryogenic amplifier, the different slope is due to different value of feedback resistor.

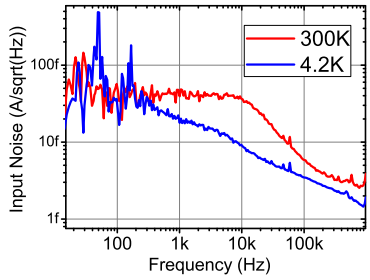

Figure 4.13: Input spectral density of noise of out amplifier, as expected the thermal noise reduce while flicker noise becomes dominant going to 4K. Also the pole are visible and respect the theoretical value of 14kHz.

one opamp and a current source. We obtain with this simple circuit about a $1.3pA_{RMS}$ resolution over 10kHz bandwidth at 4K. Better than room temperature circuits presented in chapter 2 by factor almost 10.

Unfortunately our system has still some inconvenient: first of all the input virtual ground is not at zero voltage but it's at voltage $V_p - |V_{th}|$ and this input offset voltage modifies the DUT bias; it's possible to trim V_p in order to obtain a 0V input offset but it's hard to ensure this in long term measurement. In figure 4.13 we see also a huge amount of disturbs, this are spurious piked up due our big loop due to double stage structure. The way we pursue to solve the offset and the disturbs problem is to synthesize a whole integrated transimpedance amplifier able to work even at 4K. In this way the offset voltage will be in mV range thanks to differential structure and also disturbs can be reduced thanks to smaller loop system but it requires a huge design care respect to single transistor circuit here described.

Chapter 5

Integrated Cryogenic Transimpedance

In this chapter we will present the design, realization and testing of a whole integrated cryogenic transimpedance amplifier, showing the design procedure in detail, the measurements and the limits. In the final section we'll also present a current amplifier with gain 1000.

In chapter 4 we described an amplifier which had a first stage at 4K and a second stage at room temperature showing the advantage in term of resolution respect to room temperature electronics; it has some problems: first of all it suffer of an high input offset due to the common-source cryogenic stage; this affects the bias voltage applied on the sample (section 2.2.3). Moreover the very simple cryogenic stage limits the gain and make mandatory the presence of an external room temperature opamp to provide the requested gain for feedback; the external opamp limit the resolution of the system in high frequency range (equation 4.15). To obtain low noise performances with higher bandwidth it's mandatory to put all the part of the opamp at cryogenic temperature.

5.1 Design of full cryogenic circuit

A fundamental step to design integrated circuit is the computer simulation, in figure 5.1 we compare a simulation with spectre and the correspondent measurement of drain current in a mosfet, below 80 kelvin the simulator is no more reliable due to temperature effect. We need to find another way to proceed with simulation. Our idea is extract the parameters at 4K via simple models and use them in a simulator as we would be in a room temperature circuit. We characterize the technology at 4K in chapter 3, discussing the result and the limits of validity. We see that mosfet with small W/L can work

properly at 4K even with a high threshold voltage and higher mobility. But the problem is that extracted parameters are not constant with geometries, obviously the synthesis of a cryogenic integrated circuit is strictly related to the capability to tune the optimized geometries for transistors for a specific function.

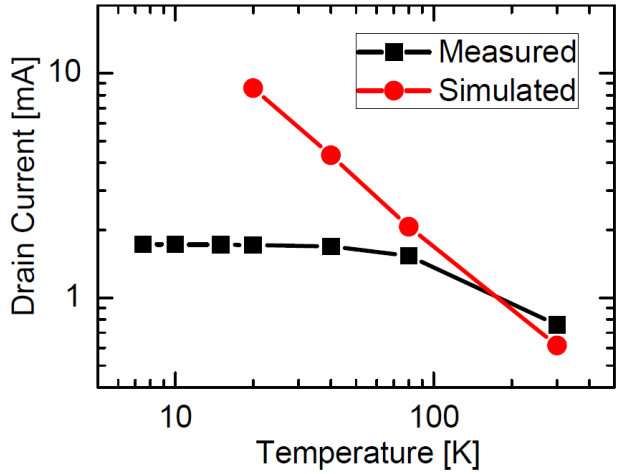

Figure 5.1: Comparison of drain current simulation and measurement on a Pmos $80\mu m/14\mu m$, with voltages: $|V_{GS}| = |V_{DS}| = 3V$. Below the 80K the simulation and the measurement disagree.

To overcome this problem we decide to use only one geometry for Pmos and one for Nmos to synthesize the whole circuit, combining them in parallel or in series to reach the equivalent mosfet geometry needed. We chose as transistor base the devices shown in table 5.1 as they are the most conductive transistors which not suffers to freeze-out effects (section 3.2).

	$k_n(k_p)$	V_{TH}	λ
Nmos $50\mu m/1.4\mu m$	$4mA/V^2$	0.88V	$0.0102V^{-1}$
Pmos $50\mu m/0.7\mu m$	$-220\mu A/V^2$	-1.3V	$0.059V^{-1}$

Table 5.1: Resume of mosfet parameter at 4.2K

Two mosfets with geometry (W/L) connected in parallel are equivalent to one mosfet with geometry $2 \cdot (W/L)$; while two mosfet in series are equivalent to a mosfet with half (W/L) of course this method has the limitation: first only multiple or fraction 1/N of base transistor can be synthesized[1]. There

[1]Actually all fraction of base transistors can be realized but the number of transistor used may diverge, to synthesize a 2/5 dimension we need 10 transistors

have also higher parasitic, finally two transistors in series have also one more node respect equivalent transistor and they have more singularities associated with it.

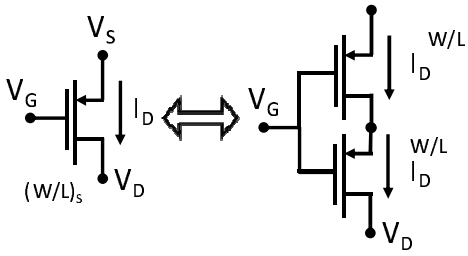

Figure 5.2: Two mosfet in series with W/L act like a single mosfet in which $(W/L)_S = (W/L)/2$.

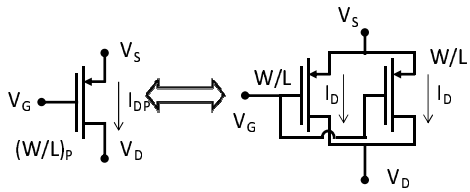

Figure 5.3: Two mosfet in parallel with W/L act like a single mosfet in which $(W/L)_P = 2 \cdot (W/L)$.

From characterization in chapter 3 we found another limitation for design a cmos circuit: it should be avoided to work with high drain to source voltage because Nmos suffers of kink effect these voltage. The kink effect is an increase in drain current at high V_{DS}, it reduces drastically the output resistance of mosfet r_0 related to flatness of mosfet's characteristic in saturation region ($r_0 = dV_{DS}/dI_D$), small r_0 provokes a reduction on DC gain of stages.

5.2 Cryogenic transimpedance

The synthesis of a whole cryogenic amplifier starts defining the environment of our cryogenic amplifier; the circuit is inserter into a cryostat at about 20cm far from the sample, with an estimate of 50pF parasitic. The output of cryogenic amplifier is a long wire of about 3-4 meters longitude through the room temperature acquisition system; the output capacitance, obviously bigger is about 1nF; this high capacitance limits the room temperature resolution as seen on chapter 2, but now this is no more a input capacitance an so has a lower impact on performances. Respect to room temperature devices, the input capacitance is reduced and the output capacitance is increased.

In figure 5.4 there is the schematic of the system described with the parasitic capacitance. The value of the resistance can be defined by noise specific: the specific introduced in chapter 2 are $10fA_{RMS}$ of resolution over 10Hz bandwidth, the feedback resistance is designed to satisfy this requirement according

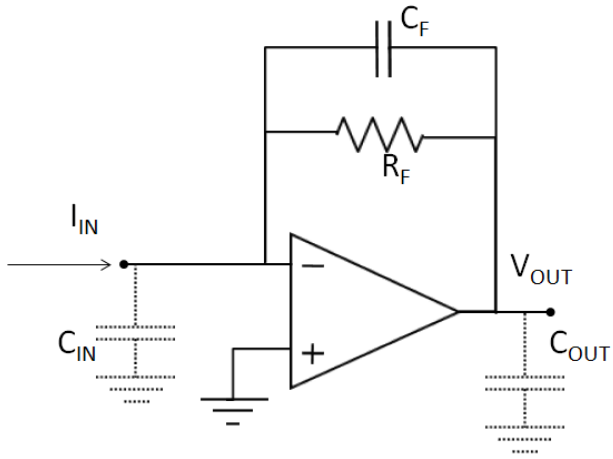

Figure 5.4: Scheme of cryogenic transimpedance inserted into cryostat, the input capacitance is about 50pF due to the wire from the sample, the output capacitance is 1nF due to the long wire for reach the room temperature acquisition system; the gain is $V_{out}/I_{in} = -R_f$.

to the relationship:

$$S_i = \frac{10fA}{\sqrt{10Hz}} = \sqrt{\frac{4kT^*}{R_f} \cdot \Delta f} \Rightarrow R_f = \frac{4kT^*}{(3.16fA/\sqrt{Hz})^2} = 22M\Omega \qquad (5.1)$$

where S_i in the input spectral noise, k is Boltzmann constant and $T^* = 4K$ is the cryogenic temperature. The same equation for room temperature system gives to us a requested feedback resistor of more than $1G\Omega$, while at cryogenic temperature the resistance's thermal noise reduces and so a lower value resistor satisfy the noise requirement; this has advantages on bandwidth and dynamic range[2].

5.2.1 Integrated resistor

The $R_f = 22M\Omega$ should be integrated in the cmos chip, this value is uncommon in cmos integrated circuit because the polysilicon used for synthesis of resistor has a sheet resistance about $50\Omega/\square$ so considering a width of $1\mu m$ to obtain a $22M\Omega$ the length should be 27mm so it would occupy a big amount of area and increases the cost; it' possible to use a N^+ well as resistor which has $1k\Omega\square$ but has a huge temperature dependence. Our technology $0.35\mu m$ from AMS has an high resistive additional mask which allow high resistive polysilicon with $1.2k\Omega/\square$ moreover in chapter 3 we have seen that polysilicon

[2]With a lower feedback resistor it's possible to acquire a higher input current, which is limited by output voltage saturation of opamp

resistor raise of a factor 2.4 from 300K to 4.2K. So to obtain a low temperature resistance we need a polysilicon resistor of $1\mu m$ x $3000\mu m$ that, with a S shape occupy a reasonable area of $40\mu m$ x $370\mu m$.

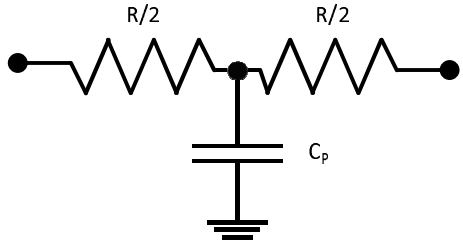

Figure 5.5: Model of an integrated resistor of value R, it uses two resistors and between the middle node and ground there is a parasitic capacitance. In a $22M\Omega$ resistor this parasitic it's about 1pF.

5.2.2 Parasitic on feedback resistor

The occupation of area is not the only limit for high value resistor in integrated circuit but also parasitic capacitance took a fundamental role. A more realistic model of an integrated resistor is shown in figure 5.5. The parasitic capacitance is caused by polysilicon layer and the substrate under it, according to technology model parameters for $22M\Omega$ with dimension $1\mu m$ x $3mm$ the parasitic capacitance result about 1pF. The ideal gain of structure in figure 5.4 is:

$$\frac{V_{out}}{I_{in}}(s) = \frac{-R_f}{1 + sC_fR_f} \tag{5.2}$$

the capacitance feedback aid to obtain a stable circuit. Considering the model in figure 5.5 for the feedback resistor, the ideal gain becomes:

$$\frac{V_{out}}{I_{in}}(s) = -R_f \frac{1 + s\frac{R_fC_p}{2}}{1 + sC_fR_f + s^2\frac{R_f^2C_pC_f}{4}} \tag{5.3}$$

So a pole-zero pair is added, for $C_p > C_f$ the two poles are complex conjugated, in this case is no more convenient reduce C_f in order to expand the bandwidth because overshoot and damped response will appear, so the parasitic capacitance value in figure 5.5 is the minimum usable for feedback capacitance to avoid complex singularities. However at cryogenic temperature we expected that parasitic capacitance reduces as the gate capacitance in interdiction region of mosfet (figure 3.9). So we expect lower parasitic on it.

5.2.3 Signal bandwidth

We have seen that using a higher value resistors can damage the response introducing complex poles and also occupies a significant portion of silicon area. We decide to implement the minimum resistor which satisfy the noise requirement $R_f = 22M\Omega$ without increasing it. To design the feedback capacitor let supposing to have a 50MHz gain bandwidth product opamp; the loop gain has the same behavior than room temperature transimpedance amplifier already presented in chapter 2, showed and in figure 5.6.

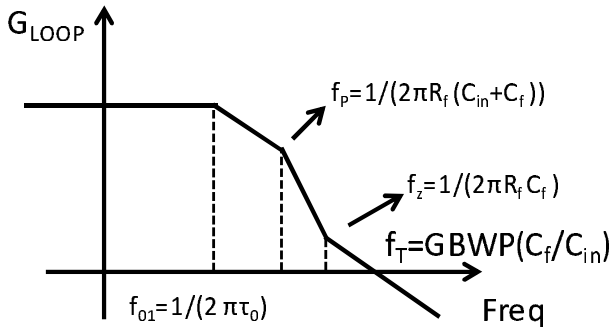

Figure 5.6: Loop gain of cryogenic transimpedance amplifier, the first pole is due to operation amplifier, the others are due to feedback net. To obtain a good phase margin the zero must be one decade before the cut-off frequency f_T.

The stability of the feedback system is described in term of phase margin that is the phase of loop gain at frequency in which the module of loop gain is 1. If the phase margin is >90° the system is stable, between 90° and 45° small overshoot may appear in response, below 45° the system is near instability and damped oscillation appears. The phase of loop gain is 180° at DC (due to minus sign), after f_0 and f_p the phase lose 90° for each pole and becomes 0°, at frequency f_z the phase raise to 45° and if f_T is one decade far from f_z the phase at f_T reaches about 90°. To be conservative we decide to have a good phase margin of 90° approximatively at $f_T = 10 \cdot f_z$, obtainable with:

$$f_T = GBWP\frac{C_f}{C_{in}} = 10 \cdot \frac{1}{2\pi C_f R_f} \Rightarrow C_f = \sqrt{10\frac{C_{in}}{2\pi R_f GBWP}} = 270fF \quad (5.4)$$

we design a 250fF as feedback resistor, although is smaller than parasitic capacitor on feedback resistor and so conjugated pole may appears; we trust in a reduction of parasitic at low temperature. The signal bandwidth result $1/(2\pi R_f C_f) = 29kHz$, we note that for stability reason the signal bandwidth, correspondent to f_z in figure 5.6, is one tenth respect to cut-off frequency that is the bandwidth of feedback loop.

5.3 Cryogenic Opamp Design

After design the feedback devices the synthesis of a fully integrated cryogenic amplifier continues with the synthesis of the cryogenic opamp. We choose a cmos technology $0.35\mu m$ 3.3V from AMS. The characterization described in chapter 3 and resumed in table 4.1 notes a higher threshold voltage at 4 kelvin, huger in particular for Pmos ($V_{TH} = -1.3V$) and a higher lambda factor which corresponds to a reduced drain resistance ($r_0 = 1/(I_d\lambda)$). A small r_0 reduces also the gain of amplifier stage[3]; the gain is increasable by cascode structure but the high threshold voltage makes difficult the use of telescopic cascode which requires a ratio between supply voltage and threshold voltage of about 4-5, and also for power consumption reason we reject the folding cascode structures. We remember that the circuit will work inside a cryostat and we had to avoid that power consumption affect the cryostat functioning. For all these consideration we chose for our amplifier a simple two-stage structure, which has a good DC gain compensating the lower r_0 at 4 kelvin. It is a simple structure with two stages: a first differential stage and a second common-source stage (figure 5.7).

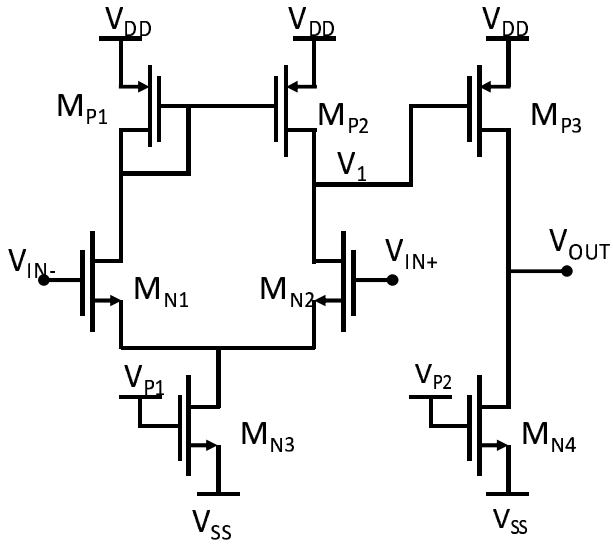

Figure 5.7: Scheme of simple two stage operation amplifier, the first stage is a differential stage with output on node V_1 and the second is a standard common source stage. The composition of two stage gain compensate the reduction of drain resistance. The frequency compensation is not shown.

[3]The maximum gain in a simple stage is $G = 1/(\lambda V_{ov})$ in which V_{ov} is the overdrive voltage

The most important devices are the input pair transistor because they limit the noise performances, the input offset voltage and common mode dynamic range. They are M_{n1} and M_{n2} in figure 5.7. We choose a Nmos pair to have good common mode dynamic range. The input terminal corresponds to terminal + and - in figure 5.4; the voltage applied on positive terminal it is at least the bias voltage of DUT about $\pm 50mV$. The supply voltage are $V_{dd} = +1.5V$ and $V_{ss} = -1.5V$, the sources of input pair are connected together to the drain of tail mosfet; assuming V_{cm} the common-mode voltage in input, the sources node has a voltage $V_{cm} - V_{THn} - V_{ov1}$; to work in saturation region the transistor tail must have $V_{ds3} > V_{ov3}$ these two relationship can be merged in $V_{ov1} + V_{ov3} - V_{cm} < +|V_{ss}| - V_{thn} = 0.7V$, if using Pmos input pair this relationship would be $V_{ov1} + V_{ov3} - V_{cm} = V_{DD} - V_{thp} = 0.2V$ in this last case the voltage margin for overdrive and the common mode range is drastically reduced, we choose as consequence a Nmos input pair although Pmos has less flicker noise.

5.3.1 Noise of input pair

Let calculate now the noise contribute of input pair to minimize it. According to our technology model, Nmos has a current noise equal to:

$$i_n^2 = \frac{2}{3} 4kTg_m + \frac{K_f I_d^{A_f}}{C_{ox} L^2 f} \tag{5.5}$$

in which f is the frequency, k is Boltzmann constant, T is the temperature, C_{ox} is the density of gate capacitance, L is the length of gate, g_m is the transconductance, K_f and A_f are constant due to process and I_d is the bias drain current. The first term is white thermal noise and the second is the flicker noise prominent at low frequencies. Supposing that input pair transistor are the only noisy components of opamp the total input noise of opamp can be calculated referring to input the transistor current noise:

$$e_n^2 = 2 \cdot \frac{i_n^2}{g_m^2} = \frac{4}{3} \frac{4kT}{g_m} + \frac{2K_f I_d^{A_f}}{C_{ox} L^2 g_m^2 f} \tag{5.6}$$

The opamp parallel current noise in cmos technology can be neglected because it's related to shot noise due to gate leakage which is very small in cmos technology.

In figure 5.8 there is the transimpedance stage in which we add the noise sources from opamp (e_n) and from feedback resistor. The equivalent input noise spectrum of transimpedance is:

$$S_{in}^2 = \frac{e_n^2}{R_f^2} + \frac{4kT}{R_f} + s^2 e_n^2 C_{in}^2 \tag{5.7}$$

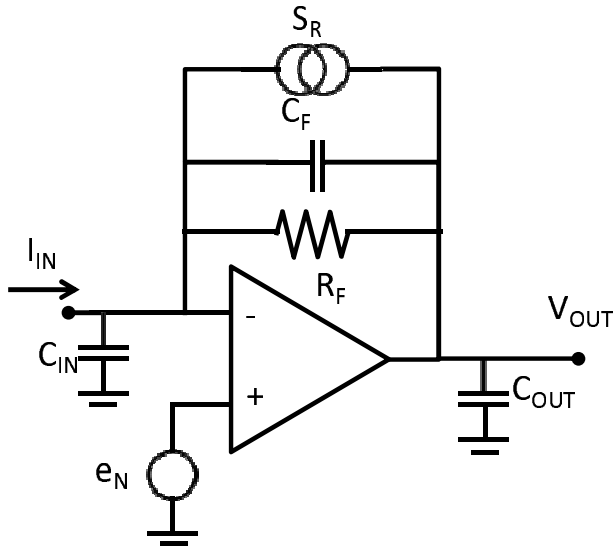

Figure 5.8: Scheme of cryogenic transimpedance amplifier with the associated noise sources, we had neglected the current noise of opamp as in cmos technology it's very low. For opamp noise we consider only the noise due to input pair.

if we substitute the equation 5.6 into equation 5.7 and integrating the spectrum into a bandwidth B we obtain a rms input current noise:

$$I_{RMS}^2 = \left[\frac{4kT}{R_f}\left(1+\frac{4}{3g_mR_f}\right)\right]\cdot B + \frac{2K_fI_D^{A_f}}{C_{ox}L^2g_m^2R_f^2}ln\left(\frac{B}{f_{low}}\right) + \\ + \frac{2K_fI_D^{A_f}}{C_{ox}L^2g_m^2}4\pi^2C_{in}^2\frac{B^2}{2} + \frac{16kT}{3g_m}4\pi^2C_{in}^2\frac{B^3}{3} \tag{5.8}$$

f_{low} is the minimum frequency of integration band (that can not be exactly zero because flicker noise will diverge); it's related to measurement time. The first term of expression 5.8 can be approximated with $4kT/R_f$ if $g_m >> 4/(3R_f) = 61nA/V$ easy obtainable in a opamp. C_{in} is the input capacitance, it's composed by parasitic due to input wire C_p and by gate capacitance of input mosfet $C_{ox}WL$. We can substitute $C_{in} = C_p + C_{ox}WL$ in which W and L are width and length of gate of input transistor. Moreover we can explicit the geometries dependence on $g_m = \sqrt{2\mu_nC_{ox}\frac{W}{L}I_d}$; considering this two substitution the equation 5.8 becomes:

$$I_{RMS}^2 = \overbrace{\frac{4kT}{R_f}B}^{first\,term} + \overbrace{\frac{K_f I_d^{A_f-1}}{\mu_n C_{ox}^2 W L R_f^2} ln\left(\frac{B}{f_{low}}\right)}^{second\,term} + \\ + \overbrace{\frac{16\pi^4}{3}\frac{4kT}{\sqrt{2\mu_n I_d}}\frac{\left(C_p + C_{ox}WL\right)^2}{\sqrt{C_{ox}\frac{W}{L}}}\frac{B^3}{3}}^{third\,term} + \\ + \overbrace{\frac{4\pi^2 K_f I_d^{A_f-1}}{\mu_n}\frac{\left(C_p + C_{ox}WL\right)^2}{C_{ox}^2 WL}\frac{B^2}{2}}^{forth\,term} \tag{5.9}$$

The first term is due to thermal noise from feedback resistance, the second term is due the flicker noise of opamp, the third term is due to white noise of opamp and input capacitance and the forth term is due to flicker noise from opamp and input capacitance.

We have to find the design parameters W, L and I_d which minimize the expression 5.9; the first term is due to feedback resistance that is already been designed. The second term belongs to opamp's flicker noise it can be minimized reducing the bias current or increasing the mosfet dimensions. The third is more complicated can be reduced by increasing the drain current and, focusing on dimension, it is:

$$third\,term \propto \frac{\left(C_p + C_{ox}WL\right)^2}{\sqrt{C_{ox}WL}} \cdot L \tag{5.10}$$

Which has a minimum if is satisfied the following the relationship:

$$C_{ox}WL = \frac{C_p}{3} \tag{5.11}$$

minimizing the term in 5.10 requires to use a minimum length L and a W that satisfy the relation 5.11. The same approach can be applied also in forth term in equation 5.9 obtaining:

$$forth\,term \propto \frac{\left(C_p + C_{ox}WL\right)^2}{C_{ox}WL} \overset{minimizing}{\rightarrow} C_p = C_{ox}WL \tag{5.12}$$

The parasitic capacitance C_p is due to the wire connecting the cryogenic electronics to the sample, it is long about 20-30 cm and his capacitance can be estimated into 50pF. In the chosen technology C_{ox} is $4.45 fF\mu m^2$ so to satisfy

the relationship 5.11 the area should be $WL = 3745\mu m^2$ and $WL = 11235\mu m^2$ to satisfy the relation 5.12. As the length should be minimized for reduce the term in 5.11, we design $L = 1.4\mu m$ that is the length of characterized Nmos. The width resulting is $W = 3745\mu m^2/1.4\mu m \approx 2500\mu m$ equivalent to fifty Nmos 50/1.4 in parallel. Satisfying the relationship 5.12 lead to use 150 Nmos. We design the geometries of input pair as Nmos $2500\mu m/1.4\mu m$ to save area reducing also the related parasitics.

Focusing on third and forth term in equation 5.9 the dependence on input current is different while third term is bigger for small current, the forth is exactly the opposite; considering that $A_f = 1.36$ and $K_f = 25.5e-27$ in our technology. The minimum noise of respect to drain current can be find making this two term equal and explicit the current, obtaining:

$$I_d = \left(\frac{16\sqrt{2}}{9} \frac{\sqrt{K_n W} kTC_{ox} L^{\frac{3}{2}}}{K_f} \cdot B \right)^{\frac{1}{A_f - 0.5}} = 236nA \tag{5.13}$$

It's a very low bias current because the flicker noise is prominent respect the thermal noise at low temperature.

But such a low current may lead the input transistors into sub-threshold region, that is a region which has to be avoided according to characterization done in chapter 3; in particular in sub-threshold region the sensitivity of current dispersion over threshold voltage dispersion is increased. The sub-threshold region appears when the overdrive voltage of a transistor is near the thermal voltage; at 4K the thermal voltage is $kT/q = 345\mu V$, to rest in saturation region the overdrive should be bigger like 3mV, the minimum drain current consequently results:

$$I_d = \frac{1}{2} \cdot 4m \frac{A}{V^2} \cdot \frac{2500\mu m}{1.4\mu m} (3mV)^2 = 32\mu A \tag{5.14}$$

So the current should be not less that $32\mu A$ to avoid sub-threshold and ensuring a good coupling between input mosfet. We fix the bias current value at $50\mu A$; with these parameters the transconductance of input pair result:

$$g_m = \sqrt{2k_n \frac{W}{L} I_d} = 26.7m \frac{A}{V} \tag{5.15}$$

5.3.2 Double current mirror

Once designed the input pair transistor with length $1.4\mu m$ and width $2500\mu m$ we continue with Pmos mirror which has the task convey the signal current from input transistors to the gain node. The structure in figure 5.7 suffers of

a problem, the drain of M_{N2} is attached to gain node 1; the M_{N2} has 2.5mm of width and this provokes an high parasitic capacitance between drain and bulk. This big parasitic connected on a gain node introduce a low frequency pole in opamp transfer function. To avoid this we need to separate the gain node from the big input transistors which have big parasitic capacitance.

A simple solution is shown in figure 5.9; the current from the input transistors is read by two transistor M_{P1} and M_{P2} in transdiode configuration which exhibit a low impedance avoiding low frequency poles. The current mirrors $M_{P1}-M_{P3}$, $M_{P2}-M_{P4}$ and $M_{N4}-M_{N5}$ convey the signal current from input transistor to gain node 1. The input impedance of Pmos M_{P1} and M_{P2} is the inverse of its transconductance $1/g_{mP}$, if C_{db} is the parasitic capacitance of drain of input pair, of about 2pF; the pole result at frequency $g_{mP}/(2\pi C_{db})$, to bring it over 200MHz, in order to not interfere into loop gain bandwidth the transconductance should be $g_{mP} = 2.4mA/V$ and as the bias current is the same that input transistor $50\mu A$, we can design the W/L of mosfet M_{P1} to M_{P4} according to:

$$\frac{W}{L} = \frac{g_{mP}^2}{2k_p I_d} = 261 \tag{5.16}$$

so W/L of Pmos 1-4 result $200\mu m/0.7\mu$. For lower current mirror the M_{N4} and M_{N5} mosfets are dimensioned as $50\mu m/1.4\mu m$ to minimize the area in fact a single base nmos 50/0.7 is sufficient to give a low reading impedance (M_{N4}) and high output impedance (M_{N5}). The voltage gain of first differential stage is $G_1 = g_{mN1}\cdot(r_{0P3}//r_{0N5})$ and the total gain result $G = G_1\cdot g_{mP5}\cdot(r_{0P5}//r_{0N6})$.

Noise of first stage

In section 5.3.1 we calculated the noise impact of opamp only considering the noise of input pair $M_{N1} - M_{N2}$; neglecting other transistors. Now we'll verify this supposition. The differential gain of input stage is:

$$G_1 = g_{mN1}\cdot(r_{0P3}//r_{0N5}) = 26.7mA/V(340k\Omega//2M\Omega) \approx 7600V/V \tag{5.17}$$

The voltage input noise due to first stage considering all the transistor is:

$$\begin{aligned} S_i^2 &= 2\cdot\frac{2}{3}\frac{4kT}{g_{mN1}} + 2\cdot\frac{2}{3}\frac{4kTg_{mN4}}{g_{mN1}^2} + 4\cdot\frac{2}{3}\frac{4kTg_{mP1}}{g_{mN1}^2} = \\ &= 2\cdot\frac{2}{3}\frac{4kT}{g_{mN1}}\left(1 + \frac{g_{mN4}}{g_{mN1}} + 2\cdot\frac{g_{mP1}}{g_{mN1}}\right) \end{aligned} \tag{5.18}$$

in which g_{mN1} is the transconductance of input pair $M_{N1} - M_{N2}$, g_{mN4} is the transconductance of Nmos mirror $M_{N4} - M_{N5}$ and g_{mP1} is the transconductance of Pmos M_{P1} to M_{P4}. The noise of input transistor dominate as long

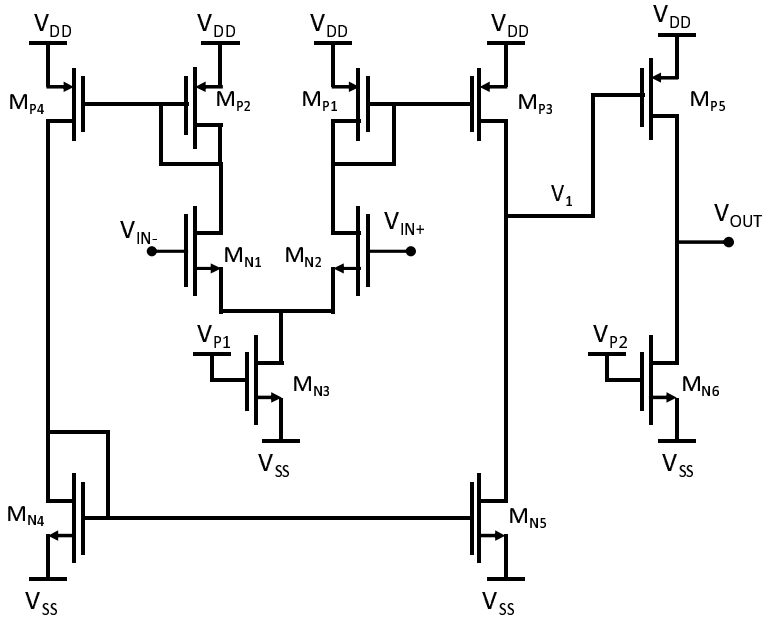

Figure 5.9: Scheme of cryogenic operational amplifier, the signal current from the big input transistors is read by low impedance transistors M_{P1} and M_{P2} in transdiode configuration. This avoid that high capacitance node of transistor M_{N1} and M_{N2} interacts with gain node 1. The Nmos current mirror M_{N4} and M_{N5} conveys the signal to the gain node 1 where the voltage gain is $G_1 = g_{mN1} \cdot (r_{0P3} // r_{0N5})$. The output gain result $G = G_1 \cdot g_{mP5} \cdot (r_{0P5} // r_{0N6})$.

as:

$$\begin{aligned} \frac{g_{mN4}}{g_{mN1}} &= \frac{3.78mA/V}{26.7mA/V} = 0.14 << 1 \\ \frac{2g_{mP1}}{g_{mN1}} &= \frac{5mA/V}{26.7mA/V} = 0.19 << 1 \end{aligned} \tag{5.19}$$

5.3.3 Second Stage and Compensation

The design of the cryogenic opamp continues with the design of second stage opamp composed by Pmos M_{P5} in common source configuration and Nmos M_{N6} as current source. While the first stage has to satisfy the noise requirement; the second stage has to raise the gain, implement a frequency compensation, required in two stage opamp, and drive correctly the output wire.

The output capacitance has a value about 1nF due to the long wire; the second stage has to drive correctly this capacitance applying the requested voltage. The slew rate reflects how fast the output voltage can move. Hypnotizing that output output voltage is a voltage sine with amplitude $V_A = V_{DD} = 1.5V$

and frequency equal to maximum signal bandwidth 30kHz, the slew rate requested is:

$$SR_{OUT} = \frac{dV_{out}}{dt}|_{MAX} = \frac{dV_A sin\omega t}{dt}|_{MAX} = \omega V_A = 282k\frac{V}{s} \tag{5.20}$$

In the opamp in figure 5.9 the slew rate is related to the maximum output current and to output capacitance according to:

$$SR = \frac{I_{OUTMAX}}{C_{OUT}} \Rightarrow I_{OUTMAX} = SR \cdot C_{OUT} = 300\mu A \tag{5.21}$$

The output current comes from M_{P5} in case of positive output voltage and from M_{N6} in case of negative voltage in this last case the maximum output current comes only from current source M_{N6} as M_{P5} is in shutdown region, for conservative reasons we design the current on M_{N6} of 1mA. For positive output voltages to obtain an output current of 1mA M_{P5} must deliver 2mA, 1mA for M_{N6} which is a current source and 1mA in output terminal.

Once fixed the bias current on second stage, we continue by designing the dimension of output stage's mosfets. The output range voltage in which mosfets rest in saturation region goes from $V_{DD} - V_{ovP5}$ and $V_{SS} + V_{ovN6}$; for higher voltages M_{P5} leaves the saturation region and goes into linear region; for lower voltage M_{N6} goes to linear region. We design the transistors with overdrive of 0.1V to enhanced the output voltage range. So we obtain:

$$\begin{aligned} \left(\frac{W}{L}\right)_{M_{P5}} &= \frac{I_D}{\frac{1}{2}\mu_p C_{ox} V_{ovP5}^2} = 909 \\ \left(\frac{W}{L}\right)_{M_{N6}} &= \frac{I_D}{\frac{1}{2}\mu_n C_{ox} V_{ovN6}^2} = 50 \end{aligned} \tag{5.22}$$

we choose $(W/L)_{M_{P5}} = 13 \cdot (50/0.7)$ and $(W/L)_{M_{N6}} = 2 \cdot (50/1.4)$. With these parameters the transconductance of M_{P5} results $g_{m2} = \sqrt{2k_n W/L I_d} = 20mA/V$. The resistance of gain node 2, equivalent to output node, is:

$$R_{02} = R_{0N6}//R_{0P5} = \frac{1}{\lambda_N I_2}//\frac{1}{\lambda_p I_2} = 98k\Omega//17k\Omega = 14.5k\Omega \tag{5.23}$$

in which $I_2 = 1mA$ is the bias current of second stage. The complete DC gain of whole two stage opamp result:

$$G = g_{m1} R_{01} g_{m2} R_{02} = 2.25 \cdot 10^6 V/V \tag{5.24}$$

Frequency compensation

The opamp in figure 5.9 has two gain nodes which are associated to two poles with constant time $\tau_1 = R_{01}C_{P1}$ and $\tau_2 = R_{02}C_{P2}$ where R_{0i} is the output resistance of stage i, C_{Pi} is the parasitic capacitance of node i. The presence of two poles in transfer function of opamp may affect the stability of the system, in fact in figure 5.10 there is the loop gain of cryogenic transimpedance amplifier with a two pole opamp. There are a pole-zero from feedback net and two pole from opamp; at the cutoff frequency the phase is less than 45° if $f_{02} < f_T$ with a consequent poor stability. To increase the stability of system f_{02} must me beyond the cut-off frequency. The most used solution is to implement the pole splitting via a capacitance amplified by miller effect.

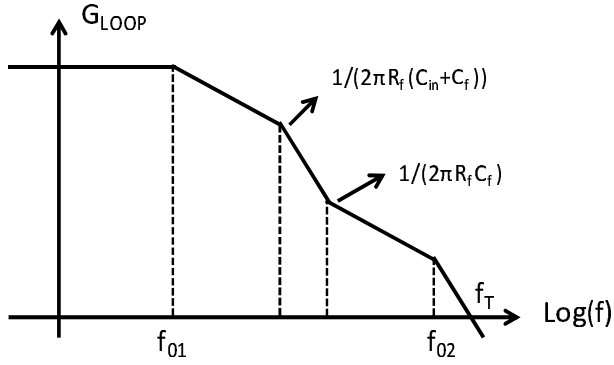

Figure 5.10: Loop gain of cryogenic transimpedance amplifier, the two pole of opamp may affect the stability if they are both before or near the cut-off frequency f_T. The higher pole must me placed at higher frequency than f_T.

The miller effect is based on insertion of a physical capacitance between the two gain node of a two stage operation amplifier. Between the note 1 and node 2 there is a voltage gain of $-g_{m2}R_{02}$ for this reason the voltage on capacitance C_c is $V_1(1+g_{m2}R_{02})$. From the first stage side the capacitance C_c behave like a higher capacitance $C_C \cdot (1+g_{m2}R_{02})$; so the pole introduced by node 1 is approximatively $f_{01} = 1/(2\pi R_{01}C_C g_{m2}R_{02})$ the first pole f_{01} moves so to lower frequencies.

But focusing on output node we can note that compensation capacitance reduce the impedance of output node at high frequency because it short the drain and the gate of M_{P5} leading the transistor in transdiode configuration[4]; so the pole associated with output node move to higher frequency. So the overall effect of miller capacitance is to split the two pole of opamp the first

[4]The output impedance of a transdiode transistor is the inverse of his transconductance $1/g_{mP5}$

towards lower frequency and the second towards higher frequency pole. The second gain node pole f_{02} can be pushed in this way at higher frequency than cut-off frequency f_T improving the stability. The transfer function of opamp

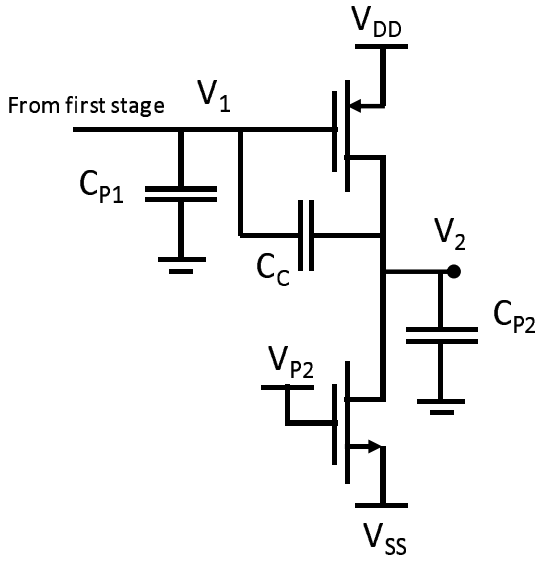

Figure 5.11: The insertion of a compensation capacitance C_c leads the pole splitting effect. Thanks to it is possible to push at higher frequency one of the two pole of opamp improving the stability.

with the compensation capacitance results:

$$\begin{aligned} A(s) &= -g_{m1}g_{m2}R_{01}R_{02}\frac{1-s\frac{C_c}{g_{m2}}}{1+sA+s^2B} \\ A &= \tau_1+\tau_2 = C_C R_{01} R_{02} g_{m2} \\ B &= \tau_1 \cdot \tau_2 = R_{01}R_{02}(C_{p1}C_{p2}+C_C(C_{p1}+C_{p2})) \end{aligned} \tag{5.25}$$

with the approximation of $f_{01} << f_{02}$, it's easy to estimate the poles as:

$$\begin{aligned} \tau_1 \approx A \Rightarrow f_{p1} &= \frac{1}{2\pi\tau_1} = \frac{1}{2\pi C_C R_{01} R_{02} g_{m2}} \\ \tau_2 = \frac{B}{\tau_1} \Rightarrow f_{p2} &= \frac{C_C g_{m2}}{2\pi(C_{p1}C_{p2}+C_C(C_{p1}+C_{p2}))} \end{aligned} \tag{5.26}$$

as expected increasing the C_C the first pole goes to lower frequencies while the second pole goes to higher frequency and when $C_C >> C_{p1}, C_{p2}$ it reach a maximum value:

$$f_{p2} = \frac{g_{mP5}}{2\pi(C_{p1}+C_{p2})} \tag{5.27}$$

The gain bandwidth product of opamp results:

$$GBWP = G \cdot f_{p1} = \frac{g_{mP1}}{2\pi C_C} \tag{5.28}$$

considering $g_{mN1} = 26.7mA/V$ to obtain a GBWP of 50 MHz, hypnotized in section 5.2.3, the requested C_C results 85pF, this is a very high capacitance for integrated circuits. We design C_C with values 10pF correspondent to a GBWP=425MHz, the cut-off frequency results $f_t = GBWP \cdot C_f/C_{in} = 2MHz$. Although the signal bandwidth should be increased up to 72kHz according equation 5.4 which returns a $C_f = 100fF$; but the parasitic capacitance on feedback resistor will limit the bandwidth according to the analysis done in section 5.2.2 so we decide to leave the bandwidth to 29kHz ($C_f = 250fF$).

So ensure stability with 90° phase margin, the second pole of opamp should be one decade higher than f_T so at 20MHz, the second gain node of opamp is also the output node with a parasitic capacitance of about $C_{p2} = C_{out} = 1nF$; the second pole f_{p2} results at 3MHz according to equation 5.27. Raise g_{mP5} in order to raise the second pole frequency could be expensive in term of area or power dissipation: both ratio W/L and I_d of mosfet M_{P5} are been designed with relative a high value ($650\mu m/0.7\mu m$ and 1mA respectively).

A simple solution for pull the second pole beyond the cut-off frequency (20MHz) without modifying g_{mP5} is to decouple the output capacitance and the gain node 2 with a simple resistor R_d as show in figure 5.12. If the pole $1/(2\pi R_d C_{out})$ is smaller that f_T; at cutoff frequency the output capacitance is hidden by the resistor so the output capacitance does not contribute to parasitic capacitance C_{p2} and the second pole of opamp moves at higher frequency as C_{p2} is just a parasitic capacitor in the order of 1pF. But the pole $f_d = 1/(2\pi R_d C_{out})$ should not limit the signal bandwidth; in our case the cut-off frequency and signal bandwidth are two different frequencies, in fact $f_{sig} = 1/(2\pi R_f C_f) = 29kHz$ while $f_T = GBWPC_f/C_{in} = 2MHz$; the output pole can be positioned in middle of this two frequencies $f_{sig} < f_d < f_T$ so does not limit the signal bandwidth but hidden at cut-off frequency the capacitance C_{out}. We choose $R_d = 800\Omega$ so the pole f_d result at 200kHz.

In transfer function of opamp in relationship 5.25, there is also a positive zero due to the presence of C_C between gate and drain of M_{p5}, we have already talk about of problem of positive real part zero in loop gain in chapter 4 and their impact on stability. However in this case the zero is already at high frequency (transconductance of mosfet 5 is high enough) his impact can be reduced by adding a series resistor R_c which blocks the multi-path structure

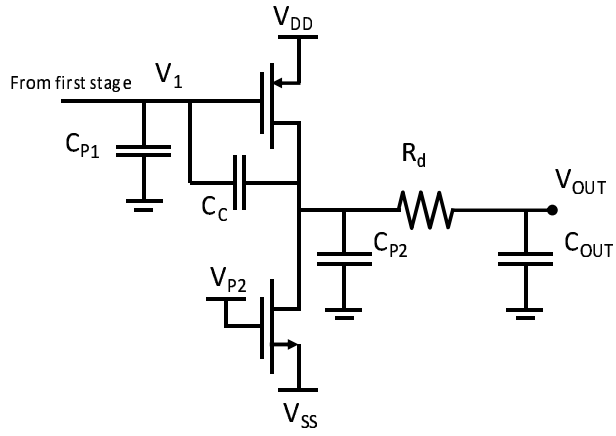

Figure 5.12: Output decoupling resistor, permits to isolate the output capacitance at cut-off frequency, without affecting the signal bandwidth.

and cancel the positive real part zero [48], if it satisfies the relationship:

$$f_z = \frac{g_{mP5}}{C_C\left(1 - g_{mP5}R_c\right)} \Rightarrow R_c = \frac{1}{g_{mP5}} \tag{5.29}$$

5.4 Measurement of Cryogenic Transimpedance

In figure 5.13 there is the final schematic of integrated cryogenic transimpedance amplifier, the current references has been implemented with a current mirror drived by a resistor in order to improve stability[5].

Our circuit has been tested from 300K up to liquid helium temperature (4K) and it works in all temperature range showing the expected results simulated. In figure 5.14 there is the characteristic of transimpedance amplifier, we measure a gain of $22.63M\Omega$ with an input dynamic of $\pm 50nA$ as expected the output voltage range is $\pm 1.4V$. We also extract the input offset voltage of 0.11mV which reflects a good coupling between the input transistors thanks to avoiding the sub-threshold bias region, also large area aid to couple the input devices. Such a low offset permits a very low bias measurement on quantum dots. The room temperature characteristic (figure 5.15) show a reduced gain due to variation of feedback resistor in temperature.

In figures 5.18 and 5.17 there are the measurements of transfer function in module and phase of cryogenic transimpedance amplifier. In this measurement was used a 100pF input capacitance as dut, we saw that while at room temperature there is an overshoot in magnitude due to the parasitic capacitance

[5]The mosfet parameters suffer of huge variation while resistors are more stable

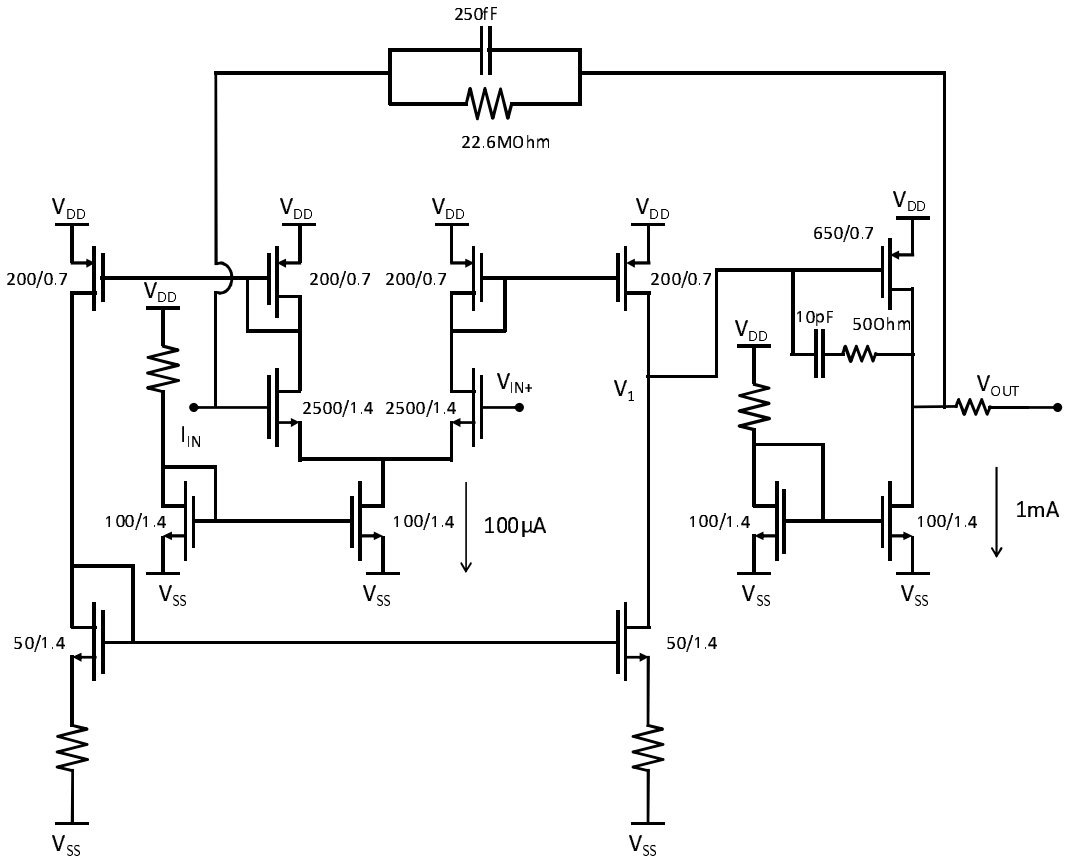

Figure 5.13: Complete schematic of cryogenic transimpedance amplifier, it's all composed by Nmos $50\mu m$ x $1.4\mu m$ and Pmos $50\mu m$ x $0.7\mu m$ integrated resistor and integrated capacitors.

in the big integrate feedback resistor, as predicted in section 5.2.2. At 4K this effect disappears, this because the parasitic capacitance reduces thanks to the freeze-out of carriers as discussed in figure 3.9. The bandwidth result 32kHz; and from the second pole at 500kHz on transfer function, it's possible to extract the GBWP as:

$$GBWP = f_T \frac{C_{in}}{C_f} = 200MHz \tag{5.30}$$

this small reduction is due probably to the non precise biasing of the input stage and process variations.

In figure 5.19 there is the comparison between the input spectral noise at 4K and room temperature (RT). At 300K we measure the thermal white noise

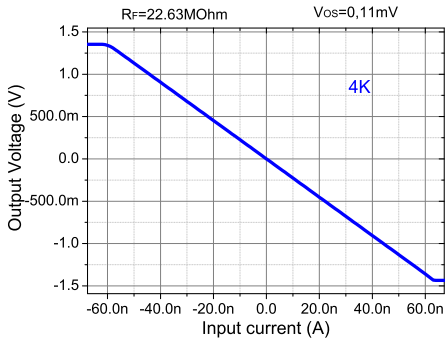

Figure 5.14: Characteristic of transimpedance amplifier at 4K.

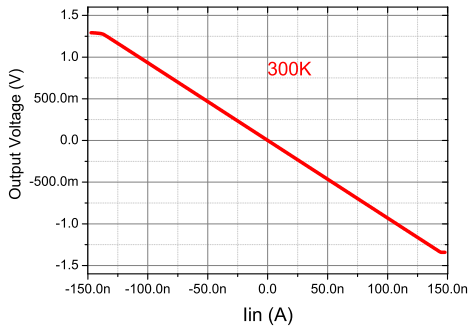

Figure 5.15: Characteristic of transimpedance amplfier at room temperature.

due to feedback resistor ($10M\Omega$ at RT):

$$\sqrt{\frac{4kT}{R_f}} = 40.7f\frac{A}{\sqrt{Hz}} \tag{5.31}$$

at low temperature the thermal noise disappears thanks both to reduction of T and to increase of R value to $22.6M\Omega$. The flicker noise appears, the fitting formula, extracted from 5.7, is:

$$S_i = \sqrt{\frac{N_f}{f}\left(\frac{1}{R_f} + 4\pi^2 C_{in}^2 f^2\right)} \tag{5.32}$$

in which $C_{in} \approx 10pF$, $R_f = 22.6M\Omega$ and $N_f = 4.3pA^2$ the theoretical value

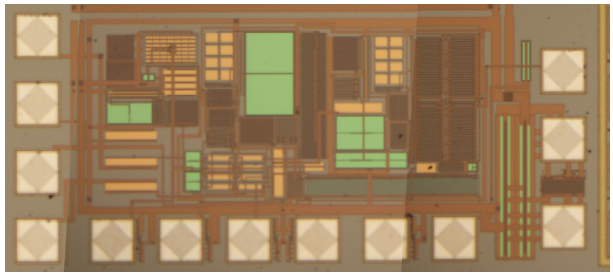

Figure 5.16: Photo of the entire cryogenic transimpedance amplifier in cmos technology $0.35\mu m$, the chip dimension are $1206\mu m$ x $560\mu m$, it uses a $\pm 1.5V$ supply with 5mA current consumption.

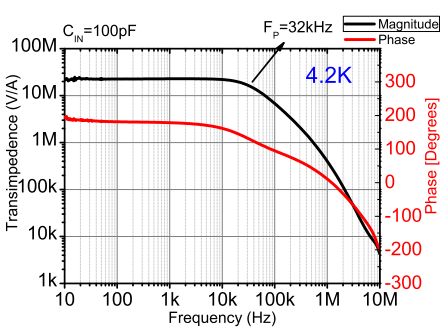

Figure 5.17: Transfer function of cryogenic transimpedance amplifier at 4K, it's evident the absence of overshoot effect due to parasitic on feedback resistor.

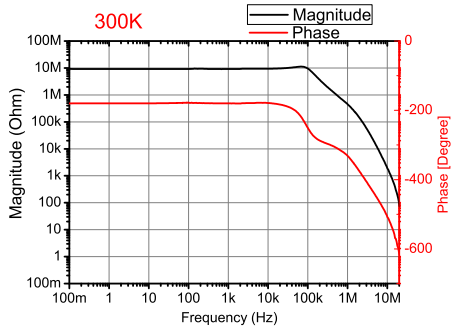

Figure 5.18: Transfer function of cryogenic transimpedance at room temperature, we can see an overshoot due to parasitic capacitance on feedback resistor.

of N_f is:

$$N_f^{THE} = \frac{2K_f I_d^{A_f}}{C_{ox} L^2 g_{mN1}^2} = 4e-13V^2 \tag{5.33}$$

in which $I_d = 50\mu A$, $A_f = 1$, $C_{ox} = 4.45fA/\mu m^2$, $L = 1.4\mu m$ and $K_f = 25.5e{-}27$ as extracted from characterization in chapter 3. A 10 times difference is understandable when considering that we are using a Nmos input pair which has much flicker noise than Pmos.

The input noise rms over 30kHz bandwidth result about $2.8pA_{RMS}$.

5.5 Transimpedance as current amplifier

We have seen that the output capacitance of cryogenic transimpedance amplifier is quite high 1nF due to the long wire before reach the room temperature acquisition system. This had implication on output stage bias current that must be able to charge and discharge correctly this output capacitance. And about stability the output capacitance introduces an in-band pole that could be destructive without the resistive decoupling implemented. We have demonstrate the functioning of a transimpedance amplifier from room temperature to 4 kelvin but the gain of the transimpedance amplifier, equivalent to $G = -R_f$, is variable with temperature as the feedback resistor double its value from 300K to 4K.

There is a very simple method to overtake this limits and obtain a fixed gain, the idea is to apply the output voltage of opamp to a resistance N

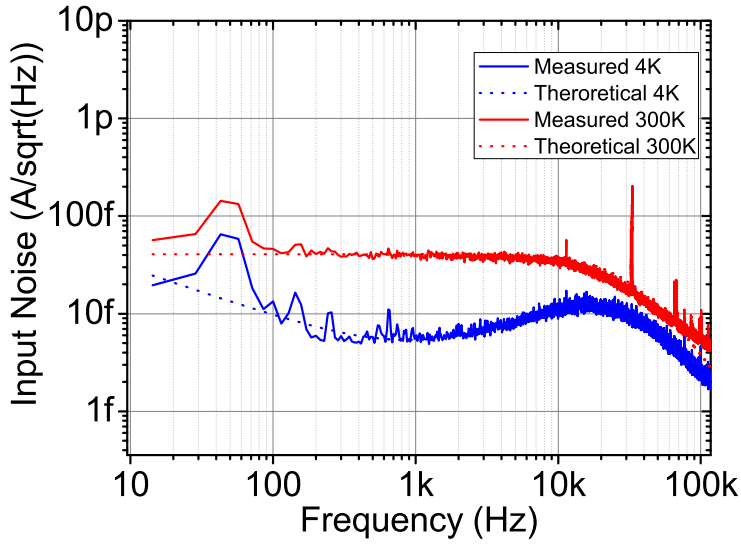

Figure 5.19: Input spectral noise density of transimpedance amplifier at 300K and 4K; at room temperature the noise is due feedback resistance thermal noise; while at 4K it disappears and flicker noise becomes dominant.

times smaller that feedback resistance and read the current flowing in this resistance via a room temperature transimpedance amplifier (figure 5.20). In this way the output resistance and the feedback resistor have the same voltage across them and so the output current is the input current multiplied the ratio of resistances. We obtain a current amplifier with gain $G = -R_f/R_{out}$ dependent on ratio and not on absolute value of resistance. If the output resistance and the feedback resistance are integrated on the same chip the temperature is the same so their ratio is only due to its geometric dimensions and not on temperature. In figure 5.21 there is the characteristic in term of output current versus input current of our cryogenic transimpedance amplifier with a integrated output resistance one thousand times smaller than feedback resistance so $22.5k\Omega$ at 4K, we can see a little non linear behavior due to output resistance; in fact according to characterization of technology; small resistance with width smaller than $10\mu m$ has a small non linear behavior. Due to coupling and occupation reasons it's not possible to raise the width of output resistance now it's $1\mu m$.

With this method the output capacitance has no longer influence on amplifier functioning because it's connected to a virtual ground of external transimpedance amplifier. It's possible to reduce the output stage bias current reducing the dissipation. Finally there are a big advantage with current output: the

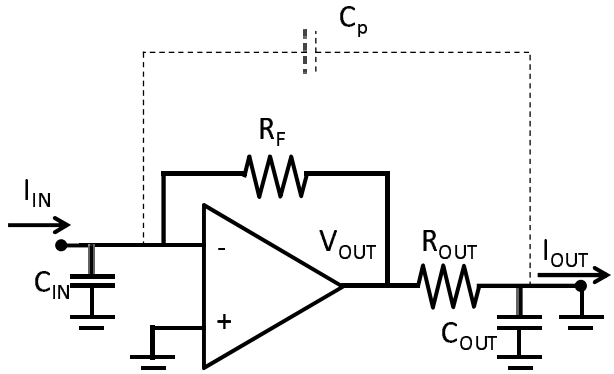

Figure 5.20: The cryogenic transimpedance amplifier used as current amplifier by adding a output resistor N times smaller than feedback resistor and reading the current flowing thought a external transimpedance, we obtain a current amplifier with gain N constant in temperature. The output capacitance should not be charged and discharges.

parasitic pad to pad capacitance C_p has no effect(figure 5.20). While using the chip like a transimpedance the parasitic capacitance between output wire is in parallel to the feedback capacitance, involving a reduced bandwidth; using the current output the parasitic capacitance is between two virtual grounds and do not affect the bandwidth.

The current amplifier describer require an external transimpedance amplifier to read the current, this transimpedance has always a big input capacitance due to the long wire like the transimpedance describer in chapter 2. But in this case the signal is 1000 times higher so the noise introduced by this external amplifier is less critical. In others words the input noise of the external transimpedance amplifier is reduced by a factor of 1000 respect the same amplifier describer in chapter 2.

5.6 Mosfet feedback current amplifier

During the synthesis of transimpedance amplifier we have seen that higher feedback resistors introduces lower noise (equation 5.1) unfortunately high resistor occupy a significant portion of area that leads to big parasitics. In this section we present a circuit in which the main idea is to use a transistor in feedback instead a resistor [49]. In fact the drain of transistor can be view as a high value resistor. See the schematic on figure 5.22 is very similar to scheme on figure 5.20 in which we change the resistances with transistors. The principle is the same: the input current flows on transistor activating a gate to source voltages V_{GS} which drives the output transistor; the two transistors have the same gate to source voltage, if the output transistor's drain is connected to

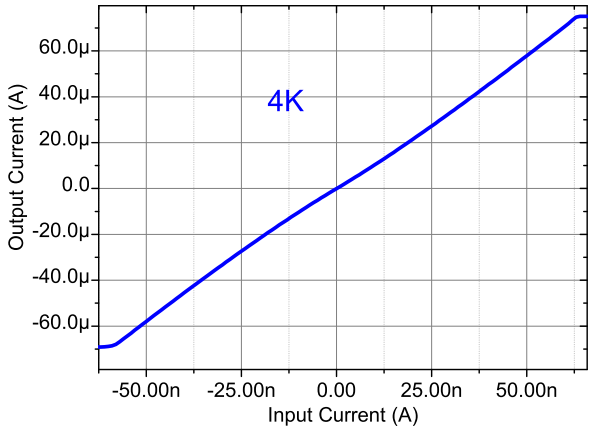

Figure 5.21: Characteristic of output current versus input current of circuit in figure 5.20, there is a small non linear characteristic due to output current but the thermal variation has been suppressed.

a virtual ground of an external transimpedance, the two transistors has the same voltages in all terminal. According to drain current relation the ratio of input and output current is due only to the ratio of geometries of transistor:

$$G = \frac{\left(\frac{W}{L}\right)_{out}}{\left(\frac{W}{L}\right)_{f}} \tag{5.34}$$

we obtain a current amplifier with gain G. The structure in figure 5.22 has two problem: first is unidirectional as the transistor in saturation region are unidirectional[6], and second the gain loop depends on input DC current as the

[6]The negative feedback equalize the drain and the gate of transistors making impossible the functioning in ohmic region

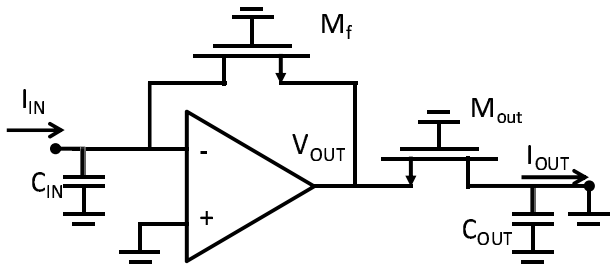

Figure 5.22: Current amplifier using two mosfet, the input current flows on feedback mosfet. As the two mosfet have the same terminal voltages the output current is magnified by N, if the output mosfet is has N times the width of feedback mosfet.

transistor has a small signal behavior function of bias current. This two problem are overtaken by inserting in parallel to Nmos a Pmos and also capacitance (figure 5.23), the Pmos manages the opposite current respect to Nmos and the capacitance at high frequency can fixes the gain loop independently from DC current.

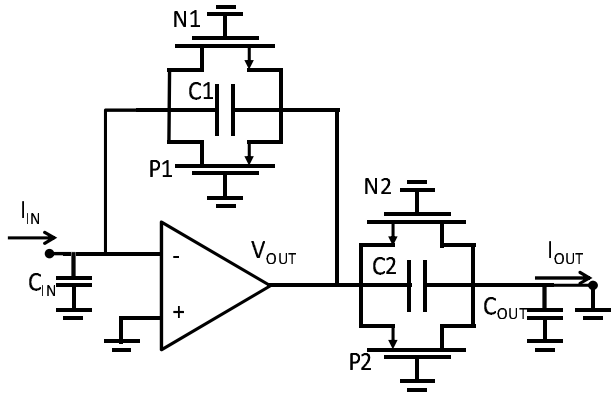

Figure 5.23: Current amplifier using two pair of complementary mosfet, the input current can be bidirectional. At high frequency the capacitor C_1 fixes the loop gain that becomes independent from DC input current. The Nmos, Pmos and capacitor must have a well fixed ratio to obtain a flat response.

If we replicate the structure in feedback, to obtain a flat response must be verified the following conditions:

$$G = \frac{\left(\frac{W}{L}\right)_{N2}}{\left(\frac{W}{L}\right)_{N1}} = \frac{\left(\frac{W}{L}\right)_{P2}}{\left(\frac{W}{L}\right)_{P1}} = \frac{C_2}{C_1} \tag{5.35}$$

A big advantage on this structure is that the current gain depend only on the ratio between W/L, the gain do not depends on absolute value of k or on W/L. So temperature variation does not affect the gain, we can use every kind of transistor geometry on first order if it satisfy the condition 5.35 and if they works at 4K.

5.6.1 Stability

The stability of a the circuit in figure 5.22 can be expressed in term of phase margin. If the phase margin is below 45° the response start being instable with damped oscillations. The loop gain of stage in figure it's:

$$G_{loop} = \frac{A_0}{1 + s\tau_0} \frac{1 + s\frac{C_1}{g_m}}{1 + s\frac{(C_{in}+C_1)}{g_m}} \tag{5.36}$$

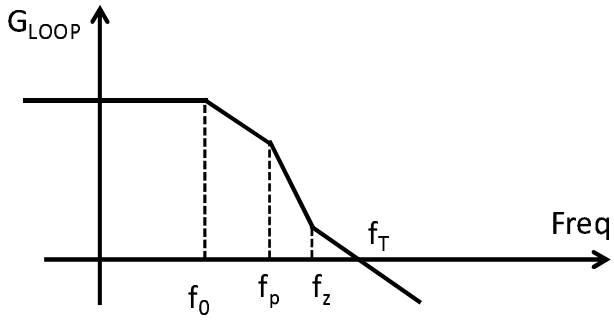

Figure 5.24: Loop gain of current amplifier as long the zero is one decade before cut-off frequency f_t the system is stable. But the zero depends on DC input current

where A_0 and τ_0 are the DC gain and dominant pole of opamp and g_m is the transconductance of the feedback mosfet.

The current gain is G=C_2/C_1, we design $C_2 = 30pF$ because higher capacitance are hard to integrate. Considering a gain of about 100, C_1 results $300fF$. Assuming that dominant pole of opamp $f_0 = 1/(2\pi\tau_0)$ is a low frequency respect the others singularities, looking at the loop gain in 5.36 we see that the ratio between the pole and the zero introduced by feedback net, is $C_1/C_{in} + C_1$, we obtain that the pole of feedback is at lower frequencies than the zero; a qualitative graph of loop gain is in figure 5.24. Without the zero the phase margin at f_T would be 0° because the phase on DC is 180° and each pole reduce the phase of 90°. The zero introduces a increment of 90° of phase full active after one decade; so the system is stable as long the zero is enough before the cut-off frequency. Considering a GBWP of 400MHz, a $C_{in} = 50pF$ and $C_1 = 300fF$ the cut-off frequency, it's $400MHz \cdot 300fF/50pF = 2.4MHz$.

There is only one active mosfet in feedback at once according to the dc input current sign, that manages the current; his transconductance g_m depends on the values of DC input current according to:

$$g_m = \begin{cases} \sqrt{2k_n \frac{W}{L} I_{in}} & \text{Saturation region} \\ \frac{I_{in}}{V_T} & \text{Subthreshold region} \end{cases} \tag{5.37}$$

where $V_T = kT/q$ is the thermal voltage, k is the gain factor of mos. So small current the transconductance g_m grows proportionally with the current, when the mosfet enters into saturation region, the g_m becomes proportional to the square root of input current. The transition current in which the regime changes from sub-threshold to saturation can be obtained by making equal the two relationship in 5.37:

$$I_r = \frac{1}{2} k_n \frac{W}{L} (2V_T)^2 \tag{5.38}$$

considering that thermal energy at 4 Kelvin is $V_T = 345\mu V$. For the characterized mosfet we obtain $I_r = 36nA$ for Nmos $50\mu m/1.4\mu m$ and $I_r = 4nA$ for the Pmos $50\mu m/0.7\mu m$.

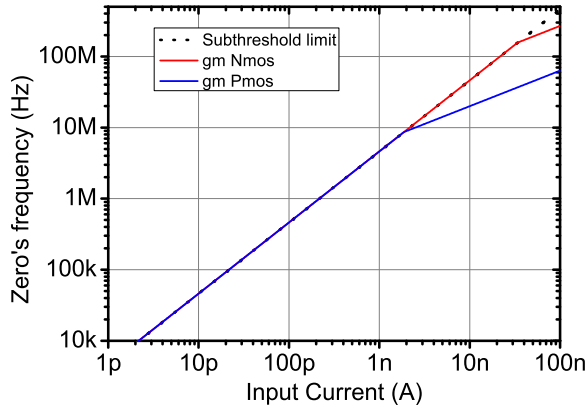

Figure 5.25: Zero frequency of loop gain in function of input current for Nmos $50\mu m/1.4\mu m$ and Pmos $50\mu m/0.7\mu m$. For current in pA range the transconductance is dominated by sub-threshold effect.

In figure 5.25 the is the position of zero of loop gain in function of DC input current for the characterized transistors. The dotted line is the zero frequency in case of sub-threshold region this is independent from transistor type and from his dimension, as the transistor are so conductive the sub-threshold region still dominate in pA range also at 4 Kelvin. The zero frequency in sub-threshold region is:

$$g_m = \frac{I_{in}}{V_t} \Rightarrow f_z = \frac{q}{2\pi C_f kT} \cdot I_{in} \tag{5.39}$$

So for low temperature the zero frequency is higher than high temperaure in sub-threshold region.

The input current range in which the zero frequency permit a stable circuit (about at $f_T = 2.4MHz$) is around 300pA, this is a very low input current, for higher current the phase margin will be about 0°. To have a phase margin of 45°, also in nA current regime, we have to use transistor less conductive in which the transition between sub-threshold and saturation region come around pA region; in saturation in fact the frequency of zero is related to the dimension by:

$$f_z = \frac{g_m}{2\pi C_1} \Rightarrow f_z = \frac{\sqrt{2k_n \frac{W}{L} I_D}}{2\pi C_1} \Rightarrow \frac{W}{L} = \frac{2\pi^2 C_1^2 f_z^2}{k_n I_d} \tag{5.40}$$

But as noted in chapter 3 the gain factor of transistor depend on dimension, in particular it reduces when we use a small ratio W/L we decide to use a $20\mu m$ x $20\mu m$ for the Pmos and $20\mu m$ x $7\mu m$ for the Nmos and $C_1 = 300fF$, in output we use devices 100 times wider. With this dimensioning the phase margin is 45° for 10nA in Nmos and 20nA in Pmos, the 45° is obtained when $f_z = f_T$ in this case:

$$\frac{W}{L} = \frac{2\pi^2 C_1^4 GBWP^2}{k_n I_d C_{in}^2} \tag{5.41}$$

The big area of transistors is required to obtain good matching, and so flat gain. We also implement a second stage with same structure to raise the current gain. This second stage has feedback transistor with dimension $15\mu m$ x 60μ for Pmos and $5\mu m$ x $60\mu m$ for the Nmos and $C_1 = 1.5pF$; in output of second stage we use devices 10 times wider to obtain a overall gain of 1000.

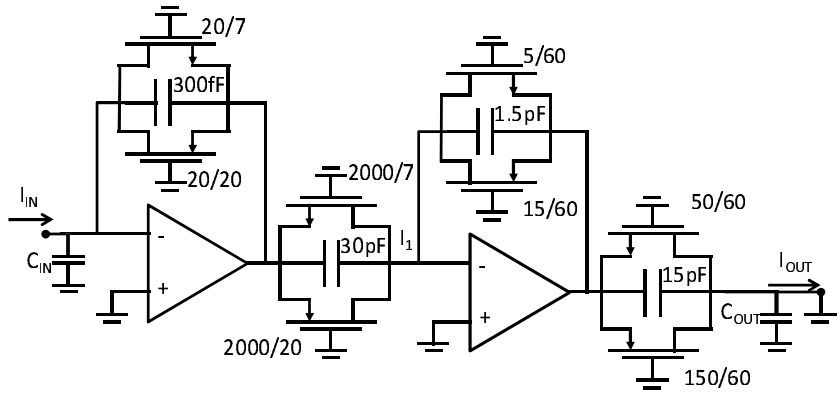

Figure 5.26: Complete schematic current amplifier the total current gain is 1000. The output current can be read via a external transimpedance.

5.6.2 Measurements

The scheme of our current amplifier is shown in figure 5.26. It is composed by two stages: the first with gain 100 and the second with gain 10. In figure 5.27 there is the measure of transfer function of the system, the pole is at 500kHz. Comparing the bandwidth respect to the cryogenic transimpedance amplifier we have now a enhancing of more than one order of magnitude thanks to the fact that we now managing also the signal flowing thought the capacitance; in cryogenic transimpedance the frequency in which the current signal flows into feedback capacitor are useless.

In figure 5.28 there is the input spectral noise of current amplifier. Due to

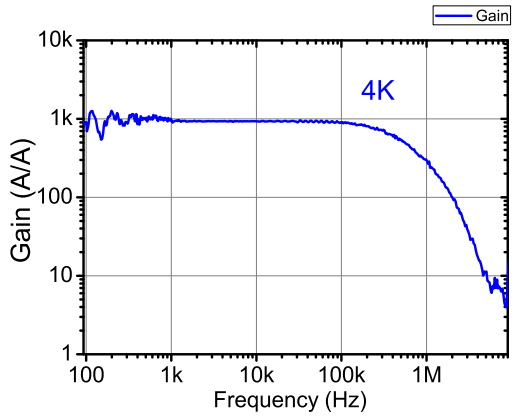

Figure 5.27: Transfer function of current amplifier, we measure -3dB pole of 500kHz; the reduction from theoretical value is due to the double stage structure.

the relation:

$$S_{in}^2 = 2qI_{in} + s^2 e_n^2 C_{in}^2 \tag{5.42}$$

The noise spectra is almost the same respect to equation 5.7 but in this case we do not have the thermal noise from feedback resistor but the shot noise from feedback transistor, or the thermal noise depending on transistor regime. Integrating the noise spectra over the bandwidth we obtain a 41pA resolution in 500kHz bandwidth.

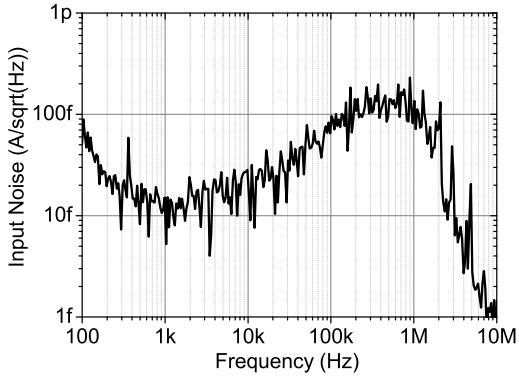

Figure 5.28: Input spectral nose of current amplifier, it reflect the noise of opamp into the input capacitance. Respect to cryogenic transimpedance amplifier we have a shot noise of transistor instead of thermal noise from feedback resistance.

The characteristic is not as we expected for negative input current so for

Pmos is good but for Nmos there are a strong non linear behavior; in figure 5.29 there is the current output of first stage with gain 100. The noise and transfer function measurements were made with almost zero dc current so the signal passes only thought capacitance which gave the expected results. In the characteristic the signal flows into the transistors which exhibit this strange effect due to coupling between mosfet as described in the following section.

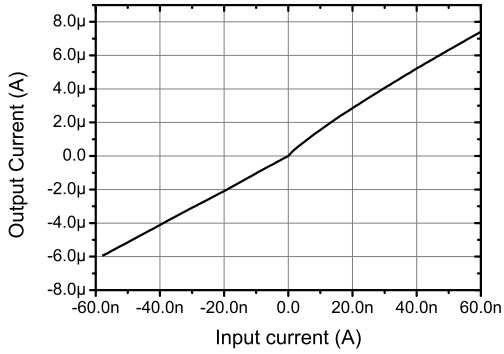

Figure 5.29: Characteristic of first stage of current amplifier, the Pmos works as expected with a current gain of 100, while for Nmos there is a non linear characteristic due to coupling of threshold voltages.

5.6.3 Effect of threshold variation

Now we analyze the effect of the threshold voltage variations between feedback and output transistors, let call V_{T1} the threshold voltage of feedback mosfet and V_{T2} the threshold voltage of output mosfet. According to technology datasheet may be a difference of about 0.5mV due to mismatches. When a input current enter on current amplifier the voltage on output terminal of operation amplifier, according to mosfet's characteristic, is:

$$V_{out} = -\sqrt{\frac{2I_{in}}{k\left(\frac{W}{L}\right)_1}} - V_{T1} \tag{5.43}$$

this voltage is the source to gate voltage of output transistor which drain current results:

$$\begin{aligned} I_{out} &= \frac{1}{2}k\left(\frac{W}{L}\right)_2\left(\sqrt{\frac{2I_{in}}{k\left(\frac{W}{L}\right)_1}} + V_{T1} - V_{T2}\right)^2 \\ &= \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}I_{in} + k\left(\frac{W}{L}\right)_2\frac{\Delta V_T}{\sqrt{\frac{1}{2}k\left(\frac{W}{L}\right)_1}}\sqrt{I_{in}} + \frac{1}{2}k\left(\frac{W}{L}\right)_2\Delta V_T^2 \end{aligned} \tag{5.44}$$

in which $\Delta V_T = V_{T1} - V_{T2}$. The first term is the ideal gain, the third is a current offset due to different threshold voltages; the second indicate a output current term depending on square root of input current. Making equal the first and the second term, we can find the transition current between square root and linear behavior.

$$I_t = 2k \left(\frac{W}{L}\right)_1 \Delta V_T^2 \tag{5.45}$$

The characteristic of figure 5.29 is explicable considering a 2mV of ΔV_T; this is compatible, because the coupling is worst between transistors at 4 kelvin respect 300 kelvin; as mentioned before [39]. To reduce the impact of this non-linear effect we should use less conductive transistors, keeping attention on parameter variations; at 4 kelvin in fact the mosfet parameters are not constant with the transistor geometry.

5.7 Conclusion

In this chapter a fully integrated transimpedance amplifier working at 4K has been designed and realized, using the model parameter extracted in chapter 3, in this way has been possible reducing the input capacitance of room temperature system improving the performances. This circuit has been used in MDM laboratories in Agrate (Italy); in figure 5.30 there is a measure of the current flowing in a quantum dot kept at 300mK, measured thought the cryogenic transimpedance amplifier, the on/off current reflects the presence of an electron in quantum dot or in a donor near it. The rise/fall time of detected telegraphic current can be estimate into $10\mu s$ compatible with specific, with room temperature system has been impossible obtain this performance.

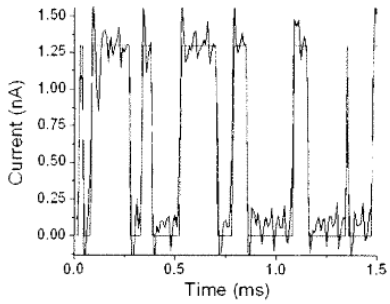

Figure 5.30: Measure of current flowing into a quantum dot at 300mK, the on/off current is due to the presence of the electron inside the dot or inside a near donor; this measurement has be done at MDM laboratories; with the cryogenic transimpedance amplifier designed in this chapter.

Chapter 6

Cryogenic integrated system

In previous chapter we presented the design, realization and characterization of a fully integrated cryogenic transimpedance amplifier working at 4K designed with simple model for transistor and using only one geometry for each Pmos and for each Nmos to overtake the problem of variation of gain factor with the geometry. During the design we had do some conservative choice: like simple structures, over designed phase margin, decoupling resistor to avoid output capacitance interaction. The measurements we do respects the simulations and the theoretical performances of our paper-and-pencil design, and confirm the validity or our model. We proceed optimizing the performances by using non-conventional structure based on opamp with internal feedback. We add others functionality to overtake some limit of transimpedance, like single input channel and also reduced gain; according to these limits we add a multiplexer allowing multi-channel input and a voltage amplifier which permit to amplify the output voltage signal before cross the long wire to acquisition system.

During the measurements in cryostat dot using the cryogenic transimpedance described in chapter 5, we observed a reduction of ^3He condensation timing from 48 hours to 35 hours; this is to the 300mK maximum measurement time. We identify the problem on amplifier supply current, in fact the wires between cryogenic transimpedance and room temperature electronics have a resistance of $40\Omega/m$ and they cross round-trip the 300mK region for 40cm, the current supply (5mA), from V_{DD} and V_{SS}, of transimpedance described in chapter 5 provokes a dissipation in this region equivalent to:

$$P_{diss} = 2 \cdot RI^2 = 2 \cdot \frac{80\Omega}{m} 0.4m \cdot 5mA^2 = 1.6mW \tag{6.1}$$

As the ^3He freezing power in 300mK region it's around $400\mu W$ is plausible that in part the P_{diss} influences the ^3He evaporation while the most part is

absorbed by other regions in cryostat. This power has to be reduced of about 10 factor by reducing the supply current under 2mA.

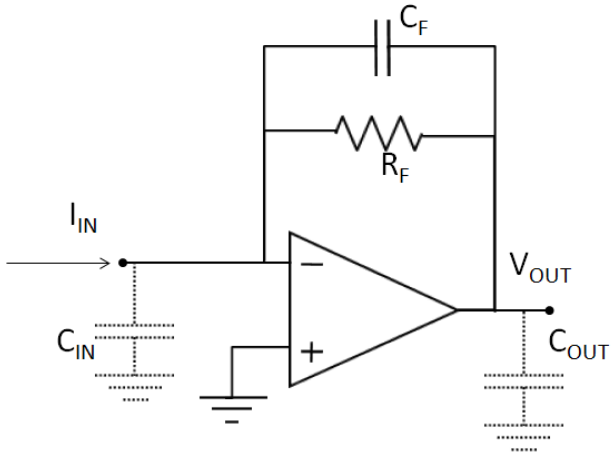

Figure 6.1: Schematic of cryogenic transimpedance, the circuit is inserted into cryostat the input capacitance is 50pF due to the wire between sample and amplifier (about 20 cm) and the output capacitance is 1nF due to long wire to reach the room temperature system (3-4 meter). The gain is $-R_f$ and signal bandwidth is $f_{sig} = 1/(2\pi C_f R_f)$.

6.1 High Speed Cryogenic Transimpedance Amplifier

The classical transimpedance amplifier schematic is in figure 6.1, the ideal gain can be calculated supposing a ideal opamp:

$$G_{id} = \frac{-R_f}{1 + sC_f R_f} \tag{6.2}$$

the loop gain results:

$$G_{loop} = A(s) \cdot \beta(s) = \frac{A_0}{1 + s\tau_0} \cdot \frac{1 + sR_f C_f}{1 + sR_f(C_f + C_{in})} \tag{6.3}$$

in which A(s) is the transfer function of opamp with DC gain A_0 and dominant pole $f_0 = 1/(2\pi\tau_0)$, and the second factor $\beta(s)$ is the transfer function of feedback network from V_{out} to the input inverting terminal of opamp (V^-); this network introduces in loop gain one zero $f_z = 1/(2\pi C_f R_f)$ and one pole $f_p = 1/(2\pi R_f(C_{in} + C_f))$. In figure 6.2 there is the graph of A(s) and $1/\beta(s)$ in function of frequency. The loop gain ($G_{loop} = A(s) \cdot \beta(s)$)in this graph

is equivalent to the area between the curves A(s) and $1/\beta(s)$; this kind of representation of the loop gain permits to separate the contribute on it due to opamp and to feedback network.

The stability of system is described by phase margin (PM) that is defined as the phase of loop gain at frequency in which his module is 1. If the phase margin is under 45° the response of the system is characterized by huge damped or spontaneous oscillation, between 60° and 45° the system has overshoot, for phase margin higher than 60° the response of the system is the typical of single pole response with constant time τ_T, in which the frequency where the magnitude of loop gain is 1, called cutoff frequency $f_T = 1/(2\pi\tau_T)$, corresponds to the frequency over which the feedback is no more active.

Considering the system in figure 6.1 with loop gain in equation 6.3 the phase margin is:

$$\angle G_{loop}(f) = DC_{phase} - atan\left(\frac{f}{f_0}\right) - atan\left(\frac{f}{f_p}\right) + atan\left(\frac{f}{f_z}\right) \tag{6.4}$$

if $f_0 << f_T$ and $f_p << f_T$ the phase at cutoff frequency f_T is approximately:

$$PM = \angle G_{loop}(f_T) \approx 180°\text{-}90°\text{-}90° + atan\left(\frac{f_T}{f_z}\right) = atan\left(\frac{f_T}{f_z}\right) \tag{6.5}$$

the stability of the systems depends so on relationship between f_T and f_z, the system can be: instable if $f_T << f_z$ (PM≈0°), moderately stable if $f_T = f_z$ (PM=45°) or stable of $f_T >> f_z$ (PM≈ 90°). But $f_z = 1/(2\pi R_f C_f)$ is the pole of signal, so there is a trade-off between stability and bandwidth: to have high PM we have to reduce the bandwidth.

The insertion of feedback capacitance C_f in figure 6.1 helps the stability because it inserts a zero in loop gain that raise the phase margin.

But this is not the only way to proceed; we can put the zero f_z requested for stability in the opamp transfer function A(s) as shown in figure 6.3, in this case no capacitance on feedback is required enhancing the bandwidth. The $1/\beta$ became $(1 + sR_fC_{in})$ the zero has moved on A(s) transfer function. The ideal gain is $G_{id}(s) = -R_f$ doesn't contain poles so the signal bandwidth coincides with cut-off frequency f_T. The trade-off bandwidth-stability due to relation between f_T and f_z has been overtaken thanks to the insertion of the negative real part zero in opamp transfer function.

6.1.1 Pole-zero Opamp

In figure 6.3 there is a opamp transfer function with one dominant pole f_{01}, one negative real part zero f_z and high frequency pole[1] f_{02}. It's not usable

[1]In real circuits the gain at infinite frequency has to be always zero, so the number of poles must be higher than the number of zeros

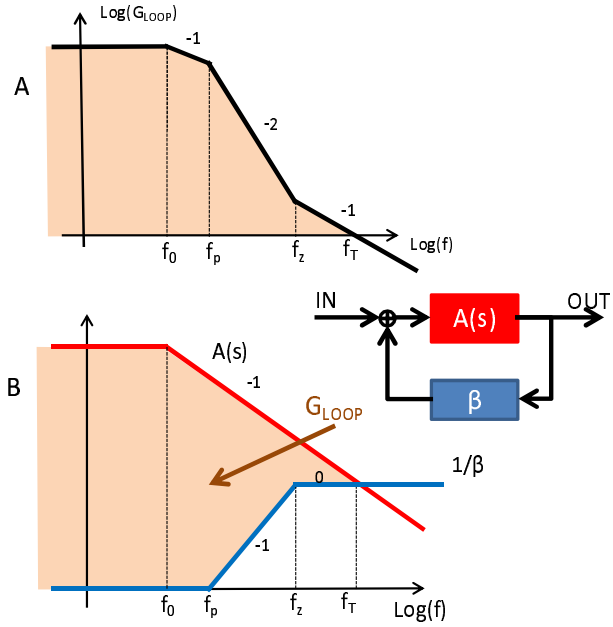

Figure 6.2: A: Module of loop gain in standard transimpedance amplifier, the system is stable if $f_z < f_T$. B: Opamp and feedback network contributes to loop gain: A(s) is the transfer function of opamp single pole; $\beta(s)$ is the transfer function of feedback network that has a pole in $f_p = (2\pi R_f(C_f + C_{in}))$ and a zero in $f_z = 1/(2\pi C_f R_f)$. f_z limit the bandwidth and determine the phase margin of the circuit.

the well-known simple structure two-stage miller compensated, used for transimpedance amplifier described in chapter 5, in this case we need a innovative topology.

A possible implementation of the transfer function in figure 6.3 is using a internal feedback loop as in figure 6.4; in which each trapezoidal shape is a trans-conductor; a block with input in voltage and output in current. The transfer function can be calculated by proceed with loop gain and ideal gain of internal loop composed by the blocks g_{m2}, R_{01} and R_{02} and in feedback the block g_{mr}. Considering a infinite gain in g_{m2} it possible to identify the node 1 as virtual ground, so the current from g_{m1} can go only to g_{mr} the voltage on R_r results $V_{in} \cdot g_{m1}/g_{mr}$. The ideal output voltage result:

$$V_{out} = \frac{g_{m1}}{g_{mr}} \cdot \frac{1 + sR_r(C_0 + C_r)}{sC_0R_r} V_{in} \tag{6.6}$$

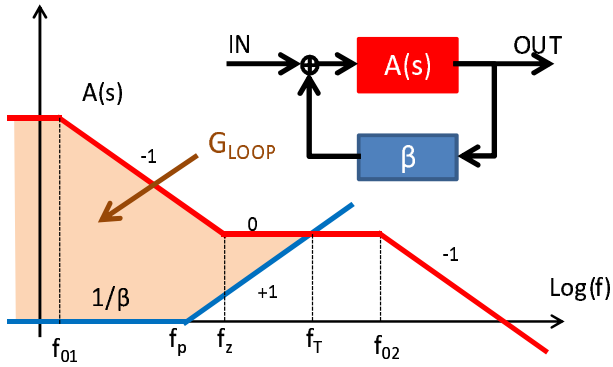

Figure 6.3: High speed transimpedance amplifier loop gain: the zero f_z is inserter into A(s) instead $\beta(s)$. No feedback capacitance, that limits the signal bandwidth, is required. The current signal is correctly amplified until the feedback is active so up to the cut-off frequency.

The internal loop gain, if $C_m >> C_1$ and $g_{m1}R_1, g_{m2}R_2 >> 1$, results:

$$G_{loop}^{int} = -G_{i0}\frac{sR_rC_0}{1+sR_r(C_0+C_r)}\frac{\left(1-s\frac{C_m}{g_{m2}(1-g_{m2}R_m)}\right)}{(1+sR_{01}R_{02}g_{m2}C_m)\left(1+s\frac{C_m(C_1+C_2)+C_1C_2}{g_{m2}C_m}\right)}$$
$$G_{i0} = g_{m2}g_{mr}R_{01}R_{02} \tag{6.7}$$

in figure 6.5 there is the internal loop gain of structure in figure 6.4. The loop gain is composed by a zero in s=0, a pole due to feedback structure f_r, and the two poles f_{01}, f_{02} and the zero f_{z1} due to miller effect and pole splitting of C_m that is a miller capacitor for block g_{m2} (section 5.3.3); the singularities are:

$$f_{01} = \frac{-1}{2\pi R_{01}R_{02}g_{m2}C_m} \tag{6.8}$$

$$f_{02} = \frac{-g_{m2}C_m}{2\pi(C_m(C_1+C_2)+C_1C_2)} \tag{6.9}$$

$$f_r = \frac{-1}{2\pi R_r(C_0+C_r)} \tag{6.10}$$

$$f_{z1} = \frac{g_{m2}}{2\pi C_m(1-g_{m2}R_m)} \tag{6.11}$$

The real gain of internal structure corresponds to ideal gain in frequencies in which the loop gain is higher than 1, the loop gain in flat region between f_{01} and f_r is $G_L = g_{mr}R_rC_0/C_m$ (figure 6.5. The module of loop gain is higher than 1 from f_A to f_B if $G_L > 1$ (figure 6.7), in which:

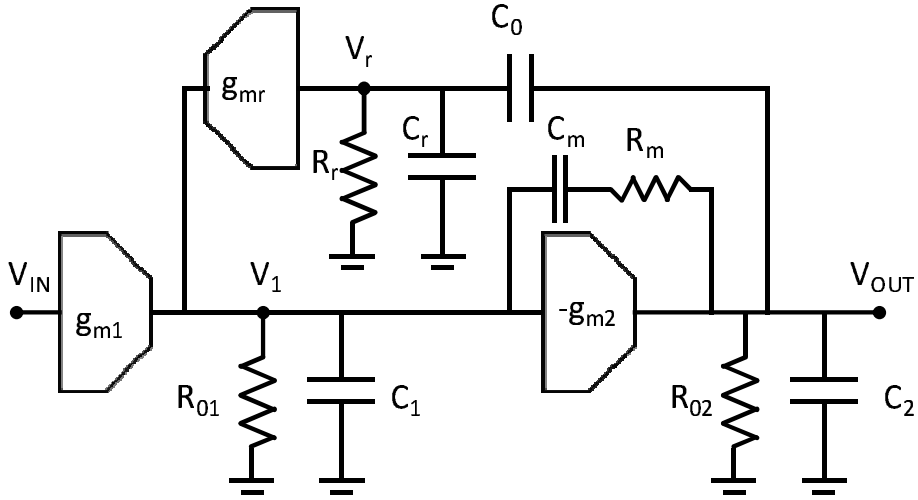

Figure 6.4: Structure of novel pole-zero opamp, the internal feedback permits the insertion of the requested zero f_z.

$$f_A = \frac{1}{2\pi g_{m2} g_{m3} R_{01} R_{02} R_r C_0} \qquad (6.12) \qquad f_B = \frac{g_{mr}}{2\pi C_m} \qquad (6.13)$$

The correspondent real gain is in figure 6.6, it coincides with ideal gain between f_A and f_B where loop gain is higher than 1. Outside this range the feedback is inhibited so the block g_{mr} in figure 6.4 can be neglected, and the real gain is coincident to the gain of two-stage opamp with miller compensa-

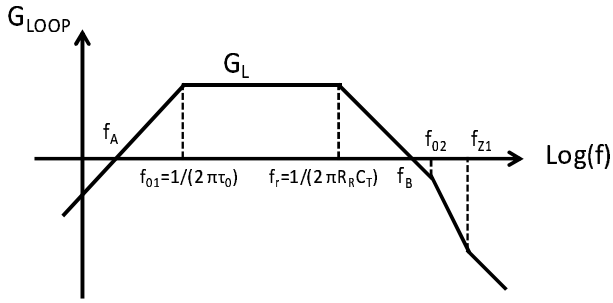

Figure 6.5: Loop gain of internal loop in opamp structure in figure 6.4, it has a magnitude higher than 1 from f_A and f_B if the flat gain $G_L = g_{mr} R_r C_0 / C_m$. is higher than 1.

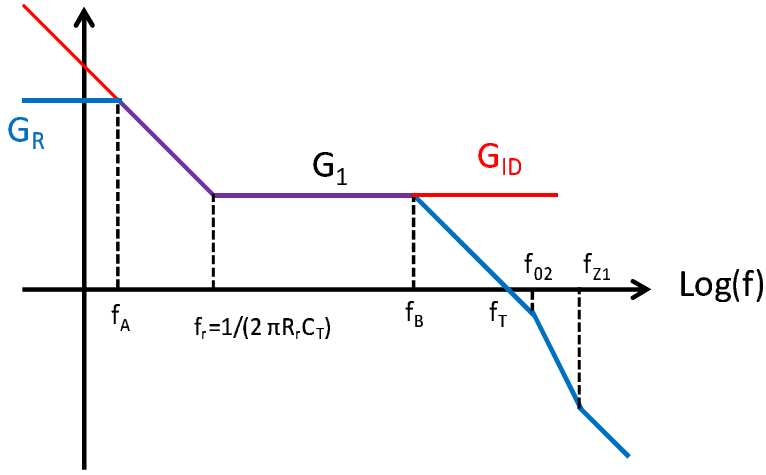

Figure 6.6: Ideal gain and real gain of internal loop in figure 6.4 in function of frequency. The real and ideal gain are coincident in frequencies in which $G_{loop}^{int} > 1$ so between f_A and f_B. When the $G_{loop} < 1$, it's not sufficient to implement a feedback and so the real gain corresponds to the gain of g_{m1} and g_{m2} blocks.

tion:

$$G_{miller} = -g_{m1}g_{m2}R_{01}R_{02}\frac{\left(1 - s\frac{C_m}{g_{m2}(1-g_{m2}R_m)}\right)}{(1 + sR_{01}R_{02}g_{m2}C_m)\left(1 + s\frac{C_m(C_1+C_2)+C_1C_2}{g_{m2}C_m}\right)} \tag{6.14}$$

combining all these information the real gain results:

$$G_r = \begin{cases} g_{m1}g_{m2}R_{01}R_{02} & f < f_A \\ \frac{g_{m1}}{g_{mr}} \cdot \frac{1+sR_r(C_0+C_r)}{sC_0R_r} & f_A < f < f_B \\ \frac{-g_{m1}}{sC_m} \frac{\left(1-s\frac{C_m}{g_{m2}(1-g_{m2}Rm)}\right)}{\left(1+s\frac{C_m(C_1+C_2)+C_1C_2}{g_{m2}C_m}\right)} & f > f_B \end{cases} \tag{6.15}$$

This real gain corresponds to the opamp transfer function requested for high speed transimpedance amplifier (figure 6.3). We have added a zero in opamp transfer function at f_r.

6.2 Low-Noise design procedures

The current resolution of the system is determined by the integral of the input noise spectrum. In figure 6.7 there is the schematic of fast transimpedance

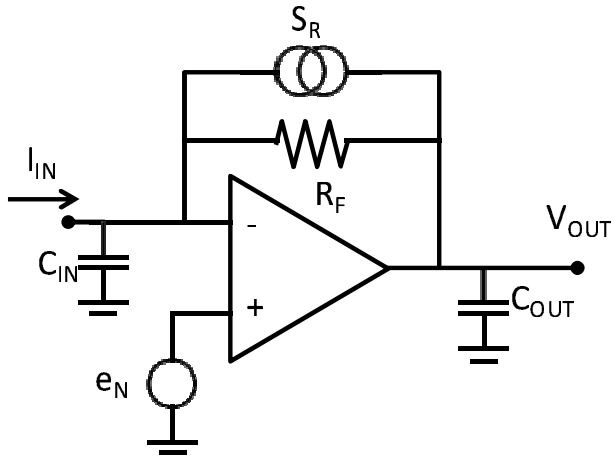

Figure 6.7: Schematic of fast transimpedance amplifier with the noise sources: the thermal noise due to feedback resistor S_r and the series noise of opamp e_N. We neglect the parallel noise due to opamp because in cmos technology it's usually negligible.

amplifier in which we add also the noise sources due to feedback resistors and to opamp, which is modeled like a voltage sources e_N on non-inverting terminal. The current noise from opamp, also called parallel noise, has been neglected because it's due to the shot noise of bias current on input terminal of opamp and that is usually negligible in cmos technology. The input noise results (see section 5.3.1 for calculations):

$$S_{in}^2 = \frac{e_n^2}{R_f^2} + \frac{4kT}{R_f} + s^2 e_n^2 C_{in}^2 \tag{6.16}$$

If we suppose that noise e_n is due only to input pair mosfet of the first differential stage of opamp (correspondent to g_{m1} block in figure 6.4) it becomes:

$$e_n^2 = \frac{4}{3}\frac{4kT}{g_m} + \frac{2K_f I_d^{A_f}}{C_{ox} L^2 g_m^2 f} \tag{6.17}$$

If we substitute the relation concerning e_n into the input noise expression, and than we integrate between the frequency f_{low} and frequency B; we obtain the same expression present in 5.9. Which can be minimized by choosing a input pair opamp with dimension W and L satisfying:

$$C_{ox} W L = \frac{C_p}{3} \tag{6.18}$$

This is the same condition on 5.11 as the parasitic capacitance C_p is the same 50pF. So the dimensions of Nmos in input pair are the same respect

cryogenic transimpedance amplifier describer in chapter 5: $W = 2500\mu m$ and $L = 1.4\mu m$. The current bias I_d is choose to minimize the noise according to:

$$I_d = \left(\frac{16\sqrt{2}}{9} \frac{\sqrt{k_n W} k T C_{ox} L^{\frac{3}{2}}}{K_f} \cdot B \right)^{\frac{1}{A_f - 0.5}} = 6\mu A \tag{6.19}$$

in which $W = 2500\mu m$, $L = 1.4\mu m$, $k_n = 4mA/V^2$, $k = 1.338e-23J/K$, $T = 4K$, $C_{ox} = 4.45e-3F/m^2$ and $K_f = 25.5e-27$. In this case the current is a bit higher respect that on chapter 5 due to the increased bandwidth B=200kHz instead B=30kHz, but this value is limited to avoid the sub-threshold region of input transistor's opamp which can affect the coupling (section 3.2.1):

$$I_d = \frac{1}{2} \cdot 4m \frac{A}{V^2} \cdot \frac{2500\mu m}{1.4\mu m} (3mV)^2 = 32\mu A \tag{6.20}$$

so we design the input pair transistor with Nmos with $I_d = 50\mu A$, $W = 2500\mu m$ and $L = 1.4\mu m$. We choose Nmos to have higher input common-mode voltage range respect to Pmos due to higher threshold.

6.3 Dimensioning

We had already dimensioned the input pair transistor parameters $I_d = 50\mu A$, $W = 2500\mu m$ and $L = 1.4\mu m$ to minimize the noise. Let see the other design proceduces starting with feedback resistor.

6.3.1 Feedback resistor

The feedback resistor of transimpedance amplifier is the most important component because it fixed the gain, the voltage range of amplifier. We want to raise the bandwidth of transimpedance from 30kHz (chapter 5) to 200kHz to are able to see high frequency effects in quantum dots. As seen in section 5.2.2 a value in $M\Omega$ range of resistor are unusual in integrated circuit because the parasitic capacitance on it will affect his functioning. In transimpedance describer and tested in chapter 5, a resistance of $R_f = 22M\Omega$ was able to work up to 30kHz with no parasitic effect at 4K while a small overshoot in transfer function is present at room temperature. The additional parasitic pole due to parasitic capacitor is proportional to:

$$f_p \propto \frac{1}{R_f C_p} \tag{6.21}$$

To avoid influence of parasitic capacitance up to 200kHz, we need to move consequently the parasitic pole; we can reduce the feedback resistor from $22M\Omega$

to about one third $R_f = 8.6M\Omega$; to move the parasitic pole over a decade; as the parasitic capacitance is proportional on resistance area so on his value at the same width; in this case we are in the same case of chapter 5.

6.3.2 First stage of opamp

The input pair transistor has been already designed of geometry W/L and bias current, in order to minimize his noise maintaining the saturation regime. The dimensioning of the first stage of opamp (the g_{m1} block in figure 6.4) follows the same design procedure respect to the first stage of opamp described in section 5.3; so we design this first stage using a the double Pmos mirror to avoid that the input pair drains are involved into high impedance gain node. The g_{m1} block is showed in figure 6.8; the transconductance of first stage is the transconductance of input pair transistor and result: $\sqrt{2k_n(W/L)I_d} = 26.7mA/V$.

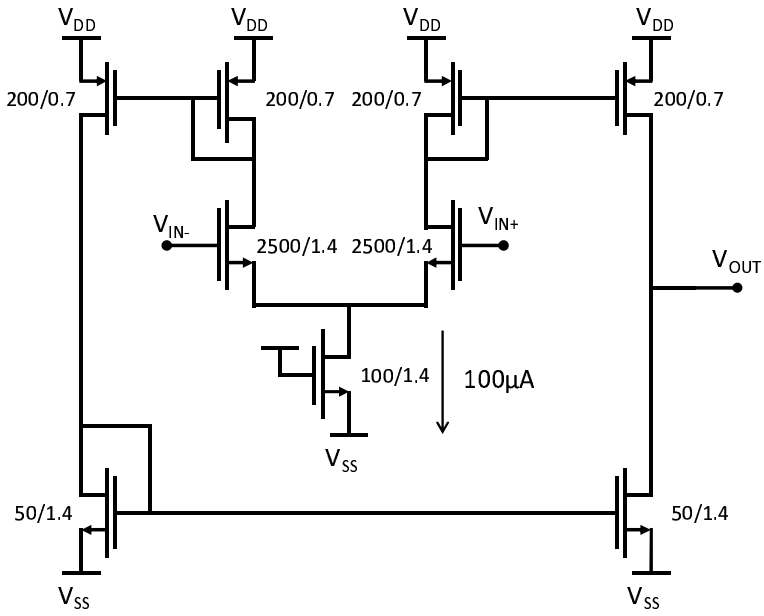

Figure 6.8: Schematic of first stage g_{m1} block in figure 6.4, the dimension are in μm, the transconductance of first block is the transconductance of input pair and results: $\sqrt{2k_n(W/L)I_d} = 26.7mA/V$.

6.3.3 Internal feedback dimensioning

The internal feedback has to solve the task to obtain the opamp transfer function shape in figure 6.9, by adding a zero in transfer function at f_z and

a second high frequency pole. Refer to figure 6.9, the feedback resistance of transimpedance amplifier has already been dimensioned for bandwidth and noise requirement at $8.6M\Omega$. With an input capacitance of 50pF the f_p is defined by:

$$f_p = \frac{1}{2\pi R_f C_{in}} = 370Hz \tag{6.22}$$

the requested bandwidth (correspondent to f_T) for our transimpedance amplifier is 200kHz, so is possible to determine the flat region gain of A(s) with:

$$G_{flat} = \frac{f_T}{f_p} = 540 \tag{6.23}$$

According to ideal gain of internal loop in figure 6.6, we can write the relationship:

$$G_{id} = \frac{g_{m1}}{g_{mr}} \cdot \frac{1 + sR_r(C_0 + C_r)}{sC_0R_r} \overset{Flat\ region}{\rightarrow} G_{flat} = \frac{g_{m1}}{g_{mr}}\left(1 + \frac{C_r}{C_0}\right) \tag{6.24}$$

Combining the equations 6.24 and 6.23; we obtain:

$$g_{mr} = \frac{g_{m1}}{G_{flat}} \frac{1}{\left(1 + \frac{C_r}{C_0}\right)} = 50\mu A/V \frac{1}{\left(1 + \frac{C_r}{C_0}\right)} \tag{6.25}$$

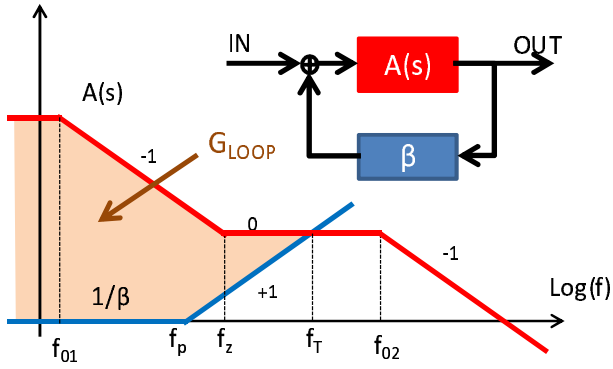

Figure 6.9: A(s) gain and $1/\beta(s)$ the cut-off frequency f_T is defined by R_f, C_{in} and by the gain of flat region of A(s) between f_z and f_{02}.

The partition between C_r and C_0 essentially defines the voltage input range of g_{mr}, referring to figure 6.4, the output node is the voltage output of transimpedance amplifier so it can be a sine wave with 1.5V amplitude and 200kHz frequency, we decided to design $C_r = C_0$ to reduce the voltage V_r up to $\pm 0.75V$ more easy to manage for g_{mr} block. The value of transconductance of g_{mr} belong to equation 6.25 is $25\mu A/V$.

Looking at figure 6.9 we can also calculate the phase margin (PM) of external loop gain:

$$\begin{aligned} PM &= DC_{phase} - atan\left(\frac{f_{01}}{f_T}\right) - atan\left(\frac{f_p}{f_T}\right) + atan\left(\frac{f_z}{f_T}\right) - atan\left(\frac{f_{02}}{f_T}\right) \\ &= 180^\circ - 90^\circ - 90^\circ + atan\left(\frac{f_z}{f_T}\right) - atan\left(\frac{f_{02}}{f_T}\right) \end{aligned} \tag{6.26}$$

so if the $f_z << f_T$ and $f_{02} >> f_T$ the phase margin result about 90°. As $f_T = 200kHz$, we impose $f_z = 20kHz$ and $f_{02} = 2MHz$ and remembering their expression, we obtain:

$$\begin{aligned} f_z &= \frac{1}{2\pi R_r(C_0 + C_r)} = \frac{1}{4\pi R_r C_r} = 20kHz \\ f_{02} &= \frac{g_{mr}}{2\pi C_m} = 2MHz \Rightarrow C_m = \frac{g_{m3}}{2\pi 2MHz} = 2pF \end{aligned} \tag{6.27}$$

we remember that f_{02} is the frequency in which the internal loop ends to be functional (correspondent of f_B in figure 6.6 defined by expression 6.1.1); from the equation 6.27 we design $C_0 = C_r = 5pF$ and $R = 800k\Omega$ as good compromise for area.

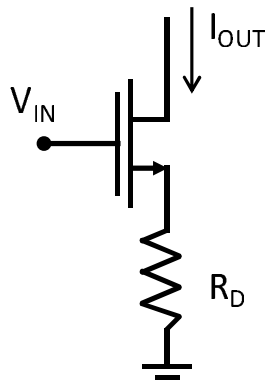

Figure 6.10: Degenerated amplifier stage, the equivalent transconductance is: $g_{mEQ} = (R_D + 1/g_m)^{-1}$ that is about $1/R_D$ if $g_m >> R_D$.

Let now dimension the g_{mr} block, according to relation 6.25 $g_{mr} = 25\mu A/V$; this transconductance is very low considering the cryogenic transistor geometry used for synthesize the whole system which with $10\mu A$ of current has a transconductance $560\mu A/V$ for Pmos $50\mu m/0.7\mu m$ and 1.6mA/V for Nmos $50\mu m/1.4\mu m$. Use a lower bias current than $10\mu A$ can be problematic, due to the sub-threshold effect on coupling of current mirror (section 3.2.1). We have

to synthesize a lower transconductance stage with high conductive transistor; our idea is to use degenerated resistors stage, like in figure 6.10; the equivalent transconductance from transistor gate voltage to drain current is:

$$g_{mEq} = \frac{1}{\frac{1}{g_m} + R_D} \overset{R_D >> 1/g_m}{\rightarrow} g_{mEq} = \frac{1}{R_d} \tag{6.28}$$

using a Nmos $50\mu m/1.4\mu m$ with $I_B = 10\mu A$ ($g_m = 1.6mA/V$) and a resistor $R_D = 40k\Omega$, we obtain the requested transconductance $g_{mr} = 25\mu A/V$. The current bias of the system in figure 6.10 is usually defined by gate voltage, but as the threshold voltage is variable from 0.4V to 0.7V from 300K to 4K; will be hard to bias correctly the transistor with $10\mu A$ because:

$$I_d = \frac{V_{gate} - V_{tn} - V_{ov}}{R_D} \tag{6.29}$$

in this case the threshold variation can affects drastically the current bias. To obtain a more stable biasing we use another identical stage driven by the requested current and in which the Nmos is connected in transdiode configuration to the gate of main amplifier transistor thought the resistance R_r in figure 6.4; refer to figure 6.11: if the mosfets M_1 and M_2 are well-coupled like also the resistances R_r and $R_r^{'}$ the voltage on gate of M_1 is the correct DC voltage that allow a current bias I_D current stable.

6.3.4 Second stage dimensioning

The second stage of opamp has to solve some important tasks, first of all he had to permit a good stable internal feedback and he also have to drive the output node in efficiency way. This second condition is related to power consumption; in cryogenic transimpedance amplifier described in chapter 5; we used as second stage, a simple common source stage with a current source for biasing. The maximum current required from the output was 1mA due to slew rate requirement and this fixed the current bias in 1mA continuously, also if not necessary in a certain moment.

In figure 6.12 there is a comparison of three different output circuits: the first is the common-source, as told before in this case the maximum amplitude of output current corresponds to bias current; the second is the push-pull stage in which each transistor behave like a source follower, in this case the bias current can be very low while the maximum output current can be high, but the output voltage range of push-pull stage is $V_{dd} - V_{ss} - V_{tp} - V_{tn} = 1V$,in fact due to threshold voltages we lose 2V of output range and this is unacceptable. The last output circuit is a inverter-like output circuit, the output maximum current is the maximum saturation current of each mosfet, while the bias

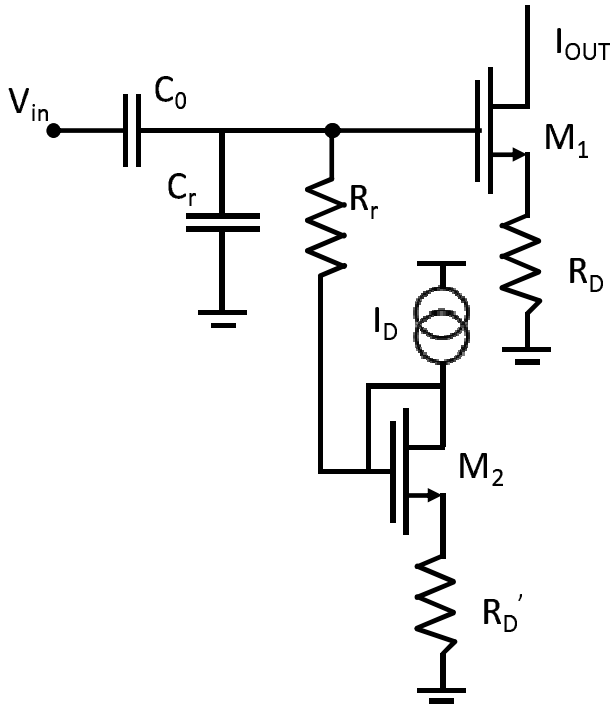

Figure 6.11: Bias for degenerated amplifier stage g_{mr}; if the mosfet M_1 and M_2 and the resistance R_r anr $R_r^{'}$ are well-coupled; the dc bias current $I_{out} = I_D$ on the degenerated stage is stable with process variation in temperature.

current can be very low. We choose this third circuit, because it has high efficiency than the first (common-source) and higher output voltage range than the second (push-pull). But this output circuit requires for a good biasing two different nodes for drive the two output transistor's gates. A very good structure which permit a precise biasing of output stage is in figure 6.13 in which each output transistor is driven by a different gain node.

So the second stage, equivalent to g_{m2} in figure 6.4, is a bit complex than second stage in opamp described in chapter 5, where it was composed by two transistors; now we had a stage g_{m2} which drives the output Nmos (which act as an additional gain stage), while the Pmos is driven directly by input node and this path is in parallel to stage g_{m2}. In this way, neglecting the internal feedback, the operational amplifier is composed by three gain stages; first stage (g_{m1}) in figure 6.8, second stage (g_{m2} in figure 6.13) and a third gain composed by output transistor.

The multistage operational amplifier has been long studied because it can allows a good gain operational amplifier also for low voltage technology, in

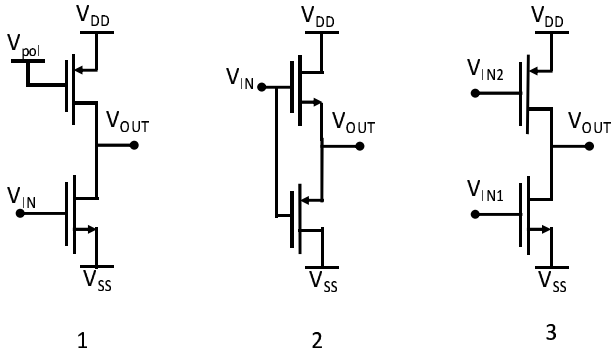

Figure 6.12: Comparison of different output circuit: 1 is a source common, 2 is a push-pull, 3 is a inverter-like output.

which the low supply reduces the dc gain of stages [50]. They require a non-trivial compensation due to the presence of three gain nodes. Miller compensation and pole splitting is no more usable as before.

6.3.5 Stability of inner loop

In this section we will analyze the stability of the inner loop in figure 6.4; in fact to obtain a stable multi feedback circuit every loop must be stable. We start by calculating the transfer function of g_{m2} block which is as seen on previous section it's not a single gain stage, but his equivalent block system is on figure 6.14. This is the equivalent A(s) of inner loop and the g_{mr} stage is the equivalent feedback, the two miller capacitance C_{m1} and C_{m2} are the nested miller compensation capacitance [50] requested to obtain a pole splitting also in multi-stage opamp.

The transfer function of this second stage is:

$$\frac{V_{out}}{I_{in}} = -g_{m2}g_{m3}R_1R_2R_3\frac{1+C_{m2}\left(\frac{g_{mf}-g_{m2}}{g_{m2}g_{m3}}\right)s-\frac{C_{m1}C_{m2}}{g_{m2}g_{m3}}s^2}{(1+s\tau_0)\left(1+\frac{C_{m2}(g_{mf}+g_{m3}-g_{m2})}{g_{m2}g_{m3}}s+\frac{C_3C_{m2}}{g_{m2}g_{m3}}s^2\right)} \tag{6.30}$$

in which $\tau_0 = C_{m1}g_{m2}g_{m3}R_1R_2R_3$ is the first miller pole present in figure 6.5 as f_{01}. The others pole has to be far from cut-off frequency of inner loop f_T in order to obtain a 90° phase margin on internal loop. The cut-off frequency of internal loop should be 2MHz (see relationship 6.27) so the other singularities of 6.30 has to been at least at 20MHz. We design $g_{m3} = g_{mf}$ to have a

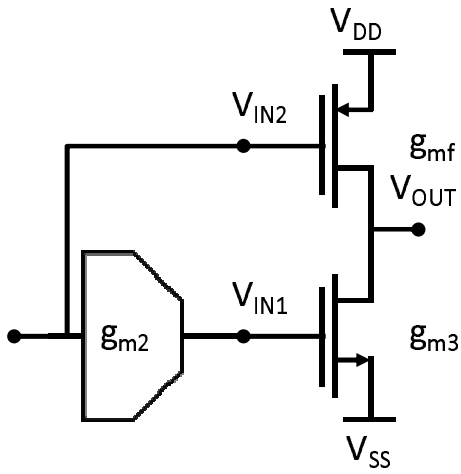

Figure 6.13: Schematic of block g_{m2} in figure 6.4. It used a single stage and then a inverter-like output stage. The is also a feed-thought path on gate of output Pmos

symmetric output stage, and if we consider $g_{m3} >> g_{m2}$ we obtain:

$$\begin{aligned} f_{p2} &= \frac{g_{m2}g_{m3}}{2\pi(g_{mf}+g_{m3}-g_{m2})} \approx \frac{g_{m2}}{4\pi C_{m2}} = 20MHz \Rightarrow g_{m2} = 250\mu A/V \\ f_{p3} &= \frac{g_{mf}+g_{m3}-g_{m2}}{2\pi C_3} \Rightarrow g_{m3} = 125\mu A/V \end{aligned} \tag{6.31}$$

in which we suppose $C_{m2} = 1pF$ and $C_3 = 2pF$, C_{m2} has to be higher than parasitic capacitors C_1 and C_2 while C_3 is the capacitance of output node which is usually higher than internal parasitics. According to the condition $g_{m3} >> g_{m2}$ we design $g_{m3} = 2.3mA/V$.

Zeros compensation

In transfer function of internal loop present in 6.30 there are also two zero associated to the miller capacitance C_{m1} and C_{m2}. These two zeros must be places beyond the cut-off frequency of internal loop $f_T = 2MHz$ because right half-plane zero near f_T reduce drastically the phase margin. There are several ways to cancel or move away at high frequency like using nulling resistors [51] or voltage buffer [52], or current buffer [53].

The zeros in transfer function 6.30 are caused by the parallel signal path of miller capacitance. There are several ways to break this parallel path maintaining the internal feedback that ensures the miller effect; for example a series resistance yet described in chapter 5, that can delete the zero if:

$$R_m = \frac{1}{g_m} \tag{6.32}$$

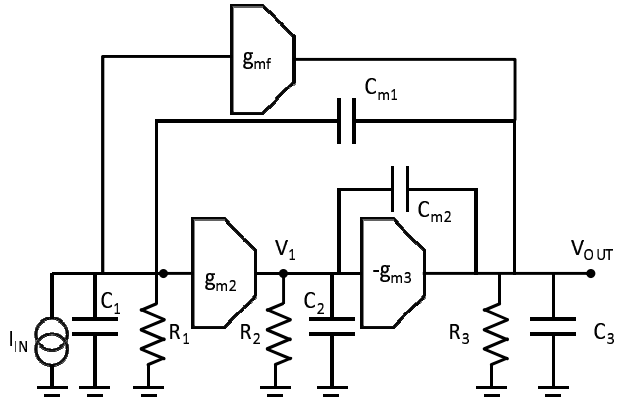

Figure 6.14: Block diagram of second stage of opamp, the feed-through trans-conductor g_{mf} is the output Pmos on figure 6.13. The main path is composed by two gain stages g_{m2} and g_{m3}; a nested miller compensation is necessary to obtain a stable system even with multistage amplifier[50].

but this requires a well coupling between a transconductance and a resistance; not so easy to obtain in integrated technology where the absolute precision of integrated parameters is about 10%.

The voltage buffer method is also used to eliminate totally the parallel path. But this method requires a new voltage stage which use as input the output voltage of transimpedance amplifier; a large input voltage range is required for this voltage buffer stage.The last is current buffer method do not affect the output node; the current buffer is less affected by output variations, it has low input impedance and high output impedance and it's a block in which the input current is equal to the output current. The input terminal is

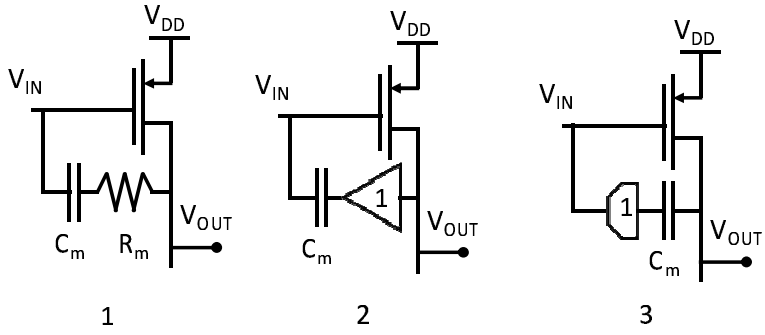

Figure 6.15: Different networks for zero compensation: 1 is nulling resistor, 2 is voltage buffer, 3 is current buffer. The current buffer method do not require good coupling and reduce the impedance on miller capacitance C_m.

connected to the miller capacitance C_m while the output is connected to the gate of transistor as in figure 6.15. With current buffer no high precision is required like in nulling resistor method, and moreover it also maintain a low impedance on miller capacitors [53] which aid to keep at high frequency non wanted poles.

Finally we design the bias current of second stage $I_d = 10\mu A$ and output stage $I_d = 50\mu A$. The current as been designed in order to have the lowest current possible but avoiding the sub-threshold region, with a reasonable value of W/L. The requested slew-rate of transimpedance amplifier is:

$$SR_{req} = \frac{dV_{out}}{dt}_{MAX} = 2\pi 200kHz1.5V = \frac{1.88V}{\mu s} \tag{6.33}$$

The internal slew-rate of circuit is due the output current of each stage and the miller capacitances of the next stage; we obtain:

$$\begin{aligned} SR_1 &= \frac{I_1}{C_{m1}} = \frac{50V}{\mu s} \\ SR_2 &= \frac{I_2}{C_{m2}} = \frac{10V}{\mu s} \end{aligned} \tag{6.34}$$

Where $I_1 = 100\mu A$, $I_2 = 10\mu A$, $C_{m1} = 2pF$ and $C_{m2} = 1pF$. For third stage the slew rate is due to maximum output current and the load capacitor; the maximum current in output stage in figure 6.14 is $I_P = 0.5K_pW/L(3V - V_{tp})^2 = 1.5mA$ and for $I_N = 0.5K_nW/L(1.5V - V_{tn})^2 = 45mA$ according to current sign. Supposing a output capacitance of 2pF the output slew rate is: $1.5mA/2pF = 750V/\mu s$ higher than requested.

6.4 Constant biasing

The complex system here discussed has a functioning strictly depending on the mosfet parameters and in particular on mosfet's transconductance, so his performances and also it functionality depends on temperature range. We have seen that some choices have been taken to permit a functioning independently on mosfet parameters like bias of g_{mr} stage and also the zero compensation thought current buffer that is in first order independent on transconductance variations. But the others stage (g_{m1}, g_{m2} and g_{m3}) have a transconductance that changes drastically with temperature, our solution is to use a constant g_m bias circuit for generate the bias currents, see figure 6.16 [54]; the Pmos transistors are identical and equalize the current on Nmos 1 and Nmos 2 whose

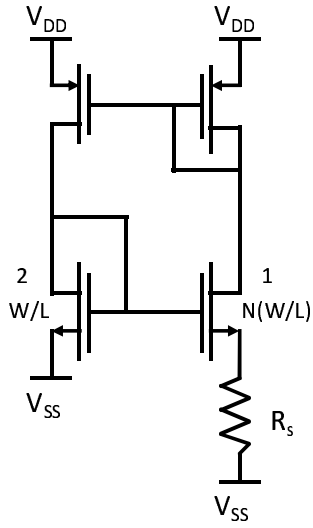

Figure 6.16: Constant g_m bias circuit, the Pmos mirror is symmetric and equalize the current on Nmos transistors. Transconductance of Nmos 2 depends only on geometrical ratio and resistance R_s.

overdrive is:

$$\begin{aligned} I_1 &= \frac{1}{2} k_n \frac{NW}{L} V_{ov1}^2 \\ I_2 &= \frac{1}{2} k_n \frac{W}{L} V_{ov2}^2 \end{aligned} \tag{6.35}$$

Considering that the currents are identical due to Pmos mirror, we obtain:

$$V_{ov2} = \sqrt{N} V_{ov1} \tag{6.36}$$

The voltage on the resistance is $V_{ov2} - V_{ov1}$ so the current I is:

$$I = \frac{V_{ov2} - V_{ov1}}{R_s} = \frac{\sqrt{N} - 1}{R_s} \cdot V_{ov1} = \frac{\sqrt{N} - 1}{\sqrt{N} R_s} V_{ov2} \tag{6.37}$$

so the transconductance of Nmos 2 can be written as:

$$g_m = \frac{2 I_d}{V_{ov2}} = \frac{2\left(\sqrt{N} - 1\right)}{\sqrt{N} R_s} \tag{6.38}$$

So the transconductance is independent on temperature variations even from 300K to 4K and on voltage supply variations.

The structure in figure 6.16 has, beyond the working point we described before, another working point that is zero current in both branch. A start-up circuit is so necessary to activate the circuit, fox example that on figure

6.17. If the system is in off-stable point the gate con M_2 should be at V_{ss}, but in this case M_{su} is in saturation region and inject current until the start-up of constant g_m bias circuit. Once M_2 is working correctly the M_{su} is in interdiction region and does't not affect the functioning of the circuit.

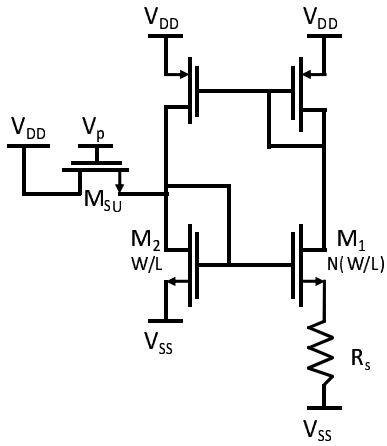

Figure 6.17: Start up of constant g_m circuit, the additional transistor M_{su} is in saturation region if the circuit is in off-state, injecting a current to set-up the circuit, but when the constant g_m circuit is on-state it is in interdiction region.

6.5 Voltage Amplifier

During the transimpedance design in the previous section we made a strong hypothesis; we suppose a 2pF of output capacitance and we design the transimpedance amplifier with this assumption; this is not true because the output terminal is connected to the wire thought room temperature systems, this wire has an output parasitic capacitance of 1nF. With such high value according to expression 6.31 the requested value for transconductance g_{m3} of output mosfet is 62mA/V, this is a very high value reachable with very large area and/or very large bias current; hard to obtain with for low-power system. In chapter 5 the same problem has been overtaken with the insertion of a resistor which decouples the output capacitance and the loop gain of transimpedance amplifier. This resistor inserts a pole $f_d = 1/(2\pi RC_{out})$, if the condition $f_{sig} < f_d < f_T$ is verified, this resistors masks the output capacitance C_{out} at f_T while maintaining unmodified the signal bandwidth f_{sig}. In this case the signal frequency and the cut-off frequency are coincident and the decoupling resistor is not more usable because the signal bandwidth would be reduced.

The solution we chose is to insert a voltage amplifier in the output of tran-

simpedance, which drives the output capacitance. This amplifier also compensates the reduction of signal amplitude due to the reduced feedback resistors, compared to transimpedance amplifier described in chapter 5.

6.5.1 Design of the output amplifier

In figure 6.18 there is the schematic of the system, after the transimpedance there is a voltage amplifier which is capable to drive the output capacitance of 1nF. First of design this block let consider now the effect of the parasitic capacitance C_p due to coupling between input pad and output pad which value can be about 100fF.

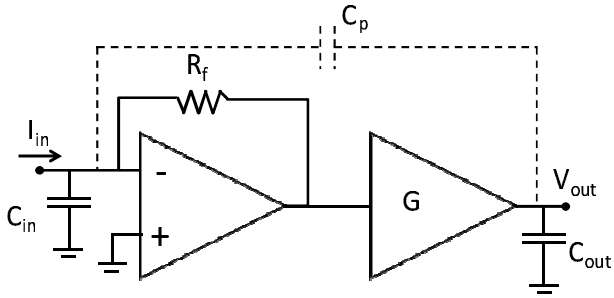

Figure 6.18: Schematic of cryogenic system, the parasitic capacitor from input pad to output pad limits the maximum gain of output voltage amplifier.

In particular let analyze the stability of this external loop due to C_p, below 200kHz the input node is a virtual ground due to transimpedance amplifier, so the loop gain is:

$$G_{loop}^{ext} = sC_p \frac{-8.6M\Omega}{(1+s\tau_1)(1+s\tau_2)} \cdot \frac{G}{1+s\tau_3} \tag{6.39}$$

where $1/(2\pi\tau_1)$ is the first pole of real gain of transimpedance that is 200kHz; $1/(2\pi\tau_2)$ is the second pole at 2MHz, G is the gain of voltage amplifier and $1/(2\pi\tau_3)$ is the pole of voltage amplifier. Over 200kHz the input node is no more a virtual ground and the input capacitance enters into loop gain expression. The transimpedance behave like voltage gain of 540 according to the real gain of transimpedance (equation 6.23). So the loop gain over 200kHz is:

$$G_{loop}^{ext} = \frac{-540}{(1+s\tau_2)} \frac{C_p}{C_p + C_{in}} \cdot \frac{G}{1+s\tau_3} \tag{6.40}$$

The resulting loop gain is graphed in figure 6.19, there is one zero in origin and 3 poles: the first at 200kHz, the second at 2MHz due to transimpedance, the flat region is $G_L = 540 \cdot C_p/C_{in} \cdot G$.

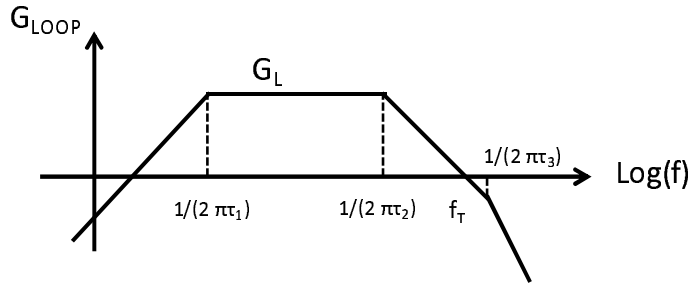

Figure 6.19: Magnitude of external loop gain of schematic in figure 6.18 there is a zero in the origin, than a pole at 200kHz, one at 2MHz due to transimpedance amplifier and one pole $1/(2\pi\tau_3)$, due to the voltage amplifier, if this last pole is beyond the cut-off frequency f_t the system will be stable.

The phase margin of this loop is:

$$\begin{aligned} PM &= atan(s) + atan(-C_p R_f G) - atan\left(\frac{f_T}{200kHz}\right) - atan\left(\frac{f_T}{2MHz}\right) + \\ &- atan\left(2\pi\tau_3 f_T\right) = \\ &= 90^\circ + atan(-G) - 90^\circ - atan\left(\frac{f_T}{2MHz}\right) - atan\left(2\pi\tau_3 f_T\right) \end{aligned} \tag{6.41}$$

the flat region of magnitude loop gain is higher than 1 also for $|G| = 1$. So the 0dB axis is crossed for sure beyond 2MHz, if G<0 the phase margin is lower than 45° because $f_T > 2MHz$. If G>0 we obtain atan(-G)=180° and the circuit is more stable; so we can not use a inverting gain for voltage amplifier. We must use a positive gain, the cutoff frequency result:

$$f_T = 540\frac{C_p}{C_{in}} G \cdot 2MHz = 7.2MHz \cdot G \tag{6.42}$$

in which $C_f = 100fF$ and C_{in} is 15pF the minimum input capacitance. The system is stable as long the cut-off frequency is well before respect to the non-dominant pole $1/(2\pi\tau_3)$ or others pole from transimpedance amplifier. With a gain of +9 the cut-off frequency results 65MHz; we define 9 as maximum gain. But we need the amplification only up to 200kHz that is the frequency of signal then the G can be G=1 reducing the cut-frequency at 7.2MHz. The non-dominant pole should be around 70MHz to obtain a good phase margin.

Let now described a few features of the voltage amplifier in figure 6.20 a classical non-inverting voltage amplifier, the gain is $G = (1 + R_2/R_1)$. The input common-mode range of it is equal to the input voltage. That is $\pm 1.5V/G$, equal to $\pm 1.5V$ for G=1 and $\pm 0.167V$ for G=9. The pole of voltage amplifier

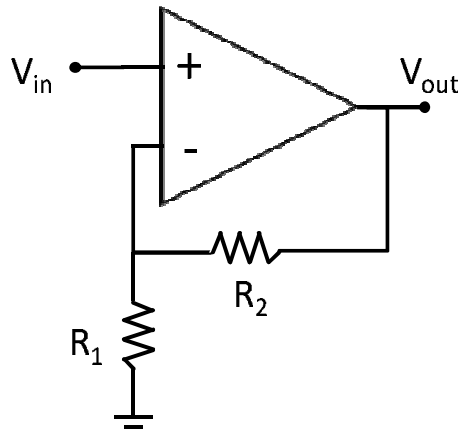

Figure 6.20: Schematic of standard non-inverting voltage amplifier, the gain is defined by $G = (1 + R_2/R_1)$.

must be at higher frequency respect $f_T^{MAX} = 65MHz$, the maximum cut-off frequency of loop in figure 6.19. The transimpedance output noise is due to feedback resistor and is:

$$S_{out} = \sqrt{\frac{4kT}{R_f}} = 43n\frac{V}{\sqrt{Hz}} \tag{6.43}$$

We impose a $4nV/\sqrt{Hz}$ as maximum acceptable input noise for voltage amplifier. From this condition we can design the value of R_1 resistance which should have a value lower than:

$$R = \frac{\left(4nV/\sqrt{Hz}\right)^2}{4kT} = 72k\Omega \tag{6.44}$$

we design $R_1 = 2k\Omega$ and $R_2 = 16k\Omega$ to being less affected by parasitic capacitance. A switch can short the R_2 resistor to obtain a gain flexible G=1 or 9. We limit the bandwidth of gain g=+9 up to 3MHz by a feedback capacitor of 3pF in parallel to R_2 so after it the gain is 1 aiding the stability.

6.5.2 Design of opamp of voltage amplifier

According to all the analysis done in the previous section, we can resume the specific for the opamp in the voltage amplifier:

- GBWP=70MHz
- Stable in unitary gain configuration

- Rail to rail input-output
- Input series noise about $4nV/\sqrt{Hz}$
- Low power
- Input parasitic capacitance of 1-2pF
- Stable up to 1nF of output capacitance

the first and the second conditions impose a non dominant pole higher than 70MHz. The input rail to rail voltage range capability is required because the input voltage range corresponds to the input voltage. The noise should be lower than transimpedance output noise to have high sensibility; the supply current should be lower than 5mA like in transimpedance amplifier presented in chapter 5. He should be able to drive correctly the output capacitance due to the long wire required before reach room temperature instruments.

The rail to rail input is obtainable by using two different pair Nmos and Pmos in the first differential stage of opamp, in order to manage high input voltage and low input voltage (figure 6.21).

The input pair has been dimensioned in order to have a constant g_m independently which pair is working, so we had to equalize the transconductance of Pmos and Nmos pair:

$$\begin{aligned} g_{mn} = g_{mp} \Rightarrow \sqrt{2k_n(W/L)_n I_d} = \sqrt{2k_p(W/L)_p I_d} \Rightarrow \\ \Rightarrow (W/L)_p = (W/L)_n \frac{k_n}{k_p} \Rightarrow (W/L)_p = 18 \cdot (W/L)_n \end{aligned} \tag{6.45}$$

The bias current is $I_d = 25\mu A$, it's has been designed as the minimum current which pushes the poles due to the mirrors be around 500MHz (one decade far from GBWP) with a reasonable dimension: the Nmos of mirrors have dimension $(W/L) = 50\mu m/1.4\mu m$, while the Pmos of mirrors have dimension $(W/L) = 200\mu m/0.7\mu m$. Consequently we define the input pair as $(W/L)_p = 500\mu m/0.7\mu m$ and $(W/L)_n = 50\mu m/1.4\mu m$. With these parameters the transconductance of input pairs is:

$$g_{mn} = g_{mp} = \sqrt{2k_p(W/L)_p I_d} = 2.7mA/V \tag{6.46}$$

The noise of input voltage amplifier results

$$S_i^2 = \frac{2}{3}\frac{4kT}{g_{mn}}\left(4 + 6 \cdot \frac{g_{mn2}}{g_{mn}} + 8 \cdot \frac{g_{mp2}}{g_{mn}}\right) = \left(0.905n\frac{V}{\sqrt{Hz}}\right)^2 \tag{6.47}$$

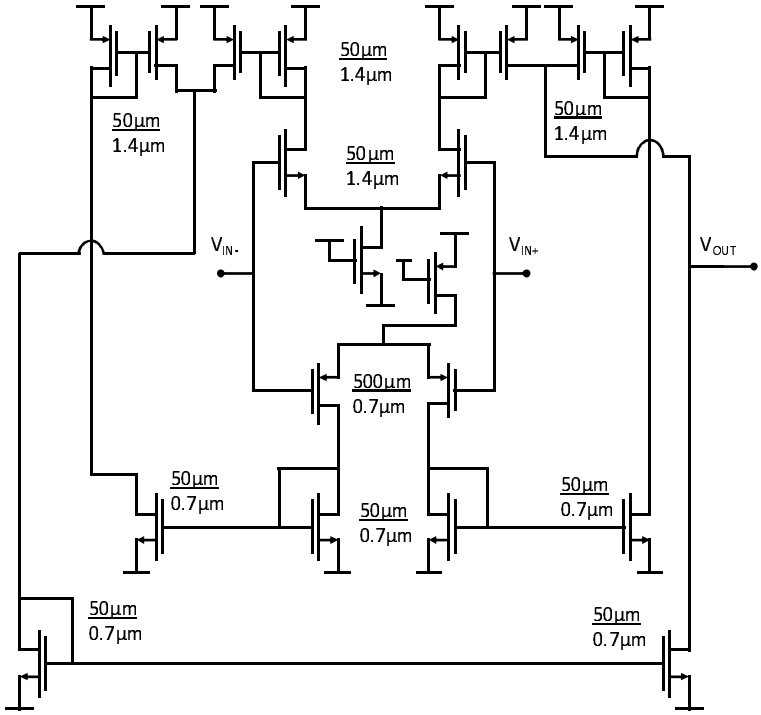

Figure 6.21: First stage of opamp in voltage amplifier, the rail to rail input is obtainable by doubling the structure of a simple differential stage inserting both a Nmos pair and a Pmos pair.

in which $g_{mn} = 2.7mA/V$ is the transconductance of input pair transistors, $g_{mn2} = 2.7mA/V$ is the transconductance of others Nmos in first stage that have all dimension $W/L = 50\mu m/1.4\mu m$, and $g_{mp2} = 1.78\mu A/V$ is the transconductance of Pmos in first stage except input pair $50\mu m/0.7\mu m$. We neglect the noise of tail transistor because it is rejected by differential structure.

6.5.3 Second stage

After dimensioned the first stage we proceed with the dimensioning of second stage of opamp in voltage amplifier. As the opamp described in section 6.2 we look for the output stage which permit a high efficiency and rail-to-rail output. As before we chose the output state 3 in figure 6.12; the inverter like circuit. Refer to figure 6.23 neglecting the M_7 M_8 and M_9 transistors. But this kind of output circuit is not so easy to bias, because but both output transistor M_5 and M_6 are gain transistor; the problem can be solved by driving this two transistor with two different gain nodes; in figure 6.23 we see that output

Nmos is driven by output of g_{m2} while Pmos is driven by output of g_{m1}; if the gain transistor of g_{m2} is a Pmos (like M_1) the current bias of output stage is due to the ratio of Pmos M_6 and M_1. But this topology require an additional stage (g_{m3}), so the opamp has at least three stage, the first (g_{m1}) has been already designed for input noise and input voltage range requirements; the second (g_{m2}) and the third stage (g_{m3}) add one pole for each; classical two-stage miller compensation are not usable in this case.

In literature exists different compensation for multistage amplifier [50]. The main idea is use two different miller capacitance between gain nodes 1-3 and 2-3 [55]. In this way the same concept of two-stage miller compensation is used also for three stage amplifier with a few difference. There are different variations of multistage compensation like multi-path [56]; with nesting of simple structure [57].

For driving high output capacitance such in this case the highest performances are achieved with AC boosting scheme [58] that respect to [57] has no additional input stage, which might introduces noise, and respect [56] has lower problems of coupling to canceling the zeros. The block diagram of the multistage AC boosting compensation is in figure 6.22 in parallel to gain stage 2 there is a ac-coupled stage which is capable to compensate the gain reduction of second stage at high frequency.

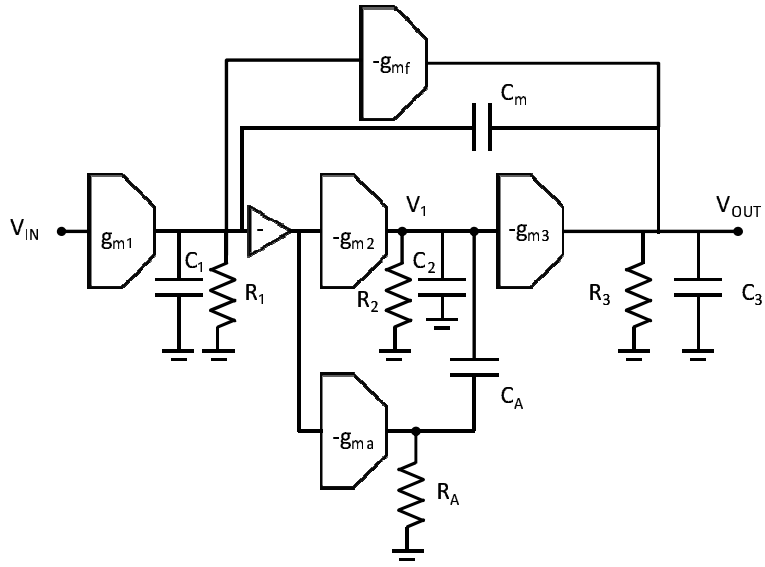

Figure 6.22: Scheme AC-boosting compensation for multistage amplifier; the second stage has a parallel path AC-coupled that compensates the reduction of gain due to high frequency.

If the following assumption are verified: $R_2 >> R_a$, $g_{m1}R_1 >> 1$, $g_{m2}R_2 >>$

1, $g_{m3}R_3 >> 1$, $C_a >> C_2$, $C_L >> C_m >> C_1$, the transfer function of amplifier in figure 6.22 can be written as:

$$A(s) = \frac{A_{DC}\left(1+\frac{s}{\omega_4}+\frac{s^2}{\omega_4\omega_5}+\frac{s^3}{\omega_4\omega_5\omega_6}\right)}{\left(1+\frac{s}{\omega_0}\right)\left(1+\frac{s}{\omega_1}+\frac{s^2}{\omega_1\omega_2}+\frac{s^3}{\omega_1\omega_2\omega_3}\right)}$$

In which

$$\begin{aligned}
A_{DC} &= g_{m1}g_{m2}g_{m3}R_1R_2R_3 \\
\omega_0 &= \frac{1}{C_m g_{m2}g_{m3}R_1R_2R_3} \\
\omega_1 &= \frac{1}{\left(A_h+\frac{g_{mf}}{g_{m3}}\right)}\frac{g_{m2}}{C_a} \\
\omega_2 &= \left(A_h+\frac{g_{mf}}{g_{m3}}\right)\frac{g_{m3}}{C_3} \\
\omega_3 &= \frac{1}{R_aC_2} \\
\omega_4 &= \frac{1}{\left(A_h+\frac{g_{mf}}{g_{m3}}\right)}\frac{g_{m2}}{C_a} \\
\omega_5 &= -\left(A_h+\frac{g_{mf}}{g_{m3}}\right)\frac{g_{m3}}{C_m} \\
\omega_6 &= \frac{1}{R_aC_2} \\
A_h &= (g_{m2}+g_{ma})\,R_a
\end{aligned} \tag{6.48}$$

A_{DC} is the dc gain, A_h is the gain of second stage at high frequency neglecting the effect of parasitic capacitance. If the poles are sufficient distant each others, we can approximate them with $p_i = -\omega_i$ for i=1,2,3 ; the same for zeros $z_1 = -\omega_4$,$z_2 = -\omega_5$ and $z_3 = -\omega_6$. As $C_3 >> C_a$, because C_3 is the output capacitance, the first non-dominant pole is p_1; it corresponds exactly to the first zero z_1, they cancel each other. The remaining non-dominant pole is p_2 and respect to the equivalent pole in a two stage miller compensation g_{m3}/C_L, it's about A_h times at higher frequency this is the main advantage of ac-boosting scheme.

In figure 6.23 there is the schematic of second, third and AC stage of cryogenic buffer; M_1 and M_2 composed the inverter to have a unitary gain there should be $g_{mM1} = g_{mM2}$, we design $(W/L)_{M1} = 500/0.7$ and $(W/L)_{M2} = 50/1.4$ for this reason. Neglecting the AC boost the non-dominant pole is:

$$f_{p2} = \frac{g_{m3}}{2\pi C_3} \tag{6.49}$$

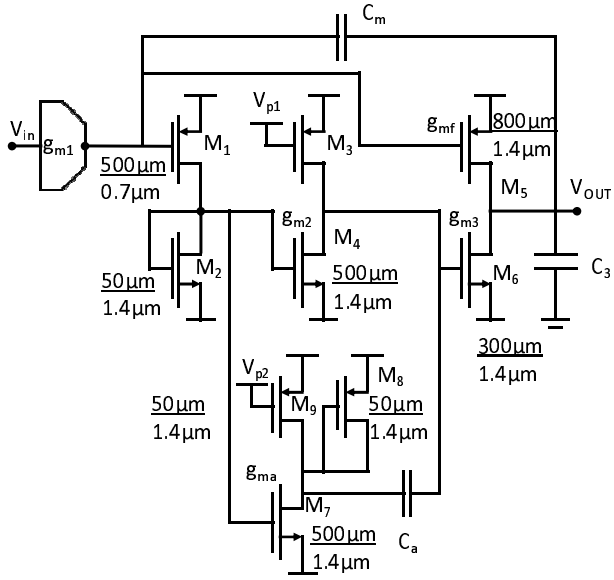

Figure 6.23: Schematic of second stage of opamp in voltage amplifier, M_1 and M_2 invert the signal, M_3 and M_4 composed the second stage, M_5 and M_6 are the output stage and M_7 and M_8 is the AC boosted second stage.

using reasonably high bias current $300\mu A$ and high area $300\mu m/1.4\mu m$ of M_6 Nmos dimension; we obtain the $g_{m3} = 22mA/V$ and the pole f_{p2} results at 3.6MHz. To move it through over 250MHz (in order to be far from GBWP=70MHz) and obtain a phase margin of scheme in figure 6.18:

$$PM = 90^\circ - arctan\left(\frac{70MHz}{250MHz}\right) = 74^\circ \tag{6.50}$$

so we had to design $A_h = 250MHz/3MHz = 85$, the ac-boosting stage in figure 6.23 suffers of one problem, as its output is ac-coupled; this results in a difficult the biasing because usually the stages are biased thanks to the dc feedback. For this reason we had to implement the load with transistor in transdiode configuration in order to well-bias the ac stage:

$$A_h = (g_{m2} + g_{ma})\, R_a = \frac{(g_{m2} + g_{ma})}{g_{mM8}} = \sqrt{\frac{k_p}{k_n}}\sqrt{\frac{I_{M7}}{I_{M8}}}\frac{\sqrt{\left(\frac{W}{L}\right)_{M4}} + \sqrt{\left(\frac{W}{L}\right)_{M7}}}{\sqrt{\left(\frac{W}{L}\right)_{M8}}} \tag{6.51}$$

In which we suppose $I_{M7} = I_{M4}$, the first factor due to technology is 4.26, the is designed with $I_{M7} = I_{M4} = 100\mu A$ and $I_{M8} = 10\mu A$. Finally we use $(W/L)_{M7} = (W/L)_{M4} = 500/1.4$ and $(W/L)_{M8} = 50/1.4$. Considering all this factor the boosting gain is about $A_h = 85$.

The bias of the output stage is obtained thought the connection between gate of M5 with gate of M1; in fact the these two mosfet has the same V_{GS} and their ratio of bias current is defined by their ratio of width, this is very common in multistage structures [50], [59], [60]. Other structures use feedback additional to control the current in output devices [61]. C_a is defined 3pF because to be higher than parasitic capacitors and the miller capacitance C_m is defined to obtain the requested gain bandwidth product:

$$C_m = \frac{g_{mn}}{2\pi GBWP} = 6pF \tag{6.52}$$

in which $g_{mn} = 2.7mA/V$ is the transconductance of first stage and GBWP is the gain bandwidth product of 70MHz.

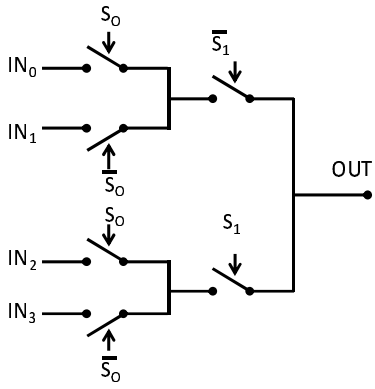

Figure 6.24: Tree structure of multiplexer the number of gates is minimal.

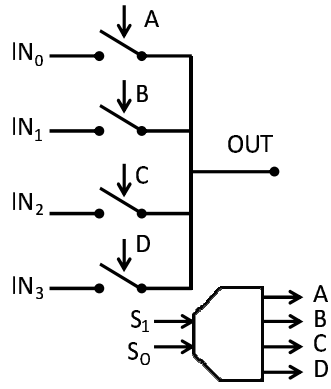

Figure 6.25: Multiplexer with minimum crossing signal. Requires a additional decoder

6.6 Cryogenic Multiplexer

As told several times in this thesis the biggest improvement of our system is the capability to insert the detection electronics into the cryostat reducing the input parasitic capacitance. The reduction on capacitance leads a non accessibility on the input node. To change the sample we need to extract the cryogenic probe and change the wire configuration, when cryostat is working; this is a dangerous situation in which we could contaminate the ^3He region with air. To allow a multi-channel measurement without extracting the probe, preventing damages into set-up, we also designed a multiplexer that connects a certain sample to the cryogenic transimpedance input. The timing of switch

sample is not critical, the capacitance of the multiplexer must be negligible respect to 50pF due to input capacitance. But the resistance has to be very low because it leads to bias modification on the quantum dot under test; if a $10\mu V$ of maximum error is allowed on bias, the resistance of multiplexed has to be:

$$R = \frac{V_{osMAX}}{I_{MAX}} = \frac{V_{osMAX}}{V_{OUTMAX}} R_f = 150\Omega \tag{6.53}$$

According to our set-up the sample region is composed by a 16 dual-in-line, considering 4 terminal for each sample, we can have up to 4 sample at the same time; accordingly to this we decide to implement a 4 channel multiplexer. We analyze two difference multiplexer topologies one in 6.24 is the topology in which the number of transistor is minimized, in fact only 2 inverter and 6 switches are required; another topology is in 6.25 here the current signal cross only one switch but a more complex combinator network is required, we decide to use this second topology because resistance requirement is more critical than area or switching time. In particular the topology in figure 6.25 requires a decoder and 4 switch. One of the four switch is showed in figure 6.26.

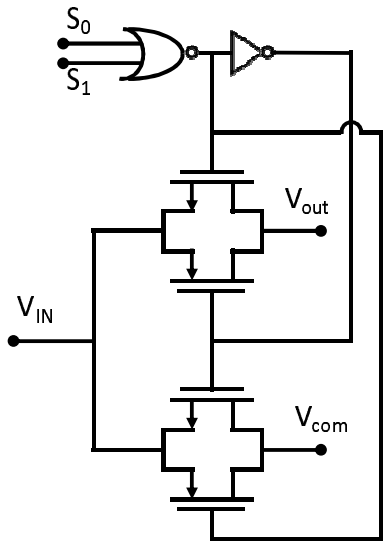

Figure 6.26: Schematic of one switch in figure 6.25 is present a OR gate, that represents the decoder network. The different switches has different selection input: S_0S_1, $\overline{S_0}S_1$, $S_0\overline{S_1}$ and $\overline{S_0S_1}$. To avoid that un-choose samples stay floating, the non-selected DUT is connected to a terminal V_{com}. The output is connected to input of cryogenic transimpedance.

For combinator network we use minimum transistor $0.4\mu m$ x $0.35\mu m$, while for switch we used a $10\mu m$ x 0.7μ Pmos and $10\mu m$ x $1.4\mu m$ Nmos to have

lower R_{dson}. Considering that the voltage of input terminal is about 0V, it's the bias on quantum dot $\pm 20mV$, results:

$$R = \frac{1}{1.5m\frac{A}{V^2}\frac{10\mu m}{1.4\mu m}(1.5V - 0.7V)} // \frac{1}{400\mu\frac{A}{V^2}\frac{10\mu m}{0.7\mu m}(1.5V - 1.3V)} = \\ = 116\Omega // 875\Omega = 100\Omega \tag{6.54}$$

in which for mobility we use the nearest extracted in table 3.2. With this designing the resistance is below the required value of 150Ω.

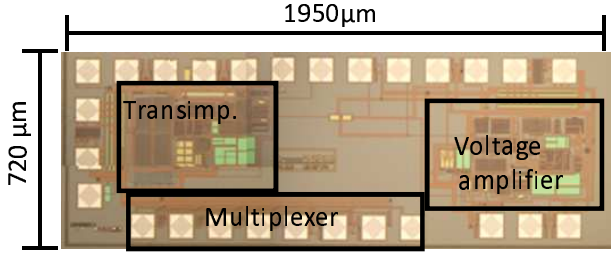

Figure 6.27: Photo of the cryogenic system, it is implemented in cmos technology $0.35\mu m$ 3.3V consuming only 1.5mA. Up to 4 different samples can be connected to allow multi-channel measurement, and changing the sample without extracting the cryogenic probe; it's able to drive the output wire thought the acquisition board at room temperature.

6.7 Experimental results

The photo of fully integrated cryogenic acquisition system is showed in figure 6.27. The entire chip occupy a $1.4mm^2$ is synthesized in cmos technology $0.35\mu m$ 3.3V; it has been tested and it consumes only 1.5mA on 3V supply so the power dissipated by the supply wires crossing the ^3He region $P = RI^2$ is reduced of a factor 11 (the supply current is reduced from 5mA to 1.5mA, according the equation 6.1). The schematic is present in figure 6.28, up to 4 different samples can be connected to the amplifier which, according to the gain of voltage amplifier, has two different equivalent transimpedance $8.6M\Omega$ and $77.4M\Omega$; so the gain can be higher respect to transimpedance describer in chapter 5.

In figure 6.29 there is the measured characteristic at 4 kelvin of the system, it shows a $8.15M\Omega$ slope, the small variation 5% is explicable considering the absolut dispertion of integrated resistors. The opamp showed a offset voltage of about 1mV which permit low bias measurement on quantum dot.

The most important improvement respect to system showed in chapter 5 is the increased bandwidth, in figure 6.30 there is the transfer function of

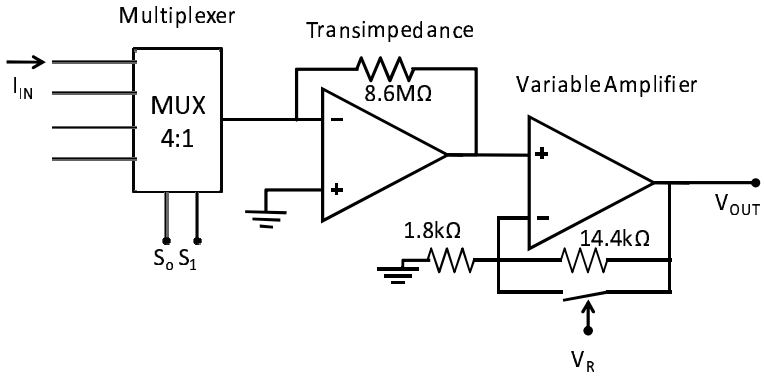

Figure 6.28: Schematic of whole acquisition system. The versatility of the system, his small dimension and his reduced power consumption make him the ideal instrument to be placed inside a cryostat for perform measurement on quantum dot.

cryogenic transimpedance we measure up to 100kHz of bandwidth. In figure 6.31 there is the measurement of input spectrum noise of transimpedance amplifier, a huge 1 over f noise is measured as predicted, by integrating the spectral noise over full bandwidth 100kHz we obtain a root mean square of $40pA_{RMS}$ allowing with high-resolution fast current measurement on quantum dot investigating the quantum computing applications.

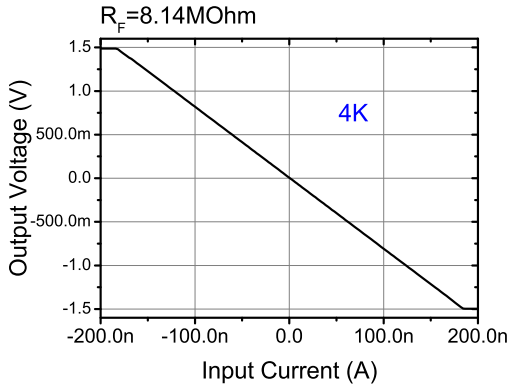

Figure 6.29: Measured characteristic of cryogenic transimpedance at 4 Kelvin, the slope is $8.15M\Omega$, the output voltage is rail to rail, and the current range is $\pm 200nA$

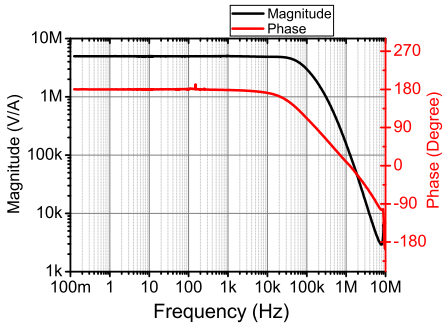

Figure 6.30: Transfer function of cryogenic transimpedance amplifier at 4K, we measure a -3dB bandwidth of about 100kHz correspondent to predicted results.

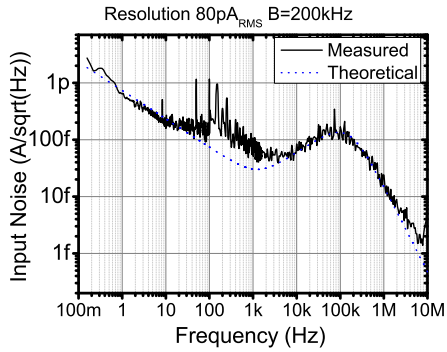

Figure 6.31: Input noise of transimpedance amplifier, on 100kHz bandwidth the root mean square noise is $40pA_{RMS}$.

6.8 Current Amplifier

The cryogenic system here designed has been measured from 4 Kelvin to 300 Kelvin and his functioning was measured (figure 6.33) this thanks to the constant gm circuit implemented and the all that tricks to permit a functioning in all temperature range, but as seen on figure 6.33 the slope of gain is changing because the feedback resistor changes his value from 4 Kelvin to 300 Kelvin. To overtake this behavior we developed a current amplifier (as already done in chapter 5) using a well coupled output resistor, like in figure 6.32. The output voltage of transimpedance amplifier is applied to a integrate resistance N times smaller than feedback resistor, in this way the output current is N time higher than input current. We use a current gain of 72 with a output resistor of $120k\Omega$; this output resistor is integrated in the same chip and we can assume that it is at the same temperature than the feedback resistor so the gain is no more dependent on first order to temperature but only on ratio of resistance. In figure 6.34 there is the measure of the characteristic of current amplifier.

We obtain a versatile, low-noise, low-power (4.5mW), small system able to detect current signal at 4 kelvin; it's the ideal instrument to be placed inside a cryostat to improve the performance respect room temperature system during the measurement on quantum dot for quantum computing.

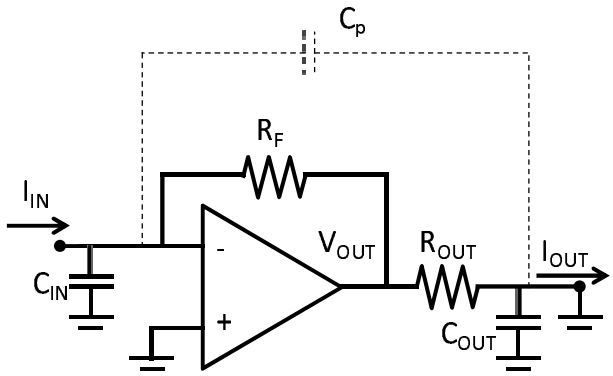

Figure 6.32: The cryogenic transimpedance amplifier used as current amplifier by adding a output resistor N times smaller than feedback resistor and reading the current flowing thought a external transimpedance, we obtain a current amplifier with gain N constant in temperature. The output capacitance should not be charged and discharges.

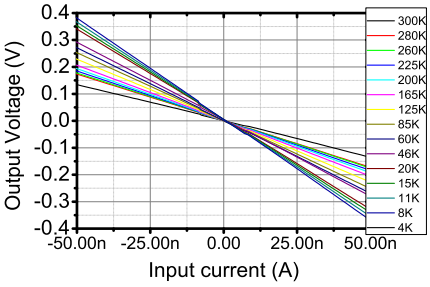

Figure 6.33: Characteristic of cryogenic integrated system from 4K to 300K. The amplification is ensured in all temperature range but the slope changes according to variation of value of feedback resistor from $8.6M\Omega$ to $3.58M\Omega$.

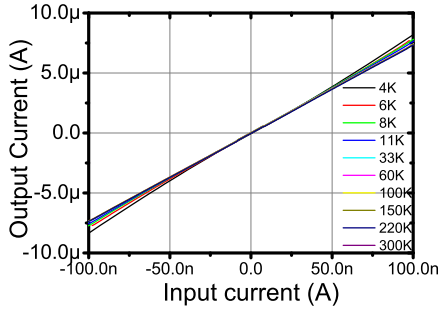

Figure 6.34: Characteristic of current amplifier from 4 Kelvin to 300Kelvin. The characteristic is more temperature independent with a current gain of 72. Small non-linear effect at high current are caused by cryogenic temperature effect on small resistance.

Conclusion

In this PhD thesis we develop several circuits for measurement on quantum dots for quantum computing. The main application is to use the spin of a trapped electron inside a quantum dot, as a bit in a conventional computer; enjoying the advantages to use a quantum magnitude [10]. The measurements are done by measuring the current flowing into or near a quantum dot thought a transimpedance amplifier which allow a perfect control of voltage on the device under test (DUT). First we described the design, realization and characterization of a complete system based on several transimpedance amplifier working at room temperature, each optimized for a particular measurement; they have resolution from 20fA to 1nA and bandwidth from 12Hz to 60kHz; there is also a low offset stage that allows measurements with voltage across quantum dot in $10\mu V$ range.

The performances of this room temperature system are limited by input parasitic capacitance due to the long wire which connect the sample to electronics. In fact to study the properties on quantum dot, without being affected by thermal effect, the sample has to be cooled at 300m Kelvin and placed in magnetic field up to 12T. These conditions were reached via a cryostat from cryogenics which permits a electrical control and sensing of the DUT only via wires of about 3-4 meters longitude. The parasitic capacitance associated with them is about 1nF and limit both the resolution and the bandwidth of transimpedance.

The only way to reduce the input capacitance is insert into cryostat the detection electronics by miniaturizing it in a integrated chip. But this circuits should be able to work to the temperature present inside the cryostat, in particular we identify a good amplifier holder at 20cm far from sample in which the temperature can reach up to 1 Kelvin. We choose a cmos technology from AMS $0.35\mu m$, as bipolar technology does not reach temperature below 80 Kelvin. The simulation models associated with technology does not are available for temperature below 250 Kelvin, so we proceeded with the characterization of the technology at liquid helium temperature 4 Kelvin. We characterize integrated resistors, their value almost double when going from

300 Kelvin to 4 Kelvin and they has a non linear effect if the width of them is below $10\mu m$. We tested also integrated capacitors which maintain almost the same value from 300 Kelvin up to 4 Kelvin.

Finally we tested also transistor, high conductive transistor does not work at 4 Kelvin due to freeze-out effects: a huge kink effect and hysteresis behavior [35] appear on mosfet's characteristic, making the devices unusable as transistor. On the other hand Pmos transistor with $W/L \leq 71$ and Nmos transistor with $W/L \leq 35$ still have a good transistor characteristic at 4 Kelvin. We extracted from them higher threshold voltages and also higher mobility respect room temperature; in Nmos at 4K still remains a small kink effect at high drain to source voltage. We notice that mobility and threshold voltages are different for different W/L. So it's not possible to extract mobility and threshold voltage valid for the technology at 4 Kelvin.

We developed a transimpedance amplifier, using a operational amplifier divided into two stages. A first stage at cryogenic temperature which is composed by only one transistor, so with a known mobility overtaking the geometry dependence. The second stage is a room temperature operation amplifier, it raises the dc gain of whole opamp. We use a cryogenic feedback resistor to enjoy the reduction of thermal noise. We measure a $1.3pA_{RMS}$ resolution over 10kHz bandwidth with a $150\mu W$ of power consumption at 4K. But the single transistor front-end have high offset voltage 1.3V which may be corrected but his variations may affect the measurement on quantum dots. To overtake this effect we design a whole integrated cryogenic transimpedance amplifier to reduce the input offset voltage. With a differential amplifier input stage the offset voltage can be reduced up to mV range. We decide to use only one Pmos $50\mu m$ x $0.7\mu m$ and one Nmos $50\mu m$ x $1.4\mu m$ and synthesizing a whole transimpedance amplifier by combine this two mosfet. In this way it is possible also to simulate the circuit at 4K, using a simple model and the parameter extracted during characterization.

The measurements confirm the simulated result, we realized a transimpedance amplifier which has a current resolution $2.8pA_{RMS}$ over 30kHz bandwidth; a voltage offset is 0.2mV which permit very low bias voltage measurements on quantum dot. The entire circuit is on a silicon chip with dimension $1200\mu m$ x $560\mu m$ and it's supplied on $\pm 1.5V$ with 5mA of supply current; this characteristic make him ideal devices to be attached inside the cryostat. It also does not require others special component at room temperature just voltage supply and acquisition system. The robust design has permitted to obtain a transimpedance working from 300K to 4K. The cryogenic transimpedance amplifier has also provided with a current output with current gain G=1000 independent from temperature, based on coupling between integrated resistors.

Finally we designed realized and tested a full cryogenic system with band-

width 100kHz and $40pA_{RMS}$ resolution, multi-channel variable gain, using a non-trivial opamp structure to improve the bandwidth without affecting the stability.

Our systems has been used in laboratory MDM IMM of the "Centro nazionale delle ricerche" a research institute in Italy for investigation on quantum dot for quantum computing.

Appendix A

Quantum mechanics

A.1 Computation

Let here resume some important concept on computation; in particular is important to clarify the meaning of *solve* a problem or equivalently compute a function. There are families of function that can be computed and families not [62]; in particular a function is defined computable if it can be simulated by a theoretical model called Turing machine [63].

In computation is not enough the computability of a function but also the *cost* of a function. Cost is can be expressed in terms of space, time or energy consumed to compute the function; very important is describe the trend of the cost when increasing the input size (n) in particular if the cost of a function is polynomial or exponential with n. As example the factorization of an integer is a problem whose cost is exponential with the number of the digit while search a data in a unordered database has polynomial trend. In computer science problems with exponential cost are considered intractable[1], in fact factorization of integer with some hundred of digit takes some millions years to be accomplished.

A.1.1 Probabilistic computer

Probabilistic computation use a different approach to solving a problem, and usually can comply tasks faster then deterministic computer, it introduces the concept of tolerable error and need the ability to generate random numbers. In next example we can see the improvement of probabilistic computation. There are N bit and only two cases are possible:

[1] Factorize an integer with two hundred of digit can take million of years with a modern computer

- The N bit are all equal (0 or 1)
- Half bit are 0 and half are 1

it occurs to distinguish between this two cases: with standard (or deterministic) computation we have to see $1 + N/2$ to solve the problem; instead with a probabilistic computer we see k random bit, if there are different values we can conclude that we are in second case if all the value are the same we conclude that we are in first case; of course in the second situation we might give the wrong answer, but the probability to mistake is [2] $1/2^k$ with k=100 the probability of a mistake is 10^{-30} so with a probabilistic computer it's possible to solve a problem with a finite but negligible error probability, note that k does not depend on N so the probability of error is the same for whatever number of input bit.

It's possible now to define of tractable problems as those problems solvable with a negligible probability of error in polynomial time.

A.2 Universal quantum gates

Now we define a universal quantum gate, one of the requirement for quantum computer (section 1.3.1):

Definition 1. *A set of quantum gates, $\boldsymbol{G}$, is called Universal if for any ϵ and any unitary matrix U on any number of bits, U can be implemented to within $\epsilon > 0$ by a sequence of gates from $\boldsymbol{G}$. In other word, the subgroups generated by $\boldsymbol{G}$ is dense in the group of unitary operators, U(n), for all n.*

A unitary matrix U is said to be approximated to within ϵ by a unitary matrix U' if $\left|U - U'\right| < \epsilon$. So with a Universal quantum set we can reasonably implement any unitary matrix of any number of bit by a succession of elementary gate. The first universal quantum set was introduced by Deutsch [64] but it works with 3 qubit gates, which seems very hard to control interactions between three particle, Di Vincenzo [19] discover that is possible to obtain a Universal quantum set with 2 qubit gates, and in a improvement [65] was proved an universal quantum gate set with a 2-qubit CNOT gate and some 1 qubit gate, that are feasible more easy to implement since involve only 1 particle and a CNOT gate has already been realized [66].

[2] It's equivalent to flip a coin k times and get the same symbol

A.3 Quantum algorithm

We continue presenting some algorithm that shows improvement of quantum computing respect to standard computing. The most famous is Shor's algorithm about factorization of integers, it has pulled up the research into quantum computation. The first quantum algorithm that combines interference and exponentiality achieving advantages respect classical algorithm is Deutsch and Jozsa [67] which resolved exactly the problem of constant and balanced bit presented in section A.1.1 with polynomial cost using the most powerful tool in quantum computing that is Fourier transform. The algorithm starts with a function f from 1,n to 0,1 and two register one with n qubit $|0^n\rangle$ and another register with only one qubit $|1\rangle$, we supposed that we have an oracle that compute f by the transformation:

$$|x\rangle|y\rangle \rightarrow |x\rangle|x \oplus f(x)\rangle \tag{A.1}$$

the oracle take two qubit and returns the first qubit and the XOR between its, the first qubit is also in output to make the function reversible. Then applying the Hadamard transformation (also called fuorier transform) to all qubit we obtain:

$$\frac{1}{\sqrt{2^{n+1}}} \sum_{x=0}^{2^n-1} |x\rangle \left(|0\rangle - |1\rangle\right) \tag{A.2}$$

Now calling the oracle (i.e. applying transformation A.1) we obtain:

$$\frac{1}{\sqrt{2^{n+1}}} \sum_{x=0}^{2^n-1} |x\rangle \left(|f(x)\rangle - |1 \oplus f(x)\rangle\right) \tag{A.3}$$

we know that f(x) is 0 or 1 in both cases the eq A.3 becomes:

$$\frac{1}{\sqrt{2^{n+1}}} \sum_{x=0}^{2^n-1} (-1)^{f(x)} |x\rangle \left(|0\rangle - |1\rangle\right) \tag{A.4}$$

Ignoring the last qubit and applying again the Hadamard transformation the result is:

$$\frac{1}{2^n} \sum_{x=0}^{2^n-1} (-1)^{f(x)} \sum_{y=0}^{2^n-1} (-1)^{x \cdot y} |y\rangle = \frac{1}{2^n} \sum_{y=0}^{2^n-1} \left[\sum_{x=0}^{2^n-1} (-1)^{f(x)} (-1)^{x \cdot y} \right] |y\rangle \tag{A.5}$$

The probability to measure $|0^n\rangle$:

$$\left| \frac{1}{2^n} \sum_{x=0}^{2^n-1} (-1)^{f(x)} \right|^2 \tag{A.6}$$

In case that f(x) is constant the probability to measure $|0^n\rangle$ is 1, otherwise is 0; this thanks to the constructive and destructive interference. This simply algorithm has showed how the interference and the exponential power has improved the solution of the problem in respect to standard computation.

A.3.1 Shor's algorithm

The most important algorithm for quantum computation is Shor's algorithm[8] for factorization of integer, it has a extremely importance because on assumption that factorization is not conventionally computable is based the RSA cryptography used in almost all internet sites where some security is needed; like banks sites, or web shopping site. After the publication of this algorithm there were an increased interest from scientist on quantum computing. RSA (described in appendix B) is based on the hardness to factorize an integer with some hundred of digit; the known algorithm for factorize integer has exponential cost[3]; Shor's algorithm permits the factorization with polynomial in log(N) cost, actually it's not about the factorization of integer but on a equivalent problem, find the order of one integer modulo N [1]. The order of an integer Y modulo N is defined as the minimum integer r that verifies the relationship $Y^r \equiv 1 mod N$ with Y and N integers coprimes. But find the order and factorize an integer are problem easily interchangeable. First than present Shor's algorithm we have to define the operator Fourier Transform over Z_Q:

$$|a\rangle \rightarrow \frac{1}{\sqrt{Q}} \sum_{b=0}^{Q-1} e^{2\pi i ab/Q} |b\rangle = |\Psi_{Q,a}\rangle \tag{A.7}$$

Suppose for simplicity $N = 2^n$, Shor's algorithm starts by taking two register one with q qubit; carrying a number from 0 to Q, ($Q = 2^q$) and the other with n qubit can carry numbers from 0 up to N-1 , where Q is an integer bigger than N:

$$|0^q\rangle \otimes |0^n\rangle \tag{A.8}$$

Apply Fourier transform on first register[4]:

$$\frac{1}{\sqrt{Q}} \sum_{l=0}^{Q-1} |l\rangle \otimes |0^n\rangle \tag{A.9}$$

[3]The fastest algorithm implemented is "General number field sieve" [68]

[4]$|0^q\rangle$ means that $q_0 = 1$ and $q_K = 0 \, \forall k \neq 0$

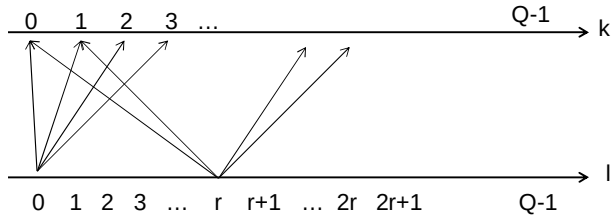

Figure A.1: For each value of k there are several possible values of l with periodicity r.

We now have all the possible state for the first register 0..Q-1 with the equal weight. Then we call a subroutine that computes $|l\rangle|d\rangle \rightarrow \left|d \oplus Y^l mod N\right\rangle$

$$\frac{1}{\sqrt{Q}} \sum_{l=0}^{Q-1} |l\rangle \otimes \left|Y^l mod N\right\rangle \tag{A.10}$$

with this step all the possible combination of Q of first register are divided into sets with period r, because $Y^l mod N = Y^{l+ir} mod N$ for every integer i. So combination of first register with distance r is cross multiplied for the same value. The next step is to measure the second register.

$$\frac{1}{\sqrt{A}} \sum_{l=0 \| Y^l = Y^{l_0}}^{Q-1} |l\rangle \otimes \left|Y^{l_0}\right\rangle = \frac{1}{\sqrt{A}} \sum_{j=0}^{A-1} |jr + l_0\rangle \otimes \left|Y^{l_0}\right\rangle \tag{A.11}$$

In this way we fixed the value of $Y^l mod N$ and the first register collapse into a superposition of l's with periodicity r but with arbitrary shift l_0. Now we have to measure the periodicity r; notice that is not possible to measure the first register twice or more to extract the periodicity because once measured the system fall in one classical status, we need to restart the algorithm but in this way also the result of the second register is in general different so we are not measuring the period of the same set of data with different l_0. To extract periodicity we applies again the Fourier Transform on the first register.

$$\frac{1}{\sqrt{Q}} \sum_{k=0}^{Q-1} \left(\frac{1}{\sqrt{A}} \sum_{j=0}^{A-1} e^{2\pi i (jr+l_0)k/Q} \right) |k\rangle \otimes \left|Y^{l_0}\right\rangle \tag{A.12}$$

Measuring of first register let k_1 to be the outcome, approximate k_1/Q by a fraction with denominator smaller than N, if the residual denominator doesn't satisfy $Y^d = 1 mod N$ throw it away, else call the denominator r_1; repeat all previous step poly(Log(N)) times to get r_1 r_2 .. and output the minimal r. To

understand this step let calculate the probability to measure a generic state $|k\rangle$ in the first register:

$$Prob(k) = \frac{1}{QA}\left|\sum_{j=0}^{Q-1} e^{2\pi ik(jr+l_0)/Q}\right|^2 = \left|\sum_{j=0}^{A-1} e^{2\pi ikrj/Q}\right|^2 \tag{A.13}$$

Suppose now that r is a divisor of Q, in this case the above geometrical series is 0 unless $e^{2\pi ikr/Q} = 1$ so we can only measure k that satisfy the relationship kr=mQ for some integer m, again the destructive interference comes into play deleting "'bad"' k's, so k/Q=m/r if this fraction is not reducible so m and r are coprime and we have found the denominator we are looking for otherwise we have to repeat the algorithm about Q/log(Q) times[5].

If r is not a perfect divisor of Q bad k's does'n not cancel out however his amplitude is very low respect to good k's so measuring bad k's is less probable. But another problem come in because now good k's does not satisfy kr=mQ we have to search approximations of this relationship:

$$-r/2 \leq krmodQ \leq r/2 \tag{A.14}$$

there are exactly r values of k that satisfy this requirement, because k run from 0 to Q-1, therefore kr runs from 0 to (Q-1)r. Now the probability to measure a good k is:

$$Prob(k) = \frac{1}{QA}\sum_{j=0}^{A-1}\left|e^{2\pi ikrj/Q}\right|^2 \approx \frac{4}{\pi^2 r} \tag{A.15}$$

in which we are assumed to be Q is bigger than N. Since there are r good k's the probability to measure a good k is $4/\pi^2$, once found k we can found r considering that:

$$\left|\frac{k}{Q} - \frac{m}{r}\right| \leq \frac{1}{2Q} \tag{A.16}$$

If Q is larger than N (about N^2) there are only one fraction m/r that satisfy the relationship A.14 and can be found by method of continued fractions. In this way we can find the order r and easily we can find the factorization of an integer [1]; which is the purpose of Shor's algorithm.

Entanglement

The entanglement is a strong coupling between different qubit, it happens when a state of one qubit is strictly dependent on the state of another qubit

[5]From the prime number theorem there are only n/log(n) numbers smaller than n and coprime with n.

for example consider the following quantum state:

$$\frac{1}{\sqrt{2}}\left(|000\rangle + |111\rangle\right) \tag{A.17}$$

in this case is we read the first qubit making collapse the wave-function; also the other qubit obtains a fixed values equal to the first although they may be far apart. Entanglement was firstly introduced by Schrodinger and the paradox EPR (Einstein Podolsky Rosen) is focused on it, is a fundamental step for obtaining a quantum computer but it's fragile and difficult to create, only pair of photons and atoms entangled were created [69] [70] but for quantum computation it's important to entangled many particles. Recently has been proposed the use of quantum computation without entanglement but with optical devices [71].

Entanglement is the most fascinating aspect of quantum physics and also a fundamental recipe of quantum computation, in shor's algorithm after call the oracle in eq. A.10 the two register are entangled because measuring the second register in eq. A.11 fix $Y^l mod N$ and in first register remains a superposition of only state indexed by an l that satisfy the relationship $Y^l mod N$.

Quantum Fourier transform

Quantum Fourier transform is the most powerful tool in quantum world and gives the exponential advantage in respect to standard algorithm. The classical discrete unitary fourier transform take a N complex vector $(x_0\ x_1 \cdots x_{N-1})$ and transforms it in another N vector $(y_0\ y_1 \cdots y_{N-1})$, similarly quantum Fourier transform of function f of a system of N qubit take the quantum state $|x\rangle$:

$$|x\rangle = \sum_{j=0}^{N-1} x_j |j\rangle \tag{A.18}$$

And change into quantum state $|y\rangle$ according to formula:

$$y_k = \frac{1}{\sqrt{N}} \sum_{j=0}^{N-1} x_j e^{jk\frac{2\pi i}{N}} \rightarrow |y\rangle = \sum_{k=0}^{N-1} y_k |k\rangle \tag{A.19}$$

The synthesis of quantum Fourier Transform (QFT) can be obtained with a Hadamantard gate and a shift phase gate [72] for this reason the quantum Fourier transform is also called Hadamantard transformation. In shor's algorithm Fourier transform is used first to randomize initial state and a second time to obtain information on period; the initial state is $|0^n\rangle$ it's a classical

state with all zero qubit, it's similarly to discrete delta only one sample is non-zero, the fourier transform of a discrete delta is a constant at all frequencies similar the quantum fourier transform of a classical state, in which only one coefficient is different from zero, is a constant so all possible states have the same probability to happen.

A.3.2 Quantum Errors

Obviously the quantum gate and operation are not error-less but we have also to consider that error may comes. In this paragraph we present the problem may come when using quantum computation; how to model the error and how to avoid a complete corruption of the elaboration.

Decoherence

A qubit in his physical synthesis will be a real devices with an environment that could affect his correct operation. In particular when interacting with his environment a qubit can loss his quantum characteristics this phenomenon is called decoherence [73], it destroy the quantum information in it; this may be due both to the external environment and to inaccuracy in quantum gates. Error operation like decoherence can be view as a unitary operator *environment* applied on the quantum system under certain assumption: no correlation between the noise processes and another assumption is that each qubit interact only with his environment and there are no interaction between these environments, we can view the total error operator over n qubit like a tensor product by single error operator each operating on a single qubit [74]:

$$\epsilon = \epsilon_1 \otimes \epsilon_2 \otimes \cdots \otimes \epsilon_n \tag{A.20}$$

is also possible define a density matrix of a state $|a\rangle$ as $\rho = |a\rangle\langle a|$, unitary operation on the environment and the system, which corresponds to quantum noise can be viewed as linear operator on the density matrix describing only the system. It's possible also to define an error rate η as the distance from the identity map on density matrix. The error rate can be viewed as the equivalent of the bit error rate (BER) in the quantum world.

A.3.3 Quantum error correction

In standard digital communication to avoid error while using a noisy channel is common to use redundancy by sending more bit in order to be able to identify and correct bit flip. For example sending three bit 111 instead one bit 1, permits not only to identify, but also to correct one bit error. We want to

do something similar in quantum computing we should think to sending the qubit $c_0|0\rangle + c_1|1\rangle$ by sending three qubit by the transformation:

$$c_0|0\rangle + c_1|1\rangle \rightarrow c_0|0\rangle + c_1|1\rangle \otimes c_0|0\rangle + c_1|1\rangle \otimes c_0|0\rangle + c_1|1\rangle \tag{A.21}$$

in this way we are able to take notice of the presence of an error. But transformation A.21 is not a linear operator so it's not possible to synthesize it. It's hard prevent error in quantum computation because information cannot be copied according to characteristic of quantum information presented in sez. 1.1; considering that coping involves measuring and coping lead to the collapse of the wave-function and the destroying of information, Concluding redundancy can not be used as tool for quantum computation.

Like standard computation [75], also in quantum computation is possible to implement a quantum error correction preventing that one error destroy the entire computation. Shor in 1995 was the first introducing the quantum error correction [8] his main intuition was to treat quantum noise as a discrete process; suppose we have n qubit with ϵ_i is the linear error operator on ith qubit and η is the error rate; we can write the final status $|a_F\rangle$ after a transmission from state $|a\rangle$ as:

$$\begin{aligned} |a_F\rangle &= \epsilon_1\epsilon_2\cdots\epsilon_n\,|a\rangle = (I_1 + \eta\epsilon_1^{'})(I_2 + \eta\epsilon_2^{'})\cdots(I_n + \eta\epsilon_n^{'})\,|a\rangle = \\ &= I_1 I_2\cdots I_n\,|a\rangle + \eta(\epsilon_1^{'} I_2\cdots I_n + \cdots + I_1 I_2\cdot\epsilon_n^{'})\,|a\rangle + \cdots + \\ &+ \eta^n(\epsilon_1^{'}\epsilon_2^{'}\cdots\epsilon_n^{'})\,|a\rangle \end{aligned} \tag{A.22}$$

For small η we can neglect higher order terms, this is the first step for quantization of quantum noise because in each term a qubit is either damaged and not; following the demonstration in [76] it's possible to conclude that everything that can happen to a qubit is the composition of 4 different operation, specifically the four matrix:

$$\chi = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}, \sigma_x = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}, \sigma_y = \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix}, \sigma_z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix} \tag{A.23}$$

the basic idea is to measure which one of the previous operator took part and then apply it's reverse operation to recover the correct information. σ_x is a bit flip, so classical recovering procedure can be used, σ_z is a phase flip but in the Fourier transform correspond to a bit flip. So with this assumption we can use classical techniques for a quantum transmission [77] in this way: we have n qubit to send, and we encode the information associated with they in k qubit by adding some ancilla qubit that are error tolerant during transmission, once received the k qubit we measure the ancilla qubit to know which error happens and correct it to decode the n qubit although if during the transmission

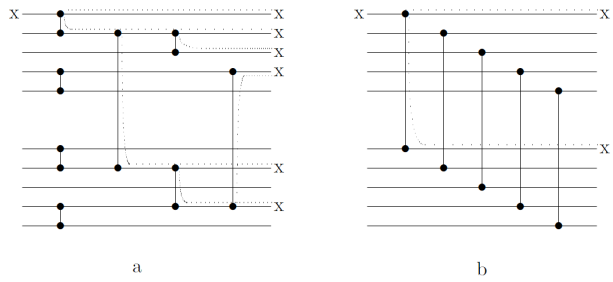

Figure A.2: Graph of quantum gates of a encoded state quantum computation: a) propagate one error on 6 qubit in b) only 2 qubit are affected by one error

some error happens. It is important to underline that also the encoding may introduce disturbs and also we should avoid that error propagate before being canceled because only a small number of error can be corrected sometimes just 1 error can be tolerated if more than one error happens the communication is total unusable. When computing the encoded states also the gates must be modified to work with encoded states they has to work with more qubit and apply the correction procedure; but most important since quantum gate work with interaction between qubit they has to avoid propagation of error.

Quantum gates has to be designed in order to avoid that one error will propagate on several qubit because only few error at once can be corrected by quantum error correction often 1, in A.2 there are two quantum gate working on 10 qubit; in case a) one qubit error it's propagated into 5 qubit while in case b) only two qubit are involved in the mistake and may be possible a successive correcting procedure.

Let now calculate the effective noise rate η_e, so the noise rate in presence of correcting procedures. If A is the places where error can occur, d is the maximum error tolerable at once and η is the error rate on uncorrected qubit; the effective error rate results:

$$\eta_e = \binom{A}{d+1}\eta^{d+1} \tag{A.24}$$

of course for a reliable quantum circuit $\eta \geq \eta_r$ otherwise correction is not convenient, can be defined a threshold error rate η_c:

$$\binom{A}{d+1}\eta_c^{d+1} = \eta_c \rightarrow \eta_c = \sqrt[d]{\frac{1}{\binom{A}{d+1}}} \tag{A.25}$$

In the error rate of a quantum gate is below the threshold; a error correction is possible. Up today [78] the threshold error rate has reach 3%. So decoherence and imprecision are no longer considered insurmountable obstacles to realizing

a quantum computing althought many problems today remains for a usable and convenient quantum computer [79]. In May 2011 D-wave system annonces to have build the first commercial quantum computer with 128 qubit; with a price is 10 million $, if the result confirmed this would be the first commecial quantum computer being a fundamental step for the next future.

Appendix B

RSA Trasmission protocol

The RSA protocol is an asymmetric transmission protocol. It is based on a private and public key; private keys are never been transmitted; while public keys are transmitted. Alice and Bob wants to communicate while somebody can read theirs message. The protocol is the following, Bob chose two very large prime integers P and Q and multiply it $N = P \cdot Q$ he also chose a integer E that is coprime with $(P-1) \cdot (Q-1)$ and he compute $D = E^{-}1mod(P-1)(Q-1)$. E and N are the public keys. Bob sends E and N to Alice; She take his message M and computes $M^E modN$, Bob once receive the message from Alice computes $\left(M^E modN\right)^D$ in order to recover the message from alice, if someone intercept the entire communication can not recover the message without the information on P and Q. With N and E it's possible to codify a message buy not to decodify. Usually the communication with RSA is used to safety communicate a shared key for symmetric communication that is more simple. The security of this cryptosystem rest on the difficulty to factoring large numbers; in fact P and Q are the only two prime factor of N. Integer with 130 digit are been factorized in a few weeks, as the only know classical algorithm has exponential cost, so time for elaboration is exponential with the number of the input digit, doubling the number of digit the time needed for the processing goes up to million years. So Alice and Bob are practically secure against classical eavesdroppers.

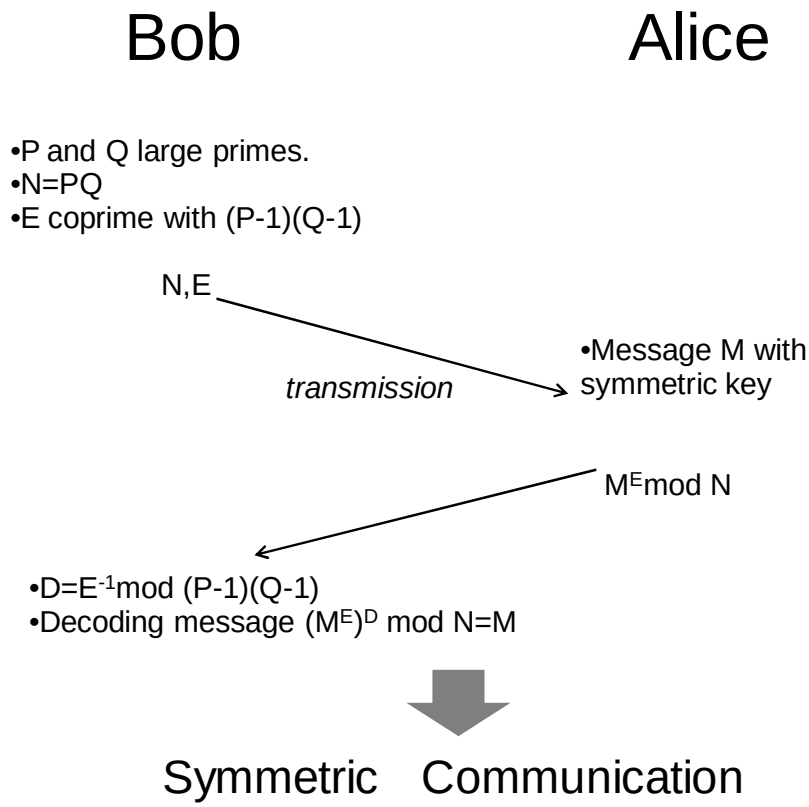

Figure B.1: Transmission protocol RSA

Appendix C

Quantum confinement

In a semiconductor device the energy permitted for electron depends on the eigenvalue of wavefunction of the electron.

C.1 Bulk semiconductor

In a Bulk semiconductor the distribution of energy level can be calculated by Schrodinger equation:

$$-\frac{\hbar}{2m}\frac{d^2\varphi}{dx^2} - U(x)\varphi = E\varphi \tag{C.1}$$

Applying Schodinger equation on a periodic potential of a lattice can be obtain a relationship between the energy E and the momentum k:

$$E(k) = \frac{\hbar k^2}{2m^*} \tag{C.2}$$

In a semiconductor electrons can not have the same quantum number, and for a cube with side L, two possible k are separated by $2\pi/L$. The density of states in k in a bulk semiconductor can be calculated by taking a sphere of radius **k** and starting counting the states by calculating how many cube of edge $2\pi/L$ there are in it by the ratio of their volumes:

$$N(k) = 2\frac{\frac{4}{3}\pi k^3}{\left(\frac{2\pi}{L}\right)^3} \tag{C.3}$$

Then it's possible to calculate the density of state dividing N by the volume V ($V = L^3$) and differentiating respect k:

$$g(k) = \frac{d\frac{N(k)}{V}}{dk} = \frac{d\frac{k^3}{3\pi^2}}{dk} = \frac{k^2}{\pi^2} \tag{C.4}$$

We can also obtain the relationship between energy and k by differentiating eq. C.2:

$$E(k) = \frac{\hbar k^2}{2m^*} \rightarrow \frac{dk}{dE} = \frac{m^*}{\hbar^2 k} \tag{C.5}$$

and finally substituing eq. C.5 into eq. C.4:

$$g_{3D}(E) = g(k)\frac{dk}{dE} = \frac{\sqrt{2}(m)^{\frac{3}{2}}}{\pi^2\hbar^3}\sqrt{E} \tag{C.6}$$

This is the

C.2 Quantum well and quantum wire

Quantum well are system in with one dimension are smaller that longitude of electron wave-function so no longer sphere has to be counted but a circle. The number of state in a circle with radius k is the ratio of the area of the circle and the area of the squares with edge $2\pi/k$:

$$N(k) = 2\frac{\pi k^2}{\left(\frac{2\pi}{L}\right)^2} \rightarrow g(k) = \frac{d\frac{N(k)}{L^2}}{dk} = \frac{d\frac{k^2}{2\pi}}{dk} = \frac{k}{\pi} \tag{C.7}$$

and substituing the parabolic dispersion (eq.C.2) we obtain:

$$g_{2D}(E) = g(k)\frac{dk}{dE} = \frac{m^*}{\pi\hbar^2} \tag{C.8}$$

So the density of state is energy independent but this relationship is valid for each energy level in the confinemente direction E_n so the density of state becomes:

$$g_{2D}(E) = \sum_n \frac{m^*}{\pi\hbar^2} H(E - E_n) \tag{C.9}$$

If a system is confined in two dimension is called quantum wire; following the same procedures on a wire long K e counting the segment $2\pi/L$ it's possible to find the density of state for a single energy in confined directions E_n:

$$g_{1D}(E) = \frac{\sqrt{2m^*}}{\pi\hbar}\frac{1}{\sqrt{E}} \tag{C.10}$$

For quantum dots the wavefunction is confined in all three dimension, it has discrete levels in which the spacing is inversely proportional to dimension of dot.

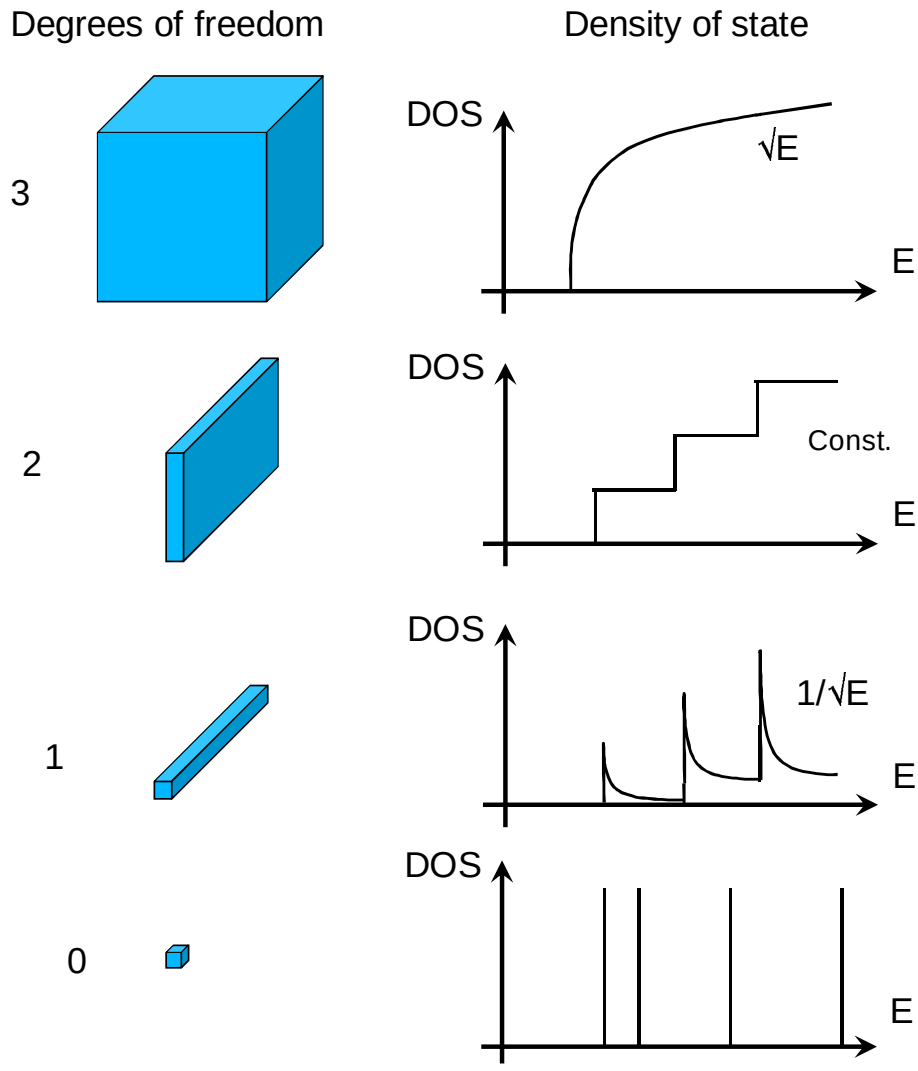

Figure C.1: Density of state for bulk, quantum well, quantum wire and quantum dot.

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