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Modeling and Fabrication of Electret-based 2D Micro Energy Harvester

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Preface

This Master's Thesis has been written in order to complete a M.Sc. program in Physics Engineering at Politecnico di Milano, Italy. The whole process has been supervised by Dr. Roman Sordan, head of the Nanoscale Device Group at L-NESS, Como, Italy
The backbone for this report has been an eight-month research stay (October 2011 - May 2012) at the Department of Micro- and Nanotechnology, Technical University of Denmark (DTU). I joined a pre-existing project (started in July 2010) on electret-based energy harvesting in the Silicon Microtechnology research group. The responsible scientist for the project, as well as my guide and supervisor, has been Assistant Professor Fei Wang.
Work has been carried out at the Nanotech Department (modeling, design, and project management), in the Danchip cleanroom (fabrication), and in the MEMS Laboratory (testing). All aforementioned facilities are located on DTU campus.
There are many people who deserve credit for their support within this project. They will be acknowledged at the end of this report.

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Contents

Abstract

A prototype micro energy harvester is designed, fabricated, and tested, with the goal of generating electrical power from two perpendicular ambient vibration components. Target vibration sources are typical machinery vibrations with low acceleration (0.01-0.5 g) and frequency in the 100-500 Hz range.

The device includes a suspended proof mass, which is excited at its resonance frequency by the vibration source. The transduction mechanism is induction charge flow between capacitor plates having a time-varying overlap due to proof mass oscillation. A permanent charge bias for electrostatic induction is provided by polymer electrets. The electret material is CYTOP©, which is patterned by Reactive Ion Etching and charged quasi-permanently up to $-3.5 \times 10^{-4}\,\mathrm{C/m^2}$ with a corona setup. CYTOP is also employed as an adhesive material for full wafer bonding processes.

The harvester is fully packaged into a $1.1 \times 1.0 \times 0.15$ cm chip fabricated with MEMS-compatible wafer-level processes exclusively. As a result, device embedding into complex microsystems can be envisioned. Powering of wireless sensor network (WSN) nodes is one of the most promising applications.

A new hybrid analytical/numerical model is proposed that describes the physics of the harvesting process and accurately predicts the device's operation performance. With the current device design, a maximum RMS power of 32.5 nW is achieved with a load of 17 MΩ, a source vibration frequency of 179 Hz, and a source acceleration amplitude of 0.03 g.

The model suggests that power outputs as high as 90 μW might be obtained by further optimization of device parameters and advances in a few key fabrication processes. Such performance level would render our energy harvester highly attractive for future applications.

Riassunto

Nel presente lavoro si discute di un nuovo tipo di *micro energy harvester* progettato, fabbricato e testato nel corso di questa tesi. Lo scopo del dispositivo è ottenere potenza elettrica da sorgenti di potenza meccanica di tipo vibrazionale presenti nell'ambiente. Possibili sorgenti di simili oscillazioni sono macchinari industriali o casalinghi che spesso presentano uno spettro vibrazionale con picchi nella regione tra i 100 e i 500 Hz, caratterizzati da ampiezza sotto il μm e bassa accelerazione (0.01-0.5 g).

Il dispositivo comprende una massa inerziale collegata tramite molle a un sistema di riferimento solidale con la sorgente vibrante: il sistema deve essere progettato in modo tale da ottenere una frequenza di risonanza coincidente con uno dei picchi dello spettro vibrazionale della sorgente. Il meccanismo di trasduzione è il flusso della carica indotta elettrostaticamente su diversi condensatori. La carica si sposta da un condensatore a un altro poichè l'overlap tra le loro armature dipende dal tempo a causa dell'oscillazione della massa inerziale. Elettreti polimerici sono inclusi nel dispositivo per fornire una carica di bias che garantisce l'induzione elettrostatica. Il polimero usato è il CYTOP©, che sarà modellato da un processo di Reactive Ion Etching e caricato quasi-permanentemente fino a $-3.5 \times 10^{-4}\,\mathrm{C/m^2}$ da una scarica corona in condizioni controllate. Il CYTOP sarà anche usato come materiale adesivo in processi di wafer bonding.

L'energy harvester è racchiuso in un chip di dimensioni $1.1 \times 1.0 \times 0.15$ cm, interamente costruito con tecniche di microfabbricazione standard per i microsistemi elettromeccanici (MEMS). Si può dunque pensare di integrare il dispositivo in esame in microsistemi di elevata complessità. L'applicazione più naturale è la fornitura di energia a sensori a basso consumo connessi alla nascente tecnologia dei wireless sensor network (WSN). Se un energy harvester potesse essere integrato in ciascun nodo del network e fornisse potenza sufficiente a tutti gli elementi del nodo, le batterie potrebbero essere eliminate e non sarebbe richiesto alcun intervento di manutenzione elettrica.

Si propone inoltre un nuovo modello, in parte analitico in parte numerico, per descrivere la fisica dell'energy harvester e del processo di conversione. Si mostrerà che il modello è in grado di prevedere accuratamente il comportamento del dispositivo. Con il design e i parametri implementati in questa tesi, si raggiungerà una potenza massima (RMS) di 32.5 nW con un carico di 17 MΩ e una sorgente vibrante a 179 Hz con un'accelerazione di ampiezza 0.03 g.

Il modello suggerisce che potenze di output oltre i 90 μW possono essere ottenute ottimizzando i parametri geometrici del dispositivo e raggiungendo un maggiore controllo di alcuni processi chiave nella fabbricazione. Un simile risultato renderebbe questo energy harvester molto promettente per future applicazioni.

Chapter 1

Introduction

1.1 Wireless Sensor Networks

A dense network of intercommunicating centimeter-sized wireless computers able to measure almost any quantity in the surrounding environment is starting to populate our world [1]. *Wireless sensor networks* (WSN) allow to ubiquitously monitor movement, pressure, temperature, pollution, location of persons, structural health of mechanical elements, and even human health. Radio-frequency (RF) wireless communication between sensor nodes allows them to be deployed in previously unaccessible places at only 1 to 10 meters from each other, which would be very costly for a wired system [2]. Each of these microsystems typically comprises: [3]

- one or more microsensors to physically interface with the environment
- an RF receiver and transmitter to exchange data with neighboring nodes
- a computational unit (microprocessor) to process sensor data and manage send/receive operations
- a device that supplies power to all these components
- an electric circuit to appropriately connect the various elements together

The standard way to power sensor nodes is through conventional batteries. Despite recent advances in low-power electronics resulting in a trend of ever-decreasing power requirements for both analog and digital circuits [4], the lifetime of a state-of-the-art non-rechargeable lithium battery for an typical sensor node is still less than one year [2]. Replacing billions of batteries on a regular basis is not feasible and impairs WSN technology from reaching its full potential. Additionally, sensor nodes often need to be placed in remote areas where maintenance is virtually impossible. For these reasons, there is a strong ongoing research effort focused both on prolonging battery lifetime and on experimenting new power sources with the ultimate goal of making future sensor nodes self-sustainable over their whole lifetime.
Energy may be provided by two main kinds of devices. *Energy reservoirs* (such as batteries, fuel cells, and micro heat engines) feature a pre-defined amount of stored energy: therefore the power they are able to provide decreases as the expected lifetime of the node increases. On the other hand *energy harvesters* are much like power plants, as they feature a transducer that instantaneously turns a form of ambient power into electrical power. If the ambient energy source is steadily available, the power supplied by such a device is not limited by the node's lifetime but solely by failure of its own components.

1.2 Overview of Micro Energy Harvesting

A *micro energy harvester* (also called *micro energy scavenger* or simply *micro generator* in the literature) is a device with features in the micro scale designed to "harvest" a specific form of energy from the surrounding environment and make it available to another appliance in the form of instantaneous electrical power. The collected power signal can be conditioned if necessary and either be used immediately to power the target device or be transferred into a separate energy accumulator. Depending on the selected energy source, the transduction mechanism into the electrical domain will vary. Table 1.1 gives a brief overview of energy harvesting technology as of today. Physical effects exploited for transduction, energy availability, state-of-the-art output powers, and limitations are listed.

Power requirements for WSN applications may vary to a great amount, but in general a higher power is needed for sensors with a higher signal rate of change. The amount of data transmitted by the RF apparatus also affects how much power needs to be harvested for correct functioning of the sensor node. The low power range is pW to nW for devices that only need to perform a few measurements per day or during their entire lifetime. A more common situation with frequent sampling would probably lead to power requirements of the order of μW or mW [11].

It is especially convenient to fabricate energy harvesters with MEMS fabrication techniques, as the device to be powered is likely to be manufactured with IC/MEMS processes as well. This allows for greater compatibility and easier integration of both elements (and related electrical circuits) on the same chip. Integration can be *monolithic*, i.e. with all components fabricated

Table 1.1: Energy harvesting techniques

Energy type	Transduction	Sources	State of the art	Limiting factors
Thermal	thermoelectric effect	body heat, waste heat (from plants, machinery, lamps), daily temperature change	$260\,\mu W/cm^3$ with a 15°C gradient; $2200\,\mu W/cm^3$ with a 35°C gradient [5]	temperature gradients, Carnot efficiency
Light	photovoltaic effect	sunlight, artificial light	$8000\,\mu W/cm^3$ (full sunlight); $4\,\mu W/cm^3$ (office lighting) [2, 6]	cloudy days, solar cell efficiency (15-20%), artificial source distance
Radio-Frequency	receiving antenna	mobile phones, Wi-Fi routers, laptops, television/ radio broadcast stations, mobile base stations	1000-5000 μW (at 1m from a 3W transmitter); 10-100 μW (at 10m) [7]	governmental regulations, transmitter's distance and emitted power, RF to DC conversion efficiency
Vibrational	electrostatic induction, electromagnetic induction, piezoelectric effect	building walls/floors, engines, bridges, vehicles, industrial machinery, kitchen/laundry equipment, human motion	$175\,\mu W/cm^3$ at 20 Hz (electrostatic, [8]), $210\,\mu W/cm^3$ at 322 Hz (electromagnetic, [9]); $375\,\mu W/cm^3$ at 120 Hz (piezoelectric, [10])	source acceleration, vibration direction, frequency matching, intermittent vibration

on the same substrate, or different elements can be manufactured separately and then packaged together with assembling techniques [12].

Five serious issues need to be considered for most kinds of energy harvesters:

1. the size of the harvester must be kept under a certain threshold in order to be efficiently embedded into centimeter-sized microsystems. Above a size of 1cm^3, the harvester would most likely dominate the system volume.

2. scavenged power under realistic environmental conditions must be high enough for its target application requirements. Since there are stringent requirements both on output power and size, a figure of merit for a generic harvester is volume power density, measured in $[\mu\text{W/cm}^3]$. This quantity has already been used in Table 1.1 to evaluate state-of-the-art harvesters. A target value that could suit a variety of applications is $100\,\mu\text{W/cm}^3$ [2].

3. parameters such as optimal load, signal frequency, voltage, and current must have reasonable values or it will be hard to make the harvested power available in the form needed by the target device.

4. if a predictable amount of energy is to be harvested per unit time, the ambient source should provide energy steadily or at least in a predictable way. Unpredictable sources make harvester design and optimization extremely difficult.

5. in general, none of the proposed harvesting techniques has a high degree of versatility. They all require environmental conditions that are quite peculiar, so every potential application must be evaluated separately and the harvester itself should be tuned each time to maximize power transfer from the available power source.

1.3 Vibrational Harvesting and Introduction to our Device

In vibrational energy harvesting a variety of acceleration sources and transduction mechanisms can be potentially employed in order to transform some mechanical power due to source vibration into usable electrical energy. A first distinction can be made between a *steady* and an *impulsive* vibration source. The former can be roughly approximated to a harmonic oscillator at constant amplitude and constant frequency, corresponding to a peak of the source's vibration spectrum (see Figure 1.1). Typical examples are machinery casings and human or animal bodies during regular motion, such as walking or running. The latter is characterized by acceleration impulses of a relatively large magnitude with a fast decay. It could be a slamming door, or tree branches being displaced due to air moved by a nearby car. We will not consider this kind of vibration source in our analysis.

Steady vibration sources can be further split into *human-based* and *machinery-based*: it is found that human body motion typically features large displacement amplitudes (a few mm) and low frequencies (a few Hz). On the other hand, machinery vibration shows lower displacement amplitudes (from nm to μm) and higher frequencies (50-500 Hz) but similar accelerations (0.01-1 g) [2]. Figure 1.1 shows measured vibration spectra of two sample machines. It is evident that machinery vibrations occur within a large bandwidth. Both spectra show relatively narrow amplitude peaks at a number of frequencies, suggesting that a resonant system could be devised in order to exploit the larger accelerations available at a few well-defined frequencies.

Machinery-based vibrations are chosen as the application target for the harvester proposed in this work. We will adopt an *inertial* mechanical system as the one shown in Figure 1.2. An inertial mass (or *proof mass*) is suspended to a fixed frame structure through a spring system. Source acceleration induces proof mass motion with respect to the frames. If the resonance

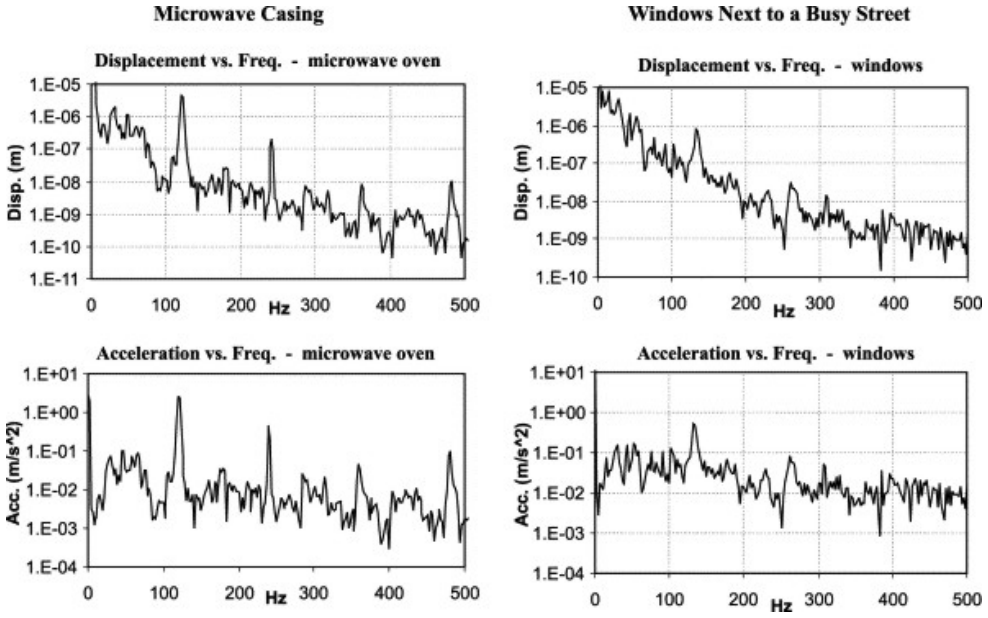


Figure 1.1: Displacement and acceleration amplitude spectra for the casing of a microwave oven and the base of a milling machine, measured with a piezoelectric accelerometer. Taken from [2].

frequency of the proof mass is tuned to match one of the amplitude peaks in the source's vibrational spectrum, a *resonant* generator is achieved. The advantage of a resonant system is that, if the frequency is tuned correctly, a small source acceleration is sufficient to drive the proof mass to large oscillation amplitudes provided that its mechanical q-factor is not too low (see Section 2.4.1). Figure 1.2 shows that our design allows for easy proof mass oscillation along two perpendicular components. As will be shown in Chapter 2 and Figure 3.3, the device's electrical domain is also designed to allow for similar harvesting performance regardless of which of the two normal directions is excited. The idea behind 2D energy harvesting is that the acceleration direction of the source is often unknown, so a two-dimensional design increases the chance of the

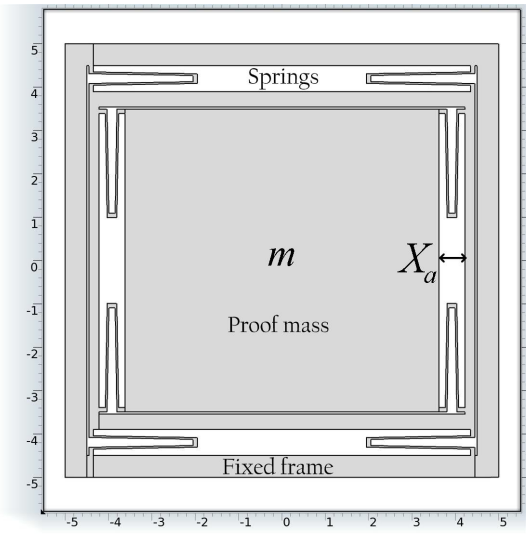


Figure 1.2: Top side view of our harvester's mechanical domain. m is the proof mass, X_a is the maximum proof mass oscillation amplitude allowed by the spring system. The proof mass can vibrate in two perpendicular directions.

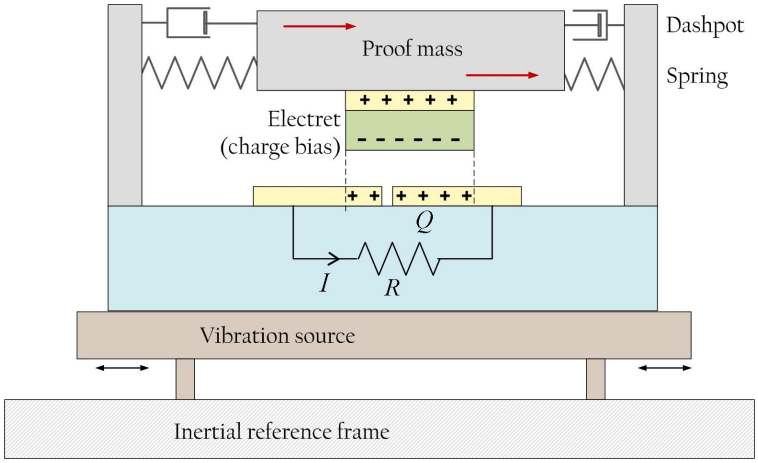


Figure 1.3: Simplified side view of our harvester during operation. Only three metal plates have been drawn for simplicity.

proof mass picking up vibrations coming from random directions. Three kinds of transduction mechanisms have been consistently employed in past resonant microgenerators:

- *piezoelectric* [10]: a flexible suspension, such as a cantilever beam, is fabricated with a piezoelectric material or at least coated with it. When it is mechanically stressed by an external vibration matching its resonance frequency, it generates charge cyclically due to the piezoelectric effect. The resulting current is led through a load resistance in order to obtain power .

- *electromagnetic* [9]: a few permanent magnets, mounted on a resonating cantilever beam, move with respect to a fixed coil. Because of the relative motion between a magnetic flux gradient and a conductor, a current is induced in the coil following Faraday's law, and it can be harvested by an external load.

- *electrostatic* [21]: With reference to Figure 1.3, a permanent charge or voltage bias is placed between two sets of capacitor plates in order to permanently induce charge on them. One set is fixed, while the other is situated on the moveable proof mass. When the mass vibrates, induction charges move periodically between connected capacitor plates due to capacitance changes related to a time-varying pattern overlap or to a time-varying gap. If a resistive load is connected between the plates where charge exchange occurs, it means that a power $P = RI^2 = R\,(dQ/dt)^2$ is harvested, where Q is the total induced charge on the connected plates.

One problem about electrostatic harvesters is that they need an extra input voltage or charge in order to generate electric fields between the capacitor plates and thus induce charge on them. A practical solution is found by using *electrets*, i.e. dielectric materials with exceptional charge retention properties (see Section 2.1). Electrets can be patterned on top of one set of capacitor plates and charged with an appropriate technique as shown in Figure 1.3. In an ideal situation, only a negligible charge decay should be observed until months or years after the charging process (see [11] and also Figure 2.1 for a partial demonstration).

1.4 Thesis Outline

This thesis will describe the application of the electrostatic harvesting principle on a real device design, and will discuss its predicted and experimental performance.

Chapter 2 lays the theoretical base for understanding basic physics of electrets and of the electret charging process. A model for device operation is then proposed by following a successive approximation procedure that adds further refinement and corrections at each step, eventually leading to a nonlinear coupled electromechanical model with the inclusion of a FEM result.

Chapter 3 presents the actual device microfabrication step by step. Challenging processes are highlighted and discussed in detail, while constant reference is made to design choices and to how they compare to fabrication results.

Chapter 4 describes the test setup used for characterization of the device output power and reports the few test results available. The level of agreement with the model of Chapter 2 is discussed, and a few unknown parameters are extrapolated from experimental results using the model.

Finally, Chapter 5 analyzes the results obtained in the different chapters and provides suggestions for future improvement in the next fabrication batches.

Chapter 2

Theory and Modeling

This chapter provides a modeling framework for the device proposed in the previous chapter. Section 2.1 presents basic properties of electrets. Types of stored charges, self-produced fields, charging methods, and charge decay mechanisms are briefly discussed, focusing on the material and techniques actually employed in this project. Section 2.2 gives theoretical background for electret charging using a corona setup and subsequent charge density measurement. Section 2.3 proposes a new electrical model of operation that applies to our harvester. In Section 2.4 a well-established model for inertial forced harmonic motion is shown. Finally, Section 2.5 couples the electrical and mechanical equations to find a general solution for proof mass motion and harvested power under a known source oscillation. A FEM study is also included to describe the effect of fringing fields on the device.

2.1 Properties of Polymer Electrets

An *electret* is a piece of dielectric material able to retain electrical charge *quasi-permanently*, i.e. the characteristic time constant for charge decay is much longer than the duration of the performed studies. If there is a non-zero net charge or if charges do not compensate everywhere in the material, Gauss's law states that an isolated electret produces a *constant external electric field*, which is also quasi-permanent (see Figure 2.1). Hence, charges can be induced on a conductive surface nearby according to the laws of electrostatics. This will be discussed in detail in Sections 2.2 and 2.3 for our specific device. In the following, a rectangular geometry as the one in Figure 2.2 will be assumed.

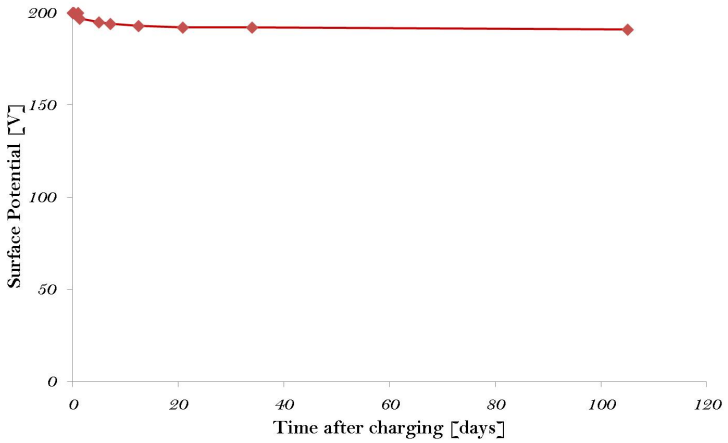


Figure 2.1: Experimental time decay of surface potential due to quasi-permanent surface charges on unpatterned 10μm-thick polymer electret film

Many types of dielectric materials can be employed as electrets. Examples are microfabrication-friendly dielectrics like silicon dioxide or silicon nitride, and amorphous polymers such as Teflon. They are typically in thin-film form, with thickness in the $1 - 100\mu$m range. A feature of amorphous polymers is a change in physical properties around a characteristic *glass transition temperature* T_G. Above this temperature, the material turns from a brittle state into a rubber-like viscous state with a smooth step in its thermal expansion coefficient, specific heat and viscosity. This is caused by thermal energy being high enough to allow for significant sliding of the polymer's molecular chains [13]. Stored electrical charge can be of various nature (see Figure 2.2):

- *molecular polarization charges*: in the absence of an electric field, intrinsic electric dipoles present in polar molecules are randomly oriented because of the uniform angular distribution of thermal forces. If an external field is applied, a torque acts on the dipoles to align them to the electric field against the thermal drifts. As a consequence, a polar material shows an average polarization in the field direction. Permanent polarization in polymer electrets can be achieved by *thermal poling*. Because there is a characteristic dipolar activation energy, a field is applied to create a net polarization at a temperature high enough to allow for easy dipole orientation. Then the field is kept constant while the sample is cooled below its glass transition temperature, where thermal energy is far below the dipolar activation energy. As a result, the polarization is frozen and it shows a slow thermal decay with a dipole relaxation frequency that decreases with decreasing temperature [14, 15].

- *real charges*: positive or negative carriers are implanted in some parts of the material without discharging. According to their space distribution, they can be described as a

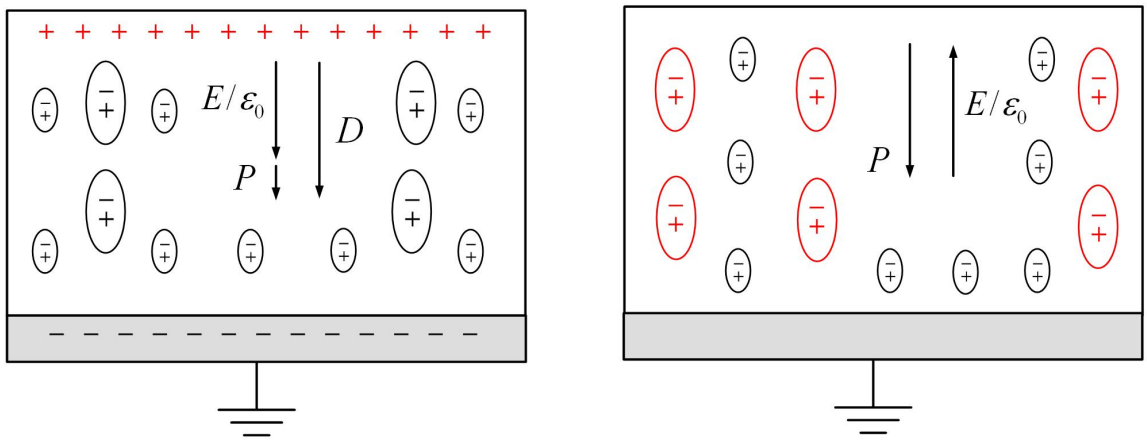


Figure 2.2: Self-fields on one-side metallized rectangular electrets. Quasi-permanent charges produced by charging techniques are drawn in red. Large and small dipoles represent molecular and atomic dipoles respectively. 2.2(a): uniform real surface charge layer. $\hat{\mathbf{E}} \neq 0$ outside the electret because of its net charge, so counter charge is induced on the metal. 2.2(b): frozen uniform polarization charges. Because of charge balance, $\hat{\mathbf{E}} = 0$ outside the electret and the metal has no induced charge

net surface or volume charge density, or as a combination of the two. Charges can be injected or deposited by contact electrification, discharges or electron/ion beams. Another technique is to generate carriers in the dielectric by radiation or heat while simultaneously separating them with an electric field. It should be remembered that, if the material is polar, the self-field given by a permanent real charge distribution will also induce a molecular polarization. Real charges are typically trapped in surface or bulk levels located in the energy gap between the valence and conduction band [14]. Their decay is associated to internal and external processes. *Internal* phenomena include ohmic conduction (from the few thermally activated intrinsic carriers) and real charge drift: electrons and holes that overcome the energy barrier between the valence and conduction band are accelerated by the internal field. The effect increases with temperature because of higher average thermal energy in carrier. Real charge diffusion involves motion of stored charges in the direction of their concentration gradient, but it usually plays a minor role. *External* processes are due to electric fields extending outside the electret and compensation charges being attracted to the electret surface in the form of atmospheric ions or polar particles.

- *electronic polarization charges*: It is important to note that non-polar materials can still be polarized by the electric field produced by their own real charge distributions, but this does not happen at a molecular level. Instead, it is a field-induced polarization due to the orientation of all *atomic* dipoles in the dielectric (consisting of nuclei and tightly-bound electrons) along the internal field direction. This type of polarization is present in all dielectrics and it is the reason why the relative permittivity ε_r is always strictly greater than 1, even in non-polar materials.

Inside an electret of any shape the general expression for the electric displacement is:

$$\hat{\mathbf{D}} = \varepsilon_0 \hat{\mathbf{E}} + \hat{\mathbf{P}}_{perm} + \hat{\mathbf{P}}_{ind} \tag{2.1}$$

where $\hat{\mathbf{D}}$ is the electric displacement, $\hat{\mathbf{E}}$ is the electric field, $\hat{\mathbf{P}}_{perm}$ is the permanent field-independent polarization, and $\hat{\mathbf{P}}_{ind}$ is the self-induced polarization. Therefore, the field in a

charged electret $\hat{\mathbf{E}}$ can be found by knowing $\hat{\mathbf{P}}_{perm}$ and $\hat{\mathbf{P}}_{ind}$, and by applying Gauss's law for a dielectric:

$$\oint \hat{\mathbf{D}} \cdot u_n \, d\Sigma = Q_r \tag{2.2}$$

Here Σ is a closed 3D surface, u_n is the unit vector perpendicular to it, Q_r is the sum of all *real* charges located inside Σ. If the electret is charged with polarization-type charges, the equation

$$\hat{\mathbf{P}} = \varepsilon_0(\varepsilon_r - 1)\hat{\mathbf{E}} \tag{2.3}$$

does not apply because it assumes that both molecular and electronic polarization are field-induced, while this is true only for electronic polarization. Thus, $\hat{\mathbf{P}}_{perm}$ must be known and an expression of $\hat{\mathbf{P}}_{ind}$ as a function of $\hat{\mathbf{E}}$ must be given in order to find the electric field.

If the electret charging only results in real charge distributions the situation is simpler: all polarization charges are self-induced so Eq. 2.3 is applicable and Eq. 2.1 reduces to:

$$\hat{\mathbf{D}} = \varepsilon_0\hat{\mathbf{E}} + \hat{\mathbf{P}}_{ind} = \varepsilon_0\varepsilon_r\hat{\mathbf{E}} \tag{2.4}$$

Rearranging this equation yields

$$\hat{\mathbf{E}} = \frac{\hat{\mathbf{D}}}{\varepsilon_0\varepsilon_r} = \frac{\hat{\mathbf{E}}_0}{\varepsilon_r} \tag{2.5}$$

It is then evident that the effect of self-induced polarization is a reduction of the internal field by a factor ε_r with respect to $\hat{\mathbf{E}}_0$, the field in the $\hat{\mathbf{P}}_{ind} = 0$ case. For a simple rectangular geometry and uniform real surface charge layers the electric fields can simply be found by applying the following boundary condition to discontinuity interfaces, i.e. material boundaries and surface charge layers:

$$\hat{\mathbf{D}}_1 - \hat{\mathbf{D}}_2 = \varepsilon_0\varepsilon_{r,1}\hat{\mathbf{E}}_1 - \varepsilon_0\varepsilon_{r,2}\hat{\mathbf{E}}_2 = \sigma_{1,2}\hat{\mathbf{u}}_{n,1} \tag{2.6}$$

where $\sigma_{1,2}$ is the real surface charge density at the interface, $\hat{\mathbf{u}}_{n,1}$ is the unit vector normal to the surface pointing towards region 1 and the other quantities refer to regions 1 and 2 (see Figure 2.3). This equation will be applied in the next section to derive the electric fields in the regions around a non-polar electret with a single real surface charge density.

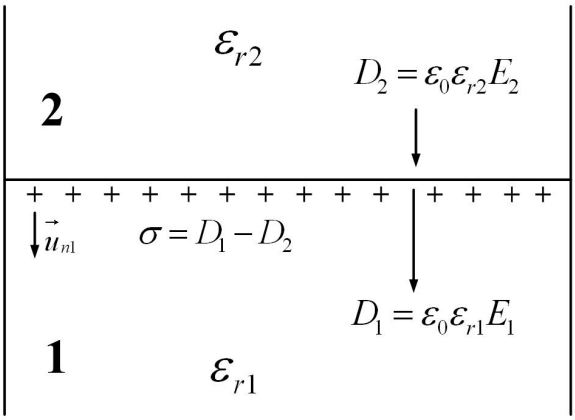


Figure 2.3: Interface between different ε_r materials with real surface charge layer

Charging of electrets is limited by breakdown effects. Dielectric breakdown takes place when charged particles in a dielectric start to accelerate under the effect of a strong electric field. The result is an avalanche ionization and a spark discharge in the dielectric, leading to the loss

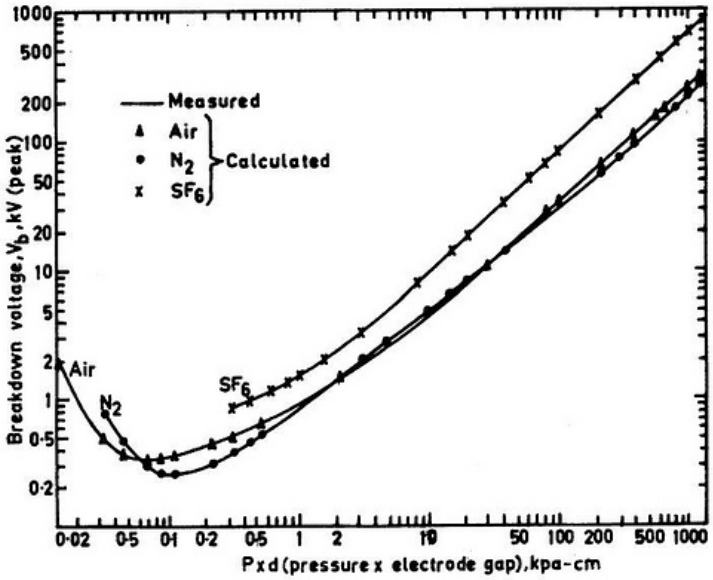


Figure 2.4: Paschen's curve for external breakdown in air and other fluids. Taken from [17]

of its insulating properties. External breakdown involves the fluid the electret is immersed in (typically air), while internal breakdown involves the electret itself.

External breakdown occurs when the voltage across the air gap between the electret and a metal electrode exceeds the value given by Paschen's law. This can be seen in Figure 2.4, where the breakdown voltage is plotted against the pressure–gap product. Paschen's curve has a minimum of 327V when $pd = 0.08$ kPa cm, which at atmospheric pressure means at a gap of about 8μm. It is evident that at a given pressure, if pd is large enough, the breakdown voltage increases linearly with the gap so that the breakdown *field* is approximately constant and is often given as a reference for dielectric strength of materials. Paschen's law applies for air gaps above approximately 3μm. Below this value, limitations given by field emission must be taken into account [16].

Internal breakdown is harder to quantify because it depends on the charge distribution in the electret. Assuming a permanent surface charge layer on one side and a metallized surface on the other, internal breakdown voltages for 10μm-thick electrets can be extrapolated from reported studies and are listed in Table 2.1.

Electret material	Breakdown voltage
Teflon	2kV [14]
CYTOP	5kV [18, 19]
SiO_2	10kV [20]

Table 2.1: Approximate internal breakdown voltages for a few popular electret materials assuming a 10μm thickness

The electret material chosen for this project is CYTOP, an amorphous non-polar polymer processed to yield a thin film (about 10μm) that is subsequently patterned into rectangles by plasma etching techniques (see also Section 3.2). The polymer is nonpolar, so molecular polarization charges can be neglected. Based on previous work on corona-charged CYTOP electrets [21, 11] it is assumed for the modeling that stored charges are situated in a uniform surface charge layer near the polymer's surface.

2.2 Corona Charging

2.2.1 Introduction

Corona charging is a popular discharge-based technique for injecting real charges into electrets. It has been employed in this project because it allows for a controlled and uniform deposition of surface charges at a high speed and relatively low cost. Electron-beam injection is far more expensive and complex to set up, while liquid contact electrification as shown in [22] is not applicable to our specific device. A corona setup is shown in Figure 2.5.

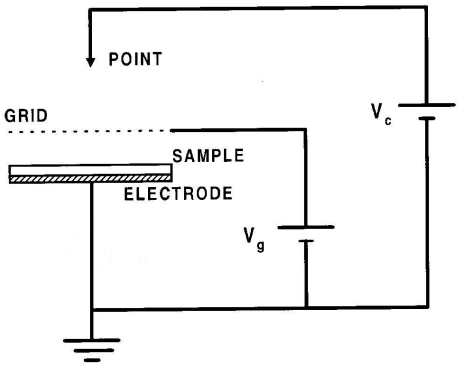


Figure 2.5: Schematic view of a corona charging setup. From [23]

A high voltage V_C is applied between a point-shaped electrode and a planar grounded electrode where the sample is placed. As a result, a discharge occurs and a current is observed in air if V_C is high enough (typically a few kV) to cause dielectric breakdown in the region near the electrode tip, where the field is the largest. This effect is enhanced by a very sharp tip, as charge accumulation in the regions with small radius of curvature produces a locally strong field. For a negatively biased tip, the discharge current is primarily made up by CO_3^- ions of thermal energy [14]. Because of their small energy, discharge ions have a low penetration depth into the sample and mostly deposit as a surface charge layer. It is assumed that they subsequently transfer their charge to surface traps in the electret. To achieve a high degree of control over the magnitude and uniformity of implanted charge, a wire grid is placed above the sample as seen in Figure 2.5. The grid is kept at constant voltage V_G to prevent the ions from accelerating towards the sample once its surface potential due to the charging has reached the value V_G. At the beginning the discharge current to the sample is "shadowed" by the grid wires but eventually the charge distribution on the sample surface is uniform if the charging time is long enough to allow the whole surface to reach the saturation potential V_G.

2.2.2 Corona Setup

In Figure 2.6 a simple model for charging is shown. Our sample is a full doped silicon wafer with a pattern of rectangular electrets with thickness t and much larger in-plane dimensions. The electrets are metallized on the substrate side with floating *base electrodes*. Between the silicon wafer and the base electrode there is a thin insulating layer of SiO_2. The silicon grounding is a critical matter for two reasons:

1. unlike metals, which typically have a resistivity of around $10^{-8}\,\Omega\,\mathrm{m}$, n- or p-doped silicon wafers available at our facilities have a resistivity of $10^{-1}\,\Omega\,\mathrm{m}$.

2. with the employed fabrication process flow, the only high-conductivity electrical path from

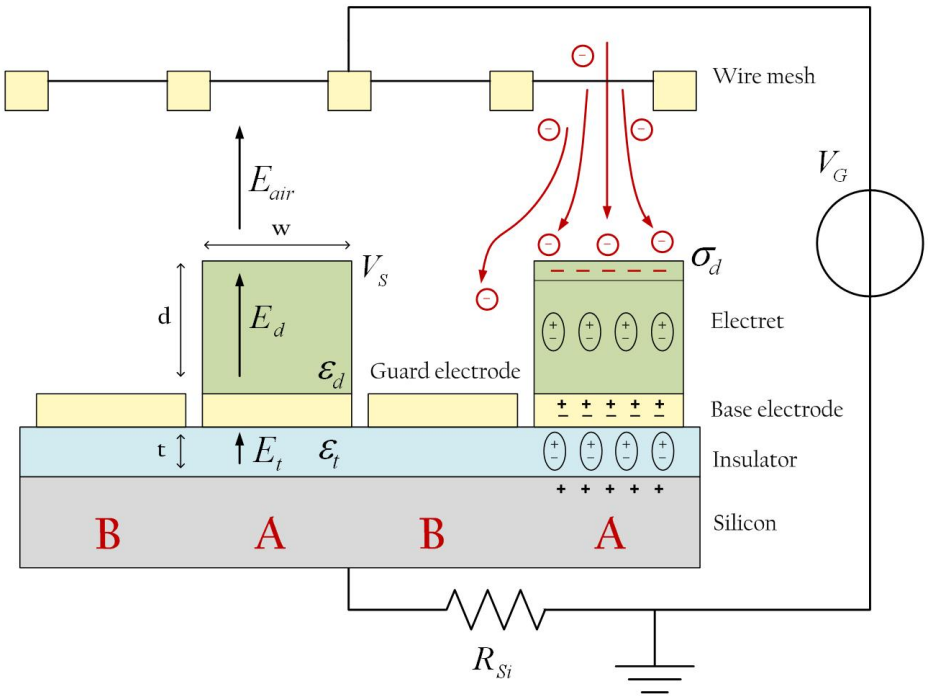


Figure 2.6: Model for electret charging. The sample is a simplified model of the device wafer fabricated for this project (see Chapter 3)

ground to the silicon beneath the electrets is through the device spring structure. The total cross sectional area for this structure is quite low.

For these reasons a significant resistance R_{Si} is expected between the silicon and the actual ground. For the theoretical model R_{Si} can be considered as zero because the effect of a finite resistance is mainly that of slowing down the charging, by introducing a time constant to the counter charge flow from silicon to ground.

Guard electrodes are employed to improve charge uniformity on the electrets, as proposed by [11]. Uniformity issues arise when ions from the corona drift experience a repulsive electrostatic force from the already charged electret surface, so that their trajectory is deflected away and the electret surface never reaches the full potential of the grid. The effect is more pronounced at the electret edges. Due to this phenomenon, the ratio V_S/V_G between the measured electret surface potential and the grid potential decreases with a higher grid voltage and a smaller electret width. Thanks to the non-zero lifetime of deposited charges on guard electrodes, the regions next to the electrets are also charged to a certain amount, resulting in a lower repulsive force driving the corona ions away from the electret. The improvement in the maximum surface potential reached by the electrets has been measured experimentally by [11] to be between 20% and 42% for a line-space electret pattern with linewidths between $90\mu m$ and $180\mu m$.

2.2.3 Physics of Charging

A simple plane capacitor model is used for the A regions in Figure 2.6. Assuming that w and V_G are small enough to neglect ion deflection, $E_{air} = 0$ in the region above the electrets after V_S has reached V_G. From Eq. 2.6 a boundary condition is applied at the air/electret interface:

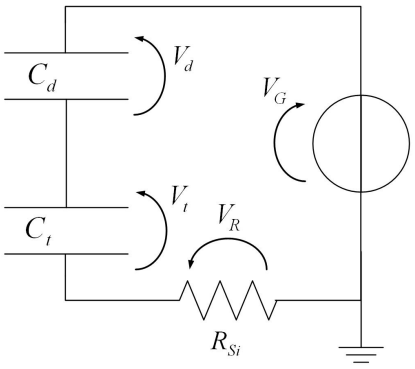


Figure 2.7: Plane capacitor circuit model for region A

$$-\varepsilon_0\varepsilon_d E_d = \sigma_d \tag{2.7}$$

so that the voltage drop across the electret is

$$V_d = \frac{E_d}{d} = -\frac{\sigma_d d}{\varepsilon_0\varepsilon_d} \tag{2.8}$$

Because the base electrode is a floating conductor, it has two surface charge layers of magnitude $-\sigma_d$ and σ_d on the electret side and insulating layer side respectively. A similar boundary condition can then be applied at the boundary between the base electrode and the insulator:

$$-\varepsilon_0\varepsilon_t E_t = \sigma_d \tag{2.9}$$

so that the voltage drop across the insulator is

$$V_t = \frac{E_t}{t} = -\frac{\sigma_d t}{\varepsilon_0\varepsilon_t} \tag{2.10}$$

Applying Kirchhoff's voltage law to the circuit as seen in Figure 2.7 results in:

$$V_G = V_d + V_t + V_R \tag{2.11}$$

Since $V_R = 0$ when the current drops to zero after the charging is completed, the implanted surface charge density can be found using Eq. 2.8, 2.10, and 2.11:

$$\sigma_d = \frac{\varepsilon_0 V_G}{\frac{d}{\varepsilon_d} + \frac{t}{\varepsilon_t}} \tag{2.12}$$

Our designed device has approximately $\varepsilon_d = 2$, $\varepsilon_t = 4$, $d = 10\mu m$, and $t = 1.5\mu m$, which means that

$$\frac{d}{\varepsilon_d} \simeq 13\frac{t}{\varepsilon_t} \tag{2.13}$$

so the insulating layer has little effect on the implanted charge density and can be neglected with an error of only $1/14 \simeq 7\%$, so a simpler expression for the charge density can be written as:

$$\sigma_d \simeq \frac{\varepsilon_0\varepsilon_d V_G}{d} \tag{2.14}$$

This model assumes a clear distinction between region A and region B. In region A $E_{air,A} = 0$ when the electret surface reaches V_G. In region B $E_{air,B} \neq 0$, the exact value depending on the

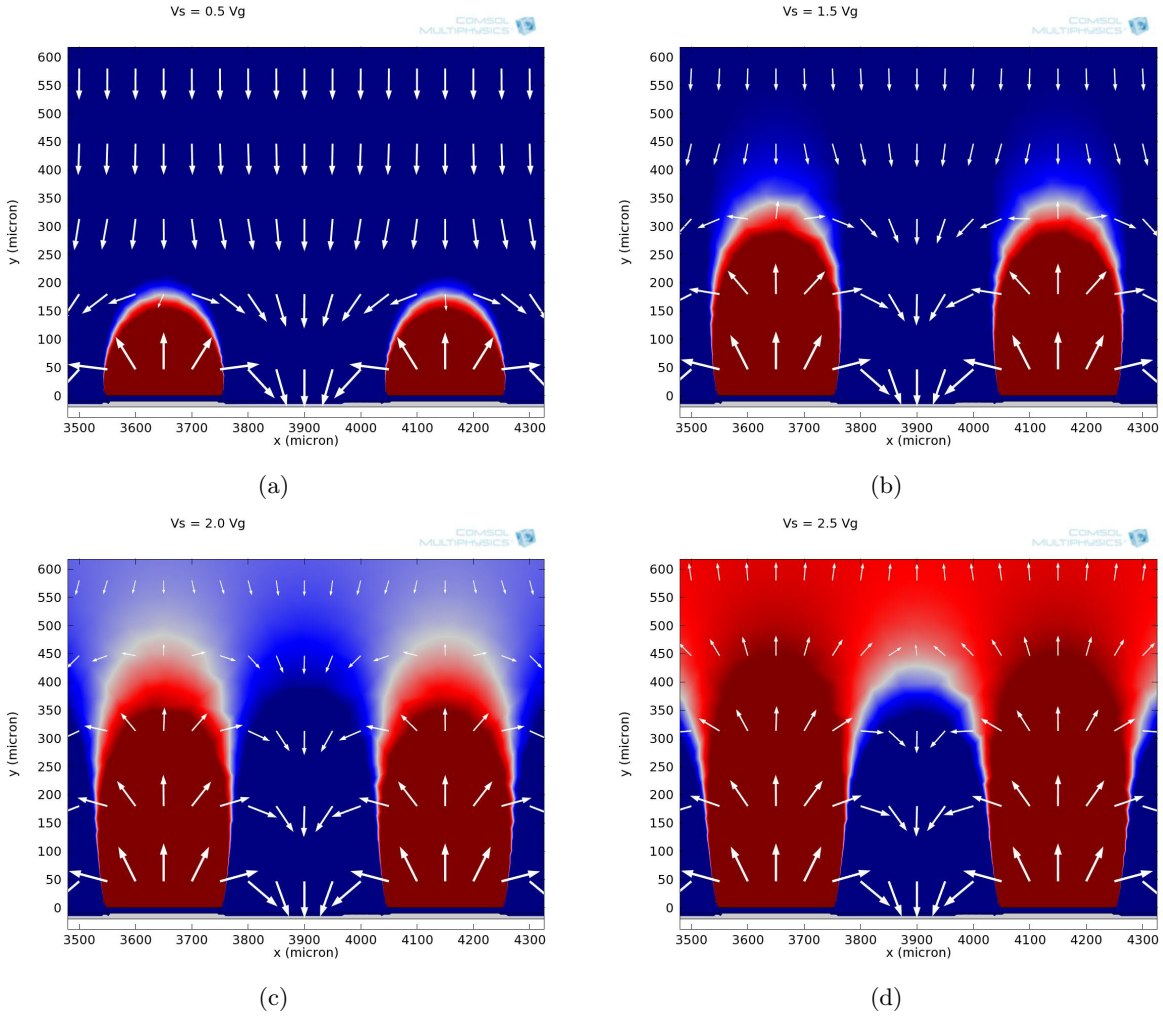


Figure 2.8: Simulated force vectors on corona ions located between the wire grid and the electret pattern for a few V_S/V_G ratios. $200\mu m$-wide electrets are placed on a grounded substrate and are spaced by $250\mu m$. No guard electrodes are present. The wire grid is kept at -200V and is 2mm away from the substrate. Colors refer to the *normal* component of the field with respect to the sample surface. Blue means attractive field, red means repulsive field. At the white border the normal field is zero. Note that the plane capacitor model predicts that the charging will stop when $V_S = V_G$. (a): $V_S = 0.5V_G$. (b): $V_S = 1.5V_G$. (c): $V_S = 2V_G$. (d): $V_S = 2.5V_G$.

instantaneous charge present in the base electrode. However, this is a limiting case only true at very small distances from the sample, where the overlap between $E_{air,A}$ and $E_{air,B}$ can be neglected. The distance between the wire grid and the sample is at least 10 times larger than the electret width, so near the grid $E_{air,A}$ and $E_{air,B}$ overlap almost completely. Eq. 2.14 is not valid anymore. Neglecting base electrode charging, in a full-overlap situation the total field is due to an array of point-like charges with magnitude $\sigma_d A_{el}$ associated to each electret (A_{el} is the surface area of a single electret). Since the device area A_{tot} is about half covered by electrets, corona ions keep accelerating past the grid until

$$V_S = \frac{\sigma_d d}{\varepsilon_0 \varepsilon_d} = (A_{tot}/A_{el})V_G \simeq 2V_G \tag{2.15}$$

To support this discussion, Figure 2.8 shows a simulation study. It is evident that the situation is qualitatively the same when V_S is well below V_G (Fig. 2.8(a)) and when V_S is well above V_G (Fig. 2.8(b)). The electric force on the corona ions is still attracting them towards

the surface until a distance that is comparable with the electret width. At this distance, an appreciable difference between region A and region B arises. Neglecting lateral deflection, corona ions can still reach the charged surface in region A if:

1. their kinetic energy in the normal direction is high enough to avoid inversion of motion before they reach the surface

2. their mean free path is at least comparable with the distance at which the normal force becomes repulsive.

It can be seen that when $V_S = 2V_G$ the large-distance normal field has almost reached zero (Fig. 2.8(c)), and that when $V_S = 2.5V_G$ it has become repulsive (Fig. 2.8(d)). This is because the surface coverage of electrets is a little less than $\frac{1}{2}$.

To conclude, a first limiting factor to the implanted charge is the $E_{air,tot} = 0$ condition. This depends on V_G but also on the surface coverage of electrets A_{el}/A_{tot} as seen from Eq. 2.15. A second limiting factor is ion deflection. Therefore, the electrets may never reach the potential given by Eq. 2.15 due to the large lateral repulsive forces arising at a shorter distance, but it should be kept in mind that electret charging beyond the grid potential is possible. As discussed in chapter 3, a stable surface potential of slightly less than -400V has been measured for an electret pattern charged under a grid voltage of -200V with a $\frac{1}{2}$ surface coverage.

2.2.4 Measurement of Implanted Charges

The surface potential measurement is carried out with a distance-compensated electrostatic voltmeter. Its operation principle is shown in Figure 2.9. A grounded rotating conductor periodically shields the probe electrode from the electric field produced by the stored charge in the electrets. As a result, induction charges on the probe electrode are modulated and an AC voltage signal is created in the probe. With a feedback mechanism, a DC voltage V_{DC} is applied between the probe electrode and the grounded substrate until the AC voltage drops to zero. Reaching this condition implies that there are no more induction charges on the probe electrode to cause an AC signal, and this only happens when $E_{air} = 0$ near the probe. Therefore, according to Kirchhoff's voltage law the DC voltage equals the voltage drop between the charged surface and the grounded substrate [14].

Similarly to the discussion for corona charging, the actual electret surface charge density can be inferred if the probe electrode is far enough from the sample so that the fields in regions A and B overlap completely, but still close enough to neglect distance-dependent field decay, namely:

$$w_{el} \ll g \ll w_{tot} \tag{2.16}$$

In this configuration, the field close to the probe is due to a capacitor with area equal to the total device area A_{tot} and charge equal to the total stored charge in the electrets $\sigma_d A_{el}$. Then, using Eq. 2.15, V_{DC} is found to be:

$$V_{DC} = \frac{Q_d}{C} = \frac{\sigma_d A_{el}}{\varepsilon_0 \varepsilon_d A_{tot}/d} = \frac{A_{el}}{A_{tot}} V_S \simeq V_G \tag{2.17}$$

The fact that the surface potential measured by the electrostatic voltmeter is the wire grid potential V_G rather than the actual electret surface potential V_S can be misleading. It should be kept in mind that in order to find V_S a multiplication of the measured value by the factor A_{tot}/A_{el} is necessary.

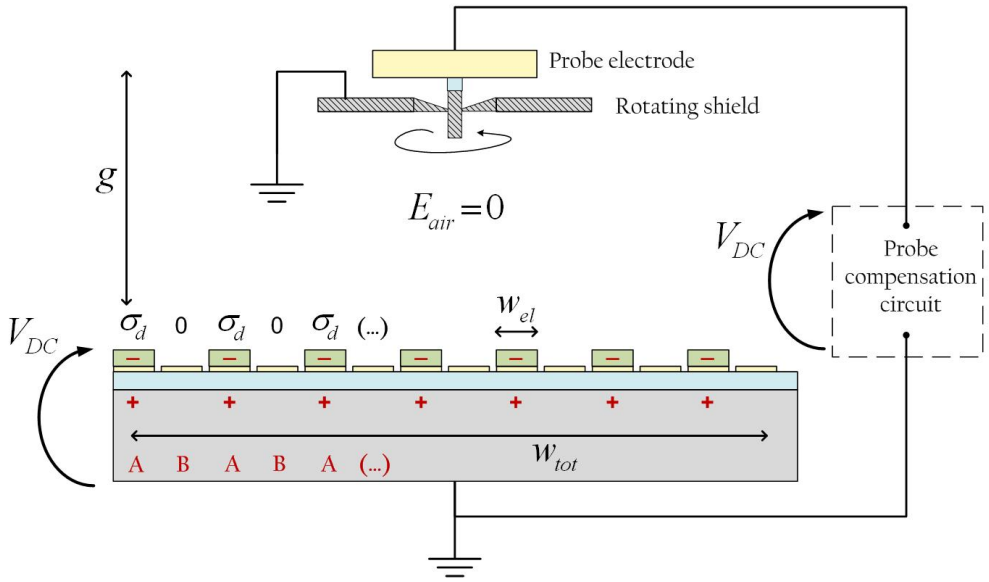


Figure 2.9: Measurement of electret surface potential with distance-compensated electrostatic voltmeter

2.3 Electrical Domain

In this section a model is developed to derive electrical quantities assuming an ideal in-plane forced harmonic oscillation of the electret pattern with respect to a *counter electrode* pattern. No coupling is assumed between the electrical and mechanical parts. Such a study should only be regarded as a preliminary investigation for the fully coupled model presented in Section 2.5.

2.3.1 Introduction

The electret and counter electrode patterns are located on a silicon and a glass substrate respectively (see also Chapter 3). Figure 2.10 gives an overview of the device electrical domain. Regions 1 and 2 both contain two time-varying capacitances due to the periodic change in overlapping area. $C_c(t)$ is the one between the counter electrodes and the electret charge layer, $C_b(t)$ is the one between the the electret charge layer and the floating base electrode. There is also another pair of capacitances between the base electrode and the silicon substrate across the insulating layer. Throughout the model, the spacing between counter electrodes is regarded as infinitely small. This is only an approximation as designed devices have spacings as large as $30\mu m$ or $50\mu m$ for an electrode width of $200\mu m$ (see Chapter 3).

It is evident that the counter electrodes with label 1 are geometrically equivalent, and so are the ones with label 2. Then, connecting all the electrodes with the same label together is like connecting their associated capacitances in parallel. This reduces the problem to studying only a single electret "cell" made up of regions 1 and 2. The total effect can be simulated by multiplying the area of one counter electrode A_0 by the number of cells n, which is like multiplying the capacitance by the same factor. The resistance R_L is placed between node 1 and node 2 to simulate the equivalent resistive load of the device to be powered by the harvester. A reference to ground is made at node 2. T Since it is practically impossible to connect the silicon substrate to ground with the current device design, it should be considered to be at floating potential. If a ground contact does occur for any reason, the model presented in the next section loses validity and reference to the model used by [24] or [11] should be made, where the substrate and counter electrode 2 are both at ground potential.

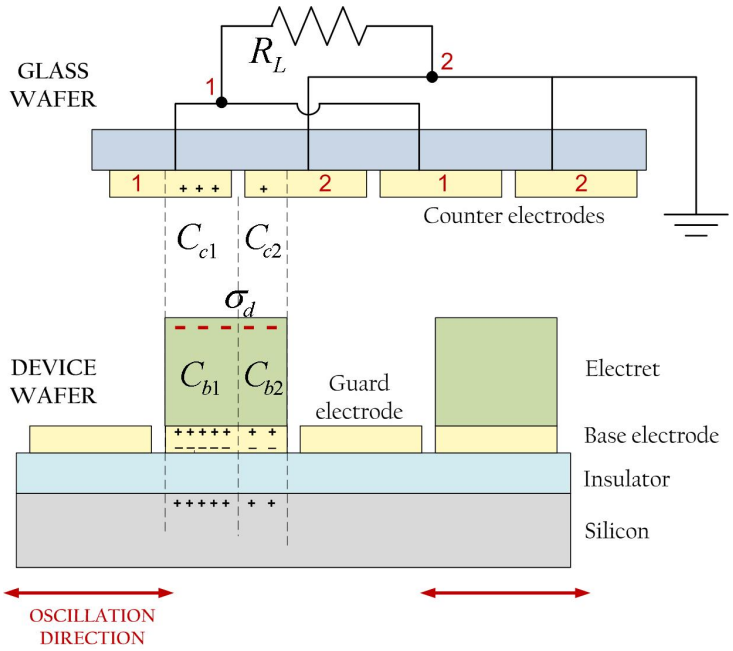


Figure 2.10: Overview of energy harvester electrical domain

2.3.2 Static Model

The validity of the equations used in the model is now discussed. A first assumption is that a plane capacitor model can be employed in which the capacitor width equals the overlap width between counter electrodes and electrets. Eq. (2.6) can then be used to calculate electric fields. This is only a rough approximation because the electret width is $200\mu m$ and the gap between the two wafers is around $100\mu m$. Especially for small overlap areas, a significant contribution from fringing fields is expected, as has been shown by [25]. This effect will be estimated in Section 2.5.4.

Another assumption is that $\hat{\mathbf{E}} = 0$ outside the system, i.e. the substrate and counter electrodes are at ground potential. Modeling becomes far more complex if this hypothesis is not met because the induced charges will be ill-defined, their actual value depending on electrical configurations outside the system. This problem can be solved by briefly grounding the substrate and counter electrodes at the same time before operation. If this is difficult to achieve in practice, one can wait until the very small currents due to a finite resistance between conductors and ground lead all conductive parts to ground potential (Figures 2.11(b) and 2.11(c)). Since in this situation $\hat{\mathbf{E}} = 0$ outside the system, the fields generated by the different charge layers must compensate outside the system. With reference to Figure 2.12, the expression for each of these contributions to the field in air is

$$E_{\sigma_x} = \frac{\sigma_x}{2\varepsilon_0} \tag{2.18}$$

so the net fields outside the system for regions 1 and 2 are:

$$\begin{cases} E_1 = \dfrac{\sigma_d + \sigma_{b1} + \sigma_{c1}}{2\varepsilon_0} = 0 \\ E_2 = \dfrac{\sigma_d + \sigma_{b2} + \sigma_{c2}}{2\varepsilon_0} = 0 \end{cases} \tag{2.19}$$

and therefore

$$\begin{cases} \sigma_d + \sigma_{b1} + \sigma_{c1} = 0 \\ \sigma_d + \sigma_{b2} + \sigma_{c2} = 0 \end{cases} \tag{2.20}$$

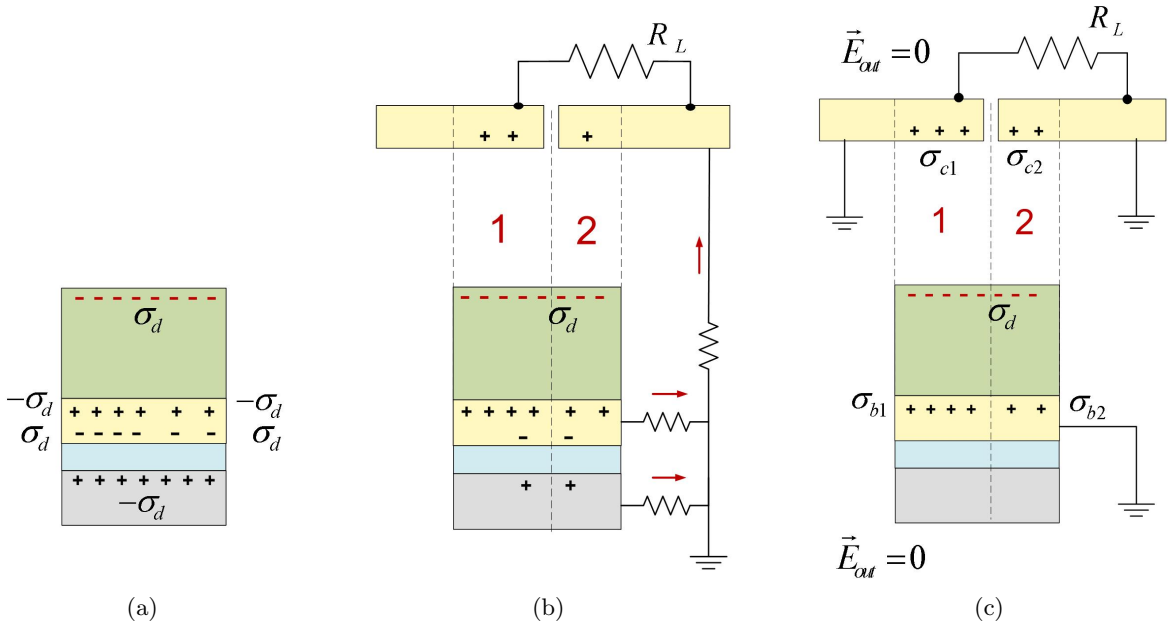


Figure 2.11: Charge distributions at different stages of device fabrication. (a): After electret charging. (b): Slow charge flow to ground after placing the counter electrode pattern at the desired distance. (c): When all conductive parts have reached ground potential.

Using these relations, the fields within the electret can be written as:

$$\begin{cases} E_{d1} = \dfrac{\sigma_{b1} - \sigma_d - \sigma_{c1}}{2\varepsilon_0\varepsilon_d} = \dfrac{\sigma_{b1}}{\varepsilon_0\varepsilon_d} \\ E_{d2} = \dfrac{\sigma_{b2} - \sigma_d - \sigma_{c2}}{2\varepsilon_0\varepsilon_d} = \dfrac{\sigma_{b2}}{\varepsilon_0\varepsilon_d} \end{cases} \tag{2.21}$$

In a similar fashion, the fields in the air gap can be written as:

$$\begin{cases} E_{g1} = \dfrac{\sigma_{c1} - \sigma_d - \sigma_{b1}}{2\varepsilon_0} = \dfrac{\sigma_{c1}}{\varepsilon_0} \\ E_{g2} = \dfrac{\sigma_{c2} - \sigma_d - \sigma_{b2}}{2\varepsilon_0} = \dfrac{\sigma_{c2}}{\varepsilon_0} \end{cases} \tag{2.22}$$

In a static situation after the whole system has been grounded $V_g = V_d$ so for region 1:

$$V_{g1} = V_{d1} \Longrightarrow E_{g1}g = E_{d1}d \Longrightarrow \frac{\sigma_{c1}g}{\varepsilon_0} = \frac{\sigma_{b1}d}{\varepsilon_0\varepsilon_d} \tag{2.23}$$

Substituting the first relation of Eq.(2.20) into the previous equation yields

$$\frac{\sigma_{c1}g}{\varepsilon_0} = \frac{(-\sigma_{c1} - \sigma_d)d}{\varepsilon_0} \tag{2.24}$$

By rearranging this equation and noticing that the same procedure can be applied to region 2, one finally gets:

$$\sigma_{c1} = \sigma_{c2} = -\sigma_d \frac{d}{d + \varepsilon_d g} = \sigma_{c0} \tag{2.25}$$

and

$$\sigma_{b1} = \sigma_{b2} = -\sigma_d \frac{\varepsilon_d g}{d + \varepsilon_d g} = \sigma_{b0} \tag{2.26}$$

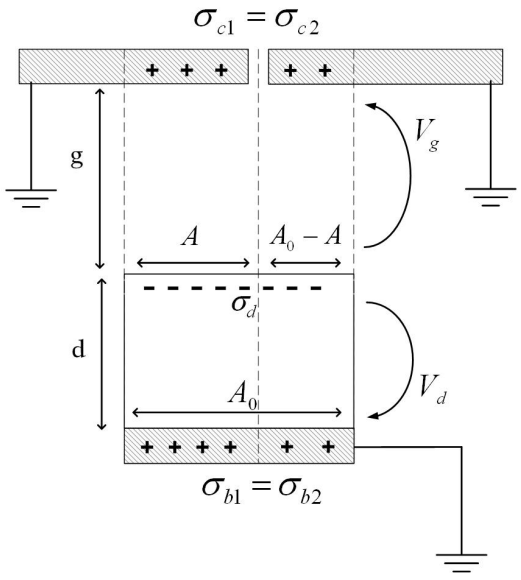


Figure 2.12: Electrical model for grounded system with static overlap

Equations (2.25) and (2.26) are the *static* charge densities on base and counter electrodes once they have all reached ground potential. For our device $d = 10\mu m$, $g = 100\mu m$, and $\varepsilon_d = 2$, so $\varepsilon_d g \simeq 20d$. Hence, 95% of the electret charge is induced on the base electrode and 5% on the counter electrode.

The system can be described (see Figure 2.11(a)) by equivalent capacitances

$$\begin{cases} C_{g1} = \dfrac{A\varepsilon_0}{g} \\ C_{d1} = \dfrac{A\varepsilon_0\varepsilon_d}{d} \\ C_{g2} = \dfrac{(A_0 - A)\varepsilon_0}{g} \\ C_{d2} = \dfrac{(A_0 - A)\varepsilon_0\varepsilon_d}{d} \end{cases} \tag{2.27}$$

and associated charges

$$\begin{cases} Q_{g1} = A\,\sigma_c \\ Q_{d1} = A\,\sigma_b \\ Q_{g2} = (A_0 - A)\sigma_c \\ Q_{d2} = (A_0 - A)\sigma_b \end{cases} \tag{2.28}$$

where $\sigma_c = \sigma_{c1} = \sigma_{c2}$, and $\sigma_b = \sigma_{b1} = \sigma_{b2}$.

2.3.3 Dynamic Model

When an in-plane relative oscillation of the two patterns occurs, overlap areas become time-dependent, i.e. $A = A(t)$ and $A_0 - A = A_0 - A(t)$. If charge densities remained constant, there would be no difference with the static case because for a plane capacitor

$$V = \frac{Q}{C} = \frac{A(t)\sigma(t)}{\varepsilon_0\varepsilon_d A(t)/d} = \frac{\sigma(t)d}{\varepsilon_0\varepsilon_d} \tag{2.29}$$

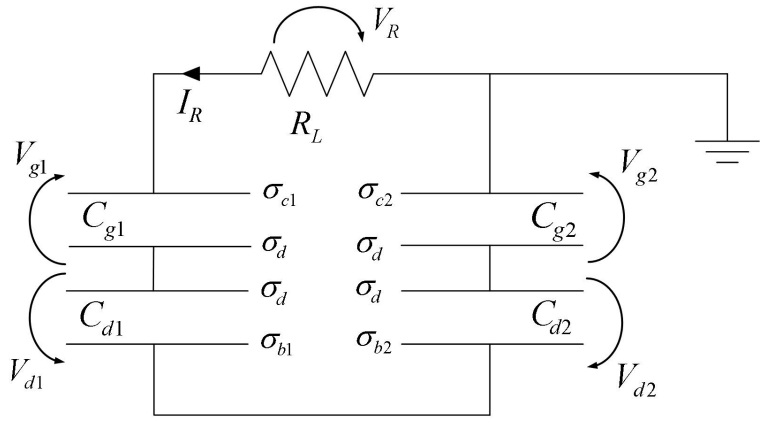


Figure 2.13: Circuit representation of operating energy harvester. σ_d and R_L are constant, whereas all other quantities are time-dependent.

If $\sigma(t)$ was constant all voltages would be the same as in the static model and there would be no voltage drop across the load resistance and no harvested power. Charge flow from counter electrode 1 to counter electrode 2 does not occur instantaneously, due to the finite response time of the system

$$\tau = R_L C_h \tag{2.30}$$

where τ is the characteristic time constant for capacitor charging, and C_h is the equivalent capacitance in parallel with the load resistance. There are substantial differences in the employed equations with respect to the static case (regarding sign conventions, reference should be made to Figure 2.13):

1. Eq. (2.20) describing complete charge induction is not strictly valid anymore. This is because now only one counter electrode is locked at ground potential. The electric potentials of other electrodes depend on this reference potential and on the instantaneous physical configuration of the system. Therefore it is not true anymore that the electric field is zero outside the system, and a net induced charge can appear on external grounded conductors. However, if such external elements are kept reasonably far from the system, the field between them and the non-grounded electrodes will be very low since it scales inversely with distance. So Eq. (2.20) will be used again.

2. Kirchhoff's voltage law should be applied for the whole circuit in Figure 2.13 as

$$V_R = V_{g2} - V_{d2} + V_{d1} - V_{g1} \tag{2.31}$$

3. Voltages for all capacitors can still be found by using Eq. (2.22).

4. The voltage drop across the load resistance considering all n electret cells can be written as

$$V_R = R_L I_R = R_L \frac{dQ_{c1}}{dt} = R_L \frac{d(nA\,\sigma_{c1})}{dt} \tag{2.32}$$

5. Since the base electrode is electrically isolated, conservation of its total charge is required:

$$A\,\sigma_{b1} + (A_0 - A)\sigma_{b2} = A_0 \sigma_{b0} \tag{2.33}$$

where σ_{b0} is the static base electrode surface charge density found with Eq. (2.26).

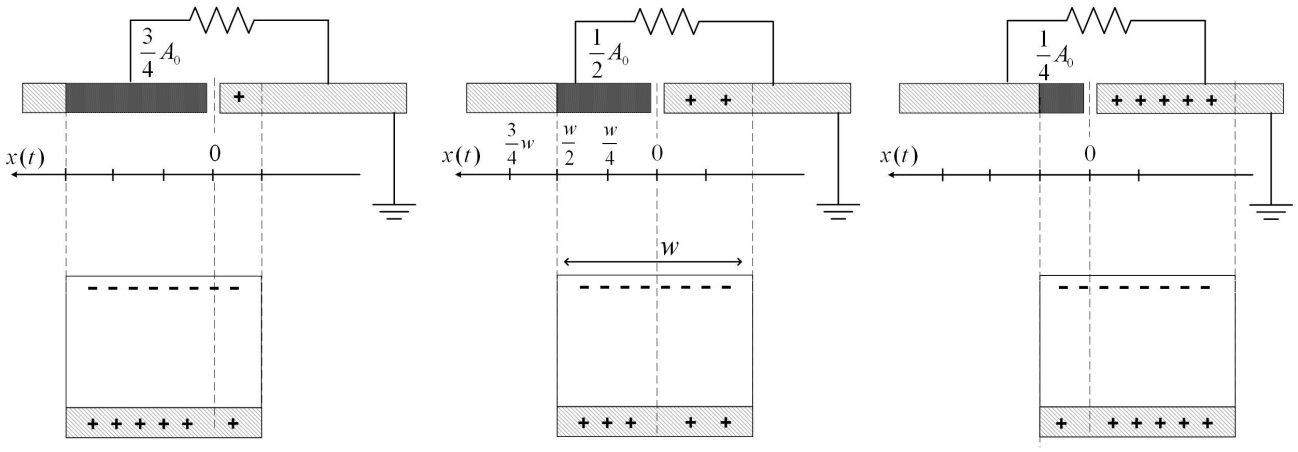


Figure 2.14: Schematic view of equilibrium point (center) and oscillation extrema (left, right)

To sum up, the following set of simultaneous equations has to be satisfied:

$$\begin{cases} \sigma_d + \sigma_{b1} + \sigma_{c1} = 0 \\ \sigma_d + \sigma_{b2} + \sigma_{c2} = 0 \\ R_L \frac{dQ_{c1}}{dt} = V_{g2} - V_{d2} + V_{d1} - V_{g1} \\ A\,\sigma_{b1} + (A_0 - A)\sigma_{b2} = A_0\sigma_{b0} \\ V_{g1} = \dfrac{(\sigma_{c1} - \sigma_d - \sigma_{b1})}{2\varepsilon_0} g \\ V_{d1} = \dfrac{(\sigma_{b1} - \sigma_d - \sigma_{c1})}{2\varepsilon_0\varepsilon_d} d \\ V_{g2} = \dfrac{(\sigma_{c2} - \sigma_d - \sigma_{b2})}{2\varepsilon_0} g \\ V_{d2} = \dfrac{(\sigma_{b2} - \sigma_d - \sigma_{c2})}{2\varepsilon_0\varepsilon_d} d \\ Q_{c1} = nA\,\sigma_{c1} \end{cases} \tag{2.34}$$

If the functional form of A(t) is known, there are 9 variables and 9 independent equations (8 algebraic, 1 differential) so no more relations are needed to find a solution. By substitution, an ordinary differential equation in Q_{c1} (from now on just called Q for simplicity) is left to solve, that is:

$$\frac{dQ(t)}{dt} = -\frac{A_0(d\varepsilon_d + g)}{\varepsilon_0\varepsilon_d RnA(t)[A_0 - A(t)]} Q(t) + \frac{A_0 d\sigma_d}{\varepsilon_0\varepsilon_d R[A_0 - A(t)]} \tag{2.35}$$

or, grouping the coefficients,

$$\frac{dQ(t)}{dt} = -m(t)Q(t) + n(t) \tag{2.36}$$

This is a linear first-order ODE: *linear* because Q and $\dot{Q}$ appear with the power of 1, and of *first-order* because the first derivative is the highest-order derivative. A sinusoidal oscillation with constant amplitude of the two electrode patterns with respect to each other will be assumed for this model, such as

$$x(t) = X_a \sin(2\pi f t) \tag{2.37}$$

where $x(t)$ is the displacement from the equilibrium position x_0, X_a is the oscillation amplitude, and f is the oscillation frequency. If the electret surface is simply a square with dimensions $w \times w$

Air gap	g	$100\mu m$
Electret thickness	d	$10\mu m$
Electret length and width	w	$200\mu m$
Number of electret cells in one device	n	450
Oscillation frequency	f	200Hz
Electret surface charge density	σ_d	3.54×10^{-4} C
Load resistance	R	$1\,G\Omega$
Electret relative permittivity	ε_d	2

Table 2.2: Parameters used to solve Eq.(2.36).

and overlap only varies in one direction, then the maximum obtainable overlap area is $A_0 = w^2$ and the instantaneous overlap area is $A(t) = w[x(t) + x_0]$. If $X_a = w/4$ and the equilibrium configuration is given by the electret laying exactly in the middle between counter electrodes 1 and 2, it follows that for the overlap area:

$$A(t) = \frac{A_0}{2} + \frac{A_0}{4}\sin(2\pi f t) \tag{2.38}$$

so that $A(t)$ oscillates harmonically between $A_0/4$ and $3/4\,A_0$ (see also Figure 2.14).

2.3.4 Results

This expression is now plugged into Eq. (2.35). An analytical solution for the equation has not been found. Therefore, an explicit expression for the output power cannot be provided. To get at least an idea of the optimal load, the model found in [11] is employed. According to this model, both the base electrode and one counter electrode are grounded and the optimal load can be found analytically to be:

$$R_{opt} = \frac{d + \varepsilon_d g}{\varepsilon_0 \varepsilon_d 2\pi f n A_0/2} = \frac{d + \varepsilon_d g}{\varepsilon_0 \varepsilon_d \pi f n A_0} \tag{2.39}$$

resulting in $R_{opt} = 1.05\,G\Omega$ for our device parameters, seen in Table 2.2. Using this optimal load, Eq. (2.35) is now solved numerically with the *NDSolve* algorithm provided by Wolfram Mathematica©. Since $A(0) = A_0/2$ it seems reasonable to impose the following initial condition to the Cauchy problem:

$$Q(0) = \frac{nA_0}{2}\sigma_{c0} \tag{2.40}$$

where σ_{c0} is the static surface charge density on the counter electrodes found in Eq. (2.25). The numerical solution with parameters given by Table 2.2 is plotted in Figure 2.15. A comparison is made with the overlap area oscillation given by Eq. (2.38). It is evident that the charge signal is delayed with respect to the mechanical oscillation. The signal seems to stabilize at the same frequency f of the oscillation, with a phase shift that will be quantified later in this section. The numerical solution becomes unstable after one period of oscillation, so no information can be extracted beyond this limit. Because of this restriction, the following optimization loop is implemented in Mathematica to find the best fit for the phase shift of the charge function:

1. the *FindFit* function is used to fit the numerical solution to a function in the form

$$Q_{fit}(t) = \frac{Q_{max} + Q_{min}}{2} + \left(\frac{Q_{max} - Q_{min}}{2}\right)\sin(2\pi f t + \varphi) \tag{2.41}$$

where Q_{max} and Q_{min} are the maximum and minimum values of the previously calculated charge function, f is the mechanical oscillation frequency, and φ is the phase shift. φ is the only fitting parameter as the others are known.

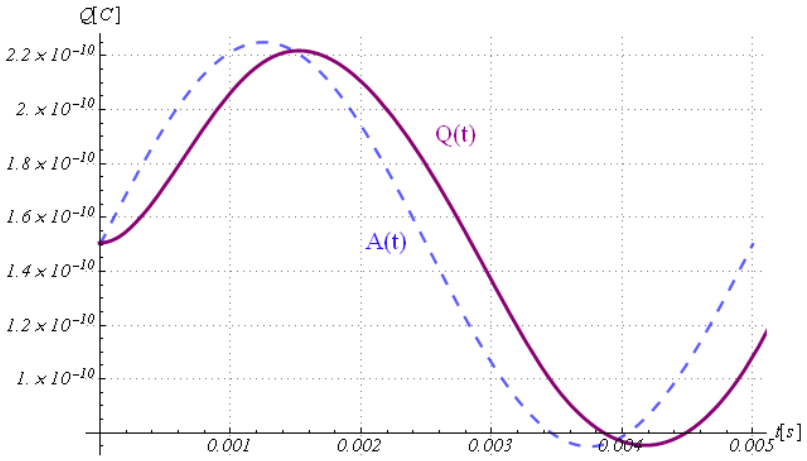


Figure 2.15: *Purple*: numerical solution of Eq. (2.35) for charge on counter electrode 1, with Eq. (2.40) as an initial condition. *Blue*: normalized plot of A(t).

2. the differential equation of the system is solved again with $Q(0) = Q_{fit}(0)$ as an initial condition.

3. the procedure is repeated until an acceptable fit is found.

After a few loops a better approximation of φ is found. For the parameters shown in Table 2.2, $\varphi \simeq 0.192\pi \simeq \frac{\pi}{5}$. This procedure also allows to visualize easily from Figure 2.16 that also the electric current signal dQ/dt has a similar phase shift with respect to the velocity of the oscillator. This is of course expected because they are the derivatives of $Q(t)$ and $x(t)$ respectively. The instantaneous harvested power is simply the power dissipated in the load resistance:

$$P_h(t) = I^2(t)R = \left(\frac{dQ}{dt}\right)^2 R \tag{2.42}$$

Since the power signal is approximately a squared sine function, its RMS value is simply 1/2 of its maximum value. Hence the predicted harvested power with the current parameters is:

$$P_{h,rms} = P_{max}/2 \simeq 4\mu W \tag{2.43}$$

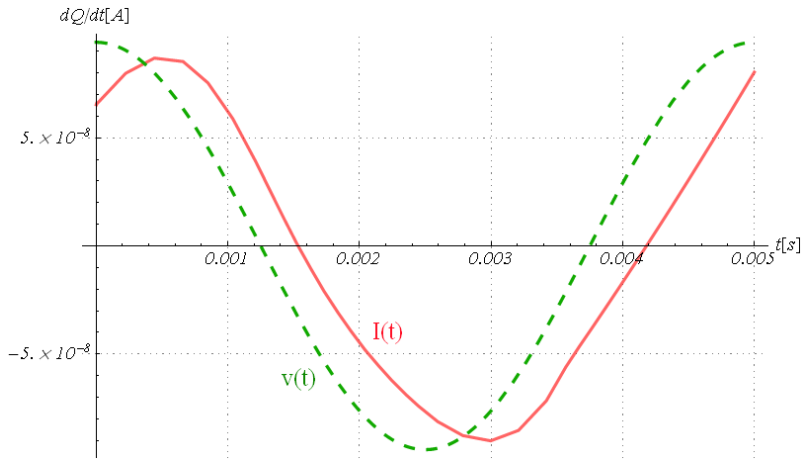


Figure 2.16: *Red*: electrical current signal as the derivative of charge signal found with optimization procedure. *Green*: normalized plot of area overlap velocity.

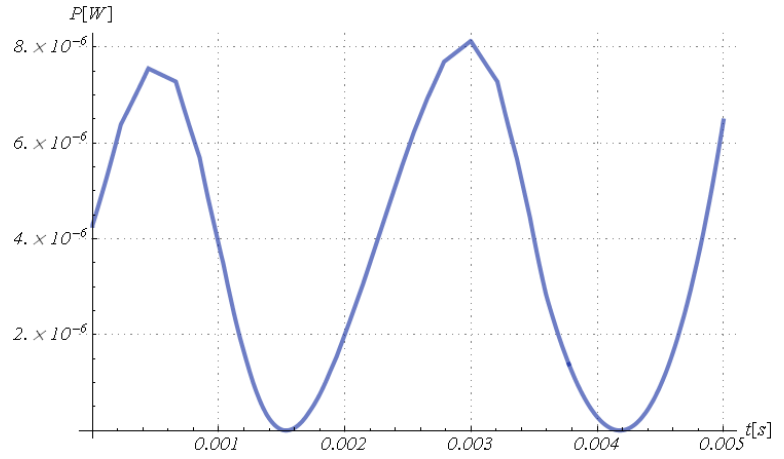
Note that this value can also be derived by calculating the area of the $Q - V_R$ hysteresis loop, where V_R is the voltage drop across the load resistance. This area corresponds to the irreversible work done by the vibration source to move charge across the voltage V_R in *one period* T of oscillation. Since the hysteresis loop is roughly elliptical, its area is approximately

$$E_T = \pi(V_{max} - V_{min})(Q_{max} - Q_{min}) \simeq 26nJ \tag{2.44}$$

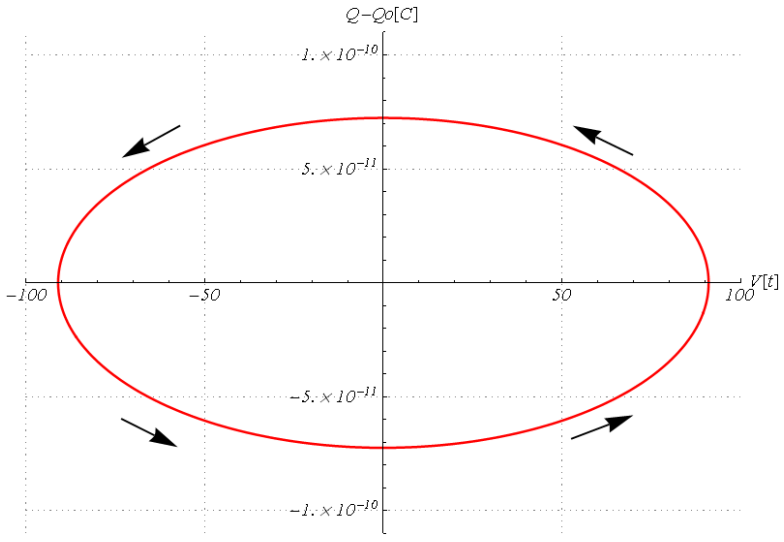
The harvested power is then

$$P_{h,rms} = E_T/T = E_T\, f = 4.1\mu W \tag{2.45}$$

in good agreement with the value found using the power signal. Note that in this calculation the harmonic fit to $Q(t)$ found with Eq. (2.41) has been used.



(a)



(b)

Figure 2.17: Two ways to calculate power output. (a): From power signal across the load resistance. (b): From hysteresis loop for counter electrode charge with respect to voltage drop in load resistance.

2.4 Mechanical Domain

In this section the main mechanical forces acting on the harvester are described, so that an equation of motion can be written for the device assuming no coupling with the electrical domain. A Finite Element analysis is included in order to estimate the resonance frequency of the device spring system.

2.4.1 Proof Mass Oscillation with Harmonic Source Motion

The proof mass is excited by the motion of a vibration source, which is modeled as a one-dimensional harmonic oscillation of frequency f and amplitude Y_0 with respect to an *inertial* reference frame Y:

$$y(t) = -Y_0 \sin(2\pi f t) \tag{2.46}$$

Of course this is only a rough approximation because the vibration source will most likely have many other harmonic components at different frequencies and directions [2]. However, a resonant system only responds to a narrow frequency range around its resonance frequency, so the latter can be designed to match a peak of the source vibration spectrum. Additionally, our device design allows two perpendicular in-plane source motion components to excite proof mass vibration, but a 2D analysis would considerably complicate the electrical model.

Following [26], a *non-inertial* reference frame X that follows the vibrating source is now introduced to simplify the analysis. If x and $\tilde{y}$ are the proof mass displacements with respect to X and Y, then

$$x = \tilde{y} - y \tag{2.47}$$

With such conventions, forces on the proof mass can be described with respect to reference frame X:

- F_{ext} is the force due to source vibration, i.e. relative motion between reference frames X and Y. From Eq. 2.47, $m\ddot{x} = m\ddot{\tilde{y}} - m\ddot{y}$ but if this force is considered alone $m\ddot{\tilde{y}} = 0$. Hence $F_{ext} = -m\ddot{y}$ in the X reference frame, which can be calculated from Eq. 2.46.

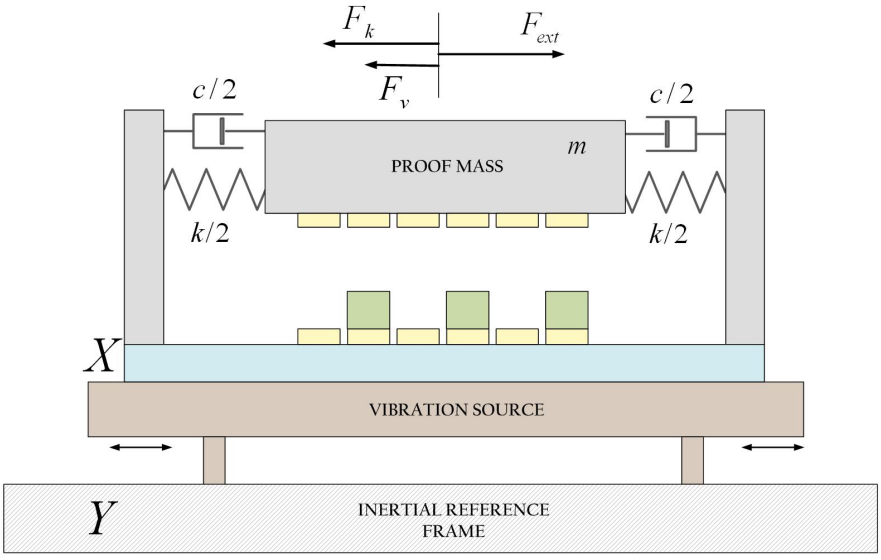


Figure 2.18: Schematic view of device's mechanical domain.

- $F_k = -kx$ is the elastic force due to the spring structure between the proof mass and the device casing. $k = 4\pi^2 {f_o}^2 m$ is the total spring constant of the spring system, and f_o its *resonance* frequency.
- $F_v = -c\dot{x}$ is a viscous damping force due to air resistance, symbolized by the dashpots in Figure 2.18. $c = 2\pi m f_o/q$ is the damping constant and q is defined as the *quality factor* of the mechanical system.

Then the following equation of motion for the proof mass can be written:

$$m\ddot{x} = F_{net} = F_{ext} + F_k + F_v = -m\ddot{y} - kx - c\dot{x} \tag{2.48}$$

If this equation is solved, the following steady-state solution is found:

$$x(t) = X_0 \sin(2\pi f t - \psi) \tag{2.49}$$

This means that, after a transient, a viscously-damped proof mass will oscillate harmonically at the same frequency of the vibration source. The oscillation amplitude X_0 shows a peak for f around f_o and has the following limiting values:

$$X_0 = \begin{cases} Y_0 & f \ll f_o \\ q\,Y_0 & f = f_o \\ 0 & f \gg f_o \end{cases} \tag{2.50}$$

The last condition only applies if the quality factor is large enough ($q \gg 1$), i.e. when viscous damping is reasonably low. From [26], the peak width at 1/2 of its maximum value (FWHM) can also be estimated by knowing the q-factor:

$$\text{FWHM} = \Delta f = \frac{f_o}{q} \tag{2.51}$$

Therefore, a low q-factor results in a sharp resonance peak with a large amplitude and a narrow bandwidth, whereas a high q-factor leads to a lower-amplitude peak with a broader bandwidth.

The phase delay ψ with respect to the source oscillation X_0 is:

$$\psi = \begin{cases} 0 & f \ll f_o \\ \dfrac{\pi}{2} & f = f_o \\ \pi & f \gg f_o \end{cases} \tag{2.52}$$

where the sharpness of the transition between 0 and π increases with an increasing q-factor.

It can be concluded from this model that, at resonance, the oscillation of the proof mass is closely related to that of the source. It will be delayed by 1/4 of a period and amplified by the q-factor.

The simple mechanical model presented in this section does not take into account any electrical force on the proof mass, so it is only valid in the case of weak electromechanical coupling. However, it can serve as a reference to estimate the mechanical q-factor from experimental data whenever coupling is absent, as for uncharged electrets. Additionally, it proves useful if the electrical force is approximately proportional to velocity. In such a case, an electrical damping constant can be added to the mechanical damping constant, yielding a "mechanical" and an "electrical" q-factor. This has been successfully done by Williams and Yates [27] but cannot be applied to our harvester, as will become evident in Section 2.5.

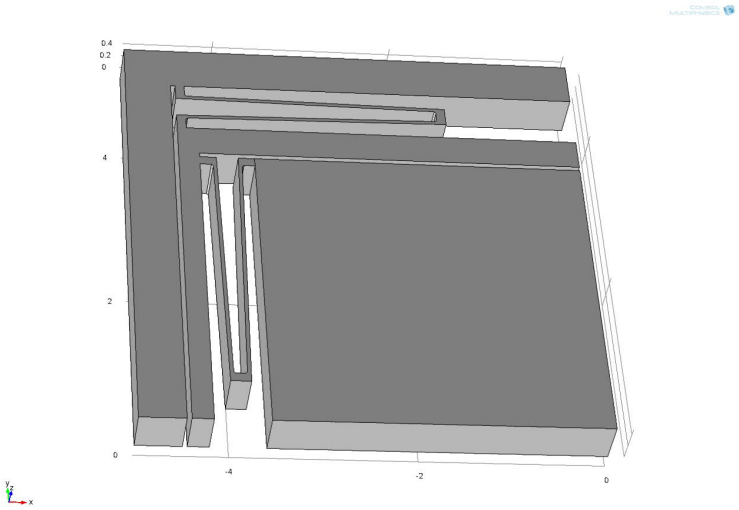


Figure 2.19: 3D view of spring system between the proof mass and the device casing.

2.4.2 FEM analysis

The resonance frequency of the system is estimated with a 2D simulation in COMSOL Multiphysics©. Because of symmetry, only 1/4 of the device area can be used allowing for faster computation. In a 2D model a single out-of-plane thickness has to be set for the whole system. To account for different thicknesses for the proof mass and springs, the out-of-plane thickness is set to the spring thickness and material density is redefined in the proof mass to give an equivalent effect as a different thickness. Eigenfrequency studies are set separately for the two in-plane easy axes by choosing appropriate symmetry and antisymmetry boundary conditions. Simulated resonance frequencies range from 201 Hz (long springs with small out-of-plane thickness) to 612 Hz (short springs with large out-of-plane thickness). There is a small difference between the two oscillation directions due to a slightly different oscillating mass (see Figure 2.19). It should be kept in mind that fabrication processes can alter significantly the spring shape, especially by thinning the width of the beams (see Chapter 3). Therefore, lower resonance frequencies are expected in practice.

Simulated values can be compared to theoretical predictions. A single spring is modeled as two cantilever beams in parallel: l is the spring length, t the out-of-plane thickness, and w the width. Then for a load in the $l-t$ plane:

$$k = \frac{Etw^3}{4l^3} \tag{2.53}$$

where E is Young's modulus for the spring material (crystalline silicon). Since one spring is modeled as two cantilever beams in parallel and there are four such springs in parallel for each

Beam length	l	$2.9mm$
Beam in-plane width	w	40μm
Beam out-of-plane thickness	t	variable
Young's modulus for silicon	E	170GPa
Proof mass	m	5.9×10^{-5} Kg

Table 2.3: Parameters used to solve Eq.(2.54).

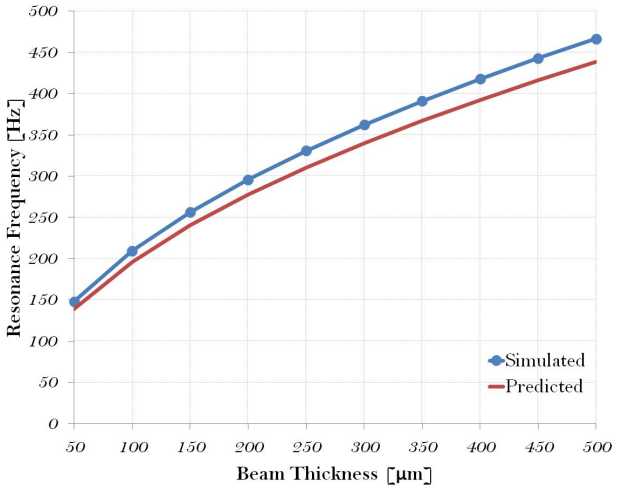


Figure 2.20: Simulated resonant frequencies for different out-of-plane beam thickness t

vibration direction, one can write for the resonance frequency:

$$f_o = \frac{1}{2\pi}\sqrt{\frac{k_{eff}}{m}} = \frac{1}{2\pi}\sqrt{\frac{8k_{eff}}{m}} \tag{2.54}$$

where m is the proof mass and $k_{eff} = 8k$ is the effective spring constant given by 8 cantilever beams in parallel. With the parameters given in Table 2.3, simulated resonant frequencies are plotted in Figure 2.20 for a few values of t, together with the $f_o(t)$ curve predicted by Eq. 2.54. The results are reasonably close and confirm that Eq. 2.53 can be used to predict resonance frequencies as a first approximation. Also the expected relation $f_o \propto \sqrt{t}$ seems to be confirmed by the simulations.

2.5 Coupled Electromechanical System

In this section the mechanical vibration of the proof mass is coupled to the electrical domain, meaning that a new force F_{el} is added to the mechanical system to account for the work done by the vibration source against the in-plane electrical forces in order to convert vibrational energy into electrical energy. The vibration source motion is assumed to be unaffected by the loss of energy due to harvesting, i.e. its total vibrational power is much higher than the harvested power.

2.5.1 In-Plane Electrical Force Analysis

The work done by the vibration source in the electrical domain can be written in a differential form according to the First Law of Thermodynamics:

$$dW_s = -dU_s = dE_h + dU_{el} \tag{2.55}$$

where dU_s is the change in internal energy for the source, dE_h is the *irreversible* energy loss due to dissipation in the load resistance, and dU_{el} is the *reversible* change in the total electrical energy stored in the device equivalent capacitance. dE_h is found from the expression of harvested power as

$$dE_h = P_h(t)\,dt = R\left(\frac{dQ}{dt}\right)^2 dt \tag{2.56}$$

while dU_{el} is found by first calculating the sum of electrostatic energies stored in the 4 capacitors of the system C_{d1}, C_{d2}, C_{g1}, and C_{g2}

$$U_{el} = \sum_{i,j} \frac{1}{2} \frac{Q_{ij}^2}{C_{ij}} \tag{2.57}$$

and then differentiating:

$$dU_{el} = \sum_{i,j} \frac{Q_{ij}}{C_{ij}} \, dQ_{ij} \tag{2.58}$$

To provide such work, the source has to exert a force F_s against the in-plane electrical force F_{el}:

$$\begin{aligned} F_s = \frac{dW_s}{dx} = \frac{dE_h}{dx} + \frac{dU_{el}}{dx} = \frac{P_h \, dt}{dx} + \frac{dU_{el}}{dt} \frac{dt}{dx} = \\ = \left(P_h + \frac{dU_{el}}{dt} \right) \frac{dt}{dx} = \left(P_h + \frac{dU_{el}}{dt} \right) \frac{1}{\dot{x}} = -F_{el} \end{aligned} \tag{2.59}$$

where only motion in the z-direction is assumed. Therefore for the in-plane electrical force:

$$F_{el} = -\left(P_h + \frac{dU_{el}}{dt} \right) \frac{1}{\dot{x}} = -\left(R \left(\dot{Q} \right)^2 + \sum_{i,j} \frac{Q_{ij}}{C_{ij}} \dot{Q}_{ij} \right) \frac{1}{\dot{x}} \tag{2.60}$$

Now the equation of motion for the electret pattern can be finally rewritten including F_{el} as

$$F_{net} = m\ddot{x} = F_{ext} + F_k + F_{el} \tag{2.61}$$

where all forces are to be interpreted as in Section 2.4. As mentioned before, W_s is assumed to be much smaller than the vibrational energy of the source so that F_{ext} is unaffected by the power loss in the source due to harvesting. Viscous damping due to air resistance, structural damping, and other forms of parasitic damping have been neglected as they are difficult to estimate without supporting experiments. Based on the analysis of [28], such a damping force is expected to be much smaller than the electrical force on the system, so it should not have an appreciable impact on the solution.

2.5.2 Coupled Equations

If the rest position for the elastic force F_k, i.e. $x = 0$, is again chosen at a point where the electret lies exactly in the middle between counter electrodes 1 and 2, the time-dependent area overlap is:

$$A(t) = \frac{A_0}{2} + w \, x(t) \tag{2.62}$$

If this expression is plugged into Eq. (2.35), a modified electrical equation is found that leaves A(t) as a degree of freedom instead of imposing it. Together with the mechanical equation provided by Eq. (2.61), it forms a set of coupled differential equations. They can be written in a compact form as a function of differential variables $Q(t)$ and $x(t)$:

$$\begin{cases} m\ddot{x} = F_{ext} + F_k(x) + F_{el}(Q, \dot{Q}, \dot{x}) & \text{(equation of motion)} \\ R\dot{Q} = V_C(Q, x) & \text{(Kirchhoff's law)} \end{cases} \tag{2.63}$$

where $V_C = V_{g2} - V_{d2} + V_{d1} - V_{g1}$ is the sum of voltage drops across the 4 capacitors in the system.

Air gap	g	$100\mu m$
Electret thickness	d	$10\mu m$
Electret length and width	w	$200\mu m$
Number of electret cells in one device	n	450
Proof mass	m	5.9×10^{-5} Kg
Driving frequency	f	200Hz
Spring system resonance frequency	f_o	200Hz
Electret surface charge density	σ_d	3.54×10^{-4} C
Load resistance	R	$1\,G\Omega$
Electret relative permittivity	ε_d	2

Table 2.4: Parameters used to solve Eq.(2.63). The driving force amplitude F_0 is left as a free parameter.

This is a set of second-order coupled ODEs with two variables: $Q(t)$ and $x(t)$. In order to search for a solution, three initial conditions must be given, such as:

$$\begin{cases} x(0) = 0 \\ \dot{x}(0) = 0 \\ Q(0) = \dfrac{nA_0}{2}\sigma_{c0} \end{cases} \tag{2.64}$$

so that initially the system is at rest position with zero velocity, and the charge on counter electrode 1 is simply given by the static condition found in Eq. (2.25). Parameters are chosen so that a *resonant* system is achieved, meaning the driving frequency f is set to be equal to the resonance frequency f_o of the spring system. A full list of parameters is given in Table 2.4.

2.5.3 Results

The Mathematica algorithm *NDSolve* is used to solve the coupled equations. The driving force amplitude parameter F_0 is swept until a solution for $x(t)$ is found that resembles the solution of Eq. (2.35) for the electrical domain with fixed oscillation. A value of $F_0 = 1.4 \times 10^{-4}$ N, corresponding to a driving acceleration amplitude of 0.24 g, yields a displacement amplitude $X_a \simeq 50\mu m$ which is about $w/4$ as assumed in the electrical model developed in Section 2.3. The maximum oscillation amplitude allowed by the designed spring system is about $230\mu m$, but the proposed model does not allow to find a solution for $X_a > w/2 = 100\mu m$ because of how

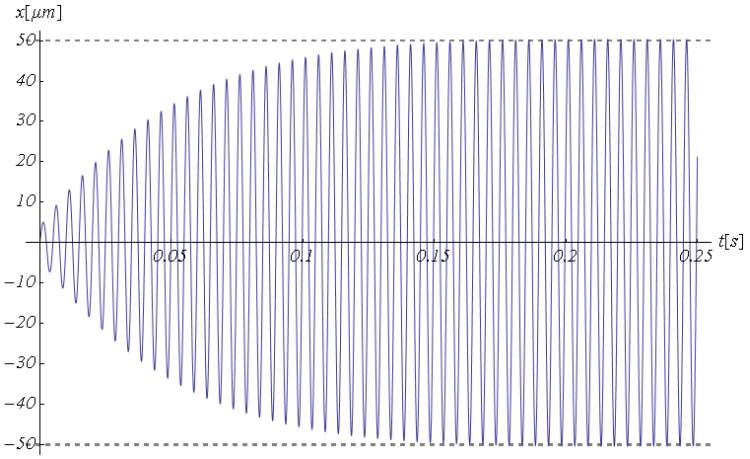


Figure 2.21: Evolution of mechanical oscillation in fully coupled system. Solution for $x(t)$ in coupled equations (2.63) with boundary conditions given by Eq. (2.64)

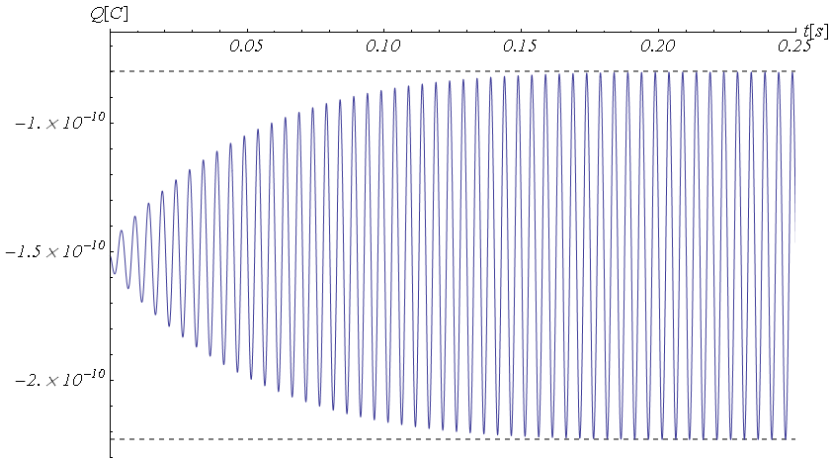


Figure 2.22: Evolution of electrical charge on counter electrodes 1 in fully coupled system. Solution for $Q(t)$ in coupled equations (2.63) with boundary conditions given by Eq. (2.64)

the overlap area is defined. Redefinition of $A(t)$ is necessary to allow for electret overlap with counter electrodes in a different cell. This will be done in Section 2.5.4.

It is seen from Figure 2.21 that, after a transient behavior due to initial conditions, the mechanical oscillation $x(t)$ stabilizes at an amplitude $X_a \simeq 50\mu m$. A similar trend is observed for charge oscillation $Q(t)$ (see Figure 2.22). Charge on counter electrodes 1 seems to stabilize at a constant amplitude $Q_a \simeq 7 \times 10^{-11}\, C$ around an average value of approximately $nA_0/2\sigma_{c0} = 1.5\ 10^{-10}$, as expected from parameter choice. Moreover, the proof mass oscillation $x(t)$ is observed to be delayed by about $\pi/2$ with respect to the driving force $F_{ext}(t)$. All results shown from now on refer to a time span located well after the end of the transient, so that an oscillation with constant amplitude can be assumed. An interesting result is immediately available from Figure 2.23. The electrical force with reverse sign $-F_{el}(t)$, defined by Eq. (2.60), is plotted together with electric current $I(t)$ and vibration velocity $v(t)$ in a normalized graph. The electrical force signal follows the current signal very closely, so a proportionality between the two can be inferred:

$$F_{el}(t) = -cI(t) \tag{2.65}$$

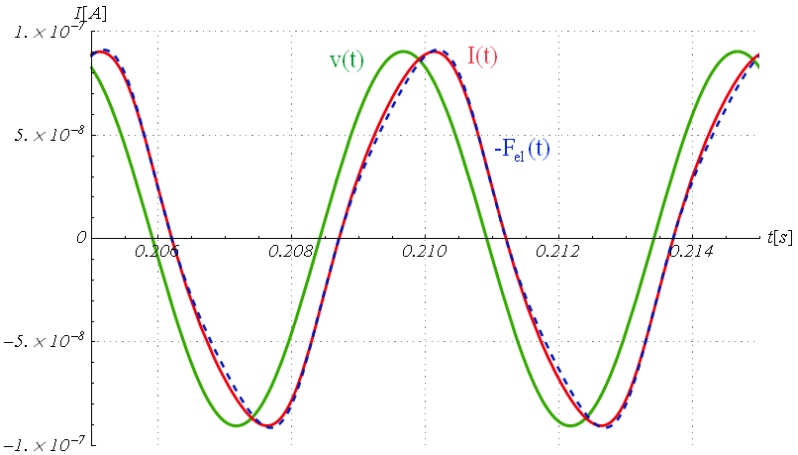


Figure 2.23: *Red*: electrical current signal as the derivative of $Q(t)$ found by solving Eq.(2.63). *Green*: normalized plot of mechanical oscillation velocity as the derivative of $x(t)$. *Dashed blue*: normalized plot of electrical force $-F_{el}(t)$ given by Eq.(2.60).

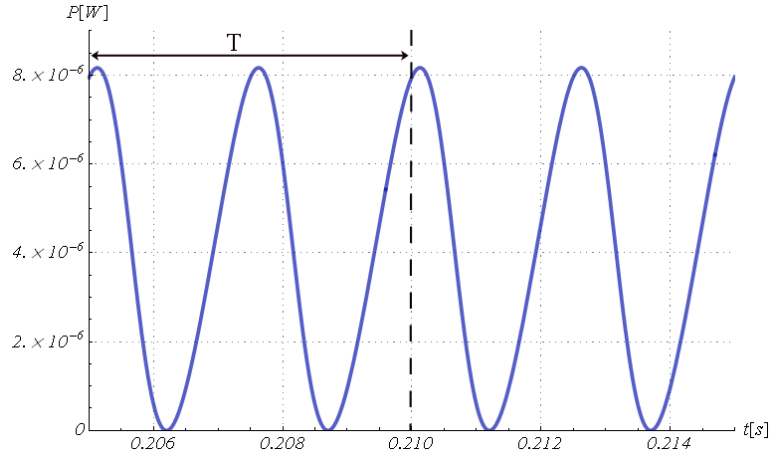


Figure 2.24: Harvested power signal in fully coupled system (calculated with Eq. (2.42))

where c is a positive constant. The value of c must depend on the device parameters, so parametric studies on the system equations are needed in order to understand such dependance. It is also observed that the current signal is slightly distorted with respect to an ideal sine function. The phase shift between $v(t)$ and $I(t)$ is calculated from fitting functions to be around $\frac{\pi}{5}$, similarly to the uncoupled case (see Section 2.3.4). A plot of harvested power, calculated with Eq. (2.42), is shown in Figure 2.24. If the signal is integrated over a few periods and divided by the integration length the equivalent RMS power is found:

$$P_{h,rms} = \frac{1}{T_2 - T_1} \int_{T_1}^{T_2} P_h \, dt \simeq 4\mu W \tag{2.66}$$

as expected from a squared sine function with amplitude $8\mu W$. If the area of the $Q - V_R$ hysteresis loop in Figure 2.25 is calculated approximately to find the harvested energy in one period, one gets a very similar result for $P_{h,rms}$ of about $4\mu W$. In Figure 2.25 the hysteresis loop for the coupled system is compared to the loop produced by an ideal harmonic oscillation of charge. It is inferred that distortion of electrical signals from harmonic behavior leads to

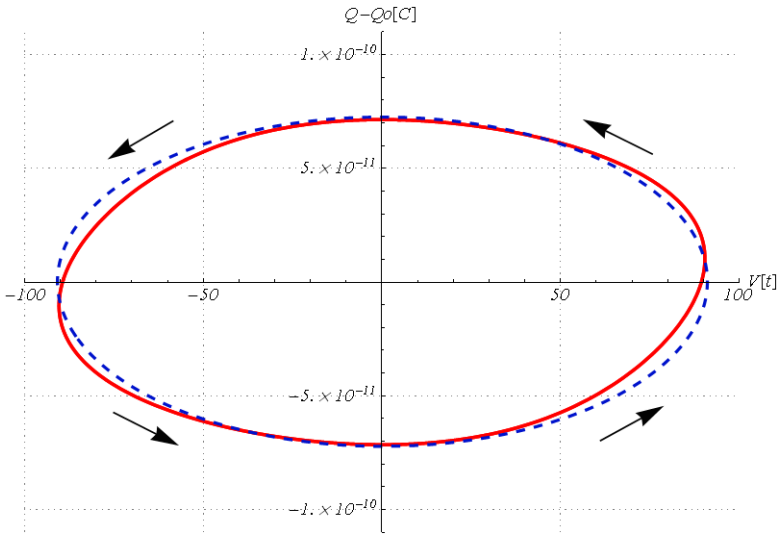


Figure 2.25: Hysteresis loop for charge displacement versus voltage drop across load resistance. *Red*: coupled system described by Eq. (2.63). *Dashed blue*: system with harmonic charge oscillation.

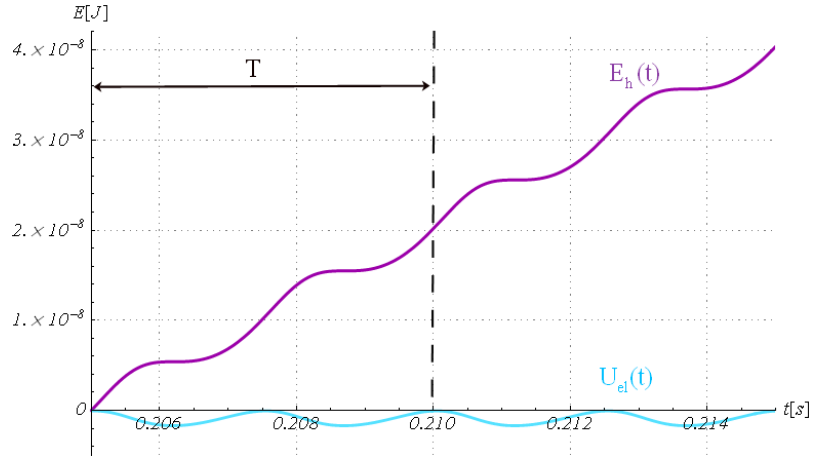


Figure 2.26: *Purple*: harvested energy as the time integral of harvested power. *Blue*: sum of potential energies stored in the device capacitors, given by Eq. (2.57).

deviation of the hysteresis loop from an elliptical shape.

Figure 2.26 shows the time behavior of harvested energy $E_h(t)$ and stored potential energy $U_{el}(t)$. As discussed in Section 2.5.1, all harvested energy is taken irreversibly out of the system so $dE_h/dt = P_h \geq 0 \, \forall t$ and the harvested energy function is therefore growing. On the other hand, $U_{el}(t)$ is associated to a periodic "bouncing" of the system between states at different potential energy. This energy transfer is reversible as the system moves back periodically to the same configuration, so there is no net transfer of energy to or from the system over one period.

2.5.4 Correction with Simulated Capacitance

A more accurate solution is now presented that includes an evaluation of fringing fields, responsible for a decrease in "contrast" between regions 1 and 2 in Figure 2.11. A FEM analysis with COMSOL Multiphysics is employed to find more realistic values for device capacitances at different area overlaps. The goal is similar to what has been shown in [25], but the simulation is carried out in a different way. In the 2D model shown in Figure 2.27, electrets are directly on top of a grounded surface and their top surfaces are set to have a constant surface charge density σ_d given by Table 2.4. The counter electrode pattern is also grounded to simulate the static fields discussed in Section 2.3.2.

The overlap between the two patterns is swept for a length of 250μm in 10μm steps in order to have a reasonable sampling of overlap states. Here a spacing of $s = 50\mu$m between counter electrodes is included to simulate a realistic device. The induced surface charge density function $\sigma_c(x)$ on one of the counter electrodes is integrated over the electret length w and multiplied by the electret width w, yielding the simulated charge on one counter electrode Q_{c1} for different overlaps:

$$Q_{c1}(x) = \sigma_{c,av} w \, x = w \int_0^w \sigma_c(x) \, dx \tag{2.67}$$

where $\sigma_{c,av}$ is an equivalent surface charge density given by the integral average of FEM charge density values over the electret length w.

With this information the capacitance between one electret and one counter electrode, equivalent for example to C_{g1} from Section 2.3.2, can be calculated as $C_{g1}(x) = Q_{c1}(x)/V_S$, where V_S is the electret surface potential given by Eq. (2.15). The results are plotted in Figure 2.28 in comparison with the capacitance predicted by Eq. (2.27) which has been used so far in this model. It is evident that the simulated capacitance function does not reach 0 at zero overlap

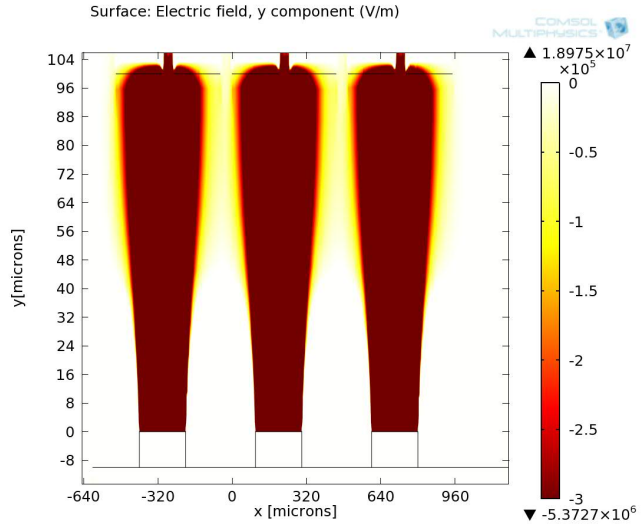


Figure 2.27: Static out-of-plane component of the electric field between electrets and counter electrodes as a result of FEM analysis. The picture is not to scale.

as is expected from a plane capacitor model. Instead, it oscillates between a minimum and a maximum value which are closer together than in the ideal case. The ratio between these two values is about 6. The simulated C_{g1} function can be fitted very well to a sinusoidal function like

$$C_{eff}(x) = \frac{C_{max} + C_{min}}{2} + \left(\frac{C_{max} - C_{min}}{2}\right) \sin\left(\frac{2\pi}{\lambda}x + \chi\right) \tag{2.68}$$

where C_{max} and C_{min} are the extrema of the simulated capacitance function, $\lambda = 2(w + s)$ is the spatial period of capacitance oscillation, and χ is a phase term that describes the overlap condition at $x = 0$. If $\chi = 0$ the overlap at rest is at its average value, i.e. the electret is located exactly in the middle between counter electrodes 1 and 2 (see Figure 2.14) as it was assumed in the previous sections. If $\chi = \pi/2$ there is full overlap between the electret and counter electrode 1, whereas $\chi = -\pi/2$ is the lowest-overlap configuration as the electret is at full overlap with counter electrode 2.

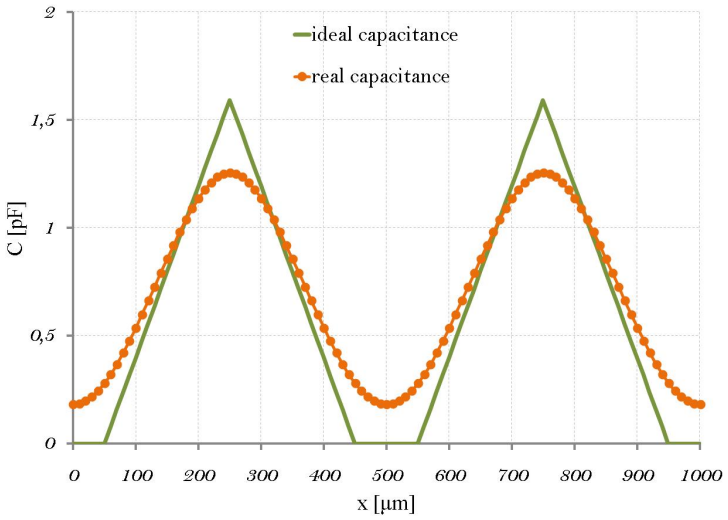


Figure 2.28: Ideal $C_{g1}(x)$ calculated with Eq. 2.27 versus FEM-simulated $C_{g1}(x)$

An effective overlap area function $A_{eff}(x)$ can be defined from this analysis as:

$$A_{eff}(x) = \frac{g\, C_{eff}(x)}{\varepsilon_0} \tag{2.69}$$

An effective full-overlap area can also be defined in a similar fashion as:

$$A_{0,eff} = \frac{g\,(C_{max} + C_{min})}{\varepsilon_0} \tag{2.70}$$

If these two relations are used instead of Eq. (2.62) to solve the coupled equations, new results are obtained. First of all, it is now possible to drive the proof mass oscillation to any displacement without the model losing validity. In the following analysis, F_{ext} will be tuned to yield a steady-state oscillation amplitude of about 230μm, which is the maximum displacement from equilibrium allowed by the our device design (see Section 3.2). Under such conditions, the system equations are solved for two different values of χ: 0 and $\pi/2$ (see Figure 2.29).

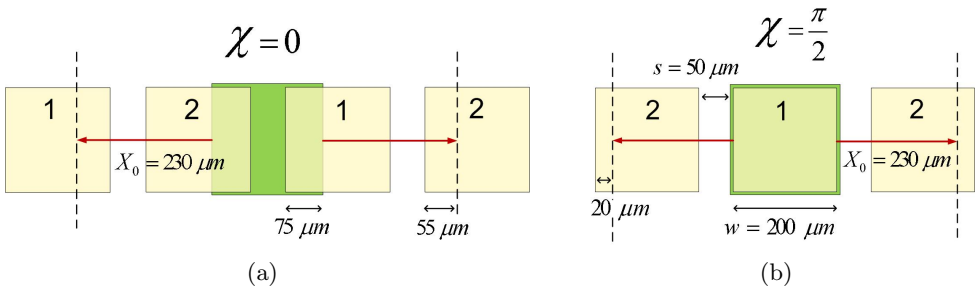
For $\chi = \pi/2$ (full initial overlap) charge is observed to oscillate at twice the frequency of the proof mass (Figure 2.30(a)). This is because, with reference to Figure 2.29(b), the electret moves between three different counter electrodes so that charge is induced on 2, 1, and 2 again during half a period. Charge oscillation has a peak-to-peak amplitude $1.8 \times 10^{-10}\, C$. The electric current signal is plotted in Figure 2.30(b) and is qualitatively compared to the proof mass velocity v and the in-plane electrical force F_{el}. Close inspection reveals that the force is approximately proportional to the current but is modulated by the velocity. The result is that its direction opposes the direction of motion almost at all times. An approximate analytical expression is proposed for the force as:

$$F_{el}(t) = -c\,|I(t)|\,\mathrm{Sign}[v(t)] \tag{2.71}$$

where c is a positive constant, $\mathrm{Sign}[v(t)]$ is the sign of the velocity function, and $|I(t)|$ is the absolute value of the current function.

For $\chi = 0$ (half initial overlap) charge has a much different behavior. Referring again to Figure 2.29(a), near proof mass oscillation extrema charge is only partially moved from 1 to 2 because only a small overlap with counter electrodes 2 is reached. Therefore sub-peaks appear in the charge function in Figure 2.30(c). From this graph it is easier to see an overall phase shift of $Q(t)$ with respect to $x(t)$. The graph in Figure 2.30(d) confirms that even in case of half initial overlap the behavior of F_{el} is consistent with its proposed analytical expression (2.71).

In Figure 2.31 hysteresis cycles are plotted for $\chi = 0$ and $\chi = \pi/2$. It is interesting to notice that for $\chi = 0$ there are actually two sub-cycles in which work is done *by the harvester* on the vibration source. Figure 2.32 finally shows the harvested power as a function of time for the



(a) (b)

Figure 2.29: Device top view, emphasizing overlap range for an oscillation of amplitude 230μm Counter electrodes 1 and 2 are drawn in yellow and are spaced by s; electret is drawn in green. (a): $\chi = 0$. (b): $\chi = \pi/2$.

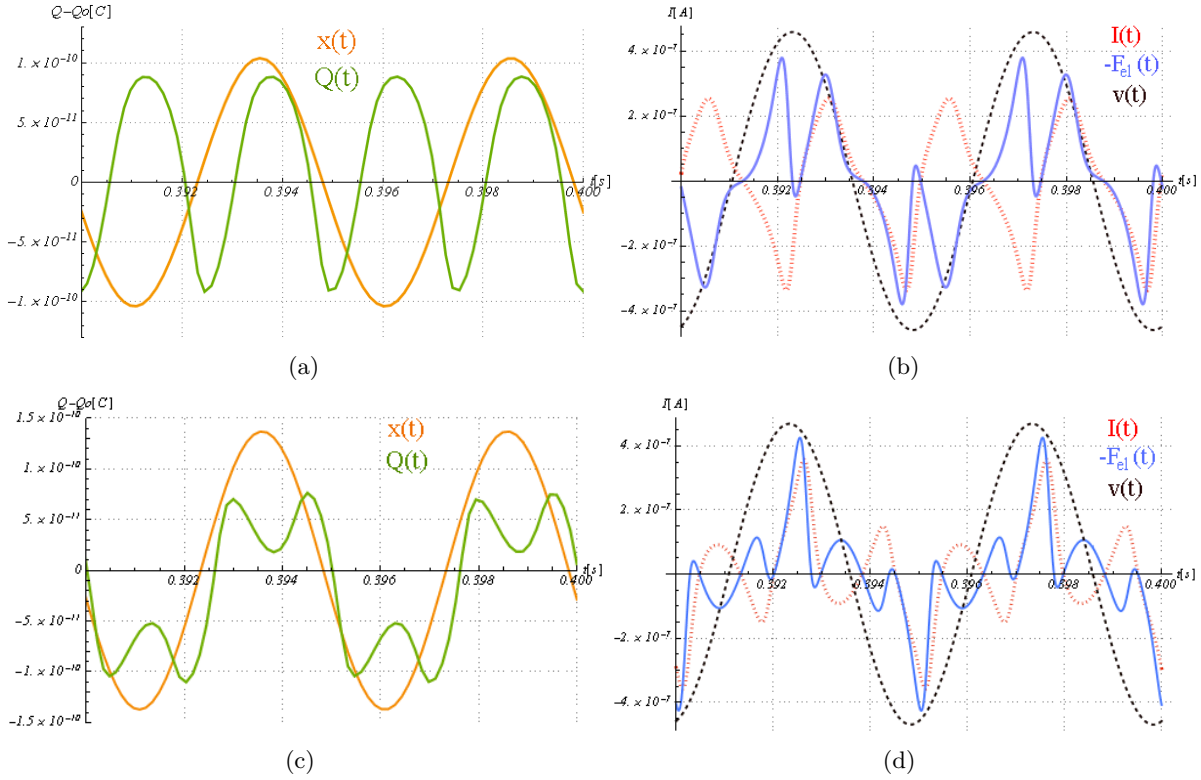


Figure 2.30: Electrical signals (charge and current) compared to proof mass oscillation properties (displacement and velocity). (a) and (b): $\chi = \pi/2$. (c) and (d): $\chi = 0$

two initial overlap configurations, calculated with Eq. (2.42). Using Eq. (2.66), RMS power is calculated to be 30μW for $\chi = \pi/2$, and 22μW for $\chi = 0$.

The conclusion is that, if other parameters are kept constant, a full initial overlap should yield a higher RMS power, whereas an initial displacement between electret and counter electrode patterns should produce higher power peaks. If the coupled equations are solved for different values of the load resistance, and F_{ext} is tuned each time to yield a steady-state oscillation amplitude of 230μm, a graph of output RMS power versus external load is obtained (Figure 2.33).

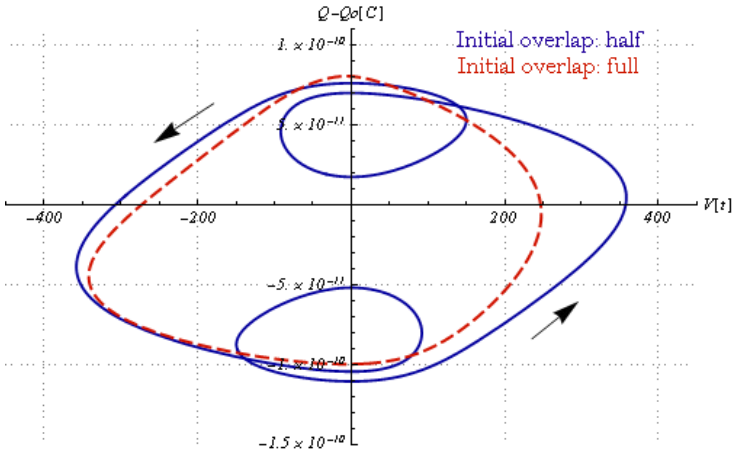


Figure 2.31: Hysteresis loop for charge displacement versus voltage drop across load resistance for $\chi = \pi/2$ and $\chi = 0$

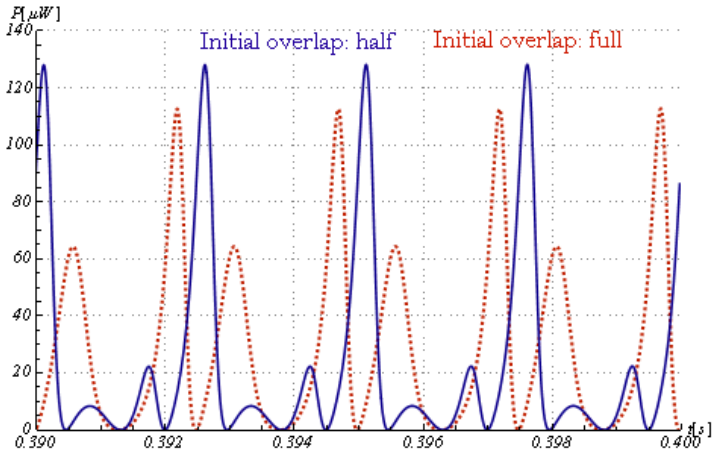


Figure 2.32: Output power signal for full initial overlap ($\chi = \pi/2$) and half initial overlap ($\chi = 0$)

An optimal load $R_{opt} \simeq 2\,\mathrm{G\Omega}$ maximizes output power to $36\mu\mathrm{W}$ under a source acceleration amplitude of 0.50 g. This is in reasonable agreement with the value $1.05\,\mathrm{G\Omega}$ found with Eq. 2.39 with reference to [11]. By knowing the optimal load, it is possible to define an equivalent harvester's capacitance C_h from the load-matching condition:

$$\frac{1}{2\pi f C_h} = R_{opt} \tag{2.72}$$

The equivalent capacitance for the device is thus $C_h = 0.4\,\mathrm{pF}$.
It should be noted that external loads involved in our discussion so far are extremely high. As will be shown in Chapter 4, test implementation is difficult under such conditions as parasitic effects become significant.

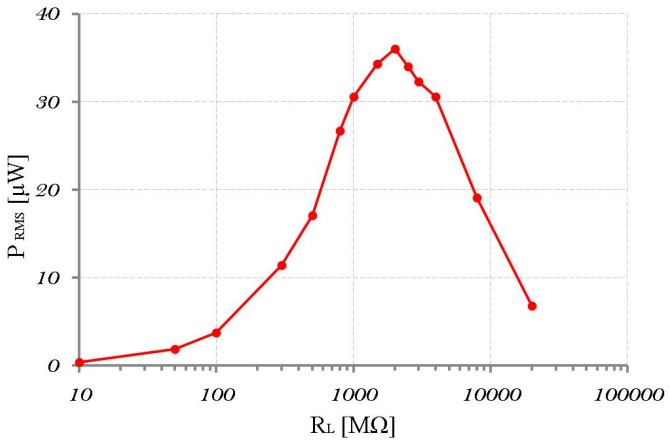


Figure 2.33: Theoretical prediction for RMS harvested power versus external load assuming full initial overlap ($\chi = \pi/2$).

Chapter 3

Design and Fabrication

In this chapter, all processes involved in the fabrication of the energy harvester are presented one by one. It was decided to merge design and fabrication topics into one chapter because design choices are easier to justify if their effect is immediately seen in actual fabrication processes and pictures. A general overview of the whole process flow is provided in Section 3.2, followed by a more in-depth discussion of each process step. All steps can be easily visualized in Appendix B, where a schematic cross-sectional view of the processed wafer is provided for each step.
Because no devices had been successfully fabricated prior to this batch, the general philosophy behind design choices was to maximize device yield. Parameters were chosen following robust design considerations, and parameter optimization for maximum energy output was a secondary concern.

Fabrication involves processing of four different substrates, which are bonded together at different stages of the process flow. Our presentation follows this trend by assigning a different section to each kind of wafer (Sections 3.3, 3.4, 3.5, 3.6). Step numbering reflects the layout of Appendix B. Additional sections cover corona charging of electrets (3.7) and wafer dicing (3.8).

Throughout this chapter, reference will be made to specialized equipment. An equipment list, together with a brief feature description, can be found in Appendix C. For more details on equipment parameters and recipes, see Appendixes B and C.

3.1 Introduction to MEMS Fabrication

In the 1960s, the invention of the planar batch-fabrication process for semiconductor devices proved to be a major technological breakthrough. It enabled multiple electronic devices, circuits, and chips to be integrated onto a single silicon substrate (a "wafer") and processed simultaneously with high reliability and low cost. The Integrated Circuit (IC) industry was born.

Soon thereafter, it became clear that such a technology could be applied to more than just electronics. In particular, Petersen [29] pointed out the excellent mechanical properties of silicon, by far the most popular semiconducting material in the electronics industry. Today, the acronym MEMS (MicroElectroMechanical Systems) refers to a wide variety of devices with micrometer-sized structures. Their working principle is typically the coupling between different physical domains (electrical, mechanical, magnetic, thermal, and chemical to name a few). Processes and materials employed for MEMS fabrication are partially borrowed from conventional IC technology, but many additional MEMS-specific techniques have been developed over the years. Most notably, starting from the 1990s bulk micromachining and wafer bonding processes have finally given MEMS devices significant access to the third dimension, by allowing complex geometrical structures to be defined in the out-of-plane direction [30].

So far, the greatest commercial success has been achieved by microsensors (namely accelerometers and pressure sensors) but the diversity of MEMS technologies and applications is growing tremendously. Fabricated devices range from biochemical sensors for *in vitro* medical diagnostics, to magnetic microactuators for optical components, to micromachined fluidic channels for DNA analysis, to micro energy harvesters.

3.2 Process Flow Overview

The process flow which has led to the first successfully fabricated batch involves separate fabrication of four different types of wafers, which are then bonded together and diced to yield 44 devices/wafer. All process steps (with the possible exception of corona charging) involve standard MEMS manufacturing techniques and are carried out at a full-wafer level. Therefore, an optimized version of this process flow could be employed in large scale production of micro energy harvesters.
The purpose of each type of wafer is presented in Table 3.1.

Type	Material	Purpose
Cap Wafer	silicon	protects critical parts (i.e. springs and electrets) from water leakage
Device Wafer	silicon	contains proof mass, spring system, and electret pattern
Spacing Wafer	silicon	defines the air gap thickness between electret and counter electrode patterns
Glass Wafer	fused silica	contains the counter electrode pattern, ending up in two conductive terminals where the external load can be connected

Table 3.1: Purpose of the four processed wafers in the energy harvesting device

Conventional microfabrication materials have been used such as silicon, silicon-based insulators, fused silica, aluminum, gold, and chromium. The electret material of choice for our harvester is CYTOP (Cyclic Transparent Optical Polymer), manufactured by Asahi Glass Co., Japan. It is an amorphous non-polar fluoropolymer with a glass transition temperature of 108°C [18]. Its advantageous properties include a very low conductivity of less than $10^{-17}\ \Omega^{-1}cm^{-1}$ and a high dielectric strength with an internal breakdown voltage of 10 kV for a $100\mu m$ thickness [18]. Although not a standard microfabrication material, CYTOP is fully MEMS-compatible: it is commercially available in the form of a diluted solution that can be easily spun onto a

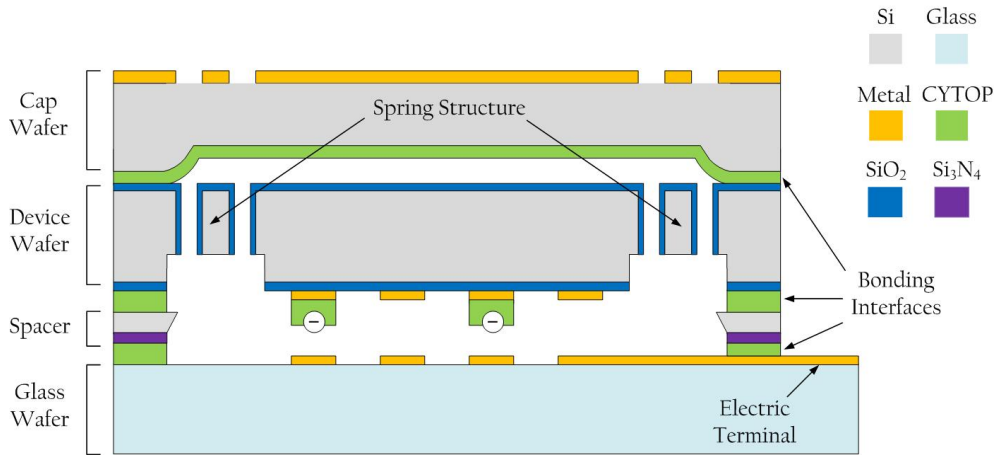


Figure 3.1: Schematic cross-sectional view of completed device

wafer multiple times with a spin-coating tool, resulting in thin layers with $1 - 20\mu m$ thickness. The film can then be patterned using Reactive Ion Etching with a photoresist mask. CYTOP can also be used in full-wafer bonding techniques as an adhesive interface material between the surfaces to be bonded.

The following list summarizes fabrication key points:

1. the area of a single device is 10mm×11mm, with an out-of plane thickness of about 1.5mm.

2. springs are made of silicon with a SiO_2 coating (D7) for protection against unwanted etching. They allow a maximum peak-to-peak proof mass oscillation amplitude of 460μm.

3. the out-of plane spring thickness is defined by a tunable Deep Reactive Ion Etching (DRIE) process from the front side (step D6). Springs remain unreleased until the end of the process flow, when another DRIE process from the backside removes all unetched silicon beneath the pre-etched springs (step D19).

4. to optimize the first DRIE process (step D6), dummy structures are drawn on the etching mask in order to obtain a constant width of 50μm for etched trenches throughout the wafer (see Figure 3.6(c)). Increased etch rate uniformity is expected with this technique [31].

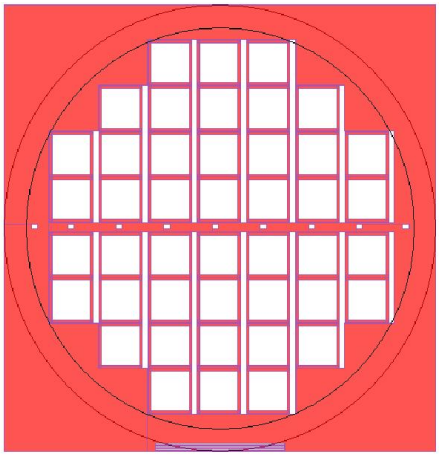
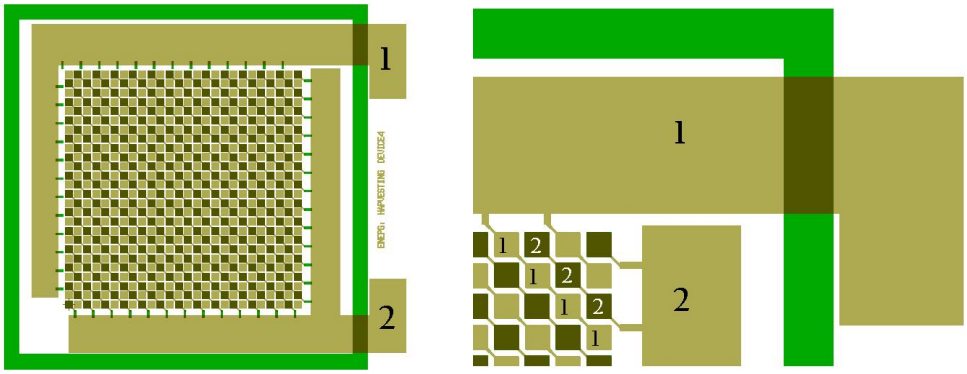


Figure 3.2: Full-wafer view of one of the 5-inch photomasks. 44 independent chips (10mm×11mm) can be obtained from a 4-inch wafer placed as in the picture.



(a) (b)

Figure 3.3: (a): Top view of some features on a sample device. *Gold*: Counter electrode pattern with terminal pads 1 and 2 (Glass_ Electrode mask). *Green*: electret pattern and bonding frame (Si_Polymer mask).
(b): Zoomed-in view, showing how equivalent counter electrodes are connected to the same terminal pad. Dark electrodes fully overlap with an electret in their equilibrium position. Light electrodes have no electret overlap.

Dummy structures can be easily removed in an ultrasonic bath when springs are finally released.

5. CYTOP is employed both as an electret material and as a "glue" for wafer bonding processes. In both cases, it is patterned by Reactive Ion Etching (RIE) with a photoresist mask. Bonding frame width is 500μm.

6. the electret-to-counter-electrode air gap is roughly equal to the spacing wafer thickness after processing, which is fully tunable.

7. Geometrically equivalent counter electrodes are connected together. With reference to Section 2.3.1, this means that all counter electrodes 1 are connected to terminal 1 and all counter electrodes 2 are connected to terminal 2. See also Figures 2.10 and 3.3.

3.3 Cap Wafer

Substrate thickness is relatively unimportant for the protective cap wafer, so a 350μm-thick blank silicon wafer is chosen as a starting point. Silicon doping is irrelevant as the cap wafer has no electrical function.

C1: The blank substrate is oxidized in a furnace for 50 minutes at 1100°C and then annealed for 20 minutes. A 500nm-thick layer of silicon dioxide is thus grown on both sides of the substrate. A wet process is chosen due to the relatively large SiO_2 thickness required. The oxide layer will serve as a mask for a later KOH etching step (C6).

C2: The oxidized wafer is primed in hexamethyldisilazane vapor (HMDS) for 5 minutes to promote photoresist adhesion. Shortly after HMDS coating, photoresist is spun by an automatic spinner on the wafer's top side to achieve a uniform film of 2.2μm thickness. A contact softbake at 90°C is performed for 90 seconds. The procedure is repeated on the bottom side, but this time a proximity softbake at 95°C is employed to avoid damage to the previously spun resist film.

C3: A 9-second UV exposure is performed on the bottom side, using the Si_Cap mask (Figure 3.4). A wet immersion development is carried out for 75 seconds, resulting in a resist pattern that follows the device bonding frames.

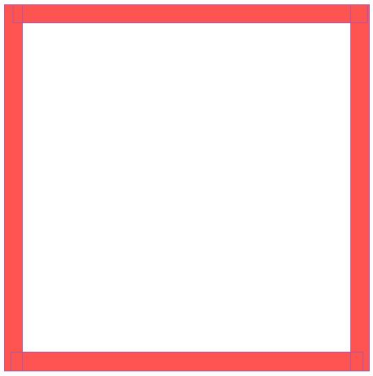


Figure 3.4: Single-device top view of Si_Cap mask. Patterned areas are the device's bonding frames (10mm×10mm).

C4: The wafer is dipped into a bHF solution for 8 minutes, with patterned resist acting as an etching mask. As a result, SiO_2 is selectively removed from the wafer bottom side, leaving the silicon surface exposed. The unpatterned resist layer prevents any etching of the top side.

C5: Photoresist is stripped in a plasma asher, using a standard recipe.

C6: A KOH etching step is performed to remove silicon from the bottom side. The target etch depth should be roughly equal to the desired proof-mass-to-cap-wafer distance. In the design phase this distance was chosen to be around 20μm (15-minute etch), to achieve a reasonable compromise between two conflicting requirements:

1. etching should be shallow enough to achieve an acceptable uniformity in the CYTOP spin-coated film that will be used for bonding (C13). Note that this would no longer be an issue if a spray-coating tool was available.

2. etching should be deep enough to make contact between proof mass and cap wafer unlikely. This has been proven to be an issue for the fabricated devices (D21).

C7: Another 8-minute bHF etch removes all SiO_2 from the wafer, leaving the silicon surface exposed everywhere.

C8: A quick KOH dip (30 seconds) has the purpose of rounding off the sidewall corners from the previous KOH etch. This step should facilitate CYTOP diffusion onto the bonding frames during the spin-coating process.

C9,C10,C11,C12: 50nm of aluminum is evaporated on the wafer's top side. A standard lithography process involving the Si_ Top_Etch mask is carried out in order to pattern the aluminum layer using a wet etchant. The mask is aligned front-to-back with the Si_Cap pattern. The patterned aluminum layer is needed to locate the correct cutting lines during dicing. Photoresist is stripped afterwards.

C13: CYTOP solution is spun onto the wafer at 800rpm for 30 seconds using a manual spinner. The CYTOP layer is baked for 10 minutes at 120°C shortly afterwards. The coating/baking process is done twice in an identical way, yielding a polymer thickness of about 4μm in the flat regions of the wafer. On top of the bonding frames the CYTOP layer is probably thinner because of the spin-coating obstacle given by surface topography (see Figure 3.5). No hardbake is applied as a small amount of remaining solvent should improve bonding [11]. It has been shown in [11] that similar polymer thickness results in satisfactory bonding strength and yield. CYTOP doesn't need to be removed from the rest of the device area as long as it is not designed to contact with any moving part. The cap wafer is now ready for bonding.

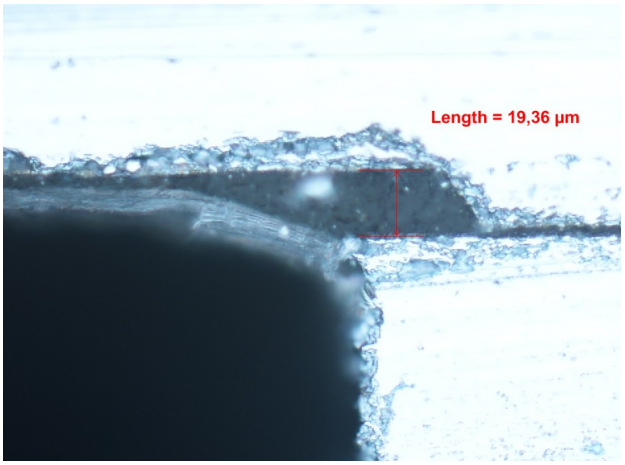


Figure 3.5: Cross-sectional view of bonding frames sidewalls on a completed device. The cap-device wafer bonding interface is seen on the right. CYTOP is the darker material in this optical microscope picture. Polymer accumulation is evident at the step base.

3.4 Device Wafer

Substrate thickness is a critical matter for the device wafer as it affects proof mass and spring thickness. Since modeling of similar devices has proven that output power increases linearly with proof mass [27, 28], a 500μm-thick blank silicon wafer is chosen in order to have a reasonably large mass. The only electrical function of the silicon substrate is to provide a ground reference during electret charging for implanted charge measurement. Hence, the substrate needs to be (p- or n-) doped enough to have a low electrical resistance. Standard wafers available at our facilities have a resistivity of $10^{-1}\,\Omega\,\mathrm{m}$, which should be adequate for the purpose (see also Section 2.2).

D1: The blank substrate is oxidized in a furnace for 10 hours at 1100°C and then annealed for 20 minutes. A 2μm-thick layer of silicon dioxide is thus grown on both sides of the substrate. Since a thick film is needed, a wet process is again chosen to reduce process time. A thick SiO_2 layer is required to mask the substrate when springs are defined by means of a deep DRIE process (D6). Also, a SiO_2 etching step (D8) will be employed to remove a newly-grown thinner oxide layer (D7), so the present layer needs to be considerably thicker to prevent through-etching.

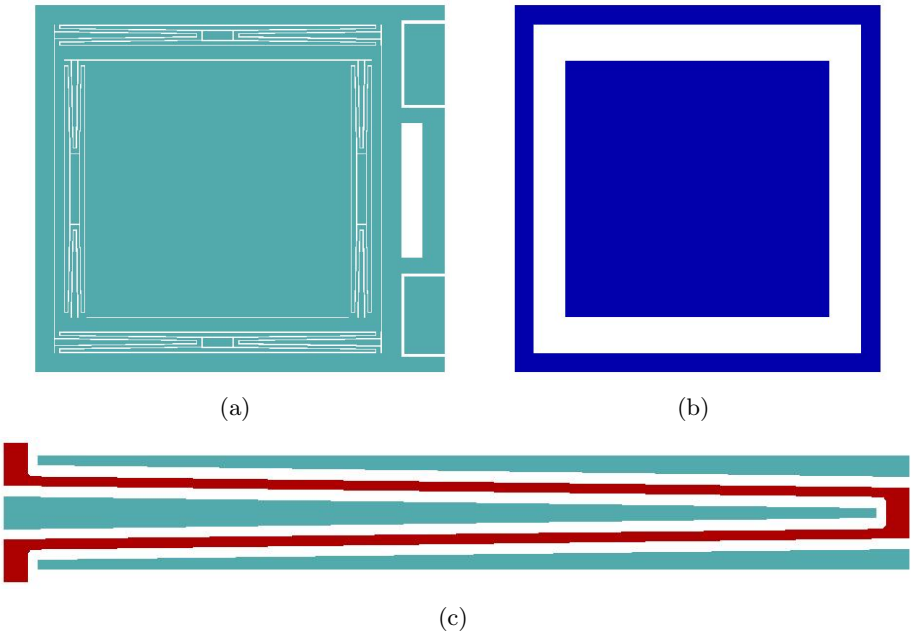
D2: After an HMDS treatment, 2.2μm of photoresist is spun on both sides of the wafer with different baking setups as in step C2.

D3: Two separate lithographic processes are carried out on the two sides of the wafer.

- top side: the Si_Top_Etch mask is used (Figure 3.6(a)). Substrate is exposed for 9 seconds and developed for 75 seconds.
- bottom side: the Si_Back_Etch mask is used (Figure 3.6(b)). Mask is aligned front-to-back to the already developed Si_Top_Etch pattern. Substrate is exposed for 9 seconds and developed again for 75 seconds.

A critical aspect of this step is double development of unexposed photoresist. However, pattern inspection with an optical microscope revealed successful lithography on both sides.

D4: Because a long bHF dip is required at this point, the wafer is baked at 120°C for 30 minutes prior to etching in order to prolong photoresist lifetime in the HF solution. A 28-minute bHF etch is performed in order to selectively remove the SiO_2 layer from both sides. Resist acts as an etching mask. A mask undercut of approximately 2μm is observed after etching. This phenomenon will lead to a decreased in-plane spring width of 36μm with respect to the 40μm that appear on the Si_Top_Etch mask (see Figure 3.7(a)).



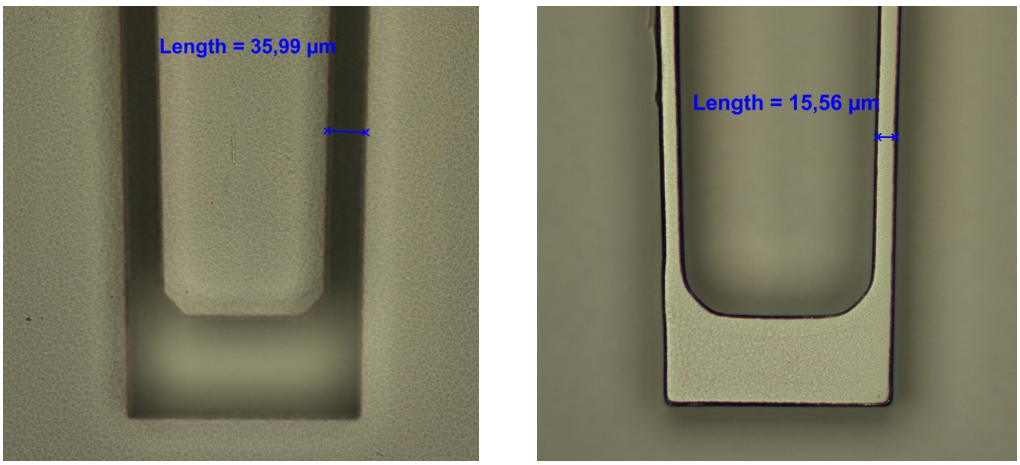
(a) (b)

(c)

Figure 3.6: (a): Single-device view of Si_Top_Etch mask. (b): Single-device view of Si_Back_Etch mask. (c): Portion of Si_Top_Etch mask, showing a sample spring design. *Red:* actual springs. *Blue:* dummy structures that will be removed after step D21. Spring width is 40μm, gap between structures is 50μm, maximum spring compression is 230μm

D5: Photoresist is stripped in a plasma asher, using a standard recipe.

D6: Silicon is etched from the front side using a DRIE process, with SiO_2 as an etching mask. A Bosch process [32] with a high etch rate is employed to keep process time low (see Appendix B). Different etch depths, corresponding to different spring thicknesses, are tested through the wafer batch. Trench depth is measured with a profiler. Only larger etched structures could be measured correctly, as the size of the profiler tip doesn't allow it to reach the bottom of the 50μm-wide trenches between spring beams and dummy structures. It is found that etching is



(a) (b)

Figure 3.7: In-plane spring width measured after step D21 by focusing microscope optics on the top and bottom of the springs. (a): Top (starting point of etch process) (b): Bottom (end point of etch process). Notice the rounding of feature corners.

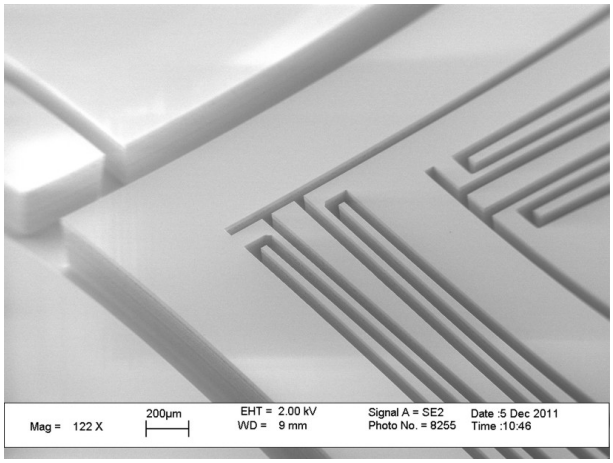


Figure 3.8: SEM image showing etched trenches on a device corner. Two spring structures are visible: each of them is surrounded by three dummy structures.

always slower in the middle of the wafer: for all samples, measured etch depth in regions near the wafer's edge is between 2% and 10% higher than in the middle. Setting a different number of etch cycles for each wafer in the batch results in average depths of 250μm to 450μm. In dry processes, etch rate typically decreases with decreasing trench width [32], so a shallower etch is expected for the spring beams. From cross-sectional microscope images (see for example Figure 3.22(a)), spring thickness was roughly estimated to be around 280μm when the profiler-measured etch depth for the larger trenches was 330μm.

An important feature observed after release of the spring structure (D21) is that trench sidewalls are considerably slanted. As shown in Figure 3.7, spring width drops from 36μm (top) to 16μm (bottom). From these data, etch profile can be calculated as:

$$90^\circ + \arctan\left[\frac{(w_t - w_b)/2}{t}\right] \simeq 91.9^\circ \tag{3.1}$$

where w_t is the top width, w_b is the bottom width, and t is the etch depth (spring thickness). As will be shown in Chapter 4, spring thinning due to non-vertical etch profile will have a dramatic effect on the device resonance frequency (see also Section 2.4.2).

D7: The wafer is RCA-cleaned to remove contaminants before entering the oxidation furnace again. The same recipe is used as in C1. The resulting SiO_2 thickness varies according to surface topography and presence of other oxide layers. Expected thickness is around 500nm in the flat areas on the bottom side where silicon is exposed, whereas no significant addition should be made in the already-oxidized regions. This is because oxidation rate is approximately proportional to $1/\sqrt{t}$, where t is the elapsed oxidation time. At the bottom of etched trenches and especially on trench sidewalls a thinner layer is predicted.
The purpose of coating the springs with SiO_2 is to protect them from unwanted thinning during a later silicon etching process (D19).

D8: A standard Reactive Ion Etching (RIE) process for SiO_2 is performed on the bottom side. The goal is to completely remove the new oxide layer from the regions beneath the springs. Measurements of bottom side oxide layer thickness after this step revealed that around 1.6μm of SiO_2 was left in the already-oxidized regions.

D9: The wafer is HMDS-coated and photoresist is spun onto the bottom side to reach a thickness of 4.2μm. A negative lithography is performed using the Si_Electrode mask to define the base/guard electrode pattern (Figure 3.11(a)). Substrate is exposed for 10 seconds, baked at 110° for 2 minutes to crosslink the resist, flood-exposed for 60 seconds and developed 70 seconds.

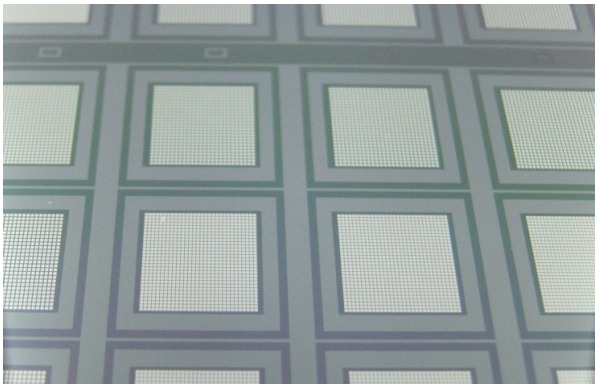


Figure 3.9: Photograph showing device wafer's bottom side after lift-off process D11. Si_Back_Etch and Si_Electrode mask patterns are superimposed. Materials visually appear with the following colors: silicon-grey, SiO_2-purple/blue, metals-white.

A relatively thick resist layer and a resist undercut profile typical of negative lithography are needed to facilitate the upcoming lift-off process (D11).

D10: A Cr/Au/Cr/Al (10/300/40/300nm) multilayer is deposited on the resist pattern by means of Electron Beam Physical Vapor Deposition (EBPVD). Originally, gold and chromium were chosen as a high-conductivity metal and an adhesion promoter respectively. It was however requested that an aluminum layer be added to the recipe to avoid chamber contamination at a later step (D16).

D11: A lift-off process is carried out in an acetone bath with ultrasonic waves. It should be noted that a relatively long process time and high ultrasonic power were required to successfully lift off all photoresist. This is probably due to the metal/resist thickness ratio being quite high because of the added aluminum layer. See Figure 3.9 for actual results.

D12: The device wafer is aligned and bonded to the cap wafer. The bonded pair will still be named "device wafer" for simplicity. The bonding technique involves raising the substrate temperature above the CYTOP glass transition temperature (108°C) and applying a uniform pressure of 0.65 MPa for 1 hour. After substrate cooling, piston pressure is released. Bonding occurs because CYTOP adheres well to other surfaces when it is in a viscous state, and the process is further eased if a small amount of solvent is left after the spin-coating and baking steps (C13). A temperature of 120°C was employed for all bonding processes through the device fabrication. Such temperature has been reported to yield a high bond strength and a low charge loss when a charged electret pattern is present [11].
After the bonding process, alignment is checked with an IR camera by inspecting the identical Si_Top_Etch patterns on the two wafers. In the ideal case they should only be misaligned by a few microns because of alignment tolerances of exposure and bonding tools. However, a significantly larger pattern displacement is observed in Figure 3.10. Misalignment is roughly estimated to be around 60μm in the y-direction and 20μm in the x-direction. Inspection of other bonded wafers revealed similar shifts with a systematic component given by a larger misalignment in the y-direction. A more detailed discussion of this phenomenon is provided in Chapter 5.

D13: CYTOP solution is spun on top of the electrode pattern. Coating and soft-baking recipes are identical to the ones in C13 but this time 5 spin-coating repetitions are applied, yielding the target electret thickness of about 10μm. Surface topography is not pronounced, so a fairly uniform coating is expected. After the last repetition, the substrate is hard-baked at 185°C for 1 hour in order to remove the remaining solvent. Because this CYTOP layer will be patterned both into the electret pattern and into the bonding frames, conflicting requirements make the hardbake step potentially critical:

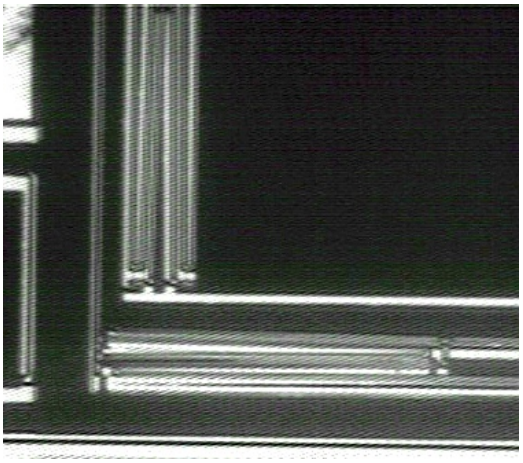


Figure 3.10: IR camera image of top pattern overlap between device and cap wafer after bonding. The lower left corner of a single device is visible. The white pattern is on the cap wafer, the grey pattern is on the device wafer.

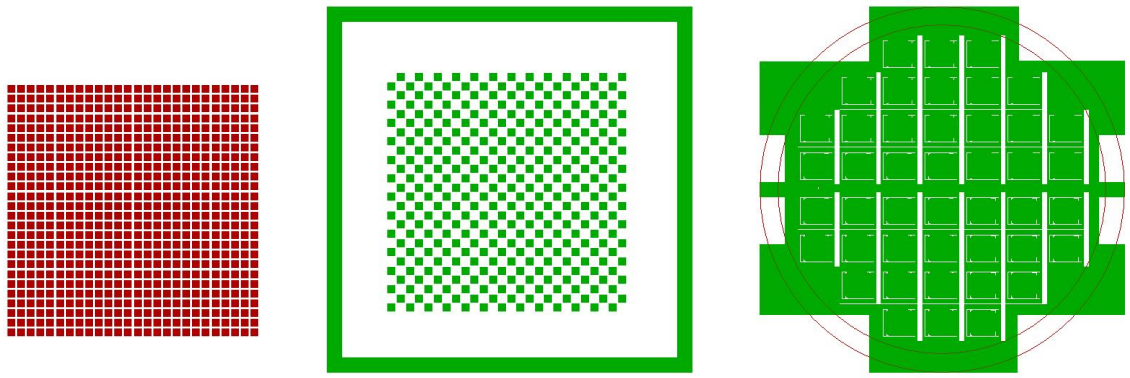
1. a higher electret charge stability is expected if CYTOP is fully dried and solvent-free

2. a higher bond yield is expected if part of the solvent is still present

It has been decided to proceed with a full hardbake, because of higher priority given to charge stability.

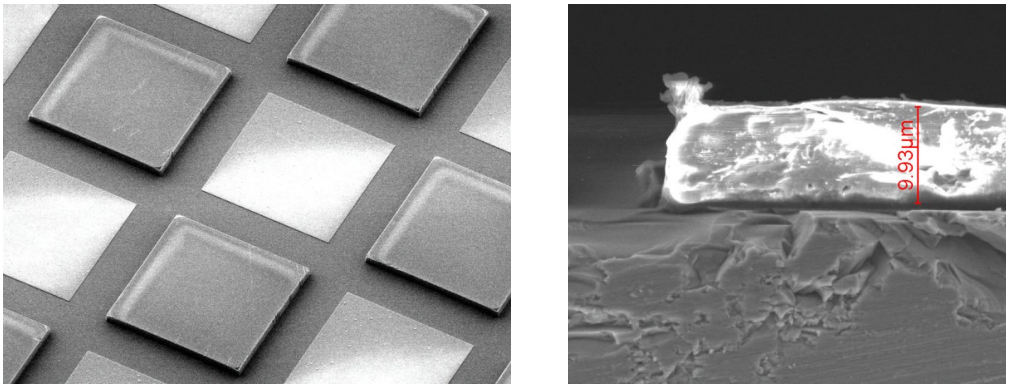
D14: The polymer surface undergoes a pre-lithography treatment, consisting of a short maskless RIE etching (20 seconds) in an oxygen plasma.

D15: A 4.2μm layer of photoresist is spun onto the CYTOP-coated surface. A positive lithography process using the Si_Polymer mask (Figure 3.11(b)), a 20-second exposure, and a 70-second development produces the resist pattern needed for the next CYTOP etching step. A relatively thick layer of photoresist is needed because of low CYTOP/resist selectivity in the RIE recipe employed in the next step. This mask has some clear-field areas near the wafer's edge (Figure 3.11(c)). Their function is to allow CYTOP removal so that the silicon surface can be reached after a later SiO_2 etching step (D20). If some silicon is exposed, the substrate can be easily connected to ground for corona charging (see Sections 2.2 and 3.7).



(a) (b) (c)

Figure 3.11: (a): Single-device view of Si_Electrode mask. (b): Single-device view of Si_Polymer mask. The electret pattern is enclosed within bonding frames. (c): Full-wafer view of Si_Polymer mask. Clear-field regions are drawn near the edge of the wafer.



(a) (b)

Figure 3.12: SEM images after CYTOP etching. (a): Tilted top view of electrets (grey) and guard electrodes (white). Square side is 200μm, distance between electrets and guard electrodes is 50μm. (b): Cross-sectional view of an electret corner. A nearly vertical etch profile and a mask undercut of about 3μm can be seen.

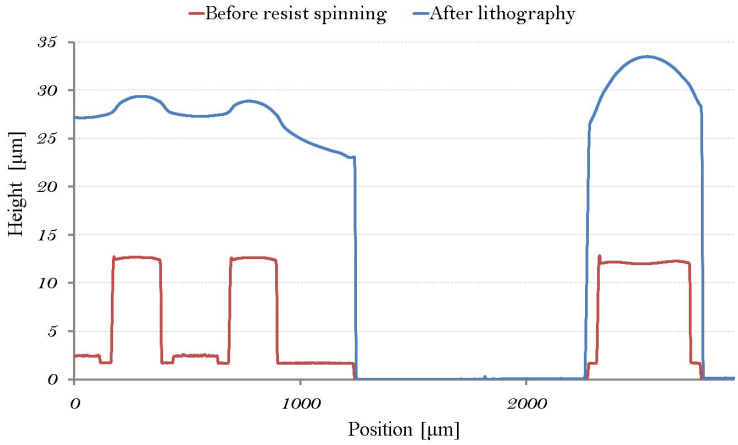
D16: Following the analysis of [33] and previous work in our group [34], CYTOP is etched with a RIE process. The optimized recipe involves a gas composition of 20% O_2 and 80% Ar, a pressure of 3 mTorr, and coil/platen powers of 600 W/300 W. Because of the low pressure, the etching process has an enhanced physical (anisotropic) component. A relatively poor selectivity to photoresist (between 5:1 and 10:1) was calculated from trench depth measurements. Figure 3.12 shows etching results; Figure 3.13(a) shows measured profiles of electrets, guard electrodes, and bonding frames.

D17: Remaining resist is stripped in an acetone bath with ultrasonic waves. Dry stripping in the Plasma Asher cannot be employed because oxygen plasma would destroy the CYTOP pattern.

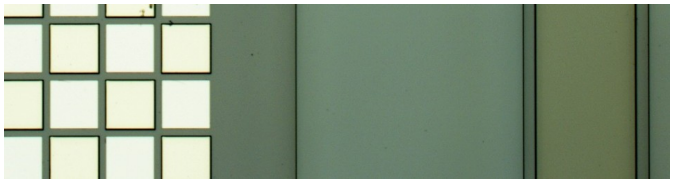
D18: A critical photoresist spin-coating step is executed in order to obtain a thick enough resist layer that will mask the upcoming DRIE process after being patterned by lithography. The step coverage of 10μm-tall topographic features given by the electret pattern and the bonding frames represents a challenge. If resist thickness in the flat regions of the substrate is comparable to the height of topographic features, a wave-like resist profile will be observed on top of surface protrusions. Therefore, a thinner masking layer is expected on top of electrets and bonding frames, especially near their sidewalls. The resist wave height is difficult to estimate quantitatively as it depends on structure height, width, distance, material, and on spin-coating parameters [35].

Depending on the etched depth of step D6, $100 - 250\mu$m of silicon need to be removed from the backside. Silicon/photoresist selectivity is reported as 40:1 for the recipe used in D19, so $2.5 - 6.25\mu$m of resist is expected to be etched during the DRIE process. A spin-coating recipe that yields a 10μm resist layer on a flat substrate is employed, with a long baking step of 10 minutes. A more viscous type of resist (AZ4562) is used, which is better suited to thicker coatings. Single and double coatings (with a 10-minute baking step in between) have been tested using the same recipe.

Optimal lithography parameters have been found by experiment: 90-second exposure and 5-minute development for a single layer, 180-second exposure and 7-minute development for a double layer. In both cases, a 10-minute postbake is included. A modified version of the Si_Back_Etch mask is used, which includes clear field areas near the wafer's edge as in step D15. Figure 3.13(a) shows two topographic profile measurements on a double-coated wafer before resist spinning and after lithography. From those data it seems that the thinnest resist layer is



(a)



(b)

Figure 3.13: Results of a double resist coating in step D16. (a): Measured surface profile before and after step D16. *Left side:* two 10μm-thick electrets together with two thin guard electrodes. *Right side:* bonding frame. The 1.6μm step between silicon and SiO_2 surfaces is also clearly visible. After lithography, a resist wave profile is seen above sharp topographic features. Resist pattern follows the Si_Back_Etch mask. (b): Microscope top view of device area measured with the profiler.

13μm on top of the electret sidewalls. This value should safely mask the electret pattern even with a very deep DRIE process. On the other hand, a single coating has proved to be sufficient up to a 150μm etch depth.

D19: Springs and dummy structures are released as silicon is etched from the bottom side with a DRIE process. It should be kept in mind that the same structures on different chips will be released at different times because of up to 10% etch depth non-uniformity across the wafer in the previous top-side DRIE process (D6). Also, larger (and deeper) pre-etched trenches will

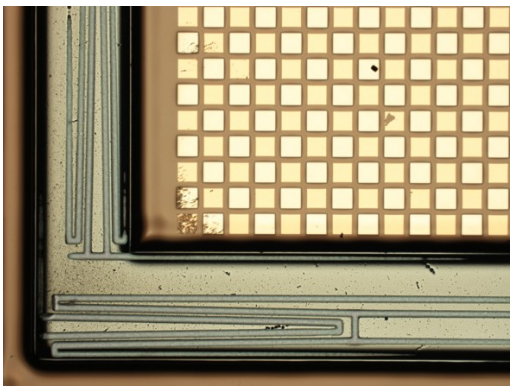


Figure 3.14: Microscope view of released springs and dummy structures with SiO_2 membranes still present. The revised recipe in step D19 has been employed. Overall resist quality is acceptable: significant degradation is only observed near bonding frame edges and proof mass sides.

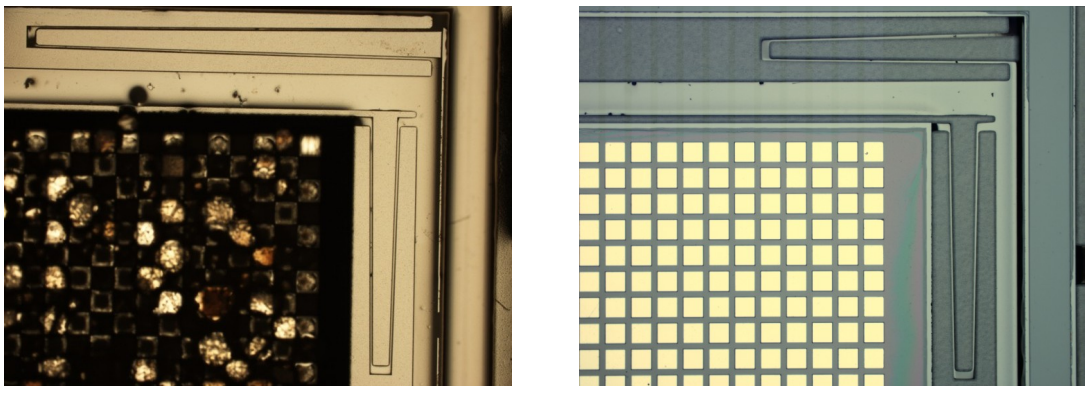
be etched through in a shorter time than narrow trenches.

A standard recipe for deep etching (Table 3.2) proved unsuccessful because resist would start to burn visibly as soon as spring structures approached full release (see Figure 3.15(a)). This is because a high-power etching recipe results in considerable heat exchange from plasma to substrate. If heat is not efficiently transferred to the chilled platen on the back of the wafer, temperature can increase dramatically on the etched surface: resist quality tends to degrade if temperature exceeds 150°C. In our case, after silicon is etched through, the only high-conductivity thermal path between the platen and the proof mass is through the thin silicon springs. Microscope inspection revealed that resist on bonding frames was mostly undegraded and resist on the proof mass had burnt earlier on devices with deeper pre-etched trenches. Hence, strong evidence exists that the main conduction "bottleneck" is in fact the spring system.

	Standard recipe (etch/passivation)	Revised recipe (etch/passivation)
Step time	(7.8s / 5.0s)	(6.0s / 5.0s)
Gas flow (SF_6, O_2 / C_4F_8)	230sccm , 23sccm / 120sccm	200sccm , 20sccm / 120sccm
Coil power	(2800W / 1000W)	(600W / 600W)
Platen power	(19W / 0W)	(10W / 0W)
Platen temperature	0°C	20°C
Pressure (APC)	87%	85%
Max number of consecutive cycles	100	10
Programmed standby step time	N.A.	2min
Silicon/resist selectivity	40:1	80:1
Etch rate	1.2μm/cycle	280nm/cycle

Table 3.2: DRIE parameters and performance of recipes used in step D19. A standard recipe for deep etching and a revised recipe for slow etching of the last few μm of silicon are compared.

To overcome this problem, the following strategy is devised: the standard high-power recipe is used until the first larger trenches are etched through; then, the etching process can proceed by switching to a revised recipe. As shown in Table 3.2, the revised recipe employs a shorter etch time, lower power, and a 2-minute standby step every 10 cycles in which plasma is switched off and resist cooling is allowed.
Release etching was successful with this strategy (see Figure 3.14). The only issue is a much



(a) (b)

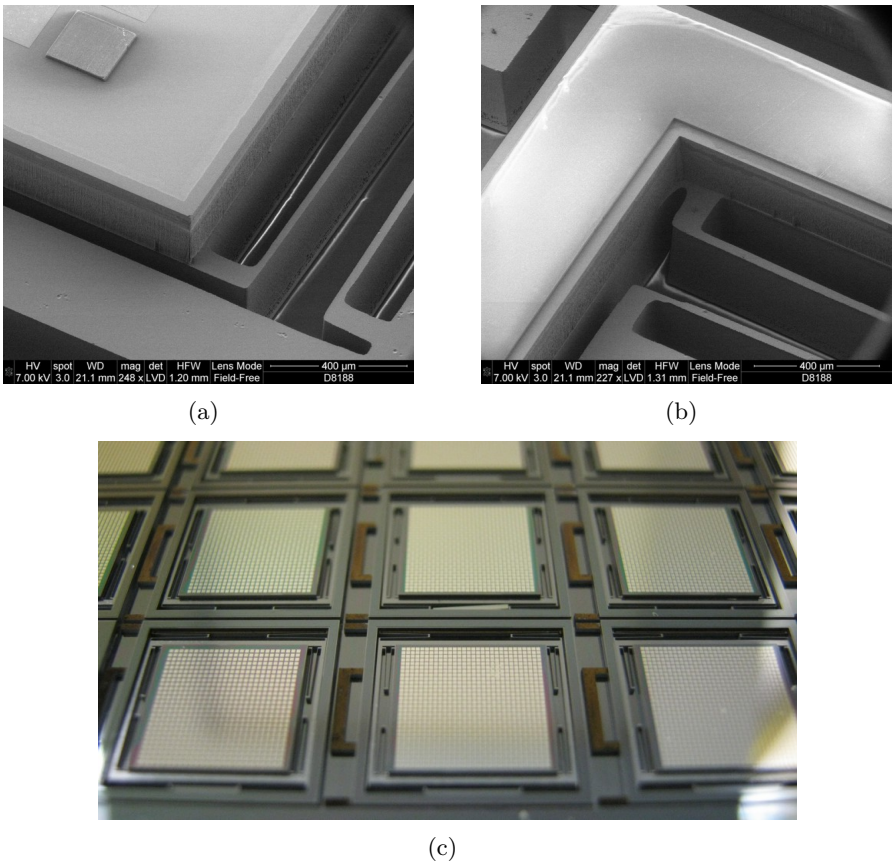
Figure 3.15: Microscope pictures showing release etch results with different DRIE recipes. (a): *Only standard recipe:* resist is burned on the whole proof mass and electret pattern is degraded. Subsequent resist strip-off will leave resist traces on the substrate. Picture taken after step D20. (b): *Standard recipe + revised recipe:* resist is kept under a critical temperature to effectively mask the release etching process. Subsequent resist strip-off is successful. Picture taken after step D21.

longer process time during which the operator has to check periodically on resist quality and degree of completion of spring release. Dummy structures and SiO_2 membranes at the bottom of the springs will be removed in the next steps.

D20: A 25-minute bHF etch removes all SiO_2 membranes between spring beams and dummy structures. Oxide is also removed completely from unmasked regions near the wafer's edge, where silicon is finally exposed and can be contacted to ground during corona charging. The etching process is performed in a beaker where the wafer can be placed horizontally in order to minimize the risk of spring breakage.

D21: The wafer is placed in a Petri dish, where resist is stripped in acetone with the aid of ultrasonic waves. Ultrasonic power is set reasonably low to avoid excessive shock to the springs. Besides removing resist effectively, ultrasonic waves have the additional advantage of ejecting dummy structures from etched trenches. As a result, spring beams are free to move.

Wafer drying cannot be carried out with a spin dryer because of the presence of fragile structures so alternative methods must be employed. If the wafer is simply wetted with ethanol and allowed to dry in a fumehood, gently touching the devices with a pair of tweezers revealed that only 20% of the proof masses were free to move after drying. This is attributed to surface tension between ethanol, proof mass, and CYTOP on the cap wafer. As ethanol progressively dries up in the device-cap gap, the proof mass is attracted towards the cap wafer and the two



(a) (b)

(c)

Figure 3.16: SEM images and photograph of completed device wafer's bottom side. (a): Partial view of one spring in the point of contact with the proof mass. An electret is visible on the top left corner. The height of the proof mass surface with respect to the spring beams corresponds to the etched depth of step D19. (b): Partial view of one spring in the point of contact with the bonding frame. Notice the CYTOP layer on top of the slightly wider silicon frame and the rounded etched corners of the spring beams. (c): Perspective view of a few chips on a full device wafer.

surfaces ultimately snap into contact. Apparently, the CYTOP layer on the cap wafer is adhesive enough to keep the proof mass surface sticking to it even under the action of an external force.

The problem was partially solved by drying the wafer at 70°C in a steady flow of evaporated ethanol, which resulted in a much better yield of 70% moveable proof masses. Figure 3.16(c) shows a portion of a successfully fabricated device wafer.

3.5 Spacing Wafer

The designed electret-counter electrode air gap is 100μm, so the thinnest available blank silicon substrate is chosen, which has a 350μm thickness. Silicon doping is irrelevant as the spacing wafer has no electrical function.

S1: The blank substrate is oxidized in a furnace using the same recipe of step D1. A 2μm-thick layer of silicon dioxide is thus grown on both sides of the substrate, which will be used as a masking layer in a later KOH etching step (S6).

S2: After an HMDS coating, photoresist is spun onto the bottom side reaching a 2.2μm thickness. The subsequent lithography process with the Si_Cap mask (Figure 3.4) includes a 9-second exposure and a 75-second development. A resist pattern is thus created on the bonding frames in order to mask them from the next bHF etching step (S3).

S3: After a 30-minute bake at 120°C, a 28-minute bHF etch is performed in order to remove the 2μm layer of SiO_2. On the top side a maskless etch takes place, so the oxide layer is removed from the whole wafer. On the bottom side, resist acts as an etching mask. As a result, silicon is now exposed everywhere except on the bonding frame pattern.

S4: Photoresist is stripped in a plasma asher, using a standard recipe.

S5: The wafer is dipped in a KOH solution for 80 minutes. As a consequence of the SiO_2 mask, 100μm-tall bonding frames are defined on the bottom side. On the top side, the wafer is simply thinned down by 100μm because of the absence of an etching mask. The height of the patterned bonding frames will be approximately equal to the air gap between electrets and counter electrodes so it is a critical parameter. 100μm have been chosen as a safe distance that keeps the electrostatic force between the two patterns low. See Appendix A for a more detailed description of the phenomenon.[1]

S6: A 200nm layer of silicon nitride (Si_3N_4) is deposited on the patterned side of the wafer with a standard Plasma-Enhanced Chemical Vapor Deposition recipe (PECVD). Its purpose is to protect the bonding frames from unwanted etching when the substrate is put again in a KOH bath (G6).

3.6 Glass Wafer

A 500μm-thick glass substrate made of fused silica is chosen for the counter electrode pattern. A glass wafer holds two advantages for our process:

1. electrical insulation, which allows metal to be deposited without the need of an additional insulating layer

2. optical transparency, which allows through-wafer bonding alignment without having to place markers on the bottom side.

[1]It would seem more sensible to define the bonding frames with a dry etching technique instead of KOH, mainly because of the resulting vertical sidewall profile. Such solution has been tested within this project but it has the severe disadvantage of a significant etch rate non-uniformity across the wafer (up to 10%, see step D6). Associated negative effects will be presented at step G6.

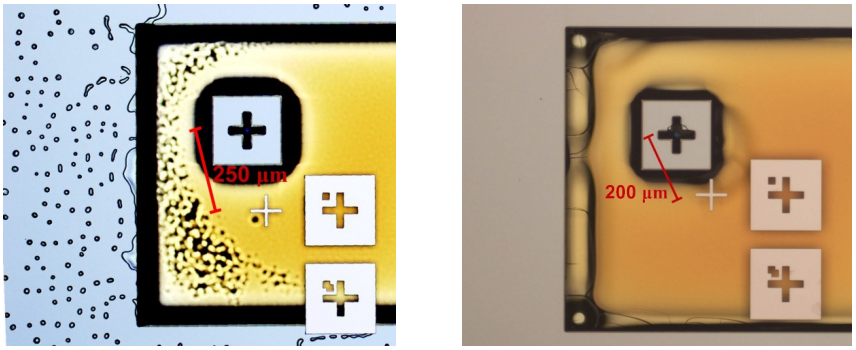
G1: As a pre-lithography treatment, the wafer is placed in a 250°C oven for 24 hours to improve resist-to-glass adhesion. A negative lithography process with the same parameters as in step D9 is carried out using the Glass_Electrode mask, in order to obtain a resist pattern that reproduces the counter electrode array and the two terminal pads (see Figure 3.3). A relatively thick resist layer and a negative lithography are employed to facilitate the upcoming lift-off process (G3).

G2: A Cr/Au/Cr (10/300/40nm) multilayer is deposited on the resist pattern by means of Electron Beam Physical Vapor Deposition (EBPVD). As in step D10, gold is chosen as a high-conductivity metal and chromium functions as an adhesion promoter for the metal/glass and metal/CYTOP interfaces.

G3: A standard lift-off process is carried out in an acetone bath with ultrasonic waves. This process required a shorter time than the analogous process in step D11, probably because of the thinner metal layer.

G4: CYTOP solution is spun onto the electrode pattern. Coating and soft-baking recipes are identical to the ones in C13. The coating/baking process is done twice in an identical way, yielding a polymer thickness of about 4μm. As in step C13, no hardbake is applied because the CYTOP layer is only used for bonding (see next step).

G5: The glass wafer is aligned and bonded to the spacing wafer. The bonded pair will still be named "glass wafer" for simplicity. The recipe used in step D12 is employed again here.
After the bonding process, alignment is checked with an optical microscope by inspecting alignment marks on both wafers. A systematic trend is observed on all bonded wafer: a shift between 150μm and 250μm always occurs in a similar direction (see Figure 3.17). Pattern misalignment is believed to take place in the bonding chamber while the substrate is heated up to 120°C and before piston force is applied. This is because patterns are still aligned when the chuck is removed from the pre-bonding alignment tool, but a shift is observed if the wafers are removed from the chamber after heating and before pressure is applied. It is assumed that wafer sliding is promoted by property changes in CYTOP above its glass transition temperature.
The systematic component of the shift is probably due to some deformation in the chuck or in the bonding apparatus, or to non-uniform wafer clamping on the chuck. The shifting amount possibly depends on bonding frame geometry and CYTOP layer thickness and uniformity. This is because resulting shifts for cap-device wafer bonding (approximately 50μm $\pm$10μm) are very different from spacing-glass wafer bonding (200μm $\pm$50μm). Since electret width is 200μm, this error will affect electret-to-counter electrode designed alignment dramatically. Possible solutions are discussed in Section 5.2.



(a) (b)

Figure 3.17: Microscope pictures showing a systematic trend in spacing wafer-glass wafer misalignment after bonding. An approximate value is given for the shift between alignment marks on the glass wafer (positive cross) and on the spacing wafer (negative cross). (a) and (b) are two different wafers in the fabrication batch.

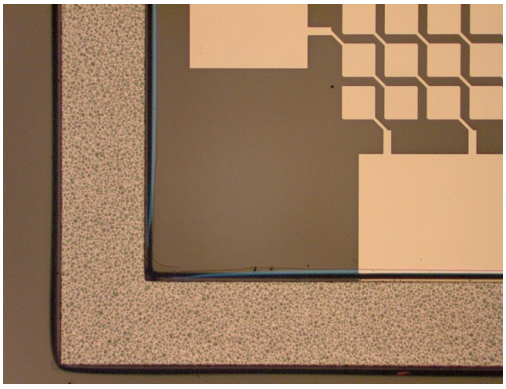
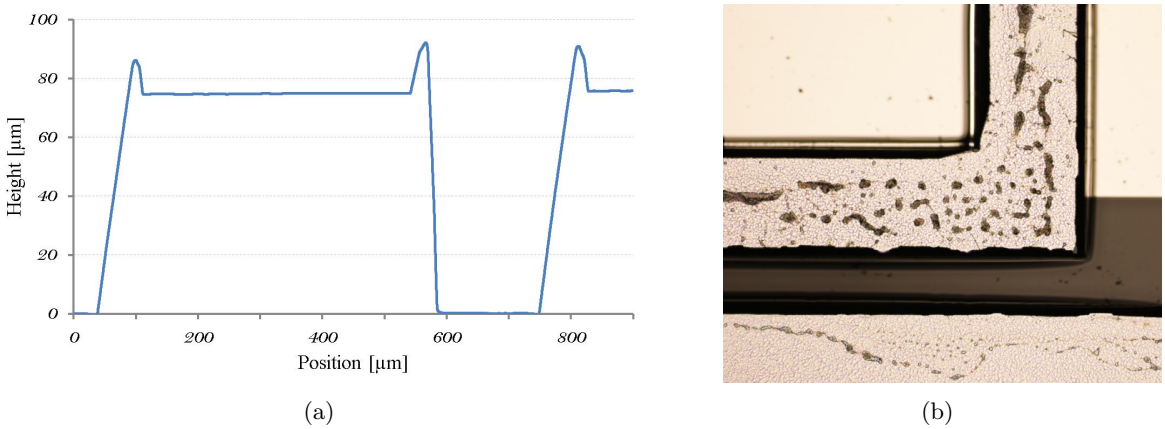


Figure 3.18: Microscope view of successful KOH etching (G6). Some Si_3N_4 (blue) is still attached to the bonding frame edges and will be removed in step G7.

G6: The bonded wafer pair is KOH-etched in order to remove silicon until the Si_3N_4 layer is reached and the bonding frames are completely defined. With reference to step S5, about 150μm need to be etched, so process time is about 2 hours in 80°C KOH. It is important to remove the substrate from the KOH bath as soon as the desired etch depth is reached, otherwise bonding frame surfaces will exhibit an out-of-plane topography to to overetching. A few nitride membranes still remain on the wafer surface after etching (see Figure 3.18). They will be removed in the next process step (G7).[2]

[2]If a dry etching technique is employed in step S5 instead of KOH, its associated etch depth non-uniformity causes the Si_3N_4 layer to be reached at different times in step G6. Up to a 15-minute delay was observed for the chips in the middle of the wafer with respect to the ones near the edge. The result is that bonding frames on edge chips are overetched and they exhibit the typical KOH profile with slanted sidewalls. It is seen from Figure 3.19(a) that KOH "spikes" are between 10 and 20μm tall. Since the CYTOP layer used for the final bonding is only 10μm thick, unsuccessful bonding can be easily foreseen. This problem has been solved by removing Si_3N_4 from the frame sidewalls after etching is complete (as in G8). An extra KOH etching step is then performed in order to flatten the bonding surface. This strategy was successful but a KOH etch in step S5 was still preferred because of less complicated processing.



(a) (b)

Figure 3.19: Results of KOH etching (G6) on a wafer that was processed with DRIE in step S5. (a): Measured surface profile of a chip near the wafer's edge. The structure in the middle is a bonding frame. KOH overetch results in 10μm- to 20μm-tall spikes on the bonding interface. (b) Microscope view of the same device. KOH spikes appear as black areas. Notice that such areas are only barely seen in Figure 3.18 where the original process flow is employed.

G7: In order to remove the remaining Si_3N_4, bHF etching is employed. bHF is reported to etch PECVD-grown nitride with an etch rate between 40 and 100μm/min [36]. After a 10-minute etch, Si_3N_4 is gone everywhere on the wafer.

G8: The CYTOP layer is etched through by means of a RIE process. Bonding frames act as an etching hard mask. As a result, the counter electrode pattern and the terminal pads become exposed. The recipe for this step is analogous to the one used for electret patterning (D16) but a different machine is employed because of material restrictions.

3.7 Corona Charging

Corona charging of electrets is performed on a completed device wafer. Figure 3.20 illustrates the main parts of the simple setup. The substrate is placed on a grounded plate, bottom side up, and clamped with a plastic ring. A metal cylinder, which includes the wire grid, sits on the plastic ring and is disconnected from ground. The thickness of the plastic ring ($\simeq$5mm) is approximately equal to the electret-wire grid distance. Aluminum foil is folded from the grounded plate to the exposed silicon regions on the wafer, in order to keep the proof masses at ground potential. A needle-shaped conductive tip is inserted into the metal cylinder and kept at about 1.5cm from the wire grid. For a duration of 5 minutes, the grid (and the whole cylinder) are set to the desired potential with respect to ground, whereas the tip is set to -8kV with respect to the grid. A negative corona discharge occurs that implants charge on the CYTOP electrets.

CYTOP has a high threshold for internal breakdown (see Table 2.1) and the out-of-plane electrostatic force should not be an issue unless a very narrow gap is desired between electrets and counter electrodes (see Appendix A). Therefore, the risk of external breakdown is the limiting factor that sets a maximum desirable implanted charge density. At atmospheric pressure, breakdown voltage for a 100μm electret-to-counter-electrode gap has a large value of 5kV (Figure 2.4). However, Paschen's curve minimum occurs at a pressure of 80mbar. Since the final bonding process (Section 3.8) is carried out at a pressure of 10^{-2} mbar, conditions for minimum breakdown voltage in air (327V) will be met at some point during pre- and post-bond pumping. In principle, the counter electrode pattern is electrically floating during final bonding so the voltage across the air gap should be much lower than the electret surface potential and discharges should not occur. If this is actually true, a very high theoretical limit to electret charging can be envisioned.

The actual electret surface potential is measured regularly after charging, using an electrostatic voltmeter as described in Section 2.2.4. Implanted surface charge density can be easily

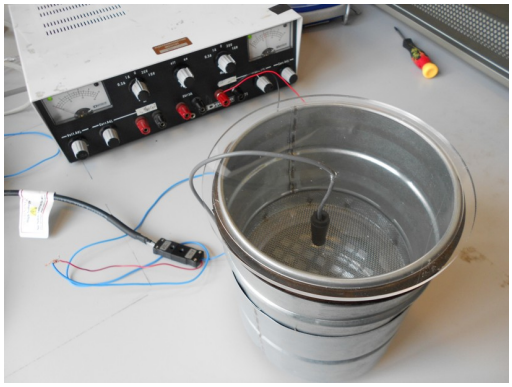


Figure 3.20: Picture of corona charging apparatus.

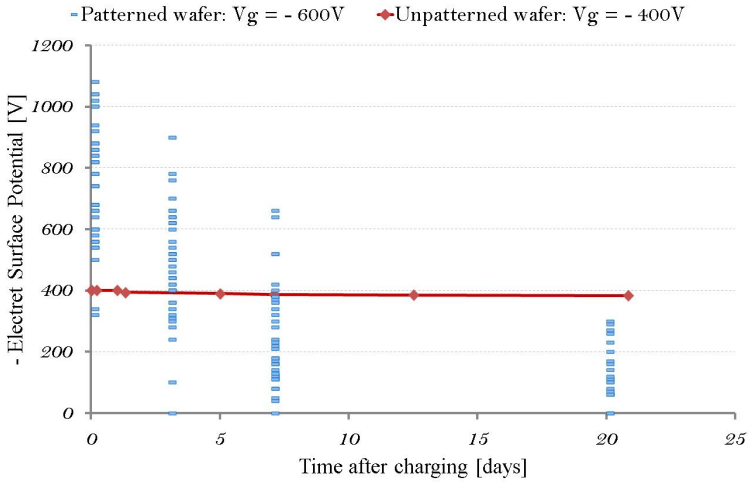


Figure 3.21: Measured surface potential decay for 10μm-thick CYTOP on two different corona-charged wafers. *Red:* wafer with an unpatterned CYTOP layer. Grid potential: -400V. *Blue:* single-chip data on a device wafer patterned with 200μm-wide electrets. Grid potential: -600V. Note that Eq. 2.17 has been used to calculate electret surface potential from the measured value of electrostatic voltmeter (see Section 2.2.4).

calculated from the surface potential measurement using Eq. 2.15. With reference to Figure 3.21, the following trends can be identified:

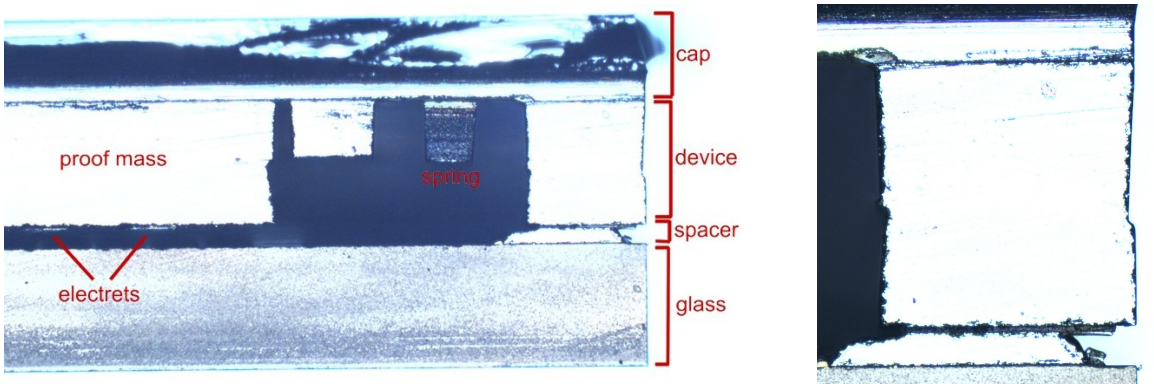
- for the patterned wafer, the initial average electret surface potential (-739V) is higher than the applied grid potential (-600V). The reason for this is explained in Section 2.2.3. A significant charge decay is observed over a period of 20 days, as the average potential drops to -126V. An overall exponential behavior can be extrapolated.
- there is a significant chip-to-chip deviation in the implanted charge level, both initially (standard deviation: 186V) and after 20 days (standard deviation: 87V)
- for the unpatterned wafer, the initial surface potential is very close (within 5V) to the applied grid potential. Charge stability is much higher, as measured potential decreases from -400V to -384V in 21 days.

From these data, reaching an electret surface potential higher than 200V seems prohibitive. Applying a lower grid potential results in similar trends with a lower asymptotic electret potential. Higher grid potentials could be tested, even though no significant improvement is expected. Maximum implanted charge levels have already been reported to decrease with decreasing electret size [11]. The main problem about device wafer charging is the dramatic charge decay over time. The reason for such a large decay is still unclear, as this phenomenon did not occur in previous experimental work [11]. Electret size does not seem to be the main factor, as $500 \times 500\mu$m electrets showed higher initial charge but a similar decay to $200 \times 200\mu$m electrets. It is suspected that poor substrate grounding might play a role. As explained in Section 2.2.2, inefficient grounding can occur because a significant resistance is encountered for current flowing through the device's thin spring system.

3.8 Final Steps

3.8.1 Device-Glass Wafer Bonding

Final bonding of device and glass wafer is a critical step. According to [11], an unpatterned 10-μm CYTOP layer with an initial surface potential of about 400V loses a significant amount



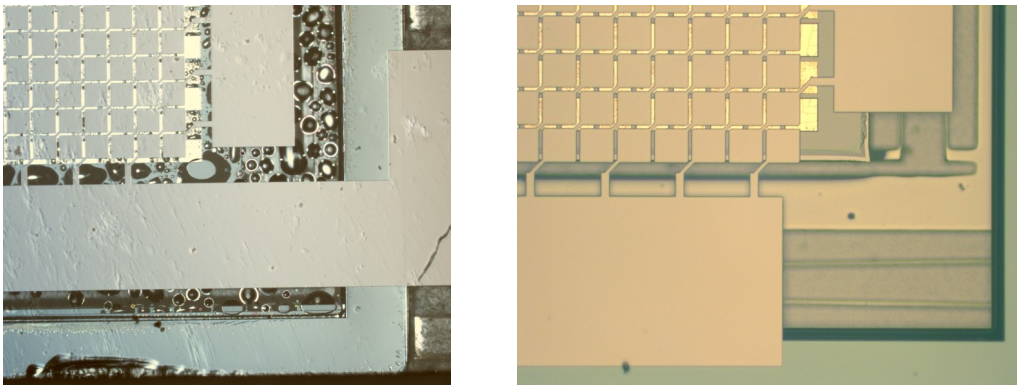
(a) (b)

Figure 3.22: Cross-sectional device views from an optical microscope. To obtain these images, a few devices have been diced by cutting in the middle of the proof mass. The device is viewed from the right with respect to the masks and top-view pictures shown in this chapter. The spacer has a different shape than in Figure 3.1 because DRIE was used at step S5 instead of KOH.
(a): Proof mass, electret pattern, and a bonding frame column are seen. A spring connects the proof mass to the bonding frame. The upper part of the cap is of a different color due to pre-dicing from the top side. Notice that the proof mass is stuck to the cap wafer (see C6).
(b) Enlarged view of the bonding frame column. Misalignments are relative to the y-direction in the top-view pictures. Spacer-glass and spacer-device y-shifts are about the same (100-150μm) but in opposite directions. Cap-device y-shift is about 30μm. Notice the thicker CYTOP layer at the device-spacer bonding interface.

of charge if stored at temperatures higher than 100°C. After a 100-minute storage at 120°C and 140°C, CYTOP surface potential is measured to be approximately 95% and 50% of its original value respectively. 100 minutes is around the time our substrates are kept at high temperature during bonding, so 120°C is expected to be beneficial for charge stability. Recipe parameters are identical to previously performed bonds.

A small number of devices was broken intentionally after dicing in order to separate the device and glass parts and quantify charge loss due to this high-temperature step. On the average, electret charge after bonding was measured to be 70% of its value before before.

The bonding process resulted again in severe wafer misalignment. The number of performed bonds is too low for statistical analysis, but it seems that shift amount and direction are com-



(a) (b)

Figure 3.23: Microscope view of two different devices after dicing. (a): Water from the dicing process leaked into the chip. (b): No water leakage is observed. In both cases, electret and counter electrode patterns are severely shifted with respect to each other.

parable to the spacing-glass wafer bonding process (G5). Figure 3.22 shows resulting bonding frame misalignment, whereas Figure 3.23 shows how bonding misalignment is reflected in electret-electrode pattern shifts.

3.8.2 Dicing

Wafer dicing allows to cut chips apart in order to have them ready for operation. Dicing equipment is a rotating saw optimized to cut Pyrex. The saw needs to be cooled by a constant water flow that also hits the wafer surface. The cap wafer is designed to protect devices from such flow. With reference to Figure 3.24, the dicing process is divided into the following sub-steps for a 1.5mm-thick wafer stack:

1. 250μm-deep vertical lines are cut from the top (cap wafer) side. Such lines are necessary in order to remove the part of the cap wafer enclosed between lines 1 and 2, so that electrical contact can be easily made to the metal terminal pads on the glass wafer. The aluminum pattern on the cap wafer's top side is used to identify the correct cut lines.

2. 1250μm-deep vertical lines are cut from the bottom (glass wafer) side, leaving 250μm uncut.

3. 1250μm-deep horizontal lines are similarly cut from the bottom side.

The yield of water-free chips varied from wafer to wafer, from a minimum of 50% to a maximum of 95% (see Figure 3.23). Presumably, an increased bonding frame misalignment results in poorer yield. This is because a narrower bonding interface makes leakage more likely.

The process flow is completed and chips can now be prepared for testing. In Figure 4.1(a) a picture is shown of a full device; see also Figure 3.25 for a separate view of the two components (glass and device parts).

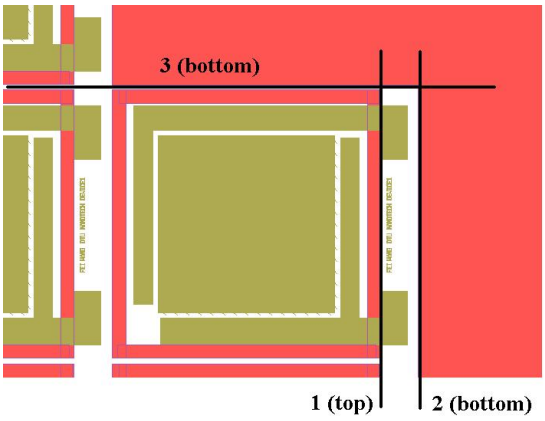


Figure 3.24: Cutting sequence for dicing process.

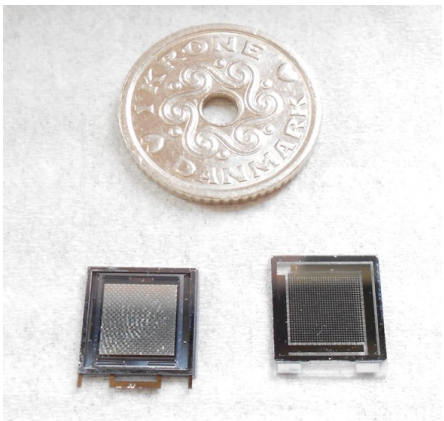


Figure 3.25: Detached device and glass chips after dicing.

Chapter 4

Testing and Results

This chapter presents a few results obtained by a fabricated harvester in terms of power output with respect to external load and driving frequency. Because of time limitations for this project, only a very basic test setup was built and just one sample device was characterized. Nevertheless, available test results prove that the proposed fabrication process flow is feasible and that the model introduced in Chapter 2 is in good agreement with the experimental data collected so far. Test results also provide hints for device parameter modification in future batches, which will be covered in Chapter 5.

Section 4.1 explains how fabricated devices are prepared in order to effectively lead the harvester's signal into an external load. Section 4.2 illustrates test procedure and setup. Finally, Section 4.3 presents actual test results. They are compared to the predictions made by the model and possible explanations are proposed for the encountered discrepancies. Additionally, some of the unknown parameters of the model (such as the mechanical q-factor and parasitic capacitances) are estimated from the experimental data using the model.

4.1 Chip Preparation

For power to be harvested, an external load must be connected between the two terminal pads of the device (see Section 2.3.3). In order to do so, a good electrical contact must be achieved between the pads and the external circuit. A direct contact with a pair of pogo pins is not possible because the pads are too small. Wire bonding the pads to a printed circuit board (PCB) is also excluded because it was impossible to bond the wire to the chromium surface. The solution to this problem is shown in Figure 4.1(a). The harvester is attached to a support board with scotch tape, together with a dummy glass chip with two larger metal pads. A strip of conductive glue is spread from each pad on the harvester to a different pad on the dummy chip. While spreading the glue it is important to avoid accidental short circuits between the two terminals or with the silicon parts of the harvester. After letting the glue dry for a few hours, it is found that contacts are satisfactory as only a small resistance of about $10\,\Omega$ is measured across the glue bridge. A pair of pogo pins can be used to easily contact with the pads on the dummy chip, so an external circuit is now connectable.

4.2 Test Setup

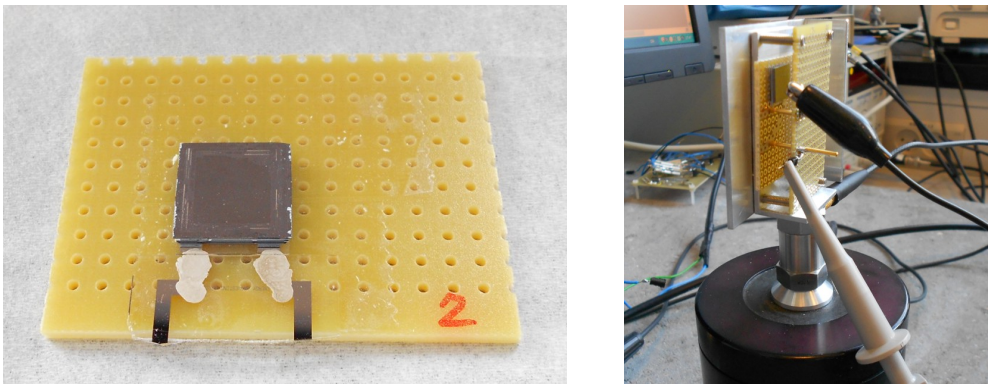
The support board with the harvester is attached to two perpendicular aluminum "L" brackets. This allows to quickly switch the tested vibration axis by simply mounting a different bracket on a piezoelectric-driven shaker (see Figure 4.1(b)). The shaker acts as the vibration source in Figure 2.18 and it can be calibrated to yield a harmonic motion in the form:

$$y(t) = -Y_0 \sin(2\pi f t) \tag{4.1}$$

which is Eq. 2.46. Hence for the acceleration:

$$\ddot{y}(t) = (2\pi f)^2 Y_0 \sin(2\pi f t) \tag{4.2}$$

If we let m be the proof mass of the harvester, $-m\ddot{y}(t) = F_{ext}$ is exactly the external force discussed in Section 2.4.1. According to equipment specifications, an acceleration amplitude $a_0 = (2\pi f)^2 Y_0$ as low as $0.015\,g$ can be provided by the piezo shaker by tuning the actuating voltage to the minimum acceptable level. In order to find the exact resonance frequency of the spring system, the driving frequency of the shaker is swept through a wide frequency range



(a) (b)

Figure 4.1: (a): Solution for leading the harvested signal out of the device. (b): Energy harvester mounted on a shaker with a connected external load.

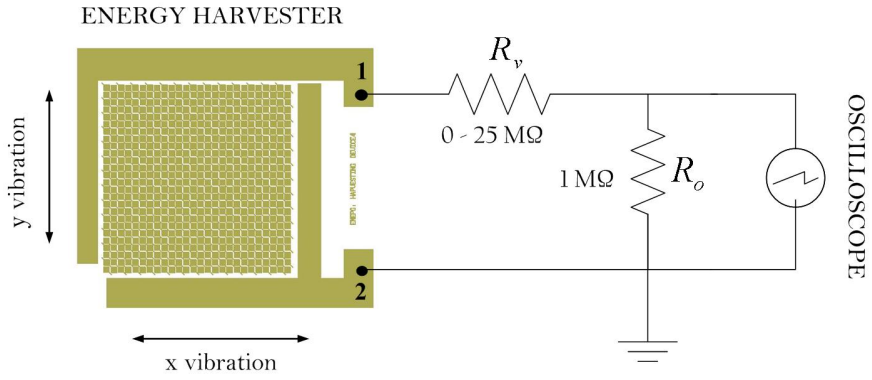


Figure 4.2: Schematic view of test circuit. $R_o = 1\,\mathrm{M\Omega}$ is the internal oscilloscope resistance, R_v is the test resistance. The shaker's motion can be either in the x- or y-direction depending on how the sample is mounted.

at constant acceleration. When a peak is found, a narrower sweep allows to accurately detect the resonance frequency corresponding to the peak center. The shaker's acceleration can be increased until a flattening of the resonance peak is observed: at this point the maximum proof mass displacement allowed by the spring design (460μm peak-to-peak) has been reached.

As shown in Figure 4.2, a variable test resistance is connected to one of the harvester's terminals. An oscilloscope (input impedance: $R_o = 1\,\mathrm{M\Omega}$) is connected in series between the variable resistance and the other harvester's terminal. With reference to Figure 2.10, the harvester's total external load is given by the two resistances in series, so $R_L = R_v + R_o$. The oscilloscope cannot be connected in parallel with R_v because its input impedance is much lower than the predicted optimal load. As a consequence, the external load seen by the harvester would always be lower than 1 MΩ.

4.3 Results and Model-Experiment Fit

For the single tested device, resonance frequencies of 179 Hz and 177 Hz were found in the x- and y-direction respectively (see Figure 4.3(b)). From the FEM analysis carried out in Section 2.4.2, resonance was expected around 510 Hz so a large discrepancy exists. As explained in Chapter 3-D6, the actual spring etching profile is 1.9° off-vertical and a mask undercut of 2μm is observed. As a result, spring beams are thinned from 36μm (top) to 16μm (bottom), instead of a constant 40μm as designed. Resonance frequency f_o should be proportional to the cube of the width (see Eq. 2.53), so an average value of 26μm is considered and the predicted resonance frequency is multiplied by a factor $(26/40)^3 \simeq 0.27$. A more realistic value of 140 Hz is estimated with this approximated procedure, but since f_o is strongly dependent on the beam in-plane width a more accurate etch profile measurement is required in order to make a better prediction.

As a next step, power output dependance on external load is investigated by calculating harvested RMS power for different values of R_v. Harvested power $P_h(t)$ is the instantaneous power dissipated in the the two load resistors. It can be easily calculated from the voltage signal $V_o(t)$ measured by the oscilloscope across its own internal resistance R_o:

$$P_h(t) = \frac{V_h^2(t)}{R_L} = \frac{{V_o}^2(t)(1 + R_v/R_o)^2}{R_v + R_o} = {V_o}^2(t)\frac{R_o + R_v}{{R_o}^2} \tag{4.3}$$

where V_h is the total voltage drop across the two resistances in series. To calculate the RMS power output, Eq. 2.66 can be used. In order to compare experimental data to the model presented in Section 2.5.4, the parameters χ and σ_d need to be known. χ is found by inspecting

electret-to-counter-electrode misalignment after final bonding with an optical microscope. The shift in the vibration direction is used to estimate χ; the shift in the direction perpendicular to vibration results in an amplitude decrease of the A_{eff} function in Eq. 2.69. σ_d is measured after testing is complete: the harvester is broken in order to separate the device and glass wafer parts and allow surface potential measurement with the electrostatic voltmeter. For the only tested device $\chi = \pi/7$ and $\sigma_d = -1.6 \times 10^{-4}\,\mathrm{C/m^2}$ ($V_S = -90\,\mathrm{V}$).

It was impossible to perform any measurements beyond 25 MΩ of total load, because the oscilloscope signal $V_o(t)$ (80mV peak-to-peak) was starting to be comparable with the noise level of the instrumentation (30mV peak-to-peak). Some filtering technique, such as a band-pass filter centered on the harvester's resonance frequency, should be employed in order to increase the signal-to-noise ratio. Nevertheless, available data are sufficient to draw four conclusions:

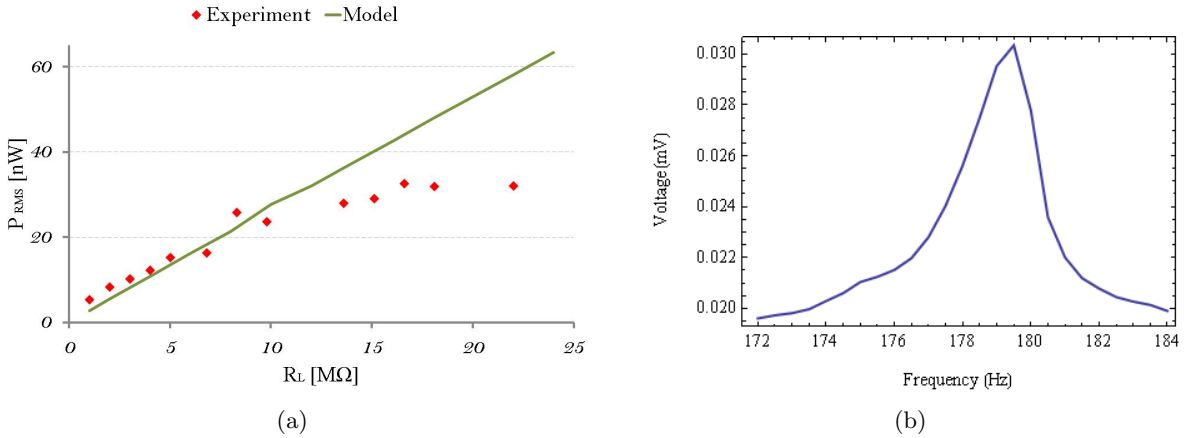
1. power generation occurs when the device is vibrated in either the x- or y-direction.

2. in the low resistance range, there is an excellent agreement between the model and the experimental results. This applies both to RMS power values (Figure 4.3(a)) and to the functional form of the electric signal (Figure 4.4).

3. starting at 10 MΩ there is a sharp deviation from linearity in the experimental power output, while the model predicts an essentially linear behavior until hundreds of MΩ. Data suggest that optimal power might be around or just above 20 MΩ, while it should be around 2 GΩ according to the model. A maximum output RMS power of 32.5 nW is obtained with $R_L = 16.6\,\mathrm{M\Omega}$. This phenomenon is attributed to parasitic capacitances in the external circuit and within the harvester. They have the deleterious effect of introducing circuit poles that cut signals above their characteristic frequency. If a single equivalent parasitic capacitance C_p is introduced in parallel with the harvester's terminals, the optimal load will be given by the following modified load-matching condition

$$\frac{1}{2\pi f(C_h + C_p)} = R_{opt} \tag{4.4}$$

where f is the signal frequency and $C_h \simeq 0.4\,\mathrm{pF}$ is the harvester's equivalent capacitance calculated in Section 2.5.4. If the experimental optimal load is estimated as 20 MΩ from the available data, it follows that $C_p = 44\,\mathrm{pF}$. This is consistent with the value of the only known parasitic capacitance, i.e. the internal capacitance of the oscilloscope $C_o = 15\,\mathrm{pF}$.



(a) (b)

Figure 4.3: (a): Harvested RMS power versus total external load according to experiment and model. (b): Resonance peak of harvested signal around 179 Hz.

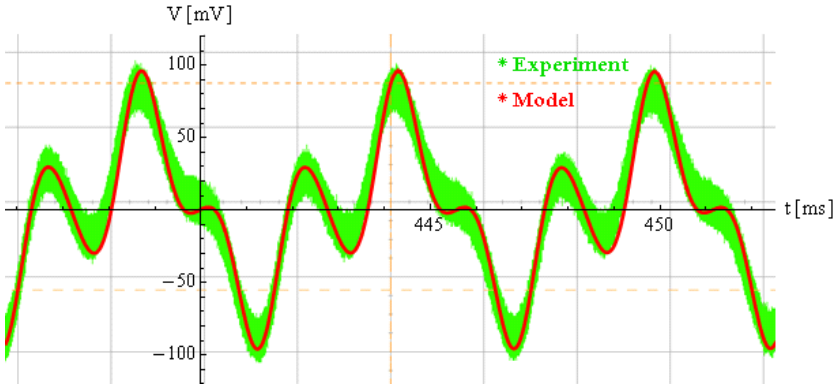


Figure 4.4: Comparison between the oscilloscope signal with $R_L = 1\,M\Omega$ and the model prediction.

The conclusion is that the total parasitic capacitance encountered with the present test setup seems to be much larger than the equivalent capacitance of the power generator. This poses a serious limit on the maximum load that can be connected without degrading the harvester's signal due to circuit poles.

4. the driving acceleration required to reach the maximum allowed proof mass displacement is $0.02\,g_{rms}$ ($\sim 0.03\,g$ amplitude), which is two orders of magnitude higher than what is expected by the model for the tested loads. This means that, at least within this load range, mechanical damping plays a major role and cannot be neglected as in Section 2.5.1. Using the model, the amount of mechanical damping can be extrapolated from experimental data as follows. The equation of motion for the proof mass (Eq. 2.61) can be rewritten as:

$$F_{net} = m\ddot{x} = F_{ext} + F_k + F_{el} + F_v \tag{4.5}$$

where F_v is simply the mechanical damping force acting on the proof mass. As explained in Section 2.4.1:

$$F_v = -c\dot{x} = -\frac{2\pi m f_o}{q}\,\dot{x} \tag{4.6}$$

where c is the mechanical damping constant and q is the resonator's mechanical quality factor (unknown). If the driving acceleration amplitude is now set to the experimental value of $0.03\,g$ and coupled equations 2.63 are solved using Eq. 4.5 instead of Eq. 2.61, one can find the empirical value of the q-factor for which an oscillation amplitude equal to the maximum displacement allowed by the spring design is reached. A value of 700 for the mechanical q-factor has been found with this procedure.

Chapter 5

Discussion and Future Improvement

5.1 Modeling

From a combination of modeling and test results, an *external* model of the harvester during operation can be finally provided in terms of circuit elements. Proof mass oscillation amplitude is regarded as a fixed parameter, therefore source acceleration has to be tuned for each external load used.
With reference to Figure 5.1, the energy harvesting device is represented by a current generator I_h with a capacitance C_h in parallel. The generated current signal does not vary with the external load and is equal to the current calculated with the model in Section 2.5.4 *under short-circuit conditions* (R_L=0). The harvester's equivalent capacitance C_h is calculated with Eq. 2.72 after finding the optimal load without parasitic capacitances. A resistive load R_L is connected between the harvester's output terminals to simulate the input impedance of the device to be powered. Another capacitance C_p in connected in parallel to account for parasitic capacitive effects in the circuit, in the load, and within the harvester itself. Under these conditions, the transfer function of the circuit is:

$$\frac{I_{out}}{I_h} = \frac{1}{1 + j\,2\pi f_e R_L (C_h + C_p)} \tag{5.1}$$

where f_e is the frequency of the electric signal and j is the imaginary unit. Therefore the circuit has a pole at $R_L = [2\pi f_e (C_h + C_p)]^{-1}$ which cuts the output current signal for loads higher than

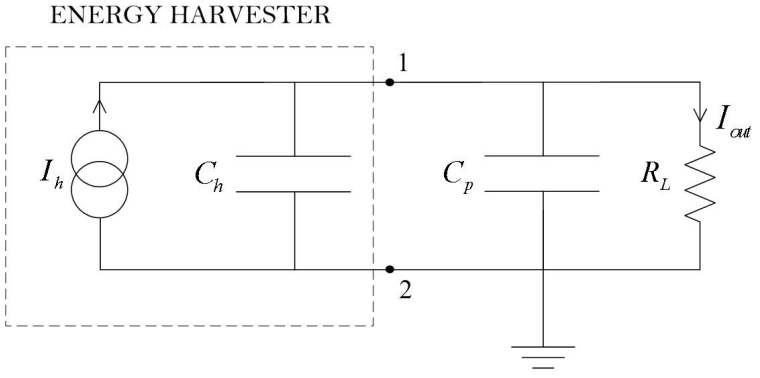


Figure 5.1: Circuit representation of operating harvester with a resistive load and an equivalent parasitic capacitance.

R_L. Hence for the output RMS power:

$$P_{out} = {I_{out}}^2 R = \frac{{I_h}^2 R_L}{|1 + j\, 2\pi f_e R_L (C_h + C_p)|^2} \tag{5.2}$$

If this function is maximized one obtains:

$$P_{max} = \frac{{I_h}^2 R_{opt}}{2} \tag{5.3}$$

$$R_{opt} = \frac{1}{2\pi f_e (C_h + C_p)} \tag{5.4}$$

where RMS values of P_{max} and I_h have been used. It is seen that maximum output power, but also optimal load, are maximized if C_p is minimized. It should also be remembered that the definition of f_e is ambiguous, because the signal is more complex than a sinusoidal function with the same frequency as the mechanical oscillation. However, this method allows to quickly estimate R_{opt} and P_{max} when C_p is known, or alternatively to extrapolate C_p from the experimental value of R_{opt}.

An issue about the model is that it does not make an *a priori* prediction for the q-factor of the mechanical resonator, which has to be estimated from experimental data instead. A more accurate prediction of optimal source acceleration would be obtained if an analytical expression for the mechanical q-factor was available. Air damping due to Couette flow of the vibrating proof mass with respect to the static cap is expected to be the major cause of mechanical damping. A fluid-mechanical FEM analysis of the actual device geometry could be employed to confirm analytical results.

It would be desirable to derive a linearized form of the whole model, in order to obtain closed-form solutions to differential equations. This would lead to analytical expressions for output power and optimal load with respect to design parameters, which would make redesigning faster and more intuitive, albeit less accurate.

Better understanding of the discharge mechanisms in corona-charged square electrets would be beneficial in order to gain more control on the long-term implanted charge magnitude and stability. This is critical for future development, as unstable electret charge and high chip-to-chip deviation limit the device lifetime and yield.

5.2 Fabrication and Process Optimization

A few devices have been successfully fabricated with the current process flow. However, the wafer with the highest yield of testable devices reached a mere 15% and the electrical patterns were severely misaligned on all wafers in the batch. For 1D energy harvesters [21, 37] this is not a crucial matter and pattern shifts only lead to a different χ in Eq. 2.68. For our 2D design, even a small misalignment in one direction results in a serious reduction of power output for vibration in the direction perpendicular to it. This was in fact encountered in our tested device: an almost perfect alignment in the y-direction and a 60μm shift in the x-direction resulted in a reduction of the power output by a factor of 3 for oscillation along y.

Poor yield is mostly due to three causes:

1. proof mass sticking to cap wafer after the last drying step (D21). This phenomenon should be reduced if a larger gap between the two structures is achieved in step C6 by a longer KOH etch. The downside of a deeper trench is that CYTOP thickness and uniformity on top of the bonding frames might be worsened to an amount that will cause a lower yield due to a poorer cap-device wafer bonding (D12). Therefore, an optimal etch depth for

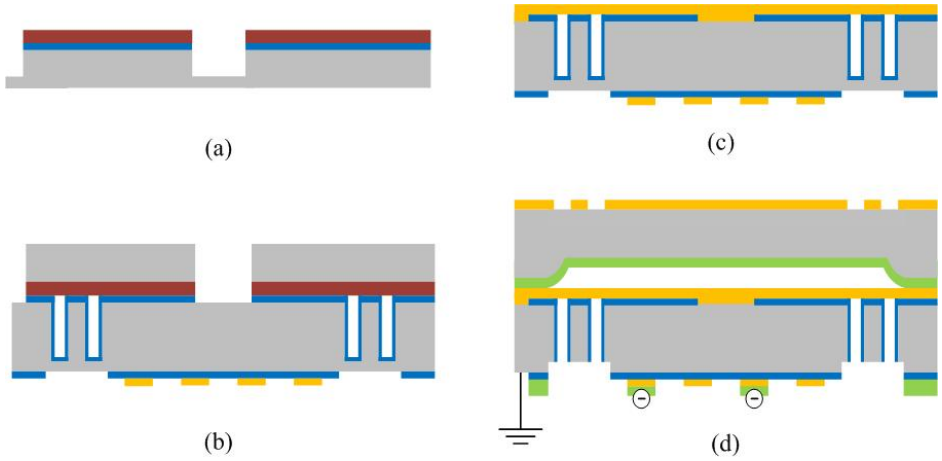


Figure 5.2: Extra process steps to be added between D11 and D12 for better proof mass grounding during charging. Note that the etched area on the left of new silicon wafer is not on the bonding frame as it would seem, but rather in unpatterned areas near the wafer's edge (see step D15 and Figure 3.11(c)).

step C6 needs to be found. Alternative drying techniques, such as critical point drying, can also be tested.

2. high chip-to-chip variability for electret charge and high charge decay. This is probably due to poor proof mass grounding in the corona process (see Sections 2.2.2 and 3.7). A few extra steps can be added to the process flow between steps D11 and D12, which should lead to a more effective ground contact. As shown in Figure 5.2, a new oxidized silicon wafer is patterned by lithography and etched (DRIE) all the way through in regions corresponding to the middle of the proof mass and in a few areas near the wafer's edge (a). Then it is bonded to the device wafer's top side with the remaining resist as a gluing agent, in order to act as a hard mask for a dry SiO_2 etching step on the device wafer (b). The hard mask is subsequently removed and a metal deposition process provides a high-conductivity layer connecting all proof masses to the edge of the wafer through the springs' top side (c). When the electrets are corona-charged, the ground contact on the bottom side easily reaches the metal layer through only 500μm of silicon (d).

3. water leakage during the dicing process due to poor sealing at bonding interfaces. This is probably due to a combination of insufficient CYTOP uniformity on the bonding frames, non-optimal bonding recipe, and bonding frame misalignment. The final bonding process (Section 3.8) seems to be the main responsible, as the only bonding failures occurred at the device-spacing wafer interface during dicing. More tests are required in order to understand how recipe parameters affect bonding performance given our wafer topography and CYTOP layer thickness.

Sliding of wafers in the bonding chamber, resulting in pattern misalignment, is probably the main fault of the current process flow (see also step G5). From glass-spacing wafer bonding tests it was found that a double CYTOP coating caused an average shift of 200μm, while a single coating produced a smaller shift of 50μm. However, a single coating also resulted in high KOH leakage into the device cavities in the next silicon etching step (G6), so a double coating is still preferable. A partial solution could be switching to an anodic bonding procedure for the glass-spacing wafer bond. This would involve direct bonding of the silicon-glass interface at 400°C, without the need of the adhesive CYTOP layer. A significant bonding alignment improvement is expected.

The problem is still open for the final bond though: a low-temperature technique is needed because of the unavoidable presence of charged electrets. One could try to pattern some matching bump/hole features on the two bonded wafers, which can be inserted into each other during wafer pre-alignment on the bonding chuck. By allowing almost no in-plane relative motion, such features should prevent any large misalignment from occurring in the bonding chamber.

Both DRIE processes associated with the spring system (D6, D19) can be improved. The recipe used for top-side spring etching should be modified in order to achieve an etch profile that is as close to vertical as possible. A reproducible vertical profile enables a great degree of control over the resonance frequency of the spring system, which can be easily predicted. Depending on the source's vibration spectrum, the harvester's resonance frequency can be adjusted by simply tuning the beam out-of-plane thickness, i.e. the etch depth of step D6. For the bottom-side release etch (D19), further modification of the revised recipe might decrease process time while still keeping resist at a safe temperature.

The base/guard electrode pattern could be turned into a uniform metal layer covering the whole proof mass. With our design there is no need to separate base and guard electrodes like in [11], because both base and guard electrodes are electrically floating during charging (see Figure 2.6). A complete surface coverage by a metal layer should remove unwanted charging of the exposed SiO_2 in the gaps between electrodes.

5.3 Testing

In order to detect smaller voltage signals from the harvester, the signal-to-noise ratio must be improved by employing some filtering technique. With the current test setup, noise amplitude at the oscilloscope is around 30mV peak-to-peak. Because the harvester's signal has a relatively narrow bandwidth around the resonance frequency of its own mechanical system, a band-pass filter would probably be beneficial. Limiting parasitic capacitances in the measurement circuit would also be beneficial as it would allow to explore device performance in the high load range.

5.4 Parameter Optimization

The most urgent design change prompted by test results is a significant decrease of the optimal load without parasitic capacitances. Since it is $2\,\mathrm{G\Omega}$ with our current design, it needs to be reduced by at least two orders of magnitude or parasitic effects will continue to dominate at the theoretical optimal load. With reference to Eq. 2.72, if the mechanical vibration frequency f_m is fixed there are two ways to decrease R_{opt}:

1. *by increasing C_h*: this could be implemented by increasing total device area or by reducing the electret-counter electrode gap g. Since device area is taken as a design constraint, g is varied in the model in order to quantify this behavior. Using the notation of Appendix A, if the initial gap z_0 is set to 10μm and $V_S = -80$V, then the out-of-plane force analysis predicts a 7.5μm equilibrium gap (z_{eq}) without any additional unstable equilibrium point. With such a gap, the model predicts an optimal load of $100\,\mathrm{M\Omega}$ without parasitic capacitances, which yields an output power of 40μW at $V_S = -80$V, $f = 200\,\mathrm{Hz}$, $\chi = \pi/2$, and $a_0 = 0.58\,\mathrm{g}$.
   The technical feasibility of such a small gap still has to be proved, as gap uniformity is critical and unwanted out-of-plane vibration and shocks might easily lead to electrets sticking to counter electrodes due to the attractive electrostatic force. Moreover, an optimal source acceleration amplitude of $0.58\,\mathrm{g}$ is classified as "high" [38], which would considerably shorten the list of potential vibration sources. The most obvious way to decrease

Maximum power (RMS)	P_{max}	92μW
Peak power	P_p	0.4 W
Optimal load	R_{opt}	110 MΩ
Electret surface charge density (potential)	σ_d (V_S)	-1.42×10^{-4} C (-80 V)
Source acceleration amplitude	a_0	0.6 g
Spacing wafer thickness	g_o	10μm
Electret-counter electrode gap (at equilibrium)	g	7.5μm
Electret thickness	d	10μm
Electret length and width	w	100μm
Electrode spacing	s	20μm
Number of electret cells in one device	n	1800
Proof mass	m	11.8×10^{-5} Kg
Proof mass thickness	p	1mm
Mechanical vibration frequency	f	200 Hz
Maximum proof mass vibration amplitude	$X_{a,max}$	230μm
Electret-counter electrode phase factor	χ	$\pi/2$

Table 5.1: Predicted performance and parameters for a proposed new design.

source acceleration requirements is to increase the mass of the proof mass by employing a thicker wafer. Using the model, it seems that the optimal acceleration for full proof mass displacement amplitude is approximately proportional to $1/m$ as predicted by [27] for a generic vibrational harvester. A 1mm-thick proof mass would require half the acceleration of a 500μm-thick proof mass at the same vibration frequency.

2. *by increasing f_e*: this is achieved by increasing the number N of counter electrodes overlapped by a single electret square during a full oscillation cycle. $N = 3$ with our current design (see Figure 2.29(b)) and $f_e \propto N$ if $\chi = \pi/2$, i.e. patterns are aligned. From Eq. 5.4 it seems that $R_{opt} \propto 1/N$. From Eq. 5.3 it also appears that $P_{max} \propto N$ because the same charge is transferred between terminals 1 and 2 in a shorter time resulting in a higher current ($I_h \propto N$).
   A higher N could be implemented either by changing the spring design to increase the maximum allowed proof mass displacement, or by decreasing electret size. However, both solutions have downsides:

   - increasing proof mass travel means reducing the total electret area on the device, resulting in lower total electret charge $2n\sigma_d$ and lower equivalent capacitance C_h. The combination of the two effects decreases output power and increases optimal load.
   - decreasing electret width w means decreasing the maximum level of implanted charge that can be reached by corona charging [11]. Additionally, the effect of fringing fields is amplified for capacitor plates with a smaller area, which leads to a lower effective overlap (see Section 2.5.4) and lower output power.

Based on this analysis, decreasing both g and w seems to be the most sensible strategy to achieve a higher P_{max} and a lower R_{opt}. The argument is that scaling all capacitor dimensions simultaneously has the extra advantage of keeping fringing fields low. The main challenges are: charging of smaller electret structures, gap uniformity and stability, and stringent requirements on bonding alignment. If such issues are finally overcome, the model predicts an RMS power generation of 92μW with the parameters given in Table 5.1. A comprehensive optimization study, similar to [39], could be devised in order to have a more quantitative view.

Conclusion

A resonant electret-based micro energy harvester, packaged into a $1.1 \times 1.0 \times 0.15\,\text{cm}$ chip, was successfully designed and fabricated with MEMS-compatible wafer-level processes exclusively. The goal was to generate electrical power exploiting two perpendicular ambient vibration components. Target vibration sources are typical machinery vibrations with low acceleration (0.01-0.1 g) and frequency in the 100-500 Hz range.

The electret material of choice was CYTOP©, which was patterned into 10μm-thick, $200 \times 200\,\mu\text{m}$ squares by Reactive Ion Etching and charged quasi-permanently up to $-3.5 \times 10^{-4}\,\text{C/m}^2$ with a corona setup. CYTOP was also employed as an adhesive material for full wafer bonding processes.

A new hybrid analytical/numerical model was proposed by the author. The model was able to predict output power and output signal shapes with excellent accuracy within the collected data range. To the author's knowledge, it is the first model describing an electret-based harvester where counter electrodes and base electrodes are not kept at the same potential. Instead of simply approximating the in-plane electrical force on the proof mass as a viscous or Coulomb damping force [27, 28], an explicit force expression was provided from a thermodynamical analysis. It was shown that the electrical force was proportional to the output current but modulated by the proof mass velocity. A FEM analysis was included in order to account for boundary effects given by fringing fields.

With the current device design, a maximum RMS power of 32.5 nW was achieved with a load of 17 MΩ, a source vibration frequency of 179 Hz, a source acceleration amplitude of 0.03 g, and an electret surface charge density of $-1.6 \times 10^{-4}\,\text{C/m}^2$. The fabricated devices were plagued by an extremely high predicted optimal load of 2 GΩ. Maximum power was found experimentally at a much lower load due to parasitic effects. Unfortunately, high optimal loads seem to be a recurrent issue in electret-based energy harvesters [21, 37, 40]. Pattern misalignment during bonding processes and unpredictable implanted charge levels of electrets resulted in a non-reproducible fabrication process flow.

Advances are necessary in several areas in order to increase output power, decrease optimal load, increase device yield, and improve pattern alignment for effective two-dimensional harvesting. Nevertheless, the model suggests that power outputs as high as 92 μW can be obtained by optimization of device parameters if a higher degree of control is reached in a few key fabrication processes. The new set of parameters proposed in Table 5.1 is ambitious but it should not be technically prohibitive. The proposed values of source acceleration and frequency correlate well with a characteristic vibrational mode found in microwave oven casings when power is turned on (see [2] and Figure 1.1).

All these potential features would render an optimized version of our energy harvester highly attractive for future powering of wireless sensor network (WSN) nodes.

Appendix A

Out-of-Plane Force Analysis

An important factor to be considered in device design is the out-of-plane equilibrium position of the proof mass and its stability region. Device parameters must be chosen carefully in order to keep the risk of proof mass-to-electret snap-in low. Hence a force equilibrium study is carried out with reference to Figure A.1. There are three main out-of-plane forces acting on the proof mass. $F_{el,z}$ is the attractive electrostatic force between counter electrodes and electrets, mg is the gravitational force (with m intended as the proof mass), and $F_{k,z}$ is the force arising from a finite spring stiffness in the z-direction. The gravitational force is taken in the negative z-direction to account for the worst possible case. z_{eq} is the equilibrium air gap between the two patterns and Δz is the displacement between z_{eq} and the spring rest position $z_0 = z_{eq} + \Delta z$, which is taken as a fixed design parameter. The variable z is used instead of g to avoid confusion with the gravitational constant. This study assumes the electrically static situation described in Section 2.3.2. The electrostatic force is given by:

$$F_{el,z} = -\frac{dU_{el}}{dz} \tag{A.1}$$

Counter electrodes and substrate are assumed to be short-circuited as in such a situation F_{el} has a higher-order dependence on the air gap and thus is more dangerous for the device. Short-circuits can occur for example during wafer dicing, where the sample is exposed to a large water flow. One can then write for the total potential energy:

$$U_{el} = \frac{1}{2}\frac{{Q_{c0}}^2}{C_g} + \frac{1}{2}\frac{{Q_{b0}}^2}{C_d} = \frac{nA_0 d{\sigma_d}^2}{2\varepsilon_0}\frac{z}{d + \varepsilon_d z} \tag{A.2}$$

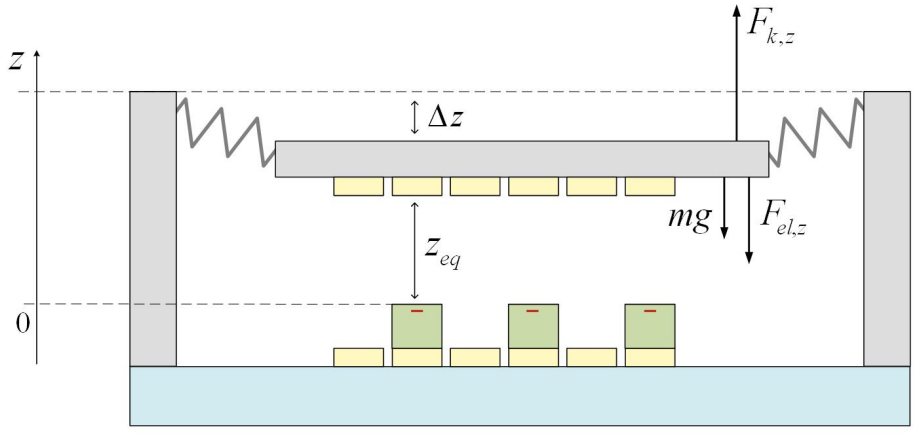


Figure A.1: Force equilibrium study in the out-of-plane direction

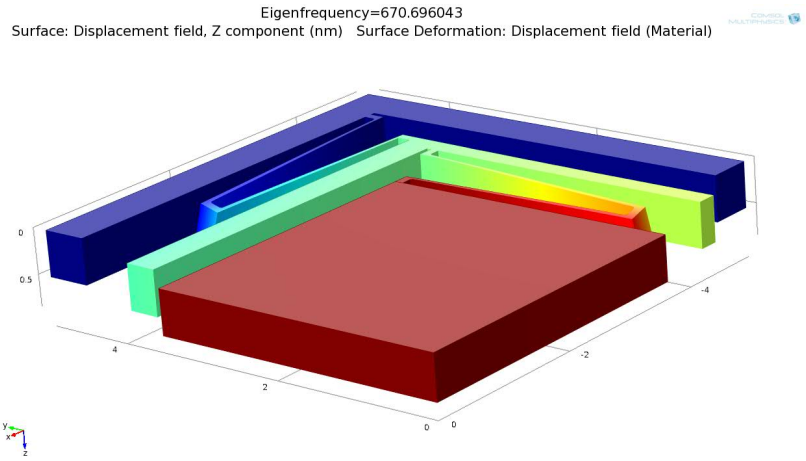


Figure A.2: Z-direction eigenfrequency simulation with COMSOL Multiphysics.

With reference to Section 2.3.2, $Q_{c0} = nA_0\sigma_{c0}$ is the total charge on counter electrodes, $Q_{b0} = nA_0\sigma_{b0}$ is the total charge on base electrodes, $C_g = n(C_{g1} + C_{g2})$ is the total capacitance across the air gap, and $C_d = n(C_{d1} + C_{d2})$ is the total capacitance across the electret. Then for the electrostatic force:

$$F_{el,z} = -\frac{dU_{el}}{dz} = -\frac{nA_0 d^2 {\sigma_d}^2}{2\varepsilon_0(d + \varepsilon_d z)^2} \tag{A.3}$$

which is a strictly attractive force whose magnitude increases with decreasing air gap z. Assuming an approximately linear spring force in the z direction with z_0 as the spring rest position, one can simply write:

$$F_{k,z} = k_z(z_0 - z) \tag{A.4}$$

An estimate for the out-of-plane spring constant is provided by an eigenfrequency simulation in the z-direction with COMSOL Multiphysics. In the worst case, with the lowest-k spring design (long and thin beams), a resonant frequency of $f_{res,z} \simeq 600\,\text{Hz}$ is found, corresponding to $k_z = 4\pi^2 m f_{res,z}^2 \simeq 850\,\text{N/m}$ (see Figure A.2).

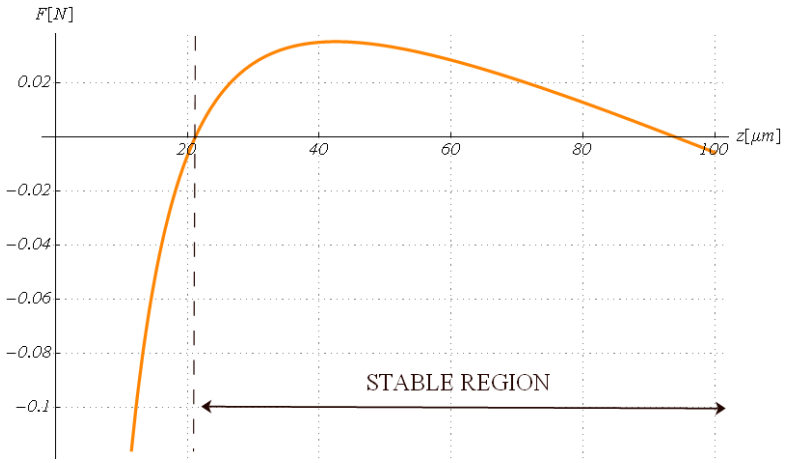


Figure A.3: Net force on the proof mass in the out-of-plane direction with respect to instantaneous air gap, assuming $z_0 = 100\mu$m and a worst-case situation. A positive force is repulsive, a negative force is attractive.

With these data, the force function with respect to z is

$$F_{net}(z) = k_z(z_0 - z) - mg - -\frac{nA_0 d^2 {\sigma_d}^2}{2\varepsilon_0(d + \varepsilon_d z)^2} \tag{A.5}$$

This function is plotted in Figure A.3 for parameters chosen in the high-risk regions, i.e. the lowest simulated k_z and a very high electret surface potential of $V_S = 800V$. It is observed that the net force equals zero at two points. One is a stable equilibrium point for the system, located at $z_{eq} = 93\mu$m. The counter electrode pattern will always move back asymptotically to this equilibrium point unless a large enough perturbation occurs that reduces the air gap below the point of unstable equilibrium $z_{neq} = 23\mu$m. In this case, the net force on the proof mass will be directed toward the electret pattern and the two surfaces will snap together. With $k_z = 1.8$kHz and $V_S = 200V$, corresponding to an average situation, z_{eq} rises to 99.9μm and z_{neq} disappears. When the silicon substrate is electrically floating, F_{el} does not depend on z because charges in Eq. (A.2) are constant. z_{eq} turns out to be similar to the short-circuit case and the unstable equilibrium point disappears.

Appendix B

Fabrication Process Flow

A sketch of the whole process flow is provided here as a quick reference guide.
Notes:

- cross-sectional drawings refer to a single device. In total, 44 devices are fabricated on one wafer.
- a small area on the left side of the drawings is etched from step D16 onwards. This area does not belong to the device bonding frames as it would appear from the sketches. Instead, it is located near the edge of the wafer in a region that is not occupied by devices. Its function is explained in Section 3.4.

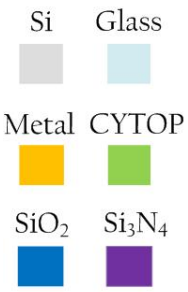


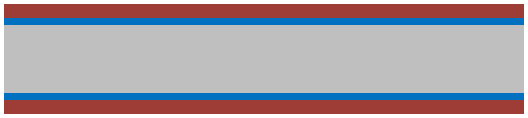
Figure B.1: Color legend for fabrication process flow

CAP WAFER

Substrate: Double polished silicon wafer
n- or p-doped
Thickness: 320 – 350 µm

C1. Thermal Oxidation (wet)
Furnace: Bor Drive-in
50min oxidation at 1100°C + 20min anneal
SiO_2 thickness: 500nm

C2. Double-side photoresist spin coating
HMDS oven, then SSE spinner
Proximity bake for the second coating
Resist thickness: 2,2µm



C3. Positive lithography
KS Aligner
- Mask: Si_Cap; main flats alignment
- Hard contact, 9s exposure, 75s development

C4. SiO_2 wet etching
bHF bath
Etch time: 8min

C5. Photoresist strip-off (dry)
O_2 Plasma Asher
O_2: 210 sccm; N_2: 70 sccm; Power: 1000W; Time: 30 min

C6. Silicon wet etching
KOH bath at 80°C
Etch time: 15min (etch depth: 20µm)

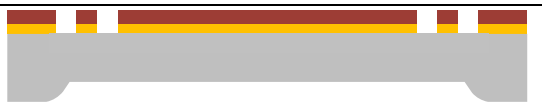
C7. SiO_2 wet etching
bHF bath
Etch time: 8min

C8. Silicon wet etching
KOH bath at 80°C
Etch time: 30sec

C9. Aluminum deposition
Wordentec
E-beam evaporation - Al thickness: 50nm

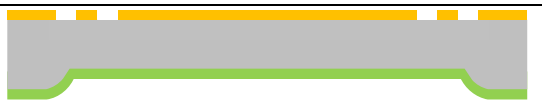
C10. Positive lithography
SSE spinner, KS aligner
Resist thickness: 1,5µm
- Mask: Si_Top_Etch (aligned to Si_Cap)
- Hard contact, 6s exposure, 70s development

C11. Aluminum wet etching
Al etching bath
Etch time: 2min



C12. Photoresist strip-off (dry)
O_2 Plasma Asher
O_2: 210 sccm; N_2: 70 sccm; Power: 1000W; Time: 30min

C13. CYTOP spin coating
Manual spinner: 800 rpm for 30s
Softbake: 120°C hotplate for 10min
Coating and baking done twice



DEVICE WAFER

Substrate: Double polished silicon wafer
n- or p-doped
Thickness: 500 - 550 µm

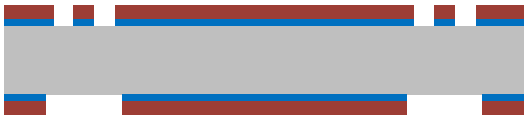
D1. Thermal Oxidation (wet)
Furnace: Bor Drive-in
10hr oxidation at 1100°C + 20min anneal
SiO_2 thickness: 2µm

D2. Double-side photoresist spin coating
HMDS oven, then SSE spinner
Proximity bake for the second coating
Resist thickness: 2,2µm

D3. Positive lithographies
KS Aligner
Front: - Mask: Si_Top_Etch; main flats alignment
- Hard contact, 9s exposure, 75s development

Back: - Mask: Si_Back_Etch; backside alignment
- Hard contact, 9s exposure, 75s development

D4. SiO_2 wet etching
30min hardbake at 120°C , then bHF bath
Etch time: 28min



D5. Photoresist strip-off (dry)
O_2 Plasma Asher
O_2: 210 sccm; N_2: 70 sccm; Power: 1000W; Time: 30 min

D6. Silicon etching (DRIE)
DRIE-Pegasus
Recipe: Process A, T = 20°C
Etch – 7s, SF_6: 550 sccm, coil/platen: 2800/45 W
Passivation – 4s, C_4F_8: 200 sccm, coil/platen: 2000/0 W
Etch depth: desired spring thickness (250-450µm)

D7. Thermal Oxidation (wet)
RCA clean, then Furnace: Bor Drive-in
50min oxidation at 1100°C + 20min anneal
SiO_2 thickness: variable

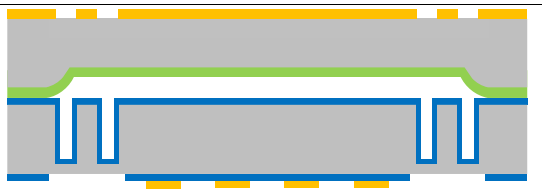
D8. SiO_2 backside etching (dry)
RIE1
Recipe: 1SiO2msi (CF_4: 8 sccm; CHF_3: 40 sccm)

D9. Negative lithography
HMDS oven, SSE spinner, KS aligner
Resist thickness: 4,2µm
- Mask: Si_Electrode (aligned to Si_Back_Etch)
- Hard contact, 10s exposure
- Reversal bake: 110°C hotplate for 2min
- 10min wait, 60s flood exposure, 70s development

D10. Metal multilayer deposition
Wordentec
E-beam evaporation
Starting from substrate: Cr/Au/Cr/Al 10/300/40/300nm

D11. Lift-off
Ultrasonic acetone bath

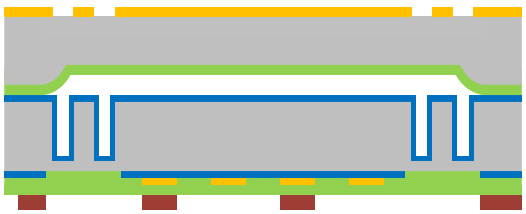
D12. Polymer bonding with Cap Wafer
EVG-NIL
Crosshair alignment between Si_Cap and Si_Back_Etch
Piston Force: 5kN for 1 hour
T = 120°C, p = 10^{-2} mbar



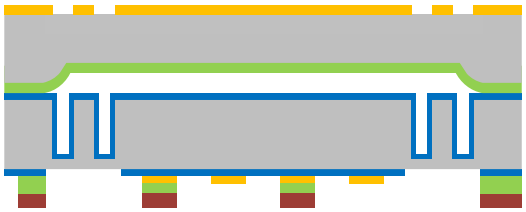
D13. CYTOP spin coating
Manual spinner: 800 rpm for 30s
Softbake: 120°C hotplate for 10min
Coating and baking done 5 times (final thickness: ~ 10µm)
Final hardbake at 185°C for 1 hour

D14. CYTOP surface revision (dry polymer etching)
RIE2
Recipe: feipre (O_2: 98 sccm; N_2: 20 sccm)
Etch time: 20s

D15. Positive lithography
SSE spinner, KS aligner
Resist thickness: 4,2µm
- Mask: Si_Polymer (aligned to Si_Electrode)
- Hard contact, 20s exposure, 70s development

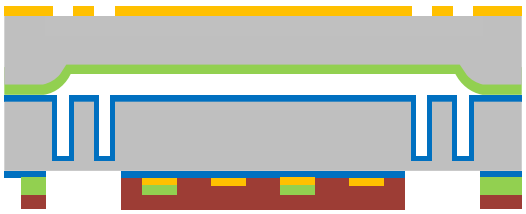


D16. CYTOP etching (dry)
ASE
Recipe: feicy3 (O_2: 5 sccm; Ar: 20 sccm)



D17. Photoresist strip-off (wet)
Acetone bath

D18. Positive lithography
SSE spinner, KS aligner
Resist thickness: 10µm
- Mask: Si_Back_Etch (aligned to Si_Electrode)
- Hard contact, 90s exposure, 5min development

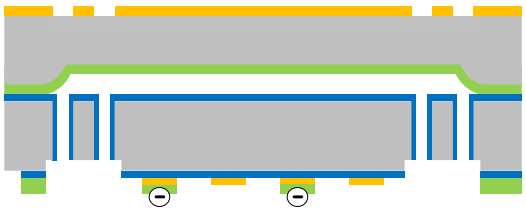


D19. Silicon etching – release of spring structure (DRIE)
ASE
Etch: SF_6; Passivation: C_4F_8
1st recipe: feideep (etch step: 7.8s, coil/platen: 2800/19 W)
2nd recipe: feislseq (etch step: 6s, coil/platen: 600/10 W)

D20. SiO_2 wet etching
bHF bath
Etch time: 25min

D21. Photoresist strip-off (wet)
Acetone bath

D22. Corona charging
Tip voltage: -8kV
Grid voltage: as desired (-100V to -600V)
Sample voltage: 0V (ground potential)
Tip-grid distance: 15mm
Grid-sample distance: 5mm
Charging time: 5min



SPACING WAFER

Substrate: Double polished silicon wafer
n- or p-doped
Thickness: 320 – 350 µm

S1. Thermal Oxidation (wet)
Furnace: Bor Drive-in
10hr oxidation at 1100°C + 20min anneal
SiO_2 thickness: 2µm

S2. Positive lithography
HMDS oven, SSE spinner, KS aligner
Resist thickness: 2,2µm
- Mask: Si_Cap; main flats alignment
- Hard contact, 9s exposure, 75s development

S3. SiO_2 wet etching
30min hardbake at 120°C , then bHF bath
Etch time: 28min

S4. Photoresist strip-off (dry)
O_2 Plasma Asher
O_2: 210 sccm; N_2: 70 sccm; Power: 1000W; Time: 30 min

S5. Silicon wet etching (double-sided)
KOH bath at 80°C
Etch depth: desired electret-counter electrode gap (100µm)

S6. Si_3N_4 deposition
PECVD 3
Recipe: fewasin (deposition time: 20min)
Si_3N_4 thickness: 200nm

GLASS WAFER

Substrate: fused silica wafer
thickness: 500 - 550 µm

G1. Negative lithography
250°C oven (24 hours), SSE spinner, KS aligner
Resist thickness: 4,2µm
- Mask: Glass_Electrode; main flats alignment
- Hard contact, 10s exposure
- Reversal bake: 110°C hotplate for 2min
- 10min wait, 60s flood exposure, 70s development

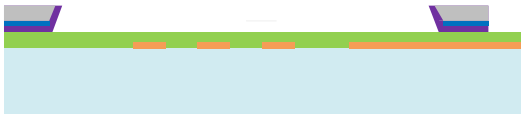
G2. Metal multilayer deposition:
Wordentec
E-beam evaporation
Starting from substrate: Cr/Au/Cr 10/300/40nm

G3. Lift-off
Ultrasonic acetone bath

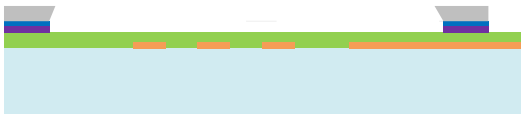
G4. CYTOP spin coating
Manual spinner: 800 rpm for 30s
Softbake: 120°C hotplate for 10min
Coating and baking done twice

G5. Polymer bonding with Spacing Wafer
EVG-NIL
Transparent alignment between Si_Cap, Glass_Polymer
Piston Force: 5kN for 1 hour
T = 120°C, p = 10^{-2} mbar

G6. Silicon wet etching
KOH bath at 80°C
Etch time: 2-3 hours depending on pre-etched depth



G7. Wet etching of Si_3N_4 residuals
bHF bath (etch time: 10min)

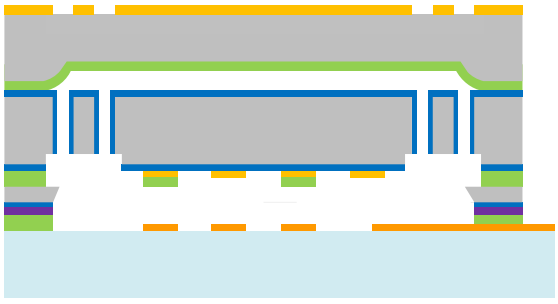


G8. CYTOP dry etching
RIE2
Recipe: feicy1 (O_2: 5 sccm; Ar: 20 sccm)

FULL DEVICE

Glass-device wafer bonding
EVG-NIL
Transparent alignment
Piston Force: 5kN for 1 hour
T = 120°C, p = 10^{-2} mbar

Chip dicing
Disco Saw



Appendix C

Equipment

- **ASE:** dry etching tool used for deep anisotropic etching of silicon using the Bosch process (DRIE), or for polymer etching using various gas compositions in the plasma.
- **DRIE-Pegasus:** state-of-the-art DRIE tool used for high-aspect-ratio anisotropic etching of silicon exclusively. Extremely high etch rates allow for fast processing.
- **EVG-NIL:** tool used for imprinting in polymers (Hot embossing) or wafer bonding with various techniques. For bonding purposes, the two wafers are first stacked on a chuck, kept at a small distance (typically 100μm) and manually aligned with the aid of a microscope. If one of the wafers is transparent, the two wafers can be aligned to each other directly (transparent alignment), otherwise each of them can be aligned separately to fiducial marks on the tool (crosshair alignment). After this procedure, the wafers are brought to contact and securely clamped to the chuck, which is transferred to a bonding chamber. Here, the wafers are pressed together by a chosen piston force at the desired chamber pressure and temperature.
- **KS aligner:** UV exposure tool with integrated mask alignment system. A 350W mercury arc lamp irradiates the wafer with an light intensity of $7\,\mathrm{mW/cm^2}$ at a wavelength of 365nm (spectral i-line of Hg). It follows that the exposure dose used in the process flow to pattern, say, 2.2μm of AZ5214E photoresist is $18.4\,\mathrm{mJ/cm^2}$ for a positive lithography. The photomask can be aligned directly to a pattern on the exposed side of the wafer, or front-to-back using fiducial marks on the the tool. A hard contact mode is chosen for all exposure steps in the process flow, meaning that a N_2 pillow provides additional force on the wafer against the mask.
- **Furnace: Bor-Drive-in:** tool used to grow a thin layer of silicon dioxide on both sides of a silicon wafer batch. The process can be dry or wet. In wet oxidation water vapor is added to the furnace to yield a higher oxidation rate at the cost of a lower film quality.
- **Manual spinner:** tool used to spin a wafer at the desired rotational speed and acceleration. The spin-coat solution is dispensed manually with a syringe or similar equipment.
- **PECVD 3:** tool used to perform Plasma Enhanced Chemical Vapor Deposition of a thin film onto a substrate.
- **Plasma asher:** tool used for isotropic plasma etching of a variety of materials, especially polymers.
- **RIE (1 and 2):** dry etching tool for shallow etching of various materials with a good degree of anisotropy and selectivity using Reactive Ion Etching.

- **SSE spinner:** automatic tool used to spin-coat a full wafer batch with the desired thickness of a standard type of resist. After spinning, wafers are transferred automatically to a hotplate for a soft-bake step. Wafers can be baked in contact or proximity mode.
- **Wordentec:** tool used for deposition of thin metal layers by means of thermal evaporation, Electron Beam Physical Vapor Deposition (EBPVD), and sputtering.

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