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Dipartimento di Elettronica e Informazione

Temperature control circuit for energy-dispersive X-ray imaging detectors.

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Sommario

Questo lavoro e' finalizzato allo sviluppo di un circuito *general-purpose* per la riduzione e la stabilizzazione della temperatura di sistemi di rivelazione per mezzo del controllo della corrente di una cella termoelettrica Peltier.

Il lavoro e' centrato sull'ottimizzazione di un modulo di rivelazione basato su un rivelatore a deriva controllata in silicio per la rivelazione di immagini bidimensionali di raggi X congiuntamente alla misura dell'energia di ciascun fotone X rivelato. In questo particolare tipo di rivelatore il raffreddamento del rivelatore e' essenziale per raggiungere la risoluzione energetica ottimale grazie alla riduzione della corrente di buio. E' altresi' importante stabilizzare la temperatura di lavoro del rivelatore in quanto, attraverso la mobilita' dei portatori, questa influenza la velocita' di deriva e, in questo rivelatore, la misura della posizione di incidenza. Sulla base di questi requisiti e' stato sviluppato e caratterizzato un circuito di controllo della temperatura.

1. Introduction

This work is focused on the development of a general-purpose circuit able to reduce and regulate the temperature of a detector system by controlling the current of a thermoelectric Peltier cooler.

Temperature effects on the achievable performances in a semiconductor detector are well known. Semiconductor detectors systems used for radiation sensing (e.g.

X-rays, gamma-rays, charged particles) feature a clear dependence of their energy resolution as well of their time resolution on electronic noise, on the reverse leakage current of the detector itself and on the transport properties of the generated signal charges. All these elements show a specific temperature dependence and therefore by controlling the detector temperature we would be able to improve the overall performance of the detection system.

In this work we focused on an existing detection module based on a Controlled Drift Detector, that is a novel type of 2D X-ray imaging device which also provides energy resolution of each detected X-ray. In this system the aim is to reduce the temperature as much as possible in order to reduce the integration of the leakage current that dominates at room temperature the overall noise of the system. However, as in this device the position measurement is obtained by means of the measurement of the arrival time of the signal charges at the collecting anodes, the stabilization of the operating temperature, not just its low value, is an issue because changes in the operating temperature during the acquisition will produce changes in the electron velocity by way of the temperature dependence of electron mobility and therefore in the measured position.

The developed circuit is based on temperature sensing from a Pt100 thermo resistor, placed in close thermal contact to the detector, which is read by an instrumentation amplifier block. This first sensing stage is followed by a second stage of the circuit where we make the comparison of the set temperature with the actual detector temperature sensed by the Pt100. The last part of the circuit controls the current in a Peltier cell whose cold face is in thermal contact to the ceramic board that holds the detector chip. Several options are included like temperature displays, frequency compensation.

Chapter 2 will describe the principle of semiconductor drift detector as it is useful to understand the principle of operation of these special type of detectors. Chapter 3 will describe the impact of temperature on the electronic noise and therefore on energy and time resolution. Chapter 4 will describe the developed circuit and the whole cooling system of the Controlled Drift Detector X-ray imager. Finally Chapter 5 shows the first experimental characterization of the system.

2. Silicon drift detector principles

2.1 Concept of the Silicon Drift Detector

The basic form of the Silicon Drift Detector (SDD) was proposed in 1983 by Gatti and Rehak .It consists of a volume of fully depleted silicon in which an electric field with a strong component parallel to the surface drives signal electrons towards a small sized collecting anode.

The outstanding property of this type of detector is the extremely small value of the anode capacitance, which is practically independent of the active area. This feature allows to gain higher energy resolution at shorter shaping times. recommending the SDD for high count rate applications.

To take the full advantage of the small output capacitance the front-end transistor of the amplifying electronics is integrated on the detector chip and connected to the anode by a short metal strip. This way the stray capacitance of the connection detector - amplifier is minimized, and moreover noise by electrical pickup (series

white noise) and microphonic effects are avoided. The collecting anode is generally discharged from signal electrons in a continuous mode. Thus the SDD can be operated with dc voltages with no detector dead time caused by a clocked reset mechanism.

Although the elaborated process technology used in the SDD fabrication the leakage current level can be so low that the drift detector can be operated with good energy resolution at room temperature, too (FWHM < 300 eV @ 5.9 keV). With moderate cooling by a single stage Peltier element the SDD's energy resolution (FWHM < 175 eV @ 5.9 keV) can already be compared to that of a Si(Li) or Ge detector requiring expensive and inconvenient liquid nitrogen cooling.

As the device is fully depleted the total thickness of 300 μm is sensitive to the absorption of X-rays. This feature translates to a detection efficiency > 90% at 10 keV and > 50% at 20 keV while at the low energy end the detection efficiency is limited by the transmission of the Be entrance window .

The spectrum of a Fe^{55} source recorded with a SDD at Peltier temperature (appr. -10°C) with Gaussian shaping of 0.5 μsec shows an energy resolution in terms of FWHM of the Mn-Kα line at 5.9 keV typically better than 175 eV. The active area of the SDD is 5 mm^2. Selected chips have a FWHM < 160 eV, as shown in Fig. 2.1. The peak-to-background ratio is typically 700, with a special collimator it is > 3000.

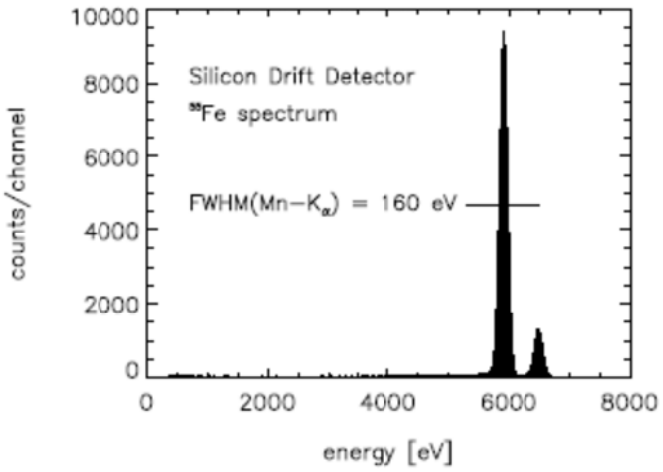

Fig 2.1 Fe spectrum recorded by a SDD with Peltier cooling (-10°C).

Due to its extremely small overall capacitance the SDD can be operated with very short shaping times and consequently at extremely high count rates. Fig. 2.2 shows the measured FWHM at 5.9 keV as function of the input count rate. Spectroscopic measurements are possible up to count rates close to 10^6 cps! .

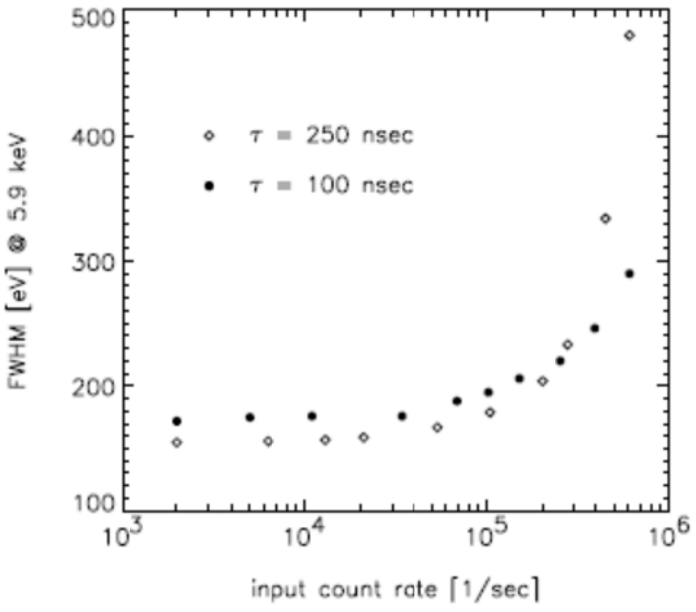

Fig 2.1 Energy resolution of the SDD at different input count rates.

2.2 The working principle of SDD

The working principle may be explained by starting from the diode (Fig. 2.3 And Fig. 2.4a) if one realizes that the ohmic N+ contact does not have to extend over the full area of one wafer side but can instead be placed anywhere on the undepleted conducting bulk (Fig. 2.4b).

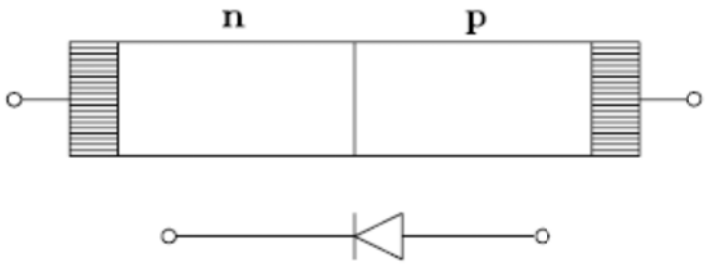

Fig 2.2 A p–n diode junction: structure and device schematic.

Then we have space to put diodes on both sides of the wafer (Fig. 1.4c). At small voltages applied to the N+ electrode, we have two space-charge regions separated by the conducting undepleted bulk region (hatched in Fig. 1.4). At high enough voltages (Fig. 1.4d) the two space-charge regions will touch each other and the conductive bulk region will retract towards the vicinity of the N+ electrode.

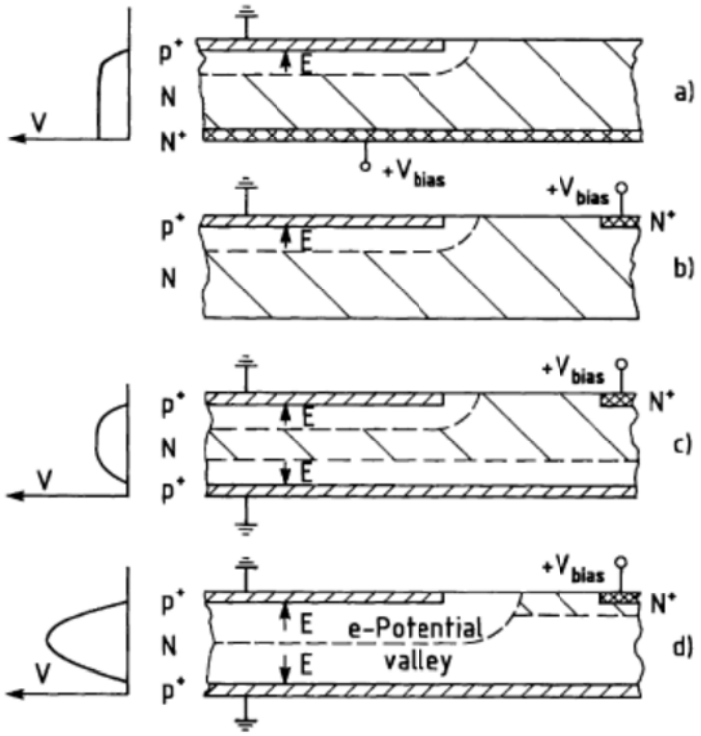

Fig 2.3 Basic structures leading towards the drift detector: diode partially depleted (a); diode with depletion from the side (b); double diode partially depleted (c); double diode completely depleted (d).

Thus it is possible to obtain a potential valley for electrons in which thermally or otherwise generated electrons assemble and move by diffusion only, until they eventually reach the N+ electrode (anode), while holes are drifting rapidly in the electric field towards the P+ electrodes.

Based on this double-diode structure with sideward's depletion, it is easy to arrive at a construction of the drift detector if one adds an additional electric field component parallel to the surface of the wafer in order to provide for a drift of electrons in the valley towards the anode. This can be accomplished by dividing the diodes into strips and applying a graded potential to these strips on both sides of the wafer (Fig 2.5).

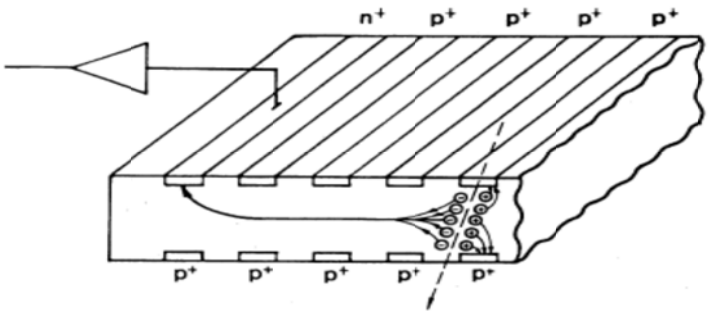

Fig 2.4 Principle of the semiconductor drift detector. An ionizing particle traverses the the detector and creates electron–hole pairs along its path. Holes are swept out to the p+-doped strips. Electrons move towards the potential valley and drift towards the collecting anode.

Other drift field configurations (e.g. radial drift) can be obtained by suitable shapes of the electrodes. Drift chambers may be used for position and/or energy measurement of ionizing radiation. In the first case the position is determined from the drift time. Furthermore, dividing the N+ strip anode in Fig 1.5 into pads, one achieves two-dimensional position measurement .

2.3 Illustrating the operation of a silicon drift diode

The silicon drift detector (SDD), sketched in Fig 2.6, uses a planar cathode but the anode is very small and surrounded by a series of electrodes. The SDD layout has cylindrical symmetry, so the anode is a small circle and the drift electrodes are annular. These electrodes are biased so as to create an electric field which guides the electrons through the detector, where they are collected at the anode. The rest of the signal processing electronics is nearly identical to that used with the Si-PIN diode. The small area of the anode keeps the capacitance very small. Since the active volume of the diode is enlarged by adding more electrodes with the same

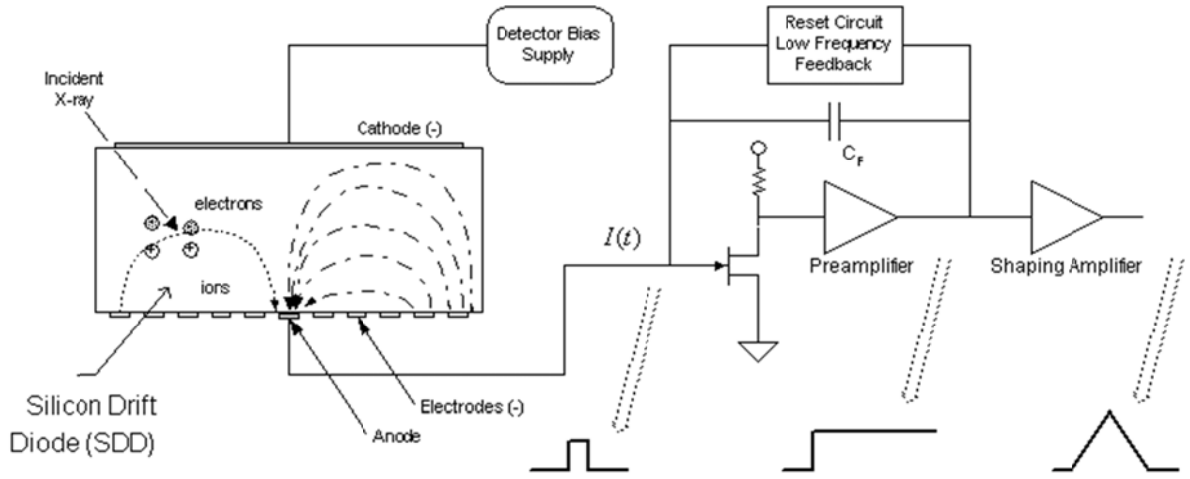

Figure 2.5 Sketch illustrating the operation of a silicon drift diode.

anode area, the input capacitance is independent of detector area. This is important because the dominant noise source in silicon X-ray spectroscopy is voltage noise, which is proportional to the total input capacitance and increases at short shaping times. The SDD, with its low capacitance, has lower series white noise, particularly at very short shaping times.

2.4 Readout of Semiconductor Drift Devices and Measurement Precision

As has been seen already, semiconductor drift devices are very well suited for both position and energy measurement. Compared with other position-sensitive detectors, such as strip detectors, they offer the advantage of a smaller number of readout channels while providing approximately the same position resolution (although at limited particle rates). Compared with other energy-sensitive detectors, such as large-area diodes, they have an extremely small detector

capacitance, and this leads to low noise (white parallel noise) and hence to excellent energy resolution.

Position is calculated from the time between primary ionization (the passage of the particle) and collection of the signal charge at the anode, while the energy is found from the total collected charge. As a consequence, optimization of electronics will depend strongly on the type of information required.

As the charge-transfer loss in silicon drift devices is usually negligible, energy resolution can be derived in the same way as for planar diodes but taking into account the very small detector capacitance. We therefore will concentrate here on position-measurement precision.

In order to measure the position, the readout electronics will in general convert the charge signal sensed at the readout electrode into a pulse or a bipolar signal. The center of this pulse, or the zero crossing of the bipolar signal, will be taken as a measurement of the arrival time.

The position measurement precision (i.e. the time resolution) is inversely proportional to the signal charge while it is directly proportional to the shaping time constant and to the electronic noise. Position resolution will therefore be limited by effects within the detector and by the electronic noise generated in the readout electronics. Effects of the first kind are:

- variation of the drift time with the depth of generation of the signal charge;
- widening of the signal peak due to diffusion and electrostatic repulsion, and the corresponding statistical fluctuations;
- dark current flowing in the detector.

The first of these effects is intrinsic to the detector and its influence on the measurement precision is independent of the properties of the readout system.

Reasons for this effect are inhomogeneities in the field distribution due to (for example) the finite width of the field-shaping electrodes and nonuniformities in crystal doping.
The second effect depends on the drift time - therefore on the position of incidence and electric field strength- and on the level of charge generation, while the dark current in the detector is to a large extent dependent on the quality of the technological process. In addition, it is a strong function of temperature. It can be reduced markedly when draining the surface-generated current to an electrode separated from the signal electrode.

The question of matching a detector with its readout electronics can be seen as choosing the optimal shaping of the signal in order to obtain maximum measurement precision. We will restrict ourselves here, therefore, to a few remarks. The width of the output signal pulse will be a convolution of the signal width due to diffusion and the shaping of the electronics. Superimposed on the signal is the electronic noise created by the dark current of the detector and by the readout electronics. As the shaping time is increased, it will produce a decrease of the series electronic noise but at the same time an increase of the contribution from the parallel noise. As the diffusion width is dependent on the drift field and the position of incidence of the radiation, each operating condition of the device would in principle require its own signal shaping condition in order to obtain optimum measurement precision. Furthermore, this optimum shaping is dependent on the point of incidence, the amount of ionization charge, and on the angle of incidence of ionizing particle tracks.

3. Impact of temperature on detector performance

3.1 Electronic noise

In order to satisfy the requirement on the energy resolution of the detector system, the contribution of the electronic noise $\Delta E_e(FWHM)$ must satisfy the following relationship:

$$\Delta E_e \leq \sqrt{\Delta E_{mr}^2 - \Delta E_i^2} \qquad (1)$$

where ΔE_{mr} is the required full-width at half - maximum energy resolution of a mono-energetic peak and $\Delta E_i(FWHM)$ is the intrinsic resolution of the detector, due to the unavoidable statistical fluctuation in the generation of the charge after the interaction of a photon with the semiconductor, expressed by :

$$\Delta E_i(eV) = 2.35\sqrt{F\ E(eV)\varepsilon(eV)}, \qquad (2)$$

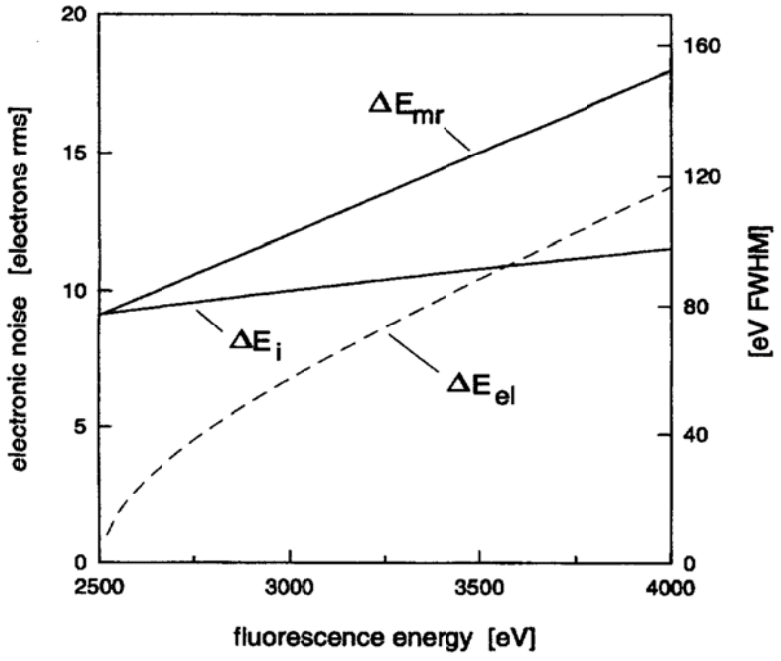

Fig 3.1 required energy resolution of the detection system (ΔE_{mr}), the intrinsic resolution of silicon (ΔE_i) and maximum acceptable value of the electronic noise (ΔE_e) are plotted as a function of the

fluorescence energy .experiment at low fluorescence energy are more demanding for the energy resolution because the separation between the fluorescence and scattering peaks is smaller.

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where F is the Fano factor (about 0.12 in the silicon at room temperature), E is the mean energy required of the photon and ε is the mean energy required to generate an electron - hole pair (3.62eV at 300K,and 3,76eV at 77 in silicon). In Fig. 3.1 the required resolution ΔE_{mr} as well as the intrinsic resolution detector ΔE_i and the maximum acceptable value of the electronic noise contribution ΔE_e is plotted in the range 2.5-4 keV. From the Fig.3.1 it's possible to see that the Eq.(1) can be satisfied only for energies greater than 2.5 keV ,because for lower energies $\Delta E_i > \Delta E_{mr}$ as shown as in Fig 3.1, the energy range from 2.7 to 4 keV, the required electronic resolution is comprised between 4 and 14 rms.

The contribution of electronic noise is usually expressed in term of Equivalent Noise Charge (ENC) that is the amount of charge which, applied as δ-pulse of current to the detector, would give at the output of electronic measurement chain a signal equal to the rms value of the output signal due to the noise only:

$$\Delta E_e(eV) = \frac{ENC\ (coulomb)}{q\ (coulomb)} \qquad (3)$$

Let's evaluate the ENC for the detector amplifier system represented schematically in Fig 2.2. the capacitance C_d includes the detector capacitance, the stray capacitance of the connection detector and preamplifier input capacitance C_i is usually the gate to source capacitance of the input JFET. The considered noise sources are: the series white noise a_w due to the thermal in the JFET channel, the series $a_f|f|$ noise of the JFET , and the parallel white noise b_w due to the leakage

current at the detector anode and parallel $b_f|f|$ noise due to the dielectric losses. it can be shown that :

$$ENC^2 = A_1 a_w C_T^2 \frac{1}{T_m} + A_2 \left[2\pi a_f C_T^2 + \frac{b_f}{2\pi}\right] + A_3 b_w T_m \qquad (4)$$

in which $C_T = C_i + C_d$ is the total capacitance at the preamplifier input and A_1 , A_2 , and A_3 are constant dependant on the type of shaping of the output pulse but not on the shaping time T_m.

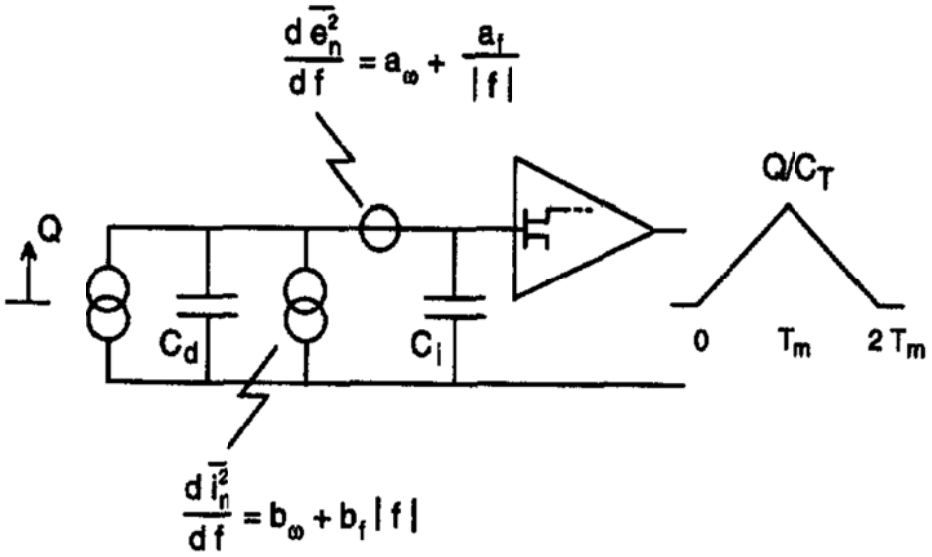

Fig 3.2 . schematic of the detector -amplifier system for the evaluation of the equivalent noise charge **.**

3.1.1 Series white noise

It is customary to describe the noise properties of the amplifier by a single series voltage source a_w representing the effects of all sources transferred to the input. The presence of this noise voltage will result in an output voltage even if there is no signal charge present. For an evaluation of the corresponding equivalent noise

charge, it is easiest to consider the charge necessary to produce the same effect of the noise voltage: ENC^2 due to series noise $=A_1 a_w C_T^2 \frac{1}{T_m}$ (5)

where : $a_w = \gamma \frac{2KT}{g_m}$, (6)

where γ =0.7 for the ideal JFET, k is the Boltzmann constant, T is the temperature, and g_m is the is the transconductance of the JFET . From Equation (5) we can see that this noise is strongly dependent on the total capacitance at the preamplifier input shown in Fig 2.3. From Equation (6) we can also see that there is a direct relationship between the series white noise and the temperature.

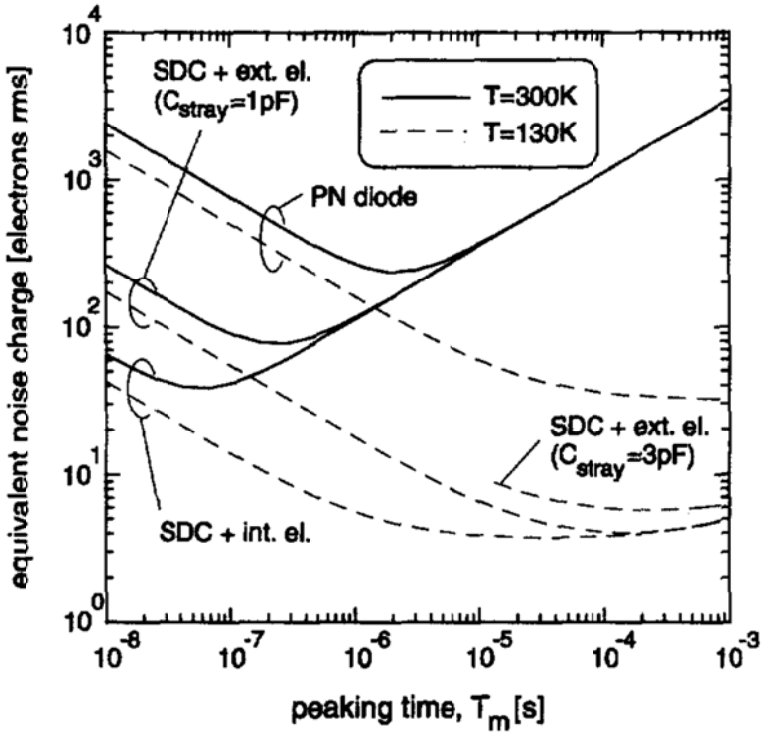

Fig 3.3 ENC versus peaking time ,at room temperature(solid line),and at 130k(dashed line).evaluate for three detectors: pn diode ,SDD for external electronics(for two values of stray capacitances) and SDD with integrated electronics.

In the silicon drift detector the input capacitance is very small, thus the series white noise become small become very small, but still if we decrease the temperature, the noise will become lower .

3.1.2 Parallel white noise

A realistic detector will draw some leakage current, which has statistical fluctuations. These fluctuations can be represented as a noise current source b_w feeding into the amplifier input. This current source b_w equal to :

$$b_w=2qI_l \qquad (7)$$

where I_l is the sum of leakage current of the detector and of the input transistor biasing current. In order to reduce the parallel white noise, we have to reduce the reverse leakage current which flows in the detector .

3.2 The leakage current

This leakage current in a p-n diode is generally a combination of diffusion current and generation current components: $q\sqrt{\frac{D_P}{\tau_P}}\frac{n_i^2}{N_D}+\frac{qn_iW}{\tau_e}$ (8)

where D_P is the diffusion coefficient, τ_P is the minority lifetime, W is the depletion width, n_i is the intrinsic carrier concentration, N_D is the dopants concentration, q is an electron charge, and $1/\tau_e$ is the generation rate in the depleted area.

The diffusion component is caused by the minority carriers generated in the neutral area, diffusing to the edge of the space charge region, and therefore it is independent of the applied reverse bias, at least until the full depletion is reached. If the generation centers are distributed uniformly, the generation component is

directly proportional to the depletion width, W; from which the generated carriers (minority and majority) are collected.

From the relationship in Equation 8 we can see that the leakage current is strongly dependent on the intrinsic carrier concentration. The leakage current increase with the increase of the intrinsic carrier concentration.

3.3 Intrinsic carrier concentration dependence on temperature

The thermal excitation of a carrier from the valence band to the conduction band creates free carriers in both bands. The concentration of these carriers is called the intrinsic carrier concentration, denoted by n_i. Semiconductor material which has no impurities added to it in order to change the carrier concentrations is called intrinsic material. The intrinsic carrier concentration is the number of electrons in the conduction band or the number of holes in the valence band in intrinsic material. This number of carriers depends on the band gap of the material and on the temperature of the material. A large band gap will make it more difficult for a carrier to be thermally excited across the band gap, and therefore the intrinsic carrier concentration is lower in higher band gap materials. Alternatively, increasing the temperature makes it more likely that an electron will be excited into the conduction band, which will increase the intrinsic carrier concentration. in the fig 3.4 shows the relationship between temperature and the intrinsic carrier concentration.

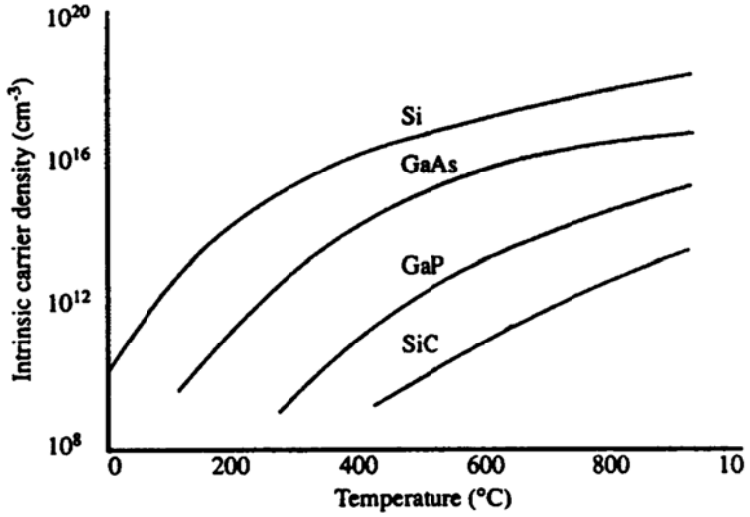

Fig 3.4 the relationship between temperature and the intrinsic carrier concentration.

3.4 Temperature dependence of SDD performance

The energy resolution of SDDs was studied by varying the temperatures from 100 K to 200 K. The squares and the left axis in fig 2.5 correspond to the energy resolution of an SDD in units of eV at 5.9 keV with statistical errors. The energy resolution is minimized to about 150 eV for SDD temperatures from 130 K to 200 K. Within this temperature range, the energy resolution is stable, but it becomes worse below 120 K. This effect might be attributed to operating limits of the FET.

The time resolution of an SDD, Δt_{SDD} was measured as a function of its temperature, presented on the right axis (circles) in fig 3.5. It improves with decreasing temperature due to the reduction of thermal noise. This temperature behavior was investigated by comparing Δt_{SDD} to the electron mobility in silicon because the time resolution is a measure for the electron travel time in silicon, reciprocally related to the electron drift velocity and the latter in turn dependent on the electron mobility.

The electron mobility in silicon is proportional to the temperature by the power law T^{-n} , with n around 2.5 for temperatures between 100 K and 300 K. Therefore the values for Δt_{SDD} were fitted with a T^{-n} function (solid line in fig 2.5):

$$\Delta t_{SDD}(T) = a.\left(\frac{T}{T_\circ}\right)^n + b \qquad (9)$$

with $T_\circ$ =300 k , The fit gives a = (2942 ± 63) ns , b = (190 ± 6) ns and, n = (3.00 ± 0.06). In order to understand the fit values a and b, a brief estimate of the relation of electron mobility and time resolution in our detectors follows: The electron drift velocity υ and the electron mobility μ are related via the drift field E:

$$\upsilon = E.\mu \qquad (10)$$

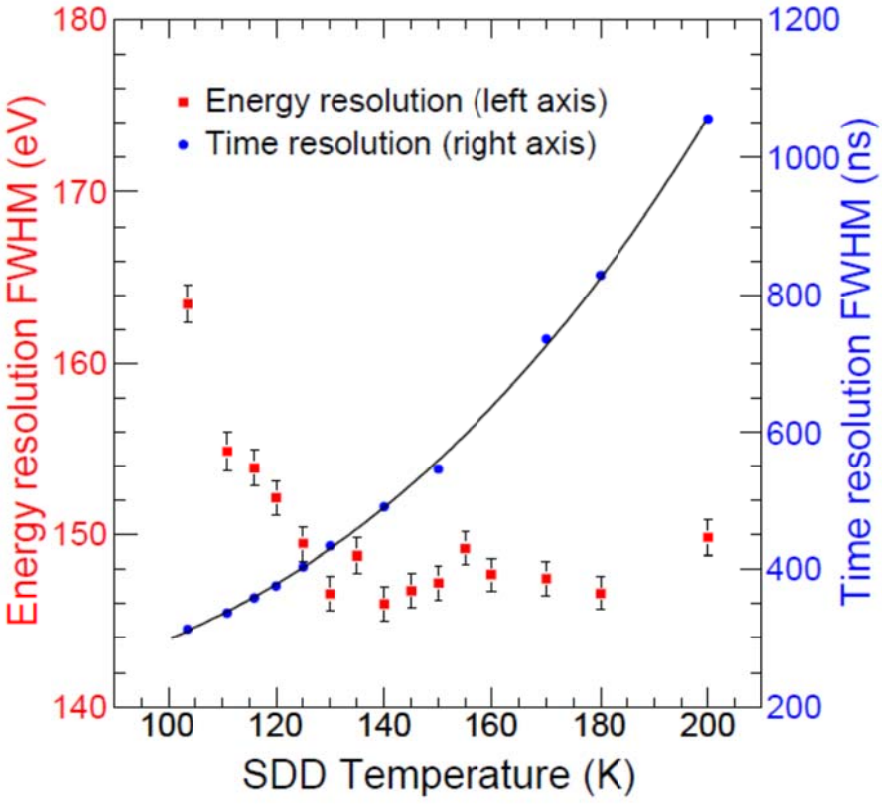

Fig 3.5 Energy resolution in eV (squares) and time resolution in ns (triangles) vs. temperature on SDD. The fit corresponds to a $\boldsymbol{T^n}$ function.

For the sake of simplicity, the drift field E in a two-dimensional and circular shaped assumed SDD with radius R can be described by the ratio of the voltage difference between center and edge to the maximum electron drift path R. Furthermore, the electron drift velocity can also be expressed as the ratio of its drift path in the SDD to its drift time. In this simple model, the difference between the maximum and the minimum electron drift time is taken as a measure for the time resolution Δt_{SDD}. From this it follows that the relation of time resolution and electron mobility can be expressed via:

$$\Delta t_{SDD}(T) = \frac{R}{\mu_{\circ}.E} \cdot \left(\frac{T}{T_{\circ}}\right)^{n} + c \qquad (11)$$

with $\mu_{\circ}$ as the electron mobility at the reference value $T_{\circ}$ and c as a constant, representing to Δt_{SDD}. at T = 0 K. In comparison with equation 9, it shows that the constant a thus includes geometrical characteristics of the detector, of the electrical field and of material properties.

Also the Mn-K_{α} peak center was plotted as a function of SDD temperature in Fig 2.6. Below 130 K the observed tendency might be caused by a reduced performance of the FET at low temperatures. Above 130 K, the peak centers show an increasing behavior with increasing temperature. The linear fit in fig 3.6 delivers a gradient of 0.19 channels perKelvin, which corresponds to 0.6 eV/K.

To understand this gradient, the behavior of the peak shifts was compared to the temperature dependence of the electron-hole pair creation energy in silicon. The SDDs' output signal height for an X-ray, from which the ADC derives a corresponding peak center, is proportional to the energy of this incident X-ray and therefore to the number of the created electrons. The number of created electrons on the contrary is inversely proportional to the electron-hole pair creation energy in

silicon. it decreases with 10^{-4}eV per Kelvin. Thus, the X-ray peak centers also might be shifted with increasing temperature by a factor of 10^{-4} of the incident X-ray which is consistent with the measured peak shift of 0.6 eV/K corresponding to 10^{-4} of the X-ray energy (5.9 keV) per Kelvin.

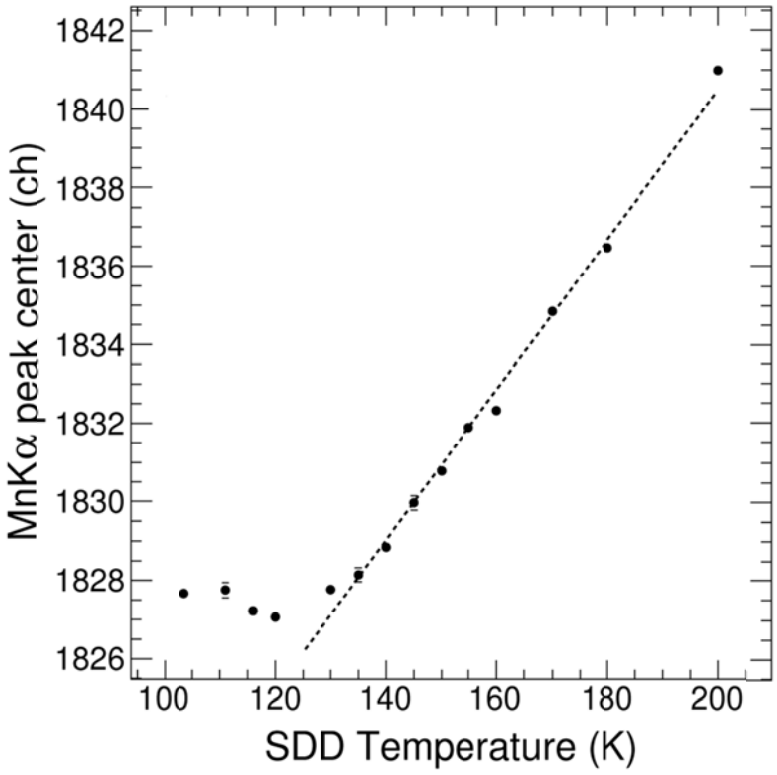

Fig 3.6 Mn-K_α peak center as a function of temperature on SDD. The linear shift occurring above 130 K and represented by the dashed line is due to the temperature behavior of electron-hole pair creation energy in silicon]. The shift of 0.19 channels/K is equivalent to 0.6 eV/K..

3.5 The motivation of our work

From the previous discussion we can conclude that, by controlling the temperature of the silicon drift detector and keeping it at low temperature, we can improve the resolution of detector (time and energy). In our work we developed a new temperature control system in order to pursue this.

4. Development of a cooling system for an X-ray imager based on a Controlled Drift Detector

4.1 Cooling system.

The introduction of a cooling system arises from the need to increase the energy resolution obtainable from the entire experimental apparatus, going to improve the performance, from the point of view of noise, the detector and the first part of the chain of signal acquisition. In this chapter the construction and operation of such an apparatus including the electronic system for regulating the temperature is treated.

4.2 Thermoelectric cooler (Peltier)

The basic idea behind the Peltier effect is that whenever DC current passes through the circuit of heterogeneous conductors, heat is either released or absorbed at the conductors' junctions, which depends on the current polarity. The amount of heat is proportional to the current that passes through conductors. The basic thermoelectric (Peltier) cooler unit is a thermocouple, which consists of a p-type and n-type semiconductor elements, or pellets. Copper commutation tabs are used to interconnect pellets that are traditionally made of Bismuth Telluride-based alloy, shown in Fig 4.1.

Thus, a typical thermoelectric cooler (TEC) consists of thermocouples connected electrically in series and sandwiched between two Alumina ceramic plates. The number of thermocouples may vary greatly - from several elements to hundred of

units. This allows to construct a TEC of a desirable cooling capacity ranging from fractions of Watts to hundreds of Watts.

When DC moves across Peltier cooler, it causes temperature differential between TEC sides. As a result, one thermoelectric cooler face, which is called cold, will be cooled while its opposite face, which is called hot, simultaneously is heated. If the heat generated on the TEC hot side is effectively dissipated into heat sinks and further into the surrounding environment, then the temperature on the thermoelectric cooler cold side will be much lower than that of the ambient by dozens of degrees. The thermoelectric coolers cooling capacity is proportional to the current passing through it. TEC's cold side will consequently be heated and its hot side will be cooled once the TEC's polarity has been reversed.

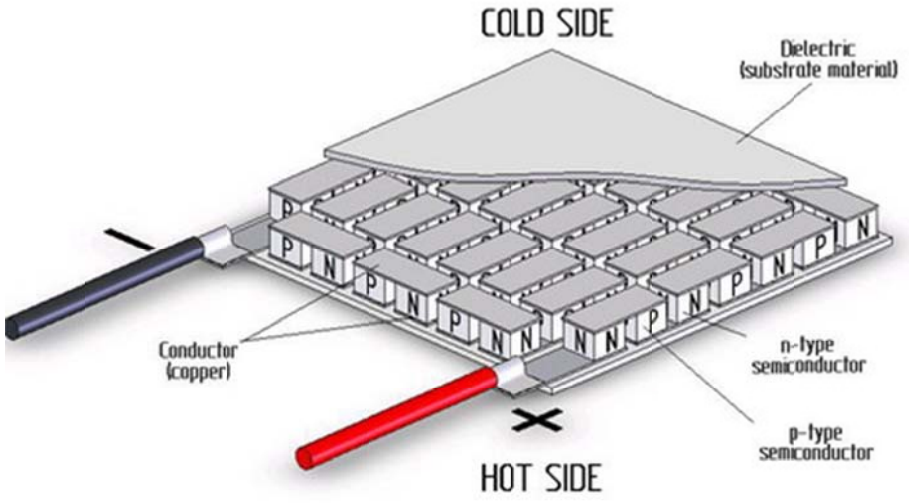

Fig 4.1 basic construction of the thermoelectric cooler (peltier).

4.3 Controlled Drift Detector system module

As we have seen in the previous chapter, the most important element to be cooled is the detector, in such a way as to reduce the dominant contribution of noise at room temperature related to the leakage current, and thus be able to discriminate energies much closer together. It is recalled that, around room temperature, the leakage current is reduced approximately by a factor of about 2 down to 8 ° C in temperature.

But, even the cooling of electronics closer to the detector may include some benefits. In particular the buffers present on the motherboard of the detector dissipate a power far from negligible that it degrades the performance with regard to the thermal noise, and contributes to heat the working environment (motherboard and detector box) also indirectly by influencing the detector itself. The structure currently realized only takes care of cooling the detector even if it has already been provided for a parallel structure very similar, and independent from the point of view of measurement and regulation of temperature, for cooling the buffer.

The detector chip is pasted on a ceramic made especially for the present system, which works as an interface with the motherboard with on board part of the electronics for the signal reading and the polarization of the device. The ceramic is formed by the superposition of three layers of alumina which are passed between the conductor tracks in addition to those present on the two outer surfaces to have a total of four levels of slopes. The tracks were then connected through micro-solderings or bondings to the motherboard and to the detector. Since the bondings

are very delicate and very close, to avoid any stresses that may detach them, the ceramic has been connected to the motherboard by means of four metallic tweezers, visible in Fig 4.2 on all four sides, which guarantee a good flexibility.
Inside the detector box, the motherboard and the detector are kept close to lid and then opening for the input of X-rays by four support spacers as shown in Fig 4.3. Below the entire ceramic is finally present a block of copper (detector block) that interfaces directly with the rest of the cooling system. To extract the power dissipated by the detector and transmitting it to the outside of the detector box, use is made of a Peltier cell that, in addition to being identified to ensure the required performance, it has the advantage of having a compact size and low cost. Initially there were two Peltier, to cool regardless of the detector and buffer, dimensioned according to an estimate of the dissipated powers to be disposed of.

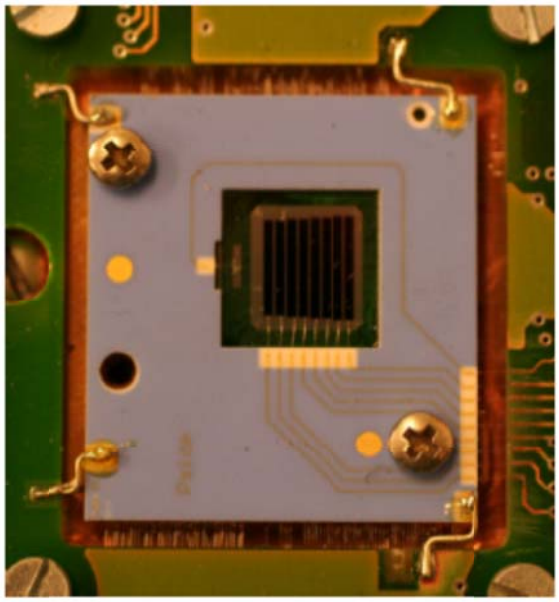

Fig 4.2 image of the detector used. You may notice on the four corners which support the ceramic tweezers where he was glued to the device. On the sides we can see the thin bonding linking the tracks on the motherboard with the ceramics. Below the ceramic is instead located a copper block for interfacing the ceramic with the cooling system.

As for the detector, taking into account the three resistive dividers and transistors integrated, the power dissipated in the worst case is about 250 mW and the Peltier chosen is able to dispose of 5.3 W.

Instead the current generators present on the motherboard and buffers, with a current of bias of 10 mA each and a Vds of 5V, dissipate overall equal to about 1.6 W; the Peltier chosen in this case is able to dispose of up to 33.4 W to cool the detector.

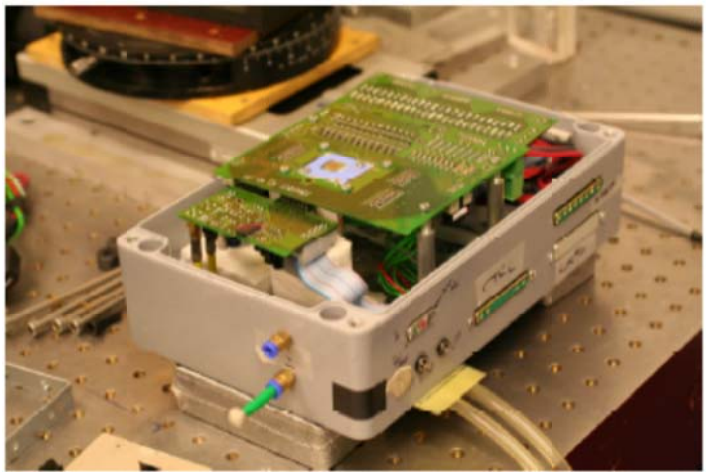

Fig 4.3 complete image of the apparatus of the detector consists of a motherboard suspended on four supports, by a tab switching to switch from the phase drift to that of integration, and by a tab host preamplifiers voltage.

Then the cell is supported on the bottom of the detector box, far away from the detector. This positioning is due to the fact that the Peltier to transport heat dissipates a power which is also not negligible, and it is desired to minimize the path of this flow of heat towards the outside to have no significant loss of temperature. As a link between the cold face of the Peltier and the copper block below the detector has been inserted a structure consisting of two major blocks of copper, one horizontal resting along the entire face of the Peltier and one vertically

above it, and a final strip between the vertical block and the detector block as shown in Fig 4.4.

This band allows the flexibility needed to be processed at the time of assembly of the apparatus so as to be positioned correctly below the locking detector without introducing excessive voltages that may break the bondings. However because of the reduced section, it constitutes a bottleneck for the transported power and consequently produces a temperature drop across its terminals that will be quantified later.

In order to reach the lowest temperature achievable by the system, the heat dissipated by the cell and delivered on the hot face and then on the bottom of the box is disposed of by means of a heat exchanger copper, screwed on the outside and in which is slid a flow of water. The water is kept at a temperature of 15 ° C by means of an external cooler.

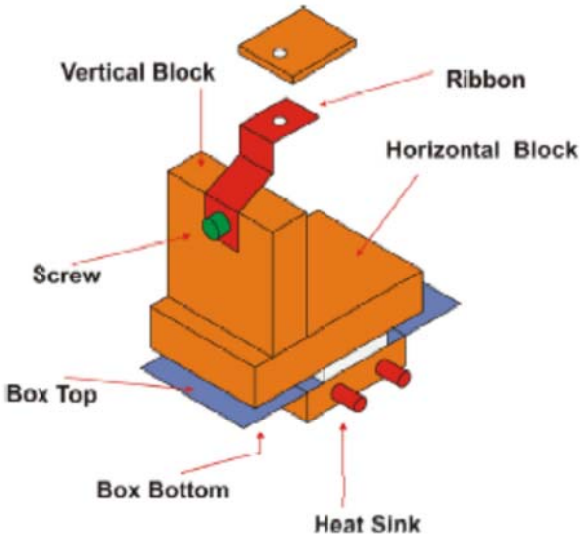

Fig 4.4 diagram of the structure built to transport the heat from the copper block present in the pottery of the detector to the cell peltier. A strap, indicated in the figure with Ribbon, the system guarantees the necessary flexibility to not blow the bondings of the detector during assembly.

Optionally you can keep the water at lower temperatures (with suitable liquids even to values below 0 ° C) but there is a risk that the occurrence of condensation on the bottom of the box that may short the electronic circuit.
The same issue is also present within the detector box, so even worst for low temperatures achievable (to below 0 ° C) where it would formation of ice due to water vapor in the air, and consequently possible short circuits could happen, which could damage the detector and control electronics. To overcome this problem the box of the detector (detector box) is completely sealed and through two openings, nitrogen can enter and expel the air and humidity present. Inserting inside a sensor for humidity reading was possible to monitor any interruptions in the flow of nitrogen to allow to turn off as soon as the cooling system.
The system is completed by the box containing the electronics that takes care of the measurement and display of temperature and electronics for the control of the Peltier with the purpose of maintaining the desired temperature value. For the temperature measurement is made using a PT100 bonded to the ceramic of the detector.

4.4 Thermal model of the system

Because the system is realized constituted by real elements, due to the finite thermal conductivity and the reduced section, all the parts used have a thermal resistance to heat flow transported. The consequence is a temperature difference between the two heads of the various blocks used, which results in a reduction of performance achievable by the system and the minimum temperature at which the flow rate can be ceramic of the detector. For an estimate of the performance obtainable with the system realized you can build one equivalent electrical diagram

shown in Fig 4.6 , in which the various elements used are modeled according to their size and thermal conductivity.

The first element to be analyzed is the Peltier cell whose main characteristics are reported here in table 1:

Qmax	33.4 W
ΔTmax	67 °C
Vmax	15.4 V
Imax	3.9 A

table 1

This cell is capable of transferring a thermal power from a side of said cold face to another said hot face thereby creating a difference ΔT at its ends. The Peltier used is able to provide a ΔTmax = 67 ° C polarized with the maximum current and zero load, that is with zero heat flow. By increasing the flow of heat transferred ΔT obtainable decreases linearly as can be seen in the graph in Fig 4.5

With maximum load ,that is a transfer of power equal to 33.4 W, the ΔT obtained would be invalid. In the ideal case the power to be transferred would be only that of the detector, over a factor of 100 below the maximum power which can be dissipated, and then the ΔT would be close to 67 ° C, but in the actual situation in the flow joins the power transported by convection from buffers and preamplifiers.

for transporting the heat, the cell dissipates the same power that must be disposed of from the hot face through the heat exchanger with water at 15 ° C, taking care to reduce the one that returns to the cold face through alternative routes. For this

purpose to fasten the blocks of copper, supported above the peltier, with the bottom of the box, have been used nylon screws that have low thermal conductivity.

The cell also is not in operation at maximum current of 3.9 A, but is limited to a value of 3.3 A to increase the operating life and does not damage it. It can then be modeled approximately as a voltage generator with a value Fd ΔT ideal little above 60 ° C in series with its resistance Rd, with a value 2 K / W, which takes into account the reduction of ΔT due to the flow of heat transferred . The model is completed by a current generator Pd on the hot face of the value of 50 W which takes into account the electrical power dissipated by the cell.

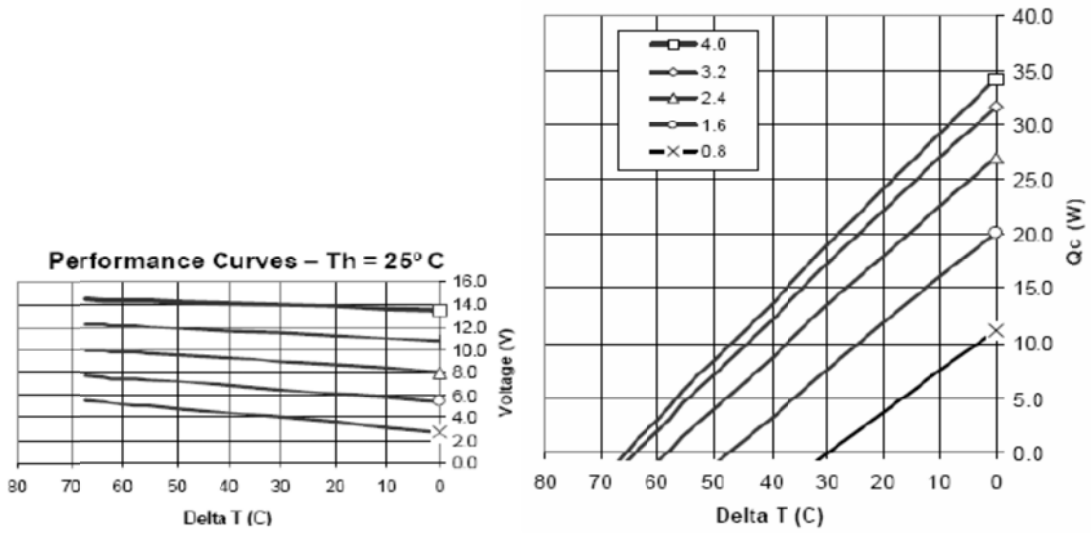

Fig 4.5 characteristic curves of the Peltier cell selected for cooling the detector. From the curves of the right is known as the temperature difference achievable between the hot face and cold face becomes zero when the device is intended to transport the maximum heat flow for which it was designed.

The resistance indicated with Rpd instead represents the thermal resistance of the parallel path to the Peltier cell, characterized mainly by the fixing screws of the

column of copper with the bottom of the box. The calculated value due to the four screws 3mm nylon used is of about 1470 K / W which is a good thermal insulation.

The connection between the cold face of the Peltier and the copper block below the ceramic consists of the contribution due to the copper block horizontal and vertical with a total resistance of 0.21 K / W, totally negligible compared to the resistance introduced by 4 cm the ribbon threaded between vertical block and block detector. The resistance, indicated with Rp, is about 16 K / W, and may result in a fall of less than 4 ° C taking into account only the flow of power coming from the detector.

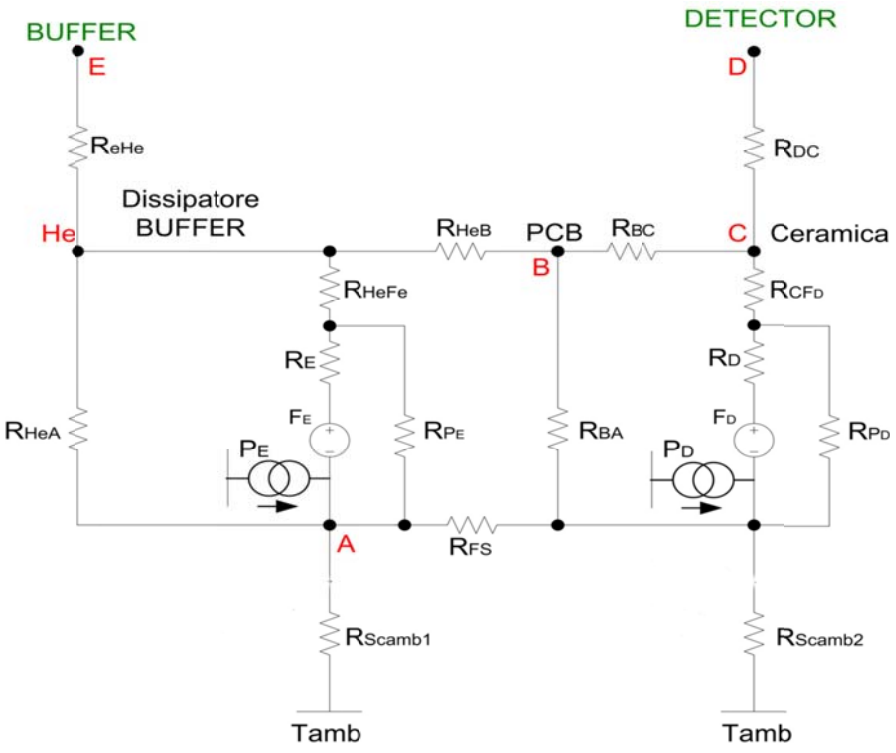

Fig 4.6 circuit diagram constructed to evaluate the theoretical performance obtainable with the system designed to transport the heat from the detector and from buffers to heat exchangers.

The resistance indicated by Rbc is the most important, it links between the pcb motherboard (and therefore the area incorporating the buffer) and the cooling circuit of the detector with the ceramic and the copper column. . The contribution to this resistance is given by the bonding of very high value, with a size of 104, because of the small supply section (diameter of 25 microns), while the preferential path for the heat, placed in parallel, is linked to the four tweezers metallic support of the ceramic. This results in a total value of around 280 K / W. In complete project, then cooling also buffers, a high value for this resistance is desirable in order to maintain isolates the two systems of cooling and can adjust them independently.

Finally Rdc represents the thermal resistance offered by the path between the detector chip and the copper block at the bottom of it, consists mainly of the glue fixing the chip to ceramics and ceramics same. Its value is around the 8.2 K / W and with 250mW of power which crosses add a drop of 2 ° C.

The resistance of the heat exchanger and that of the bottom of the box are negligible, around 0.015 K / W and even if the power that passes through them is high even having to move the energy dissipated from the cell, the thermal head and limited (less than 1 ° C).

Regarding buffers the project, still to be realized, requires a further Peltier cell identical to that used for the detector, and modeled in the diagram with Fe, Re and Pe and parallel with the usual thermal resistance offered by nylon screws Rpe. Above the peltier is thought to realize a column of copper similar to that used for the detector, connected in this case by means of two flat plates to a further block of copper fixed to the motherboard shown if Fig 4.7 .

The resistance RHeFe takes into account all the contributions to this process and is about 3.3 K / W. The further indicated resistance with Rehe takes into account the thermal connection between the buffer and the beginning of the pedestal of copper relative to them, and the fact that the transistors are located on the opposite side of the pcb and those where it is fixed the final block of column cooling. Taking into account the size of the area concerned and the thermal resistivity of *vetronite* the calculated value is 4.6 K / W. The Rheb resistance is the resistance of the residual path of the motherboard between the pedestal of heat dissipation of the buffer and the area of the detector, which falls to be added to Rbc presented previously.

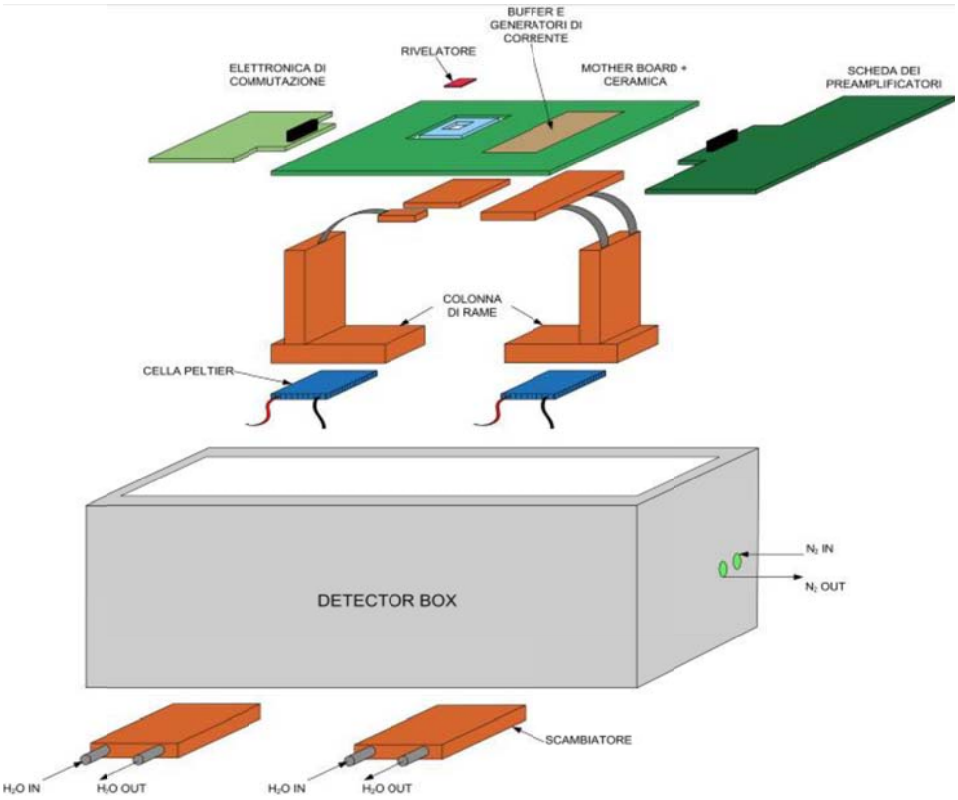

Fig 4.7 complete diagram of the apparatus designed to cool the detector and thermal buffers.

Even this resistance is of high value, 520 K / W helping to isolate the two cooling channels. The diagram also shows the strengths and Rhea Rba representing alternative paths between PCB and bottom of the box, mainly due to the support pillars of the motherboard and the transport of heat by convection.

It therefore remains to estimate the temperature drop undergone by the water flow in the heat exchanger. The duct portion taken into consideration is that between the inlet sections and outlet of the heat exchanger. If we assume a steady state, conservation of energy requires that the incoming energy per unit time in the heat exchanger is equal to the outgoing one. In reference to figure then the power to the outlet section of the heat exchanger holds:

$$P_o = P_i + P_d \qquad (12)$$

where Pd is the power to be dissipated in the heat exchanger inlet. Even for the mass of water which passes through the exchanger unit of time mh2o [kg / s], said flow rate, the same principle applies. At this point it is necessary to define the thermal capacity of the fluid with regard to the flow rate using the specific heat at constant pressure water C_{PH_2O} = 4186 [J / (kg * K)]: (13)

capacity of heat flow $C_{H_2O} = m_{H_2O}.C_{pH_2O}$ (14)

Consequently, the thermal power absorbed by the water is equal to $C_{H_2O}.(T_o - T_i)$

where T_o and T_i are respectively the temperatures of the water at the entrance and exit of the heat exchanger. For the first principle exposed this power corresponds to the power Pd to be disposed of, and then:

$$P_D = C_{H_2O}.(\Delta T) \qquad (15)$$

With a power P_D to dissipate around 60 W, due for the most part to the electrical power of the Peltier cell, and a minimum flow rate of the chiller of 11 l / min, the DT obtained should be less than 0.1 K.

In theory, considering only the power dissipated by the detector and the resistance overall crossed towards the heat exchanger, one could cool to -38 ° C with the water temperature maintained at 15 ° C. Now it remains to estimate the temperature reached under field conditions, having also dissipate some of the heat from the environment inside the detector box.

4.5 Electronics for the closed loop regulation of the temperature

As we have discussed previously, the temperature does not intervene only in the amount of noise of the detector but also modifies the mobility of the charge carriers. A variation of the temperature behaves accordingly also a variation in the time of drift of charge packets from the pixels to the anodes. Choosing the desired working temperature is very often important to keep it stable as possible for the entire duration of the measurement made. This reduces the variation in the enlargement of the electron cloud from acquisition to the next. So you can get more precise measurements with only one initial calibration of the detector. At the same time allows to simplify the reconstruction of the scanned image since the drift time of the center of each pixel remains constant.

The cooling system is completed by an electronic control box outside the detector with which you can monitor the temperature of the detector, set the desired temperature and edit it by means of the Peltier. In summary the electronic acts as a linear closed loop within the system since it reads a temperature, compares it with the temperature set by the user and, based on the difference detected and the

control method implemented, acts on the Peltier cell's current to match the two values.

The system is composed by three main blocks: the first is in charge of the temperature reading by means of a PT100 resistance, the subsequent amplification of the corresponding electrical signal and of its packaging, so as to have it in an easily readable format, for example with a tester; the second compare the measured temperature with the desired temperature and implements the type of adjustment chosen also taking care to keep the temperature stable over time and to limit the oscillations that can occur in closed loop. The third block then functions as the power stage and controls the Peltier cell, by setting the current that flows according to the signal coming from the regulator block.

To supply the electronic control system of the temperature is chosen a voltage of 15V because the cell Peltier from 33.4W can be polarized to the maximum with this value. Since it was decided to feed every block with the same source, all other voltages required and all references are machined from a suitable bias network

4.5.1 Thermo resistor PT100

The heat resistance, commonly called resistance thermometer is a temperature sensor that exploits the variation of the resistivity of certain materials as the temperature varies. In particular for metals there is a linear relationship that binds resistivity and temperature:

$$\rho(T) = \rho_o(T_o).\{1 + \alpha(T - T_o)\} \qquad (16)$$

where T is the temperature , $\rho(T)$ is the resistivity of the material at a temperature T, ρ_o is the resistivity of the material at a temperature T_o ,and α is a coefficient that

depends on the material = 0.00358° C^{-1}. Exploiting the relationship between resistance and resistivity (via the section S and the length L of the conductor):

$$R = \frac{\rho L}{S}$$

we obtain that:

$$R = R_o.\{1 + \alpha(T - T_o)\} \qquad (17)$$

with R_o = 100Ω .so at T=T_o ,we sense 0 degree.

4.5.2 temperature reading Circuit by PT100

The temperature is measured by a PT100 resistance welded as close as possible to the detector. In particular the resistance, which has a flat side and thermally conductive in order to better adapt to the surface to be measured, has been welded on ceramic support to the detector. Since the resistance requires a bias current, the link from the ceramic to the box containing the electronic control takes place by means of four wires, two for the polarization and two for reading, so as to measure only the signal and not the voltage drops that occur along the path.

In Fig 4.8 is the schematic of the proposed analog circuit that deals with the reading and the polarization of the signal coming from the PT100.

The circuit is polarized between the ground (VEE) and +15 V (VCC) supplied from an external power supply while analog ground is defined a referenced by the signal along the amplification chain. The analog ground is derived from +15 V via a suitable network present on the second tab, that of the temperature regulation.

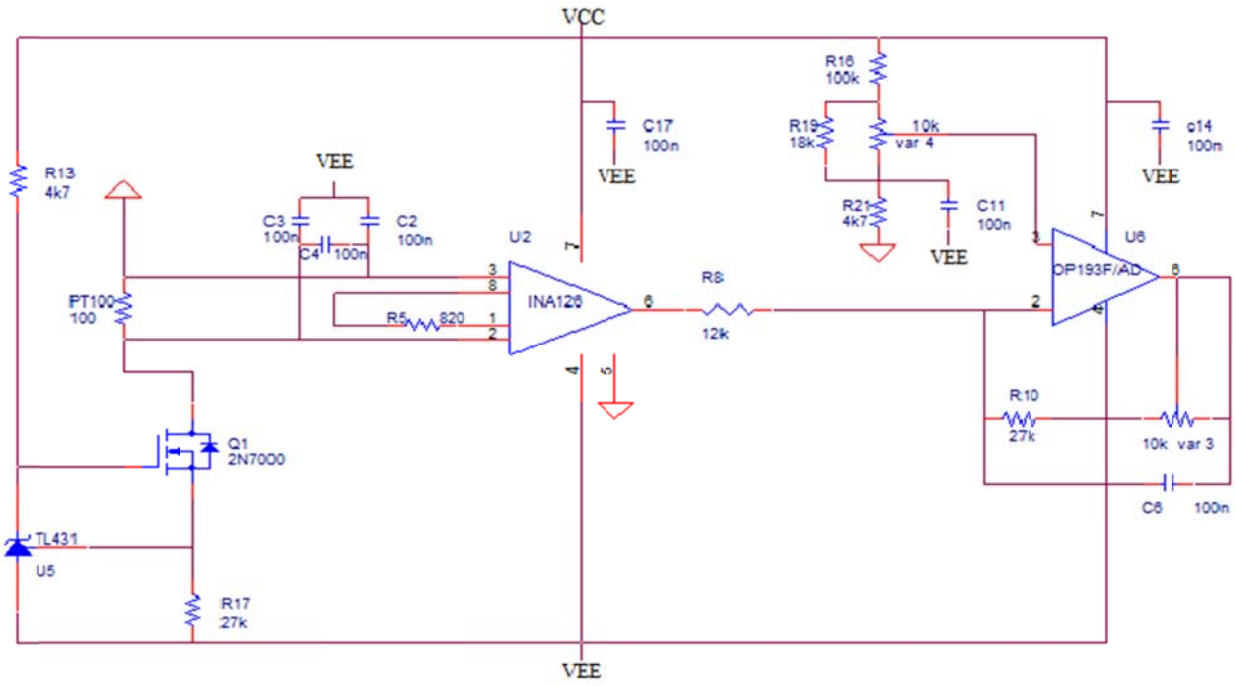

Fig 4.8 circuit diagram of the circuit reading by PT100 temperature.

The PT100 is biased with a fixed current delivered by the current generator formed by the transistor Q1, the regulator U5 and the resistance R17. The regulator TL431 used maintains the two terminals of interest a voltage of 2.5 V. This voltage that falls to the heads of R17 = 27 k produces a current of about 93 µA. this current drained to the PT100 through the transistor Q1 (2N7000) .

From the previous part we have got that the value of PT100=100 Ω at 0℃. so that we will read a voltage at 0℃ due to the bias current:

$$V_{os} = R_{PT100} * 93\ \mu A = 9.3mV \quad (18)$$

This offset must be deleted from the circuit that follows in order to have a voltage differential with respect to the analog ground of 0V to 0 ° C and make easier the conversion of the signal. if there is one degree difference between $T\ and\ T_o$:

$$R = 100 * \{1 + 0.00358\} = 100.358\ \Omega$$

so the difference in the resistor per degree equal to $\mp$ 0.358 Ω ,so For each degree of difference is obtained a useful signal (without the offset component) of input equal to $\mp$ 35.8 μv .

The signal undergoes a first amplification by means of an input stage with an INA gain set by R5 equal to :

$$G = 5 + \frac{80\ k\ \Omega}{R5} \qquad (19)$$

and R5 its value selected to be 820 Ω ,so the gain equal to 103. Output of the amplifier is thus obtained a signal of about 3.7 mV / ° C, relative to analog ground and the offset is not yet eliminated.

A second stage, constituted by the amplifier U6 OP193F in the figure, allows to amplify the signal again to obtain outgoing -10 mV / ° C. The required gain calculated as ratio (var3+ R10) / R8, finely adjustable via potentiometer var3 feedback, is therefore approximately equal to - 2.7 shown in this equation:

$$G_{op193} = \frac{R_{10}+ver_3}{R_8} \qquad (20)$$

where R10=27k Ω ,ver3=10k max, and R8=12K. This second stage also takes care to remove the offset by comparing the input signal with a negative voltage, adjustable by trimmer var4, positive input.

This trimmer has been adjusted so as to give a voltage equal to about Vos · GINA 2.7/3.7 ≅ 0.7V, obtained by dividing the offset, amplified output to the second stage, for the gain seen from the entrance of positive 3.7. As for the signal at each node of this first circuit, also the comparison voltage for the elimination of offset is referred to the analog ground (AGnd) which equal to 4.256 V. the range of the voltage entering to the - input of U6 can calculated like the following equations :

$$V_1 = \frac{R_{21}}{R_{16}+R_{21}+R_{19}||Ver_4}(VCC - AGnd) \qquad (21)$$

$$V_2 = \frac{R_{21}+R_{19}||Ver_4}{R_{16}+R_{21}+R_{19}||Ver_4}(VCC - AGnd) \qquad (22)$$

where V_1 , V_2 are the voltages which can appear on the negative terminal of the amplifier OP193F in two cases ,when the trimmer at low and high values , R_{21}=4k7 Ω , R_{16}=100k Ω , $R_{19} = 18$ kΩ , Ver4 = 10 kΩ max. from calculation we have got difference in voltage between them ≅ 0.7V over the analog ground and that's what we need to eliminate the offset voltage comes from the INA.

The differential signal output from the circuit with respect to the analog ground will then be negative for temperatures above 0 ° C and positive for lower temperatures.

4.5.3 Temperature regulation and control of the Peltier current

On a second stage Fig 4.9 were made the following sections of the control system: the network that implements the type of operation to be performed, the network of power for driving the Peltier cell. This stage receives in the input, the voltage value of the read and amplified PT100 and provides in the output, the current require for the Peltier.

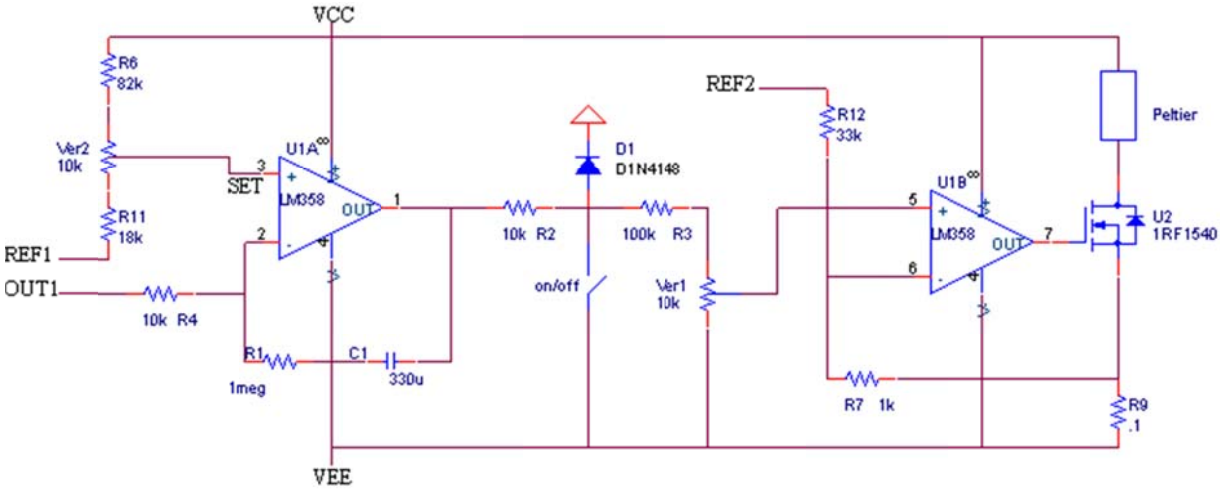

Fig 4.9 circuit diagram of the board of temperature regulation and control of the Peltier cooler.

The first stage of the circuit , constituted by the amplifier U1A, compare the voltage proportional to the measured temperature (OUT1) with a reference voltage proportional to the temperature (SET) to be obtained on the detector. As for the signal from the reading stage , even the reference voltage will be negative for temperatures above 0 ° C and positive for lower temperatures. If the measured temperature is higher than the set output of this stage rises to the positive supply and it lead the power stage to work.

The range of the SET voltage proportional to the required temperature can be calculated from this equations:

$$SET\ voltage\ min = \frac{R_{11}}{R_{11}+R_6+ver_2}\ (VCC - REF1) \qquad (23)$$

$$SET\ voltage\ max = \frac{R_{11}+ver_2}{R_{11}+R_6+ver_2}\ (VCC - REF1) \qquad (24)$$

where $REF1$ is one of the reference voltages which will be discussed in the next part. $REF1 = 1.75v$, R_{11}=18k, ver_2=10k max , and R_6= 82k. after calculation the

SET voltage will be between 2.17v and 3.373 referred to REF1,the corresponding temperature range will be between (35 ℃ and -87 ℃).

The second stage shown, constituted by the amplifier U1B and the power transistor IRF1540, sets the current in the Peltier cell as a function of the control voltage coming from the first stage.

The feedback amplifier operates in practice as a buffer and, by acting on the Vgs of the transistor, brings the voltage read on the positive input terminal and to the heads of the power resistor R9 = 0.1 Ω. The current that is invoked by the transistor through the load is the same as that flowing in the resistance.

The diode D1 between the first and the second stage performs a camping voltage to about 0.7V above the analog ground and limits the current flowing through the resistive divider following. By means of the trimmer var1 is instead possible to set the limit value of the current that can flow in the load. For the present system, it was decided to set the maximum current in the cell Peltier to 3.3 A

To avoid the risk of destroying the device, a value that corresponds to a maximum voltage, set by the trimmer on the input terminal, of 340 mV and obtained when the output of the stage regulator rises above the value for camping of the diode.

Given the high value of the current request, in addition to cell Peltier also the transistor used must be able to dissipate a high power during certain operating conditions, especially when the cell is working with half of its maximum current. The value to be disposed of is in fact of 14.6 W for a current of 1.95 A. To dispose of as much as possible the heat generated, the transistor has been screwed to a heat sink with fan in such a way that the maximum temperature not ascended above 60 °C. However in purpose apparatus that value should be reached only during the transition phases as for the temperatures of the operating conditions provided

below 0 °C the cell is working with a current exceeding 3A and a negligible dissipation on the transistor.

The switch is used to switch on or switch off the second stage of the power transistor thus will also switch on and of the Peltier.

4.5.4 The derivation of the reference voltages

All references used in this circuit are derived from the part of the circuit shown in Fig 4.10. One of the two regulators used TL431 (U7) fixed 2.5 V across the resistor R14 = 10k and consequently a current of 250μA. The same current flows through R1 so as to obtain a total voltage drop at the terminals of the two resistors 10.75V. The analog ground (AGnd) used as reference for PT100 signal is fed to the lower end of R14. Its value is 15v-10.75v =4.25v.

A second reference value, indicated in the figure with REF1, is maintained at 2.5V below the analog ground, then to 1.75V. The last reference, indicated with REF2, is set by diode D2 to approximately 0.7 V above the negative supply (VEE) of 0V. Be noted that all references used within the chain of reading and comparison of the signal are connected to analog ground in turn maintained at a fixed distance to either the positive.

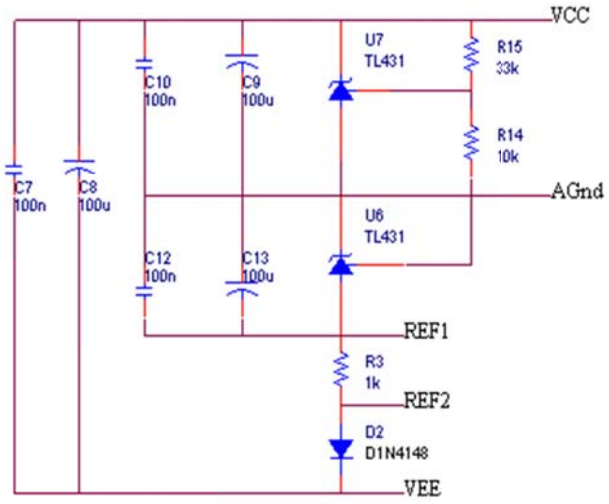

Fig 4.10 circuit diagram of the network made to derive the references used in the readout circuitry and temperature control.

This means that any noise or variations on the +15 V do not affect the correct processing of the signal. This is an important feature for the stability of the readings since for feeding the power stage and the stage of reading using a single source, and under varying conditions of current consumption of the Peltier cell are obtained falls of some tens of mV on the cables variables over time.

4.6 The PC board

We have done the layout in two layers(top and bottom) shown in Fig 4.11. All the component will be on the top layer mostly all the tracks will be on the bottom layer. In the bottom layer we have put the ground plane by using copper pour. The dimension of the layout is 60 mm × 100 mm.

In the Fig 4.11, PT100 will be mounted through wires in the connector J1. the connector J1 is a four way connector and its pins will be connected to four pins shown in the table1 :

the pins 2 and 3 used to measure and amplify the voltage over the PT100 by INA126,while pins number 1and 4 used for polarize the signal into PT100

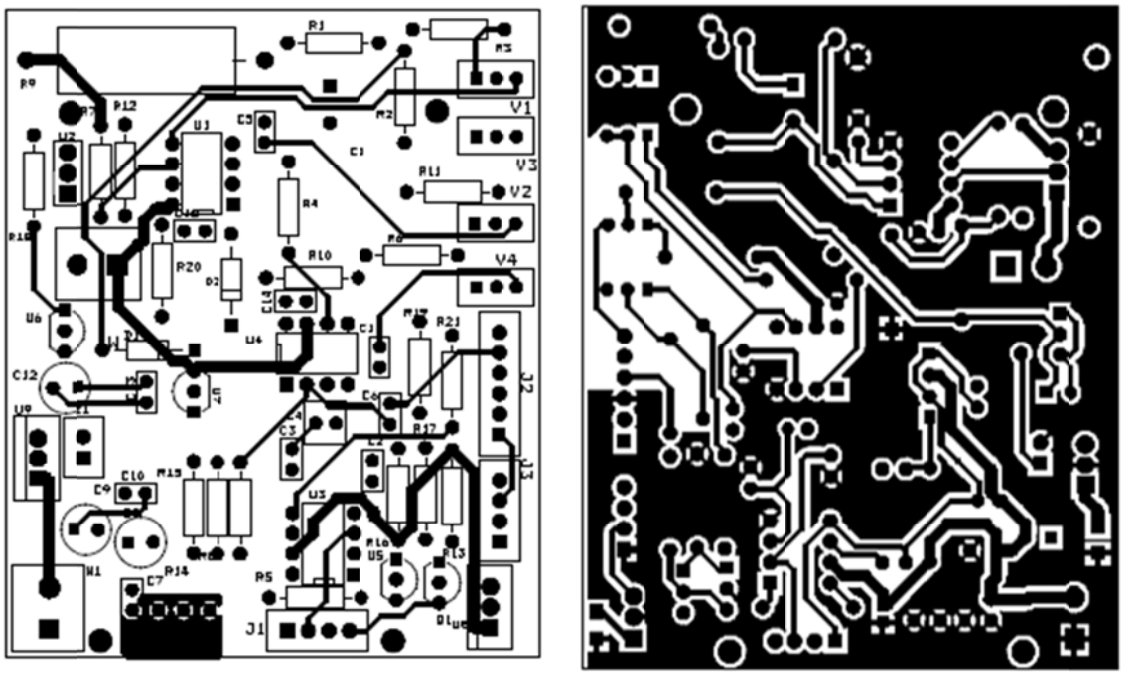

Fig 4.11 top and bottom layer of the LAYOUT

Pin number	Connected to
1	Analog ground (AGND)
2	+In of INA126
3	-In of INA126
4	The drain of transistor 2N7000

table 2

All the vias are metalized and the thickness of the copper is 35µm Cu .the thickness of the board is 1.6mm.

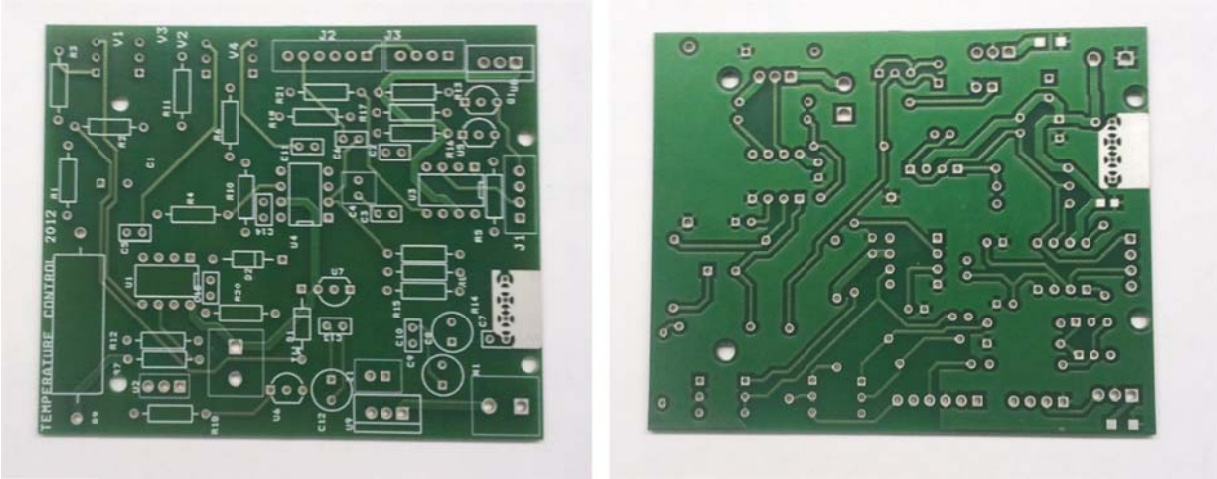

Fig 4.14 top and bottom layer of the PCB board

the connector J2 used to connect the reading voltage proportional to the reading temperature ,the measured voltage proportional to the measured temperature ,the ground VEE ,the analog ground AGnd ,and the reading voltage of the humidity sensor proportion to the humidity .the order of pins will be shown in table 3:

Pin number	Connected to
1	Humidity sensor reading
2	NC
3	VEE
4	AGnd
5	Measured temperature
6	Reading temperature

table 3

all this points will be connected to the through wires from the connector to the selector MRX 204 shown in Fig 4.12:

Fig 4.12 selector MRX 204

this selector is a double poles with four positions selector .we connect VEE and AGnd to the 2 poles in the selector . we will use three position for the measured temperature ,the reading temperature, and the humidity reading . this selector connected to a voltammeter display DPM160 will be discussed later .

The connector J3 is used to connect the voltage required for the humidity sensor, and to connect the humidity reading from the connector for the Peltier through wires to the connector J2 in the PCB board .the order of its pin shown in table 4:

Pin number	Connected to
1	VEE
2	Voltage required for humidity sensor
3	Reading of humidity sensor

table 4

The connector M1 is used to connect the power VCC and the ground VEE to the circuit the order of its pin shown in table 5:

Pin number	Connected to
1	VEE
2	VCC

table 5

The connector N1 is mounted to connect the current required for the Peltier from the circuit to the connector for the Peltier through wires.

All the amplifiers used in the circuit will be mounted through sockets. All the trimmers (ver1,ver2,ver3,and ver4) will be mounted on the edge of the board. all the trimmer will be side adjustment.

4.7 The display DPM160

The DP160 is a 4.5 digits display which act as a voltmeter shown in Fig 4.15. We will use this display to measure and monitor the the setting voltage proportional to the setting temperature, and reading voltage proportional to the reading temperature referred to the AGnd and also to display the reading of humidity sensor referred to the Ground VEE. the full scale range of this display is 200mv . we need a full scale range of 20V, thus we will scale the full scale range by two resistor (100K and 910K) as it shown in Fig 4.15. the input of this display comes from the selector MRX 204 .we will use a floating battery of 9v to power on the display and also switch to turn on and off the display. this display and its switch will be mounted on the wall of the box .

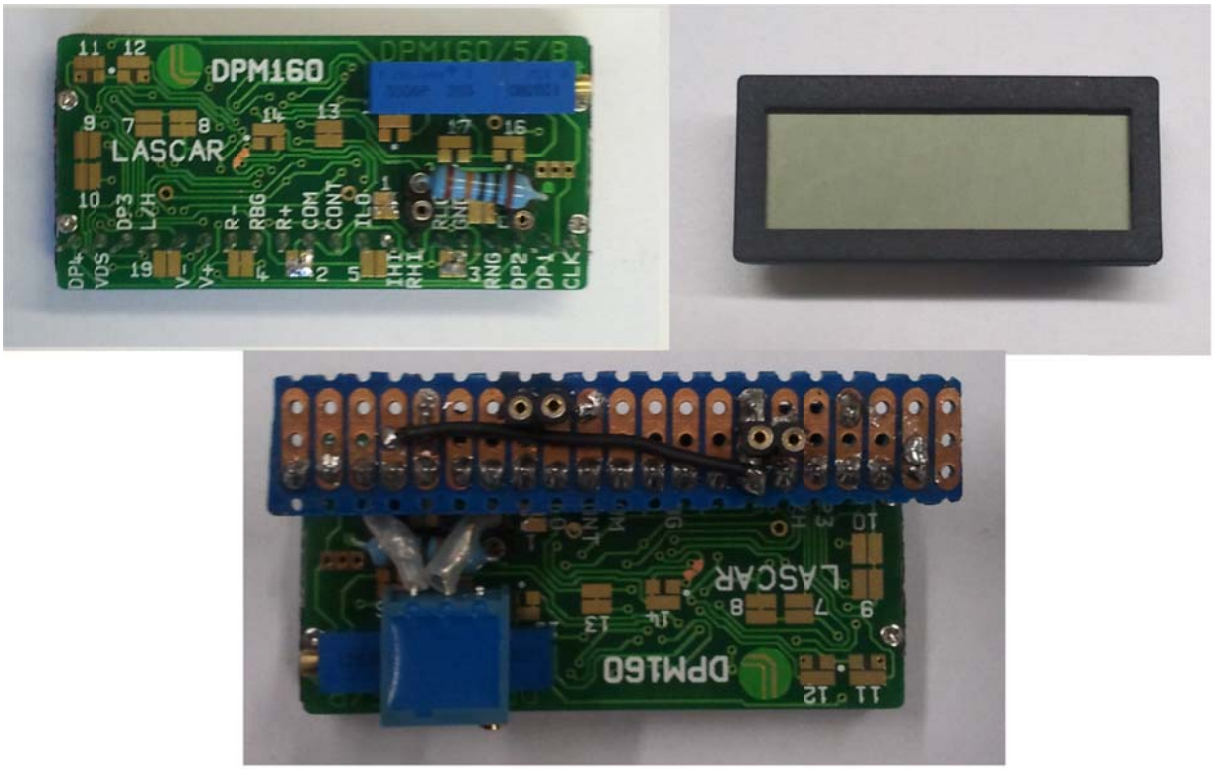

Fig 4.15 the front back view, and the small board which connected to the display

the small board connected to the display used to connect the inputs from the selector and also to connect the wires from the battery to power on and off the display.

5. Experimental results

Starting from the generation voltages which will be used as a reference' voltages in the circuit . the analog ground AGnd measured and it's equal to 4.291 v. the voltage REF1 is measured and its value is 1.787v. finally REF2 measured and its value is 0.67 V.

The current which will flow the PT100 is measured and its value is $94.5\mu A$. we used a trimmer instead of the PT100 to test the output of the stage of INA126 and this is the result we have got shown in table 6 :

Value of the PT100	Output of the INA126 referred to AGnd
89.26 Ω	0.874v
96.42 Ω	0.944 v
99.64 Ω	0.975v
100 Ω	0.979v
100.358 Ω	0.982v
103.58	1.014v
110.74	1.084v

table 6

from this results it appears that the gain of INA ≈ 103.59 .

the value trimmer ver4 is set in order to eliminate the offset voltage of the INA .Also the value of the trimmer is set in order to have at the output of the OP193 ,an output of -10mv/℃.and after the setting them we measured the output of the OP193 and here we have some results of the test shown in table 7:

PT100	Corresponding temp	OP193 output referred to AGnd
89.26 Ω	-30℃	300mv
96.42 Ω	-10℃	101mv
99.64 Ω	-1℃	9.89mv
100 Ω	0℃	0v
100.358 Ω	1℃	-10mv
103.58	10℃	-100.45mv
110.74	30℃	-299.8mv

table 7

from the result we see that we have got an output voltage of the OP193 =-10mv/℃. the first part of the second stage is the OPAMP LM358,the positive input of this amplifier is the setting voltage proportional to the setting temperature and the negative input is the output comes from OP193 .this amplifier works as a comparator . if the positive input is higher it will give an output of 13.636v otherwise it will give an output of 5.6mv .we test this stage with the feedback network of this amplifier ,and without .we can see the results from this two graphs first the test without the feedback network shown in Fig 5.1. in this case the transient happened so fast due to the open loop in the feedback . which will make the gain very high . we fixed the setting temperature at 0℃ means at 4.291 vand we change the value of the measured temperature between 4.261 v and 4.31v in the Fig 5.2 we test the output of the LM358 with feedback capacitor and resistor (C1 and R1) .now the transit happened in longer time because output stage will not saturate at the supply voltages and the duration of the output transient will be limited by the time constant of the feedback network.

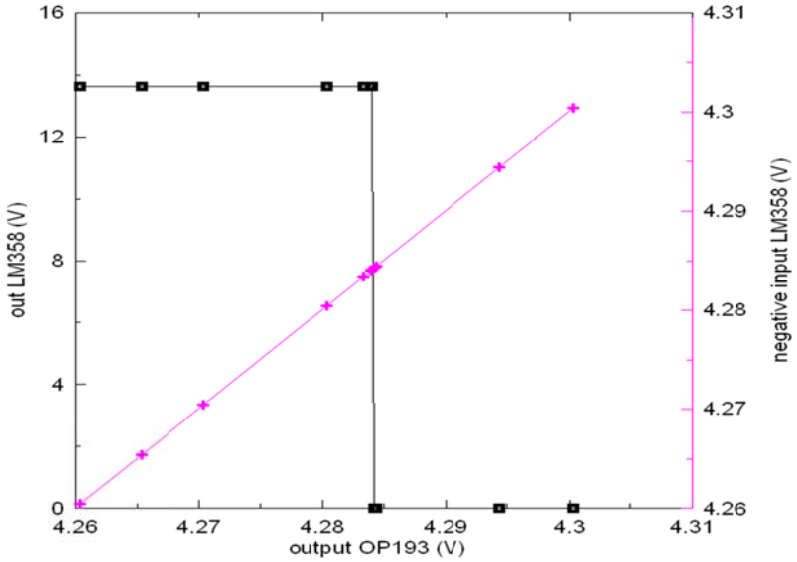

Fig 5.1 the output of LM358 with now feedback network .the curve in pink color Represents the change of the measured temperature ,and the black curve Represents the output of lm358

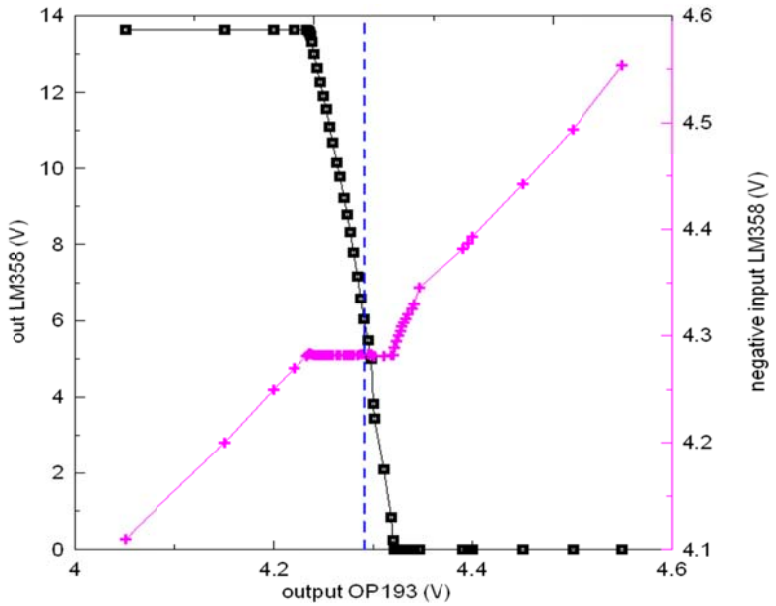

Fig 5.2 the output of LM358 with now feedback network .the curve in pink color Represents the change of the measured temperature ,and the black curve Represents the output of lm358