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DEVELOPMENT OF ULTRA FAST READ OUT ELECTRONICS FOR THE EUROPEAN X-RAY FREE ELECTRON LASER

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Abstract

The aim of this Doctoral activity has been the study, the realization and finally the integration of the analog front end for the DEPFET Sensor with Signal Compression (DSSC) project in the framework of the imagers development for the European X-ray Free Electron Laser (European XFEL). To cope with the challenging requirements of high frame rate, very low noise, power consumption and area occupancy a novel filtering architecture has been proposed. The circuit, called Flip Capacitor Filter (FCF), processes directly the current signal of the detector to achieve high frame rates still providing excellent noise performances. Two correlated measurements per read out cycle can be performed, one of the baseline current before signal arrival and one afterwards. The difference between the two values is obtained by flipping the feedback capacitor in the integrator stage, hence the name of the architecture. A single operational amplifier is used to save area and power consumption. A dedicated stage is introduced to cope with threshold shifts in the detector after irradiation and non-homogeneities in the imager.

In recent years, other circuits based on the current readout approach have been proposed. As an example, VELA (VLSI ELectronics for Astronomy) is a multi-channel ASIC developed at Politecnico di Milano that implements a trapezoidal weighting function by means of the Switched Current Technique (SCT). It has excellent noise performances

at processing times in the order of some μs, where the more common source follower approach starts to show its intrinsic limitations. The same filtering technique has also been used as a second stage in ASICs that try to exploit the advantages of both readout approaches, like VERITAS. In these chips the signal is initially read out in voltage mode and then converted to a current that can be processed with the SCT. In any case, none of the available solutions was able to fulfill the requirements of the European XFEL and thus a dedicated design was needed. In fact, the DSSC project specifications go beyond any existing instrumentation in terms of speed, noise, area and power consumption. The FCF represents therefore a state-of-the-art circuit in the field of current based filter architectures, and besides matching the specific project requirements it can be successfully employed as analog input stage in other spectroscopic experiments.

The recent development of Free Electron Lasers based on the Self-Amplified Spontaneous Emission technique has allowed a considerable reduction of the emitted wavelength. Nowadays it is possible to provide coherent light pulses in the X and γ-regime with unprecedented brilliance and short pulse duration. Having laser sources at these short wavelengths is beneficial for various applications ranging from medical diagnostic to biology and physical studies. A European X-ray Free Electron Laser is currently under construction in the Hamburg area, Germany. The first lasing operation is foreseen for the 2015. Thanks to the superconducting nature of its linear accelerator this facility will be able to provide the highest pulses rate ever achieved, with X-ray pulses only 220ns apart and grouped in bunches of 2700 flashes each. The energy range will be tunable between 206.6eV and 12.4keV, corresponding to a wavelength span from 0.1nm to 6nm. The Full Width at Half Maximum (FWHM) of the pulses will be less than 100fs, thus providing an extremely high peak brilliance.

To detect the X-ray photons several imagers are under development, including single-point, 1-D and 2-D detectors. Among others, the DSSC project aims to provide wide energy coverage with single photon detection capability thanks to its very low noise. To

achieve this result a novel detector structure with a compressive characteristic based on the DEPFET concept is under development at the Max-Planck-Institute Halbleiterlabor (MPI-HLL), Munich. The high gain for small collected charge and the compression for large signals will provide both desired features of single photon detection capability and wide dynamic range. The imager will be composed of 1024x1024 detectors, each one bump bonded to a dedicated read out channel. Full parallel read out is mandatory due to the high frame rate. Each channel will comprise a fast, low noise analog front end, an 8-bit analog-to-digital converter and a static RAM to store the information. Data will be sent out from the focal plane during the long gaps between subsequent macro bunches.

The first Chapter of this thesis describes the working principle of Free Electron Lasers, comparing them to standard light sources. The European XFEL project is also introduced in its main aspects and characteristics. The second Chapter introduces the imagers' development for the facility, and focuses on 2-D systems. Three different projects are under development for 2-D X-ray detection, one of them being the DSSC. The latter is analyzed in details in the third Chapter.

The fourth Chapter describes the FCF working principle and the design solutions adopted to implement the filter and cope with the DSSC guidelines. Measurements on a dedicated FCF ASIC are shown in the fifth and sixth Chapters, both for the FCF alone and coupled to a standard technology, linear DEPFET detector. Finally, Chapter seven shows the measurements obtained with small, 8x8 DSSC pixels matrix prototypes integrating all foreseen building blocks. In particular, the measurements that are relevant for the filter characterization are presented.

Italian abstract

Lo scopo della mia tesi di Dottorato è stato lo studio, la realizzazione ed infine l'integrazione dello stadio di *front end* analogico per il progetto DSSC nel contesto dello sviluppo di rivelatori per lo *European X-ray Free Electron Laser* (progetto Europeo XFEL). Per soddisfare i requisiti di elevato *frame rate*, basso rumore, consumo di potenza ed occupazione di area una nuova architettura di filtro è stata proposta. Il circuito, chiamato *Flip Capacitor Filter*, processa direttamente il segnale di corrente in arrivo dal rivelatore per ottenere un'elevata velocità mantenendo eccellenti prestazioni di rumore. Vengono effettuate due misure correlate, una della corrente di *baseline* prima dell'arrivo del segnale ed una subito dopo. La differenza tra le due misure è ottenuta girando la capacità in retroazione nello stadio di integrazione, operazione da cui deriva il nome dell'architettura. Un solo amplificatore operazionale è utilizzato così da risparmiare area e limitare il consumo di potenza. Inoltre, per far fronte alle variazioni della tensione di soglia del rivelatore in seguito ad irraggiamento ed alle disomogeneità della matrice uno stadio dedicato è introdotto nella struttura. Oltre a soddisfare le specifiche richieste del progetto in esame, la soluzione proposta può essere utilizzata in altri esperimenti di spettroscopia.

Negli ultimo anni sono stati proposti altri circuiti basati sulla lettura in corrente. Ad esempio, VELA (VLSI *ELectronics for Astronomy*) è un ASIC multi canale sviluppato al Politecnico di Milano

che implementa una funzione peso trapezoidale sfruttando la *Switched Current Technique* (SCT). Il circuito è in grado di fornire eccellenti prestazioni di rumore a tempi di processamento dell'ordine del μs, dove la più comune lettura a *source follower* comincia a mostrare i propri limiti intrinseci. La stessa architettura di filtraggio è anche stata usata come secondo stadio in ASIC che cercano di sfruttare i vantaggi di entrambe le tecniche di lettura, come VERITAS. In questi chip il segnale è inizialmente processato in tensione e poi convertito in una corrente che può essere elaborata tramite SCT. In ogni caso, nessuna delle soluzioni disponibili era in grado di soddisfare le richieste dell'XFEL Europeo, rendendo necessario uno sviluppo dedicato. Infatti, le specifiche del progetto DSSC vanno oltre le prestazioni di qualsiasi strumento esistente in termini di velocità, rumore, area e consumo di potenza. Il circuito FCF si pone quindi come stato dell'arte nel campo delle architetture di filtraggio basate sulla lettura in corrente, ed oltre a soddisfare le specifiche richieste del progetto DSSC può essere utilizzato con successo come stadio analogico di ingresso in altri esperimenti di spettroscopia.

Il recente sviluppo di *Free Electron Lasers* basati sulla tecnica di *Self-Amplified Spontaneous Emission* ha consentito una sensibile riduzione della lunghezza d'onda d'emissione. Al giorno d'oggi è possibile generare impulsi di luce coerente nel campo dei raggi X e γ con caratteristiche di brillanza e brevità senza precedenti. Varie applicazioni, dalla diagnostica medica alla biologia ed alla fisica traggono vantaggio dalla disponibilità di sorgenti laser in questo *range* di energie. Un *Free Electron Laser* Europeo operante nel campo dei raggi X (progetto Europeo XFEL) è attualmente in fase di realizzazione nell'area di Amburgo, Germania. L'attivazione del fascio laser è prevista per il 2015. Grazie alla natura superconduttiva del suo acceleratore lineare questa struttura sarà in grado di generare il più elevato tasso di impulsi mai raggiunto, con *flash* di raggi X separati di soli 220ns e raggruppati in treni da 2700 impulsi ognuno. L'energia sarà regolabile tra 206.6eV e 12.4keV, ossia tra 0.1nm e 6nm di lunghezza d'onda. La *Full Width at Half Maximum* (FWHM) degli impulsi sarà inferiore a 100fs, da cui deriva una brillanza di picco estremamente alta.

Vari sistemi di rivelazione sono in fase di sviluppo, tra cui sistemi *single-point*, mono-dimensionali e bi-dimensionali. Lo scopo del progetto DSSC (*DEPFET Sensor with Signal Compression*) è di fornire un sistema 2-D con vasta copertura energetica e basso rumore per consentire la rivelazione di singoli fotoni. Per ottenere questo risultato una nuova struttura di rivelatore, basata sul concetto del DEPFET e su di una caratteristica non-lineare di tipo compressivo, è stata proposta dal Max-Planck-Institute Halbleiterlabor (MPI-HLL) di Monaco. L'elevato guadagno per bassi fotoni e la compressione per grandi segnali forniranno allo stesso tempo la capacità di rivelare singoli fotoni e un vasto *range* dinamico. Il sistema completo sarà composto da 1024x1024 rivelatori, ognuno dei quali collegato a un canale di lettura dedicato. Questo tipo di lettura completamente parallela è dettata dall'elevato *frame rate*. Ogni canale sarà composto da un *front end* analogico veloce e a basso rumore, da un convertitore analogico-digitale a 8 bit e da una memoria RAM statica per immagazzinare l'informazione. I dati saranno inviati all'elettronica esterna durante gli intervalli tra due *macro bunch* successivi.

Il primo Capitolo di questa tesi descrive il principio di funzionamento dei *Free Electron Lasers*, offrendo un confronto con le sorgenti laser tradizionali. Il progetto Europeo di XFEL è introdotto nei suoi aspetti principali. Il secondo Capitolo introduce lo sviluppo e le richieste dei rivelatori d'immagine, concentrandosi in particolare sui sistemi 2-D. Tre diversi progetti sono allo studio per questo settore, uno dei quali è il progetto DSSC. Quest'ultimo è analizzato dettagliatamente nel terzo Capitolo.

Il quarto Capitolo introduce il *Flip Capacitor Filter* e descrive le soluzioni progettuali adottate per implementare il filtro e soddisfare le specifiche di progetto. Le misure sul filtro in un ASIC dedicato sono mostrate nel quinto e nel sesto Capitolo, sia per il circuito da solo che collegato a un rivelatore DEPFET lineare. Infine, il settimo Capitolo mostra le misure ottenute su matrici 8x8 di pixel in formato definitivo. In particolare, le misure che sono rilevanti per la caratterizzazione del filtro sono descritte in dettaglio.

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CHAPTER 1

The Free Electron Lasers

1.1 Historical background

The discovery of X-rays in 1985 by W. C. Röntgen played a fundamental role in basic science and medical diagnostics [1]-[2]. In fact, it was labeled a medical miracle and X-rays soon became an important diagnostic tool, allowing doctors to see inside the human body for the first time without surgery. The most important discoveries made using X-rays and awarded with the Nobel Prize are listed in Table 1.1. However, in spite of the considerable efforts made to build high-power Roentgen tubes, the obtained progress was only moderate for a long time, in particular if compared to the tremendous progress which was made with synchrotron radiation sources in terms of flux and brightness (Figure 1.1).

	Main discoveries made using X-rays awarded with the Nobel Prize
1915	W. H. Bragg and W. L. Bragg, in physics, for the determination of crystal structures using X-rays.
1936	P. Debye, in chemistry, for determining molecular structures by X-ray diffraction in gases.
1962	M. F. Perutz and J. C. Kendrew, in chemistry, for determining the structure of hemoglobin and myoglobin.
1962	F. Crick, J. Watson and M. Wilkins, in medicine, for their discoveries concerning the molecular structure of nucleic acids and its significance for information transfer in living material.
1964	D. Crowfoot Hodgkin, in chemistry, for the determination of the structure of penicillin and other important biochemical substances.
1979	A. M. Cormack and G. N. Hounsfield, in medicine, for the development of computerized tomography.
1985	H. A. Hauptman and J. Karle, in chemistry, for the development of direct methods for X-ray crystallographic structure determination.
1988	J. Deisenhofer, R. Huber and H. Michel, in chemistry, for the determination of protein structures crucial to photosynthesis.

Table 1.1 *List of the main discoveries made using X-rays and awarded with the Nobel Prize (source: www.nobelprize.org).*

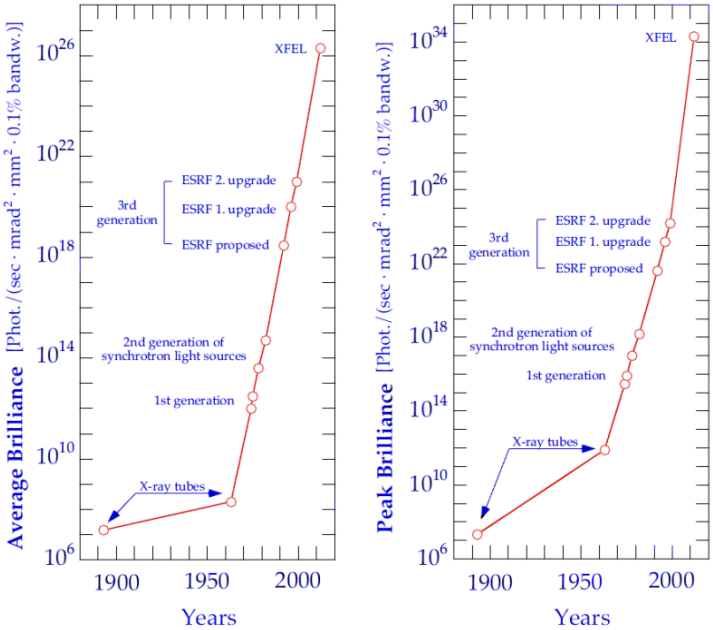

Figure 1.1 *Brilliance development of X-ray sources since the discovery of X-rays by W. C. Röntgen in Würzburg, in 1895.*

After the first observation of synchrotron radiation [3] and the evolution of cyclic electron synchrotrons and then storage rings for high energy physics applications, it was realized that these accelerators could also be exploited as much more intense X-ray sources. Many scientific disciplines ranging from physics, chemistry and biology to material sciences, geophysics and diagnostics would benefit from a powerful X-ray source with pulse lengths in the femtosecond range. The main reason for this is that the X-ray wavelength, that determines the smallest distance one can study with such a probe, is comparable to atomic dimension. The availability of such a radiation source would allow, for example, time-resolved observation of chemical reactions with atomic resolution.

The first-generation of synchrotron sources utilized radiation from storage rings built for high-energy physics purposes. Initially only bending magnet radiation was used and experiments were carried out parasitically during high-energy physics runs. The second-generation machines were built on purpose, but still initially used bending magnet radiation [4]. The design and construction of storage rings with special magnetic insertion devices, called wigglers and undulators, has led to third generation facilities specially designed for synchrotron radiation research [5]. However, in these machines all electrons emit their radiation field without a fixed phase relation leading to a nearly incoherent superposition.

A different concept was thus needed to realize a powerful radiation source with laser-like properties. Already in the 1951, Motz [6] showed that an electron bunch travelling through an undulator magnet array can coherently amplify radiation, and in 1960 Philips developed Ubitron [7], a microwave tube quite similar to what we now call a Free Electron Laser (FEL). Theoretical work on FELs was done in the 1960s and 1970s by Palmer [8], Robinson [9] and Csonka [10], and the first FEL was operated in 1971 by Madey [11] at 10μm radiation wavelength.

While the existence of an exponentially growing solution for the FEL equations has been studied by many authors [12], the first theory of a Self-Amplified Spontaneous Emission (SASE) FEL in the 1-D case, including the start from spontaneous radiation and saturation, was given

in [13]. The theory was then extended to three dimensions [14]. The first proposal for a single pass soft X-ray FEL starting from noise was published by Murphy and Pellegrini in 1985 [15], but the project was still based on a storage ring structure. This limited the performances due to storage ring collective effects.

The development of radio frequency photocathode electron guns [16] and the work on linear colliders have allowed overcoming these limitations. In particular, the continuous improvements in linear accelerators have demonstrated that it is possible to accelerate and time compress electron beams without spoiling their brightness [17]. In fact, while the theory of the SASE FEL has been developed starting in the 1980s, experimental results have been obtained only during the last few years. The first demonstration of the SASE mechanism was carried out in 1997 and concerned lasing in the infrared wavelength [18]. In September 2000, a group at Argonne National Laboratory (ANL) became the first to demonstrate saturation in a visible (390 nm) SASE FEL [19]. Soon after, in September 2001 a group at DESY (Hamburg, Germany) demonstrated lasing to saturation deep into the vacuum-UV at 98nm [20].

Through several workshops [21-23] it became clear that these new sources are so fundamentally different from previous lasers that they will become for many fields a complementary tool and will open up completely new areas of X-ray science and applications. The discussions convinced nearly all participants that linear accelerator based FELs would be the most effective machines for continuing to improve the performance of X-ray sources, and in particular, would provide the only viable route to a diffraction-limited hard X-ray source.

1.2 FELs working principle

The emitted radiation from a FEL has much in common with radiation from a conventional optical laser, such as high power, narrow bandwidth and diffraction limited beam propagation. On the other hand, the working principle is completely different. One of the main differences

between the two lasers is the gain medium. In a conventional laser, the amplification comes from the stimulated emission of electrons bound to atoms, either in a crystal, liquid dye or a gas. Therefore, the set of possible energy states an electron can occupy is finite, which directly translates to a limited output spectrum. Conversely, the amplification medium of the FEL is represented by free (unbounded) electrons stripped from atoms in an electron gun and then accelerated to relativistic velocities. Since the electrons in the FEL are not limited to specific transitions, the output wavelength of the laser is tunable over a wide range. Moreover, the lack of a lasing medium in the cavity allows the laser to operate at very high power levels without heating problems.

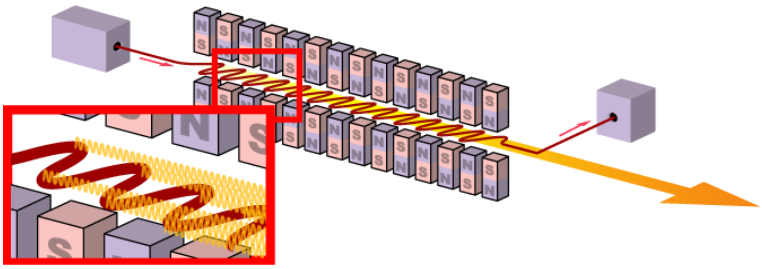

Figure 1.2 *Working principle of a single-pass FEL. By travelling through a magnetic undulator electrons emit photons that are in phase with each other, thus generating a coherent output pulse.*

The basic principle makes use of the fact that an electron beam of sufficient quality, propagating through a long, periodic magnetic dipole array – a so called undulator – exponentially amplifies an initially existing radiation field. This amplification is initiated by an increasingly pronounced longitudinal density modulation of the electron bunch. In the magnetic structure, the electrons travel on an oscillatory path imposed by the periodic sequence of transverse magnetic fields through the Lorentz force (Figure 1.2). The initial radiation field can be an external source that co-propagates with the electron bunch, for example provided by an external seed laser, or an internal field generated by the spontaneous emission in the undulator. In the latter case it is called a SASE FEL [24]-[25]. The two different activation techniques will be described in the next section.

In the undulator, the deflection of charge from the forward direction is comparable to the opening angle of the synchrotron radiation cone. Thus, the electrons emit synchrotron radiation in a narrow cone and the radiation generated while travelling along the individual magnetic periods overlaps. This interference leads to a spontaneous, on-axis undulator emission into a narrow bandwidth around a resonance wavelength λ_{ph} determined by the undulator parameters and the beam energy:

$$\lambda_{ph} = \frac{\lambda_u}{2\gamma^2}(1 + K^2), \text{ with } \gamma = \frac{E}{m_e c^2} \text{ and } K = \frac{ecB_u\lambda_u}{2\pi m_e c^2} = 0.934 B_u \lambda_u$$

Here, E is the electron energy, m_e the electron rest mass, e the elementary charge, c the speed of light in vacuum, λ_u the undulator period in cm, and B_u the peak magnetic field in the undulator measured in Tesla. K is called the averaged undulator parameter, and varies between 1 and 10 for a permanent magnet undulator that has a few centimeters long period [26]. Two main advantages of the FELs are evident from the last equation: the tunability of the wavelength by varying the electron energy or the magnetic field, and the possibility to achieve very short photon wavelengths at high electron energies.

The interference condition basically means that, while travelling along one period of the undulator, the electrons slip by one radiation wavelength with respect to the electromagnetic field. In fact, since the radiation is faster than the electrons it overtakes the charges travelling ahead and interacts with them along the way. Depending on the relative phase between radiation and electron oscillation, electrons experience either a deceleration or acceleration: electrons that are in phase with the electromagnetic wave are retarded while the ones with opposite phase gain energy. As a result, a longitudinal periodic charge density modulation of the electrons at the electromagnetic wavelength is established (Figure 1.3). This process of micro-bunching amplifies the electromagnetic field. More and more electrons begin to radiate in phase, which results in an increasingly coherent superposition and enhanced power of the radiation emitted from the micro-bunched electrons. The more intense the electromagnetic field gets, the more pronounced the

longitudinal density modulation of the electron bunch, and vice versa. This is what leads to the high intensities and laser-like properties of FELs.

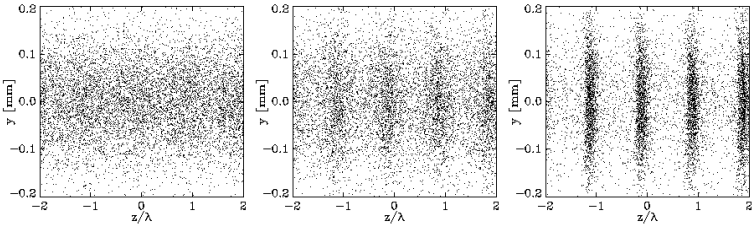

Figure 1.3 *Example of the development of micro-bunching of the electron beam along the undulator. The electron density is represented by the density of dots. Left, at the undulator entrance. Middle, along the exponential growth regime. Right, saturation at the undulator exit.*

The lack of suitable mirrors in the extreme ultraviolet and X-ray regimes prevents the operation of an XFEL oscillator. This is due to the low reflectivity in normal incident geometry at these wavelengths and potential mirror deformation, or even damage, due to the high absorbed power. Consequently, there must be suitable amplification over a single pass of the electron beam through the undulator and this leads to very long structures.

1.3 Activation techniques

In the previous section it is stated that to start the FEL micro-bunching process an initial electromagnetic field is necessary inside the magnetic undulators. This starting condition can be obtained in two different ways:

i. by using an external, conventional laser at the desired λ_{ph} wavelength, realizing a so-called seeded FEL. Power increase in a high gain mode, seeded FEL is directly related to the energy modulating process of the electrons. High quality radiation can

be generated since it is directly derived from the seed. On the other hand, by using conventional lasers this technique poses limitations to the obtainable output wavelengths;

ii. by amplifying the spontaneously emitted radiation in the initial part of the magnetic undulator by the electrons, in which case the system is called a SASE FEL, as already described in section 1.2. In SASE mode no external laser sources are needed, thus it is possible to fully exploit the FEL properties and generate very short wavelength photons. Moreover, since it is completely independent of atomic excitation levels it can be tuned over a wide range by acting on the undulators parameters.

The second technique is here discussed in more details, since it is the one that will be used at the European X-ray FEL. The SASE process implies a very short, high energy electron pulse producing a similarly short and very intense FEL radiation pulse. Therefore, to obtain the desired behavior different criteria have to be met. First of all, it is necessary to have a good electron beam quality, specifically high peak current, small emittance, small energy spread and short bunch length. These properties can be produced by linear but not circular accelerators. Moreover, a sufficient overlap between radiation pulse and electron bunch along the undulator has to be guaranteed. Finally, an intensity gain in excess of 10^7-10^8 has to be provided in the short wavelength regime. At this level of gain, the shot noise of the electron beam can be amplified up to complete micro-bunching.

Before micro-bunching takes place, all the N_e electrons (with usually $N_e > 10^9$) can be treated as individually radiating charges with a power due to spontaneous emission that is proportional to N_e. The interaction of the electrons with this initial radiation starts the lasing action, and if the charge density and undulator length are sufficient the micro-bunching process takes place. With complete micro-bunching, all electrons radiate almost in phase leading to a radiation power that is proportional to N_e^2. Therefore, an amplification of many orders of magnitude with respect to the initial condition is obtained and the

radiation power along the longitudinal z-axis can be written as follows [27-29]:

$$P(z) = AP_{in}e^{\frac{2z}{L_g}}$$

where L_g is the field gain length for the electromagnetic field, P_{in} is the effective input power, and A is the input coupling factor. For a one-dimensional FEL with an ideal electron beam this constant is equal to 1/9. Concerning the initial input power, for a SASE FEL it is possible to estimate this parameter by the spontaneous radiation power on the initial part of the undulator and within the laser bandwidth. The exponential amplification continues until the electrons are completely grouped in micro-bunches, after which the bunch is over modulated resulting in saturation of the obtainable power (Figure 1.4). If the undulator length is sufficient, the system does not require a multi-pass cavity to reach saturation and can hence deliver light with wavelengths where optical mirrors are ineffective. In this way it is possible to reach the ultraviolet and X-ray regime, with photons having a wavelength down to less than an Angstrom. Beginning from shot noise, it typically takes a SASE FEL about 18 to 20 L_g to reach saturation.

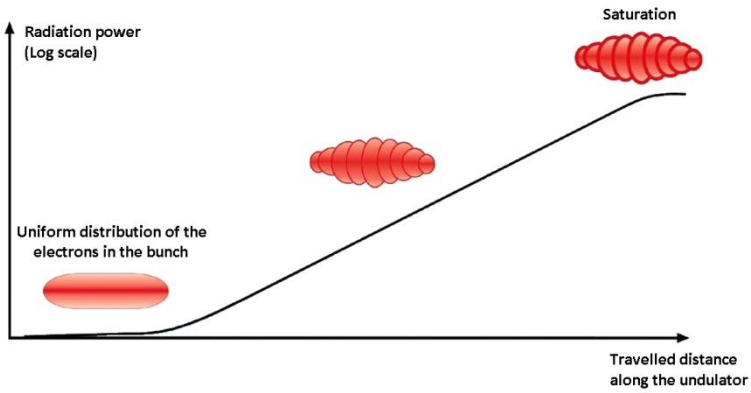

Figure 1.4 *The longitudinal density modulation of the electrons bunch is shown together with the resulting exponential growth of the radiation power along the undulator. In reality the number of micro-bunches is much larger.*

In the 90's two long wavelengths projects were started to prove that the SASE process works as theoretically predicted, the TESLA Test Facility (TTF) FEL at DESY in 1995 (with wavelengths between 1000Å and 60Å) [30] and the Low Energy Undulator Test Line (LEUTL) at Argonne National Laboratory (Illinois, United States) in 1996 in the short wavelength part of the visible spectrum. Both experiments were successful in 2000, and opened the way towards the construction of new SASE-based X-ray FELs.

The first lasing and operation of LCLS in 2010 [31] has produced results in very good agreement with standard FEL theory and numerical simulations, indicating that FEL physics in the X-ray wavelength range is well understood.

1.4 FEL properties

The output radiation of a SASE XFEL has most of the properties that characterize conventional lasers. Although many transverse modes can be excited at the beginning of the undulator, by the end of the exponential growth regime a fundamental mode with the highest growth rate will dominate. As a result, a SASE FEL has excellent transverse coherence at saturation and can be usually approximated by a fundamental Gaussian mode.

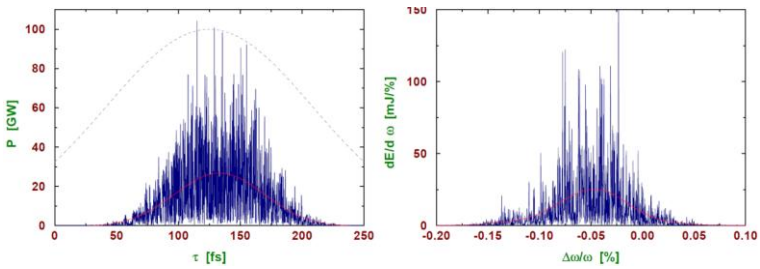

Figure 1.5 *Typical temporal (left) and spectral (right) structure of the radiation pulse from a SASE XFEL at a wavelength of 1Å. The red lines correspond to averaged values. The dashed line represents the axial density profile of the electron bunch.*

On the other hand, compared to conventional optical lasers and to seeded FELs the longitudinal coherence of an X-ray SASE FEL is rather poor due to the initial radiation from shot noise. Examples of temporal and spectral structures of the radiation pulse from an X-ray FEL are shown in Figure 1.5. The output radiation consists of a large number of independent wave packets that give rise to spikes whose characteristic duration is the coherence time [32]. Within one wave packet, transverse and longitudinal coherence characterizes the radiation. Anyway, the consequence of the shot noise based startup is recognizable in the chaotic nature of the output radiation.

In addition to laser-like properties, a FEL has the following peculiarities:

i. tunability: as described in section 1.2 the electron beam represents the gain medium of a FEL and the resonant condition can be easily modified by changing either its energy or the magnetic field strength. For these reasons, FELs are tunable over a wide spectral range. A factor of 10 in the obtainable frequency has already been achieved using the same accelerator and undulator;
ii. high peak power: the lack of a physical lasing medium allows FELs to produce very high peak powers. Giga-watt peak powers have already been demonstrated [20]-[33]-[34];
iii. flexible pulse structure: this property descends from the fact that the pulse structure of the radiation follows the initial pulse structure of the electron beam. Therefore, linear accelerators can be used to manipulate and control the FEL output structure. Picoseconds pulses with very low jitter can be produced, and their interval can be varied with the possibility of realizing complex pulse structures;
iv. broad spectrum coverage: since the gain medium is transparent at all wavelengths, in principle FELs are capable of generating radiation at any desired wavelength. In practice, electron beam energy, required current, emittance, and energy spread requirements become prohibitive at very short wavelengths.

1.5 The European XFEL project

FELs have been developed since the 1960's but short wavelengths, down to the X-ray regime, have been obtained only after the realization of SASE FELs in the late 1990's. As already mentioned, systems working in this spectral range are called X-ray FELs, or simply XFELs. After the first successful development of a FEL in the soft X-ray region at the Free Electron LASer (FLASH) in Hamburg, several other facilities have recently started, like the Linac Coherent Light Source (LCLS) at the Stanford Accelerator Center (SLAC) National Laboratory, or have been proposed. In particular, a European XFEL laboratory for the Å wavelength range is under construction since 2009 [35]. Starting from 2015, this facility will deliver ultra-short pulses of soft to hard X-rays. It will then be open for experiments starting from the following year. To realize and operate the European XFEL, international partners agreed on the foundation of an independent research organization named the European XFEL GmbH. At present, a total of 12 countries are participating in the project: Denmark, France, Germany, Greece, Hungary, Italy, Poland, Russia, Slovakia, Spain, Sweden and Switzerland.

The laboratory will be located in the federal states of Hamburg and Schleswig-Holstein, Germany. Although it will comprise three large sites above ground, the European XFEL will be mainly located underground, along tunnels with a depth between 6 to 38 meters. The network of tunnels will have a total length of about 5.77km. The 3.4km long facility will run from DESY in Hamburg-Bahrenfeld to the town of Schenefeld (Figure 1.6) that will host the research campus where international scientists will carry out the experiments. Electrons generated from a solid cathode by an optical laser beam will be accelerated by a radio frequency gun up to 120MeV. The electron bunches will then be steered to the superconducting, low frequency linear accelerator that will occupy the first 2.1km of the facility, with an effective acceleration length of 1.7km. The electrons will be brought to relativistic velocities by means of micro waves inside niobium resonators, which will be

maintained at a temperature of 2.15K to exploit the superconductivity advantages. In particular, due to the low losses in these cavities large beam currents can be accelerated at high power efficiencies. According to the present concept, it is planned to vary the bunch charge from 20pC to 1nC with a maximum peak current close to 5kA [36]. Along the accelerator, two stages of bunch compression will be located to produce the short and very dense electron bunches required to trigger the SASE process.

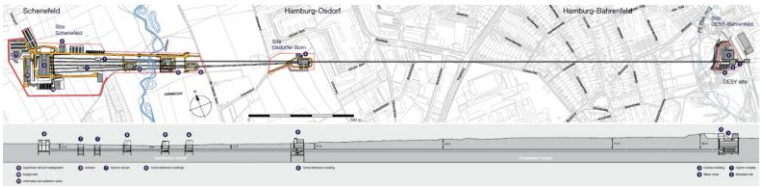

Figure 1.6 *The top view indicates the dimensions and the placement in the surrounding area. The side cross-sectional view shows the ground profile and the various shaft buildings.*

The multi bunch property and the flexible pulse structure will provide an efficient way to have a multi-user facility. In fact, each electron bunch will pass through the system only once, giving the possibility to extract individual bunches and guide them to various undulators. Multiple extraction lines will be built in parallel to have different beam energies in a quasi-simultaneous manner. To fulfill experimental requirements, operation at different electron energies of 17.5GeV, 14GeV and 10.5GeV is foreseen. The system will also be able to provide a maximum energy of 50GeV on one line in case new scientific applications will require a higher energy. At the end of the extraction tunnel, a beam switchyard is foreseen to distribute the beam to different undulators. Three undulator systems, named SASE-1, SASE-2, and SASE-3 will deliver photons to six experimental stations dedicated to a specific field of research (Figure 1.7) [37]. Each of these undulators section produces X-ray radiation by the SASE process. The SASE-1 and SASE-2 beam lines will deliver photons in the range of 0.1nm to 0.4nm but extension to shorter wavelength seems possible. The SASE-3 beam line will be dedicated to soft X-ray range between 0.4nm and 3nm. The

undulators will be of different types to change polarization and photon energy range.

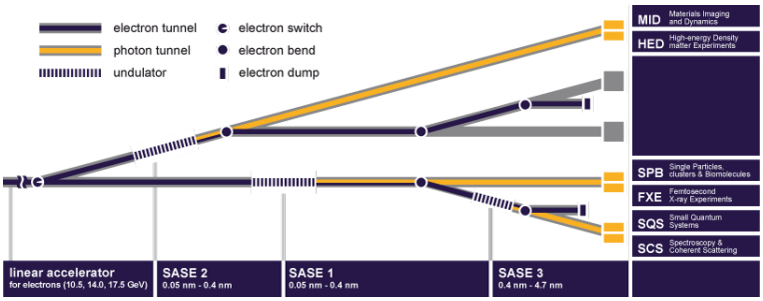

Figure 1.7 *Layout of the three undulators foreseen for the startup phase of the European XFEL.*

Properties of the radiators as foreseen in the baseline design for the European XFEL			
	SASE-1	SASE-2	SASE-3
Length [m]	201.3	256.2	128.1
Energy [keV]	12.4	3.1–12.4	0.25–3.1
Photons/pulse	10^{12}	$1.6x10^{13}$–10^{12}	$3.7x10^{14}$–$1.6x10^{13}$
Beam size [μm]	70	55–85	60–90
Beam div. [μrad]	1	3.4–0.84	18–3.4
Spectral BW [%]	0.08	018–0.08	0.65–0.2

Table 1.2 *Main properties of the five radiators of the European XFEL, as foreseen in the initial design [35].*

The photons generated by the undulators are transported through the respective photon beam lines. A higher magnetic field results in a wider travelling path for the electrons and thus in X-ray radiation with a longer wavelength, and vice versa. Therefore, reducing the electron energy at the end of the accelerator would generate longer wavelengths, in case they are required by some experiments. The photon pulse length will be approximately 1000 times shorter than at classical third generation synchrotron storage rings, with an expected FWHM of about 100fs to be compared to the 30ps of available synchrotron sources. Moreover, the horizontal and vertical emittance will be smaller by a factor of 100 and 3, respectively, with the number of photons per pulse a

factor of 300 higher and the natural mono chromaticity a factor of 10 better. All of these give an increase in peak brilliance of nine orders of magnitude (Figure 1.8).

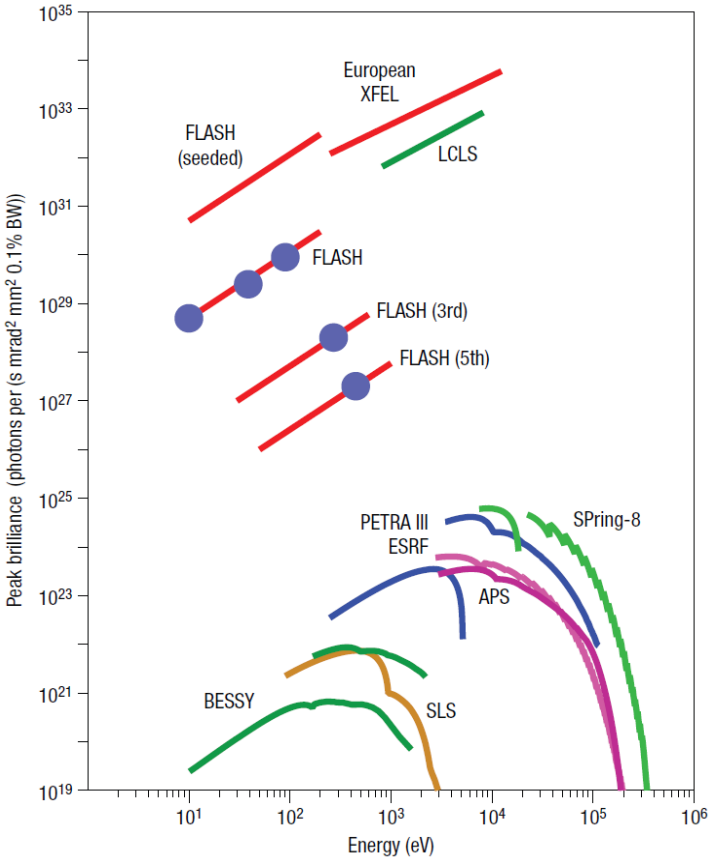

Figure 1.8 *Peak brilliance of XFELs and undulators for spontaneous radiation at TESLA and at the LCLS, Stanford, in comparison to the undulators at present third generation synchrotron radiation sources. In addition, also the spontaneous spectrum of an XFEL undulator is shown.*

Thanks to the superconducting accelerator technology, the system will be able to deliver X-ray flashes per second. This high repetition rate is what makes the European XFEL unique among the X-ray lasers in the world. As a comparison, the average rate of X-ray pulses for the Linear Coherent Light Source (LCLS) in the USA is 120Hz, while for the

Spring-8 Compact SASE Source (SCSS) in Japan is 60Hz. In fact, both facilities use normal-conducting, room temperature linear accelerators. Pulses in the European XFEL will be only 220ns apart one from the other and grouped in bunches with a frequency of 10Hz. Every train of pulses will thus be composed by approximately 2700 X-ray flashes, for a total duration of about 600μs after which a long period of 99.4ms will be dedicated to the cooling of the linear accelerator (Figure 1.9).

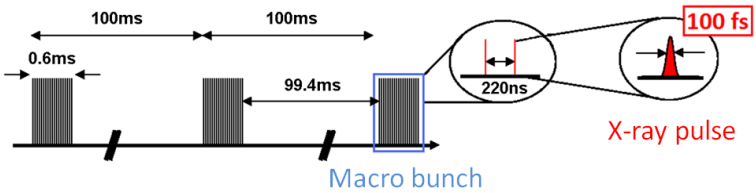

Figure 1.9 *Temporal structure of the European XFEL pulses.*

At the end of each undulator it will be possible to selectively guide the pulses to lower the repetition rate if the experiments require so. This is another peculiarity of the facility, as the electron bunches can be prepared and distributed according to the needs of the experiments. In Table 1.3 the main properties of various XFEL facilities are listed.

Comparison between different XFEL facilities					
		LCLS	SCSS	PSI XFEL	EU XFEL
Wavelength	(nm)	0.15	0.1	0.1	0.1
Design peak brilliance	(*)	$8x10^{32}$	$5x10^{33}$	$1x10^{33}$	$5x10^{33}$
Electron energy	(GeV)	14.35	8	5.8	17.5
Normalized slice design emittance	(μm)	1.2	1	0.43	1.4
Undulator period	(mm)	30	18	15	35.6
Saturation length	(m)	92	80	39	140
Facility length	(m)	3000	750	910	3400
Start of operation		2009	2010	2016	2015

Table 1.3 *Comparison between different XFEL facilities. (*) The peak brilliance is measured in ph/(s mm^2 mrad^2 0.1%bw).*

1.6 Scientific possibilities

Given the revolutionary properties of the European XFEL, accurate projection of its scientific applications is difficult. Nevertheless, major advances can be anticipated in many fields of research, exploiting the high photon number per pulse, ultra-short pulse duration and high coherence of FEL radiation. For instance, scientists will be able to map atomic details thanks to the short wavelengths and benefit from the very high repetition frame rate to study processes as they evolve in time.

Possible areas that would benefit from this facility are listed in the following part of the section [35]:

i. analysis of microscopic structures: thanks to the very short wavelengths of the order of atoms dimensions and to the laser-like properties of the pulses scientists will be able to study the structure of bio-molecules and materials at the atomic scale. X-ray radiation sources now available do not generate enough power to study single molecules. These researches will allow better understanding of biological cells and creating new materials with improved properties. Moreover, the duration of the flashes is so short that the molecule hardly changes during the exposure. The molecule starts to decay – due to the enormous forces generated by the strong incident light – only after the X-ray flash has passed the sample and the picture of the atomic structure has been taken. Special emphasis will be put on viruses that cannot be crystallized, for instance the viruses responsible for AIDS and herpes;

ii. study of very fast processes: the small FWHM of the pulses makes it feasible to follow molecules behavior in time with an unprecedented precision, enabling scientists to study for example the formation of molecules and functional processes at cell membranes. Snapshots can be taken without moving details becoming blurred, and with short wavelengths even atomic details become visible. This property can be important to

investigate infection processes and thus pave the way to the development of new therapies. Another field of research that would benefit from the short pulses concerns catalytic processes and the reactions that are involved in the energy generation. A deeper understanding of these processes can lead to significant improvements in energy production;

iii. generation and study of extreme states of the matter: using XFEL pulses scientists will be able to investigate the behavior of matter under extreme conditions. In fact, the European XFEL pulses will be so powerful that they will allow reaching pressure and temperature conditions similar to those present inside planets. With a secondary laser beam, it will be possible to study the plasma state and develop new models for astrophysics. The theoretical description of these conditions is extremely difficult, especially since there are only very little experimental data. The European XFEL offers unique opportunities to both create and study matter in extreme states;

iv. observing small objects in strong fields: the X-ray flashes will enable novel experiments with atoms, molecules, ions and clusters. Thanks to the high intensity of the flashes, the particles are excited into new, previously unknown states. One example is highly ionized states in which they lose several electrons at once. In these conditions particles exhibit new properties. Investigating these states – which scientists were unable to observe so far – is very important for the understanding of atomic physics phenomena. Such insights could also benefit research into energy generation.

In particular, in the TDR eight main scientific fields are identified: Small Quantum Systems (SQS), High Energy Density Matter (HED), Coherent X-ray Scattering and Lensless Imaging in Materials Science (CXI), X-ray Photon Correlation Spectroscopy (XPCS), X-ray Absorption Spectroscopy (XAS), Femtosecond Diffraction Experiments (FDE), Single Particles and Biomolecules (SPB) and Research And Development (RAD). Table 1.4 shows a possible distribution of scientific instruments on the photon beam lines as initially foreseen. Since XFEL

features a relatively small number of photon beam lines, each of them needs to serve more than one application or X-ray technique. The electron bunches can be prepared and distributed according to the needs of the experiment. The specific electron beam parameters could be the time pattern, the electron energy (and, therefore, the photon energy) or even more sophisticated parameters of the X-ray pulse.

Experimental stations and assigned scientific applications for the startup phase		
Beam line	X-ray features	Proposed instruments
SASE-1	About 12keV High coherence High flux	PCS 1–X-ray Photon Correlation Spectroscopy FDE 1–Femtosecond Diffraction Experiments SPB 1–Single Particles and Biomolecules
SASE-2	3.1keV–12.4keV High coherence High flux	CXI 1–Coherent X-ray Imaging HED 2–High Energy Density XAS 2–X-ray Absorption Spectroscopy
SASE-3	0.25keV–3.1keV High coherence High flux	HED 1–High Energy Density SQS 1–Small Quantum systems XAS 1–X-ray Absorption Spectroscopy SQS 2–Small Quantum systems PCS 2–X-ray Photon Correlation Spectroscopy CXI 2–Coherent X-ray Imaging

Table 1.4 *Possible assignment of the scientific applications for the various experimental stations of the European XFEL [35]. Main X-ray features of the beam lines are indicated (see also Table 1.2).*

1.7 Bibliography

[1] A. Asmuss, “Early histoty of X-rays”, available on-line.

[2] O. W. Linton, “Medical applications of X-rays”, available on-line.

[3] J. P. Brewett, Phys. Rev. 69 (1946) 87.

[4] J. Arthur, et al., “Linac Coherent Light Source (LCLS) Design Study Report”, SLAC-R-521, December 1998.

[5] B. Buras and G. Materlik, Nucl. Instrum. Meth. A246, 21(1986).

[6] H. Motz, J. Appl. Phys. 22, 527 (1951); H. Motz, W. Thon, R.N. Whitehurst, J. Appl. Phys. 24, 826 (1953); H. Motz, M. Nakamura, Ann. Phys. 7, 84 (1959).

[7] R. M. Philips, IRE Trans. Electron Devices 7, 231 (1960).

[8] R.V. Palmer, J. Appl. Phys., 43, 3014 (1972).

[9] K.W. Robinson, Nucl. Instr. and Meth, A239, 111 (1985).

[10] P. Csonka, Part. Acc. 8, 225 (1978).

[11] J. M. J. Madey, J. Appl. Phys. 42, 1906 (1971); L. R. Elias, W.M. Fairbank, J. M. J. Madey, H. A. Schwettman, T. I. Smith, Phys. Rev. Lett. 36, 717 (1976); D.A.G. Deacon et al., Phys. Rev. Lett. 38, 892 (1977).

[12] N. M. Kroll, Phys. Quantum Electron. 5, 115(1978); P. Sprangle, R. A. Smith, NRL Memo-Report 4033 (1979); A. M. Kondratenko, E. L. Saldin, Dokl. Aka. NAUK SSSR, 249, 843 (1979); D. B. McDermott, T. C. Marshall, Phys. Quantum Electron. 7, 509 (1980); A. Gover, P. Sprangle, IEEE J. Quantum Electron. QE-17, 1196 (1981); G. Dattoli et al., IEEE J. Quantum Electron. QE-17, 1371 (1981); R. Bonifacio, C. Pellegrini, L. Narducci, Opt. Commun., 50, 373 (1984); J. B. Murphy, C. Pellegrini, R. Bonifacio, Opt. Comm. 53, 197 (1985); J. Gea-Banacloche, G. T. Moore, M. Scully, SPIE 453, 393 (1984); P. Sprangle, C. M. Tang, C. W. Roberson, Nucl. Instr. and Meth, A239, 1 (1985); E. Jerby, A. Gover, IEEE J. Quantum Electron QE-21, 1041 (1985); R. Bonifacio, F Casagrande, C. Pellegrini, Opt. Comm. 61, 55 (1987).

[13] R. Bonifacio, C. Pellegrini, L. Narducci, Opt. Commun., 50, 373 (1984).

[14] G. T. Moore, Nucl. Instr. and Meth, A239, 19 (1985); E. T. Scharlemann, A. M. Sessler, J. S. Wurtele, Phys. Rev. Lett. 54, 1925 (1985); M. Xie, D.A.G. Deacon, Nucl. Instr. and Meth,

A250, 426 (1986); K.-J. Kim, Phys. Rev. Lett. 57, 1871 (1986); L.-H. Yu, S. Krinsky, R. Gluckstern, Phys. Rev. Lett. 64, 3011 (1990); Z. Huang, K.-J. Kim, Nucl. Instr. and Meth, A475, 59 (2001).

[15] J. B. Murphy, C. Pellegrini, Nucl. Instr. and Meth, A237, 159 (1985); J. B. Murphy, C. Pellegrini, J. Opt. Soc. Am. B2, 259 (1985); K.-J. Kim et al., Nucl. Instr. and Meth, A239, 54 (1985).

[16] J. S. Fraser, R. L. Sheffield, E. R. Gray, "A new high brightness electron injector for free-electron lasers driven by RF linacs", Nucl. Instr and Meth, A250, pp. 71-76, 1986.

[17] K. Bane, "Wakefield Effects in a Linear Collider", AIP Conf. Proc., vol. 153, p. 971 (1987); J. Seeman et al, "Summary of Emittance Control in the SLC Linac", US Particle Accelerator Conference, IEEE Conf. Proc. 91CH3038-7, p. 2064 (1991); J. Seeman et al, "Multibunch Energy and Spectrum Control in the SLC High Energy Linac", US Particle Accelerator Conference, IEEE Conf. Proc. 91CH3038-7, p. 3210 (1991); T. Raubenheimer, "The Generation and Acceleration of Low Emittance Flat Beams for Future Linear Colliders", SLAC-Report 387 (1991).

[18] M. Hogan, et al., "Measurements of Gain Larger than 10^5 at 12 μm in a Self-Amplified Spontaneous-Emission Free-Elektron Laser", Phys. Rev. Lett. 81, 4867, 1998.

[19] S. V. Milton, et al., "Exponential gain and saturation of a self-amplified spontaneous emission free electron laser", Science 292, 2037–2041 (2001).

[20] V. Ayvazyan, et al., "Generation of GW radiation pulses from a VUV free-electron laser operating in the femtosecond regime", Phys. Rev. Lett. 88, 104802 (2002).

[21] International Workshop on X-Ray Free Electron Laser Application, DESY, Hamburg, September (1996).

[22] Potential Future Applications in Structural Biology of an X-ray Free Electron Laser at DESY, EMBO Workshop, DESY, Hamburg, July (1999).

[23] SLAC/DESY International Workshop on Interactions of Intense Sub-picosecond X-Rays with Matter, SLAC, Stanford, January (1997).

[24] A. M. Kondratenko and E. L. Saldin, "Generation of coherent radiation by a relativistic electron beam in an ondulator", Part. Accelerators 10, 207 (1980).

[25] R. Bonifacio, C. Pellegrini and L.M. Narducci, "Collective

instabilities and high-gain regime in a free electron laser", Opt. Commun. 50, 373 (1984).

[26] LCLS-II Conceptual Design Review, Chapter 4, "FEL physics".

[27] E. L. Saldin, E. A. Schneidmiller, M. V. Yurkov, "The Physics of Free Electron Lasers", Springer, Berlin-Heidelberg (2000).

[28] K. J. Kim, Phys. Rev. Lett. 57, 1871 (1986).

[29] S. Krinsky and L.H. Yu, Phys. Rev. A35, 3406 (1987).

[30] T. Åberg et al., "Conceptual Design Report of a VUV FEL at the TESLA Test Facility at DESY", DESY Report TESLA-FEL 95-03, Hamburg (1995).

[31] P. Emma et al., "First lasing and operation of an Ångstrøm-wavelength free-electron laser", Nature Photonics 4, 641 (2010).

[32] E. L. Saladin, E. A. Schneidmiller, and M. V. Yurkov, "Statistical properties of radiation from VUV and X-ray free electron laser", Opt. Commun. 148, 383 (1998).

[33] E. L. Saldin, E. A. Schneidmiller, M. V. Yurkov, "Gigawatt-class vacuum ultraviolet Free Electron Laser at DESY Paves the way for the fourth-generation X-ray source", EUROCON 2007, Warsaw.

[34] V. Ayvazyan, et al., "First operation of a free-electron laser generating GW power radiation at 32nm wavelength", Eur. Phys. J. D 37, 297-303 (2006).

[35] M. Altarelli et al., "European X-ray Free Electron Laser. Technical Design Report", DESY 2006-097, ISBN 978-3-935702-17-1, July 2007.

[36] E. A. Schneidmiller, M. V. Yurkov, "Photon beam properties at the European XFEL", XFEL-EU TR-2011-006, September 2011.

[37] J. Gaudin, H. Sinn, Th. Tschentscher, "The European XFEL in Hamburg: status and beamlines design", UVX 2010 (2011) 63-67.

CHAPTER 2

Imagers for the European XFEL

2.1 Detectors for the experimental end-stations

The European XFEL will be used for diffraction experiments in which the sample under study is illuminated by the X-ray flashes and the scattered photons carry the desired information. Typical sets of experiments will be of spectroscopic nature, where the emission lines of a highly excited state of specimen must be recorded as function of energy. Another set of experiments consists of the detection of elastic or inelastic scattering from a sample where a set of diffraction lines must be recorded as a function of position in space. On one hand the scattering function can be local in space, i.e. it may consist of a single diffraction line of high

intensity (Bragg or Bragg-like scattering); here one has to detect the correct position (scattering angle) and scattering intensity (integrated intensity of the whole scattering curve). On the other hand the scattering can be nearly uniform in space (diffuse scattering), but exhibit characteristic features which have to be identified above the uniform background.

The realization of these experiments has a high demand for appropriate detectors, since all scattering events have to be detected in space, time and energy. Many of the requirements and challenges are intrinsic and common to all XFEL sources. However, an additional challenge for the detectors at the European XFEL, as compared to other systems at LCLS, SCSS or at the FERMI project in Italy, is the non-uniform time structure of the source. For instance, LCLS and SCSS use so called “warm” (meaning non-superconducting) accelerator technology and produce 120 and 60 evenly spaced pulses per second, respectively [1]-[3]. On the contrary, the European XFEL will use superconducting accelerating cavities, with the capability to produce an extremely high number of pulses per second and the drawback that all flashes have to be delivered in only 0.6% of the time to avoid heating of the system. Moreover, since the system has great flexibility in the filling pattern of the bunch train, the detector should be programmable to receive any bunch pattern. This irregular time structure has major consequences for the X-ray detectors design.

To read out the signal different detector systems are under development, which meet the various requirements in different wavelength ranges and with different properties. For instance, the very large energy range from 250eV for SASE-3 up to 90keV for U1 and U2 cannot be covered by a single detector or detector technology and different systems need to be developed, each one optimized for a limited energy range. A common requirement for all systems is the ability to deal with the very fast repetition rate of light pulses, as single-shot imaging capability is fundamental for various experiments where the sample under study is destroyed by the X-ray pulses and no averaging techniques can be employed (Figure 2.1) [4].

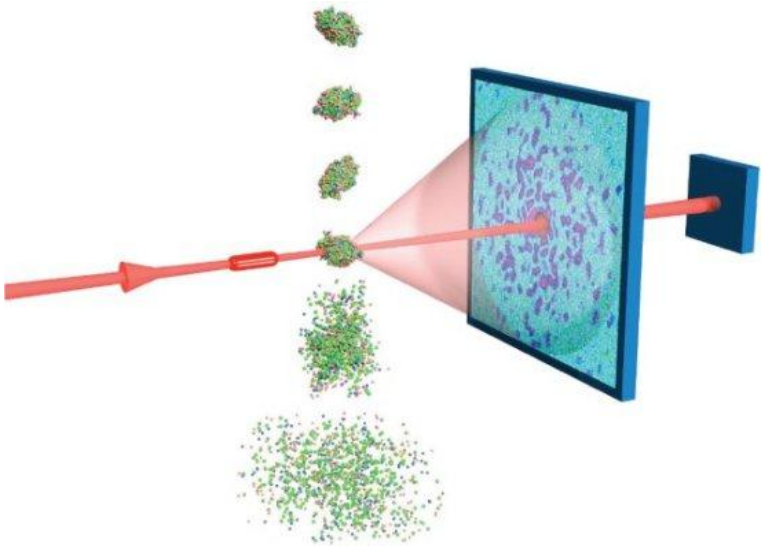

Figure 2.1 *Sketch of an experiment in which the sample under study is destroyed by the highly energetic X-ray pulse. This can be the case of Single Molecule Imaging and Coherent X-ray Imaging experiments.*

In fact, even though the energy absorbed by a particle during an ultra-intense XFEL pulse will destroy its chemical structure because of massive ionization and a subsequent Coulomb explosion of the sample, a pulse that is short enough should still yield relevant scattering information directly related to the original electron density of the particle. This is because the X-rays are scattered before the Coulomb explosion occurs [5]. In addition, the detector systems must be large size for angular coverage and have a high dynamic range. As a final note, it must be considered that the extreme photon flux will generate a total absorbed dose in the 100Grad range within few years of operation for high energy photons and 500μm thick silicon sensor. In fact, some of the experiments expect a maximum of $5x10^4$ photons per pulse per pixel and for small angle scattering, as well as for liquid scattering experiments, these intense parts will always be more or less in the same place of the detector. Even though this is a worst case scenario and the total integrated noise might well be much lower, radiation tolerant technologies for both the sensor and the front end electronics are mandatory.

Detectors types include point, linear (1-dimensional) and area (2-dimensional) systems for electron, particle and photon detection. The detectors will be fully functional and commissioned systems, integrated into the general DAQ. The current main focus is on 2-dimensional X-ray detectors, for which three different projects are being designed: AGIPD, DSSC and LPD. In the following part of the section a brief description of the various detectors is provided, with particular attention to the DSSC project that is the framework of this dissertation.

2.2 Single point and linear detectors

A certain class of experiments foreseen at the European XFEL could be served very well by 1-dimensional detectors, at least in the beginning [6]. Examples are liquid scattering, or powder diffraction experiments of non-oriented samples, when the scattering pattern is circularly symmetric. Femtosecond Diffractions Experiments (FDE) requirements in particular can be well covered by this type of systems. Another, very important area where 1-dimensional detectors are of prime importance is for beam diagnostics and beam steering.

Currently an inventory of the requirements for the different 1-dimensional detectors is being made, with the goal to design a solution that is as generic as possible. A lot of the requirements for these systems are similar to the 2-dimensional detectors. Thus, it is envisaged that parts of the system, in particular the back end electronics, will be common.

2.3 2-D detectors requirements

Requirements for the 2-dimensional X-ray detectors are described in [7]. In the following a brief summary of the main aspects that drive the design is provided. Additional requirements are strongly dependent on the scientific experiment. These include for instance angular coverage

and detector size, angular resolution, pixel size and number of pixels, in vacuum operation capability and sample to detector distance.

For what concerns the photon energy range, if direct detection in silicon is used and single photon sensitivity is required at low energies along with the ability to measure up to 10^4 photons per pulse per pixel even at higher energies, then combining the two aspects in a single system becomes very challenging. The different photon energies will also have different consequences for possible radiation damage, in particular for underlying microelectronics in case of hybrid pixel detectors. In fact, whereas 250eV photons are fully absorbed by 300µm thick silicon sensors, 25% of the 12keV photons will be transmitted (Figure 2.2). In this case special radiation hard electronic structures have to be used. For all of these reasons, a dedicated optimization for different photon energies is appropriate.

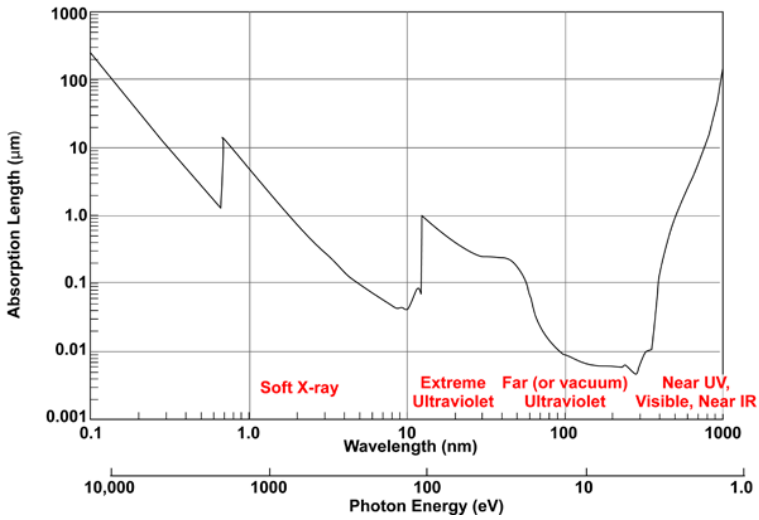

Figure 2.2 *Absorption length in silicon at different photon wavelengths or equivalent energies.*

Single shot imaging capability is very important for all the experiments in which the sample under study will not survive the X-ray flashes. Every single shot has to be treated as a separate experiment in these cases. For statistical relevancy many pixels in the imager must

record more than one photon, thus excluding the possibility to do photon counting to achieve high signal to noise ratios. Consequently, for these experiments integrating X-ray detectors will have to be used. For single shot imaging to be effective, a complete image has to be recorded every 220ns during the 600μs long macro bunch. Since it is not possible with current technology to transmit a full image in the short time between X-ray pulses, the front end electronics must provide storage capability and send the information out during the long burst gaps. This means either an analog or digital pipeline per pixel. In case the first solution is employed, special care has to be taken to assure that the signal is not altered by the leakage of both the storage capacitors and the switches.

Ideally, the detector system should be able to store all images during the pulse trains, which would mean large pixel sizes. This is not acceptable for many applications, so that a compromise, based on the scientific application, is most likely needed. Fast triggering and vetoing will be used to store only useful images. For instance, this can be useful when fast moving samples are under investigation, and not every X-ray pulse overlaps with the sample in time and space. Moreover, since the European XFEL is based on the SASE principle, the accelerator might occasionally produce low intensity and unusable pulses that have to be vetoed.

Since the primary X-ray beam has sufficient energy to ablate most materials, small primary beam stops cannot be used in front of the detectors, as it is customary at storage ring sources. Therefore, the X-ray imaging detectors in the forward scattering direction need a central hole to let the direct beam through. To minimize the loss of small-angle data this hole has to be as small as possible, while still being large enough to allow for occasional small fluctuations in the direct beam position.

2.4 2-dimensional detector systems projects

To meet the described requirements for 2-dimensional imaging systems three independent projects have been funded to meet the

challenging aspects of the European XFEL in a conceptually different manner. Common sensor issues have been studied collaboratively. These include the capability to reach a high dose [8] and to control the charge explosion of the e-h pairs generated in the detector. At the same time, they target different applications and wavelength ranges.

All three projects agreed on the use of the IBM 130nm CMOS technology for the front end electronics design. This technology will be the standard for LHC upgrades, based on the excellent experience with the 250nm process already employed. The 130nm technology is well established for layout based radiation hardening, permits sufficiently high integration intensity and provides long term availability. The development of some common blocks like LVDS IOs and enclosed standard cells will be shared among the groups.

The main characteristics of the projects are outlined in the remaining of this Chapter. Similar 2-dimensional systems are under development also in the United States for the LCLS source [9]-[10].

2.4.1 The AGIPD project

The Adaptive Gain Integrating Pixel Detector (AGIPD) is a hybrid pixel detector that employs a dynamically switched gain to accommodate the large dynamic range, with a silicon-sensor bump-bonded to a read out ASIC [11]. The AGIPD Project is led by DESY and is a collaboration between DESY, Paul Scherrer Institut (PSI), University of Bonn and University of Hamburg.

Each pixel contains a charge sensitive amplifier with three different gain settings which integrates the current generated by X-ray absorption. The gain of the preamplifier is dynamically switched, so that when the integrated signal rises towards the preamplifier’s upper limit, the pixel commutes to a lower gain setting. An analog pipeline for in pixel frame storage during the bunch trains is used, and the recorded images are subsequently read out and digitized off-chip during the 99.4ms interval between bunch trains (Figure 2.3).

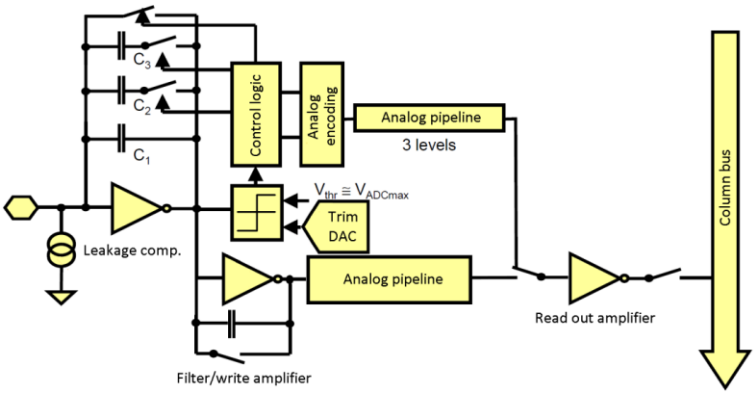

Figure 2.3 *Schematic layout of the pixel cell for the AGIPD detector.*

The storage capacitors in the pipeline have to be low leakage, which is possible using either MIM (Metal-Insulator-Metal) capacitors or DGN (dual oxide n-FET in n-well) capacitors. A major concern for the AGIPD design is the switches that connect the amplifier to the storage capacitors. They should permit charging within the 220ns inter-bunch spacing, but minimize discharging due to leakage. At the same time the storage cells have to be kept as small as possible in order to record the maximum possible number of images during the bunch train.

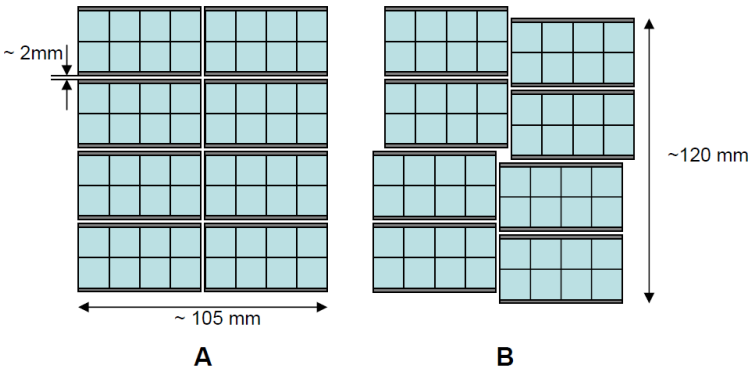

Figure 2.4 *Layout of the 1M pixel detector, built with modules of 2x4 ASICs with a monolithic sensor. A) and B) show two different layouts, where B) provides a central hole for the primary beam.*

The goal is to build a 1 mega pixel detector composed by four quadrants, with 200μmx200μm pixel size containing more 350 storage capacitors, and a central hole for the primary, un-scattered beam (Figure 2.4). The quadrants that compose the imager can be moved with respect to each other in order to adjust the central hole size. The silicon sensors and read out ASICs will be mounted in vacuum, while the interface electronics will be housed at ambient pressure to facilitate access for maintenance. The main scientific applications are Coherent X-ray imaging and Photon Correlation Spectroscopy at 12keV photon energies. The noise requirement is about 300 to 400 electrons, to allow for the requested single photon sensitivity [12].

2.4.2 The LPD project

The Large Pixel Detector (LPD) is also a hybrid pixel detector, using three different gain settings (low, medium and high) in parallel per pixel as well as three corresponding analog pipelines (Figure 2.5). An analog-to-digital converter will be included in the chip.

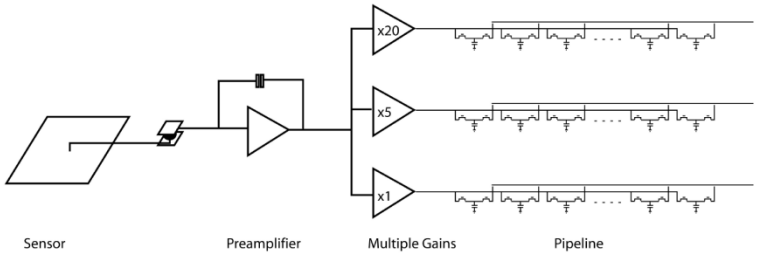

Figure 2.5 *Schematic layout of the pixel cell for the LPD detector.*

The LPD front end module will include an interposer between the silicon sensor and the ASIC, which gives the flexibility to have different pixel sizes and layouts between the two parts. It also provides extra radiation shielding, relaxing the required radiation hardness of the ASIC. The three fold layout requires relatively large pixels of 500μm, and hence the name of the project.

An interesting aspect of the LPD approach is the possibility to string together the three analog pipelines, which will allow to record up to

1500 images per macro bunch. To exploit this option the required gain setting has to be know in advance, which is normally the case for liquid scattering experiments where the scattering pattern is very reproducible.

Each LPD chip will contain 16x32 pixels and 8 chips will be bump bonded to a monolithic sensor to give a 128x32 pixels tile. Sixteen of these tiles will be used to obtain the so called super modules with 256x256 pixels that can be used to construct the final 1024x1024 pixels imager. A central hole for the direct beam transport will be included [13].

The LPD focuses on the 12keV photon energy range, and is optimally suited for liquid scattering experiments. The project is managed by the detector group of the Rutherford Appleton Laboratory and executed in conjunction with the University of Glasgow.

2.4.3 The DSSC project

The DEPFET Sensor with Signal Compression (DSSC) project adopts a pixellated detector architecture based on an innovative single pixel structure [14]. The detector has a non-linear gain response to provide signal compression and relax the large dynamic range requirements for the following electronic. The pixel has a hexagonal shape with size of approximately 200x200μm^2. Even though the system will be able to work at room temperature, the optimum working point will be at -30°C [15].

An advantage of the DEPFET based detector is the low noise performance, which makes this solution well suited for low energy experiments, down to a few hundreds eV. For instance, the corresponding specification for the DSSC system is to have an Equivalent Noise Charge (ENC) of less than 50 electrons r.m.s., enabling single photon resolution with a SNR of at least 5 for 1keV photons at maximum operating frequency. For the high energy range, the system is designed such that the resolution is limited by the Poisson statistics at of incoming photons. In this way it is possible fulfill the requirements of noise, dynamic range and speed simultaneously. The target energy range is from 500eV up to 12keV photons, with optimized performances for energies up to 6keV

and a dynamic range greater than 6000 photons (at 1keV) per pulse per pixel. The capability to read out the signal with the challenging 220ns frame rate combined with low energy single photon resolution goes beyond all existing instruments.

The detectors are each connected to a dedicated read out channel in a custom mixed signal ASIC to be bump bonded to the detector matrix. This type of connection minimizes stray capacitances and easily accommodates the connections for the 1024x1024 foreseen channels. The read out ASIC has built-in ADC and digital pipeline storage that follow the analog filter stage. It will possible to store at least 640 frames per macro bunch in each pixel. A veto mechanism will give the possibility to discard uninteresting events during the burst.

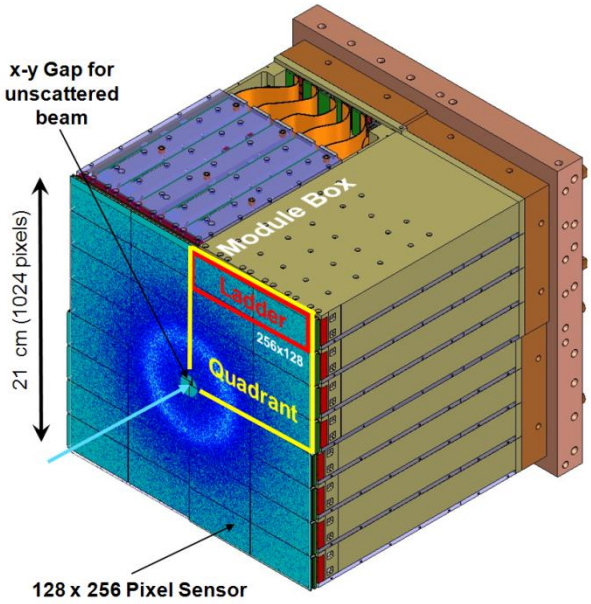

Figure 2.6 *Full instrument arrangement, composed of four quadrants geometrically arranged such that a central hole is left for unscattered photons.*

The total sensitive area will be of approximately 210x210mm². The ASICs will be connected to a monolithic DEPFET sensor of 128x256 pixels. Two of these monolithic units will be used to build a ladder with

128x512 pixels, that can then be stitched together to form the final 1M pixels imager. The insensitive area between the individual detector modules is about 15% with the present mechanical design. As in the AGIPD and LPD projects, a central hole in the forward scattering direction will be present to let the direct beam pass through without damaging the imager (Figure 2.6).

The DSSC Consortium, led by MPI-HLL (Munich), has the following partners: Deutsches Elektonen Synchrotron DESY, Ruprecht Karl Universität Heidelberg, Politecnico di Milano – Dipartimento di Elettronica e Informazione, Università degli Studi di Bergamo and the Universität Siegen.

This PhD dissertation places itself in the framework of the DSSC project, so this detector system is described in details in Chapter 3, underlining the project aspects that have a direct consequence on the analog filter design. The front end design is analyzed in Chapter 4, while measurement results are presented in the last Chapters.

2.4.4 Comparison between the 2D imagers projects

The key characteristics of each detector system are summarized in the following Table 2.1.

Comparison between the 2D imagers projects			
	AGIPD	LPD	DSSC
Detector type	Hybrid pixel detector	Hybrid pixel detector	DEPFET-based
Target energy range	12keV	12keV	0.5keV–12keV
Number of pixels	1024x1024	1024 x 1024	1024x1024
Pixel size	200μm x 200μm	500μm x 500μm	200μm x 200μm
Noise	~300-400el$^-$	~700el$^-$	~50el$^-$
Concept	Adaptive gain switching	Multiple gain paths	Non-linear detector
Data storage	2 bit digital and analog	Threefold analog	Digital (SRAM)
Storage capability	>350	up to 1500	>640

Table 2.1 *Comparison between the main properties and characteristics of the three projects under development for 2D imagers.*

2.5 Bibliography

[1] G. Penco, "Overview of FELs under construction including FELs at Fermi Elettra, SPring-8 and Frascati SPARC".

[2] J. Arthur, et al., "Linac Coherent Light Source (LCLS) Conceptual Design Report", SLAC-R-593, April 2002.

[3] T. Shintake and XFEL/SPring-8 Joint Team, "Status report on Japanese XFEL construction project at SPring-8", Proceedings of IPAC'10, Kyoto, Japan (2010).

[4] H. N. Chapman et al., "Femtosecond diffractive imaging with a soft-X-ray free-electron laser", Nat. Phys. 2 (2006) 839.

[5] R. Neutze, R. Wouts, D. van der Spoel, E. Weckert, and J. Hajdu, "Potential for biomolecular imaging with femtosecond X-ray pulses," Nature, vol. 406, no. 6797, pp. 752–757, Aug. 2000.

[6] M. Altarelli, et al., "The European X-ray Free Electron Laser technical design report", DESY 2006-097, ISBN 978-3-935702-17-1, July 2007.

[7] H. Graafsma: "Requirements for and development of 2-dimensional X-ray detectors for the European X-ray Free Electron Laser in Hamburg", Jour. Inst. 4 P12011, 2009

[8] A. K. Srivastava et al., "Numerical Modelling of Si sensors for HEP experiments and XFEL", Proceedings 9th International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors, 2009 Florence, Italy [PoS(RD09)019].

[9] L. J. Koerner, H. T. Philipp, M. S. Hromalik, M. W. Tate and S. M. Gruner, "X-ray tests of a Pixel Array Detector for coherent x-ray imaging at the Linac Coherent Light Source", 2009 JINST 4 P03001.

[10] G. A. Carini et al., "Tests of small X-ray Active Matrix Pixel Sensor prototypes at the National Synchrotron Light Source", 2009 JINST 4 P03014.

[11] B. Henrich et al., "The adaptive gain integrating pixel detector AGIPD a detector for the European XFEL", Nucl. Instr. and Meth. A (2010.

[12] A. Marras, "Front end electronics for European XFEL sensor: the AGIPD project", International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (PIXEL2012).

[13] A. Blue et al., "Edgeless sensor development for the LPD

hybrid pixel detector at XFEL", Nuclear Instruments and Methods in Physics Research A 607 (2009) 55-56.

[14] G. Lutz et al., "DEPFET Sensor with intrinsic Signal Compression developed for use at the XFEL free electron laser radiation source", Nuclear Instruments and Methods in Physics Research A 624 (2010) 528-532.

[15] M. Porro et al., "Expected performance of the DEPFET sensor with signal compression: A large format X-ray imager with mega-frame read out capability for the European XFEL", Nuclear Instruments and Methods in Physics Research A 624 (2010) 509-519.

CHAPTER 3

The DSSC project

3.1 The DEPFET detector

The DEPFET (DEpleted P-channel FET) concept has been proposed by J. Kemmer and G. Lutz in 1987 [1]. It is a silicon radiation sensor that combines both detection and amplification in a single device. This result is obtained by exploiting the advantages of sideward depletion [2] and by implementing a p-channel FET transistor on a high resistivity, high purity and fully depleted n-type silicon bulk (Figure 3.1). In common sideward depleted sensors the stray capacitance due to connections from the detector to the read out electronic worsens the noise performances of the system. This problem is no longer present with

DEPFETs, as the amplification of the signal is directly realized at the detector level. Therefore, this solution allows minimizing the parasitic capacitance associated with the anode and obtaining a very low noise, which has anyway to be maintained by the following read out electronic [3]. Arrays of DEPFETs of this type are used as active pixel sensors for X-ray imaging spectroscopy, for example in satellite-based X-ray observatories [4].

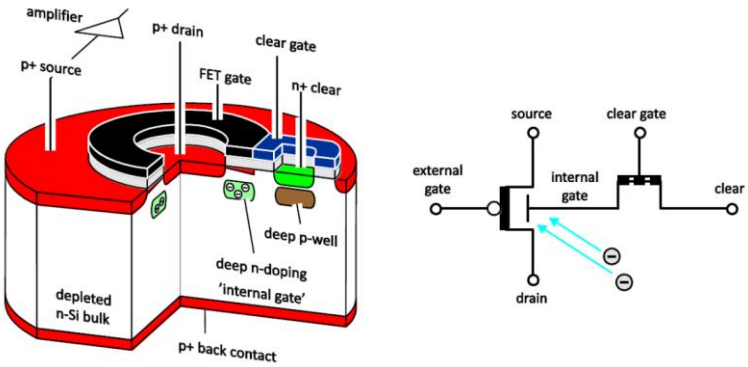

Figure 3.1 *Cutaway of a cylindrical DEPFET (left) and device symbol (right). Signal electrons are collected in the 'internal gate', modulating the transistor current. These charges can be removed via the n-MOS 'clear' transistor. A large area diode is realized on the opposite side of the wafer.*

As shown in Figure 3.1, a p-channel FET is located on one of the two surfaces of the detector, while on the other side a p-n junction is grown. The gate voltage determines the proper DEPFET biasing conditions to minimize the noise contribution and maximize the gain [3]. The n-type bulk is completely depleted by biasing at negative voltages the p^+ contacts of the back and transistor with respect to the voltage of the substrate. The entire bulk is therefore sensitive to incident radiation and the backside can be used as an entrance window improving spectroscopic performances, especially for low energy photons.

After full depletion of the detector volume a potential minimum for electrons occurs at a plane parallel to the front. Solving the one-dimensional Poisson equation with the given boundary conditions

($\varphi(0) = V_u$, $\varphi(d) = V_d$) yields the potential distribution φ as a function of the depth z in the detector substrate (Figure 3.2):

$$\varphi(z) = \frac{qN_D}{2\varepsilon_S} z(d - z) + \frac{z}{d}(V_d - V_u) + V_u$$

where q is the elementary charge, N_D is the doping concentration of the substrate, d is the total wafer thickness, ε_S is the dielectric constant of the semiconductor and V_d, V_u are the voltages applied to the back and the front side, respectively. Thus, the depth of the potential minimum z_{min} is given by:

$$z_{min} = \frac{d}{2} + \frac{\varepsilon_S}{qN_D d}(V_d - V_u)$$

If the voltages are equal the potential minimum is formed in the middle of the detector, while by applying asymmetric voltages it can be shifted arbitrarily in depth. The principle of sideward depletion is commonly used in semiconductor drift chambers [2].

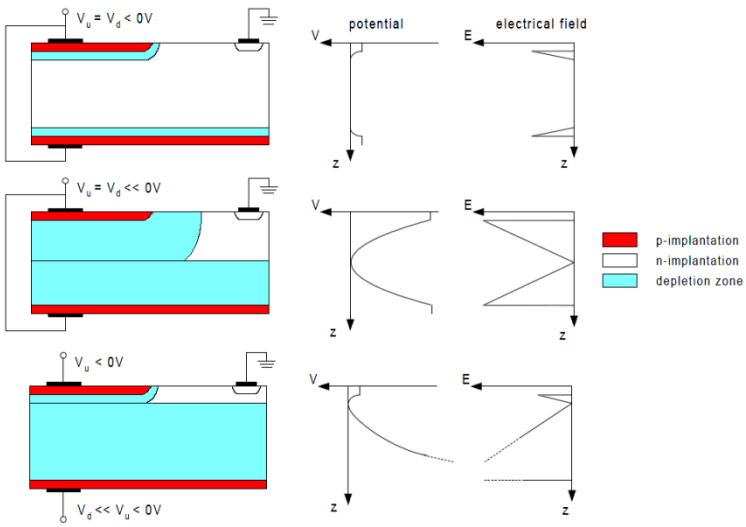

Figure 3.2 *Principle of sideward depletion (left). Distribution of the resulting electrical field (right) and potential in the detector substrate (center) for different biasing conditions.*

By buried doped regions and by applied voltages the local minimum for electrons in the DEPFET is located underneath the transistor channel at a plane parallel to the front (Figure 3.3). Due to asymmetric voltages at the transistor channel (about -5V) and the detector backside (about -100V), the potential minimum plane is shifted very close to the detector surface, where the embedded transistor is located. By additional n-implants below the transistor this region is confined laterally.

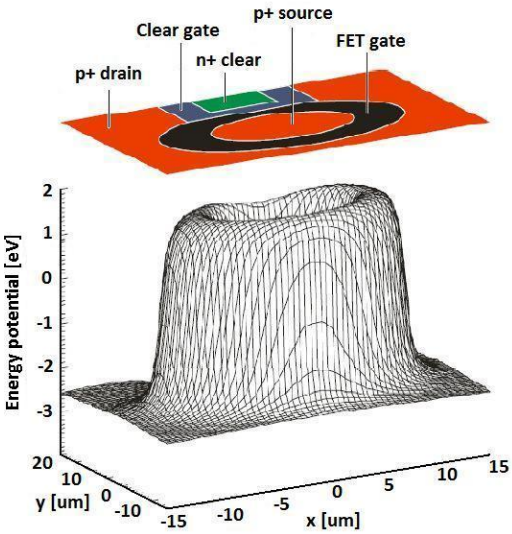

Figure 3.3 *Potential distribution inside the silicon bulk across a section parallel to the device front surface in normal working conditions.*

Electron-hole pairs released in the bulk by thermal generation or by absorption of ionizing radiation are separated by the internal depletion field. While holes travel towards the back contact, electrons are collected and stored in the potential minimum that acts as collecting anode. As signal and thermally generated electrons are collected, the electric field inside the device is modulated. If the gate and source voltages of the p-channel transistor are fixed, the charge enhances the channel conductivity by inducing positive mirror charges. Therefore, the measurement of the DEPFET current provides the information on the amount of stored charge and thus on the absorbed energy. Alternatively for fixed transistor current (source follower configuration) the source voltage will change after

charge collection. Because of its current steering function the potential minimum is called internal gate, IG [5].

During the charge integration the clear contact is biased to a relatively negative voltage to repeal electrons. This contact is isolated from the substrate by means of a deep p-well. Moreover, the clear gate electrode is also biased to a negative voltage to create a barrier for the electrons that otherwise would flow from the IG to the clear contact.

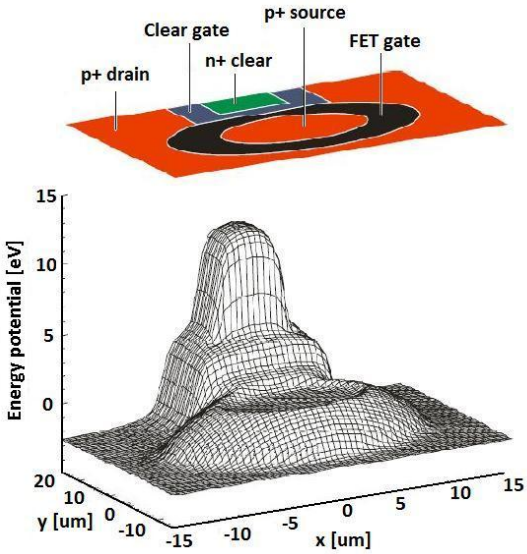

Figure 3.4 *Potential distribution inside the silicon bulk across a section parallel to the device front surface during the clear phase.*

However, it is necessary from time to time to remove the collected charge and avoid saturation of the internal gate. To achieve this result a positive voltage is applied to the n^+ clear contact. By also driving the clear gate contact the corresponding reset transistor is turned on creating a conductive path that removes the charges from the IG and drives them to the clear contact. The latter acts as a drain for the electrons. The energy potential in the bulk when the clear signal is applied is depicted in Figure 3.4.

It has been experimentally demonstrated that the clear procedure does not introduce additional noise contribution. In other words, there is no statistical fluctuation in the amount of left over charge. This characteristic qualifies the DEPFET as a “reset noise free” device [6]. For what concerns the read out procedure, charge can be measured by the current increase after charge collection or by the current difference before and after clearing of the IG.

Since the electrons are confined in a potential well, the read out of the signal does not destroy the information on absorbed energy. For this reason, apart from offering detection and amplification for incoming photons, the detector also acts as an analog memory cell with respect to the collected charge, providing signal storage capability for on-demand read out. It is worthwhile to underline that the IG is present even when no current is flowing in the external FET structure. The device can be switched on only to read out the signal. Thanks to this characteristic, it is not mandatory to have a dedicated read out channel per DEPFET pixel. For this reason, DEPFETs have been used in a big matrix arrangement, with the possibility of random pixel access [7].

The sensitivity of the current from the external gate is defined $g_{m,E}$ (external transconductance) and can be very easily measured. Conversely, a measurement of the IG transconductance is very complicated, and it is even impossible to experimentally obtain the capacitance between this potential minimum and the transistor channel [3]. For these reasons, even though the charge is physically collected into the IG and amplified by its transconductance, it is simpler to associate the signal and noise sources to the external FET gate. The effects on the output current are made to be the same by the definition of an equivalent input capacitance C_{eq}.

To evaluate this parameter we suppose that a charge Q_{in} is collected into the IG, so that a DEPFET current variation ΔI_D is induced. We can therefore define the equivalent capacitance as:

$$C_{eq} = \frac{Q_{in}}{\Delta V_g}$$

where ΔV_g is the voltage to be applied at the external gate to obtain the same ΔI_D, with no collected charge. A C_{eq} in the order of 40fF has been calculated for a DEPFET biased at 100μA.

The gain G_q of the DEPFET can be defined as the current variation ΔI_D corresponding to a certain amount of collected charge Q_r inside the IG for a given gate-to-source voltage V_{GS} and drain-to-source voltage V_{DS}:

$$G_q = \frac{\Delta I_D}{Q_r}\bigg|_{V_{GS},V_{DS}} = \left[\frac{A}{e^-}\right]$$

The G_q can also be expressed in terms of the holes mobility μ_h and of the transistor gate length L for a given saturation voltage V_{DS}^{sat} [8]:

$$G_q = -\frac{\mu_h}{L^2} V_{DS}^{sat}$$

A common value for G_q in spectroscopy DEPFETs is around 200pA/e^- for a bias current of 100μA [9].

3.2 The DEPFET Sensor with Signal Compression

A large variety of DEPFET matrices have been developed in recent years. For the European XFEL project, a novel detector structure called DEPFET Sensor with Signal Compression (DSSC) is under development in which the IG extends beyond the channel into the source region [10]. As a consequence, only part of the electrons will be stored right under the channel, giving a large effect on the transistor current, whereas additional electrons will be stored increasingly under the source region, having a reduced effect on the transistor current. As a result, a non-linear gain characteristic is obtained. This feature allows having simultaneously high energy resolution at low signal charge and an extended dynamic range.

Apart from signal compression, the DSSC design brings the additional advantage of an increased charge handling capability with respect to standard DEPFETs. The maximum dynamic range is therefore extremely high for these devices. With the actual design a maximum of about 440fC can be stored into the IG.

The desired signal compression will be implemented by a triple staggered concentration of deep n-doping diffusions (Figure 3.5). This physical implementation also generates an electric field facilitating a short charge collection time and a fast clear process.

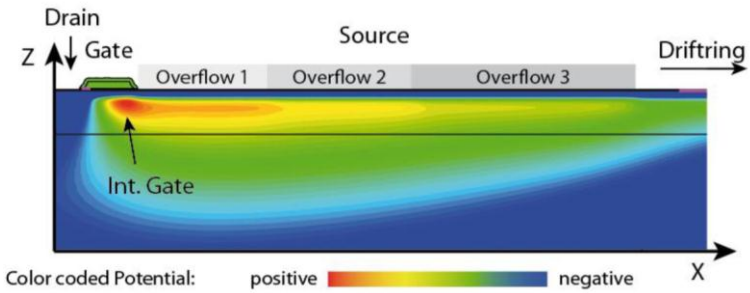

Figure 3.5 *Simulated potential of a DSSC detector. The color-coded potential indicates the staggered doping of the internal gate's overflow region.*

A fundamental parameter for the European XFEL application is the collection time of generated charges. If we consider the 220ns interval between two subsequent X-ray pulses, the longer is the time dedicated to signal collection, and also to the following DSSC clear phase, the shorter is the time available for the electronics to filter the signal. As a result, a higher noise is obtained, as white noise is the dominant source at these short processing times. To minimize collection and clear times each pixel will have a regular hexagon shape with a side length of 136μm. The DEPFET will be located in the middle of the structure, surrounded by a small drift chamber (Figure 3.6) [11]. The detector will be enclosed by two drift rings, with the outer one biased at a more negative voltage with respect to the inner. This configuration defines a funnel-like potential distribution guiding signal electrons towards the central DEPFET.

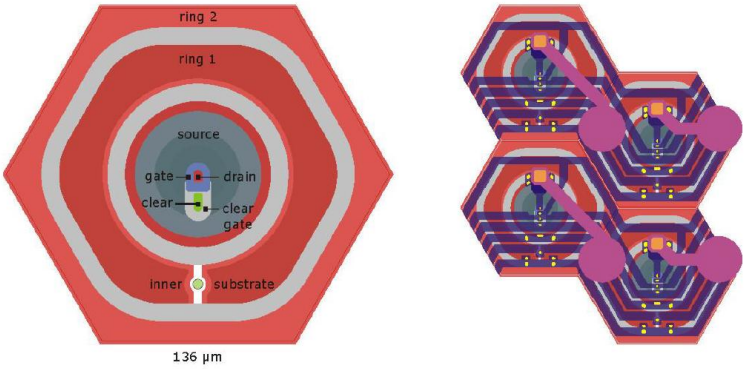

Figure 3.6 *Left: DSSC pixel layout showing the poly-Si gates, field plates (grey, blue) and doped regions (red, green). Right: 2x2 pixels detail of a sensor showing the zigzag on-chip wires in Al (dark blue) and the Cu connections (purple) to the circular bump bond pads.*

Compared to a square pixel of comparable area the hexagon has on average a shorter distance from the center to the edge, translating to a shorter charge collection time. It is expected that about 50-60ns will be necessary to collect charges from the far edges of the pixels, and the same amount of time will be necessary to obtain a good reset of the device. The collection and the clearing times are obviously independent from the operating speed of the European XFEL system.

The hexagonal shape of the drift rings will also provide a more homogeneous drift field and it will be more effective in focusing the charge into the internal gate. In addition the hexagonal shape minimizes the fraction of split events [11], i.e. absorption events close to the pixel border resulting in charge sharing between two or more neighboring pixels, as it provides a more efficient perimeter-to-area ratio. The DSSC mesh results in different pixel pitches in the horizontal (204µm) and vertical (236µm) directions. This size is compliant with the minimum pitch of 200µm allowed by the IBM C4 process that will be adopted to bump bond the read out ASICs.

From several conceptual and technological aspects the DEPFET array for the DSSC system is a completely new development. For this reason the production steps have been validated in recent years through

the realization of small scale prototype arrays. Of particular concern are: the realization of the signal compression, radiation hardness and bump bonding compatibility and yield. Different designs have been studied to obtain a consistent model description for the DSSC and optimize its performances. Production of the 128x256 full format sensors providing the desired shape of the non-linear response has started in June, 2011.

Regarding the compressive characteristic, a 7-cell cluster of non-linear DEPFETs was produced and tested at room temperature at MPI-HLL (Figure 3.7) [12]. The prototypes have been processed on a wafer together with spectroscopy-type DEPFET devices. For this reason the process technology was not the one optimized for DSSC performance. In particular, the prototypes have a thicker gate oxide and features only one n-diffusion for the overflow region. Thus the gain curve basically consists of two linear parts with different gain values. In any case these devices offered the opportunity to study the signal compression experimentally.

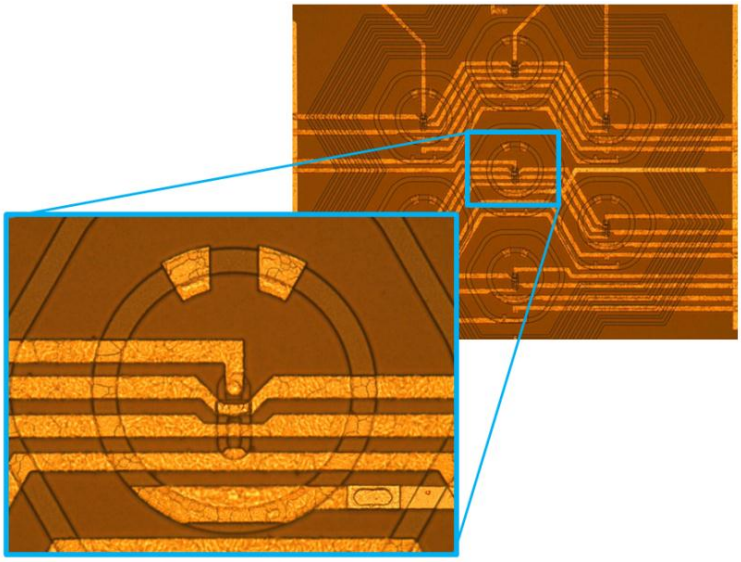

Figure 3.7 *Micro-photographs of a DSSC prototype device: seven cells cluster and close-up of the central device. The pixel format is identical and the detector layout similar to the final DSSC design. The cluster is enclosed by a series of guard rings.*

The detector was configured for drain current read out using an external current to voltage converter and associated ADC. AC signals for clear and clear gate were applied via programmable SWITCHER ICs [13]. Applying a series of calibrated laser pulses the non-linear gain curve has been directly measured (Figure 3.8). As expected, the linear region extends to an integrated energy of roughly 100keV. For comparison, in the final device a depth of the linear region of about 10keV is foreseen.

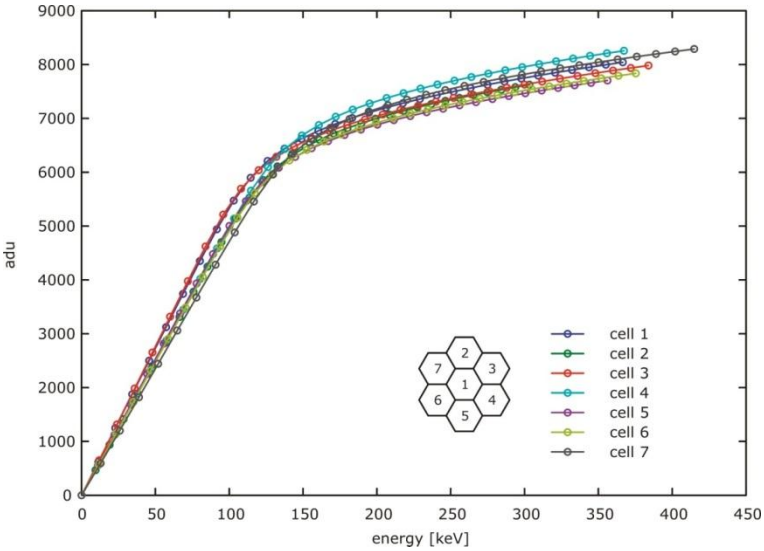

Figure 3.8 *Non-linear gain curves of the seven cells cluster DSSC prototype measured using a series of calibrated laser pulses.*

From the measurements on the 7-cells prototype, the sensitivity in the linear region is about 600pA per signal electron. In the compression region the gain is reduced by a factor of 17.5. The signal current reaches a maximum of about 25μA for the energy of 400keV. The pixel-to-pixel non-homogeneity of the seven curves in Figure 3.8 settles to a 10% level that in the final system can be compensated by the read out ASIC and calibration procedures. This measurement is the very first proof of principle of the new detector concept.

Figure 3.9 shows a room temperature simulation of the charge collection time for the final DSSC design in the case charge generation

takes place at the edge of the pixel, at a distance of 115μm from the center. In this worst case scenario about 60ns are sufficient to collect 99% of the injected charge into the internal gate. Faster collection times are expected for lower temperatures, since higher electrons mobility is obtained.

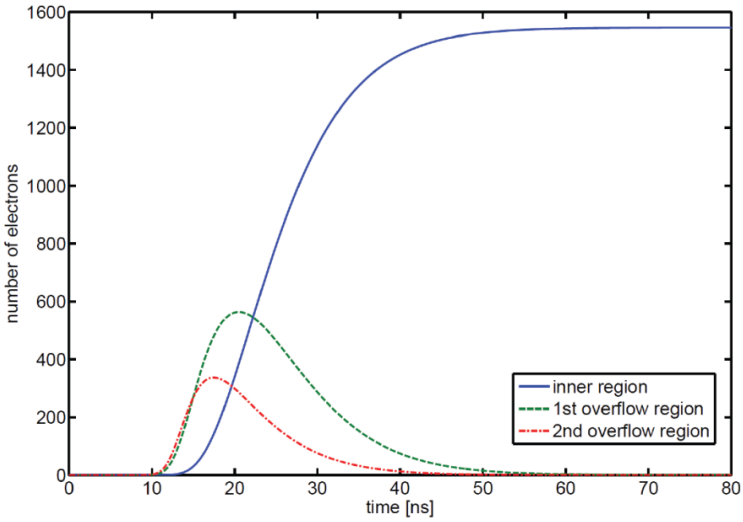

Figure 3.9 *Simulation of the charge collection for the final DSSC topology. The charge is generated at the edge of the pixel at a depth of 175μm. At the end, all the electrons are collected into the inner region of the IG (solid blue curve). Part of the charge transits through the first and second overflow regions (green dashed and red dashed-and-dotted curves).*

As a final remark, recalling the definition of the equivalent input capacitance given in the previous section, it is evident how the C_{eq} is not a constant parameter for these devices. In particular, its value increases with the signal level since to obtain the same output current variation it is necessary to collect more and more charge into the IG. These considerations make the noise evaluation of the system a task that must be carried out appropriately. For the DSSC project the goal is to have Poisson limited performance on the entire dynamic range. A detailed analysis of this topic is given in the section 3.5.

3.3 The read out ASIC

The DSSC based mega-pixel camera will feature 1024x1024 pixels, divided in four quadrants of 512x512 pixels each. Each quadrant will be realized by eight DSSC sensor chip, having a final format of 128x256. The associated mixed-signal read out ASIC will be composed by 64x64 channels and each block will be flip-chip connected to the DSSC detectors (Figure 3.10) [14].

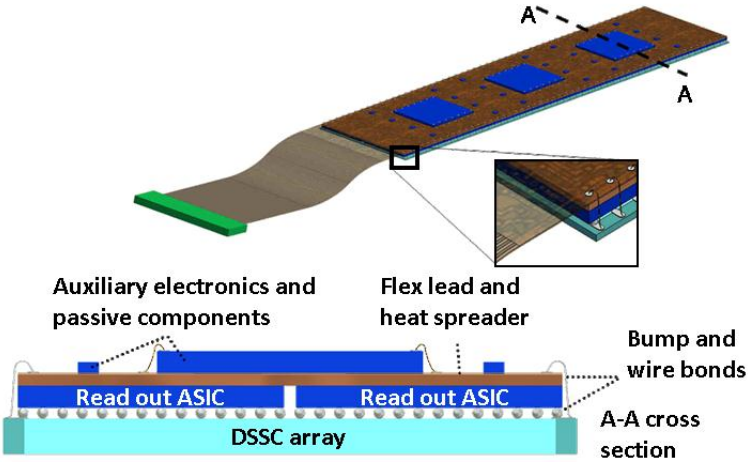

Figure 3.10 *Sketch of a ladder assembly, comprising a DSSC monolithic matrix and eight associated read out ASICs. To realize a full focal plane 16 ladders will be employed.*

Full parallel read out of all pixels is imposed by the high repetition rate of X-ray pulses. In fact, the 220ns interval avoids the possibility to multiplex several pixels to the same channel and read them out sequentially by exploiting the charge storage capability of the DEPFETs. As a consequence all pixels have to be powered during the pulse train. The size of a single electronic channel is limited by the DSSC pixel; however, its shape will be rectangular for simplicity. Taking into account the need of a lateral pads row for power supplies, digital control, input and output signals, the total area of the ASIC will be about 13x14mm^2.

The design of the ASIC is carried out by several institutions: the University of Heidelberg, DESY, the University of Bergamo and the Politecnico di Milano. In particular, Politecnico is mainly focused on the realization of the analog filter, which is the main subject of this thesis.

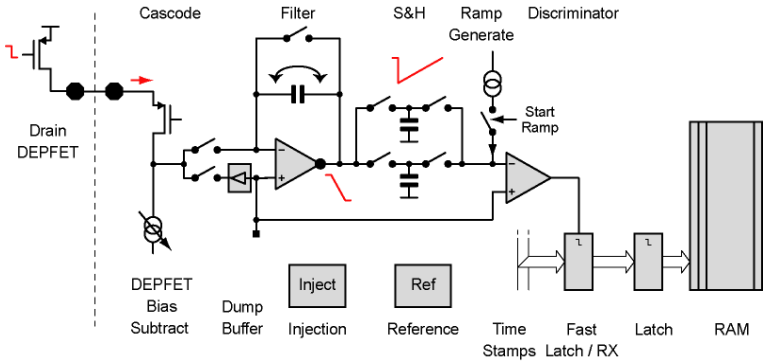

Figure 3.11 *Simplified block diagram of one pixel of the DSSC read out ASIC.*

Every channel in the chip will provide low noise read out and in-pixel digitization and storage of the DSSC signal by employing a current read out strategy. It will be able to run at the maximum speed of 4.5MHz and also allow for slower operation. A blocks diagram representation of the pixel architecture is shown in Figure 3.11. Apart from the blocks in the pixel, some global circuits like IO pads (both CMOS and LVDS), references, bias DACs, slow control, ADC control (Gray coded counter), RAM control, main control and a data serializer are provided in the ASIC.

The power dissipation is dominated by the DEPFET, the analog front end and the ADC. It will amount to about 1mW per pixel, so that one chip dissipates more than 4W when active. Only 300µA are available to power a complete read out channel. In order to relax the burden on the cooling system, nearly all elements will be turned off during macro bunch gaps. The cycling of the current is a mayor system challenge. Moreover, commercial power regulators are not fast enough to maintain a stable

voltage in the short macro bunch time. As a consequence external bypass capacitors are fundamental to provide the necessary charge to the system.

In the remaining part of the Chapter the key properties and the main design concepts of the channel building blocks are discussed. The design and realization of the analog input filter is covered in details in Chapter 4. The development and prototyping of all building blocks in the pixel, as well as of two first 8x8 complete matrices (mini-matrices MM1 and MM2), have been successfully carried out starting from 2009. A complete 64x64 ASIC will be submitted by the end of 2012. Representative results are shown in the remaining of this Chapter for the main building blocks, while for the analog input filter a detailed characterization is given in Chapters 5 to 7 along with results from the complete matrices.

3.4 The analog input filter

To achieve single photon resolution capability at low energies it is fundamental to reduce the front end noise contribution, providing the most suitable filter function with respect to the experiments constraints in terms of read out speed and energy resolution. To choose the appropriate strategy let's consider the following acquisition chain (Figure 3.12):

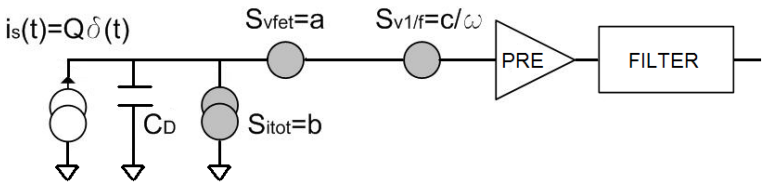

Figure 3.12 *Schematic representation of a read out chain. All the noise sources are referred to the input node. The detector is assumed to be equivalent to a current source i_s delivering a charge Q on the capacitor C_D. The electronic is composed by a pre amplifier followed by a filter.*

The bilateral power spectral densities of the physical noise sources of the system shown in Figure 3.12 are:

i. $S_{v,fet} = \frac{2\gamma k_B T}{g_m} = a$, series noise component mainly related to the thermal noise of the input transistor;

ii. $S_{v,1/f} = \frac{a_f}{|f|}$, 1/f noise component related to the trapping and release of charges in the transistor channel; a_f is the flicker noise coefficient;

iii. $S_{i,tot} = q(I_d + I_g) = qI_L = b$, parallel noise component given by the leakage current I_g of the transistor and I_d of the sensor.

The filter electronics can be represented by its weighting function *w*(t) normalized to unity area, such that a delta input signal Q_s produces an output response of amplitude Q_s/C_D where C_D is the input capacitance. The Equivalent Noise Charge (ENC) of the system can now be expressed as:

$$ENC^2 = aC_D^2 \int_{-\infty}^{+\infty} \omega^2 \, |W(\omega)|^2 \, \partial\omega + 2\,\pi\, a_f \, C_D^2 \int_{-\infty}^{+\infty} |\omega||W(\omega)|^2 \, \partial\omega + b \int_{-\infty}^{+\infty} \frac{|W(\omega)|^2}{\omega^2} \, \partial\omega$$

where $W(\omega)$ is the Fourier transform of the weighting function *w*(t). This formula can be written in the following equivalent form in which the terms related to the shape of the weighting function are separated from the terms connected to its duration:

$$ENC^2 = aC_D^2 A_1 \frac{1}{\tau} + a_f C_D^2 A_2 + b\tau A_3$$

The parameter τ is the shaping time, and it represents the duration of the output response of the filter. Its definition is arbitrary, but the values of the shape parameters $A_1 - A_3$ are derived from it:

$$A_1 = \frac{1}{2\pi} \int_{-\infty}^{+\infty} x^2 \frac{|W(x)|^2}{\tau^2} \, \partial x$$

$$A_2 = \frac{1}{2\pi} \int_{-\infty}^{+\infty} |x| \frac{|W(x)|^2}{\tau^2} \, \partial x$$

$$A_3 = \frac{1}{2\pi}\int_{-\infty}^{+\infty} \frac{|W(x)|^2}{\tau^2}\,\partial x$$

where the variable $x = \tau\omega$ has been used.

Considering that the DEPFET implements both the detection and amplification of the incoming photons it is possible to identify the pre amplifier stage of the DSSC chain with the device itself. The input capacitance C_D is given by C_{eq} (see section 3.1). It is therefore possible to express the ENC of the DSSC system as follows:

$$ENC^2(Q_{in}) = \frac{a}{\tau}C_{eq}^2(Q_{in})A_1 + 2\pi a_f C_{eq}^2(Q_{in})A_2 + b\tau A_3$$

where the dependency of C_{eq} from the input charge Q_{in} is put in evidence. It can be demonstrated that the ideal shape to minimize white series noise, which is the dominant noise source at the European XFEL fast operating speed, is the triangular [15-19]. The signal should be instantaneously delivered on the peak of the shape to maximize the gain. However, this weighting function cannot be realized since a finite time interval is needed for the X-ray pulse to arrive and electrons to be collected into the IG. The introduction of this flattop entails a trapezoidal weighting function (Figure 3.13). This shape still minimizes the white noise contribution, having the same factor A_1 as for the triangular case.

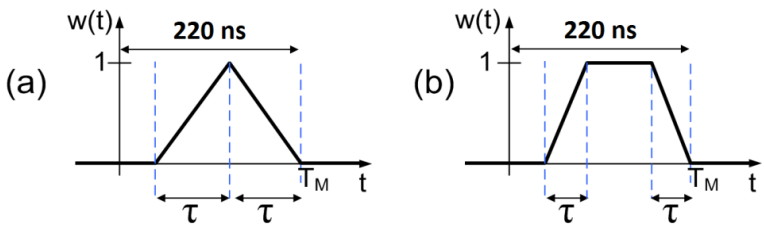

Figure 3.13 *Triangular (a) and trapezoidal (b) weighting functions. The first is the ideal time-limited shape to minimize noise, but cannot be implemented in the XFEL case since a finite time is necessary between the two integrations for charge generation and collection. The DSSC clear phase takes place at the beginning of the read out cycle.*

On the other side, the value of the other factors A_2 and A_3 increases with the flattop duration, making the contribution of the 1/f and of the parallel noise sources more important (Figure 3.14).

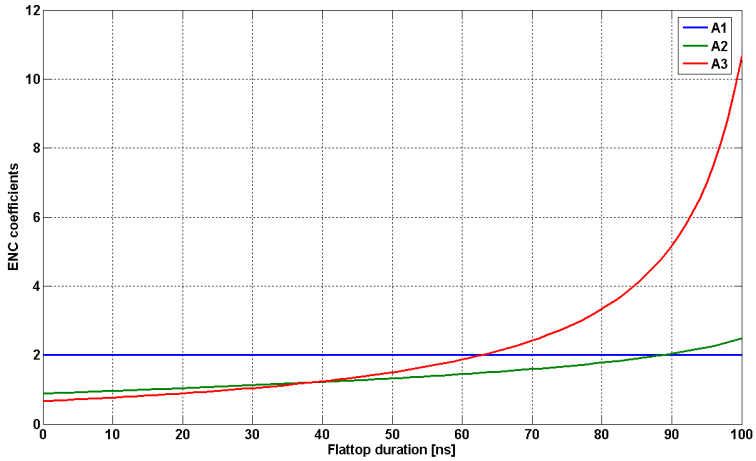

Figure 3.14 *ENC coefficients for different flattop values, considering an available processing time of 220ns and a clear phase of the same length of the flattop. The coefficients for the parallel and flicker noise components increase with the flattop duration.*

Since the signal arrival time in the European XFEL is known, a time variant filter implementing the desired weighting function can be successfully used. Two different read out techniques have been developed since 2009 and are described in the following, a source follower strategy at MPI and a current approach at Politecnico di Milano.

3.4.1 Source follower read out approach

DEPFET detectors have been usually read out in source follower mode. The first integrated circuits designed for DEPFETs based on this approach are CAMEX (CMOS Amplifier and MultiplEXer) [20] and ASTEROID [21], with a read out time from 4µs up to about 16µs. In this configuration the drain of the detector is biased with a constant voltage and the current flowing in the channel is set by a current source (Figure 3.15). Since the current in the FET channel is fixed, charges collected into the IG lead to a negative voltage shift at the source node, that is AC

coupled to the front end electronics. The amplitude of this step gives the information about the energy of the incident radiation.

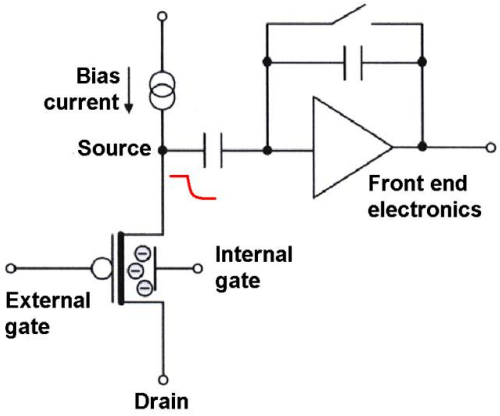

Figure 3.15 *Simplified schematic diagram of the source follower read out approach. The voltage at the source changes with a finite constant time due to the capacitive load at the node.*

This approach is intrinsically insensitive to threshold voltage variations that might be induced by either mismatches in the detectors matrix and by absorbed radiation. Any difference that can be present between sensors in the array leads to slightly different gate-to-source voltages without altering the signal measurement.

The main limitation of the source follower approach is the time needed to process the signal. After charge has been collected into the IG it is necessary to wait a certain amount of time to properly set the source voltage at the final value. This time is defined by the capacitive load at the source node and the transconductance of the DEPFET [6], as it will be obtained in the following. A small signal equivalent circuit for the DEPFET in source voltage read out topology is shown in Figure 3.16 [22]. C_p is the sum of the IG-to-back and IG-to-drain parasitic capacitances, while C_1 is the IG-to-source capacitance. When the detector works in saturation regime, this capacitance is dominated by the coupling between the IG and the conductive channel. C_2 is the input capacitance of the voltage preamplifier, with $C_2 \gg C_1$.

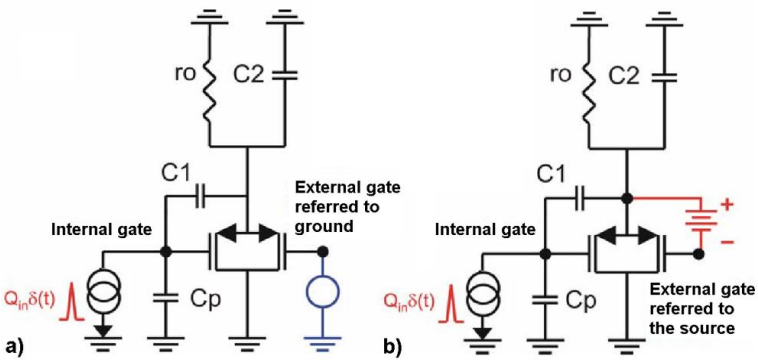

Figure 3.16 *Floating-gate equivalent circuits for the DEPFET in source follower configuration. In a) the external gate is referred to ground, while in b) it is referred to the source via a floating battery.*

The gain is independent of C_1, as the source-to-gate voltage remains constant due to the unitary voltage gain of the source follower. Thus, C_p should preferably be small to obtain a large amplification. If the external gate is referred to ground, the output resistance R_{out} of the system is determined by the parallel of the output resistance of the bias source r_o and the external transconductance of the detector $g_{m,e}$. The following approximated expression for the settling time can be obtained:

$$t_r \approx 2.2\left[C_1 + C_2\left(1 + \frac{C_1}{C_p}\right)\right]R_{out} = \left[C_1 + C_2\left(1 + \frac{C_1}{C_p}\right)\right]\frac{r_o}{1 + g_{m,e}\, r_o}$$

where r_o is usually about 50kΩ depending on the pixel geometry, while common values for $g_{m,e}$ are between 50μS to 100μS.

This finite time introduces a low pass filtering of the weighting function implemented by the filter when the detector is connected, thus worsening noise performances when the read out has be done in a short time. The final value of the source voltage can be expressed as follows:

$$\lim_{t\to\infty} v_{source}(t) \approx -\frac{R_{out} g_{m,i}}{C_1} Q_{in}$$

Figure 3.16 shows also a second possible configuration in which the external gate is referred to the source via a floating battery. In this case the output resistance of the system is defined only by r_o. As a consequence, the time response of the circuit is slower.

It is worthwhile to point out that the amplification of the system is directly proportional to the value of the output resistance, as it is the rising time of the signal at the source node. So a high amplification necessarily corresponds to a slow rising time. Another disadvantage of this configuration is that the voltage shift at the source node has to be compatible with the maximum allowed voltage at the input of the ASIC.

In the first phase of the electronics development for the DSSC project, the source follower approach has been studied and also implemented in the MM1 chip as a possible filtering scheme for the signal [23]. In fact, the small stray capacitance foreseen at the source node, on the order of 1pF, provides an estimated rising time of about 20-30ns. Even though the implemented weighting function is severely filtered such a value is still feasible with the 220ns X-ray pulses repetition rate.

To overcome the difficulty in modulating the bandwidth to optimize the signal-to-noise ratio the proposed source follower implementation made use of the same filter stage implemented for the drain current approach to synthesize a trapezoidal weighting function, as already done in ASTEROID (Figure 3.17).

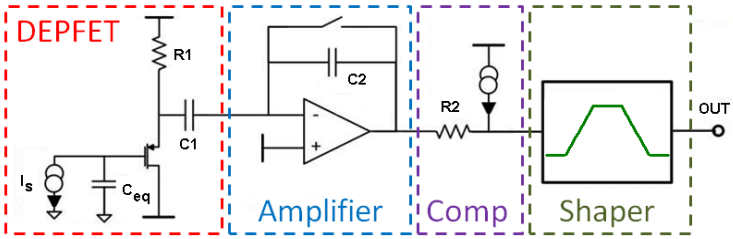

Figure 3.17 *Proposed source follower read out architecture, including a voltage-to-current converter (R_2), a current compensation stage and the trapezoidal shaper designed for the drain current read out mode.*

The input voltage step is converted to a current signal compatible with the input of the filter. The 100kΩ bias resistor and the 0.5pF coupling capacitor would have been integrated directly on the sensor pixel, complicating the design of the DSSC detectors. In addition, an offset current compensation at the output of the pre-amplifier was needed to account for the different DC levels between the output of the source follower amplifier and the input of the filter. Three different techniques have been studied and implemented for this purpose.

Initial simulations for the source follower configuration showed a long settling time up to 80ns in the worst case. Moreover, the noise performances obtained from the first ASIC prototype were not within specification (Figure 3.18). For the above mentioned reasons, the DSSC collaboration decided to focus on the current read out approach with its better noise performance, lower power dissipation and simplified sensor design.

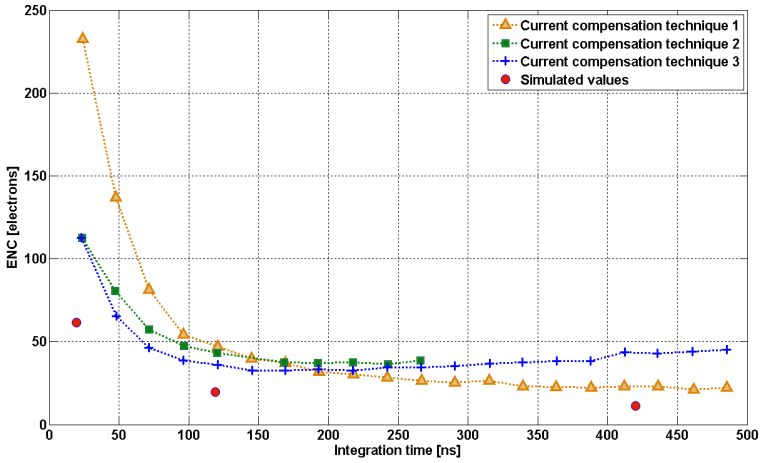

Figure 3.18 *Measured equivalent noise charge at the input of the source follower read out chain for the three implemented current compensation solutions, along with simulated values.*

3.4.2 Current read out approach

Even though less common than the source follower approach, current read out mode of DEPFET detectors has been already employed

in previous works [24-26]. In the basic current read out configuration, the detector is biased with a fixed gate-to-source voltage so that electrons collected into the IG produce a variation in the current flowing in the device (Figure 3.19). No passive components are required in the pixel cell, simplifying the sensor design and moving the DSSC bias power dissipation to the chip, which is better for thermal management. The detector drain can be made a low impedance node by introducing a cascode stage before the filter. In this way any parasitic capacitance that might be present at the node does not contribute a significant time constant, making it feasible to operate the system at high frequencies. In first approximation, the settling time of the system corresponds to the charge collection time. The output current follows the charge collection with insignificant delay [11]. It is worthwhile to note that in this configuration the detector has all external nodes at a fixed voltage. This is beneficial to obtain stable and repeatable performances from the detector.

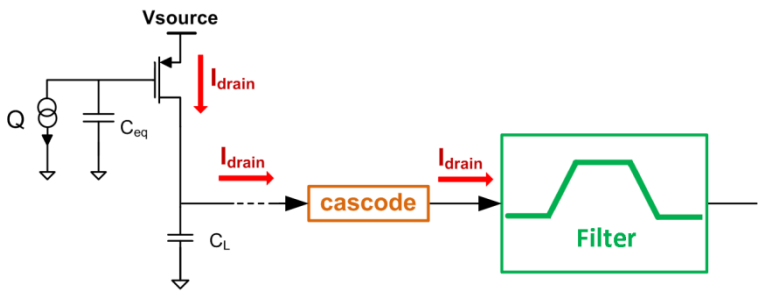

Figure 3.19 *Basic configuration of the current read out approach.*

Another advantage of this approach compared to the source follower read out is the possibility to bias the detector at relatively high current. As previously described, the tradeoff between rising time and gain sets a relatively small bias current for the latter approach. Conversely, in current read out mode a higher current leads to a higher gain G_q that reduces the input referred noise without major drawbacks. Common values for the detector current are around 100μA, and this is also the baseline value for the DSSC project taking into account power dissipation constrains.

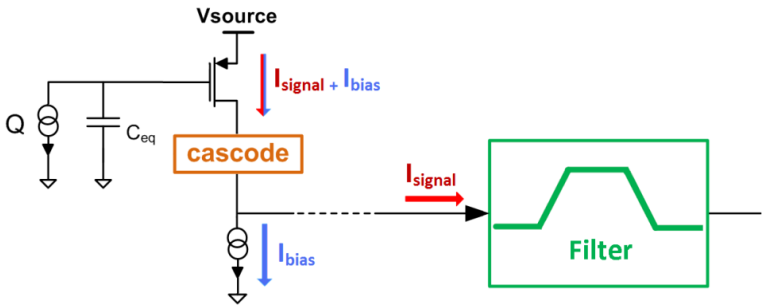

Figure 3.20 *Current read out basic scheme with the addition of a current generator to subtract the bias current of the detector and leave only the signal component to be processed by the trapezoidal filter.*

The bias current of the detector is normally removed by a programmable current source to leave only the current signal to be processed by the trapezoidal filter and thus maximize the output dynamic range (Figure 3.20). For the XFEL case this requirement is stressed by the limited voltage supply of the IBM technology. The current source also provides a mean to cope with threshold shifts and non-homogeneities in the detector array. In fact, the sensitivity to threshold shifts after significant dose irradiation is a potential drawback of the current read out solution if compared to the source follower technique that is a self adjusting configuration [27].

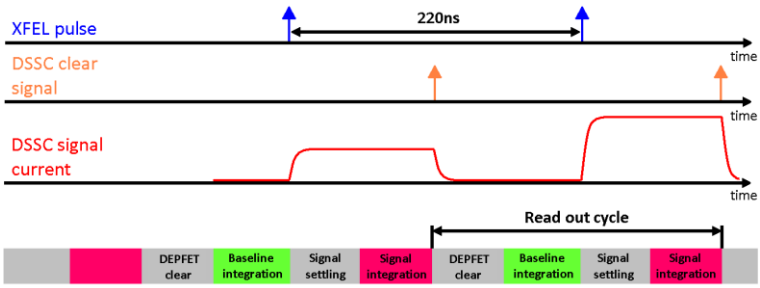

Figure 3.21 *Current read out timing scheme, showing the various phases of the time-variant trapezoidal filter (bottom row) along with a sketch of the XFEL pulses timing (top row), the DSSC clear signals (second row) and a simplified drawing of the signal current component (third row).*

To implement the trapezoidal shape two correlated measurements can be used. The corresponding timing scheme for the XFEL case is sketched in Figure 3.21. The result of a first integration of the current before signal arrival (baseline integration) is subtracted from the value of the subsequent signal integration. The duration of each integration represents the shaping time τ of the associated weighting function. Moreover, this implementation removes any baseline that might occur due to a non-optimum cancellation of the detector bias current and to reduce 1/f noise contribution [28].

In the following a detailed analysis of the filter action on the input current is derived. Let's define $I_{cascode}$ as the current delivered by the cascode stage. After a clear phase no charge is stored into the IG and its value can be written as $I_{cascode} = I_{bias} + n(t)$, where $n(t)$ represents the noise contribution from the detector. For what concerns the current generator, it is also necessary to include a constant value n_o corresponding to the sampled noise on the current source after the programming has completed. Thus it is possible to write:

$$I_{current\ source} = I_{bias} + n_o + n_g(t)$$

where $n_g(t)$ is the noise contribution of the generator. The current that flows to the filter during the first baseline integration is:

$$I_1 = I_{cascode} - I_{current\ source} = I_{bias} + n(t) - \left[I_{bias} + n_o + n_g(t)\right] = n(t) - n_o - n_g(t)$$

and for the corresponding output voltage variation:

$$\Delta V_1 \alpha \int_o^\tau \left[n(t) - n_o - n_g(t)\right]\partial t = -n_o\tau + \int_o^\tau \left[n(t) - n_g(t)\right]\partial t$$

Thus, as the n_o contribution is constant, in this first integration the detector and programmable current source noise contributions are averaged by the filter. The voltage is stored to be subtracted from the following signal integration result.

After charge collection into the IG the drain current in the DSSC detector, and thus the current delivered by the cascode, increases and can be written as follows:

$$I_{cascode} = I_{bias} + n(t) + I_s$$

where I_s represents the signal contribution. As in the previous situation, the filter receives the difference between the current from the cascode and that flowing towards the current source:

$$\begin{aligned} I_2 &= I_{cascode} - I_{current\ source} = \\ &= I_{bias} + n(t) + I_s - \left[I_{bias} + n_o + n_g(t)\right] = \\ &= n(t) + I_s - n_o - n_g(t) \end{aligned}$$

In this second case the output voltage variation is:

$$\Delta V_2 \alpha \int_{t_1}^{t_1+\tau} \left[n(t) + I_s - n_o - n_g(t)\right] \partial t = \\ = (I_s - n_o)\tau + \int_{t_1}^{t_1+\tau} \left[n(t) - n_g(t)\right] \partial t$$

where t_1 is the time the second integration starts. Taking the difference between the two voltage variations leads to the following result:

$$\Delta V_f = \Delta V_1 - \Delta V_2 \alpha - \tau I_s + \int_o^{\tau} \left[n(t) - n_g(t)\right] \partial t \\ - \int_{t_1}^{t_1+\tau} \left[n(t) - n_g(t)\right] \partial t$$

As can be seen, the final value of the output voltage is proportional to the input signal, while the noise is filtered by the two integrations. The sampled noise from the current source does not appear in the result since it is a constant contribution.

Even though the presence of the flattop does not directly impact the ENC, it reduces the available time for the integrations once the total processing time is given. For instance, with the European XFEL

operating at maximum speed only 45ns might be available in this configuration for each integration, since a considerable amount of time is needed for charge collection and for clearing of the detector. When slower operation will be employed, a longer time can be dedicated to each integration, thus improving the noise performances of the system. Since the drain current provided by the detector is independent from the timing read out scheme, to maintain the same output voltage swing in these cases it is necessary to reduce the gain of the filter.

To allow for longer integration times at high repetition rates an alternative read out scheme has been proposed, in which a single baseline measurement per macro bunch is done before X-ray pulses start to arrive. Then, between subsequent pulses a single, longer signal integration can be performed. With this approach the baseline value is stored on the current source generator, which can be programmed before every macro bunch start. The corresponding timing scheme for this second approach is shown in Figure 3.22. The time interval between the baseline measurement and the signal integration gets longer as X-ray pulses arrive. As a consequence, flicker noise is differently filtered for pulses in the macro bunch, the last one being the more affected by the reduced noise filtering efficiency.

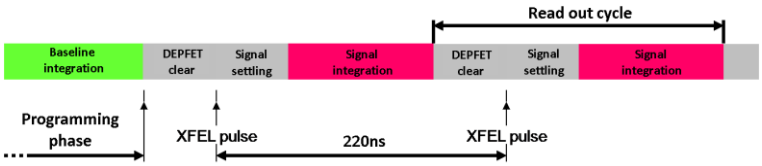

Figure 3.22 *Timing structure in which a single baseline measurement is done before the macro bunch starts, allowing for a longer integration in each cycle.*

3.5 Analog-to-digital converter

The output voltage of the analog filter is sampled onto a capacitor after the signal has been processed. While the following pulse is stored

onto a second capacitor, a single slope 8 bit ADC converts the information on the first one into a timing value (Figure 3.11) [29]. Due to its simplicity, low power consumption, and small area requirement this type of ADC is suitable for pixel-level implementations. The time required until the capacitor in the double buffer is discharged to a fixed threshold level is measured by latching gray coded time stamps. These are distributed column-wise to the pixels as low swing differential signals on coupled coplanar waveguides, with a fast 800MHz external clock that is used to toggle the counter on both edges. This gives a timing resolution of 65ps. The Gray Code minimizes the Hamming distance of two adjacent ADC bins therefore minimizing the probability of latching an incorrect value and also reducing the toggling frequency. The ramp is started with a precise strobe, common to the whole chip, along 13mm long transmission lines.

The foreseen full-scale range (FSR) at the ADC input is 800mV, ranging from 0.95V when no signal has arrived to 0.15V for the maximum signal. A serial control register stores data for adjusting the sample and hold capacitors, the current reference for the ramp generation, the pixel delay for offset compensation and the starting value of the gray code counter. The control data are written during an initialization phase into the register. When operating at repetition rates lower than 4.5MHz, a 9th bit can be obtained by toggling a flip-flop in the pixel. The LSB size is about 3.125mV for 8 bits and about 1.56mV when 9 bits are desired.

The analog-to-digital converter exploits the fact that X-rays are perfectly monochromatic. By knowing the energy of incoming photons it is possible to set the ADC bins in the low part of the dynamic range to match the single X-ray photon. This condition can be obtained by properly setting the gain of the system: a first adjustment can be made by changing the gain of the front end filter, while fine regulation is achieved regulating the discharge current. The offset can be adjusted by adding a delay in the signal which latches the time stamps.

The one to one correspondence between the number of collected photons and the number of ADC bins holds in the whole linear region of the output characteristic of the DSSC (Figure 3.23).

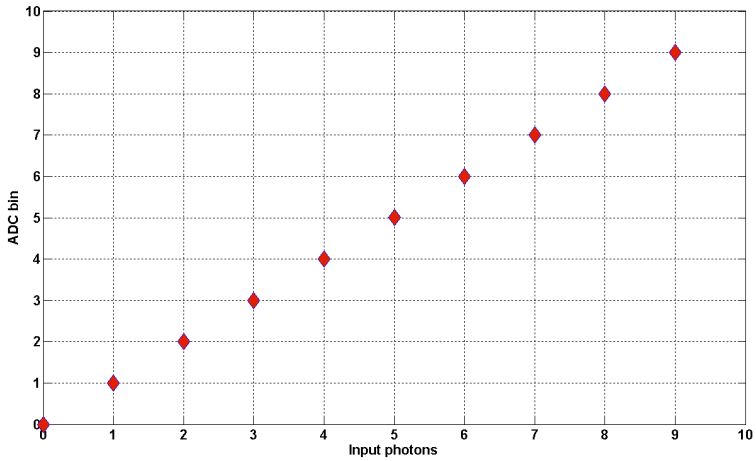

Figure 3.23 *In the linear part of the DSSC characteristic a one-to-one correspondence between input photons and ADC bins is desired. The uncertainty introduced by the Poisson statistics of the incoming photons is negligible with respect to the electronic noise introduced by the front end and the converter.*

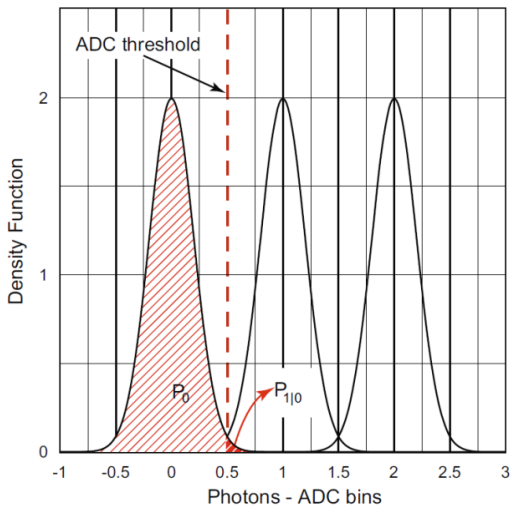

Figure 3.24 *Density function of the electronic noise, that can be considered Gaussian, centered in the various ADC bins. The threshold is placed in the middle of the bins.* $P_{1|0}$ *is the probability that a pixel erroneously detects one photon because of the electronic noise, even if no photon has been collected.*

With the actual detector design it is foreseen that the linear part of the characteristic will cover an energy range equivalent to about 10 to 20 photons at 1keV. In this low energy region no quantization error is present, since the input signal is already discrete. This means that there is no uncertainty in the number of the collected photons given by the ADC. The electronic noise, mainly given by the detector and the analog front end, is the major source of fluctuations that may lead to an incorrect measurement of the photons signal and thus to a wrong bin attribution. To have a sufficiently small probability a noise level of less than 50 electrons is required (Figure 3.24). For a 1keV photon the corresponding probability is less than 0.1%, sufficient for the requirements of the target application [11].

For higher absorbed energies, an increasing number of photons will be converted to the same digital word (Figure 3.25). As a consequence in this part of the dynamic range it is possible to know the number of collected photons only with an intrinsic uncertainty. This would be true even if the system was completely free of electronic noise.

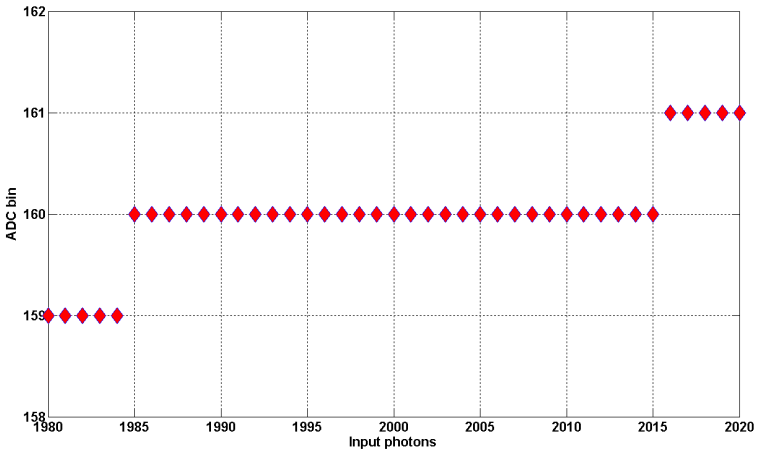

Figure 3.25 *Due to the compressive characteristic of the detector an increasing number of photons is assigned to the same ADC bin for higher absorbed energies.*

The root mean square value of the quantization noise can be evaluated as the number of photons assigned to a single ADC level

divided by $\sqrt{12}$. In other words, the distribution of photons in one bin can be considered, in first approximation, uniform. It follows that for high dynamic range the uncertainty of the ADC becomes higher. However, the system is designed in such a way that the quadratic sum of electronic and quantization noise is negligible with respect to the Poisson generation noise on the whole dynamic range [30]. The 8 bit resolution is sufficient for this purpose, and this is true even though the electronic noise contribution gets more relevant in the high part of the dynamic range because of the reduced detector gain.

The ADC resolution has a direct impact on the achievable dynamic range of the system. This parameter depends on the shape of the DSSC characteristic and on the number of ADC bits, once the first input photon is assigned to the first bin of the converter. This topic is analyzed in details in section 4.6.

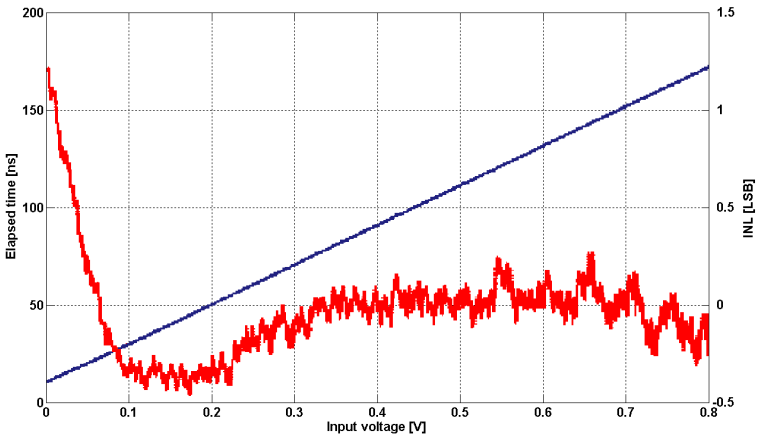

Figure 3.26 *Time interval between conversion start and GCC latching (blue) and INL (red) versus input voltage.*

Experimental data of the voltage to time transfer function are shown in Figure 3.26 for the first ADC chip production [31]. The system was operated at full speed, and the integral non linearity is also sketched. The characteristic is relative to one of the two sample and hold capacitors, and its slope amounts to 203ns/V, very close to the nominal design value of 5MV/s. The gain for the second sample and hold

capacitor was measured to be 201.7ns/V. Measurements on the developed ADC chips demonstrate the achievement of a signal-to-noise ratio of 67 dB, a mean DNL of less than 0.3 LSB, and an INL below 0.5 LSB for the 5MHz sampling rate.

Several chip prototypes comprising an 8-by-8 ADC matrix representing a single 64-pixel column of the final matrix have been fabricated. The area and power dissipation of the ADC pixel circuitry amounts to 0.0139mm^2 and 634µW, respectively. The global blocks require an area of 0.0143mm^2, and consume a mean power of 3.07mW.

3.6 The in-pixel memory

Since it is not feasible to send the complete image out from the ASIC in only 220ns, digital data is stored locally within the pixels before it is read out in between of the XFEL bunch trains. In order to accumulate a maximum number of events during the XFEL bunch trains, a compact digital memory solution is required. For this reason, two approaches have been studied: a static version uses the dense SRAM cell layout provided by IBM with an area of 2.04µm^2 per bit and a dynamic version based on a three pMOS transistors dual ported cell [32]. Test chips for both versions have been submitted and tested.

Figure 3.27 *Schematic (left) and layout (right) of a cell of the dynamic memory designed in a first phase of the DSSC project.*

The dynamic memory is based on a custom 3T dynamic storage cell. The layout of the cell is four sides abuttable and can be made very compact as it only uses one type of transistor. PMOS transistors are used

because they project better radiation hardness and lower leakage. The single cell occupies an area of 1.64x0.84μm^2 (Figure 3.27).

The operating conditions of a DRAM for the chip would require a retention time of more than 20μs, which is only feasible with an extra supply voltage. Discharge of the stored level is mainly through the closed switch M_1 and its reversely biased drain diode. It has been measured that without extra voltages, 13% of all cells are erroneous at a refresh rate of 20μs. Figure 3.28 shows the measured retention times of three different cell types for a nominal supply voltage of 1.2V and for different off voltages at the M_1 gate. It can be seen how an increase of 100mV in this turn off voltage improves retention time by more than an order of magnitude, following an exponential relationship that demonstrates how data loss is due to leakage. The red curve in Figure 3.28 shows one of the very few cells where the effect saturates at a certain voltage. At this state, the diode leakage through the drain of M_1 becomes dominant, which cannot be influenced by external voltages.

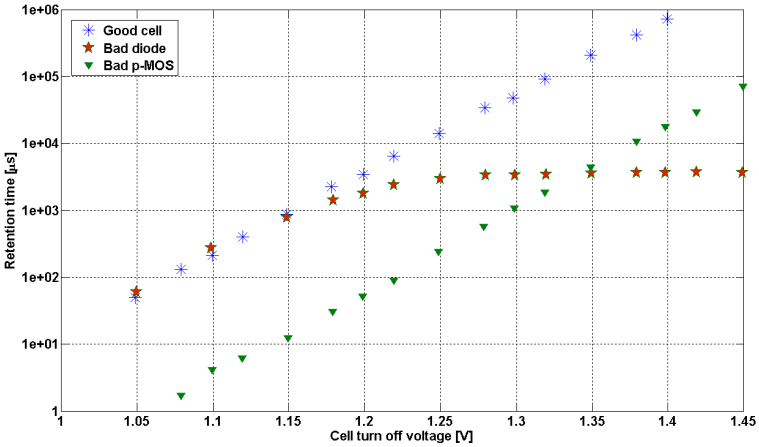

Figure 3.28 *Retention time as a function of the turn off voltage for a supply voltage of 1.2V.*

The static solution uses a classical 6T SRAM cell. The pixel memories are organized in 9 blocks as shown in Figure 3.29, each of them storing one bit position of each digital word. The column selection is implemented with a two stage nMOS pass gate multiplexer. This

arrangement yields a perfect usage of area and wiring because transistors can be abutted efficiently and the differential data busses and intermediate nodes are very short.

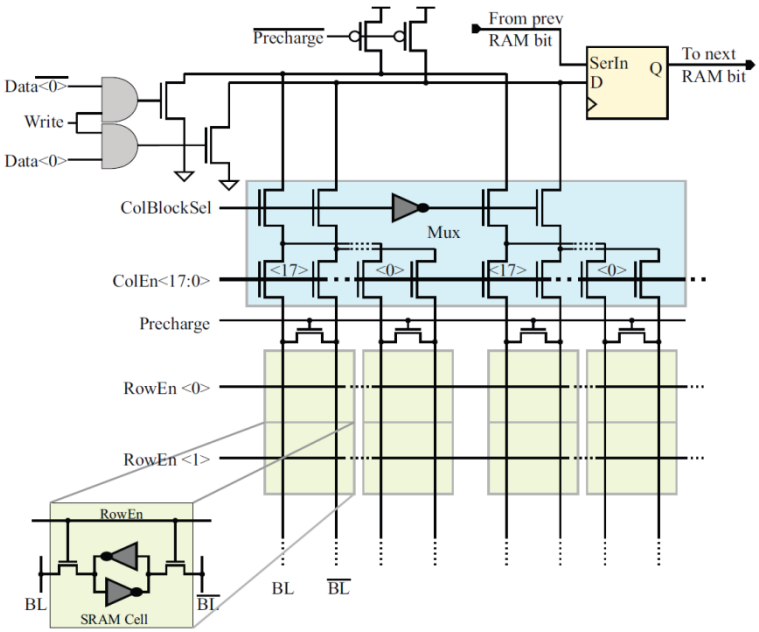

Figure 3.29 *Architecture of a SRAM block storing a single bit of each word. This circuit is replicated nine times to store the full words.*

Reading is done by simply connecting a selected cell to their bit lines. Because access times of more than 200ns are required, no sense amplifier is needed and it suffices to evaluate one of the bit lines with simple CMOS logic. In order to avoid corrupting the stored data when the cell is connected, the bit lines have to be pre-charged before.

Writing of a cell is done by forcing the cross coupled inverters to one of the two stable states. This is done by pre-charging both bit lines to VDD and then driving one of the bit lines to GND before connecting the selected cell to the bit lines. Enabling a row always connects all cells of that row to their respective bit lines. In order to prevent corrupting the stored data, all bit lines have to be pre-charged before a new row is selected.

To test the radiation tolerance of this solution, one DRAM and one SRAM chips have been irradiated up to a dose of 5Mrad from an X-ray tube, without showing bit errors.

The sensitivity of the dynamic version to transistor leakage and the additional power needed for refresh led to the decision to use the SRAM with a small penalty in density. The memory currently has a size of 640 9bit words and occupies about one third of the pixel area. There is still some room to increase the size to 720. The periphery overhead within the pixel is only 15%.

3.7 Bibliography

[1] J. Kemmer, G. Lutz, “New semiconductor detector concepts”, Nucl. Inst. Meth. A, 253 (1987) 356-377.

[2] E. Gatti, P. Rehak, “Semiconductor drift chambers: an application of a novel charge transport scheme”, Nucl. Inst. Meth. A, 225 (1984) 608-621.

[3] M. Porro et al., “Spectroscopic Performance of the DEPFET detector/amplifier device with respect to different filtering techniques and operating conditions”, IEEE Trans. Nucl. Sci., vol. 53, no. 1, 401, Feb. 2006.

[4] J. Treis et al., “DEPFET based focal plane instrumentation for X-ray imaging spectroscopy in space”, 2007 IEEE Nuclear Science Symposium Conference Record, pp. 2226-2235.

[5] G. Lutz et al., “DEPFET detector-amplifier structure: properties, achievements and new developments, concepts and applications”, 2007 IEEE Nuclear Science Symposium Conference Record, pp. 988-994.

[6] M. Porro, “New Solid State Systems for X and Gamma Ray Imaging and Spectroscopy”, Doctoral Dissertation, Politecnico Di Milano, 2005.

[7] J. Treis et al., “DEPMOSFET Active Pixel Sensor Prototypes for the XEUS Wide Field Imager”, IEEE Trans. Nucl. Sci., vol. 52, no. 4, pp. 1083-1091, Aug. 2005.

[8] P. Klein, “Entwicklung, Bau und Test eines Halbleiter-Bildzellendetektors f¨ur den Einsatz in der Teilchenphysik”, Doctoral Dissertation, University of Munich, 1995.

[9] J. Treis et al., “First results of DEPFET based active pixel sensor prototypes for the XEUS wide field imager”, Proceedings of SPIE, High Energy Detectors in Astronomy, 5501:89-100, 2004.

[10] G. Lutz, P. Lechner, M. Porro, L. Strüder, G. De Vita, “DEPFET sensor with intrinsic signal compression developed for use at the XFEL free electron laser radiation source”, Nucl. Inst. Meth. A, 624 (2010) 528-532.

[11] M. Porro et al., “Expected performance of the DEPFET sensor with signal compression: A large format X-ray imager with mega-frame readout capability for the European XFEL”, Nucl. Inst. Meth. A, 624 (2010) 509-519.

[12] P. Lechner, L. Andricek, S. Aschauer, A. Bahr, G. De Vita, K.

Hermenau, T. Hildebrand, G. Lutz, P. Majewski, M. Porro, R. Richter, C. Sandow, G. Schaller, H. Soltau, L. Strüder, "DEPFET active pixel sensor with non-linear amplification", 2011 IEEE Nuclear Science Symposium Conference Record, pp. 563-568.

[13] R. Kohrs, L. Andricek, P. Fischer, M. Harter, M. Karagounis, H. Kruger, G. Lutz, H. Moser, I. Peric, M. Porro, L. Reuen, R. Richter, C. Sandow, L. Strüder, M. Trimpl, N. Wermes, "Development of a prototype module for a DEPFET pixel vertex detector for a linear collider," IEEE Trans. Nucl. Sci., vol. 52, no. 4, pp. 1171 – 1175, Aug. 2005.

[14] P. Fischer, M. Bach, F. Erdinger, S. Facchinetti, C. Fiorini. K. Hansen, P. Kalavakuru, M. Manghisoni, M. Porro, C. Reckleben, G. De Vita, "Pixel Readout ASIC with per Pixel Digitization and Digital Storage for the DSSC Detector at XFEL", 2010 IEEE Nuclear Science Symposium Conference Record, pp. 336-341.

[15] E. Gatti, M. Sampietro, P. F. Manfredi, "Optimum filters for detector charge measurements in presence of 1/f noise", Nucl. Inst. Meth. A, 287 (1990) 513-520.

[16] E. Gatti et al., "Suboptimal filtering of 1/f noise in detector charge measurements", Nucl. Inst. Meth. A, 297 (1990) 467-478.

[17] M. Porro, C. Fiorini, L. Strüder, Nucl. Inst. Meth. A, 512 (2003) 513.

[18] L. Bombelli et al., IEEE Trans. Nucl. Sci., vol. 54 (2007) 1359.

[19] M. Porro et al., IEEE Nuclear Science Symposium Conference Record (2007) 2392.

[20] W. Buttler, G. Lutz, V. Liberali, F. Maloberti, P. F. Manfredi, V. Re, V. Speziali, "Evolution in the criteria that underline the design of a monolithic preamplifier system for microstrip detectors", Nucl. Inst. Meth. A, 288 (1997) 140-149.

[21] M. Porro, G. De Vita, S. Herrmann, T. Lauf, J. Treis, A. Wassatsch, L. Bombelli, C. Fiorini, "ASTEROID: A 64 channel ASIC for source follower readout of DEPFET arrays for X-ray astronomy", Nucl. Inst. Meth. A, 617 (2010) 351-357.

[22] M. Porro et al., "Spectroscopic Performance of the DePMOS Detector/Amplifier Device With Respect to Different Filtering Techniques and Operating Conditions", IEEE Trans. Nucl. Sci., vol. 53, no. 1, pp. 401-408, Feb. 2006.

[23] G. De Vita, M. Porro, S. Herrmann, A. Wassatsch, L. Bombelli,

S. Facchinetti, C. Fiorini, F. Erdinger, "A 5MHz Low-Noise 130nm CMOS Analog Front-End Electronics for the Readout of Non-Linear DEPFET Sensor with Signal Compression for the European XFEL", 2010 IEEE Nuclear Science Symposium Conference Record, pp. 139-144.

[24] P. Fischer, W. Neeser, M. Trimpl, J. Ulrici, N. Wermes, "Readout concepts for DEPFET pixel arrays", Nucl. Inst. Meth. A, 512 (2003) 318-325.

[25] L. Bombelli, C. Fiorini, M. Porro, S. Herrmann, S. Wölfel, "VELA: the CMOS circuit based on fast current read-out for X-ray spectroscopy with DePMOS", IEEE Trans. Nucl. Sci., vol. 54, Issue 4, 1359, Aug. 2007.

[26] M. Trimpl, "Design of a current based readout chip and development of a DEPFET pixel prototype system for the ILC vertex detector", Doctoral Dissertation, University of Bonn, 2005.

[27] E. Fretwurst, F. Januschek, R. Klanner, H. Perrey, Pintilie, F. Renn, "Study of the radiation hardness of silicon sensors for the XFEL", 2008 IEEE Nuclear Science Symposium Conference Record, N30-400, pp. 2535–2538.

[28] C. C. Enz, G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization", Proceeding of the IEEE, Volume 84, Issue 11, pp. 1584-1614, Nov. 1996

[29] K. Hansen, C. Reckleben, I. Diehl, M. Bach, P. Kalavakuru, "Pixel level 8-bit 5-MS/s Wilkinson type digitizer for the DSSC X-ray imager: concept study", Nucl. Instr. Meth. A, vol. 629, pp. 269-276, Feb. 2011.

[30] M. Porro, L. Andricek, A. Castoldi, Carlo Fiorini, P. Fischer, H. Graafsma, K. Hansen, A. Kugel, G. Lutz, U. Pietsch, V. Re, L. Strüder, "Large format X-ray imager with mega-frame readout capability for XFEL, based on the DEPFET Active Pixel Sensor", 2008 IEEE Nuclear Science Symposium Conference Record, N14-7, 1578, Oct. 2008.

[31] C. Reckleben, K. Hansen, P. Kalavakuru, I. Diehl, "Pixel level 8-bit 5-MS/s per-pixel ADC in an 8-by-8 matrix", 2011 IEEE Nuclear Science Symposium Conference Record, pp. 668-672.

[32] F. Erdinger, P. Fischer, "Compact digital memory blocks for the DSSC pixel readout ASIC", 2010 IEEE Nuclear Science Symposium Conference Record, pp. 1364-1367.

CHAPTER 4

The Flip Capacitor Filter

4.1 Review of a current read out circuit

In Chapter 3 the current read out mode is introduced underlying its main benefits. As an example the VELA (VLSI ELectronics for Astronomy) analog front end is briefly presented next [1]-[2]. The ASIC has been developed to comply with the requirements of space missions such as IXO (International X-ray Observatory), XEUS (X-ray Evolving Universe Spectroscopy) [3] and SIMBOL-X [4]. In particular, low noise and a processing time on the order of some micro seconds are common requirements to all these projects.

VELA is a 64 channels ASIC designed to read out a spectroscopic-type DEPFET matrix by processing one row at a time, while the others are turned off (Figure 4.1). Each row collects the signal when it is off while the electronics reads another row of the matrix. In fact, DEPFETs are able to collect and store charge into the internal gate even though the external FET structure is not active, thus providing on-demand read out capability.

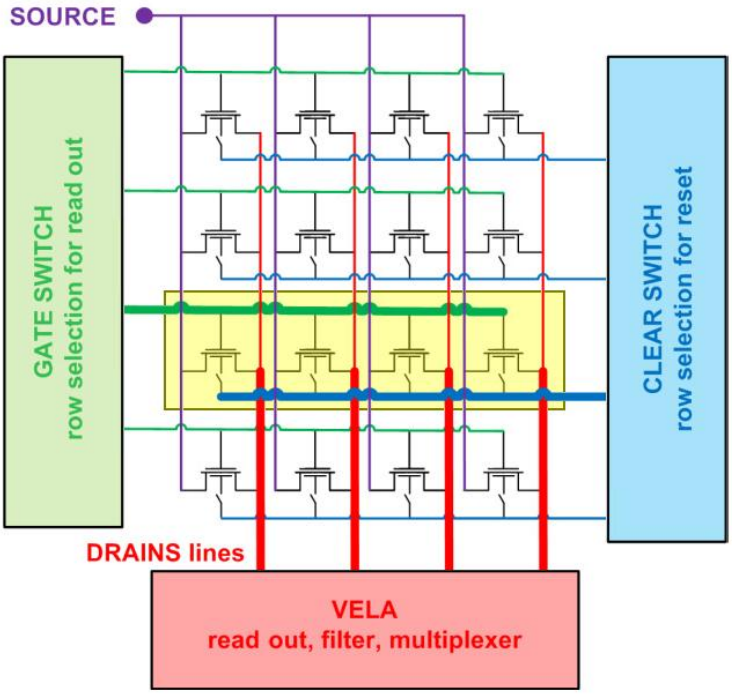

Figure 4.1 *Block scheme for the operation of a DEPFET matrix in conjunction with the VELA ASIC. The Gate Switch and Clear Switch blocks represent dedicated circuitry designed to operate the detectors.*

In such a matrix arrangement all drain and source nodes of the detectors in a column are shorted together. Only one DEPFET per column at a time is turned on to read out the signal. For a mega pixel imager with a typical detector size of 75μmx75μm the drain lines have a length of about 8cm. The stray capacitance associated with the node is thus very high, in the order of 30pF to 40pF. Considering the results

presented in Chapter 3 a corresponding rise time for the source follower approach of more than 1μs is obtained. VELA has been developed to overcome the noise limitations due to this long settling time and implement an almost ideal trapezoidal weighting function. This result is obtained thanks to the Switched Current Technique, SCT [5]. The channel block diagram of a single analog channel is sketched in Figure 4.2.

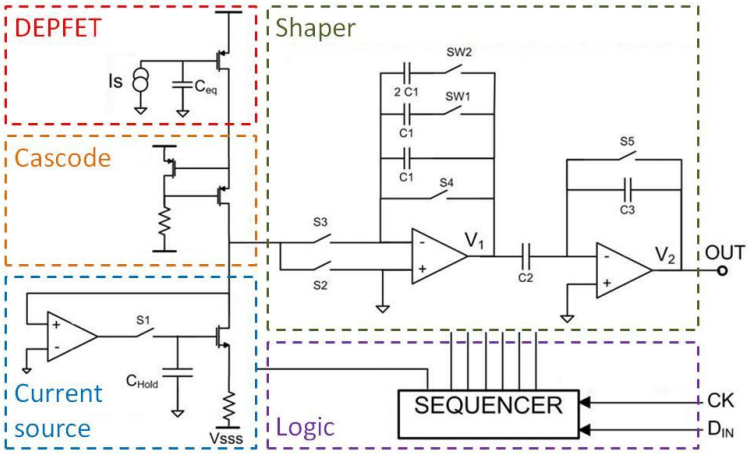

Figure 4.2 *Simplified schematic of the VELA read out channel.*

Each channel comprises an input cascode stage connected to the drain of the DEPFETs, a programmable current generator and a time variant filter that implements the desired trapezoidal weighting function, thus recalling the basic scheme described in the previous Chapter. The ASIC is realized using the 0.35μm 3.3V CMOS technology from Austrian Micro Systems. Power consumption is about 4mW per channel.

The input cascode is studied to stabilize the drain voltage of the DEPFET detector. A simple cascode stage, realized with only one transistor, would not be effective due to the relatively small transconductance of the devices in the adopted technology. A local reaction that lowers the node impedance is thus implemented to move at high frequencies the pole associated to the drain nodes of all detectors in a column. The trapezoidal weighting function is realized using two

stages. The first one is an integrating stage, with different programmable gains, while the latter is used to store the value of the first measurement that has to be subtracted from the second one. This operation is achieved by properly operating the switches, thus implementing the SCT. An on-chip sequencer is used to generate the digital signals, and the final output value is the difference of the voltages at the end of the two integrations. The read out speed can be adjusted to cope with different experiments and can be as short as 1μs per matrix line. The current generator is necessary to subtract the bias current of the DEPFETs and process only the current signal. In this way it is possible to maximize the gain of the first stage in the front end. The current source must be programmable to match the current delivered by the different detectors among which the ASIC input is switched. Thus, a programming phase is needed before every DEPFET read out. This phase determines the voltage on the capacitor C_{hold} by means of a local feedback loop that is then removed when the filter is processing the signal. Neither the sampled current noise nor the kTC contribution influence the final measurement, since they act as a constant parameter n_0 that does not change between the two correlated measurements performed by the filter and is therefore removed (see also section 3.4.2).

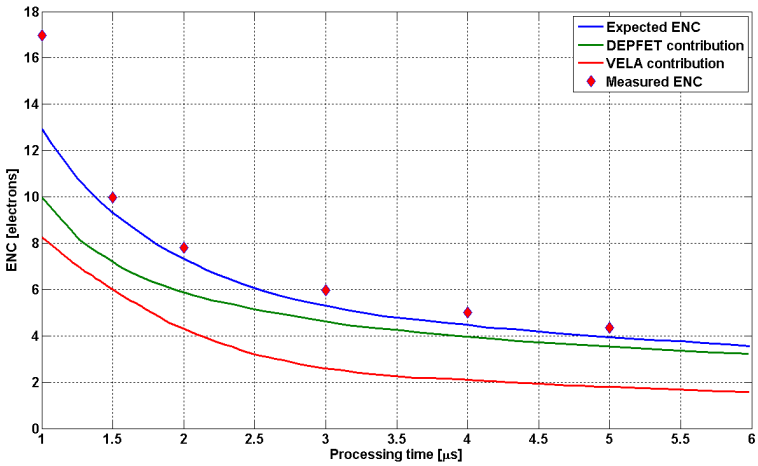

Figure 4.3 *Comparison between the different noise contributions and the measured noise for the VELA read out ASIC. The processing time is defined as the time required to read out a line of the detector matrix.*

Noise performances of VELA are shown in Figure 4.3. The detectors were biased with a current of about 180µA. Obtained results show very good noise performances with processing times down to 1µs.

4.2 Preliminary studies for XFEL

Even though the same principles of the VELA front end could be used, the DSSC project required the development of a new circuit to cope with the very demanding aspects of the European XFEL. For instance, a very fast filter is needed to implement the desired trapezoidal weighting function in only 220ns. Moreover, as every read out channel has to match the size of a single DSSC pixel, also area becomes a primary issue, and considering the huge number of channels power consumption has to be minimized as much as possible. For all of these reasons, the VELA architecture is not feasible for the European XFEL and other solutions had to be developed.

Preliminary studies on a possible architecture for the DSSC project have been presented in [6] and [7]. The circuit is based on the same topology of VELA and was designed in IBM technology (Figure 4.4).

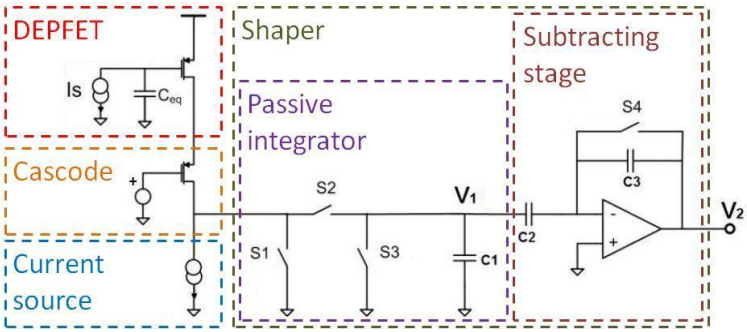

Figure 4.4 *Schematic of the first analog front end architecture proposed for the DSSC read out ASIC.*

Thanks to the high transconductance of the devices in this technology the input cascode can be realized as a simple transistor, thus removing the power consumption associated with the local loop branch present in VELA channel. Typical values for the transconductance are in the order of some hundreds of μS. Moreover, since a single detector is associated with the read out channel the stray capacitance is reduced with respect to DEPFET matrices that are scanned line by line. The expected value for the stray capacitance at the drain is in the order of 0.5pF to 1pF.

The filtering stage employs the SCT and it is still based on an integrator followed by a subtracting stage. To reduce power consumption a single amplifying stage was employed in the shaper. A passive integrator based on capacitor C_1 was foreseen to avoid the need to bias an active integrator stage at relatively high currents to comply with the high signal current arriving from the DSSC. The following active stage can be biased at low currents if capacitors C_2 and C_3 are chosen sufficiently small. In these preliminary studies, the two capacitors were set to be both equal to 0.6pF to minimize the noise contribution of the amplifier [7].

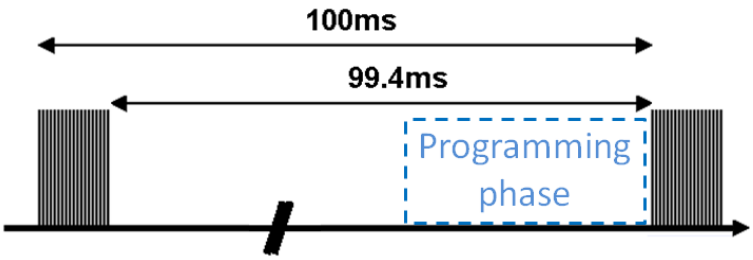

Figure 4.5 *Timing diagram of the European XFEL macro bunch structure. The programming phase of the front end current generator can be done before X-ray pulses start to be delivered.*

As it is done also in VELA, a programmable current generator was introduced to subtract the detector bias current. Since every channel will read out always the same DSSC pixel the current source can be programmed only once before a macro bunch starts to arrive, and not between subsequent pulses (Figure 4.5). In this way it is not necessary to use part of the 220ns and the programming can be very slow since the

time interval between macro bunches is extremely long. Having a small bandwidth programming loop is beneficial from the noise point of view.

Figure 4.6 shows simulated waveforms for two consecutive pulses corresponding to a signal of 10^4 photons of 6keV each. On the left side the voltage V_1 on the integrator is shown while on the right side the output V_2 of the filter is reported (see Figure 4.4). Even though a 770mV voltage swing is present at the output of the integrator, in agreement with the simulated signal and the value of capacitance C_1, the voltage V_2 shows a smaller voltage swing. This effect is due to the very low gain of the amplifier, which was in the order of 40 since the single stage architecture was used to have a current consumption of only 100µA.

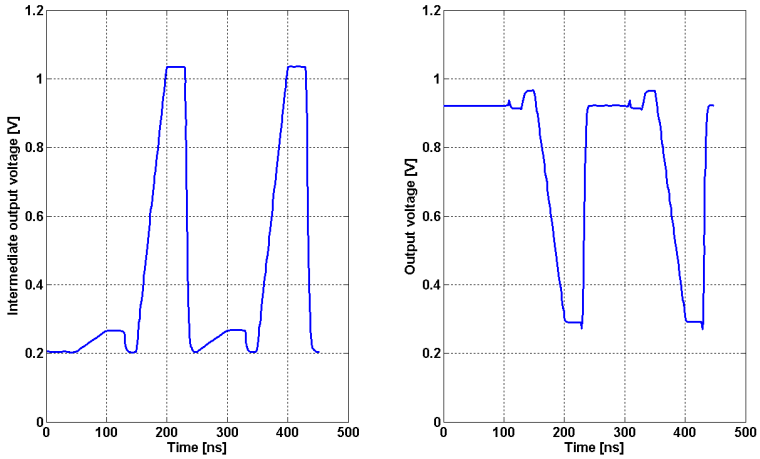

Figure 4.6 *Simulated waveforms of the current read out circuit for a simulated signal corresponding to 10^4 photons of 6keV each. Left, output voltage of the integrator. Right, output voltage of the subtracting stage.*

The main problem of this architecture is that the voltage at node V_1 changes with the signal that is accumulated onto the integrating capacitor, as it is not a virtual ground. Since the gain of the following stage is one and the input range of the following ADC is about 800mV, this node would need to swing by the same amount on a voltage supply of 1.2V. Such a condition would complicate the design of the programmable current generator, as the voltage at its terminals would not be constant.

4.3 The Flip Capacitor Filter

Starting from VELA and these preliminary studies the design and realization of a new filter architecture implementing the current read out approach has been carried out [8]-[9]. A first ASIC prototype with only the analog front end has been realized and fully characterized to prove the adequacy of adopted solutions. The filter has also been integrated in the 8x8 matrices MM1 and MM2 along with all other DSSC channel blocks.

To reduce as much as possible power consumption and area occupation a single operational amplifier is used to realize both functionalities of integrating and subtracting stage. The proposed solution is shown in Figure 4.7.

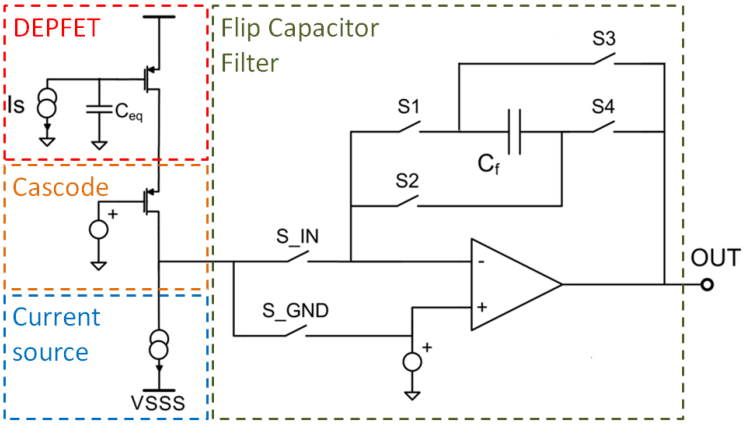

Figure 4.7 *Architecture of the Flip Capacitor Filter solution for the DSSC project.*

The circuit realizes a trapezoidal weighting function by flipping the feedback capacitor in between the two integrations. For this reason the circuit is called Flip Capacitor Filter (FCF). In addition, the same amplifier is used to program the current source that subtracts the bias current drawn by the detector. All building blocks of VELA and of the preliminary architecture can still be identified. However, it can be noticed

that in this solution a virtual ground is present at the drain of the input cascode, thus removing the issues connected to the use of a passive integrator.

The reference timing scheme, composed by four different phases, is the one described in section 3.4.2 and shown again here for simplicity (Figure 4.8). The filter uses two correlated measurements to reduce the flicker noise, one measurement of the drain current before the signal arrival (baseline read out) and one afterward (signal and baseline read out).

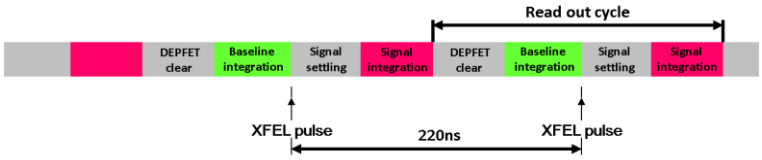

Figure 4.8 *Sketch of the timing scheme for the FCF, in which two correlated measurements are foreseen.*

A read out cycle starts with the clear of the detector and the concurrent reset of the front end electronics. The latter is obtained by shorting the feedback capacitance C_f thanks to the simultaneous closure of all switches S_1 to S_4. The current source subtracts the bias contribution of the detector. Any residual baseline that might arrive from the input branch flows towards the reference voltage through the switch S_{GND}, while the switch S_{IN} is open.

At the end of this initial phase the IG of the DSSC is completely empty and only the bias current flows in the input branch. By changing the state of the two input switches S_{IN} and S_{GND} the baseline current is integrated on the feedback capacitor, with switches S_1 and S_4 closed and switches S_2 and S_3 left open. The charge that accumulates on the capacitor and the corresponding output voltage variation can be expressed as follow:

$$Q_{baseline} = I_{baseline}\tau$$

$$\Delta V_{out,1} = \frac{Q_{baseline}}{C_f} = \frac{I_{baseline}}{C_f}\tau$$

where τ is the integration time. The circuit situation after this first integration is shown in Figure 4.9.

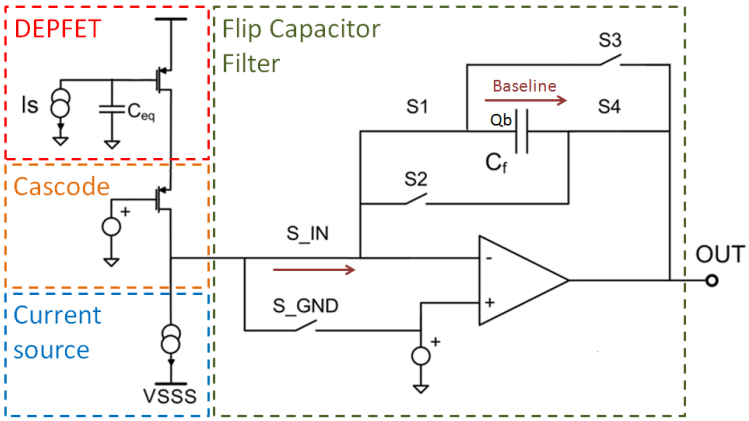

Figure 4.9 *Configuration of the FCF during the first integration phase. The baseline can be due both to 1/f noise and to a mismatch between the current source and the bias contribution of the detector.*

In the following phase an X-ray pulse will be delivered and scattered photons will be collected by the DSSC detectors. To maintain unchanged the value corresponding to the baseline integration, the two input switches are commuted again. In the meanwhile, switches S_1 and S_4 are opened, while switches S_2 and S_3 are closed, which results in a flipping of the feedback capacitor (Figure 4.10). Ideally, the stored charge does not change and therefore at the end of this phase the output voltage has an opposite polarity around the reference level with respect to the previous situation:

$$\Delta V_{out,2} = -\Delta V_{out,1} = -\frac{I_{baseline}}{C_f}\tau$$

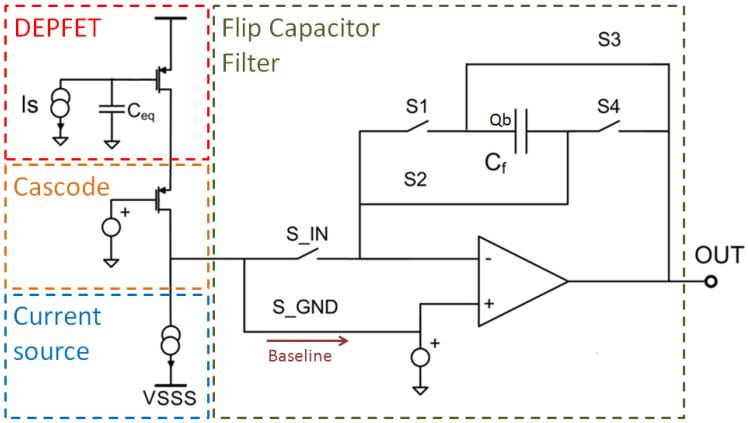

Figure 4.10 *Configuration of the FCF right after the feedback switches have changed their state to enter the flip phase, in which X-ray photons can hit the detector.*

In the last phase the signal integration is carried out. By switching again S_{IN} and S_{GND} the current is sent towards the feedback capacitor (Figure 4.11). Both the baseline and the signal contribution are integrated, and therefore the total charge that is deposited on the capacitor plates is:

$$Q_{baseline\,\&\,signal} = (I_{baseline} + I_{signal})\tau$$

Considering the initial condition given by the first integration the charge that is present at the end of the read out cycle can be expressed as follows:

$$Q_f = Q_{baseline\,\&\,signal} - Q_{baseline} = I_{signal}\tau$$

Only the charge corresponding to the signal is left onto the capacitor plates, while the baseline contribution is cancelled by the filter operation. The final output voltage is related only to the charge collected in the DSSC and can be written as:

$$\Delta V_f = \frac{Q_f}{C_f} = \frac{I_{signal}}{C_f}\tau$$

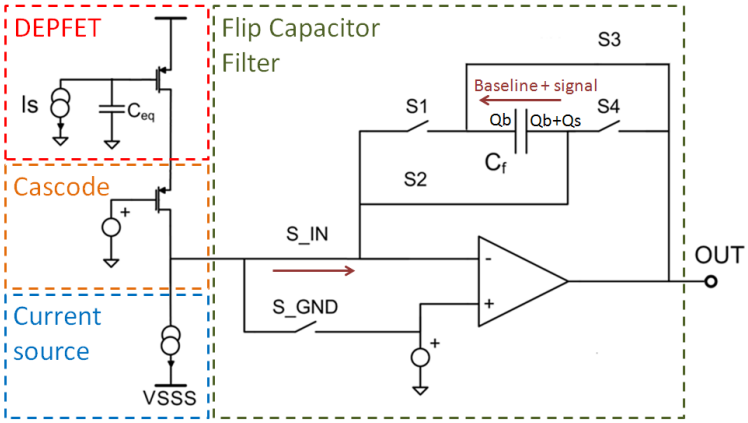

Figure 4.11 *Configuration of the FCF during the second integration. The charge is deposited on the other plate of the feedback capacitor with respect to the first integration, thus cancelling out the baseline component.*

Four feedback capacitors are available to set the gain and cope with different photon energies. In Figure 4.12 simulated waveforms of the output voltage for different values of the baseline are represented, showing that the filter output returns to the same value when no signal is applied. The final spread in the output voltage is considerably lower than the ADC bin size of about 3.125mV. A typical output waveform in presence of a signal is shown in Figure 4.13.

For what concerns the noise, the result obtained in section 3.4.2 is valid and is here reported for convenience:

$$\Delta V_f = \frac{I_{signal}}{C_f}\tau - \int_o^{\tau}[n(t) - n_g(t)]\partial t + \int_{t_1}^{t_1+\tau}[n(t) - n_g(t)]\partial t$$

where $n(t)$ and $n_g(t)$ are the detector and current generator noise components that are filtered by the analog front end, τ is the integration time and t_1 is the time at which the second integration starts.

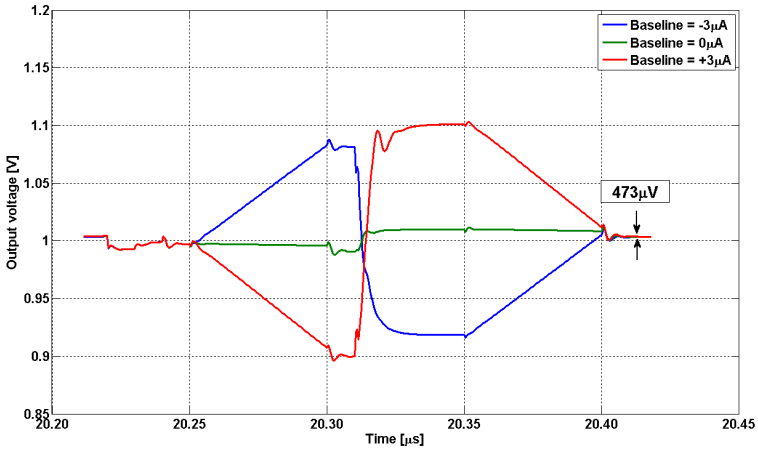

Figure 4.12 *Simulated waveforms of the output of the FCF for three different values of the baseline. The integrations last for 50ns, from 20.25μs to 20.30μs and from 20.35μs to 20.40μs. The flip phase takes place in between. The reference voltage of the operational amplifier is set to 1V.*

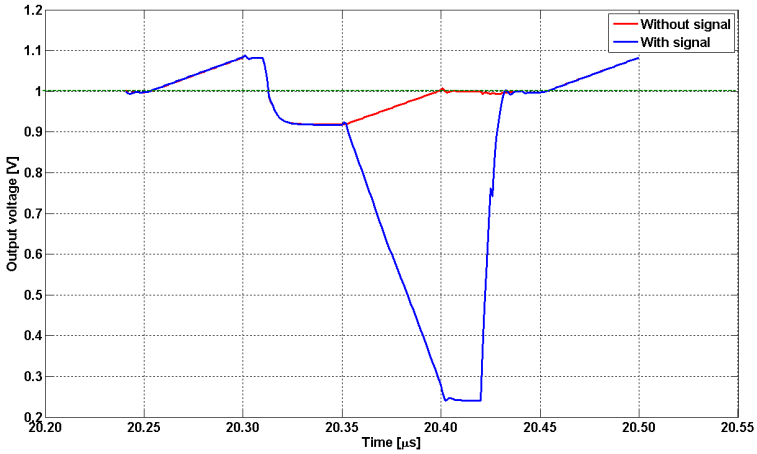

Figure 4.13 *Simulated waveforms of the output of the FCF with and without signal. The timing and the reference voltage are the same of Figure 4.12. The reset phase is also shown, starting at 20.42μs.*

In Figure 4.14 the transitions of the switches in the four phases is sketched.

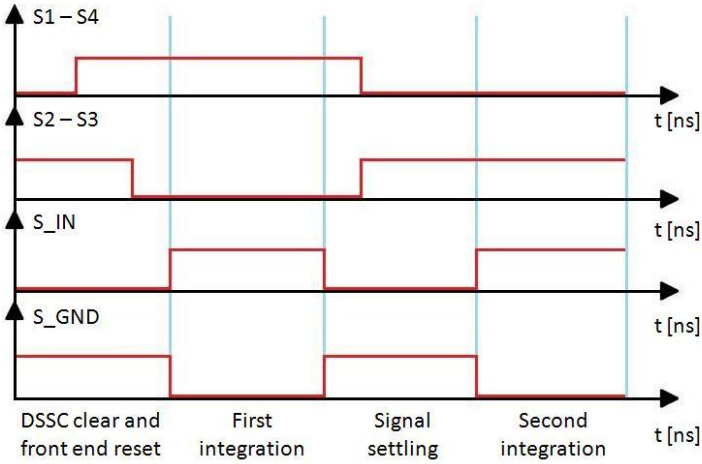

Figure 4.14 *Timing diagram of the switches transitions during a complete FCF read out cycle. The flipping of the capacitor takes place during the "Signal settling" interval.*

4.4 The flip phase

The stray capacitances and the charge injections make the flip phase very delicate. In particular, the stray capacitance that is initially connected to the output node injects a certain amount of charge after the flipping phase. This charge flows through the feedback capacitor, leading to an error in the baseline subtraction.

To briefly clarify this point, let's consider the circuit in Figure 4.15, where the parasitic components associated with C_f are sketched. C_t and C_b are respectively the top and bottom stray capacitances. During the baseline integration ideally no charge flows onto the C_b that is connected to the virtual ground. On the other hand, the output voltage varies by a quantity proportional to the baseline current. The charge that is left on the stray capacitance can be written as:

$$Q_{Ct} = (V_{ref} - \Delta V_{out,1})C_t = \left(V_{ref} - \frac{I_{baseline}}{C_f}\tau\right)C_t$$

where V_{ref} is the reference voltage at the non-inverting input of the amplifier. With the flipping phase the position of C_t and C_b with respect to the main amplifier is switched. Since the virtual ground is at a different potential from the reference voltage, the operational amplifier delivers a current to cancel this difference. This current flows through the feedback capacitor, thus altering the stored value of the baseline.

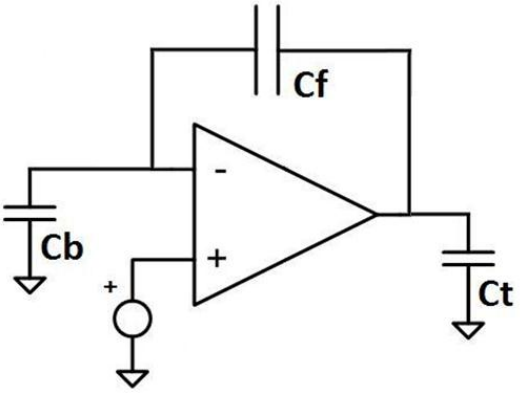

Figure 4.15 *Sketch of the FCF main amplifier along with the parasitic components associated with the feedback capacitor during the first integration.*

Since the charge stored onto the top plate stray capacitance is:

$$Q_{Ct} = \Delta V_{out,1}C_t = \frac{I_{baseline}}{C_f}\tau C_t$$

then the final voltage across the feedback capacitor, considering also the baseline contribution, can be expressed as follows:

$$\Delta V_{Cf} = \frac{Q_{baseline} + Q_{Ct}}{C_f} = (C_f + C_t)\frac{I_{baseline}}{C_f^2}\tau$$

This variation depends on the baseline, which is unknown. For what concerns C_b, the current needed to charge it to the final value is

directly provided by the low impedance of the output of the amplifier and thus does not influence the measurement.

It is important to notice that the effect of C_t is always to increase the charge stored onto the feedback capacitor, regardless of the direction of the baseline current. Therefore, to solve this issue an additional capacitor is included that during the first integration subtracts the same charge that is injected after the flip phase.

From the circuit point of view this result can be achieved by connecting the new capacitor as shown in Figure 4.16. Since during the first integration only the switches S_1 and S_4 are closed, the C_{add} is effectively connected in parallel to C_f. Thus, the charge that is stored onto the feedback capacitor is reduced by a quantity:

$$\Delta Q_{Cf} = I_{baseline}\tau - \frac{C_f}{C_f + C_{add}} I_{baseline}\tau = \frac{C_{add}}{C_f + C_{add}} I_{baseline}\tau$$

The corresponding output voltage, and thus the voltage on C_t, is also modified by the additional capacitor and settles to the following value:

$$V_{Ct} = V_{ref} - \frac{I_{baseline}}{C_f + C_{add}}\tau$$

After the flipping phase the C_{add} does not play any role, since now only the switches S_2 and S_3 are closed. The spurious charge that is injected is equal to:

$$Q_{Ct} = \frac{C_t}{C_f + C_{add}} I_{baseline}\tau$$

By requiring this contribution to be equal to the reduction in the stored charge it can be found that the additional capacitor must have the same value of the top plate stray capacitance. Simulations demonstrated the effectiveness of this solution in considerably reducing the output voltage spread for different values of the baseline. Anyway, a small value of only 5fF was extracted for the parasitic capacitance. Therefore, in the

first ASIC prototype a filter channel including the additional capacitor and one without it have been implemented to experimentally verify the simulated values.

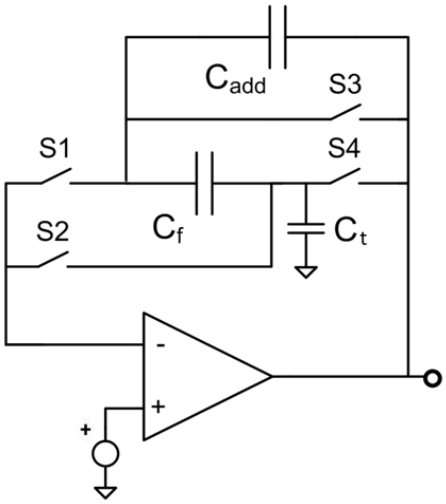

Figure 4.16 *Introduction of a second capacitor in the feedback network to compensate for the spurious charge injected by the top plate parasitic component.*

4.5 The feedback switches

The switches in the feedback path are very delicate since they can both inject charge and cause a charge loss if all closed at the same time during the flipping phase. For what concerns the charge injection, it has to be noticed that the switches S_1 and S_2 have a voltage on the drain and source nodes that does not depend on the signal and is set by the reference voltage of the amplifier. In particular, when S_1 is opened during the flipping phase it injects a charge that is almost the same in every read out cycle. Thus, its charge injection acts as a constant contribution that can be accounted for during calibration. The same conclusion is valid also for S_2. For this reason both switches are implemented as simple p-MOS transistors.

Conversely, switches S_3 and S_4 have voltages on the drain and source nodes that are related to the input signal, since they are connected to the output node of the filter. As a consequence, when S_4 is opened during the flip phase it injects an amount of charge that varies from cycle to cycle. To provide a first order compensation, and also to guarantee a low resistance on the full output voltage range, these two switches are realized as transmission gates, with a p-MOS and an n-MOS connected in parallel. In the last version of the FCF for the complete pixel matrices dummy transistors canceling the charge injection have also been added.

To avoid the possibility of charge loss during the flip phase it is fundamental that the switches commute in a precise order. For instance, if the switches S_1 and S_4 would open when S_2 and S_3 are already closed there would be an interval in which the feedback capacitor is shorted. As a consequence the stored charge would be altered in an unpredictable way, leading to wrong signal estimations.

To guarantee the correct transitions sequence a dedicated logic network has been introduced (Figure 4.17). Two blocks are present for each feedback capacitor, one generating the driving signals for S_1 and S_2 and the other the signals for S_3 and S_4. The pMOS outputs are used to drive the p-type transistors, while the nMOS signals are connected to the n-type devices that are present in S_3 and S_4. Even though S_1 and S_2 are implemented as simple p-MOS switches, the logic network is the same for both couples of switches to maintain the same delay between the edges.

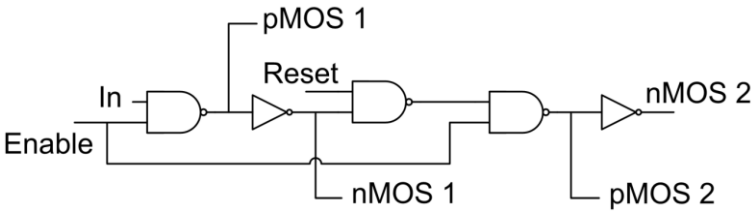

Figure 4.17 *Logic network introduced to determine the correct sequence of transitions for the feedback switches. The outputs are all off when the "Enable" input is low. The "Reset" is used to force the closure of all switches at the same time.*

A single input is used to derive the four gate signals. The delay time introduced by the gates is used to determine the edges order and thus eliminate the possibility of any charge loss. A simulation of the switches transition during the flip phase is shown in Figure 4.18, where the signals relative to the p-type transistors are considered.

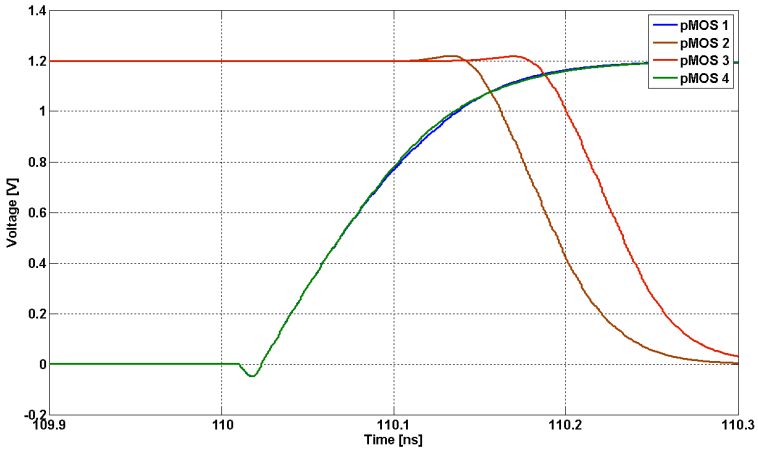

Figure 4.18 *Simulated waveforms of the driving signals for the p-type transistors of the feedback switches. It can be noticed how S_2 and S_3 close after the other two switches are opened.*

By acting on the "Enable" signal, common to the two networks associated with a feedback capacitor, it is possible to set the gain of the filter. In fact, when this signal is high the outputs of the logic network are active and commute as expected. On the contrary, when the "Enable" is low all the switches connected to the network are open and thus the corresponding feedback capacitor is left floating. It is thus possible to determine the number of capacitors connected in feedback by enabling the various logic networks.

The reset signal is used to force all the switches to be closed during the clear phase of the detector (Figure 4.19).

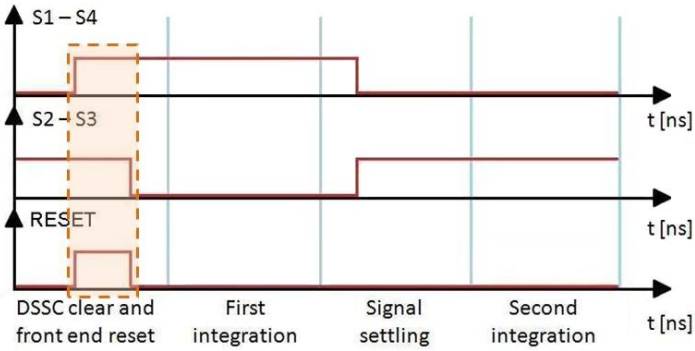

Figure 4.19 *By setting the "Reset" signal of the logic network all the feedback switches are forced to be closed.*

4.6 The operational amplifier dynamic range

As the collected charge in the IG leads to an increase of the detector current it follows that the output of the integrating stage has a corresponding negative swing. To maximize the output dynamic range it is therefore necessary to bias the operational amplifier so that the output is near the positive supply rail. To reserve enough voltage drop for the operational amplifier's current generators and considering the ADC input dynamic range of about 800mV, the output is biased at about 950mV (Figure 4.20). On the other hand, the baseline can flow in both directions and so the output node can also move towards the 1.2V supply. To avoid saturation of the stage a very good programming of the subtraction current source is thus fundamental.

The extremely high dynamic range foreseen for the experiments using the DSSC imager is handled first of all at the detector level. By knowing the shape of the DSSC characteristic, the number of bits of the ADC, the number of bins associated to the signal produced by the first collected photon and the photon energy, the achievable dynamic range, expressed in number of photons, can be evaluated.

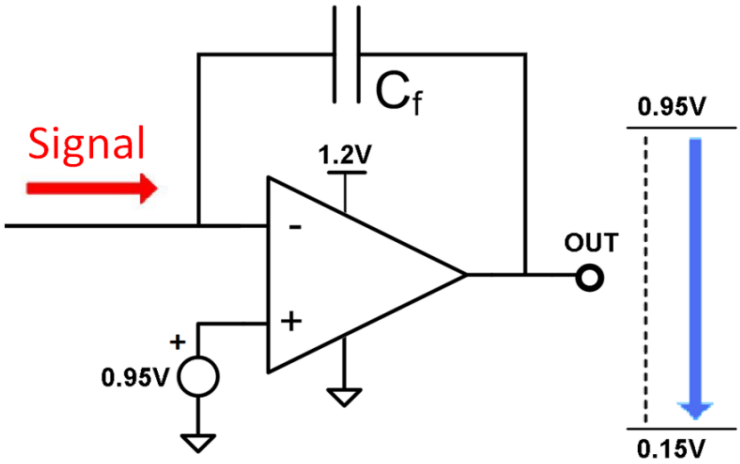

Figure 4.20 *To comply with the polarity of the incoming signal and match the input range of the following ADC the output of the filter is biased near the positive supply rail.*

Once the photon energy is fixed then the signal current corresponding to a single collected photon is known. This defines the bin size of the ADC and by a suitable combination of gain settings in the pixel it is possible to assign one or two bins of the ADC to this signal.

The assigned number of bins to the first photon is chosen such that the quantization noise is always smaller than one half of the Poisson noise. Based on this assumption, it is possible to calculate that for 12keV photons it is necessary to assign 2 bins to the first collected photon for both the 8 and the 9 bit operation modes by increasing the gain of the front end. Lower energies require only one bin per photon to obtain the desired result.

To determine the input signal current I_{LSB} corresponding to one ADC bin the gain of the detector G_q, the energy of synchrotron photons E_γ and the number of ADC bins per photon $N_{bin/\gamma}$ have to be known. In formula:

$$I_{LSB} = \frac{E_\gamma}{3.62eV}\frac{1}{N_{bin/\gamma}}G_q$$

For example, for 500eV photons, an expected gain of 520pA/e$^-$ for the detector and one bin per photon resolution the corresponding current signal is:

$$I_{LSB} = \frac{E_\gamma}{3.62eV}\frac{1}{N_{bin/\gamma}}G_q = 71.32nA$$

Once I_{LSB} is fixed, the achievable dynamic range and the system noise can be obtained. In particular, the bin size multiplied by the number of ADC bins gives the maximum input current that can be processed:

$$I_{max} = I_{LSB}2^N$$

This process is depicted in Figure 4.21, where a simulation of the characteristic of the final DSSC is used.

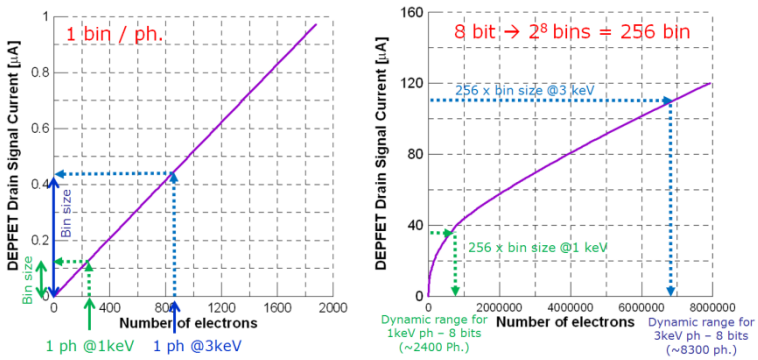

Figure 4.21 *To detect single photons the bin size of the ADC is given by the corresponding output current of the DEPFET. The bin size multiplied by the number of ADC bins gives the maximum signal that can be acquired. The offset is set in such a way that the signal produced by few photons falls in the middle of the bins.*

The achievable dynamic range expressed in number of input photons is presented in Table 4.1 for different operating frequencies. For all energies the first photon is assigned to the first ADC bin, except for the 12keV case where two bins are dedicated to the first incoming photon. Thanks to the introduction of photon energy dependent selectable gains it is possible to obtain a dynamic range of a few thousands photons

also for high energy operation. As can be noticed, the dynamic range increases with the photon energy and with the ADC number of bits. On the contrary, the dynamic range decreases non-linearly as the number of bins attributed to the first photon increases. It is worth to underline that the dynamic range does not depend on the operating speed of the European XFEL machine.

Dynamic range expressed in number of photons					
Ph. Energy [keV]	Frame rate				
	0.9MHz		2.2MHz		4.5MHz
	8 bit	9 bit	8 bit	9 bit	8 bit
0.5	900	4690	900	4690	NA
1	2370	12080	2370	12080	2370
3	8318	23220	8318	23220	8318
6	11539	15600*	11539	15600*	11539
12	5765	8000*	5765	8000*	5765

Table 4.1 *Dynamic range of the system for different photon energies and frame rates. The asterisk means that the corresponding value is limited by the detector's IG charge capacity.*

Dynamic range expressed in number of 1keV photons					
Number of bins attributed to the first photon	Frame rate				
	0.9MHz		2.2MHz		4.5MHz
	8 bit	9 bit	8 bit	9 bit	8 bit
1	2370	12080	2370	12080	2370
2	453	2360	453	2360	NA
3	162	905	162	905	NA

Table 4.2 *Dynamic range of the system for 1keV photons and different frame rates when assigning one or more bins to the first collected photon.*

While assigning one bin to the first photon is mandatory in order to achieve single photon resolution, assigning two bins to the same signal is beneficial in order to decrease the quantization noise even if this reduces the available dynamic range. As an example, the dynamic range for 1keV photons and for different numbers of bins attributed to the first

photon is shown in Table 4.2. Gain settings can be switched during experiments to meet the best performances in terms of noise and dynamic range.

Based on this explanation and considering the expected DSSC gain in the linear region of 520pA/e^-, the minimum and maximum current values for different energies and XFEL operating frequencies can be found (Table 4.3). As it can be seen, a range of three orders of magnitude in the current signal has to be processed by the analog filter. Therefore, to accept input photons of different energies and preserve the dynamic range a coarse gain adjustment is needed. Considering the following ADC section and the requirement to place the first incoming photon in the center of the first bin, this is accomplished by increasing the size of the feedback capacitance in the integrator stage and by regulating the shaping time.

Minimum and maximum signal current with single photon detection						
Ph. Energy [keV]	Frame rate					
	0.9MHz				4.5MHz	
	8 bit		9 bit		8 bit	
0.5	718nA	18.39μA	718nA	36.77μA	NA	
1	147nA	36.77μA	147nA	73.55μA	147nA	36.77μA
3	431nA	110.32μA	431nA	220.64μA	431nA	110.32μA
6	862nA	220.64μA	862nA	300.00μA*	862nA	220.64μA
12	862nA	220.64μA	862nA	300.00μA*	862nA	220.64μA

Table 4.3 *Minimum and maximum signal current for different photon energies and operating frequencies. For the 12keV case the first photon is assigned to two ADC bins. The current values with an asterisk are extrapolated from available DSSC curves and correspond to a full IG.*

4.7 Choice of the feedback capacitors

In the front end the input current is converted to a voltage by integrating it during a time interval τ, common to all pixels, onto a feedback capacitor C_f, which can be chosen separately in every pixel. By

knowing the maximum current $2^N I_{LSB}$ it is possible to determine the value of the feedback capacitor based on the integration time and the corresponding maximum output swing ΔV at the output of the filter:

$$C_f = 2^N I_{LSB} \frac{\tau}{\Delta V} = 2^N \frac{E_\gamma}{3.62eV} \frac{1}{N_{bin/\gamma}} G_q \frac{\tau}{\Delta V}$$

To increase the signal-to-noise ratio the maximum available swing of the filter output should be exploited. In the present design, this swing is about 800mV over a supply voltage of 1.2V. If the supply voltage is increased to 1.4V, the swing would increase correspondingly. The range for ΔV is therefore:

$$0.8V \leq \Delta V \leq 1.0V$$

Given a specific frame rate, the maximum possible integration time should be used to reduce noise. Considering that a total of 120ns might be needed to collect the charge into the IG and to remove it after the signal read out, a maximum filter integration time of 50ns, 162ns and 495ns for the frame rates of 4.5MHz, 2.25MHz and 0.9MHz respectively is available. The range for τ is therefore:

$$50ns \leq \tau \leq 495ns$$

Feedback capacitor value for different photon energies and frame rates						
Ph. Energy [keV]	Frame rate					
	0.9MHz				4.5MHz	
	8 bit		9 bit		8 bit	
0.5	10.66pF[(a)]	7.40pF[(b)]	3.70pF[(b)]	7.40pF[(b)]	NA	
1	7.40pF [(b)]	4.60pF[(c)]	7.40pF[(b)]	4.60pF[(c)]	2.30pF[(c)]	NA
3	6.90pF[(c)]	11.03pF[(d)]	6.90pF[(c)]	11.03pF[(d)]	6.90pF[(c)]	NA
6	11.03pF[(d)]	22.06pF[(d)]	11.03pF[(d)]	22.06pF[(d)]	11.03pF[(d)]	NA
12	11.03pF[(d)]	22.06pF[(d)]	11.03pF[(d)]	22.06pF[(d)]	11.03pF[(d)]	NA

Table 4.4 *Values of the feedback capacitance to cope with the maximum signal current from the detector at different photon energies and frame rates. The integration time is chosen to obtain relatively small values of the capacitance. a) τ=454ns, b) τ=161ns, c) τ=50ns, d) τ=40ns.*

Possible values for the integration capacitance at different frame rates and energies are shown in Table 4.4. A voltage swing of 800mV is considered, with the values for the maximum signal current shown in Table 4.3. Even though a long integration time is beneficial for the noise, when high energy photons have to be accommodated in one ADC bin it is mandatory to reduce τ since the gain cannot be reduced enough by increasing the feedback capacitor. This is because the feedback capacitor is limited by layout constrains to about 13pF, a value that already requires significant economization in other parts of the ASIC. Therefore compromises must be made and available ranges are restricted.

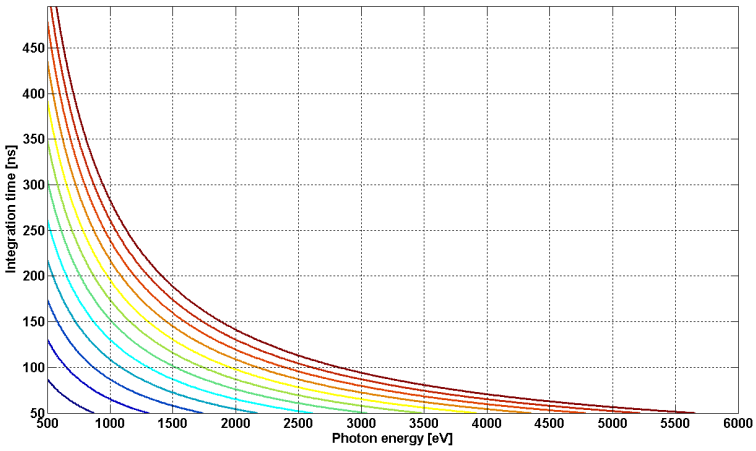

Figure 4.22 *Contour plot of feedback capacitor value for various photon energies and integration times. The lines have a spacing of 1pF and end at 13pF.*

Contour lines of the feedback capacitance value for various photon energies and integration times are shown in Figure 4.22. A maximum value of 13pF for the capacitance is considered. From the graph it is evident how short integration times are needed when the system has to detect high energy photons. The set of integration time and corresponding feedback capacitance is therefore limited. However, when high energy photons have to be detected the electronic noise requirements are more relaxed.

The agreed values of the feedback capacitors for the final chip are based on all these considerations and are chosen to minimize the percentage increment between one capacitance configuration and the following. The goal is to cover all possible gain values by a suitable combination of integration time, feedback capacitance and ramp current. For this reason binary scaled capacitors are not used. The chosen values for the four capacitors are 1pF, 1.5pF, 3.4pF and 7.9pF. A maximum capacitance of 13.8pF can be obtained, thus covering all 8 bit cases and also lower energies if working at 9 bits. The increment in total feedback capacitance for the various configurations is shown in Figure 4.23 and compared to the case of binary scaling.

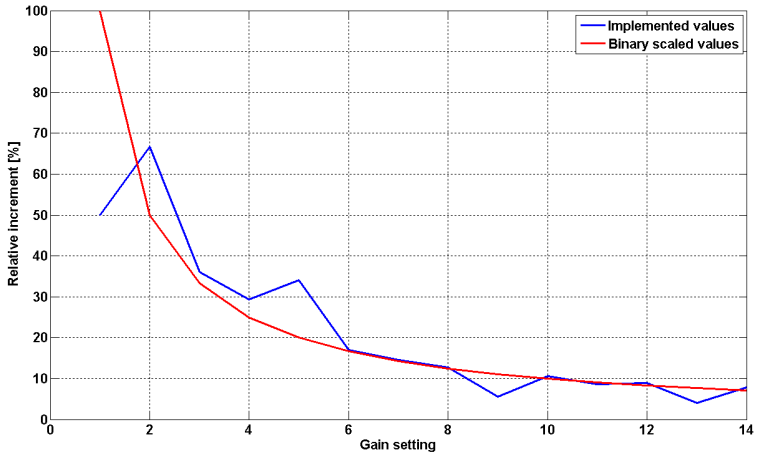

Figure 4.23 *Relative increment between a gain setting and the previous one for the chosen values in the FCF and for the case of binary scaling.*

4.8 Current boost

Besides being beneficial from a noise point of view, a high detection gain requires an electronic front end able to withstand extremely large signals, as shown in Table 4.3. For the DSSC project, if a standard two-stages operational amplifier is used then the input transistors have to be n-type to accommodate the high bias point of the

system. Thus the output stage would comprise a p-MOS with a fixed current provided by a current generator.

The signal current, flowing towards the output of the operational amplifier, would be drawn by the n-MOS current generator and balanced by a reduction of the current in the actively driven p-type device. As a consequence, to cope with high converted energies it would be necessary to bias the second stage of the operational amplifier with a consistently high current. This situation is stressed even more by considering the current required to discharge the following sample and hold capacitor (Figure 4.24).

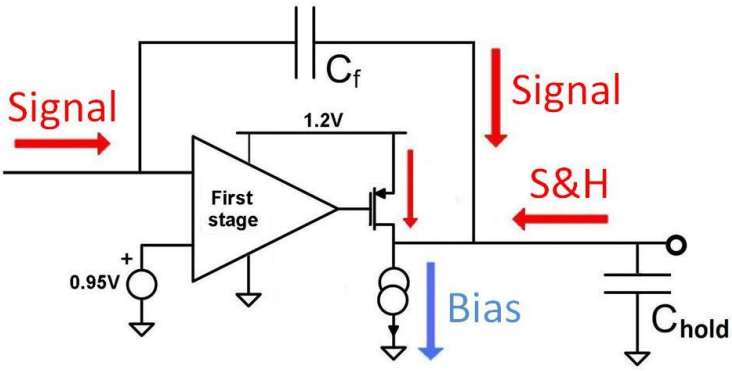

Figure 4.24 *Circuit situation during the signal integration. The current generator of the second stage of the amplifier has to be biased with a sufficiently high current to sink both the signal and the S&H contribution.*

The limitation of the two stages architecture is that the current in the output n-MOS is fixed and it is only redistributed between the p-MOS current, the signal and the S&H contribution. By actively driving the n-MOS it is possible to reduce the static bias current in the output stage and at the same time to cope with large signals. For this reason the adopted architecture comprises an additional branch able to boost the output current on-demand (Figure 4.25).

During signal integration the current in the additional branch increases and so does the current in the output transistor M_6. The mirrors are sized to guarantee a total current consumption that is less than in a

classical two stages amplifier with the same signal capability. In the adopted architecture the output branch is biased with approximately 120μA and the additional branch with about 25μA, for a total of 145μA to be compared with the at least 200μA needed for the output stage a standard amplifier. The maximum current that can be absorbed is obtained when the input stage is completely out of balance, and is therefore the double of the 120μA static current.

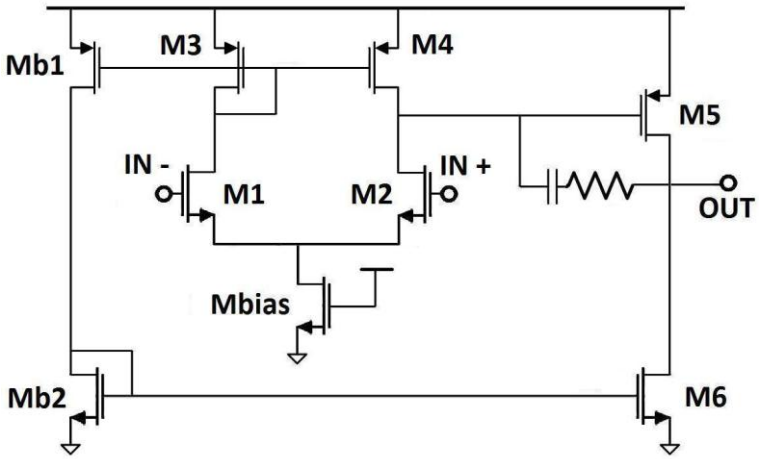

Figure 4.25 *Architecture of the FCF operational amplifier. The branch composed by M_{b1} and M_{b2} is implemented to boost the current of the n-MOS M_6 proportionally to the signal, thus reducing the average power consumption.*

This architecture provides also two other benefits. First of all, for a fixed current flowing towards the output the variation of the virtual ground is reduced since a higher gain is provided. In particular, the gain of the amplifier in terms of output current versus input voltage can be written as follows:

$$\frac{i_{out}}{v_{in}} = g_{m,in} r_{out,1} g_{m,5} + \frac{1}{2} g_{m,in} \lambda_{M3-Mb1} \lambda_{Mb2-M6}$$

where $g_{m,in}$ is the transconductance of the input transistors, $r_{out,1}$ is the output resistance of the first stage at the gate of M_5 with a

transconductance of $g_{m,5}$, and λ_{M3-Mb1} and λ_{Mb2-M6} are the ratios for the mirrors in the additional branch.

The second advantage concerns the frequency response of the amplifier. The additional branch is very fast in responding to the input signal because it comprises only low impedance nodes. Moreover, as the virtual ground increases to accommodate the signal so does the gate of the output n-MOS and this determines a negative swing of the output voltage (Figure 4.26).

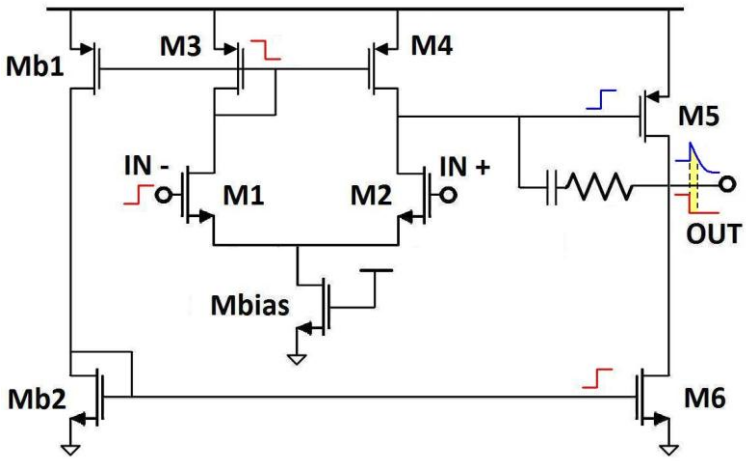

Figure 4.26 *A positive variation at the inverting input of the amplifier propagates to the output along two different paths. The one associated with the additional branch (red steps) has the opposite polarity with respect to the path through the compensation branch (blue).*

This counter balances the initial positive output variation that is induced by the right plane zero associated with the compensation capacitor, and therefore improves stability. With a 1.6pF capacitor and a small resistor of about 400Ω the bandwidth of the operational amplifier is set to about 60MHz with a phase margin of about 75°. From Figure 4.27 it can be noticed that even with no resistor the system would have been stable, but with a lower phase margin, thanks to the effect of the additional branch.

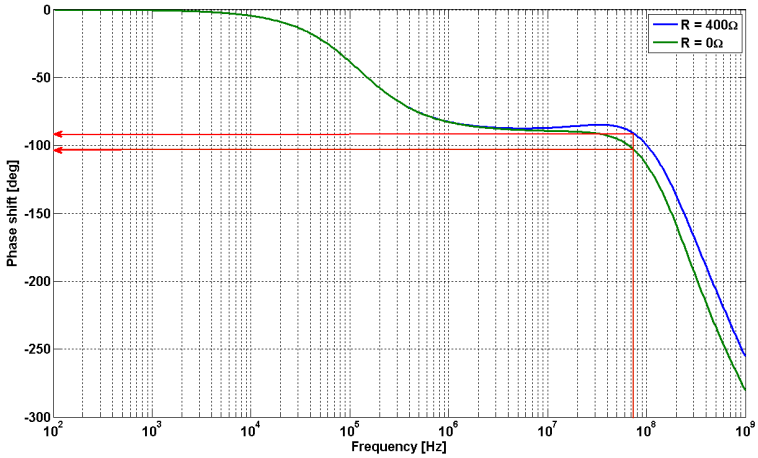

Figure 4.27 *Bode diagram of the phase of the FCF operational amplifier. The introduction of a small resistor in series with the compensation capacitor provides a phase margin of about 75°.*

The total power consumption of the operational amplifier is about 240μW, a value that is within the project specifications. However, with this architecture it is still not possible to measure high energy photons, since the maximum signal current is still too high. For this reason the possibility to increase the size, and thus the current capability, of the output n-MOS has been included. To obtain this result a static switch used to connect a second transistor in parallel to M_6 has been introduced in the latest FCF design.

4.9 The reset phase

During the reset phase the feedback capacitors are short circuited and thus the output goes back to the reference voltage. However, also the compensation capacitor inside the operational amplifier has to go back to the bias conditions. Since the needed current is provided by the first stage then the virtual ground has to move quiet a lot and moreover this process has been found to be not fast enough.

To avoid biasing the first stage with a higher current to increase the slew rate, an additional switch is added in the architecture that short circuits the compensation capacitor during the reset. In this way a very fast recovery is obtained (Figure 4.28). This solution can be exploited since the voltage drop on the capacitor in static conditions is zero.

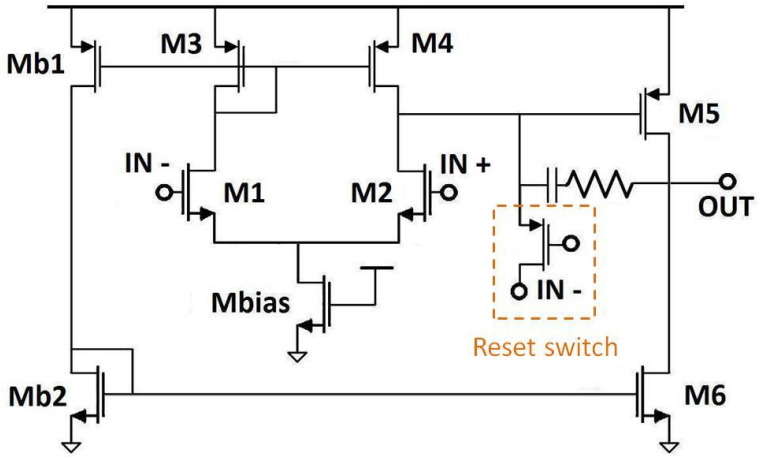

Figure 4.28 *To obtain a fast recovery during the reset phase an additional switch is introduced in the operational amplifier architecture.*

4.10 The dump amplifier

The DSSC signal current must be dumped to a low impedance node at the same potential of the amplifier input during the flip phase. Since the reference block that biases the non-inverting input is not able to sink current, and also to avoid disturbances on the reference voltage, a dedicated buffer to dump the current is introduced in the circuit (Figure 4.29). This block was not included in the first FCF ASIC and also not in the first 8x8 mini-matrix.

A source follower output configuration following a standard two stages architecture is used to provide very low resistance and high output current capability maintaining low power consumption. The circuit

occupies a very small area of about 10x10µm^2 and consumes only 22µA, still being able to cope with signals as high as 300µA.

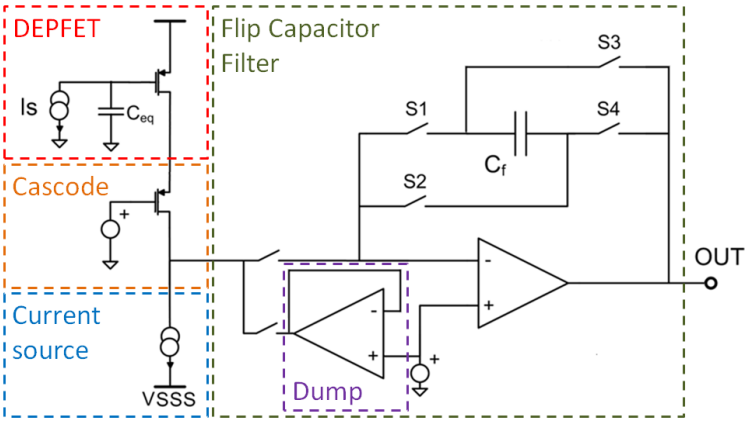

Figure 4.29 *Architecture of the FCF with the introduction of a buffer to dump the current coming from the detector between integrations.*

4.11 The programmable current generator

Threshold shifts in the DSSC detector are expected after X-ray irradiation. Since the FET is a p-type device, trapped charges into the gate oxide lead to an increase of the threshold voltage and thus tend to turn off the device. Measurements have been conducted on a dedicated run to study the radiation hardness of the detector. The test devices were processed in the technology scheduled for the DSSC production and they have been irradiated at the DORIS-F4 beam line at DESY from 100krad up to 100Mrad in three steps per decade. The analysis was focused on p-MOS transistors with and without channel implantation that are representative of the gate and the clear gate of the detector. The threshold voltage shift at a dose of 100Mrad is about 4V for the depletion type and about 5.5V for the enhancement type transistors (Figure 4.30).

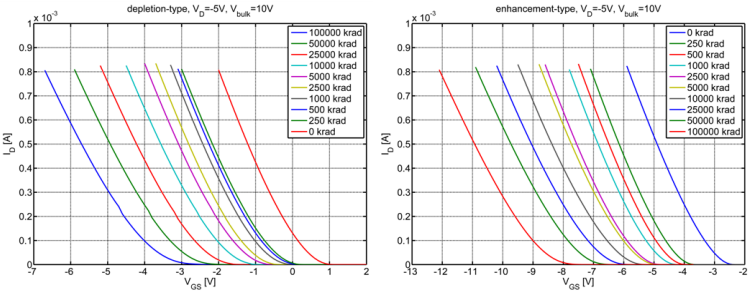

Figure 4.30 *Transfer characteristics of a depletion-type (left) and of an enhancement-type (right) transistor at different levels of irradiation. The first case is representative of the DEPFET gate, the latter of the clear gate.*

For the DEPFET gate the limitation is given by the dynamic range of the ASIC in terms of the minimum and maximum bias current that the front end is able to sink. For the clear gate the limitation is given by the effective operation window, which is assumed to have a width of less than 3V based on simulations and experience with similar devices. Both constrains translate to an allowed absorbed dose of roughly 100krad. The transfer from the absorbed dose to the number of absorbed photons per pixel as a function of photon energy is shown in Figure 4.31.

To avoid having dead pixels in the matrix a possibility is to decrease the external gate voltage of the transistor to compensate for the increased threshold. However, since the gate voltage is not provided separately to every pixel such a choice will lead to a considerable bias current spread on the imager. As a consequence, the front end must be able to cope with a wide range of bias current. Also flicker noise can determine a slow variation between subsequent macro bunches and it is fundamental to avoid saturation of the filter because of a too large baseline.

The proposed current generator is based on a two steps process: a coarse regulation of the current is obtained setting the bits of a digital-to-analog converter, while fine regulation is achieved controlling the gate voltage of the transistors in the active branches of the DAC. While the bits can be set once for a certain number of experiments, the gate voltage

has to be continuously updated to be effective. As already foreseen in the preliminary studies, this programming phase can be done before X-ray pulses start to arrive on the imager.

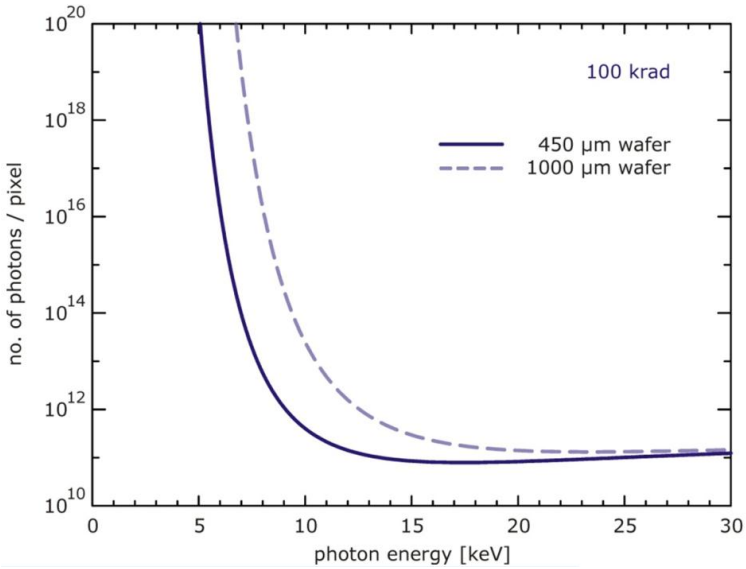

Figure 4.31 *Radiation tolerance of the DSSC sensor in terms of maximum number of photons per pixel as a function of the photon energy. The solid line refers to the actual wafer thickness of 450µm. The dashed curve refers to a wafer thickness of 1 mm as an option for future device generations.*

4.11.1 The programming loop

The time structure of X-ray pulses gives the possibility to program the current source before the start of a new macro bunch, and makes feasible to use the same amplifier used for the filtering phase to set the DAC gate voltage when closed in a different loop, once more saving area. One simple inverting stage must be included in the loop to have a negative feedback. This block is realized using an icon cell (Figure 4.32). The error current arriving from the drain of the cascode flows in the first branch of the icon and is mirrored to the output with opposite direction. The cell is biased fixing the gate voltages of the central transistors at the same reference voltage of the filter amplifier, thus blocking also the input

node at the same value. The icon is off when no current is arriving, thus saving power, while it is very fast in reacting when needed.

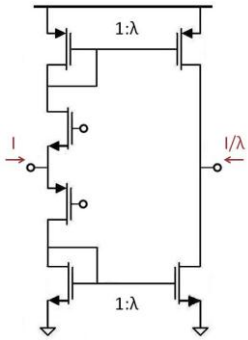

Figure 4.32 *Schematic of the icon cell used in the FCF front end to obtain a negative programming loop.*

At the end of the programming phase this cell is left floating, and does not require current from the supply. The circuit configuration during the programming phase is shown in Figure 4.33. The voltage on the gate is sampled onto a dedicated capacitor to maintain the programmed current stable during the macro bunch. The size of this capacitor has to be large enough to minimize the voltage variation due to leakage and to reduce coupling from the filter input node through the parasitic components of the transistors. A value of 2pF has been chosen.

When the single integration read out scheme is employed (see section 3.4.2) the weighting function of the filter is no longer trapezoidal, since the baseline measurement is obtained by means of the programming closed loop configuration with a finite bandwidth. As a result, an exponential shape following the time constant of the programming loop is obtained. Measured weighting functions with this behavior are presented in Chapter 5.

The gain of the programming loop is about 65dB, so that a residual baseline current proportional to the bias component is always present. The filter is designed to withstand a residual current after compensation of 3μA in either direction with the nominal reference voltage.

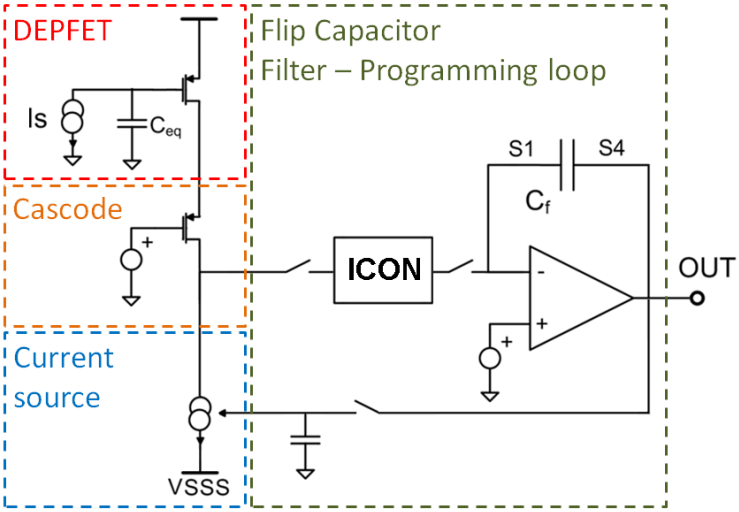

Figure 4.33 *Circuit configuration during the programming phase of the current source.*

4.11.2 Noise considerations and current source architecture

The noise of the current generator has to be minimized, since this block is directly connected to the input node and its noise contribution directly compares to the signal arriving from the detector. If the cascode stage is considered ideal, then current noise spectral density flowing towards the filter can be expressed as follows:

$$\overline{n_i^2} = \frac{4k_BT}{R_{eq,DEPFET}} + \frac{4k_BT}{R_{eq,DAC}} = \frac{4k_BT}{R_{eq,DEPFET}}\left[1 + \frac{R_{eq,DEPFET}}{R_{eq,DAC}}\right]$$

where $R_{eq,DEPFET}$ is the detector equivalent resistance that gives the same noise spectral density as the DSSC itself, with a value of 8.3kΩ. $R_{eq,DAC}$ accounts for the programmable generator noise contribution. It is therefore mandatory to use sufficiently high resistors in the current generator architecture.

In the initial phase of the project, with an expected gain of the detector around 350pA/e$^-$, this required an additional negative voltage to bias the resistors. The initially designed current generator architecture,

shown in Figure 4.34, has been implemented in the first versions of the front end ASIC and also in the mini-matrices chips, with a small modification for what concerns the MM2 ASIC. The architecture is studied to avoid the possibility that internal nodes reach too negative values. For this reason it is not possible to switch off the current in the unused branches. The p-MOS transistors are then connected to the supply to provide an alternative path for the current. As a consequence, current absorption depends on the programmed word, complicating the design of the external power boards.

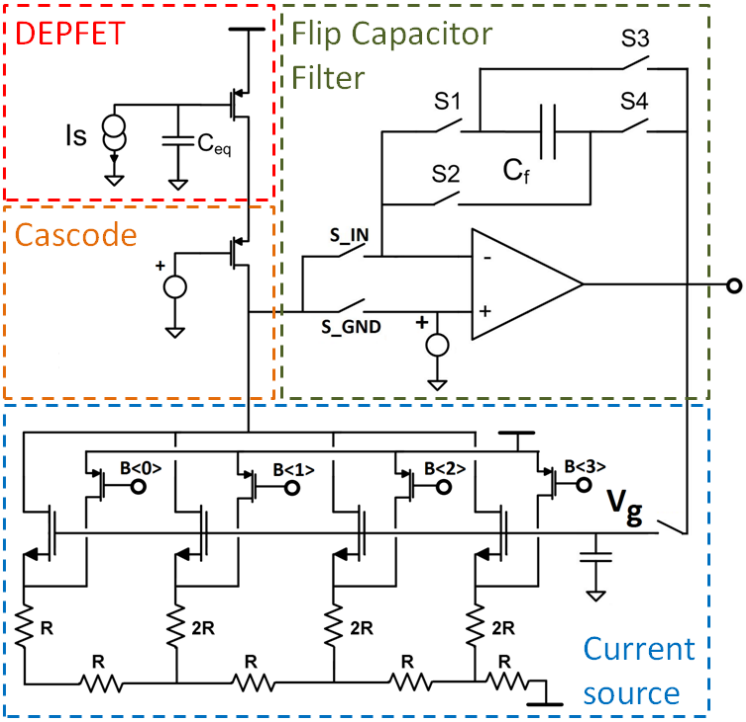

Figure 4.34 *Architecture of the first version of the programmable current source. The icon and the dump are not shown for simplicity.*

The nominal value of the external voltage VSSS is -3V, but the possibility to lower this level was also foreseen to increase the maximum current that the generator could draw. Current ratios between the branches are on a quasi-binary scaling, as the dimensions of the

transistors, moving from the LSB $B_{<0>}$ to the MSB $B_{<3>}$. The circuit always sinks the same current to VSSS, taking the difference to the DEPFET bias current from the ASIC supply. Simulated values for the current drawn by the first version of the programmable current source are shown in Figure 4.35.

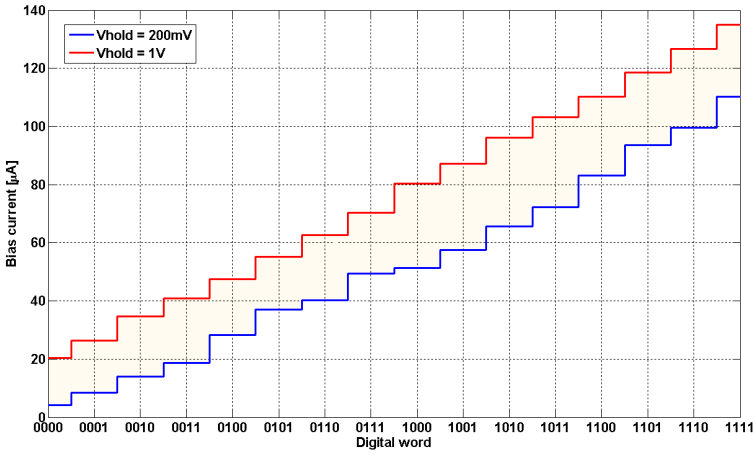

Figure 4.35 *Simulated values for the current drawn by the first version of the programmable current source for the minimum (0.2V) and maximum (1V) voltages at the control gate and for different binary codes applied for the coarse regulation. The shadowed area represents the coverable detector biasing.*

After the measurements on the DSSC prototypes and the simulations of the detector in the final technology a higher gain of about 520pA/e^- is expected, so that the noise requirements on the current generator are relaxed. For this reason, in the last design of the system the external voltage has been removed to simplify the external power boards design, and smaller value resistors are used. Secondly, only one branch is connected to the gate voltage regulation loop, while the others are connected to the reference voltage. The current in the unused branches is set to zero by opening a switch in the branch: this was not possible in the previous architecture since a zero voltage drop on the resistors would have lowered the source voltages of the transistors too much. In this way there is no additional contribution to the overall power consumption,

since this circuit only sinks the detector current. The new architecture is shown in Figure 4.36.

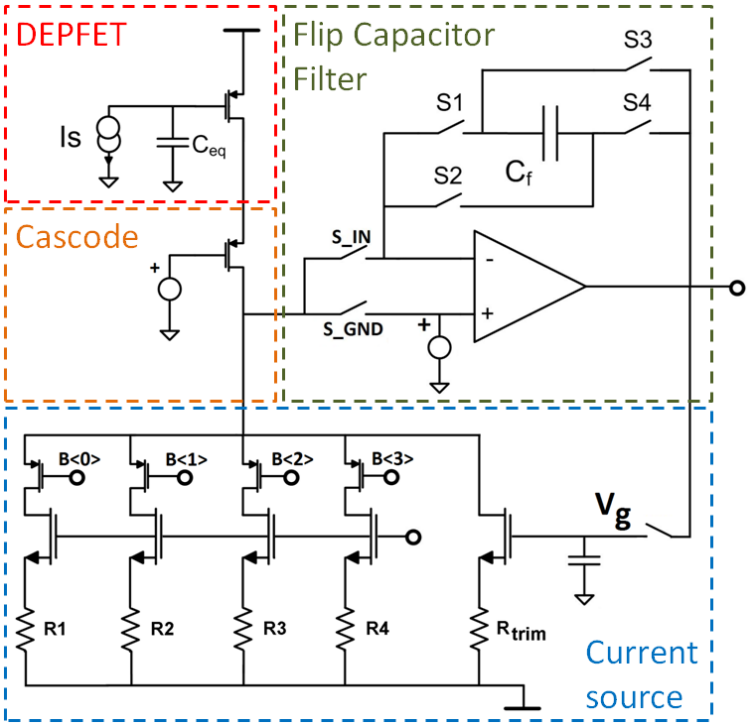

Figure 4.36 *Architecture of the new version of the programmable current source along with the complete FCF front end circuit. The VSSS node is now at ground potential. The icon and the dump are not shown for simplicity.*

The aspect ratio of the n-MOS transistors connected to the reference voltage along with the resistors values is determined by the desired maximum programmable current and step size. Current ratios are on a binary basis. To increase the values of the resistors as much as possible the structure employs zero-threshold devices. Design values are of 7.5kΩ, 15kΩ, 30kΩ and 60kΩ. The fine tuning branch with a resistor of 25kΩ is designed so that it is possible to cover a current range of about 2 to 3 steps with the same binary code, providing a suitable combination of bits and gate voltage to comply with any bias current value that is in

dynamic. The switches are p-type devices sized to minimize the series resistance when on and thus guarantee that the n-MOS transistors work in saturation.

A simulation of the characteristic for this new architecture is shown in Figure 4.37. The circuit is able to cope with bias currents ranging from about 230µA down to only 10µA. The step size for a fixed gate voltage and changing the digital word by one bit is 12-14µA, while the fine regulation range at a fixed binary code is about 23µA.

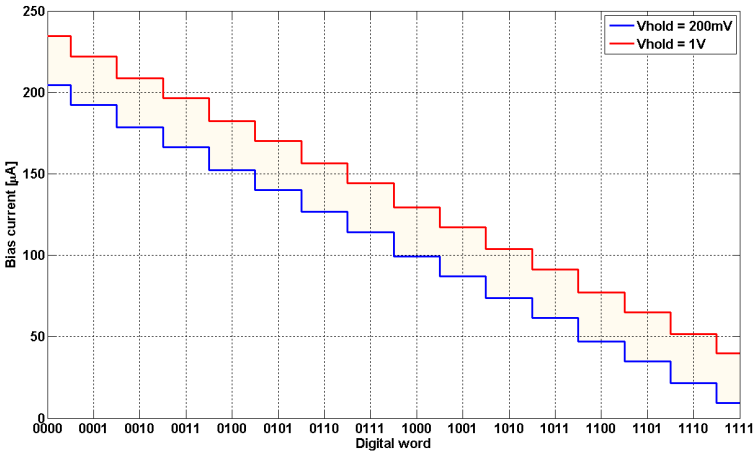

Figure 4.37 *Simulated values for the current drawn by the new version of the programmable current source for the minimum (0.2V) and maximum (1V) voltages at the control gate and for different binary codes applied for the coarse regulation. The shadowed area represents the coverable detector biasing.*

4.12 Complete circuit and layout

In the first phase of the DSSC project all building blocks have been submitted on dedicated ASICs. The FCF ASIC includes all blocks described in this Chapter, with the exception of the dump amplifier that has been introduced in a second moment.

The expected noise performances of the analog front end are shown in Table 4.5.

Expected noise values					
4.5MHz (τ=40ns)		0.9MHz (τ=400ns)		4,5MHz (τ=80ns), single integration	
DEPFET	32el$^-$	DEPFET	10.3el$^-$	DEPFET	22.8el$^-$
FCF circuit	25.3el$^-$	FCF circuit	5.3el$^-$	FCF circuit	14.8el$^-$
Total	**42el$^-$**	Total	**11.6el$^-$**	Total	**27.2el$^-$**

Table 4.5 *Expected noise values as reported in [8]. The initially foreseen gain of 350pA/e$^-$ for the detector is used. This is the same value of the gain obtained during measurements with a standard type DEPFET.*

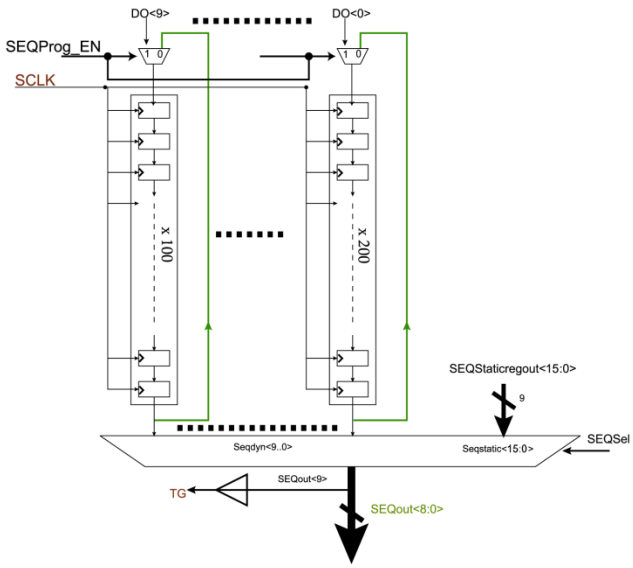

Figure 4.38 *Architecture of the sequencer implemented in the first FCF ASIC. This block has been designed in conjunction with MPI- HLL and the University of Mannheim.*

A digital sequencer (Figure 4.38) is included to provide the signals for the internal switches. Dedicated test inputs and outputs allow verifying the functionality of the filter and characterizing its performances. In particular, dedicated circuitry gives the possibility to

test the ASIC without a detector connected. A sample and hold stage is included and a dedicated buffer with high current capability is present to bring out the output signal. A second buffer is used to monitor the voltage on the programmable current source.

Three similar structures have been implemented to test slightly different design details in the circuit. In this first ASIC all feedback capacitors have the same value of 1.6pF. The chip size is 1.4x4.4mm^2, while the area of the FCF is about 150x160μm^2. The layout of the filter, along with the output buffers, is shown in Figure 4.39.

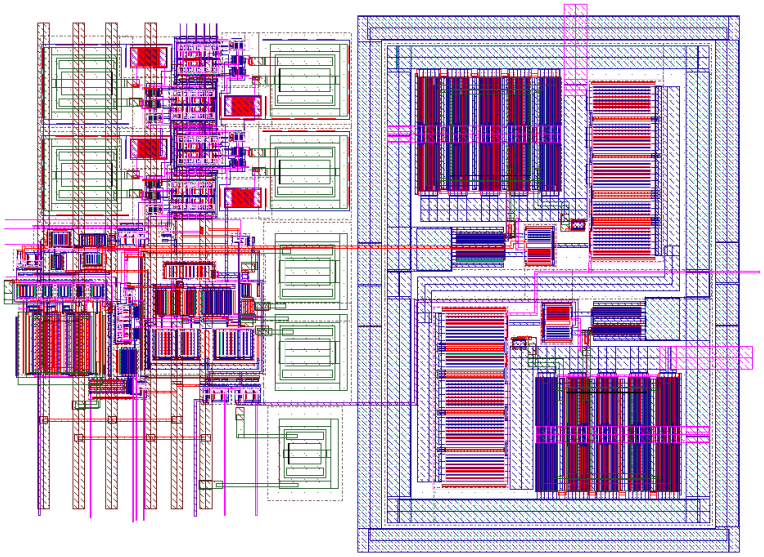

Figure 4.39 *Layout of the first version of the FCF. On the left side are located the main filter amplifier, the programmable current source and the feedback capacitors. The right side is occupied by the output buffers.*

After characterization of the various ASICs, two mini-matrices have been produced integrating all DSSC blocks. The dump amplifier is included in the second version of the 8x8 chip, called MM2. The layout of the filter has been optimized to fit in the available space and the final area is 88x84μm^2. This is less than 20% of the total pixel area. The new programmable current generator has been included in the MM3 chip, submitted in May, 2012.

4.13 Bibliography

[1] L. Bombelli, C. Fiorini, M. Porro, S. Herrmann, S. Wölfel, "VELA: the CMOS circuit based on fast current read-out for X-ray spectroscopy with DePMOS", IEEE Trans. Nucl. Sci., vol. 54, Issue 4, 1359, Aug. 2007.

[2] L. Bombelli, C. Fiorini, A. Marone, S. Facchinetti, M. Porro, J. Treis, S. Herrmann, A. Wassatsch, "A new readout method based on source-current readout for DEPFET-based imagers", 2010 IEEE Nuclear Science Symposium Conference Record, pp. 131-134.

[3] IXO/XEUS website, http://sci.esa.int/xeus/

[4] The Simbol-X website, http://www.asdc.asi.it/simbol-x/

[5] C. Fiorini, A. Pullia, E. Gatti, A. Longoni, W. Buttler, "First experimental characterization of ROTOR: the new switched-current VLSI amplifier for X-ray spectroscopy with silicon drift detectors", IEEE Trans. Nucl. Sci., vol. 47, issue 3, 823, Jun. 2000.

[6] E. Bonanomi, "Studio di fattibilità di circuiti per la lettura veloce di rivelatori in esperimenti al X-ray Free Electron Laser", Master of Science thesis, Politecnico di Milano, 2008.

[7] L. Bombelli, "Development of low-noise analog readout for fast X-ray imaging applications based on DEPFET pixel detector", Doctoral Dissertation, Politecnico Di Milano, 2009.

[8] L. Bombelli, C. Fiorini, S. Facchinetti, M. Porro, and G. De Vita, "A fast current readout strategy for the XFEL DePFET detector", Nucl. Instrum. Methods Phys. Res. A, vol. 624, pp. 360-366, 2010.

[9] S. Facchinetti, L. Bombelli, A. Castoldi, C. Fiorini, C. Guazzoni, D. Mezza, M. Porro, G. De Vita, F. Erdinger, "Fast, low-noise, low-power electronics for the analog readout of non-linear DEPFET pixels", 2011 IEEE Nuclear Science Symposium Conference Record, pp. 1846-1851.

CHAPTER 5

Characterization of the FCF

5.1 Experimental setup for the FCF ASIC

A dedicated experimental setup, shown in Figure 5.1, has been developed to test the performances of the FCF, both alone and together with a single pixel linear DEPFET [1]-[2]. The setup has been prepared in collaboration with MPI-HLL, Munich. The first board carries the FCF chip and a 4x4 DEPFET matrix, and is connected to the second main PCB which delivers the bias voltages and the digital signals necessary for the system operation and provides adequate amplification of the filter output signal. Moreover, two DG419CJ analog multiplexers from Maxim Integrated Products are used to generate the clear and clear gate signals.

An adjustable pole-zero compensation network is also introduced to speed up the transitions and remove possible oscillations at the multiplexers output.

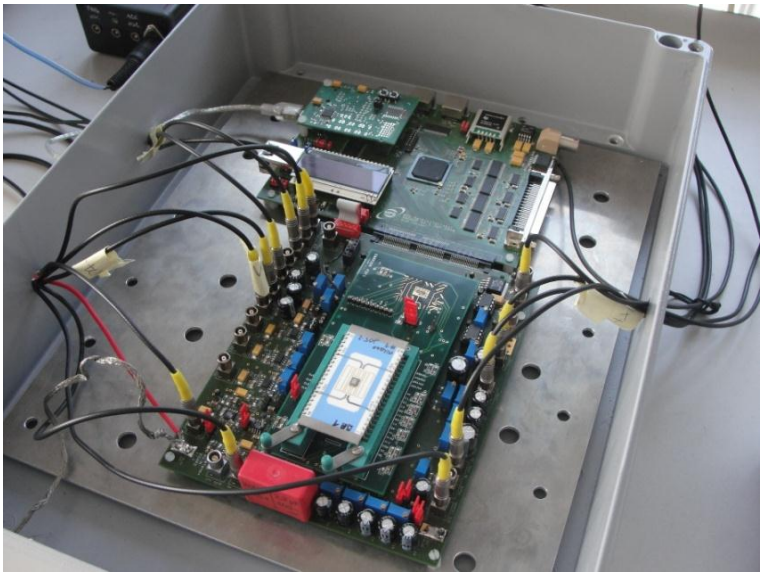

Figure 5.1 *Picture of the experimental setup for the characterization of the FCF ASIC. The boards are placed in a box to screen the detector from external light.*

A last board hosts a VIRTEX II FPGA that regulates the global timing of the signals, programs the on-chip digital sequencer and handles the communication with the PC. LVDS lines are sent to the main board through a high speed connector and then converted by a dedicated CPLD to 1.2V CMOS signals compatible with the ASIC dynamic. The LCMXO1200E from Lattice Semiconductor is used for this purpose. The clock for the on-chip sequencer is provided by the FPGA at a frequency of 82.5MHz, thus giving a 12.12ns time resolution.

To test the ASIC alone, the detector can be emulated by means of a test signal given by an Agilent 33250A external pulser. The output signal of the filter is finally processed by a Multi-Channel Analyzer (MCA). The entire setup is controlled via PC through software developed

in LabVIEW. A conceptual blocks diagram of the setup is sketched in Figure 5.2.

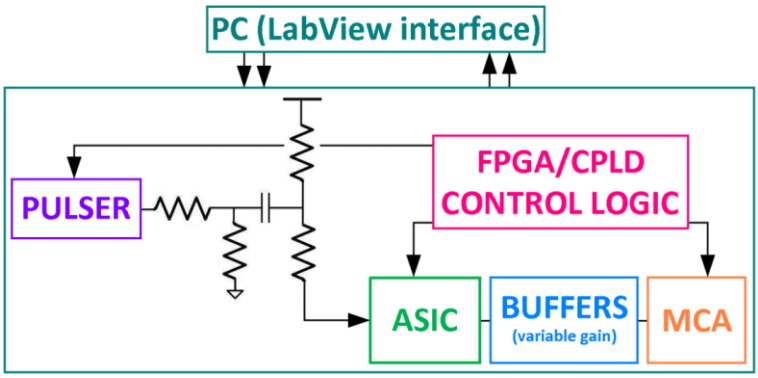

Figure 5.2 *Sketch of the setup interfaces arrangement.*

5.2 External network to generate the bias and signal

In Figure 5.3 a schematic representation of the network used to simulate the detector is shown. The resistors R_1 and R_2 provide signal termination from the pulser and also give the possibility to generate signals with an amplitude lower than the minimum provided by the pulser. The series of the R_3 and R_4 resistors is used to provide a constant current similar to the bias current of the DSSC. The voltage pulse provided by the Agilent 33250A is AC coupled to the middle node of these resistors and is converted to a current signal that can be processed by the filter.

By assuming that the input node of the filter is a ground for the signal, thanks to the low impedance provided by the cascode, the transfer function between the signal from the pulser and the voltage at node A is:

$$\frac{V_A(s)}{V_{PULSER}(s)} = \frac{R_2}{R_1 + R_2} \frac{sC(R_3//R_4)}{1 + sC[(R_1//R_2) + (R_3//R_4)]}$$

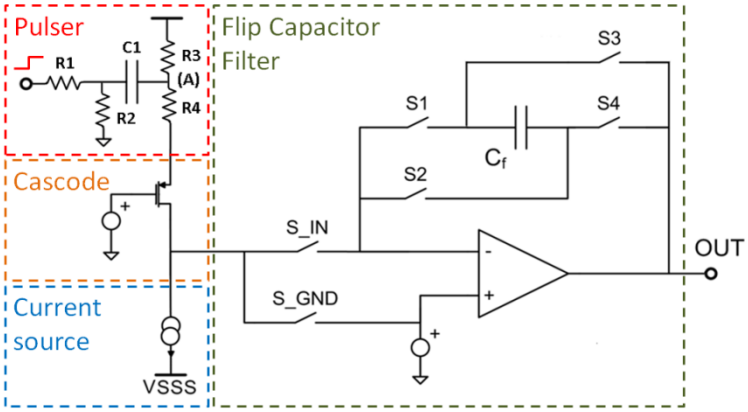

Figure 5.3 *Schematic including the FCF architecture and the external network ("Pulser") used to emulate the detector.*

The implemented RC time constant τ_p of the network can be evaluated using the values in Table 5.1:

$$\tau_p = C[(R_1//R_2) + (R_3//R_4)] \cong 10ms$$

Input network parameters				
R1	R2	R3	R4	C1
40Ω	10Ω	1kΩ	51kΩ	10μF

Table 5.1 *Values of the components in the network connected between the pulser and the FCF input.*

This value is larger than the pulse duration, so that the input current can be effectively considered constant in the interval of interest. On the edge of the input pulse the transfer function can be written as follows:

$$\frac{V_A(s=\infty)}{V_{PULSER}(s=\infty)} = \frac{(R_3//R_4)//R_2}{R_1 + (R_3//R_4)//R_2} \cong \frac{R_2}{R_1 + R_2}$$

To a first approximation the corresponding input current induced by the pulser is then:

$$I_{signal} = \frac{V_A}{R_4} = \frac{R_2}{R_1 + R_2}\frac{V_{PULSER}}{R_4}$$

Inside the ASIC a second resistor of the same value of R_4 is implemented that can be used when small signals are desired. On the other side, it is not effective when large currents are needed due to the big voltage drop that would develop across the component.

5.3 Oscilloscope waveforms

Figure 5.4 shows the oscilloscope waveforms corresponding to the amplified output of the filter and to a reference digital signal that is high during the FCF integration phases. The inversion of the capacitor takes place in the short time between the two integrations. It can be noticed that the output voltage goes back to the initial value, as expected since no signal is applied and only a baseline contribution in present. The output signal is low pass filtered with respect to the output of the chip because of the external amplifiers bandwidth.

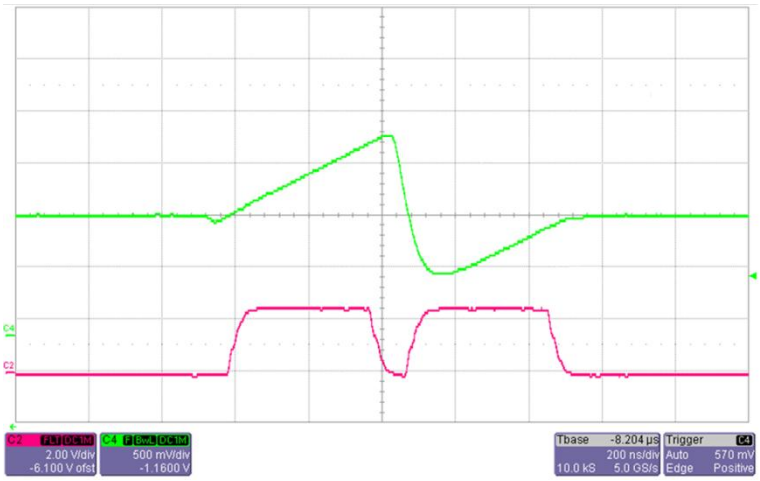

Figure 5.4 *Oscilloscope waveforms of the amplified output of the filter (green) and of a digital signal indicating the two FCF integrations (purple) for the double integrations read out scheme.*

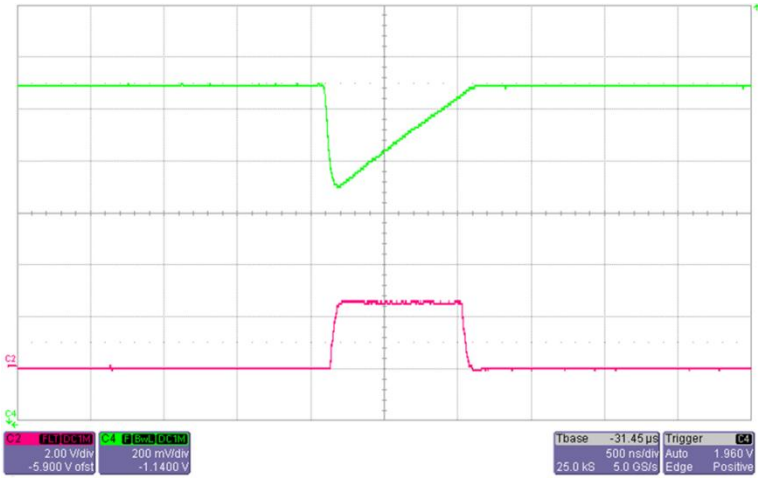

Figure 5.5 *Oscilloscope waveforms of the amplified output of the filter (green) and of a digital signal indicating the FCF integration (purple) for the single integration read out scheme.*

The same traces are shown in Figure 5.5 for the single integration per read out cycle approach. Again, no signal is applied and only a baseline contribution is provided. In this case, the value of the baseline is stored on the programmable current source and thus the output voltage level after the reset is not the same as at the end of the integration. This difference corresponds to the presence of a residual baseline that flows towards the filter. However, the final level is the same for every cycle and so it can be considered as an offset contribution.

5.4 The programmable current generator

In the FCF ASIC the first version of the programmable current source is implemented (refer to section 4.10.2). The current range drawn by this block is defined by two parameters: the external negative voltage VSSS and a four bit binary code. The former sets the maximum value that can be programmed, while the latter defines the coarse regulation of the structure. Then, fine regulation in the defined range is obtained by setting the control gate voltage.

The current values drawn by the circuit for a nominal VSSS value of -3V and for different digital words are shown in Figure 5.6. The values are obtained by placing the minimum (0.2V) and maximum (1V) voltages at the control gate; these voltages roughly correspond to the output dynamic range of the filter. For a given binary code, the current is programmable in the range between the two extremes given by these voltages. As can be seen, the current generator can be programmed within a range of about 140µA, in good agreement with simulations. This value can be extended to about 250µA by lowering VSSS to -6 V (Figure 5.7). Lower values are not allowed by the technology.

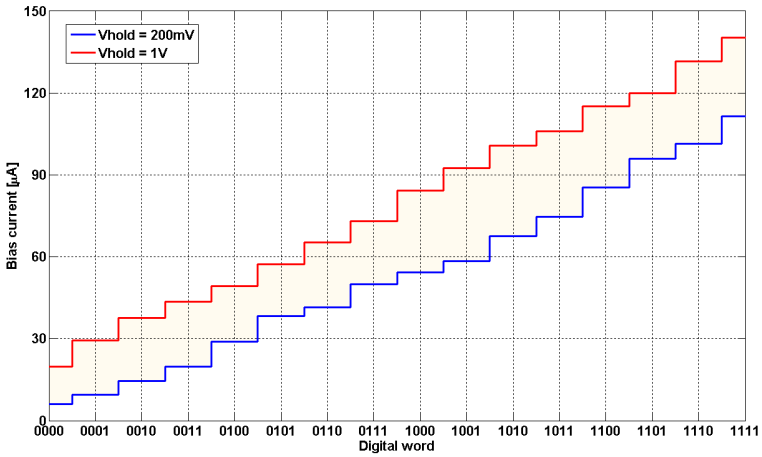

Figure 5.6 *Measured values for the current drawn by the programmable current source for the minimum (0.2V) and maximum (1V) voltages at the control gate and for different binary codes applied for the coarse regulation. VSSS is set to -3V. The shadowed area represents the coverable detector biasing. Obtained values are close to expected ones.*

Figure 5.8 shows that the source voltage of the input cascode does not increase too much even when large currents are flowing in the input branch. This is because the device has a very large transconductance.

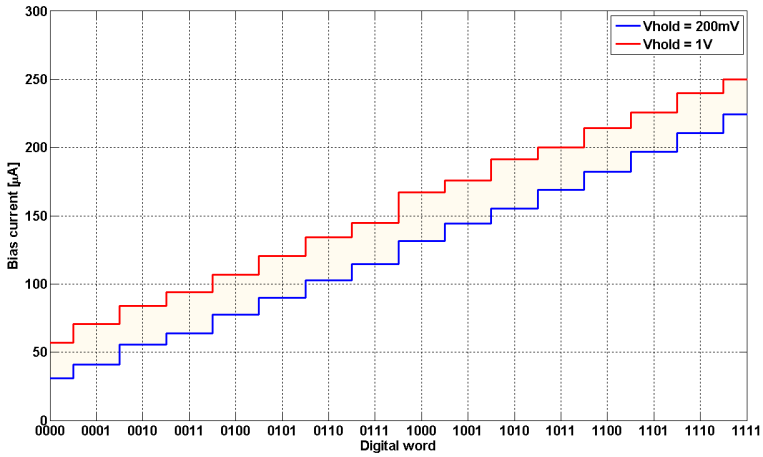

Figure 5.7 *Measured values for the current drawn by the programmable current source for the minimum (0.2V) and maximum (1V) voltages at the control gate and for different binary codes applied for the coarse regulation. VSSS is set to -6V. The shadowed area represents the coverable detector biasing.*

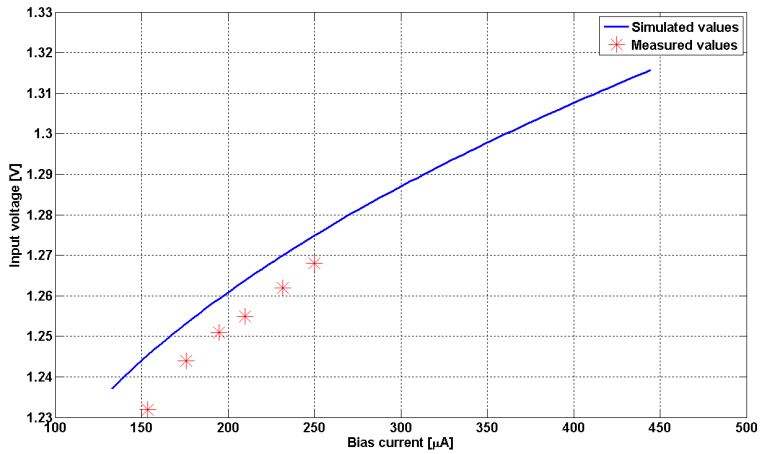

Figure 5.8 *Input voltage for different values of the DEPFET bias current. The gate of the cascode is at 950mV. Measured values are limited by the actual implementation to the maximum current of 250µA (with a VSSS of -6V).*

Figure 5.9 shows the acquired waveform of the amplified output of the filter when a 2.45µA current step over a static current of 100µA is

applied during the programming phase. One feedback capacitor is connected in integrator stage. The circuit reacts to accommodate the new value of the bias current by increasing the gate voltage of the current generator. The acquired waveform has a negative swing since the external gain is inverting. When the current step is removed the voltage on the current source goes back to the previous value.

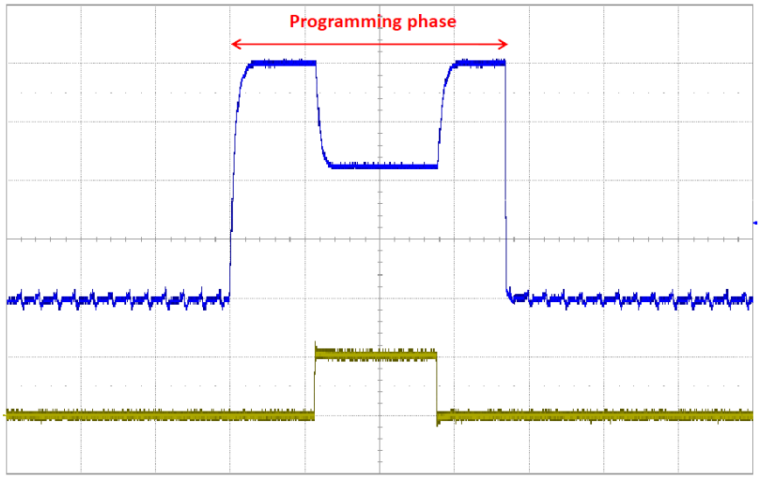

Figure 5.9 *Oscilloscope traces of the amplified output of the filter (blue) and of the input current (yellow). A step is induced during the programming phase. Vertical scale: 500mV/div, horizontal scale: 2μs/div.*

The filter gain in the programming phase has no impact on the current range that can be set, but is important for noise performances. In fact, to reduce the noise introduced by this phase the best solution consists of connecting all possible feedback capacitors in the filter, thus lowering the bandwidth of the programming loop. This is particularly important when the single integration read out scheme is employed, since the noise sampled on the hold capacitor is not removed by the two correlated measurements introducing fluctuations between different macro bunches. The effect of an increased value of the feedback capacitance is shown in Figure 5.10, when the same current step as the previous case is provided. By enabling more capacitors, a slower

programming loop is obtained and this can be seen in the longer time constant of the output node of the filter.

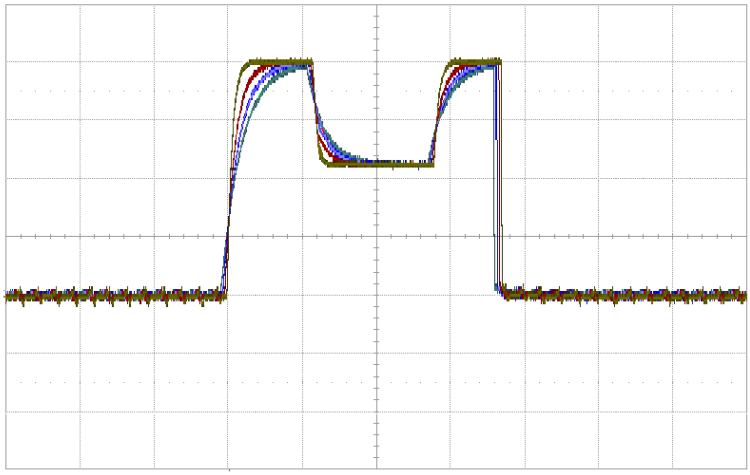

Figure 5.10 *Oscilloscope traces of the amplified output of the filter for different values (1.6pF, 3.2pF, 4.8pF and 6.4pF) of the feedback capacitance. Vertical scale: 500mV/div, horizontal scale: 2µs/div.*

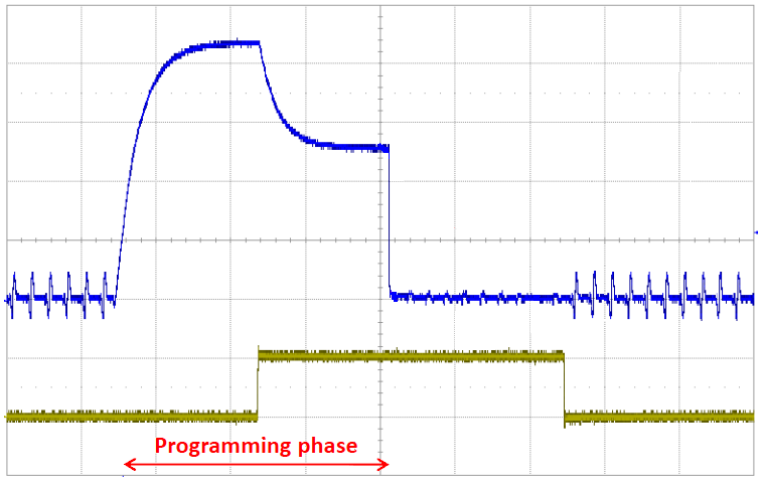

Figure 5.11 *Oscilloscope traces of the amplified output of the filter (blue) and of the input current (yellow). A step is induced that runs across the programming phase and is removed during the filtering phase. Vertical scale: 500mV/div, horizontal scale: 2µs/div.*

Finally, in Figure 5.11 a current pulse that extends over the filtering phase is provided. In the first read out cycles the output voltage is basically constant thanks to the correct programming of the current generator. Therefore, no baseline current flows towards the filter. When the additional current is removed, a mismatch between the bias and the programmable generator currents is introduced, determining a baseline contribution. However, it can be noticed that the final output voltage after the double correlated measurement is the same as it is without any baseline, thus confirming also the capability of the filter to reject constant contributions.

5.5 Weighting functions

The FCF implements a trapezoidal weighting function to minimize the series white noise contribution, as already described in section 3.4.2. In the following measured weighting functions of the filter alone are presented. In all weighting function figures, the horizontal axis represent the time interval between the application of the input signal and the instant in which the filter output is sampled, with the latter occurring at the end of the read out cycle.

In the FCF ASIC prototype two similar structures are integrated to verify whether the impact of the additional capacitor is effective as expected (see section 4.4). This can be deducted by looking at the weighting functions of the circuit. A significant stray capacitance would lead to different slopes in the weighting function, and thus the initial and final values would not be at the same level. As a consequence flicker noise is not completely canceled out by the filter. In particular, the final level should be higher than the initial one.

Figure 5.12 shows the measurements corresponding to a frame rate of 0.9MHz, with an integration time of about 400ns. The approximation is given by the limited FPGA clock resolution. First of all, it can be noticed that the obtained weighting functions are very close to an ideal trapezoid for both configurations. Moreover, the additional

capacitor works as expected, lowering the final value with respect to the other case in which no compensation is used.

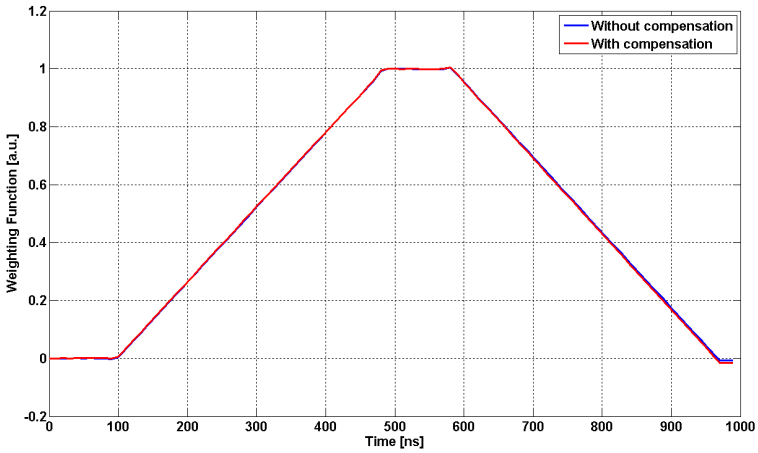

Figure 5.12 *Measured weighting functions with and without the additional compensation capacitor for an integration time of about 400ns.*

However, the weighting function without compensation is lower than the initial value, differently from what expected. This is probably because stray capacitances were not correctly estimated in the extracted layout. The error is in the order of less than 1% for both cases, with a difference between the two configurations of less than 0.5%. Such a small value is compatible with the operation of the front end, so that even though the proposed solution is effective the DSSC collaboration agreed to not implement it. All the measurements presented next are obtained with the FCF without additional capacitor.

The measured weighting functions for the double integration read out scheme are shown in Figure 5.13 for three different integration times of about 35ns, 100ns and 400ns. These values correspond to the operating frequencies of 4.5MHz, 2.25MHz and 0.9MHz. In this solution, the filter uses two correlated measurements to reduce flicker noise in every cycle, one measurement of the drain current before the signal arrival (baseline read out) and one afterward (signal and baseline read out). As already shown in Figure 5.12, the baseline returns to zero within 1% at the end of

second integration for all cases. However, the effect is negligible and obtained performances are completely adequate for XFEL operation. Figure 5.14 shows measured weighting functions for a different number of feedback capacitors connected in the filter. The results are very similar for all configurations.

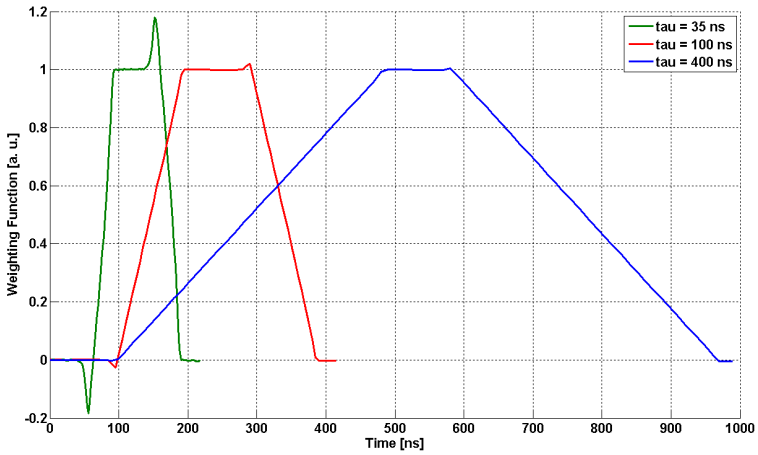

Figure 5.13 *Measured weighting functions for the double integration read out scheme and for different operating frequencies.*

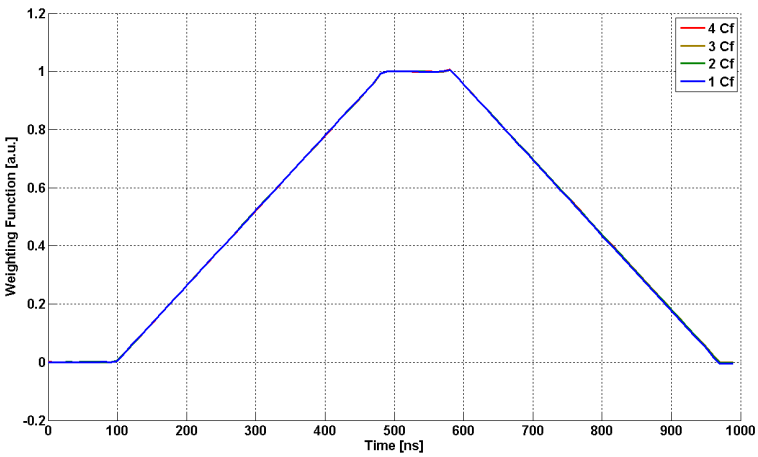

Figure 5.14 *Measured weighting functions for different number of feedback capacitors connected in the FCF for an operating frequency of 0.9MHz.*

Spikes in the weighting functions are visible, due to the finite time response of the power supply in stabilizing the operational amplifier reference, to which the signal current is injected between subsequent integrations. In fact, in the first FCF chip the current dump amplifier is not implemented, so the reference voltage for the operational amplifier is provided externally. This explanation has been also confirmed by simulations. The spikes amplitude appears to be different because of the normalization process.

The timing scheme corresponding to a single integration in every read out cycle has been tested, too. In Figure 5.15 the weighting functions for different values of the feedback capacitance are shown at an operating frequency of 0.9MHz. The integration lasted about 800 ns and the output signal was acquired at the end of what would be the first read out cycle in the macro bunch. As expected, the weighting function is no longer trapezoidal, showing an exponential tail in correspondence of the finite bandwidth of the current source programming loop.

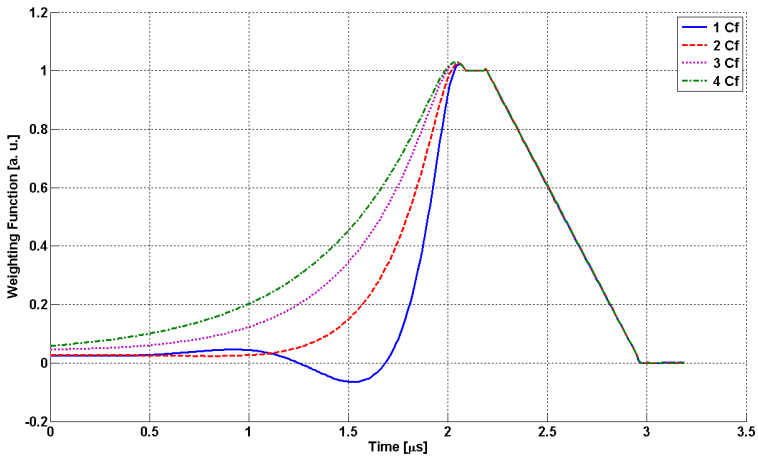

Figure 5.15 *Measured weighting functions for the single integration read out scheme varying the number of feedback capacitors.*

As already described, to have a low noise programming, it is necessary to connect all the available filter capacitors in this phase to reduce the bandwidth. To be more precise, the weighting function slope

must be lower when pulses arrive in the programming phase with respect to the slope for pulses arriving during integrations. At short processing times, where the gain is the highest, it is therefore mandatory to connect all the available capacitors. For this reason, in the last implementations of the DSSC pixel the "Enable" is gated with the signal that determines the programming phase so that all capacitors are connected regardless of the desired gain.

5.6 Linearity measurements

The filter linearity without detector has been extracted with particular attention to the first region, where a one-to-one correspondence between input photons and ADC bins is required. The gain of the circuit, defined as the ratio of the output voltage swing to the input current signal, has been measured for different values of the feedback capacitance (Figure 5.16).

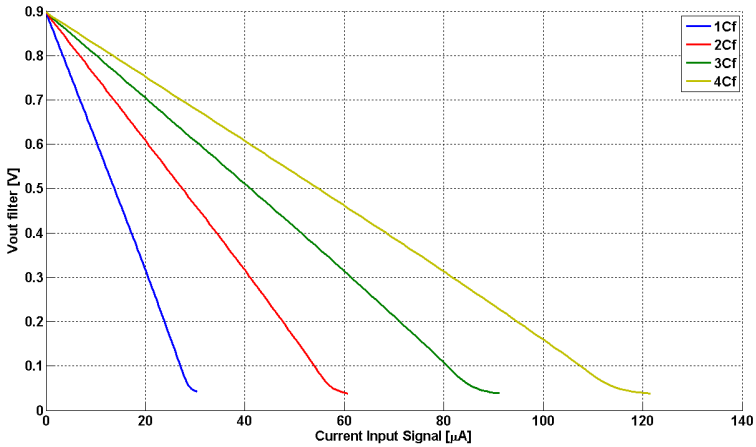

Figure 5.16 *Measured output characteristics for different numbers of feedback capacitors connected in the filter. The reference of the operational amplifier is set to 900mV.*

Obtained numbers, reported in Table 5.2, are within 4% of simulated values and scales correctly with the number of integration

capacitors. The difference in absolute values will be accounted for during calibration. For instance, it will be possible to act on the integration time and on the ADC ramp current to properly set the desired gain.

Measured gain of the FCF			
1 C_f connected–G_1	2 C_f connected–G_2	3 C_f connected–G_3	4 C_f connected–G_4
29.3kΩ	14.65kΩ	9.8kΩ	7.35kΩ
	G_2/G_1=0.501	G_3/G_1=0.335	G_4/G_1=0.251

Table 5.2 *Measured gains for different numbers of feedback capacitors connected in the filter and relative ratios.*

The system has been studied for different supply voltages around the 1.2V nominal value, to investigate the effect of non-ideal conditions on the circuit behavior. For lower voltages, the operational amplifier reference has also been changed to avoid saturation of the output node and provide the complete dynamic range of 800mV.

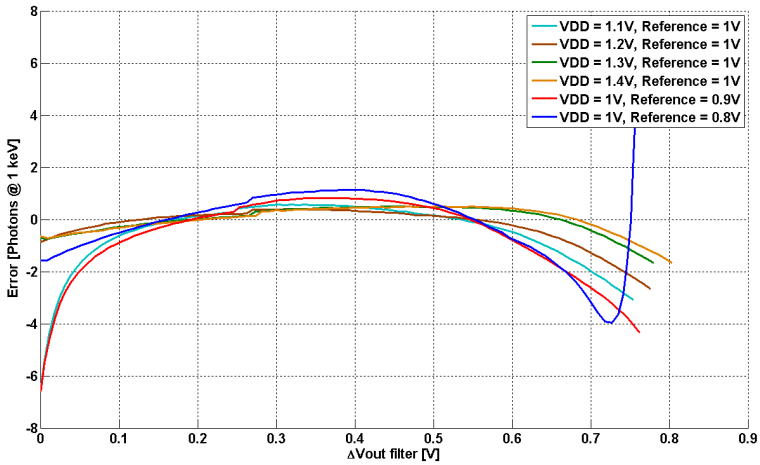

Figure 5.17 *Linearity error for different operating conditions in the filter. The fitting is done on the whole dynamic. The error is quoted in fractions of incoming photons at 1keV.*

Results are shown in Figure 5.17, where the error is quoted in fractions of incoming photons at 1keV. The circuit behaves properly if there is a difference of about 200mV between the positive voltage supply

and the reference of the operational amplifier. At the same time, in order to provide 800mV of dynamic range with a good linearity, the reference should be at least 900mV. Presently, this voltage has been fixed to 950mV to ensure good filter performance.

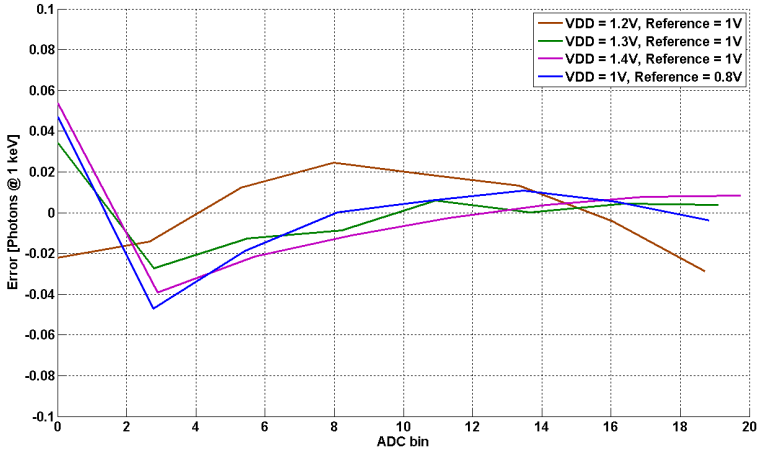

Figure 5.18 *Linearity error when the fitting is done on the initial part of the range. Only the first part of the characteristic is shown. The error is quoted in fractions of incoming photons at 1keV.*

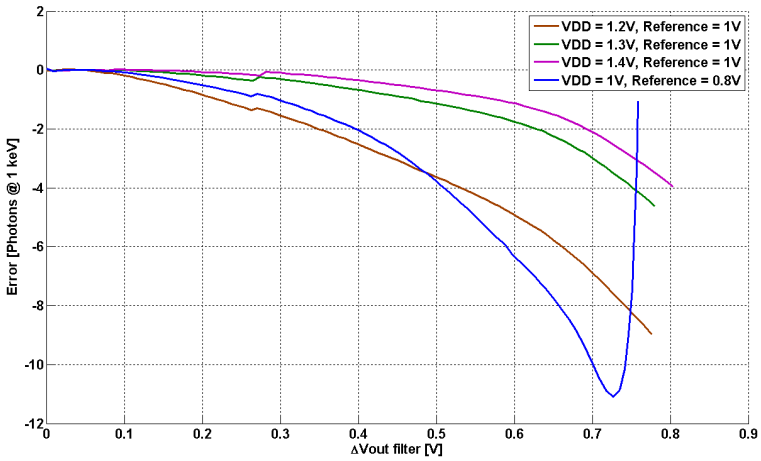

Figure 5.19 *Linearity error when the fitting is done on the initial part of the range. The complete output voltage range is shown. The error is quoted in fractions of incoming photons at 1keV.*

In Figure 5.18 and Figure 5.19 the linear fit is done only on the first part of the dynamic, to an extent corresponding to an incoming signal of about 20 photons at 1keV. These values are in agreement with the expected range of linearity for the final DSSC, where it is fundamental that no systematic errors are introduced by the filter. In the first figure the linearity in this initial range is shown, and the error is quoted in fractions of photons at 1keV versus ADC bins. The filter shows an adequate behavior, especially at the beginning of the characteristic. The non-linearity error is below 0.05 photons at 1keV, which is sufficiently low to ensure that the signal of N-absorbed photons is correctly placed within the corresponding N_{th} ADC bin on the considered range. In the second figure the error on the complete dynamic range for the same fitting curve is shown. The non-linearity error increases when moving away from the initial range on which the linearization is performed. Anyway, the impact of the non-linearity for larger signals is less critical and can be evaluated only in combination with the characteristic of the final DSSC detector.

5.7 Noise performance of the filter alone

Noise performances have been studied for various integration durations and for both timing schemes proposed. The following results refer to the case of low energy X-ray photons, when the DSSC characteristic is still linear. A detector gain of 350pA/e^- is assumed to evaluate the ENC, according to the gain measured on devices used in the tests. This value is to be compared with the expected gain of 520pA/e^- foreseen for the final DSSC devices.

Measured and expected ENC values for the double integration read out scheme are shown in Figure 5.20. The τ variable is the shaping time of the filter, corresponding to the length of each integration. The points corresponding to the operating frequencies of 4.5MHz, 2.25MHz and 0.9MHz are highlighted. The 4.5MHz operating frequency points to

two ENC values depending on the time reserved for the flattop and clearing phase.

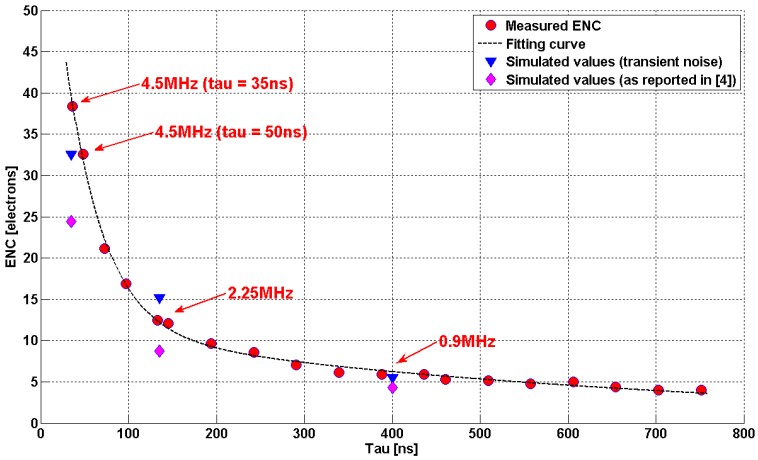

Figure 5.20 *Measured ENC values for different integration durations. The points corresponding to the operating frequencies of 4.5MHz, 2.25MHz and 0.9MHz are highlighted and compared to simulated values.*

Measured noise is reasonably consistent with the theoretical noise levels. The achieved values are from 30% to 50% worse than expected from the first design phase, which were obtained by integrating the noise spectral density. The discrepancy might be related to poorly accurate noise analysis carried out in the design phase. Simulations employing a tool that considers transient noise analysis have been carried out after these measurements and predict that the implemented filter should actually have higher noise than previously expected. Values obtained with this tool are also reported in Figure 5.20.

For the single integration read out scheme the flattop of the weighting function gets longer for the last read out cycles within the macro bunch. Consequently, flicker noise is differently filtered for the pulses, the last one being most affected. Due to limitations in the experimental setup, a maximum length of the read out phase of about 300µs can be obtained, a value that should be compared with the 600µs duration expected for a complete macro bunch in XFEL.

Measured values show that the 1/f contribution is negligible on the considered interval. Results are summarized in Table 5.3. At 4.5MHz a remarkable improvement in noise performance with regard to the double integrations read out scheme was observed, with a measured ENC of only 17 electrons. For the 0.9MHz operating frequency, with an integration of 800ns, an ENC of 5 electrons for the first cycles and of 5.4 electrons for the last ones have been obtained when connecting four feedback capacitors during the programming phase. As expected, these values get higher (9.2 and 10.1 electrons, respectively) if only one feedback capacitor is used for the sampling of the baseline.

Measured ENC for the single integration read out scheme		
	ENC–first cycles	ENC–last cycles
Frame rate=4.5MHz (τ=70ns)	18.6el	20.5el
Frame rate=0.9MHz (τ=800ns), with four C_f connected	5el	5.4el
Frame rate=0.9MHz (τ=800ns), with only one C_f connected	9.2el	10.1el

Table 5.3 *Measured noise values for the single integration read out scheme for different operating conditions. The last filtering cycles are about 300µs after the end of current programming.*

5.8 Bibliography

[1] S. Facchinetti, L. Bombelli, C. Fiorini, M. Porro, G. De Vita, F. Erdinger, “Characterization of the Flip Capacitor Filter for the XFEL-DSSC Project”, IEEE Transactions on Nuclear Science, Vol. 58, No. 4, August 2011.

[2] S. Facchinetti, L. Bombelli, A. Castoldi, C. Fiorini, C. Guazzoni, D. Mezza, M. Porro, G. De Vita, F. Erdinger, “Fast, low-noise, low-power electronics for the analog readout of non-linear DEPFET pixels”, 2011 IEEE Nuclear Science Symposium Conference Record, pp. 1846-1851.

CHAPTER 6

Measurements with a detector

6.1 Measurements with a radioactive source

The behaviour of the filter has been tested with standard DEPFETs and a ^{55}Fe radioactive source. A 4x4 detector array was used, with each pixel having dimensions of 75x75µm^2 (Figure 6.1). One detector was connected to the analog filter to process the signal. The detector arrays were wire bonded to ceramic boards, and one was inserted onto the PCB that hosts the filter chip.

Since the radioactive source is not synchronous with the ASIC operation, as it will be in XFEL, the read out timing scheme was changed

and the phase ordering of each cycle was rearranged as shown in Figure 6.2, similar to the timing scheme of the VELA ASIC.

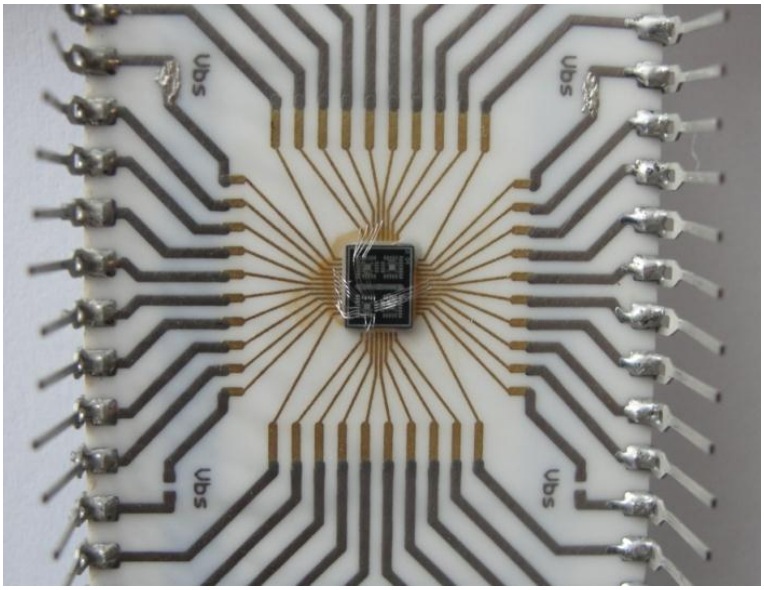

Figure 6.1 *Picture of the DEPFET chip. It comprises four detector arrays of 4x4 pixels each. The die is mounted on a ceramic and one of the four available structures is wire bonded.*

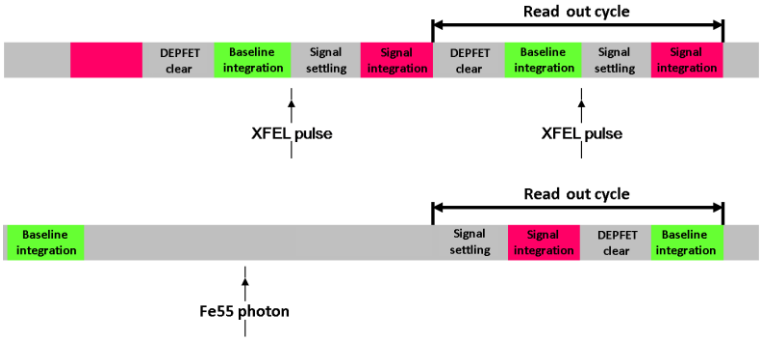

Figure 6.2 *Timing scheme of XFEL (top) and the one employed for the acquisition of ^{55}Fe spectra with a single pixel DEPFET (bottom).*

Photons are collected in the first phase, which has to be longer than the trapezoidal filter duration to increase the probability of photon

absorption given the low emission rate of the source. Two integrations were performed with a clear operation phase in between. The first integration was devoted to the signal read out, and the second one to the measure of the baseline. In this configuration the signal polarity is the opposite of that expected for XFEL. However, the low energy of ^{55}Fe photons avoids the possibility of saturating the output. The XFEL timing scheme was also tested, thus placing the clear phase at the beginning of the read out cycle with the anticipated duration for the corresponding operating frequency. In this case the probability that a photon is absorbed in the correct interval is so low that acquired spectra show only the noise peak, making the calibration not possible. In any case, to validate obtained results with the VELA timing scheme the noise peaks acquired with the XFEL sequence have been evaluated, using the conversion gains obtained with the VELA timing scheme. Comparable ENC values were obtained, thus confirming the validity of the results presented.

One of the main difficulties when operating at high frequencies is to obtain a sufficiently fast clearing of the detector. For this purpose the DG419 analog multiplexers from Maxim were used. However, switching the electrodes with the necessary voltage swing of 20V requires about 300ns to properly set all the voltages in the detector. Therefore, a longer time than expected was dedicated for the clear phase in the measurements, but this does not affect noise evaluation since the white noise dominant contribution depends only on integration time, which was kept constant with respect to the corresponding operating frequencies.

Small detector area makes the contribution of photons absorbed on the detector borders quite relevant. Their energy is split between neighbouring pixels, giving rise to a low energy tail in the peaks. To reduce the effect of splitting events the detector was illuminated from the front side; in this way, charge is generated closer to the IG and the probability of energy splitting between pixels is lowered. In fact, after generation the shape of the charge distribution is a disk in the drift direction with a growing radius because of the radial diffusion [1]. As a consequence, broadening of the charge distribution is proportional to the time needed to reach the IG and hence to the depth of ionization.

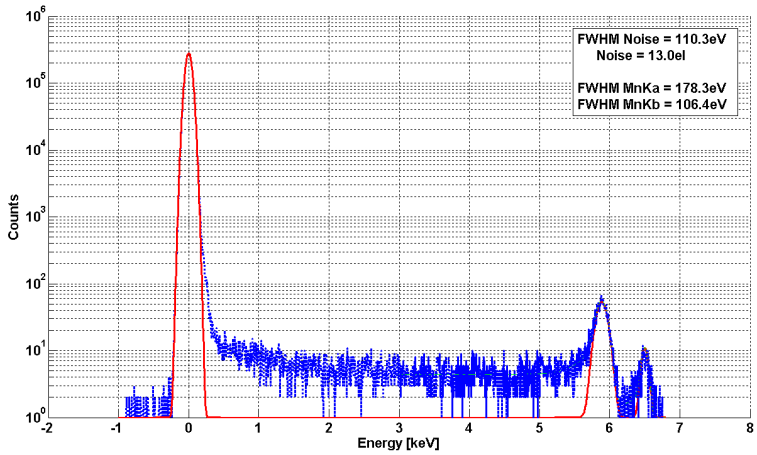

Figure 6.3 *Measured ^{55}Fe spectrum with the FCF and a standard type DEPFET for the operating frequency of 0.9MHz. Two correlated measurements were performed.*

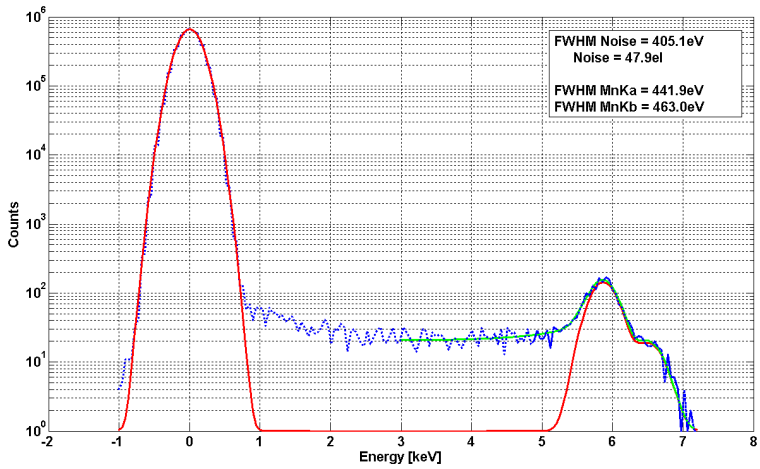

Figure 6.4 *Measured ^{55}Fe spectrum with the FCF and a standard type DEPFET for the operating frequency of 4.5MHz. Two correlated measurements were performed also in this case.*

Two different detector prototypes were used and gave similar results. Measured gain of the employed DEPFETs is 350pA/e$^-$. This is the value initially foreseen also for the final DSSC devices. As an example, in Figure 6.3 the measured spectrum for the operating frequency of

0.9MHz using the double integration read out scheme is shown. From the fitting of the baseline peak an ENC value of 13 electrons is extracted. This is related to the electronic noise only. For the K_α peak an ENC of 15 electrons is obtained by removing the Fano statistics contribution of 119eV. These values are absolutely adequate for single photon counting at 0.9MHz and must be compared with the expected value of 11.6 electrons from simulations. The measured spectrum at 4.5MHz is shown in Figure 6.4. An electronic noise of 48 and 50 electrons is extracted from the noise and K_α peak, respectively, with an integration time of 50ns. From simulations a value of 42 electrons with an integration time of 40ns was expected (see Table 4.5). The noise for different integration times and the double integration read out scheme is shown in Figure 6.5.

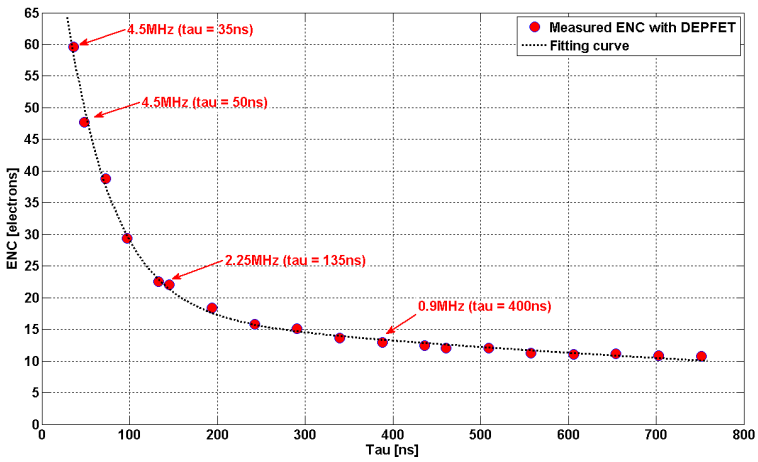

Figure 6.5 *Measured ENC values with the detector for different integration durations and double integration read out scheme.*

The single integration solution has also been tested with the detector, giving an ENC of 34 electrons at the maximum frequency of 4.5MHz, with an integration time of 70ns. The measured spectrum is shown in Figure 6.6. The results obtained for what concerns the ENC are summarized in Table 6.1 in which a comparison between expected values and measured ones is reported. In the lower part of the Table the total noise values are taken from spectra previously presented. The noise contributions of the circuit are the ones obtained with the circuit alone,

scaled accordingly to consider the DEPFET gain of 350pA/e$^-$. Detector noise is then extracted from the total and circuit contributions. As it can be noticed, measured performances are very close to what expected, even for the maximum operating frequency of 4.5MHz.

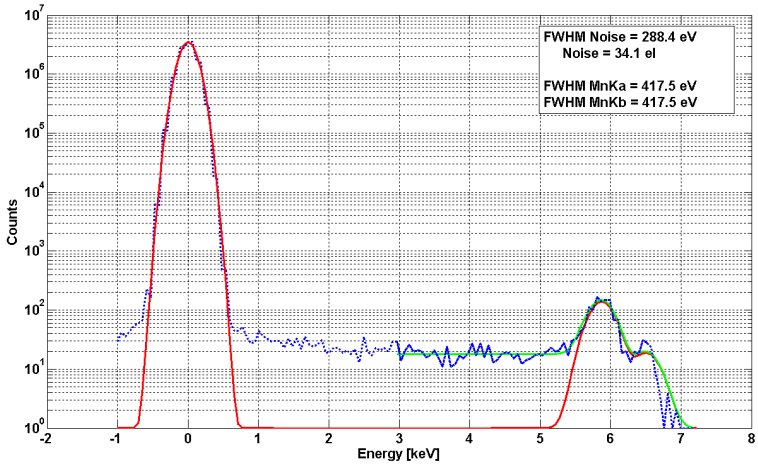

Figure 6.6 *Measured spectrum of ^{55}Fe with the FCF and a standard type DEPFET for an operating frequency of 4.5MHz and single integration read out scheme.*

Expected noise values					
4.5MHz (τ=40ns)		0.9MHz (τ=400ns)		4.5MHz (τ=80ns), single integration	
DEPFET	32el$^-$	DEPFET	10.3el$^-$	DEPFET	22.8el$^-$
FCF circuit	25.3el$^-$	FCF circuit	5.3el$^-$	FCF circuit	14.8el$^-$
Total	**42el$^-$**	Total	**11.6el$^-$**	Total	**27.2el$^-$**
Measured noise values					
4.5MHz (τ=50ns)		0.9MHz (τ=400ns)		4.5MHz (τ=70ns), single integration	
DEPFET	35el$^-$	DEPFET	11.2el$^-$	DEPFET	29.8el$^-$
FCF circuit	32.6el$^-$	FCF circuit	6el$^-$	FCF circuit	16.3el$^-$
Total	**48el$^-$**	Total	**13el$^-$**	Total	**34el$^-$**

Table 6.1 *Comparison between expected (top part) and measured (bottom part) noise values.*

6.2 Measurements with a laser setup

The FCF front end connected to a DEPFET has also been tested with a laser test suite (Figure 6.7). The setup features an x-y mechanical movement section with micrometer positioning capabilities and a fast infrared pulsed laser having a FWHM of less than 100ps, able to generate the desired signal charge. An optical axis that allows beam splitting is also included to both focus the infrared laser pulse and visualize the laser spot on the detector surface with a video camera. The laser driving system allows for repetition rates up to 80MHz, thus matching the requirements of speed to test the FCF in an XFEL-like time structure. The laser intensity can be adjusted to deliver pulses with energies up to 40pJ which is well suited to simulate a wide dynamic range of intensities, including the expected level from the future European XFEL.

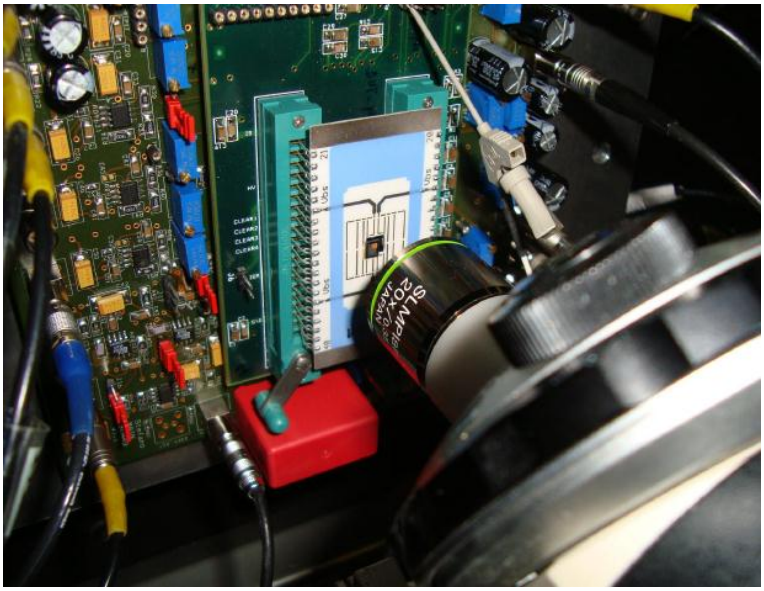

Figure 6.7 *Picture of the laser test setup used to characterize the FCF in conjunction with a detector and employing light pulses synchronous with the filter operation. The DEPFET ceramic is visible in the center of the image.*

Infrared pulses can well simulate the effects of X-ray ionization. In fact, the carrier density profile inside the bulk produced by the laser can be quite similar to the ionization profile generated by X-rays. The wavelength of the employed laser head is 905nm (+/-10nm) which assures an absorption length in silicon of about 30µm at room temperature. The standard deviation of the Gaussian function describing the laser spot diameter is less than 10µm FWHM, a value that has to be compared with the 75µm side length of a single DEPFET pixel.

6.2.1 Weighting functions

The laser setup allows injecting charge into the detector at well-defined times so that for instance weighting functions of sensor signals can be determined. This was not possible during spectral measurements, where an asynchronous radioactive source was used.

The measured weighting functions for the double integration read out scheme are shown in Figure 6.8. For the 4.5MHz operating frequency the flattop lasts 65ns, whereas for both slower operations (2.25MHz and 0.9MHz) the flattop has been set to 100ns. These measurements nicely confirm previous results obtained by electronic injection of the front end alone.

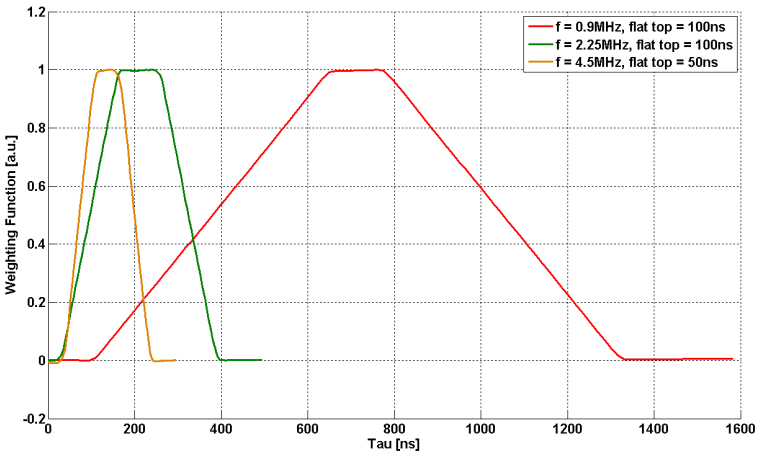

Figure 6.8 *Measured weighting functions for the double integration read out scheme for different operating frequencies.*

For the single integration read out scheme the behaviour is different depending on the clear timing of the DEPFET. Consider a pulse that arrives during the programming phase and that is converted in a current step by the detector: the corresponding change in DEPFET bias current is then stored in the current generator. If a clearing is done before signal integration, a mismatch between the DEPFET current and that of the generator is introduced. This is seen as a negative baseline by the filter. Moreover, any pulse arriving between the end of the programming phase and the clear gives no effect on the output, since the charge generated is cancelled before signal integration. Finally, any pulse arriving after the clear phase gives maximum output until it enters the signal integration. As a result, the weighting function behaviour presented in Figure 6.9 is obtained.

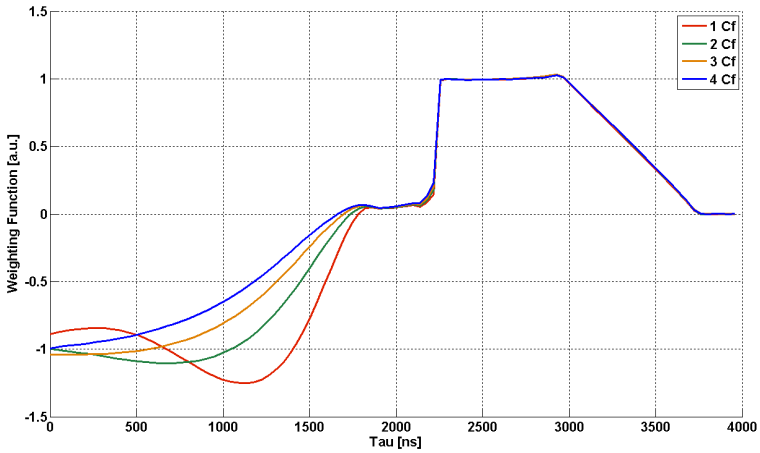

Figure 6.9 *Measured weighting functions for the single integration read out scheme. A clear phase is present before signal integration.*

A different behaviour is obtained if no clear is provided between the pulse arrival and the signal integration. In this case if a pulse arrives during the programming phase, the corresponding increase in DEPFET current lasts for the whole measurement. Since it is compensated by the current generator it gives no effect on the output. This leads to the weighting functions shown in Figure 6.10, which corresponds to previous results obtained when pulsing the filter alone.

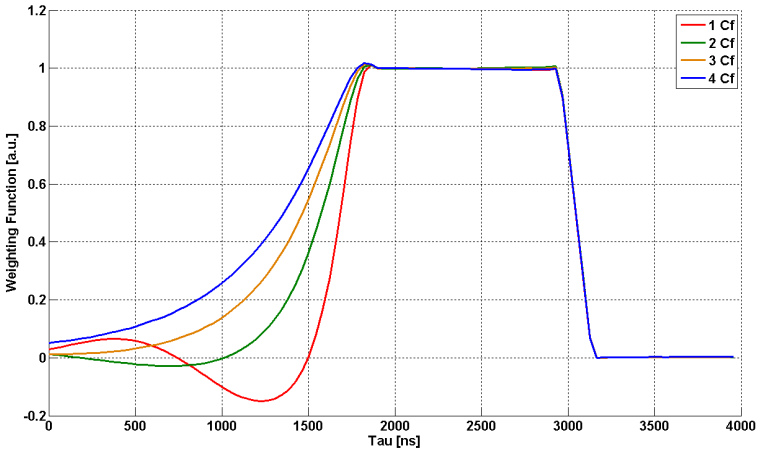

Figure 6.10 *Measured weighting functions for the single integration read out scheme. In this case there is no clear phase between the end of the programming phase and the signal integration.*

Both situations are significant to evaluate the performances of the circuit. The former weighting function applies to noise sources that are affected by the periodic clear of the detector, i.e. the parallel noise. The latter applies to noise sources that are not affected by the removal of charges from the internal gate, i.e. the white noise that is determined by the properties of the external FET structure.

6.2.2 Long flattop

The effect of a long flattop in the weighting function has been investigated. In Figure 6.11 three different measurements with identical settings of a very long flattop of 144µs are shown. The vertical scale is strongly zoomed around unity. No deterministic behaviour like a constant decrease is observed along the flattop which stays within 2% of the maximum value for the whole duration. The deviations can be attributed to noise in the output signal and fluctuations of the intensity of light pulses.

This measurement demonstrates that very long flattops can be achieved, for instance for source testing. The gain of the filter with different lengths of the flattop has also been measured and found to be in

agreement with previous results. This analysis is important for the calibration phase, since a sufficiently long flattop would allow the use of an asynchronous radioactive source to determine the gain of the complete chain, starting from the detector, avoiding the need of laser sources (which output energy is known with insufficient precision) or the need to modify the filter functioning.

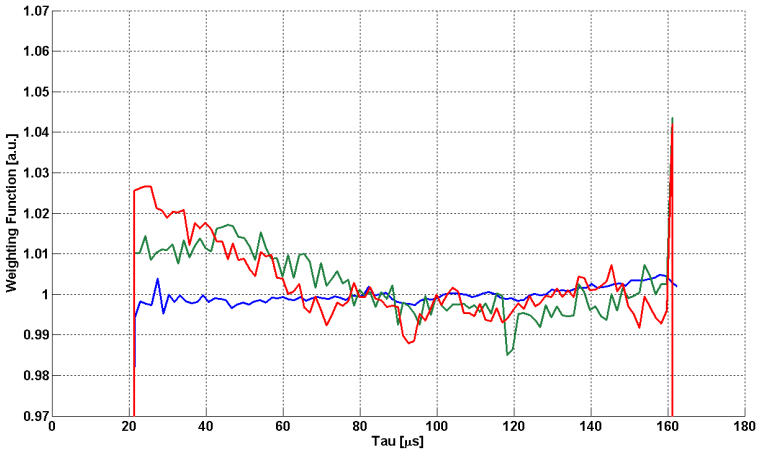

Figure 6.11 *Measurements of a 144µs long flattop. The three curves were obtained repeating the acquisition with the same settings for statistical purposes. The vertical scale is strongly zoomed around unity.*

6.3 Bibliography

[1] E. Gatti, A. Longoni, P. Rehak, M. Sampietro, “Dynamics of electrons in drift detectors”, Nucl. Instrum. Methods Phys. Res. A, vol. 253, pp. 393-399, 1987.

CHAPTER 7

Measurements on the 8x8 prototypes

7.1 ASIC description and test setup

The MM1 and MM2 matrix chips contain an array of 8x8 pixels with some additional global control circuits [1]. This includes the gray code counter, differential buffers, a digital sequencer for timing signal generation and analog monitoring buffers. They represent a small version of the final DSSC read out ASIC with close to final layer assignments, power and control signal distribution. The die size is 2.5x3.2mm^2 with about 100 wire pads. A full speed clock of 800MHz is used. Power consumption is as expected.

The MM2 pixels contain also an injection circuit to characterize the system without detector (Figure 7.1), designed by the University of Bergamo and to be included also in the final DSSC pixels [2]. The pulse amplitude can be selected by writing into an 8-bit current steering DAC located in the chip periphery. The current is then mirrored in each pixel where a pulser circuit generates the desired signal and feeds it directly into the input of the detector read out. The signal current source injects a current into the drain of the input cascode, while the bias current source emulates the detector bias. The latter can be disabled after mounting the DSSC chip onto the sensor.

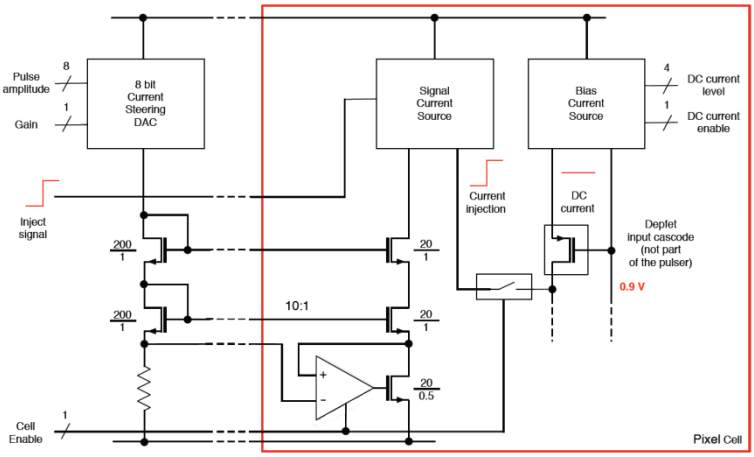

Figure 7.1 *Architecture of the injection circuit included in the ASICs. The same four bits provided to the programmable current source in the FCF are sent to the DAC which generates the DC bias current level emulating the one drawn by the block in the filter.*

In the MM1 chip both the source follower and the drain read out front ends are implemented, along with a double buffering S&H, the ADC with differential receivers and a dynamic RAM array. A pixel control register is used to set the various configuration bits. A serial read out of the ADC bypassing the RAM is also possible. Figure 7.2 shows the layout of the chip realized by the group of the University of Heidelberg. The power and time stamp busses use a snake pattern to mimic a full length column of the final chip of 64x64 pixels.

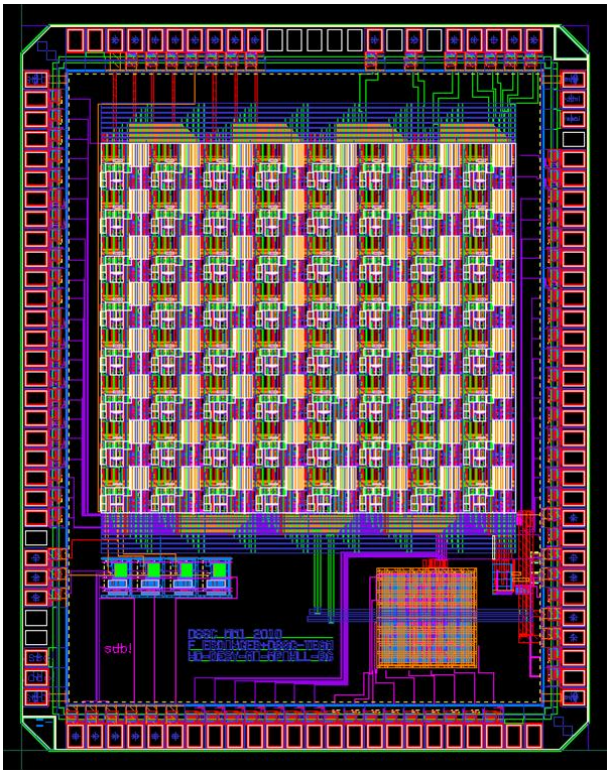

Figure 7.2 *Layout of the MM1 ASIC with 8x8 full pixels.*

The second matrix chip includes optimized building blocks, with the addition of LVDS IO pads that are not present in MM1. Only the FCF is implemented, with a static memory that can store 640 words. The layout of the complete chip is similar to that of MM1. In Figure 7.3 the organization of the various DSSC blocks in each pixel is shown. Even though all blocks already fit in the MM2 pixel, for the 64x64 matrix the area occupancy of all blocks will be reduced even more and free space will be filled with further SRAM rows and decoupling capacitors.

A large effort has been made to minimize crosstalk and voltage drops in the MM chips. This includes, but are not limited to, significant routing resources reserved for power, reduction and nearly constant consumption of pixels during operation, voltage drop insensitivity using

local references, shielding, differential signal transmission and significant in-pixel decoupling.

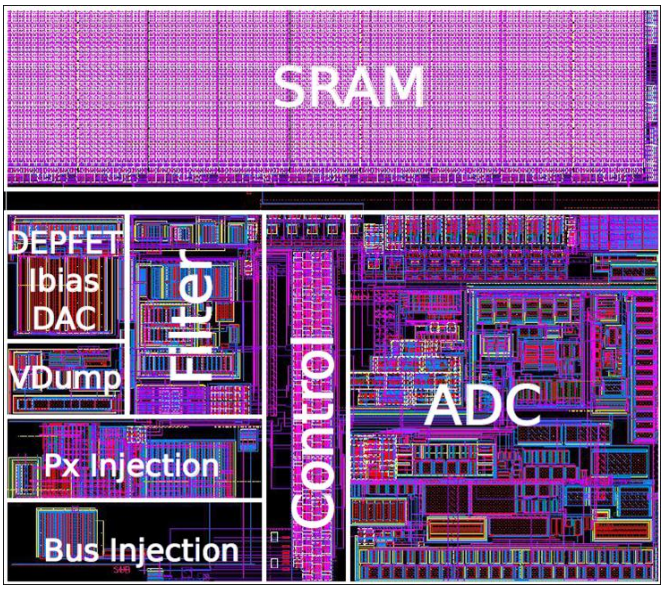

Figure 7.3 *Single pixel layout in the MM2 ASIC. This is very close to the final DSSC pixel layout.*

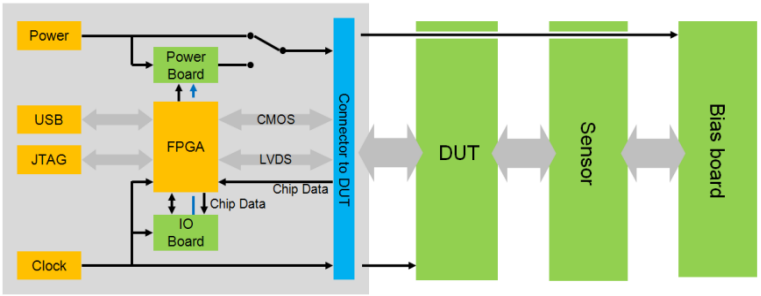

Figure 7.4 *Sketch of the test setup developed for the DSSC matrices.*

To test the DSSC matrix chips, including both the small 8x8 ASICs and also the future full matrices, a compact and versatile system has been design and manufactured (Figure 7.4). The system provides add-on connectors which allow for power cycling of the matrices using the DSSC power board and data read out at full speed. A device-under-test

board for the mini-matrices in combination with DEPFETs on ceramic carriers is used. A bias board has been designed and realized to easily program most analog supply and bias voltages required by the detector and allow for simple automated measurements (Figure 7.5).

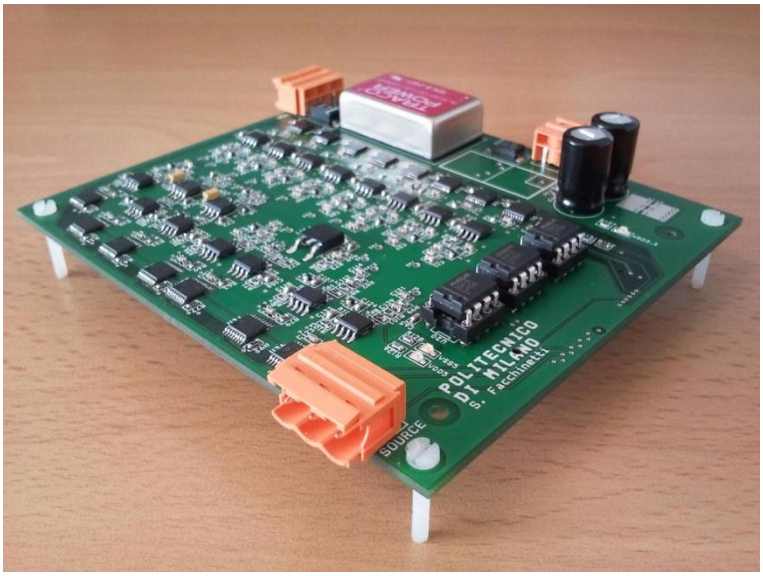

Figure 7.5 *Picture of the bias board developed for the DSSC test setup. The board is able to provide all the voltages needed by the detector and is programmed via FPGA and dedicated software.*

7.2 FCF characterization in the MM chips

Measurements on the programmable current generator provide similar results as with the FCF chip. Inside MM1 the first proposed solution with a 4-bit DAC and an external voltage is implemented (see Figure 4.34). Figure 7.6 shows the measured characteristic for MM1 with the nominal VSSS voltage of -3V. The programmable current range goes from about 5µA up to 150µA, matching very well the results obtained on the FCF ASIC within experimental dispersion.

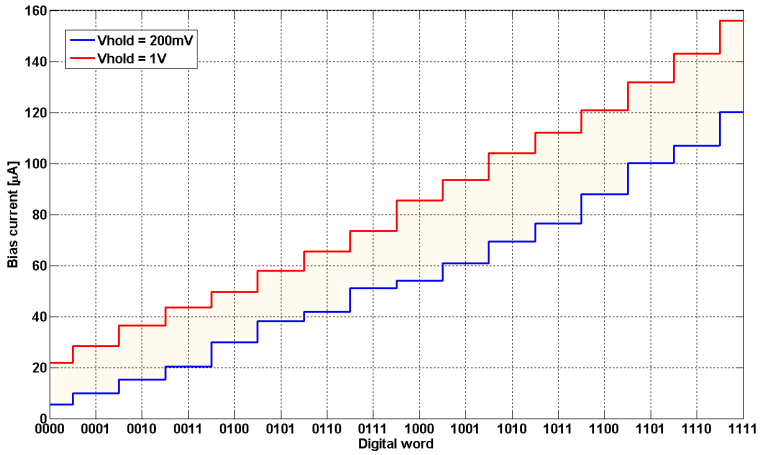

Figure 7.6 *Measured values for the current drawn by the programmable current source in MM1 for the minimum (0.2V) and maximum (1V) voltages at the control gate and for different binary codes applied for the coarse regulation. VSSS is set to -3V. The shadowed area represents the coverable detector biasing.*

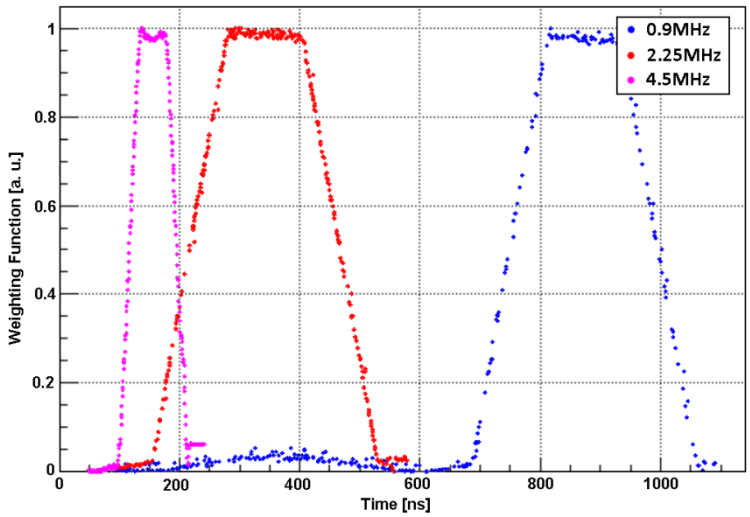

Figure 7.7 *Measured weighting functions with MM1 for the double integration read out scheme and for different operating frequencies.*

Measured weighting functions with the MM1 ASIC are shown in Figure 7.7 for different operating frequencies. The curves are obtained by

applying a voltage step on an internal resistor at various points in time during the read out cycle. A small offset between final and initial values is visible, recalling what already measured with the FCF chip.

The gain of the filter for all pixels has been extracted to evaluate the dispersion across the matrix. An external resistor has been used to allow for higher voltage steps than in the weighting functions measurements. Figure 7.8 shows the gain for four feedback capacitors divided by the gain for one, two and three feedback capacitors. The values have been measured using the internal ADC, so that the complete readout chain is evaluated. The standard deviation is about 0.7% for all three cases, and average values are within 1% of the measured values on the FCF ASIC.

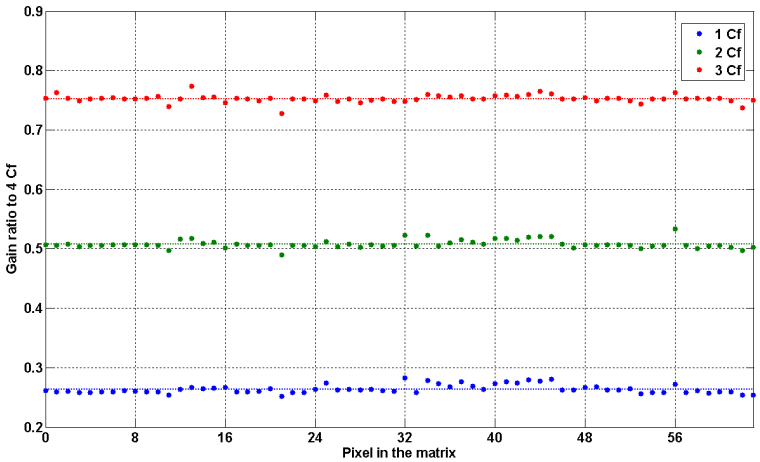

Figure 7.8 *Gain of the FCF inside MM2 for every pixel in the matrix. The value of the gain using four feedback capacitors is normalized to the values of the gain when one, two and three capacitors are connected in the filter. The mean value for each case is also shown (dashed lines).*

The noise of the FCF and of the ADC has been measured in MM1 by sending a signal current of 0.5μA into the front end through a resistor. The amplitude of the signal roughly corresponds to the signal from a ^{55}Fe radioactive source with the initially expected gain of 350pA/e^{-} for the detector. Figure 7.9 shows a measurement carried out

with a 250ns integration time and one feedback capacitor, i.e. with high gain. The noise is 0.4 ADC bins, which corresponds to about 13 electrons. This value should be compared to the about 9 electrons obtained with the FCF alone (see Figure 5.20).

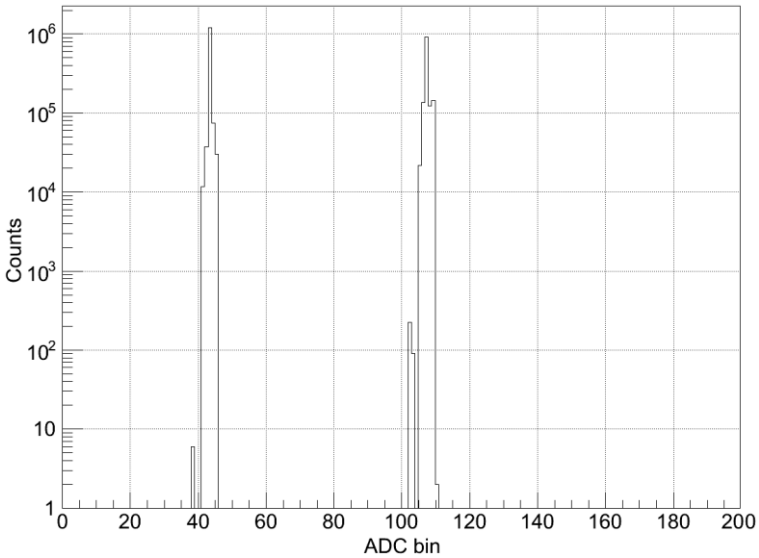

Figure 7.9 *Noise histograms measured with the pixel ADC of a MM1 pixel for no input signal and 500nA input current. One feedback capacitor is used in this measurement carried out at 1MHz rate.*

7.3 Measurements with a detector

Spectroscopic measurements with the full pixel in the MM1 ASIC have been carried out using a linear DEPFET and an ^{55}Fe source for calibration, as for the FCF ASIC. The detector area of 75x75μm^2 is also the same. A long flattop of 10μs was used to increase the probability of photon collection. As an example, Figure 7.10 shows a spectrum taken with the last pixel of the matrix with an integration time of 250ns. The width of the noise peak is 0.43 ADU which corresponds to about 14.4 electrons. This matches very well to the noise value of 15 electrons

measured with the FCF setup. Missing codes in the ADC are due to the routing of the transmission lines in the ASIC.

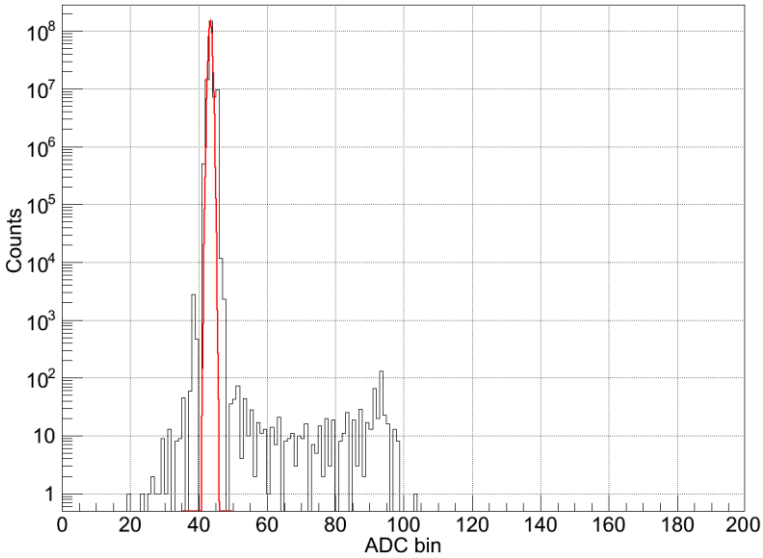

Figure 7.10 *Spectrum of a ^{55}Fe radioactive source measured using the MM1 ADC. The width of the pedestal peak is about 14.4 electrons.*

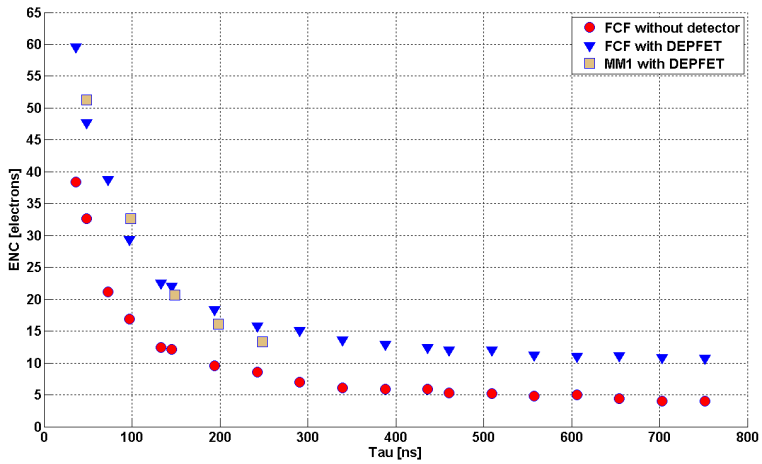

Figure 7.11 *Measured ENC values for different integration durations. Measured values with the MM1 chip are very close to the numbers obtained with the FCF ASIC.*

Measured noise values for various integration times are shown in Figure 7.11, where also the values obtained with the FCF ASIC are reported. Obtained values for the two cases are very close, showing that it is possible to obtain a very low noise at high frame rates even with the complete DSSC read out pixel.

Finally, Figure 7.12 shows the first characteristic obtained with a non-linear detector and the complete read out chain, including the analog front end and ADC. The signal was provided by pulsing one of the rings of the DSSC structure. The curve nicely resembles the shapes obtained testing the detector alone, demonstrating the correct operation of the complete DSSC read out chain.

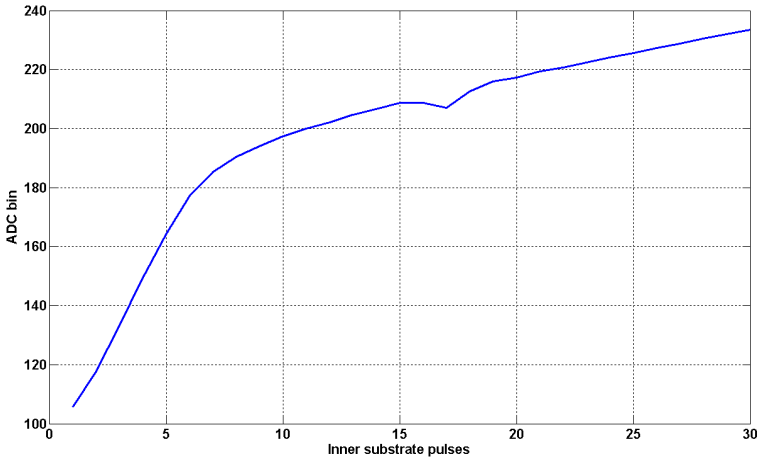

Figure 7.12 *Non-linear characteristic obtained using one of the first non-linear DEPFET devices along with the MM2 ASIC array.*

7.4 Bibliography

[1] F. Erdinger, L. Bombelli, D. Comotti, S. Facchinetti, P. Fischer, K. Hansen, P. Kalavakuru, M. Kirchgessner, M. Manghisoni, M. Porro, E. Quartieri, C. Reckleben, J. Soldat, J. Szymanski, "The DSSC pixel readout ASIC with amplitude digitization and local storage for DEPFET sensor matrices at the European XFEL", 2012 IEEE Nuclear Science Symposium Conference Record, N4-8.

[2] E. Quartieri, M. Manghisoni, "Performance of a High Accuracy Injection Circuit for in-Pixel Calibration of a Large Sensor Matrix", 2011 IEEE Nuclear Science Symposium Conference Record, pp. 677-681.

Discussion and conclusions

In this Doctoral dissertation the design, realization and testing of a novel filter architecture has been discussed. The compliance of the Flip Capacitor Filter (FCF) solution to the DSSC project requirements has been demonstrated through both analytical evaluation and experimental characterization. The circuit takes advantage of the current read out technique to avoid long settling times associated with stray capacitances at the detector output. It is able to provide a trapezoidal shaping with variable gain even at the shortest processing time foreseen of 200ns. A single operational amplifier is used to realize two correlated integrations and take their difference by flipping the feedback capacitor between the two measurements. The gain can be regulated by acting on the integration time and the number of feedback capacitors.

Even though previous works based on the current read out principle are available the tight requirements of the DSSC project mandated the development of a new solution. In its final version the FCF circuit, developed in the IBM 130nm CMOS technology, occupies a very small area of 88x84μm^2. This corresponds to less than 20% of the total DSSC pixel area. Power consumption is limited to about 0.35mW per channel, but still the filter is able to correctly process large current signals comparable to its total current consumption. This result has been obtained by implementing the operational amplifier in the main integrator stage such that it can increase its current capability when needed. Also the reset

phase has been carefully studied to obtain a very fast recovery of the system after signal integration. A dedicated switch inside the amplifier architecture is placed to short circuit the compensation capacitor, avoiding the circuit from going in slew rate conditions.

The bias component of the detector current is removed by a dedicated current generator to maximize the filter dynamic range. This block is programmable to withstand threshold shifts in the detector after irradiation and mismatches in the DSSC matrix. Two different versions of the current generator have been designed, according to the specifications on the DSSC gain. Both structures are based on 4 bits DAC architectures with pixel wise settings that provide a coarse regulation of the current. Fine matching is obtained by setting the voltage in the active branches by means of a closed loop configuration that is operated before the X-rays burst. In this programming phase the filter is used as an error amplifier. Measurements on the first version of the FCF have demonstrated the capability of the current generator to cope with very large current variations, from a few μA to about 150μA. The new version, that has been implemented in the last mini matrix chip and will be used in the final DSSC pixel, will provide the same current range with the advantage of a simpler architecture, capitalizing on the higher gain foreseen for the detector.

Measurements on all realized prototypes, both for the FCF alone and within the complete DSSC pixel, have proven the correctness of the proposed solution. For instance, by careful design of the feedback networks and by regulating the digital signals transitions no charge loss has been noticed due to the flipping phase. Weighting functions are very close to an ideal trapezoidal shape even for short processing times. Linearity is sufficiently good to ensure that the first collected photons are placed in the middle of the first ADC bins. Spectroscopic measurements using an iron source and a standard type linear detector have been done and gave results very close to expectations. The FCF connected to the DEPFET has also been tested with a pulsed laser, to replicate the foreseen operating speed of the future European XFEL. The circuit was able to

work at the maximum frame rate foreseen, and weighting functions similar to that obtained on the FCF alone have been measured.

In particular, the capability to filter the signal with low noise implementing two correlated integrations in a processing time of only 220ns has been successfully demonstrated. For instance, a total of less than 50 electrons has been obtained for the filter connected to a standard type, linear DEPFET with an integration time of 50ns.

Initially, a current and a voltage read out filters have been studied and implemented in the MM1 chip. After measurements on both circuits' prototypes and on the mini matrix chip the DSSC collaboration has decided to focus on the FCF solution with its better noise performance, lower power dissipation and simplified sensor design. This decision confirmed the adequacy and quality of the proposed filter architecture.

A common test system has been set up by the collaboration which allows for characterization of test chips, mini matrices and later full size pixel chips. The boards provide add-on connectors which will allow for power cycling of the matrices using the DSSC power board and data read out at full speed. A bias board allows easy programming of most analog supplies and bias voltages required by the detector for simple automated measurements. The FCF performances in the complete DSSC pixel match very well what obtained on the dedicated chip submission. The noise of the complete system, from the detector to the ADC, has been determined with a ^{55}Fe source for gain calibration. Obtained values are consistent with the noise of the FCF alone and match very well the DSSC goals.

All building blocks, including the FCF, are now very close to their final form. Also the pixel layout of the MM2 ASIC is representative of the final blocks organization, and it anticipates a large matrix for what concerns the supply routing and the transmission lines organization. The submission of the first 64x64 DSSC pixels matrix with bump bond pads is foreseen for the beginning of 2013.