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Nanopatterning for Light Trapping in Thin Film Crystalline Silicon Solar Cells

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Abstract

The increasing demand of crystalline silicon based Photovoltaics as a leading technology in the electrical power generation industry has brought research to face several challenges related to the need to go to cost effective technologies that still do not neglect the performances. Because of the costs related to the active material, thin film technology has been proposed. Nevertheless, several issues related to optical losses arise when considering low thicknesses for the active material and conventional light trapping methods seems to be not compatible due to the total material consumption.

In this work, the idea of a sub wavelength-scale patterning on thin film silicon surface, in order to reduce front side reflectance and increase light trapping inside the bulk with low material consumption, will be presented by means of two different technologies: hole-mask colloidal lithography and nano-imprint lithography.

Hole-mask colloidal lithography is a technique that utilizes random dispersion of colloidal particles, on silicon surface, to define the pattern. This work will be focused on the absorption enhancement provided by such technology.

Nano-imprint lithography consists of transferring a pattern from a prefabricated stamp to the silicon surface by means of a mechanical press. In this work optical result will be presented, together with cell results. The deteriorating effect on carrier lifetime will be analyzed and different solution to that issue will be proposed.

Sommario

L'aumento progressivo della domanda di moduli fotovoltaici in silicio monocristallino, oggi tecnologia di punta nel campo dell'industria per la produzione di energia elettrica, ha posto la ricerca di fronte a importanti sfide in relazione al bisogno di sviluppare tecnologie che garantiscano da un lato costi sostenibili e dall'altro ottime prestazioni. Per ragioni legate al costo del materiale attivo, è stato intrapreso lo sviluppo della tecnologia a film sottile. Ciononostante, nel momento in cui si considerano spessori minimi per il materiale attivo, vengono riscontrati parecchi inconvenienti riguardanti le perdite ottiche e sembra che i metodi convenzionali di intrappolamento della luce non siano compatibili a causa del consumo eccessivo del materiale.

Il progetto in questione intende investigare un modello della superficie del film sottile su silicio su scala di dimensioni inferiori alle lunghezze d'onda del visibile, al fine di ridurre la riflettanza all'interfaccia e aumentare l'efficienza di cattura della luce nel substrato con relativo basso consumo del materiale. Questa idea di modello sarà presentata per mezzo di due differenti tecnologie: hole-mask colloidal lithography e nano-imprint lithography.

Hole-mask colloidal lithography è una tecnica litografica che consiste nella dispersione casuale di particelle colloidali in soluzione sulla superficie del silicio, la deposizione di un film sottile di una maschera di allumino, rimozione delle particelle colloidali e la rimozione di materiale attivo attraverso le forature sulla maschera mediante il reactive ion etching.

Nano-imprint lithography, consiste nel trasferimento di un reticolo di diffrazione da uno stampo prefabbricato sulla superficie del silicio attraverso una deformazione meccanica: la superficie del silicio viene inizialmente coperta con un resist termoplastico, lo stampo viene quindi pressato sul silicio

attraverso uno strumento meccanico ed infine il silicio viene rimosso mediante il reactive ion etching.

Riepilogo

Il lavoro si focalizza sulla necessità di trovare soluzioni tecnologiche per far fronte al problema del basso assorbimento della radiazione solare da parte di celle fotovoltaiche su silicio mono-cristallino a film sottile. Le ridotte dimensioni del materiale attivo, in queste celle, compromettono in modo significativo l'efficienza di conversione dei dispositivi: la corrente foto-generata, prodotta da queste celle, mostra valori significativamente più bassi rispetto a celle convenzionali con spessori maggiori. Diventa quindi essenziale integrare nelle suddette celle strutture che permettano di intrappolare nel substrato la radiazione incidente.

Le convenzionali tecniche di intrappolamento consistono in lavorazioni superficiali in modo da ottenere strutture piramidali; tali strutture permettono un accoppiamento obliquo delle onde nel materiale. Le tecniche si basano dunque sui principi di ottica geometrica e cercano di sfruttare al meglio la legge secondo la quale al di sopra di un dato angolo critico, si ottiene riflessione interna totale.

Le tecniche sopracitate sono ampiamente utilizzate nel settore del fotovoltaico e grazie ad esse sono state prodotte le celle con maggiore efficienza. Tuttavia la realizzazione delle strutture piramidali è del tutto incompatibile con celle a film sottile a causa dell'eccessivo consumo di materiale attivo. In questa relazione vengono proposte e ampiamente descritte due tecniche che permettono di ottenere strutture superficiali di dimensioni nanometriche, precisamente, dello stesso ordine di grandezza della lunghezza d'onda dello spettro del visibile, mediante l'uso di cristalli fotonici. Con strutture di dimensioni paragonabili alla lunghezza d'onda della radiazione incidente una descrizione

geometrica non è più valida, bisogna invece considerare gli effetti diffrattivi. Si dimostra nell'elaborato che le strutture introdotte permettono di ottenere valori di assorbimento paragonabili ai valori ottenuti nelle celle convenzionali. Il miglioramento delle prestazioni rispetto al caso di silicio non lavorato è causato dagli effetti diffrattivi e della variazione graduale dell'indice di rifrazione vista dall'onda incidente.

La prima tecnica, hole-mask colloidal lithography, è una tecnica litografica che consiste nella dispersione casuale di particelle colloidali in soluzione sulla superficie del silicio, la deposizione di un film sottile di una maschera di allumino, rimozione delle particelle colloidali e la rimozione di materiale attivo attraverso le forature sulla maschera mediante il reactive ion etching. Il risultato finale, ottenuto con un conclusivo processo di rimozione della maschera, consiste in una struttura che presenta una disposizione casuale di scanalature piramidali che mantengono comunque una distanza fissa tra i centri. Le scanalature hanno dimensioni laterali e in profondità inferiori al micron, di conseguenza la quantità di materiale attivo consumato è compatibile con dimensioni di film fino a 1 micron di spessore.

La seconda tecnica, nano-imprint lithography, consiste nel trasferimento di un reticolo di diffrazione da uno stampo prefabbricato sulla superficie del silicio attraverso una deformazione meccanica: la superficie del silicio viene inizialmente coperta con un resist termoplastico, lo stampo viene quindi pressato sul silicio attraverso uno strumento meccanico ed infine il silicio viene rimosso mediante il reactive ion etching. La tecnica consente di ottenere strutture che presentano un forte intrappolamento della luce con un conseguente aumento dell'assorbimento nel materiale attivo. Tuttavia, il bombardamento ionico caratteristico della tecnica di rimozione del materiale (reactive ion etching) aumenta il numero di difetti. Questo fatto comporta

un peggioramento delle prestazioni elettroniche. In questo elaborato viene quindi descritto uno studio sulle tecniche di passivazione che potrebbero rimediare alla degradazione portata dalla tecnica in questione.

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Chapter 1

Introduction

The idea of fossil fuels as a source capable to meet the needs of the global energy demand and not significantly harmful for the environment has been undermined with the increase of the population [1] (Fig.1.1). This has resulted in a shift towards alternative energy and especially renewable resources (Fig.1.2). In recent years, the need of moving to renewable energy as a pri-

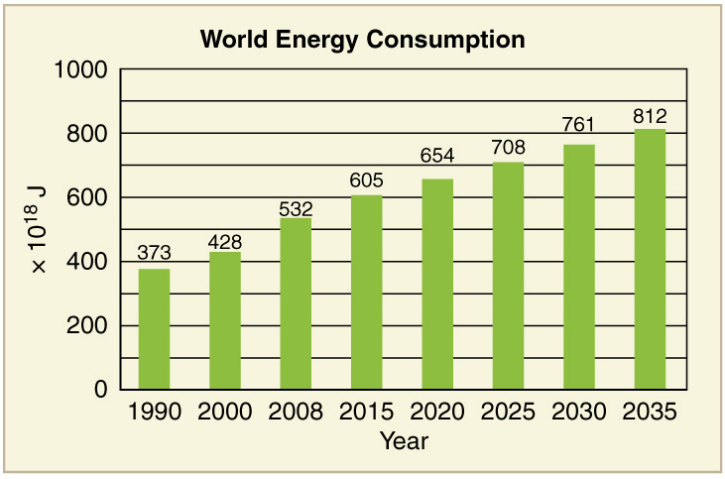


Figure 1.1: World energy consumption [2]

mary source for electricity generation has brought to a rapid growth of the

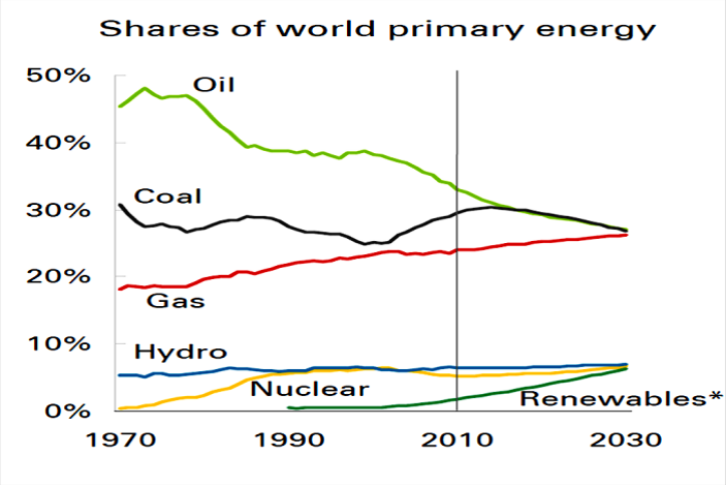


Figure 1.2: Share of World primary energy [3]

solar industry [4]. Precisely, Photovoltaics, a process with the unique ability to directly convert light into electricity using solar cells, has gained importance in the sector. Nevertheless, such technology, in order to acquire a dominant position in an industrial level and enlarge its market share, requires an enhancement of the performances and lower fabrication costs compared to the current competitors (Tab.1.1). Historically crystalline silicon

Energy Plant Type	Cost in cent per Kwh
Natural Gas	6.4
Wind Turbine	7.5
Conventional Coal	8
Advanced Nuclear	10
Solar PV	15
Solar thermal	16

Table 1.1: PV market competitors [5]

was chosen as the designated substrate to be used as the active material in PV,because it absorbs a large range of the solar radiation spectrum, it is very abundant, non-toxic, stable and can be processed using well known

techniques [6]. Nowadays, different materials are studied but c-Si (crystalline silicon) still plays a major role and it is plausible that this trend will not go through significant changes in the incoming years [4].

Until now, PV research has been deeply focusing in methods to enhance the efficiency of solar cells; that means fabricating structures that absorb most of the solar radiation, convert most of the absorbed photons in electric carrier and minimize parasitic losses (currents and absorption). As it will be made clear in the following sections, an ideal situation might be reached if the cell was made of several materials in order to take into advantage most part of the solar spectrum and with a large thickness so that the bulk-to-surface ratio is maximized also. However, despite the high efficiency obtainable from such a structure, the production costs would critically increase, not allowing it to be considered as sustainable in an industrial level. There is therefore a need to find a synergy between cost and efficiency. Later in this work, the thin film technology, for c-Si, as a possible way to reach such compromise will be presented, highlighting the advantages and the issues, especially related to optical performances. Subsequently, possible technical solutions to optimize optical and electronic properties of thin film c-Si cells will be deeply described and that will represent the core of the project. At first though, a brief description of the Physics of PV cells will be given with emphasis on light management.

Chapter 2

Physics of photovoltaic solar cells

2.1 Operation

A photovoltaic solar cell is an electronic device that directly converts radiation in electrical power: such conversion is in practice and conventionally achieved by means of semiconductors in a p-n junction [7](Fig.2.1).

The full process of power generation can be summarized in the following steps [8]:

- Generation of carriers from radiation absorption
- Collection of carriers and current generation
- Voltage generation across the device
- Power dissipation in the load and in parasitic resistances

Let us consider a diode under illumination. The absorption of photons in the device generates excess carriers; far from the junction there is equilib-

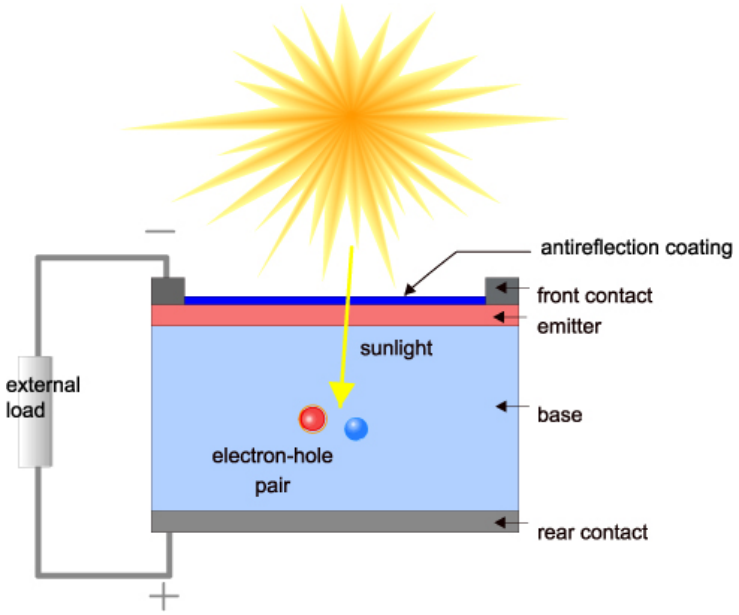


Figure 2.1: Solar cell operation [8]

rium between the carrier generation and subsequent recombination but near the depletion area, where the field effect is not negligible, minority carriers are swept over resulting in a gradient of electrons and holes to the junction (Fig.2.3). There is therefore a current of minority carriers flowing in the device. Such photo-current flows through an external load and thus, a forward voltage is generated across the device [7]. The net current of a solar cell is obtained as the sum of the photo generated current, that reaches the maximum when no voltage is applied to the diode, or rather under short circuit conditions and the forward bias current, which cancels out the photo generated one when the voltage exceeds the threshold value, or rather under open circuit conditions.

The I-V characteristic curve of a solar cell diode can be simply built as a superposition of the dark IV curve and illuminated IV characteristic [7] (Fig.2.4). Quantitatively, the expressions in the next paragraphs show the

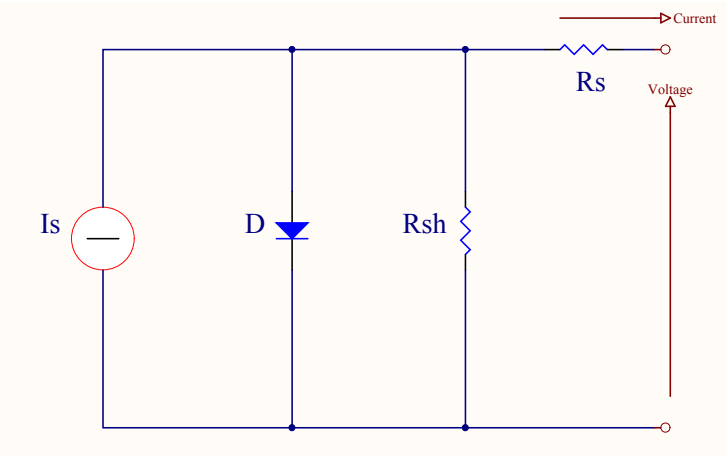


Figure 2.2: Equivalent circuit

actual behaviour.

2.1.1 Diode under illumination

$$-D_n\frac{\partial^2 n}{\partial x^2}+\frac{n-n_0}{\tau_n}-G=0 \tag{2.1}$$

$$-D_p\frac{\partial^2 p}{\partial x^2}+\frac{p-p_0}{\tau_p}-G=0 \tag{2.2}$$

$$n_1(x=0)-n_0=0 \qquad n_1(x=\infty)-n_0=\tau_n G$$

$$p_1(x=0)-p_0=0 \qquad p_1(x=\infty)-p_0=\tau_p G$$

$$J_{n1}(x)=\frac{qD_n\tau_n G}{L_n}exp(-\frac{x}{L}) \tag{2.3}$$

$$J_{p1}(x)=\frac{qD_p\tau_p G}{L_p}exp(-\frac{x}{L}) \tag{2.4}$$

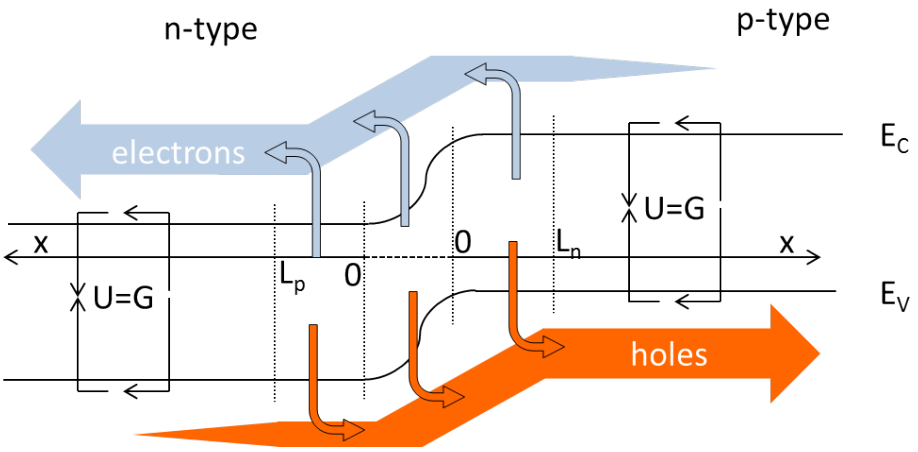


Figure 2.3: minority carrier gradient

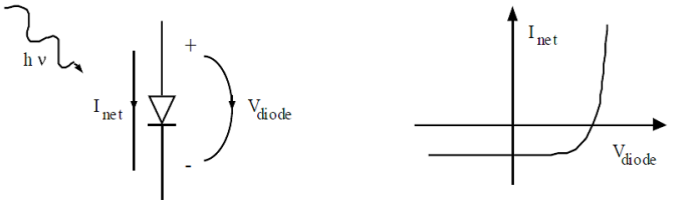


Figure 2.4: IV curve

2.1.2 Diode in the dark

$$-D_n\frac{\partial^2 n}{\partial x^2}+\frac{n-n_0}{\tau_n}=0 \tag{2.5}$$

$$-D_p\frac{\partial^2 p}{\partial x^2}+\frac{p-p_0}{\tau_p}=0 \tag{2.6}$$

$$\tag{2.7}$$

$$n_2(x=0)-n_0=n_0 exp(\frac{V_{pn}}{V_T}-1) \qquad n_2(x=\infty)-n_0=0$$

$$p_2(x=0)-p_0=p_0 exp(\frac{V_{pn}}{V_T}-1) \qquad p_2(x=\infty)-n_0=0$$

$$J_{n2}(x) = \frac{qD_n n_0}{L_n} e^{-\frac{x}{L}} exp(\frac{V_{pn}}{V_T} - 1) \tag{2.8}$$

$$J_{p2}(x) = \frac{qD_p p_0}{L_p} e^{-\frac{x}{L}} exp(\frac{V_{pn}}{V_T} - 1) \tag{2.9}$$

2.1.3 Total current

$$J = J_1(x = 0) + J_2(x = 0)$$

$$J = -qG(\frac{D_n\tau_n}{L_n} + \frac{D_p\tau_p}{L_p}) + q(\frac{D_n n_0}{L_n} + \frac{D_p p_)}{L_p})exp(\frac{V_{pn}}{V_T} - 1) \tag{2.10}$$

$$J_{sc} = qG(\frac{D_n\tau_n}{L_n} + \frac{D_p\tau_p}{L_p}) \qquad J_0 = q(\frac{D_n n_0}{L_n} + \frac{D_p p_)}{L_p})$$

$$\boxed{J = J_{sc} + J_0 exp(\frac{V_{pn}}{V_T} - 1)} \tag{2.11}$$

$$\boxed{V_{oc} = V_T ln(-\frac{J_{sc}}{J_0} + 1)} \tag{2.12}$$

2.2 Limiting factors in total efficiency

Given the characteristic of the curve one can observe that the maximum power generated from a solar cell is not given by the simple product between the short circuit current and the open circuit voltage (Fig.2.5). The fill factor is defined as

$$FF = \frac{V_M I_M}{V_{oc} I_{sc}} \tag{2.13}$$

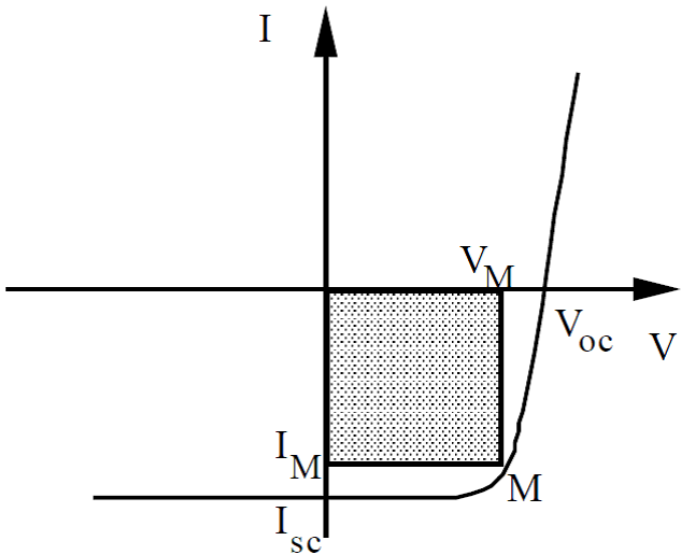


Figure 2.5: Fill factor

The curvature itself is then a limiting part of the total efficiency, which is defined as

$$\eta = \frac{P_M}{P_L} \tag{2.14}$$

$$\eta = \frac{J_{sc} V_{oc} FF}{\int_0^\infty P(\lambda) d\lambda} \tag{2.15}$$

The fill factor is not though the only limiting factor of the total efficiency of PV cells. Several losses due to the basic Physical limitations of semiconductors, like long wavelength losses, excess energy losses and voltage factor losses drastically decrease the performances and are not avoidable. Others, related to fabrication and technical issues, like incomplete absorption and collection, rather than shadowing factor and reflectance losses further reduce

the total efficiency [7] [9] [10](Fig.2.6).

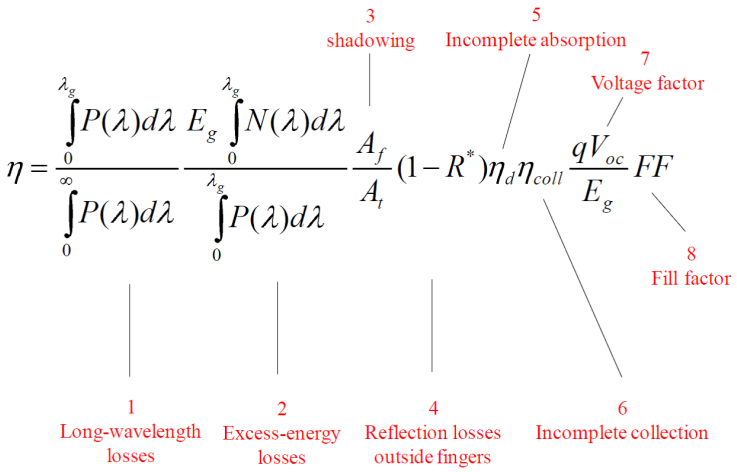


Figure 2.6: Limiting efficiency

2.3 Recombination and resistive losses

From what has been presented until now, it is clear that, given a high absorption from the device and carrier generation, it is fundamental to optimize the collection of the latter and avoid huge power dissipation from parasitic resistances.

Recombination losses affect both the current collection (and therefore the short-circuit current) as well as the forward bias injection current (and therefore the open-circuit voltage). In order for the p-n junction to be able to collect all of the light-generated carriers, both surface and bulk recombination must be minimized. In silicon solar cells, the two conditions commonly required for such current collection are [8]:

- the carrier must be generated within a diffusion length of the junction, so that it will be able to diffuse to the junction before recombining

- in the case of a localized high recombination site (such as at an unpassivated surface or at a grain boundary in multicrystalline devices), the carrier must be generated closer to the junction than to the recombination site. For less severe localized recombination sites, (such as a passivated surface), carriers can be generated closer to the recombination site while still being able to diffuse to the junction and be collected without recombining.

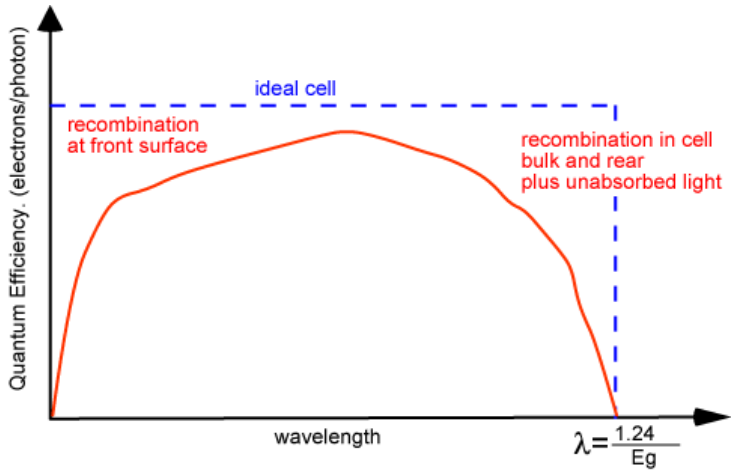


Figure 2.7: Recombination [8]

There are three major kind of recombination that may take place in a solar diode [8]:

- Radiative recombination: in this case electron-hole recombination results in a photon emission; this kind of recombination is uncommon for indirect band gap materials like silicon.

- Auger recombination: in this case the recombination released energy enables a second electron to be promoted to higher energy level

- Shockley-Read-Hall recombination: this process is mainly caused by recombination sites situated inside the gap of the material; such traps may be generated because of different species inside the bulk or defects present in the periodic lattice. Since the surfaces represent a brake of the crystal lattice periodicity, it provides several dangling bonds which act like recombination sites.

Defining the carrier lifetime as the average time it takes for a minority carrier to recombine, one can obtain the following expressions:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{radiative}} + \frac{1}{\tau_{SRH}} \tag{2.16}$$

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S}{W} \tag{2.17}$$

The objective is therefore to maximize the carrier lifetime.

Moreover a well working cell must minimize the resistive losses.
The characteristic resistance of a solar cell is the output resistance of the solar cell at its maximum power point. If the resistance of the load is equal to the characteristic resistance of the solar cell, then the maximum power is transferred to the load and the solar cell operates at its maximum power point [8]. Resistive effects in solar cells reduce the efficiency of the solar cell by dissipating power in the resistances. The most common parasitic resistances are series resistance and shunt resistance.
Series resistance in a solar cell has three causes: firstly, the movement of current through the emitter and base of the solar cell; secondly, the contact resistance between the metal contact and the silicon; and finally the resistance of the top and rear metal contacts. The main impact of series resistance

is to reduce the fill factor, although excessively high values may also reduce the short-circuit current.
Low shunt resistance causes power losses in solar cells by providing an alternate current path for the light-generated current. Such a diversion reduces the amount of current flowing through the solar cell junction and reduces the voltage from the solar cell.

2.4 Light management

Until now the performances and the losses related to the ratio between the generated power and absorbed radiation has been considered. A fundamental matter is also to enhance the absorption itself and typical technical models to do so will be here presented.

Ideally, any photon with higher energy than the material band gap should be absorbed. In a realistic picture though part of the incoming light is reflected from the top contact, part from the front side, part is transmitted, even though it is usually negligible, and part of the radiation reflected from the back contact escapes from the material from the front side (Fig.2.8). At last, provided that the previous losses are diminished, not all the light is absorbed in the silicon solar cell. An important manufacturing issue is therefore to minimize these optical losses in order to enhance the carrier generation.

The typical methods used to enhance absorption in solar cells consist of using anti reflection coating, texturing the front side and promoting light trapping. An ARC (anti-reflection coating) is a thin layer of dielectric material with an intermediate refractive index between the active material and air and with dimension specially chosen so that the reflected wave from the

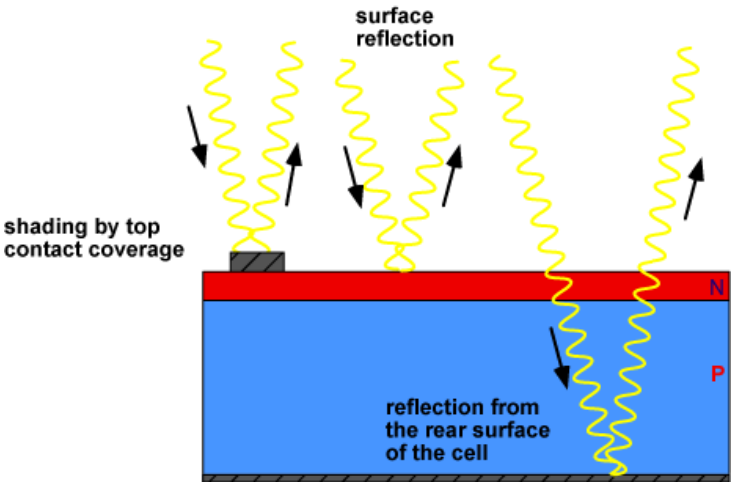


Figure 2.8: Optical losses in solar cells [8]

surface of the coating destructively interfere with the waves that escape from the material, after being reflected from the active material (Fig.2.9) [8]. The

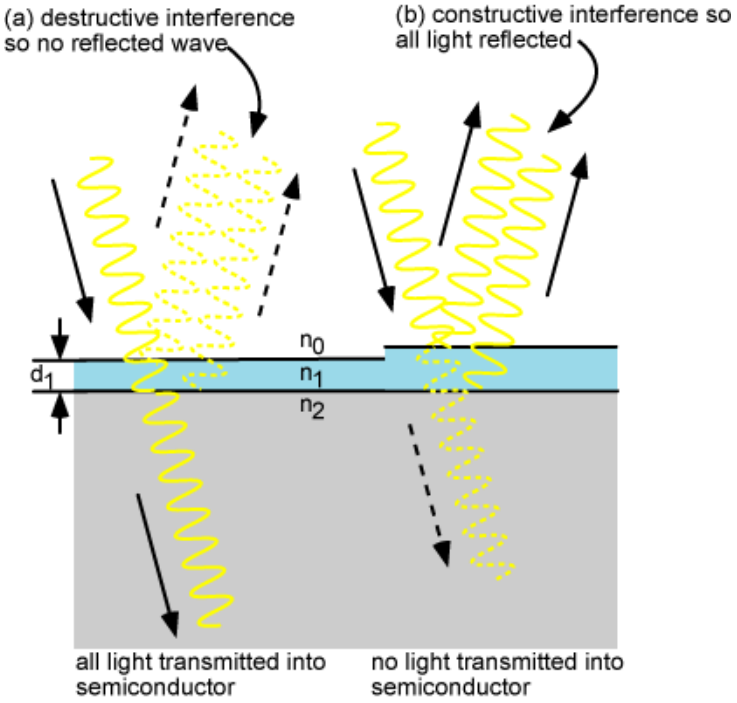


Figure 2.9: Anti reflection coating [8]

ARC thickness is chosen with the criteria that inside the dielectric material the radiation has a quarter-wavelength compared to the incident one. In case of a transparent material with refractive index n_1 and being λ_0 the wavelength of the radiation in air, the thickness d_1 follows the rule

$$d_1 = \frac{\lambda_0}{4n_1} \tag{2.18}$$

Reflection can be further reduced by adding different ARC layers.

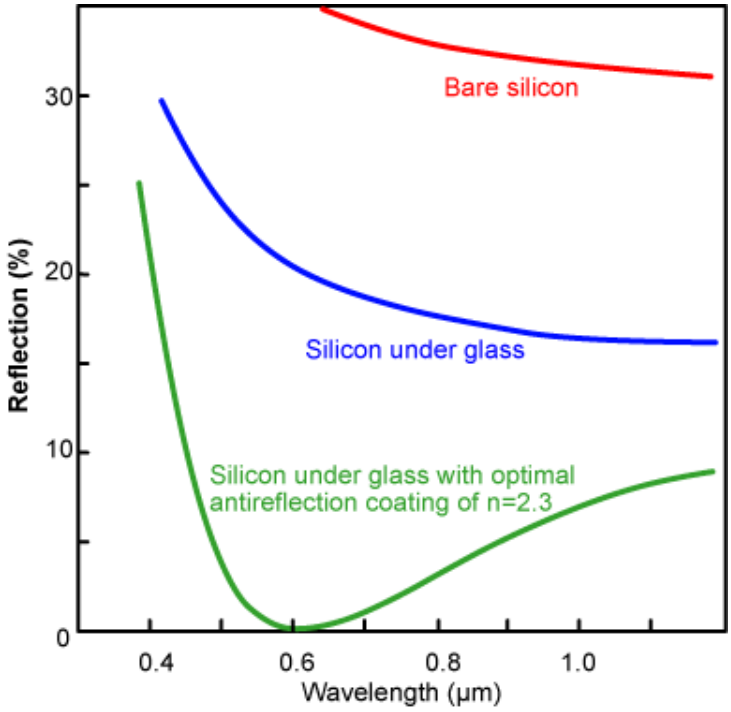


Figure 2.10: Reflection ARC [8]

Another well founded technique to reduce reflection is texturing the front surface. Any "roughening" of the surface reduces reflection by increasing the chances of reflected light bouncing back onto the surface, rather than out to the surrounding air. Currently, the benchmark for surface texturing are the Random Pyramid Texturing and Inverted Pyramid texturing [9] [11]. All

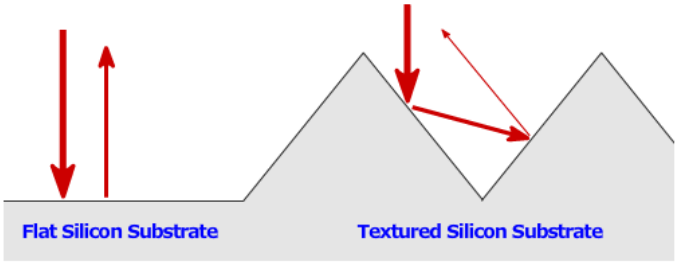
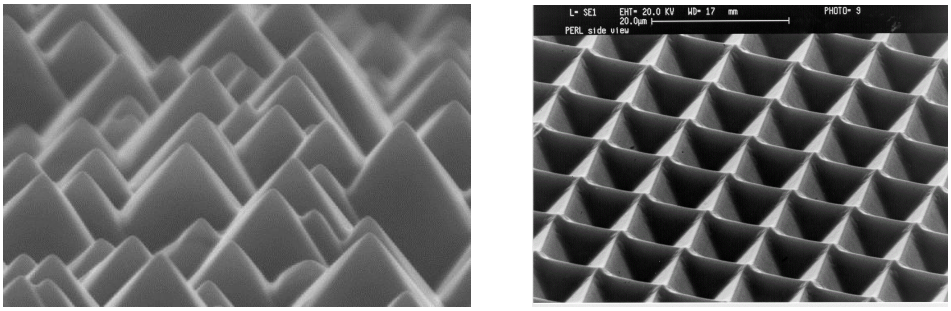


Figure 2.11: Front side texturing [8]



(a) Random pyramid texturing (b) Inverted pyramid texturing

Figure 2.12: Pyramid texturing [8]

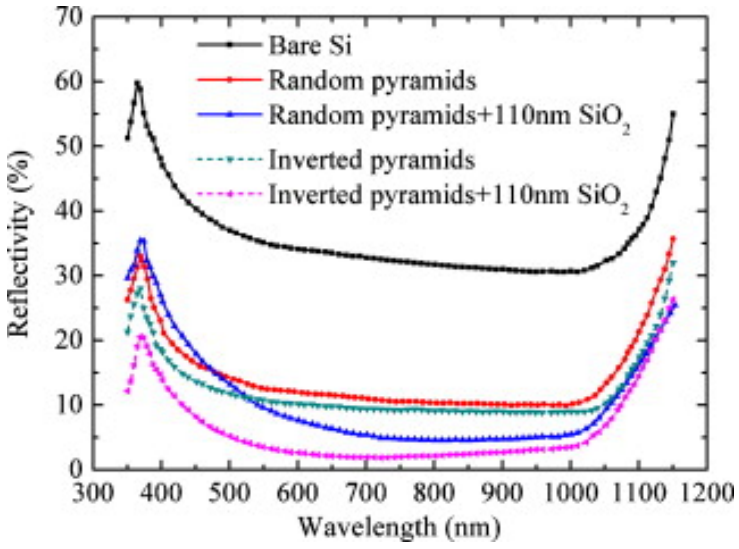


Figure 2.13: Reflection from textured surface [8]

these techniques will be later deeper discussed.

Provided now that the reflection of the device is optimized, it is essential that light is absorbed in the silicon solar cell. To ensure that, the absorption coefficient of the material and the optical path length has to be considered. The absorption coefficient determines how far into a material light of a particular wavelength can penetrate before it is absorbed. In a material with a low absorption coefficient, light is only poorly absorbed, and if the material is thin enough, it will appear transparent to that wavelength [8]. An useful parameter is the absorption depth, the inverse of the absorption coefficient, that gives the distance at which the intensity of the radiation drops of a factor 1/e of the incident intensity.
The optical path length, in this case, refers to the distance that an unabsorbed photon may travel within the device before it gets absorbed.

Thickening the cell may represent a solution, but as already stated, if the photon is absorbed at distances above the electron diffusion length, collection problems arise.
An optimal device is the one that provides light trapping, i.e. enables the optical path length to be several times the material thickness.
Light trapping is usually achieved by changing the angle at which light travels in the solar cell by having it be incident on an angled surface. A textured surface will not only reduce reflection on the surface as previously described but will also couple light obliquely into the silicon, thus giving a longer optical path length than the physical device thickness. Moreover, if the internal incident angle of the traveling radiation exceeds the critical value, total internal reflection may occur. At last if a back reflector that randomizes the direction of the reflected light is used, i.e. a labertian back reflector, the ideal case where the optical path is enhanced by a factor $4n^2$, where

n is the refractive index of the material (here silicon), can be reached [8]. The last scenario is known as Lambertian limit and can be considered the current benchmark for light trapping. In this work however, possible way to overcome this limit will be presented by means of shifting from geometrical optics to diffractive optics. Reminding that for conservation law, the sum of the fractions of the total incident radiation that is reflected, transmitted and absorbed is constant and equal to one, and assuming an ideal back reflector so that the trasmittance is negligible, the enhancement of the optical path length inside the device, from an optical characterization point of view, results in a reduction of the total reflectance from the material.

It is interesting here to consider an important characteristic of crystalline silicon that surely has contributed to its wide use in the PV sector: if we consider Fig.2.14, we notice that c-Si has an absorption coefficient which is considerably lower, for a wide spectrum, compared to other materials. Nevertheless, its high refractive index enables it a better light trapping compared to the competitors because of the $4n^2$ law.

2.5 Thin film crystalline silicon PV cells

Presently, more than 30% of the total cost for a PV module is due to the silicon wafer cost [12]. In order to find the aforementioned synergy between cost and efficiency other materials as active material or thin film technology for crystalline silicon PV has to be considered. In recent years, several materials have been studied with this purpose: compounds like cadmium telluride [13] have proved to be cheaper than traditional c-Si cells. Amorphous silicon as well has been utilized as a possible solution [14]; the last has been involved in p-i-n structures with total thicknesses in the order of a few mi-

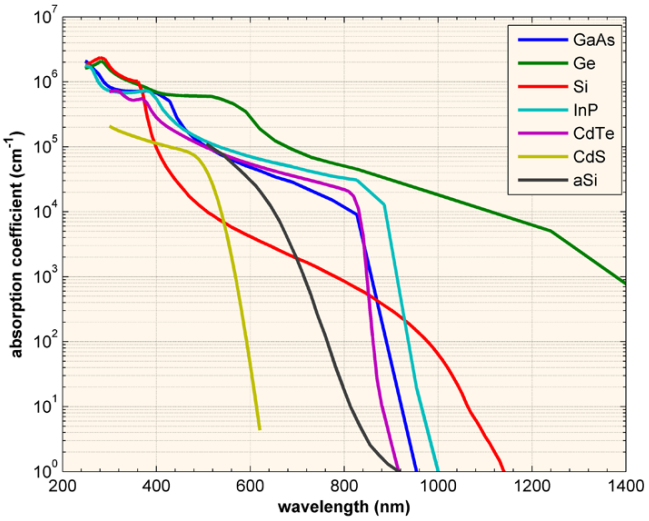


Figure 2.14: Absorption coefficient [8]

crons. However, fundamental issues related to toxicity, cell degradation with time and lower efficiencies compared to c-Si, arise when shifting to these new materials [9] [10], issues that thin film crystalline silicon substrates are able to overcome. Nevertheless, different problems, basically related to optical losses, stand up when the latter structures are considered.

2.5.1 Optical losses in thin film c-Si solar cells

Let us consider Fig.2.15 and Fig.2.16: reminding that the wavelength range of interest for silicon goes up to 1200nm *ca*, one can observe that thicknesses over 1000 microns are needed to absorb the whole part of solar radiation below the silicon band gap limit. Current cells display a few hundreds of microns thickness and this allow them to absorb most part of the desired spectrum. If we now consider cell thicknesses of a few tens of microns, eg. 40 microns, the absorption spectrum stops at the infrared region. Taking into account limiting cases like 1 micron thick substrate, we observe that a

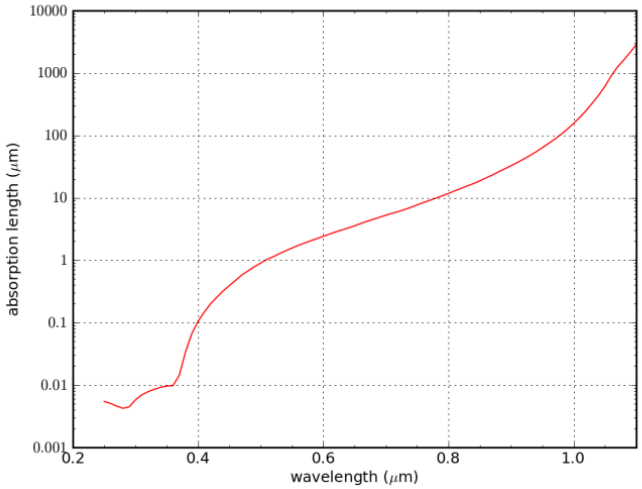


Figure 2.15: Silicon absorption depth [8]

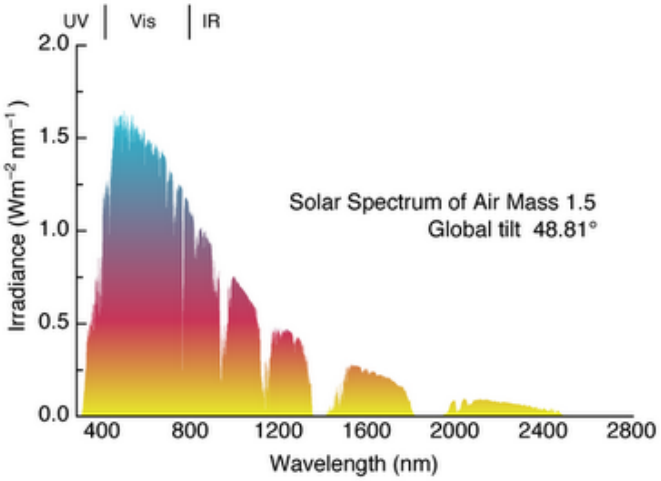


Figure 2.16: Solar spectrum [8]

substantial part of visible spectrum will be lost (here we consider it a limiting case since several technical difficulties arise to further thin the substrates). In Fig.2.17 and Fig.2.18, the effect of the lost radiation in terms of photocurrent is illustrated.

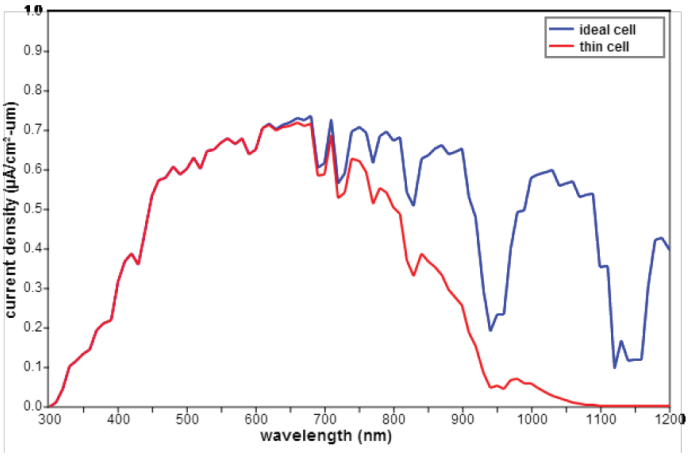


Figure 2.17: Current density in 10 microns thin films [8]

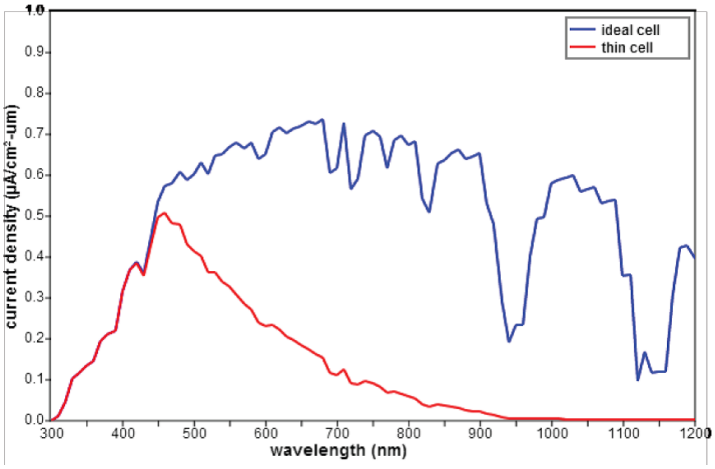


Figure 2.18: Current density in 1 microns thin films [8]

It is fundamental therefore to provide light trapping, in order to increase the optical length path, if thin films of a few tens of microns are to be used in the PV industry. As already stated, the traditional techniques to promote light trapping are based on texturing the surface. The conventional methods, eg random pyramid texturing, consist of immersing silicon substrate in solutions like KOH or TMAH [9]; these solutions etch silicon following crys-

tallographic planes, obtaining the pyramidal structures. A big advantage of such technique comes also from the simplicity, rather than the optical performances enhancement. However such technique is not compatible with thin film substrates; from Fig.2.19 one can observe that the utilized solution at first removes 5-10 microns of active material and then starts etching other 3-5 microns following crystallographic planes. There is therefore an overall material loss of 10 microns [15]. For a thick cell, such dimensions are negligible, but when thin substrate are considered, such losses happen to be significant.

2.5.2 Technologies for thin film crystalline silicon substrates fabrication

Conventional methods to produce thin film c-Si substrate consist of epitaxial growth. This method requires a foreign substrate where to grow crystalline silicon. Usually low quality and highly doped c-Si wafers of a few hundreds microns thickness are used for this purpose. A few microns of high quality doped crystalline silicon is then epitaxially grown by means of PECVD technique.

A non conventional method to fabricate thin films of thicknesses of around 40µm, called epifoil, is now under development. The fabrication starts with an electrochemical etching step of a highly doped silicon substrate that results in the formation of a double porous layer: a top layer presenting low porosity and a larger bottom layer presenting high porosity. This step is then followed by a H_2 baking step in order to allow a reorganization of the porous layer. Afterwards doped c-Si emitter and base are deposited on the top of the low porosity layer, which represents a good template for epitaxy, by CVD. At this level, the epitaxially grown layer is attached to parent substrate, strongly

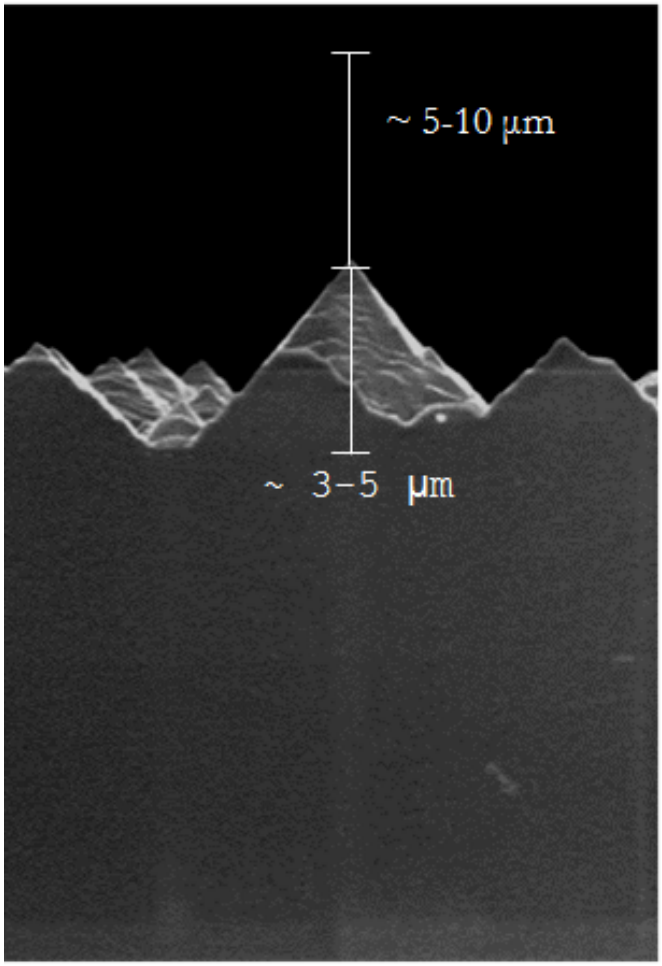


Figure 2.19: Material consumption in random pyramid texturing

enough to sustain front-side processing yet weakly enough to be detachable after bonding. After the front side processing, the foil is bonded to glass by silicone and subsequently detached from the parent substrate in ultrasonic bath [16] [17].

Epitaxial growth results in a very high quality silicon deposition but presents issues related to the foreign substrate and needs expensive techniques. This last aspect is in contrast with the idea to go towards thin film technology in order to reduce the costs. A novel technique that does

not make use of any epitaxy, called epifree, is here presented [18]. This method is based on the formation of silicon-on-nothing structures by means of thermal annealing of silicon trenches. The first step consists of a deep-UV lithography followed by a dry etching process. After this step a pre-studied disposition of pores array is obtained. Afterwards, by thermal annealing at high temperature, a reorganization takes place and three different layers are formed: the silicon substrate, a thin air layer and a suspended layer of c-Si about 1µm thick. The suspended layer is weakly attached to the initial silicon surface and can be detached from it by bonding it to a glass substrate. The initial silicon substrate can then be used again for further epifree fabrication. The overall process is summarized in Fig.2.20. This process enables

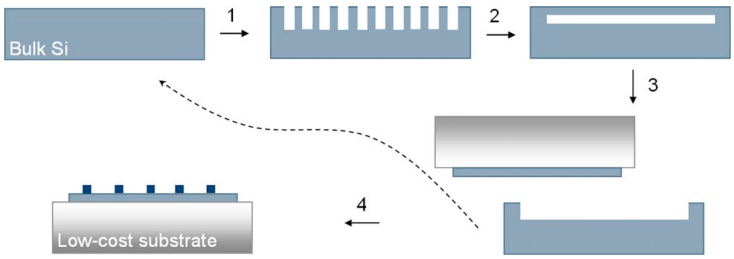


Figure 2.20: Epifree fabrication [18]

the fabrication of ultra-thin pure c-Si layers without any epitaxy.

Chapter 3

Light trapping schemes

In the previous chapter, thin film technology for c-Si PV technologies was introduced, highlighting the related optical issues. Precisely, it was said that for indirect band gap materials, like c-Si, thinning the active layer results in incomplete absorption and, as a consequence, the photo-current generation is critically reduced. Light trapping schemes are therefore crucial in order to obtain reasonable values of the electrical efficiency. Conventional techniques for light trapping consist in texturing the surface. Light trapping was first rigorously and analytically studied by Yablonovitch and Cody using a statistical approach [19] [20]. In such analysis a randomly scattering surface consisting of micron-size features was considered and, therefore, a geometrical optics approach was utilized. The developed theoretical model stated that the absorption enhancement in a material was upper limited by the factor $4n^2/sin\theta$, where θ is the angle of the emission cone of the material surrounding the cell.

As previously showed, the texturing techniques presently in use for solar cells with thicknesses of a few hundred microns are not compatible with thin film technology because of the material consumption. In recent years

though, the idea of submicron-scale patterning has been intensely studied and proposed. The aforementioned analysis made by Yablonovitch however is no more applicable when nano-photonic regimes are considered; the presence of sub-wavelength structures requires the use diffraction theory and effective medium theory[21]. Several works have proved that the use of diffraction grating may actually overcome the Lambertian limit opening new avenues for highly efficient new generation solar cells [21][22][23].

In this chapter a few novel schemes for light trapping in thin film c-Si solar cells are presented. Precisely, studies involving structures that provide scattering from metal nano-particles near their localized plasmon resonance, presenting a metal back reflector or o rear reflector coated with dielectric particles are shown. Moreover techniques consisting of wet etching to obtain "black silicon" are considered. Finally, technologies that make use of photonic crystals resulting in a back side or front side diffraction grating are introduced. For this latter case, since the core of the experimental work of this project is mainly focused on a lithographic technique, nano-imprint lithography, that enables a front side diffraction grating, a theoretical study investigating the physical aspects that contribute to light trapping in nano-imprinted samples is deeply described.

3.1 Metal nano-particles

Intense studies on the integration of metal nano-particles in thin film solar cells have been carried in the recent decades after the discovery that Raman scattering can be increased by order of magnitude through the use of such structures [24]. In metals the plasmon resonance is the effect of the collective oscillation of conduction electrons that arise with the incident radiation.

When sub-wavelength particles are used, the conduction electrons start oscillating in phase, resulting in charge polarization at the surface giving rise to a resonantly enhanced field throughout the particle and also outside of it [25]. When such structures are placed on the interface of two media with a high and a low refractive index, the overall effects are the scattering of a higher fraction of light in the medium with higher refractive index and a broad distribution of angles of the scatter light [26]. Because of this last aspect, the idea of integrating the particles at the front or at the back surface of the active material of the solar cell, in order to enhance the optical path, has been proposed.

This technique, enables light trapping without any consumption of the active material and thus is compatible with thin film technology. However, a main drawback of such technology is presented by the fact that the introduction of metal particles contributes to higher Ohmic losses lowering the total cell efficiency. Moreover, it has been reported [26] that when the particles are placed on the front side, the incident light destructively interfere with the scattered radiation (Fano resonance) leading to an absorption suppression. Therefore, the integration of the structures at the rear side is preferred.

The fabrication of the overall cell structure is usually achieved by interposing silver nano-particles between the rear reflector and the silicon layer. The choice of silver is made because of its low absorption properties and since it has the plasmonic resonance in the desired wavelength range for solar applications. The region where the nano-particles are placed is usually separated from the reflector and from the semiconductor by means of dielectric spacers. The array of particles are obtained by means of hole-mask colloidal lithography [27] , which allows a pseudo-periodic distribution, or by annealing, which results in a random distribution. For the back reflector,

Aluminum stack can be used rather than particles of dielectric materials, like titanium dioxide, that presents high refractive index, therefore a high reflectance, and good scattering properties. Fig.3.1 shows a reflectance plot obtained by characterizing the described structured.

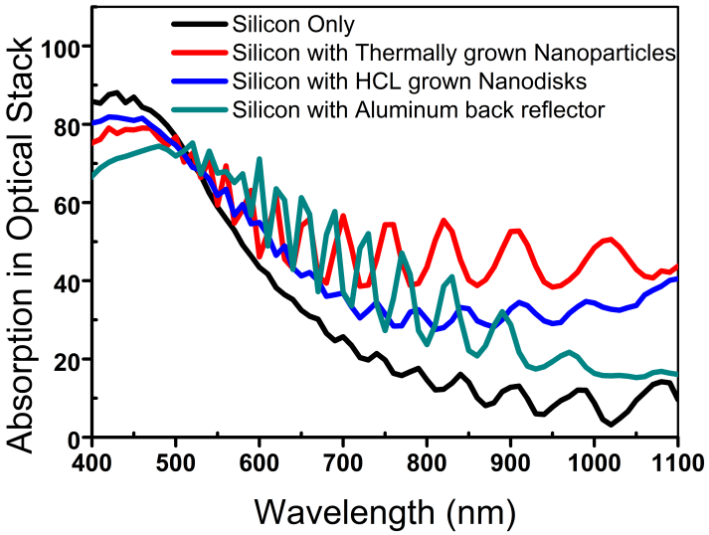


Figure 3.1: Reflectance of plasmonic solar cell [25]

3.2 Black etching

Black etching is a method for nano-scale texturing of silicon surface that by means of an ultra-thin film metal deposition and a wet chemical etching step provides structures which present an absorbance over 95% without any ARC (Fig.3.2) [28]. The process suggested by Koynov *et al*, consists of a thermal evaporation of gold for a nominal thickness of $1 - 2$nm. Such low thickness allows a non-uniform deposition resulting in nanoclusters, which composition define the texturing. The deposition is then followed by a wet chemical etching step carried out at room temperature in an aqueous solu-

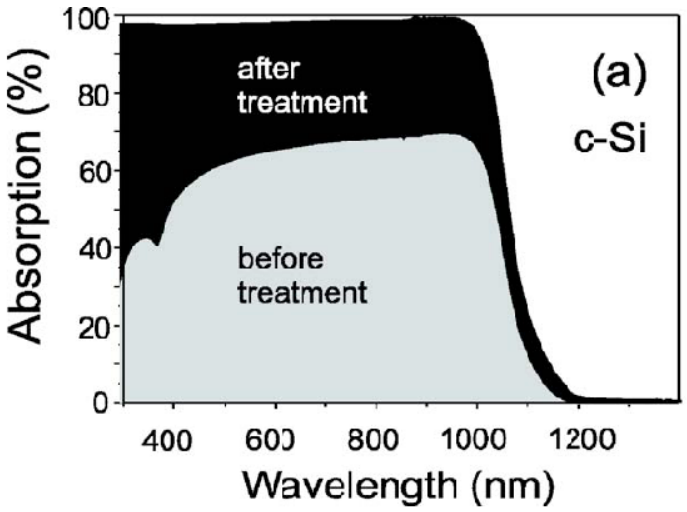


Figure 3.2: Absorbance of black silicon [28]

tion of hydrofluoric acid and hydrogen peroxide. Such solution etches clean silicon with an etch rate below 1nm/min. The gold catalytic effect however consent a much higher etching rate. The final result, obtained after 90s of wet etching, consist of densely packed randomly distributed hillocks featuring average lateral sizes within the range of $50 - 100$nm and average heights of 250nm (Fig.3.3). This texturing is thus compatible with thin film

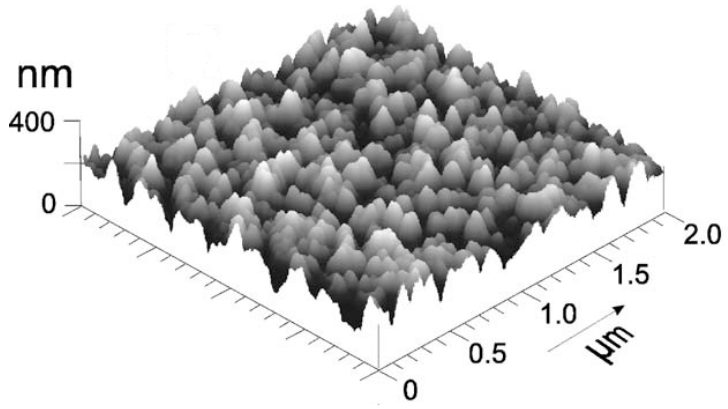


Figure 3.3: Topography of black silicon [28]

technology because of the very low material consumption and presents good anti-reflection properties.

3.3 Photonic crystal

Photonic crystals are periodic optical nano-structures with a periodical modulation of refractive index that alters the photonic density of states. The name is justified by the similarity of the motion of photons in these structures with the case of electrons in crystal lattice; equally to the electronic case, photonic crystals exhibit a forbidden band gap.

Previously it was stated that by means of a statistical and geometrical optics approach an upper limit to the absorption enhancement, when random micron size texturing are considered, can be found. The statistical optics derivation assumes that the incident rays are fully randomized inside the textured solar cell so that all the photonic states are equally filled. The density of photonic states $\rho(\omega)$ is proportional to n^2, which gives rise to the $4n^2$ law [29]. However, when considering silicon in PV application, only a small window of the total solar spectrum is of interest. The use of photonic crystals in solar cell is then suggested by considering the possibility to chose an optimal grating so that the gap in $\rho(\omega)$ falls below the silicon absorption edge and the peaks in $\rho(\omega)$ fall just above it [30]. Briefly, such a structure subtracts photonic states from non-absorbing regions and increase states in absorbing regions, consenting the overcome of the Lambertian limit for photons in the frequency range of silicon absorption spectrum.

2-D photonic crystals consisting of a periodic patterning featuring holes either on a dielectric material or in the active material have been proposed and studied in the recent years [15] [31] [32] [33]. In order to fulfil the character-

istics stated above, the features presents wavelength-scale sizes and therefore the patterning results to be a diffraction grating. Such grating can be integrated in the front side, in the rear side or in both sides in a solar cell.
When the grating is placed on the backside, the weakly absorbed photons that reach the rear side are reflected from the contact and diffracted by the grating. This results in a broad angle reflection that may enable total internal reflection on the front side. Works showing theoretical results [34] and experimental results [15] [35] of cells with backside grating with different parameters have been reported.
In case of front side integration, apart from the the angle broadening aspect achieved by diffraction, an anti-reflective property, because of the graded refractive index profile, is observed.

In order to present a proper theoretical model able to describe light propagation through a nano-patterned interface,the absorption enhancement and the overcoming of the Lambertian limit, RCWA method and FDTD technique should be properly used and explained in detail. Hereafter, a model developed by A. Herman *et al* [36] is shortly presented. The study does not focus on the overcoming of the Lambertian limit; it does instead, give an explanation of the specific contribution of the impedance matching in the absorption enhancement in a nano-patterned surface compared to a flat surface.

In the model an ultra-thin c-Si layer, patterned in the front side with a periodic square array of holes, is considered. The holes are mathematically described using a normalized super-Gaussian profile which value is $f(r) = \exp[-(r^2/2\sigma^2)^m]$ where r is the radius of the hole, m is a real number which determines the actual shape of the hole and $\sigma^2 = R^2/2[ln(T/B)]^{1/m}$ Fig.3.4.
In order to study the specific contribution of the impedance matching in the

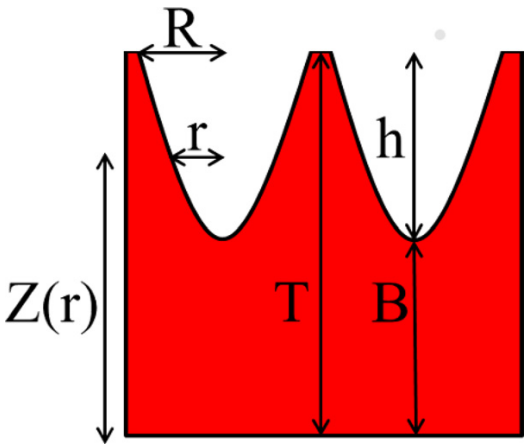


Figure 3.4: Parameters of the super-Gaussian function [36]

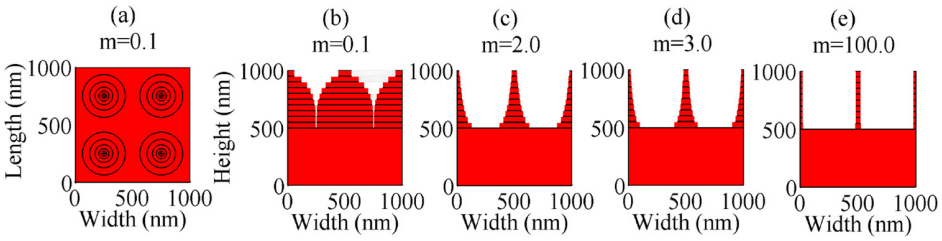


Figure 3.5: Hole shapes [36]

absorption enhancement the effective medium theory is used. The effective permittivity is given by the Maxwell-Garnett formula:

$$\epsilon = \epsilon_{c-Si} + 2f\epsilon_{c-Si}\frac{\epsilon_{air} - \epsilon_{c-Si}}{\epsilon_{air} + \epsilon_{c-Si} - f(\epsilon_{air} - \epsilon_{c-Si})} \tag{3.1}$$

To be noted here that the appropriate conditions for the effective medium theory to be used is that the wavelength of the incident light is much larger than the distances between the inclusions. Here, since the distances and the wavelength are of the same order of magnitude, the theory is used as an approximation.

The effective medium theory is used in two ways: first, the inhomoge-

neous part of the slab (air/c-Si) is replaced by a single homogeneous one; second, every inhomogeneous layer containing a cylinder of air is replaced by a homogeneous layer.

In order to optically characterize, total absorption calculation, together with the integrated quantum efficiency, defined as:

$$\eta = \frac{\Phi_A}{\Phi_{inc}} = \frac{\int_{\lambda min}^{\lambda max} \frac{\lambda}{hc} S(\lambda) A(\lambda) d\lambda}{\int_{\lambda min}^{\lambda max} \frac{\lambda}{hc} S(\lambda) d\lambda} \tag{3.2}$$

are used. At last the simulated results, obtained with different parameters, were compared between themselves and respect to experimental results, this last step in order to validate the model.

In the mentioned work, the first part of results and discussion was focused on the optimization of the pattern parameters; here that part will not be recalled but the effect of the impedance matching and of light trapping will be considered only. Later in this work, the parameters optimization part will be handled again.

The absorption enhancement in the nano-patterned structure is due to both impedance matching and light trapping (mode coupling). At first the influence of the holes shape in both contribution was studied by considering the different absorption spectra with different shapes. Fig.3.6 shows that, at short wavelengths, below 450nm, where the the impedance matching plays the major role, the absorption is clearly effected by the shape of the holes.

Effective medium theory (EM) was then used, in order to identify the importance of both impedance matching and mode coupling effects.

At first, the patterned layer was replaced by a single effective layer and subsequently by several effective layers, obtaining a graded index profile. From Fig.3.7 an increase in absorption and an approach to the actual patterned

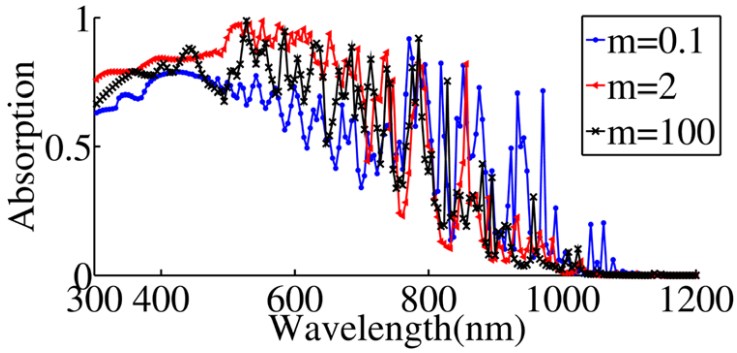


Figure 3.6: Absorption for different shapes of the holes [36]

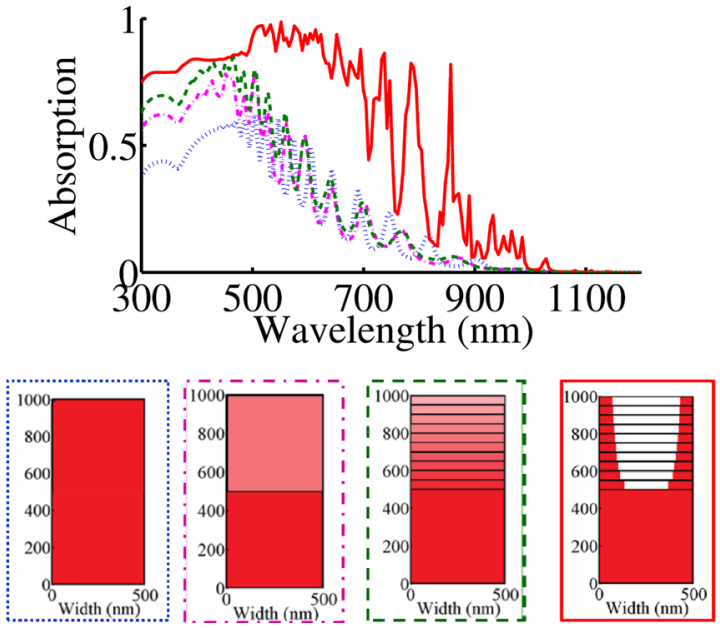


Figure 3.7: Role of holes in the anti-reflective part [36]

layer behaviour can be observed, below 450nm, when several layers are used. It was shown then, that the holes are responsible for an anti-reflective effect (below 450nm), in which the shape plays an important role due the fact that they create a graded index [36].

For long wavelength though (over 450nm), the absorption enhancement

cannot be explained by the anti-reflective effect, as can be observed in Fig.3.7. In that regime, the effective medium theory is therefore of no help. For this last range of wavelengths, the influence of the shape on the merit factor FOM and on the photo-current J was considered. From Fig.3.8 one can observe that

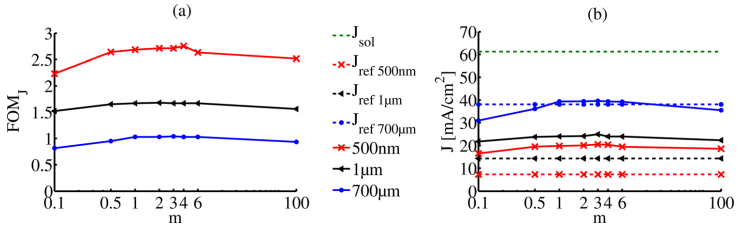


Figure 3.8: Influence of the shape on FOM (a) and J (b) [36]

thinner slabs, where light reaches the back, are more improved than thicker slabs. In thin substrates, therefore, back reflectors plays a role increasing the light path inside the material, inducing photonic light trapping. For longer wavelength thus, the holes enhance absorption via diffraction giving a light trapping effect[36].

In order to validate the model, the theoretical results were finally compared to the experimental ones obtaining considerable feedback (Fig.3.9).

Until now, a fully periodic structure for front-side patterning was considered only. However, structures presenting a random texturing, like black silicon obtained by wet chemical etching, were said to achieve very low reflectances. In addition, random nano-scale patterning obtained by plasma texturing have recently proved to reach considerable absorption values [37]. Nevertheless, the lack of periodicity in these structures prohibits them to overcome the Lambertian limit. Said that, structures featuring a global randomness with local periodicity may present interesting characteristic and considerable absorption enhancement as well. It has been shown that broader

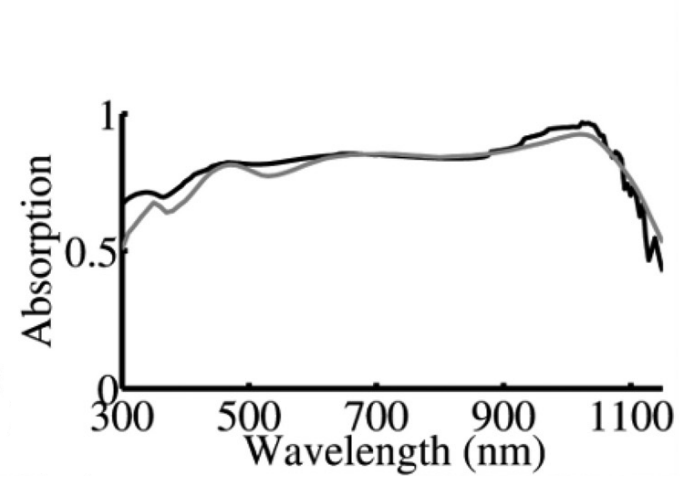


Figure 3.9: Experimental absorbtion spectrum (gray) and simulated (black) [36]

diffraction resonances compared to a periodic nanopattern, without completely losing diffraction, as it would be the case for a purely random texture, may be reached with structures featuring a partial order [38] [39] [40] [41]. Whether a fully periodic structure gives better performances or not, compared to a more disordered one, is still an open question. In the following chapters two different techniques for nano-patterning c-Si surface will be presented and the unsolved problem with periodicity will be considered again.

Chapter 4

Experimental work

In this chapter two different techniques to pattern the front side surface of c-Si will be extensively presented, describing the various experimental set up, the optical results and the advantages and drawbacks of the technologies. Precisely, at first a method that enables a globally random structure with only local order, obtained by means of colloidal lithography, will be described. Subsequently, an imprint lithography technique, enabling a fully periodic patterning will be considered. For the latter case, the effect of patterning on the electronic properties of the p-n junction will be analyzed by means of carrier lifetime measurement and actual cell performances leading to passivation study.

4.1 Hole-mask colloidal lithography

Hole-mask colloidal lithography consists in dispersing sub-micron size colloidal particles diluted in water on silicon surface, depositing a hard mask, removing the beads and etching down silicon through the holes [27] [39] (Fig4.1).

Figure 4.1: Hole-mask colloidal lithography

4.1.1 Experimental setup and process description

The substrate used for the experimentation was 700µm thick mirror-polished wafers cut in 1.5 x 1.5 cm square-shaped pieces. Those wafers were a test vehicle and the thickness was such that the front side effect could be isolated from the back side (for 700µm thicknesses, most of the light is absorbed before reaching the back side).

In order to remove any sort of undesired particle or dirt on the surface, that would have compromised the outcome of the experiments, the samples were first cleaned in acetone (CH_3-CO-CH_3) and isopropyl alcohol ($(CH_3)_2CHOH$)). This step was done by immersing the substrate in both solvents for five minutes and by performing ultra-sonication to loosen any particle adhesion to the surface.

In principle, a cleaned silicon surface with no metal contaminant or oxide on it, is hydrophobic. In our case, where a water based solution containing particles was dispersed, expecting the particles to attach to the surface, such hydrophobic characteristic was a limiting factor. Therefore, the cleaning step was followed by a surface activation step. Precisely, a plasma activation, with 18sccm of Oxygen, at 200W and at a pressure of 500mTorr was performed for two minutes in order to increase the polarity of the surface and thus the adhesion.

The colloidal particles used for our purpose consisted of polystyrene beads of

three different diameters (140nm, 200nm, 500nm). Such particles present a negatively electrical charged density. In order to improve the attachment between the colloidal particles and the silicon surface, the substrate was coated by a thin layer of positively charged material. For this purpose, PDDA (Polydiallyldimethylammonium chloride, 0.2% in water) was drop casted on silicon surface, the samples were rinsed in cold water and then dried with nitrogen flush.

Finally, the solution containing the beads (sulfate latex 0.2 % in water) was drop casted and subsequently the substrate was rinsed in cold water and dried with nitrogen.

The combination of the attractive force between the surface and the particles, the electrostatic repulsive forces between the beads and the attractive forces between the same due to capillary interaction, rising from the drying process, resulted in the structure shown in Fig.4.2, where beads with 140nm diameter are displayed. The above step was followed by the hard mask deposition,

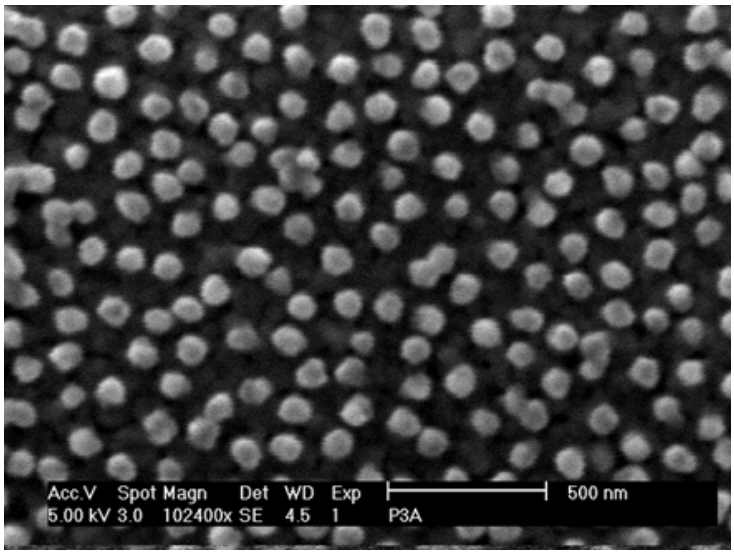


Figure 4.2: Beads distribution

precisely, 50nm of aluminum was deposited by means of an electron beam physical vapor deposition tool. This tool operates at pressures below $10^{-6}bar$ in order not to contaminate the deposition with other particles. The substrate is kept overturned facing the target, in this case aluminum. The target is then bombarded by an electron beam, obtained by thermionic emission, causing part of it to transform in gaseous form and subsequently re-deposit in a solid form on the sample. The thickness of the thin film deposited is controlled by a quartz crystal monitor. Such crystal is crossed by a RF voltage and vibrates at its natural frequency; when a thin film is deposited on the crystal, its resonance frequency gets lower and by analyzing this change, the thickness of the material is detected.

The successive step was to remove the beads, with aluminum on top, from the silicon surface. To do this a residue-free adhesive tape was used, resulting in a structure where silicon was covered by an aluminum mask featuring holes, with sizes smaller than the beads, in random position but yet preserving a local order.

The two final steps consisted in transferring the pattern from the hard mask to the silicon surface and then remove the mask. The pattern transfer was achieved by means of reactive ion etching. The latter etching technology consists of material removal by chemical reaction assisted by plasma, created by accelerating electrons in an AC electric field. In our specific case, a mixture of SF_6 and O_2 gasses (100sccmSF_6, 30sccm O_2) was used at a pressure of 100mTorr at 100W for 25 seconds, in order to etch the silicon surface. Silicon does not react with SF_6, but the presence of plasma clacks SF_6 , ionizing fluorine that reacts with silicon forming volatile gases. The above recipe allows to etch silicon for 250-300nm avoiding therefore too much material consumption. The described etching parameters were chosen in order to control not

only the etching depth, but also the lateral hole enlargement. After the pattern transfer step, the aluminum mask was removed by immersing the sample in OPD (Tetramethylammonium Hydroxide in water), an organic base used as a positive resist developer due to its reactive properties with metals; a low concentration was used, i.e. < 5wt%, in order not to etch silicon as well. Fig4.3 shows an image of the final result

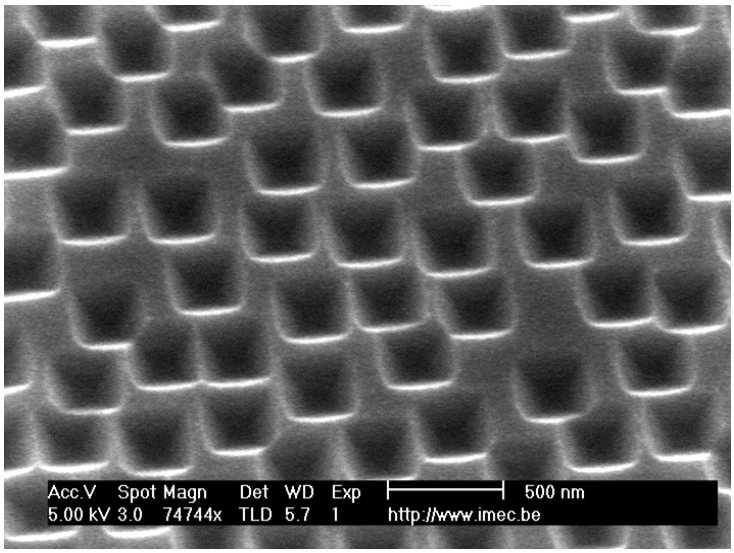


Figure 4.3: Patterned silicon surface with HCL

4.1.2 Topoghraphy characterization

An important aspect of the described process is to obtain structures where, given a global randomness of the position of the holes, a local order is preserved; precisely the desired pattern is the one that shows a fixed center-to-center hole distance, such that these distances are of the same magnitude of the holes size and, therefore, the regions presenting flat silicon are minimized. Regions with beads agglomeration or non-patterned areas where flat silicon is only present, would critically decrease the light absorption from the

material. The choice of the beads size and the etching recipe was then made in a way that the structure followed the above characteristics.

For these reasons, the idea was to develop the process starting with small beads and then integrate it with particles with higher diameters, in order to minimize the flat silicon regions by not relying only on the etching step. It was shown previously that with 140nm beads a good topography was reached. When shifting to larger beads however, e.g. 200nm diameter, many areas showed strong beads agglomeration (Fig.4.4). The origin of such agglomerations can be explained if the capillary forces between the beads are considered. During the drying process, particles are at a given point only

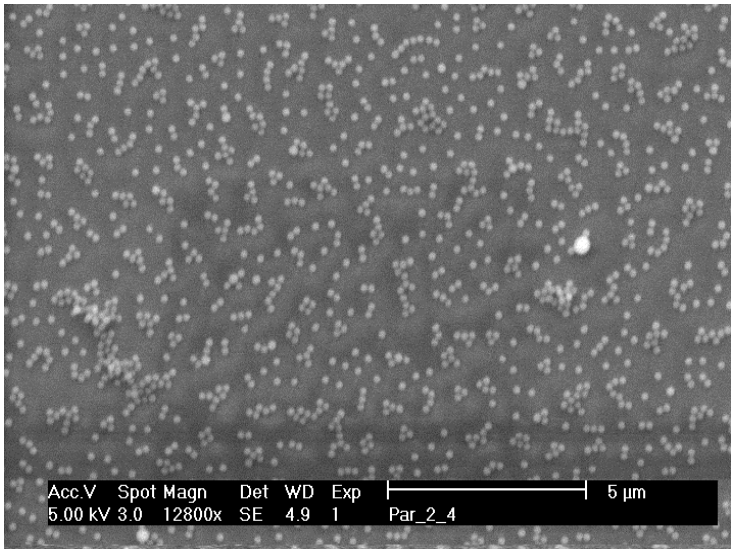


Figure 4.4: 200nm beads agglomeration

partially immersed in water with a consequent deformation of the liquid surface that give rise to capillary attractive forces between the particles. These lateral interactions caused by the curved meniscus between the beads bring to a high tendency for agglomerations. It can be shown that in case of partially immersed spherical particles with equal radii the capillary forces are

proportional to the square of the radius of the involved particles and to the surface tension of the liquid.

The approach suggested then, was on lowering the interaction between the beads by reducing the surface tension of the liquid. This was done by adding two steps to the standard procedure described above. Specifically, after the PDDA coating, a surfactant (Triton X100 0.5 % in water) was drop casted and then the sample was dried by nitrogen flush; then, after the beads casting, the samples were dipped in hot water at 95°C and then rinsed in cold water as stated before. These modifications resulted in a better patterning,

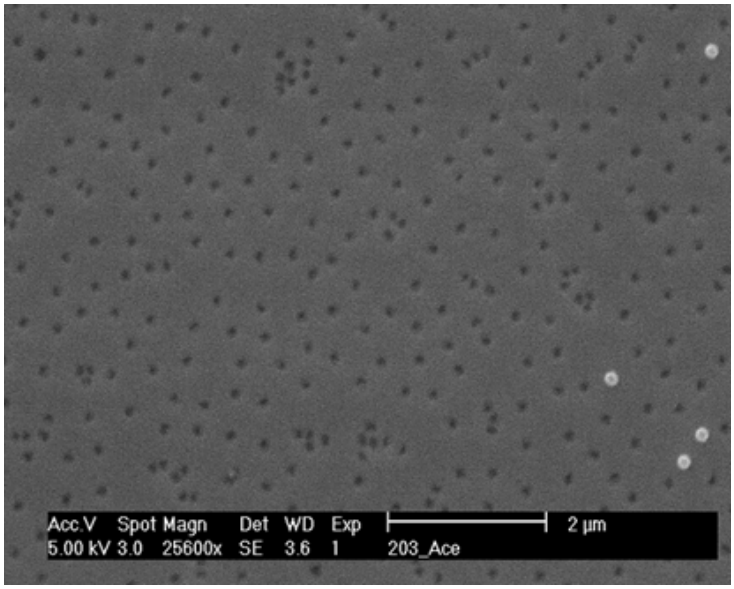


Figure 4.5: HCL with 200nm beads

with a reduced number of agglomerations, in case of 200nm beads, as shown in Fig.4.5. However, the square-law dependence of the capillary interaction with the radii of the beads was critically high when bigger beads, in our case 500nm diameter, were involved leading to non-uniform distribution and several agglomerations (Fig.4.6). in order to overcome this issue for 500nm

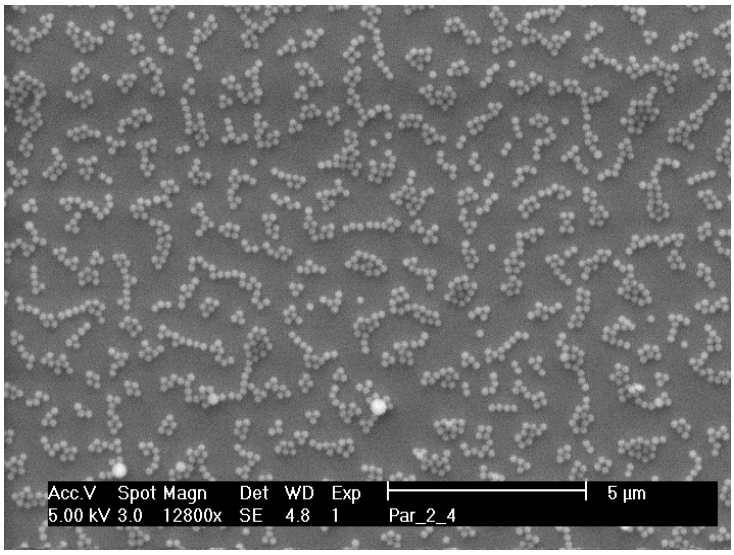


Figure 4.6: 500nm beads agglomerations

beads, different solutions were proposed. Since with 200nm particles it was observed that raising the temperature could help on our purpose, a first trial was made by keeping the samples with the beads on top in hot water for 30, 60 and 90 seconds (Fig.4.7, Fig.4.8 Fig.4.9). The conclusion was that effectively the agglomeration could have been avoided with the help of the hot water rinsing step. Nevertheless, when the rinsing time was 30s, the agglomerations were not significantly reduced, while when the sample was rinsed for 90s, the inter-beads distances were critically high, allowing large regions of flat silicon. The best case was observed with 60s rinsing, however, the ideal situation was not reached yet. Because of lack of reproducibility, as with short change in time significant changes were seen in the topography, the idea of performing HCL with beads bigger than 200nm was abandoned.

By looking at the shape of the holes (Fig.4.10), interesting considerations can be made. It was expected from the knowledge on plasma etching, that

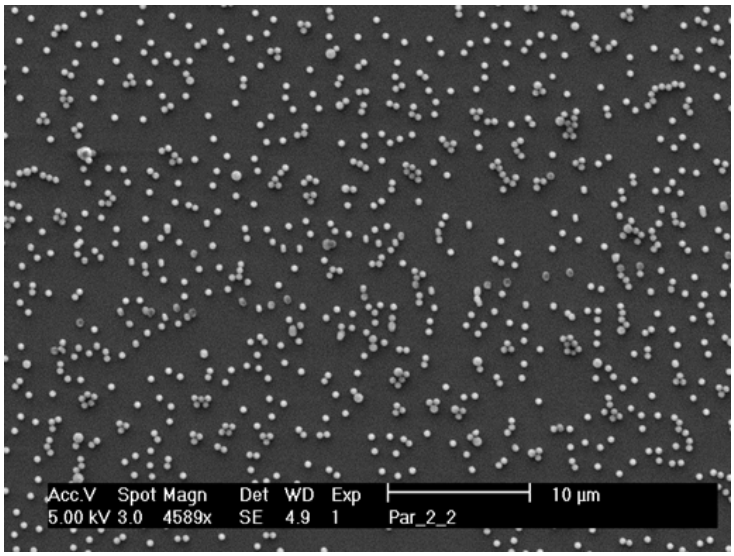


Figure 4.7: HCL with 500nm beads after 30s in hot water

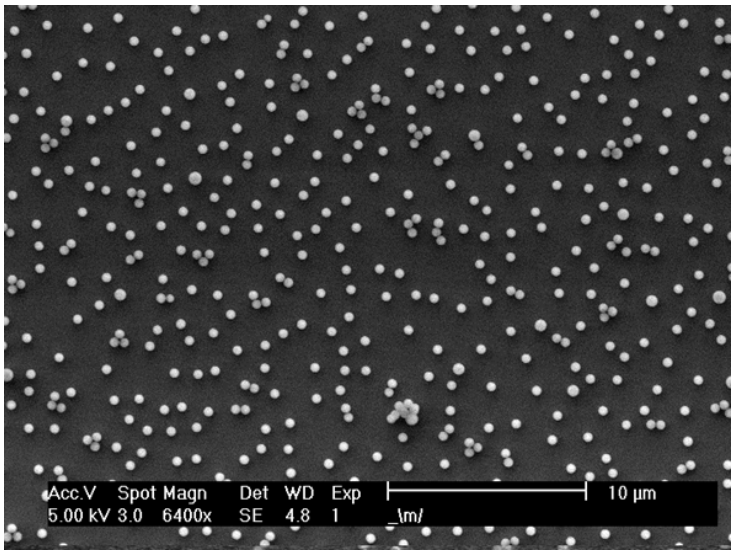


Figure 4.8: HCL with 500nm beads after 60s in hot water

it would have resulted in a isotropic etching. However, in our case, instead of having a U-shaped profile, an inverted square-based pyramid like feature, showing the $< 111 >$ planes, is obtained, reminding the profile that is com-

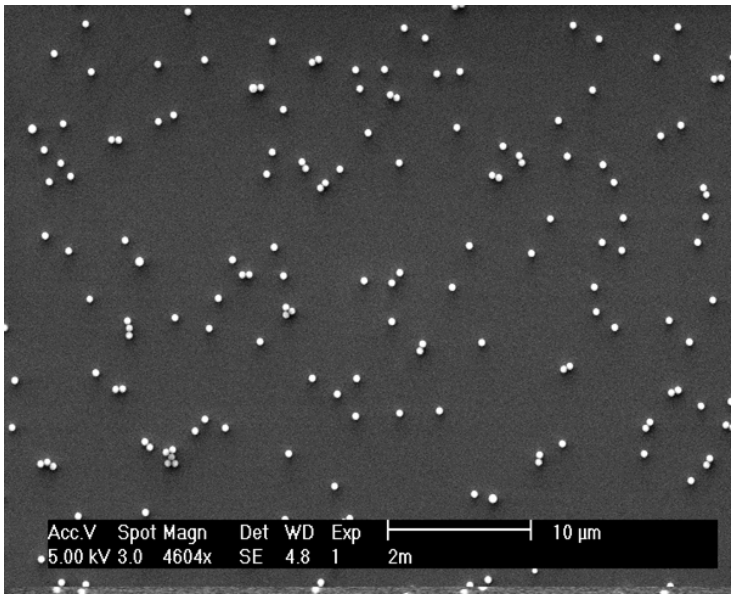


Figure 4.9: HCL with 500nm beads after 90s in hot water

mon when wet etching is performed. Such profile is explainable considering the catalysing effect of aluminium, used as the hard mask, in the reaction between SF_6 and silicon. This results in an increase of fluorine atoms which are not sufficiently energetic to break silicon bond in all crystal planes. Therefore, the $< 111 >$ planes, which have a low etch rate with respect to the $< 100 >$ and $< 100 >$ crystal orientations, are revealed [42] [43]. In order to check the validity of the statement, a different hard mask, silicon oxide, was deposited by sputtering. This process utilizes energetic particles that hit the target enabling atom ejection from it. The atoms then contribute to the formation of the thin film on the sample. Because of the high energy involved, the deposition resulted less soft than the one obtained by evaporation; in particular the lateral pressure exercised by the oxide on the beads was much stronger than the pressure exercised from aluminum. Because of this factor, the lift-off step with the adhesive tape was less effective and many

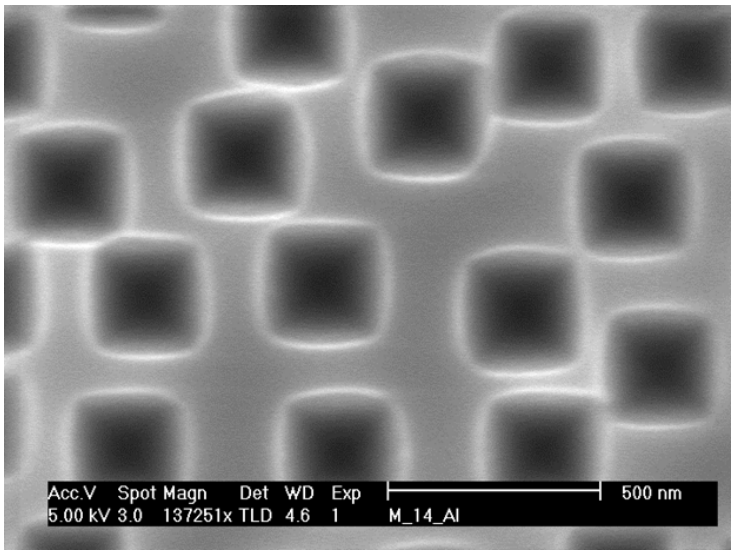


Figure 4.10: Inverted pyramids with HCL

beads were not removed afterwards (Fig.4.11). The post etch profile shown in

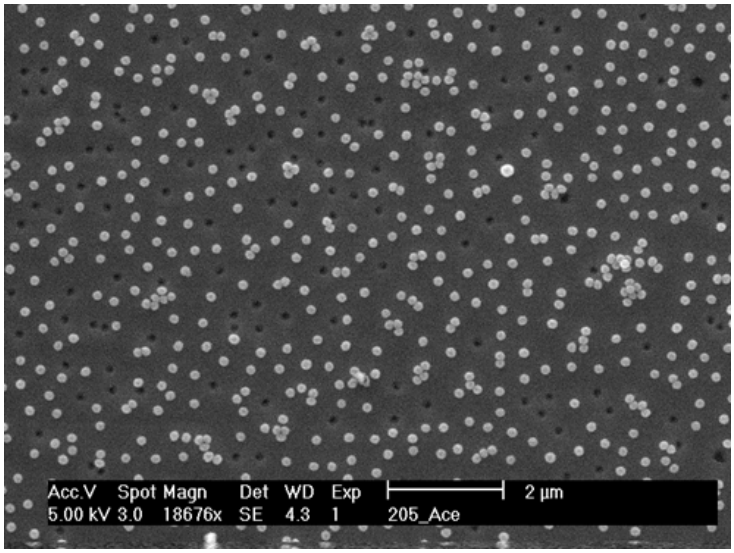


Figure 4.11: HCL with silicon oxide hard mask

Fig.4.13 exhibits the expected isotropy with U-shaped holes. This suggested the correctness of the statement according to which the hard mask played an

important role on the etching orientation.

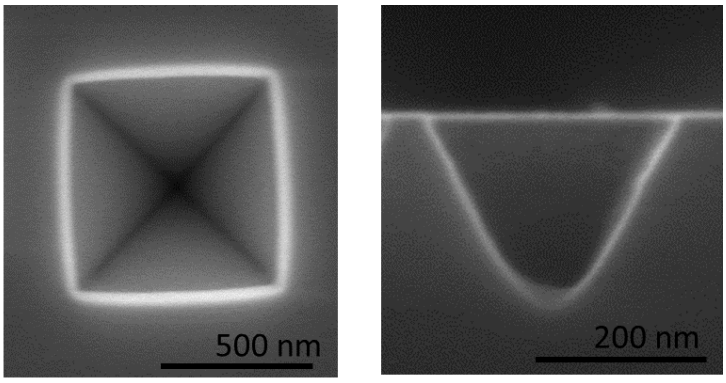


Figure 4.12: Effect of aluminum mask in HCL

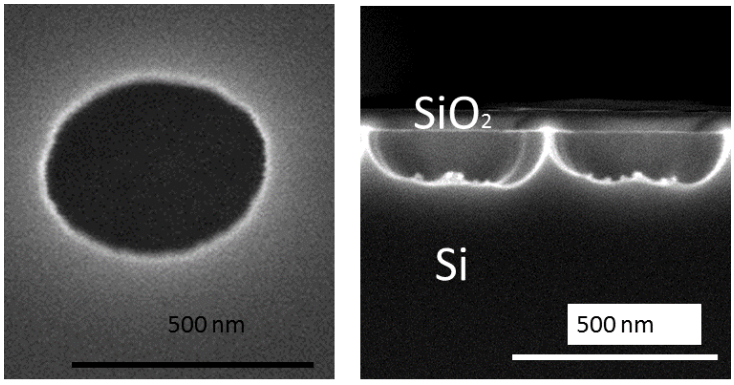


Figure 4.13: Effect of silicon oxide mask in HCL

4.1.3 Optical characterization

Here the optical results will be presented showing the absorption enhancement obtained with the described technology. The spectral absorbance, which is the fraction of incident light absorbed at a given wavelength, was indirectly calculated by measuring the reflectance and by using the relation $A = 1-R-T$. Dealing with 700µm thick wafers, the trasmittance was always

considered to be zero. For the optical characterization a xenon arc lamp, a monochromator, an integrating sphere (Fig.4.14), a silicon photodiode and a lock in amplifier were used. An integrating sphere is a photometric and radiometric tool consisting of a spherical cavity with internal walls covered with a highly diffusive reflective white coating, presenting three holes: the first one to let the light enter the cavity, a second one, opposite to the previous one, to put the sample and a last hole to place the photodiode. Light coming

Figure 4.14: Optical characterization tool [44]

from the source and after being monochromatized and reflected by an aligned mirror enters the cavity with an angle θ and hits the sample. The mirror is used to control the angle in order to avoid the light hitting regions of the reflective walls instead of the sample. The radiation is then reflected from the sample; such reflected light can be decomposed in a specular component and in a diffused component. The overall radiation inside the cavity is then collected by the photodiode and a current is generated (Fig.4.15). The current is passed through the lock in amplifier in order to decrease the noise and then presented at the user interface. From the given description, it is clear that

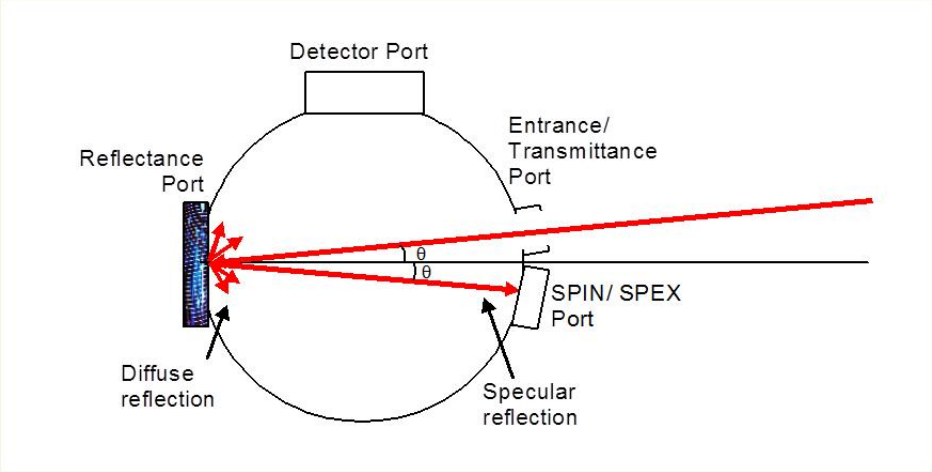


Figure 4.15: Operation of optical characterization tool [44]

an electrical current signal is obtained by the full process. In order to have information on the reflectance, a previous calibration has to be performed. This is done by replacing the silicon sample with another one that has the same diffusive white coating of the internal walls of the integrating sphere. The current detected in this case, is the maximum current obtainable, corresponding to the 100% reflectance. The spin port indicated in Fig.4.15, can be removed; when this is done, the specular component exits the material and only the diffused reflected radiation is detected. The information on the diffused radiation gives an idea on the importance of the diffraction grating in the absorption enhancement. Fig.4.16 shows the reflectance plots of flat silicon, patterned silicon surface with 500nm diameter beads and patterned silicon surface with 200nm diameter beads. It can be seen here that both samples that present the nano-patterning shows lower reflectance than flat silicon. The 500nm one though, because of beads agglomerations and flat silicon regions issues, exhibits higher reflactance with respect to the case where the sample is patterned with 200nm beads. A comparison of absorbance

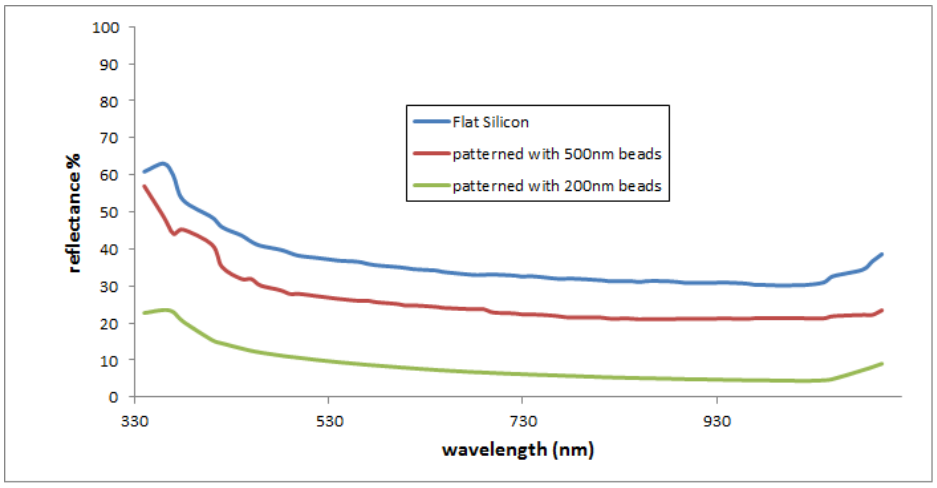


Figure 4.16: HCL reflectance plots

values between nano-patterned silicon and silicon textured with micron-size random pyramids is shown in Fig.4.17. It can be observed here that the described technology is able to reach the same enhancement achievable with the benchmark technique and, in some spectral regions, even surpass it. A

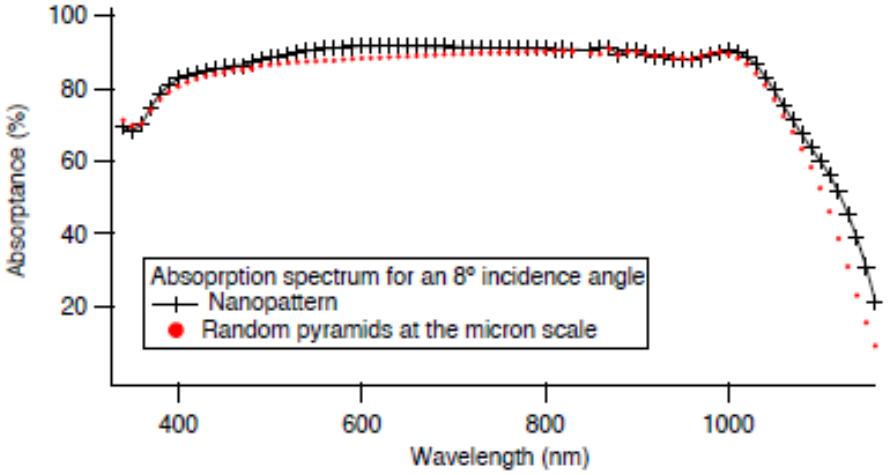


Figure 4.17: HCL and RPT reflectance plot

key aspect for the annual energy yield of solar cells is the angular evolution

of absorption [39]. When micron scale texturing is used, a geometric optics approach is needed and light is assumed to interact with flat surfaces at fixed angles. In this scenario, the integrated absorption is strongly dependent on the incidence angle. For wavelength scale texturing instead, wave nature of radiation has to be considered. In this case, increasing the angle of incidence of light has mainly the impact of slightly changing (by a cosine factor) the effective dimension of the pattern seen by the incident light Fig.4.18.

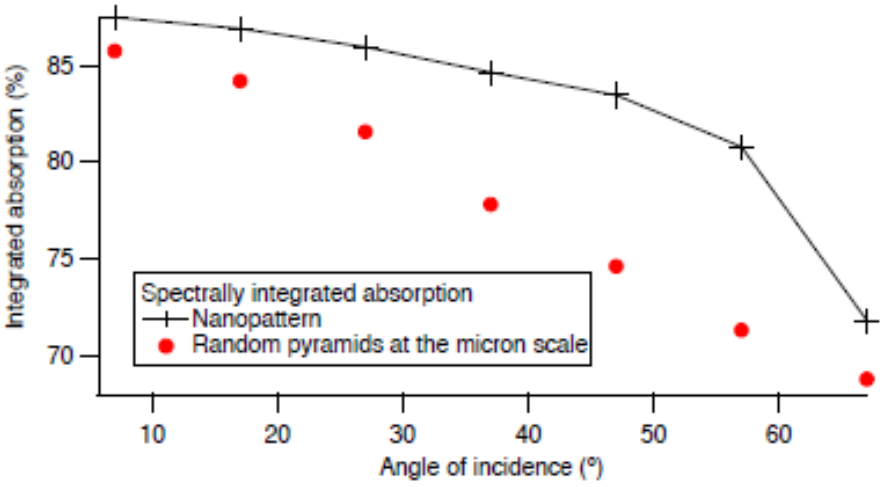


Figure 4.18: Nano-patterning angular robustness [39]

4.1.4 Conclusions and outlooks

In this section, a texturing technology, HCL, featuring nano-scale inverted pyramids for patterning front side surfaces in solar cells was introduced and thoroughly described. This method results to the formation of a pattern governed by an overall randomness but preserving a local range order. The dimensions of the pattern are such that this technology is likely to be integrated in thin film solar cells, because of the low material consumption.

Despite the low material consumption, the optical results shows even better performances compared to RPT (random pyramid texturing) concerning the absorption enhancement and the angular robustness as well. Nevertheless, in order to be integrated in solar cell industry, the technology needs further optimization. The almost totality of manual work, on one hand makes the technique extremely simple, fast and cost effective, but on the other brings serious issues related to reproducibility. Further studies has to be done also in the field of colloidal particles dispersion and agglomerations when dispersed in a solution on a surface, in order to gain more flexibility.

4.2 Nano-imprint lithography

Nano-imprint lithography is a technique that enables sub-micron scale patterning on a resist coated surface, by means of a mechanical pressure and a subsequent pattern transfer to the substrate through an etching step [15] [32] [45]. This technology therefore, needs a prefabricated stamp featuring the negative pattern of the desired one (Fig.4.19).

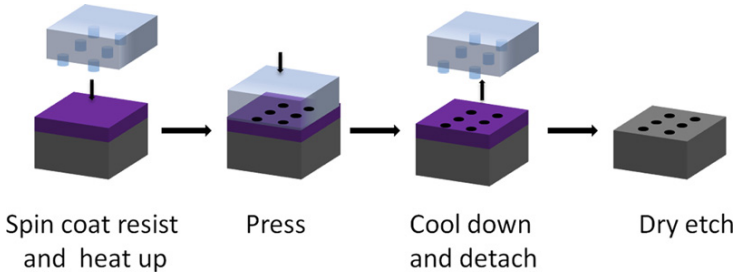


Figure 4.19: Nano imprint lithography

4.2.1 Experimental setup and process description

The substrates used for the experimental work, in order to investigate only the optical properties, were 700µm thick mirror polished wafers, cut in 5 x 5 cm square shaped pieces. As previously stated, a prefabricated stamp is needed to perform this kind of lithography. In our case the stamp consisted of a soft PDMS stamp obtained in turn by master stamps on silicon substrate fabricated with deep UV lithography. The reason why soft stamps were used instead of directly using the master stamp was that a single soft stamp can be used for several imprints unlike master stamps. This allows a process which is less time consuming, since a soft stamp fabrication is much faster than a master stamp fabrication and less expensive as well.

The soft stamp fabrication process consisted in preparing a mixture of PDMS and curing agent in ratio 10 : 1 followed by a degas step in order to strengthen the substance. Afterwards the mixture was poured in a metal mold containing the master stamp and baked for two hours at 80°C. Finally the mold was cooled down for a few hours and then the soft stamp was detached.

It is important here to notice an aspect related to the master stamp parameters, which are the period of the pillars, the height and the diameter of the same: These parameters are the one that are defined at first, in order to have a final product that images the desired one. Nevertheless the depth and width of the final product are mainly controlled by the etching step. Moreover, during the soft stamp fabrication an unavoidable mismatch shows up with respect to the master stamp features. The only parameter that remains almost unchanged between the initial deep UV lithography step and the final product is the period, which features a small growth of about 10%. In order to have a final patterned silicon surface that matches the desired properties

therefore, one has to calculate the optimal parameters throughout numerical models and proceed backwards defining the UV lithography specifications, taking always in consideration the impact of the dry etching process and the several mismatches that occurs during the full procedure.

The first step was to coat the samples with a thermoplastic polymer resist. For these kind of resists, when the temperature is risen over the glass transition temperature of the polymer, both the Young's modulus and the viscosity drop of several order of magnitude compared to tha values measured at room temperature. For this step a spin coater was used; in details, the substrate was spun with a few droplets of resist on it for 30s at a speed of 1000rpm. This speed was chosen after a few considerations about the thickness of the resist needed to optimize the uniformity of the imprint. These considerations were based on the following empirical expressions:

$$Cavitycoverage = (pitch)^2 - \pi * (diameter)^2/(pitch)^2 \tag{4.1}$$

$$Fillingpercentage = Resistthickness/(Cavitycoverage * Height) \tag{4.2}$$

The aim was to maximize the filling percentage with the given parameters from the soft stamp: assuming the filling percentage to be 100% with pitch=800nm, hole diameter=200nm and pillar height=200nm approximately. Again, these parameters are the ones featured by the soft stamp, which are slightly different from the ones of the master stamp, because of cavity coverage issues during the fabrication and material relaxations after. It was then derived that the optimal resist thickness was 160nm. The speed was then selected after consulting the data sheet of the used resist, mr-I 7010R (Fig.4.20). After the spin coating, the substrate was baked at 100°C for one

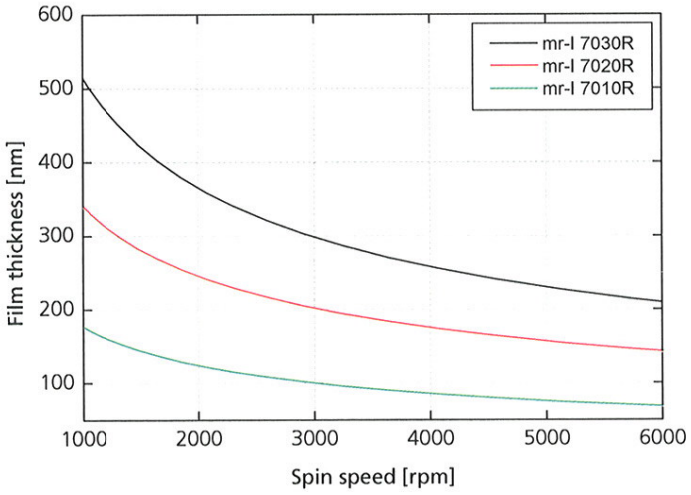


Figure 4.20: NIL resist thickness and spin coating speed

minute, in order to change the mechanical properties of the resist.
The following step consisted of transferring the pattern from the soft stamp to the resist by means of a mechanical press, which plates were previously heated up to 130°C. At first the plates were left simply touching the sample with the stamp on it for 60 seconds, without any force being applied. This was done for both the sample and the stamp to reach the same temperature. Subsequently a pressure of 1.5MPa was applied on the sample. At last, keeping the same pressure applied, the plates were cooled down to 50°C (the working temperatures were all indicated on the data sheet of the resist). The result was a silicon substrate with a patterned resist (Fig.4.21). The subse-

Figure 4.21: Patterned resist

quent step consisted in transferring the pattern from the resist to the silicon

substrate. In the standard NIL procedure this was done by performing RIE. It is important to notice here that after the resist imprint, there is no window opened directly to silicon; even where the resist is pressed by the pillars of the soft stamp, a residual quantity of the polymer, approximately 10nm, is left. The very first step with the etching then was to remove the residual resist. This was done by applying an oxygen flash (50sccmO_2) at 50mTorr at 50W for 5 seconds. Afterwards a mixture of SF_6 and O_2 gases was used to etch silicon, in details: 100sccm SF_6, 30sccm O_2, at 100mTorr at 100W for 45s. As expected, the dry etching resulted in an istropric profile revealing U-shaped features as shown in Fig.4.22, presenting holes with diameters of around 800nm and heights approximately of 550nm. Finally the resist was

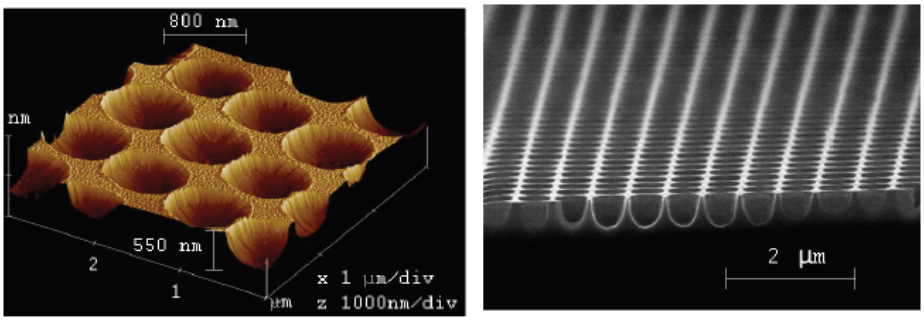


Figure 4.22: AFM (left) and SEM (right) images of nano imprinted silicon surface

removed by putting the sample in ultrasonic bath first in acetone and then in IPA for 10 minutes each.

4.2.2 Optical results and parameters optimization

The optical performances of the patterned silicon are shown in Fig.4.23. As it can be seen, a reasonable reduction in reflactance was obtained. The patterned sample was able to reach an average absorbance over 80% without

the use of any anti-reflection coating. Previously a work by Herman *et al* [36]

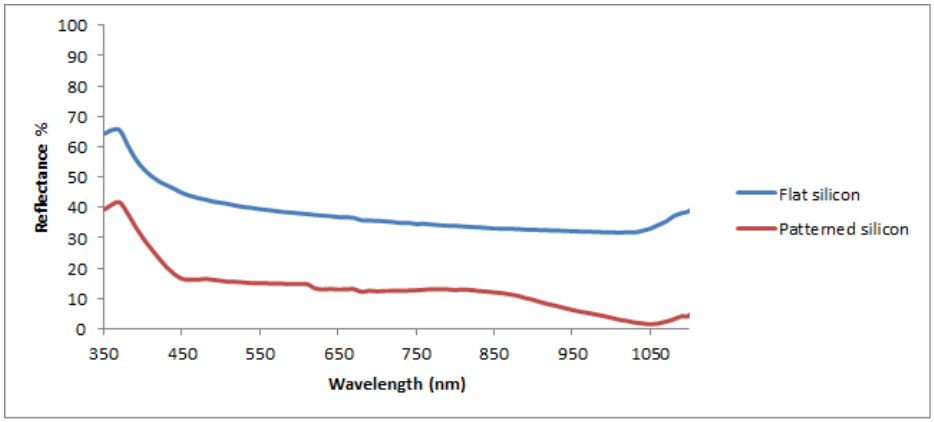


Figure 4.23: Reflectance plot of NIL-ed sample

was shown analyzing the physical reasons behind the absorption enhancement in nano-patterned surfaces. A that point, it was also said the the same work contained numerical models and study regarding the the optimal parameters to be used in order to have the best performances. Briefly, it is stated in the work, that the optimal height of the holes and period increases with the thickness of the material. This is explained in terms of diffraction inside the material and interference between the diffraction orders. Specifically, the period in increased for thicker slabs in order to diffract low energy light in the material, while the height is responsible for the constructive interference between the diffracted orders. In the same work three different slab thickness were considered and the extracted values are shown in Tab.4.1 (these values refers to the parameters of the final product). Since the aim of the our work was to integrate the nano-patterning technique in thin film technology, specifically the final objective was to fabricate solar cells with thicknesses in a range of 1-40µm, it was decided to fabricate master stamps featuring smaller features, principally the period. From the deep UV process, master

	500nm c-Si slab	1µm c-Si slab	700µm c-Si slab
Period	500nm	500nm	700nm
Height	300nm	500nm	700nm

Table 4.1: Optimal parameters

stamps with 600nm period, 400nm pillar diameter and 230nm pillar height, were fabricated. Reminding that the depth and the width of the final product were controlled by the etching step and that the period generally presented a 10% growth, an absorption enhancement was also expected for 700µm thick wafers, with respect to the previously presented results.

With smaller features size, several issues related to the soft stamp fabrication process arose. The detachment step of the soft stamp from the master stamp resulted in a critically damaged soft stamp. Fig.4.24 show the topography of a silicon substrate imprinted with damaged soft stamp. This

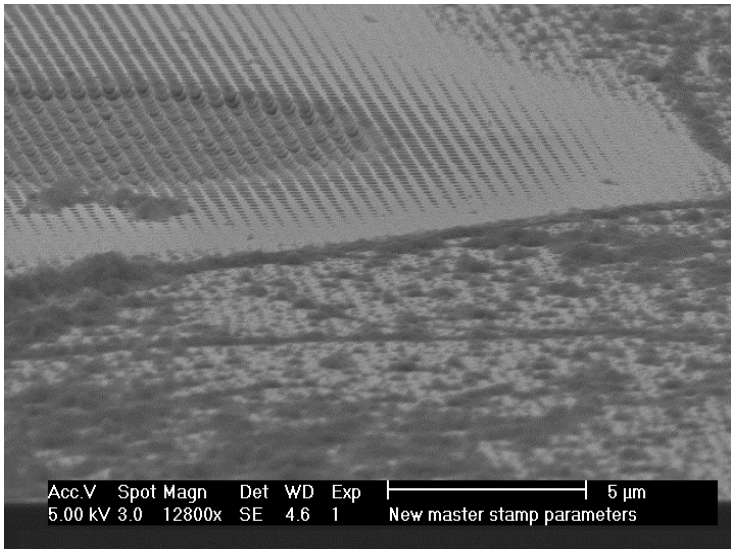


Figure 4.24: Damaged imprint

problem was partly solved by changing the holes in the master stamp from

a square shape to a trapezoidal one (Fig.4.25). With such modifications it was possible to fabricate a few soft stamps. Another issue regarding the new

Figure 4.25: New master stamp hole shape

parameters was related to the spin coating step. As previously stated the spinning speed and accordingly the resist thickness was selected in order to optimize the imprint step and was strongly dependent on the stamp parameters. Reusing the empirical expression showed above, a thickness of 130nm was chosen as the optimal one.

At first though, a standard NIL was performed with the same specifications as above; The optical results and the topography are shown in Fig.4.26, Fig.4.27. Subsequently, 2000rpm speed was used to spin coat the resist

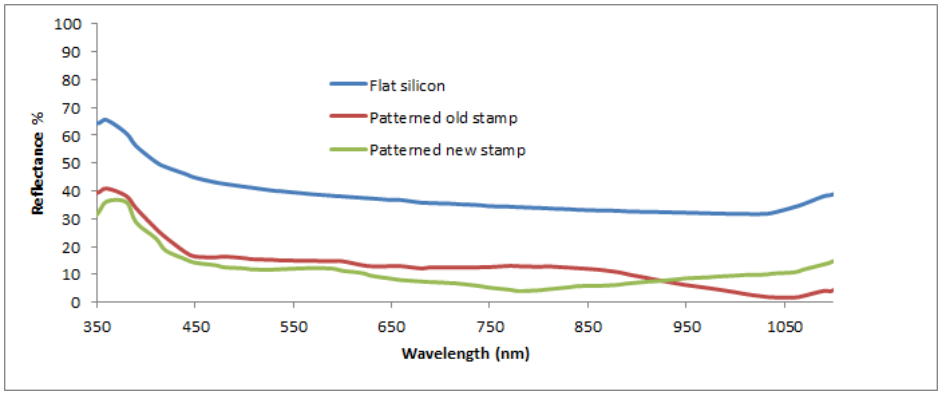


Figure 4.26: Standard NIL with new parameters

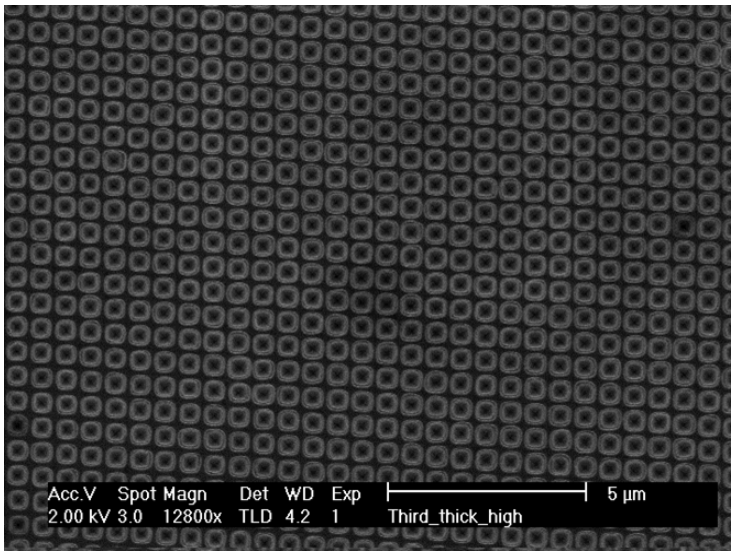


Figure 4.27: Standard NIL with new parameters topography

resulting in a resist thickness of 120-130nm. The reflectance plot is shown in Fig4.28 keeping the previous results, with 160nm resist, as reference. It

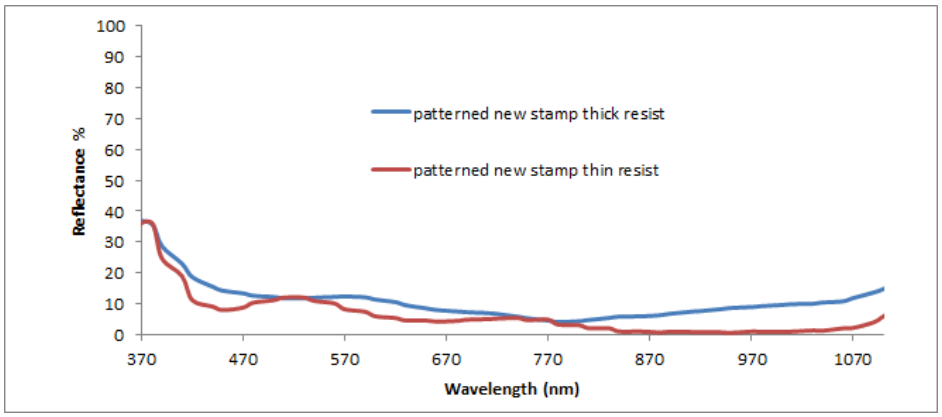


Figure 4.28: NIL with new parameters and thin resist

can be seen here that by thinning the resist a lower reflectance is obtainable. This can be explained with the fact that with a thinner resist and by using the same etching recipe, the sample ran out of resist and the over etch made

the surface rougher causing more scattering. Here an important consideration has to be made: the objective was to integrate the patterning in a solar cell where not only the optical performance is important, i.e. the capacity to absorb the maximum quantity of light, but the electronic performances are as well; the final product must be able to guarantee a reasonable collection of photo-generated carrier. Therefore, if one one hand the over-etching and the consequent roughening seems to enhance absorption, on the other, it may be responsible for severe defect formation on the crystal lattice. Fig.4.29 and Fig.4.30 show SEM images of the surface of the patterned silicon when a thinner resist as above was used. It can be noticed, from the cross section

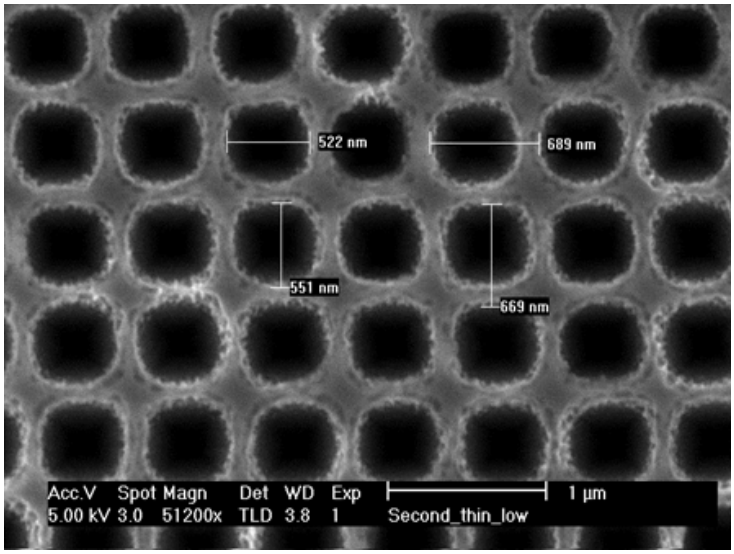


Figure 4.29: NIL with new parameters and thin resist topography

picture, that the silicon surface appears to be slightly damaged by the over etching. An even thinner resist was tried, to see if uniform imprint could be obtained, by putting the spinning speed to be 3000rpm, resulting in 100-110nm thick resist. Fig.4.31 and Fig.4.32 show that in this case the pattern was severely damaged in some regions, regions that are likely to contribute

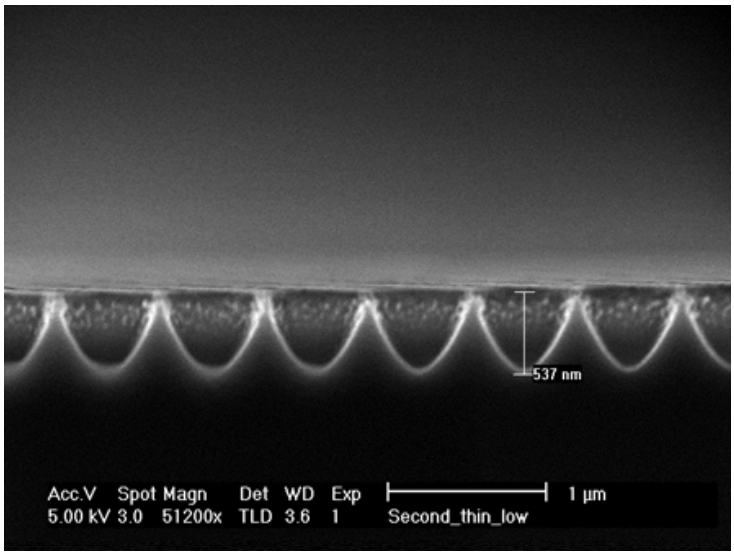


Figure 4.30: NIL with new parameters and thin resist topography

to significantly poor electronic properties. Previously the optical results of

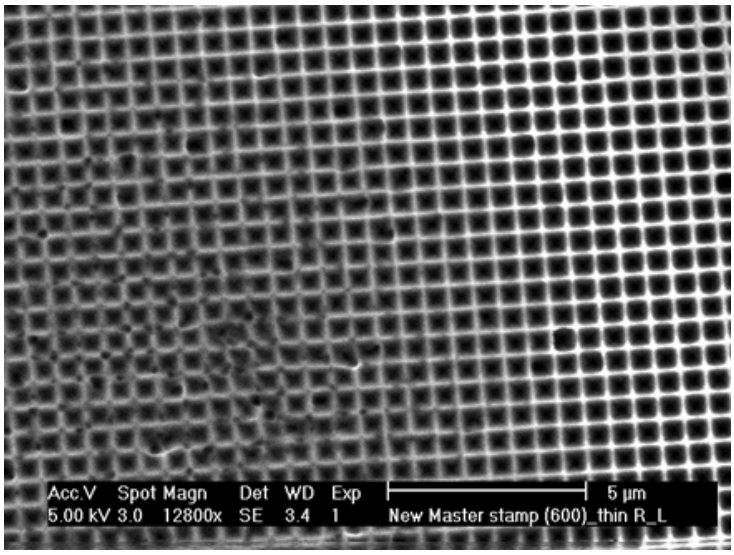


Figure 4.31: NIL with 110nm resist: surface topography

nano-imprinted substrates were presented. It was showed that the technique provides efficient light trapping and enhances light absorption as expected

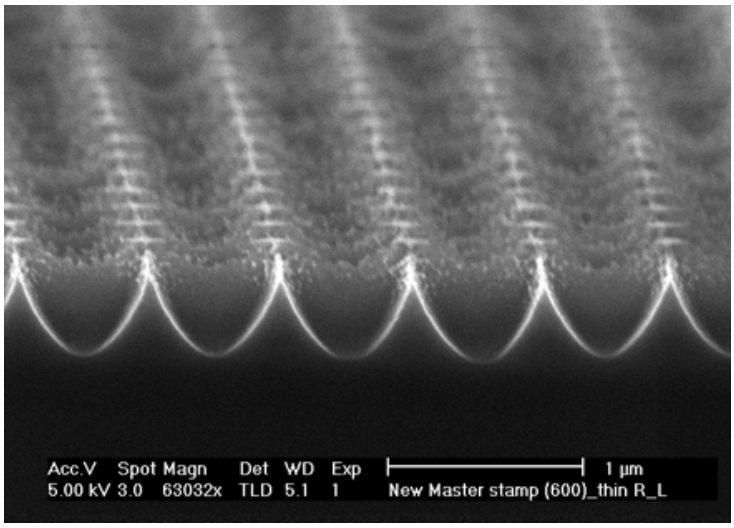


Figure 4.32: NIL with 110nm resist: cross section

from simulation. From the very simulations, it was also shown that by shifting to optimal parameters, further improvement in light absorption can be achieved. The standard procedure though needs to be changed in order to be compatible with smaller features. Practically, several issues arises during the detachment step in the soft stamp fabrication process. To avoid such issues, stronger substances than PDMS may have to be considered. Moreover, a good imprint is strongly dependent on the resist thickness and also the spin coating step has to adapted to the new structures. At last, provided that an optimal resist thickness is found, the RIE recipe has to be readjusted, to avoid damaging the silicon surface.

4.2.3 Cell fabrication

In the previous section a well founded technology for patterning front side surfaces of thin film solar cells, in order to promote light trapping, was described and optical results were analysed. Here the effective integration of

such texturing in a cell level will be described and the overall results will be presented and discussed. The cell run included also a study on the effect of the doping level on the total efficiency, but for the topic of this report, those results will not be analyzed here.

Experimental setup

For the cell fabrication, a 1µm thick c-Si substrate, fabricated with epifree process, p-type doped was used. Flat silicon to be kept as a reference and NIL-ed silicon, with non optimal parameters, were used for this study. The main steps for the cell fabrication are briefly listed below.

At first the passivation layer and the emitter were deposited on the sample. For this purpose, *i*a-Si and n^+a-Si were deposited by plasma enhanced chemical vapor deposition. This technique consists of one or several gases being decomposed, by means of ion bombardment (plasma), on a hot substrate in the reactor chamber. Later ITO, serving as anti reflection coating, was sputtered. Afterwards, the emitter contact was evaporated with an e-beam evaporator, right after a photolithography and a subsequent etching step. For the emitter contact titanium, palladium and silver were used, while for the back contact, aluminum was utilized. The final cell structure is shown in Fig.4.33.

Cell characterization and discussion

Once fabricated, the cell were characterized optically as well as electronically to study the overall behaviour. Fig.4.34 and Fig.4.35 show the absorbance plots of flat silicon and patterned silicon, both with anti reflection coating.

From the plots it is clear that the nano-patterned substrates, in case of both low doping level and high doping level, present higher absorption with

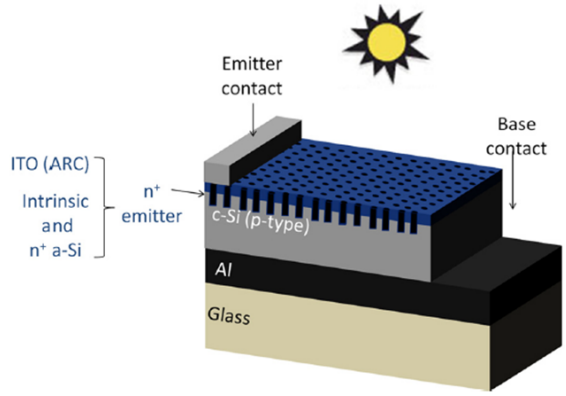


Figure 4.33: Epifree cell structure

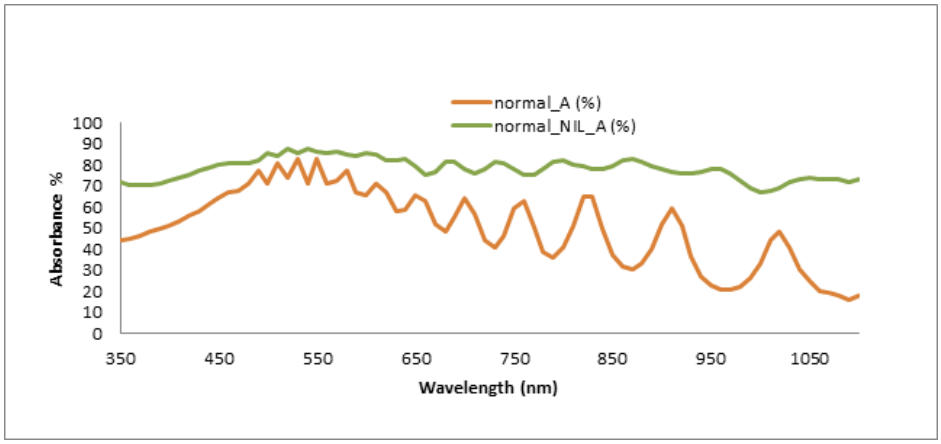


Figure 4.34: NIL-ed and flat silicon absorbance

respect to a flat silicon surface with anti reflection coating.

An overall picture of the cell performances is reported with the IV curves in Fig.4.37 and Fig.4.38 and the respective values in table 3. For the IV characteristic, a steady state illumination by lamps mimicking AM1.5G spectrum and irradiance was applied. The experimental setup is shown in Fig.4.36.

It is clear from the IV curves and respective values that not only the patterning technique was correctly integrated in the cell but it had effectively

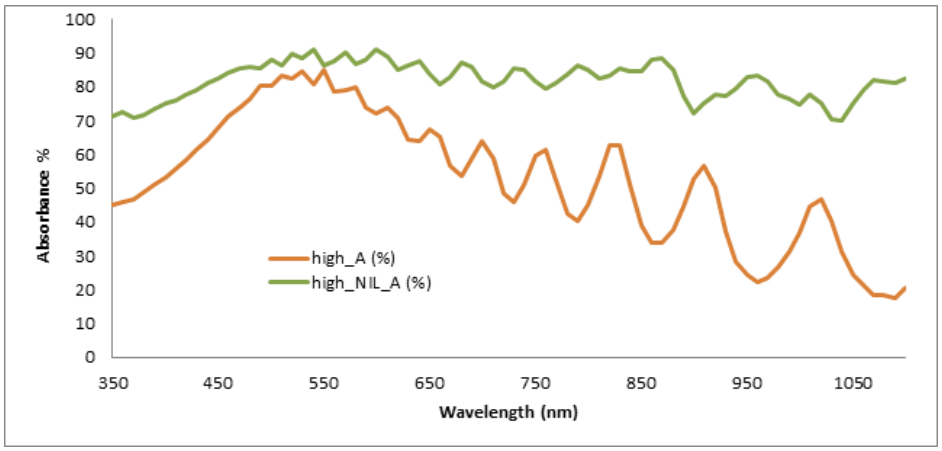


Figure 4.35: NIL-ed and flat highly doped silicon absorbance

	$J_{sc}[mA/cm^2]$	$V_{oc}[mV]$	Fill Factor [%]	Efficiency [%]
Flat	13.3	324.7	57	2.45
NIL-ed	14.8	260.6	65.7	2.5

Table 4.2: Normal doping cell characterization

	$J_{sc}[mA/cm^2]$	$V_{oc}[mV]$	Fill Factor [%]	Efficiency [%]
Flat	7	626.5	39	1.74
NIL-ed	12.5	460.6	58	3.35

Table 4.3: High doping cell characterization

increased the absorption of light, promoting light trapping, resulting in a higher J_{sc}. Nevertheless the efficiency values were significantly low as compared to the ones conventionally obtained with thicker cells. An interesting point is to notice how on one hand the effect of the nano-patterning was to increase the generated current but on the other was to reduce the V_{oc}. The reduction of such parameter can be explained by considering the parasitic resistive losses, which effects can be seen also in the fill factor values, and recombination losses. The last ones, results in a decrease of the carrier

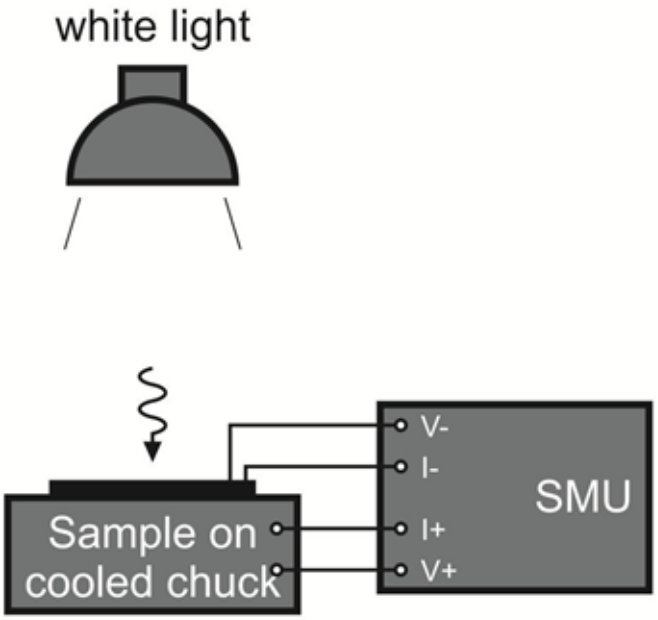


Figure 4.36: Solar simulator

lifetime.

Conclusions and outlooks

For any crystalline material, the surface represents an interruption of the lattice periodicity. Such interruption causes the formation of dangling bonds and defects which act as recombination sites. In thin films, like in our case, where the surface to bulk ratio is reasonably high compared to thicker films, the negative effect of surface recombination becomes significantly high. From Tab.4.2 and Tab.4.3 it can be observed how the open circuit voltage in flat

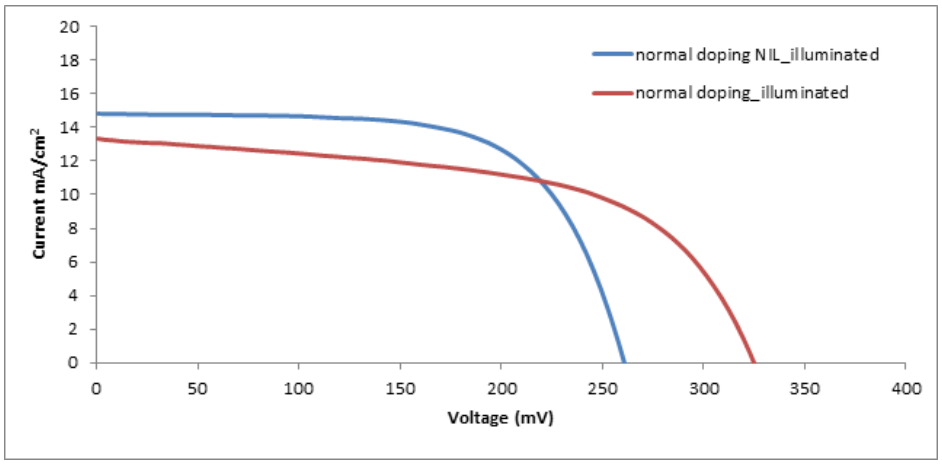


Figure 4.37: Normal doping IV curve

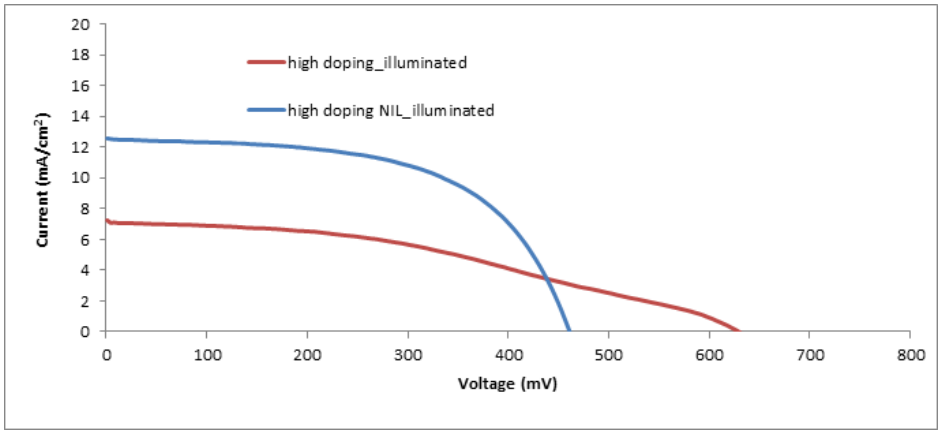


Figure 4.38: High doping IV curve

silicon is considerably low compared to the common values obtained for PV cells, which is around 0.7 V. However it was shown that NIL-ed sample reached even lower values of V_{oc} than flat silicon. The first consideration to be made is that by simply texturing the surface, the surface to bulk ratio is increased. Moreover, by performing NIL, lateral interruptions of the crystal lattice periodicity take place as well, resulting in more dangling bonds and defects. These two factors contribute in lowering the carrier lifetime inside

the material and, even with a well acting passivation layer, they represents unavoidable fabrication losses. Finally, as already stated, the dry etching process is a technology that make use of ion bombardment; this is likely to further increase the number of defects on the surface. In addition the U-shaped profile obtained by dry etching, conduces to a dis-uniform deposition of the passivation layer. In order to fabricate efficient thin film solar cells then, the passivation aspect has to be taken deeply in consideration.

4.2.4 Passivation study and post etch treatments after NIL

It has been shown that by nano-texturing the front surface on c-Si solar cells, by means of nano imprint lithography, a reasonable enhancement in light absorption is obtainable with a consequent increase of the photo-generated current, with respect to the flat silicon case. The effect of the such lithography though is to critically decrease the open circuit voltage as well. Omitting here the effects of resistive losses, the reasons for this reduction are mainly to be found in the dry etching process [46].

Hereafter, a study on the effects of NIL on carrier lifetime is presented. Secondly, possible post etch treatments in order to reduce the defects caused by plasma etching are shown. At last, an alternative etching technique, that results in a different profile from what has been described, is introduced.

Experimental setup

For the study, the following method was followed: keeping one sample as a flat reference and one as NIL-ed reference with no treatment, both with passivation on both sides, NIL was performed on polished 200µm flote zone silicon substrates with sufficiently high bulk lifetimes.

On a first series of samples, annealing at three different temperatures, after NIL, was tried to remove the defects. Annealing consists of a heat treatment, performed in a proper oven, that enables to refine the structure, in our case the silicon surface. For this study, 400°C, 450°C and 500°C heating temperatures were used.

On a second series of samples wet etching as post dry etching treatment was used: the aim was to completely remove a few nanometres of silicon. For this purpose, polyetch solution (H_2O:BHF:HNO_3=10 : 1 : 40) was used. These solution has a typical etch rate of 100nm/min. For this study, the samples were immersed in the solution for 20s.

At last, a full replacement of the plasma etching step with a wet etching step was proposed. The procedure is described in the following section.

Afterwards, all the sample were passivated with $i, n^+a - Si$, deposited via PECVD technique. Thin films of hydrogenated amorphous silicon (a-Si:H) can be deposited on crystalline silicon surface; their bandgap is wider than that of crystalline silicon and in the intrinsic form they can reduce c-Si surface state density by hyrogenation. Doped a-Si on the other hand, has a deteriorating effect. The reason why it was deposited, was that in this study the aim was to have realistic results and not considering the emitter would have lead to an over-estimation of the lifetimes. This process was done after a cleaning step where the samples were first immersed in piranha solution (H_2SO_4:H_2O_2=4 : 1) for 10 minutes at 90°C, to remove any organic matter an metal oxides, and then HF dipped (H_2O:HCL:HF=20 : 1 : 1) for 2 minutes, in order to remove the native oxide.

Finally the samples were characterized to evaluate the minority carrier lifetimes. This step was performed by means of a photoluminescence and calibrated photoluminescence tool, able to show a map of the effective minority

carrier lifetime and give QSS-PC (quasi steady state photo-conductance) results. In PL measurements, the sample is illuminated by a IR light source giving rise to a photo-generation of free carrier inside the material. The generated carrier recombines radiatively and this last signal is detected by a IR camera. A map of the PL signal deriving from the whole surface is then generated. It has to be considered here, that silicon is an indirect band gap material and the major recombination ways are Auger and SRH ones, therefore, these are the ones that has to be minimized to have good electronic properties. Since two different recombination are mutually exclusive, the regions where the radiative recombination is dominant, the other two are negligible. In this picture, higher the radiative recombination, higher the effective carrier lifetime. PL measurements give a spatial map of the recombination sites on the material, but is not capable to present quantitative values. In order to gain information on an average carrier lifetime over the whole surface, calibrated PL was used. This technique is based on the following assumptions: the carrier photo-generation results in an increase of the wafer conductance given by

$$\sigma_L = q(\Delta n \mu_n + \Delta p \mu_p)W = q\Delta n(\mu_n + \mu_p)W \tag{4.3}$$

where Δn and Δp are the excess carrier density and equal to each other, and W is the wafer width. In a steady state, the photo-generation is exactly balanced by the recombination. Equaling the two rates as current densities and expressing the recombination rate in terms of carrier lifetime, the following relations are obtained:

$$J_{ph} = J_{rec} \qquad J_{rec} = (q\Delta nW)/\tau_{eff} \tag{4.4}$$

$$\tau_{eff} = \frac{\sigma_L}{J_{ph}(\mu_n + \mu_p)} \tag{4.5}$$

In the PL calibrated tool, the conductance increase is measured by a coil positioned below the wafer, while the photo-generated current is measured by means of a reference solar cell. In order to have a good calibration with the reference cell, reflectance measurements on the sample, prior to this step, were made.

Results and discussion

The measured reference carrier lifetime were for flat silicon $3.2ms$ and for NIL-ed silicon $44\mu s$ The results of annealing as a post etch treatment are depicted below showing the PL map and the average minority carrier lifetime values Fig.4.39, Fig.4.40, Fig.4.41. The lifetime values show that no improvement was achieved by performing an annealing after NIL. Moreover, by increasing the temperature, a trend was found towards lower lifetime values. All this can be explained by assuming a diffusion of defects in the substrate caused by the heat, bringing to a worsening of the electrical properties of the substrate.

In Fig.4.42 the result of the wet etching as post etch treatment is presented. The interesting part of this test was that it could have actually stated the entity of the damage caused by plasma etching: since a few nanometres of material was completely removed, most part of the damaged portion was likely to be dismissed. As expected, the lifetime value was considerably high with respect to the only NIL case. Precisely an enhancement of around seven times was obtained by removing approximately 25nm of material. This result on one hand indicated a possibility to partially overcome the recombination issues of NIL-ed samples and on the other, helped to learn quantitatively the

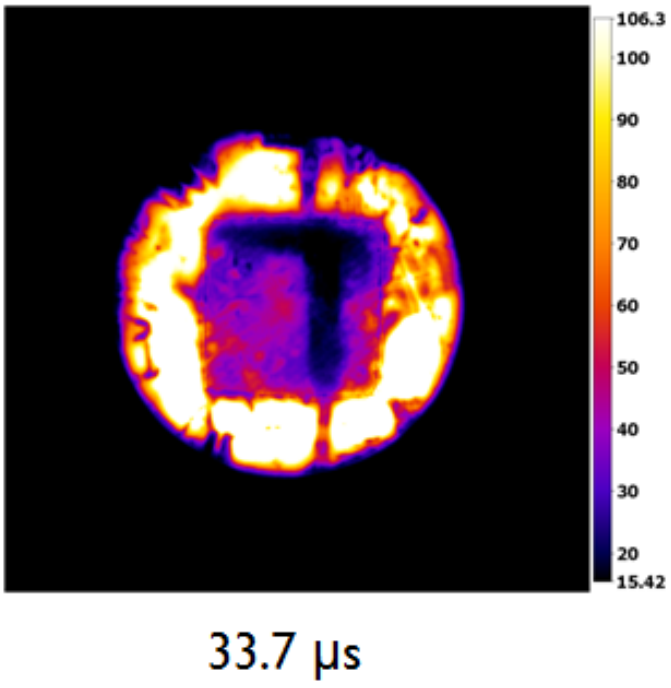


Figure 4.39: Carrier lifetime after 400°C annealing

effect of plasma etching on their electronic properties.

At last, the results of a wet etched sample is presented in Fig.4.43, together with a SEM image of a typical wet etched sample profile (Fig.4.44). As it can be seen, the carrier lifetime was remarkably higher compared to the only NIL-ed sample case once the dry etching step was replaced by a wet etching step. Wet etching is achieved by immersing the sample in hydroxide solution. In crystalline silicon the (111) plane has the highest packing density with the lowest number of out of plane dangling bonds. This makes such plane the lowest reactive of all resulting in a very low etch rate compared to the other planes. Since the wet etching process rely only on chemical reactions, which are much softer than the ion bombardment provided by plasma etching, an anisotropic profile is obtained and the (111) planes revealed. This technique

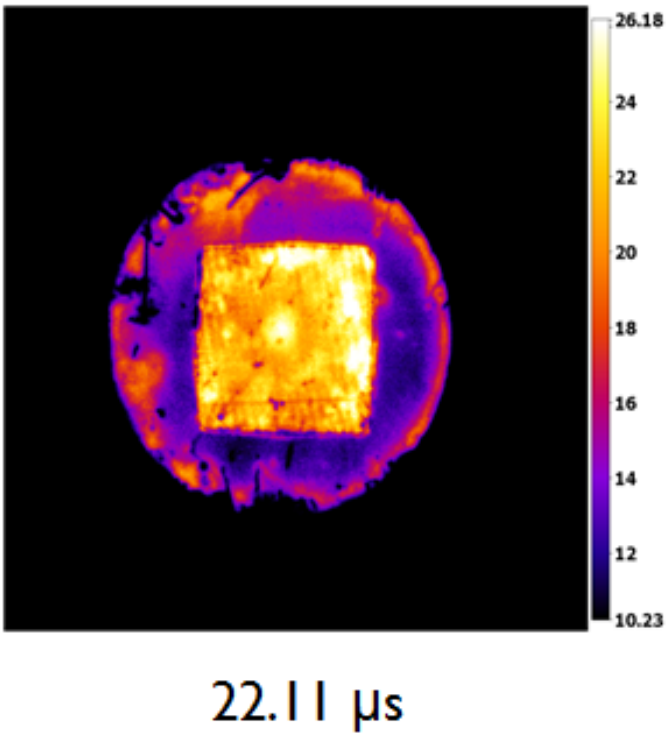


Figure 4.40: Carrier lifetime after 450°C annealing

provides no damages caused by plasma, lower number of dangling bonds and more uniformity of deposition of the passivation layer. The experimental setup in order to perform wet etching and the technical difficulties related to it is later described in this report, in the dedicated section.

In conclusion, a passivation study was done on NIL-ed samples by analyzing different post dry etching treatments to remove the damages caused by plasma.

It was found that by refining the surface through annealing, a deteriorating effect was achieved, probably because of the diffusion of the defects in the bulk.

By completely removing a few tens of nanometres by means of wet chemical

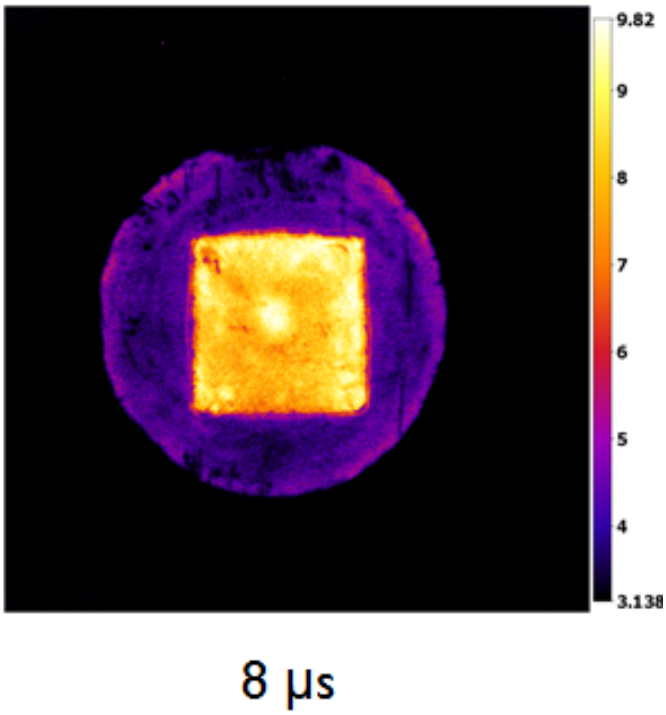


Figure 4.41: Carrier lifetime after 500°C annealing

etching, the carrier lifetime increased of seven times with respect to the case where no treatment was done after NIL. Such treatments thus can be considered as a valid process in order to increase the V_{oc} of nano-textured solar cells.

At last the effect on carrier lifetime of wet etching as the pattern transfer method, was shown. Precisely lifetime values comparable to the ones conventionally obtained after micron size texturing in thick substrates were shown, making the wet etching process a certain candidate to be integrated in the NIL procedure.

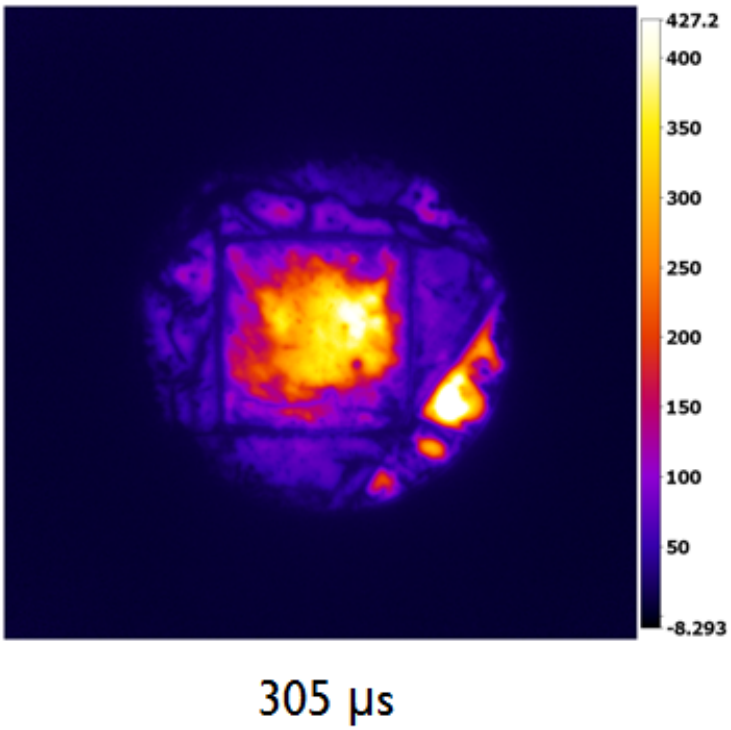


Figure 4.42: Carrier lifetime after poly-etch

4.2.5 Wet etching

In this part, a more detailed description of the wet etching process, to transfer the nano-texturing on silicon surface, is given.

Experimental setup

The idea was to perform NIL as it is described in the standard procedure and then replace the plasma etching step by an alkaline etchant. However, the polymer resist used for the imprint is not compatible as a hard mask when such chemical etchants are used. The alkaline etchant used for this purpose was an aqueous solution containing TMAH (Tetramethylammonium hydroxide, 25 % in water at 80°C). The choice of TMAH over KOH was made

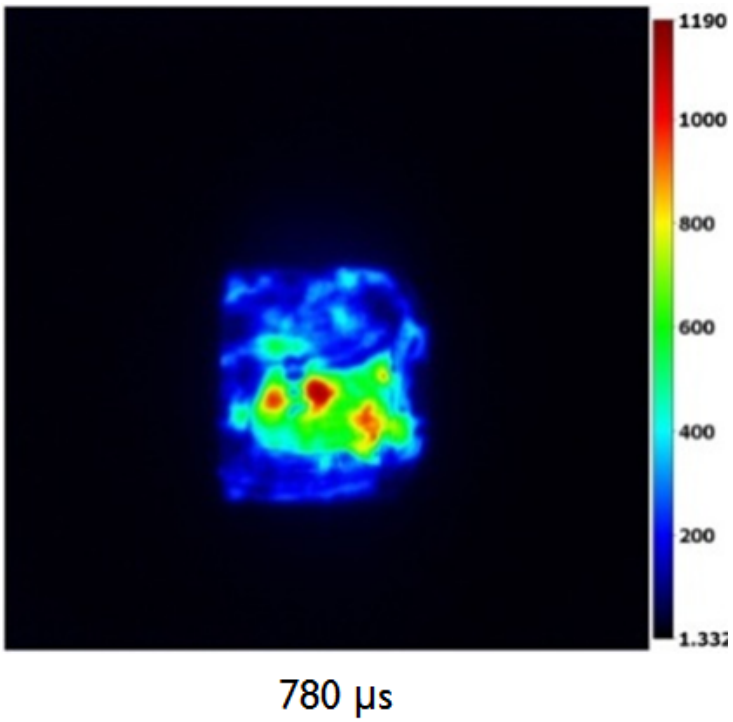


Figure 4.43: Carrier lifetime after wet-etching

because it contains less metal ion contamination [47]. Since the TMAH mixture does not contain HF, silicon oxide was used as the hard mask.

The full process consisted of depositing 110nm of SiO_2 on flat c-Si by PECVD, coating the oxide with the thermoplastic resist, perform NIL, dry etch silicon oxide, with the resist acting as hard mask, so that a window was opened to silicon and, finally, TMAH etch silicon for 60s. As it will be cleared, the most critical step in the full procedure consisted in the dry etching step of the oxide.

The etching recipe used was a mixture of SF_6 and O_2 gases (100sccm of SF_6 and 10sccm of O_2) at 80mTorr at 200W. Several attempts were made to figure out the necessary time to open the window to silicon. The first trials reported that by running the recipe for 25s, approximate 50 % of the oxide

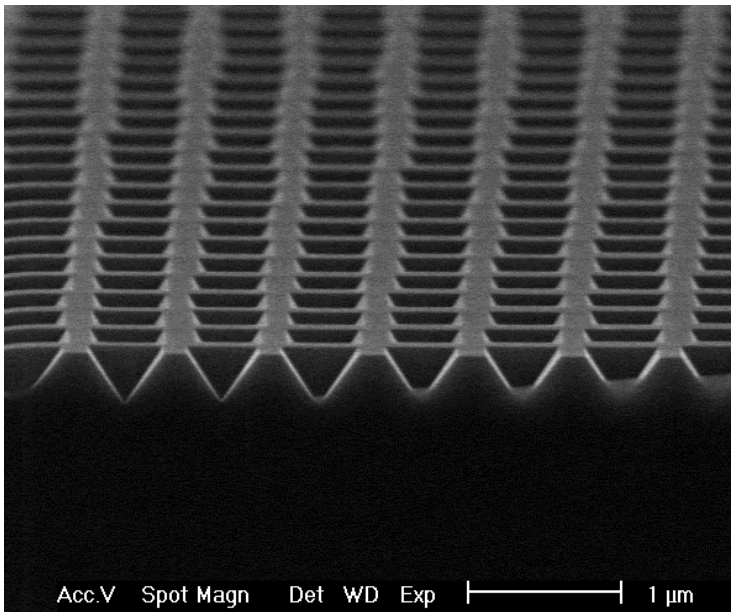


Figure 4.44: Wet-etched sample topography

was removed Fig.4.45. By assuming the etching rate to be linear, 60s was

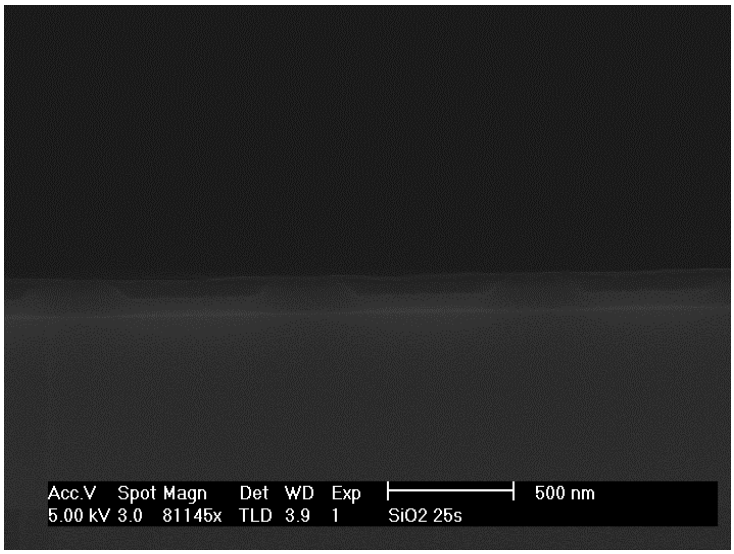


Figure 4.45: Silicon oxide etching after 25s

subsequently successfully utilized Fig.4.46. Nevertheless, several issues re-

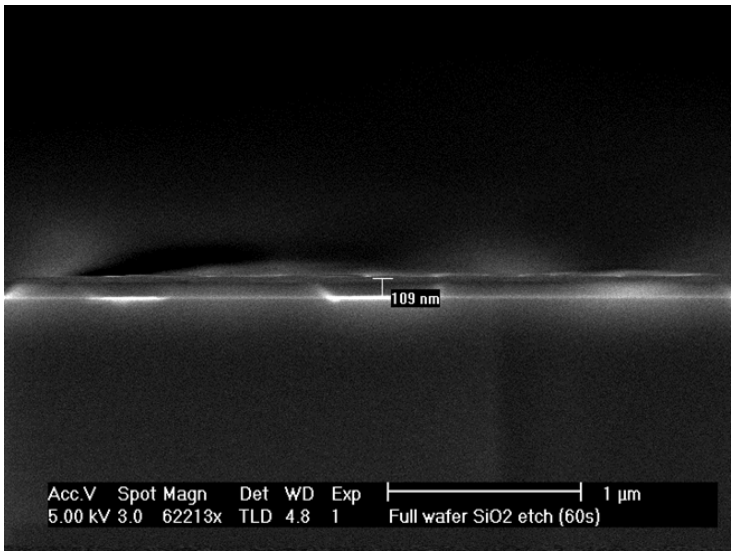


Figure 4.46: Silicon oxide etching after 60s

garding the reproducibility related to plasma etching arose. Two important considerations are that at first, etching recipe did not show a good selectivity between silicon and silicon oxide and, moreover, a mismatch of a few nanometres was observed between two samples etched with the recipe and for the same amount of time. This small mismatch is negligible when dry etching is used to transfer the pattern but for wet etching case it is fundamental to avoid under-etching, as that would result in a mask without any aperture, and over-etching as well. To better understand the reason why over-etching may represent an issue a few remarks are stated on the properties of wet etching.

As already stated, wet etching results in an anisotropic profile; this is so because of different etch rates for different crystallographic planes in c-Si. Precisely, when TMAH is used, the etching rate of (100) planes, quantitatively 0.3-1µm/min, happens to be almost 40 times higher than the etching rate of (111) planes. The etching rates of the (110) planes presents an etching

rate of approximately 0.6-1.8µm/min, higher than the (100) case [47]. This means that the lateral etching rate is generally higher than etching rate on the normal direction to the surface. This also means that in the presence of over-etched substrates, where a few nanometres of silicon were already removed by dry etching, performing wet etching with TMAH for 60s may result in a lateral over-etching with respect to the normal direction, causing the lost of the pattern. This was the case for several samples: in many of them, by visual inspection, it was seen that in a time-lapse below 60s the pattern was completely lost.

In addition to what has been said before, because of the electric field involved in plasma etching, such technique is extremely sensible to the shape and the width of the utilized substrates. As a matter of fact, for bigger substrates, higher etching time was needed, making it extremely difficult to define a unique reproducible recipe.

Ultimately, a more selective recipe utilizing 100sccm of CHF_3 gas at 200mTorr, at 100W for 220s was used for dry etching silicon oxide. All the results are presented in the following section.

Results and discussion

In Fig.4.47 the best topography, using the mixture of SF_6 and O_2 for plasma etching, achieved by wet etching is shown. Subsequently, in Fig.4.48, a reflectance plot of the same, compared to the one obtained from dry etching is presented. As it can be seen, by performing wet etching, worsening of the optical properties occurred, resulting in a higher total reflectance. This is explainable by considering the flat silicon regions that are shown in FIG WE4 and that do not contribute to the anti-reflective effect. In order to improve the performances, a merging of the borders of the inverted pyramids

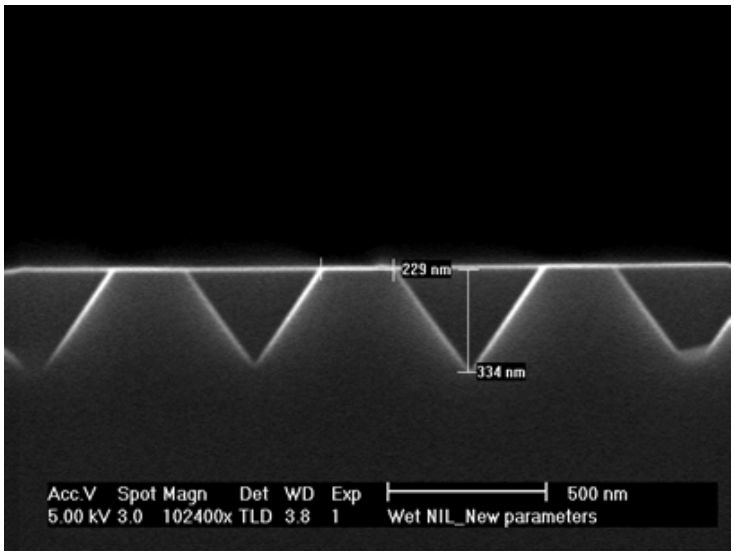


Figure 4.47: Wet etching best topography

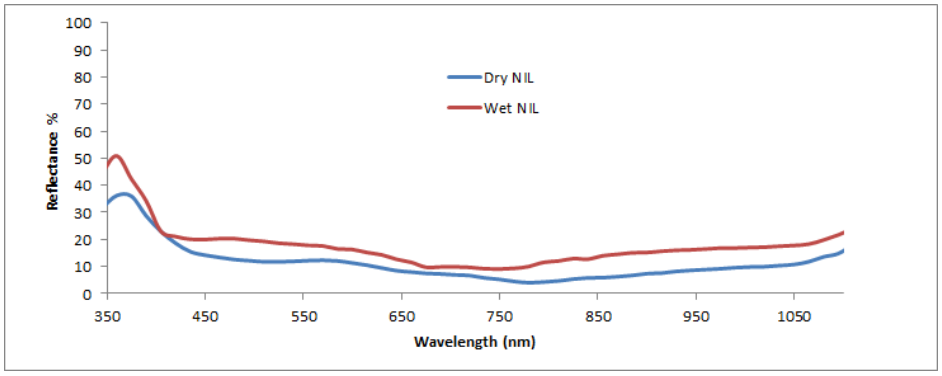


Figure 4.48: Reflectance plot: wet-etch vs dry-etch

is needed. This is achievable by increasing the etching time, but with the used recipe and because of the issues depicted in the previous section, this would result in the lost of the pattern.

Hereafter Fig.4.49, the topography images of a substrate which oxide was etched with CHF_3 gas is shown. Such gas provides a more selective etching and was expected to dismiss the above problems. It is noticeable here that

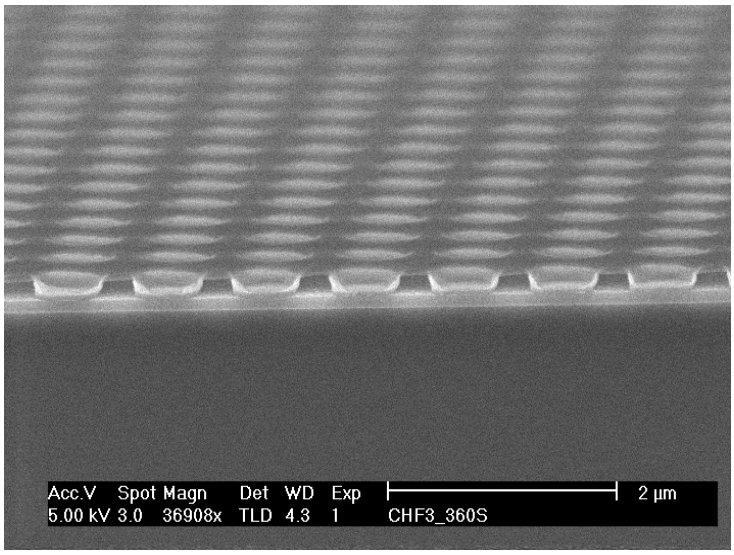


Figure 4.49: Resist film re-deposition

the oxide was completely untouched because of o thin film re-deposition of the resist, caused by the reaction between the polymer resist and the etching gas. The re-deposition of the resist is a phenomenon that takes place in the standard dry etch process; it usually re-deposit and passivate the side-walls after the etching of silicon. In this case, this step happened before any etching of the oxide. In order to force the etching, the ion bombardment was enhanced by increasing the power, from 100W to 300W, and lowering the pressure, from 200mTorr to 70mTorr (the minimum value of pressure reachable inside the chamber when the mentioned gases are present). The results are presented in Fig.4.50. In this case, the oxide was successfully etched and the window to silicon was opened. From several attempts, each with different etching time, it was also noticed that the quantity of silicon etched was approximately the same always. Nevertheless, the resist redeposited on the surface after the oxide etching. The substance redeposited was actually the result of the reaction between the gas and the resist and it had different

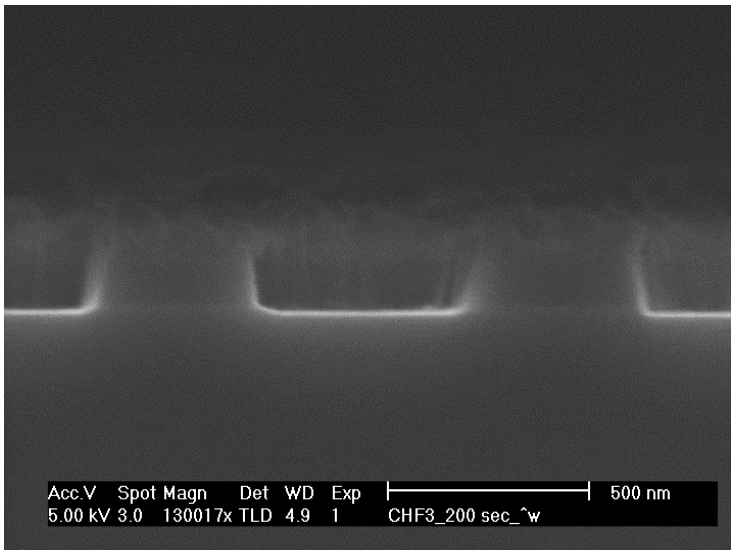


Figure 4.50: Resist re-deposition

properties from the initial resist. As a matter of fact, it was not possible to remove it with acetone and IPA and neither with TMAH. It was not possible then to successfully perform wet etching.

After analyzing the passivation study, wet etching was considered to be the most promising process to take over the pattern transfer step from plasma etching. Nevertheless, several issues related to opening the oxide mask bring to the need of a process optimization. It was stated that a unique and reproducible recipe to etch the oxide was not found during the study made. However, it was seen that one recipe acted well on the resist-oxide interface and the other on the oxide-silicon interface; This suggest that an use of a combined recipe where SF_6 is used to remove half of the oxide and CHF_3 to etch the remaining part, may be helpful for the purpose.

Chapter 5

Conclusions and outlooks

In this report, two different lithographic technologies for texturing thin film single-crystalline silicon solar cells were presented. Their low material consumption, around 500nm in depth, allow them to be successfully integrated in thin film technologies. Moreover, optical characterizations of nano-patterned samples showed remarkable absorption enhancement with respect to flat silicon case and similar values compared to substrates textured with conventional micron size features. In addition, they presented higher angular robustness confronted to pyramid texturing. The absorption enhancement was explained by considering the combined effect of impedance matching on the surface, due to the graded refractive index profile, and diffraction inside the material; as a matter of fact, by shifting to sub-wavelength scale features, the geometric optics approach is no more valid and the wave-like nature of light becomes dominant. Consequently, the optical path length limit, known as Lamertian limit, which was calculated considering only geometric optics notions, is no more applicable and the possibility to overcome such limit arises.

Hole-mask colloidal lithography is a technique that makes use of a ran-

dom dispersion of colloidal particles, in order to define the 2-D pattern, and undergoes a hard mask deposition step and a dry etching step, to define the in-depth profile. The balance between all the forces acting on the colloidal particles results in a short range order of the holes, where the center-to-center distances of the cavities present the same magnitude of the diameters of the same. The result of the experiments was an inverted nano-pyramids structure. Despite the considerable absorption enhancement provided by the technique, several reproducibility issues related to the substantial amount of manual works were faced. In order to efficiently integrate this technique in a cell level, further studies, especially to fully control the dispersion of colloidal particles on crystalline silicon surface, have to be carried.

Nano-imprint lithography is a technique than enables sub-micron scale texturing through a pattern transfer from a pre-fabricated stamp to the silicon surface. This is done by means of a polymer resist, a mechanical press and an etching step to define the in-depth profile; in the standard procedure, RIE was utilized. The nano-patterned surfaces exhibited very high level of absorption. It was shown that further improvement could have been reached when optimal parameters, derived from theoretical works, were used. The procedure though, principally the resist coating step and the etching recipe, has to be re-adapted to the new features. The technique was shown to be efficiently integrable in thin film solar cells, resulting in improved optical performances with respect to flat silicon case. However, values for open circuit voltage were drastically low, compromising the efficiency of the cells. This was explained by considering the dry etching step critically damaging for the surface causing the formation of several recombination sites. A passivation study was then made and two methods to overcome the recombination issues were proposed. A method where a few nanometres of material was removed,

removing also the defects, was first considered and, secondly, the complete replacement of the dry etching step by a wet etching process was tried. This last resulted in a very promising procedure since carrier lifetimes much higher than the dry etching case were obtained, suggesting new cell fabrication runs where such etching process is incorporated. Nevertheless the wet etching featured reproducibility problems. In order to efficiently replace RIE from NIL, further studies on the the process are needed. Combining wet-etching and nano-patterning may result in very high efficiency thin film solar cells.

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