POLITECNICO DI MILANO

Scuola di Ingegneria dell'Informazione

POLO TERRITORIALE DI COMO

Master of Science in Computer Engineering

DSP board analysis and software implementations for professional audio applications

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Academic Year 2012 – 2013

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Laurea Specialistica in Ingegneria Informatica

Analisi scheda DSP e implementazioni software per applicazioni nel campo dell'audio professionale

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Anno Accademico 2012 - 2013

Abstract

Architettura Sonora (AS) power amplifiers, with preamplifier boards equipped with DSP on-board, are affected by a limited input dynamic of the whole AS system. This limitation forbids that CD players or Mixers with output voltages up to 5 Vrms, can drive an AS amplifier with DSP, without preamplifier harmonic distortions due to the clipping of the active electronics within the card.
Aim of this work is the exploiting of the DSP on-board of preamplifier cards, in order to implement software solutions, combined with hardware developments, able to optimize the input stage of AS systems.
In particular, input stage optimization has been implemented by means of a software/hardware solution able to dynamically recognize the family of the most well-known devices, like Portable, CD player and Mixers, which the device plugged into the system belongs to. Dynamic recognition allows preamplifier to apply a suitable gain that is able to give a boosting for portables and two different attenuations, one for CD players and one for Mixers. In this way each device, plugged into an AS amplifier, receives a suitable gain correction that produces an attenuation if device is in clipping danger or boosting if input belongs to a portable, with the objective of achieving a normalized maximum output voltage level for all input devices. Recognizer works as a states machine where to each state corresponds a correction gain for the preamplifier board. A reset condition based on input voltage level (0V input) brings the machine back to its initial state.
Implemented input stage development, reaches the aim, for which, any device can interface an AS amplifier, avoiding clipping and giving a boosted gain for portables. Furthermore dynamic recognition of devices family which input device belongs to, make allowable a normalized output voltage level for all devices plugged into the system. Nevertheless latencies during gain commutation states of recognizer occur and they are not bounded within the first listening, that can be defined as *calibration listening*. This restriction can be overcome with a future development that switches the recognizer reset condition caller toward a channel open circuit detection instead a channel voltage level listener.

Sommario

Gli amplificatori di potenza prodotti da Architettura Sonora (AS), equipaggiati con schede di preamplificazione provviste di DSP, presentano una limitata dinamica di ingresso dell'intero sistema. Tale limitazione impedisce a dispositivi, come CD player o Mixer con uscite fino a 5 Vrms, di poter pilotare un amplificatore AS con DSP, senza che la scheda di preamplificazione introduca distorsioni armoniche dovute al clipping dei componenti attivi al suo interno.
Obbiettivo di questo lavoro, è stato quello di sfruttare il DSP a bordo, per implementare soluzioni software, accompagnate da migliorie hardware, capaci di ottimizzare lo stage di ingresso del sistema.
In particolare, l'ottimizzazione dello stage di ingresso è stata implementata mediante una soluzione software/hardware capace di riconoscere dinamicamente la famiglia di dispositivi più diffusi, quali Portable device, CD player e Mixer, alla quale il dispositivo in input al sistema appartiene. Il riconoscimento dinamico consente al preamplificatore di applicare un opportuna correzione guadagno, capace di fornire un boosting per i dispositivi portatili e due diverse attenuazioni per i lettori CD e i Mixer. In questa maniera ogni dispositivo riceve un'adeguata amplificazione, attenuando i device a rischio clipping e amplificando i dispositivi portatili, con il fine di garantire un livello massimo di uscita del preamplificatore normalizzato ad uno stesso valore di tensione.
Il riconoscitore funziona come una macchina a stati, in cui ad ogni stato corrisponde una correzione di guadagno per la scheda di preamplificazione. Una condizione di reset basata sul livello di ingresso di canale (0V in input) riporta il riconoscitore allo stato iniziale.
L'ottimizzazione implementata, ha raggiunto l'obbiettivo di poter interfacciare un amplificatore AS, con DSP, con tutti i dispositivi audio più diffusi, evitando distorsioni armoniche da clipping e fornendo un'amplificazione ulteriore per i dispositivi portatili. Inoltre, il riconoscimento dinamico della famiglia di afferenza del dispositivo in ingresso, permette di avere un sistema AS in grado di fornire uno stesso valore massimo di uscita del preamplificatore per tutti i dispositivi in ingresso ad esso.
Tuttavia restano delle latenze nella commutazione dello stato di guadagno correttivo del riconoscitore, che purtroppo non sono circoscritte al primo ascolto, definibile come *ascolto di calibrazione*. Tale restrizione però, risulta superabile mediante uno sviluppo futuro basato su un sistema di riconoscimento provvisto di un rilevatore di reset strettamente legato ad una lettura dell'impedenza di ingresso del canale e non sulla misurazione del suo livello di tensione, ossia riconoscendo direttamente se un device è interfacciato all'amplificatore o l'ingresso è in stato di circuito aperto.

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Introduction

Architettura Sonora (AS) manufacturing overview

Architettura Sonora (AS) is a branch of the eminent B&C Speakers, worldwide leader loudspeakers manufacturer. AS aim is developing and production of composite sound modules which have design and architecture as main requirements. These sound architectures are associated with proper amplifiers manufactured by AS as well. Design requirements of the sound modules often require that complex and tiny products don't have enough space to encapsulate bulky analog cross-over networks. But cross-over networks are essential to feed all drivers, included into the sound module, with the adequate frequency band of the input signal. To overcome space requirements limitations, many AS amplifiers exploit DSPs directly integrated into the power amplifier, in order to implement digital cross-over in a programming way, avoiding the usage of bulky analog ones plugged into sound modules.

Description of the work

This work starts from the study of the AS amplifiers structure and their component in particular the preamplifier board and DSP card. Processor exploited by many AS amplifiers is an Analog Device (AD) product. It's a fixed-point chip referred as ADAU1701 which is interfaceable by an AD programming block language known as Sigma Studio. Chip architecture, its operating principles and Sigma Studio program language have been deepened in order to realize software solutions to improve some limitations of AS amplifiers.
In particular, low input dynamic of DSP-equipped AS amplifiers and different gain amplification of preamplifier for different devices, are the main aspects taken into account for their development implementations.

Exploiting DSP programming and hardware improvements, it has implemented a software able to recognize the input device and give it the proper preamplifier gain, attenuating it if the device is in clipping risk or a boosting if it belongs to low output signal device family like MP3. For this purpose three families of devices have been located, classified by the output voltage maximum values. In detail, these families are:

1. Portable devices, like MP3 players, iPod or smart-phones whit maximum output voltages of 0.5 V (or 0.36 Vrms)
2. CD players with maximum output voltages of 2.0 V (or 1.44 Vrms)
3. Mixers devices having maximum output voltages up to 5.00 Vrms

When a device is plugged into the AS amplifier, the program recognizes the family which it belongs to and correct the preamplifier gain, giving attenuations for CD or

Mixer devices to avoid clipping and boosting for portables in order to produce a normalized gain amplification for every devices in input.

Thesis structure

The structure of this work is composed of 2 parts.
The first one describes the AS amplifiers. In detail, chapter 1 describes the structure of AS amplifiers with an introduction about power amplifiers, details about the preamplifier stage of AS amplifiers and final amplification stage that exploits Bang&Olufsen switching amplifiers technology. Chapter 2 shows details about structure and operating principles of DSp on-board of AS amplifiers while chapter 3 depicts the structure of the AS DSP boars, which are cards equipped by 4 ADAU1701 for each one, that interfaces preamplifier board. In chapter 3 is shown a brief description of interfacing hardware between ADAU1701 and PCs. Furthermore an overview about Sigma Studio environment closes the chapter.

The final part shows the optimizations developed on AS amplifiers. Chapter 4 depicts the input stage optimization of the preamplifier board, highlighting the implementations, tests and performances evaluations of the development.

Conclusions and future developments section closes the work.

Part I

AS (Architettura Sonora) amplifiers

Chapter 1

AS (Architettura Sonora) power amplifiers

In this chapter *Architettura Sonora* (AS) power amplifiers will be described. AS is a branch of the eminent *B&C Speakers* company, worldwide leader of loudspeakers design and production for audio devices.
It will come first a brief recall about large signal amplifier operation and parameters for performances evaluation.

1.1 Introduction to power amplifiers

A power amplifier can be defined as a *controlled converter*, characterized by a circuital configuration able to convert the power supply into load power as a function of a control signal [1]. A power amplifier operation principle is shown in fig. 1.1. Usually in audio industry the load is represented by a loudspeaker, which avails the power delivered from the amplifier circuit.

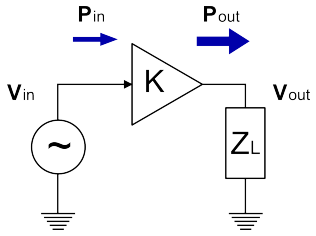


Figure 1.1: Amplifier scheme working principle

Signals of high value are generated exploiting circuital configurations employing active devices either unipolar (MOSFET) or bipolar (BJT).
In order to quantify the amplifier delivered power, let us take the example shown in fig. 1.2, where a BJT transistor amplifier delivers power to a totally resistive load R_{L}. The current i_{C} constitutes the total instant collector current and i_{c} specifies the instant variation collector current from the rest value I_{C}. In the same way, i_{B}, i_{b} and I_{B} represent base currents. The collector-emitter instant voltage is v_{C} and v_{c} is the instant variation voltage from rest collector voltage V_{C}.

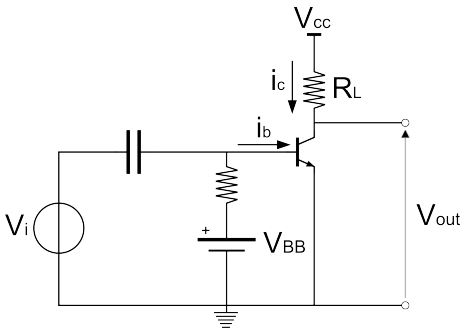


Figure 1.2: BJT amplifier circuit

Let us assume that output characteristics are evenly spaced when input base current i_b increases of equal amounts, as shown in fig. 1.3. If i_b is a sinusoid, output current and voltage will be sinusoidal too. Ignoring nonlinear distortion, output power can be computed as follows:

$$P = V_\mathrm{c} I_\mathrm{c} = {I_\mathrm{c}}^2 R_\mathrm{L} = \frac{{V_\mathrm{c}}^2}{R_\mathrm{L}} \tag{1.1}$$

where V_c and I_c are root mean square values of output voltage v_c and current i_c.

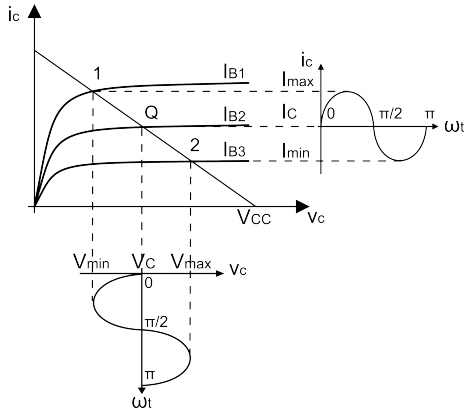


Figure 1.3: Wave forms of current and voltage output characteristics, referred to circuit in fig.1.2, for a sinusoidal input i_b

1.2 Power amplifier performances evaluation

A power amplifier is characterized by the amount of power it is able to deliver to the load. In audio amplification systems, power must be evaluated in relationship to the fidelity of played sound [2]. This operation accuracy is evaluable taking into account *noise* and *distortion*. A verdict on a power amplifier must be stated also taking into account other two parameters, related to energetic performances: *efficiency* and *power dissipation*.

1.2.1 Noise

Usually a power amplifier is formed by a cascade of amplifying stages. Each stage must introduce a noise amount as low as possible, otherwise the noise generated at each stage will be amplified by next ones, getting the signal-to-noise ratio (SNR) worse. Since the complete noise removal is complicated, the design aim is to limit electronic noise below human audibility threshold.

1.2.2 Distortion

An accurate amplification operation means that the amplifier must just increase the power of a signal avoiding any content degradations. How an amplifier output signal content is similar to what has been fed in input, is depicted by the idea of distortion. Three kind of distortions have been evaluated: linear, harmonic and intermodulation distortion.

Linear distortion

Each electronic circuit or amplifier module is characterized by a frequency response which is band limited. In fig. 1.4 is shown a frequency interval, called as *full power band*, included between two cut frequencies: ω_{L} and ω_{H}.
To avoid linear distortion, two conditions must occur, one for module and one for phase:

$$|A(\omega)| = A_0 \tag{1.2}$$

$$\phi(\omega) = k\omega \tag{1.3}$$

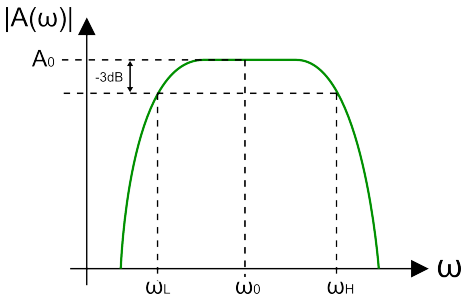
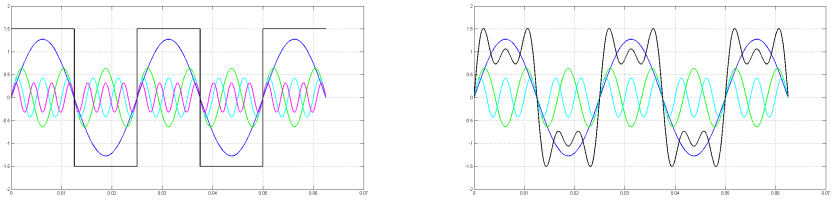


Figure 1.4: Generic amplifier frequency response

Referring to fig. 1.4, condition 1.2 won't be verified, if input signal harmonics have frequencies which stay outside the full power band. In this case, outsider harmonics will be amplified with a gain value lower than A_0 or even amplified at all.
Fig. 1.5 shows a linear distortion of an input square wave signal [1]. If the full power band doesn't contain all the input signal harmonics, output signal results distorted.
Even if condition 1.2 occurs but 1.3 doesn't, linear distortion will affect output signals. Fig. 1.6 shows a case of linear distortion due to non occurring of both linear conditions. The VII harmonic isn't amplified and the III one is out-of-phase in respect of I and V.

[1] A square wave has a development in an infinite summation of odd harmonics multiple of fundamental



(a) (b)

Figure 1.5: Input square wave signal as I, III, V and VII harmonics summation (a), distorted output due to non amplification of VII harmonic (b)

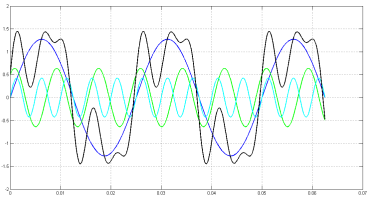


Figure 1.6: Module and phase linear distortion

In audio amplifier to avoid linear distortion, the system frequency response must be as wide as the audible band (20Hz to 22kHz), with a flat behavior of the module and a linear phase within this band.

Harmonic distortion

In fig. 1.3, BJT behavior has been idealized as linear. Furthermore the dynamic characteristic (i_c as function of i_b) isn't a straight line, because output characteristics i_C aren't equidistant for equal boosts of input current I_B. For this reason a sinusoidal input can be damaged during the amplifying process, giving an output signal not more sinusoidal, like has been shown in fig. 1.7. In this situation, wave form of the output signal has been clipped due to the input signal exceeding saturation and cut-off limits. These kind of distortions are referred as nonlinear.
For nonlinear distortion bulk evaluating, the dynamic characteristic is developed as a power series rather than as a straight line. As opposed to put input i_b and output i_c in linear relationship $i_c = Ci_b$, is more effective the following:

$$i_c = C_1 i_b + C_2 {i_b}^2 + C_3 {i_b}^3 + C_4 {i_b}^4 + \dots \tag{1.4}$$

where C_i values are coefficients of each dynamic characteristic. Considering a sinusoidal input signal:

$$i_b = I_{bm} cos(\omega t) \tag{1.5}$$

after suitable trigonometric transformations, relation 1.4 becomes:

$$i_C = I_C + i_c = I_C + B_0 + B_1 cos(\omega t) + B_2 cos(2\omega t) + B_3 cos(3\omega t) + B_4 cos(4\omega t) + \dots \tag{1.6}$$

where B_i are constant values related to C_i.
The last equation highlights that a sinusoidal input application to a non ideal amplifier

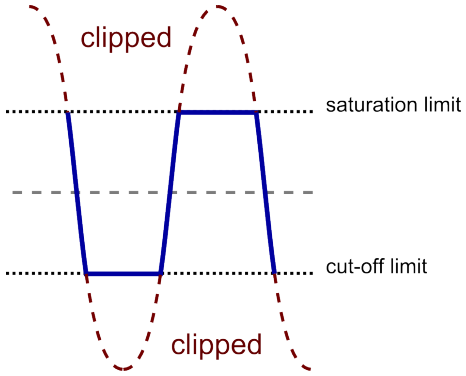


Figure 1.7: Output signal clipping, due to the input excursion beyond saturation and cut-off limits

gives an output current having harmonics with frequency multiple of fundamental ω and a constant current B_0, which increases the rest current value I_C.
Harmonic distortion is defined as:

$$D_2 \equiv \frac{|B_2|}{|B_1|} \qquad D_3 \equiv \frac{|B_3|}{|B_1|} \qquad D_4 \equiv \frac{|B_4|}{|B_1|} \qquad \dots \qquad D_n \equiv \frac{|B_n|}{|B_1|} \tag{1.7}$$

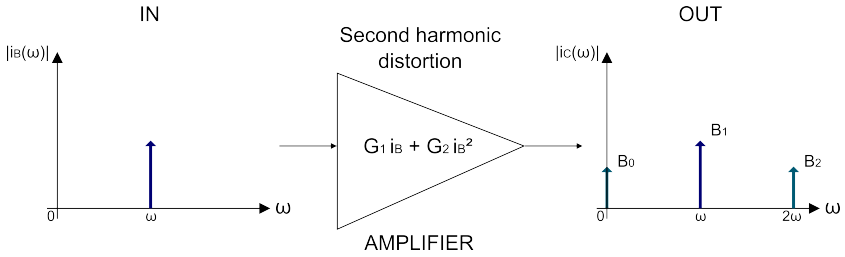


Figure 1.8: II harmonic distortion effect in frequency domain

Example of fig. 1.8 shows a second harmonic distortion. Putting in input a sinusoidal signal with frequency ω, a signal with three frequency components, B_0, B_1 and B_2, will result as output. Is suitable that B_0 leads the other two harmonics, in this way the frequency content of output signal will get close to the input one.
In audio field computing the whole nonlinear distortion contribution, in respect of fundamental frequency, is considerable important. The *Total harmonic distortion* (THD) is defined as:

$$THD \equiv \sqrt{\sum_{i=2}^{n} {D_i}^2} \tag{1.8}$$

where D_i are nonlinear contribution for each harmonic.
If nonlinear distortion isn't negligible, output delivered power for fundamental frequency is:

$$P_1 = \frac{{B_1}^2 R_L}{2} \tag{1.9}$$

while total output power is:

$$P = ({B_1}^2 + {B_2}^2 + {B_3}^2 + \dots)\frac{R_\mathrm{L}}{2} = (1 + {D_2}^2 + {D_3}^2 + \dots)P_1 \tag{1.10}$$

thus:

$$P = (1 + THD^2)P_1 \tag{1.11}$$

In design process THD percentage amount must be taken in check. Desirable aim should be: let keep THD as low as possible. Furthermore in human audio perception the same amount of THD results more annoying as harmonics order of distortion increases. So low THD percentage of high order harmonics is to avoid as well.

Intermodulation distortion

Consider an input signal to amplify:

$$i_\mathrm{b} = I_{\mathrm{b}1}cos(\omega_1 t) + I_{\mathrm{b}2}cos(\omega_2 t) \tag{1.12}$$

and taking into account the same second harmonic distortion of previous section, the output signal is:

$$\begin{aligned} i_\mathrm{C} = I_\mathrm{C} + B_0 + B_{11}cos(\omega_1 t) + B_{12}cos(\omega_2 t) + B_{21}cos(2\omega_1 t) + \\ + C_1 cos[(\omega_1 + \omega_2)t] + C_2 cos[(\omega_1 - \omega_2)t] \end{aligned} \tag{1.13}$$

The frequencies sum $\omega_1 + \omega_2$ and difference $\omega_2 - \omega_1$, are referred as *intermodulation frequencies*.

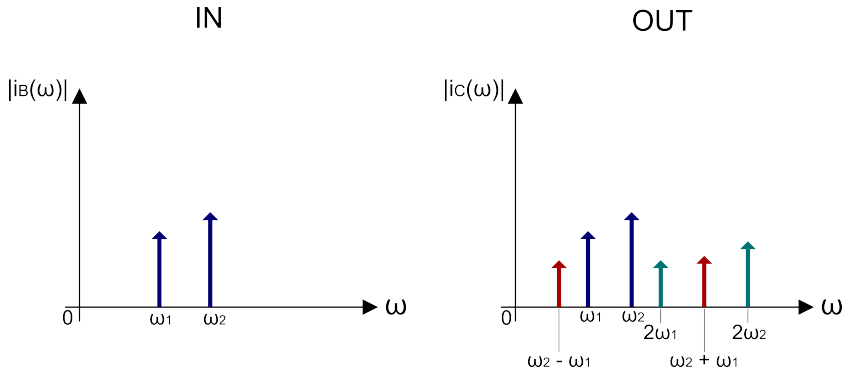


Figure 1.9: Intermodulation distortion effects in frequency domain

In fig. 1.9 is reported an intermodulation distortion example. Putting an audio signal with frequencies ω_1 and ω_2 as input, the resulting output spectrum has: desired components (blue), nonlinear distortion harmonics (cyan) and intermodulation distortion frequencies (red).

1.2.3 Efficiency

Amplifier efficiency can be stated through a parameter known as *conversion efficiency* η. This parameter is a measure of an amplifier capability to convert the DC power supply into AC power delivered to the load. Percentage conversion efficiency is:

$$\eta \equiv \frac{Power\ output}{Power\ supply}100\% \tag{1.14}$$

Generally:

$$\eta = \frac{\frac{1}{2}{B_1}^2 R_{\mathrm{L}}}{V_{\mathrm{CC}}(I_{\mathrm{L}} + B_0)} 100\% \tag{1.15}$$

If components due to harmonic distortion are negligible:

$$\eta = \frac{\frac{1}{2}V_{\mathrm{m}} I_{\mathrm{m}}}{V_{\mathrm{CC}} I_{\mathrm{L}}} 100\% = 50 \frac{V_{\mathrm{m}} I_{\mathrm{m}}}{V_{\mathrm{CC}} I_{\mathrm{L}}}\% \tag{1.16}$$

where V_{m} and I_{m} are peak values of sinusoidal input voltage and current.
The upper limit of η is reached when all power supply is converted in power output. So high η percentages mean high amplifier efficiency.

1.2.4 Power dissipation

Amplifier power dissipation is evaluable by means of the *figure of merit* F. Figure of merit is defined as the ratio between the maximum dissipated power by each active electronic devices $P_{\mathrm{D(MAX)}}$ and the maximum useful power delivered to load $P_{\mathrm{L(MAX)}}$:

$$F = \frac{P_{\mathrm{D(MAX)}}}{P_{\mathrm{L(MAX)}}} \tag{1.17}$$

The lower limit of F is zero, which implies the ideal condition where there is no power dissipation. About power dissipation, in real situations, a suitable amplifier has low values of F.
Figure of merit allows to size amplifier dimensions, because the dissipators sizes and needed cooling fans number, depend on the amount of dissipated power.

1.3 Amplifiers classification

A first distinction among amplifiers operation classes is related to how the amplifier produce the power amplification [3]. In this sense we can distinguish two kind of operations: *analogical* and *switching*.
In this section will be proposed an analysis of the most important operation classes of amplifiers, taking into account distortions, efficiency and power dissipation.

1.3.1 Analogical operation amplifiers

To understand the behavior of amplifiers which use transistors in analogical operation, is preferred to think to the fluctuation of the work point Q onto the load characteristic line, between the saturation and cut-off regions, rather than an analysis based on circuit equivalent models. For this reason has been proposed an amplifiers classification established on the kind of circuits *polarization* and the *conduction angle*[2] of the output current.

Class A

In fig. 1.10 is shown the schema of a class A amplifier circuit, made by a bipolar transistor.
The work point Q of a class A amplifier is forced in the middle of linear operation region (fig. 1.12).

[2] time, expressed as degrees, for which active electronic components are conducting current

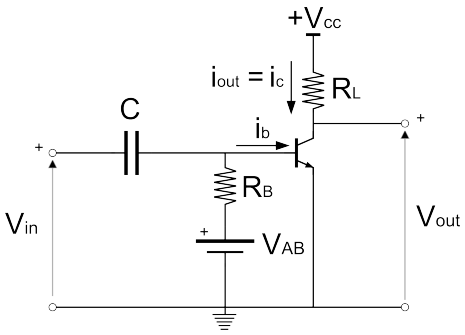


Figure 1.10: Direct-coupled A class amplifier scheme

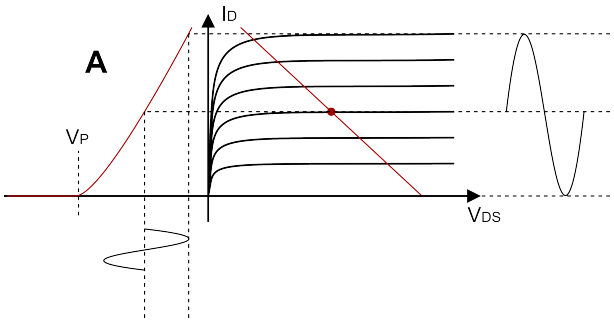


Figure 1.11: Operation principle of an A class amplifier

If a sinusoidal signal is fed in input to the circuit of fig. 1.10 and polarized as fig. 1.11, output current flows into R_{L} for all the period duration of the input signal. The conduction angle Φ is 2π. This situation is shown in fig. 1.12.

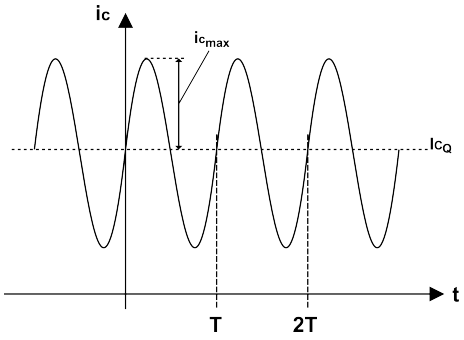


Figure 1.12: Conduction angle of 360°

Class A amplifiers work in the middle of the characteristic linear region and for this reason they have the capability to amplify large input signals avoiding clipping. So class A has high audio fidelity. Furthermore the transistors conduct current also when no input signal is fed to the system. This is a limit from an energetic point of view. Indeed the maximum theoretical conversion efficiency η is 25%. The figure of merit F is equal to 2.
The issue of power dissipation during rest condition has been fixed decoupling the

load by means of a transformer as shown in fig. 1.13.

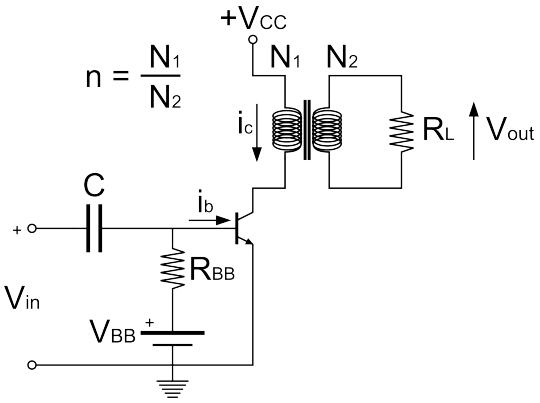


Figure 1.13: Uncoupled A class amplifier scheme

Through decoupling, theoretical conversion efficiency improves to 50%, but the figure of merit remains 2, thus high.
Looking at real values of conversion efficiency and figure of merit, the whole system energetic efficiency decreases further. First of all, a real amplifier cannot deliver the whole power supply to the load, so effective η decreases; second, in real situations, an amplifier gets in input signals as music or speech and not pure sinusoids, so power delivered to load is about 10% of the maximum load deliverable power.
Class A employs high amount of dissipated power thus amplifiers need a suitable cooling system with dissipators and fans, involving bulky implementations.
In summary, class A amplifiers are easy to implement, have high fidelity behavior but low energetic performances. For these reasons they are employed in the production of pre-amps which require low power to deliver and high audio fidelity.

Class B

Fig. 1.14 shows an example of class B amplifier circuit made with a BJT.

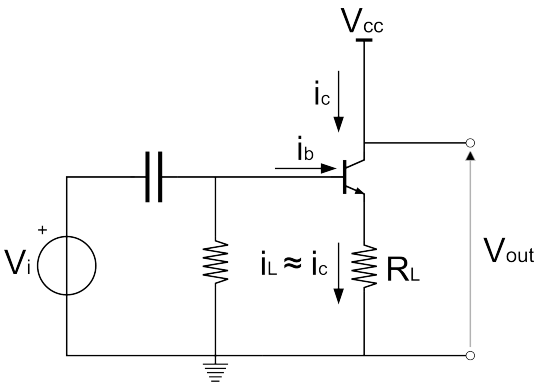


Figure 1.14: Emitter follower circuit scheme

Fig. 1.15 depicts the polarization of class B amplifier. The work point is placed at the lowest limit of the characteristics, so that absorbed power, in the rest condition,

is very low. In this way, positive part of signal is linearly amplified while the negative one is cut away.

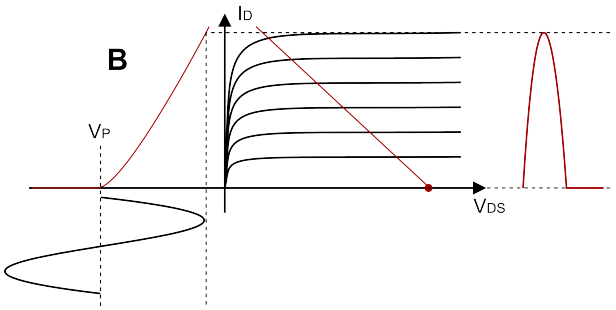


Figure 1.15: Operation principle of a A class amplifier

In this configuration rest conditions output currents and voltages are null. If input signal is sinusoidal, $i_{\mathrm{L}} \cong i_{\mathrm{C}}$ is sinusoidal for a half of period and zero for the other half. Efficiency increases and conduction angle, shown in fig. 1.16, is $\Phi = \pi$. In other words, circuit in fig. 1.14 operates as a rectifier. In order to make a follower emitter an amplifier circuit, has been proposed the the solution in fig. 1.17.

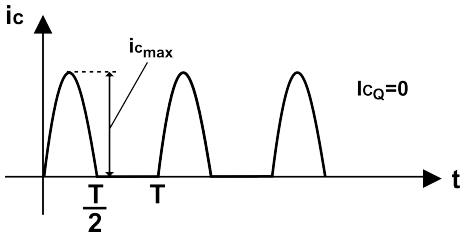


Figure 1.16: Conduction angle of 180°

This configuration is called *push-pull*. For positive values of input v_{i}, Q_2 conducts, while Q_1 is off ($i_2 = 0$), so that i_2 is the positive half wave of fig. 1.15. For negative values of v_{i}, Q_2 is off, while Q_1 conducts, generating the negative half wave carried by i_1. The output current i_{L} is the difference of i_1 and i_2. As a result, theoretically, we'll have a perfect sinusoidal current i_{L}.

Furthermore work point Q lies on the limit of cut-off and if BJTs polarization is altered during the commutation of half waves, can happen that none transistor conducts current. In this way, output wave will result as not continuous as the input one. Phenomenon shows in fig. 1.18, is referred as cross-over distortion. It can heavily affect the quality of played sound, because it introduces odd harmonics.
Nevertheless, if cross-over distortion is limited, B class amplifier has several advantages in respect of class A: higher conversion efficiency (about 70%), higher output power and negligible dissipation power in rest condition.
The main disadvantage of B class is the cross-over distortion. If active devices are identical, currents i_1 and i_2 are equal and out of phase of 180.
Current flowing into Q_1 is:

$$i_1 = I_{\mathrm{C}} + B_0 + B_1 cos(\omega t) + B_2 cos(2\omega t) + B_3 cos(3\omega t) + \dots \tag{1.18}$$

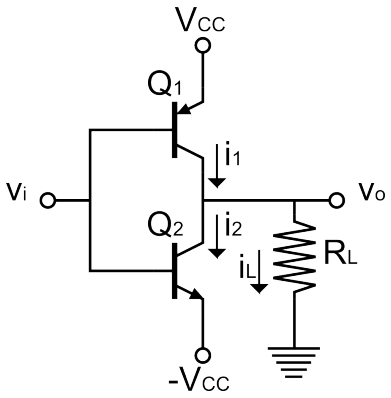


Figure 1.17: Push-pull configuration

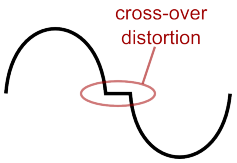


Figure 1.18: Cross-over distortion

While the output current of Q_2 is obtained substituting $\omega t + \pi$ to ωt in the previous relationship:

$$i_2 = I_C + B_0 + B_1 cos(\omega t + \pi) + B_2 cos2(\omega t + \pi) + B_3 cos3(\omega t + \pi) + \dots \quad (1.19)$$

Thus:

$$i_2 = I_C + B_0 - B_1 cos(\omega t) + B_2 cos(2\omega t) - B_3 cos(3\omega t) + \dots \quad (1.20)$$

Total current flowing into the load is:

$$i_L = i_1 - i_2 = 2[B_1 cos(\omega t) + B_3 cos(3\omega t)] \quad (1.21)$$

The last equation shows that in a push-pull configuration, all the output even harmonics are neglected and the distortion effect is related just to the odd harmonics of the signal. If active devices are not identical the even harmonics are no more negligible, so they will increase the cross-over distortion effect.

Class AB

To minimize the cross-over distortion, amplifiers must operate in AB class, with a small output current in the rest condition. The prize payed for this solution is a decrease of conversion efficiency and an increase of wasted power at rest.
The polarization scheme of AB class amplifier is shown in fig. 1.19, in which the conduction during the negative half wave, lasts a small time.
AB class amplifier has an hybrid operation between A and B class amplifiers. Fig. 1.20, depicts the conduction angle $\pi < \Phi < 2\pi$, which says that output signal is null for a time duration lower than the input signal half-period.

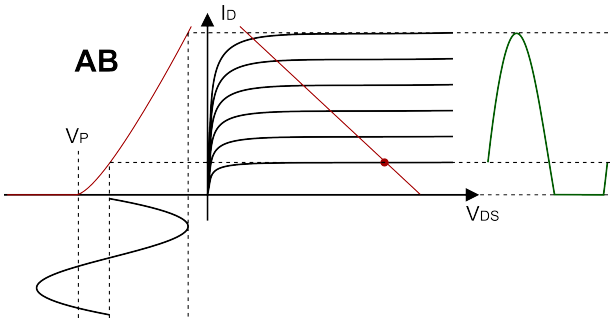


Figure 1.19: Operation principle of a AB class amplifier

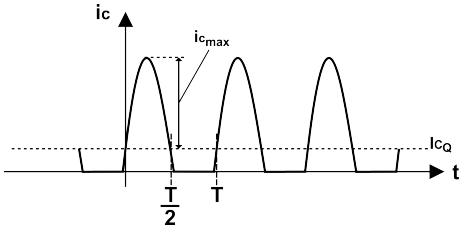


Figure 1.20: AB class conduction angle

Class C

As highlighted by the polarization scheme in fig. 1.21, the work point Q is placed below the cut-off voltage, in order to null the output current for more than a half-period of input signal. This yields a conduction angle $\Phi < \pi$, shown in fig. 1.22.

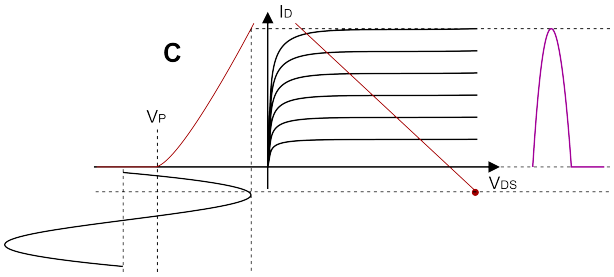


Figure 1.21: Operation principle of a C class amplifier

An input signal can be hugely amplified even if the output wave form signal doesn't fit the input one. Indeed the output signal is hugely distorted and absolutely useless for audio application.
Class C amplifiers have conversion efficiency of 90% and are employed in radio communications to amplify signals that will be sent by antennas.

1.3.2 Switching operation amplifiers

Efficiency of class A, B and AB amplifiers is less than 80%. In order to improve it, have been developed several kinds of switching amplifiers.
These amplifiers haven't a linear relationship between input and output, transistors

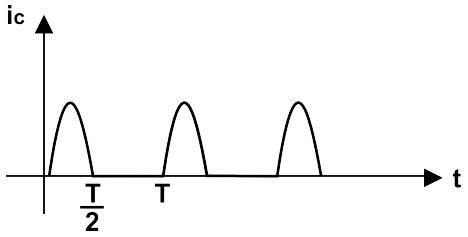


Figure 1.22: C class conduction angle

(usually MOSFET) operate as binary switches (indeed, the name of the amplifier family derives from this operation principle) and input signals are coded, exploiting a *pulse width modulation* (PWM), in impulses train control signals able to pilot amplification procedure through their duty cycle.
D class belongs to this amplifiers family.

Class D

Fig. 1.23 shows a typical D class amplifier configuration. Amplification operation is partitioned in three stages: a modulation stage of input signal, amplification phase and a demodulation process.

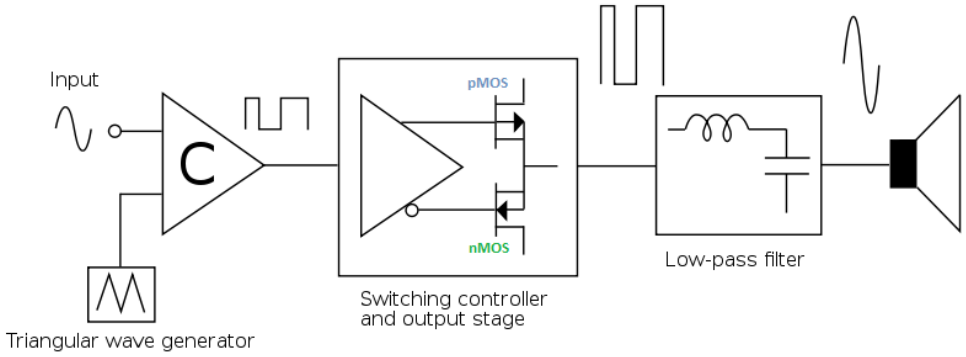


Figure 1.23: D class amplifier

During the modulation phase, the input signal (modulating signal) is compared with a triangular signal (carrying signal) by means of a comparator (in fig.1.23 called C). From this comparison is generated a control signal used to drive transistors in the next stage. The control signal is generated exploiting a pulse width modulation procedure. The effect of PWM is shown in fig. 1.24. The modulation produces a square wave signal having variable duty cycle as a function of the comparison between the input signal and the triangular wave. If input is higher than carrying, the modulated signal is high, conversely, if input is lower than carrying thus control signal is low.
In the amplification phase, the control signal pilots the MOSFETs, employed in a push-pull circuit, operating in forward-active region, one at a time (because when the control signal is high only one transistor conducts while the other one is off, and conversely when control signal is low). Referring to fig.1.23, when control signal is high the n-type MOSFET conducts and p-type is off, conversely, when the control is high, p MOSFET conducts and n-type is off.

Signal outgoing from the previous stage, is an altered amplified version of the input. It's necessary to demodulate this signal to achieve the input signal amplification. The demodulation phase is performed by means of a high-cut filter and produces the amplified output signal.

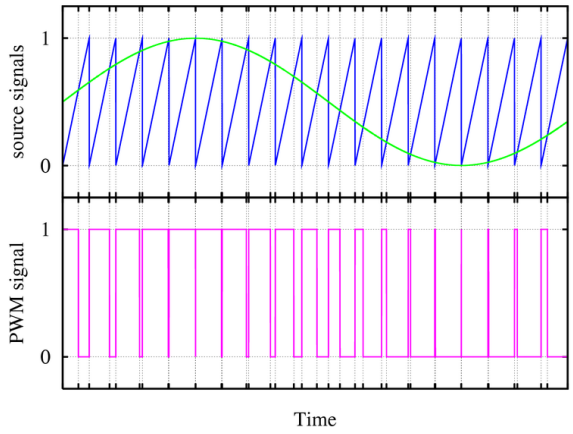


Figure 1.24: PWM modulated sinusoidal signal

Evaluating D class amplifiers performances, can be observed that frequency response is flat on the audible band, with an oscillation lower than 0.5 dB. The phase also is almost linear on this band, just suffering of delays at high frequencies.
The audio quality of D class is lower than A class, due to effects of modulation procedure that introduces harmonic components at high frequencies. Nevertheless THD values can be easily kept below 1%.
The most valuable advantage of D class amplifiers is energy efficiency. All power supply is delivered on load. It's possible to achieve very high efficiency, theoretically up to 100% and using the push-pull configuration, energy consumption is optimized.
No theoretical power dissipation within circuit are expected, for this reason dissipators and cooling fans can be avoided, giving the opportunity to reduce amplifier dimensions considerably.
Due to high audio performances, class D amplifiers are employed in professional audio industry. Usually they are placed at the end of the amplification chain, exploiting their low output impedance.

1.4 AS amplifiers

Architettura Sonora (AS) develops power flexible and high audio quality amplifiers exploiting *ICEPower*[3] technology, to guarantee the highest quality output signal for loudspeakers driving. It produces multi-channel amplifiers, designed to pilot acoustic modules manufactured by AS as well.
AS amplifiers are modular and capable to drive from 1 up to 8 stereo devices (from 2 up to 16 channels) delivering powers from 50W up to 700W for each channel.
AS amplifier implementations with DSPs (digital signal processor) on-board are avail-

[3]Bang&Olufsen technology

able too. These amplifiers exploit computational power of processors to perform equalizations or implement digital cross-over networks [4].

1.4.1 General overview

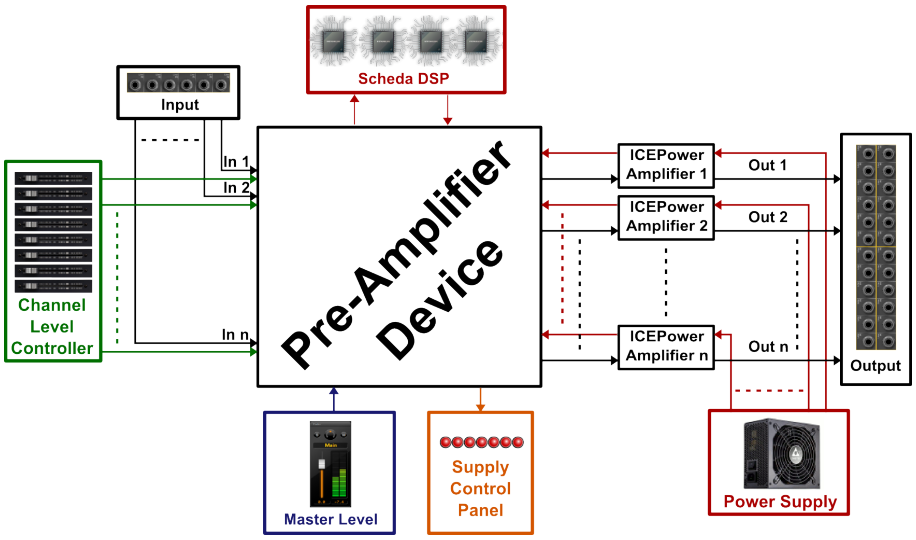


Figure 1.25: AS amplifier blocks scheme

As shown in fig. 1.25, AS amplifiers are composed by two main amplification stages: a *pre-amplification* by means of a preamplifier device, manufactured by AS, and a *final power amplification stage* made up by *Bang&Olufsen* ICEPower D class amplifiers. Preamplifier device has been implemented to easily interface a DSP card, containing *Analog Device* ADAU1701 DSPs, manufactured by AS.
Just one power pack delivers AC current to final stage ICEPower devices. They have also the function to provide DC current to preamplifier board, to supply *VCA* (voltage controlled amplifier) circuits of the card. Note that for each channel there are one VCA and one D class amplifier.
A volume control level panel allows to regulate each channel levels and the main volume level of the system.
Furthermore a led control panel, shows preamplifier malfunctions, occurring when an ICEPower device cannot provide DC supply to VCA of the channel.

1.4.2 Preamplifier board

The blocks scheme of an AS preamplifier board is shown in fig. 1.26. The card is basically composed by two circuital components for each channel: a VCA and a line balancer.
Each VCA extracts current from its channel input signal and returns an amplified signal, as a function of values of volume control level panel triggers (potentiometers). Each VCA is supplied by ICEPower amplifier of the channel.
In tab. 1.1 [5] are shown typical specification values of VCA That2181, manufactured by *That Corporation*, that are employed into AS preamplifier boards.

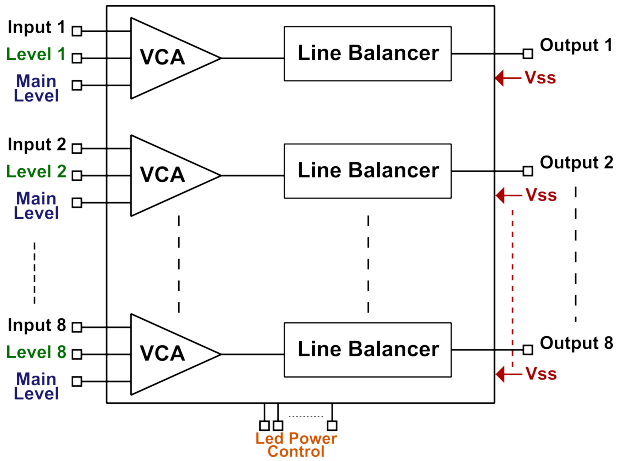


Figure 1.26: 8 channels preamplifier blocks scheme

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
A	Nominal Gain Range		-	130	-	dB
$V_{N,0}$	Idle Noise Voltage	20Hz<f<20kHz	-	9	-	μV
THD+N	THD+N	V_{IN}=1V, f=1kHz	-	0.01	-	%
D	Dynamic range		-	120	-	dB
B_W	Bandwidth		-	20		MHz

Table 1.1: VCA That2181 specifications

In tab. 1.2 [6] are depicts typical values of few specifications of operational amplifiers NE-5532, manufactured by *Philips*, employed in the implementation of output balancers of the AS preamplifier card.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{N,0}$	Idle Noise Voltage	22Hz<f<22kHz	-	4	-	μV
THD+N	THD+N	f=1kHz	-	0.0006	-	%

Table 1.2: AS preamplifier balancers specifications

Complete signal management for each channel, within the preamplifier, is shown in fig. 1.27.
An AS amplifier allows both balanced and unbalanced input. A balanced input signal is made unbalanced by means of a summing block (Signal Adder in the picture). Summing block output flows through an input stage, in which it gets a weak amplification, a high-cut filtering and a phase inversion. It is followed by main pre-amplification (referred in figure as VCA That2181), performed by VCAs, as function of a control level signal computed as summation of channel volume level and main level during the potentiometer stage.
At this point, signal management is assigned to the AS DSP board, which returns a signal with a phase inversion.
AS preamplifier allows two different types of output, in order to feed both the final power amplifiers kinds: stereo mode (SE) and bridge mode (BTL).

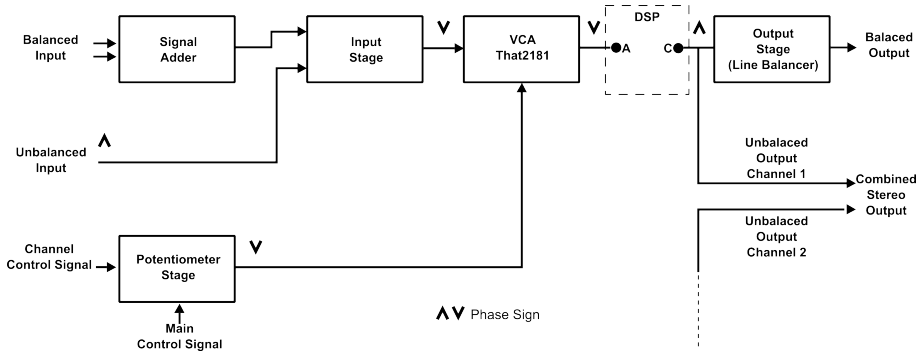


Figure 1.27: Detailed blocks scheme of an AS preamplifier channel

BTL output is a balanced signal, performed by the balancer block, to be suitable for BTL ICEPower input specifications. These final amplifiers require a 7-pins structured input, with 2 poles of the signal and the ground system.
SE output is a combination between the unbalanced output of the current channel and the unbalanced output of the next one, according to the channel couples 1-2, 3-4, 5-6, 7-8. SE ICEPower amplifiers require a 4-pins structured input with preamplifier outputs of the two channels and the ground of the system.

1.4.3 Final power amplifiers

The second and final amplification stage of an AS amplifier is represented by D class amplifiers. Due to high energy efficiency performances, excellent power qualities, low distortions and electronic safety of ICEPower technology, AS prefers these amplifiers, manufactured by Bang&Olufsen, for its purposes.
All the details about operation principles, specifications and performances evaluation of ICEPower amplifiers are treated within the section 1.5.

1.4.4 Performances evaluation

AS amplifier frequency response is identical to final amplifiers one, because VCAs and line balancers of preamplifier have a bandwidth wider than audible range with cut frequencies lower than 20Hz and higher than 20kHz. Frequency response magnitude of ICEPower devices isn't subjected to further attenuations within the full power band and the same happens for the phase linearity.
AS system THD remains almost the same of ICEPower one, because preamplifier doesn't tend to damage audio signals.
Preamplifier contribution is mainly perceived due to noise which it introduces. An increase of about 20 μV of the ICEPower output noise has been noticed. Furthermore, this noise boost becomes higher as delivered power level increase. Nevertheless this aspect doesn't affect considerably the whole system performances, especially when output power are not very high.
AS amplifier efficiency remains high, on average above of 80%, in spite of further power dissipations introduced by the preamplifier, volume level trimmers and the led control panel.

1.5 ICEPower amplifiers

In this section will be depicted ICEPower technologies and their specifications. Devices ICEPower50ASX2, ICEPower125ASX2 and ICEPower1000ASP, manufactured by Bang&Olufsen, will be illustrated referring to official datasheets [11] [12] [13]. As last step, a comparison among performances will be shown, taking into account the following parameters:

- ◇ Power delivered on load (as a function of THD and test input signal frequency)
- ◇ Voltage gain
- ◇ Bandwidth
- ◇ Frequency response
- ◇ Output impedance
- ◇ Total Harmonic Distortion and noise (THD+N)
- ◇ Open circuit noise voltage
- ◇ Intermodulation distortion
- ◇ Dissipated power
- ◇ Figure of merit η
- ◇ Power before shutdown
- ◇ Stand-by power
- ◇ Quiescent power
- ◇ Dynamic range (ratio between maximum and minimum undistorted output signal voltage, in dB scale)
- ◇ Load impedance Range

1.5.1 COM, HCOM and MECC topologies

Basic D class amplifiers based on PWM method, as that is shown in fig. 1.23, have several limitations [9]:

- ◇ don't provide a power supply rejection (PSR)
- ◇ distortions due to transistors in the amplification stage
- ◇ output demodulation filter is not linear, yielding distortions and an output impedance strongly frequency dependent

To overcome these limitations a system having a feedback control is indispensable [9].

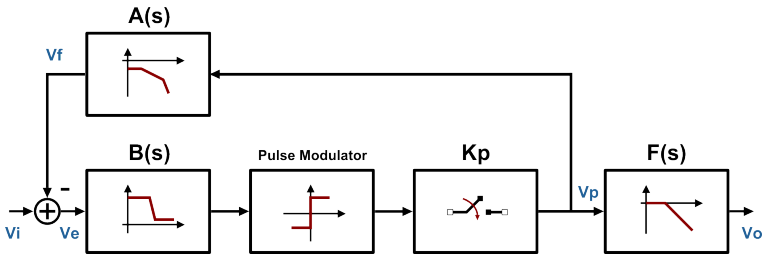


Figure 1.28: COM topology switching amplifier

The controlled oscillation modulator (COM), is a system having an auto-oscillation feedback path. It's composed by just one loop which gets the signal just after the

switching circuit. Blocks scheme of COM topology is shown in fig. 1.28.
COM technology assures following advantages:

- ◇ increase of power supply rejection ratio (PSRR) which reaches 60dB
- ◇ decrease of distortions introduced by transistors

On the other hand, the main drawbacks [9] are:

- ◇ correction effect provided by loop ignores the output filter for which no correction error is performed
- ◇ feedback introduction makes the system frequency response load dependent, thus stability is not guaranteed especially for capacitive loads

With the aim to overcome these COM limits, a hybrid variation has been developed: HCOM (hybrid feedback controlled oscillation modulator). ICEPower50ASX2 and ICEPower125ASX2 exploit this technology.

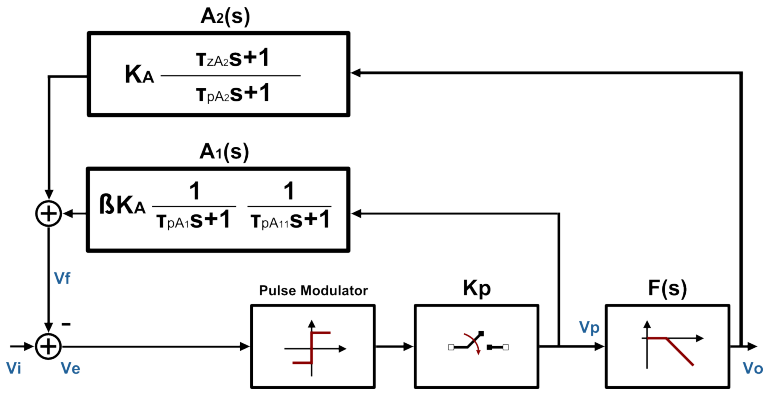


Figure 1.29: HCOM topology switching amplifier

An example of a HCOM amplifier is shown in fig. 1.29. The circuit is composed by two feedback paths giving to this topology several qualities [9]:

- ◇ filter output error compensation is provided exploiting the second feedback path
- ◇ output impedance is reduced
- ◇ system frequency response is load independent, except for purely capacitive loads

ICEPower exploits also benefits of multivariate enhanced cascade control (MECC). An implementation of this topology is shown in fig. 1.30.

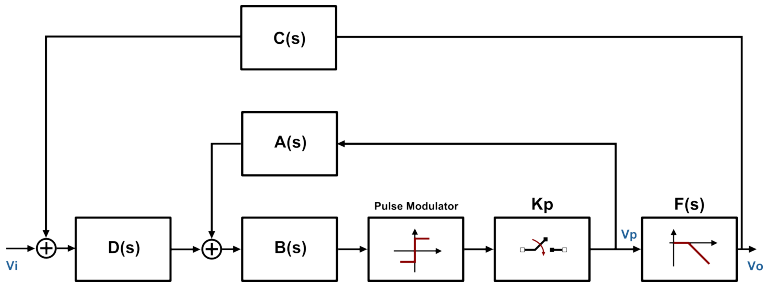


Figure 1.30: MECC topology switching amplifier

MECC topology has two feedback paths. The first after the output filter $F(s)$, to

compensate the non linearities of the filter, and a second loop before the filter $F(s)$, to correct non linearities due to the amplification stage and the modulation[7].
This topology gives several advantages in respect to the basic PWM amplifier [10]:

- ◇ gives high power with low distortions
- ◇ keeps low the circuital complexity
- ◇ increases the PSRR (power supply rejection ratio)
- ◇ achieves a load variations independence

COM (or HCOM) and MECC technologies combination, gives to ICEPower amplifiers the following benefits:

- ◇ extension of full power band (from 10Hz up to 20kHz)
- ◇ distortion reduction with THD value lower than 1%
- ◇ output impedance load independent, except for purely capacitive loads
- ◇ low output impedance [8]

1.5.2 ICEPower50ASX2

ICEPower50ASX2 is an integrated device manufactured in two types. Single-ended (SE) version with stereo output and the bridge (BTL) version with mono output. It's a reliable and safe device, giving protections in case of overheating or power overload.

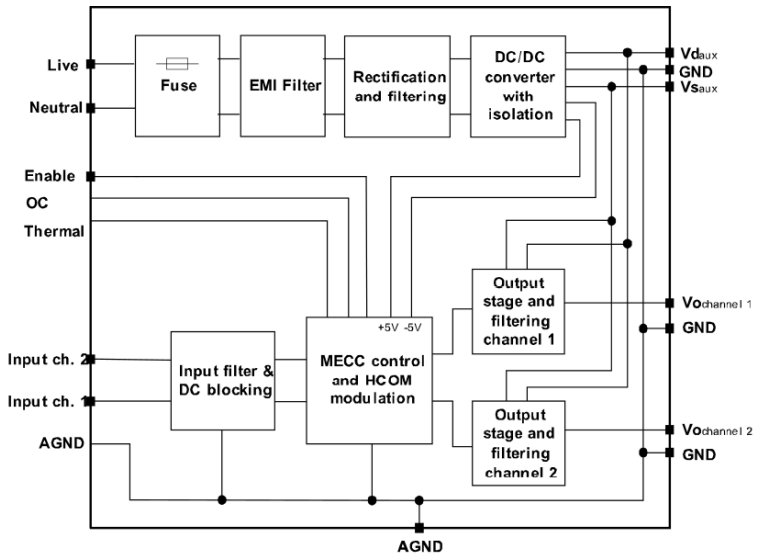


Figure 1.31: ICEPower50ASX2 amplifier blocks scheme

As depicted in fig. 1.31, it has 5 areas for external interfacing. Input and output areas, power supply interface, auxiliary voltage output up to ±25V and the area of pins for additional/protective functions as overheating, overload detection or safety shutdown.

ICEPower50ASX2-SE technical specifications

In tab. 1.3 and 1.4 are shown technical specifications of ICEPower50ASX2 device in stereo mode.

If not specified reference conditions are: f=1kHz, P_O=1W, T_a=25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_O	Output Power @ 1% THD+N 20Hz<f<20kHz both channel driven	R_L=4Ω 230 V_{ac}/50Hz	-	47	-	W
P_O	Output Power @ 1% THD+N 20Hz<f<20kHz one channel driven	R_L=4Ω 230 V_{ac}/50Hz	-	50	-	W
A_V	Nominal Gain Voltage	f=1kHz	20	20.5	21	dB
f	Frequency response	20Hz - 20kHz All loads	-	±0.1	±0.5	dB
f_U	Upper Bandwidth limit (-3dB)	R_L=4Ω R_L=8Ω	- -	130 95	- -	kHz kHz
f_L	Lower Bandwidth limit (-3dB)	All loads	-	1.5	-	Hz
THD+N	THD+N (4Ω)	f=100Hz P_O=1W	-	0.003	0.01	%
IMD	Intermodulation	f=18.5kHz,1kHz P_O=10W	-	0.0007	-	%
TIM	Transient intermodulation	P_O=10W	-	0.007	-	%
$V_{N,0}$	Output idle Noise		15	25	70	μV
D	Dynamic range	50W,4Ω	-	120	-	dB
Z_O	Output Impedance	f=1kHz	-	14	25	mΩ
Z_L	Load Impedance range		3	4	∞	Ω

Table 1.3: ICEPower50ASX2-SE general audio specifications

If not specified reference conditions are: f=1kHz, R_L=4Ω, 230V mains, T_a=25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_T	Continuous output Power without thermal shutdown Both channel driven		-	43	-	W
P_{SMPS}	Quiescent power consumption Amplifier Disabled	Enable pin low	-	4	-	W
P_Q	Quiescent Power consumption Amplifier Enabled	P_O=0W	-	7	-	W
η	Total Power Efficiency	P_0=100W P_0=170W	- -	80 81	- -	% %

Table 1.4: ICEPower50ASX2-SE power specifications

ICEPower50ASX2-BTL technical specifications

In tab. 1.5 and 1.6 are shown technical specifications of ICEPower50ASX2 device in mono mode.

If not specified reference conditions are: f=1kHz, P_O=1W, T_a=25℃

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_O	Output Power @ 1% THD+N 20Hz<f<20kHz	R_L=4Ω 230 V_{ac}/50Hz	-	170	-	W
A_V	Nominal Gain Voltage	f=1kHz	26	27	28	dB
f	Frequency response	20Hz - 20kHz All loads	-	±0.2	±0.6	dB
f_U	Upper Bandwidth limit (-3dB)	R_L=4Ω R_L=8Ω	- -	100 75	- -	kHz kHz
f_L	Lower Bandwidth limit (-3dB)	All loads	-	1.5	-	Hz
THD+N	THD+N (4Ω)	f=100Hz P_O=1W	-	0.002	0.005	%
IMD	Intermodulation	f=18.5kHz,1kHz P_O=10W	-	0.0002	-	%
TIM	Transient intermodulation	P_O=10W	-	0.003	-	%
$V_{N,0}$	Output idle Noise		15	20	70	μV
D	Dynamic range	170W,4Ω	-	125	-	dB
Z_O	Output Impedance	f=1kHz	-	18	30	mΩ
Z_L	Load Impedance range		3	4	∞	Ω

Table 1.5: ICEPower50ASX2-BTL general audio specifications

If not specified reference conditions are: f=1kHz, R_L=4Ω, 230V mains, T_a=25℃

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_T	Continuous output Power without thermal shutdown		-	50	-	W
P_{SMPS}	Quiescent power consumption Amplifier Disabled	Enable pin low	-	4	-	W
P_Q	Quiescent Power consumption Amplifier Enabled	P_O=0W	-	7	-	W
η	Total Power Efficiency	P_0=100W P_0=170W	- -	80 81	- -	% %

Table 1.6: ICEPower50ASX2-BTL power specifications

1.5.3 ICEPower125ASX2

ICEPower50ASX2 is an integrated device manufactured in only one type. It gives the capability to work in two different modes: single-ended (SE) mode with stereo output and the bridge (BTL) mode with mono output. The operation modes are selectable through hardware configuration.

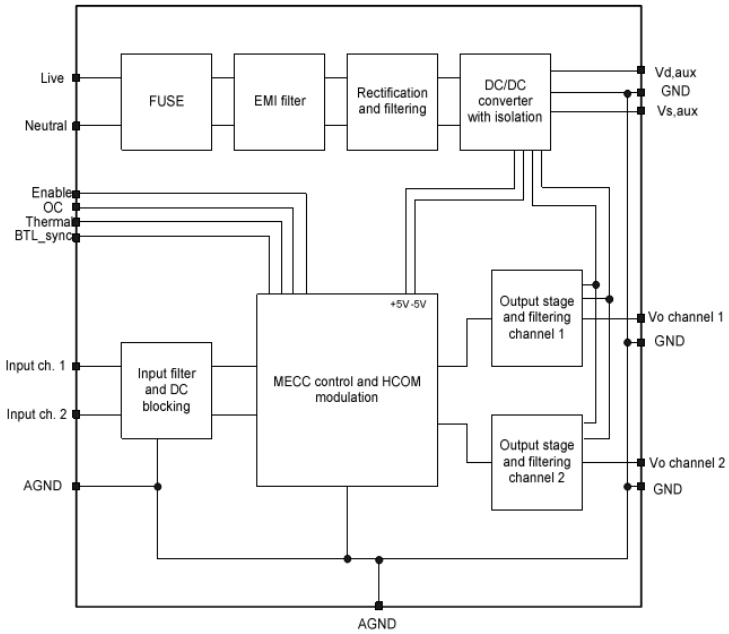


Figure 1.32: ICEPower125ASX2 amplifier blocks scheme

As it shown in fig. 1.32, this amplifier has the same 5 interfacing areas of the ICE-Power50ASX2, with the adding of pin *BTL_sync*. If this pin is put low the amplifier works in BTL mode, conversely the selected operation modality will be the stereo one.

ICEPower125ASX2-SE technical specifications

In tab. 1.7 and 1.8 are shown technical specifications of ICEPower50ASX2 device in stereo mode.

If not specified reference conditions are: f=1kHz, P_O=1W, T_a=25℃

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_O	Output Power @ 1% THD+N 20Hz<f<20kHz both channel driven	R_L=4Ω 230 V_{ac}/50Hz	-	120	-	W
P_O	Output Power @ 1% THD+N 20Hz<f<20kHz one channel driven	R_L=4Ω 230 V_{ac}/50Hz	-	130	-	W
A_V	Nominal Gain Voltage	f=1kHz	24.3	24.8	25.3	dB
f	Frequency response	20Hz - 20kHz All loads	-	±0.15	±0.5	dB
f_U	Upper Bandwidth limit (-3dB)	R_L=4Ω R_L=8Ω	- -	120 90	- -	kHz kHz
f_L	Lower Bandwidth limit (-3dB)	All loads	-	1.5	-	Hz
THD+N	THD+N (4Ω)	f=100Hz P_O=1W	-	0.003	0.01	%
IMD	Intermodulation	f=18.5kHz,1kHz P_O=10W	-	0.0009	-	%
TIM	Transient intermodulation	P_O=10W	-	0.007	-	%
$V_{N,0}$	Output idle Noise		20	30	80	μV
D	Dynamic range	125W,4Ω	-	117	-	dB
Z_O	Output Impedance	f=1kHz	-	18	25	mΩ
Z_L	Load Impedance range		3	4	∞	Ω

Table 1.7: ICEPower125ASX2-SE general audio specifications

If not specified reference conditions are: f=1kHz, R_L=4Ω, 230V mains, T_a=25℃

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_T	Continuous output Power without thermal shutdown Both channel driven		-	65	-	W
P_{SMPS}	Quiescent power consumption Amplifier Disabled	Enable pin low	-	6	-	W
P_Q	Quiescent Power consumption Amplifier Enabled	P_O=0W	-	9.5	-	W
η	Total Power Efficiency	P_0=100W, 4Ω P_0=400W, 4Ω P_0=500W, 4Ω P_0=250W, 8Ω	- - - -	75 80.4 81.4 86.4	- - - -	% % % %

Table 1.8: ICEPower125ASX2-SE power specifications

ICEPower125ASX2-BTL technical specifications

In tab. 1.9 and 1.10 are shown technical specifications of ICEPower50ASX2 device in mono mode.

If not specified reference conditions are: f=1kHz, P_O=1W, T_a=25℃

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_O	Output Power @ 1% THD+N 20Hz<f<20kHz	R_L=4Ω 230 V_{ac}/50Hz	-	450	-	W
A_V	Nominal Gain Voltage	f=1kHz	29.7	30.7	31.7	dB
f	Frequency response	20Hz - 20kHz All loads	-	±0.3	±0.7	dB
f_U	Upper Bandwidth limit (-3dB)	R_L=4Ω R_L=8Ω	- -	100 70	- -	kHz kHz
f_L	Lower Bandwidth limit (-3dB)	All loads	-	1.5	-	Hz
THD+N	THD+N (4Ω)	f=100Hz P_O=1W	-	0.003	0.005	%
IMD	Intermodulation	f=18.5kHz,1kHz P_O=10W	-	0.0003	-	%
TIM	Transient intermodulation	P_O=10W	-	0.006	-	%
$V_{N,0}$	Output idle Noise		25	35	80	μV
D	Dynamic range	500W,4Ω	-	121	-	dB
Z_O	Output Impedance	f=1kHz	-	18	30	mΩ
Z_L	Load Impedance range		3	4	∞	Ω

Table 1.9: ICEPower125ASX2-BTL general audio specifications

If not specified reference conditions are: f=1kHz, R_L=4Ω, 230V mains, T_a=25℃

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_T	Continuous output Power without thermal shutdown		-	70	-	W
P_{SMPS}	Quiescent power consumption Amplifier Disabled	Enable pin low	-	6	-	W
P_Q	Quiescent Power consumption Amplifier Enabled	P_O=0W	-	9.5	-	W
η	Total Power Efficiency	P_0=100W, 4Ω P_0=400W, 4Ω P_0=500W, 4Ω P_0=250W, 8Ω	- - - -	75 80.4 81.4 86.4	- - - -	% % % %

Table 1.10: ICEPower125ASX2-BTL power specifications

1.5.4 ICEPower1000ASP

It's an integrated device ables to deliver high power with high efficiency. As it shown in fig. 1.33, this amplifier has 6 interfacing areas. Input, output and power supply areas, auxiliary voltage output (with 4 different DC voltages available), monitoring interface, protection area and an interface to manage the clipping detection and its removing.

ICEPower1000ASP technical specifications

In tab. 1.11 and 1.12 are shown technical specifications of ICEPower1000ASP.

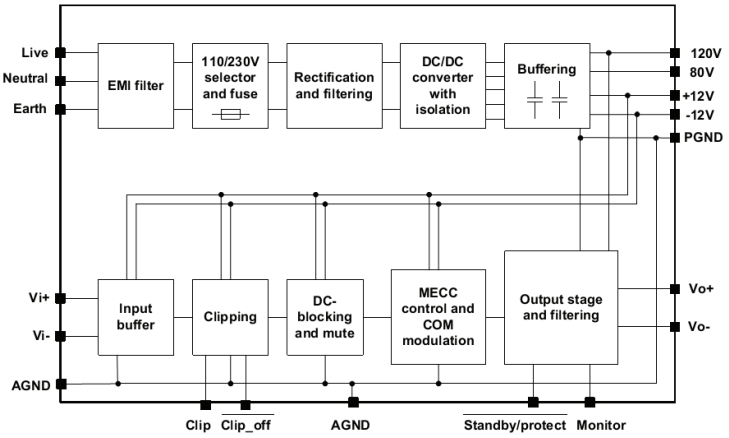


Figure 1.33: ICEPower1000ASP amplifier blocks scheme

If not specified reference conditions are: f=1kHz, P_O=1W, T_a=25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_O	Output Power @ 0.2% THD+N 10Hz<f<20kHz	R_L=4Ω R_L=8Ω	- -	1100 525	- -	W W
P_O	Output Power @ 1% THD+N 10Hz<f<20kHz	R_L=4Ω 230 V_{ac}/50Hz	-	1175	-	W
A_V	Nominal Gain Voltage	f=1kHz	26.7	27.2	27.7	dB
f	Frequency response	20Hz - 20kHz All loads	-	±0.5	±1	dB
f_U	Upper Bandwidth limit (-3dB)	R_L=4Ω R_L=8Ω	- -	31 38	- -	kHz kHz
f_L	Lower Bandwidth limit (-3dB)	R_L=4Ω R_L=8Ω	- -	5.3 5.3	- -	Hz Hz
THD+N	THD+N (4Ω)	f=100Hz P_O=1W	-	0.007	0.015	%
IMD	Intermodulation	f=14kHz,15kHz P_O=10W	-	0.002	-	%
TIM	Transient intermodulation	P_O=10W	-	0.003	-	%
$V_{N,0}$	Output idle Noise		65	80	105	μV
D	Dynamic range		115	118	120	dB
Z_O	Output Impedance	f=1kHz	-	5	10	mΩ
Z_L	Load Impedance range		2	4	∞	Ω

Table 1.11: ICEPower1000ASP general audio specifications

If not specified reference conditions are: f=1kHz, R_L=4Ω, 230V mains, T_a=25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P_T	Continuous output Power without thermal shutdown		-	85	-	W
P_{SMPS}	Stand-by power dissipation	Amplifier Disabled	-	4.1	-	W
P_Q	Quiescent Power consumption Amplifier Enabled	P_O=0W	-	15.8	-	W
η	Total Power Efficiency	P_0=1000W P_0=500W	- -	79 78	- -	% %

Table 1.12: ICEPower1000ASP power specifications

1.5.5 Evaluations

It's interesting to compare ICEPower evaluations under the same conditions.
Typical gain values are shown if tab. 1.13 for test sinusoidal input signal with $f = 1kHz$ and load impedance $R_L = 4\Omega$.

	50ASX2-SE	50ASX2-BTL	125ASX2-SE	125ASX2-BTL	1000ASP
$\mathbf{A_V}$ (dB)	20.5	27	24.8	30.7	27.2

Table 1.13: Gain voltages of DUTs

Best device, looking at gain values, is ICEPower125ASX2 in BTL mode.

Taking into account bandwidth of full power band and the dB fluctuations in respect to the flat reference, DUTs frequency characteristics analysis have been proposed. Evaluations are made taking into account input sinusoidal signals with frequencies within the range 20Hz-20kHz and a load impedance of 4Ω. Typical values are shown in tab. 1.14.

	50ASX2-SE	50ASX2-BTL	125ASX2-SE	125ASX2-BTL	1000ASP
f (dB)	±0.1	±0.2	±0.15	±0.3	±0.5
$\mathbf{f_U}$ (kHz)	95	75	90	70	31
$\mathbf{f_L}$ (Hz)	1.5	1.5	1.5	1.5	5.3

Table 1.14: Frequency responses of DUTs

It can be noted that the device with the more flat and wide frequency response is ICEPower50ASX2-SE. Nevertheless all amplifiers guarantee a flat behavior in the audible range.

It's crucial evaluate the delivered power as a function of distortions and efficiency of the DUT. Typical values are shown in tab. 1.15, 1.16, 1.17 and 1.18.

Evaluations made under conditions: 1% THD+N, 10Hz<f<20kHz, R_L=4Ω, T_a=25°C.
For stereo amplifiers (SE) has been considered just one output channel applied to the load

	50ASX2-SE	50ASX2-BTL	125ASX2-SE	125ASX2-BTL	1000ASP
$\mathbf{P_O}$ (W)	50	170	130	450	1175

Table 1.15: Power

Evaluations made under conditions: f=100Hz, P_OW, R_L=4Ω

	50ASX2-SE	**50ASX2-BTL**	**125ASX2-SE**	**125ASX2-BTL**	**1000ASP**
THD+N (%)	0.003	0.002	0.003	0.003	0.007

Table 1.16: Distortion

Evaluations made under conditions: P_O=10W, f1=18.5kHz, f2=1kHz per 50ASX2 e 125ASX2.
For 1000ASP: P_O=10W, f1=14kHz, f2=15kHz.

	50ASX2-SE	**50ASX2-BTL**	**125ASX2-SE**	**125ASX2-BTL**	**1000ASP**
IDM (%)	0.0007	0.0002	0.0009	0.0003	0.002
TIM (%)	0.007	0.003	0.007	0.006	0.003

Table 1.17: Intermodulation distortion

Evaluations made under conditions: f=1kHz, R_L=4Ω

	50ASX2-SE	**50ASX2-BTL**	**125ASX2-SE**	**125ASX2-BTL**	**1000ASP**
η (%), P_O=100W	80	80	75	75	-
η (%), P_O=170W	81	81	-	-	-
η (%), P_O=400W	-	-	80.4	80.4	-
η (%), P_O=500W	-	-	81.4	81.4	78
η (%), P_O=1000W	-	-	-	-	79

Table 1.18: Efficiency

From tab 1.15, 1.16, 1.17 and 1.18, following considerations can be made:

- ◇ The device ables to deliver the highest power with the lowest THD is the ICEPower1000ASP. From technical data of this device (tab. 1.11), it can be seen that the amplifier can deliver 1000W keeping THD+N under 0.2%.
- ◇ ICEPower50ASX2-BTL can deliver higher power than ICEPower125ASX2-SE, with better performances of THD+N at low frequencies, intermodulation distortions and efficiency up to 100W.
- ◇ ICEPower50ASX2-BTL has the lowest percentage of distortions among the DUTs
- ◇ ICEPower1000ASP gives highest powers paying higher distortions percentage, however limited to the third decimal digit
- ◇ Among ASX2s, ICEPower50ASX2-BTL offers better intermodulation distortion performances. However all DUTs have high qualities under this aspect.
- ◇ Up to power of 500W, ICEPower125, both SE and BTL, gives a better efficiencies and lower distortions than ICEPowerASP.

Let us conclude, comparing typical values of output impedance Z_O (when has been applied a signal test with f=1kHz) and the noise at void $V_{N,0}$. Tab. 1.19 shows these results.

	50ASX2-SE	**50ASX2-BTL**	**125ASX2-SE**	**125ASX2-BTL**	**1000ASP**
$\mathbf{A_{N,0}}$ (μV)	25	20	30	35	80
$\mathbf{Z_O}$ (mΩ)	14	18	18	18	5

Table 1.19: Open circuit noise and output impedance

From values of tab. 1.19, we can conclude that the best output impedance belongs to ICEPower1000ASP, but having a higher idle noise level. However these voltage noise have values of μV, thus with perceptive effects not perceivable by human ear.

Concluding, all DUTs have high fidelity characteristics both for performances and electronic safety. Choice of one rather than an other must be evaluated taking into account:

- ◇ Delivered power
- ◇ Maximum distortion which can be paid
- ◇ Type of output signal (balanced or unbalanced)
- ◇ Desired efficiency

Chapter 2

Analog Device ADAU1701 processor

DSPs used within some AS amplifiers, are manufactured by Analog Devices. They constitute the core of signal processing, during the realization of solutions needed to pilot peculiar composite audio diffusion systems.
In this chapter will be depicted the features of the ADAU1701 processor and its operation principles.
Analog Device, to realize ADC and DAC mounted on ADAU1701 chip board, exploits conversion techniques known as Sigma-Delta. A brief summary of this technology will be illustrated at the beginning of the chapter.

2.1 Sigma-Delta architecture

With the development of digital filtering, A/D and D/A conversions have been rebuilt in order to be integrated into VLSI (very large scale integration) systems and achieve low distortion artifacts [14].
Sigma-Delta is a digital converter architecture on board of ADAU1701 chips and its technology is based on concepts of: oversampling, noise shaping and decimation.

1. **Oversampling**
   Is a method that consists in to consider a digital signal as it has been sampled with a sampling frequency higher than its real sampling rate. This produces an effect of spectrum shrinking, reducing aliasing effects.
2. **Noise shaping**
   It's an operation of shaping the quantization error power spectrum, gathering the most of frequency content onto specific frequency bands, in order to be easily filtered out exploiting digital filters after the noise shaper.
3. **Decimation**
   It's a low-pass filtering followed by a downsampling. A M downsampling operation, is a process that, assigned a signal sampled with a sampling rate of f_s, takes just the M-samples discarding all the others. This produce the opposite effect of oversampling, extending the spectrum, increasing the risk of aliasing. To avoid aliasing, the decimation process, provides a low-pass filtering with a cut frequency equal to π/M, before the downsampler.

After this operation a signal is considered as it has a new sampling frequency lower than the previous one.

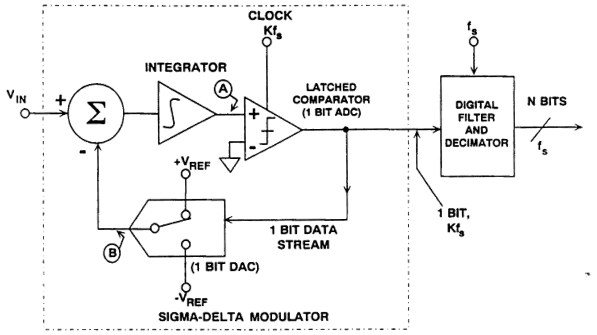


Figure 2.1: First-order Sigma-Delta ADC

A Sigma-Delta A/D converter is composed by 4 main blocks: an oversampling block, a noise shaper, a digital filter and a decimator. Fig. 2.1 shows a scheme of a first-order Sigma-Delta A/D converter. The operation of sampling and oversampling is performed by the *Latch Comparator* and the *Integrator*. While noise shaping operation is performed by the feedback loop and the *DAC 1-bit*. In this way output signal has a quantization noise gathered at high frequencies, so it can be removed by a low-pass filter. Filtering is followed by a decimation to bring the signal back to its original frequency rate. Sigma-Delta D/A conversion can be thought as an inverse procedure

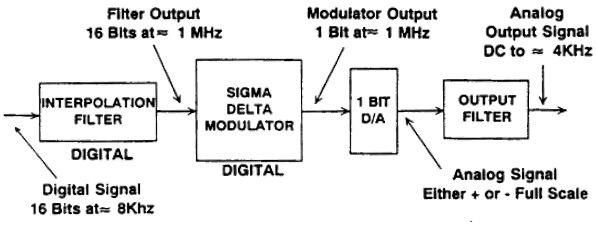


Figure 2.2: Sigma-Delta DAC

of A/D conversion, where all the basic functions of the digital filter and modulator are the same of those related to the A/D converter. Also for this converter, oversampling gives an advantage to avoid aliasing. Fig. 2.2 shows a blocks scheme of a Sigma-Delta D/A converter. All the blocks are the same of the A/D converter except for the modulator, which is digital in this implementation.

2.2 The DSP

ADAU1701 is a complete single chip audio system equipped with:

- ◇ 1 audio DSP, working at 28 bits or at double precision (56 bits)
- ◇ 2 Sigma-Delta ADC (Analog Digital Converter)
- ◇ 4 Sigma-Delta DAC (Digital Analog Converter)
- ◇ 4 auxiliary ADCs

◇ 2 micro-controller interfaces

DSP under analysis is completely programmable. This capability results extremely simple exploiting SigmaStudio software, which allows to graphically configure a processing signal operations flow, through functional blocks, as biquad filters, level and *GPIO* (General Purpose Input/Output) interface controllers [15].
Programs can be loaded into DSP at startup by means of an EEPROM memory or an external micro-controller. At shutdown, it's possible to write the internal chip parameters onto the EEPROM, and automatically recall them at next startup.
The device communicates through an I^2C bus or a SPI port with 4 connectors.

2.2.1 Architecture

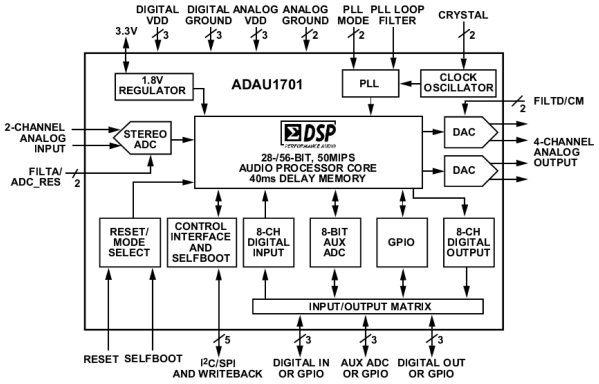


Figure 2.3: Functionalities blocks diagram of ADAU17010

Fig. 2.3 shows the chip architecture.
Analog signal input section is composed by the block *Stereo ADC* that is a stereo A/D converter. While the analog output section has 4 D/A converters, in the picture represented by 2 stereo DACs. Each chip guarantees two analog inputs and 4 analog outputs.
The whole system is supplied by a voltage regulator which allows to give DC voltage of 1.8V getting in input DC voltage of 3.3V.
ADAU1701 has its own clock circuit. Section related to the system clock is represented by blocks *PLL* and *Clock oscillator*
Very important section is the *control port*, depicted in the picture as *Control Interface and SelfBoot*. This is the communication interface with the DSP, which can be driven by an EEPROM or a micro-controller.
The second communication interface is the GPIO (General Purpose Input/Output). All the blocks connected to *Input/Output Matrix* belongs to this interfacing section.

2.2.2 General audio and power specifications

The following tables report the main general audio specifications of the chip. Parameters about analog behavior of the chip are crucial to understand its audio properties, so ADC and DAC technical specifications have been highlighted.
Tab. 2.1 and 2.2 show ADC and DAC audio characteristics.

If not specified, reference conditions are: AVDD = 3.3 V, DVDD = 1.8 V, PVDD = 3.3 V, IOVDD = 3.3 V, master clock input = 12.288 MHz

Symbol	Parameter	Min.	Typ.	Max.	Units
N_{CH}	Number of Channels	-	2	-	
Res	Resolution	-	24	-	Bits
SNR	Signal to Noise Ratio	-	100	-	dB
D	Dynamic Range	95	100	-	dB
THD+N	Total Harmonic Distortion and Noise	-	-83	-	dB
C_{tlk}	Analog channel-to-channel Crosstalk	-	-82	-	dB

Table 2.1: ADAU1701 ADC audio specifications

If not specified, reference conditions are: AVDD = 3.3 V, DVDD = 1.8 V, PVDD = 3.3 V, IOVDD = 3.3 V, master clock input = 12.288 MHz

Symbol	Parameter	Min.	Typ.	Max.	Units
N_{CH}	Number of Channels	-	4	-	
Res	Resolution	-	24	-	Bits
SNR	Signal to Noise Ratio	-	104	-	dB
D	Dynamic Range	99	104	-	dB
THD+N	Total Harmonic Distortion and Noise	-	-90	-	dB
C_{tlk}	Analog channel-to-channel Crosstalk	-	-100	-	dB

Table 2.2: ADAU1701 DAC audio specifications

2.2.3 The Chip

In fig.2.4 is depicted the chip with its 48 connection pins. Are highlighted the input (green), output (yellow) ports, the control interface (red) and the multi-purpose (GPIO) connection (blue). Control ports is used to write/read instructions or parameters to/from internal RAM memory and registers. While GPIO interface is used to write/read setting parameters during a processing or to manage digital input/output and auxiliary A/D converters.

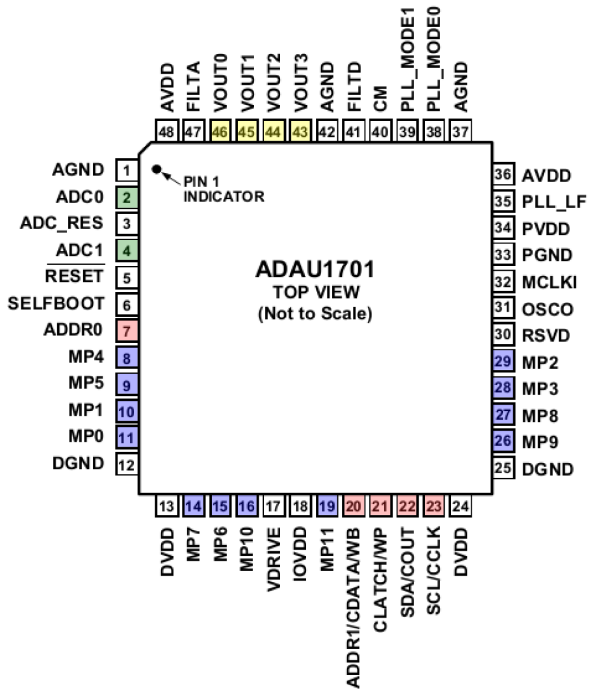


Figure 2.4: 'ADAU1701 pins scheme

In fig. 2.5 is shown a complete circuital system using an ADAU1701, highlighting connection pins between the chip and the external blocks necessary to the system operation.

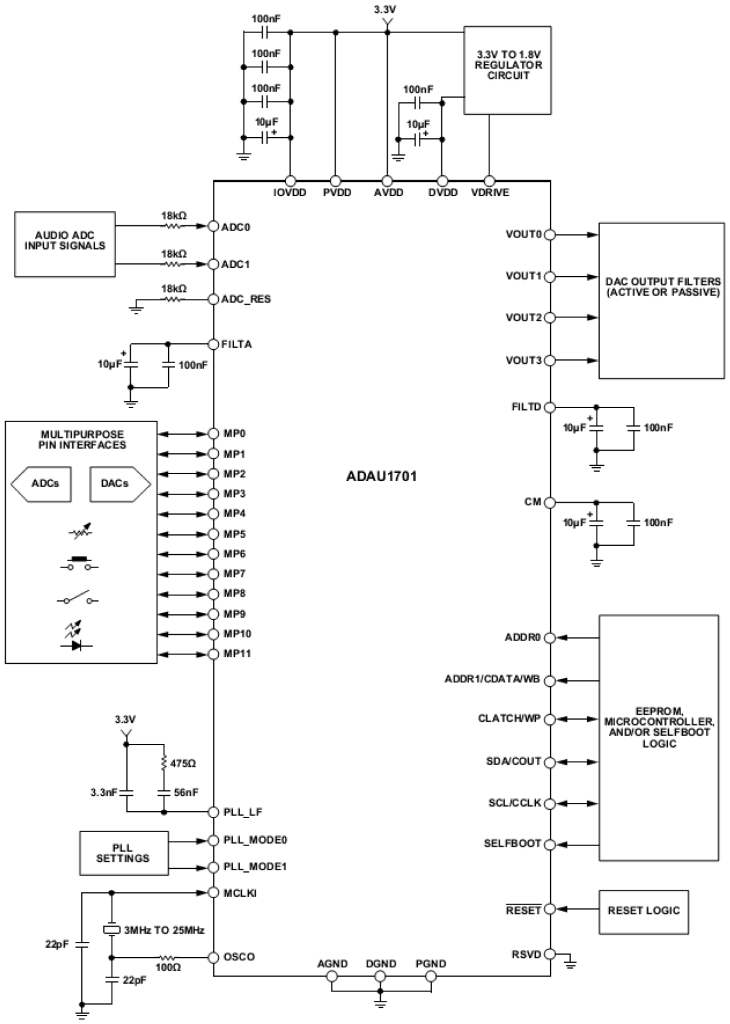


Figure 2.5: Blocks scheme of a system with ADAU1701

2.2.4 The Core

The microprocessor represents the core of a ADAU1701.
It's equipped by:

- ◇ a fixed-point ALU with 28 bits input multiplier and 56 bits accumulator for full-precision operation
- ◇ an internal ROM memory, which stores the default program, automatically started at system startup. This default program provides a simple association among ADCs, DACs and serial input/output as shown in fig. 2.6
- ◇ 34 registers of 8, 16, 32 or 40 bits
- ◇ 1 Parameter RAM with 1024 32-bits locations, for the parameters storing
- ◇ 1 Program RAM with 1024 40-bits locations, for program instructions storing

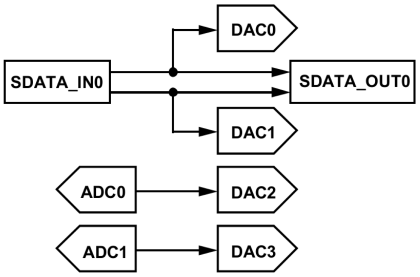


Figure 2.6: Default program of input/output association

All these 3 memory areas (2 RAMs and 34 registers), are considered as a unique block for locations indexing. Considering that the total locations numbers is 2088, it follows that words of 11 bits (2 byte with the first 5 MSB equal to 0) are able to index each address.

2.2.5 Internal number representation

ADAU1701 manages number values with a 28 bits fixed-point representation in a signed 5.23 format. First MSB represents the sign bit (0 for positive numbers and 1 for negative ones), 4 bits for the integer part and 23 bits for fractional component. In this scenario the *dynamic range* and *resolution* of the number representation are:

- ◇ dynamic range: $(2^4 - 2^{-23} : -2^4) = (15.999999880790710449218 75 : -16)$
- ◇ resolution: $2^{-23} = 0.00000011920928955078125$

Thus the signed 5.23 numbers representation manages decimal real number strictly bounded into its dynamic range and all representable real values are equally spaced of the resolution quantity. Each real number in order to be represented in 5.23 format must be quantized taking into account the quantization step of 2^{-23} and the bounding limits of the dynamic range.
All negative values are two's complemented.

2.3 Operation modes

Control port, made up by 5 pins highlighted in red in fig.2.4, represents the main communication interface of the device. It can be used to directly write programs which core will execute or read/write registers and parameters. Control port can operate in 2 different modes, using either I^2C or SPI protocol. While ADAU1701 has 3 principles of operation:

1. I^2C (Inter-Integrated Circuit), 2 communication wires interface
2. SPI (Serial Peripheral Interface), 4 communication wires control interface
3. Self-boot mode, allows system utilization avoiding an external micro-controller, which is essential in the previous operation modes

In all the previous operation modes, control port allows read/write operations onto all the memory locations of the chip.

2.3.1 Initialization

At system boot, or reboot, in order to a correct initialization of an ADAU1701, are required 3 steps, the former automatically executed:

1. Power-Up sequence. It consists in 3 inner steps, all automatically executed at boot or reboot:
   (a) Default program is loaded into Program RAM from the ROM of the Core. This program performs an associations among input and outputs, referring to the scheme shown in fig.2.6
   (b) All registers and parameters are set to 0
   (c) System provides to lock the oscillator to the PLL circuit, in order to generate the main clock of the whole system
2. It's necessary to set the Core Control Register bits [4:2] to 1, in order to enable signal processing and remove the muting of all ADCs and DACs
3. It's necessary to initialize the DAC Setup Register bits [1:0] to 01, in order to enable DACs

These were the main initialization steps, then it's possible to effectuate other settings, as sampling rate choice or EEPROM write protection enabling.

2.3.2 I^2C

It's the default device communication mode. It's enabled at boot and it consists in a 2 wires connection.
The SDA (Serial Data) pin carries data in both directions: outgoing from the Core to controller and in input to the Core from the controller. SCL (Serial Clock) pin is the connection which carries the system main clock. It's an input pin in I^2C mode, where a controller or a generic Master, controls the timing of ADAU1701, which works as Slave.
Note that in Self-boot mode, SCL is an output pin, since in this operation mode the DSP generates its own system clock, which is also used to time the EEPROM.

In this operation mode, an ADAU1701 works for all the time as a Slave and so it cannot start any data transfer. Each Slave is recognized by an unambiguous address (Chip address), assigned through pins ADDR1 and ADDR0 of the chip. As a result just 4 unambiguous addresses are available, thus just 4 Slave devices for each micro-controller are permitted.
Address format of a Chip Slave, is shown in tab.2.3. It can be noted that into the address is specified also the type of request performed by the Master, through the bit $R/\bar{W}$. If bit $R/\bar{W}$ is 1 a read operation has been required, conversely for a write the bit value is 0.

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	1	1	0	1	ADDR1	ADDR0	$R/\bar{W}$

Table 2.3: Chip Salve address in I^2C mode

Data transfer

Data transfer, in I^2C mode, is enclosed between two conditions: Start Condition and Stop Condition, which can be sent by the Master at any given moment of the transfer. At the beginning, each Slave device is in a listening state (Idle), in which it's able to receive a Start Condition to enable itself.
Start Condition is coded giving a high-to-low variation on pin SDA while the signal

on SCL remains high. Once this message has been sent onto the bus I^{2}C, on which all the Slaves are listening, all ADAU1701 devices enable themselves to receive the first byte of the Chip Address, in order to understand who is the addressee and what type of operation is required.
At the clock cycle subsequent to the Start Condition, the Master provides to sent the first byte, composed by the Chip Address (7 bits) and the request type ((bit R/$\bar{W}$). Since the connection has just one communication data wire, 8 clock cycles are necessary to forward one byte. Slave device which recognizes to be the addressee of the query, enables itself and answers, at ninth clock cycle, with a 0 on the SDA. This is an Acknowledgement Slave (AS) bit, which says, to the controller, that the queried Slave is active and ready to get new data.
At this stage, Master sends the first byte of the Slave memory location (Subaddress[0]) address, to read or write. Once transaction is done, the Slave answers with an AS bit. The operation is repeated for the next byte, containing the Slave address memory second part (Subaddress[1]). Again the Salve answers with an AS as transaction is done. If, for instance, the address is wrong, the AS bit won't be sent as answer and the data transfer operation will be aborted.
If the address received is correct, controller proceeds to send data, if the operation is a write, or a new Chip Address if the it's a read. For each byte sent by the controller, the queried Slave answers with an AS. The same happens, if the roles are reversed, when the Slave sends requested data in a read operation. In this case, for each byte sent by the Slave, the Master will answer with an Acknowledgement Master bit (AM). Read/write operations of single word o in burst mode are available. In the burst mode, data sent or requested are related to a number of memory locations contiguous to the Subaddress specified by the query.
The stop condition is coded giving a low-to-high variation onto SDA pin while the SCL is maintained high. Once this message has been sent onto the bus, each device which wasn't in the listening state, passes to Idle.

Examples of I^{2}C transactions are shown in the next figures, where:

- ◇ S = Start Condition
- ◇ AS = Acknowledgement Slave
- ◇ AM = Acknowledgement Master
- ◇ P = Stop Condition

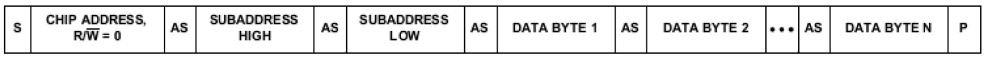


Figure 2.7: I^{2}C single-word Write request

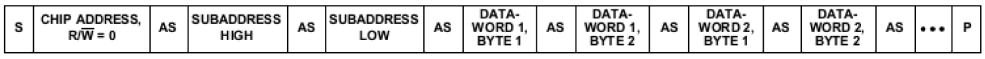


Figure 2.8: I^{2}C burst Write request

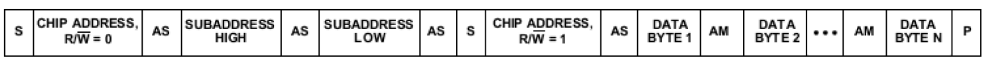


Figure 2.9: I^{2}C single-word Read request

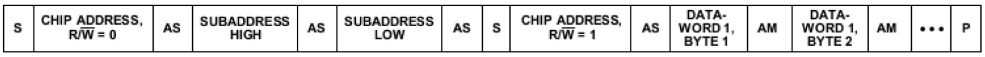


Figure 2.10: I^2C burst Read request

2.3.3 SPI

The ADAU1701 default mode at boot is I^2C. In order to switch to SPI control mode, it's needed to put low 3 times CLATCH/WP pin.
Also in this modality, the device can be used just as a Slave driven by an external controller (Master).
In SPI, control port uses a communication interface with 4 connection wires. These are associated to the pins CLATCH, CCLK, CDATA and COUT that have the following functions:

- ◇ CLATCH. It's an input pin, which is used to establish the start and the end of a transaction. It must be 0 to start and continue a transaction while it must be set to 1 to stop it
- ◇ CCLK. It's an input pin and it carries the main system clock, generated by the external controller
- ◇ CDATA. It's an input pin, which is used to receive requests sent by Master
- ◇ COUT. It's an output pin, which is used to answer to Read queries with data stored into Slave memory locations

Each ADAU1701 is indexed by an unambiguous address (Chip Address), which is assigned just by the ADDR0 pin. For this reason a Master-Slave net in SPI mode, can be formed by just 2 ADAU1701.

Data transfer

Each transaction starts with 3 low values on CLATCH line. After this signal, the controller sends on CDATA the first byte containing the Chip Address (7 bits) and the operation code (R/$\bar{W}$ bit), which is 1 for Reads and 0 for Writes.
At this stage, master sends two bytes with the Slave memory location address (Subaddress) to manage.
If the query is a Write, Master sends data bytes onto CDATA line, while, if the transaction is a parameter read operation, the addressed Slave will answer onto COUT wire with the requested bytes.
Read/Write operations can be referred to single-word or data contained into memory locations contiguous to the Subaddress specified into the query. In this last case the operation is referred as a burst mode transaction.

2.3.4 Self-boot Mode

To power-up the device in Self-boot mode, is necessary that SELFBOOT and WP (Write Protection) pins must be high. WP pin allows o denies the capability to perform writing operations onto external EEPROM, which is connected to the DSP by means of the control port.
During a self-boot, DSP loads a program and a set of parameters, which have been stored previously into the EEPROM, avoiding the necessity of an external microcontroller to pilot the core of the system. The opportunity of a direct communication with the DSP is even now available, exploiting the GPIO communication interface.

At boot, in Self-Boot mode, ADAU1701 will act as Master onto the I^2C port, generating a main system clock (as specified by I^2C protocol, which imposes a duty-cycle of 3/8) equal to 8 times the sampling frequency in use.
When you want to load a new program into the EEPROM, in order to boot the system with that program at the next power-up, the pin WP must be putted low, but it has to be reset high as writing is done, before the system rebooting.

EEPROM messages structure

External Memory is considered as divided into two consecutive pages, where the first one gathers the operations to load into the Program RAM and the second one contains the functional parameters stored previously by a Write-Back operation.
Well-formed instructions, which can be stored into the first page of the EEPROM, must follow the protocol showed in tab.2.4.

Byte 0	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**...**	**Byte n**
Message Type	Following Bytes		Chip Address	Memory Address		data	...	data

Table 2.4: Structure of a message stored into the EEPROM

An example of a writing message of a memory location of 32 bits is shown in tab. 2.5.

Byte 0	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**...**	**Byte 9**
Message Type	Following Bytes		Chip Address	Memory Address		data	...	data
0x01	7		0x00	0x03A2		0x23	...	0xA3

Table 2.5: Example of write message stored into the EEPROM

7 different kinds of allowable operations can be performed at boot. These message types are shown in tab.2.6.

Id	**Type**	**Description**
0x00	End	-
0x01	Write	Write operation
0x02	Delay	Delay setting
0x03	NOP	No operation
0x04	Set Multi WB	Multiple WB activation [Not supported]
0x05	Set falling edge sensitive WB	WB activation from program and not from WB pin
0x06	End and Wait for WB	-

Table 2.6: Accepted message types at boot in Self-boot mode

Write Back operation

It's the operation which allows to write the Interface Registers content, starting from the second page of the EEPROM. This operation allows to save user functional parameters onto the external memory, before the shut-down, giving the capability to recall them at the next device boot.

It's necessary that WP (Write Protect) pin is set low when Write Back operation is performed, otherwise the EEPROM writing request will be denied.
Write Back operation can be performed putting high WB pin, or using the instruction *Set falling edge Sensitive WB*, storing it into the EEPROM, which will enable Write Back operation at next boot.
Just the Interface Registers content will be copied into the EEPROM, so it's necessary that DSP has previously copied parameters to save, from the Parameter RAM to those registers.

2.4 Registers

The Core contains 34 registers of 8, 16, 32 or 40 bits, which are listed in tab. 2.7.

Name	Quantity	Bit	Description
Interface	8	32	Gather parameters data of volume level or equalization used into a program, which are written into the EEPROM when the Write Back operation is called
DSP Core Control	1	16	Register with the main settings of the whole system
GPIO pin settings	1	16	GPIO interface pin settings
Auxiliary ADC	4	16	Gather data generated by Auxiliary ADCs
Safeload Address	5	16	Gather RAM addresses on which, Safeload writing operations will write data contained into Safeload Data registers
Safeload Data	5	40	Gather data to write, in Safeload mode, into RAM locations pointed by Safeload Address registers
Data Capture	2	16	Are used to gather data returned by each step of the flow program execution
Serial Output Control	1	16	Gathers the output serial port settings
Serial Input Control	1	8	Gathers the input serial port settings
MP pin Configuration	2	32	Gather informations about utilization aim of the 12 MP pins
Aux ADC and Power Control	1	16	Gathers information of ADCs and DACs turning-on and turning-off settings
Aux ADC Enable	1	16	Necessary to enable ADCs
Oscillator Power Down	1	16	Allows the management of the system oscillator operation
DAC Setup	1	16	Gathers DACs muting settings

Table 2.7: ADAU1701 Core registers

2.4.1 Structure of register Read/Write requests

Through the control port, it's feasible to read or write any memory locations, registers too. These requests need to be performed according to a specific protocol.
Each data register read/write request packet is composed by

- ◇ 1 byte in order to select the chip (last 7 bits) and specify the requested operation type (MSB of the byte)
- ◇ 2 byte to localize the memory location on which the operation will be performed (the first 6 bits are 0 while the last 11 represent the location address)

◇ n byte containing data to write, whose number varies according to the register to write

Tab. 2.8 shows an example of a request packet directed to the writing of a 16 bits register (2 bytes of data).

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
W/R, chip_adr[6:0]	00000, reg_adr[10:8]	reg_adr[7:0]	data[15:8]	data[7:0]

Table 2.8: 16 bits register writing request packet

2.4.2 Detailed description of main registers

Main features will be shown, taking into account functionalities and bits meaning of the most important ADAU1701 registers.

Core Control register

It's a 2 bytes register, gathering settings of the system and the other registers.

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
RSVD	RSVD	GD1	GD2	RSVD	RSVD	RSVD	AACW
Bit 8	**Bit 9**	**Bit 10**	**Bit 11**	**Bit 12**	**Bit 13**	**Bit 14**	**Bit 15**
GPCW	IFCW	IST	ADM	DAM	CR	SR1	SR0

Table 2.9: Core Control register structure

Most important bits are:

◇ SR[1:0]: Sampling Rate, represents the sampling rate with which the chip will work; 3 sampling frequencies are available: 44.1 kHz/48 kHz, 96 kHz and 192 kHz

◇ CR: Clear Internal Registers, when is 1, it allows signal passing through the Core, otherwise any input won't be precessed

◇ DAM: DAC Mute, when is 1, it disables the default muting option of the system DACs

◇ ADM: ADC Mute, when is 1, it disables the default muting option of the system ADCs

◇ IST: Initiate Sefeload Transfer, when is 1, it enables the Safeload writing and, when operation ends, it's automatically reset to 0

◇ ICFW: Interface Control Port Write Mode, when is 1, allows the Interface Registers writing, by means of the control port, denying DSP to access to Interface registers

Interface registers

In an ADAU1701 there are 8 Interface registers, everyone of 4 bytes. These registers are used to store the parameters state of some program settings, which will be written into the external EEPROM, by the Write Back procedure. In this way is achievable to recall saved parameters, into the EEPROM, at the next DSP power-up.
The parameters saved into these registers are repeatedly refreshed, as a new input sample is processed, with the corresponding parameters stored into the Parameter

RAM, of which they are a copy.
User can also directly write Interface Registers, if the Core Control Register IFCW bit has been set to 1. If the direct writing is enabled, the DSP won't be authorized to access to these registers until IFCW bit remains 1.

Safeload Address/Data registers

Consider the following scenario, taking into account that ADAU1701 can write just one parameter at a time.
Suppose a signal processing using a biquad filter and the need to update all the filter coefficients at real-time. All the coefficients should be update simultaneously, because the possible coexistence of old and new coefficients, doesn't guarantee the filter stability. A filter instability behavior produces unwanted effects capable to last for many processed samples, randomly altering the processed signal. Nevertheless just one parameter can be update at a time. To overcome this limitation, ADAU1701 has a logic dedicated to the Parameter RAM access and 5 Safeload Data registers which will contain data to write into the RAM at the same time.
Safeload mode writing procedure consists in:

1. Write the Safeload Address registers with the Parameter RAM addresses of the parameters which require the update
2. Write the Safeload Data register with the updating parameter values
3. Set Core Control register IST bit to 1

In this way, when the Core Control Register IST bit is high, the Core will provide to copy to Parameter RAM, the content of just the Safeload Data registers which have been update, in order to guarantee the consistency of the memory.
Safeload operations allow 5 parameters management at a time.

DAC Setup register

It's a 2 bytes register, necessary to initialize ADAU1701 DACs. This operation must be performed at the system startup or reboot. It allows just one configuration, that is DACs initialization, setting DS[1:0] bits to 01.

Bit 0	**Bit 1**	**Bit 2**	**Bit 3**	**Bit 4**	**Bit 5**	**Bit 6**	**Bit 7**
DS0	DS1	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Bit 8	**Bit 9**	**Bit 10**	**Bit 11**	**Bit 12**	**Bit 13**	**Bit 14**	**Bit 15**
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Table 2.10: DAC Setup register structure

Aux ADC and Power Down register

It's a 16 bits register necessary for the operation setting of some system components as DACs and ADCs.

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
D3PD	D2PD	D1PD	D0PD	RSVD	VRPD	VBPD	AAPD
Bit 8	**Bit 9**	**Bit 10**	**Bit 11**	**Bit 12**	**Bit 13**	**Bit 14**	**Bit 15**
FIL0	FIL1	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

Table 2.11: Auxiliary ADC and Power Control register structure

Most important bits are:

- ◇ AAPD: ADC Power Down (both the ADCs), when is 1 turns the input ADCs off
- ◇ DxPD: DAC x Power Down, are bits which turn the correspondent DAC x (0, 1, 2, 3) off

Multipurpose Pin Configuration registers

They are 2 registers of 32 bits, necessary to indicate the utilization mode of the GPIO interface 12 MP pins. 4 bits are needed to configure each MP pin, thus 24 bits for each Multipurpose Pin Configuration register. So, the 8 MSBs of each register are reserved.
Tab. 2.12 and 2.13, show register settings, in which each of the 12 MP pin is set by 4 contiguous bits.

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
$MP0_0$	$MP0_1$	$MP0_2$	$MP0_3$	$MP1_0$	$MP1_1$	$MP1_2$	$MP1_3$
Bit 8	**Bit 9**	**Bit 10**	**Bit 11**	**Bit 12**	**Bit 13**	**Bit 14**	**Bit 15**
$MP2_0$	$MP2_1$	$MP2_2$	$MP2_3$	$MP3_0$	$MP3_1$	$MP3_2$	$MP3_3$
Bit 16	**Bit 17**	**Bit 18**	**Bit 19**	**Bit 20**	**Bit 21**	**Bit 22**	**Bit 23**
$MP4_0$	$MP4_1$	$MP4_2$	$MP4_3$	$MP5_0$	$MP5_1$	$MP5_2$	$MP5_3$

Table 2.12: First Multipurpose Pin Configuration register structure

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
$MP6_0$	$MP6_1$	$MP6_2$	$MP6_3$	$MP7_0$	$MP7_1$	$MP7_2$	$MP7_3$
Bit 8	**Bit 9**	**Bit 10**	**Bit 11**	**Bit 12**	**Bit 13**	**Bit 14**	**Bit 15**
$MP8_0$	$MP8_1$	$MP8_2$	$MP8_3$	$MP9_0$	$MP9_1$	$MP9_2$	$MP9_3$
Bit 16	**Bit 17**	**Bit 18**	**Bit 19**	**Bit 20**	**Bit 21**	**Bit 22**	**Bit 23**
$MP10_0$	$MP10_1$	$MP10_2$	$MP10_3$	$MP10_0$	$MP11_1$	$MP11_2$	$MP11_3$

Table 2.13: Second Multipurpose Pin Configuration register structure

Modalities with each MP pin can be used, are shown in tab. 2.14, where the 4 bit setting code has been highlighted.

MPx[3:0]	Setting
1111	Auxiliary ADC input
1100	Serial data port-inverted
1011	Open-collector output-inverted
1010	GPIO output-inverted
1001	GPIO input, no debounce-inverted
1000	GPIO input, debounced-inverted
0100	Serial data port
0011	Open-collector output
0010	GPIO output
0001	GPIO input, no debounce
0000	GPIO input, debounced

Table 2.14: Setting of allowed functionality for each MP pin

Main Multiporpose port utilization categories are:

1. **Auxiliary ADC**
   MP Pins MP2 MP3, MP8 and MP9, can be set, into the Multipurpose Pin Configuration registers, in order to be used as input of analog external signals, through the Multipurpose port. These signals are A/D converted by my means of the 4 Auxiliary ADCs (8 bits resolution), giving to the system the capability to process other 4 analog signals in addiction to the 2 inputs of the main input port.
2. **Serial Data**
   Digital informations, coded according to ADAU1701 specifications, coming from external A/D converters, can be reach the Core by means of MP pins, set as Serial Data into MP configuration registers.
   Otherwise, data have been processed by the Core, can be directly sent, as digital, to Serial Data output port, if Serial Input/Output registers have been set according to the Data Format selected.
3. **GPIO**
   A processing can be controlled (in input) by means of external buttons and rotary encoders or it can monitoring its status, driving LEDs, in order to send messages outside (in output).
   Due to the noises and contact disturbances of switches, buttons and rotary encoders, ADAU1701 provides anti-bouncing circuits associated to MP pins. It's possible to set a MP pin as GPIO debounced or not, changing its configuration into Multipurpose Pin Configuration registers.

2.5 RAM memories

ADAU1701 core is equipped with two RAM memories, one used for parameters and the other one for processing instructions to execute. Parameter RAM has 1024 locations of 32 bits, while the Program RAM is constituted by 1024 locations of 40 bits.
Each memory address is indexable with 11 bits, so 2 bytes having the first 5 MSB equal to 0.
In next sections, main write/read operation modes will be shown and the structures of these packets will be illustrated.

2.5.1 Read and write methods

Instructions RAM is exclusively accessible by means of direct read or write operations of single-word or in burst mode. Burst mode allows to read or write up to 3 instructions stored in contiguous memory locations of the address specified into the request, using just one query.

For Parameter RAM, is possible to perform direct read/write operations of a single-word or in burst mode, as is the case of Program RAM, but it's allowed the capability of perform a write operation in Safeload mode, exploiting Safeload registers, whose operation has been described into the section 2.4.2.

2.5.2 Structure of Read and Write requests

In tab.2.15 and 2.16 are shown the structures of Read/Write requests of a single-word parameter or in burst mode.

Byte 0	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
W/R, chip_adr[6:0]	00000, mem_adr[10:8]	mem_adr[7:0]	param[31:24]	param[23:16]
Byte 5	**Byte 6**			
param[15:8]	param[7:0]			

Table 2.15: Single-word parameter Read/Write packet structure

Byte 0	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
W/R, chip_adr[6:0]	00000, mem_adr[10:8]	mem_adr[7:0]	param1[31:24]	param1[23:16]
Byte 5	**Byte 6**	**Byte 7**	**Byte 8**	**Byte 9**
param1[15:8]	param1[7:0]	param2[31:24]	param2[23:16]	param2[15:8]
Byte 10	**Byte 11**	**Byte 12**	**Byte 13**	**Byte 14**
param2[7:0]	param3[31:24]	param3[23:16]	param3[15:8]	param3[7:0]

Table 2.16: Parameter Read/Write packet structure in burst mode

In tab. 2.17 and 2.18 are shown the structures of Read/Write requests of a single-word instruction or in burst mode.

Byte 0	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
W/R, chip_adr[6:0]	00000, mem_adr[10:8]	mem_adr[7:0]	instr[39:32]	instr[31:24]
Byte 5	**Byte 6**	**Byte 7**		
instr[23:16]	instr[15:8]	instr[7:0]		

Table 2.17: Single-word instruction Read/Write packet structure

Byte 0	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**
W/R, chip_adr[6:0]	00000, mem_adr[10:8]	mem_adr[7:0]	instr1[39:32]	instr1[31:24]
Byte 5	**Byte 6**	**Byte 7**	**Byte 8**	**Byte 9**
instr1[23:16]	instr1[15:8]	instr1[7:0]	instr2[39:32]	instr2[31:24]
Byte 10	**Byte 11**	**Byte 12**	**Byte 13**	**Byte 14**
instr2[23:16]	instr2[15:8]	instr2[7:0]	instr3[39:32]	instr3[31:24]
Byte 15	**Byte 16**	**Byte 17**		
instr3[23:16]	instr3[15:8]	instr3[7:0]		

Table 2.18: Instruction Read/Write packet structure in burst mode

Chapter 3

AS DSP card

AS DSP card has been manufactured and developed by AS. It's used to provide audio solutions for loudspeakers driving and frequency response correction as cross-over networks or equalizers. Some composite loudspeaker modules, have strong designing constraints, for example: small size. In this situation an analog cross-over circuit cannot be an acceptable solution, therefore the utilization of DSPs guarantees to verify the loudspeaker designing constraints, since, exploiting its functionalities, provides a digitalized version of the cross-over network required.
In the next sections will be proposed: the structure analysis of an AS DSP card, the programming interface (Evaluation Card) between the card and PC and finally a brief introduction to the software SigmaStudio, exploited in order to program and configure ADAU1701 DSPs.

3.1 AS DSP card architecture

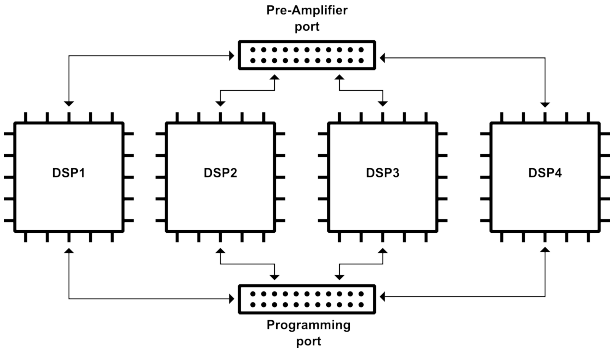


Figure 3.1: AS DSP card

The fig. 3.1 shows, an AS DSP card, which is equipped with 4 processing circuits, an interfacing port with the preamplifier card and a communication port needed to the chips programming.
Each processing circuit is composed by an Analog Device ADAU1701 DSP. The programming, of each of these chips, is achievable by an evaluation system composed by a Chip Control Card and an evaluation board manufactured by Analog Device.

Usually an AS amplifier uses 6-8 input channels and each ADAU1701 allows the simultaneous processing of two signals, therefore an AS DSP card will provide the management of 8 different input signals. Each DSP can deliver 4 output, 2 for each input, therefore an AS DSP card allows 16 different outputs.
Each ADAU1701 works in Self-boot mode. In this mode, the DSP uses its own clock system and it's interfaced with an external EEPROM memory, which is timed by the chip clock. EEPROM communicates to DSP through its control port, using the I^2C protocol.
The external memory will contain the desired processing program, which will be loaded and executed by the chip as the AS amplifier is turned on.

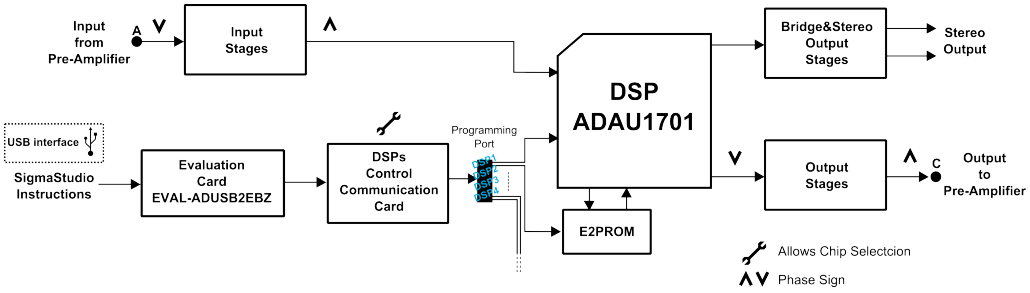


Figure 3.2: Block diagram of a single processing circuit within an AS DPS card

Fig. 3.2 shows the block diagram of one of the 4 AS DSP card processing circuits. It also depicted the chips programming system interface with SigmaStudio software through USB port.
Signal outgoing from preamplifier channel, flows into a stage input, in which it's high-cut filtered and phase reversed. Through the analog chip input, the signal is processed according to the processing program loaded into the DSP from the EEPROM, at the system boot.
Once the processing has been done, AS DSP cards provides 2 different kinds of output:

1. A stereo output directly connected to the AS amplifier output, without the ICE-Power final amplification. In this case, the stage *Bridge&Stereo* delivers an amplification, an high-cut filtering and a stereo-construction of the signal
2. A basic output, which returns the signal to the preamplifier in order to send the processed signal to the ICEPower final amplifiers. The necessity to return the signal to the preamplifier, before the final stage amplification, is due to the need of ICEPower modules (BTL or SE) to have inputs balanced (BTL) or stereo combined with another signal channel (SE).

Output stage is necessary to phase reversing the signal, before returning it to the preamplifier, through the C node. All the returning outputs to the preamplifier, are gathered into the input/output communication port referred as *Pre-Amplifier Port* in fig.3.1
Programming port considers a bidirectional communication with each of the ADAU1701 chips and EEPROMs.

3.2 AS DSP card interfacing system and programming

Interfacing system between an AS DSP card and the programming chip software is shown in fig. 3.3. It consists in 2 cards:

- ◇ Control/Selection Card, in order to select the desired DSP of the AS DSP card
- ◇ Evaluation Card manufactured by Analog Device, having a USB port in order to interface a PC

Control/Selection Card hes been been built through an esy procedure depicted in next section, and it allows the selection of one of the 4 ADAU1701, to which Analog Device evaluation board will communicate.

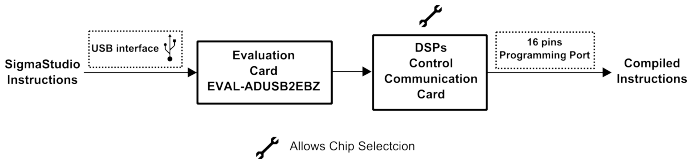


Figure 3.3: Block diagram of an AS DPS card programming system

3.2.1 Control Card for DSP selection

In fig. 3.4 is shown a representation of the board for the AS DSP card chip selection. It consists of 2 communication ports and 2 groups of switches. Communication ports are necessary to interface the selected chip to program and the Analog device evaluation board.

Selection groups allow the configuration of communication procedure with the chip

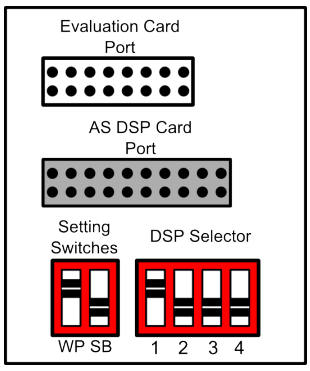


Figure 3.4: Scheda di controllo per la selezione del DSP

and the selection of one of the 4 DSPs on board of the AS DSP card. In particular, the Setting Switches group allows to select the communication mode enabling or disabling the write protection of the EEPROM though the switch WP (Write Protection)[1]. Obviously the switches group DSP Selector allows the selection of the chip to program. For example, the configuration of fig. 3.4, says that the writing of chip 1 EEPROM is

[1]Note that the logical values of these switches are inverted in respect to the ADAU1701 WP and SB (Self-boot mode) pins specification [15]

enabled, because the WP is set high (reversed in respect to DSP specifications) and the DSP Selector has the switch number 1 set to high.

The Control board has been realized by means of using a PCB (Printed Circuit Board). Steps of the tracks printing onto the base are shown in fig. 3.5.

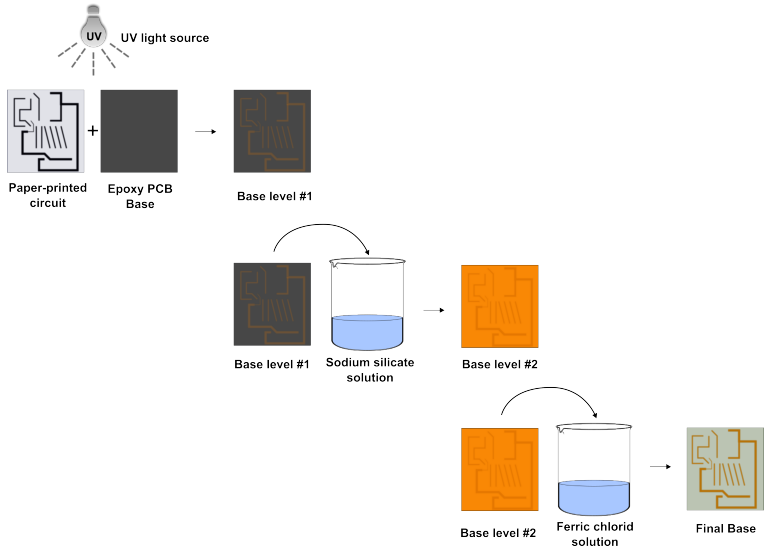


Figure 3.5: Procedure of the Control Card circuit printing

The tools needed for card realization are:

1. switches and communication ports
2. circuit tracks printed onto contact paper
3. a PCB base protected by an epoxy surface
4. an UV light exposer
5. a Disodium metasilicate solution
6. a Ferric Chloride solution

By means of a circuit drawing software, the desired circuit is printed onto a contact paper sheet. Applying this print onto the PCB and exposing under an UV light, epoxy reacts in order to preserve the circuit drawing onto its surface. Immersing the impressed PCB into the Disodium metasilicate solution, the unimpressed epoxy is removed, uncovering the underlying copper surface. Now, the Ferric Chloride solution is used to remove the copper surface except the copper tracks preserved by epoxy, which is also removed at the end of this last procedure. At the end of this last step, the desired circuit tracks will be printed onto the PCB base. The next step is to drill the base to apply switches and communication ports and proceed to their welding.

3.2.2 Evaluation board Analog Device

The evaluation card EVAL-ADUSB2EBZ (in SigmaStudio referred as USBi), implements a communication conversion between USB and I^2C or SPI protocols. It allows the interfacing among the Analog Device SigmaStudio software and a lot of the Analog Device chips [16], permitting to simultaneously control up to 5 slave devices.

EVAL-ADUSB2EBZ is an ideal solution for code downloading and register setting of a SigmaDSP [16] chip, exploiting a mini-USB connection with a PC. Fig. 3.6 shows

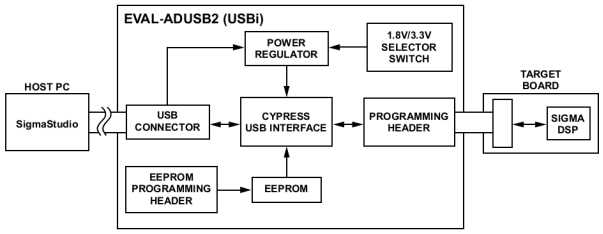


Figure 3.6: Blocks diagram of an evaluation board EVAL-ADUSB2EBZ

the structure of an evaluation board used in this work.
USBi is a standalone communication interface which translates USB control commands coming from SigmaStudio, toward SigmaDSP chips according to I^2C o SPI protocols. The device is directly supplied by USB connection, indeed, as shown in fig. 3.6, the voltage regulator allows the conversion between the 5V USB supply to 3.3V or 1.8V according to voltage mode of the system to program. A selection between these two voltage operation values is achievable through an on-board selector.
Key components of USBi are:

1. **Internal E2PROM**
   Includes the firmware loaded into the Cypress USB at device booting. This firmware represent the instructions set, needed by the system in order to perform the conversion between USB and I^2C or SPI protocols. This firmware is stored into the internal EEPROM during the manufacturing of the evaluation card.
2. **Cypress USB interface**
   It's the EVAL-ADUSB2EBZ core. It's a micro-controller which performs the protocol conversion, acting as stack FIFO (First In First Out) between PC and the device under programming.
   This interface has its own clock system, generated by an oscillating circuit and a piezoelectric crystal mounted onto the device.
3. **"Programming Header" block**
   Allows the right micro-contreller Cypress USB booting from the E2PROM, removing any devices from bus I^2C, during this step. This isolation status ends as booting is complete.

USBi usage is possible after an Analog Device drivers installation.

3.3 Sigma Studio: chip programming

SigmaStudio is a graphical IDE used for the programming, software development and setting of SigmaDSPs. Processing audio blocks can be connected into elaboration scheme in a graphical way, and the program compiler will provide to the generation of the DSP operation code, which corresponds to the designed elaboration flow. It's allowable also the codification of the desired chip registers settings.The IDE gives to user without any machine-code programming, the capability to easily program a SigmaDSP with their own projects [17].
SigmaStudio includes an extended algorithms library for the audio processing, with

integrated tools to perform filtering, mixing and dynamical processing [17]. The software will be briefly depicted in the next sections.

3.3.1 A new SigmaStudio project

Once the creation of a new project has been requested, the SigmaStudion screen is shown in fig. 3.7. Main software sections have been highlighted in fig. 3.7 and

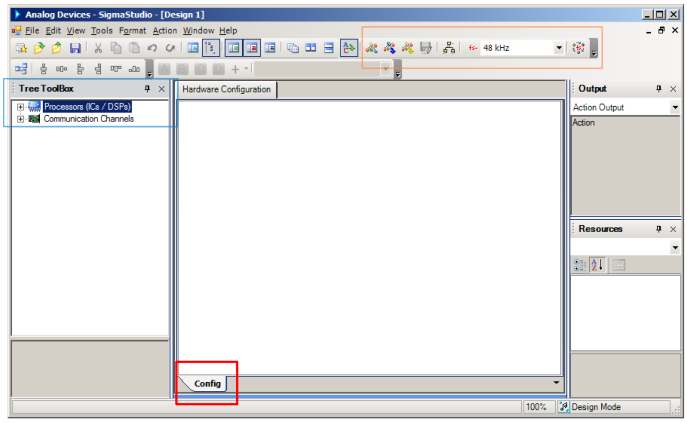


Figure 3.7: Initial screen for a new SigmaStudio project

described below.

- ◇ **Compilation, download and frequency rate selection bar (orange)**
  Through this tool is possible to compile and write a project onto the SigmaDSP in use, changing the frequency rate of the system.
- ◇ **"Tool TreeBox" (cyan)**
  This section gathers tools needed to the system composition (as evaluation board, SigmaDSPs or EEPROM memories) or all the algorithms for modeling the needed processing flow.
- ◇ **System Hardware configuration board (red)**
  It's the board where to place the blocks representing the real system virtualization. In the case of an AS DPS card, it will be need to place onto the "Config" board, the virtual devices corresponding to the real ones. Therefore it will be needed an evaluation board USBi, a chip ADAU1701 and an EEPROM memory. All these block are available, just dragging them from the "Tool TreeBox' section to the board.

3.3.2 USBi interface, chip and E2PROM memory

Once the system virtualization has been done, the screen of the software is shown in fig. 3.8, where are highlighted the following sections:

- ◇ **"Capture" window (green)**
  It's a viewing tool about all the writing/reading operations performed by each devices into the virtual system. Each writing operations performed onto the chip or the EEPROM, is shown in this window, listing the memory location address, data and the time duration of the operation.

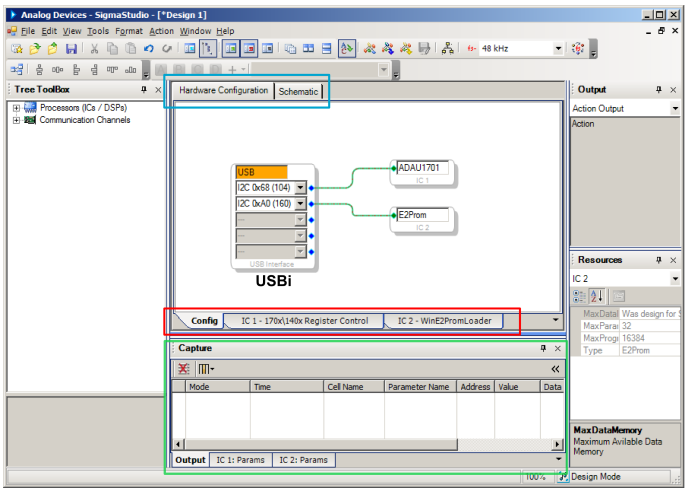


Figure 3.8: System composition in SigmaStudio

- ◇ **Processing flow designing board (cyan)**
  Once a SigmaDSP has been dragged onto the configuration board ("Config"), the software enables the internal chip programming, introducing a panel "Schematic", where user can write its own processing flow exploiting the available algorithms gathered into the tool section "Tool TreeBox".
- ◇ **Integrated circuits (DSP and E2PROM) hardware management boards (red)**
  Once an integrated device has been placed into the virtualized system, software proceeds to open a panel in order to manage all the registers of the device.
  For example, in the case of a DSP AS card, which uses an ADAU1701 and an EEPROM, SigmaStudio will allow the chip registers management and the EEPROM configuration. Fig. 3.9 and 3.10 show the hardware Configuration panel content of the chip and the external memory.

The EEPROM hardware management panel, shown in fig. 3.10, allows internal settings, as page dimension of the device, and gives the capabilities to visualize the memory content, saving it onto an external file and the direct memory writing from an external source.

3.3.3 Processing program design

SigmaStudio allows the management of a SigmaDSP program, by means of the panel "Schemtaic", which is selectable in main board, only if a SigmaDSP block has been placed into the "Config" section.
In fig. 3.11, is shown a simple processing flow for an ADAU1701 chip. This program is just an association between analog inputs and outputs.

3.3.4 Self-boot Mode

Once a project is complete, user proceeds to the compilation of the program and to download it onto the chip RAM memories. AS DSP card provides the Self-boot mode operation of its chips. Therefore a processing flow must be written into the EEPROMs

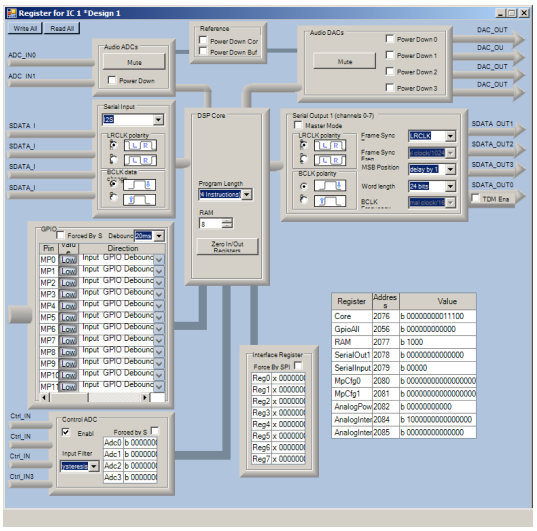


Figure 3.9: Chip ADAU1701 Hardware configuration

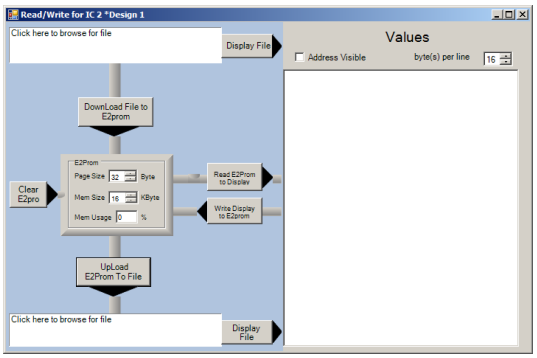


Figure 3.10: E2PROM Hardware configuration

of the AS DSP cards in order to be executed at amplifier power-up. SigmaStudio allows the memory writing as shown in fig. 3.12.
If the Selection Card is allowing the memory writing (WP switch must be high), the designed program can be stored into the EEPROM.

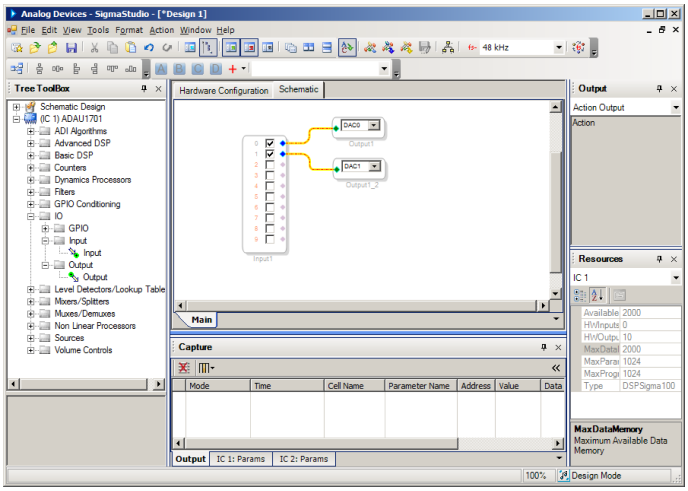


Figure 3.11: Composition of a simple processing program

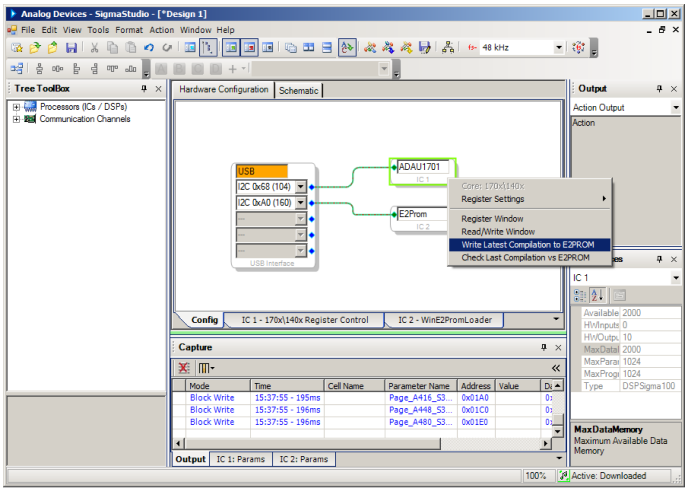


Figure 3.12: E2PROM program storing

Part II

AS amplifiers optimization

Chapter 4

Input stage optimization

In this chapter will be illustrated:
- ◇ limitations of AS amplifiers input section
- ◇ an electronic and DSP-based optimization
- ◇ results about tests performed

4.1 Preamplifier card considerations

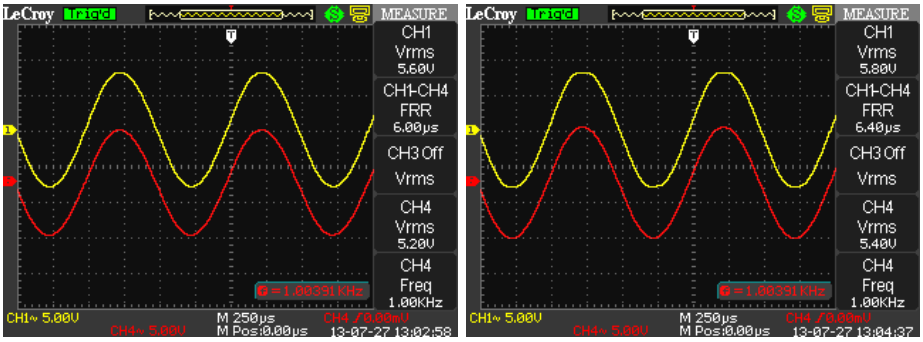
AS preamplifier cards have been designed to accomplish the following purposes:
- ◇ to interface different kinds of input signal (balanced and unbalanced)
- ◇ to be able to be extended from an input channels number point of view
- ◇ to interface an external processing module (AS DSP card)
- ◇ to correctly combine and transform the output in order to feed the final power amplifiers according to their input specifications

An AS amplifier achieves high output powers exploiting the roles of the final power amplification stage, while preamplifier boards work essentially as buffers (almost unitary gain).

The performances of AS preamplifier cards have been depicted in section 1.4.2. Taking into account AS amplifiers without DSP on board, the following consideration about input dynamic range can be stated.

Operational chips, That2181 VCAs included, mounted onto preamplifier cards, saturate for system input signal of about 5.20 Vrms (Volt root mean square). This saturation produces signal clipping, causing a harmonic distortion which nullify high fidelities properties of AS amplifier systems.

Fig. 4.1(a) shows the input signal limit threshold below the VCA clipping, while fig. 4.1(b) depicts the effect of harmonic distortion for sinusoidal signal tests with frequency of 1kHz. The input signal is represented by the red colored wave form, while output is the yellow signal. Furthermore, pictures show the buffer behavior of an AS preamplifier card, indeed the output value is almost equal the input one.



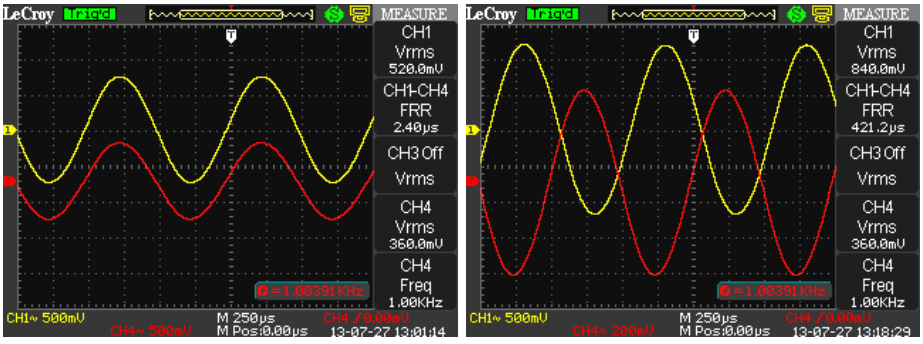
(a) (b)

Figure 4.1: Dynamic range of an AS preamplifier without DSP board, before (a) and after (b) output clipping

Under these conditions, an AS preamplifier card, without DSP, can drive, avoiding clipping distortions, high input signals outgoing from lots of devices[1], like mixers which have maximum output voltage of 5 Vrms or CD players, having 2 V of peak output voltages.

4.1.1 Input dynamic limitation

When an AS DSP card is plugged into preamplifier board, the situation of input dynamic range drastically changes. Employing of DSP gives an extra amplification, of about 4 dB, of input signals, decreasing significantly the clipping threshold of VCAs.



(a) (b)

Figure 4.2: AS preamplifier card gain voltage without (a) and with (b) DSP on board

Fig. 4.2(a) and fig. 4.2(b) show the effect of AS DSP card introduction on preamplifier gain. For inputs (red signal) of 0.36 Vrms, preamplifier without DSP output (yellow wave form) is almost 0.52 Vrms, while that of DSP-equipped system is 0.84 Vrms.

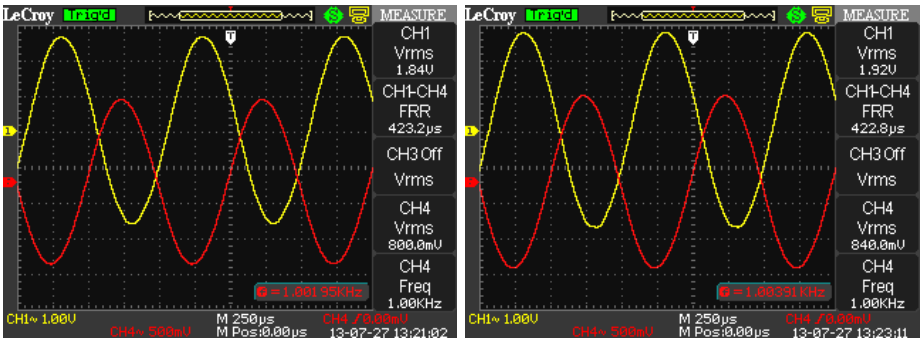
[1]Note that input ICEPower specifications, like maximum input voltage of ± 3.3 V_p (volt of peak), must be verified, thus preamplifier outputs of 5.00 Vrms cannot be acceptable.

The gain increasing is:

$$G_{\text{extra}} = 20log_{10}\left(\frac{0.84}{0.52}\right) = 4.16dB \tag{4.1}$$

Fig. 4.2(b) shows also another effect of DSP plugging: preamplifier output is subject to a phase shift due to DSP operation. Nevertheless this delay is about 0.40 ms, thus undetectable by human auditive system.

Additional 4 dB gain introduced by DSP on board of the preamplifier card, changes drastically the input dynamic range of the AS preamplifier boards. Fig. 4.3(a) shows the input threshold before the clipping while fig. 4.3(b) depicts the effect of VCA clipping (inputs in red and output in yellow).



(a) (b)

Figure 4.3: Dynamic range of an AS preamplifier with DSP board, before (a) and after (b) output clipping

Threshold of input signals in order to avoid VCA clipping, decreases to 0.80 Vrms, thus about 1.13 V of peak.
The input dynamic range of an AS DSP-equipped preamplifier board decreases to 0.80 Vrms from 5 Vrms of the configuration without DSP.

In this situation an AS amplifier with DSP cannot be driven by neither:

1. CD players
2. Mixer devices

4.1.2 Further development considerations

AS preamplifier boards without DSP act as buffer also in order to guarantee an acceptable high input dynamic. When DSPs are plugged into preamplifier boards, this buffer behavior doesn't change a lot.
Under this condition, pre-amplification of low input signals (e.g. voltage values of 0.5V) keeps output signals low. In these cases preamplifier feeds ICEPower modules with signals having not optimal voltage values and the resulting total amplification is poor with wasting power.

As result, when devices like MP3 players, iPods and smart-phones which give output signals with maximum peaks of ±0.5 V, i.e. 0.36 Vrms, are used to drive an AS amplifier, an inadequate amplification is provided.
Furthermore, under this condition, an AS amplifier will amplify different devices with different perceptive gains according to the different output voltages of the device which is plugged into the system.

4.2 Proposed solution

Most widespread audio players belong to one of the following three audio devices families. Criterion of this classification is based on output voltage value of the device. Families are:

1. **Portable devices**, like MP3 players, smart-phones and iPods, which have maximum output ranges of 0.5 V_p or 0.36 Vrms
2. **CD Players** having maximum output ranges of 2.0 V_p or 1.44 Vrms
3. **Mixers** which commonly have maximum output ranges of 5 Vrms[2]

An AS amplifier must be able to be driven by any of the audio player devices belonging to the three families avoiding clipping distortion. The preamplifier development proposed for this work, must accomplish the following aims:

1. detect the family which any device plugged into the system, belongs to
2. modify VCA gain voltage level in order to attenuate input signal which should clip (like CD players or Mixer outputs) or boost input signals which belong to Portable device family
3. provide a *maximum preamplifier output voltage* (V_{MNO}) normalized up to a fixed common level for each device plugged into the the system

Normalized maximum output voltage V_{MNO} of preamplifier board is fixed to a value of 1.84 Vrms, which is the output voltage value achieved when an input voltage of 0.80 Vrms (equal to input voltage limit under clipping threshold) is fed to the system.

The VCA gain voltage alteration is performed by adding or subtracting an *additional gain control* (AGC). This gain control is a fixed voltage value built in 3 instances, one for each devices families taken into account. Each AGC is found putting in input the maximum output voltage value, of each devices family, and boost or attenuate the gain control until the V_{MNO} is reached.

- ◇ AGC_{mp3} is selected using a system input of 0.36 Vrms and boosting the VCA gain, up to reach a preamplifier output of 1.84 Vrms
- ◇ AGC_{CD} is selected using a system input of 1.44 Vrms and attenuating the VCA gain, up to reach a preamplifier output of 1.84 Vrms
- ◇ AGC_{MXR} is selected using a system input of 5.00 Vrms and attenuating the VCA gain, up to reach a preamplifier output of 1.84 Vrms

The development proposed must allow the recognition of which devices family, the plugged-in device, belongs to and select the adequate AGC_* in order to regulate accordingly the preamplifier output.

[2]Not all mixer devices available for sale fall within the 5 Vrms maximum output ranges, but there are many devices which exceed this voltage level, in many cases above 7-8 Vrms

4.3 Implementation

As shown in fig. 1.27, in which has been detailed the structure of an AS preamplifier board, the input signal routing within the card denies a pure software-based solution to implement the proposed solution. Indeed, it's easy to see that the pre-amplification, performed by VCA chips, occurs before the DSP processing. This means that every anti-clipping solutions at expense of just ADAU1701 are completely useless, because an input signal should clip before it is processed by the DSP.
Thus a hardware integration on the preamplifier board is mandatory.

4.3.1 Hardware development

Fig. 4.4 shows the implemented hardware development in order to fit the proposed solution requirements.

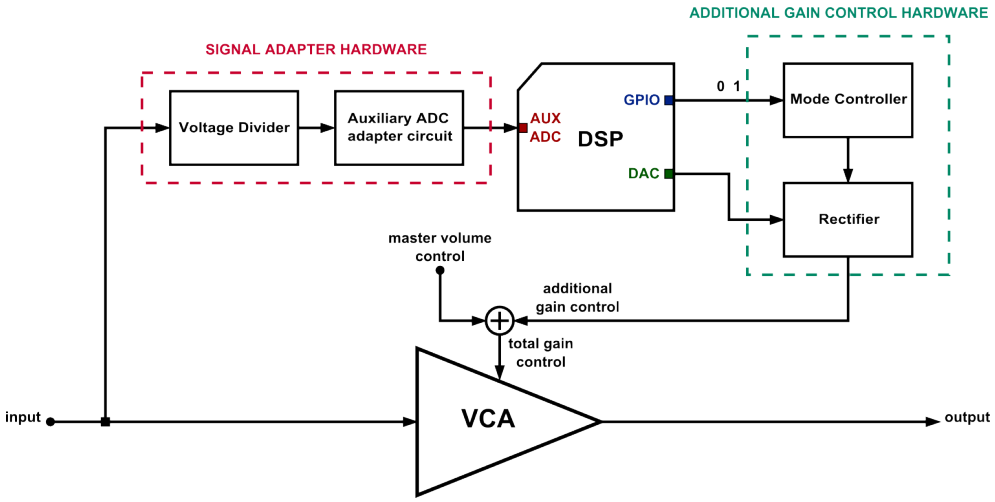


Figure 4.4: Hardware blocks scheme of proposed solution

The performed improvements can be summarized as follows:

1. Fetching of VCA input signal, before the VCA amplification, in order to use it as *input control signal*.
2. Using the *input control signal* as input of one of the 4 AUX ADC of the DSP, in order to detect the voltage level of the input signal before the amplification and find out which devices family the source belongs to.
   Due to the AUX ADC input requirements, shown in the datasheet of the the chip, it has been necessary include an additional hardware to match them. In particular, a voltage divider is essential in order to reduce the input signal voltage, which should be much high to be fed directly into the AUX ADC input port.
3. Generating an additional gain control signal that exploits a DAC of the ADAU1701. VCA gain requires a DC voltage signal while the DSP DAC output can be only an AC voltage signal. So a rectifier hardware is necessary and this hardware must provide a double DC output one positive and one negative, in order to allow an attenuation or a boost to the VCA control level. Furthermore the selection of only one of the DC rectifier output must be performed. To do this a logic output from

a GPIO output port of DSP is used. This logic signal drives an other additional switch hardware able to chose only one rectifier output.

4. Adding the DC additional control gain (AGC) to the master volume control gain, in order to regulate the total VCA control gain according to the output maximum voltage requirement (V_{MNO}).

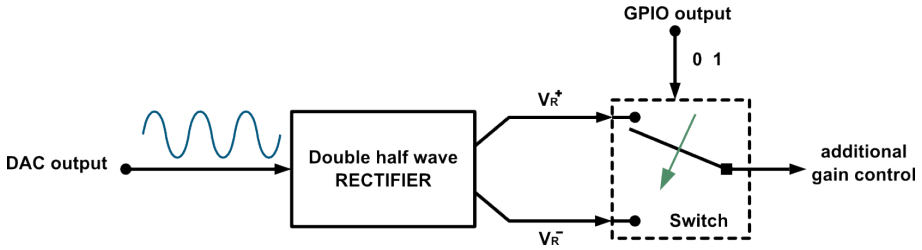


Figure 4.5: Additional gain control hardware scheme

A detailed description of the operating principle of the *Additional control hardware* is depicted in fig. 4.5. A sinusoid output coming from DSP DAC is fed into the rectifier which produces two amplified and rectified copies of the input sinusoid one negative V_R^- and one positive V_R^+. The positive signal yields an attenuation of the VCA total gain while the V_R^- produces a boost.
The *Additional control hardware* gives just one output signal, choosing one of the two V_R^+ and V_R^-. This selection is performed by a switch chip which shortcuts its exit pin with the positive V_R^+ pin output or the negative one, according to the GPIO output it gets. If GPIO output is 0 (0 is logical value which corresponds to 0V) the switch shortcuts exit pin with V_R^+ and the additional gain control will produce an attenuation of VCA total gain, while if GPIO output is 1 (1 is logical value which corresponds to 3.3V) the switch shortcuts exit pin with V_R^- and the additional control gain will produce a boosting of VCA total gain.

4.3.2 Software development

Provided software implementation has started from a *static gain controller* Sigma Studio patch. Fig. 4.6 shows a block scheme of the patch.
As one can see, the structure of the whole software solution is composed of two main parts:

- ◇ a "channel association" part (enclosed into the green dashed box)
- ◇ a "control" part (enclosed into the blue dashed box)

"Channel association" performs the simple signal path establishment within the DSP. This part allows the input/output association from the 24 bits ADC input port to a DAC output port.
"Control part" represents the core of the software. It is composed by:

- ◇ a static selection input of 3 different numeric states
- ◇ a gain table containing additional gain attenuation/boost values
- ◇ a mode table containing the logic selector values for the switch chip of the additional gain control hardware
- ◇ an oscillator with a frequency of 10kHz which is used to produce the AC version of the additional gain control signal, multiplied by the gain value selected from the gain table

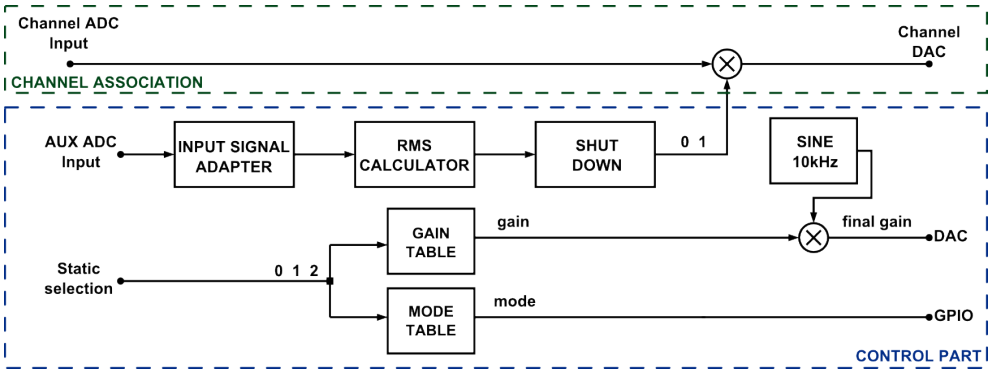


Figure 4.6: Software block scheme of a static gain controller

The static selection values and their relationships with the gain and mode tables factors, are depicted in tab. 4.1.

Static Selection	Gain factor	Mode
0	g_{mp3}	1 (boosting)
1	g_{CD}	0 (attenuation)
2	g_{mxr}	0 (attenuation)

Table 4.1: Gain and mode tables content association with static selection indexes

The control input signal, for this static software solution, is used only for a shutdown operation if an input signal greeter than 5.00 Vrms is fed into the system. Signal above 5.00 Vrsm should clip because the attenuation capabilities of the rectifier hardware are unable to avoid clip artifacts for this kind of signal.
Input control signal is managed by an adaption block which corrects the mean of signal, since the AUX ADC requirement constrains its input to have a DC component that confers it a non-zero mean. This mean correction is necessary to allow a correct calculation of control input RMS value. This RMS value is used to check if the shutdown condition occurs. The shutdown block gives a gain factor which multiplies the channel input signal, in order to produce a normal channel DAC output if shutdown condition doesn't occur or a zero channel output if it does.

This static implementation achieves just two of the three aims proposed:

1. modify VCA gain level voltage in order to attenuate or boost the input signal
2. provide a normalized preamplifier output voltage fixed up to a max value of 1.84 Vrms

An input devices family detection must be provided.

Starting from this static software implementation, the all proposed solution aims are fitted developing a dynamic gain selector version of the static patch. Fig. 4.7 shows the block scheme of the final software implementation, while fig. 4.8 depicts the Sigma Studio implementation of the dynamic solution.
"Channel association" part (highlighted by the green dashed box) is exactly the same of the static implementation. Also the functionalities of the shutdown, oscillator, RMS

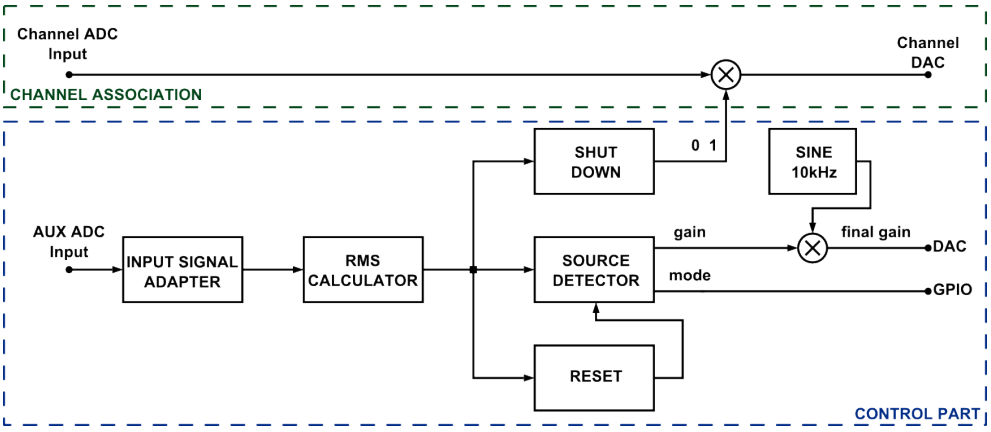


Figure 4.7: Software block scheme of a dynamic gain selector

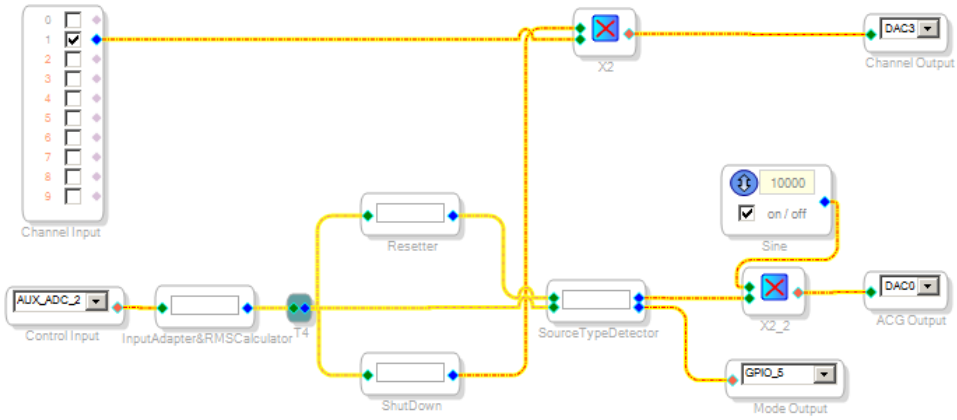


Figure 4.8: sigma Studio patch of a dynamic gain selector

calculator and input adapting boxes are the same of the previous static case.

The introduction of the source detector block yields a dynamic recognition of the devices family which input device belongs to. This software block, operates in a toggle-sense, for this reason a reset block is necessary, in order to reset the detector. Fig. 4.9 depicts in detail the operating principle of the block and fig. 4.10 the Sigma Studio implementation.

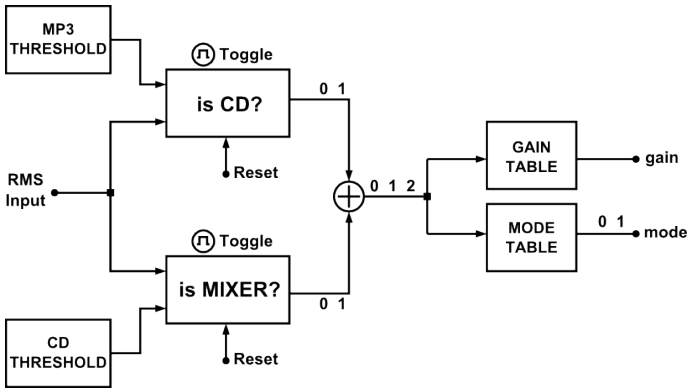


Figure 4.9: Detailed scheme of "Source Detector" block

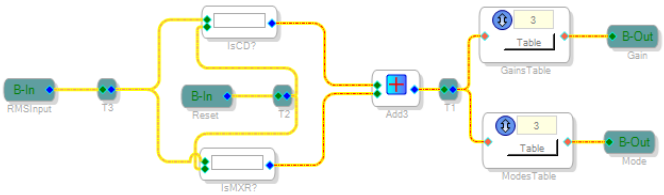


Figure 4.10: Sigma Studio patch of "Source Detector" block

Once the RMS value of control input signal has been computed, this quantity is compared with two threshold values (quantity coded into full-scale domain) by two logic toggle selectors: "isCD?" and "isMIXER?" blocks. Each of this blocks returns 1 if the RMS input is higher of a threshold or 0 if it isn't. The detection is performed in a toggle-sense, this means that once the threshold is exceeded the detector response rests high until a reset condition occurs. The detectors outputs are summed in order to produce 3 indexes values 0, 1 and 2 needed to access the gain and mode tables in order to extract the accordingly gain value and mode bit.
Reset condition occurs when RMS input value is 0, that means no input signal is fed into the system.
Fig. 4.11 shows the Sigma Studio implementation of "isCD?". The "isMIXER?" block has exactly the same structure of "isCD?" block but with a different threshold value.

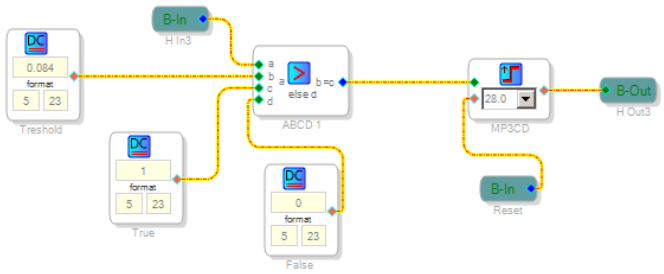


Figure 4.11: Sigma Studio patch of "IsCD?" block

The working principle of the patch can be summarized as follows:

- ◇ the initial state, which coincides with the state after reset condition, make the patch operating as if a Portable device is plugged into the system, so gain output is g_{mp3} and mode logic output is 1
- ◇ when RMS control input exceeds $MP3\_threshold$ the gain output rests fixed to g_{CD} value and the mode logic bit is 0, until a reset condition or a $CD\_threshold$ passing occurs
- ◇ when RMS control input exceeds $CD\_threshold$ the gain output rests fixed to g_{mxr} value and the mode logic bit is 0, until a reset condition occurs
- ◇ when RMS control input exceeds the shutdown threshold the gain output rests fixed to g_{mxr} value and the mode logic bit is 0, until a reset condition occurs, but the channel DAC output is brought to 0 with a time-by-time shutdown detection

All the software threshold values are coded into full-scale amounts, the same happens for gain factors needed to attenuate or boost processed signals. So measurements, made with tests bench, have been performed in order to get a relationship between signal (Vrms domain) and chip full-scale (SigmaStudio) quantities. Results are shown in tab 4.2

Description	**System input (Vrms)**	**SigmaStudio input RMS (full-scale)**	**SigmaStudio gain (full-scale)**	**SigmaStudio mode (logic)**	**Preamplifier output (Vrms)**
Reset condition	0.008 [3]	0.034	0.5 (g_{mp3})	1 (boost)	0
CD threshold	0.36	0.084	0.32 (g_{CD})	0 (attenuate)	1.8
Mixer threshold	1.44	0.3	1.2 (g_{mxr})	0 (attenuate)	1.84
Shutdown condition	5.04	0.96	1.2 (g_{mxr})	0 (attenuate)	0

Table 4.2: Measured relationships between full-scale and Vrms values

From tab. 4.2 is possible to extract the gain factor values, coded in full-scale notation, used to fill up the gain table of the software patch. The procedure used in order to discover these values is briefly summarized as follows:

1. feed the system with an input signal equal to the max voltage output of device family under test (0.36 Vrms for Portables, 1.44 Vrms for CD players and 5.00 for Mixers)
2. change mode factor according if a boosting or an attenuation is necessary
3. change the gain factor until a preamplifier output of 1.84 Vrms is reached
4. repeat this procedure for the max voltage output of each devices family

4.4 Test and results

The implemented solution has been tested in order to evaluate its performances. The following sections depict how the tests have been performed, the obtained results and a discussion about them.

[3]Note that reset condition does not exactly correspond to 0 Vrms, this is due to noise disturbance which affects the AUX ADC input.

4.4.1 Evaluation tests

Two types of tests have been performed. The first one is a *quantitative* evaluation, carried out using a sinusoidal input signal test and varying its amplitude in order to measure the preamplifier output responses. The second type of test is a *qualitative* evaluation, performed using song tracks played by more audio devices in order to verify the system development operation for real employment situations.

Quantitative test

In order to perform the quantitative test, the following tools have been employed:

- ◇ **Waveform generator**: Protek, Audio Generator B850
- ◇ **Oscilloscope**: Teledyne LeCroy, WaveAce 234

The waveform generator produce a sinusoid input test with 1kHz frequency. This signal is used to feed the developed AS amplifier. The oscilloscope is exploited to measure and visualize the input signal test and the preamplifier output.
Measurements are repeated changing the input test amplitude of about 0.2 Vrms at time. Starting from 0 Vrms input test signal and increasing it of 0.2 Vrms, measurements end when a signal test of 5.00 Vrms is fed into the system.

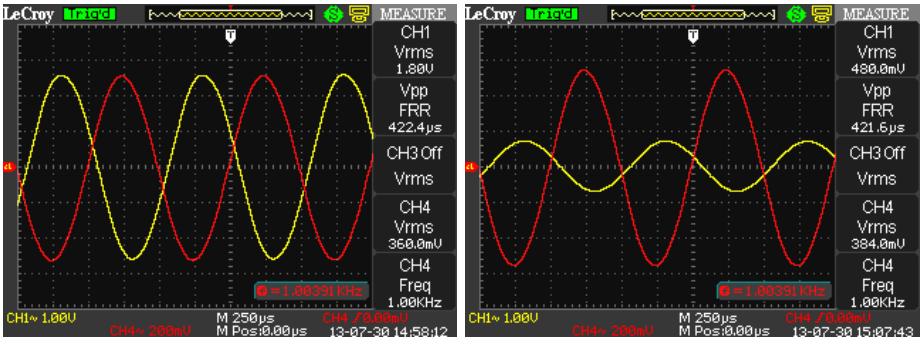
Tab. 4.3 depicts the obtained results highlighting:

- ◇ input and output Vrms measurements
- ◇ RMS value of the input as SigmaStudio codes and computes it
- ◇ gain and mode factors in full-scale domain
- ◇ delay between the input test sinusoid and the preamplifier output waveform

System input (Vrms)	SigmaStudio input RMS (full-scale)	SigmaStudio gain (full-scale)	SigmaStudio mode (logic)	Preamplifier output (Vrms)	Delay Input/Output (μs)
0.008	0.034	0.5	1	0.008	0.0
0.2	0.046	0.5	1	1.0	419.2
0.36	0.084	0.5	1	1.8	422.4
0.6	0.123	0.32	0	0.76	423.6
0.8	0.157	0.32	0	1.00	420.6
1.0	0.196	0.32	0	1.24	421.6
1.2	0.235	0.32	0	1.52	422.0
1.44	0.285	0.32	0	1.84	421.2
1.6	0.314	1.2	0	0.56	421.6
1.8	0.358	1.2	0	0.64	426.5
2.0	0.393	1.2	0	0.72	418.2
2.2	0.436	1.2	0	0.80	420.8
2.4	0.475	1.2	0	0.88	420.0
2.6	0.515	1.2	0	0.96	418.8
2.8	0.554	1.2	0	1.04	421.2
3.0	0.567	1.2	0	1.08	417.6
3.2	0.604	1.2	0	1.16	418.0
3.4	0.646	1.2	0	1.24	416.8
3.6	0.688	1.2	0	1.32	417.2
3.8	0.728	1.2	0	1.40	418.0
4.0	0.760	1.2	0	1.44	417.6
4.2	0.794	1.2	0	1.52	418.5
4.4	0.833	1.2	0	1.6	418.4
4.6	0.887	1.2	0	1.64	417.5
4.8	0.909	1.2	0	1.72	418.6
5.04	0.948	1.2	0	1.8	417.9

Table 4.3: System test results for 1 kHz sine input signal

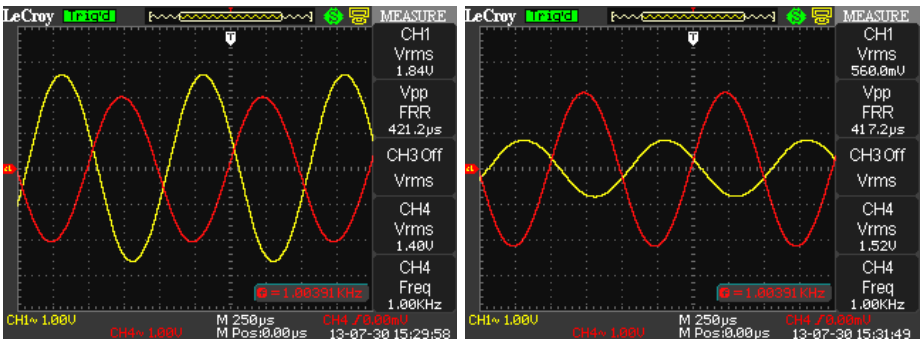
In order to emphasize performances of the implemented preamplifier development, snapshots of the commutation states have been taken. In all the figures the red waveform represents the system input test signal while the yellow one is the preamplifier output.



(a) (b)

Figure 4.12: Gain amplification switching from Mp3 (a) to CD (b)

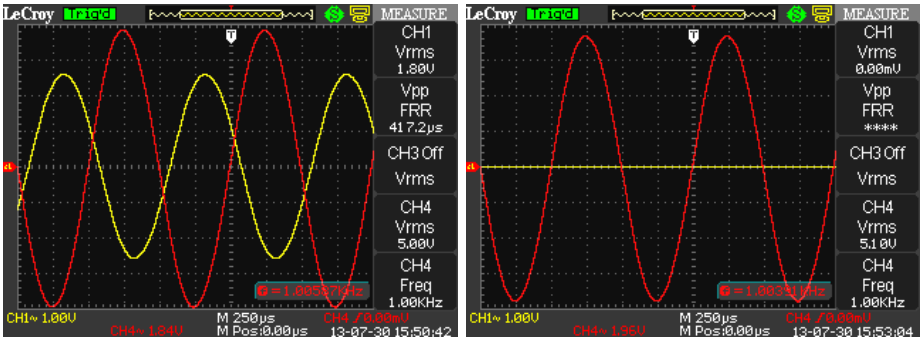
Fig.4.12 shows the amplification gain commutation from the situation in which input test signal is detected as an MP3 signal 4.12(a) to its detection as a CD signal 4.12(b), due to the $MP3\_threshold$ exceeding.



(a) (b)

Figure 4.13: Gain amplification switching from CD (a) to Mixer (b)

Fig.4.13 shows the amplification gain commutation from the situation in which input test signal is detected as a CD signal 4.13(a) to its detection as a Mixer signal 4.13(b), due to the $CD\_threshold$ exceeding.



(a) (b)

Figure 4.14: Amplification before (a) and after (b) output shutdown

Fig.4.14 shows the commutation from the situation in which input test signal is detected as a Mixer signal 4.13(a) to the output shutdown state 4.13(b), due to the *Shutdown_threshold* exceeding.

Qualitative test

This test has been performed playing 5 song tracks using each of the following audio sources:

- ◇ **Mp3 player**: Apple, iPod Nano 5g
- ◇ **Smart-phone**: Samsung, Galaxy S plus I9001
- ◇ **CD player 1**: Sony, CDP-M42
- ◇ **CD player 2**: Pioneer, PD-101

No measurements have been taken except for checking the gain factor utilization and reset condition occurring through SigmaStudio "Readback" programming block.
The test is focused on the sound perception to verify if an optimal amplification is performed from an aural point of view.
A 3 inches test tweeter has been used to fit this aim.

Three key aspects have been taken into account during this evaluation test:

1. if gain commutation takes place correctly
2. if misleading reset condition occurs
3. if a delay of gain commutation is perceivable

Tab. 4.4 summarizes the test results performed using four different audio players, two belonging to Portable devices family and two CD players. All these devices have played the same 5 audio tracks.

Device	Gain commutation	Reset condition during playing	Delayed gain commutation
iPod	not expected	yes	no
Smart-phone	not expected	yes	no
CD player 1	correct	no	yes
CD player 2	correct	no	yes

Table 4.4: System qualitative test results

4.5 Performances considerations

Results of the quantitative test can be summarized as follows:

- ◇ Clipping artifacts have been completely removed, providing a preamplifier input dynamic extension up to 5.00 Vrms.
- ◇ Input signal detected as MP3 signals are boosted while those considered as CD and MIXER signals are accordingly attenuate.
- ◇ Gain condition, as boosting or attenuation, keeps its state until the input signal exceeds a threshold or a reset condition occurs.
- ◇ Gain commutations correctly and quickly occur when an input signal exceeds a threshold limit. As one can see from fig. 4.12, for input signal voltage up to 0.36 Vrms, the system detects input source as a Portable device and gives it a boosting. As soon as the test signal exceeds the threshold of the MP3 devices, the system switches to attenuate the signal because considers it played by a CD player.
  The same happens for CD to Mixer switching and for the shutdown commutation, as shown in fig. 4.13 and fig. 4.14.
- ◇ A maximum voltage preamplifier output, fixed to 1.84 Vrms, is guaranteed for any devices family plugged into the system.

From results of qualitative test can be inferred the following considerations:

- ◇ Boosting for Portable sources and attenuation for CD players are guaranteed.
- ◇ Gain commutations correctly occur thus a correct devices detection is performed.
- ◇ During Portable devices driving misleading reset conditions happen. This is due to the reset threshold level higher than 0 Vrms, which brings the system to consider Portable signal voltage lower than 0.008 Vrms as a reset condition. The high-noisy AUX ADC input denies to use reset condition threshold lower than 0.008 Vrms. Nevertheless this situation doesn't produce any amplification error because when a reset condition occurs the system is reset to its initial amplification state which is exactly the MP3 amplification state.
- ◇ CD players meet with delayed gain commutation especially for audio tracks starting with fade in level or very low intros. Until the toggle state of CD amplification is established, the system detects source as a Portable one, giving an incorrect gain to the signal. As soon as input signal exceeds the $MP3\_threshold$ the correct gain is provided and the system keeps this state until a reset condition occurs. This misleading source detection is due to the overlapping of the level ranges of the three devices families under test. The fig. 4.15 depicts this situation, highlighting ambiguity levels for the devices. A mixer device has its output range which contains CD and MP3 ranges, thus it has a II ambiguity level because both CD and Portable players can produce output included into its output range. In this way a mixer signal can be initially wrongly considered as a Portable or CD signal and can receive an incorrect gain amplification which can produce audible artifacts when gain commutation occurs.
  CD players have a I ambiguity level because their output range includes the MP3 one. As happened during the qualitative test, a low CD signal can be initially considered by the system as a Portable signal and can be boosted rather than attenuated. When the commutation occurs an audible artifact is perceived because a sudden change of sound level happens.
  The delayed gain commutation risk occurs every time the system receives a reset condition, because the toggle behavior of the detection allows to keep the correct amplification state until a reset occurs.

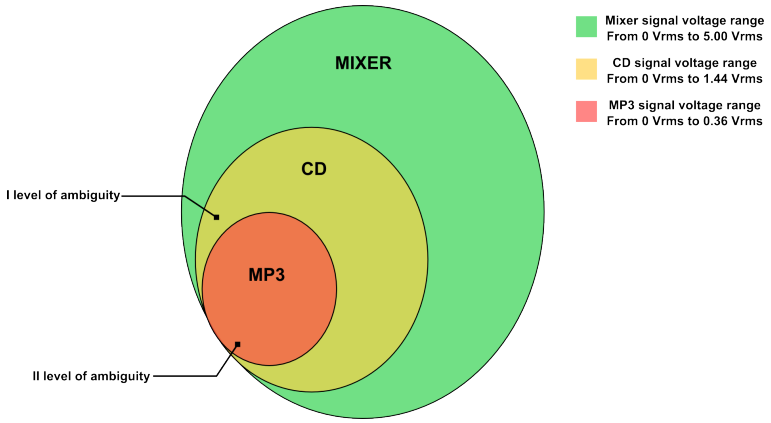


Figure 4.15: Devices output ranges level overlapping

Conclusions and future developments

In this chapter will be highlighted final evaluations about proposed solution for the dynamic input extension. Furthermore will be briefly treated future development solutions.

Input dynamic extension

The combined hardware and software AS preamplifier solution has provided an optimal fitting of 2 of the 3 aims proposed:

1. Preamplifier input dynamic extension up to 5.00 Vrms in order to allow CD and mixer devices interfacing to AS systems
2. Normalized preamplifier maximum output, fixed to 1.84 Vrms, for any device plugged into the system, providing a boosting for Portable sources and attenuation for CD players and mixers.

About the source device detection. the achieved result suffers of a delay during the gain commutation due to the overlapping output ranges of the 3 devices families (Portable, CD players and mixers). Thus the device detection has a "calibration" delay which produces, at least at the first listening, a delayed gain commutation artifact.
Unfortunately this "calibration" delay doesn't occur just on the first ambiguous listening, because the correct gain state is lost each time the input source produces output below the a 0.008 Vrms (reset condition), e.g. during a CD track switching with a pause between 2 consecutive songs or during a pause/stop session.
This misleading detection persistence is due to the way which the reset condition occurs for. Indeed, it happens any time the source output drops below 0.008 Vrms. If reset condition was thrown just when the amplifier input channel was in open circuit state, e.g. when no source is plugged to the system, detection procedure should suffer just of a single "calibration" delay, hence the gain commutation artifact should occur only on the first time.

A future development in order to overcome limitation explained so far, is the introduction of an hardware that listens to open-circuit condition on any input channel. This hardware must be the only reset condition caller of the whole system.

Another significant limitation of the proposed solution in this work, is the usage of two DACs DSP for each input channel, because one DAC is used for the normal input/output association while another one is required in order to produce the VCA

gain correction signal. In this way each input channel cannot drive anymore double loudspeaker modules without external cross-over networks or splitters.

Overcoming this limitation should require an high cost solution, the usage of 8 ADAU1701 processors AS DSP boards or a chip substitution with one equipped by more than 4 DACs per processor.

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