POLITECNICO DI MILANO

Facoltà di Ingegneria Industriale

Corso di Laurea Magistrale in Ingegneria Elettrica

RE-ENGINEERING OF CESI SYNTHETIC TEST LABORATORY: TEST RATING EXTENSION TO 550 kV VOLTAGE CLASS CIRCUIT-BREAKERS

Relatore: Prof. Enrico Ragaini

Correlatore: Ing. Guido Galliano

Tesi di Laurea Magistrale di:
Andrea D'Adda
Matr. 782314

Anno Accademico 2012-2013

Ecco la parte più difficile della Tesi: i RINGRAZIAMENTI.
Si ha sempre paura di dimenticare qualcuno, cercherò di ricordarmi di tutti ma chiedo scusa in anticipo se non riuscirò a farlo.

In primis, ringrazio il Prof. Enrico Ragaini per aver accettato di seguirmi in questo lavoro. I suoi preziosi consigli si sono rivelati indispensabili.

Ringrazio il mio tutor, l'Ing. Guido Galliano, per essere stato sempre disponibile e presente ed avermi insegnato tanto.

Ringrazio l'Ing. Roberto Nicolini per avermi dato la possibilità di svolgere la Tesi presso CESI.

Ringrazio l'Ing. Christian Faiella e l'Ing. Angelo Merlino, per il preziosissimo aiuto che mi hanno dato e per tutto il tempo che mi hanno concesso.

Ringrazio la mia famiglia, che mi ha sempre sostenuto e spronato e che mi ha dato la possibilità di concentrarmi interamente sull'Università. Un grazie speciale a mio papà Eugenio, fonte di ispirazione, senza di te non credo sarei riuscito a concludere questo percorso.

Ringrazio la mia Martina per avermi sostenuto, soprattutto sopportato durante questi mesi, nei quali sono stato davvero insopportabile. Non ho ancora capito come ci sia riuscita.

Ringrazio Paolo e Danielino, compagni di studio e di vita, se sono arrivato fin qui è anche un po' merito vostro.

Ringrazio i miei compagni di corso, fare nomi sarebbe riduttivo. Grazie per i fantastici 5 anni vissuti insieme.

Ringrazio i miei amici di sempre: Bono, Faby, Robi, Gabri, Andre, Verde, Rebu… so che potrò sempre contare su di voi.

Ringrazio Denise, la compagna d'ufficio migliore che mi potesse capitare e con la quale è nata una grande amicizia. Nessun giornata era normale in sua presenza.

Ringrazio Davide Sanvito e gli amici dell'Ufficio Acquisti di CESI, per avermi fatto sentire come a casa mia.

Un ultimo pensiero va ai miei nonni, che da lassù vegliano su di me. Spero di avervi resi orgogliosi.

TABLE OF CONTENTS

INDEX OF FIGURES

INDEX OF TABLES

ABSTRACT

High Voltage circuit-breakers require a number of tests before they can be deployed. Testing methods and equipment are of crucial importance to guarantee the final performance of switchgear.
In particular, specific tests are required in order to ensure that a High Voltage circuit-breaker is capable of interrupting fault currents under specified conditions and in a safe way.
Synthetic Testing is a method by which the effects of a High Power network are reproduced by means of two independent electrical circuits, one to generate pre-interruption current and the other to generate post-interruption voltage. This is often the only possible way in which some severe fault conditions can be tested.

Subject of this work is the Synthetic Laboratory of CESI, dedicated to testing High Voltage circuit-breakers. Our aim is to evaluate the feasibility of an increase of performance of the Laboratory, to upgrade the maximum test voltage for circuit-breakers from the present 420 kV to 550 kV.

This work

- starts by a general description of A.C. High Voltage switchgear,

- outlines test procedures required by Standards about Synthetic testing methods,

- describes the current setup of the CESI Laboratory, and represents it by a mathematical model of the present Synthetic test circuit (ATP software is used for this). Such model is based on the present Laboratory configuration and has been validated comparing results obtained with real wave shapes measured in Laboratory,

- suggests two solutions for the repowering of the CESI Laboratory:

  - ✓ First option: revamping of the present High Voltage Synthetic circuit.
  - ✓ Second option: building a new oscillating circuit in addition to the existing one.

For each of the above options, a mathematical model is defined, based on the one developed for the current 420kV configuration. The dynamic response as per Standard requirements is obtained by calibration of main electrical components value in each model.

The Single Line Diagram for each solution and the specifications relevant to all electrical components (capacitances, inductances, resistances, DC charging units) are then obtained (i.e. main values, rated voltage, rated insulation, energy, etc.).

On the basis of results, two solutions considered are compared to obtain a preliminary evaluation based on the relevant advantages and disadvantages.

SOMMARIO

Gli interruttori ad Alta Tensione necessitano di alcune prove prima di essere messi sul mercato. I metodi e le apparecchiature di prova hanno un'importanza cruciale per garantire il corretto funzionamento dell'apparecchiatura.
In particolare, gli interruttori ad Alta Tensione richiedono prove specifiche per assicurare che siano in grado di interrompere correnti di guasto in condizioni specifiche e in totale sicurezza.
Le Prove Sintetiche sono un metodo nel quale il comportamento fisico di una rete ad alta tensione è riprodotto grazie alla combinazione di due sorgenti indipendenti tra di loro: una che genera la corrente di guasto pre-interruzione e l'altra che genera la tensione che si manifesta ai capi dell'interruttore una volta avvenuta la separazione dei contatti. Questo metodo è spesso l'unico modo possibile per ricreare certe condizioni di guasto.

Oggetto di questo lavoro è il Laboratorio Sintetico di CESI, dedicato alle prove su interruttori ad Alta Tensione fino a 420 kV. Il nostro obiettivo è quello di valutare la fattibilità dell'aumento della massima tensione di prova fino a 550 kV.

Questo lavoro si propone di

- fornire una descrizione generale delle apparecchiature ad Alta Tensione,

- delineare le procedure di Prove Sintetiche definite dalla Normativa,

- descrivere l'attuale Laboratorio di CESI e rappresentare il circuito di Prova Sintetica attraverso un modello matematico (utilizzando ATP come programma di simulazione). Questo modello si basa sull'attuale configurazione del Laboratorio ed è estato validato confrontando i risultati ottenuti dalle simulazioni con le forme d'onda misurate in Laboratorio durante una sessione di prova,

- Proporre due soluzioni per il potenziamento del Laboratorio CESI:

    - ✓ Prima opzione: rinnovamento dell'attuale circuito di Prova Sintetica.
    - ✓ Seconda opzione: costruzione di un nuovo circuito oscillante in aggiunta a quello esistente.

Per ogni opzione sopra citata viene definito un modello matematico basato su quello precedentemente redatto per il 420 kV. Il comportamento dinamico richiesto dalla Norma si ottiene calibrando i principali componenti elettrici presenti in ogni modello.

Per ogni soluzione vengono quindi redatti lo Schema Unifilare contenente i principali componenti (capacità, induttanze, resistenze, generatori di carica) e le loro specifiche elettriche, cioè valore nominale, tensione nominale, livello di isolamento, energia, etc.

Sulla base dei risultati ottenuti, si confrontano le due opzioni considerate per ottenere una valutazione preliminare dei vantaggi e degli svantaggi che ciascuna soluzione comporta.

1. FOREWORD

CESI S.p.A. – **Centro Elettrotecnico Sperimentale Italiano "Giacinto Motta"** – was established in 1956 to provide testing laboratories and certification services for the electromechanical industry.

To this purpose, CESI Milan site is equipped with laboratories to perform High Voltage tests, Medium Voltage tests, EMC tests, etc.

One of the most important laboratories in CESI Milan site is the High Power Synthetic Test Laboratory. In this Laboratory, High Voltage circuit-breakers produced by manufacturers coming from everywhere in the world are tested.

The goal of this work is to evaluate the feasibility of an increase of performance of the **High Voltage Synthetic Laboratory,** to upgrade the maximum testing voltage for circuit-breakers from the present 420 kV to 550 kV.
Such increase is aimed at keeping the technical and performance level of the lab in line with changes in design and engineering practice by utilities all over the world. The trend towards the use of higher voltage in power transmission grids is well-established and can be expected to continue in following years.

Two possible technical solutions are considered:

1. revamping of the present circuit, maintaining the same buildings and the same test method (Weil circuit).

2. deployment of a new oscillating circuit to overcome the limitations of the existing one (parallel current injection plus voltage injection).

In the following chapters these two solutions will be investigated and compared, and for each of them a Single Line Diagram and a preliminary electrical specification of main components will be proposed.

The study only focuses on the High Voltage oscillating circuit. Analysis of the Medium Voltage current circuit, even if connected to the High Voltage Synthetic Laboratory, is not in the scope of this work.

This work is organized in the following chapters:

Chapter 2 describes the main technical requirements of High Voltage apparatus, in particular of circuit-breakers, which are specifically designed to interrupt short-circuit currents.

Chapter 3 describes test procedures required by standards High Voltage circuit-breakers must comply with. Because the most critical operation is current interruption, interruption testing is especially important.

Chapter 4 describes Synthetic interruption testing methods, applied in most laboratories in the world, including CESI. Testing parameters defined by standards are examined in some detail.
Based on technical parameters defined in previous chapters, Chapter 5 outlines the preliminary project requirements for the feasibility of extension of Laboratory capabilities: starting from the present situation, purpose is to raise maximum testing voltage to 550kV.

Chapter 6 describes the current setup of the CESI Laboratory, in terms of both electrical components and facility arrangement. A detailed representation of such setup, in the form of a circuit model, is then presented in Chapter 7. The model needs to be detailed enough to give an accurate description of transient phenomena related to current interruption (in particular, Transient Recovery Voltage). In the same chapter, validation of the model is carried out by comparing theoretical current and voltage transients with real test oscillograms.

Chapter 8 describes the first option for repowering the Laboratory: the same circuit structure is kept, but some components are replaced and improved. A model for this new configuration is derived from the one developed in the previous chapter. Calculations are then performed to assess the limits in performance that can be obtained.

Similarly, the second repowering option, with some much deeper modification to the circuit structure, is examined in Chapter 9, along with calculation results.

The two options are then compared, and possible course of action is discussed, in the final chapter.

2. HIGH VOLTAGE SWITCHGEAR

2.1. Generals

High Voltage switchgear (disconnectors, interrupters, circuit-breakers, etc.) are electrical devices designed for indoor or outdoor installation and for systems having nominal voltages above 1000 V A.C. or 1500 V D.C..
CEI 62271-1 standard, translation of IEC Standards 62271-1, establishes common ratings as rated voltage and related insulation level, rated normal current, rated short-time withstand current, etc.
Rated voltages of switchgear according to the maximum system voltage for which the equipment is designed are shown below.
CEI 62271-1 standard defines two ranges of A.C. voltages, **I** and **II,** as follows:

- Range I: rated voltages up to 245 kV

  3,6 kV – 7,2 kV – 12 kV – 17,5 kV – 24 kV – 36 kV – 52 kV – 72,5 kV – 100 kV – 123 kV – 145 kV – 170 kV – 245 kV

- Range II: rated voltages above 245 kV

  300 kV – 362 kV – 420 kV – 550 kV – 800 kV

2.2. High Voltage A.C. circuit-breakers

2.2.1. Generals

A.C. circuit-breakers are electrical devices designed for indoor or outdoor installation and for operations at 50 ÷ 60 Hz.

A.C. circuit-breakers can operate in normal service conditions (switch normal load current, connect and disconnect no-load lines, cables or capacitor banks, transformers, withstand the over-voltages due to lightning or operation of other switching devices, etc.) and in case of fault, with the purpose to promptly interrupt the fault current and prevent damage to the electric grid and to other related assets.

IEC standards [1] define the circuit-breakers as a switching device able to establish, conduct and interrupt normal and abnormal currents (with the exception that conduction of fault currents is limited in time).
The feature that differentiates circuit-breakers from other switching devices is the ability to interrupt fault currents. This is actually the most critical operation, and for this reason a number of specific tests are aimed at establishing under what conditions it can be successfully performed.

High Voltage circuit-breakers may be three-pole or single-pole.
In this work, only single-pole circuit-breakers, for three-phase system, will be considered.

Three typical aspects of the circuit -breaker design have to be considered:

- Insulation phase to phase and towards earth.
- Operating mechanism.
- Arc extinguishing medium.

2.2.1.1. Insulation phase to phase and towards earth

Two main technologies exist: **AIS** (**Air Insulated Switchgear**) and **GIS** (**Gas Insulated Switchgear**):

- **AIS** (Air Insulated Switchgear):
  Circuit-breakers and other switching devices where the insulation is given by air at atmospheric pressure (*Fig.2.1*).

- **GIS** (Gas Insulated Switchgear):
  Circuit-breakers and other switching devices where the insulation is obtained by gas, usually SF_6 (*Fig.2.2 and Fig.2.3*).

Figure 2.1 - AIS circuit-breaker, commonly named "live tank circuit-breaker", because the enclosure that contains the breaking mechanism is at high voltage.

Figure 2.2 - 420 kV GIS circuit-breaker, equipped with bushings for the connection to the line, commonly named "dead tank circuit-breaker", because the enclosure that contains the breaking mechanism is grounded.

Figure 2.3 - 420 kV GIS circuit-breaker in a Gas Insulated Electrical Station

2.2.1.2. Operating mechanism

Two types of design structures are generally used:

- ✓ Single-pole operating mechanism: each pole of the three-phase circuit-breaker is equipped with one operating mechanism.
- ✓ Three-pole operating mechanism: one operating mechanism common to the three poles.

Present the state of the art technology allows the use of common operating mechanisms to circuit-breakers up to 245 kV rated voltage.

Three types of operating mechanism are used:

- ✓ Electro-mechanical: operation of the circuit-breaker by springs reloaded by a motor.
- ✓ Electro-hydraulic: operation of the circuit-breaker by oil at high pressure.
- ✓ Electro-pneumatic: operation of the circuit-breaker by pressurized air.

2.2.1.3. Arc extinguishing medium

In the vast majority, modern High Voltage circuit-breakers employ one of the following arc extinguishing media:

- ✓ Vacuum: for circuit-breakers rated up to 36 kV.
- ✓ SF6 gas: for circuit -breakers rated 72.5 kV and above.

3. TESTS ON ALTERNATING CURRENT HIGH VOLTAGE CIRCUIT-BREAKERS

3.1. Generals

CEI 62271-100 Standard, translation of IEC 62271-100, establishes the tests to be performed on High Voltage circuit-breakers to prove the good design and the reliability of the apparatus. The tests are split into two categories: **type tests** and **routine tests.**

- **Type tests**: to verify the ratings and characteristics of switchgears, their operating devices and their auxiliary equipment.

  They are performed on some samples representatives of the future mass production.
  Some type tests may impair the original characteristics of the test object.

  Type tests are listed below:

  - ✓ Dielectric tests
  - ✓ Radio Interference Voltage test (R.I.V.)
  - ✓ Measurement of the resistance of circuits
  - ✓ Temperature-rise tests
  - ✓ Short-time withstand current and peak withstand current tests (S.T.C.)
  - ✓ Making and breaking tests (relevant to the present work)
  - ✓ Tests to verify the degrees of protection of enclosures
  - ✓ Tightness tests
  - ✓ Mechanical tests
  - ✓ Environmental tests
  - ✓ Dielectric tests on auxiliary and control circuit

  For convenience of testing, the type tests may be grouped, that is some non-destructive type tests may be performed on the same sample.

  A typical grouping of tests is: Dielectric tests + R.I.V. + Dielectric tests on auxiliary and control circuit + Measurement of the resistance of circuits + S.T.C. or as alternative Mechanical tests + Tightness tests.

  The maximum number of samples to be tested is defined by the standard.

  Type tests must be performed by a third party independent organism to prove that the test object is in accordance with Standards requirements.

- **Routine tests:** to reveal faults in material or construction.

  They do not impair the properties and reliability of a test object.

Routine tests shall be made wherever reasonably practicable at the manufacturer's works on each apparatus manufactured, to ensure that the product is in accordance with the equipment on which the type test have been passed.

Routine tests comprise:

- ✓ Dielectric test on the main circuit
- ✓ Test on auxiliary and control circuit
- ✓ Measurement of the resistance of the main circuit
- ✓ Tightness test
- ✓ Design and visual checks
- ✓ Mechanical operating test

3.2. Making and breaking tests

These tests are aimed at establishing if the circuit-breaker can safely establish and interrupt a certain value of current, under specified voltages and under specified conditions of the circuit.
With reference to the above definition [2], current to be established or interrupted is described by a sine wave of given RMS value, plus an unidirectional component of given amplitude. Voltages involved include in particular supply voltage and transient recovery voltage (TRV). TRV, defined [2] as the transient voltage between terminals of the circuit-breaker after interruption of a current, is especially critical in current interruption, because based on its value and rate of change, arc restrikes might occur (see section "TRV" below).

Making and breaking tests are listed here below:

1. Short-circuit tests (fault occurs at the terminal of the circuit-breaker).
2. Out-of-phase tests (when two electric systems are connected together with the voltages not correctly synchronized).
3. Capacitive current switching tests (operations on no-load lines, cables or capacitor banks).
4. Short-Line Fault (SLF) tests (short-circuit on an overhead line at a short, but significant, distance from the terminals of the circuit-breaker) (see 3.2.4).

Note: **Single-phase and Double-earth fault tests and Short-Line Fault tests are not within the scope of this study**.

Miscellaneous provisions for making and breaking tests are described in CEI 62271-100 standard.
Circuit-breakers shall be capable of making and breaking at the rated voltage all currents up to the rated short-circuit breaking current. Tests items 1 and 2 are representative of a fault condition in the electric network, while tests item 3 are representative of a normal switching operation that could produce very high over-voltages dangerous for the electric grid (re-strike phenomena).

3.2.1. Short-circuit test-duties (terminal fault)

They consist of 5 test-duties (labeled T10 – T30 – T60 – T100s – T100a, where T means “Terminal fault”) at the assigned test voltage, with test currents from 10% (T10) to 100% of the rated short-circuit current in symmetrical and asymmetrical conditions (T100s and T100a).

In order to test 550 kV circuit-breakers, IEC Standards require a first-pole-to-clear factor (**f.c.p.f.** or k_{pp}) less than or equal to 1.3.

The first-pole-to-clear factor is the ratio between the recovery voltage across the first pole to clear after current clearance and the phase to ground voltage of the system. It depends on the grounding arrangement of the electrical system.
Standards define two values of this factor:

- For **systems with ungrounded neutral, k_{pp} is or tends towards 1.5**. Such systems can be met with rated voltages less than 245 kV; however this configuration it is not common at transmission voltages, i.e. greater than 72.5 kV, as effective grounding is the norm.

- For **effectively grounded neutral systems**, the realistic and practical value is dependent upon the sequence impedances of the actual earth paths from the location of the fault to the various system neutral points (ratio X_0/X_1). For these systems this ratio is considered to be less or equal to 3 and **k_{pp} is 1.3**.

Equation below shows how to calculate the first-pole-to-clear factor:

$$k_{pp} = \frac{3X_0}{X_1+2X_0}$$

where X_0 is the zero sequence, and X_1 the positive sequence reactance of the system:

- If $X_0 \gg X_1$, as in **ungrounded system ➔ k_{pp} = 1.5**
- If $X_0 = 3 \cdot X_1$, as in **effectively grounded neutral system ➔ k_{pp} = 1.3**

The following chart reports the first-pole-to-clear factors requested by IEC 62271-100 Standard with their related standardized voltage levels:

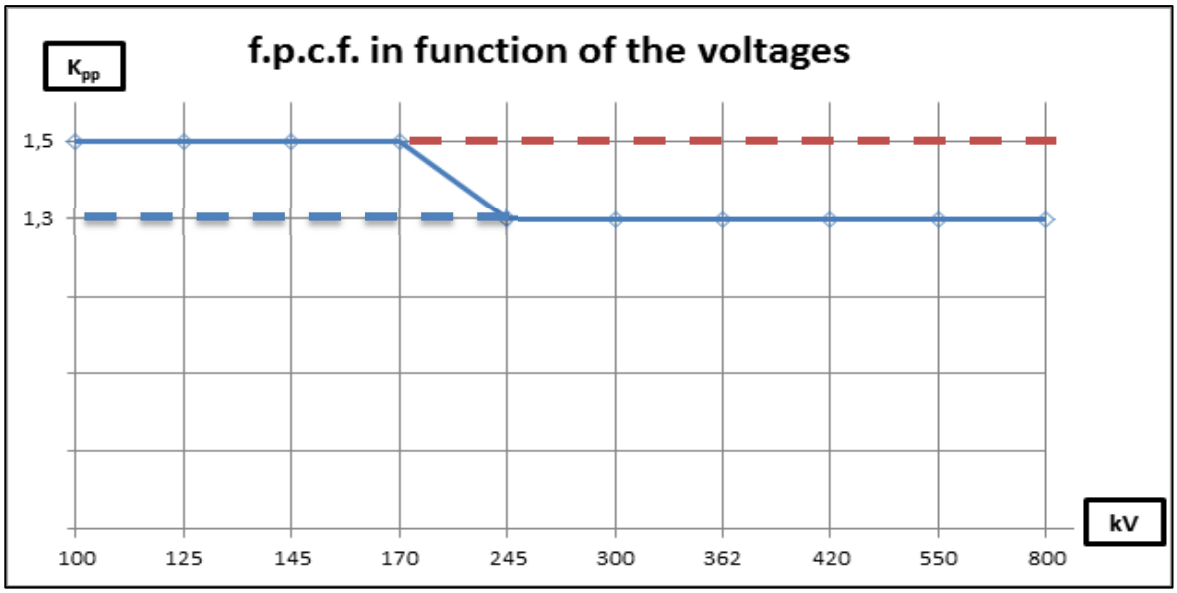


Figure 3.1 - First-pole-to-clear factor in function of the voltages

However, for special applications in transmission systems with effectively grounded neutral where the probability of three phase ungrounded faults cannot be disregarded, a test with first-pole-to-clear factor of 1.5 may be required (red dashed line in the chart).

For the above mentioned reason some manufacturers require tests with a first-pole-to-clear factor equal to 1.5.

Table on next page reports a summary of short-circuit test-duties.

Table 3.1 - Short-circuit test-duties rated values

Rated breaking current	**Test duty**	**Test voltage**			**Test current**			**Transient Recovery Voltage (TRV)**		
I_r [kA]	**N°**	**k_{pp} [p.u.]**		**U [kV]**	**I [kA]**	**Toll. %**	**$I_{MAX/min}$ [kA]**	**k_{af} [p.u.]**	**U/t [kV/μs]**	**Wave shape**
50	T10	1.5	IEC	476	5	+20	6	0.9·1.7	7	2p
						-20	4			
	T30	1.3	IEC	413	15	+20	18	1.54	5	2p
		1.5	Special application	476		-20	12			
	T60	1.3	IEC	413	30	+10	33	1.5	3	4p
		1.5	Special application	476		-10	27			
	T100	1.3	IEC	413	50	-	50	1.4	2	4p
		1.5	Special application	476		-				
63	T10	1.5	IEC	476	6.3	+20	7.56	0.9·1.7	7	2p
						-20	5.04			
	T30	1.3	IEC	413	18.9	+20	22.7	1.54	5	2p
		1.5	Special application	476		-20	15.1			
	T60	1.3	IEC	413	37.8	+10	41.6	1.5	3	4p
		1.5	Special application	476		-10	34			
	T100	1.3	IEC	413	63	-	63	1.4	2	4p
		1.5	Special application	476		-				

where k_{af} is the amplitude factor of the Transient Recovery Voltage and U/t is the rate-of-rise of the Transient Recovery Voltage [2].

3.2.2. Out-of-phase test-duties

They consist of two test-duties OP2 and OP1 (not mandatory) at the assigned test voltage, the first-one at the rated out-of-phase breaking current (25% of rated short-circuit breaking current) and the other at 30% of rated out-of-phase breaking current.

Taking into account that 550 kV electrical systems are generally effectively earthed, a multiplication factor ***m.f.*** equal to 2 is considered to be applied to the phase to ground voltage (see IEC Standard 62271-100, clause 6.110.2).

m.f. = 2 is graphically explained with diagram below:

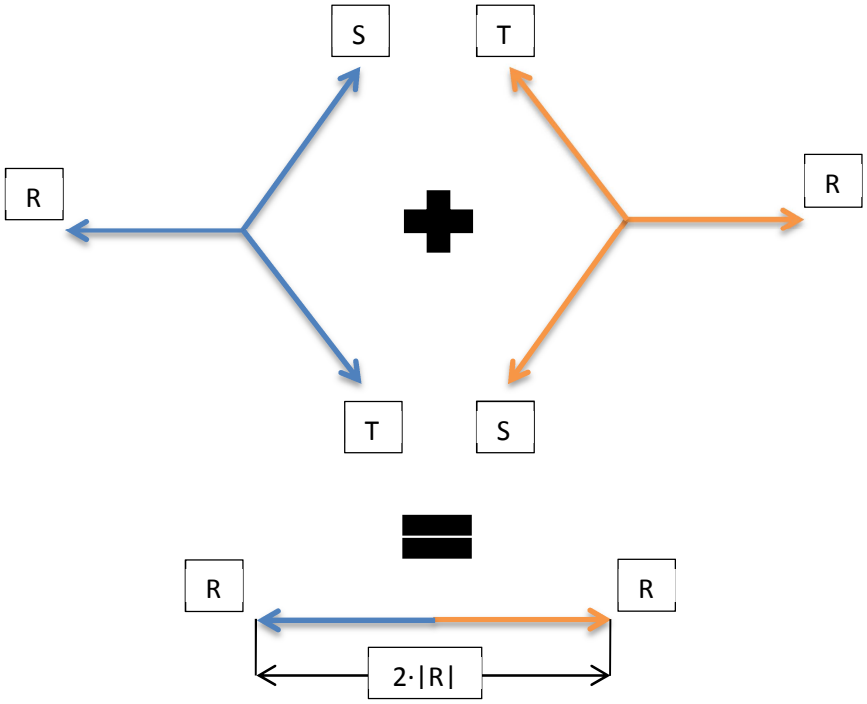


Figure 3.2 - Out-of-phase: graphical demonstration of multiplication factor equal to 2.

Table below shows the most important values for this type of tests:

Table 3.2 - Out-of-phase test-duties rated values

Rated breaking current	Test-duty	Test voltage		Test current	Transient Recovery Voltage (TRV)		
I_r [kA]	N°	*m.f.* [p.u.]	U [kV]	I [kA]	k_{af} [p.u.]	U/t [kV/µs]	Wave shape
12.5	OP1	2	636	2.5 ÷ 5	1.25	1.54	4p
	OP2			12.5			
15.75	OP1			3.15 ÷ 6.3			
	OP2			15.75			

3.2.3. Capacitive current switching tests

Consist of two test-duties for each service condition at the assigned test voltage for no-load lines switching (LC1-LC2), cables switching (CC1-CC2) or single capacitor banks (BC1-BC2). One test-duty is performed at the assigned rated value while the other is performed with a test current in the range 20% ÷ 40% of the rated value.

Since Standards define that a 550 kV electrical system must be effectively earthed, IEC Standards 62271-100, clause 6.111.7 define a phase voltage multiplication factor k_c to be applied to the phase to ground voltage according to the electrical system conditions.
Table below summarize capacitive current switching tests:

Table 3.3 - Capacitive current switching tests rated values

Test-duty	**Test voltage**		**Test current**	**Test frequency**	**Recovery Voltage (1-cos) wave shape**	
N°	k_c **[p.u.]**	**U [kV]**	**I [A]**	f **[Hz]**	U_c **[kV]**	**Time-to-peak [ms]**
LC1, CC1, BC1	1.0	318	100 ÷ 200	50	900	10
				60		8.3
	1.2	382		50	1080	10
				60		8.3
	1.4	445		50	1260	10
				60		8.3
LC2, CC2, BC2	1.0	318	500	50	880	10
				60		8.3
	1.2	382		50	1055	10
				60		8.3
	1.4	445		50	1225	10
				60		8.3

3.2.4. Short-Line Fault test-duties

SLF test-duties are performed with an artificial line that simulates a short-circuit on an overhead line at a short distance from line-side terminal of the circuit-breaker (the other terminal is on the source-side).
This distance is not more than few kilometres (“short line”).

As per 62271-100 Standard requirements, for rated voltages from 100 kV to 800 kV, test-duties L_{75} and L_{90} are considered, where

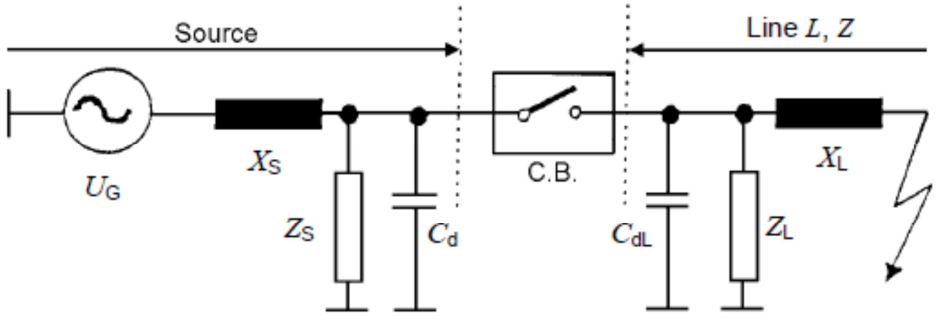
- L means “Line” (Short-LINE Fault)

- the two specified numeric values (75 and 90) are percentage values (75% and 90%). They specify the values of the A.C. component of the rated short-circuit breaking current, reduced due to the presence of line-side impedance:

  - ✓ L_{75} ➔ 25% of line-side impedance is considered; it means that the short-circuit breaking current is de-rated to 75% of the rated short-circuit breaking current.
  - ✓ L_{90} ➔ 10% of line-side impedance is considered; it means that the short-circuit breaking current is de-rated to 90% of the rated short-circuit breaking current.

Further information are available on IEC 62271-100 Standard.

Figure below shows a basic Short-Line Fault circuit.



U_G	supply voltage, phase to earth value	X_L	power frequency line side reactance
X_S	power frequency source side reactance	Z_L	line side TRV controlling components
Z_S	source side TRV controlling components	C_{dL}	time delaying line side capacitance
C_d	time delaying source side capacitance	Z	surge impedance of line
C.B.	circuit-breaker	L	length of line to fault

Figure 3.3 - Basic Short-Line Fault circuit

3.3. Performing of making and breaking tests

Making and breaking tests are performed in testing laboratories that can use **direct** or **synthetic** testing methods:

- **Direct tests:** the test voltages (applied, recovery and transient recovery voltage - TRV) and test current may be all obtained from a single power source.
- **Synthetic tests**: the test voltages (applied, recovery and TRV - see 4.4) and test current may be obtained from several sources where all of the current, or a major portion of it, is obtained from one source, and the test voltages are obtained entirely or in part from one or more separate sources.

Several methods based either on direct or on synthetic test methods may be used.

If possible, the complete circuit-breaker is tested in a three-phase circuit. However, if this is not possible due to limitations of the testing facilities, short-circuit performance can be proved by one of the following procedures with a single-phase test circuit:

- ✓ Single-pole testing (one complete pole is tested)
- ✓ Unit testing (if the pole includes several interruption chambers in series, one of them is tested)

3.4. Transient Recovery Voltage (TRV)

The Transient Recovery Voltage (TRV) related to the short-circuit breaking current is the reference voltage limit of the prospective transient recovery voltage of circuits which the circuit-breaker shall be capable of withstanding under fault conditions.

TRV waveforms that has to be applied to circuit-breaker under test are specified by the Standard. Two possible classes of waveform envelopes are described, and expressed as a function of

- two parameters (labeled: 2p TRV envelope)
- four parameters (labeled: 4p TRV envelope); in this case Standards define three envelopes.

The two parameters and four parameters envelopes have been introduced in order to facilitate the comparison of a TRV obtained during testing and a specified TRV. Two parameters and four parameters envelopes are used respectively for oscillatory and exponential TRV:

- oscillatory TRV occurs generally when a fault is limited by a transformer or a series reactor and no transmission line or cable surge impedance is present to provide damping.

  To be oscillatory, the condition is $Z_{eq} \geq \frac{1}{2}\sqrt{\frac{L_{eq}}{C_{eq}}}$, where $Z_{eq}$is the equivalent surge impedance, L_{eq} and C_{eq} are the equivalent source inductance and capacitance. Figure on next page shows the above mentioned case.

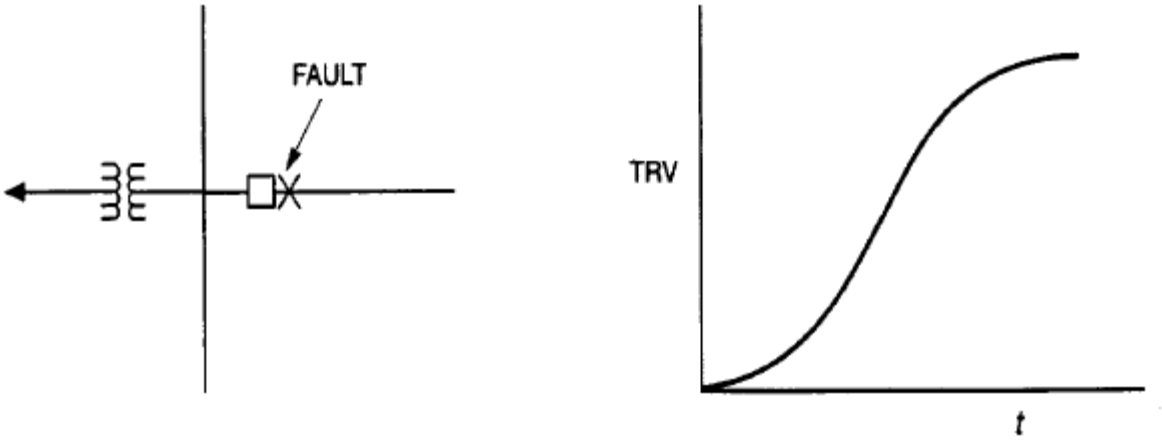


Figure 3.4 - Oscillatory TRV

- Exponential TRV is obtained typically on the source-side of a circuit-breaker during interruption of a fault at the circuit-breaker terminals. This exponential part of TRV occurs when $Z_{eq} < \frac{1}{2}\sqrt{\frac{L_{eq}}{C_{eq}}}$, where $Z_{eq}$is the equivalent surge impedance of the *n* connected lines in parallel, L_{eq} and C_{eq} are the equivalent source inductance and capacitance.
  The exponential part of TRV, defined by equation $V_{cb} = V_0\left(1 - e^{-t/\tau}\right)$ appears also as travelling waves on each of the transmission lines. Reflected waves returning from open lines contribute also to the TRV as shown in figure below:

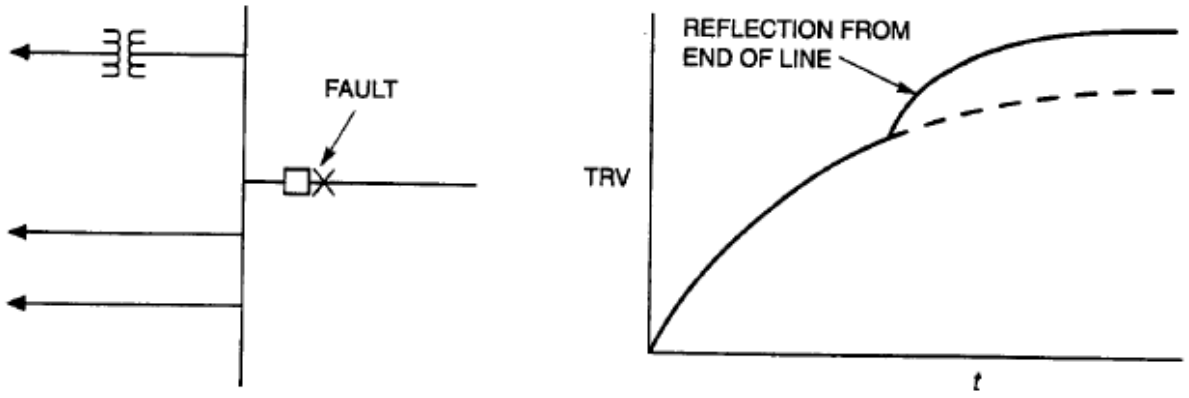


Figure 3.5 - Exponential TRV

For standardization purposes, two parameters envelopes are specified for circuit-breakers rated less than 100 kV, at all values of breaking current, and for circuit-breakers rated 100 kV and above if the short-circuit current is equal or less than 30% of the rated breaking current. Four parameters envelopes are specified in other cases.

Basing on the consideration described above, two parameters representation of the TRV is used for test-duties T10 and T30, while a representation by four parameters of the TRV is used for test-duties T60, T100, SLF and out-of-phase tests.

Figures reported on next pages show 2p TRV envelope and 4p TRV envelopes.

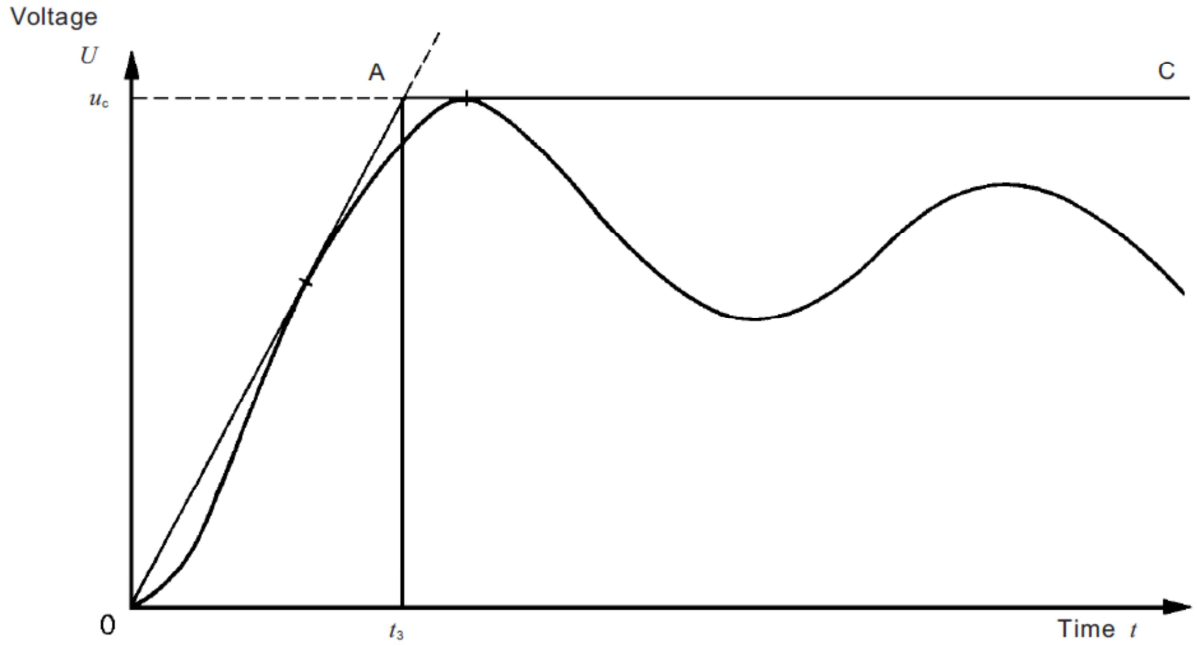


Figure 3.6 - 2 parameters TRV envelope (fig. E.4 of ANNEX E, IEC 62271-100)

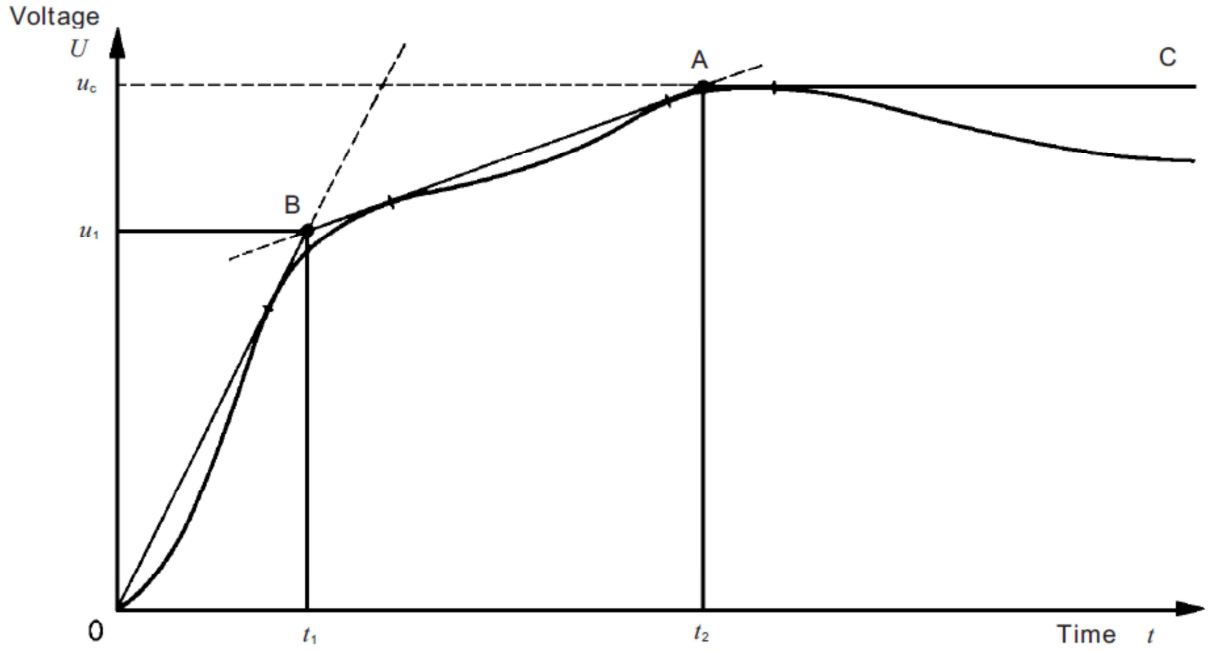


Figure 3.7 - 4 parameters TRV envelope (fig. E.2 of ANNEX E, IEC 62271-100)

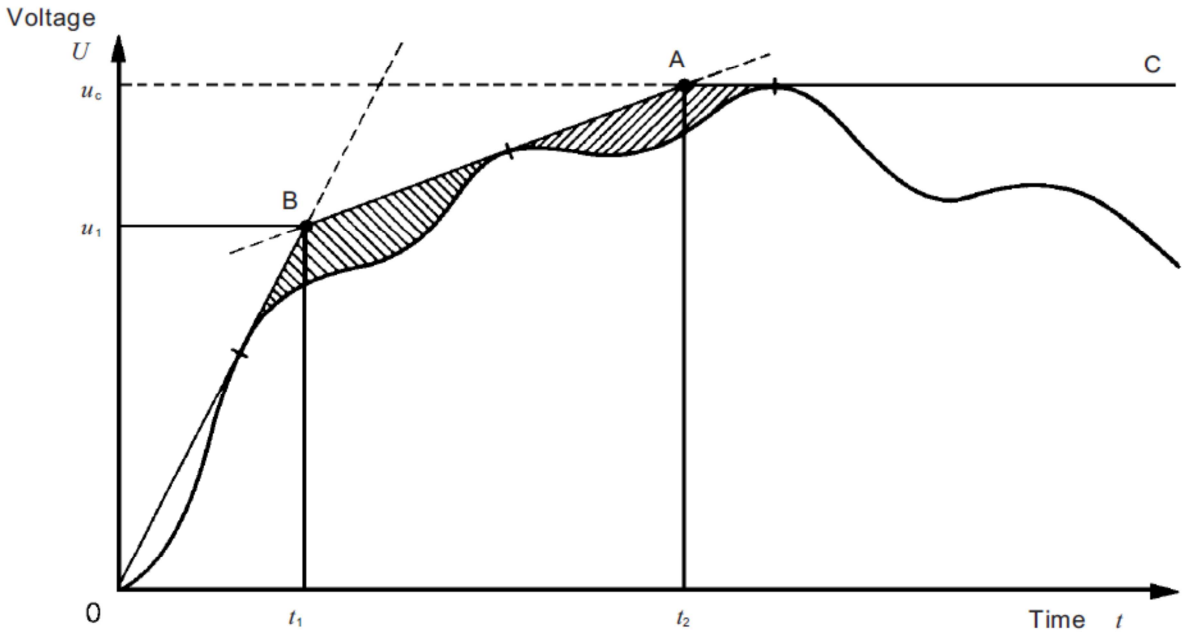


Figure 3.8 - 4 parameters TRV envelope (fig. E.3 of ANNEX E, IEC 62271-100)

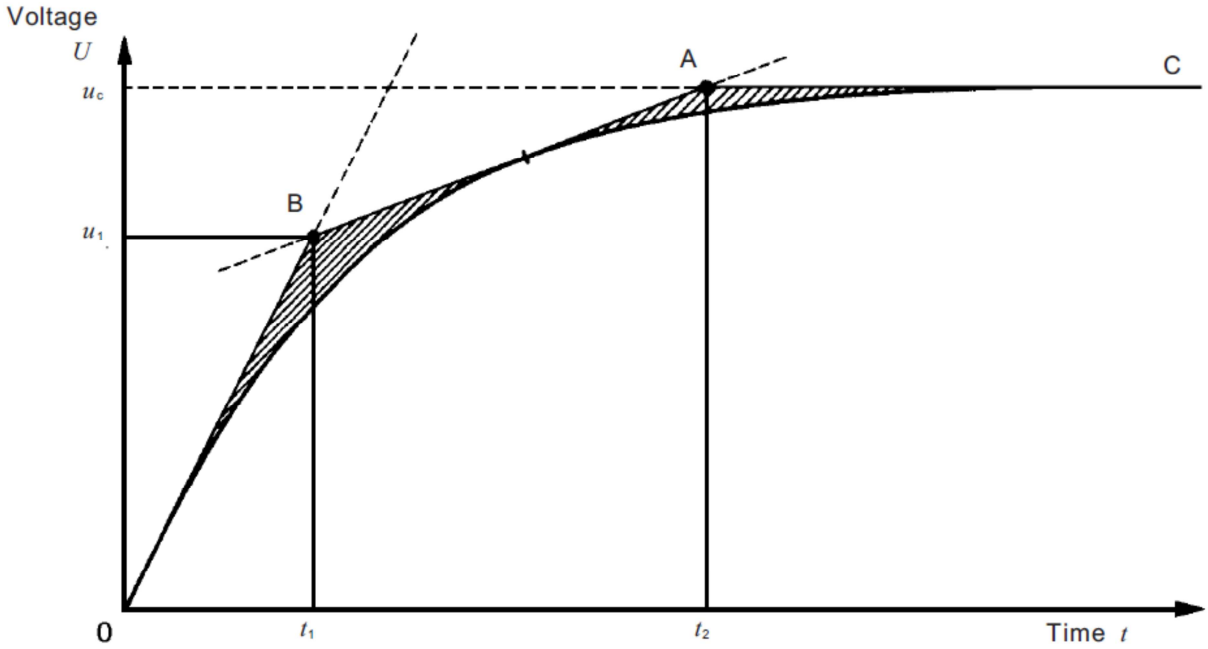


Figure 3.9 - 4 parameters TRV envelope (fig. E.1 of ANNEX E, IEC 62271-100)

4. SYNTHETIC TESTS

4.1. Generals

Standard [3] defines synthetic test as follows:

"Tests in which all of the current, or a major portion of it, is obtained from one source (current circuit), and in which the applied voltage and or the recovery voltages (transient and power frequency) are obtained entirely or in part from one or more separate sources (voltage circuits)".

So, synthetic test is the combination of a current source supplying the arc current causing thermal stress on the device, and a separate voltage source, supplying the transient recovery voltage which causes the dielectric stress.

With the increasing breaking capacity of circuit-breakers, synthetic testing has become common today, because it requires less expensive and complex test facilities in comparison with direct testing.

In fact, by using a power source with a relatively low output voltage (in the range 10 ÷ 30 kV) for the short-circuit current, and a capacitor circuit charged at a high voltage for the transient recovery voltage and recovery voltage (A.C., D.C. or oscillating), synthetic testing is an economic way to cope with the limitations of the direct power source of a high-power laboratory. In addition, because current and voltage circuit are separated, the same current source must be used to test different kind of breakers at different voltages.

Another benefit of synthetic testing is the reduction of required energy: unlike direct testing, where energies are very high, synthetic testing allows safer tests with less damage for the test object in case of test failure: direct tests are destructive in case of test failure, because of the higher energy involved. Moreover, synthetic tests prevent the risk of explosion: this means less expensive civil works, and allows manufacturers to inspect the breaking unit after a failure, or the repetition of the test(s) with the same device under different conditions, i.e. gas pressure, speed of contacts, etc…

4.2. Synthetic testing methods for short-circuit breaking tests

Two synthetic testing techniques are used:

- current injection methods
- voltage injection methods

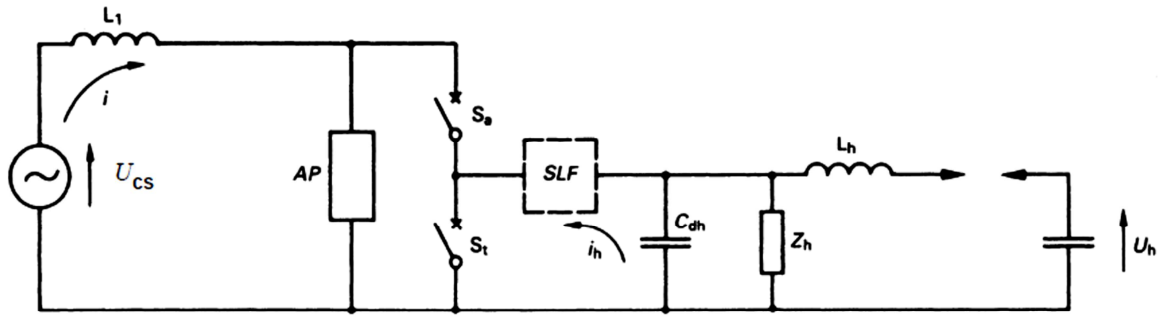
4.2.1. Current injection methods

The superposition of the currents takes place shortly before the zero of the power-frequency short-circuit current. A current of smaller amplitude but higher frequency, derived from the voltage circuit, is superimposed by injection either in the test circuit-breaker or in the auxiliary circuit-breaker. The instant of switching in this injected current is selected by means of a current-dependent control circuit. This instant should

be such that the character of the resulting current wave in the test circuit-breaker corresponds to that of the specified breaking current prior to the current zero during the interval of significant change of arc voltage. In this way, the circuit-breaker under test is automatically connected into the voltage circuit after the interruption of the current in the auxiliary circuit-breaker, so there will be no delay between the current stress and the application of the voltage stress.

There are two types of circuit layout:

- **Current injection circuit with voltage circuit in parallel with the test circuit-breaker (parallel circuit)**
  Circuit below (*Fig.4.1*) describes a typical current injection method with voltage circuit in parallel with the test object.



U_{cs}	voltage of current circuit	C_{dh}	capacitance for time delay of voltage circuit
L_1	inductance of current circuit	L_h	inductance of voltage circuit
AP	arc prolonging circuit	U_h	charging voltage of voltage circuit
S_a	auxiliary circuit-breaker	i	current of the current circuit
S_t	test circuit-breaker	i_h	injected current
Z_h	equivalent surge impedance of voltage circuit	SLF	short-line-fault circuit (for the corresponding tests)

Figure 4.1 - Simplified layout of a current injection parallel circuit (fig. B.1 of ANNEX B, IEC 62271-101)

The voltage circuit is switched in shortly before the zero of the power-frequency short-circuit current, prior to the interaction interval (see IEC 62271-101 sub-clause 4.1.3).

Fig.4.2 on next page shows the typical current wave shape in the circuit-breaker under test.

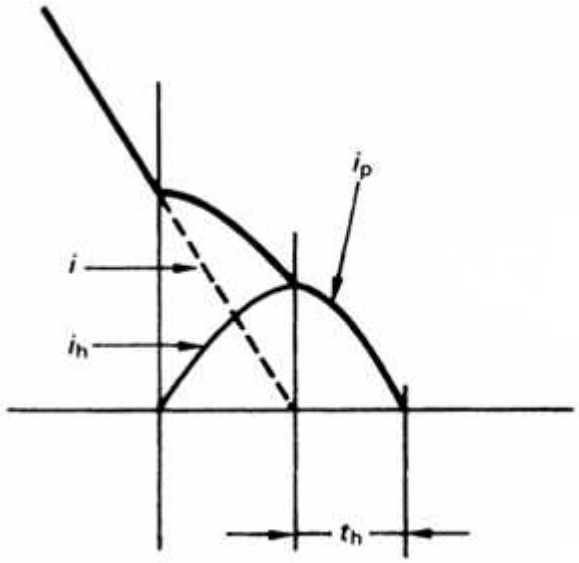


Figure 4.2 - Current wave shape in the circuit-breaker under test (fig. B.2 of ANNEX B, IEC 62271-101)

At this time the high-frequency oscillatory current i_h is superimposed on the power-frequency short-circuit current i, with the same polarity to give a resultant test current in the test circuit-breaker.
After the auxiliary circuit-breaker interrupts the power-frequency short-circuit current i, the test circuit-breaker is connected only to the voltage circuit and i_h is the only remaining current.
The voltage circuit also provides the recovery voltage across the test circuit-breaker after the current is interrupted.

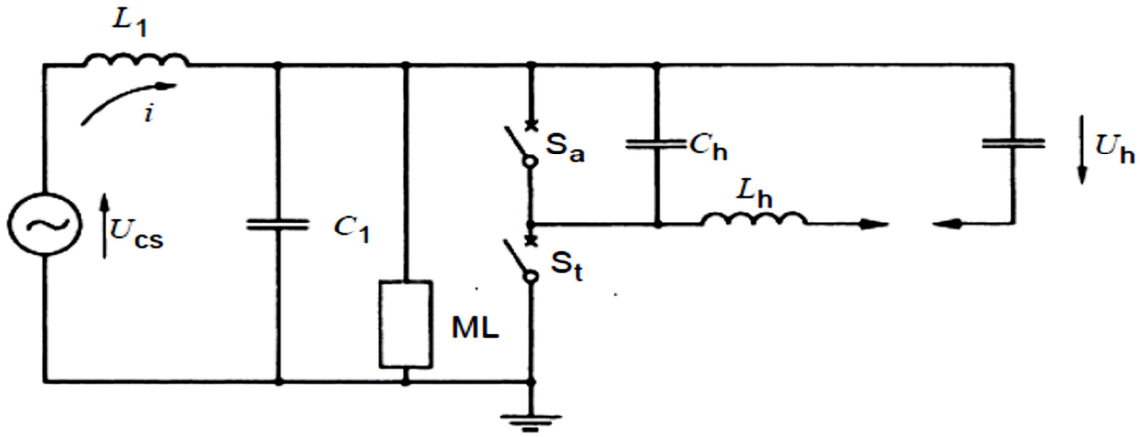
- **Current injection circuit with the voltage circuit in parallel with the auxiliary circuit-breaker (series circuit)**
  This circuit is not of common usage.
  Information are available in IEC 62271-101.

4.2.2. Voltage injection methods

The current circuit provides the entire short-circuit current for the test circuit-breaker and also, after current zero, the first part of the transient recovery voltage.
By suitable choices of its voltage and natural frequency, the correct values of the power factor, current and first part of the TRV can be obtained.
About at the time of the first peak of the transient recovery voltage of the current circuit, the voltage circuit is switched in by means of a voltage-dependent control circuit in such a way that the specified transient recovery voltage is continued and so that there will be no delay between the current stress and the voltage stress.
CEI 62271-101 standard describes two main types of voltage circuit layout, but only the voltage injection series circuit is in common usage.

- **Voltage injection circuit with the voltage circuit in parallel with the auxiliary circuit-breaker (series circuit):**
  The current circuit supplies the entire short-circuit current. A capacitor of suitable value is connected in parallel with the auxiliary circuit-breaker. After the current zero of the power-frequency short-circuit current, this capacitor transmits the entire

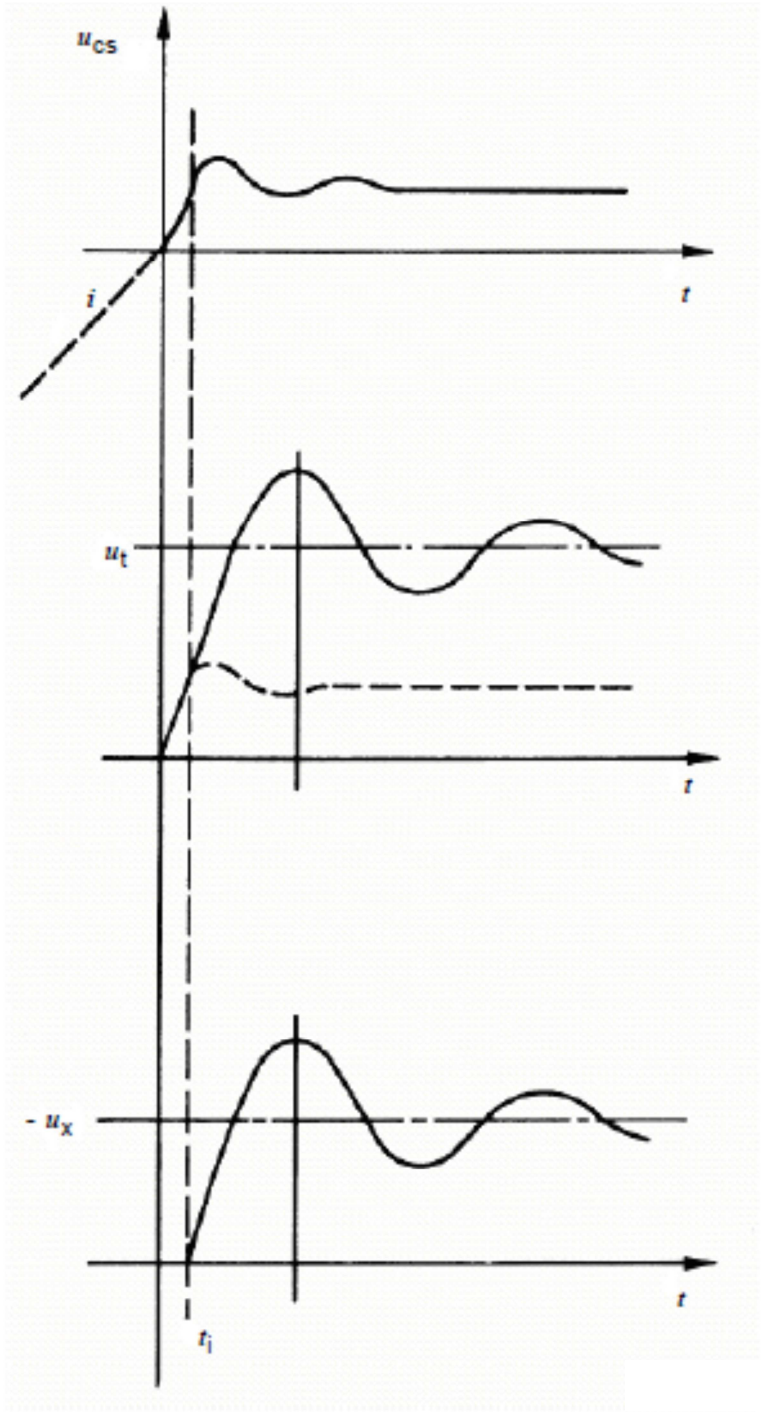
transient recovery voltage of the current circuit to the test circuit-breaker, providing the energy required for the post-arc current.
About the time of the first peak of this transient voltage, the voltage circuit will be switched in and from this moment onwards the transient recovery voltages of both circuits are added together to form the transient recovery voltage across the test circuit-breaker.
A simplified layout of the voltage injection series circuit is represented in *Fig.4.3*:



U_{cs}	voltage of current circuit	S_t	test circuit-breaker
L_1	inductance of current circuit	C_h	capacitance of voltage circuit which together with L_h controls the major part of the TRV
C_1	capacitance of current circuit which together with L_1 controls the first part of the TRV	L_h	inductance of voltage circuit
ML	multi-loop re-ignition circuit	U_h	charging voltage of voltage circuit
S_a	auxiliary circuit-breaker		

Figure 4.3 - Simplified layout of the voltage injection series circuit (fig. C.1 of ANNEX C, IEC 62271-101)

Figure 4.4 (next page) shows the typical TRV wave shapes obtained with this type of voltage injection circuit.



i	power-frequency current in test and auxiliary circuit-breakers	u_t	voltage across test circuit-breaker
u_{cs}	TRV from current circuit	u_x	voltage across auxiliary circuit-breaker
		t_i	instant of voltage injection

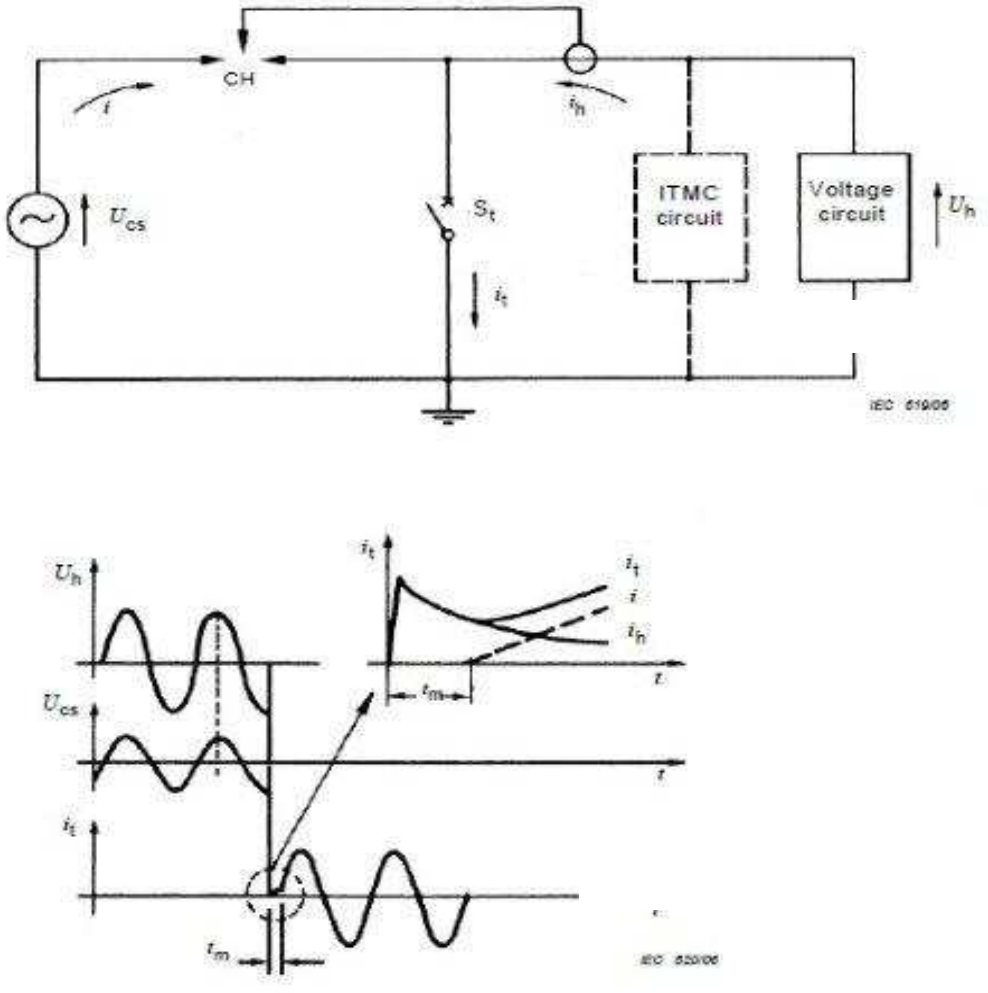
Figure 4.4 - TRV wave shapes of a voltage injection circuit (series circuit)(fig. C.2 of ANNEX C, IEC 62271-101)

4.3. Synthetic testing methods for short-circuit making tests

During a closing operation onto short-circuit, the circuit-breaker contact gap is subjected to the applied voltage. After the instant of breakdown, the circuit-breaker is subjected to the short-circuit current.

The synthetic test circuit consists of two sub-circuits: the current circuit at reduced voltage that supplies the short-circuit current, and the voltage circuit that applies the required test voltage to the circuit-breaker under test. The current circuit is connected to the circuit-breaker immediately after breakdown of the contact gap by means of a fast making device, e.g. a triggered spark-gap., so that the circuit-breaker is subjected to the correct pre-arc energy and electro-dynamic forces due to the current and contacts friction forces. The applied voltage may be A.C., D.C., or a combination of the two.

A simplified test circuit scheme (similar to the circuit used at CESI) is shown in the following *Fig.4.5*:



Key			
U_{cs}	voltage of current circuit	U_h	applied voltage
CH	making device (triggered spark gap)	i_h	initial transient making current (ITMC)
i	power-frequency current supplied by current circuit	i_t	current in the test circuit-breaker
S_t	test circuit-breaker	t_m	time delay of making device

Figure 4.5 - Test circuit scheme for synthetic making tests (fig. 5 of IEC 62271-101)

4.4. Other synthetic test circuits

Other synthetic test circuits have been developed, combining current injection and voltage injection methods, and for switching of capacitive current, to overcome the limitations of direct tests in terms of available test voltage and reactive power of capacitor bank.

The synthetic test circuits developed and used by CESI for out-of-phase and capacitive current switching tests are described below.

4.4.1. Synthetic test circuit for out-of-phase tests

The circuit is a combination of a current injection circuit (red dots) and a voltage injection circuit (blue dots) each of their applied to one terminal of the circuit-breaker under test.

Each circuit provides a 2p TRV, and their proper combination results in the requested 4p TRV between the terminals of the circuit-breaker.

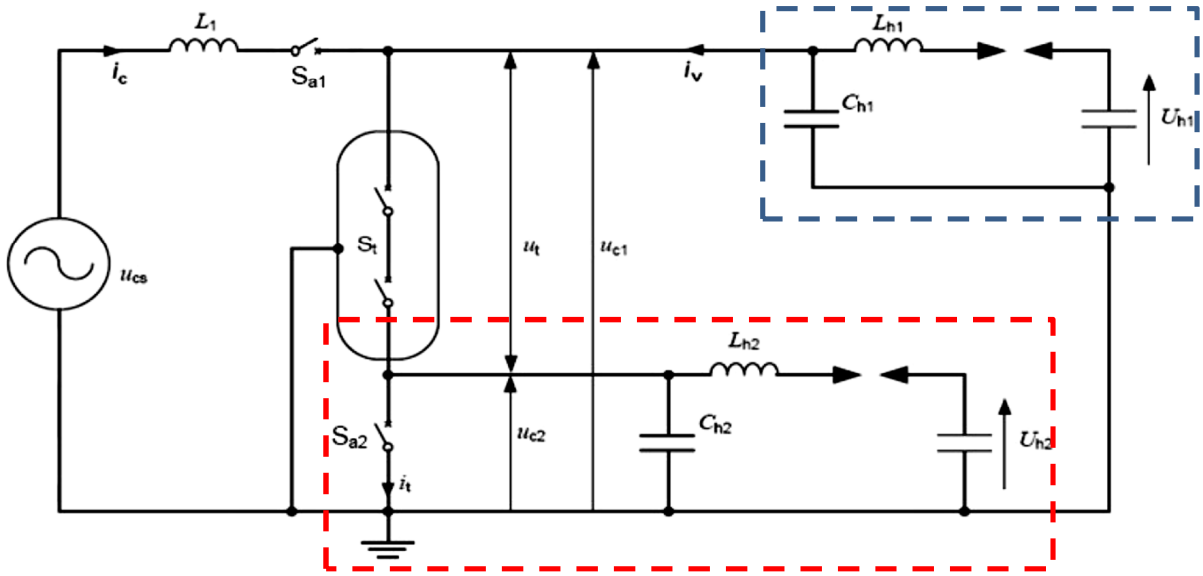
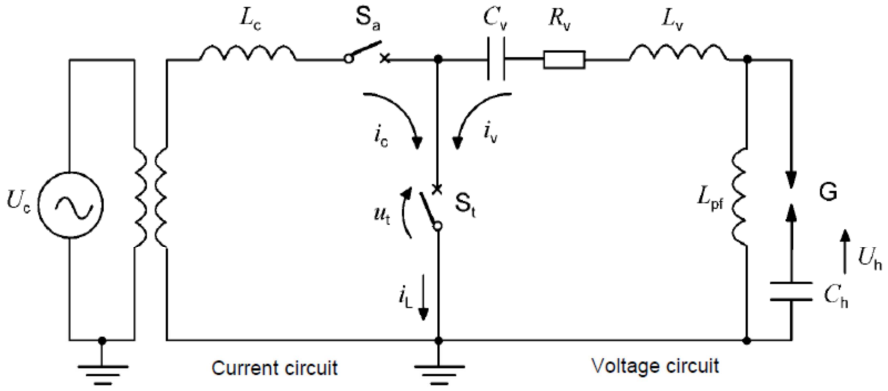


Figure 4.6 - Simplified test circuit scheme for out-of-phase tests (see fig.10 of STL guide for IEC 62271-101)

4.4.2. Synthetic test circuits for capacitive current switching tests

The circuits used at CESI are shown in the fig. 4.7, 4.8 and 4.9.



$U_c = u_t/n$	$U_h = \frac{(C_v + C_h)}{C_h} U_t \sqrt{2}$
$i_c = I_l$	$i_v = \frac{U_h}{\omega_0 L_v} e^{-\alpha \hat{t}} \sin \omega_0 \hat{t}$, with $\alpha = \frac{R_v}{2L_v}$ and $\omega_0 = \sqrt{\frac{1}{L_v}\left(\frac{1}{C_h} + \frac{1}{C_v}\right) - \left(\frac{R_v}{2L_v}\right)^2}$
$\omega L_c = \frac{1}{n \times \omega \times C_L}$	$L_v = \frac{U_h}{i_L \times \omega \times \sqrt{2}}$
C_L = equivalent load capacitance	

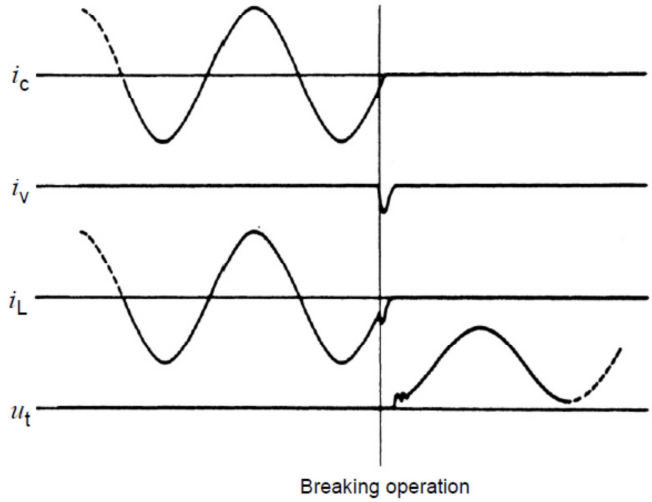
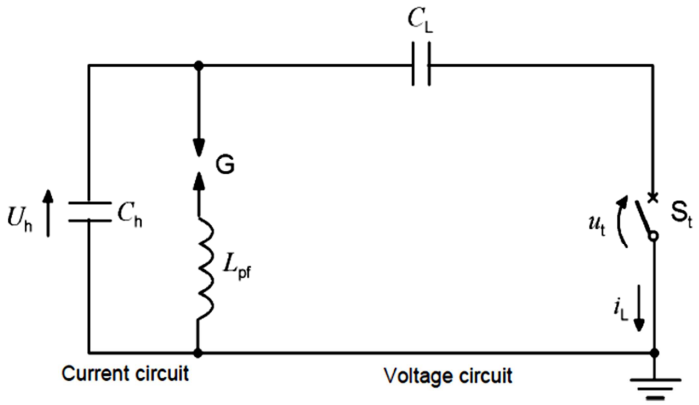
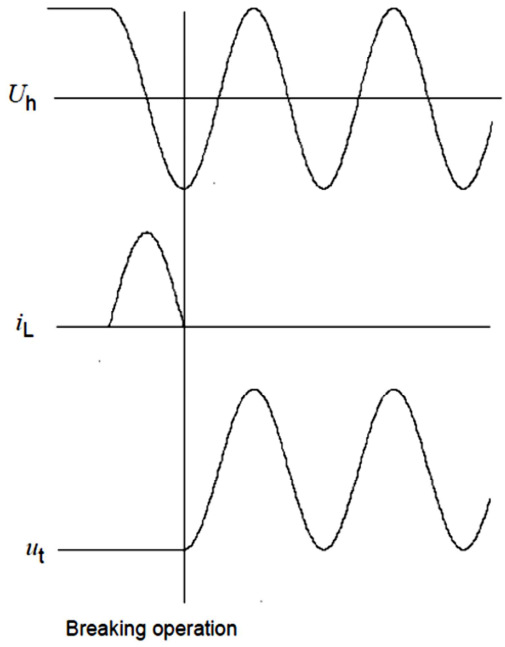


Figure 4.7 - Current injection circuit (fig.G.2 of ANNEX G, IEC 62271-101)

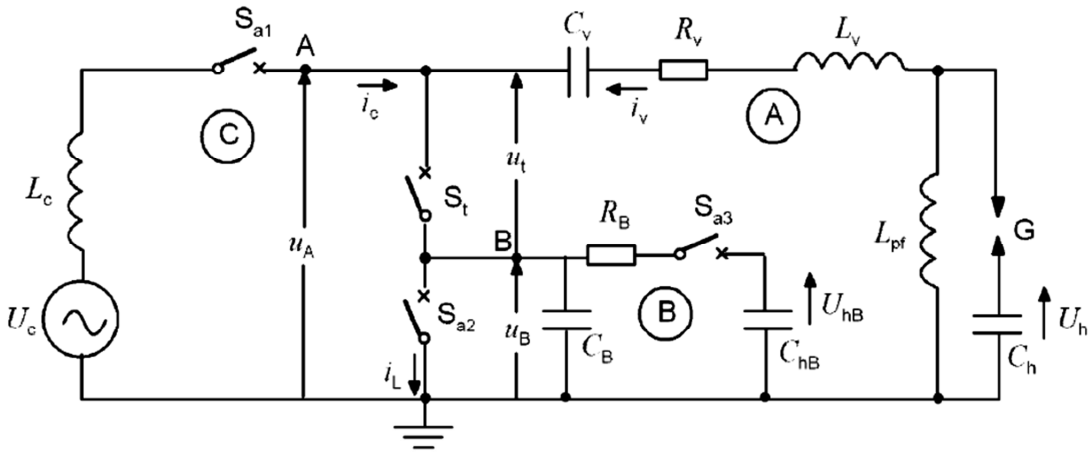


$U_h = U_t\sqrt{2}$	$i_L = 2\pi f_L \times C_L \times U_h$
$f_{RV} = \frac{1}{2\pi\sqrt{C_h \times L_{pf}}}$	$f_L = \frac{1}{2\pi\sqrt{(C_h + C_L) \times L_{pf}}}$
C_L= load capacitance	



C_h and C_L are pre-charged at the voltage U_h.

Figure 4.8 - LC oscillating circuit (fig. G.3 of ANNEX G, IEC 62271-101)



This test circuit consists of three circuits:

- circuit A is a conventional current injection circuit connected to one terminal of the test circuit breaker earth supplying a recovery voltage U_A of (1-cos) waveshape;
- circuit B is connected to the other terminal of the test circuit-breaker applying an exponential voltage (1-exp(-t/t_0)waveshape). Its amplitude, rate of decay and timing are chosen with consideration to the voltage applied on the other terminal of the test circuit-breaker, so that the correct recovery voltage (u_t) is applied across the contacts;
- circuit C supplies the test current.

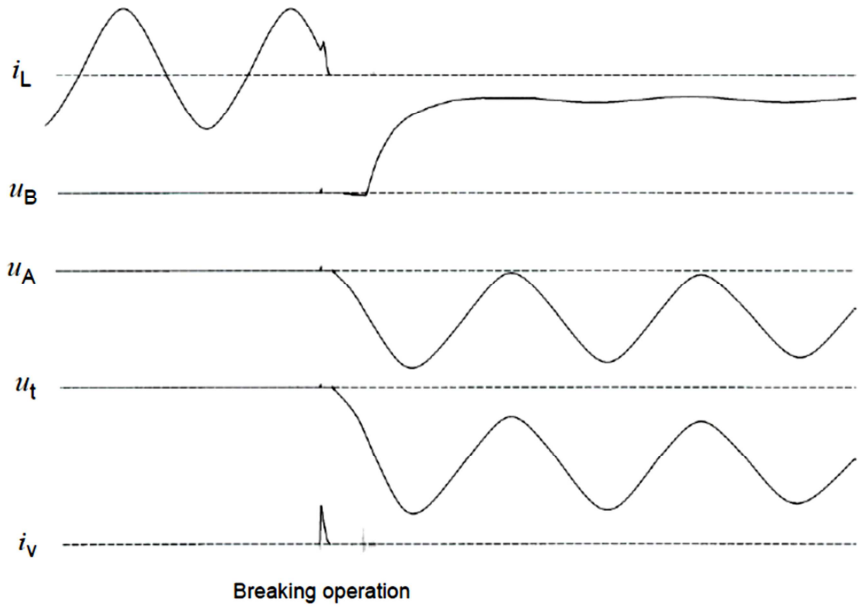


Figure 4.9 - Current injection circuit, recovery voltage applied to both sides of the circuit - breaker (fig. G.7 of ANNEX G, IEC 62271-101)

5. PROJECT REQUIREMENTS

5.1. Present situation

Today CESI High Voltage Synthetic Laboratory allows to perform all tests on circuit-breakers up to 420 kV, as prescribed by IEC 62271-101 [3].

Such tests are the following:

- ✓ Short-circuit (terminal fault): test-duties T10, T30, T60, T100, $f.p.c.f. = 1.3 \div 1.5$.
- ✓ Out-of-phase test-duties OP1 (not mandatory) and OP2, $m.f.$ = 2.
- ✓ Capacitive current switching tests (lines, cables and capacitor banks) k_c = 1, 1.2, 1.4.
- ✓ Short-Line Fault (SLF) test-duties L90, L75.

Note: SLF test-duties are not included in this study, because this test needs a self-standing artificial line, that does not affect the oscillating circuit design.

5.2. Expected capabilities of the new laboratory

The new laboratory must perform the same tests of the current one, but at the next higher level of rated voltage, i.e. 550 kV.

5.2.1. Short-circuit conditions

As explained in 3.2.1, in this work a first-pole-to-clear factor equal to 1.3 (IEC) and equal to 1.5 (special applications) is taking into account.

5.2.2. Out-of-phase conditions

As explained in 3.2.2, in this condition circuit-breaker must operate with the double phase to ground voltage across its contact. So, in this work a multiplication factor ***m.f.*** equal to 2 is considered.

5.2.3. Capacitive current switching conditions

As explained in 3.2.3, if a 550 kV is considered, k_c = 1.4 must be applied and $V = 1.4 \cdot 550\ kV/\sqrt{3}$ is the maximum voltage value applicable to a 550 kV circuit-breaker under test.

5.3. Preliminary design

This work has been organized as follows:

- ✓ The existing 420 kV Synthetic Laboratory has been modeled, and the model has been validated by comparison with the actual current and voltage wave shapes measured during tests. Such wave shapes are available and reliable, because they are used by laboratory operators in their daily work. Typical wave shapes ("inherents") representing the dynamic response of the Laboratory circuit during a test are included in plant documentation (operators' manual).
  In fact, laboratory operators work using plant manuals in which wave shapes reporting are inserted. These wave shapes represent the real dynamic response of the Laboratory during tests.

- ✓ After the 420 kV laboratory model validation by 420 kV laboratory inherents, the model has been upgraded and modified in order to reach 550 kV laboratory performance.

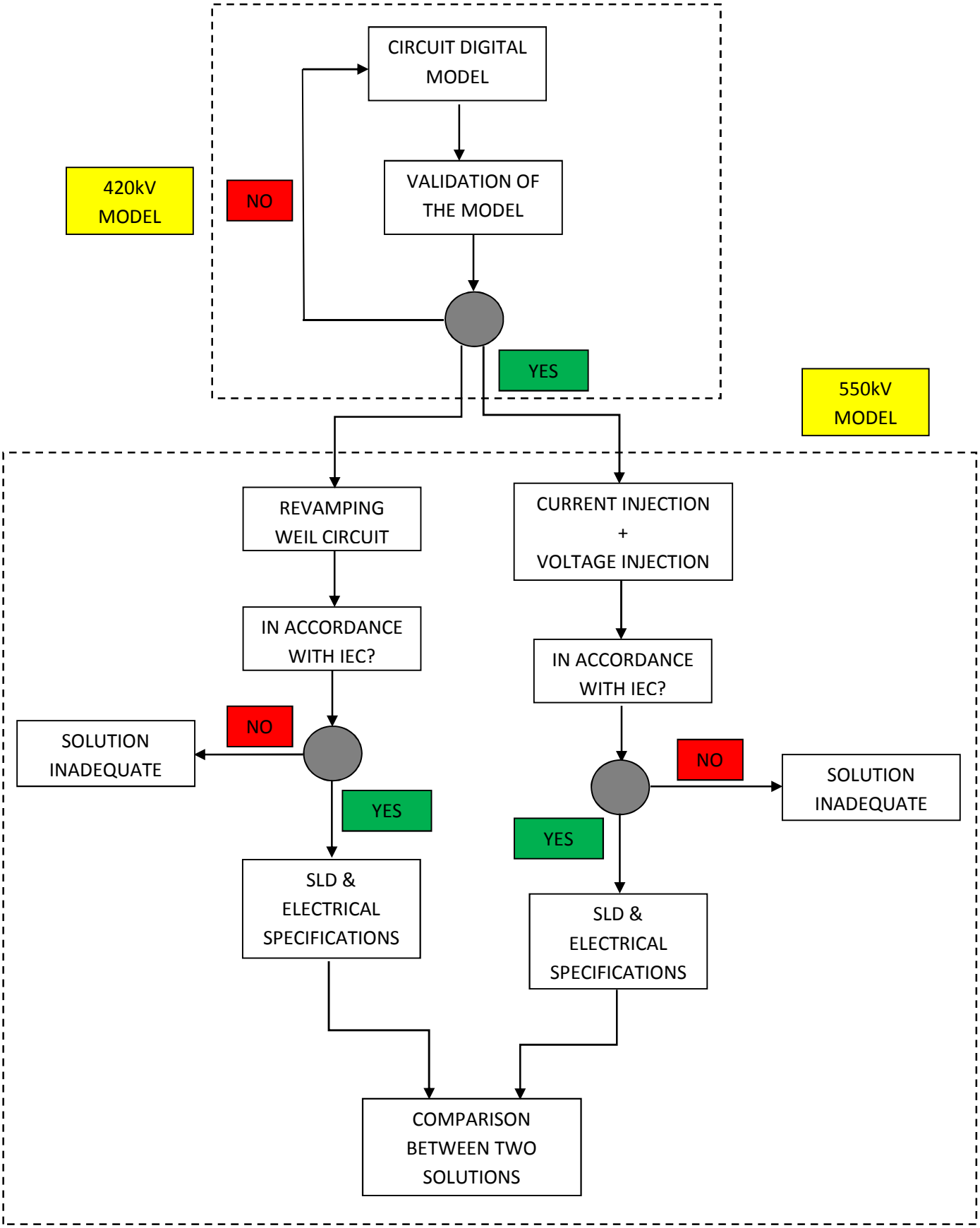
- ✓ New 550 kV inherents, calculated by means the model, have been compared with Standard requirements, after proper calibration of circuit elements.

- ✓ If the final results comply with Standard requirements, two documents are generated:

  - ➢ Single Line Diagram (SLD) reporting the circuit configuration and lumped parameters components and relevant values.
  - ➢ Preliminary Electrical specification, reporting list of major components and the range of their possible values (min/MAX).

- ✓ In conclusion, advantages and disadvantages of the possible circuit solutions are compared.

The following block diagram summarizes the above-described work flow.


420kV MODEL
CIRCUIT DIGITAL MODEL
VALIDATION OF THE MODEL
NO
YES
550kV MODEL
REVAMPING WEIL CIRCUIT
IN ACCORDANCE WITH IEC?
NO
SOLUTION INADEQUATE
YES
SLD & ELECTRICAL SPECIFICATIONS
CURRENT INJECTION + VOLTAGE INJECTION
IN ACCORDANCE WITH IEC?
NO
SOLUTION INADEQUATE
YES
SLD & ELECTRICAL SPECIFICATIONS
COMPARISON BETWEEN TWO SOLUTIONS

6. THE CESI HIGH VOLTAGE SYNTHETIC TEST LABORATORY

6.1. Present layout

The present CESI High Voltage Synthetic Test Laboratory allows short-circuit tests, out-of-phase tests and capacitive current switching tests on a single pole of a three-pole 420 kV, 63 kA circuit-breaker, with first-pole-to-clear factor (f.p.c.f.) 1.3 ÷ 1.5, multiplication factor $m.f.$ = 2 and k_c = 1.4 respectively (single-phase tests).
The majority of short-circuit, out-of-phase and single-phase or double-phase fault tests, and all short-line fault tests, are performed with a current injection method using the parallel circuit (see *Fig.4.1*), but it is possible to perform tests with voltage injection method using the series circuit (see *Fig.4.3*) or with circuits that combine the two testing methods (see *Fig.4.6*).
Depending on standards requirements, 2p or 4p Transient Recovery Voltages (TRV) may be applied.
The current injection circuit is mandatory when performing Short-Line-Fault tests or Short-circuit tests with initial TRV (ITRV).
Depending on the rated voltage of the circuit-breaker, capacitive current switching tests may be performed with direct test, with synthetic tests or a combination of both.

CESI Synthetic Laboratory consists of 5 parts:

- Current circuit
- High Voltage oscillating circuit
- Voltage circuit for making operation
- Auxiliary circuit-breakers hall
- Test Bay

Main components of each part are described below.

6.1.1. Current circuit

Test current at power frequency may be supplied by a short-circuit generator + short-circuit power transformers or, in alternative, by short-circuit power transformers supplied by the utility (ENEL) grid at 220 kV.
Maximum available short-circuit power is 1000 MVA by short-circuit generator 50/60 Hz or 1125 MVA by ENEL grid at 50 Hz. The two power sources can’t be used together.

Figure on next page represent the simplified SLD of the current circuit.

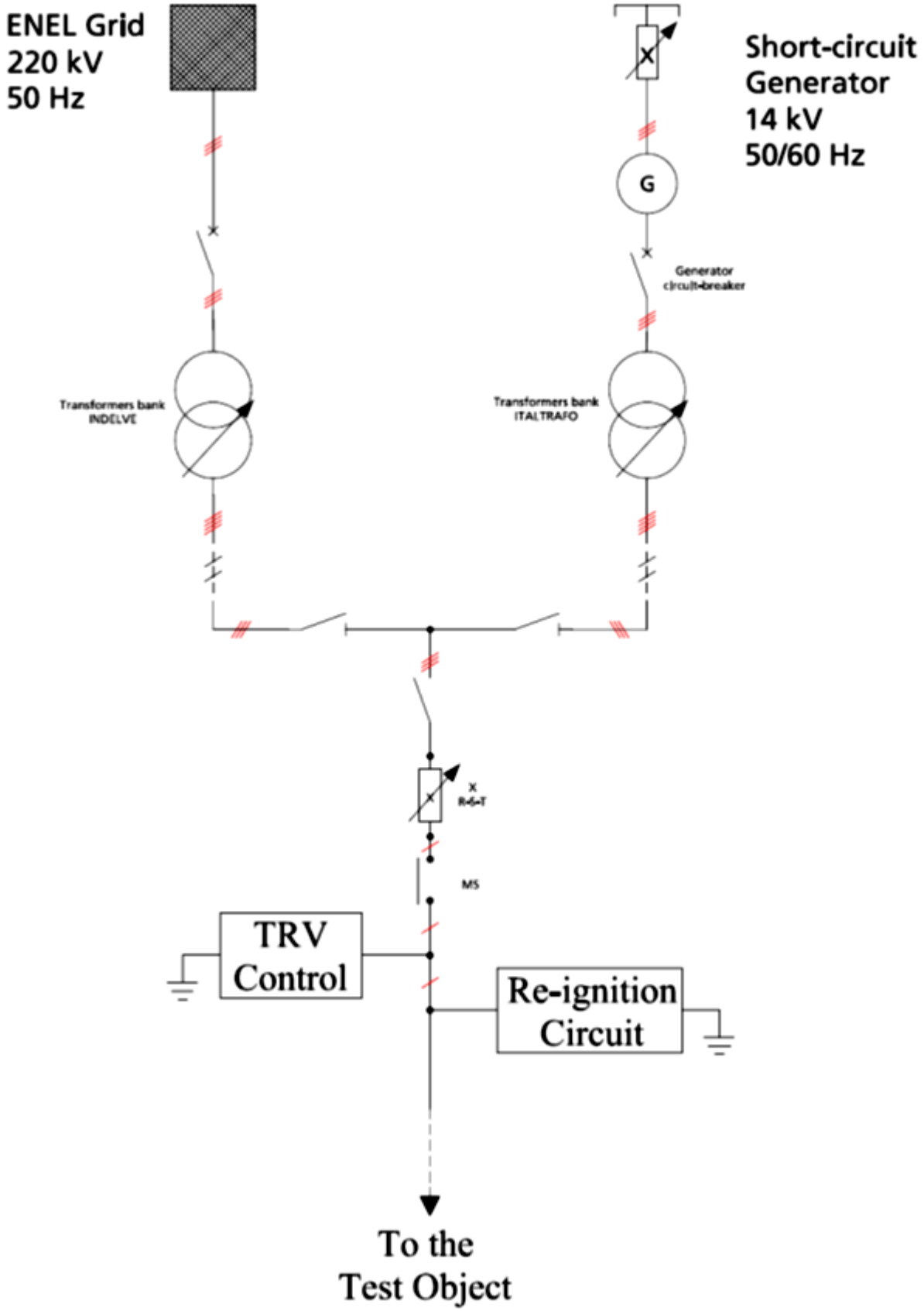


Figure 6.1 - Current circuit Single Line Diagram

Rated insulation level:

- LIWV (Lightning Impulse Withstand Voltage) (1.2/50 µs): 325 kV
- SIWV (Switching Impulse Withstand Voltage) (250/2500 µs): 200 kV
- A.C. voltage: 72 kV

The circuit consists of:

- reactor banks for the regulation of the test current
- capacitor/resistor banks for the control of the TRV of the current circuit
- apparatus to prolong the arcing time of the circuit-breaker under test (re-ignition circuits)
- making switch (MS)

6.1.2. High Voltage oscillating circuit

Rated insulation level:

- LIWV (1.2/50 µs): 1200 kV
- SIWV (250/2500 µs): 1000 kV
- D.C. voltage: 550 kV for 10 min

The circuit consists of :

- DC charging system
- main capacitor bank C_h
- spark-gap
- reactors bank L_h to control the di/dt of the injected current
- resistor – capacitor - reactor banks C_2,C_1, C_0, C_3 – R_1, R_2, R_0 –L_0 to control the TRV (2p or 4p)
- reactors bank $L_{50/60}$ to obtain an oscillating A.C. recovery voltage

6.1.3. Voltage circuit for making operation

The circuit consists of:

- MV/MV transformer to control the test voltage
- MV/HV transformer (named KOC) for the application of the A.C. test voltage to both the circuit-breaker under test and the synthetic making device
- RC branch to supply the **I**nitial **T**ransient **M**aking **C**urrent (ITMC)

6.1.4. Auxiliary circuit-breaker hall

In this area are located:

- auxiliary circuit-breaker
- synthetic making device (FMD) and a relevant circuit-breaker, named “saving breaker”, to shunt FMD 20 ms after current making

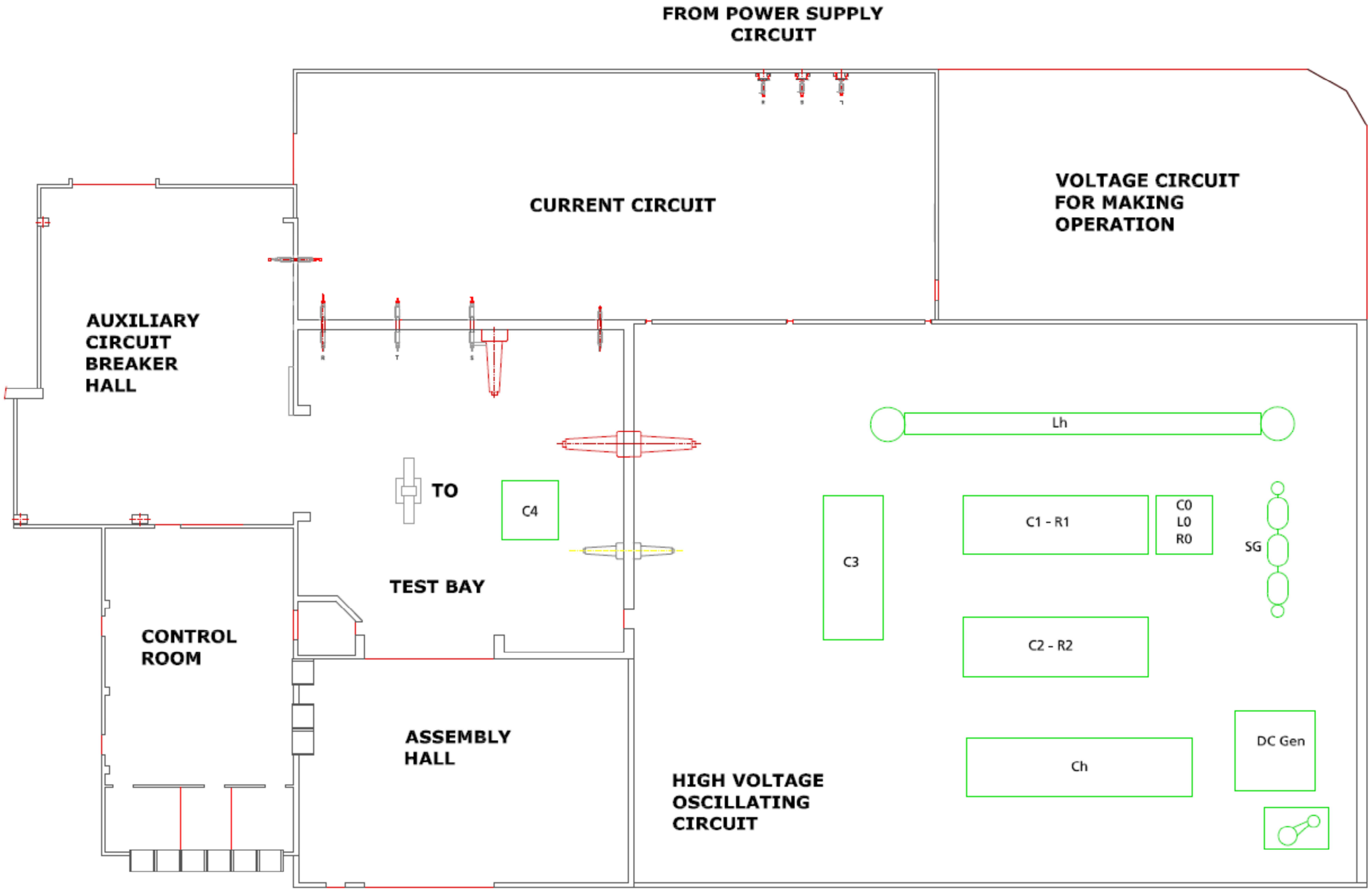
6.1.5. Test Bay

Circuit-breaker under test (T.O. or E.U.T.) is installed in this area, that is connected to the terminals of Current circuit and High Voltage oscillating circuit.

A movable bank of capacitor C_4 may be connected to the circuit-breaker to control the time-delay (t_d) of the TRV if necessary.
In this area the devices (shunts, RCR divider) are installed to measure the test currents and test voltages quantities.

Layout of the CESI High Power Synthetic Laboratory that represents the disposition of main components located in Laboratory is represented on next page.

6.2. CESI Synthetic Laboratory present layout



6.3. Rated characteristics of the main components of the High Voltage oscillating circuit

6.3.1. Main capacitor bank C_h

N°of sets:10
Max capacitance of each set: 130.55 µF
Max capacitance with 10 sets in series: 13.05 µF
Max charging voltage: 550 kV D.C.
In Table 6.1 below, the main characteristics of the unit of capacitor that form the bank are summarized.

Table 6.1 - Main capacitor bank C_h

Unit of capacitor	Charging voltage	Insulation level (SIWV)	Power frequency withstand voltage 50/60 Hz [KV_{rms}]					
[µF]	[kV D.C.]	[kV]	Continuously	100ms	200ms	1s	1min	30min
2.3	55	100	12.35/11.3	33.5	30.4	25.8	19.7	17.5/16
4.75	55	55	8.75/6	24	21.8	18.5	14.2	12.3/11.3

6.3.2. Capacitor banks C_1 and C_2

The two banks are identical.
Each bank consists of
N°of sets:10
Max capacitance of each set: 31.175 µF
Max capacitance with 10 sets in series: 3,175 µF
C_2 bank is insulated from ground for a SIWV equal to 800 kV.
In Table 6.2 below the main characteristics of the unit of capacitors that form each bank are summarized.

Table 6.2 - Capacitor banks C_1 and C_2

Unit of capacitor	Withstand voltage	Insulation level (SIWV)	Power frequency withstand voltage 50/60 Hz [KV_{rms}]					
[µF]	[kV D.C.]	[kV]	Continuously	100ms	200ms	1s	1min	30min
2.3	55	100	12.35/11.3	33.5	30.4	25.8	19.7	17.5/16
1.0			15.2/13.9					
0.125								

6.3.3. Capacitor bank C_3

N°of sets:10
Max capacitance of each set: 3.875 µF
Max capacitance with 10 sets in series: 0.3875 µF
In Table 6.3 below, the main characteristics of the unit of capacitors that form the bank are summarized.

Table 6.3 - Capacitor bank C_3

Unit of capacitor	Withstand voltage	Insulation level (SIWV)	Power frequency withstand voltage 50/60 Hz [KV_{rms}]					
[µF]	[kV D.C.]	[kV]	Continuously	100ms	200ms	1s	1min	30min
1	55	100	15.2/13.9	33.5	30.4	25.8	19.7	17.5/16
0.125								

6.3.4. Capacitor bank C_0

N°of sets: 4
Max capacitance of each set: 10.475 µF
Max capacitance with 4 sets in series: 2.62 µF
In the following Table 6.4 are summarized the main characteristics of the unit of capacitors that form the bank.

Table 6.4 - Capacitor bank C_0

Unit of capacitor	Withstand voltage	Insulation level (SIWV)	Power frequency withstand voltage 50/60 Hz [KV_{rms}]					
[µF]	[kV D.C.]	[kV]	Continuously	100ms	200ms	1s	1min	30min
2.3	55	100	12.35/11.3	33.5	30.4	25.8	19.7	17.5/16
1			15.2/13.9					
0.125								

6.3.5. Reactor bank L_h

The reactor bank consists of 11 reactors.
Max inductance: 210 mH
Rated characteristics of each reactor are shown in Table 6.5 below.

Table 6.5 - Reactor bank L_h

Quantity	Rated inductance	Peak withstand current at 350 Hz	Lightning impulse withstand voltage (1.2/50µs)	Withstand voltage at 350 Hz	Rated time constant at 500 Hz
N°	[mH]	[kA]	[kV]	[kV_{rms}]	[ms]
1	0.25	32	50	12.5	70
1	0.5	32	80	25	70
1	1	32	150	50	70
2	2	32	300	100	70
1	5	25	1100	390	70
1	10	23	1100	390	70
2	20	12.5	1100	390	60
1	50	5	1100	390	60
1	100	2.5	1100	390	50

6.3.6. Reactor bank L_0

The reactor bank consists of 8 reactors. Characteristics are as in Table 6.6:

Table 6.6 - Reactor bank L_0

Quantity	Rated inductance	Peak withstand current at 350 Hz	Lightning impulse withstand voltage (1.2/50µs)	Withstand voltage at 500 Hz	Rated time constant at 500 Hz
N°	[mH]	[kA]	[kV]	[kV_{rms}]	[ms]
1	0.25	20	60	15.5	20
1	0.5	20	60	31	20
1	1	20	120	63	20
2	2	20	220	125	20
1	5	15	400	235	20
1	10	7.5	400	235	20
1	20	3.75	400	235	20

6.3.7. Resistor banks R_1 and R_2

Each bank consists of the following 8 resistive modules:
800 Ω, 400 Ω, 200 Ω, 100 Ω, 50 Ω, 25 Ω, 12.5 Ω, 6.25 Ω

6.3.8. Resistor bank R_0

The bank consists of resistive modules of different values that can be connected in series, parallel or series-parallel.

- Minimum available value: 6.25 Ω
- Maximum available value: 13 kΩ approx.

6.3.9. Reactor bank $L_{50\text{-}60/pf}$

The bank consists of 6 reactors that can be connected in series, parallel or series-parallel.
Rated characteristics of each reactor:

- Inductance: 1 H
- LIWV (1.2/50µs): 750 kV
- Short-time withstand current: 400 A x 1s / 1000 A_p

7. HIGH VOLTAGE OSCILLATING CIRCUIT DIGITAL MODELS

A model of the oscillating circuit was developed using ATP (Alternative Transient Program, http://www.ece.mtu.edu/atp/), a widely used software packages for circuit simulation. Comparison between the TRV measured in Laboratory during a test session and the same calculated with ATP has been performed in order to validate the ATP circuit models.

The following test conditions, relevant to 420 kV circuit-breaker, have been considered:

- Short-Circuit 2 parameters TRV
  - ✓ *Test - duty T10 $I = 6.3\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.5*
  - ✓ *Test - duty T30 $I = 18.9\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.5*

- Short-Circuit 4 parameters TRV
  - ✓ *Test - duty T60 $I = 30\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.3*
  - ✓ *Test - duty T60 $I = 37.8\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.3*
  - ✓ *Test - duty T60 $I = 37.8\ kA$ $f = 60\ Hz$ f.p.c.f. = 1.5*
  - ✓ *Test - duty T100 $I = 40\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.3*
  - ✓ *Test - duty T100 $I = 50\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.5*
  - ✓ *Test - duty T100 $I = 63\ kA$ $f = 60\ Hz$ f.p.c.f. = 1.5*

- Out-of-phase
  - ✓ *Test - duty OP2 $I = 15.75\ kA$ $f = 50\ Hz$ m.f. = 2*

- Capacitive current switching
  - ✓ *Test - duty LC2 $I = 400\ A$ $f = 50\ Hz$ $k_c = 1.4$*

Results of model validation are shown below.

7.1. Short-Circuit 2p TRV

The test circuit diagram and the equivalent ATP digital model are shown in *Fig. 7.1* and *7.2* respectively.

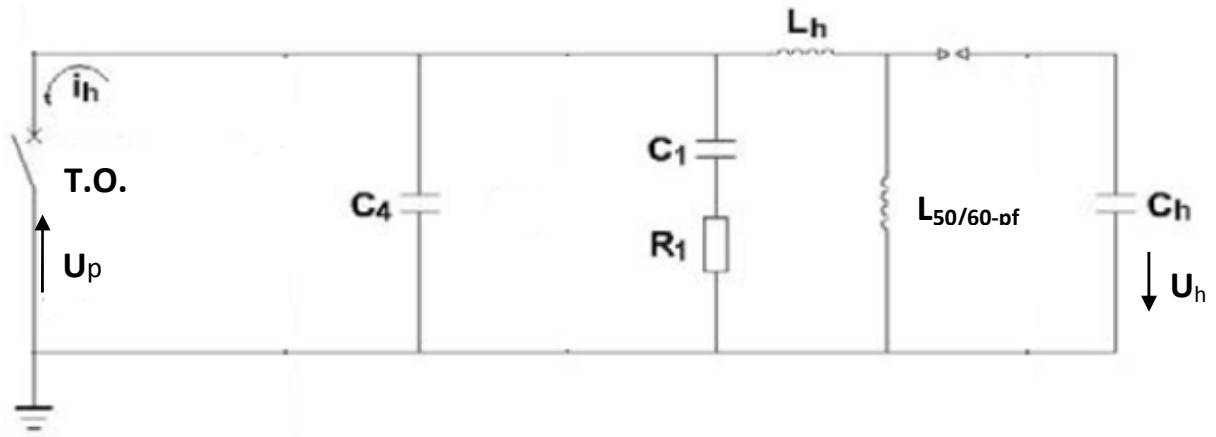


Figure 7.1 - Test circuit diagram

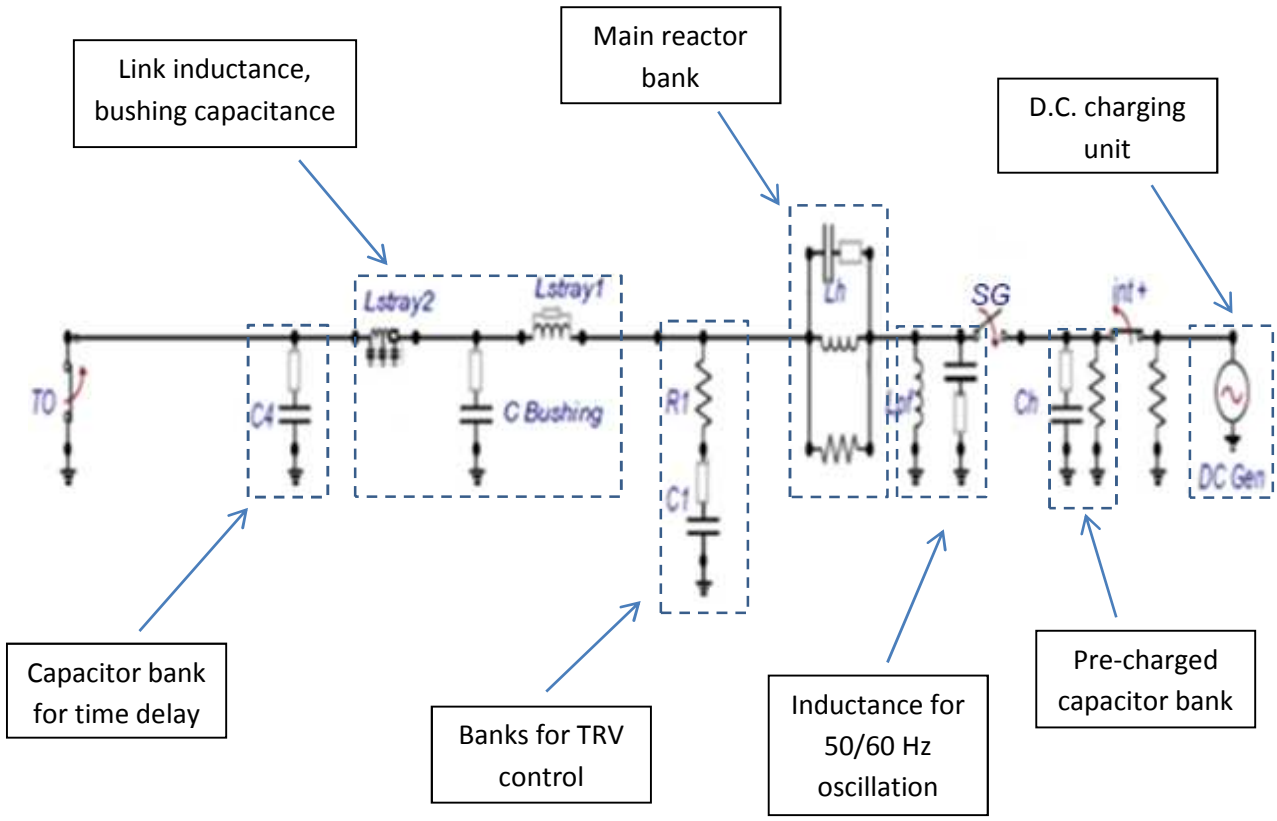


Figure 7.2 - ATP digital model

7.1.1. *Test - duty T10: I = 5.7 kA f = 50 Hz f.p.c.f. = 1.5*

Test circuit parameters

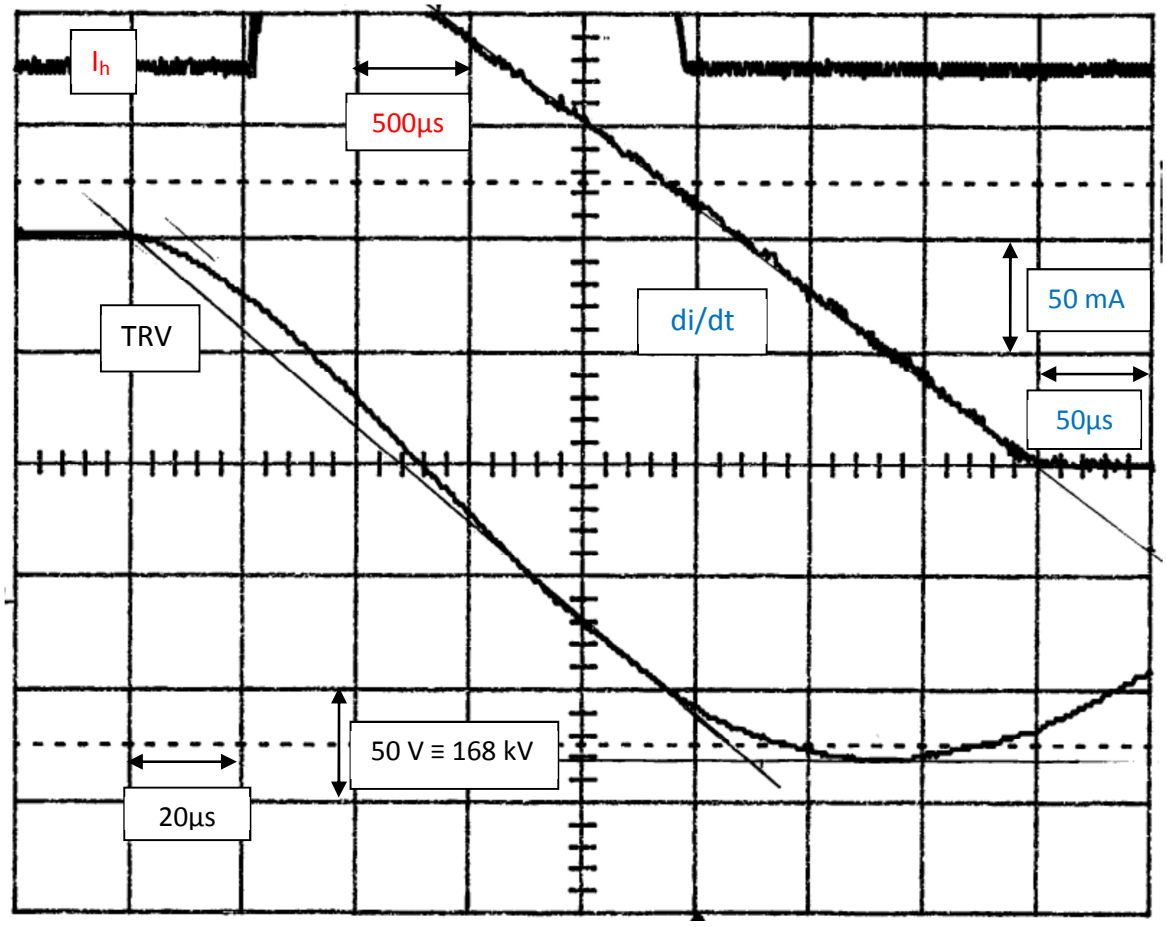
C_h [µF]	L_h [mH]	L_{pf} [mH]	C_1 [µF]	R_1 [Ω]	C_4 [µF]
2.13	185	5000	0.007	4365	0.004

Comparison between Laboratory TRV and ATP digital model

	U_h [kV]	Injected current (i_h)		TRV	
		f_h [Hz]	di/dt [A/µs]	U_c [kV]	t_3 [µs]
Laboratory TRV	487	260	2.53	785	112
ATP model	506	257	2.53	770	108
% difference		-1.2	-	-1.9	-3.6

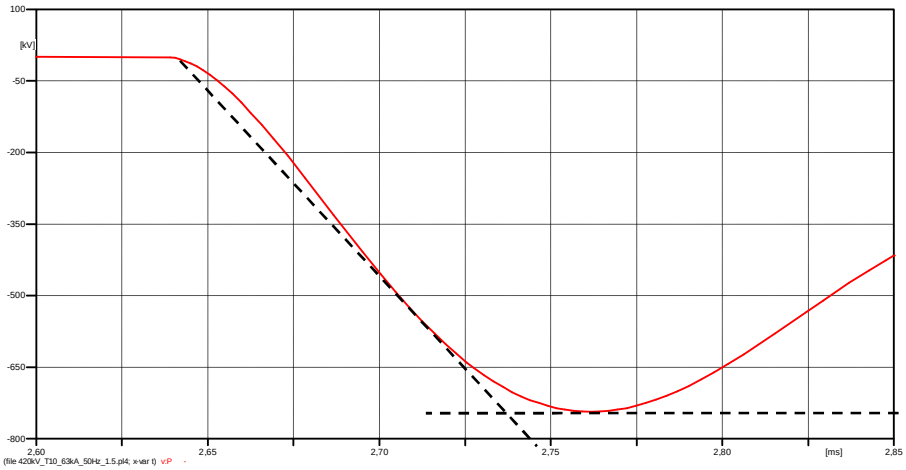
LABORATORY TRV

Figure below represents a real TRV wave shape measured during a test-duty:

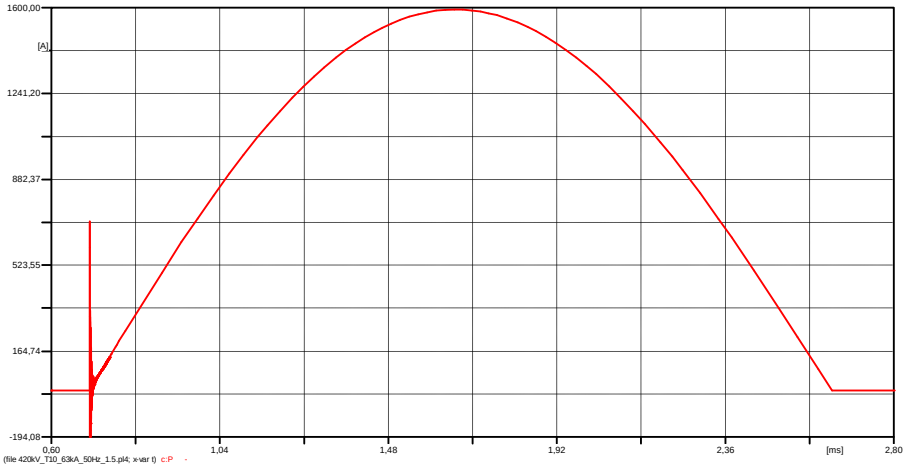


ATP DIGITAL MODEL

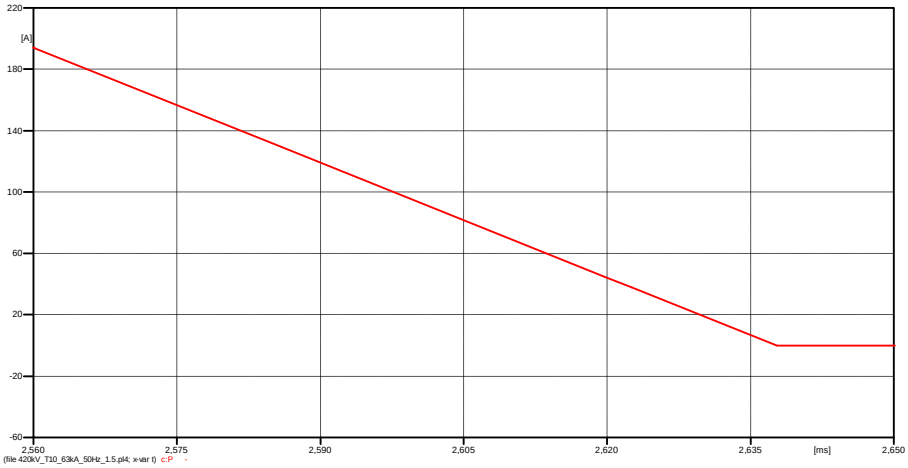
Figures below show results obtained simulating circuit represented in *Fig.7.2.*



TRV



Injected current i_h



di/dt at zero of injected current i_h

7.1.2. *Test - duty T30: I = 18.9 kA f = 50 Hz f.p.c.f. = 1.5*

Test circuit parameters

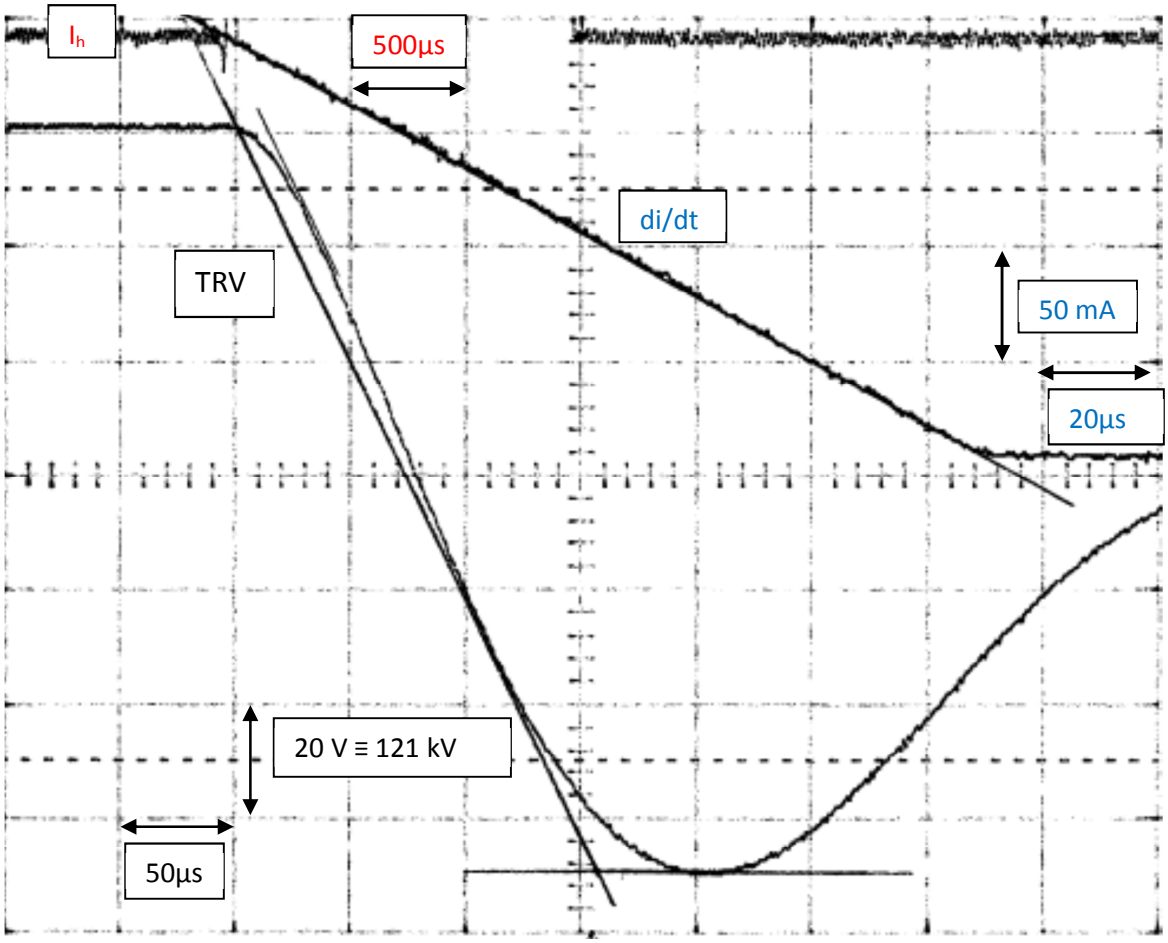
C_h [µF]	L_h [mH]	L_{pf} [mH]	C_1 [µF]	R_1 [Ω]	C_4 [µF]
4.03	62	3000	0.075	600	0.021

Comparison between Laboratory TRV and ATP digital model

	U_h [kV]	Injected current (i_h)		TRV	
		f_h [Hz]	di/dt [A/µs]	U_c [kV]	t_3 [µs]
Laboratory TRV	530	325	8.39	787	160
ATP model	545	320	8.39	752	165
% difference		-1.5	-	-4.4	3.1

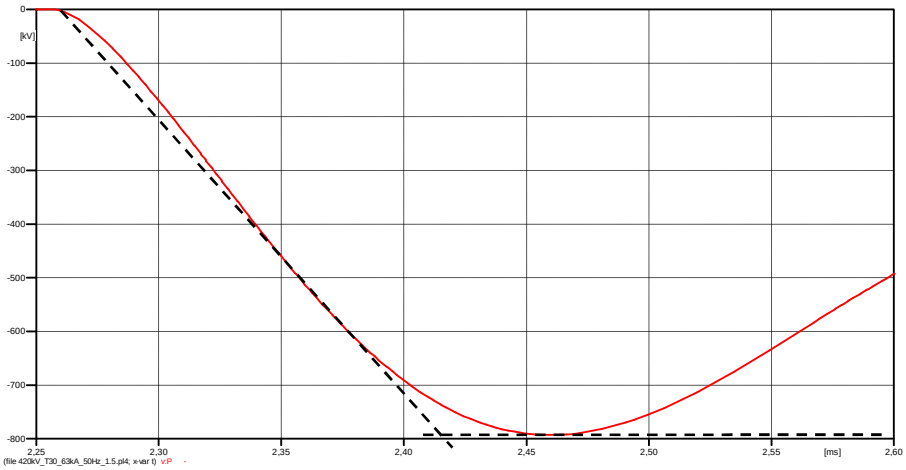
LABORATORY TRV

Figure below represents a real TRV wave shape measured during a test-duty:

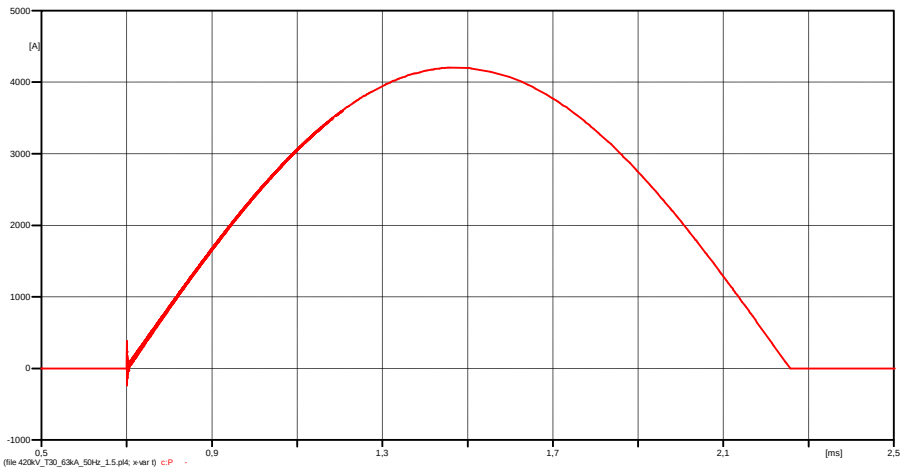


ATP DIGITAL MODEL

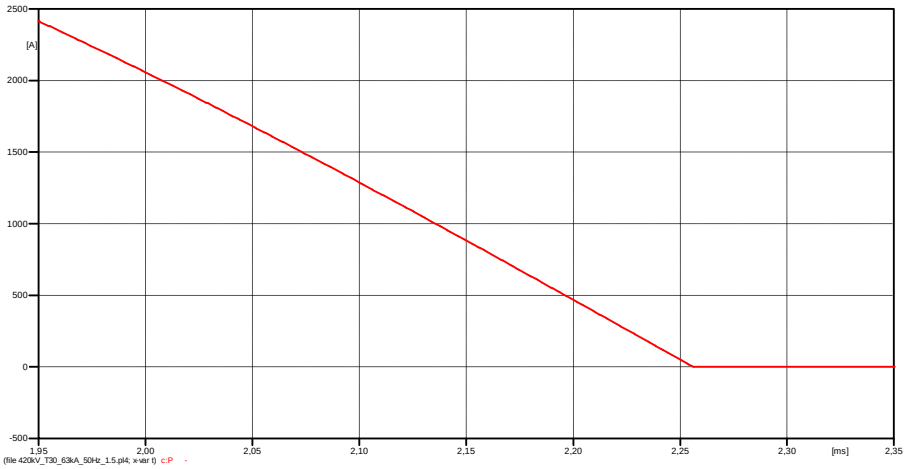
Figures below show results obtained simulating circuit represented in *Fig.7.2.*



TRV



Injected current i_h



di/dt at zero of injected current i_h

7.2. Short-Circuit 4p TRV

The test circuit diagram and the equivalent ATP digital model are shown in *Fig.7.3* and *7.4* respectively.

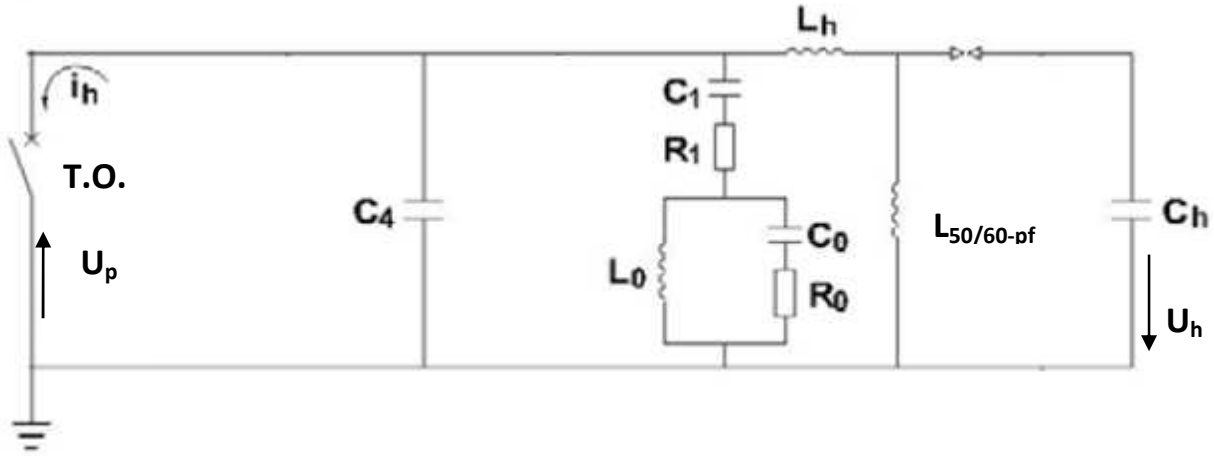


Figure 7.3 - Test circuit diagram

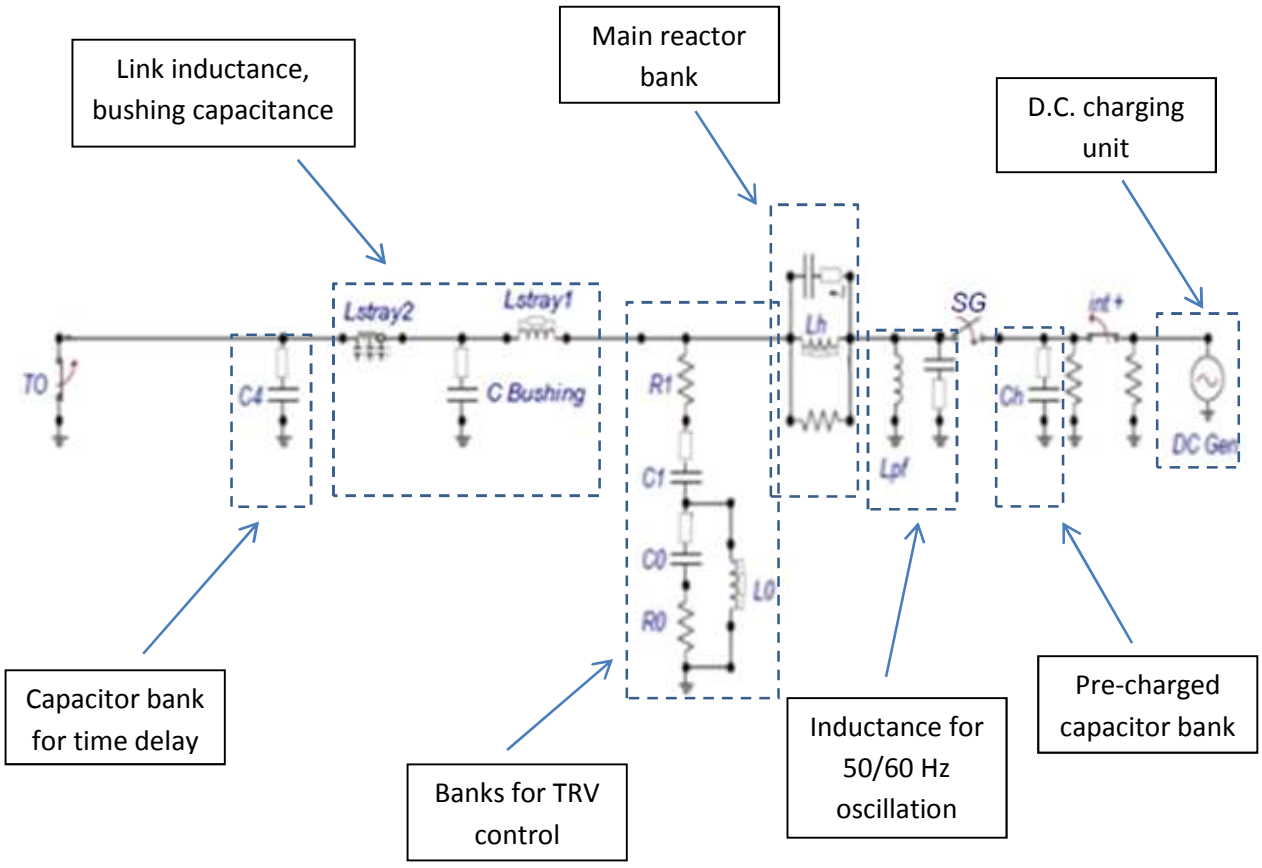


Figure 7.4 - ATP digital model

7.2.1. *Test - duty T60: I = 30 kA f = 50 Hz f.p.c.f. = 1.3*

Test circuit parameters

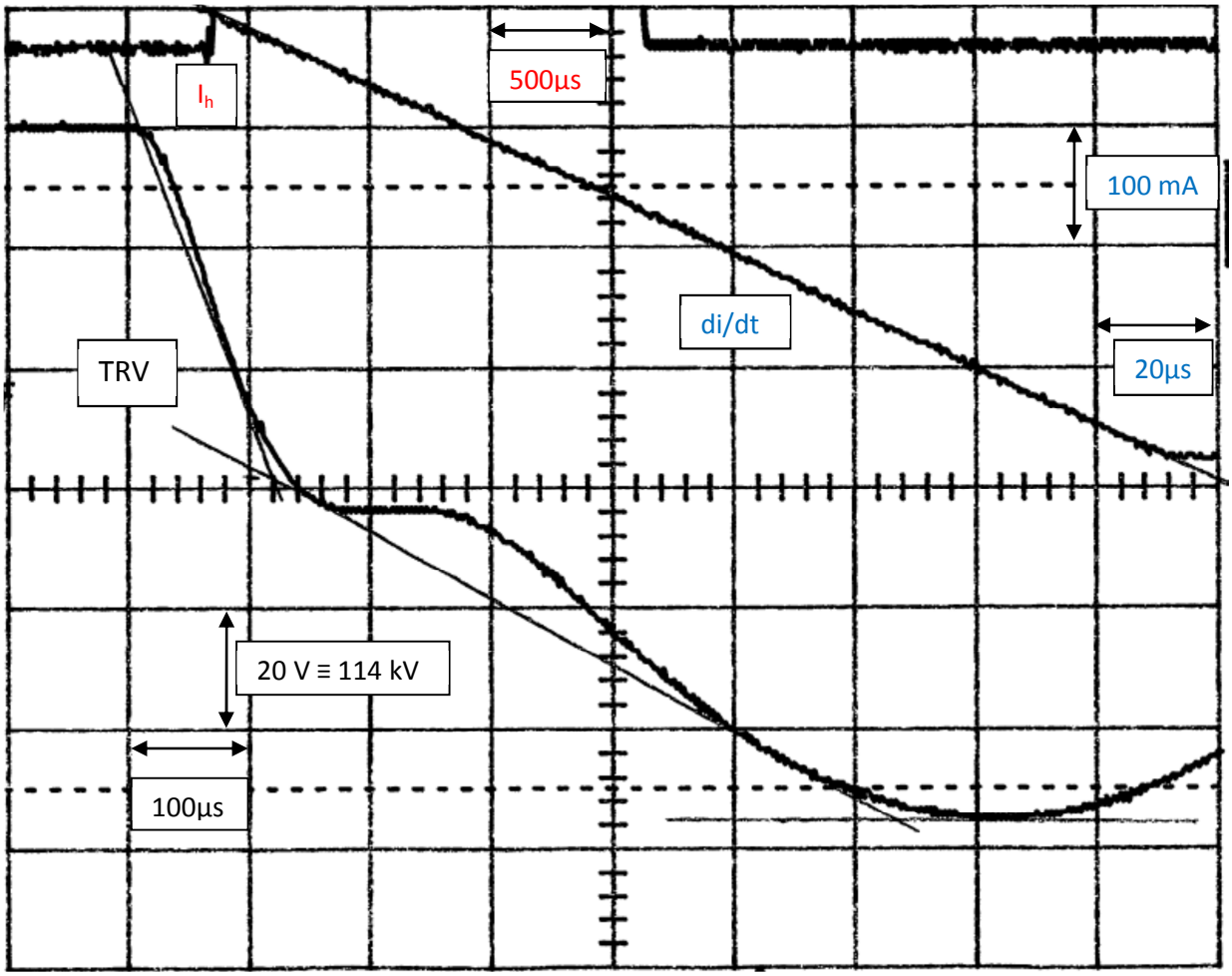
C_h [µF]	L_h [mH]	L_{pf} [mH]	C_1 [µF]	R_1 [Ω]	L_0 [mH]	C_0 [µF]	R_0 [Ω]	C_3 [µF]	C_4 [µF]
9.5	37	1000	0.9575	12.5	26	0.25	445.75	0.0625	0.021

Comparison between Laboratory TRV and ATP digital model

	U_h [kV]	Injected current (i_h)		TRV			
		f_h [Hz]	di/dt [A/µs]	U_1 [kV]	t_1 [µs]	U_c [kV]	t_2 [µs]
Laboratory TRV	524	276	13.32	334	111	670	627
ATP model	545	271	13.9	337	109	670	625
% difference		-1.8	4.3	0.8	-1.8	-	-0.3

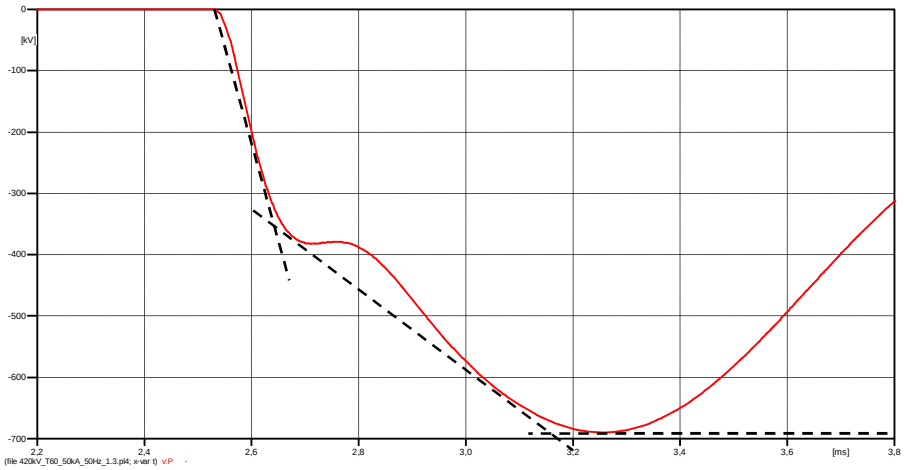
LABORATORY TRV

Figure below represents a real TRV wave shape measured during a test-duty:

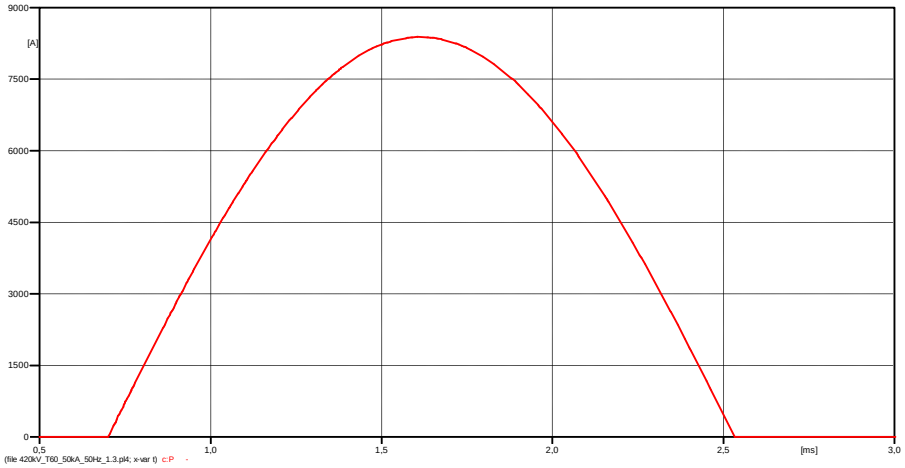


ATP DIGITAL MODEL

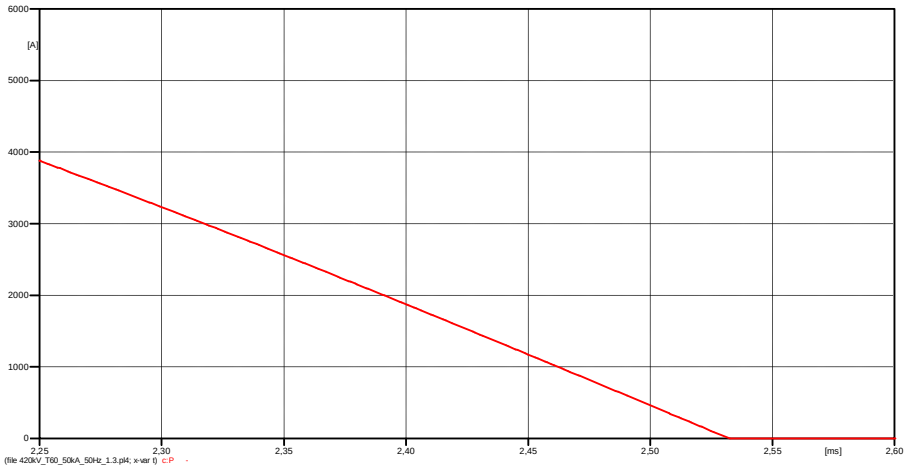
Figures below show results obtained simulating circuit represented in *Fig.7.4.*



TRV



Injected current i_h



di/dt at zero of injected current i_h

7.2.2. *Test - duty T60: I = 37.8 kA f = 60 Hz f.p.c.f. = 1.3*

Test circuit parameters

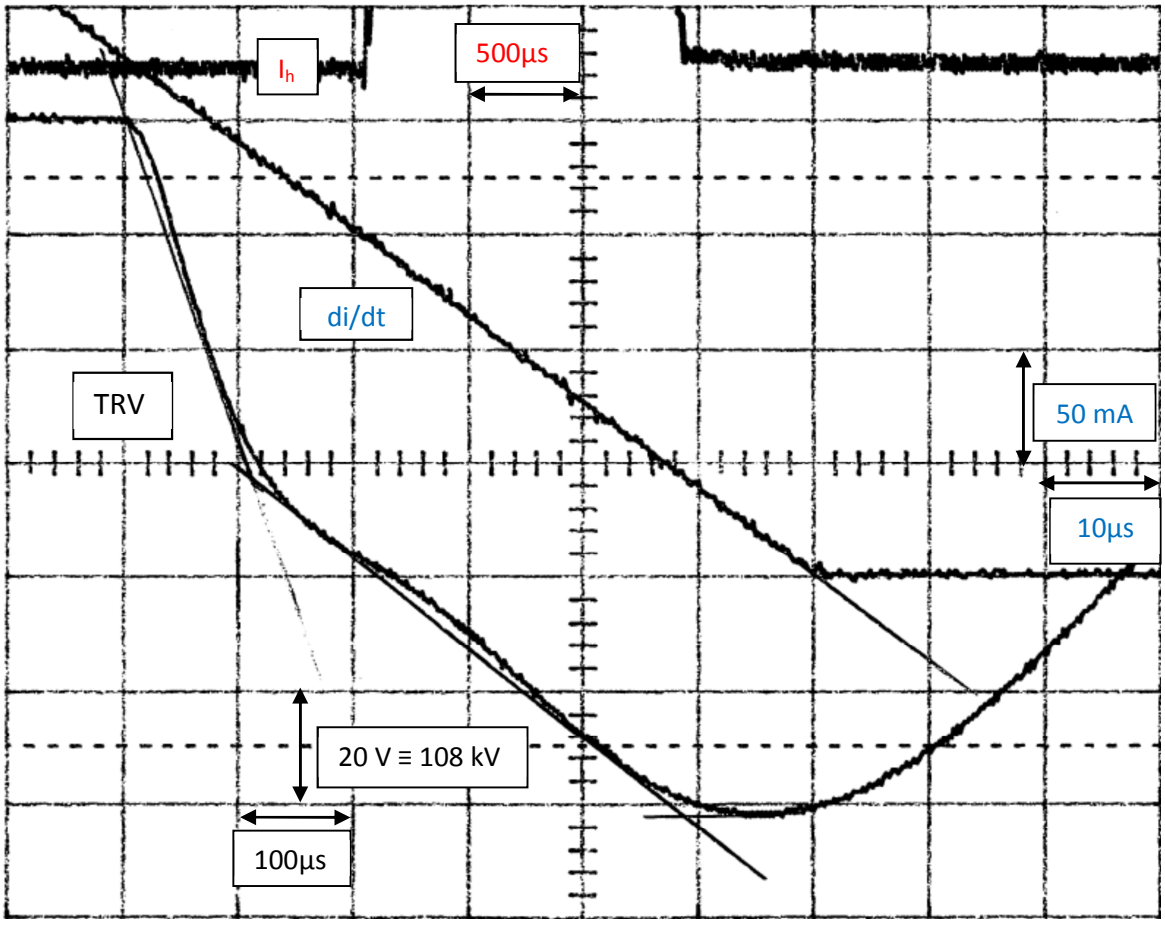
C_h [µF]	L_h [mH]	L_{pf} [mH]	C_1 [µF]	R_1 [Ω]	L_0 [mH]	C_0 [µF]	R_0 [Ω]	C_3 [µF]	C_4 [µF]
8.08	25	1000	0.9	6.25	15.5	0.41	233	0.0625	0.021

Comparison between Laboratory TRV and ATP digital model

	U_h [kV]	Injected current (i_h)		TRV			
		f_h [Hz]	di/dt [A/µs]	U_1 [kV]	t_1 [µs]	U_c [kV]	t_2 [µs]
Laboratory TRV	525	364	20.15	345	113	655	497
ATP model	525	355	19.7	340	108	643	487
% difference		-2.4	-2.2	-1.4	-4.4	-1.8	-2

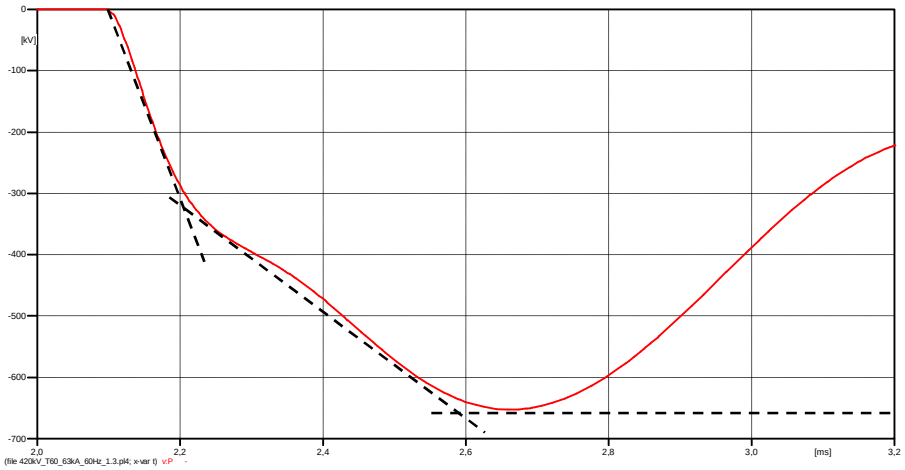
LABORATORY TRV

Figure below represents a real TRV wave shape measured during a test-duty:

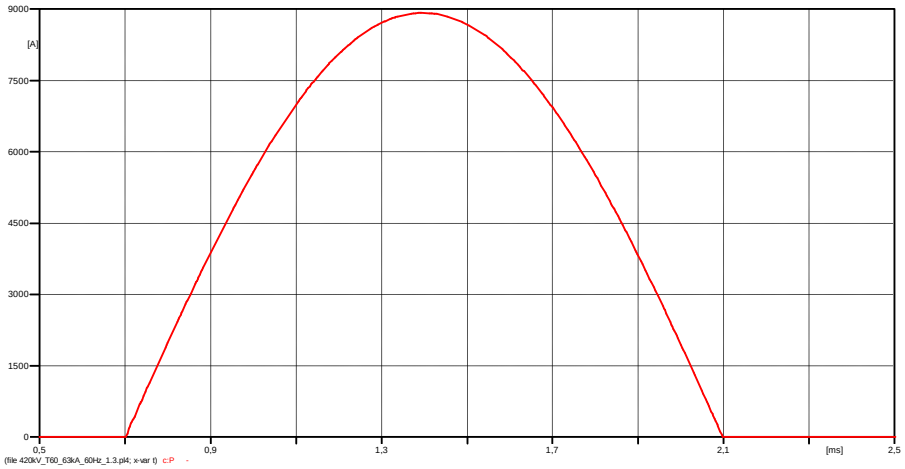


ATP DIGITAL MODEL

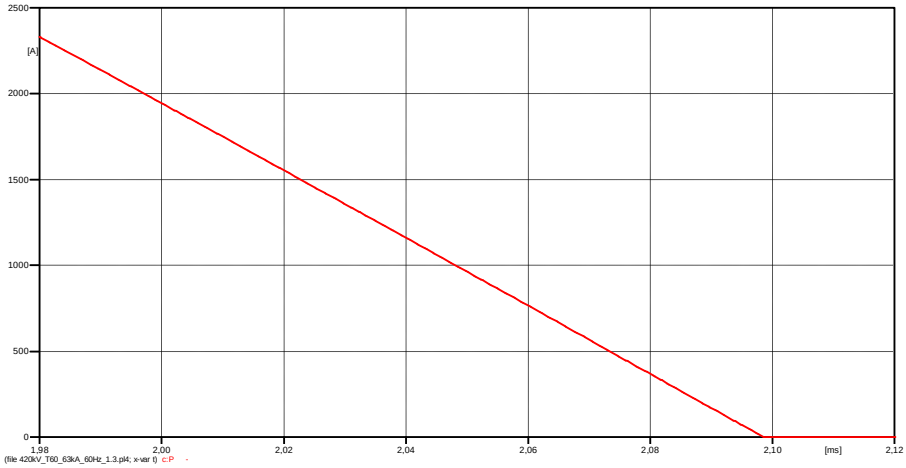
Figures below show results obtained simulating circuit represented in *Fig.7.4.*



TRV



Injected current i_h



di/dt at zero of injected current i_h

7.2.3. *Test - duty T60: I = 37.8 kA f = 60 Hz f.p.c.f. = 1.5*

Test circuit parameters

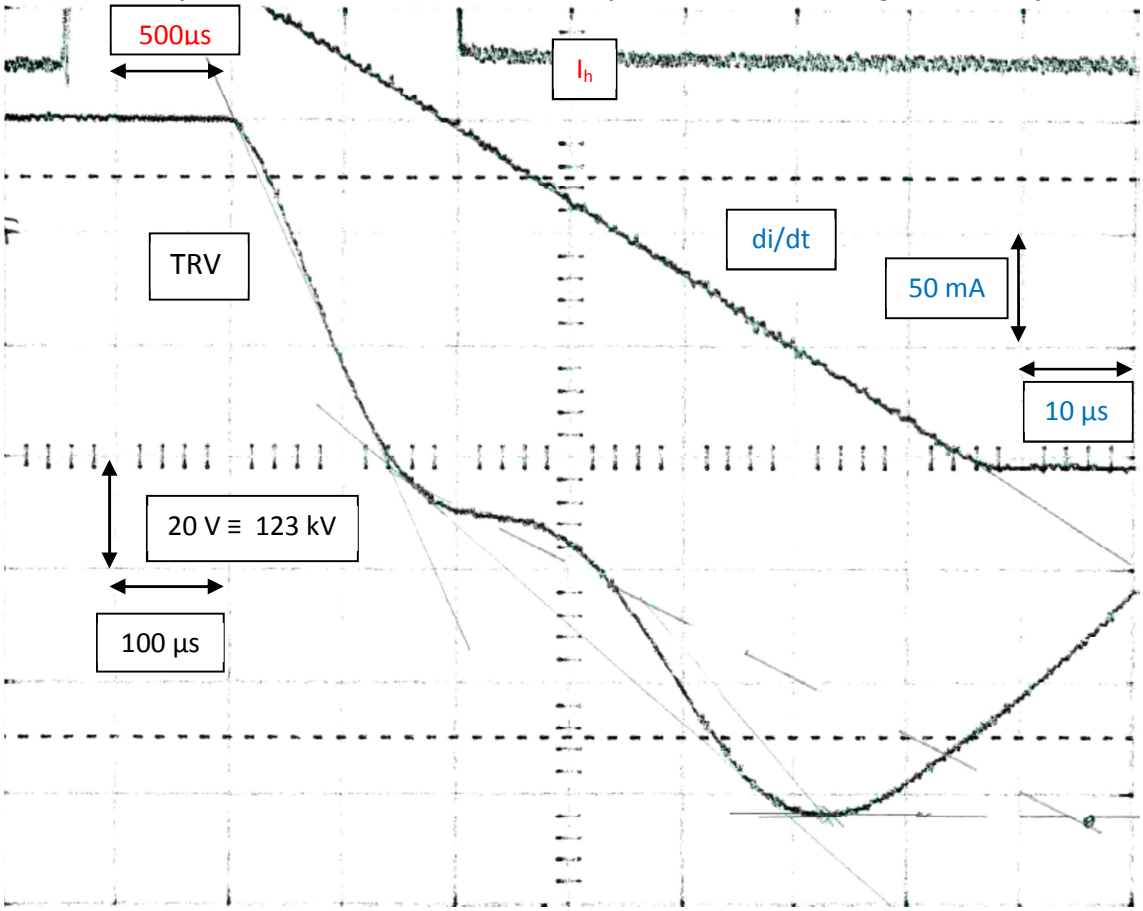
C_h [μF]	L_h [mH]	L_{pf} [mH]	C_1 [μF]	R_1 [Ω]	L_0 [mH]	C_0 [μF]	R_0 [Ω]	C_3 [μF]	C_4 [μF]
12.8	25.5	660	0.91	12.5	10.75	0.375	60	0.0375	0.021

Comparison between Laboratory TRV and ATP digital model

	U_h [kV]	Injected current (i_h)		TRV			
		f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Laboratory TRV	525	290	20.15	380	130	763	495
ATP model	527	284	19.75	361	133	749	502
% difference		-2.1	-2	-5	2.3	-1.8	1.4

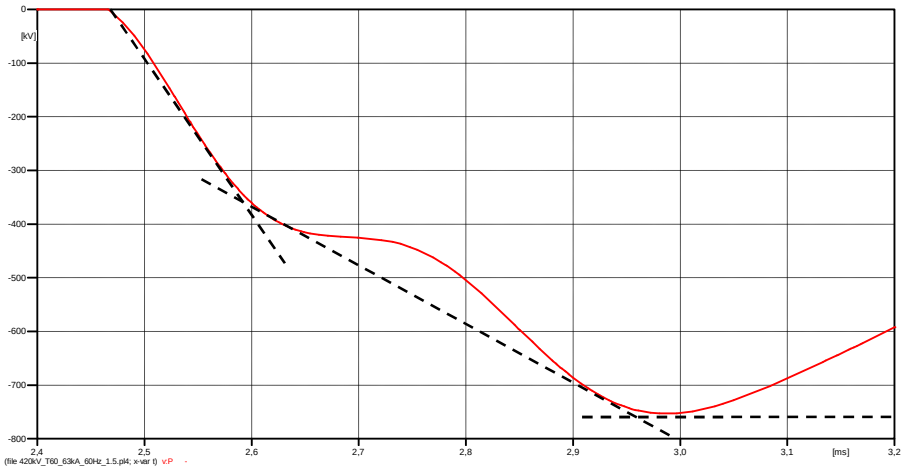
LABORATORY TRV

Figure below represents a real TRV wave shape measured during a test-duty:

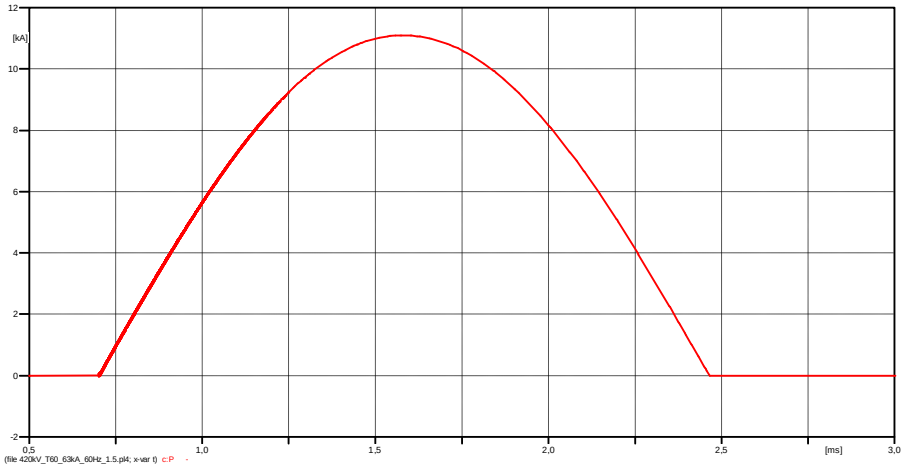


ATP DIGITAL MODEL

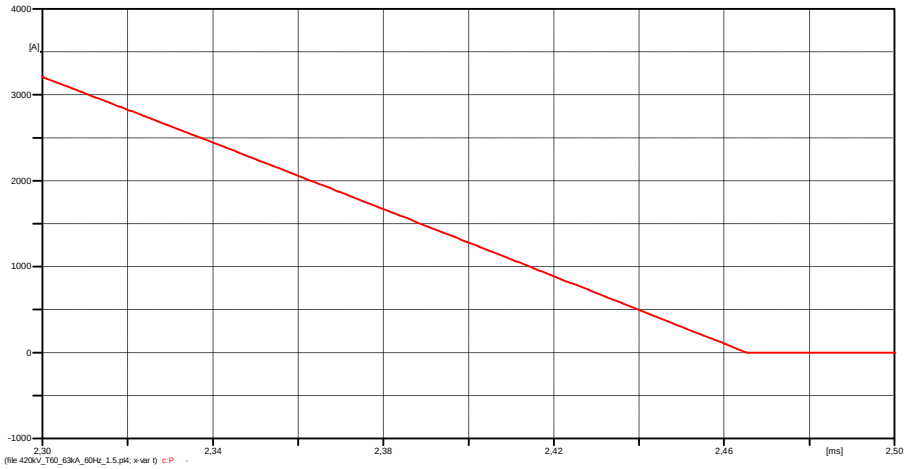
Figures below show results obtained simulating circuit represented in *Fig.7.4.*



TRV



Injected current i_h



di/dt at zero of injected current i_h

7.2.4. *Test - duty T100: I = 40 kA f = 50 Hz f.p.c.f. = 1.3*

Test circuit parameters

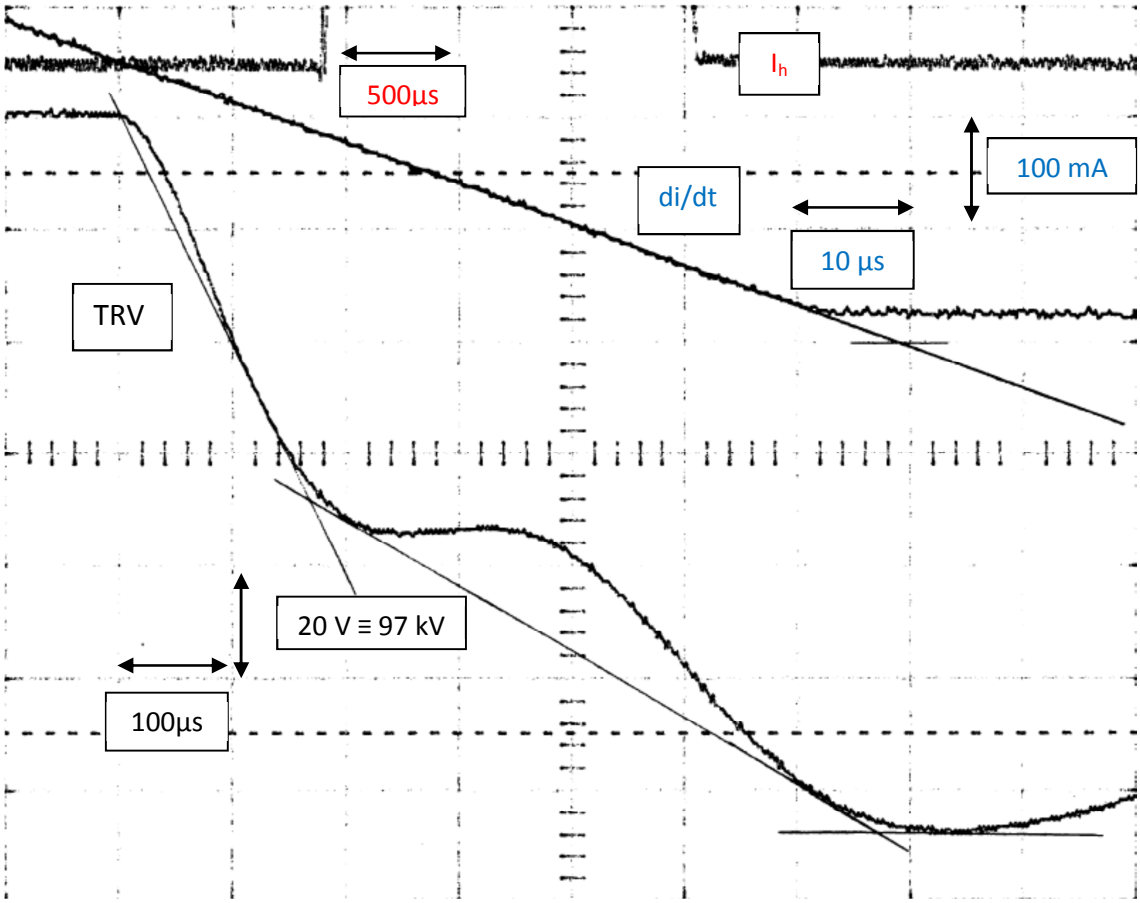
C_h [µF]	L_h [mH]	L_{pf} [mH]	C_1 [µF]	R_1 [Ω]	L_0 [mH]	C_0 [µF]	R_0 [Ω]	C_3 [µF]	C_4 [µF]
10.9	27.75	670	1.85	12.5	14.5	0.5	151	0.163	0.021

Comparison between Laboratory TRV and ATP digital model

	U_h [kV]	Injected current (i_h)		TRV			
		f_h [Hz]	di/dt [A/µs]	U_1 [kV]	t_1 [µs]	U_c [kV]	t_2 [µs]
Laboratory TRV	503	300	17.8	334	167	624	670
ATP model	508	293	17.5	339	175	613	700
% difference		-2.3	-1.7	1.5	4.7	-1.7	4.4

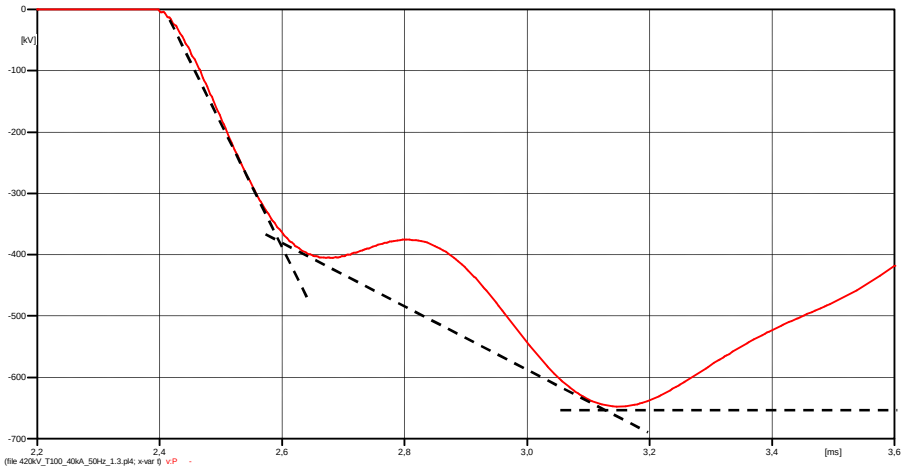
LABORATORY TRV

Figure below represents a real TRV wave shape measured during a test-duty:



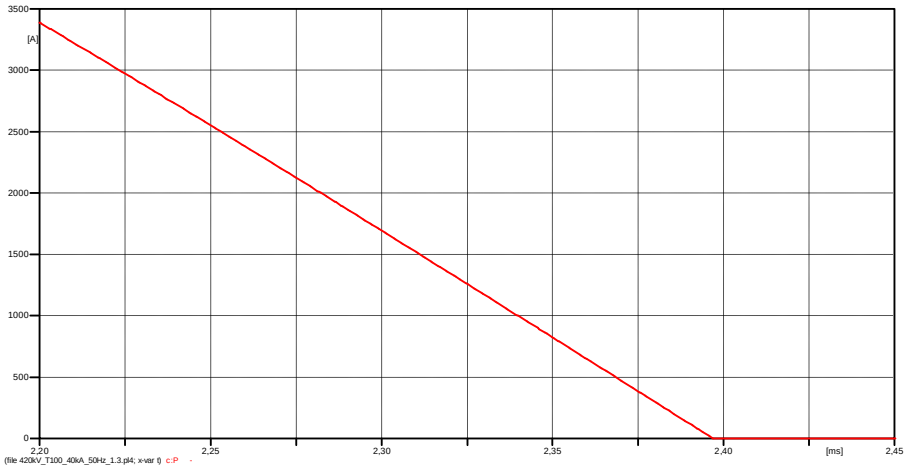
ATP DIGITAL MODEL

Figures below show results obtained simulating circuit represented in *Fig.7.4.*



TRV

Injected current i_h



di/dt at zero of injected current i_h

7.2.5. *Test - duty T100: I = 50 kA f = 50 Hz f.p.c.f. = 1.5*

Test circuit parameters

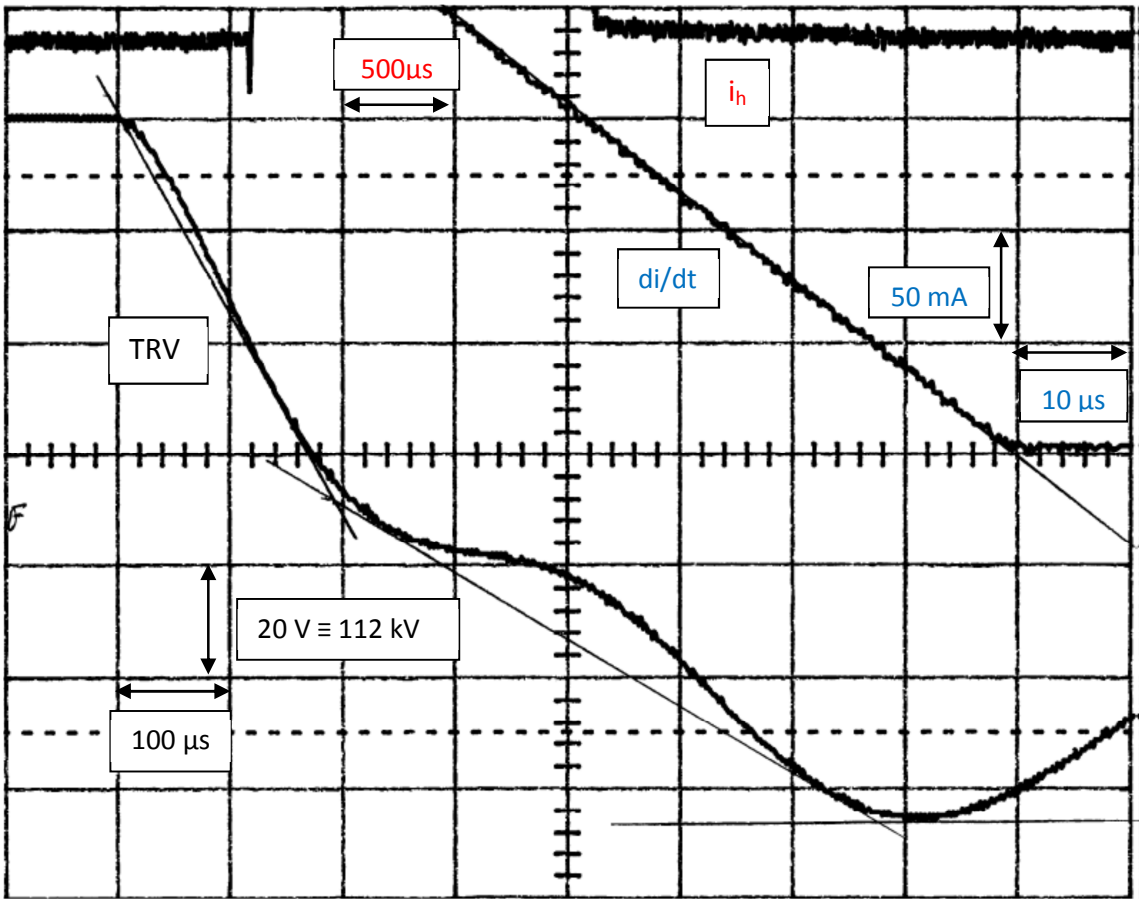
C_h [µF]	L_h [mH]	L_{pf} [mH]	C_1 [µF]	R_1 [Ω]	L_0 [mH]	C_0 [µF]	R_0 [Ω]	C_3 [µF]	C_4 [µF]
10.45	24	1000	1.8225	12.5	10.5	0.72	69.6	0.175	0.012

Comparison between Laboratory TRV and ATP digital model

	U_h [kV]	Injected current (i_h)		TRV			
		f_h [Hz]	di/dt [A/µs]	U_1 [kV]	t_1 [µs]	U_c [kV]	t_2 [µs]
Laboratory TRV	560	326	22.2	385	193	720	680
ATP model	565	321	22.9	385	190	712	700
% difference		-1.5	3.2	-	-1.5	-1.1	2.9

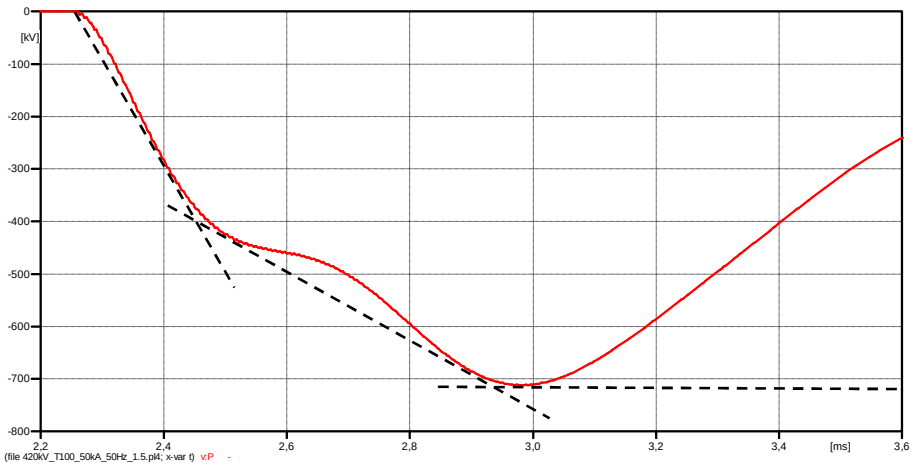
LABORATORY TRV

Figure below represents a real TRV wave shape measured during a test-duty:

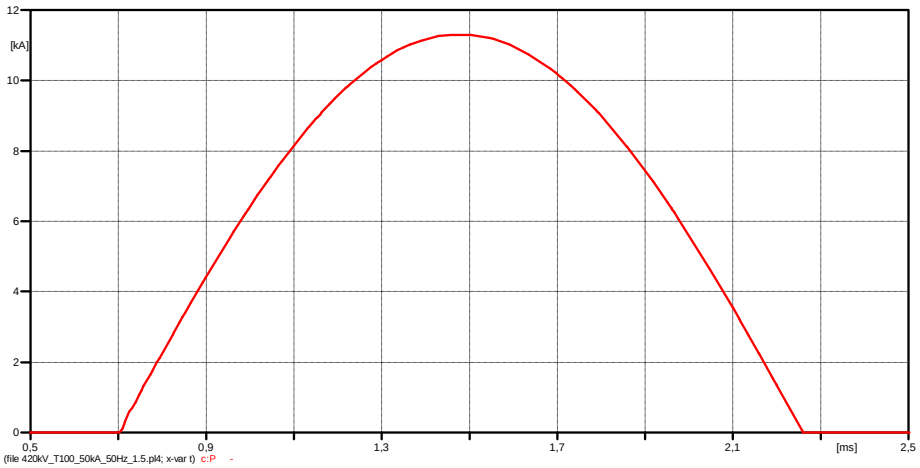


ATP DIGITAL MODEL

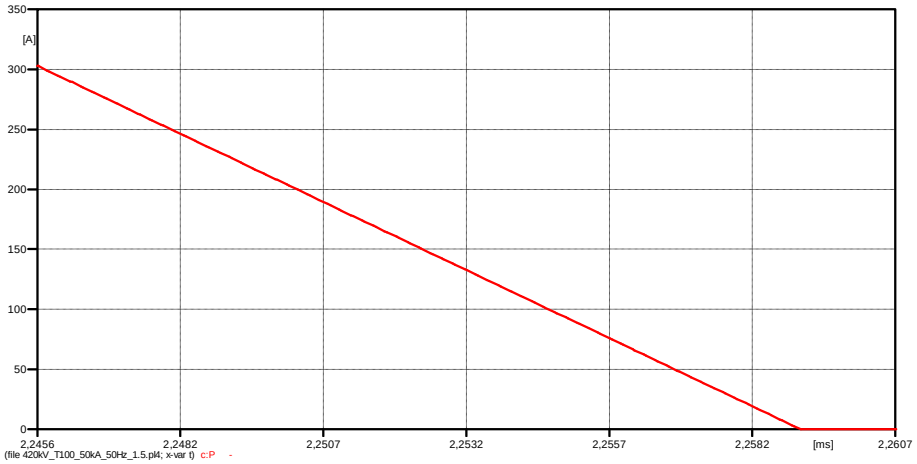
Figures below show results obtained simulating circuit represented in *Fig.7.4.*



TRV



Injected current i_h



di/dt of injected current i_h

7.2.6. *Test - duty T100: I = 63 kA f = 60 Hz f.p.c.f. = 1.5*

Test circuit parameters

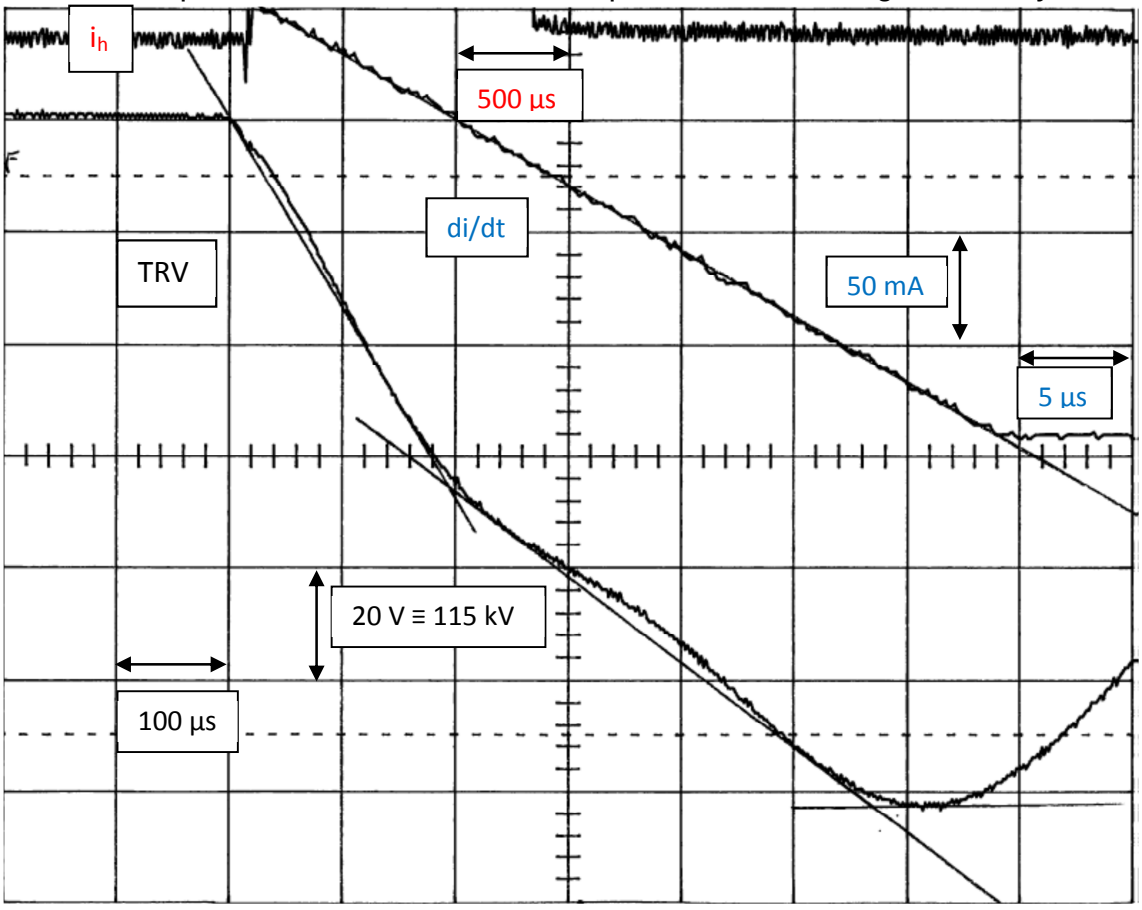
C_h [µF]	L_h [mH]	L_{pf} [mH]	C_1 [µF]	R_1 [Ω]	L_0 [mH]	C_0 [µF]	R_0 [Ω]	C_3 [µF]	C_4 [µF]
11.15	15.5	666	2.3	6.25	4.25	1.49	22	0.0375	0.021

Comparison between Laboratory TRV and ATP digital model

	U_h [kV]	Injected current (i_h)		TRV			
		f_h [Hz]	di/dt [A/µs]	U_1 [kV]	t_1 [µs]	U_c [kV]	t_2 [µs]
Laboratory TRV	540	395	33.6	386	193	720	570
ATP model	558	385	33.8	370	190	711	583
% difference		-2.3	0.6	-4.1	-1.5	-1.6	2.3

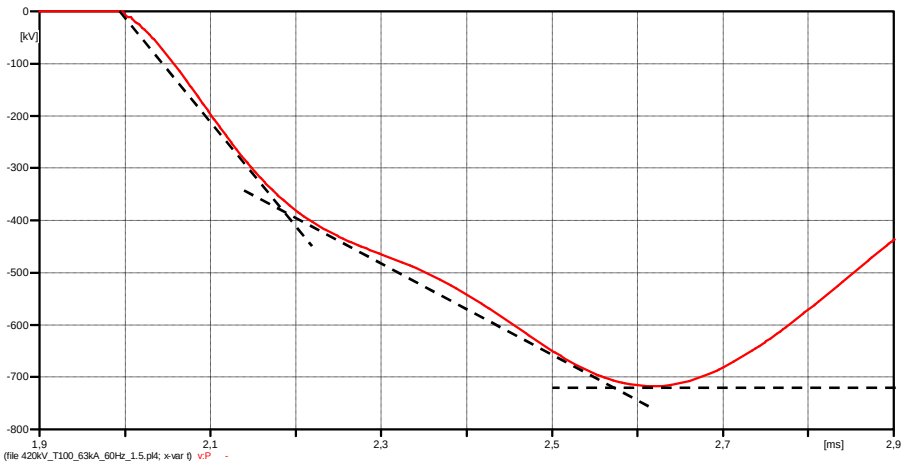
LABORATORY TRV

Figure below represents a real TRV wave shape measured during a test-duty:

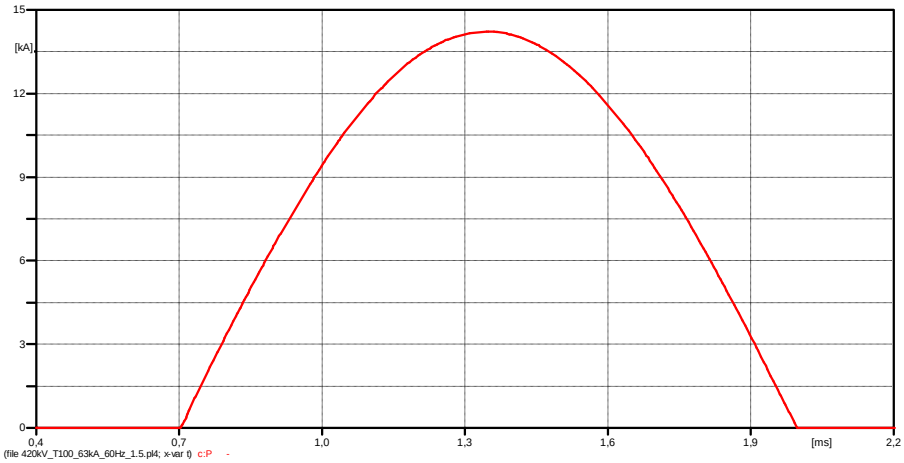


ATP DIGITAL MODEL

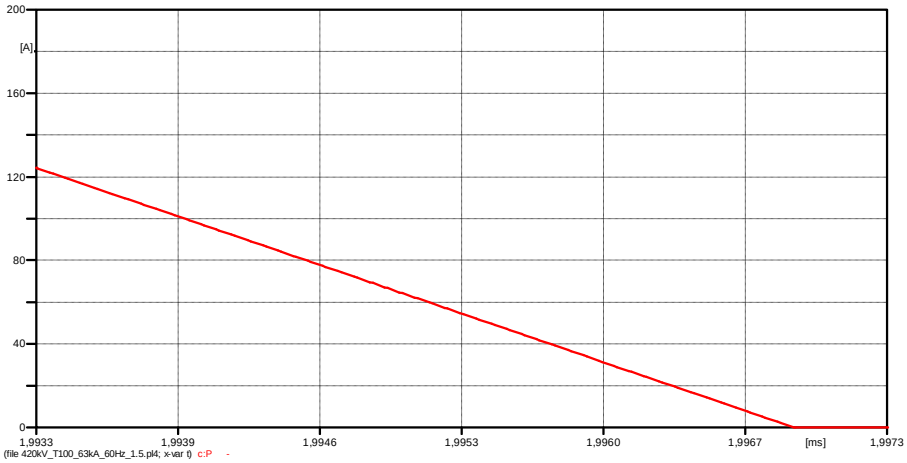
Figures below show results obtained simulating circuit represented in *Fig.7.4.*



TRV



Injected current i_h



di/dt at zero of injected current i_h

7.3. Out-of-phase test

The test circuit scheme and the equivalent ATP digital model are shown in *Fig. 7.5* and *7.6* respectively.

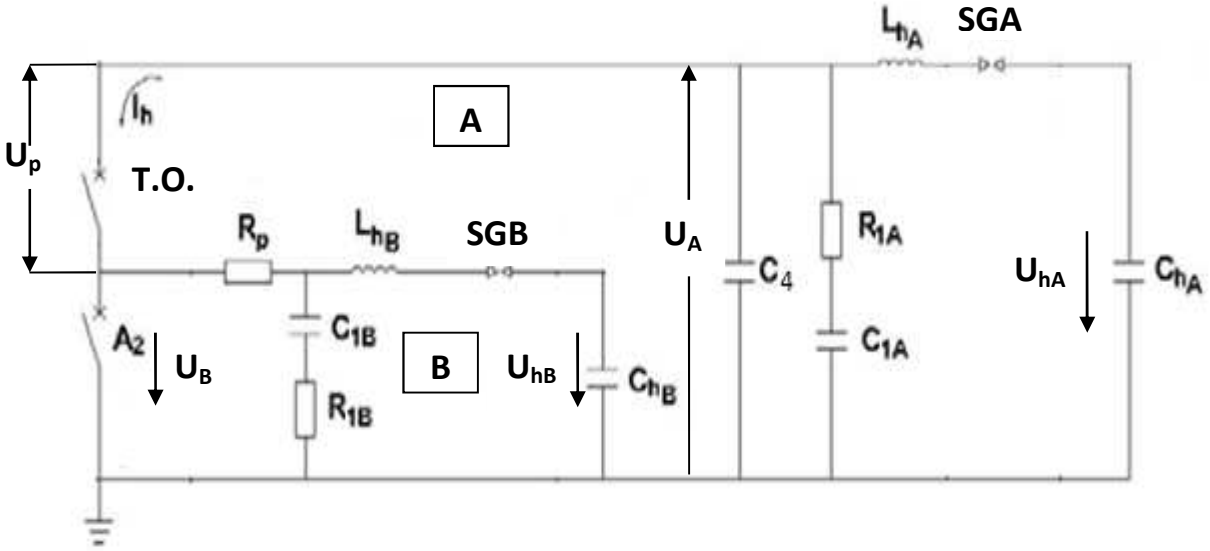


Figure 7.5 - Test circuit diagram

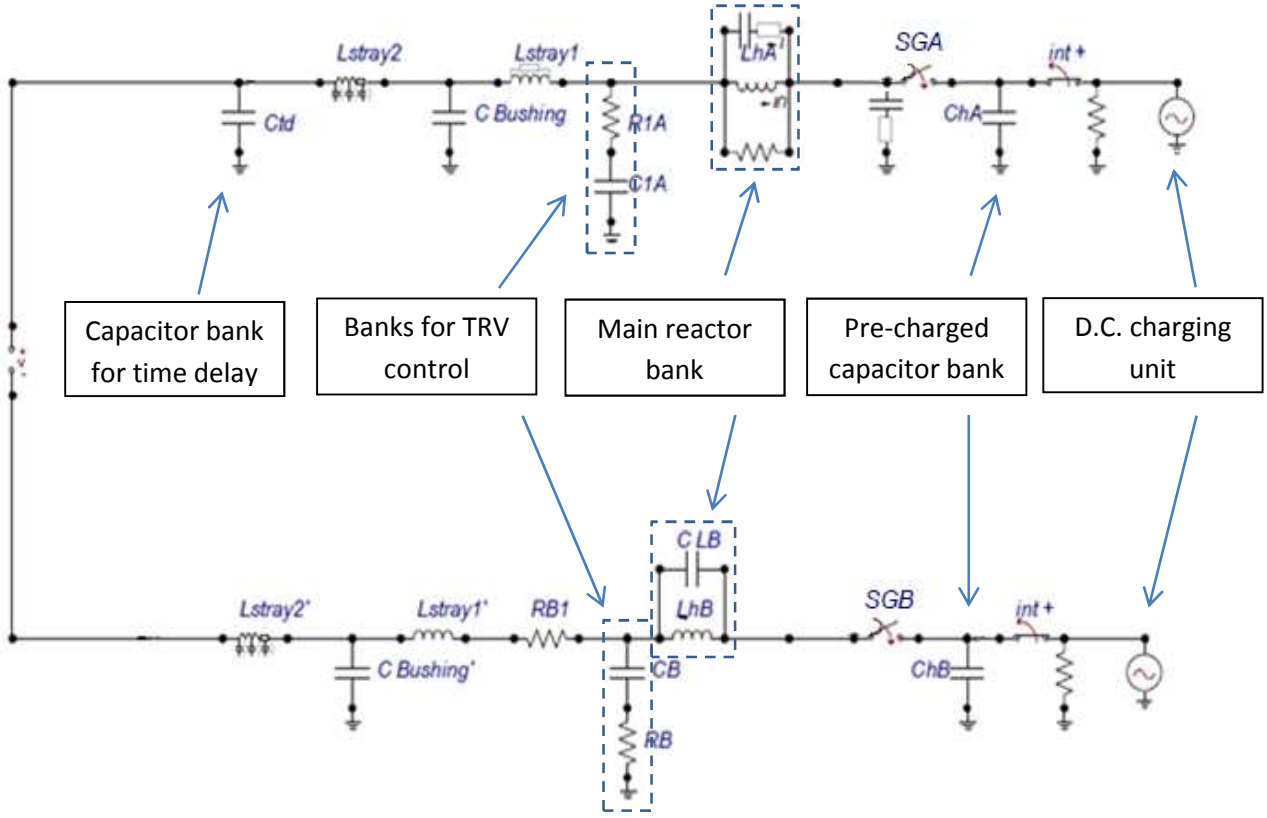


Figure 7.6 - ATP digital model

Test- duty OP2: I = 15.75 kA f = 50 Hz m.f. = 2

Test circuit parameters

	C_h [μF]	L_h [mH]	C_1 [μF]	R_1 [Ω]	C_4 [μF]
Circuit A	3.56	72	0.6725	187.5	0.021
Circuit B	3.005	2000	0.0125	4480	-

R_p (R_{B1}): resistor of 360 Ω inserted in the circuit B for protection in case of over-voltages.

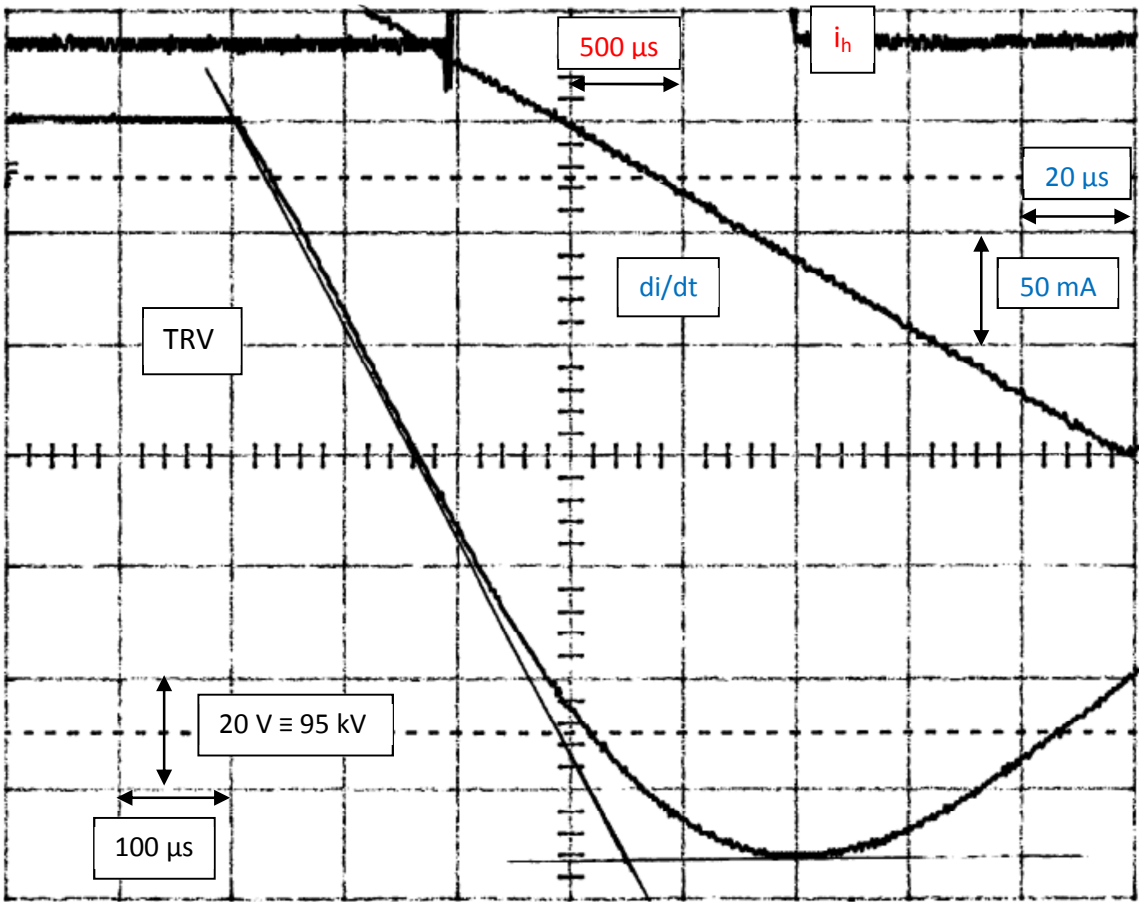
Comparison between Laboratory TRV and ATP digital model

		U_h [kV]	Injected current i_h		TRV			
			f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2-t_3 [μs]
Laboratory TRV	**Circuit A**	511	323	7.0	-	-	630	354
	Circuit B	255	-	-	-	-	500	700
ATP model	**Circuit A**	533	321	7.04	-	-	600	370
	Circuit B	266	-	-	-	-	480	710
% difference	**Circuit A**		-0.6	-	-	-	-4.6	4.8
	Circuit B		-	-	-	-	-4	1.4

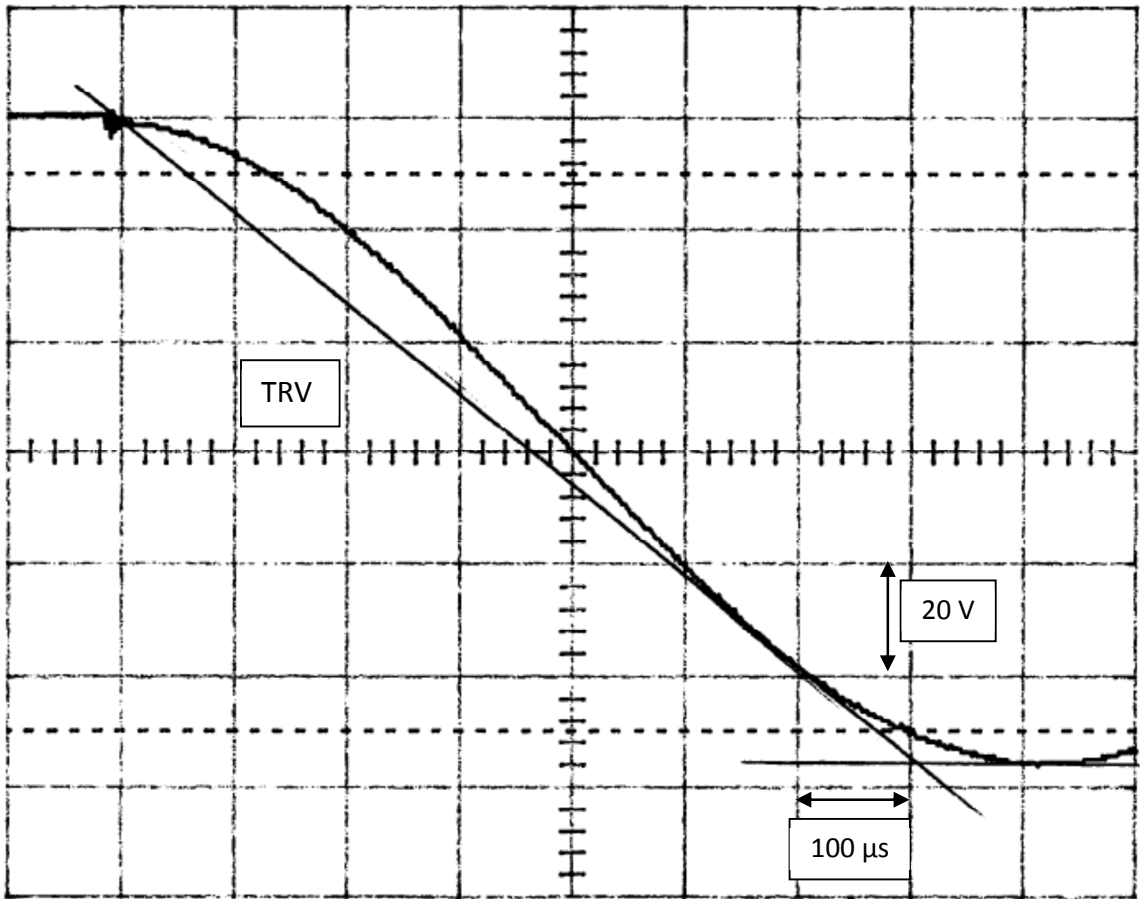
LABORATORY TRV

Figure below represents a real TRV wave shape measured during a test-duty:

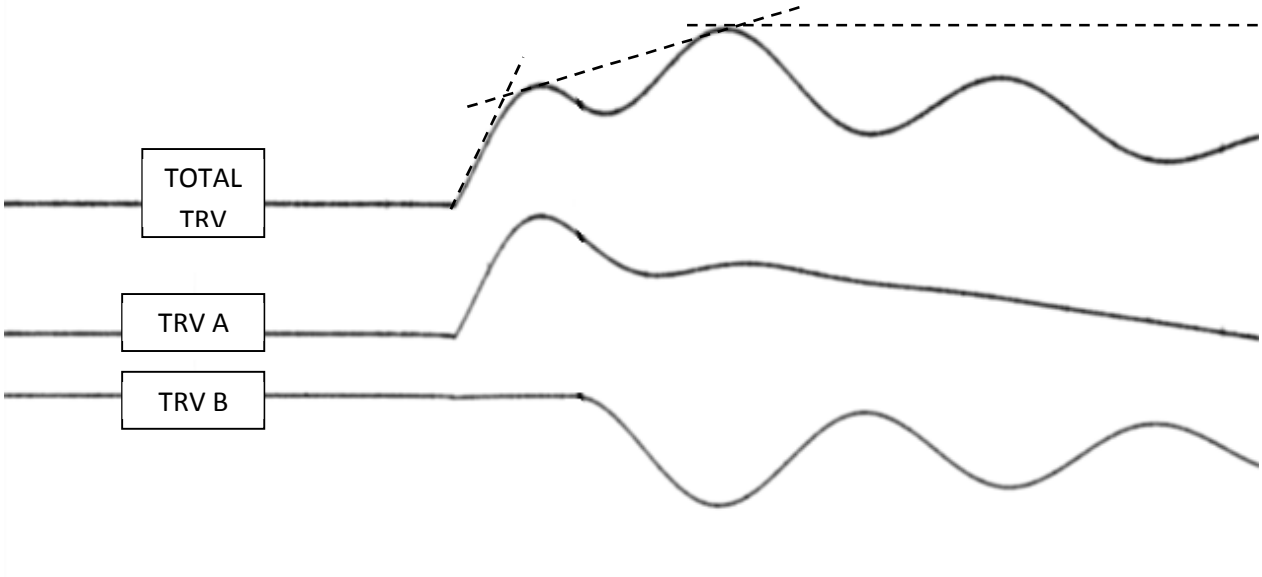
CIRCUIT A



CIRCUIT B



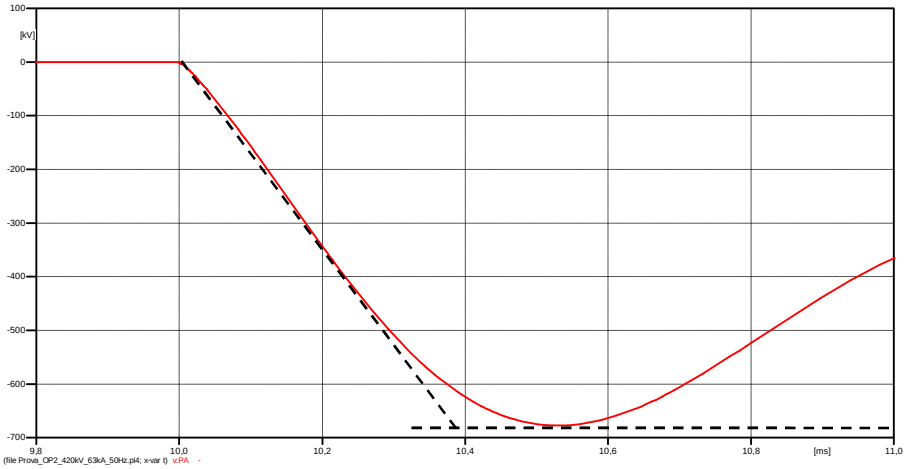
TOTAL TRV



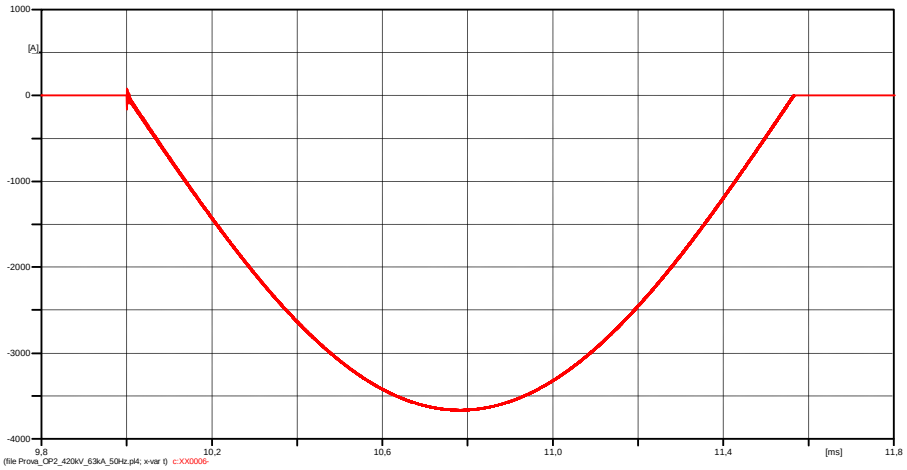
ATP DIGITAL MODEL

Figures below show results obtained simulating circuit represented in *Fig.7.6.*

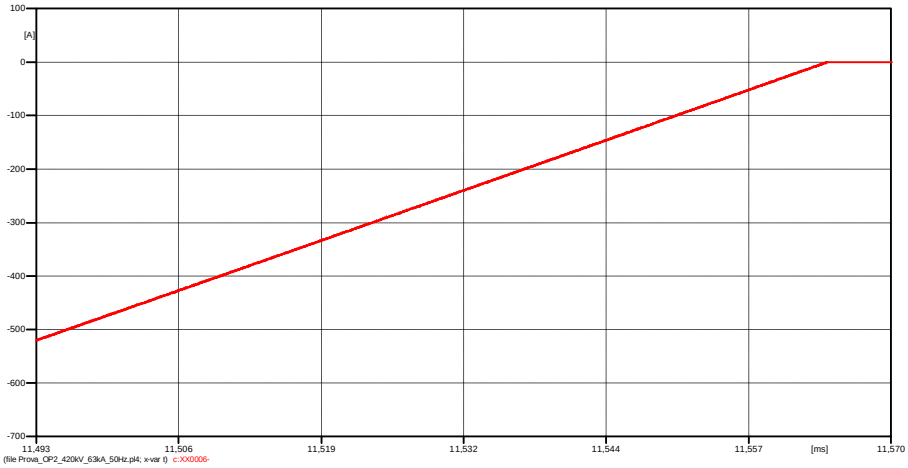
CIRCUIT A



TRV

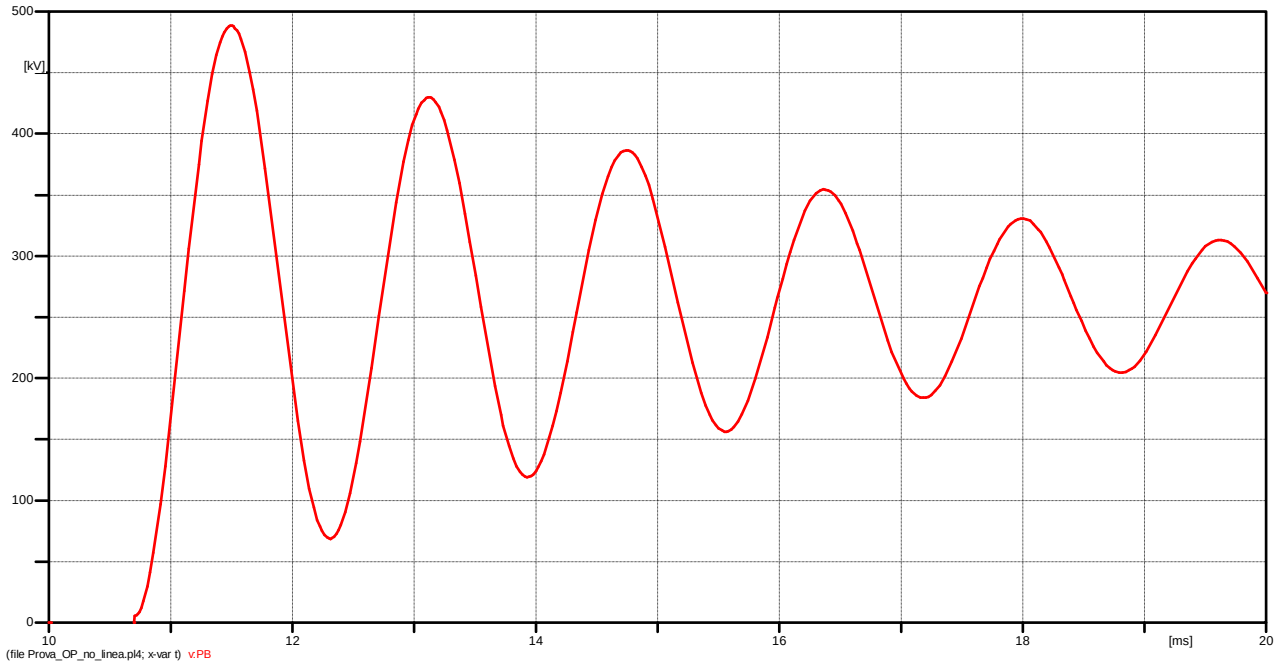


Injected current i_h



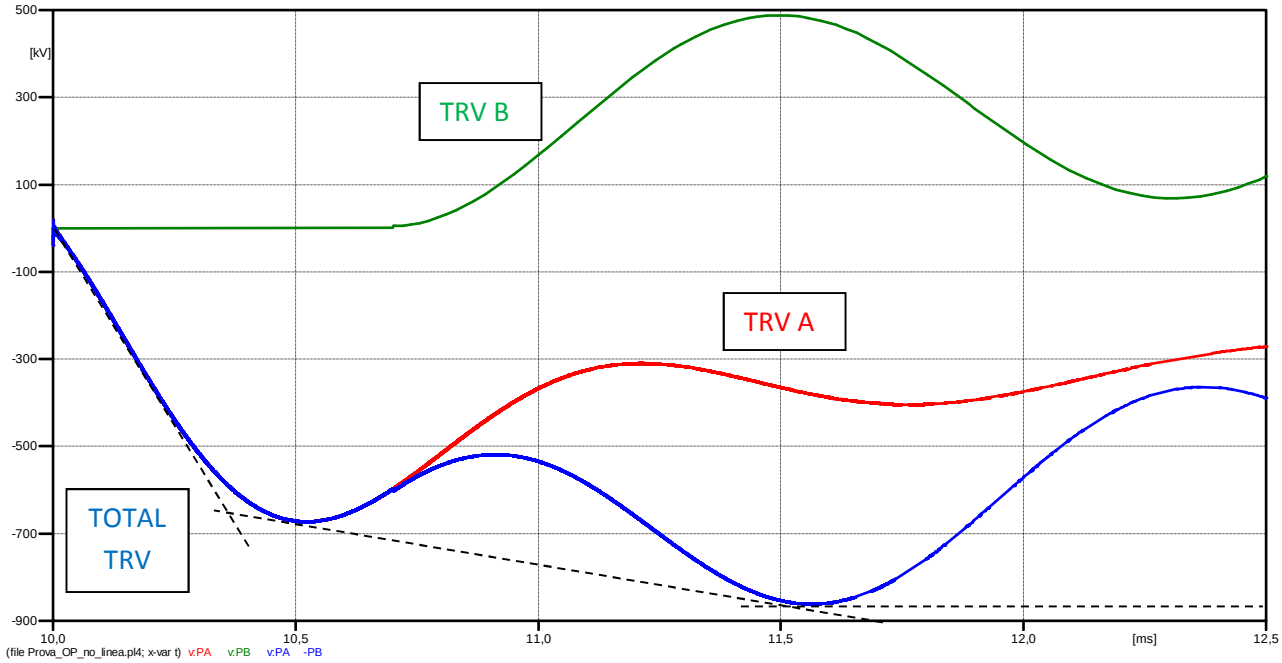
di/dt at zero of injected current i_h

CIRCUIT B



TRV

TOTAL TRV



7.4. Capacitive current switching

The test circuit scheme and the equivalent ATP digital model are shown in *Fig. 7.7* and *7.8* respectively

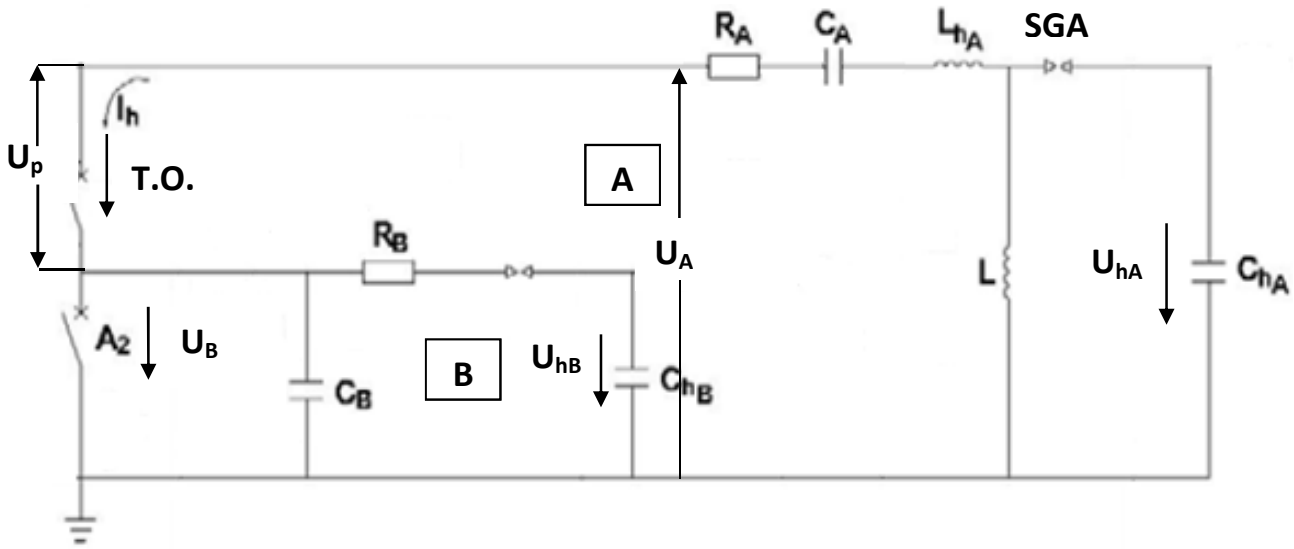


Figure 7.7 - Test circuit diagram

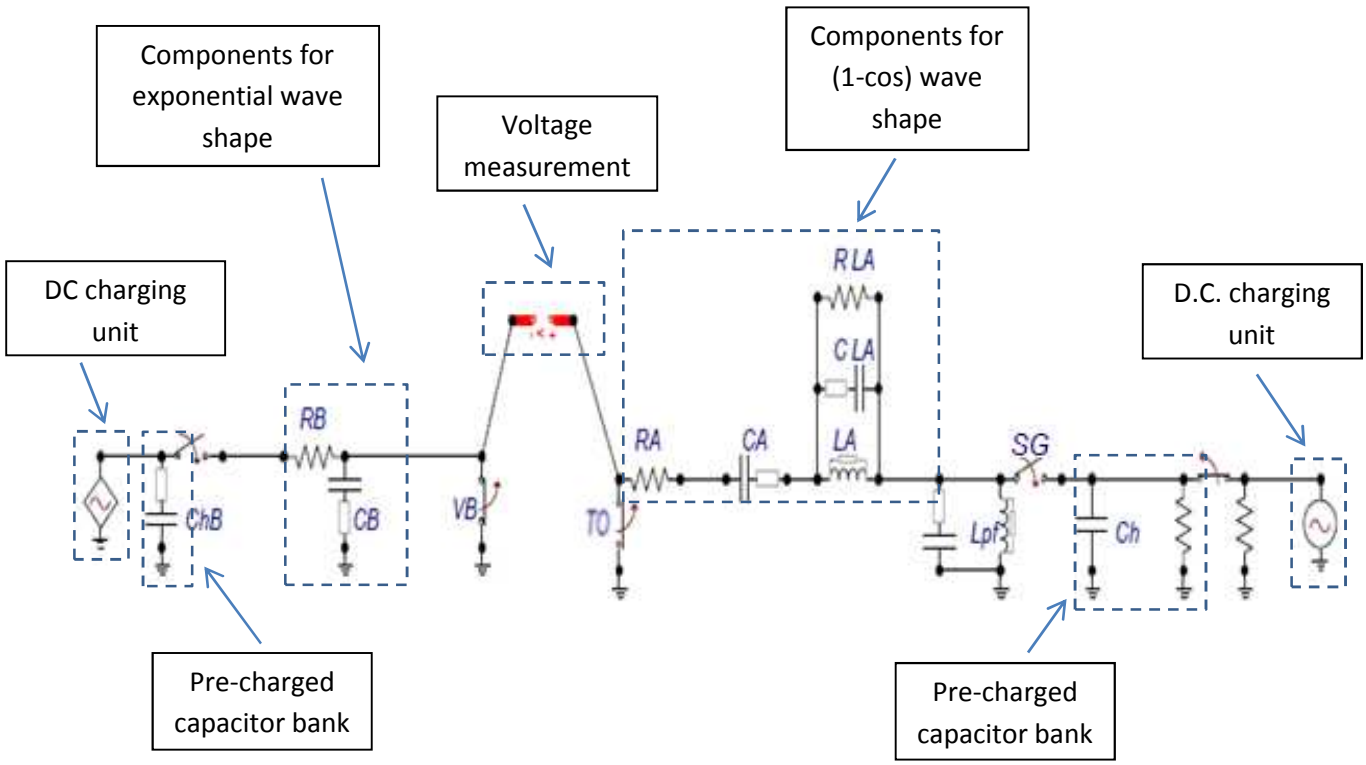


Figure 7.8 - ATP digital model

Test - duty LC2: I = 400 A f = 50 Hz kc = 1.4

Test circuit parameters

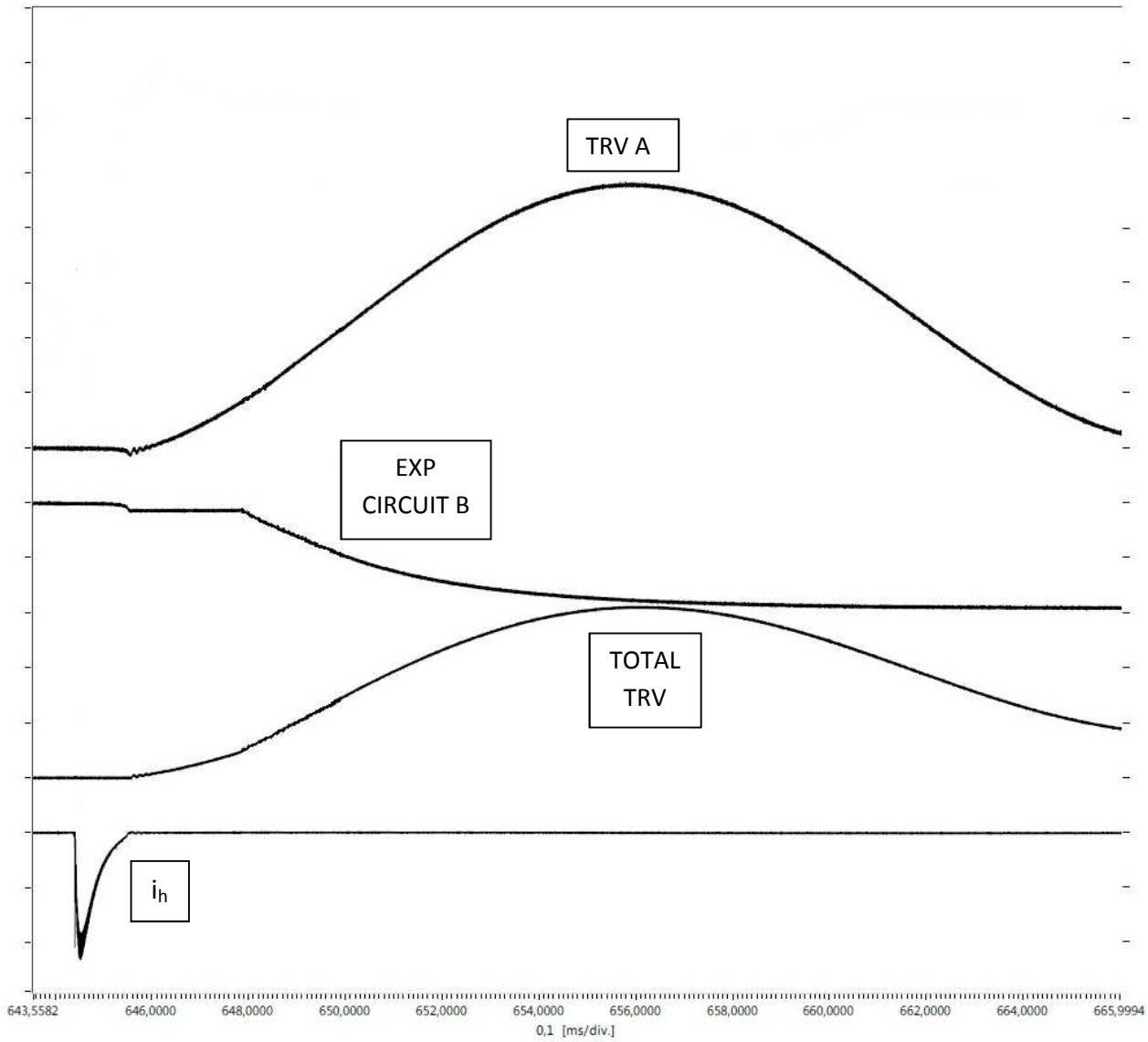
	C_h [µF]	L_h [mH]	L [H]	C [µF]	R [Ω]
Circuit A	5.2	80	2	0.25	1000
Circuit B	1.5	-	-	0.021	180000

Comparison between Laboratory TRV and ATP digital model

		U_h [kV]	Injected current i_h		TRV		
			f_h [Hz]	di/dt [A/µs]	U_c [kV]	t_3 [ms]	t_0 [ms]
Laboratory TRV	**Circuit A**	413	382		745	8.7	-
	Circuit B	207	-		-	-	4
ATP model	**Circuit A**	413	400		753	8.4	-
	Circuit B	207	-		-	-	3.86
% difference	**Circuit A**		4		1.1	-3.4	-
	Circuit B		-		-	-	-3.5

LABORATORY TRV

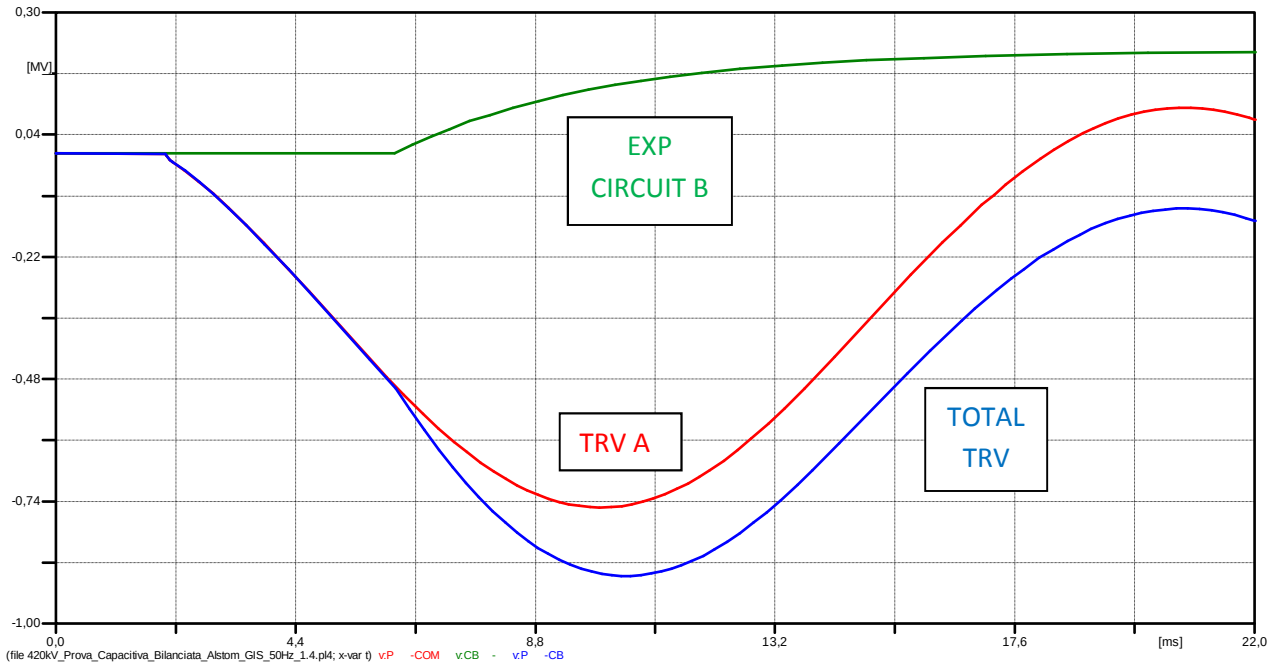
Figure below represents a real TRV wave shape measured during a test-duty:

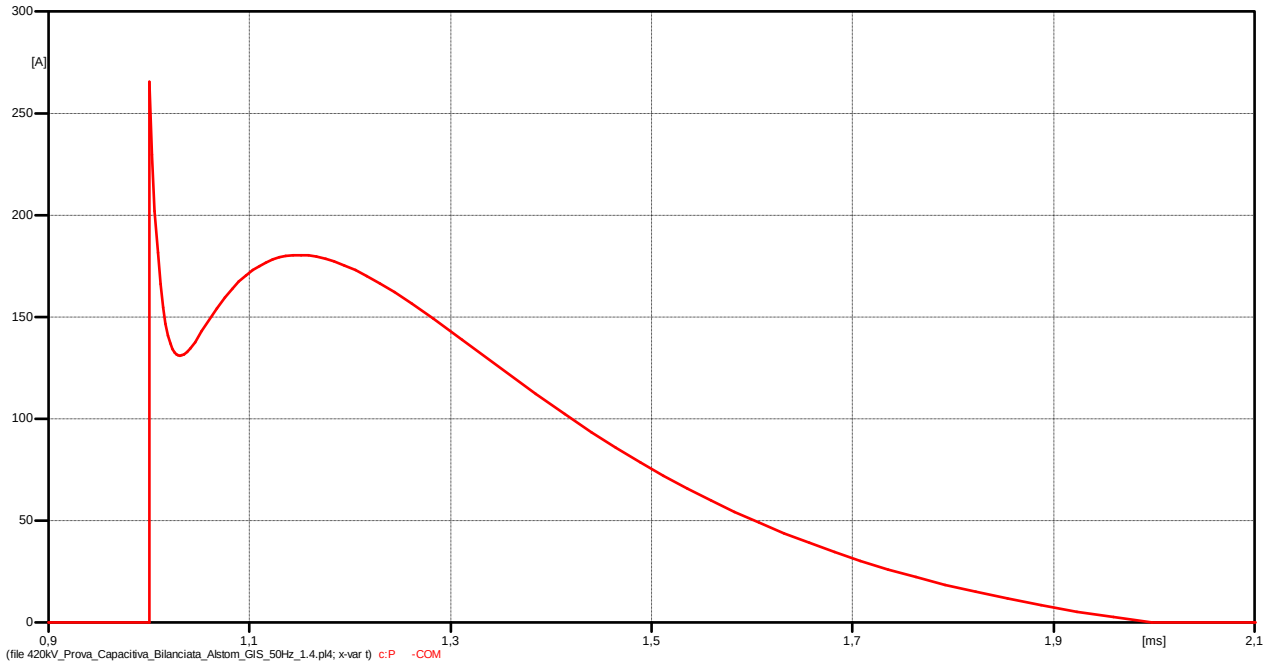


ATP DIGITAL MODEL

Figures below show results obtained simulating circuit represented in *Fig.7.8.*

TOTAL TRV





Injected current i_h

7.5. Conclusions

Comparison between Laboratory TRV and ATP digital models shows a difference between values always under 5%.
So, our ATP digital models of the synthetic circuit can be used to simulate the real circuit behavior with good accuracy.

8. FIRST REPOWERING SOLUTION: REVAMPING OF CESI SYNTHETIC LABORATORY

8.1. Revamping the present High Power Synthetic Laboratory

8.1.1. Solution description

The first solution taken in consideration is to refurbish the present Laboratory without changing the Single Line Diagram: new values of circuit parameters, however, are selected. These values must be calculated in order to obtain a new laboratory able to test 550 kV circuit-breaker.

The present Laboratory configuration is the following:

- **Voltage circuit**: parallel current injection method circuit, named “Weil” circuit, that provides 2/4 parameters TRV.
- **Current circuit** (see point 6.1.1): short-circuit generator to provide the test current (MAX 63 kA) at about 16 kV, with a short-circuit power of 1000 MVA.

8.1.2. Advantages of Revamping solution

- Test bay rating increases from 420 kV @ 63 kA to 550 kV @ 63 kA.

- Civil work on Laboratory buildings will not be required: generator hall, High Voltage hall, control room and test bay will remain about unchanged.

- No impact on operator testing procedure, because the voltage circuit remains the same used today for testing, so the test method is unchanged:

- Present voltage circuit is located in an over-dimensioned building, so that insulation distances between live components and the building structure are also suitable for the new voltage level: this means that the building will remain unchanged

- Since the voltage circuit remains unchanged, current circuit also remains the same, based on 1 auxiliary circuit-breaker connected in series to 1 circuit-breaker under test (see fig. B.1 of ANNEX B, IEC 62271-101).
  Today, auxiliary circuit-breaker has 2 interruption chambers, while circuit-breaker under test may have 1 or 2 interruption chambers, for a maximum total of 4 interruption chambers.

  Commonly, for a safe control of the energy during the arcing period, each interruption chamber needs about 4 kV.
  Since short-circuit power is 1000 MVA, at the maximum current of 63 kA, supply voltage is:

$$V = \frac{1000\ MVA}{63\ kA} \cong 16\ kV$$

If the maximum number of interruption chamber in series is considered, the supply voltage required is:

$$V = 4 \cdot 4 = 16\ kV$$

that is right the short-circuit generator supply voltage. So, considering this configuration, generator power (current and voltage) is adequate.

8.1.3. Disadvantages of Revamping solution

- As results of simulations will show, Weil circuit has an inherent physical limit in testing 550 kV circuit-breakers with first-pole-to-clear factor equal to 1.5, as already shown by [6]. Voltage waveforms at 550 kV with a first-pole-to-clear factor of 1.5 are not in accordance with IEC Standards, especially for short-circuit test-duties T60 and T100.
  With Weil circuit it is only possible to test 550 kV circuit-breakers with a first-pole-to-clear factor of 1.3. This is in accordance with Standard prescriptions, but doesn't fulfill the requirement of testing with a first-pole-to-clear factor of 1.5 put forward by some manufacturers.
  As an additional consequence of such a physical limit, future enhancements of the Laboratory beyond 550kV (e.g. to test 800kV circuit-breakers) will not be possible with a parallel current injection circuit.

  Remark. Results obtained with our model of the synthetic circuit are in accordance with the known physical limitations described in previous references. i.e., the model of the circuit accurately reproduces not only the dynamic behavior but also its physical constrains. This fact increases the confidence about the reliability of the results obtained by means of the model; they can thus be used as a sound basis for the next steps of the project (basic and detail).

- Testing activities must be stopped during the High Voltage plant revamping period. Additional time will be devoted to Laboratory offline and setup tests; during these periods, tests cannot be performed and this loss of income must be taken into account in budgetary cost estimation.

- Charging voltage (U_h), to be applied to C_h in order to perform tests, about duplicates in some conditions.
  In fact Standards define the voltage required to test a 550 kV circuit-breaker ($U_n = 550\ kV$):

$$U_P = \frac{U_n}{\sqrt{3}} \cdot k_{pp}$$

It can be demonstrated [5] that:

$$U_h = \sqrt{2} \cdot U_p \left(1 + \frac{C_1}{C_h}\right)$$

Today, testing a 420kV circuit-breaker, a $^{L_h}/_{L_d} = 1 \div 1.15$ is adequate to obtain TRV wave shape in accordance with Standards requirements. C_1 and C_h values are a consequence of this $^{L_h}/_{L_d}$ value calibration.

For example (see point 7.2.1.):

$$^{L_h}/_{L_d} = 1.12$$

values obtained are:

$$C_h = 9.5\ \mu F$$

$$C_1 = 0.9575\ \mu F$$

$$U_P = \frac{420\ kV}{\sqrt{3}} \cdot 1.3 = 316\ kV$$

$$U_h = 545\ kV$$

$$f_h = \frac{1}{2 \cdot \pi \cdot \sqrt{(L_h \cdot C_h)}} = 268\ Hz\ (Standards\ range: 250\ Hz \div 1000\ Hz)$$

Passing to test 550kV circuit-breaker:

- ✓ With $^{L_h}/_{L_d} = 1.14$

$$^{L_h}/_{L_d} = 1.14$$

values obtained are:

$$C_h = 8\ \mu F$$

$$C_1 = 1.8\ \mu F$$

$$U_P = \frac{550\ kV}{\sqrt{3}} \cdot 1.3 = 413\ kV$$

$$U_h = 710\ kV$$

$$f_h = \frac{1}{2 \cdot \pi \cdot \sqrt{(L_h \cdot C_h)}} = 252\ Hz\ (Standards\ range: 250\ Hz \div 1000\ Hz)$$

But with $^{L_h}/_{L_d} = 1.14$, the resulting TRV is not in accordance with Standards requirements (see next figure and point 4.4. for relevant evaluation criteria).

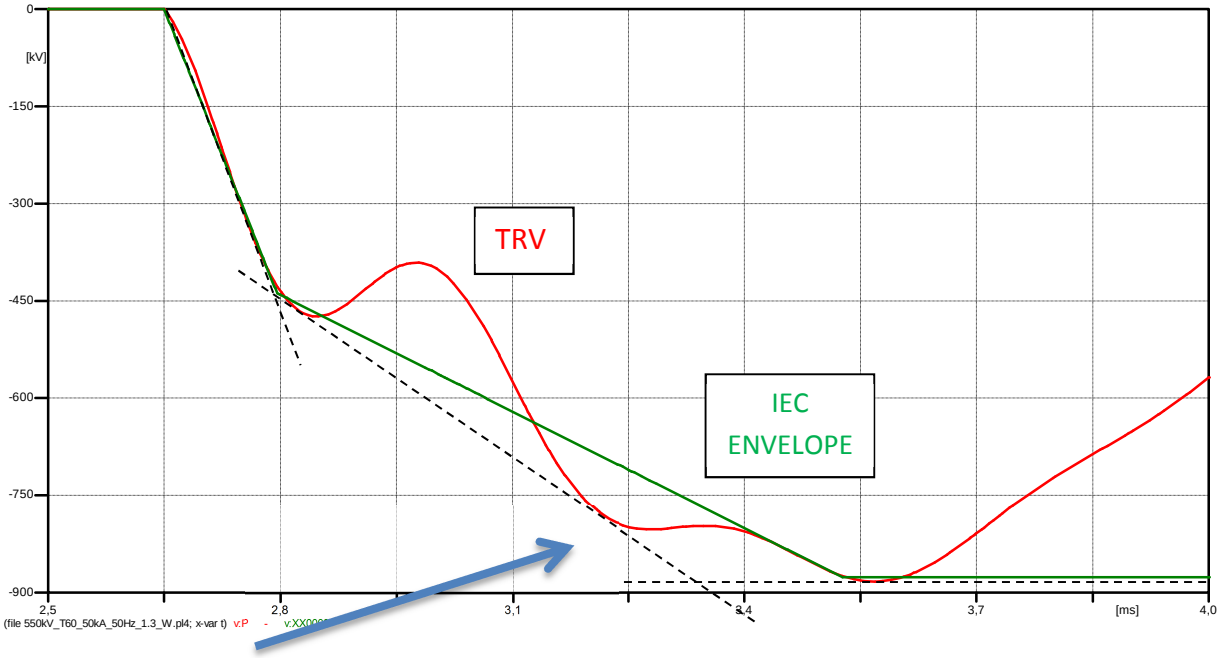


Figure 8.1 - a non-compliant TRV wave shape

✓ With $^{L_h}/_{L_d} = 1.5$ (upper limit set by [3]), TRV wave shape obtained is in accordance with Standards requirements (see 8.2.2.1.); in this case:

$$^{L_h}/_{L_d} = 1.5$$

values obtained are:

$$C_h = 6.2\ \mu F$$

$$C_1 = 3.1\ \mu F$$

$$U_P = \frac{550\ kV}{\sqrt{3}} \cdot 1.3 = 413\ kV$$

$$U_h = 960\ kV$$

$$f_h = \frac{1}{2 \cdot \pi \cdot \sqrt{(L_h \cdot C_h)}} = 251\ Hz\ (Standards\ range: 250\ Hz \div 1000\ Hz)$$

The figure below shows a TRV wave shape in accordance with Standards.

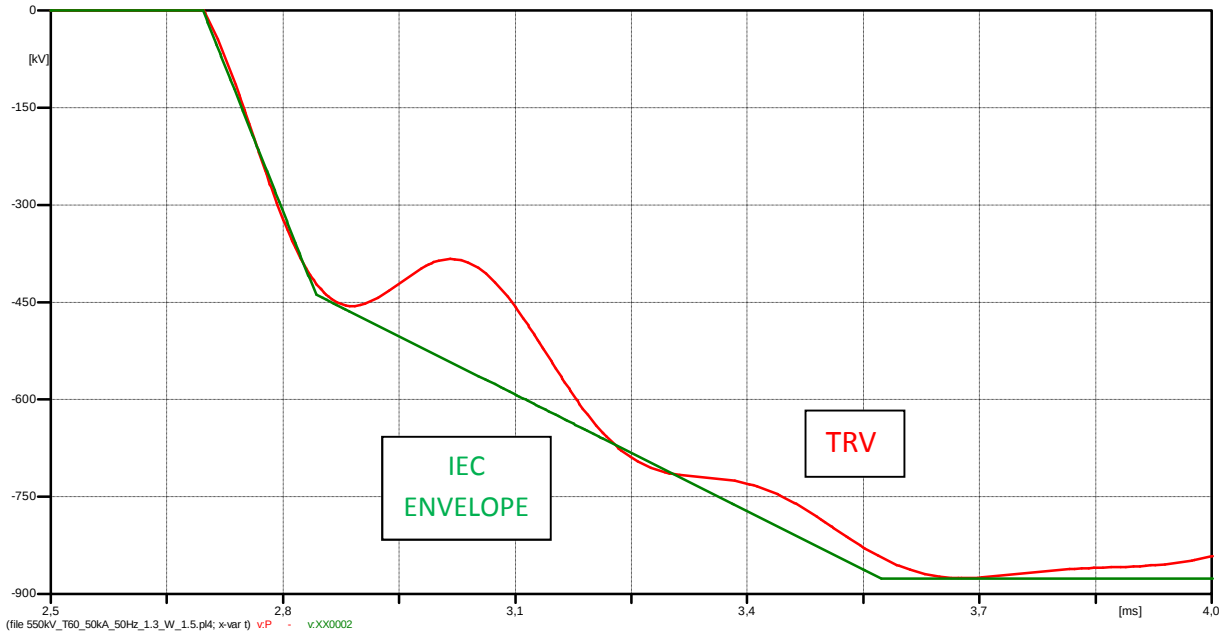


Figure 8.2 - a compliant TRV wave shape

In summary: today, using the same test-duty, to test a 420 kV circuit-breaker, the charging voltage U_h required is about 550 kV. To test a 550 kV, with the same test-duty and oscillating circuit parameters unchanged, the U_h should be 710 kV. But considering the oscillating circuit parameters calibration required to obtain a TRV in compliance to Standard requirements, U_h value increases up to about 1000 kV.

It's evident from the next chart that the charging voltage U_h is strongly dependent from L_h/L_d ratio.

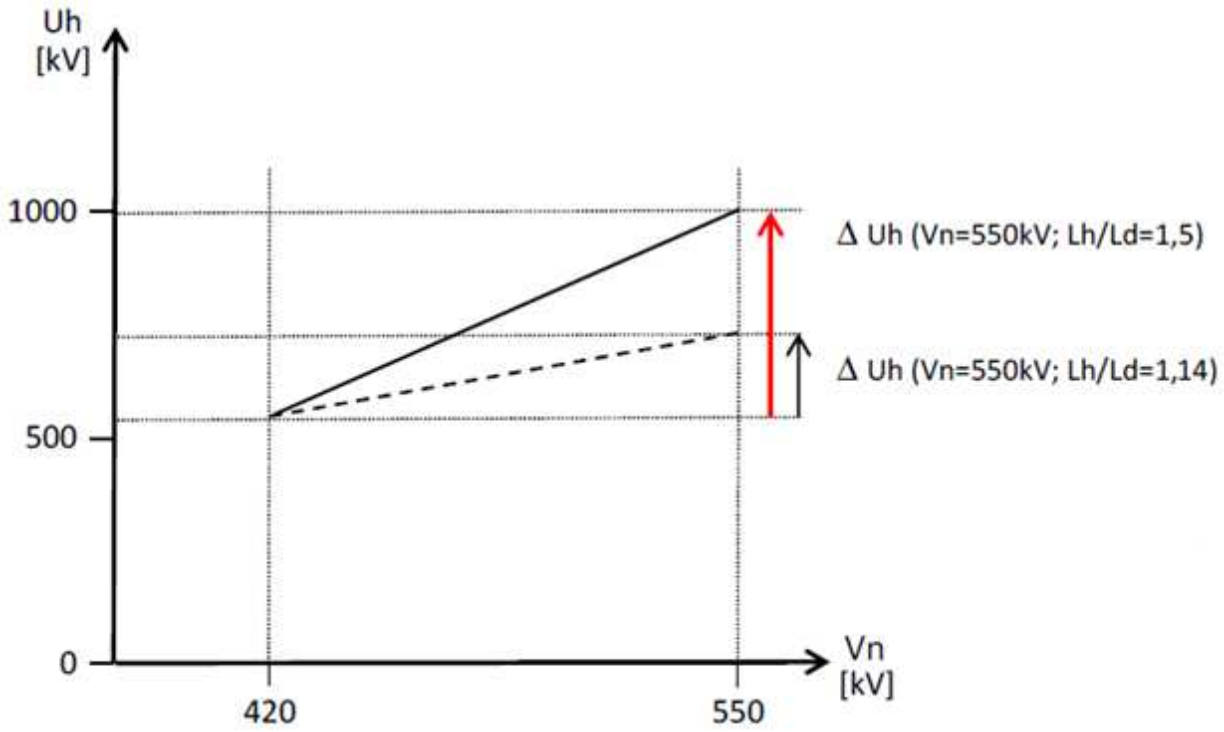


Figure 8.3 - relationship between rated voltage and charging voltage

8.2. Revamping solution: digital simulation results

The digital circuit simulations covered the following cases:

- Short-Circuit 2 parameters TRV (values requested by Standards)

Table 8.1 - Short-Circuit 2 parameters TRV (values requested by Standards)

Short-circuit current [kA]	Test-duty	Test Current [kA]	Frequency [Hz]	k_{pp}	Compliant to IEC 62271-100
50	T10	5 (0.1·50)	50	1.5	YES
50	T10	5 (0.1·50)	60	1.5	YES
63	T10	6.3 (0.1·63)	50	1.5	YES
63	T10	6.3 (0.1·63)	60	1.5	YES
50	T30	15 (0.3·50)	50	1.3	YES
50	T30	15 (0.3·50)	60	1.3	YES
63	T30	18.9 (0.3·63)	50	1.3	YES
63	T30	18.9 (0.3·63)	60	1.3	YES

- Short-Circuit 2 parameters TRV (values requested by some manufacturers)

Table 8.2 - Short-Circuit 2 parameters TRV (values requested by some manufacturers)

Short-circuit current [kA]	Test-duty	Current [kA]	Frequency [Hz]	k_{pp}	Compliant to IEC 62271-100
50	T30	15 (0.3·50)	50	1.5	YES
50	T30	15 (0.3·50)	60	1.5	YES
63	T30	18.9 (0.3·63)	50	1.5	YES
63	T30	18.9 (0.3·63)	60	1.5	YES

- Short-Circuit 4 parameters TRV (values requested by Standards)

Table 8.3 - Short-Circuit 4 parameters TRV (values requested by Standards)

Short-circuit current [kA]	Test-duty	Current [kA]	Frequency [Hz]	k_{pp}	Compliant to IEC 62271-100
50	T60	30 (0.6·50)	50	1.3	YES
50	T60	30 (0.6·50)	60	1.3	YES
63	T60	37.8 (0.6·63)	50	1.3	YES
63	T60	37.8 (0.6·63)	60	1.3	YES
50	T100	50	50	1.3	YES
50	T100	50	60	1.3	YES
63	T100	63	50	1.3	YES
63	T100	63	60	1.3	YES

- Short-Circuit 4 parameters TRV (values requested by some manufacturers)

Table 8.4 - Short-Circuit 4 parameters TRV (values requested by some manufacturers)

Short-circuit current [kA]	Test-duty	Current [kA]	Frequency [Hz]	k_{pp}	Compliant to IEC 62271-100
50	T60	30 (0.6·50)	50	1.5	NO
50	T60	30 (0.6·50)	60	1.5	NO
63	T60	37.8 (0.6·63)	50	1.5	NO
63	T60	37.8 (0.6·63)	60	1.5	NO
50	T100	50	50	1.5	NO
50	T100	50	60	1.5	NO
63	T100	63	50	1.5	NO
63	T100	63	60	1.5	NO

- Out-of-phase
  - ✓ *Test -duty OP2* $I = 15.75\ kA$ $f = 50\ Hz$ $m.f. = 2$

- Capacitive current switching
  - ✓ *Test -duty LC2* $I = 500\ A$ $f = 50\ Hz$ $k_c = 1.4$

8.2.1. Short-circuit 2p TRV

The equivalent ATP digital model used to obtain 550 kV TRV wave shapes is shown in *Fig.8.4*, and it is the same used to obtain 420 kV TRV wave shapes since the same testing methods is taking into account.

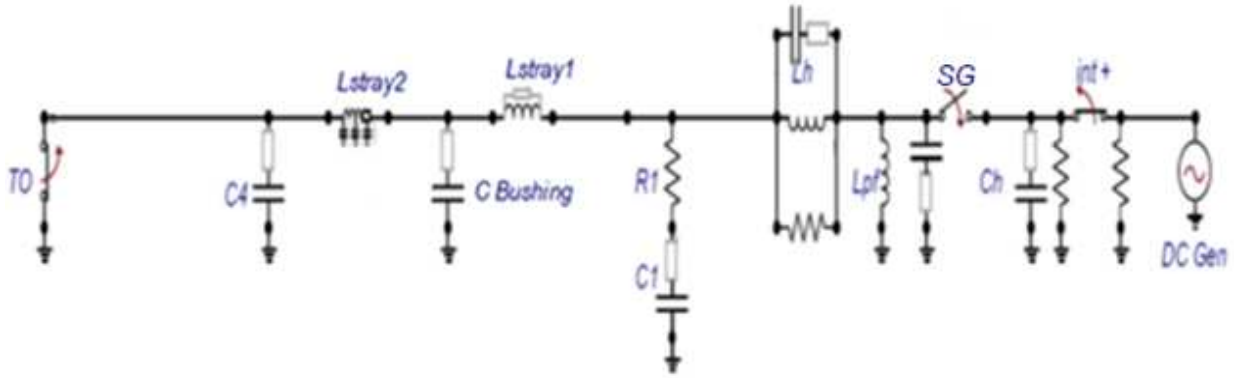


Figure 8.4 - ATP digital model

2 parameters TRV wave shapes, with tables containing the main components values and a comparison between ATP digital models and Standards TRV values are shown below.

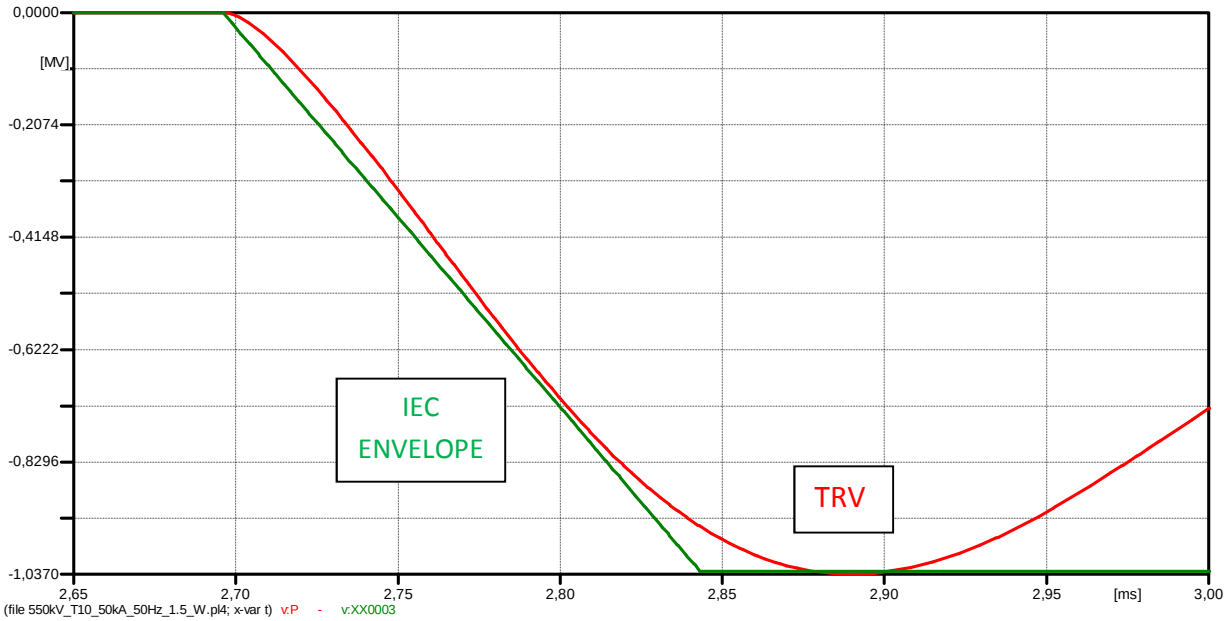
Even if all simulation have been executed, as per Standards indications, in the next section only simulations relevant to 50 kA 50 Hz and 63 kA 60 Hz are reported.

8.2.1.1. Test - duty T10: I = 5 kA f = 50 Hz f.p.c.f. = 1.5

Test circuit parameters

U_h [kV]	C_h [µF]	L_h [mH]	C_1 [µF]	R_1 [Ω]	C_4 [µF]
790	1.3	310	0.014	2600	0.002

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

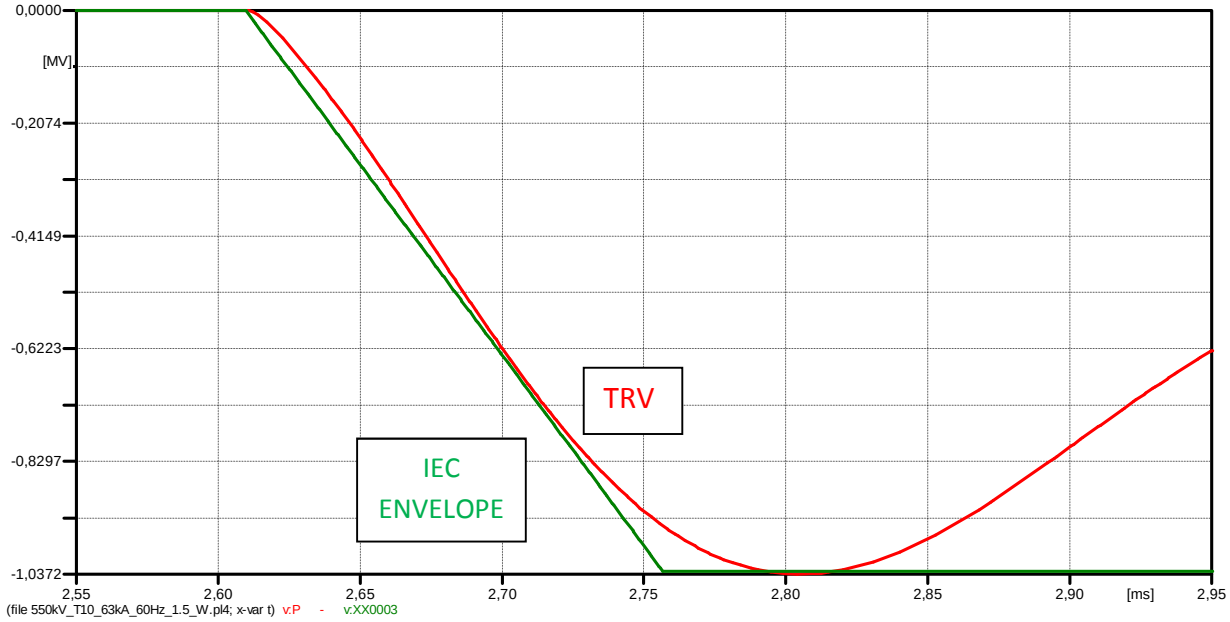
	Injected current (i_h)		TRV	
	f_h [Hz]	di/dt [A/µs]	U_c [kV]	t_3 [µs]
Standards values	250÷ 1000	2.2	1031	147
ATP model	251	2.19	1015	143
% difference		-0.4	-1.5	2.7

8.2.1.2. Test - duty T10: I = 6.3 kA f = 60 Hz f.p.c.f. = 1.5

Test circuit parameters

U_h [kV]	C_h [µF]	L_h [mH]	C_1 [µF]	R_1 [Ω]	C_4 [µF]
770	1.8	205	0.023	1600	0.002

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

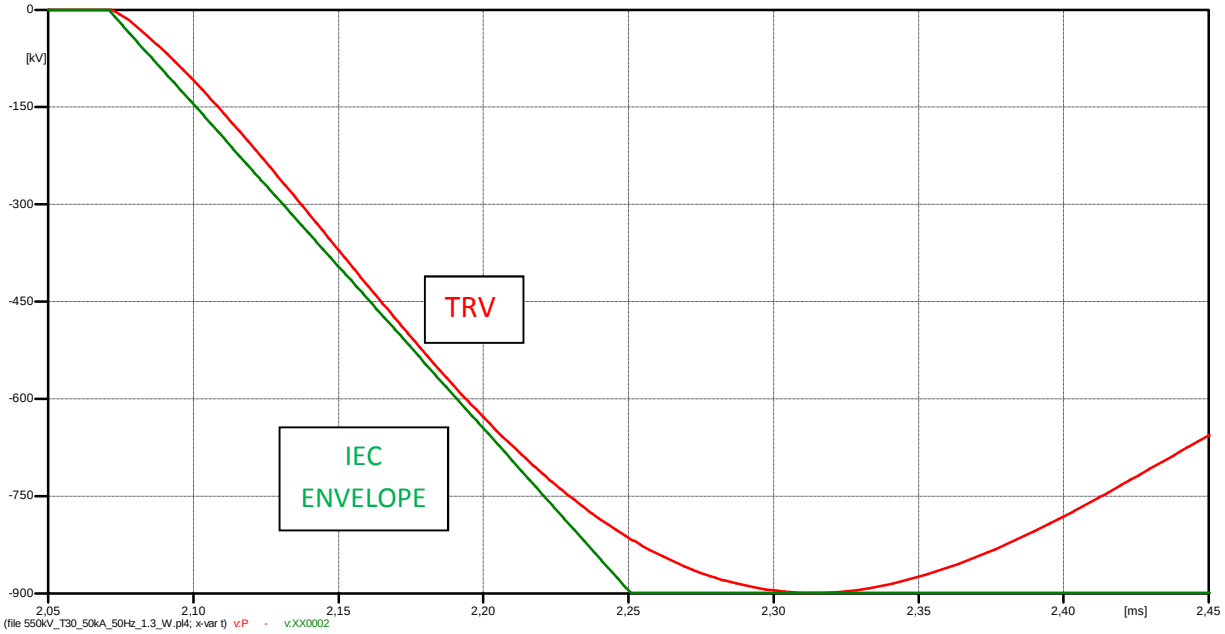
	Injected current (i_h)		TRV	
	f_h [Hz]	di/dt [A/µs]	U_c [kV]	t_3 [µs]
Standards values	250÷ 1000	3.35	1031	147
ATP model	262	3.35	1005	142
% difference		-	-2.5	-3.4

8.2.1.3. Test - duty T30: I = 15 kA f = 50 Hz f.p.c.f. = 1.3

Test circuit parameters

U_h [kV]	C_h [µF]	L_h [mH]	C_1 [µF]	R_1 [Ω]	C_4 [µF]
670	1.9	100	0.08	600	0.005

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

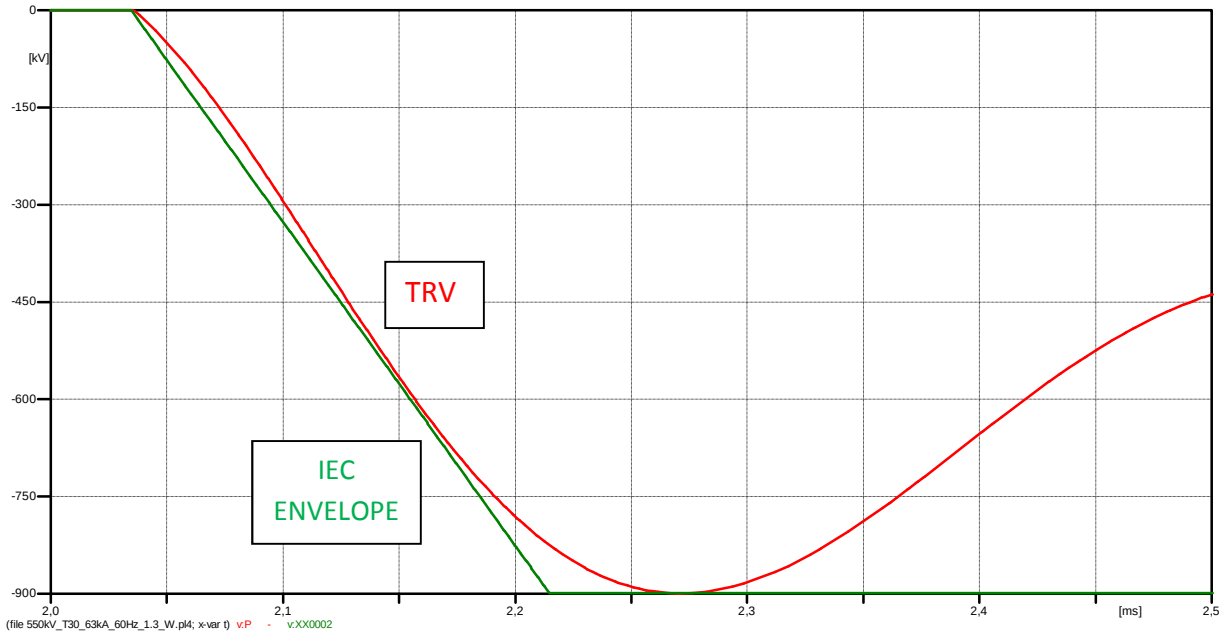
	Injected current (i_h)		TRV	
	f_h [Hz]	di/dt [A/µs]	U_c [kV]	t_3 [µs]
Standards values	250÷ 1000	6.64	899	180
ATP model	364	6.3	885	186
% difference		-3.4	-1.5	3.3

8.2.1.4. Test - duty T30: I = 18.9 kA f = 60 Hz f.p.c.f. = 1.3

Test circuit parameters

U_h [kV]	C_h [µF]	L_h [mH]	C_1 [µF]	R_1 [Ω]	C_4 [µF]
650	3	60	0.125	325	0.005

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

	Injected current (i_h)		TRV	
	f_h [Hz]	di/dt [A/µs]	U_c [kV]	t_3 [µs]
Standards values	250÷ 1000	10.04	899	180
ATP model	374	10	880	182
% difference		-0.4	-2.1	1.1

8.2.2. Short-circuit 4p TRV

The equivalent ATP digital model used to obtain 550 kV TRV wave shapes is shown in *Fig.8.5*, and it is the same used to obtain 420 kV TRV wave shapes, since the same testing methods is taking into account.

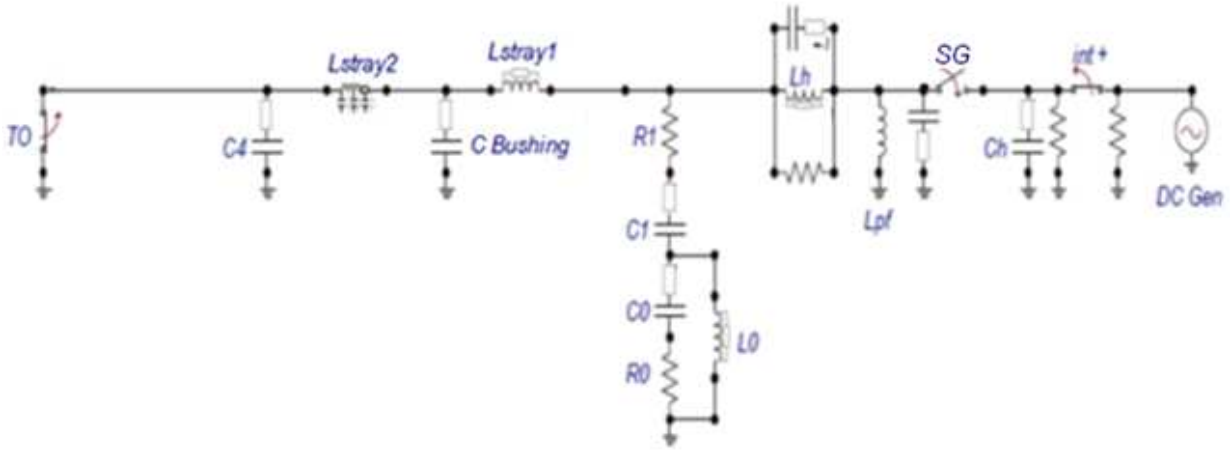


Figure 8.5 - ATP digital model

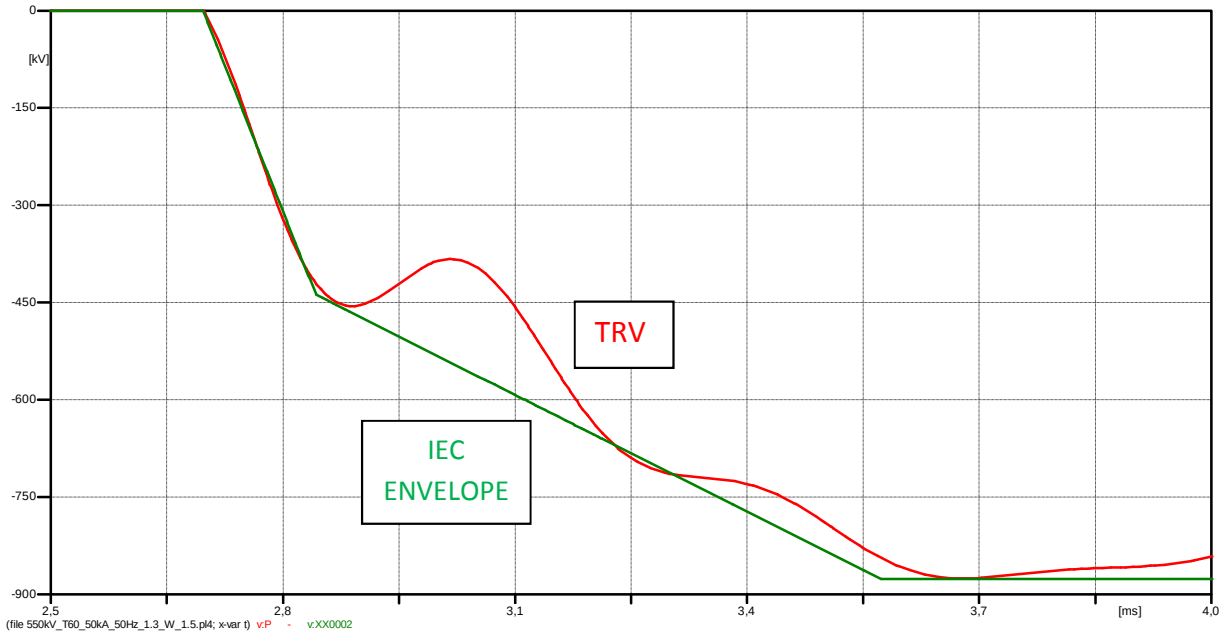
4 parameters TRV wave shapes, with tables containing the main components values and a comparison between ATP digital models and Standards TRV values are shown below.

8.2.2.1. Test - duty T60: I = 30 kA f = 50 Hz f.p.c.f. = 1.3

Test circuit parameters

U_h [kV]	C_h [μF]	L_h [mH]	C_1 [μF]	R_1 [Ω]	L_0 [mH]	C_0 [μF]	R_0 [Ω]	C_4 [μF]
960	6.2	65	3.1	65	18	0.25	80	0.01

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

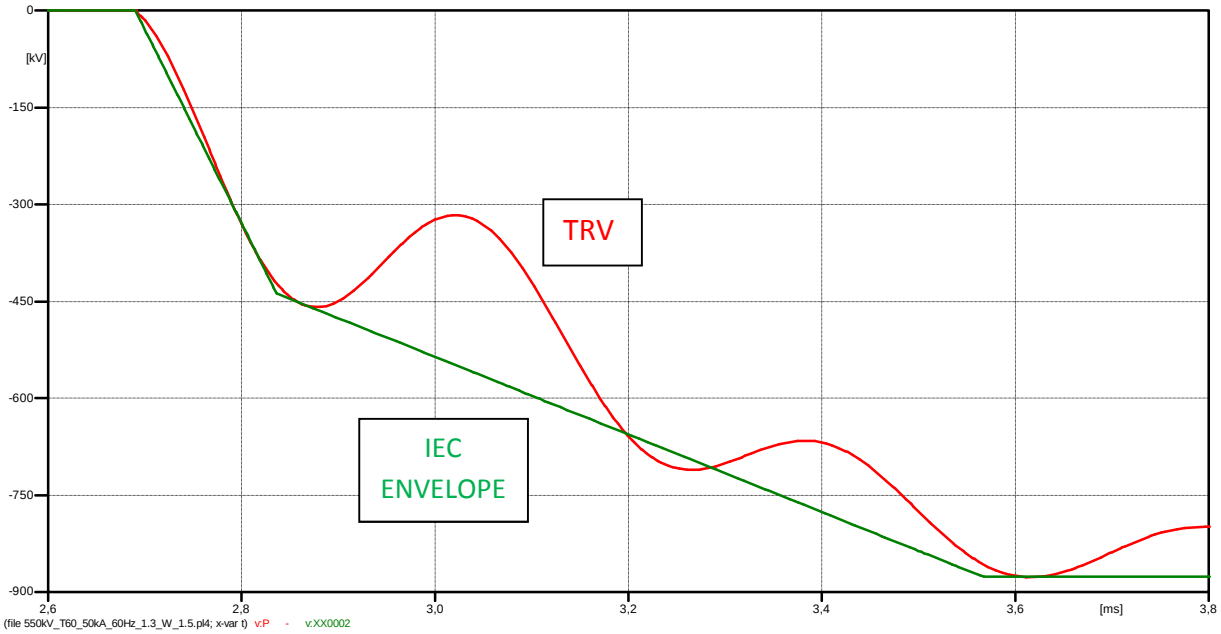
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	13.28	438	146	876	876
ATP model	250	13.96	425	140	865	860
% difference		5	-2.9	-4	-1.2	-1.8

8.2.2.2. Test - duty T60: I = 30 kA f = 60 Hz f.p.c.f. = 1.3

Test circuit parameters

U_h [kV]	C_h [μF]	L_h [mH]	C_1 [μF]	R_1 [Ω]	L_0 [mH]	C_0 [μF]	R_0 [Ω]	C_4 [μF]
815	8.7	46	3	40	15.5	0.29	35	0.008

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

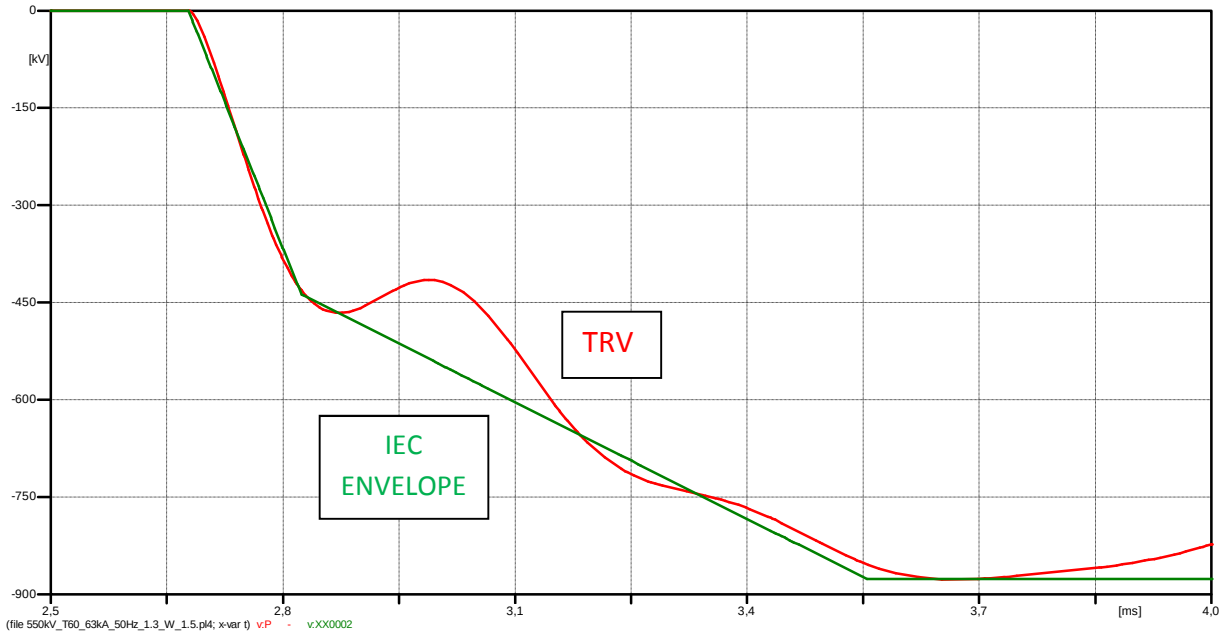
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	15.94	438	146	876	876
ATP model	251	16.65	422	141	860	870
% difference		4	-3.6	-3.4	-1.8	-0.7

8.2.2.3. Test - duty T60: I = 37.8 kA f = 50 Hz f.p.c.f. = 1.3

Test circuit parameters

U_h [kV]	C_h [μF]	L_h [mH]	C_1 [μF]	R_1 [Ω]	L_0 [mH]	C_0 [μF]	R_0 [Ω]	C_4 [μF]
960	7.6	52	3.7	60	15	0.27	110	0.05

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

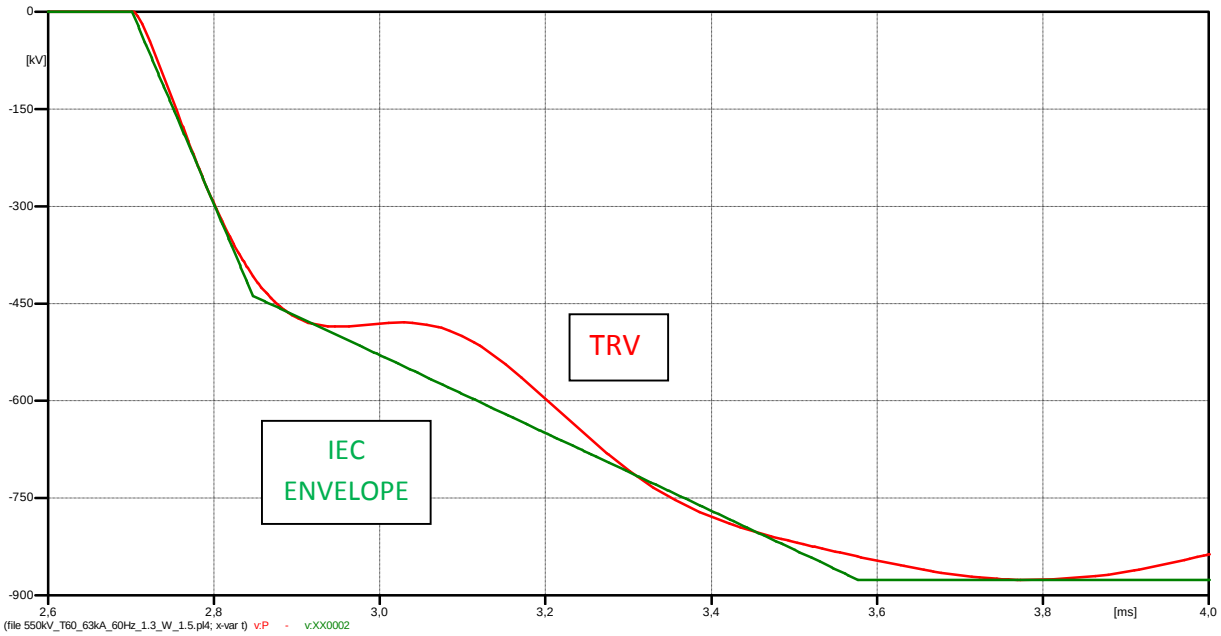
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	16.73	438	146	876	876
ATP model	253	17.4	420	139	870	890
% difference		4	-4.1	-4.7	-0.6	1.5

8.2.2.4. Test - duty T60: I = 37.8 kA f = 60 Hz f.p.c.f. = 1.3

Test circuit parameters

U_h [kV]	C_h [μF]	L_h [mH]	C_1 [μF]	R_1 [Ω]	L_0 [mH]	C_0 [μF]	R_0 [Ω]	C_4 [μF]
960	9.3	43.5	4.5	50	13	0.5	95	0.05

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

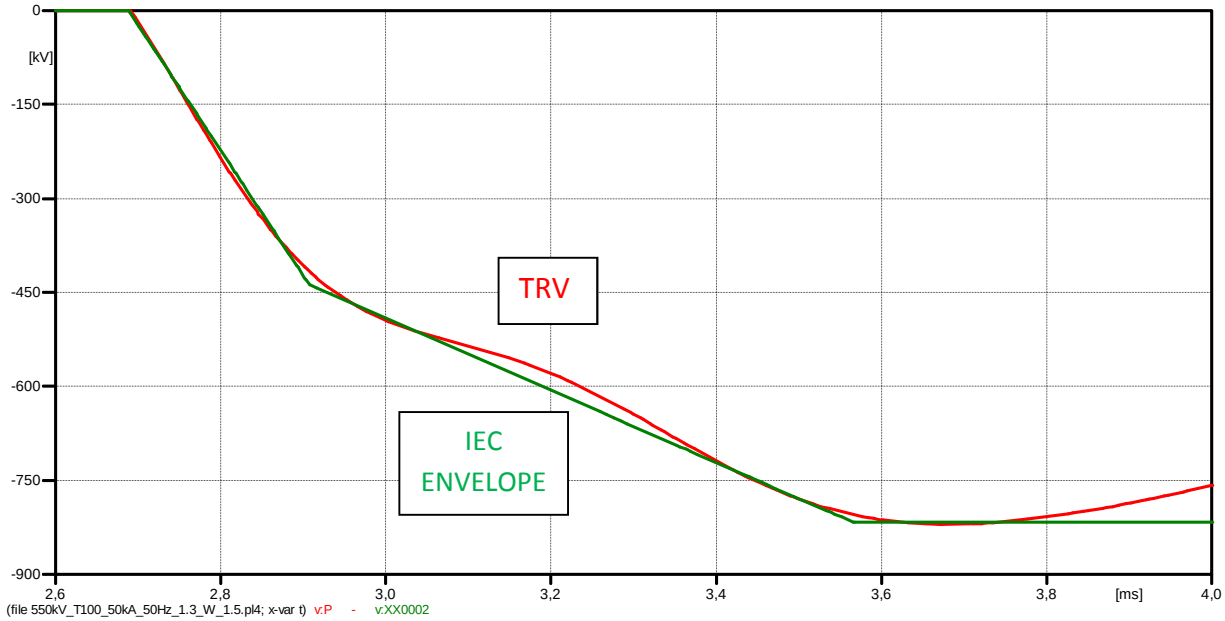
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	20.09	438	146	876	876
ATP model	250	20.91	418	146	845	875
% difference		3.9	-4.5	-	-3.5	-0.1

8.2.2.5. Test - duty T100: I = 50 kA f = 50 Hz f.p.c.f. = 1.3

Test circuit parameters

U_h [kV]	C_h [μF]	L_h [mH]	C_1 [μF]	R_1 [Ω]	L_0 [mH]	C_0 [μF]	R_0 [Ω]	C_4 [μF]
900	10.5	38	5.8	48	7.75	1.55	40	0.05

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

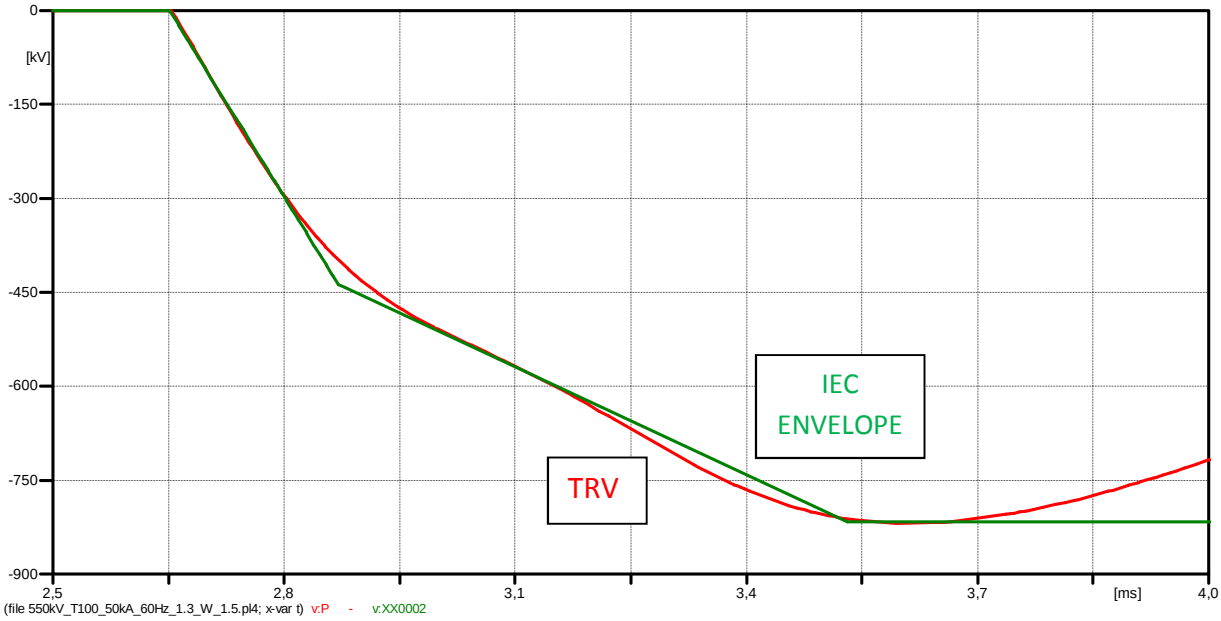
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	22.13	438	219	817	876
ATP model	251	22.63	421	220	808	875
% difference		2.2	-3.8	0.4	-1.1	-0.1

8.2.2.6. Test - duty T100: I = 50 kA f = 60 Hz f.p.c.f. = 1.3

Test circuit parameters

U_h [kV]	C_h [μF]	L_h [mH]	C_1 [μF]	R_1 [Ω]	L_0 [mH]	C_0 [μF]	R_0 [Ω]	C_4 [μF]
900	12	32	6.7	45	5	2.3	30	0.05

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

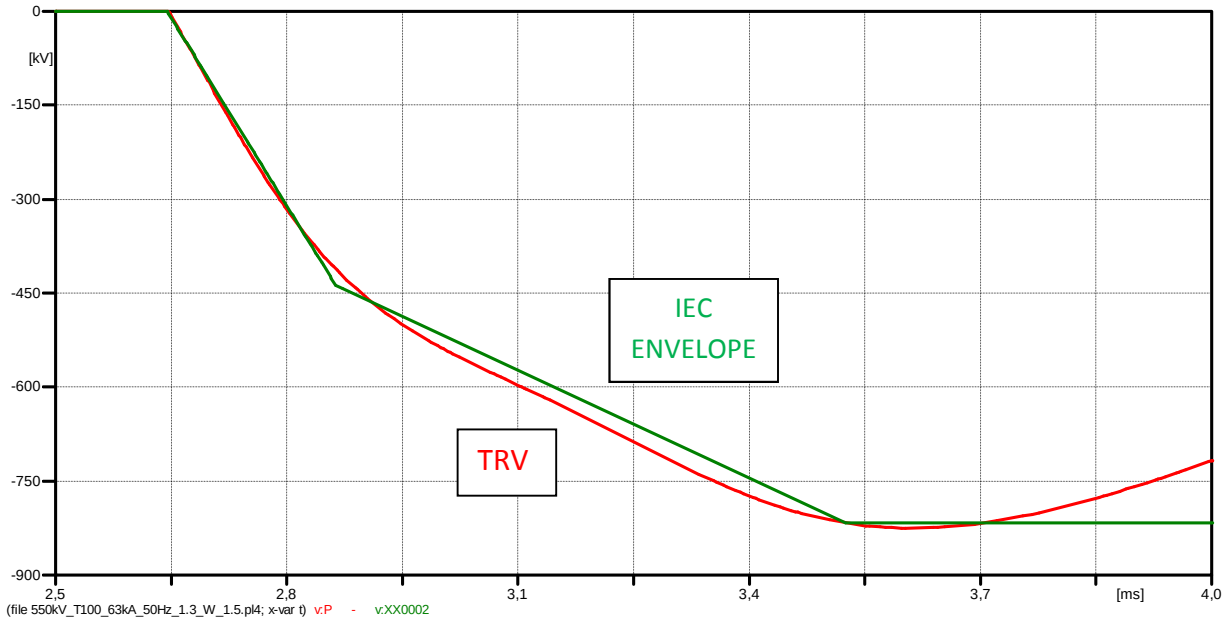
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	26.58	438	219	817	876
ATP model	256	26.69	417	227	800	839
% difference		-0.4	-4.8	-3.6	-2	-4.2

8.2.2.7. Test - duty T100: I = 63 kA f = 50 Hz f.p.c.f. = 1.3

Test circuit parameters

U_h [kV]	C_h [μF]	L_h [mH]	C_1 [μF]	R_1 [Ω]	L_0 [mH]	C_0 [μF]	R_0 [Ω]	C_4 [μF]
900	12.5	30.5	6.9	45	5	2.7	30	0.05

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

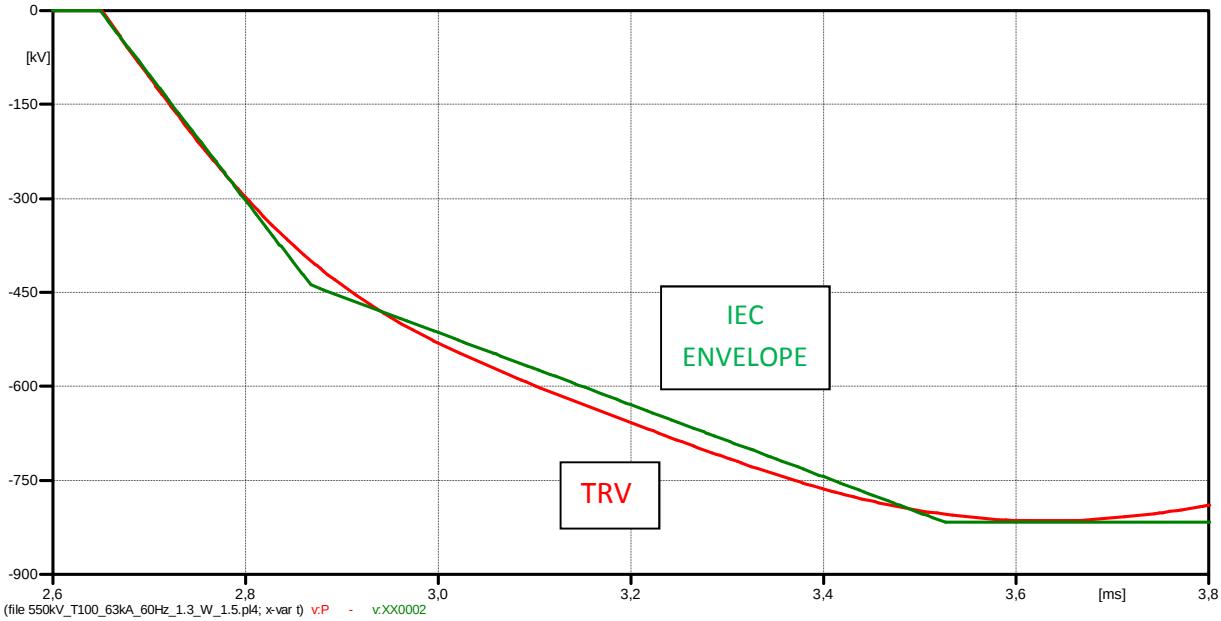
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	27.9	438	219	817	876
ATP model	257	28.04	416	212	801	835
% difference		0.5	-5	-3	-1.9	-4.6

8.2.2.8. Test - duty T100: I = 63 kA f = 60 Hz f.p.c.f. = 1.3

Test circuit parameters

U_h [kV]	C_h [µF]	L_h [mH]	C_1 [µF]	R_1 [Ω]	L_0 [mH]	C_0 [µF]	R_0 [Ω]	C_4 [µF]
900	15	25.5	8.3	37.5	4	4	25	0.05

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/µs]	U_1 [kV]	t_1 [µs]	U_c [kV]	t_2 [µs]
Standards values	250÷ 1000	33.48	438	219	817	876
ATP model	256	33.33	417	224	810	866
% difference		-0.4	-4.7	-2.2	-0.8	-1.1

8.2.3. Out-of-phase test

The equivalent ATP digital model used to obtain 550 kV TRV wave shapes is shown in *Fig*.8.6 and it is the same used to obtain 420 kV TRV wave shapes, since the same testing methods is taking into account.

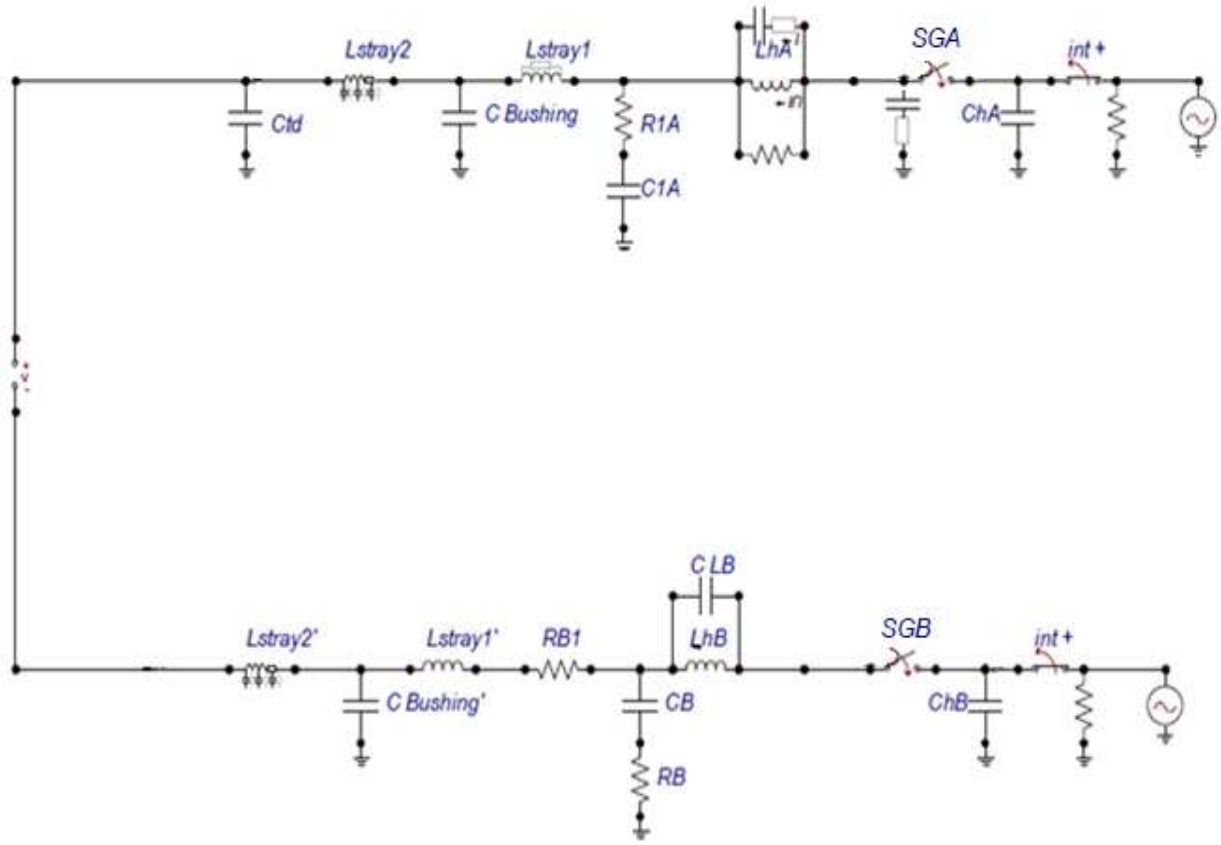


Figure 8.6 - ATP digital model

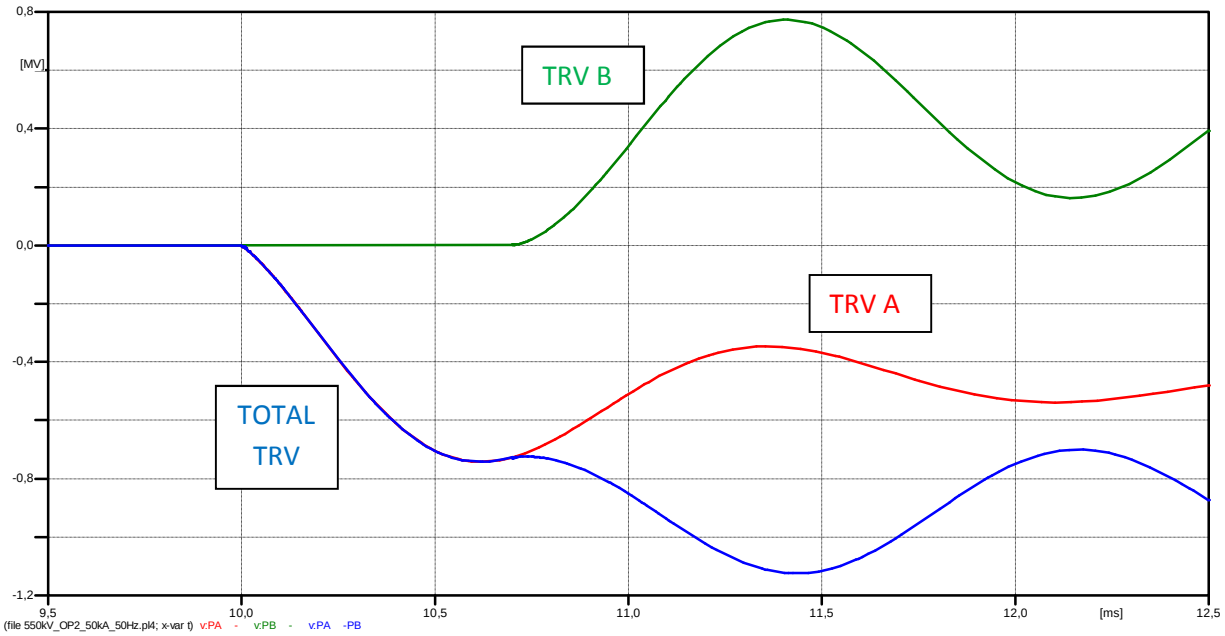
Test - duty OP2: I = 15.75 kA f = 50 Hz m.f. = 2

Test circuit parameters

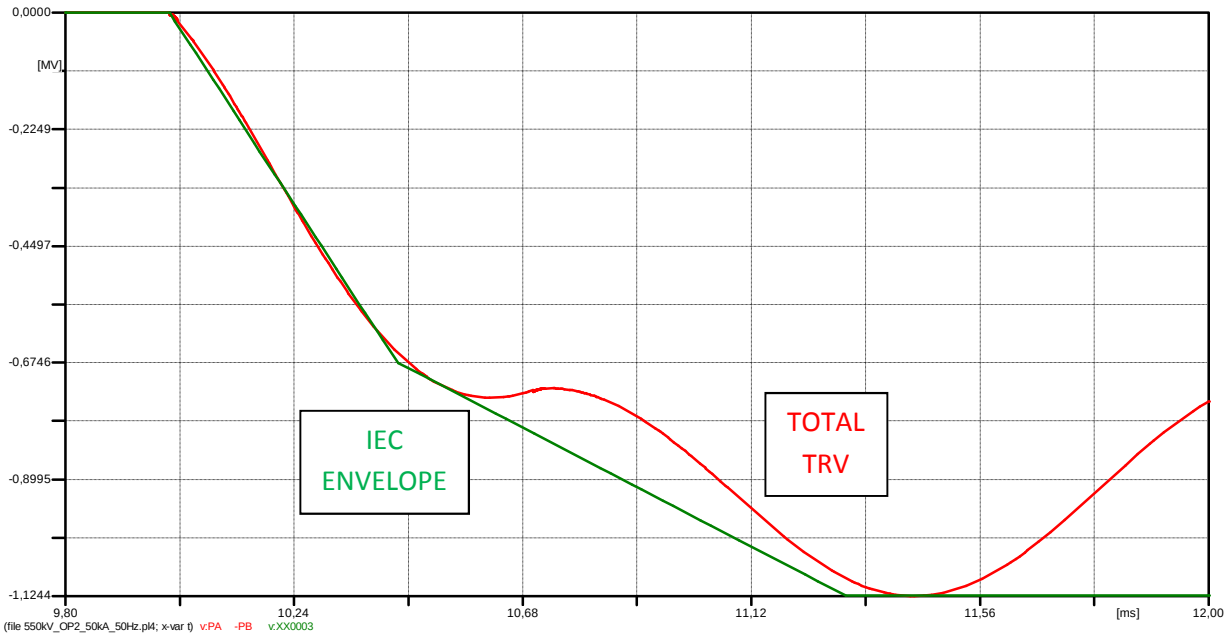
	U_h [kV]	C_h [µF]	L_h [mH]	C_1 [µF]	R_1 [Ω]	C_4 [µF]
Circuit A	550	4	100	0.6	200	0.01
Circuit B	500	2	200	0.3	150	0.021

R_p (R_{B1}): resistor of 360 Ω inserted in the circuit B for protection in case of over-voltages.

ATP DIGITAL MODEL
CIRCUIT A + CIRCUIT B



TOTAL TRV



Comparison between Standards values and ATP digital model

	Injected current (i_h)		**TRV**			
	f_h [Hz]	**di/dt [A/μs]**	**U_1 [kV]**	**t_1 [μs]**	**U_c [kV]**	**t_2 [μs]**
Standards values	250÷ 1000	7	674	438	1123	876÷ 1752
ATP model	620	7.2	655	440	1110	1361
% difference		-2.8	-2.8	0.4	-1.1	

8.2.4. Capacitive current switching

The equivalent ATP digital model used to obtain 550 kV TRV wave shapes is shown in *Fig*. 8.7 and it is the same used to obtain 420 kV TRV wave shapes, since the same testing methods is taking into account.

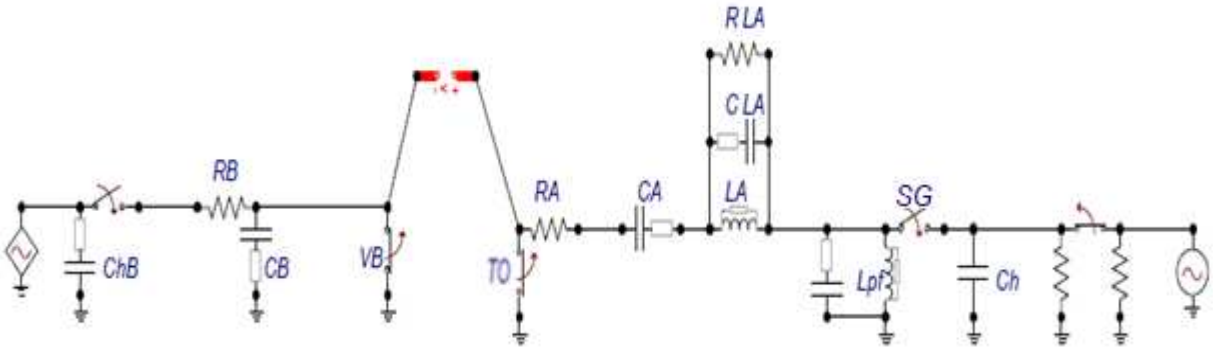


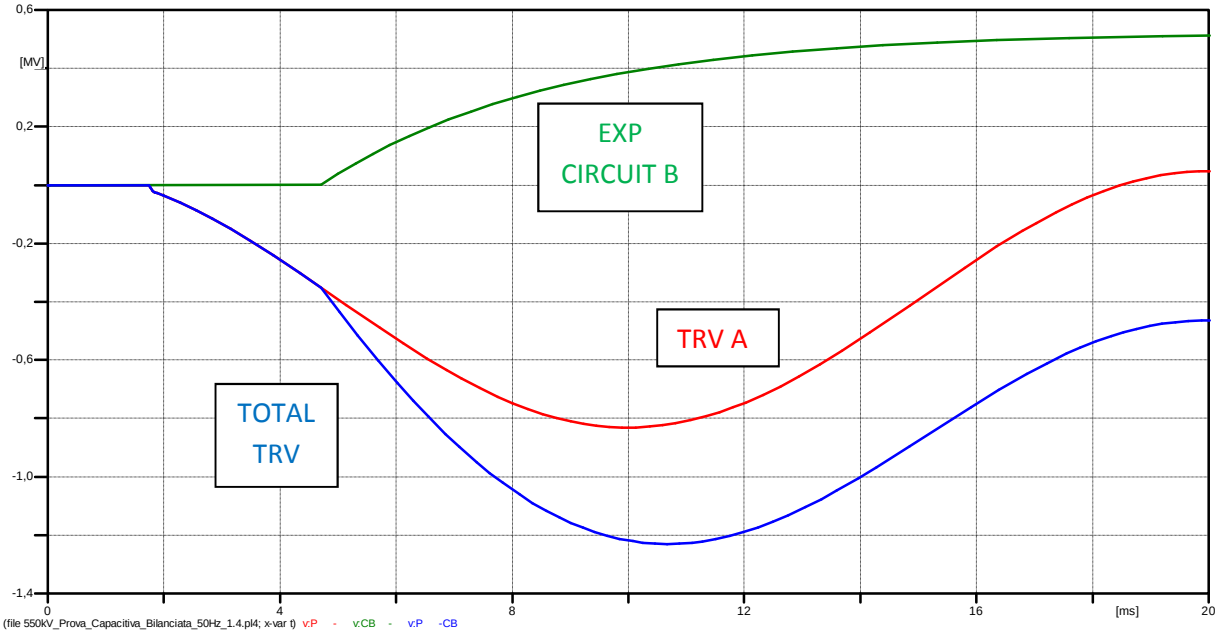
Figure 8.7 - ATP digital model

Test - duty LC2: I = 500 A f = 50 Hz k_c = 1.4

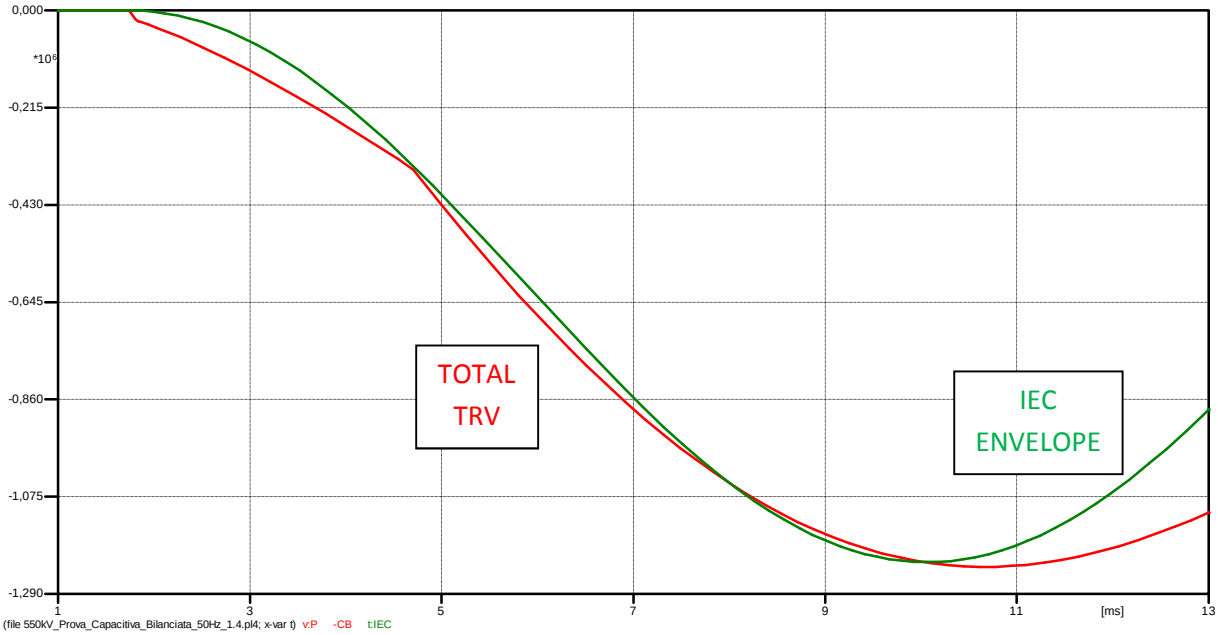
Test circuit parameters

	U_h [kV]	C_h [μF]	L_h [mH]	L [H]	C [μF]	R [Ω]
Circuit A	440	5.2	80	2000	0.25	1000
Circuit B	530	1.5	-	-	0.021	190000

ATP DIGITAL MODEL
CIRCUIT A + EXP CIRCUIT B



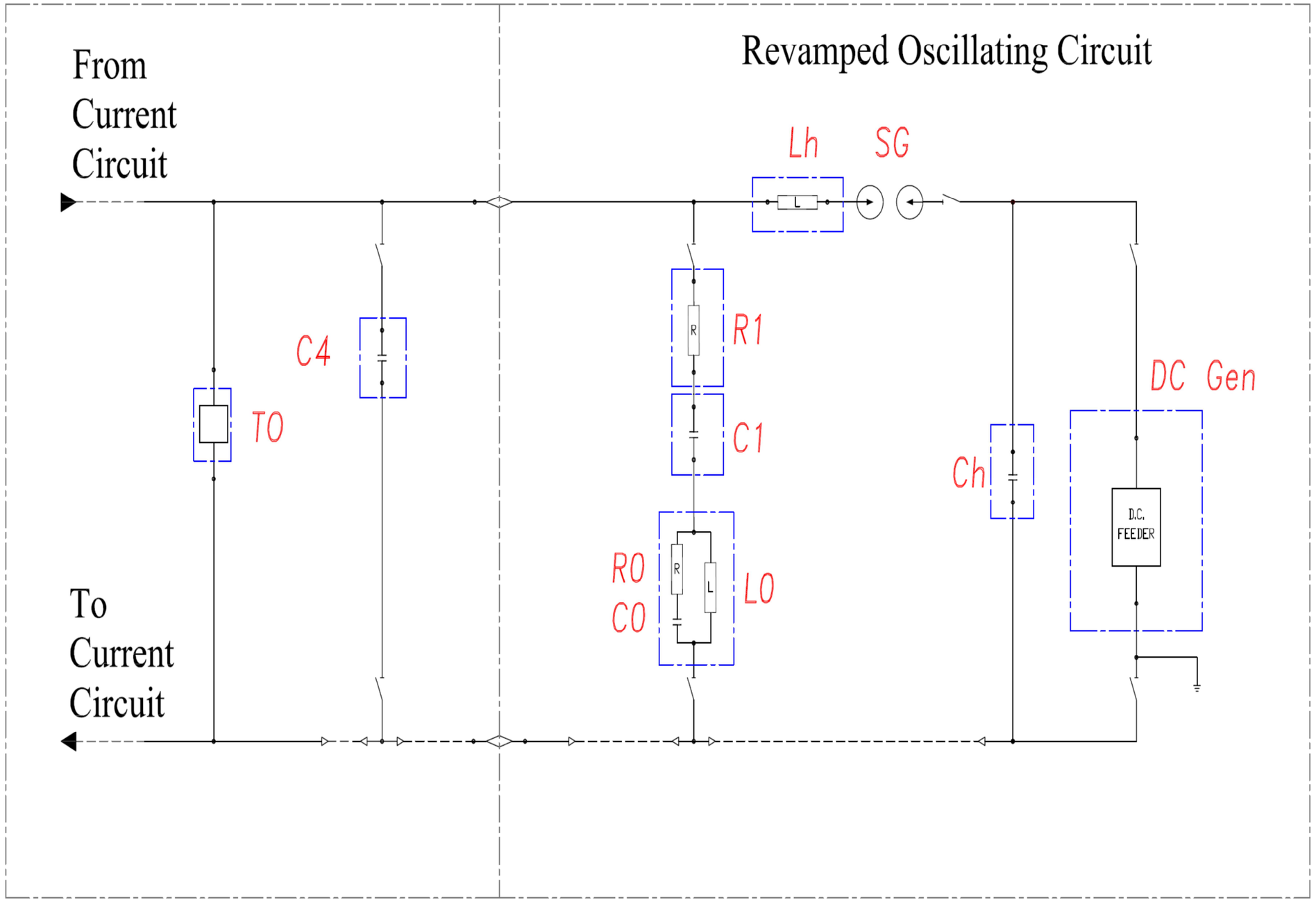
TOTAL TRV



Comparison between Standards values and ATP digital model

	Recovery voltage	
	U_c [kV]	**Time-to-peak [ms]**
Standards values	≤ 1224	10
ATP model	1224	10
% difference	-	-

8.3. Single Line Diagram of Revamping solution



8.4. Preliminary electrical specification of main components (Revamping solution)

8.4.1. Capacitor banks

Table 8.5 - Capacitor banks values

Label	Section	Function	Capacitor bank value [μF]	Rated voltage [kV]	Ground insulation [kV]
C_h - $C_{h(CAP)}$	Oscillating circuit	Main capacitor bank	1.3 ÷ 15	960 kV D.C. (Max charging voltage)	Not Required
C_1	Oscillating circuit	Bank for TRV control	0.013 ÷ 8.3	SIWV 950 kV_p	Not Required
C_0	Oscillating circuit	Bank for TRV control	0.25 ÷ 4	SIWV 300 kV_p	Not Required
C_{td} - $C_{B(CAP)}$	Test Bay	Time delay - exponential circuit	0.002 ÷ 0.05	SIWV 1050 kV_p	Not Required
$C_{hB(OP)}$ - $C_{A(CAP)}$	Oscillating circuit	Banks for OP-CAP test	0.25 ÷ 2	500 kV D.C. (Max charging voltage)	Not Required
$C_{hB(CAP)}$	Oscillating circuit	Banks for CAP test	1.5	550 kV D.C. (Max charging voltage)	Not Required

8.4.2. Reactor banks

Table 8.6 - Reactor banks values

Label	Section	Function	Reactor bank value [mH]	Rated voltage [kV]	Ground insulation [kV]	Energy [kJ]
L_h - $L_{hA(OP)}$ - $L_{A(CAP)}$	Oscillating circuit	Main reactor bank	25.5 ÷ 310	SIWV 1100 kV_p	1100 kV_p	5600
L_0	Oscillating circuit	Bank for TRV control	4 ÷ 18	SIWV 300 kV_p	Not Required	180
$L_{hB(OP)}$	Oscillating circuit	Bank for OP test	200	SIWV 800 kV_p	800 kV_p	30

8.4.3. Resistor banks

Table 8.7 - Resistor banks values

Label	Section	Function	Resistor bank value [Ω]	Rated voltage [kV]	Ground insulation [kV]	Energy [kJ]
R_1 - $R_{1A(OP)}$	Oscillating circuit	TRV control - OP test	37.5 ÷ 2600	SIWV 1100 kV_p	Not Required	2000
R_0	Oscillating circuit	Bank for TRV control	25 ÷ 110	SIWV 100 kV_p	Not Required	40
$R_{B(OP)}$	Oscillating circuit	Bank for OP test	150	SIWV 100 kV_p	100 kV_p	35
$R_{A(CAP)}$	Oscillating circuit	Bank for CAP test	1000	SIWV 400 kV_p	400 kV_p	20
$R_{B(CAP)}$	Oscillating circuit	Bank for CAP test	190000	SIWV 550 kV_p	550 kV_p	3

8.4.4. D.C. charging unit

Table 8.8 - D.C. charging unit characteristics

Label	Section	Function	Max charging voltage [kV]	Energy [kJ]	Charging time [s]
DC Gen	Oscillating circuit	Unit for main capacitor bank charging	1100	6100	60

8.5. Discussion of Revamping solution

8.5.1. Short-circuit simulations result

Tables at 8.2 report all test-duties executed by this circuit.

Table 8.1 and table 8.3 report test-duties executed taking into account the values requested by Standards, i.e. with a first-pole-to-clear factor equal to 1.3; digital simulations show that TRV wave shapes obtained are in accordance with TRV envelope defined by Standards. Thus this configuration is able to perform tests following standards requirements.

Table 8.2 and table 8.4 report test-duties executed taking into account the values required by some manufacturers (exceeding Standard requirements), i.e. with a first-pole-to-clear factor equal to 1.5; digital simulations show that TRVs of test-duties T30 are in accordance to TRV envelope (calculated with a first-pole-to-clear factor 1.5) but TRVs of test-duties T60 and T100 are not in accordance to the previously mentioned TRV envelope. This fact means that these test-duties may be used for development tests only, not for certification tests.

Digital simulations considered with a first-pole-to-clear-factor equal to 1.5 are:

- *Test - duty T30 $I = 15\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.5 ➔ PASSED*

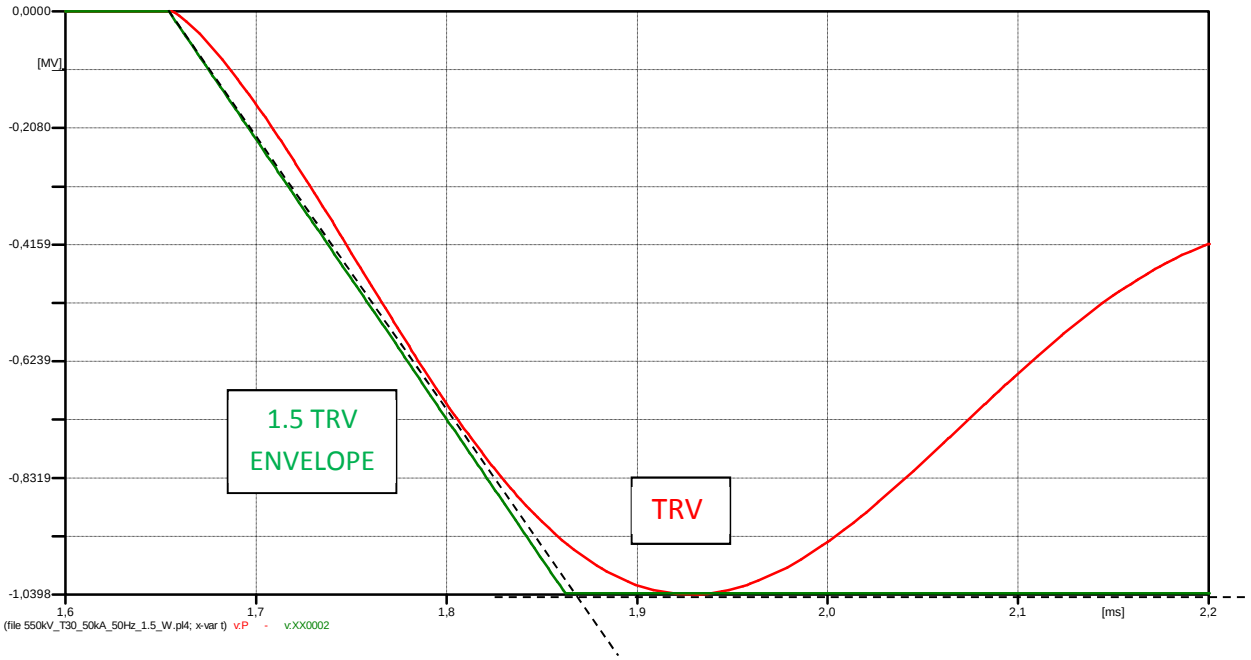
T30 TRV obtained faithfully reproduce TRV envelope (green) calculated with a first-pole to-clear factor equal to 1.5.

- *Test - duty T60 $I = 30\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.5 ➔ FAILED*
- *Test - duty T100 $I = 50\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.5 ➔ FAILED*

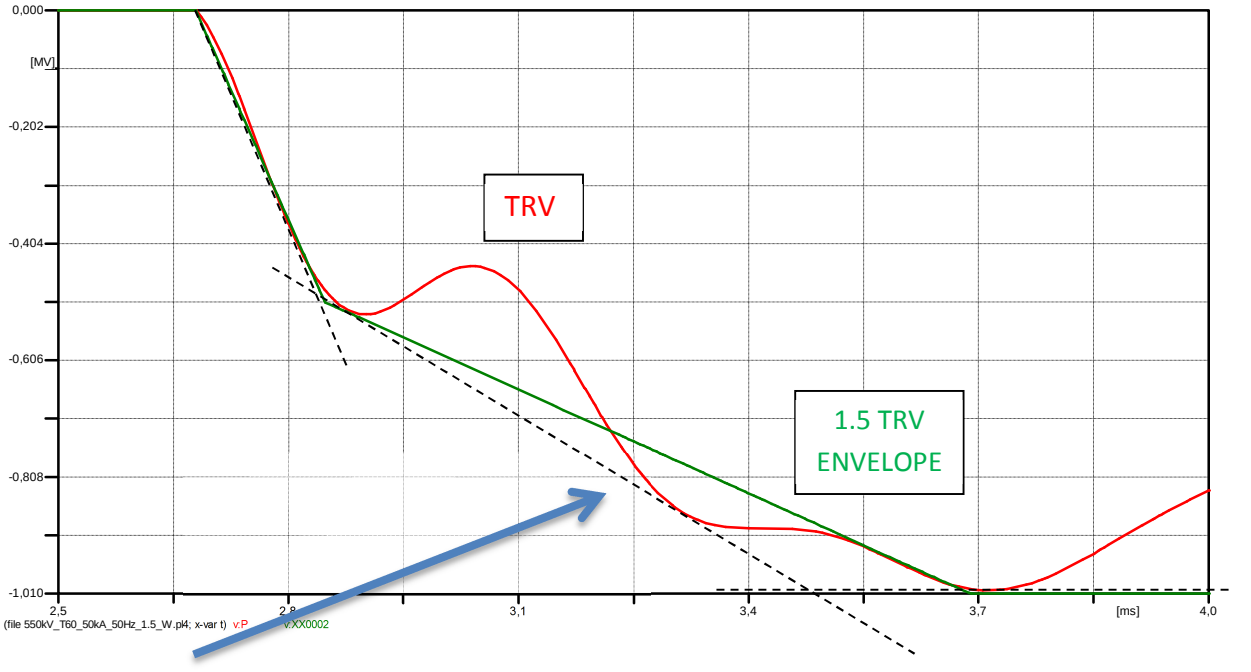
Test-duties T60 and T100 show a hardest TRV: values obtained are higher than Standards values reported to a first-pole-to-clear-factor equal to 1.5 (green envelope).

In the following pages the above mentioned digital simulation are shown. It's apparent that TRV wave shapes of test-duties T60 and T100 are not suitable for a certification test.

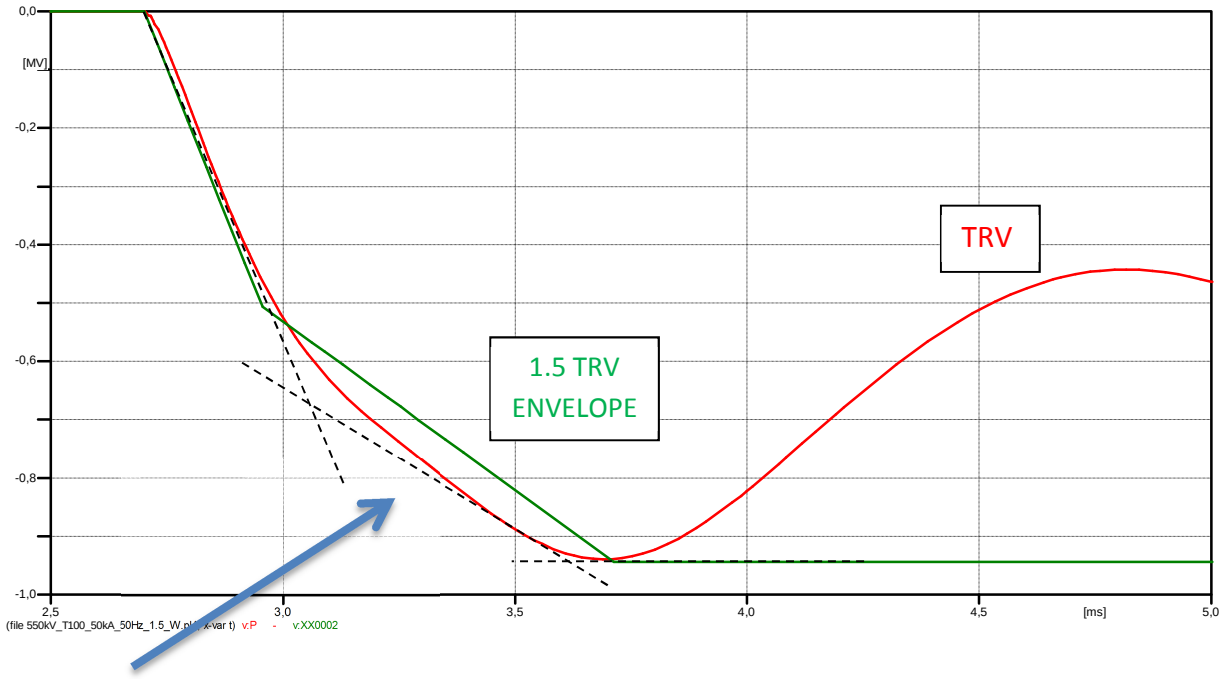
- *Test - duty T30 I = 15 kA f = 50 Hz f.p.c.f. = 1.5*



- *Test - duty T60 I = 30 kA f = 50 Hz f.p.c.f. = 1.5*



- *Test - duty T100 $I = 50\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.5*



8.5.2. Out-of-phase simulation result

Results obtained from digital simulation show that the obtained TRV wave shape is in accordance to TRV envelope defined by Standards maintaining the same testing method presently used at CESI.

8.5.3. Capacitive current switching simulation result

Results obtained from digital simulation show that the obtained TRV wave shape is in accordance to TRV envelope defined by Standards maintaining the same testing method presently used at CESI.

9. SECOND REPOWERING SOLUTION: NEW OSCILLATING CIRCUIT

9.1. New Oscillating Circuit solution

9.1.1. Solution description

The second solution taken in consideration to test 550 kV circuit-breakers is to add a new oscillating circuit to the Synthetic Laboratory.

The new oscillating circuit configuration is:

- parallel current injection method circuit, named “Weil” circuit, that provides 2/4 parameters TRV (it is the present oscillating circuit, without modification)
- new voltage injection circuit providing 2 parameters TRV.

This configuration has been proposed by KEMA Laboratories [6] and it is currently used to test circuit-breakers up to 1200 kV.

The figure below shows the new configuration (blue dots: the existing oscillating circuit; red dots: new oscillating circuit):

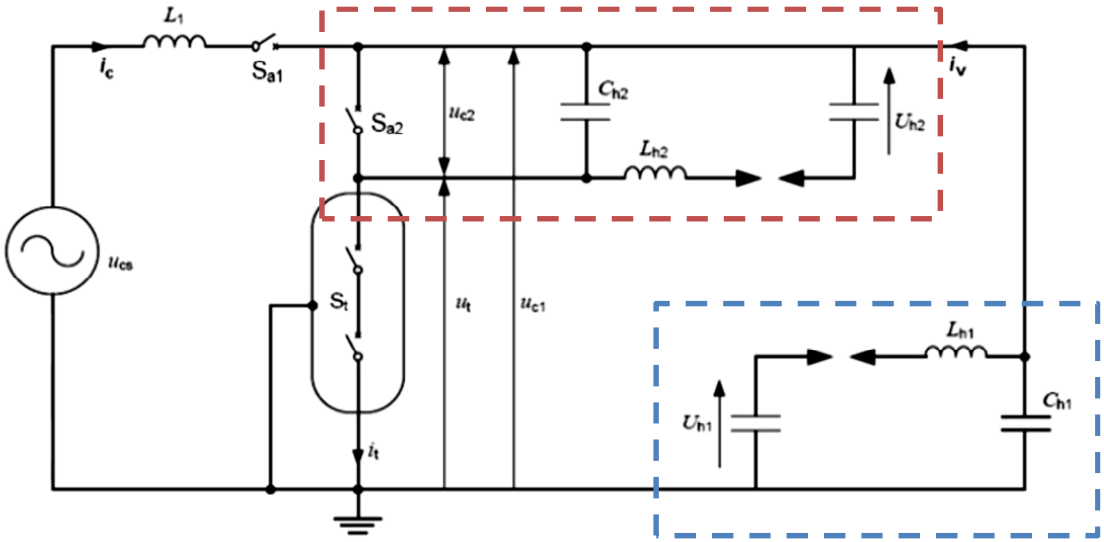


Figure 9.1 - Current injection + voltage injection method scheme (see fig.2 of STL guide for IEC 62271-101)

This High Voltage circuit is based on a combination of a current injection circuit and a voltage injection circuit; it applies the requested TRV to one terminal of the tested circuit-breaker, while the other is earthed.

The proper combination of 2 parameters TRVs supplied by the two High Voltage oscillating circuits, provides the requested 2/4 parameters TRV on the tested circuit-breaker.

9.1.2. Advantages of solution based on a new oscillating circuit

- A new test bay will be built between the existing oscillating circuit building and the new oscillating circuit building (see 9.4.). The present test bay remains unchanged; also the test rating remains unchanged (420 kV @ 63 kA).

- The present voltage circuit remains unchanged.

- This configuration allows to test all 550 kV circuit-breaker with first-pole-to-clear-factor equal to 1.5 (see following digital simulation results) up to 80 kA, that is the next standardized current after 63 kA value.
  In fact, with 2 short-circuit generators (see 9.1.3. – same power), the short-circuit power available in the test bay is

$$A = A1 + A2 = 2000\ MVA$$

  With 3 circuit-breakers connected in series (2 auxiliary breakers + 1 breaker under test) the voltage required is

$$V = 3 \cdot 2 \cdot 4 = 24\ kV$$ (see 9.1.3.)

  And the current available is

$$I = \frac{A}{V} = \frac{2000\ MVA}{24\ kV} > 80\ kA$$

- Future possibility to test 800 kV circuit-breakers by this circuit can be taken in consideration: in fact, no intrinsic physical limits relevant to oscillating circuit preclude future repowering of this Laboratory to test higher voltage circuit-breakers, maintaining this High Voltage circuit configuration.

9.1.3. Disadvantages of the solution based on a New oscillating circuit

- A new oscillating circuit is a space consuming solution: new buildings are needed to host:
  - oscillating circuit
  - auxiliary circuit-breakers and making switch
  - new test bay.

- This configuration needs higher power to perform tests than the configuration shown in previous chapter.
  In fact, by this configuration, the series of 3 circuit-breakers must be taken in account: 2 auxiliary circuit-breakers are required to be connected to the circuit-breaker under test (see *Fig.9.1*).

Auxiliary breakers are commonly equipped with 2 interruption chambers each (2 circuit-breakers = 4 interruption chambers). Circuit-breaker under test can be equipped with 1 or 2 interruption chamber, in function of the relevant configuration.
The maximum total number of interruption chambers is equal to 6.
Typically, in order to have a safe control of the energy during the arcing period, for each interruption chamber about 4kV are required. If the maximum number of interruption chamber in series is considered (6), the supply voltage required is:

$$V = 4\ kV/chamber \cdot 6\ chamber = 24\ kV.$$

The minimum power required in the test bay to perform tests is:

$$A\ (phase - to - phase) = V \cdot I = 24\ kV \cdot 63\ kA \cong 1500\ MVA.$$

These values (V and A) are not compatible with the maximum voltage provided by the present short-circuit generator:

$$V = 16\ kV$$

$$A = 1000\ MVA.$$

Hence, a second short-circuit generator is needed, connected in parallel to the existing one.

In this case the total power available in test bay should be 2000 MVA, sufficient to perform the tests.

Second short-circuit generator is a space consuming and capital intensive solution:

- ✓ Space consuming, mainly due to
  - o generator building,
  - o generator auxiliaries,
  - o short-circuit transformers.

- ✓ Capital intensive, mainly due to short-circuit generator and short-circuit transformers costs.

9.2. New oscillating circuit solution digital simulation results

Digital simulations considered are reported below:

- Short-Circuit 2 parameters TRV (values requested by Standards)

Table 9.1 - Short-Circuit 2 parameters TRV (values requested by Standards)

Short-circuit current [kA]	**Test-duty**	**Current [kA]**	**Frequency [Hz]**	k_{pp}	**Compliant to IEC 62271-100**
50	T10	5 (0.1·50)	50	1.5	YES
50	T10	5 (0.1·50)	60	1.5	YES
63	T10	6.3 (0.1·63)	50	1.5	YES
63	T10	6.3 (0.1·63)	60	1.5	YES
50	T30	15 (0.3·50)	50	1.3	YES
50	T30	15 (0.3·50)	60	1.3	YES
63	T30	18.9 (0.3·63)	50	1.3	YES
63	T30	18.9 (0.3·63)	60	1.3	YES

- Short-Circuit 2 parameters TRV (values requested by some manufacturers)

Table 9.2 - Short-Circuit 2 parameters TRV (values requested by some manufacturers)

Short-circuit current [kA]	**Test-duty**	**Current [kA]**	**Frequency [Hz]**	k_{pp}	**Compliant to IEC 62271-100**
50	T30	15 (0.3·50)	50	1.5	YES
50	T30	15 (0.3·50)	60	1.5	YES
63	T30	18.9 (0.3·63)	50	1.5	YES
63	T30	18.9 (0.3·63)	60	1.5	YES

- Short-Circuit 4 parameters TRV (values requested by Standards)

Table 9.3 - Short-Circuit 4 parameters TRV (values requested by Standards)

Short-circuit current [kA]	Test-duty	Current [kA]	Frequency [Hz]	k_{pp}	Compliant to IEC 62271-100
50	T60	30 (0.6·50)	50	1.3	YES
50	T60	30 (0.6·50)	60	1.3	YES
63	T60	37.8 (0.6·63)	50	1.3	YES
63	T60	37.8 (0.6·63)	60	1.3	YES
50	T100	50	50	1.3	YES
50	T100	50	60	1.3	YES
63	T100	63	50	1.3	YES
63	T100	63	60	1.3	YES

- Short-Circuit 4 parameters TRV (values requested by some manufacturers)

Table 9.4 - Short-Circuit 4 parameters TRV (values requested by some manufacturers)

Short-circuit current [kA]	Test-duty	Current [kA]	Frequency [Hz]	k_{pp}	Compliant to IEC 62271-100
50	T60	30 (0.6·50)	50	1.5	YES
50	T60	30 (0.6·50)	60	1.5	YES
63	T60	37.8 (0.6·63)	50	1.5	YES
63	T60	37.8 (0.6·63)	60	1.5	YES
50	T100	50	50	1.5	YES
50	T100	50	60	1.5	YES
63	T100	63	50	1.5	YES
63	T100	63	60	1.5	YES

- Out-of-phase
  - ✓ *Test - duty OP2* $I = 15.75\ kA$ $f = 50\ Hz$ $m.f. = 2$

- Capacitive current switching
  - ✓ *Test - duty LC2* $I = 500\ A$ $f = 50\ Hz$ $k_c = 1.4$

9.2.1. Short-circuit 2p TRV

The equivalent ATP digital model used to obtain 550 kV TRV wave shapes is shown in *Fig.9.2.*

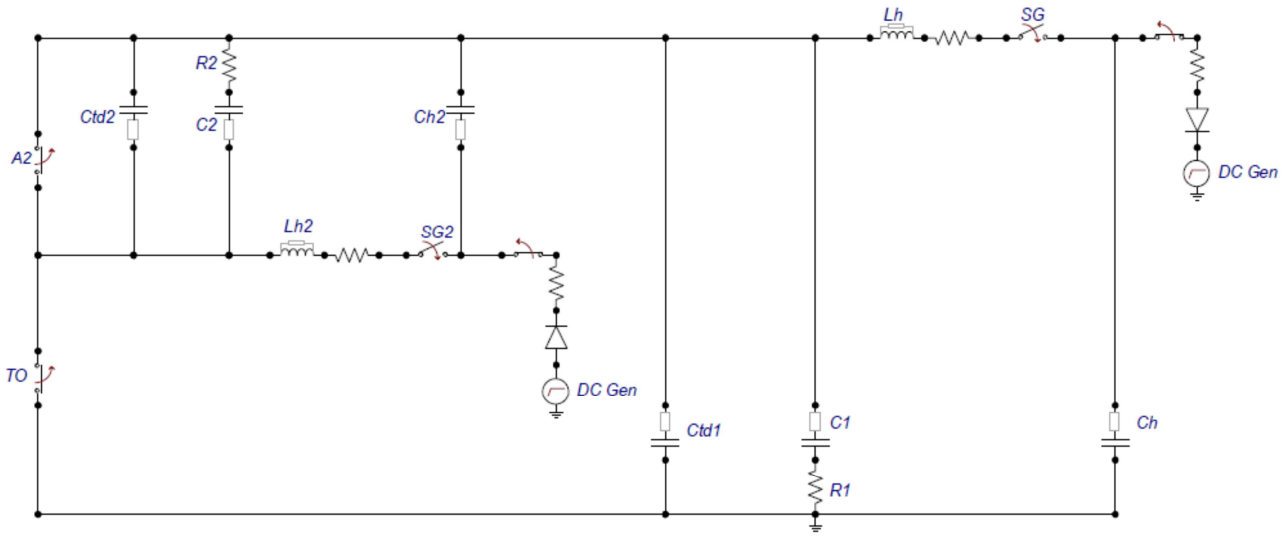


Figure 9.2 - ATP digital model

2 parameters TRV wave shapes, with tables containing the main components values and a comparison between ATP digital models and Standards TRV values are shown below.

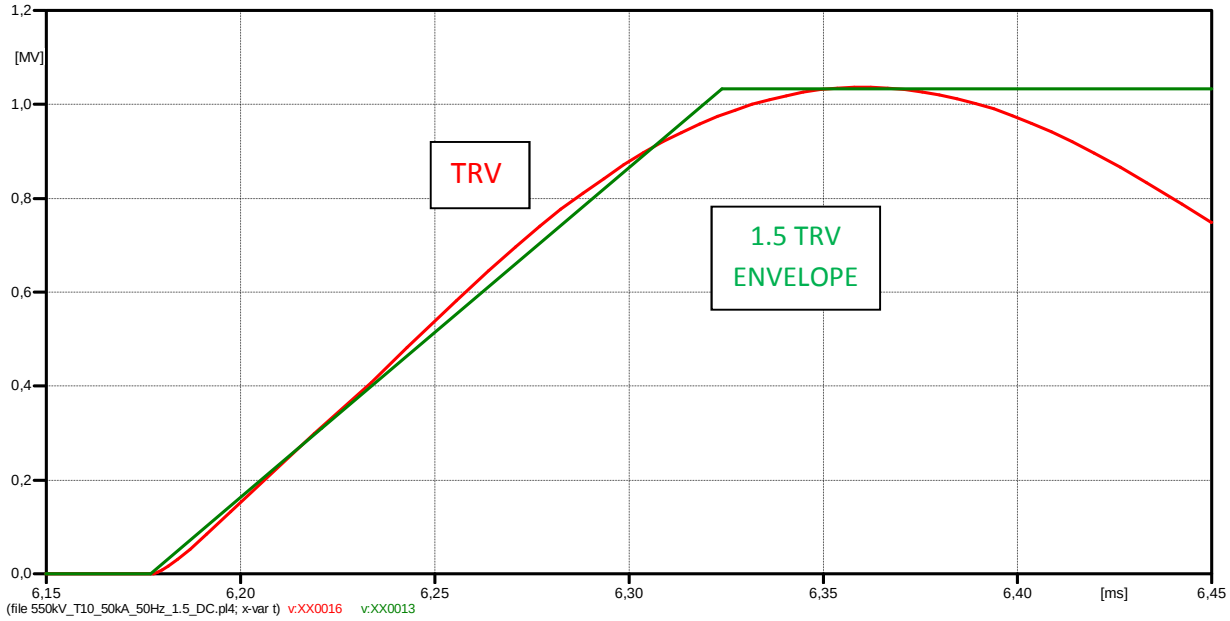
Even if all simulation have been executed, following Standards suggestions, in the next point only simulations relevant to 50 kA 50 Hz and 63 kA 60 Hz are reported.

9.2.1.1. Test - duty T10: I = 5 kA f = 50 Hz f.p.c.f. = 1.5

Test circuit parameters

	U_h [kV]	C_h [μF]	L_h [mH]	C [μF]	R [Ω]	C_{td} [μF]
Circuit 1	375	1.4	150	0.01	2700	0.001
Circuit 2	360	2	185	0.004	2500	0.01

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

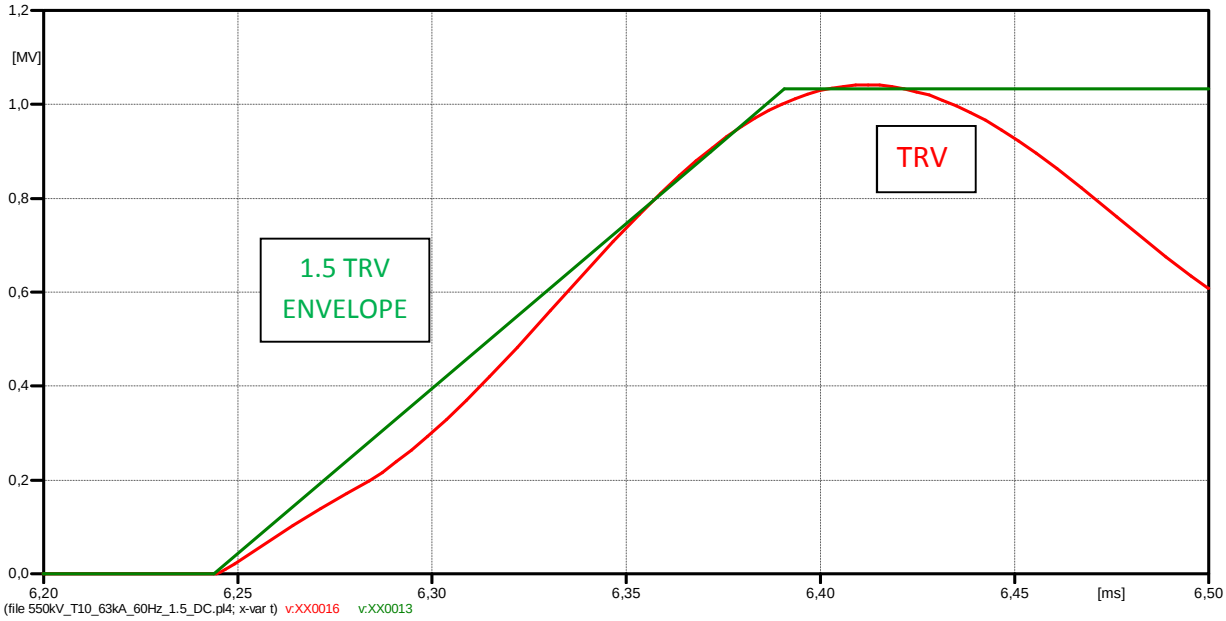
	Injected current (i_h)		TRV	
	f_h [Hz]	di/dt [A/μs]	U_c [kV]	t_3 [μs]
Standards values	250÷ 1000	2.2	1031	147
ATP model	347	2.3	985	140
% difference		-4.5	-4.4	-4.7

9.2.1.2. Test - duty T10: I = 6.3 kA f = 60 Hz f.p.c.f. = 1.5

Test circuit parameters

	U_h [kV]	C_h [μF]	L_h [mH]	C [μF]	R [Ω]	C_{td} [μF]
Circuit 1	375	2	115	0.06	1800	0.001
Circuit 2	310	2	130	0.004	2500	0.01

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

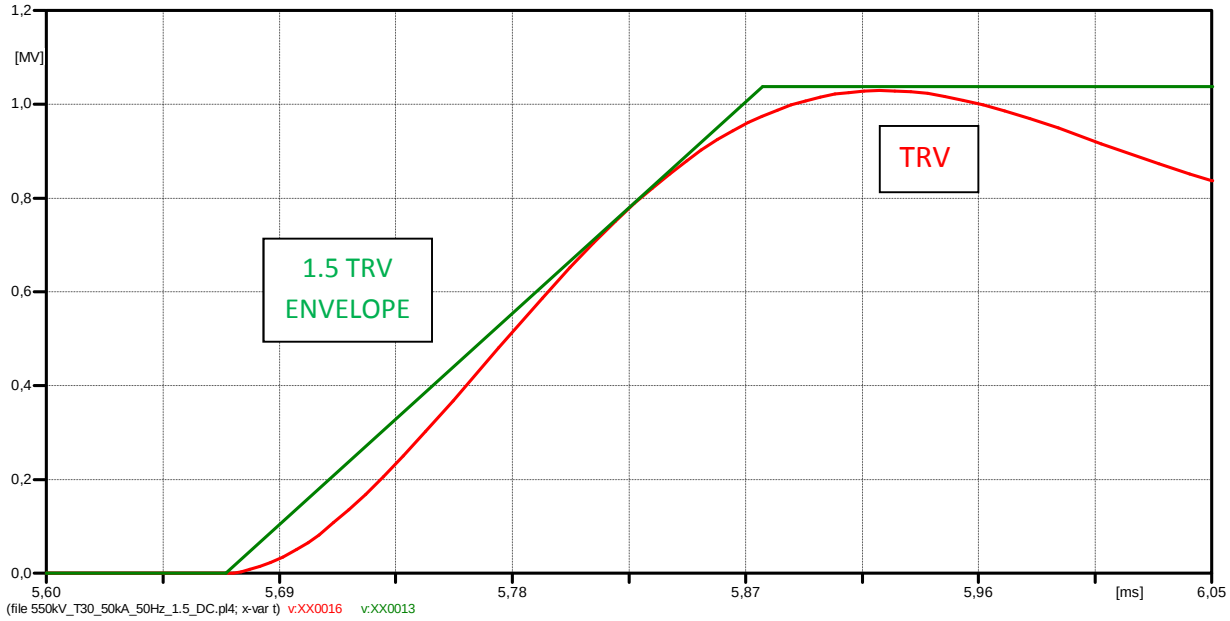
	Injected current (i_h)		TRV	
	f_h [Hz]	di/dt [A/μs]	U_c [kV]	t_3 [μs]
Standards values	250÷ 1000	3.35	1031	147
ATP model	332	3.22	1010	147
% difference		-3.8	-2	-

9.2.1.3. Test - duty T30: I = 15 kA f = 50 Hz f.p.c.f. = 1.5

Test circuit parameters

	U_h [kV]	C_h [µF]	L_h [mH]	C [µF]	R [Ω]	C_{td} [µF]
Circuit 1	430	1.355	65	0.06	470	0.03
Circuit 2	410	2	50	0.47	70	0.01

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

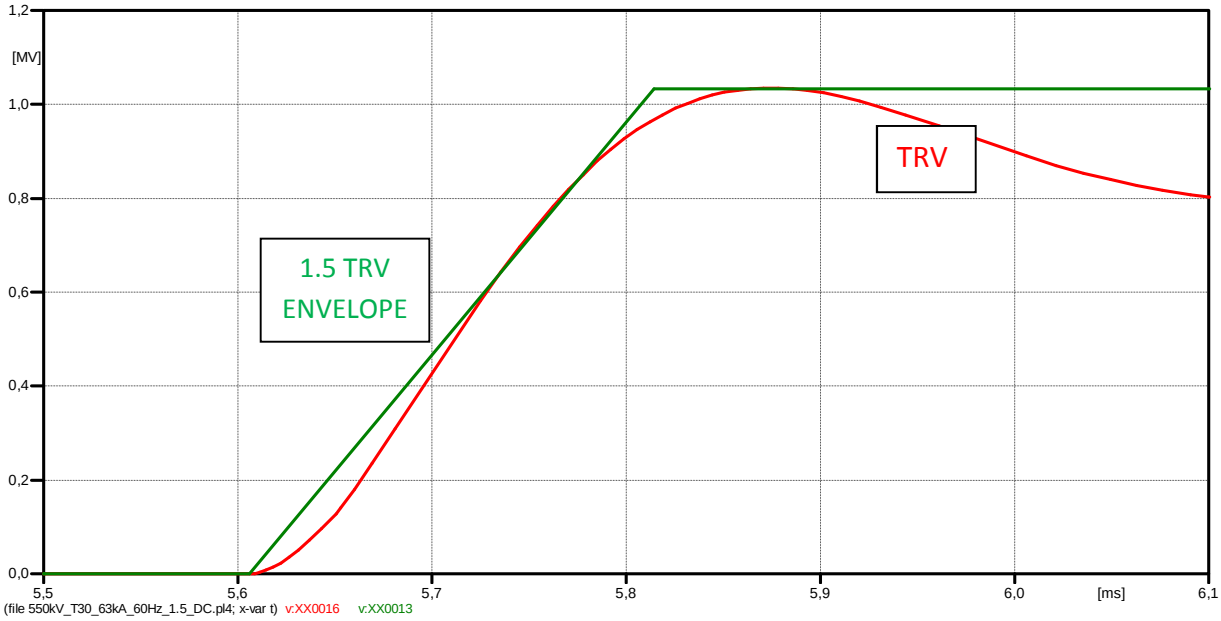
	Injected current (i_h)		TRV	
	f_h [Hz]	di/dt [A/µs]	U_c [kV]	t_3 [µs]
Standards values	250÷ 1000	6.64	1038	207
ATP model	441	6.55	990	208
% difference		-1.3	-4.3	-

9.2.1.4. Test - duty T30: I = 18.9 kA f = 60 Hz f.p.c.f. = 1.5

Test circuit parameters

	U_h [kV]	C_h [μF]	L_h [mH]	C [μF]	R [Ω]	C_{td} [μF]
Circuit 1	450	1.73	44.2	0.12	460	0.044
Circuit 2	420	2	40	0.5	100	0.01

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

	Injected current (i_h)		TRV	
	f_h [Hz]	di/dt [A/μs]	U_c [kV]	t_3 [μs]
Standards values	250÷ 1000	10.05	1038	207
ATP model	575	9.9	995	210
% difference		-1	-4	1.4

9.2.2. Short-circuit 4p TRV

The equivalent ATP digital model used to obtain 550 kV TRV wave shapes is shown in *Fig.9.3.*

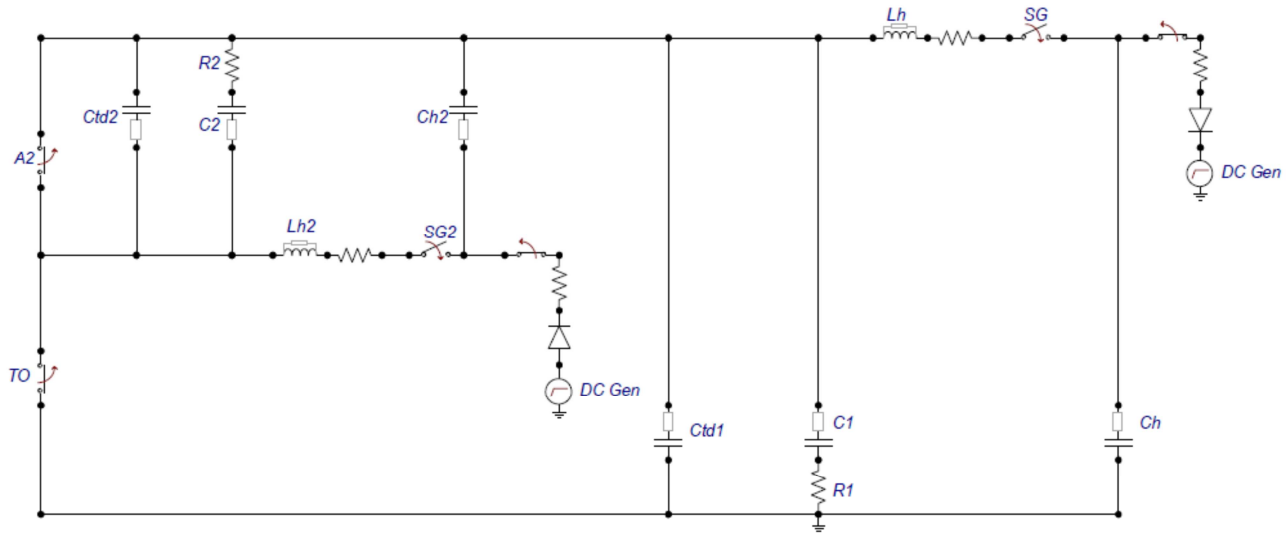


Figure 9.3 - ATP digital model

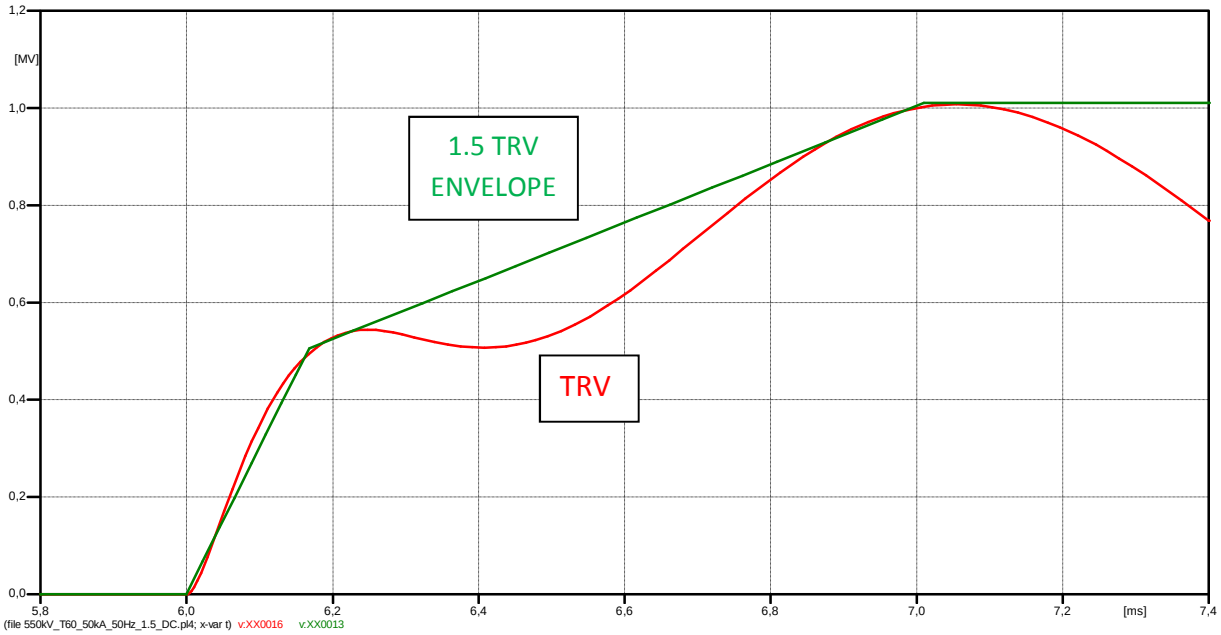
4 parameters TRV wave shapes, with tables containing the main components values and a comparison between ATP digital models and Standards TRV values are shown below.

9.2.2.1. Test - duty T60: I = 30 kA f = 50 Hz f.p.c.f. = 1.5

Test circuit parameters

	U_h [kV]	C_h [μF]	L_h [mH]	C [μF]	R [Ω]	C_{td} [μF]
Circuit 1	450	5	32.3	0.44	360	0.044
Circuit 2	445	2	100	0.85	20	0.01

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

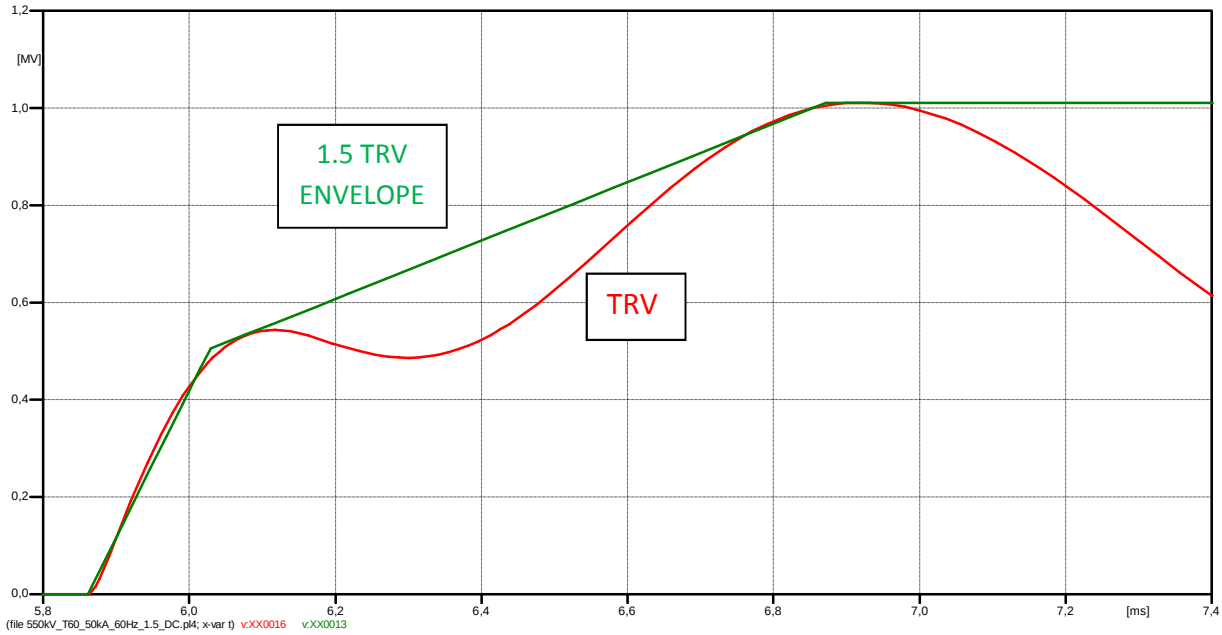
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	13.28	505	168	1010	1010
ATP model	396	13.62	485	162	997	1000
% difference		2.2	-3.9	-3.5	-1.2	-0.9

9.2.2.2. Test - duty T60: I = 30 kA f = 60 Hz f.p.c.f. = 1.5

Test circuit parameters

	U_h [kV]	C_h [μF]	L_h [mH]	C [μF]	R [Ω]	C_{td} [μF]
Circuit 1	440	5	25.6	0.5	240	0.044
Circuit 2	455	2	100	0.85	20	0.01

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

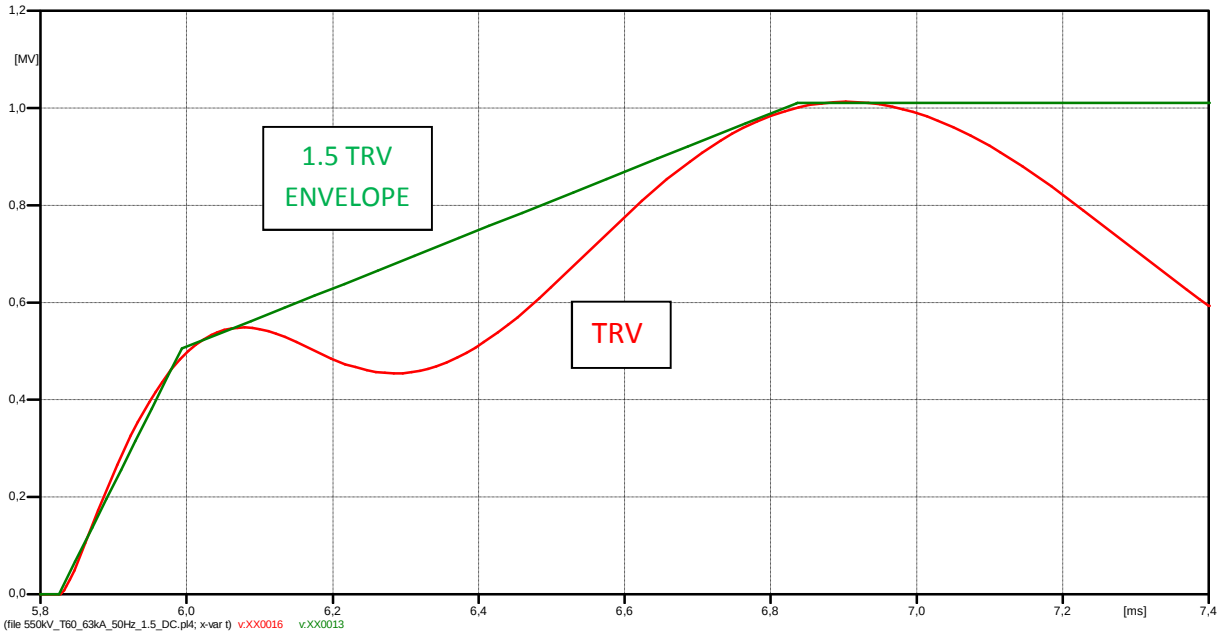
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	15.95	505	168	1010	1010
ATP model	445	16.63	481	165	995	1000
% difference		3.7	-4.8	-1.7	-1.5	-0.9

9.2.2.3. Test - duty T60: I = 37.8 kA f = 50 Hz f.p.c.f. = 1.5

Test circuit parameters

	U_h [kV]	C_h [μF]	L_h [mH]	C [μF]	R [Ω]	C_{td} [μF]
Circuit 1	440	5	24	0.5	220	0.044
Circuit 2	450	2	100	0.81	20	0.01

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

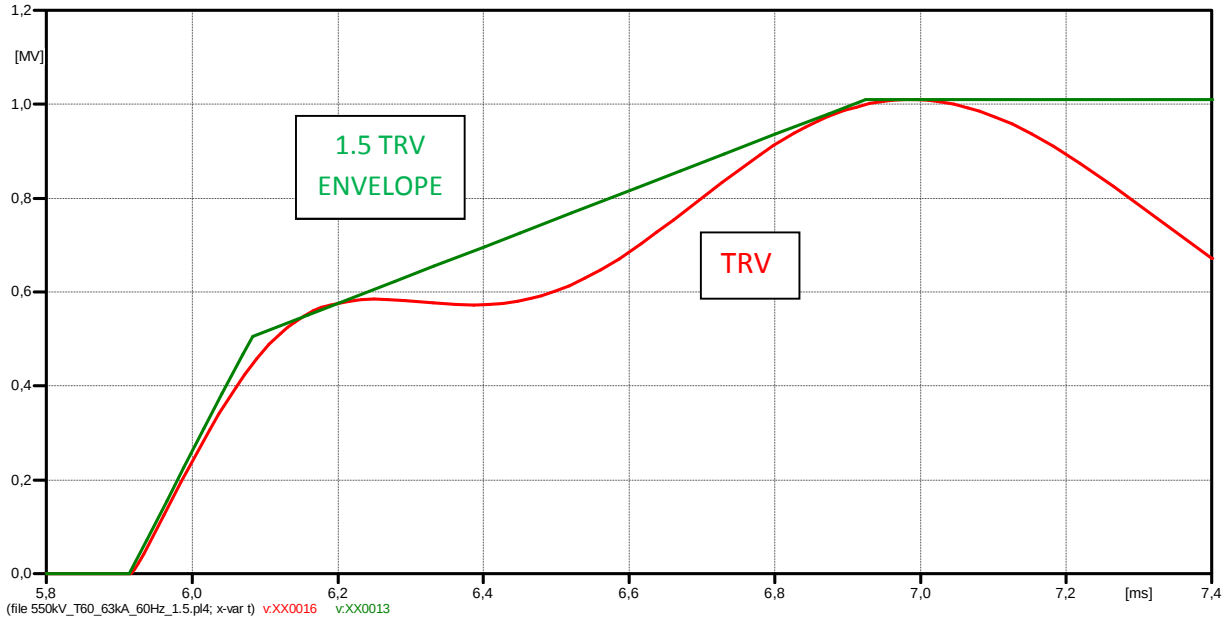
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	16.73	505	168	1010	1010
ATP model	460	17.81	482	162	1010	1010
% difference		5	-4.5	-3.5	-	-

9.2.2.4. Test - duty T60: I = 37.8 kA f = 60 Hz f.p.c.f. = 1.5

Test circuit parameters

	U_h [kV]	C_h [µF]	L_h [mH]	C [µF]	R [Ω]	C_{td} [µF]
Circuit 1	460	6.26	22.4	0.75	142	0.044
Circuit 2	450	2	100	0.9	20	0.01

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

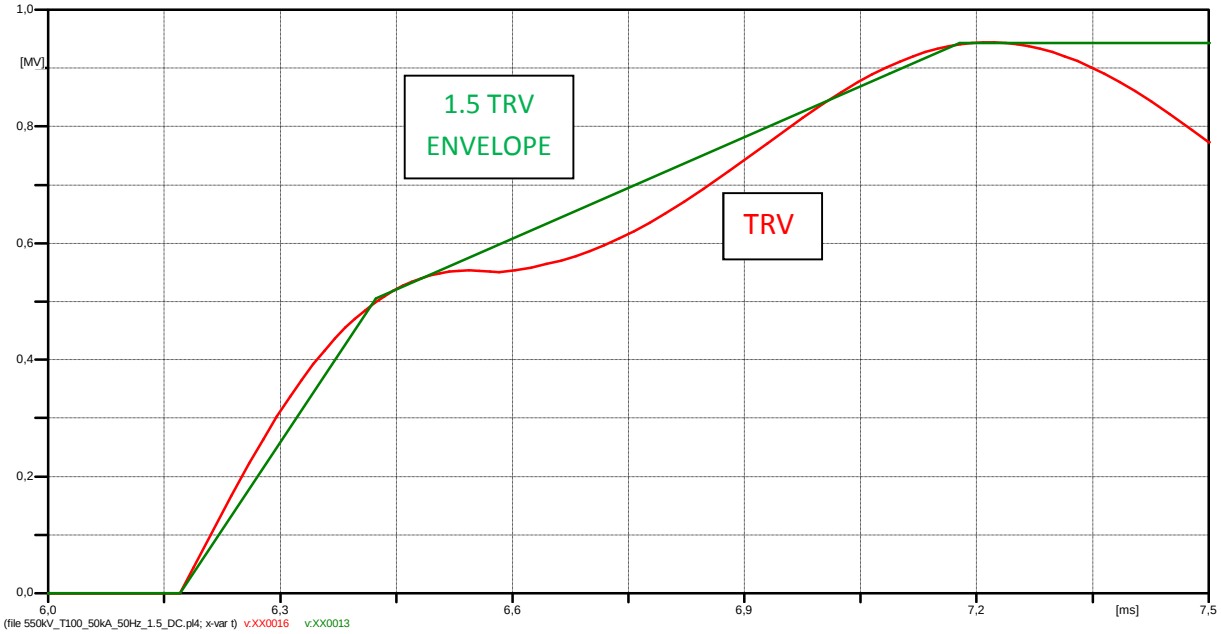
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/µs]	U_1 [kV]	t_1 [µs]	U_c [kV]	t_2 [µs]
Standards values	250÷ 1000	20.15	505	168	1010	1010
ATP model	425	19.43	500	175	1000	1000
% difference		-2.9	-0.9	4.1	-0.9	-0.9

9.2.2.5. Test - duty T100: I = 50 kA f = 50 Hz f.p.c.f. = 1.5

Test circuit parameters

	U_h [kV]	C_h [μF]	L_h [mH]	C [μF]	R [Ω]	C_{td} [μF]
Circuit 1	465	10.4	20	1.4	110	0.001
Circuit 2	440	1	160	0.38	130	0.006

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

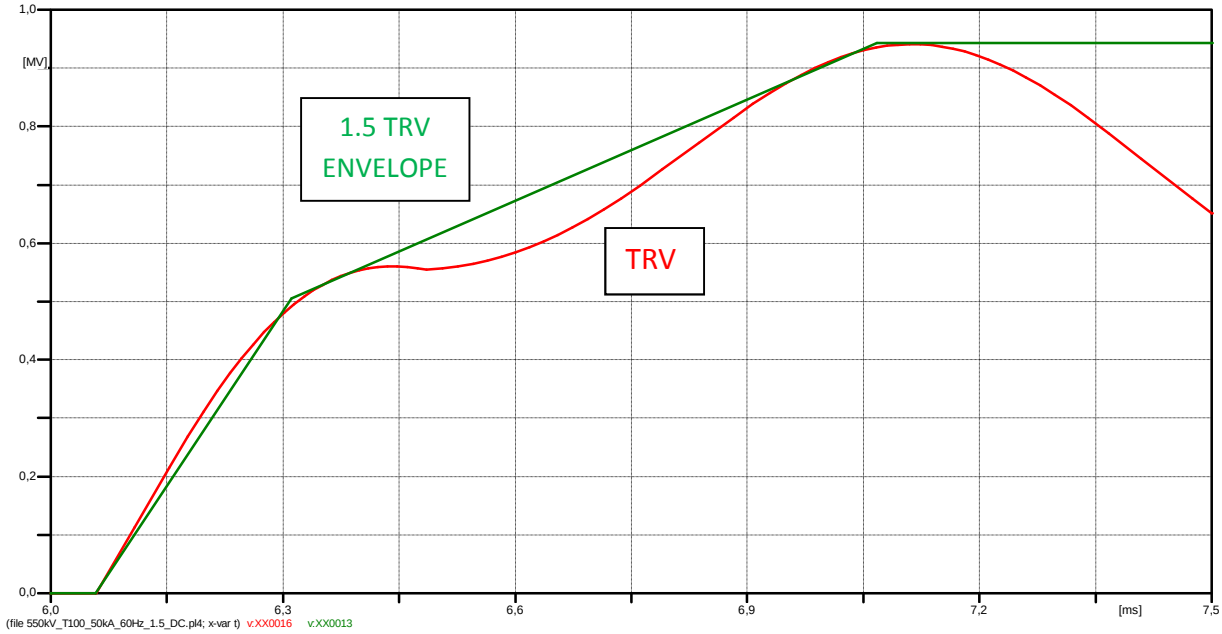
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	22.2	505	253	942	1010
ATP model	349	22.3	485	240	935	995
% difference		-0.4	-3.9	-5	-0.7	-1.9

9.2.2.6. Test - duty T100: I = 50 kA f = 60 Hz f.p.c.f. = 1.5

Test circuit parameters

	U_h [kV]	C_h [μF]	L_h [mH]	C [μF]	R [Ω]	C_{td} [μF]
Circuit 1	465	10.4	17	1.65	80	0.001
Circuit 2	440	1	160	0.35	130	0.006

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

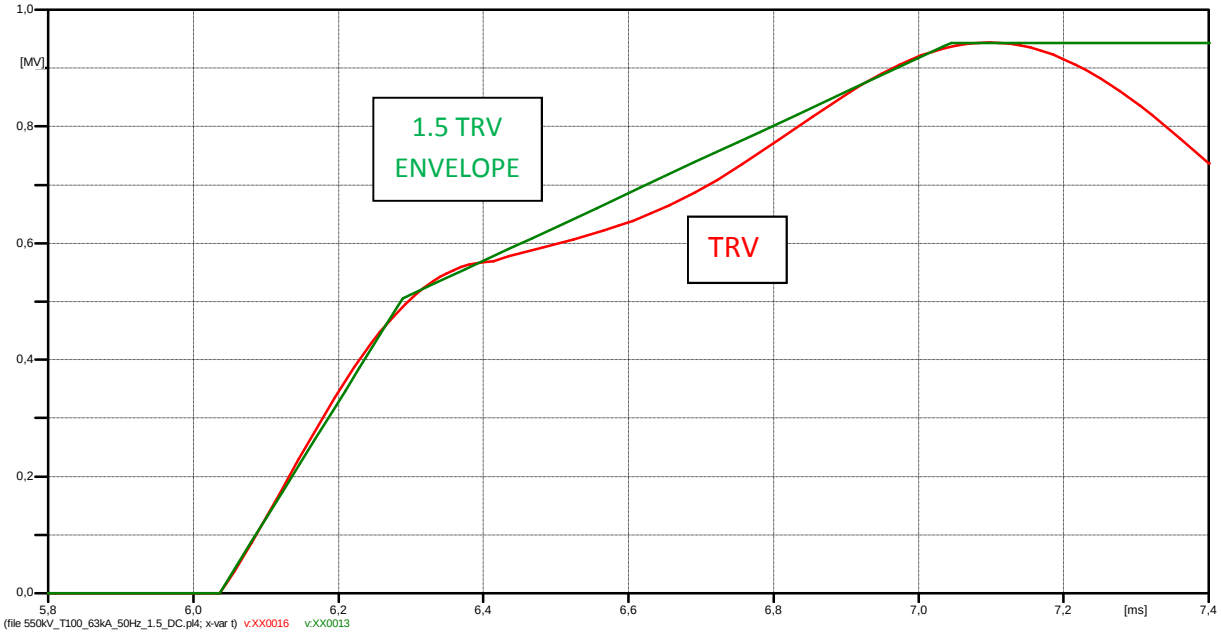
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	26.58	505	253	942	1010
ATP model	380	26.36	480	245	940	1005
% difference		-0.8	-4.9	-3.1	-0.2	-0.4

9.2.2.7. Test - duty T100: I = 63 kA f = 50 Hz f.p.c.f. = 1.5

Test circuit parameters

	U_h [kV]	C_h [μF]	L_h [mH]	C [μF]	R [Ω]	C_{td} [μF]
Circuit 1	450	11.4	15	1.65	60	0.001
Circuit 2	465	1	160	0.4	120	0.006

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

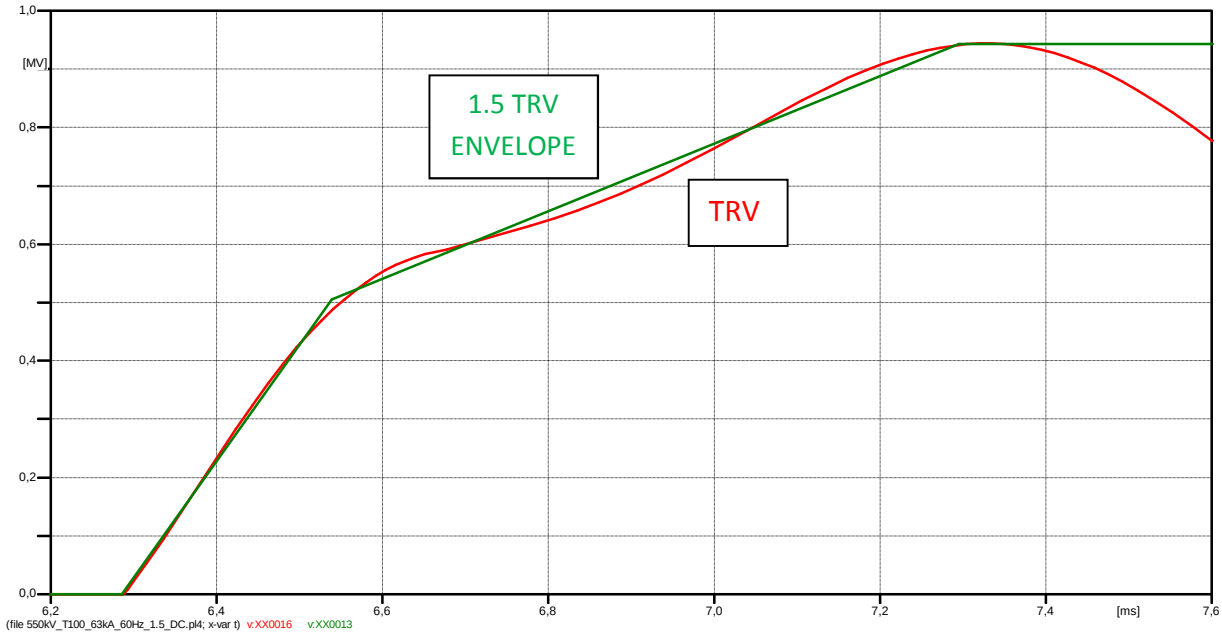
	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/μs]	U_1 [kV]	t_1 [μs]	U_c [kV]	t_2 [μs]
Standards values	250÷ 1000	27.89	505	253	942	1010
ATP model	385	29.25	495	245	940	1010
% difference		4.8	-1.9	-3.1	-	-

9.2.2.8. Test - duty T100: I = 63 kA f = 60 Hz f.p.c.f. = 1.5

Test circuit parameters

	U_h [kV]	C_h [µF]	L_h [mH]	C [µF]	R [Ω]	C_{td} [µF]
Circuit 1	470	18	13.5	2.16	55	0.044
Circuit 2	400	1	210	0.25	100	0.01

ATP DIGITAL MODEL



Comparison between Standards values and ATP digital model

	Injected current (i_h)		TRV			
	f_h [Hz]	di/dt [A/µs]	U_1 [kV]	t_1 [µs]	U_c [kV]	t_2 [µs]
Standards values	250÷ 1000	33.48	505	253	942	1010
ATP model	323	32.73	490	250	930	995
% difference		-2.1	-2.9	-1.2	-1.3	-1.5

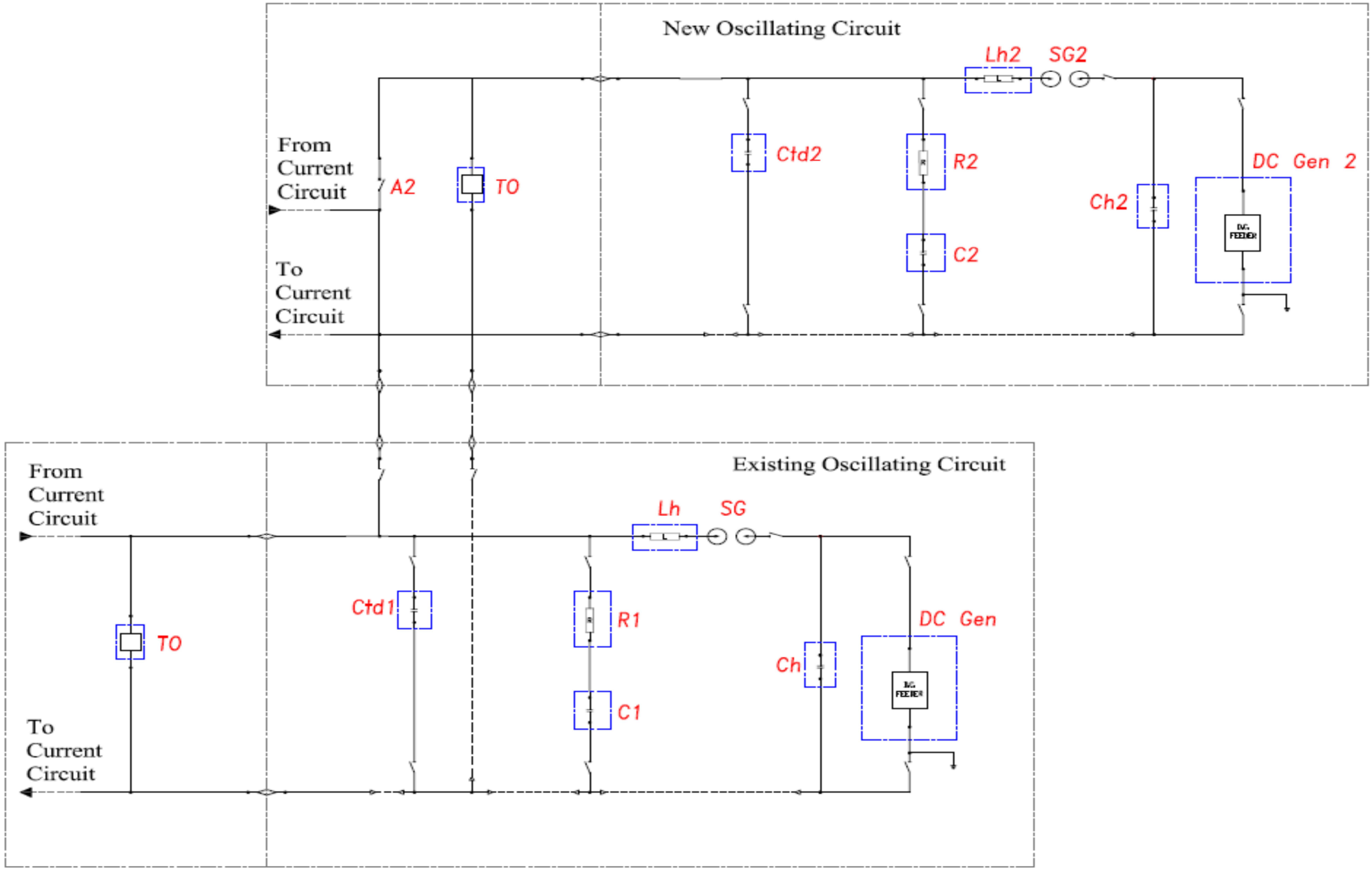
9.2.3. Out-of-phase test

See 8.2.3.

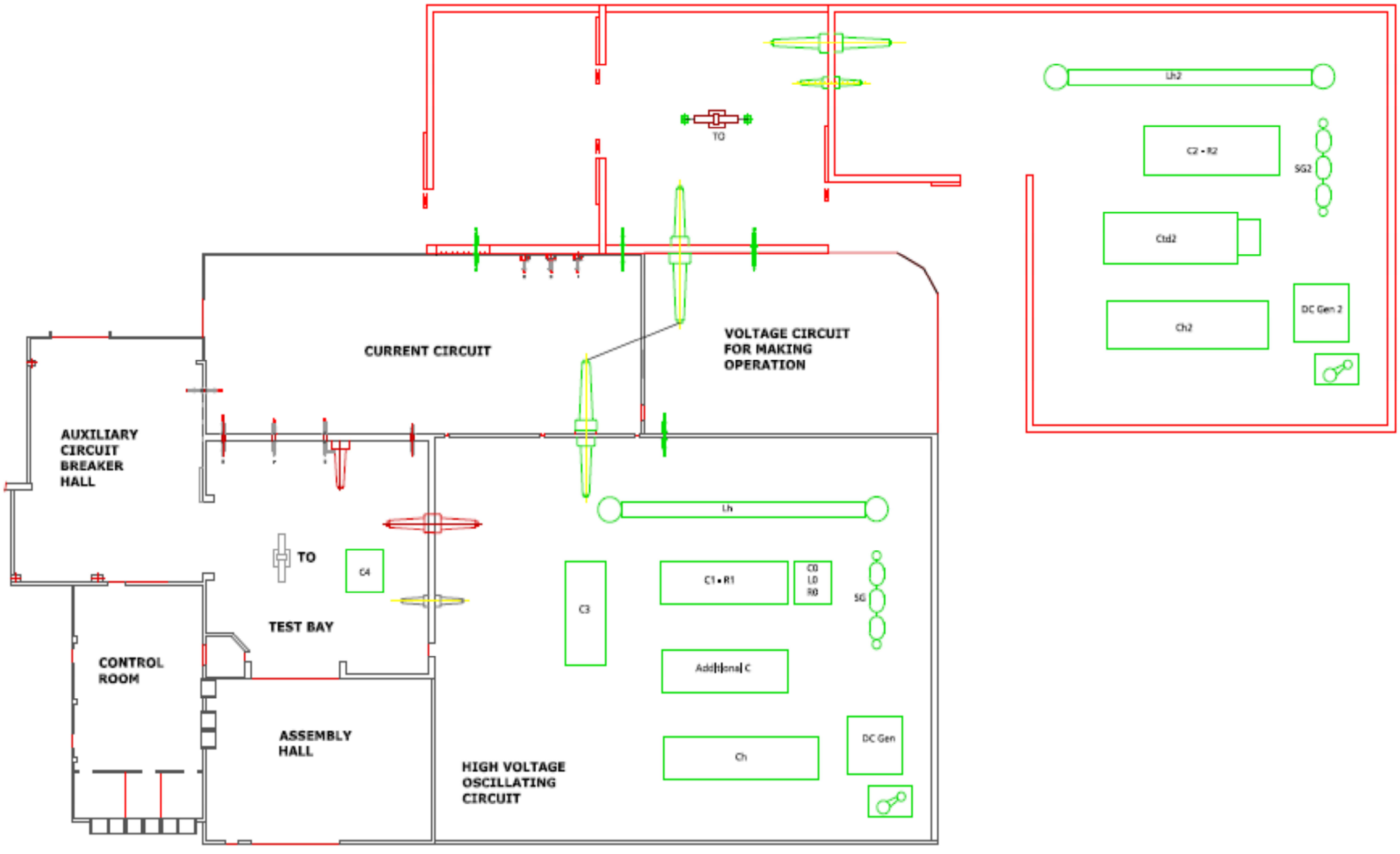
9.2.4. Capacitive current switching

See 8.2.4.

9.3. New oscillating circuit Single Line Diagram



9.4. New oscillating circuit layout



9.5. Preliminary electrical specification of main components (New oscillating circuit solution)

9.5.1. Capacitor banks

Table 9.5 - Capacitor banks values

Label	Section	Function	Capacitor bank value [μF]	Rated voltage [kV]	Ground insulation [kV]
C_{h2}	New oscillating circuit	Main capacitor bank	1 ÷ 2	500 kV D.C. (Max charging voltage)	650 kV_p
C_2	New oscillating circuit	Bank for TRV control	0.004 ÷ 1	SIWV 1050 kV_p	650 kV_p
C_{td2}	New oscillating circuit	Bank for time delay	0.01 ÷ 0.02	SIWV 1050 kV_p	650 kV_p

9.5.2. Reactor banks

Table 9.6 - Reactor banks values

Label	Section	Function	Reactor bank value [mH]	Rated voltage [kV]	Ground insulation [kV]	Energy [kJ]
L_{h2}	New oscillating circuit	Main reactor bank	50 ÷ 210	SIWV 1100 kV_p	1100 kV_p	15

9.5.3. Resistor banks

Table 9.7 - Resistor banks values

Label	Section	Function	Resistor bank value [Ω]	Rated voltage [kV]	Ground insulation [kV]	Energy [kJ]
R_2	New oscillating circuit	TRV control	20 ÷ 2500	SIWV 1100 kV_p	Not Required	2000

9.5.4. D.C. charging unit

Table 9.8 - D.C. charging unit characteristics

Label	Section	Function	Max charging voltage [kV]	Energy [kJ]	Charging time [s]
DC Gen	New oscillating circuit	Unit for main capacitor bank charging	500	250	60

9.6. Discussion of New oscillating circuit solution

9.6.1. Short-circuit simulations result

Tables at 9.2 report all test-duties executed by this circuit.

Table 9.2 and table 9.4 report test-duties executed taking into account the values required by some manufacturers (exceeding Standard requirements), i.e. with a first-pole-to-clear factor equal to 1.5; digital simulations show that TRVs are in accordance with TRV envelope (calculated with a first-pole-to-clear factor 1.5).

Table 9.1 and table 9.3 report test-duties executed taking into account the values requested by Standards, i.e. with a first-pole-to-clear factor equal to 1.3. Some digital simulations will be shown below, to check if TRV wave shapes obtained are in accordance with TRV envelope defined by Standards.

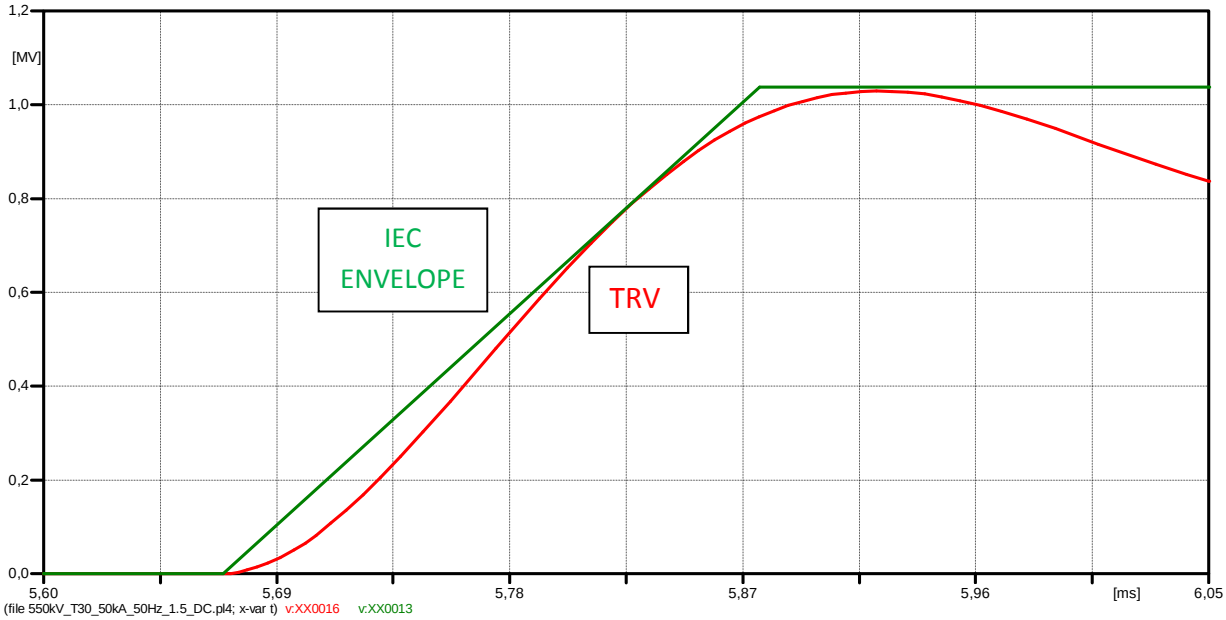
It is apparent that this configuration is able to perform tests following standards requirements as well.

Digital simulations considered with a first-pole-to-clear-factor equal to 1.3 are:

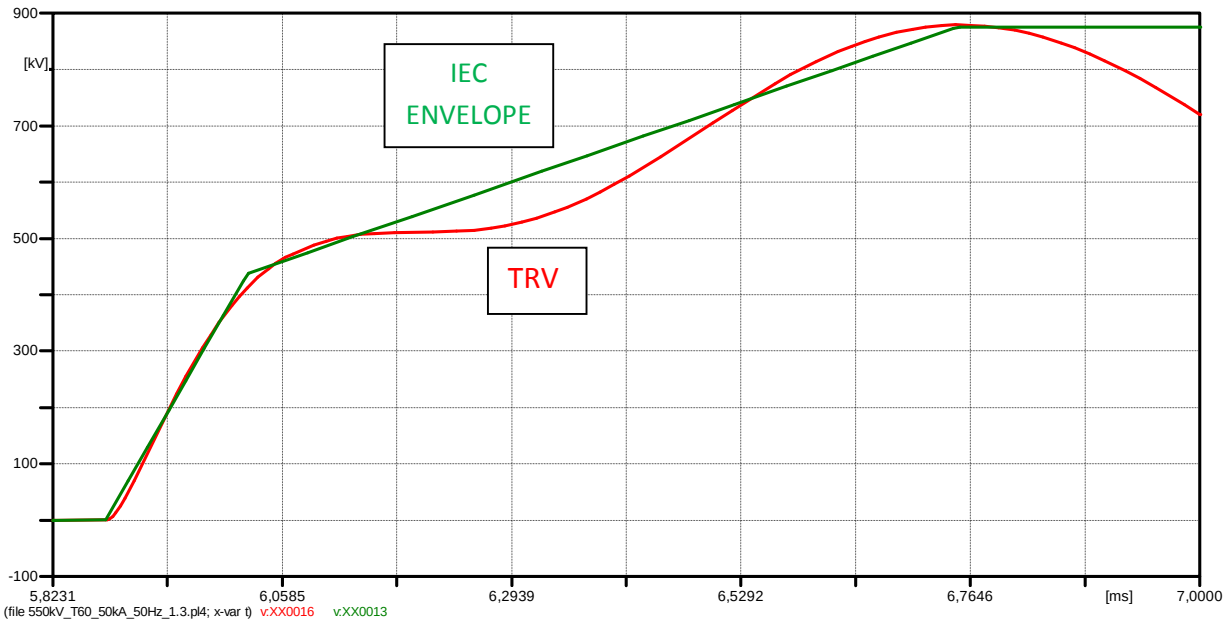
- *Test - duty T30 $I = 15\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.3 ➔ PASSED*
- *Test - duty T60 $I = 30\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.3 ➔ PASSED*
- *Test - duty T100 $I = 50\ kA$ $f = 50\ Hz$ f.p.c.f. = 1.3 ➔ PASSED*

Above mentioned digital simulations are shown in the following pages.

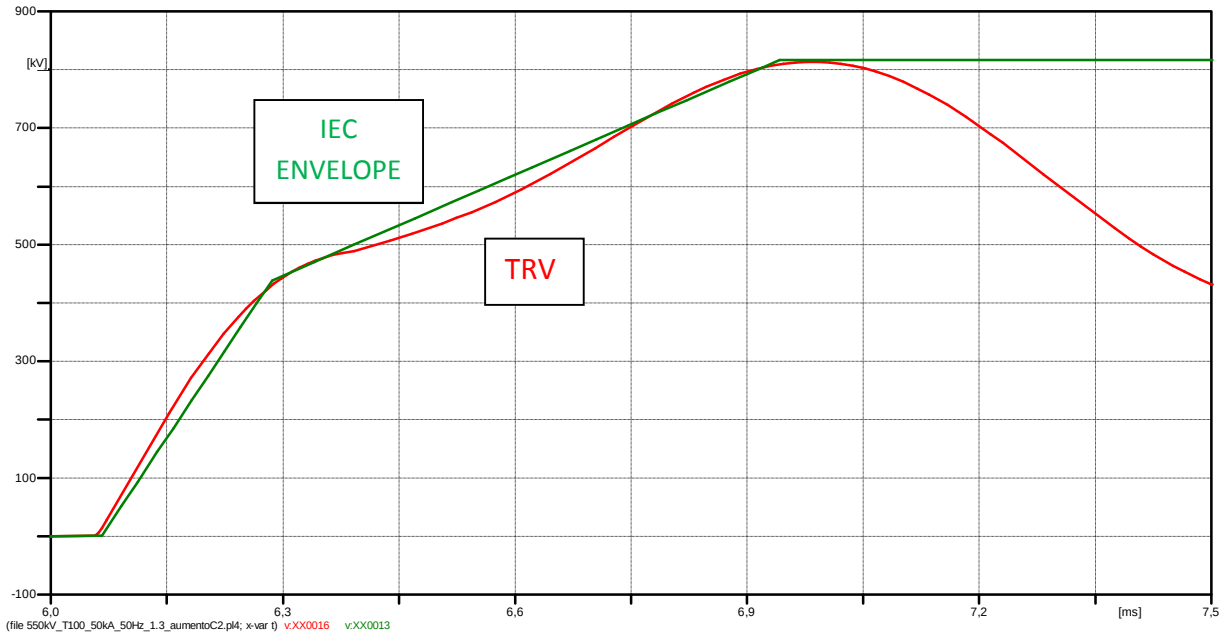
- *Test - duty T30 I = 15 kA f = 50 Hz f.p.c.f. = 1.3*



- *Test - duty T60 I = 30 kA f = 50 Hz f.p.c.f. = 1.3*



- *Test - duty T100 I = 50 kA f = 50 Hz f.p.c.f. = 1.3*



9.6.2. Out-of-phase simulations result

Results obtained from digital simulation show that the obtained TRV wave shape is in accordance to TRV envelope defined by Standards maintaining the same testing method presently used at CESI.

9.6.3. Capacitive current switching simulations result

Results obtained from digital simulation show that the obtained TRV wave shape is in accordance to TRV envelope defined by Standards maintaining the same testing method presently used at CESI.

10. CONCLUSIONS

The aim of this work is to evaluate the feasibility of an increase of performance of the present CESI High Voltage Synthetic Laboratory in order to test 550 kV circuit-breakers.
In fact, Laboratory presently is able to make test on circuit-breakers up to 420 kV.

First of all, a preliminary evaluation of limits and constrains of the present Laboratory has been made, in order to define the repowering strategy. Two options to achieve the goal have been suggested:

- First option: revamping of the present oscillating circuit.
- Second option: building a new oscillating circuit in addition to the existing one.

On the basis of the present Synthetic test circuit, a digital model has been created and validated comparing results obtained with real wave shapes measured in Laboratory during a test session: the digital model created accurately reproduces the same wave shapes recorded during a circuit-breaker breaking operation.

This tool has been updated in order to design the two suggested options. The above mentioned validation is a guarantee about the obtained results reliability.

For each option the output is:

- electrical Single Line Diagram of the oscillating circuit,
- main components electrical Specification.

Each option identifies a different way to increase the performance of the present CESI High Voltage Synthetic Laboratory.

First option consists in maintaining the same testing method and the same oscillating circuit configuration without additional buildings: only required change is values of main components. Second option needs a new building for the new oscillating circuit; moreover a new testing method is required.

First option allows to test 550 kV circuit-breakers with a first-pole-to-clear factor up to 1.3 (as per Standards requirements) but its implementation requires putting the Laboratory out-of-service during construction, which means a loss of income.
This circuit configuration (Weil) doesn't allow any future increase in voltage (e.g. from 550 to 800 kV), current (e.g. from 63 up to 80 kA) or first-pole-to-clear factor (e.g. from 1.3 to 1.5); this due to circuit intrinsic physical limit in the oscillating circuit and MV current loop.

Second option allows to test 550 kV circuit-breakers with a first-pole-to-clear factor equal to 1.5 (as per some Utilities requirements); in this case, no out-of-service of the Laboratory is needed during construction, because the present oscillating circuit remains almost unchanged.

This circuit configuration allows future increases in voltage (from 550 to 800 kV) and current (from 63 up to 80 kA).
However, this circuit configuration requires deployment of an additional short-circuit generator, for reasons explained in 9.1.3. This means that the second option is more space consuming (because new buildings are necessary) and more expensive (considering costs of new buildings and new short-circuit generator).

Table below shows a comparison between the two above mentioned options, pointing out advantages (🟢) and disadvantages (🔴) of each option.

Table 10.1 - Advantages/disadvantages of the two considered options

	REVAMPING OPTION	NEW OSCILLATING CIRCUIT
k_{pp} = 1.3	🟢	🟢
k_{pp} = 1.5	🔴	🟢
REQUIRED INVESTMENT	🟢	🔴
REQUIRED SPACE	🟢	🔴
INCOME LOSS	🔴	🟢
FUTURE EXPANSION (800 kV)	🔴	🟢
FUTURE EXPANSION (80 kA)	🔴	🟢

Our results show that, by the first option, it is possible to reach the required voltage level, but with a significant limitation to the first pole to clear factor. Such limitations can only be overcome by the second option, i.e., adding a new circuit.

This conclusion is based on analysis of all the technical factors involved. A sound basis has thus been provided for future implementation decisions, which shall keep economical and organizational issues into proper account.

11. REFERENCES

[1] International Standard IEC 62271: *High-Voltage Switchgear and Controlgear – Part 1: Common specifications,* 2010

[2] International Standard IEC 62271: *High-Voltage Switchgear and Controlgear – Part 100: High-Voltage Alternating-Current Circuit-Breakers,* 2010

[3] International Standard IEC 62271: *High-Voltage Switchgear and Controlgear – Part 101: Synthetic testing,* 2012

[4] STL guide to the interpretation of IEC 62271: *High-Voltage Switchgear and Controlgear – Part 101: Synthetic testing,* 2006

[5] CESI internal study K-219: *Circuito sintetico ad iniezione di corrente con regolazione serie (Weil): analisi dei limiti fisici del circuito, studio del metodo di calcolo dei parametri per ottenere TRV con inviluppo a norma IEC, metodo di calcolo della capacità relative al tempo di ritardo, rendimenti in potenza del circuito*, 1971

[6] R.P.P. Smeets, S. Kuivenhoven, A.B. Hofstee, *Realization of Transient Recovery Voltages for Ultra High Voltage Circuit-Breakers in Testing*, IPST2011, June 2011, Delft, The Netherlands

[7] A.L.J. Janssen, L.H. te Paske, R.P.P. Smeets, Y.J. Shin, *Limitations of High Power testing methods for EHV and UHV circuit-breakers,* CIGRE Session 2002

[8] R.P.P. Smeets, *High Power testing of circuit-breakers needs a proper choice of test-circuits,* CIGRE A3 Colloquium, September 2007, Rio de Janeiro, Brazil

[9] D. Dufournet, K. Smith, *Transient Recovery Voltages for High Voltage Circuit-Breakers,* IEEE PES Tutorial, available on: http://www.ewh.ieee.org/soc/pes/switchgear/presentations/2008cbtutorial/speaker4apaper.pdf

[10] E. Emolumento, E. Figini, S. Rovelli, *Balanced synthetic circuit for short-circuit and capacitive current switching tests of High Voltage and Extra High Voltage circuit-breakers,* SWICON-88, June 1988, Bangalore, India

[11] S. Manganaro, A. Romiti, S. Rovelli, *Recent experience with synthetic circuits for capacitive current switching tests on HV circuit-breakers,* CESI Technical Issue, 1983

[12] International Standard IEC 60071: *Insulation co-ordination – Part 1: Definitions, principles and rules,* 2008

[13] Andrew R. Hileman, *Insulation Coordination for Power Systems,* Marcel Dekker, Inc. 1999