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Techniques for High Speed and Low Power Digital-to-Analog Converters

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Abstract

The extraordinary evolution of today communication systems towards higher levels of integration is increasingly leading to the implementation of more and more complex functions in the digital domain. This process drives the need for the realization of high performance data converters in low-cost ultra-scaled nanometer CMOS processes, connecting the systems digital core to the real analog world.

In particular, academic and industrial research in the field of high-speed Nyquist-rate Digital-to-Analog Converters (DACs) is pushed forward by the growing interest in multi-carrier multi-band transmitters, for both wireless and wireline systems. Several communications standards have been recently developed requiring a DAC in the transmitter path with a sampling frequency in the GS/s range, while posing, at the same time, extremely stringent constraints on resolution, linearity and power.

Unfortunately, the feature device scaling and the supply voltage reduction, in addition to the typically noise environment of large Systems-on-Chips (SoCs), are introducing critical issues on the design of such converters. More precisely, the analysis of state-of-the-art CMOS DACs reveals two fundamental trade-offs limiting their performances: the first one between low-frequency and high-frequency linearity while the second one between linearity and power efficiency.

The essential objective of this thesis is the definition and the development of new design methodologies and techniques for the realization of high-speed high-performance DACs suitable for the integration in ultra-scaled CMOS technologies, which allow overcoming the fundamental trade-offs limiting performances.

In particular, the thesis core will be the introduction of a new digital technique for the linearization of DAC static characteristic, which is based on the extensive use of digital adaptive filtering. As static non-linearity due to analog circuits impairments is canceled out in digital domain, a design full-oriented at optimizing high-frequency performances is allowed. Furthermore, the digital style of the proposed method particularly fits into integration in nanometer

CMOS processes, further benefiting in terms of area and power consumption. To demonstrate its effectiveness, the proposed technique has been applied to the design of a 10-bit 2.5 GS/s current-steering DAC in 28 nm CMOS, to be integrated in the baseband section of a 60 GHz transmitter.

This Ph.D. dissertation is organized as follows.

Chapter 1 introduces basic concepts on high-speed digital-to-analog conversion in communications systems. State-of-the-art DACs performances are deeply examined and essential trade-offs in terms of static/dynamic linearity and power efficiency are inferred. A new Figure-of-Merit (FoM) is defined, which allows a fair comparison of DACs performances at the Nyquist frequency.

Chapter 2 is focused on DACs implemented in a current-steering configuration, which is the most commonly used in high-frequency applications. Main sources of non-linearity are investigated, making clear distinction between static and dynamic errors. The analysis of their dependencies on frequency and circuit parameters leads to a deep understanding of main DACs trade-off. Finally, a brief overview of main solutions reported in literature, aimed at improving performances in DACs with sampling frequencies in the GS/s range, is provided.

In **Chapter 3** a new accurate discrete-time DAC behavioral model suitable for the implementation in Matlab environment is introduced. Behavioral modeling is proven useful in both top-down and bottom-up approaches, reducing simulation and verification time. After the analysis of theoretical aspects, the effectiveness of the proposed model in describing both static and dynamic effects is demonstrated by comparing behavioral simulation against circuit simulation results.

Chapter 4 introduces the new digital adaptive linearization technique, which cancels out DAC static non-linearity by making use of digital adaptive filtering. Based on the sign-error version of the Least Mean Square (LMS) algorithm, the proposed system linearizes the DAC static characteristic regardless of the errors source (not only mismatch-induced errors). After having discussed in details both theoretical aspects and practical issues related to the application to current-steering DAC, the effectiveness of the proposed method in overcoming the high-frequency linearity trade-off is proved by behavioral simulations. The Spurious-Free Dynamic Range improvement goes from 26 dB at DC to 15 dB at the Nyquist frequency.

Finally, **Chapter 5** deals with the circuit design of a 10-bit 2.5 GS/s DAC in 28 nm CMOS. Circuit implementation aspects are discussed for both the current-steering DAC and all the other blocks which are required for the overall

linearization system (i.e. an accurate low-frequency DAC and a sample-and-hold circuit). Furthermore, a brief discussion of the standard cell digital section implementation is carried out. Simulations of the overall design show a DAC SFDR greater than 65 dB across the entire Nyquist bandwidth ($\mathrm{SFDR}|_{\mathrm{DC}} = 78\,\mathrm{dB}$ and $\mathrm{SFDR}|_{\mathrm{Nyq}} = 65\,\mathrm{dB}$), while consuming 36 mW analog power from a 1 V supply voltage and delivering a maximum -2 dBm power to the load.

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Chapter 1

High Speed Digital-to-Analog Conversion for Communications

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1.1 Introduction

The continuous evolution towards higher levels of integration and costs reduction in communication systems is increasingly leading to a digital implementation of functions traditionally realized in the analog domain. Contrary to their analog counterparts, digital circuits benefit from the scaling of silicon CMOS technologies in terms of power consumption, area and speed.

This process drives the need for high performance Analog-to-Digital and Digital-to-Analog Converters (ADCs and DACs), connecting the digital core to the *real* analog world, which must be implemented in low-cost nanometer CMOS processes. However, the feature device scaling and the supply voltage lowering, in addition to the noisy environment of large Systems-on-Chips

(SoCs), are introducing critical challenges on the design of high-speed low-power data converters. Today, ADCs and DACs are often the bottleneck in the signal processing chain of a transceiver, limiting the accuracy and speed of the overall communication system.

In particular, the growing interest in multi-carrier multi-band transmitters, for both wireless and wireline communications, is pushing forward research in the field of high-speed Nyquist-rate Digital-to-Analog Converters. As it will be clear in the following, the most critical challenge in such DACs is achieving a transfer function from the digital input code to the analog output waveform with the highest possible linearity over the entire Nyquist bandwidth, while having, at the same time, high sampling frequency and low power consumption.

Main focus of this thesis will be in the area of CMOS Digital-to-Analog Converters with sampling frequency in the GS/s range. Several communications standards have been recently developed requiring a DAC in the transmitter with such high sampling frequency, while posing stringent constraints on resolution, linearity and power. In the following two different DAC application examples are provided: a mm-Wave transmitter for IEEE 802.15 standard and a 10GBASE-T Ethernet transmitter.

1.1.1 IEEE 802.15 WPAN transmitter

The release of unlicensed bandwidth of about 8 GHz around 60 GHz has given rise to a variety of applications including wireless HDMI, short-range high data-rate Wireless Personal Area Networks (WPANs) and automotive radar. The IEEE 802.15 WPAN standard allocates four 2.16 GHz wide channels in the frequency range between 57.2 GHz and 65.8 GHz [1]. The resulting spectrum allocation is shown in Fig. 1.1, along with the architecture of a direct-conversion transmitter suitable for such applications.

In this Cartesian configuration the I/Q baseband digital codes are converted into analog signals by means of two DACs in parallel and then low-pass filtered. Two mixers in quadrature perform the up-conversion. The resulting modulated carriers are added together and fed to the Power Amplifier, which drives the antenna. The channel selection is achieved by controlling the frequency synthesized by the Local Oscillator (LO). A CMOS implementation of such architecture promises higher levels of integration and reduced costs with respect to traditional compound semiconductor technology, but, on the other hand, it poses constraining issues on the design of analog blocks.

Let us consider DACs specifications. First of all, the wide-bandwidth base-

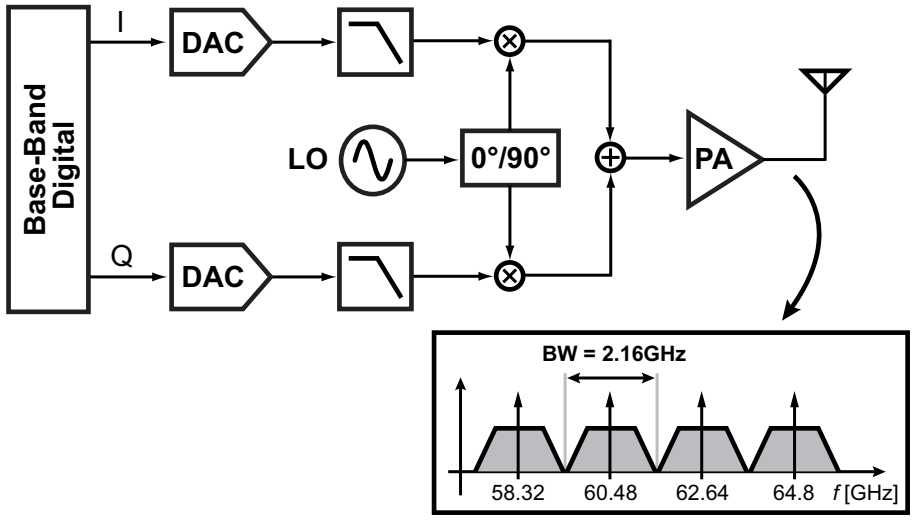

Figure 1.1 Direct-conversion transmitter for IEEE 802.15 WPAN standard.

band signal imposes a severe constraint on the sampling frequency f_S, which must be greater than 2.5 GS/s in order to meet the Nyquist sampling theorem. DAC resolution and linearity specifications are essentially determined by the required signal *quality* for the overall transceiver, in terms of noise and distortion. In RF systems they are typically quantified by two parameters [2]. The first is the Error Vector Magnitude (EVM), which is equivalent to the Signal-to-Noise and Distortion Ratio (SNDR) but defined in the complex plane, measuring the dispersion of the received symbols with respect to their ideal position. Second, the out-of-band noise, expressed by the transmitter emission mask, which defines the maximum amount of disturbances from adjacent channels that can be tolerated. The way EVM and out-of-band emissions translate into DAC resolution and linearity specifications is complicated and it depends on many factors, among which the Peak-to-Average Ratio (PAR), the number of sub-carriers of the transmitted signal and the duplexing method [3].

Anyway, once a DAC SNDR specification is given, the minimum resolution can be calculated using the well-known formula relating dynamic range to quantization noise in Nyquist-rate converters [4]:

$$n \geq \frac{\text{SNDR} - 1.76}{6.02}, \tag{1.1}$$

where n stands for the DAC number of bits (i.e. the resolution) and the SNDR is expressed in dB. Furthermore, when spectral purity is important, an additional

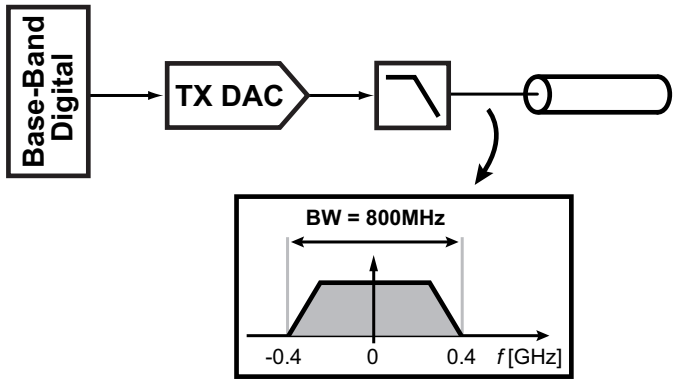

Figure 1.2 DAC-based transmitter for IEEE 802.3an Ethernet standard.

linearity specification can be given in terms of Spurious-Free Dynamic Range (SFDR), defined as the ratio between the maximum signal power and the worst distortion tone in the output spectrum:

$$\mathrm{SFDR} = 10 \cdot \log\left(\frac{P_{sig,\max}}{P_{spur,\mathrm{worst}}}\right). \tag{1.2}$$

In brief, the most stringent high-speed multi-carrier mode of the IEEE 802.15 standard requires EVM < -23 dB and out-of-band noise < -30 dBc/Hz, mandating a transmitter DAC with resolution $n \geq 8$ bits and distortion spur level below -50 dBc across the full bandwidth [1]. These linearity specifications, in conjunction with the ultra-high sampling frequency and low power requirements, imply a challenging design.

1.1.2 10GBASE-T Ethernet transmitter

The increasing demand for higher Local Area Network (LAN) bandwidth in data centers has driven the need for high speed cable networking. In this framework 10GBASE-T is the latest IEEE 802.3an Ethernet standard that set up a full-duplex bidirectional 10 Gbps data transmission over 100 m of four twisted pairs [5]. In this configuration each twisted pair transfers data at 2.5 Gbps by means of a very wideband signaling (800 MS/s).

A typical architecture for such applications is the DAC-based transmitter shown in Fig. 1.2, along with the output signal spectrum. The Digital-to-Analog Converter, cascaded with a low-pass filter, directly drives the cable. If compared to other configurations, the main advantage of this architecture is its simplicity because no other additional circuits are required [6].

	[8]	[9]	[10]	[11]	[12]	[13]
Process [nm]	65	130	65	90	180	40
Supply [V]	1.1/2.5	1.2/1.8	1.2	1.2/2.5	1.8/3.3	1.2
$\boldsymbol{I_{\mathrm{load}}}$ **[mA]**	50	10	8	16	20	16
$\boldsymbol{P_{\mathrm{TOT}}}$ **[mW]**	188	27	60	128	600	40
$\boldsymbol{P_{\mathrm{load}}}$ **[dBm]**	12	-2	-1	-7	4	-4
Resolution [bits]	12	10	9	12	14	12
$\boldsymbol{f_{\mathrm{S}}}$ **[GS/s]**	1.6/2.9	1.6	3	1.25	3/6	1.6
INL [LSB]	0.5	0.34	N/A	1.2	N/A	N/A
DNL [LSB]	0.3	0.29	N/A	0.51	N/A	N/A
$\mathbf{SFDR}\boldsymbol{\vert_{\mathrm{DC}}}$ **[dB]**	74	74	61	75	84	74
$\mathbf{SFDR}\boldsymbol{\vert_{\mathrm{Nyq}}}$ **[dB]**	52	50	53	66	57.5	70

Table 1.1 Performance comparison of most recently published CMOS DACs with sampling frequencies in the GS/s range. Power consumption data are provided at the maximum sampling frequency.

The main issue in the transmitter design is due to the full-duplex nature of the 10GBASE-T standard, which implies the need for an effective cancellation of the transmit signal and its echo components at the receiver side. This places an extremely stringent requirement on the DAC linearity [7]. As an example, in the design reported in [8] the required sampling frequency f_{S} has been set to 1.6 GS/s with a third order inter-modulation distortion (IM3) specification of at least -70 dBc up to a signal frequency of 400 MHz and -60 dBc up to 800 MHz. A few state-of-the-art published designs can meet these linearity requirements.

1.2 Performance survey of state-of-the-art DACs

The previous section pointed out the growing interest in applications requiring CMOS DACs with sampling frequencies well-beyond 1 GS/s, medium-to-high resolutions and high linearity up to the Nyquist frequency ($f_{\mathrm{S}}/2$). First of all, it can be useful to have a look at the state-of-the-art in order to identify main trends and limitations in DACs performances. To this purpose Tab. 1.1 provides a comparison of data and performances of the most recently published

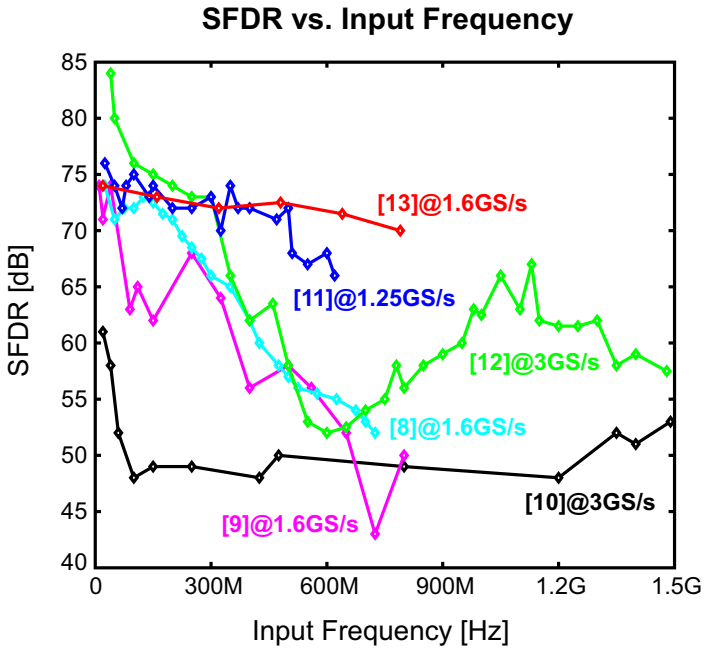

Figure 1.3 SFDR vs. input frequency for state-of-the-art DACs of Tab. 1.1.

CMOS Digital-to-Analog Converters with sampling frequencies in the GS/s range. They are all implemented in a current-steering configuration, which is the most commonly used in high frequency applications because of its inherently high speed circuitry.

Although technology, resolution, sampling frequency, power and linearity vary significantly among these designs, a closer analysis of data reveals two important design trade-offs limiting state-of-the-art DACs performances. The first one is between *static* (low-frequency) and *dynamic* (high-frequency) linearity, while the second one between linearity and power efficiency.

1.2.1 Static vs. dynamic linearity trade-off

Looking at the linearity data, two interesting considerations can be made. First, there is no apparently relationship between static linearity, expressed in terms of Integral Non-Linearity (INL) and Differential Non-Linearity (DNL), and dynamic linearity, measured by the SFDR at high frequency. If we consider designs for which data are available, even though they present comparable INL/DNL values, $\text{SFDR}|_{\text{Nyq}}$ substantially varies ranging from 50 dB in [9] to 66 dB in [11]. Obviously, SFDR is a preferable measure of DAC non-linearity,

since INL and DNL do not account for dynamic effects degrading high frequency performances.

Second and more important, all the designs exhibit a drastic reduction of the Spurious-Free Dynamic Range as the input signal frequency moves from DC ($\mathrm{SFDR}|_{\mathrm{DC}}$) to Nyquist ($\mathrm{SFDR}|_{\mathrm{Nyq}}$). This is highlighted in Fig. 1.3, where the SFDR of the DACs of Tab. 1.1 are plotted as a function of the input frequency. If compared to the others, the designs in [11] and [13] show a less evident SFDR reduction (9 dB and 4 dB, respectively) but, as it will be discussed in the next section, they suffer from a much worse power efficiency, due to the implementation of the Return-to-Zero (RZ) technique.

These considerations reveal a trade-off between static and dynamic linearity limiting performances of state-of-the-art DACs. In fact, the analysis of non-linearity errors in current-steering circuit (Chapter 2) will show that optimizing static accuracy will negatively impact on linearity at high frequency and vice-versa.

1.2.2 Power vs. linearity trade-off

Linearity is not the only parameter that matters in evaluating DACs performances. We have seen that the increasing demand for Digital-to-Analog Converters to be implemented in large CMOS Systems-on-Chips requires low power consumption and high efficiency. Tab. 1.1 includes data about output current (I_{load}), power delivered to the load (P_{load}) and total power consumption (P_{TOT}). However, absolute power numbers do not provide a meaningful comparison. For example the total power varies significantly, from 27 mW in [9] to 600 mW in [13], including both the available power for the load and the power dissipated in the DAC itself.

To make a comparison a useful figure is the DAC Normalized Power Efficiency (NPE) introduced in [8]. It is defined as the ratio between the power delivered to the load and the total power, normalized to the ideal efficiency of a class-A stage:

$$\mathrm{NPE} = \frac{P_{\mathrm{load}}}{0.25 \cdot P_{\mathrm{TOT}}} \,. \tag{1.3}$$

NPE of designs of Tab. 1.1 is displayed in Fig. 1.4, as a function of the SFDR at the Nyquist frequency. Unfortunately, even in this case there is a considerable dispersion of the values: the minimum efficiency is 1.25% in [11] while the maximum of 78.3% is achieved by [8]. Furthermore we cannot infer a straightforward

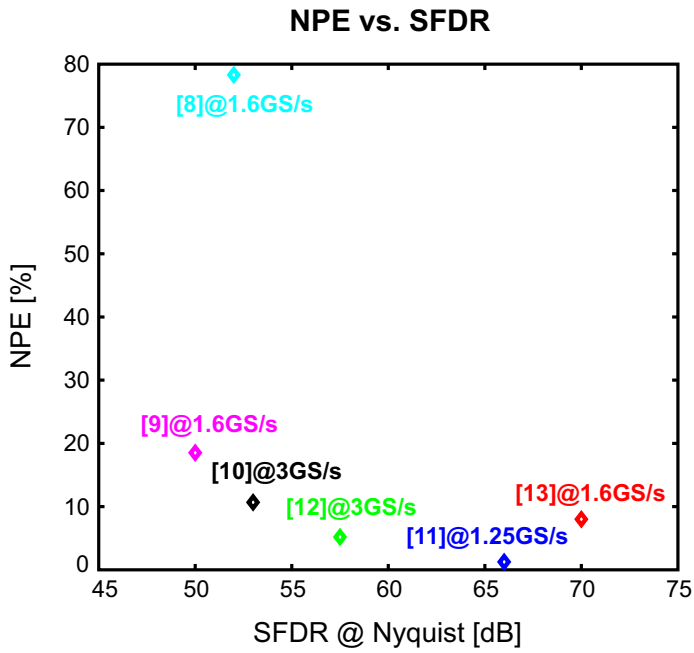

Figure 1.4 NPE vs. SFDR at Nyquist for state-of-the-art DACs of Tab. 1.1.

relationship between NPE and linearity because $\text{SFDR}|_{\text{Nyq}}$ clearly depends on the sampling frequency f_{S}, which is not accounted for in the plot of Fig. 1.4.

Therefore, in order to make a meaningful comparison between DACs a new Figure-of-Merit (FoM) must be defined including information about power efficiency, dynamic linearity and absolute value of sampling frequency. On the basis of these assumptions it can be defined as:

$$\text{FoM} = 2^{\frac{\text{SFDR}|_{\text{Nyq}} - 1.76}{6.02}} \cdot f_{\text{S}} \cdot \text{NPE}\,, \tag{1.4}$$

which is measured in Hz.[1] The first term of Eq. (1.4) is the linear dynamic range limitation imposed by the SFDR at Nyquist, as obtained by applying Eq. (1.1). In this way, assuming the SFDR inversely proportional to frequency, the DAC FoM is by definition independent on the sampling frequency f_{S}. A much simpler expression can be obtained by calculating the FoM in dBHz:

$$\text{FoM}|_{\text{dBHz}} = \text{SFDR}|_{\text{Nyq}} + [f_{\text{S}} \cdot \text{NPE}]|_{\text{dBHz}}\,, \tag{1.5}$$

[1] The explanation of this FoM definition, along with its validity hypothesis and limitations, will be provided in Chapter 2, after the analysis of non-linearity errors and power consumption in current-steering DACs.

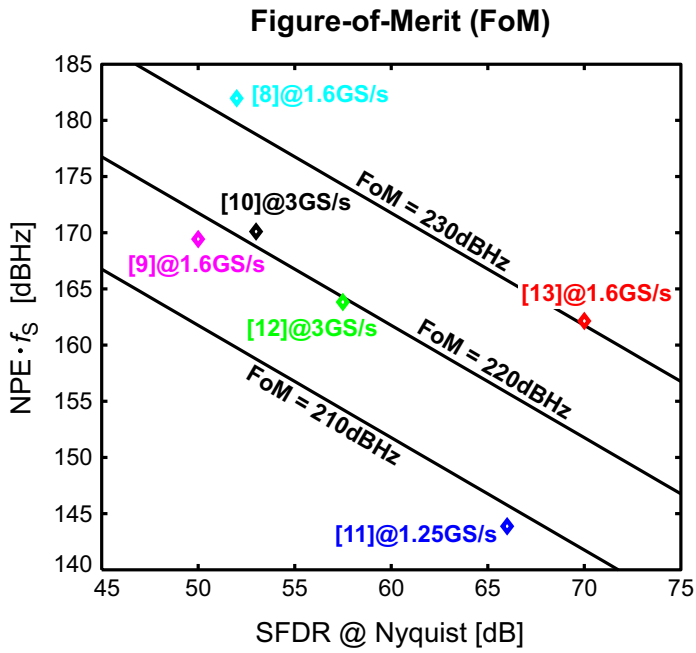

Figure 1.5 FoM of state-of-the-art DACs of Tab. 1.1.

which clearly shows that, for a given constant FoM, the $f_S \cdot \text{NPE}$ product (in dBHz) linearly depends on $\text{SFDR}|_{\text{Nyq}}$. In other words, as the SFDR increases the $f_S \cdot \text{NPE}$ term decreases and vice-versa.

On the basis of these considerations Fig. 1.5 shows $[f_S \cdot \text{NPE}]|_{\text{dBHz}}$ against $\text{SFDR}|_{\text{Nyq}}$, along with the lines corresponding to some constant FoM values. The figure captures the main trends in state-of-the-art DACs. In general, given a certain sampling frequency the high frequency linearity performances improve only at the expanse of a lower power efficiency. This is the case of the two best design reported in literature ([8] and [13]): even though they present extremely different $\text{SFDR}|_{\text{Nyq}}$ and NPE values, they approximately achieve the same FoM of about 231 dBHz revealing a substantial trade-off between dynamic linearity and power efficiency.

1.3 Thesis aim

Aim of this thesis is the definition of new design methodologies and techniques for the realization of high efficiency high performance Digital-to-Analog Converters suitable for the integration in ultra-scaled CMOS technologies. The essential objective is the development of new digital solutions allowing the

advancement of state-of-the-art, by overcoming the fundamental trade-offs limiting DACs performances.

In particular, the thesis core will be the introduction of a novel technique for the linearization of the DAC static characteristic. Based on the extensive use of digital adaptive filtering, this method cancels out static non-linearity errors due to analog circuits impairments, allowing a design full-oriented at optimizing dynamic performances. In this way the trade-off between low-frequency and high frequency linearity can be overcome without sacrificing power efficiency.

Moreover, the fully digital implementation of the proposed linearization technique especially fits into integration in nanometer CMOS processes, further benefiting from technology scaling in terms of area and power consumption. Transferring power from analog circuits to digital will be proven useful in making compromise between efficiency and linearity less constraining.

Final target is the design and implementation of a 10-bit 2.5 GS/s DAC in 28 nm CMOS technology for application in the baseband section of a 60 GHz transmitter.

Chapter 2

Non-Linearity Errors in Current-Steering DACs

Contents

2.1 Introduction

We have seen in the previous chapter that current-steering Digital-to-Analog Converters are the most popular in high speed applications, where sampling frequencies in the order of GS/s are required. Fundamentally, the current-steering circuit fits into high speed operation because no high impedance nodes are present. Furthermore, as a second advantage, it does not require any power

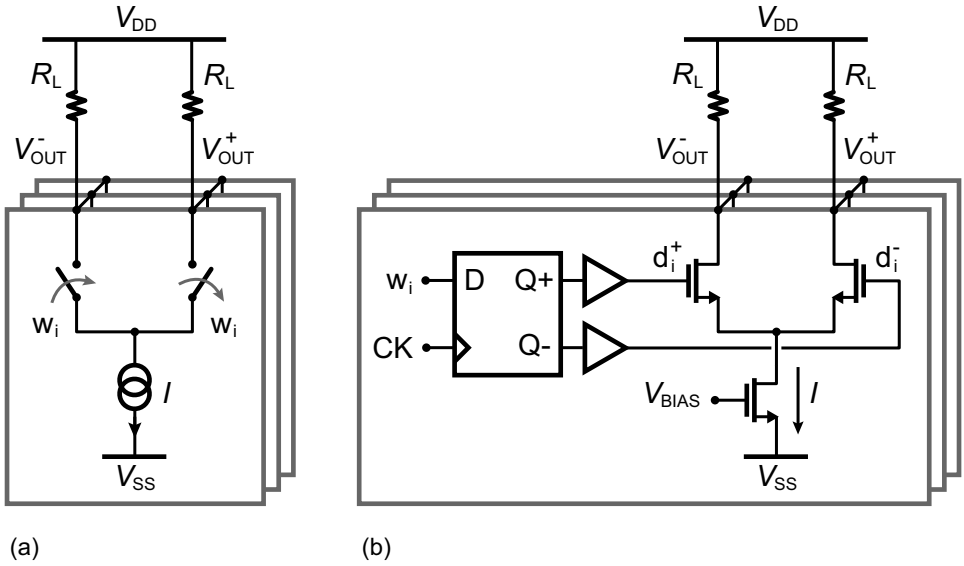

Figure 2.1 Current-steering Digital-to-Analog Converter: (a) simplified model and (b) circuit implementation.

hungry block, such as operational amplifiers or voltage buffers [4].

The conceptual model of an n-bit current-steering DAC converting an n-bit digital input $(b_{n-1}b_{n-2}\dots b_0)$ into an analog output signal (the differential output voltage $V_{\mathrm{OUT}}|_{\mathrm{diff}} = V^{+}_{\mathrm{OUT}} - V^{-}_{\mathrm{OUT}}$) is shown in Fig. 2.1(a). It consists of $N = 2^n - 1$ ideally identical current cells, connected together to a low impedance load (typically $50\,\Omega$ differential). Each current cell is realized by means of a current source connected to a differential switch that directs the unit current I, i.e. the Least-Significant Bit (LSB) current, either to positive or negative output according to the control bit w_i. The N control signals w_i, with $i = 0, \dots, N-1$, are defined such that:

$$D_{\mathrm{IN}} = \sum_{i=0}^{n-1} b_i \cdot 2^i = \sum_{i=0}^{N-1} w_i \,, \tag{2.1}$$

where D_{IN} $(0 \le D_{\mathrm{IN}} \le N-1)$ is the equivalent integer value of the digital input code. The way the n input bits b_i map to the N control bits w_i defines the DAC coding configuration. As the segmentation level varies, a DAC can be classified as binary-coded (no-segmented), thermometer-coded (fully-segmented), or partially-segmented. As it will be clear in the following, the choice of the segmentation level has a strong impact on DAC performances

[14], [15].

A possible CMOS implementation of a current-steering DAC is shown in Fig. 2.1(b), where the current source and the differential switch are realized by an nMOS transistor biased at a constant gate voltage (V_{BIAS}) and by an nMOS differential pair, respectively. The operating point of all devices, when active, must be guaranteed ins saturation region. The gates of switch transistors are controlled by a latch driver which synchronizes the complementary control signals d_i^+ and d_i^- to the clock (CK). The overall differential output voltage is given by:

$$V_{\mathrm{OUT}}|_{\mathrm{diff}} = V_{\mathrm{OUT}}^+ - V_{\mathrm{OUT}}^- = IR_{\mathrm{L}} \cdot \sum_{i=0}^{N-1} (d_i^+ - d_i^-)\,. \tag{2.2}$$

By defining the differential control signal $d_i|_{\mathrm{diff}} = d_i^+ - d_i^-$ as:

$$d_i|_{\mathrm{diff}} = \begin{cases} +1 & \text{if } w_i = 1 \\ -1 & \text{if } w_i = 0 \end{cases} \tag{2.3}$$

it follows that, in the ideal case, a linear relationship exists between the equivalent differential integer input value $D_{\mathrm{IN}}|_{\mathrm{diff}}$ ($-(N-1) \leq D_{\mathrm{IN}}|_{\mathrm{diff}} \leq N-1$) and the output voltage:

$$V_{\mathrm{OUT}}|_{\mathrm{diff}} = IR_{\mathrm{L}} \cdot \sum_{i=0}^{N-1} d_i|_{\mathrm{diff}} = IR_{\mathrm{L}} \cdot D_{\mathrm{IN}}|_{\mathrm{diff}}\,. \tag{2.4}$$

More precisely, in the following discussion it will be useful to express $V_{\mathrm{OUT}}|_{\mathrm{diff}}$ as a function of the differential load resistance $R_{\mathrm{L}}|_{\mathrm{diff}} = 2R_{\mathrm{L}}$. The output voltage becomes:

$$V_{\mathrm{OUT}}|_{\mathrm{diff}} = \frac{1}{2} \cdot IR_{\mathrm{L}}|_{\mathrm{diff}} \cdot D_{\mathrm{IN}}|_{\mathrm{diff}}\,. \tag{2.5}$$

It is essential to highlight that Eq. (2.5) represents the DAC static characteristic only, relating the stationary value of the output voltage (i.e. the DC value) to the stationary value of the digital input code. In the ideal case this relationship is perfectly linear. In practice, circuits errors and non-idealities (such as, for instance, mismatches among current sources) will inevitably affect the static transfer function, introducing non-linear distortion.

However, the static characteristic does not provide a complete description of DAC operation. In fact, the overall DAC function is to convert a digital

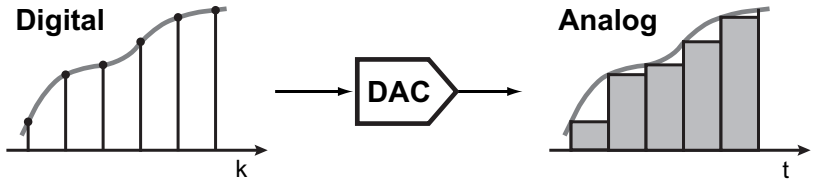

Figure 2.2 DAC operation: conversion from a digital discrete-time signal to an analog continuous-time signal.

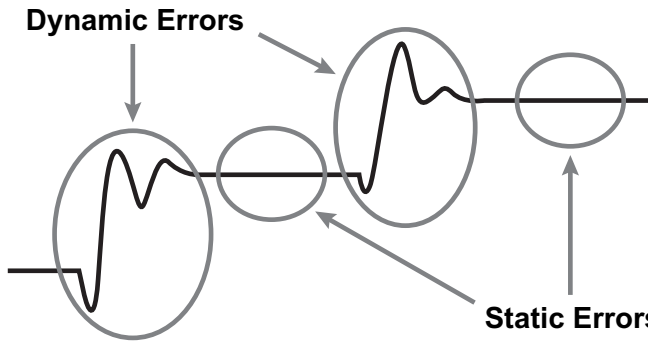

Figure 2.3 Static and dynamic errors in DAC output waveform.

discrete-time input signal into an analog *continuous-time* output waveform [16]. In other words the DAC converts a samples sequence at the input into a series of voltage (or current) pulses at the output. An example is depicted in Fig. 2.2 where the ideal Zero-Order Hold case is shown. Here the output pulse is a rectangular shape with duration equal to the sampling period $T_S = 1/f_S$ and amplitude modulated by the input sample. It follows that, in practice, most of the problems affecting DAC linearity are not related to the stationary output values, but to the dynamic effects occurring at pulse to pulse transitions.

This becomes evident from Fig. 2.3, where static and dynamic errors are highlighted for an hypothetical output waveform. While dynamic non-linearity errors are related to signal transients, because they can be different for different input transitions, static non-linearity errors become relevant at the end of each sampling period, when the signal settles to its DC value. In particular, we will demonstrate that dynamic non-linearity becomes more and more dominant with respect to the static one as the signal frequency increases.

In the past a huge amount of literature has been published on DAC designs focusing on analysis and optimization of static linearity [14]–[15], [17]–[22], while only in recent years a growing interest in the minimization of dynamic non-linearity errors for high performance high speed DACs has appeared [23]–

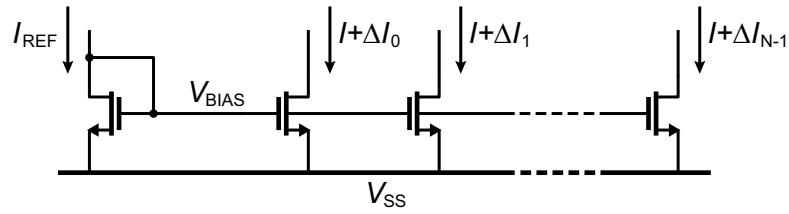

Figure 2.4 nMOS current sources with mismatches.

[26], [8]–[13]. In this chapter we will analyze main sources of static and dynamic non-linearity errors in current-steering DACs, revealing their dependencies on frequency and circuit parameters. For the sake of simplicity, all considerations will be referred to the example case of non-cascoded current cells. Anyway, all the results we will provide, can be easily extended to cascoded configurations. Finally a Figure-of-Merit will be introduced for the comparison of DAC high frequency performances.

2.2 Static non-linearity errors

This section deals with non-linearity errors affecting the stationary value of the output voltage (or current). Since they are frequency-independent, they will dominate DAC linearity at low frequencies.

2.2.1 Random Mismatches

An upper limit to the DAC achievable linearity is set by current sources random mismatches, due to the unavoidable statistical dispersion of process parameters impacting on transistors sizes, threshold voltage, mobility, etc. As shown in Fig. 2.4, each of the N generated currents of an n-bit DAC can be viewed as the sum of the ideal LSB current (I) and a current error (ΔI_i) that can be modeled as a gaussian random variable with zero mean and process-dependent standard deviation:

$$I_i = I + \Delta I_i \quad \text{for } i = 0, \ldots, N-1\,. \tag{2.6}$$

According to the Pelgrom model, the variance of the relative current variation is given by [27]:

$$\sigma^2\left(\frac{\Delta I}{I}\right) = \frac{1}{WL} \cdot \left[A_\beta + \frac{4}{(V_{\mathrm{GS}} - V_{\mathrm{T}})^2} \cdot A_{V_{\mathrm{T}}}\right], \tag{2.7}$$

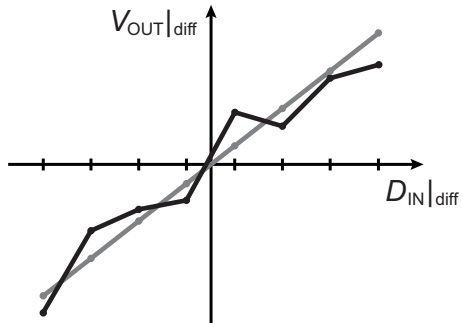

Figure 2.5 Mismatch impact on static characteristic.

where WL represents the transistor area while A_β and A_{V_T} are technology-dependent parameters describing dispersion of the current factor β and the threshold voltage V_T, respectively. Eq. (2.7) indicates that, even in the case of a proper choice of the overdrive voltage $(V_{GS} - V_T)$, the current accuracy improves only at the expanse of a larger transistor area.

The impact of mismatches on DAC linearity is depicted in Fig. 2.5, where an example of real static characteristic is compared to the ideal one. Using the real current values in place of I, Eq. (2.5) can be rewritten as:

$$V_{OUT}|_{diff} = \frac{1}{2} \cdot IR_L|_{diff} \cdot D_{IN}|_{diff} + \frac{1}{2} R_L|_{diff} \cdot \sum_{i=0}^{N-1} d_i|_{diff} \cdot \Delta I_i \,. \tag{2.8}$$

The second term of Eq. (2.8) represents the deviation of the real characteristic from the ideal one and it is usually referred to as Integral Non-Linearity (INL). It can be easily shown, after some calculations, that the standard deviation of INL normalized to the voltage LSB ($IR_L|_{diff}$) is given by:

$$\sigma_{INL} = \sqrt{2^n - 1} \cdot \sigma\left(\frac{\Delta I}{I}\right). \tag{2.9}$$

This means that the deviation, and hence the maximum value, of the INL is inversely proportional to the square root of the area of current source transistors. In particular, in order to meet the same INL requirement with a higher resolution (n), a larger area must be used for current sources. Unfortunately, as it will be demonstrated in section 2.3, the increased parasitic capacitance due to larger transistors will have a worsening impact on high frequency linearity.

A second important static parameter is the Differential Non-Linearity (DNL), which is defined as the deviation from an ideal one-LSB step between two sub-

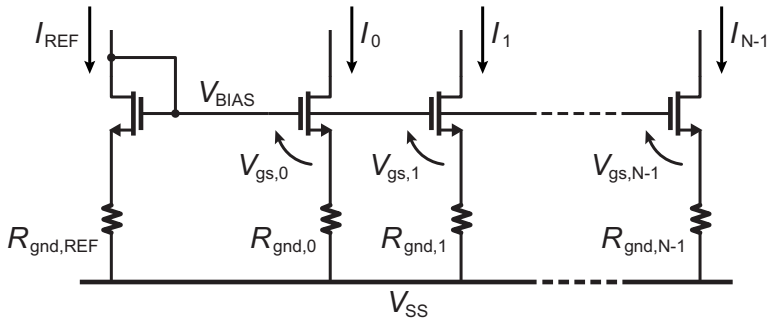

Figure 2.6 Effect of IR drop on supply lines.

sequent output levels. The DNL normalized to the LSB is given by:

$$\mathrm{DNL} = \frac{\frac{1}{2}R_{\mathrm{L}}|_{\mathrm{diff}} \cdot 2\Delta I_i}{IR_{\mathrm{L}}|_{\mathrm{diff}}} = \frac{\Delta I_i}{I} \tag{2.10}$$

and hence its standard deviation coincides to the unit current one:

$$\sigma_{\mathrm{DNL}} = \sigma\left(\frac{\Delta I}{I}\right). \tag{2.11}$$

The above derivation has implicitly assumed a thermometer-coded DAC. It can be shown that using different segmentation levels would produce more stringent requirements on current accuracy for a given DNL specification [15]. For example, in the binary-coded case σ_{DNL} equals the σ_{INL} expressed by Eq. (2.9).

2.2.2 IR drop and gradients

Current accuracy is not only affected by random mismatches, but even by systematic errors originating from process gradients (impacting on parameters like, for instance, the oxide thickness), temperature gradients and supply voltage drops induced by routing network resistances. As an example, this last issue is depicted in Fig. 2.6. Since the ground lines to the DAC cells carry current, any asymmetry in the lines parasitic resistances will result in different IR voltage drops, causing the individual gate-source voltages of different sources to be unequal. As a consequence, deviations of the generated currents from ideal values will degrade INL and DNL, similarly to what previously discussed for random mismatches. To face the problem, wide power supply lines must be used to lower the resistance. Furthermore, a binary tree configuration of the

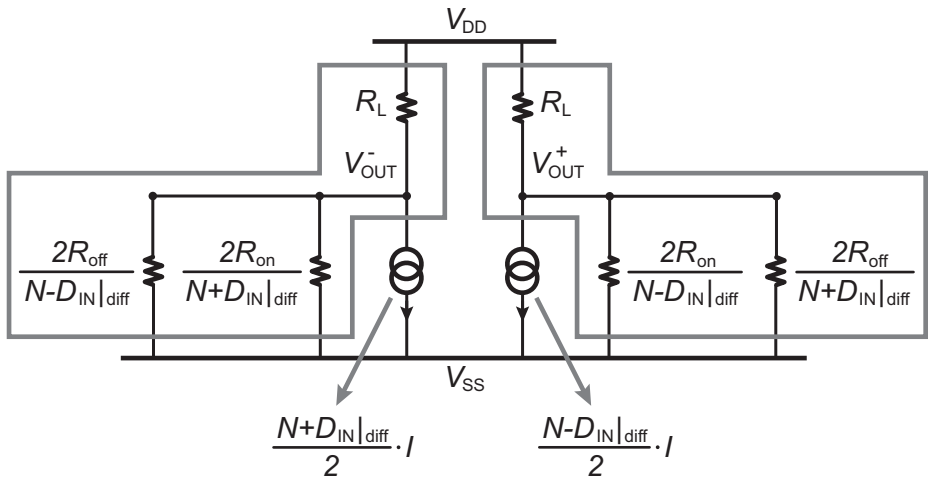

Figure 2.7 Equivalent circuit for calculation of the output resistance as a function of the input code.

supply grid is essential, in order to guarantee the required symmetry.

For what concerns other gradients errors, a straightforward countermeasure is to limit the overall DAC area, so as to reduce the distance between current sources. Unfortunately, this is in contrast with the need to increase transistor area to lower random mismatches. For this reason, techniques based on appropriate switching schemes [18], calibration [22], [28] and randomization [26] have been introduced in the past.

2.2.3 Output resistance

Even in a DAC made up of perfectly matched current sources, static non-linearity can arise if the output resistance of current cells is finite, instead of infinite as assumed in the ideal case. In fact, according to the digital input code, more or less current sources are connected to the positive (V_{OUT}^{+}) and to the negative (V_{OUT}^{-}) output nodes. Therefore, more or less finite current cell output resistances are connected in parallel with the load resistor R_{L}. This means that the DAC total differential output resistance depends on the digital input code. Furthermore, being the output voltage obtained by multiplication of code-dependent current and output resistance, this produces distortion in the output waveform [8], [29].

As a first step, to get a quantitative evaluation of the output resistance non-linearity, let us represent every current cell by its Norton equivalent circuit. For the on-side (i.e. the side through which the current flows, being the

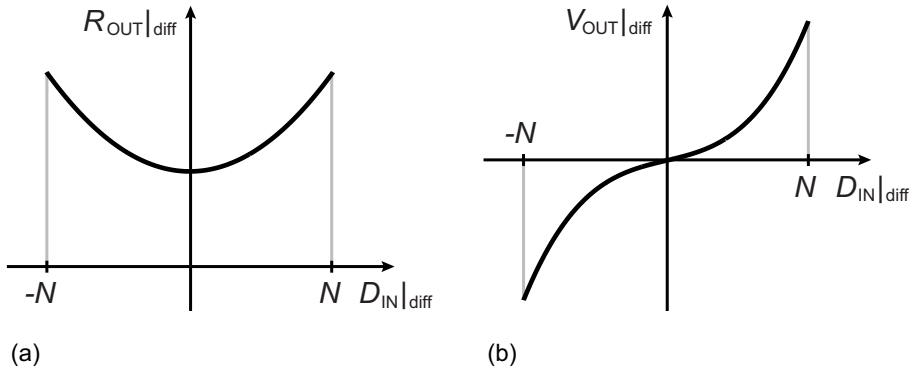

Figure 2.8 Output resistance non-linearity: (a) $R_{\mathrm{OUT}}|_{\mathrm{diff}}$ vs. input code and (b) $V_{\mathrm{OUT}}|_{\mathrm{diff}}$ vs. input code.

switch transistor on) the equivalent circuit is given by an ideal current source I in parallel with a resistor R_{on}, while for the off-side it consists only of a resistor R_{off}. Even though R_{off} could be reasonably neglected, this more general representation will be proven useful in the following analysis of high-frequency linearity. The resulting overall DAC circuit is drawn in Fig. 2.7, clearly showing code-dependency of the resistances connected to positive and negative output nodes.[1]

In order to calculate the differential output resistance $R_{\mathrm{OUT}}|_{\mathrm{diff}}$, it is initially convenient to use conductances instead of resistances:

$$\begin{aligned} G^{+}_{\mathrm{OUT}} &= G_{\mathrm{L}} + \frac{N - D_{\mathrm{IN}}|_{\mathrm{diff}}}{2} G_{\mathrm{on}} + \frac{N + D_{\mathrm{IN}}|_{\mathrm{diff}}}{2} G_{\mathrm{off}} \\ G^{-}_{\mathrm{OUT}} &= G_{\mathrm{L}} + \frac{N + D_{\mathrm{IN}}|_{\mathrm{diff}}}{2} G_{\mathrm{on}} + \frac{N - D_{\mathrm{IN}}|_{\mathrm{diff}}}{2} G_{\mathrm{off}} \end{aligned} \tag{2.12}$$

where G^{+}_{OUT} and G^{-}_{OUT} stand for the overall conductance connected to V^{+}_{OUT} and V^{-}_{OUT}, respectively. By defining $G_{\mathrm{sum}} = G_{\mathrm{on}} + G_{\mathrm{off}}$ and $G_{\mathrm{diff}} = G_{\mathrm{on}} - G_{\mathrm{off}}$, we obtain:

$$R_{\mathrm{OUT}}|_{\mathrm{diff}} = \frac{1}{G^{+}_{\mathrm{OUT}}} + \frac{1}{G^{-}_{\mathrm{OUT}}} = \frac{8G_{\mathrm{L}} + 4NG_{\mathrm{sum}}}{(2G_{\mathrm{L}} + NG_{\mathrm{sum}})^2 - D^2_{\mathrm{IN}}|_{\mathrm{diff}} \cdot G^2_{\mathrm{diff}}} \,. \tag{2.13}$$

Eq. (2.13) can be simplified under the hypothesis that $G_{\mathrm{sum}} \ll 2G_{\mathrm{L}}/N$, i.e.

[1] Hereinafter, for the sake of simplicity, we will approximate $N - 1$ with N, considering $-N \leq D_{\mathrm{IN}}|_{\mathrm{diff}} \leq N$, instead of $-(N-1) \leq D_{\mathrm{IN}}|_{\mathrm{diff}} \leq (N-1)$.

$R_{on} \gg NR_L/2$ (neglecting R_{off}), which is easily verified. In this case it results:

$$R_{OUT}|_{diff} \simeq R_L|_{diff} \cdot \left[1 + \frac{R_L^2 D_{IN}^2|_{diff}}{4\Delta R^2}\right], \tag{2.14}$$

in which ΔR is defined as the inverse of the difference between the on-side and the off-side conductances:

$$\Delta R = \frac{1}{G_{diff}} = \frac{1}{G_{on} - G_{off}} = \frac{1}{\frac{1}{R_{on}} - \frac{1}{R_{off}}} \tag{2.15}$$

and it will be referred to as *switching resistance* [8]. Let us note that ΔR tends to be equal to R_{on}, when R_{off} is sufficiently large to be neglected. Eq. (2.14) indicates that the DAC output resistance depends quadratically on the digital input code, as displayed in Fig. 2.8(a). In particular, the non-linearity term of $R_{OUT}|_{diff}$ is inversely proportional to the square of the switching resistance ΔR: as R_{on} tends to be large, in other words as R_{on} tends to be similar to R_{off}, the output resistance tends to its ideal constant value $R_L|_{diff} = 2R_L$, as expected.

Substituting the expression of $R_{OUT}|_{diff}$ in place of $R_L|_{diff}$ in Eq. (2.5), we get the overall output voltage:

$$V_{OUT}|_{diff} = \frac{1}{2} \cdot NIR_L|_{diff} \cdot \left[x + \frac{N^2 R_L^2}{4\Delta R^2} \cdot x^3\right], \tag{2.16}$$

where $x = D_{IN}|_{diff}/N$ is the normalized digital input ($-1 \leq x \leq 1$). Eq. (2.16) reveals that the output impedance non-linearity produces a third-order harmonic distortion in the output differential voltage (see Fig. 2.8(b)) given by:

$$HD_3 = \left[\frac{NR_L}{4\Delta R}\right]^2. \tag{2.17}$$

It follows that, for given resolution (N) and load resistance (R_L), the only way to reduce distortion is increasing the switching resistance. For instance, in order to pull down HD_3 below $-80\,dB$ for a 10-bit DAC with $R_L = 25\,\Omega$ ($R_L|_{diff} = 50\,\Omega$), $R_{on} > 640\,k\Omega$ is required. This can be quite easily achieved, even for higher resolutions, by proper sizing of the transistors length or by cascoding [8]. But, as it will be clear in the following, meeting the output impedance specification at higher frequencies will become more difficult.

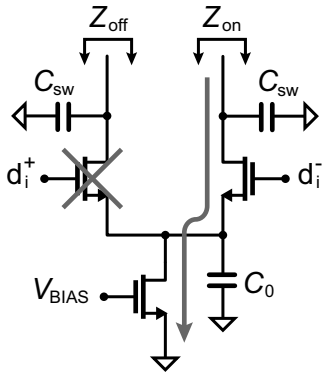

Figure 2.9 Output impedance of the unit cell.

2.3 Dynamic non-linearity errors

This section deals with non-linearity errors arising from signal transients. Due to their nature, they will dominate DAC linearity as the signal frequency increases.

2.3.1 Output impedance

The non-linearity mechanism originating from the current cell finite output resistance, that we introduced in section 2.2.3 for the stationary case, still holds even for higher signal frequencies. More precisely, output impedance distortion actually worsen as the signal frequency increases. In fact, as frequency increases, the capacitive part of cell impedance starts to dominate over the resistive one, further reducing the overall DAC differential output impedance. On the basis of these considerations, the third-order distortion in the output signal can be still described by Eq. (2.17), but with the module of the current cell *switching impedance* ΔZ instead of the switching resistance [8]:

$$\mathrm{HD}_3 = \left[\frac{NR_\mathrm{L}}{4|\Delta Z|}\right]^2 . \tag{2.18}$$

As a first step, to get the switching impedance ΔZ, the on-side and the off-side output impedances of unit current cell must be calculated. To this purpose let us refer to Fig. 2.9, in which circuit parasitic capacitances are included. C_sw stands for the gate drain overlap capacitance of switch transistors while C_0 accounts for both the drain capacitance of current source and the gate-

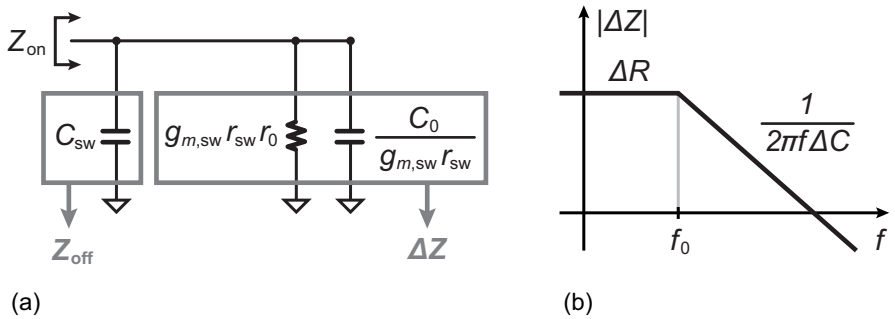

Figure 2.10 (a) Equivalent circuit for calculation of the switching impedance and (b) $|\Delta Z|$ vs. frequency.

source capacitances of differential pair. Neglecting the drain resistance of the off-switch, the output impedance of the off-side is simply given by:

$$Z_{\text{off}} = \frac{1}{sC_{\text{sw}}} \tag{2.19}$$

while, on the other side, Z_{on} can be roughly viewed as the parallel of C_{sw} and the current source impedance amplified by the switch transistor voltage gain:

$$Z_{\text{on}} = \frac{1}{sC_{\text{sw}}} \parallel \left[g_{m,\text{sw}} r_{\text{sw}} \cdot \left(r_0 \parallel \frac{1}{sC_0} \right) \right], \tag{2.20}$$

in which $g_{m,\text{sw}}$ and r_{sw} are the switch transconductance and drain resistance, respectively, and r_0 is the current source transistor output resistance.

Eq. (2.20), expressing Z_{on} as the parallel of three terms, turns out to be particularly useful to get the switching part of the output impedance. This is shown in Fig. 2.10(a). Recalling the definition of ΔZ as the inverse of the difference between on-side and off-side conductances (admittances in this case), we can easily infer from Fig. 2.10(a) that the switching impedance consists of the parallel of a switching resistance given by r_0 amplified by the switch gain, $\Delta R = g_{m,\text{sw}} r_{\text{sw}} r_0$ (which we already considered in section 2.2.3), and a switching capacitance given by C_0 reduced by the switch gain, $\Delta C = C_0 / g_{m,\text{sw}} r_{\text{sw}}$. Therefore, the resulting expression of ΔZ is given by:

$$\Delta Z = \frac{g_{m,\text{sw}} r_{\text{sw}} r_0}{1 + s r_0 C_0} \tag{2.21}$$

and the corresponding Bode diagram is shown in Fig. 2.10(b).

As for frequencies $f > f_0 = 1/2\pi r_0 C_0$ the switching capacitance ΔC domi-

nates over the resistive part, Eq. (2.18) becomes:

$$\mathrm{HD}_3 = \left[\frac{N R_\mathrm{L} \cdot 2\pi f \cdot \Delta C}{4}\right]^2 , \tag{2.22}$$

showing that third-order harmonic distortion degrades quadratically with signal frequency (for $f > f_0$) and, even more important, with ΔC. Let us underline once again that only the switching capacitance matters: any fixed capacitance (e.g. C_sw in Fig. 2.9) does not contribute to distortion. Finally, Eq. (2.22) reveals a substantial trade-off between low-frequency and high-frequency linearity: in order to optimize dynamic performances ΔC must be minimized, but, on the other hand, we have seen that the current source transistor area must be enlarged, and hence ΔC must be increased, to improve static accuracy. As we will see in the following, output impedance is not the only source of non-linearity contributing to this trade-off.

2.3.2 Switched capacitance

In addition to its effect on DAC output impedance at high-frequency, the unit cell switching capacitance ΔC also degrades linearity by means of a second mechanism, coming from the switching of current cells from one output node to the other [9]. This phenomenon, which will be referred to as *switched capacitance* non-linearity, is illustrated in Fig. 2.11(a). While the two off capacitances remain fixed at respective output nodes, the switching part of the on capacitance (i.e. ΔC) changes its voltage according to the digital input transitions. Therefore a charge variation on the unit switching capacitance occurs. For instance, when a cell switches from negative to positive output node, the charge difference is given by:

$$\Delta Q = \Delta C \cdot V_\mathrm{OUT}^+ - \Delta C \cdot V_\mathrm{OUT}^- = \Delta C \cdot V_\mathrm{OUT}|_\mathrm{diff} , \tag{2.23}$$

and it can be provided only by a corresponding current ΔI, which is superimposed on the desired output current producing distortion.

From another point of view, the switched capacitance non-linearity can be viewed as caused by variation in time of the total differential capacitance connected to the output. We indeed know that current through a capacitor can be produced by a variation in time of both the voltage and the capacitance

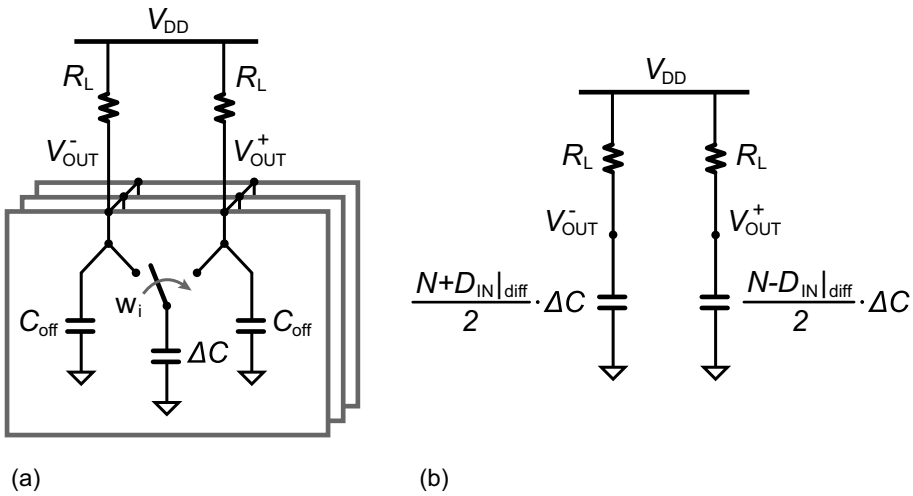

Figure 2.11 (a) Switched capacitance effect and (b) equivalent circuit for calculation of distortion.

values:

$$\Delta I = \frac{\mathrm{d}Q}{\mathrm{d}t} = \frac{\mathrm{d}C_{\mathrm{OUT}}|_{\mathrm{diff}}}{\mathrm{d}t} \cdot V_{\mathrm{OUT}}|_{\mathrm{diff}} + C_{\mathrm{OUT}}|_{\mathrm{diff}} \cdot \frac{\mathrm{d}V_{\mathrm{OUT}}|_{\mathrm{diff}}}{\mathrm{d}t} \,. \tag{2.24}$$

The second term of Eq. (2.24) accounts for current through the capacitive portion of the output impedance and its effect has been already evaluated in section 2.3.1. On the other hand, the first term is the non-linear current due to the switched capacitance effect.

For calculation of distortion, let us refer to the equivalent circuit of Fig. 2.11(b), where fixed capacitances, independent on input code, are neglected. Under this assumption, the total differential capacitance is given by:

$$C_{\mathrm{OUT}}|_{\mathrm{diff}} = \frac{N\Delta C}{4} \cdot \left(1 - x^2\right), \tag{2.25}$$

in which, as above mentioned, $x = D_{\mathrm{IN}}|_{\mathrm{diff}}/N$ is the normalized digital input. Hence, the non-linear current is obtained by multiplying the time derivative of Eq. (2.25) by the output voltage $V_{\mathrm{OUT}}|_{\mathrm{diff}} = (1/2) \cdot NIR_{\mathrm{L}}|_{\mathrm{diff}} \cdot x$:

$$\Delta I = -\frac{N^2 IR_{\mathrm{L}}|_{\mathrm{diff}}\Delta C}{4} \cdot x^2 \cdot \frac{\mathrm{d}x}{\mathrm{d}t} \,. \tag{2.26}$$

When a single-tone sine wave is applied, $x = \cos(2\pi ft)$, a third-order distortion

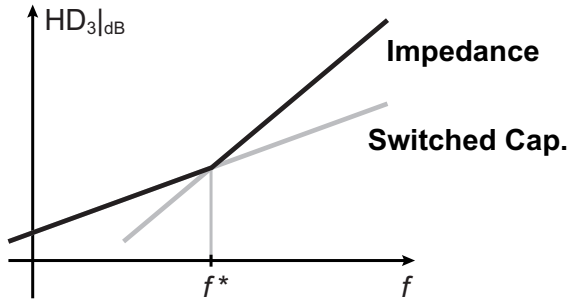

Figure 2.12 Third-order harmonic distortion as a function of frequency.

component appears leading to:

$$\mathrm{HD}_3 = \frac{NR_\mathrm{L} \cdot 2\pi f \cdot \Delta C}{4}\,. \tag{2.27}$$

Interestingly, comparing Eq. (2.27) with Eq. (2.22), it can be noticed that switched capacitance distortion is given by the same expression of output impedance distortion, but without the square power. In this case distortion linearly degrades, instead of quadratically, as signal frequency and switching capacitance increase.

At this point two essential considerations can be made. First, because of the dependency on ΔC, even the switched capacitance effect turns out to contribute to the trade-off between static and dynamic linearity. Second, given certain resolution and ΔC, a frequency value f^* can be calculated, above which the output impedance non-linearity starts to dominate over the switched capacitance one:

$$f^* = \frac{4}{2\pi N R_\mathrm{L} \Delta C}\,. \tag{2.28}$$

This is shown in Fig. 2.12. For practical values of resolution and ΔC, f^* is often above the Nyquist frequency and then HD_3 is limited by the switched capacitance effect over the entire Nyquist bandwidth. For example, in a 10-bit 2.5 GS/s DAC this happens if $\Delta C < 19\,\mathrm{fF}$, which can be easily achieved in scaled CMOS technologies.

2.3.3 Switching transients and switch driver mismatch

We have presented so far two examples of dynamic non-linearity errors, the output impedance distortion and the switched capacitance distortion, which

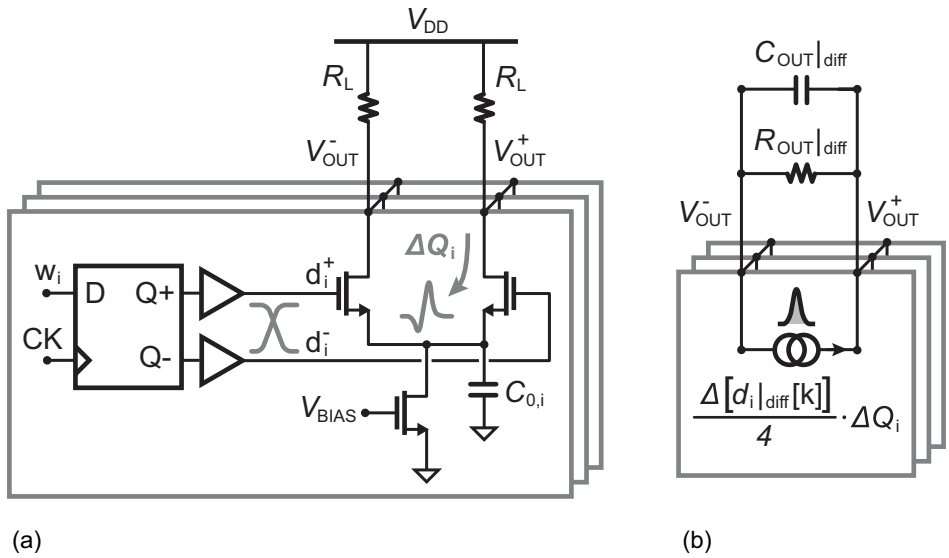

Figure 2.13 (a) Switching transient error and (b) equivalent circuit for calculation of distortion.

are intrinsically related to current-steering circuit topology. However, in addition to this kind of systematic non-linearity mechanisms, there is a class of dynamic errors originating from mismatches among current cells and their driving circuits. An example is given by the so-called *switching transient* error represented in Fig. 2.13(a) [11], [30]. For every current cell that is switching, the error comes from the different switching behavior of the transistor that turns on with respect to the one turning off. In fact, this asymmetrical transient of the differential switch produces an unavoidable voltage fluctuation at the common-source node and, hence, a charge variation on capacitance $C_{0,i}$, which is in general different for every $i = 0, \ldots, N$. Once again, the charge difference can be recovered only by a current spike superimposed to the output current generating distortion. The total glitch in the output signal is the sum of current spikes of all and only the switching cells.

On the basis of these considerations, the equivalent differential model for the evaluation of switch transients effect is shown in Fig. 2.13(b), where $R_{\mathrm{OUT}}|_{\mathrm{diff}}$ and $C_{\mathrm{OUT}}|_{\mathrm{diff}}$ non-linearities are neglected for simplicity. For what concerns the switching transient of each current cell, it is simply modeled by a delta-like current source injecting charge into the load only at the switching instants of the corresponding digital control signals $d_i|_{\mathrm{diff}}[k]$. It follows that the total

glitch charge at the k-th sample transition is given by:

$$Q_{\mathrm{OUT}}|_{\mathrm{diff}} = \sum_{i=0}^{N} \frac{1}{4} \cdot \Big[d_i|_{\mathrm{diff}}[k] - d_i|_{\mathrm{diff}}[k-1] \Big] \cdot \Delta Q_i \,, \tag{2.29}$$

in which ΔQ_i stands for the charge error of the i-cell and the factor $1/4$ accounts for both the term $1/2$ due to differential mode representation and the normalization factor of the difference $d_i|_{\mathrm{diff}}[k] - d_i|_{\mathrm{diff}}[k-1]$.

If we assume for a moment that all cells are identical, we obtain:

$$Q_{\mathrm{OUT}}|_{\mathrm{diff}} = \frac{\Delta Q}{4} \cdot \Big[D_{\mathrm{IN}}|_{\mathrm{diff}}[k] - D_{\mathrm{IN}}|_{\mathrm{diff}}[k-1] \Big] \simeq \frac{T_{\mathrm{S}} \Delta Q}{4} \cdot \frac{\mathrm{d} D_{\mathrm{IN}}|_{\mathrm{diff}}}{\mathrm{d}t} \,. \tag{2.30}$$

Eq. 2.30 reveals that in the ideal case the glitch area in the output current is strictly proportional to the time derivative of digital input and, hence, to the signal frequency. Furthermore, this means that if there were not mismatches then there would not be distortion [14]. Therefore, in practice, only the presence of mismatches (random or systematic) makes the switch transients produce a non-linear distortion that linearly degrades as frequency increases.

More in general, the validity of this analysis and modeling can be extended to all mismatch-induced dynamic errors occurring at cell transitions, such as switch charge-feedthrough, driver mismatch, etc. For instance, the effect of relative deviations between different cells switching moments due to driver circuits impairments can be modeled in the same way as seen above for switching transients. It is well known from literature that, in order to minimize distortion due to driver mismatches, fast transition of driving signals and good matching of driver devices are required [8]. Both of these countermeasures implicate an increased power consumption, leading to an obvious trade-off between dynamic linearity and power efficiency.

2.3.4 Supply noise

A fundamental phenomenon contributing to dynamic non-linearity in current steering DACs is the supply noise due to parasitic inductive impedances of both the internal supply distribution network and the IC package connections. In general, this is a critical issue affecting all modern digital and analog mixed-signal integrated circuits, in particular large SoCs which are made up for the most part by switching CMOS digital circuits, characterized by extremely steep currents absorption from power supply lines. The origin of supply noise is indeed the $L \cdot \mathrm{d}i/\mathrm{d}t$ voltage drop on supply, induced by dynamic variations

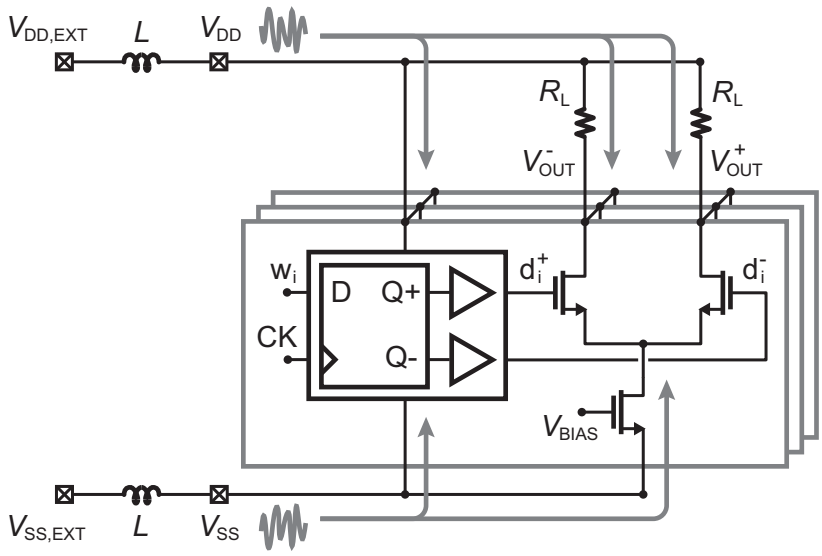

Figure 2.14 Effetct of supply noise on switch driver delay and output voltage.

of currents absorbed by switching circuits. The generated voltage ripple can, in turn, influence other sensitive analog circuits (such as PLLs, ADCs, DACs, etc.) degrading their performances.

The impact of supply noise on current-steering DACs is shown in Fig. 2.14, in which common supply voltage (V_{DD}) and ground (V_{SS}) for all circuits are assumed.[2] Aside from other possible digital circuits, not displayed in Fig. 2.14, supply noise is mainly generated by CMOS latch drivers commutations. This means that supply noise is correlated to the time derivative of DAC digital input and, as a consequence, its magnitude increases with signal frequency. Supply disturbances translate into distortion by two mechanisms. The first is the code-dependent modulation of current cells switching instants, because in turn the drivers delay depends on supply ($V_{DD} - V_{SS}$), while the second comes from the finite Power Supply Rejection-Ratio (PSRR) of the output circuits.

Contrary to other sources of non-linearity we have previously shown, supply noise can be in some way considered extrinsic to the DAC, since it is produced by factors external to the DAC itself (e.g. supply parasitic impedances). At the cost of a greater area and power consumption, supply-induced distortion can be reduced by using proper decoupling capacitors [31], on-chip linear voltage regulators [6] and flip-chip IC packages [8].

[2]In practical applications, the DAC load is usually external and hence the current cells V_{DD} is typically different from V_{DD} of other circuits. Anyway, we can assume a unique power supply without loss of generality.

2.4 FoM for Nyquist performance comparison

In previous sections we went through a complete analysis of main sources of static and dynamic distortion pointing out how much they differ from each other in terms of dependency on factors like frequency, switching impedance, device sizes, etc. This poses the problem of how we can get a fair comparison between different DACs. We indeed can not compare various DACs only on the basis of a single performance parameter, like for instance the SFDR, because they can be extremely different regarding some other aspects (e.g. sampling frequency, power efficiency, output swing, etc.). Therefore, the only way to obtain a true comparison is defining a Figure-of-Merit (FoM) accounting for, at the same time, all the main DAC performance metrics.

Unfortunately, none of DAC FoM definitions reported in literature can completely capture DAC performances, in particular at high frequency, each of them privileging one aspect over the others [9]. For this reason we propose in this section a new DAC FoM definition, especially suited for comparison of Nyquist performances of CMOS current-steering DACs with sampling frequency in the GS/s range. To this purpose, as a first step, DAC performance metrics ($\mathrm{SFDR}|_{\mathrm{Nyq}}$ and power efficiency in our case) must be mapped to physical parameters of circuit devices in order to bring out fundamental trade-offs.

2.4.1 SFDR at Nyquist frequency

Fig. 2.15 shows the generic DAC SFDR trend as a function of input signal frequency, as it resulted from analysis of static and dynamic non-linearity errors of section 2.2 and 2.3, respectively. Low-frequency linearity is typically limited by static mismatches among current sources and SFDR is constant. Then, as signal frequency increases, SFDR starts to drop with a $-20\,\mathrm{dB/dec}$ slope, because of those dynamic errors which linearly depends on frequency, i.e. switched capacitance effect, switching transients, driver mismatch and supply noise. Finally, for $f > f^*$ (let us refer to Eq. (2.28)) output impedance distortion is dominant over other effects and SFDR goes with a $-40\,\mathrm{dB/dec}$ roll-off. Since we are interested in a FoM describing performances at Nyquist frequency ($f_S/2$), we have inevitably to make a choice on the basis of some arbitrary hypothesis. For what seen in section 2.3.2, the most reasonable assumption is to consider a Nyquist frequency well below f^* and, hence, $\mathrm{SFDR}|_{\mathrm{Nyq}}$ limited by the switched capacitance effect.[3]

[3] We are implicitly assuming that mismatch-induced dynamic errors are non-dominant. This is in practice a reasonable hypothesis proved by circuit simulations.

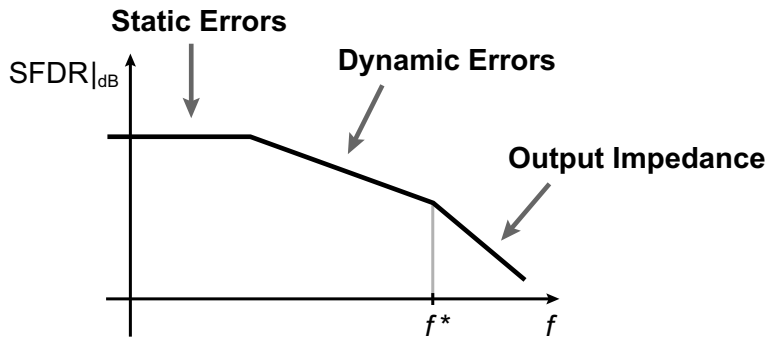

Figure 2.15 SFDR vs. frequency.

On the basis of these considerations $\mathrm{HD}_3|_{\mathrm{Nyq}}$ is given by Eq. (2.27), where the switched capacitance can be expressed as the sum of two terms, due to the switch gate-source capacitance $C_{gs,\mathrm{sw}}$ and the current source drain capacitance $C_{d,\mathrm{gen}}$, respectively:

$$\Delta C = \frac{C_0}{g_{m,\mathrm{sw}} r_{\mathrm{sw}}} = \frac{C_{gs,\mathrm{sw}}}{g_{m,\mathrm{sw}} r_{\mathrm{sw}}} + \frac{C_{d,\mathrm{gen}}}{g_{m,\mathrm{sw}} r_{\mathrm{sw}}} \,. \tag{2.31}$$

Although the simple transistor square-law model is not very accurate for ultra-scaled technologies, it is still adequate to derive simple fundamental relations. Therefore, remembering the expression of transistor gain ($g_m r_0 = 2\alpha L/V_{\mathrm{ov}}$) and current ($I = (1/2)\mu_n C_{ox}(W/L)V_{\mathrm{ov}}^2$), after some calculations, the first term fo Eq. (2.31) can be rewritten as:

$$\frac{C_{gs,\mathrm{sw}}}{g_{m,\mathrm{sw}} r_{\mathrm{sw}}} \propto \frac{L_{\mathrm{sw}}}{V_{\mathrm{ov,sw}}} \cdot I \,, \tag{2.32}$$

highlighting that the contribution of $C_{gs,\mathrm{sw}}$ to the switched capacitance, given a fixed LSB current I, can be minimized by reducing the switch length and by increasing its overdrive voltage $V_{\mathrm{ov,sw}}$. For what concerns the second term of Eq. (2.31), $C_{d,\mathrm{gen}}$ is proportional to the transistor width W_{gen}, which in turn depends on current and, indirectly, on $V_{\mathrm{ov,sw}}$ and switch gate driving voltage V_{driv}, since transistor operation must be ensured in saturation region. V_{driv} corresponds to the driver supply voltage and it can be in general different from the current cells supply voltage V_{DD}. After a few steps we obtain:

$$\frac{C_{d,\mathrm{gen}}}{g_{m,\mathrm{sw}} r_{\mathrm{sw}}} \propto \frac{L_{\mathrm{gen}} V_{\mathrm{ov,sw}}}{L_{\mathrm{sw}}(V_{\mathrm{driv}} - V_{\mathrm{T}} - V_{\mathrm{ov,sw}})^2} \cdot I \,. \tag{2.33}$$

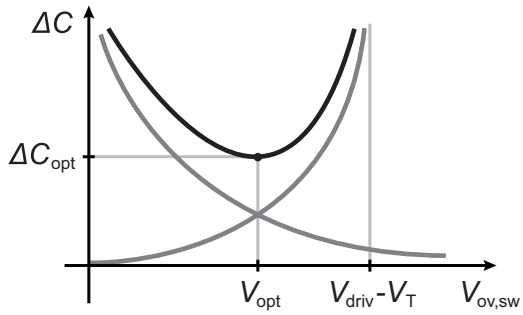

Figure 2.16 Switching capacitance vs. switch overdirve voltage.

Fig. 2.16 shows the two contributions of switching capacitance, for a given LSB current I, as a function of the switch overdrive voltage, suggesting that once having chosen L_{gen} and L_{sw} on the basis of matching and output resistance considerations, an optimum value of $V_{\text{ov,sw}}$ exists, that minimizes ΔC and hence distortion. Being both contributions directly proportional to current, we can write:

$$\Delta C_{\text{opt}} = \Delta C^*_{\text{opt}} \cdot I \,, \tag{2.34}$$

In which ΔC^*_{opt} is the optimum switching capacitance per unit of current and it is substantially determined only by process and DAC static linearity requirements.

At this point, remembering that according to the model of Eq. (2.5), the peak-to-peak differential output voltage swing can be expressed as:

$$V_{\text{OUT}}|^{\text{pp}}_{\text{diff}} = NIR_{\text{L}}|_{\text{diff}} \,, \tag{2.35}$$

we can calculate the SFDR at Nyquist frequency. Substituting Eq. (2.34) in Eq. (2.27) and rearranging the expression by using Eq. (2.35), we obtain:

$$\text{SFDR}|_{\text{Nyq}} = \frac{8}{\pi \Delta C^*_{\text{opt}}} \cdot \frac{1}{V_{\text{OUT}}|^{\text{pp}}_{\text{diff}}} \cdot \frac{1}{f_{\text{S}}} \,. \tag{2.36}$$

Interestingly, Eq. (2.36) indicates that in an optimally designed DAC limited by the switched capacitance effect, the SFDR at Nyquist inversely depends on both the maximum output swing and the sampling frequency.

2.4.2 Power efficiency

The second most important DAC performance measure is the power efficiency as defined by Eq. (1.3) in Chapter 1. To get the relationship between DAC total power consumption and circuit parameters, we can distinguish two separate contributions: the current cells power P_{cell} and the driver circuits power P_{driv}. The first term is independent on frequency, but related to the desired output voltage:

$$P_{\text{cell}} = NIV_{\text{DD}} = \frac{V_{\text{OUT}}|_{\text{diff}}^{\text{pp}}}{R_{\text{L}}|_{\text{diff}}} \cdot V_{\text{DD}}\,, \tag{2.37}$$

while the second, in the case of a CMOS implementation, is strictly proportional to f. Under the practical assumption of a tapered design of driver circuits, we can approximate P_{driv} as mainly determined by the last driver circuits, interfacing with current cells [9]:

$$P_{\text{driv}} = N(C_{g,\text{sw}}V_{\text{driv}}^2) \cdot \frac{f_{\text{S}}}{2} = \frac{L_{\text{sw}}^2 V_{\text{driv}}^2}{\mu_n V_{\text{ov,sw}}^2} \cdot \frac{V_{\text{OUT}}|_{\text{diff}}^{\text{pp}}}{R_{\text{L}}|_{\text{diff}}} \cdot f_{\text{S}} \tag{2.38}$$

where V_{driv} stands for the driver supply voltage and the maximum switching frequency has been considered ($f_{\text{S}}/2$).

Comparing Eq. (2.38) and (2.37), it is straightforward to notice that current cells power consumption dominates over the drivers one if sampling frequency is not too high (and, even more important, regardless of $V_{\text{OUT}}|_{\text{diff}}^{\text{pp}}$):

$$f_{\text{S}} < \frac{\mu_n V_{\text{ov,sw}}^2}{L_{\text{sw}}^2 V_{\text{driv}}^2} \cdot V_{\text{DD}}\,. \tag{2.39}$$

As an example, in a 28 nm CMOS DAC with $V_{\text{driv}} = V_{\text{DD}} = 1\,\text{V}$ ($\mu_n = 120\,\mu\text{A/V}^2$), the use of $L_{\text{sw}} = 30\,\text{nm}$ and $V_{\text{ov,sw}} = 200\,\text{mV}$ guarantees that power consumption is dominated by current cells for sampling frequencies $f_{\text{S}} < 5.3\,\text{GS/s}$, which is a very high limit for practical applications. It follows that in general we can roughly approximate P_{TOT} with P_{cell}. Hence, the Normalized Power Efficiency simplifies to the simple ratio between differential output swing and current cells supply voltage:

$$\text{NPE} = \frac{P_{\text{load}}}{0.25 \cdot P_{\text{TOT}}} = \frac{V_{\text{OUT}}|_{\text{diff}}^{\text{pp}}}{V_{\text{DD}}}\,. \tag{2.40}$$

2.4.3 Figure-of-Merit

After having analyzed the relationship between DAC parameters and performance metrics we can easily define a proper Figure-of-Merit. In order to be a meaningful *number*, FoM must be independent on f_S and $V_{OUT}|_{diff}^{pp}$, so that, given a certain DAC, it remains the same even for different operating conditions.

Since we have seen that $SFDR|_{Nyq}$ inversely depends on both sampling frequency and output swing, while NPE is directly proportional to $V_{OUT}|_{diff}^{pp}$, we can define the FoM as the product between $SFDR|_{Nyq}$ and NPE multiplied by the sampling frequency f_S. Combining Eq. (2.36) with Eq. (2.40), it results:

$$FoM = SFDR|_{Nyq} \cdot f_S \cdot NPE = \frac{8}{\pi \Delta C_{opt}^* V_{DD}}\,, \tag{2.41}$$

which is measured in Hz. Let us note that we used here the SFDR linear expression of Eq. (2.36). Using $SFDR|_{Nyq}$ measured in dB, FoM definition must be rewritten as:

$$FoM = 2^{\frac{SFDR|_{Nyq}-1.76}{6.02}} \cdot f_S \cdot NPE\,. \tag{2.42}$$

Looking at FoM expression given by Eq. (2.41), two essential considerations can be made. First, under the hypothesis of linearity limited by switched capacitance effect and power consumption dominated by current cells, FoM effectively describes Nyquist performances depending only on process-related parameters, ΔC_{opt}^* and V_{DD}, as desired. Second, Eq. (2.41) clearly demonstrates that in order to improve a DAC FoM, both the switching capacitance per unit of current (ΔC_{opt}^*) and supply voltage (V_{DD}) must be minimized.

This last consideration constitutes the fundamental motivation of the DAC design methodology we will present in Chapter 4, based on the use of a new digital adaptive technique allowing, at the same time, the linearization of static characteristic and the minimization of unit cell switching capacitance, even with the low supply voltage needed in ultra-scaled CMOS technologies.

2.5 Overview of state-of-the-art DACs

We are able now to carry out a brief overview of state-of-the-art DACs, focusing on main design solutions and techniques aimed at improving high-frequency performances, which have been published in recent literature. We will limit

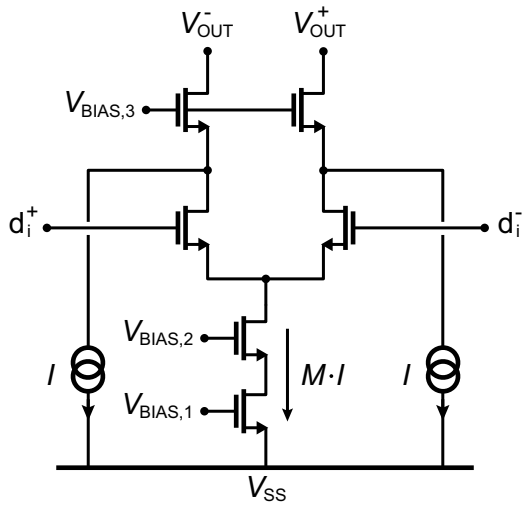

Figure 2.17 Current cell of the design presented in [8].

our analysis to the newest CMOS DACs with sampling frequencies in the GS/s range, whose performances have been already discussed in Chapter 1.

We can identify different classes of design styles and methodologies, all of them oriented at dynamic performance optimization. A first one is the class of DACs which make use of various types of cascoded current cells in the attempt to reduce the switching capacitance seen at the output [8], [9]. The most important example is given by the design presented in [8], whose current cell circuit is shown in Fig. 2.17. By adding local cascodes on top of the switches, with an always on biasing, the original switching capacitance is further divided by an additional transistor gain. Notice that this would not still hold without small currents preventing the cascodes switching off. The DAC achieves a high output swing of $2.5\,V_{pp}$ while requiring a $2.5\,V$ current cells voltage supply (because of the four stacked transistors), resulting in a FoM of about $232\,dBHz$.

Interestingly, the totally alternative approach presented in [10] demonstrates the benefit of using a minimal non-cascoded current cell consisting of near-minimum sized transistors in scaled low-voltage technologies. The DAC, implemented in $65\,nm$ CMOS, achieves a $50\,dB$ SFDR at Nyquist with a $1.2\,V$ power supply, leading to a FoM $\simeq 221\,dBHz$.

In [12] high-frequency performances are improved by implementing the so-called *quad-switch* architecture, already proposed by [24], whose fundamental concept is illustrated in Fig. 2.18. In this configuration the current cell makes

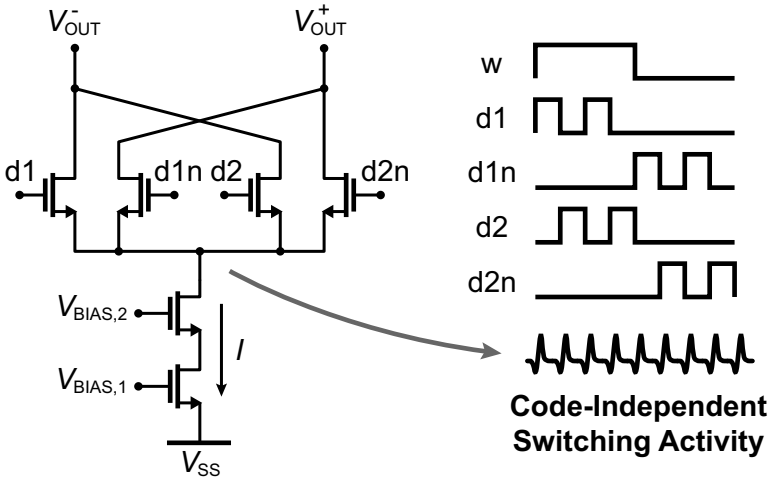

Figure 2.18 Quad-switch operation proposed in [12].

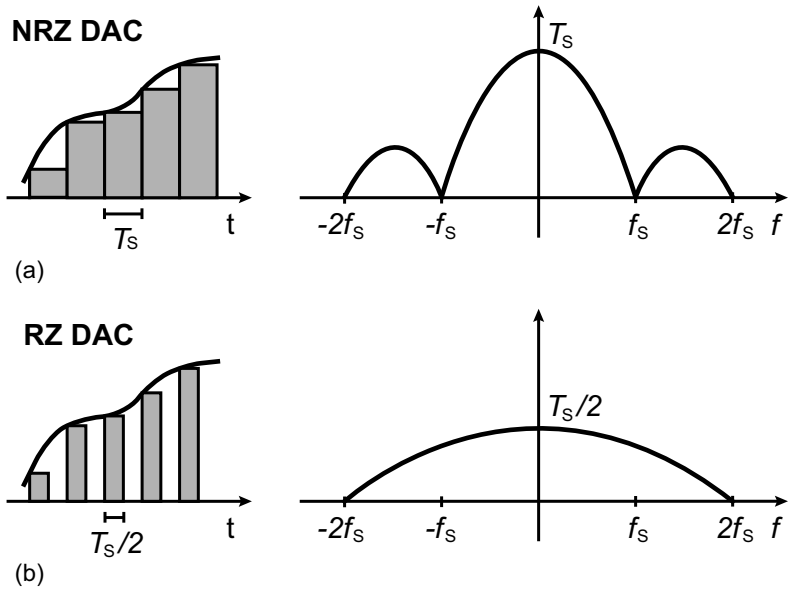

Figure 2.19 Time-domain and spectrum envelope comparison between (a) conventional Non-Return-to-Zero DAC and (b) Return-to-Zero DAC as used in [11], [13].

use of two pairs of differential switches instead of one, which are alternatively activated at each sampling period, so that to create a transient even when there is no current switching (i.e. commutation of control bits). In this way some of the mismatch-induced dynamic errors, like the switching transients, are no longer code-dependent producing noise instead of distortion. However, output impedance and switched capacitance errors still remain limiting high-frequency linearity, as evident from the SFDR vs. frequency plot of Fig. 1.3 in Chapter 1. Although the good linearity, the DAC FoM is limited to 220 dBHz, mainly because of the high power consumption (600 mW).

Finally, another emerging class is that of DACs which make use of Return-to-Zero (RZ) pulses at the output in combination with a randomization technique of the current cells selection [11], [13]. All these designs are based on the essential concepts presented in [26]: since the RZ pulses technique eliminates the inter-symbol interference between successive DAC samples the dynamic non-linearity errors are related to the digital input code, instead of its time derivative. Furthermore, by using a randomization technique, like for instance the well known Dynamic Element Matching (DEM), all the mismatch-induced errors, both static and dynamic, can be scrambled. Main drawback of this approach is its inherently low power efficiency in the first Nyquist bandwidth, as evident from the conceptual comparison between NRZ and RZ pulses in Fig. 2.19. As an example, the design reported in [13] don not reach the best Figure-of-Merit (FoM = 231 dBHz), even though the excellent linearity, just because the very low NPE.

Chapter 3

Behavioral Modeling of Current-Steering DACs

Contents

3.1 Introduction

The growing complexity of modern CMOS Systems-on-Chips for communications is posing critical limitations on design and simulation capabilities of such systems. To overcome these issues, a design methodology based on the extensive use of behavioral models of analog and mixed-signal circuits is becoming more and more essential for both top-down and bottom-up design approaches. In the former case, behavioral modeling allows the translation of high-level system specifications into requirements for building blocks circuits, while in the latter, by implementing extracted circuit parameters in behavioral models, a fast verification of system performance can be done.

Obviously, this is true even for Digital-to-Analog Converters and some ex-

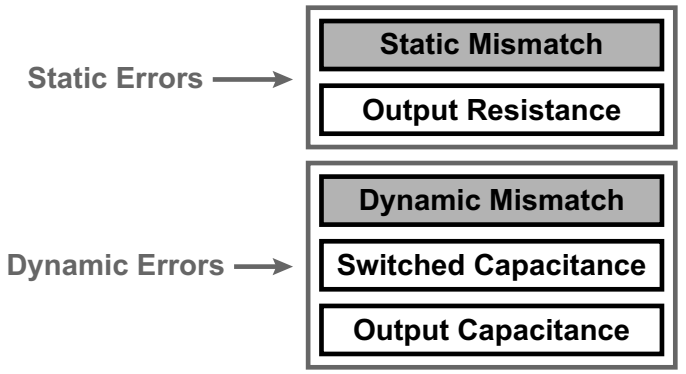

Figure 3.1 Summary of main DAC non-linearity mechanisms.

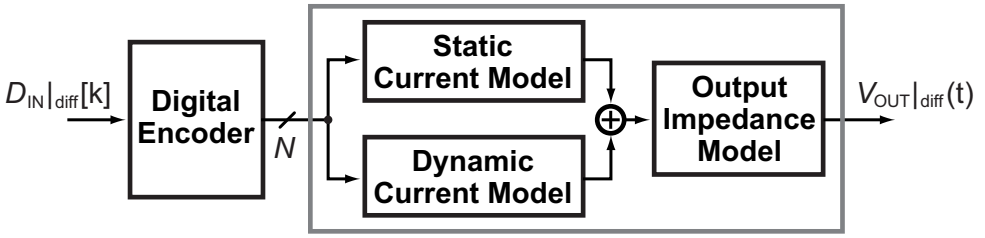

Figure 3.2 Conceptual diagram of the proposed DAC behavioral model.

amples of current-steering DAC models have been reported in literature [32], [33]. In our case in particular, an extremely accurate and, at the same time, simple DAC behavioral model accounting for all non-linearity mechanisms is further needed in order to develop, simulate and implement the digital adaptive linearization technique we will present in detail in Chapter 4.

After having analyzed in the previous chapter the main sources of static and dynamic distortion, it is straightforward now to get a DAC behavioral model which includes all non-linearity effects. To this purpose, looking at the summary scheme of Fig. 3.1, we can make same simple considerations.[1] First of all, a clear distinction exists between systematic errors, depending only on cell switching resistance ΔR and switching capacitance ΔC, and mismatch induced errors (highlighted in gray in Fig. 3.1), which are intrinsically related to static and dynamic mismatches among current cells. As a second observation, we can notice that the combination of (static) output resistance and (dynamic) output capacitance effects is what we have indicated so far as output impedance,

[1]For what seen in section 2.3.4, we can assume to be able to reduce supply noise to any arbitrary level by means of proper countermeasures. For this reason, we will neglect supply noise in the following discussion.

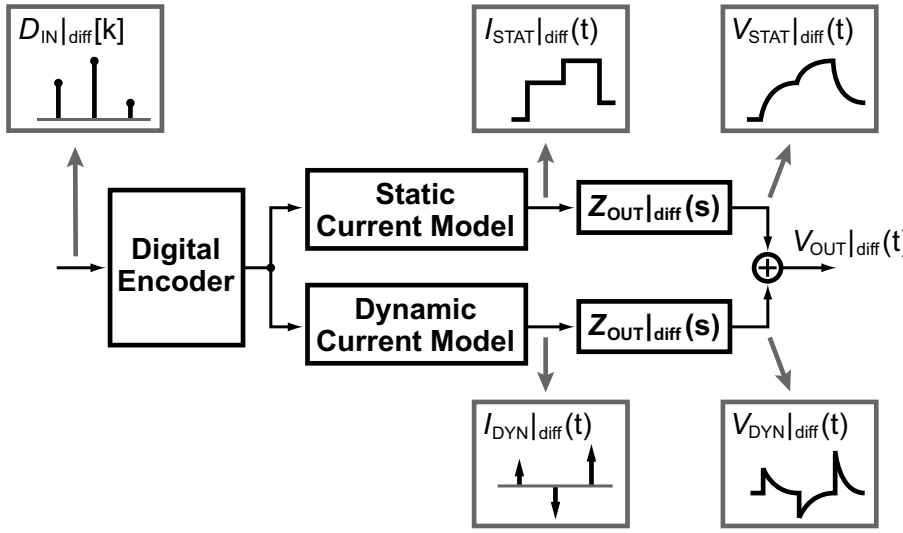

Figure 3.3 Current and voltage waveforms in DAC behavioral model.

that can be modeled as a non-linear first-order transfer function operating the conversion from output current to output voltage (see section 2.3.1). Therefore, in other words, we can distinguish between errors impacting on the output current generation (static and dynamic mismatch, switched capacitance) and errors affecting current-to-voltage conversion (output impedance).

All these preliminary considerations lead to the conceptual DAC behavioral model depicted in Fig. 3.2. The digital encoder performs the transformation from the digital input code, represented by its equivalent integer value $D_{\mathrm{IN}}|_{\mathrm{diff}}[k]$, to the N control signals $d_i|_{\mathrm{diff}}[k]$ with $i = 0, \ldots, N-1$. Then, the conversion from discrete-time control bits to continuous-time output current is carried out by two paths in parallel: the static current model, which generates a current given by the superposition of ideal value and static mismatches, and the dynamic current model, accounting for dynamic mismatch-induced errors (switching transients, driver mismatch, etc.) and switched capacitance effect. Finally, the output impedance model operates the conversion from the resulting current to the output voltage $V_{\mathrm{OUT}}|_{\mathrm{diff}}(t)$.

The fundamental difference between static and dynamic current models lies in the respective output current waveforms. For each sample, while the static current is constant over the entire period T_{S}, the dynamic component can be modeled as a delta-like current injecting charge into the load only at the occurrence of commutations of the current cells digital control signals, as already explained in section 2.3.3. This is highlighted in Fig. 3.3, where current

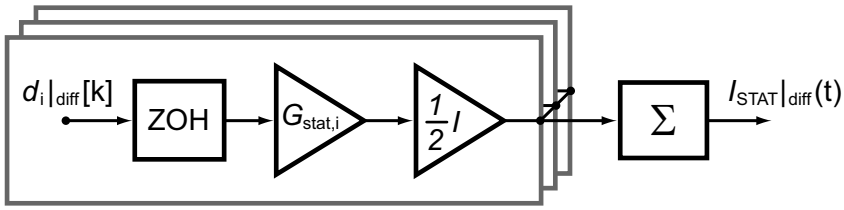

Figure 3.4 Modeling of mismatch-induced static errors.

($I_{\mathrm{STAT}}|_{\mathrm{diff}}(t)$, $I_{\mathrm{DYN}}|_{\mathrm{diff}}(t)$) and voltage ($V_{\mathrm{STAT}}|_{\mathrm{diff}}(t)$, $V_{\mathrm{DYN}}|_{\mathrm{diff}}(t)$) waveforms are shown distinguishing static and dynamic components. The Dirac-delta current approximation is justified because, in practice, actual glitches are extremely short if compared to the sampling period. Furthermore, it can be demonstrated that impact on the output spectrum mainly depends on the *area* of dynamic current, i.e. the charge injected, rather than on its shape [34], [35].

After discussing theoretical aspects, in this chapter we will introduce an accurate discrete-time DAC behavioral model suitable for the implementation in Matlab environment. The effectiveness of the proposed approach will be proved by comparing behavioral simulation against circuit simulation results.

3.2 Static current model

As anticipated in the previous section, the static current model operates the conversion from the discrete-time digital control signals $d_i|_{\mathrm{diff}}[k]$ to the continuous-time static output current $I_{\mathrm{STAT}}|_{\mathrm{diff}}(t)$. For each sample, the static current depends only on the present value of the digital input code and it can be considered as given by the sum of the ideal current (i.e. the desired current without any errors) and the static, both random and systematic, mismatches among the cells. For this reason, contrary to the dynamic counterpart, the static model generates a Zero-Order Hold current that is constant over each sampling period T_{S}.

3.2.1 Mismatch-induced static errors

The static current model is simply built by placing in parallel $N-1$ single current cell sub-models, replicating in this way the current-steering circuit topology. As shown in Fig. 3.4, in each current cell the discrete-to-continuous time conversion is performed by the Zero-Order Hold block (ZOH), which maintains its input value ($+1$ or -1) for a sampling period time interval at the output.

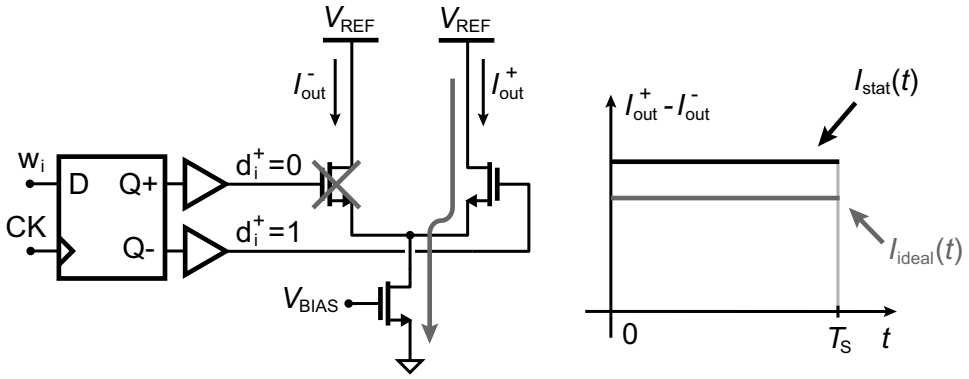

Figure 3.5 Simulation of static mismatch errors.

Then the generation of the output differential current of every i-th cell is obtained by the cascade of two gains. The first, $G_{\mathrm{stat},i}$, stands for the normalized static gain accounting for both ideal and mismatch values:

$$G_{\mathrm{stat},i} = G_{\mathrm{ideal},i} \cdot (1 + \varepsilon_{\mathrm{stat},i}) \,, \tag{3.1}$$

where $G_{\mathrm{ideal},i}$ is the ideal normalized gain (equal to 1 in a fully thermometric configuration, but to a power of two in a more general case), while $\varepsilon_{\mathrm{stat},i}$ is the relative static error resulting from combination of systematic and random effects. The successive multiplications by the LSB current I and the 1/2 factor operate the conversion to current and to differential mode, respectively. Finally, the overall static output current is obtained by summing all the currents coming from the N cells:

$$I_{\mathrm{STAT}}|_{\mathrm{diff}}(t) = \frac{1}{2} I \sum_{i=0}^{N-1} d_i|_{\mathrm{diff}}[k] \cdot G_{\mathrm{stat},i} \quad \text{for } kT_{\mathrm{S}} \le t < (k+1)T_{\mathrm{S}} \,. \tag{3.2}$$

In a top-down design approach, the relative mismatch values $\varepsilon_{\mathrm{stat},i}$ can be determined upon some preliminary assumptions on, for instance, technology matching parameters, process variations, estimations of systematic error, etc. On the other hand, in a bottom-up perspective, mismatches can be extracted by circuit simulations. The setup for simulating a current cell static error is shown in Fig. 3.5, along with the diagram of corresponding currents over an interval T_{S}. Referring to charge instead of current (for consistency with the following discussion about the dynamic current model), the relative mismatch

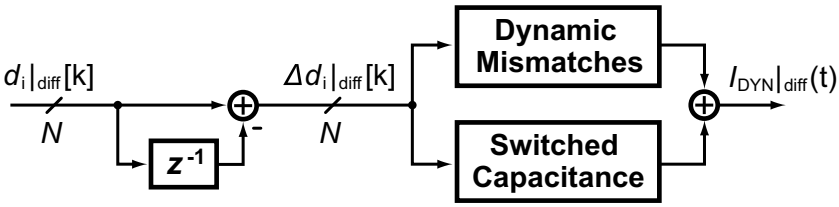

Figure 3.6 Dynamic current model.

can be expressed as:

$$\varepsilon_{\mathrm{stat},i} = \frac{Q_{\mathrm{stat},i} - Q_{\mathrm{ideal},i}}{Q_{\mathrm{ideal},i}} \,. \tag{3.3}$$

Repeating the same simulation over a great number of samples (i.e. running a Monte-Carlo simulation), we can get an estimation of the mean value and the standard deviation of $\varepsilon_{\mathrm{stat},i}$, which in turn have to be implemented in the static current model, to get a fair DAC representation.

3.3 Dynamic current model

The delta-like currents of the dynamic model are generated only at the occurrences of switchings in the digital control signals. For this reason, contrary to the stationary case, the dynamic component of each current cell can be modeled as related to the differentiation between the present and the previous values of the corresponding control signal:

$$\Delta d_i|_{\mathrm{diff}}[k] = d_i|_{\mathrm{diff}}[k] - d_i|_{\mathrm{diff}}[k-1] \,. \tag{3.4}$$

This correctly means that dynamic errors at DAC output would be null in presence of a constant digital input. In practice, we have seen that distortion is determined by the combination of dynamic mismatches and switched capacitance effect. This is depicted in Fig. 3.6, where the dynamic current model is realized by the parallel of two paths (implementing mismatch-induced errors and switched capacitance effect, respectively), fed by the N differentiation signals $\Delta d_i|_{\mathrm{diff}}[k]$.

3.3.1 Mismatch-induced dynamic errors

Modeling of dynamic mismatches is substantially analogous to that of static current model, except for some simple differences. First of all, as shown in

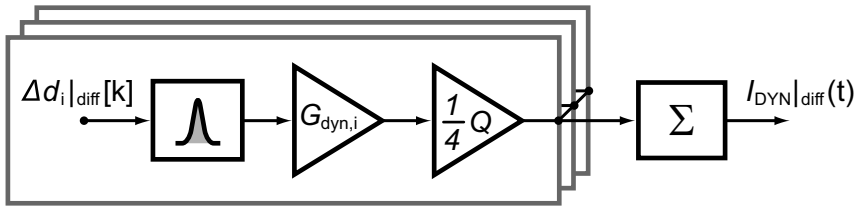

Figure 3.7 Modeling of mismatch-induced dynamic errors.

Fig. 3.7, the discrete-to-continuous time conversion in the i-th cell is achieved by means of a Dirac-delta shaper, which receives as input the differentiation signal $\Delta d_i|_{\text{diff}}[k]$. The impulse area, i.e. the charge injected into the output, is obtained by multiplication by the normalized dynamic gain:

$$G_{\text{dyn},i} = G_{\text{ideal},i} \cdot \varepsilon_{\text{dyn},i}\,, \tag{3.5}$$

followed by the gain $Q = IT_{\text{S}}$ (i.e. the LSB charge injected by a current I over a sampling period) and the scaling factor 1/4, which accounts for both differential mode representation and normalization of $\Delta d_i|_{\text{diff}}[k]$. Summing all the N dynamic currents, we obtain:

$$I_{\text{DYN}}|_{\text{diff}}(t) = \frac{1}{4} Q \delta(t - kT_{\text{S}}) \sum_{i=0}^{N-1} \Delta d_i|_{\text{diff}}[k] \cdot G_{\text{dyn},i}\,, \tag{3.6}$$

which is consistent with the analysis drawn in section 2.3.3 in Chapter 2.

The extraction of relative dynamic mismatches $\varepsilon_{\text{dyn},i}$ can be performed by the simulation setup displayed in Fig. 3.8, in which all the error sources (e.g. switching transients, driver mismatch, etc.) are included. A complete switching transient is simulated over a sampling period T_{S} in such a way that the time integral of the ideal waveform is zero. Hence, the dynamic charge error $Q_{\text{dyn},i}$ can be directly obtained by integrating the difference between positive and negative currents $I_{\text{dyn}}(t) = I^{+}_{\text{out}}(t) - I^{-}_{\text{out}}(t)$. Then, we can get the relative dynamic error by normalizing to the ideal charge that would result from a constant current (as defined in the static case):

$$\varepsilon_{\text{dyn},i} = \frac{Q_{\text{dyn},i}}{Q_{\text{ideal},i}}\,. \tag{3.7}$$

Once again, in order to estimate mean and standard deviation values of $\varepsilon_{\text{dyn},i}$ to be implemented in the dynamic current model, a Monte-Carlo simulation is needed.

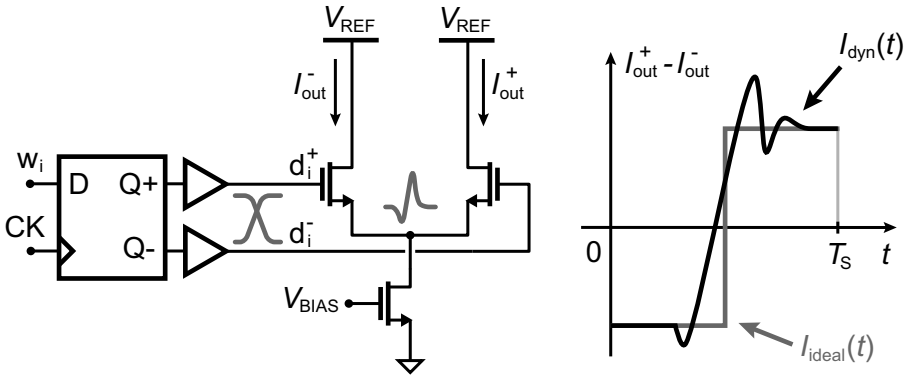

Figure 3.8 Simulation of dynamic mismatch errors.

3.3.2 Switched capacitance

Modeling of switched capacitance effect can be achieved by remembering the physical mechanism underlying distortion. We have seen in the previous chapter that the switched capacitance non-linearity is caused by charge variations due to switchings of unit current cells (and hence of their corresponding ΔC) from one output node to the other. The fundamental observation to model this effect is that the polarity of charge injected into the load does not depend on the digital input, but only on the differential output voltage. To explain this assertion, let us focus on the contribution of the single i-th unit cell. If the differentiation signal is positive ($\Delta d_i|_{\text{diff}} = +1$), ΔC switches from negative to positive output node, resulting in a charge:

$$+\Delta C \cdot (V_{\text{OUT}}^{+} - V_{\text{OUT}}^{-}) = +\Delta C \cdot V_{\text{OUT}}|_{\text{diff}} \,. \tag{3.8}$$

On the contrary, the commutation in the opposite direction ($\Delta d_i|_{\text{diff}} = -1$) produces:

$$-\Delta C \cdot (V_{\text{OUT}}^{-} - V_{\text{OUT}}^{+}) = +\Delta C \cdot V_{\text{OUT}}|_{\text{diff}} \,. \tag{3.9}$$

Comparison between Eq. (3.8) and (3.9) effectively shows that the sign of differentiation signals does not impact on distortion charge, which only depends on $V_{\text{OUT}}|_{\text{diff}}$. This is the cause of the third-order non-linearity we calculated in section 2.3.2.

On the basis of this consideration, the switched capacitance model must incorporate two essential features. First, a block calculating the absolute value of $\Delta d_i|_{\text{diff}}[k]$ is needed, so that to eliminate dependency on its sign. Second,

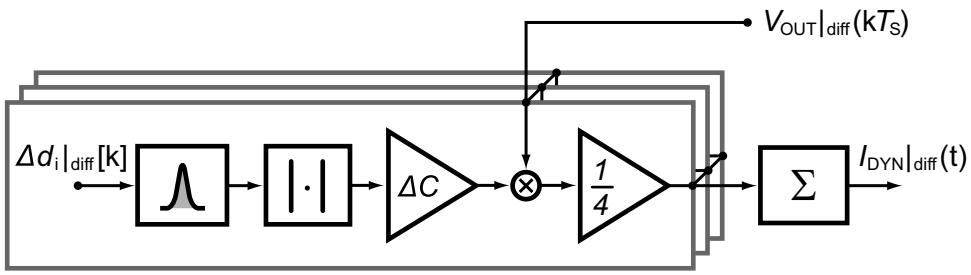

Figure 3.9 Modeling of switched capacitance effect.

a feedback path must be implemented, bringing back the DAC output signal $V_{\mathrm{OUT}}|_{\mathrm{diff}}$ (sampled at the corresponding kT_{S} time instant) to the input of switched capacitance model. This is shown in Fig. 3.9. Once again, in every current cell sub-model the continuous-time waveform is obtained by an impulse shaper, while the amplitude is determined by the product between ΔC, which can be extracted by circuit simulations, and $V_{\mathrm{OUT}}|_{\mathrm{diff}}$. Finally, 1/4 scaling factor is needed for compliance with the differential mode representation.

3.4 Output impedance model

The conversion from the overall output current $I_{\mathrm{OUT}}|_{\mathrm{diff}}(t) = I_{\mathrm{STAT}}|_{\mathrm{diff}}(t) + I_{\mathrm{DYN}}|_{\mathrm{diff}}(t)$ to the differential output voltage $V_{\mathrm{OUT}}|_{\mathrm{diff}}(t)$ is operated by the output impedance model, which has to account for both the non-linear part (due to current cell switching resistance and capacitance, ΔR and ΔC) and the fixed load components (R_{L} and C_{L}) contributing to limit the DAC output bandwidth. The simplest way to model such output impedance is by means of a non-linear first-order transfer function $Z_{\mathrm{OUT}}|_{\mathrm{diff}}(s)$ defined as:

$$Z_{\mathrm{OUT}}|_{\mathrm{diff}}(s) = \frac{R_{\mathrm{OUT}}|_{\mathrm{diff}}[k]}{1 + sR_{\mathrm{OUT}}|_{\mathrm{diff}}[k]C_{\mathrm{OUT}}|_{\mathrm{diff}}[k]}\,, \tag{3.10}$$

in which the constituent parameters $R_{\mathrm{OUT}}|_{\mathrm{diff}}[k]$ and $C_{\mathrm{OUT}}|_{\mathrm{diff}}[k]$ depend on the digital input code $D_{\mathrm{IN}}|_{\mathrm{diff}}[k]$ and, hence, they can vary from one sample k to the other. This is depicted in the conceptual diagram of Fig. 3.10.

We can calculate $R_{\mathrm{OUT}}|_{\mathrm{diff}}[k]$ and $C_{\mathrm{OUT}}|_{\mathrm{diff}}[k]$ simply on the basis of the considerations on output impedance we carried out in Chapter 2. The differential output resistance is given by the sum of overall conductances connected

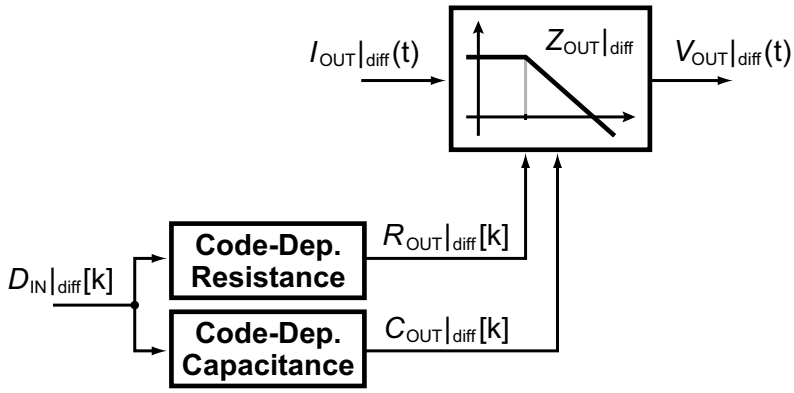

Figure 3.10 Conceptual diagram of the output impedance model.

to positive and negative output nodes:

$$\begin{aligned} G^{+}_{\mathrm{OUT}}[k] &= G_{\mathrm{L}} + \frac{N - D_{\mathrm{IN}}|_{\mathrm{diff}}[k]}{2} \cdot \Delta G \\ G^{-}_{\mathrm{OUT}}[k] &= G_{\mathrm{L}} + \frac{N + D_{\mathrm{IN}}|_{\mathrm{diff}}[k]}{2} \cdot \Delta G \end{aligned} \tag{3.11}$$

in which the current cell R_{off} has been neglected, leading to $\Delta R = R_{\mathrm{on}}$. On the other hand, the differential output capacitance is obtained by the parallel of positive and negative output contributions:

$$\begin{aligned} C^{+}_{\mathrm{OUT}}[k] &= C_{\mathrm{L}} + \frac{N - D_{\mathrm{IN}}|_{\mathrm{diff}}[k]}{2} \cdot \Delta C \\ C^{-}_{\mathrm{OUT}}[k] &= C_{\mathrm{L}} + \frac{N + D_{\mathrm{IN}}|_{\mathrm{diff}}[k]}{2} \cdot \Delta C \end{aligned} \tag{3.12}$$

where C_{L} includes both the external load capacitance and the sum of all the cells parasitic off components (C_{off}). Notice that, in order to build this model, we have to extract from circuit simulations only four parameters: ΔR, ΔC, R_{L} and C_{L}.

3.5 Matlab implementation

We have introduced so far a DAC behavioral model describing the transformation from the discrete-time digital input code $D_{\mathrm{IN}}|_{\mathrm{diff}}[k]$ to the continuous-time output voltage $V_{\mathrm{OUT}}|_{\mathrm{diff}}(t)$. However, in order to make this model suitable for implementation in Matlab environment, an additional step is required. Indeed, to be able to exploit speed and efficiency of Matlab simulations, a fixed-step

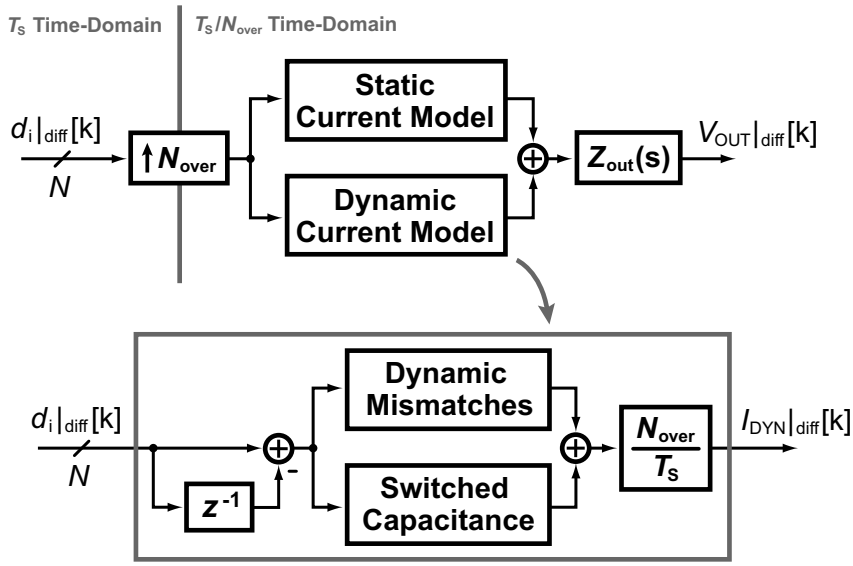

Figure 3.11 Discrete-time oversampled DAC model.

discrete-time DAC model is needed.

The most straightforward way to get it simply consists in translating the continuous-time model into an oversampled discrete-time one, as displayed in Fig. 3.11. The interface between the (external) T_S time-domain and the DAC T_S/N_{over} time-domain is operated by a Zero-Order Hold interpolation filter (the N_{over} up-sampler in Fig. 3.11), which maintains its input values $d_i|_{diff}[k]$ for N_{over} samples at the output. Although in a discrete-time way, this architecture still allows a correct model of DAC dynamic output current and voltage waveforms.

Two simple modifications have to be applied to static and dynamic current models, so as to be consistent with the oversampled configuration. First, the blocks operating the discrete-to-continuous time conversion (i.e. the Zero-Order Hold in the static model and the delta shaper in the dynamic ones) must be eliminated because of the presence of the N_{over} up-sampler in Fig. 3.11. Second, the gain N_{over}/T_S must be added to the dynamic path, for both mismatch-induced errors and switched capacitance effect, as highlighted in Fig. 3.11. This can be easily explained considering operation in the oversampled time-domain: as the differentiation of $d_i|_{diff}[k]$ generates pulses with an equivalent finite duration (T_S/N_{over}), to keep unchanged the injected dynamic charge we have to multiply pulses by the scaling factor N_{over}/T_S (obtaining in this way *current* pulses). Let us notice that this is not required on the static path, since

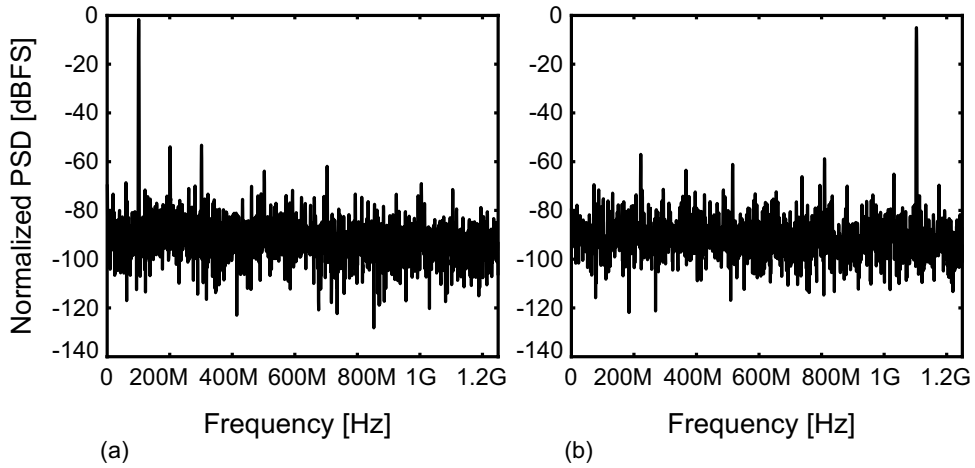

Figure 3.12 Output spectra obtained by Matlab simulations: (a) low-frequency input ($f_{\mathrm{IN}} = 100\,\mathrm{MHz}$) and (b) high-frequency input ($f_{\mathrm{IN}} = 1.1\,\mathrm{GHz}$).

it already calculates output current instead of charge.

Finally, the oversampled time-domain allows the output impedance model to be implemented by means of a first-order low-pass IIR filter, whose parameters are dependent on the digital input, as previously described. Designed using the bilinear transformation technique [36], the filter guarantees a faithful representation under the hypothesis that the oversampled frequency $N_{\mathrm{over}} f_{\mathrm{S}}$ is sufficiently higher than that of filter singularities, which is easily verified, in this case, with a proper choice of N_{over}.

3.6 Simulation results

The proposed discrete-time DAC behavioral model has been implemented and simulated in Matlab environment in order to demonstrate its effectiveness in describing real DAC linearity performances over the entire Nyquist bandwidth. To this purpose, we will refer to the behavioral model of the 10-bit 2.5 GS/s 28 nm CMOS DAC design we will present in Chapter 5. The DAC is realized according to a segmented configuration, in which a coarse thermometer-coded section with the 4 Most-Significant Bits (MSBs) is combined with a fine binary-coded section with the 6 Least-Significant Bits (LSBs). Model parameters (in terms of mean value and standard deviation of static and dynamic mismatches, unit cell switching resistance ΔR and capacitance ΔC) have been extracted by circuit simulations, while an oversampling factor $N_{\mathrm{over}} = 100$ has been used.

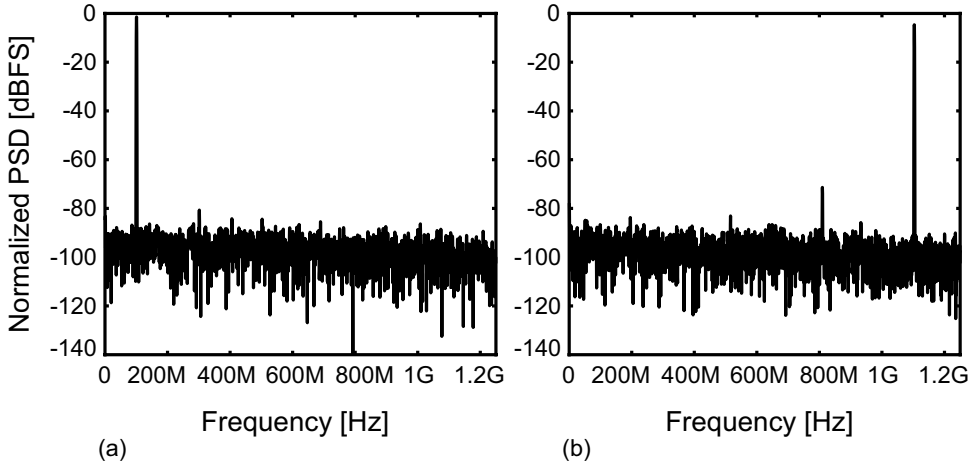

Figure 3.13 Output spectra obtained by Matlab simulations when only dynamic errors are accounted for: (a) low-frequency input ($f_{IN} = 100\,MHz$) and (b) high-frequency input ($f_{IN} = 1.1\,GHz$).

First of all, in order to get a measure of DAC linearity, the output spectrum in the case of a one-tone test has been simulated in Matlab. As an example, Fig. 3.12(a) and (b) show the normalized Power Spectral Density (PSD) of DAC output with a full-scale 100 MHz and 1.1 GHz sinusoid signal at the input, respectively.[2] The SFDR is approximately constant in both cases. It goes from 52 dB for $f_{IN} = 100\,MHz$ to 51 dB for $f_{IN} = 1.1\,GHz$, suggesting that distortion is dominated in this design by static effects, which are independent on frequency. When mismatch-induced static errors are disabled, the output spectra become as depicted in Fig. 3.13(a) and (b). The limitation posed by the only dynamic errors allows the SFDR to increase up to 78 dB and 66 dB at 100 MHz and 1.1 GHz, respectively, revealing that a technique able to cancel out only static non-linearity would be effective even in improving high-frequency performances. This is the fundamental motivation underlying the digital linearization technique we will propose in the next chapter.

In order to verify the accuracy of the proposed DAC model, a comparison with circuit simulations is needed. Fig. 3.14 shows the SFDR (as a function of input frequency f_{IN}) obtained by Matlab simulations (black plot), compared with that one resulting from circuit simulations (gray plot). The error of Matlab model remains below just 3 dB and it has to be attributed to the unavoidable differences between extractions of random mismatches in the two

[2] As it will be discussed further in details in Chapter 5, the full-scale DAC output swing is approximately 500 mV ($V_{lsb} = 500\,\mu V$), with power supply $V_{DD} = 1\,V$.

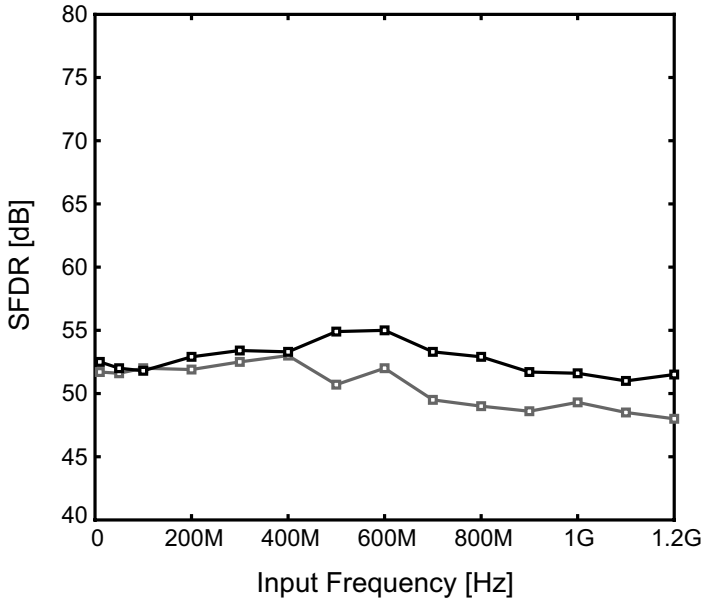

Figure 3.14 SFDR vs. input frequency: comparison between Matlab simulations (black plot) and circuit simulations (gray plot).

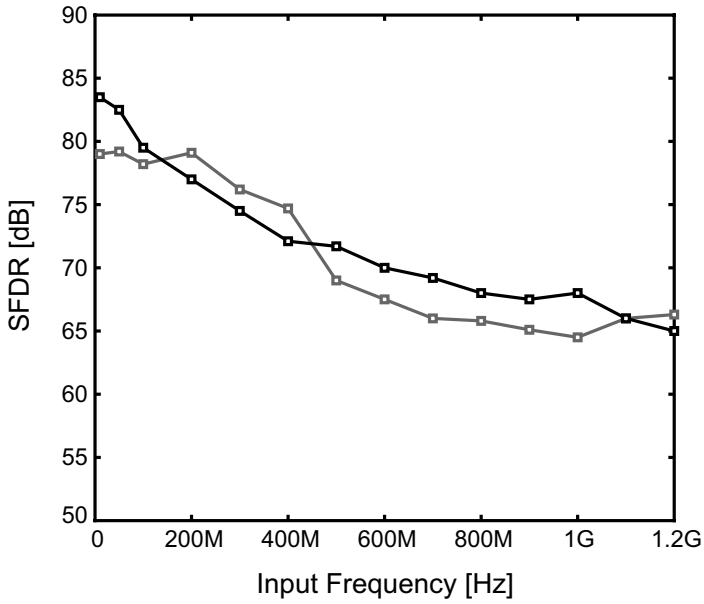

Figure 3.15 SFDR vs. input frequency when only dynamic errors are accounted for: comparison between Matlab simulations (black plot) and circuit simulations (gray plot).

simulations, confirming the reliability of the proposed modeling approach. This is further verified in Fig. 3.15, where the same comparison is shown in the case of only dynamic non-linearity errors accounted for. The SFDR trend follows the $1/f$ degradation we found out in Chapter 2 confirming, at the same time, the Matlab model accuracy once again (except for very low frequencies, where the error is about 5 dB).

Chapter 4

Digital Adaptive Cancellation of Static Non-linearity

Contents

4.1 Motivation

We have seen so far that high-speed current-steering DACs performances are substantially limited by two fundamental trade-offs. While the first one between static (low-frequency) and dynamic (high-frequency) linearity is related

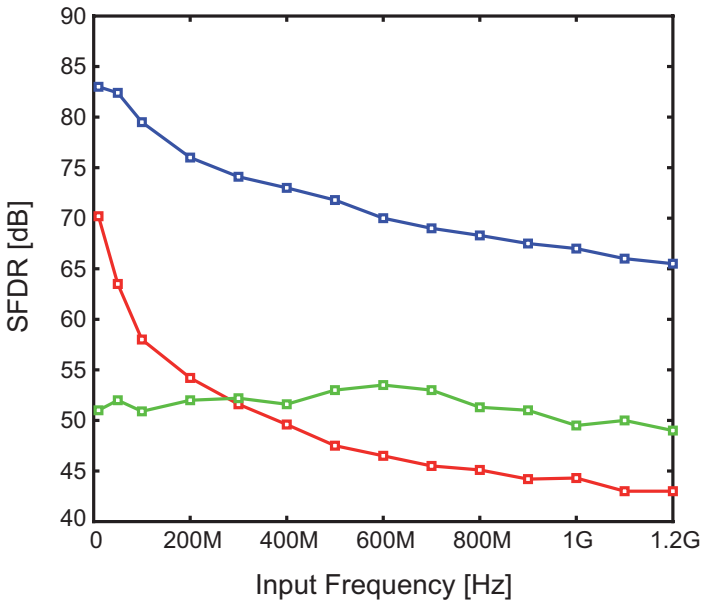

Figure 4.1 SFDR vs. input frequency resulting from Matlab behavioral simulations. Comparison between an high-accuracy DAC (red plot), a low-accuracy DAC (green plot) and a low-accuracy DAC with static non-linearity errors disabled (blue plot).

to the switching capacitance ΔC of the unit current cell, the second one between high-frequency linearity and power efficiency requires the minimization of the supply voltage V_{DD}.

This is well described by the DAC behavioral model we introduced in Chapter 3. As an example, Fig. 4.1 shows the DAC SFDR as a function of input frequency resulting from Matlab simulations for three different alternatives. All of them make use of a non-cascoded current cell so as to meet the low supply voltage requirement for power efficiency.

First of all, a DAC designed for high static accuracy has been simulated (red plot), which achieves an SFDR of about 70 dB at DC. Unfortunately, the large current source area used for static matching ($\sigma(\Delta I/I) = 1\%$) also implicates a large switching capacitance producing a fast degradation of spectral performances (SFDR below 45 dB for $f_{\mathrm{IN}} > 900$ MHz). On the contrary, a low-accuracy DAC (green plot in Fig. 4.1) designed to achieve a poor matching between current sources ($\sigma(\Delta I/I) = 15\%$) can benefit from a smaller switching capacitance at high frequencies. The resulting SFDR $\simeq$ 50 dB is almost constant over the entire Nyquist bandwidth, suggesting that dynamic errors are pulled down below the static ones. It follows that if we were able to cancel,

in some way, the static non-linearity in a low-accuracy DAC, then we would get much better high-frequency performances. This is confirmed by the blue plot in Fig. 4.1, representing the SFDR obtained by the low-accuracy DAC when model static non-linearity errors are disabled. If compared to the high-accuracy DAC, this solution would achieve an improvement of the SFDR at 1.2 GHz greater than 20 dB.

This is the fundamental motivation at the basis of the digital adaptive linearization technique we will introduce in this chapter. The proposed method will be able to cancel DAC static non-linearity without sacrificing dynamic performances, even with the low supply voltage of scaled CMOS processes.

4.2 Introduction to digitally-assisted DACs

The continuous scaling of CMOS technologies has made available high-performance analog and digital functions integrated on the same chip at low cost. One of the many consequences of this trend is the extensive use of digital techniques to correct the effects of mismatches and other analog impairments, even when these vary with time. These techniques applied both to analog and to mixed analog-digital circuits often operate in the background of the system normal operation. Examples may be found in Phase-Locked Loops (PLLs) [37]–[40], Analog-to-Digital Converters (ADCs) [41]–[44] and Digital-to-Analog Converters (DACs) [45]–[47]. In this context, digital adaptive filters based on the least-mean-square (LMS) algorithm can estimate and cancel out the effects of the non-idealities affecting circuit performance, directly in the digital domain. Their intrinsic capability of tracking the environmental variations in an adaptive fashion makes these systems very interesting for background error correction. The use of adaptive filters in the area of digital communications is well established since the sixties [48], [49]. However, only in recent years they have been applied to improve the performance of mixed analog-digital integrated circuits.

Many methods have been developed for the digital assistance of DACs with the purpose of improving their linearity. For instance, an all-digital correlation technique is proposed in [45], which mitigates the effect of component mismatches of a multi-bit DAC embedded in a pipelined ADC. In that scheme, the errors of DAC elements are estimated in the digital domain by exploiting the correlation of the digital input signal and the ADC output signal. A similar method has been applied to the DAC embedded in a MASH $\Delta\Sigma$ ADC [46].

Similarly, methods based on adaptive filtering have been applied to general-

purpose current-steering DACs [47], where an LMS calibration scheme compensates the mismatch of each current source. The error signal fed back by the LMS loop is the difference between the DAC input and output. Obviously, to perform this operation entirely in the digital domain, the output of the DAC must be converted back to the digital domain by a linear multi-bit ADC converter.

The need for an ancillary ADC clearly represents a major obstacle for the application of this approach to general-purpose DACs. In general, any calibration technique which corrects the DAC input on the basis of its analog output needs an ADC, which samples and digitizes the analog output with the necessary accuracy and linearity. Unless the DAC itself is embedded in an ADC, in which case the digitized output is already available [45], [46], this represents a serious obstacle that may drive the design process into a vicious circle. In [47], this issue has been faced by feeding the DAC output to a slow-rate ADC, which can achieve the required linearity with limited power consumption. A similar approach was adopted for the digital predistortion of the DAC input in [50].

Unfortunately, component mismatch is not the only source of static nonlinearity in DACs, even at low frequencies. In a DAC realized with ideally-matched elements, distortion would arise from other sources usually degrading the integral nonlinearity (INL) [4]. For instance, in a more general case than the current-steering one we analyzed in previous chapters, when either a buffer or an amplifier is cascaded to the DAC, this additional block adds compression at high signal levels. For this reason, in the embedded DAC in [43], two different correction techniques have been combined to counteract separately element mismatches [45] and amplifier distortion [51].

In this chapter, an original LMS-based digital scheme is proposed which linearizes the DAC static characteristic, independently on the source of nonlinearity. Fundamental concepts at the basis of this new approach have been published at an IEEE conference [52]. As it will be clear in the following, the proposed linearization technique consists in a *multipath* LMS adaptive filter that allows overcoming the trade-off between low-frequency and high-frequency linearity in high-speed DACs without sacrificing power efficiency. The scheme is based on a simple analog comparator and an ancillary slow-rate, yet linear, DAC, while it requires no linear ADC. This feature reduces the overall power dissipation, eliminates the linearity issues associated to the design of a multi-bit ADC and enables the sign-error version of the LMS algorithm which drastically simplifies digital design. Furthermore, in contrast to previously pro-

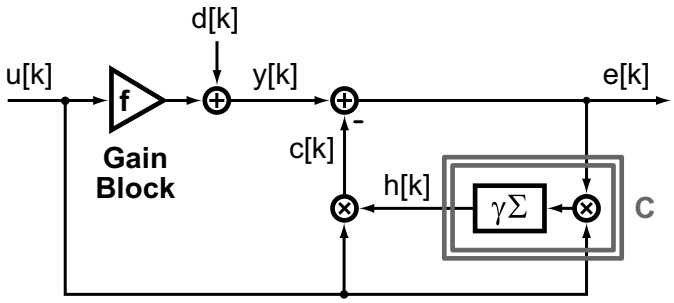

Figure 4.2 LMS-based adaptive filter which estimates the gain f.

posed techniques for general-purpose DACs, this method corrects not only for *mismatch-induced nonlinearity* but also for other sources of distortion of the static characteristic (a.k.a. *harmonic distortion* [51]).

In this chapter, after briefly recalling basic concepts on LMS algorithm, we will focus on the new multipath configuration for the estimation of DAC static non-linearity. Then, the overall linearization technique is introduced and practical aspects of its application to high-speed current-steering DACs are discussed in detail. Finally, behavioral simulation results confirming the effectiveness of the proposed approach are shown.

4.3 Automatic estimation of a linear gain

Before introducing the new multipath filter for the estimation of the DAC characteristic, it is useful to recall the basic properties of adaptive filters and their ability to estimate adaptively the gain of a generic block.

Adaptive filters have been introduced in digital signal processing in order to cancel out an undesired disturbance $u[k]$, superimposed to a desired signal $d[k]$ [48], [49]. As shown in the block diagram in Fig. 4.2, $u[k]$ passing through a block with unknown gain f is added to $d[k]$. Thus, the block output $y[k]$ is given by the sum of these two contributions: $y[k] = f \cdot u[k] + d[k]$. If the sequence $u[k]$ is known in some way, it can be cancelled out at the output by feeding it to a second stage with gain h, which perfectly replicates the gain f. Unfortunately, the coefficient f is unknown and may be time-variant. Therefore, to get accurate cancellation of $u[k]$, h must be adaptively adjusted at each time step k.

The most common updating algorithm for the h gain is based on the Widrow-Hoff recursive equation, which is an implementation of the steepest-

descent method using an estimated gradient [53]:

$$h[k] = h[k-1] + \gamma e[k-1]u[k-1]\,. \tag{4.1}$$

This is the so-called Least Mean Square (LMS) algorithm and it is implemented by the block C in Fig. 4.2. The estimation of f is performed by multiplication of the undesired but known sequence $u[k]$ by $h[k]$. Substituting the expression of the error $e[k] = d[k] + u[k] \cdot (f - h[k])$ into (4.1), we obtain that:

$$\begin{aligned} h[k] = \quad & h[k-1] - \gamma(u[k-1])^2(h[k-1] - f) + \\ & + \gamma d[k-1]u[k-1] \end{aligned} \tag{4.2}$$

The LMS algorithm estimates properly the gain f, that is the mean of $h[k]$ in the sample space $\mathrm{E}\{h[k]\}$ tends to the desired coefficient f, under the following three conditions:

1. $\mathrm{E}\{h[k]\} \simeq \mathrm{E}\{h[k-1]\}$ at the steady-state condition;
2. $\mathrm{E}\{u[k-1]^2(h[k-1] - f)\} \simeq \overline{u^2} \cdot \mathrm{E}\{h[k-1] - f\}$, where $\overline{u^2}$ is the mean square value of $u[k]$. This is verified in the practical case of small γ, i.e. in the case of slow transient of the filter coefficient $h[k]$ with respect to the undesired sequence $u[k]$;
3. $\mathrm{E}\{d[k-1]u[k-1]\} \simeq 0$, i.e. the desired and undesired signals are uncorrelated.

Calculating the expectation of both sides of (4.2) and imposing those three hypotheses, we get $\mathrm{E}\{h[k]\} \to f$.

4.3.1 Stability range and convergence speed

To study the convergence behavior of the algorithm, it is useful to define the error $g[k]$ as the difference between the estimated and target values of the coefficient at the k-th sample: $g[k] = h[k] - f$. Subtracting f from both sides of (4.2), it results that:

$$g[k] = (1 - \gamma u[k-1]^2)g[k-1] + \gamma d[k-1]u[k-1]\,. \tag{4.3}$$

From the previous assumptions, the expected value of the error $g[k]$ is given by:

$$\mathrm{E}\{g[k]\} = (1 - \gamma \cdot \overline{u^2}) \cdot \mathrm{E}\{g[k-1]\} \tag{4.4}$$

that converges to zero, i.e. the estimated gain converges to f, if $\left|1-\gamma\cdot\overline{u^2}\right|<1$. It follows that the range of values of the update parameter that ensures the algorithm stability is:

$$0<\gamma<\frac{2}{\overline{u^2}}\,. \tag{4.5}$$

If γ lies within this stability range, the solution of (4.4) is:

$$\mathrm{E}\{g[k]\}=g_0\cdot\left(1-\gamma\cdot\overline{u^2}\right)^k \tag{4.6}$$

where the starting point $g_0=g[0]$ is assumed to be a deterministic variable. It is straightforward to note that if $\gamma\cdot\overline{u^2}\ll 1$, (4.4) can be described equivalently in the continuous-time domain and the convergence time constant is given by:

$$\tau\simeq\frac{T_\mathrm{S}}{\gamma\cdot\overline{u^2}} \tag{4.7}$$

where T_S is the sampling period. Thus, the higher the adaptation parameter γ, the faster the algorithm convergence.

4.3.2 Accuracy of estimated gain

Unfortunately, increasing γ, even though advantageous for the convergence speed, produces larger fluctuations of the error $g[k]$ around zero, or equivalently, larger fluctuations of the estimated gain $h[k]$ around the target f. The inaccuracy of the algorithm is induced by the presence of the second term in the r.h.s. of (4.3), which prevents $h[k]$ to reach exactly the desired value. Thus, the higher are both γ and the mean square value of $d[k]$, the higher will be the mean square value of the error $g[k]$.

An approximated expression of $\overline{g^2}$ can be achieved by calculating the mean squared value of the two sides of (4.3). Assuming that $\gamma\cdot\overline{u^2}\ll 1$ and that the two terms of the r.h.s. of (4.3) are uncorrelated, after some simplification, we obtain that:

$$\overline{g^2}\simeq\frac{1}{2}\gamma\overline{d^2}\,. \tag{4.8}$$

As expected, a larger γ causes a larger dispersion of the estimated gain around f. In turn, the fluctuation of $g[k]$ produces additional noise at the output. To measure the adaptive-process performance, we can define the *misadjustment*

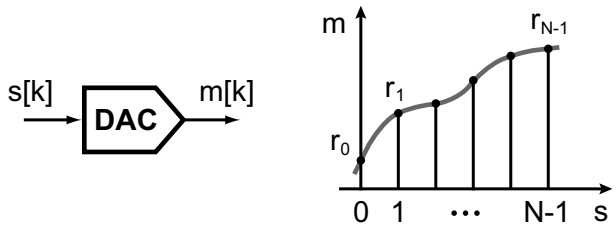

Figure 4.3 N-level DAC non-linear characteristic.

[53] as the power ratio of this extra noise to the desired signal:

$$\frac{\mathrm{E}[g[k]^2 u[k]^2]}{\overline{d^2}} \simeq \frac{\overline{g^2} \cdot \overline{u^2}}{\overline{d^2}}\,, \tag{4.9}$$

where the simplification holds for small γ values, that is, when the transients of the gain error $g[k]$ are much slower than the variations of the unwanted sequence $u[k]$.

Substituting (4.8) into (4.9) and then exploiting (4.7), we obtain an insightful expression of the misadjustment factor:

$$\frac{\mathrm{E}[g[k]^2 u[k]^2]}{\overline{d^2}} \simeq \frac{\frac{1}{2}\gamma\overline{d^2} \cdot \overline{u^2}}{\overline{d^2}} = \frac{1}{2}\gamma\overline{u^2} = \frac{T_s}{2\tau}\,, \tag{4.10}$$

which evidences that the noise induced by the algorithm is inversely proportional to the number of cycles required for convergence. This sort of speed/accuracy trade-off is typical of LMS adaptive filters.

4.4 Adaptive estimation of DAC non-linear characteristic

The idea of the automatic estimation of the gain of a linear block can be extended to the case of a non-linear transfer characteristic of a DAC. To this purpose, we will proceed by steps. First, we will limit our analysis to the case of a DAC described only by its static characteristic, neglecting all the dynamic effects. Then, dynamic non-linearity errors will be accounted for starting from section 4.6.

On the basis of this assumption, a generic DAC static characteristic can be depicted as in Fig. 4.3. In this representation, $s[k]$ stands for the equivalent digital input integer value and hence it has to be intended as an N-level

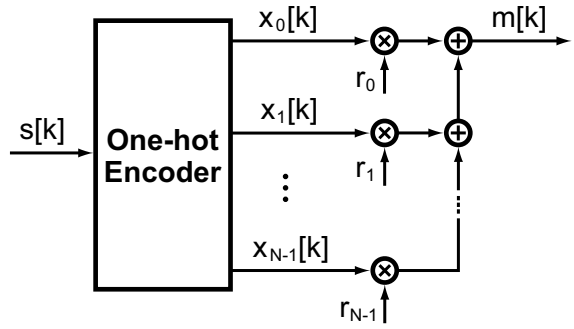

Figure 4.4 Equivalent model of the DAC non-linear static characteristic.

quantized signal. Depending on the value of $s[k]$, the output $m[k]$ will assume one of the N values in the set $\{r_0, r_1, ..., r_{N-1}\}$. The output sequence $m[k]$ is therefore

$$m[k] = r_i|_{i=s[k]} = f(s) \cdot s[k] \tag{4.11}$$

where $f(s)$ is a gain similarly to the f gain used in the linear case, but this time it is dependent on $s[k]$. The latter expression highlights that a single gain h cannot match the whole DAC characteristic as in the plain case, because of its gain dependency on input. Instead, N different values, that is one for each input level, need to be estimated.

To this purpose, the output sequence $m[k]$ in Eq. (4.11) can be conveniently rewritten as a scalar product between two vectors

$$m[k] = \mathbf{x}[k] \cdot \mathbf{r}^T . \tag{4.12}$$

where $\mathbf{r} = [r_0, r_1, \ldots, r_{N-1}]$ is the vector of the output values and $\mathbf{x}[k] = [x_0[k], x_1[k], \ldots, x_{N-1}[k]]$ is the selection vector whose elements $x_i[k]$ are defined as

$$x_i[k] = \begin{cases} 1 & \text{if } i = s[k] \\ 0 & \text{if } i \neq s[k] \end{cases} \tag{4.13}$$

for $i = 0, \ldots, N-1$. By definition, for every k, $\mathbf{x}[k]$ is a vector of all elements equal to zero except one whose position depends on the input $s[k]$. This definition of the selection vector $\mathbf{x}[k]$ is typically referred to as *one-hot* encoding.

On the basis of Eq. (4.12), we can model the DAC non-linear characteristic

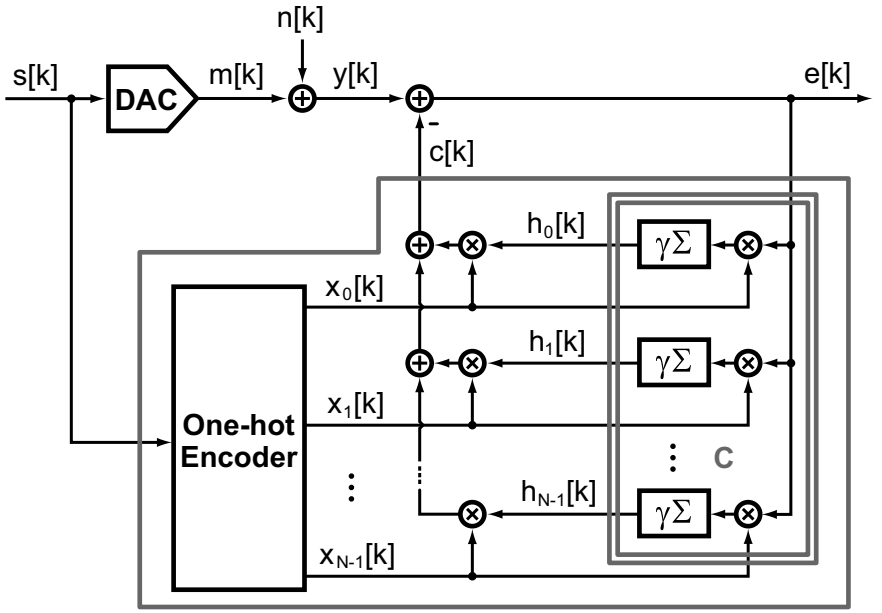

Figure 4.5 Implementation of the *multipath* LMS adaptive filter.

as the M-path filter in Fig. 4.4 fed by the selection vector $\mathbf{x}[k]$. The one-hot encoder performs the transformation from $s[k]$ to $\mathbf{x}[k]$. In this way, the DAC non-linear characteristic has been expressed as the sum of N linear gains.

Let us assume that a known $s[k]$ signal is fed to the system in Fig. 4.4 and let us refer to the i-th branch of the N-path filter. The sequence $x_i[k]$ is also known on the basis of $s[k]$. Thus, it can be canceled out at the DAC output by means of the LMS estimation of the single linear gain r_i, as we did in the previous section for a gain block. More in general, this is valid for each of the N branches of the filter in Fig. 4.4: since the whole selection vector $\mathbf{x}[k]$ is known on the basis of $s[k]$, the output sequence $m[k]$ can be completely canceled out by the estimation of the whole vector $\mathbf{r}$.

This estimation is achieved by feeding $\mathbf{x}[k]$ to a second N-path filter with the same topology of the one shown in Fig. 4.4, but with adaptive gains. The resulting scheme is shown in Fig. 4.5. The cancellation of $s[k]$ at the output of the DAC is then obtained by subtracting the output of this *multipath* adaptive filter from the DAC output. Instead, the signal $n[k]$ representing a sequence uncorrelated with the input $s[k]$ (for instance, the DAC output noise) is not cancelled. From this standpoint, the system in Fig. 4.5 is analogous to the adaptive filter for the estimation of a linear gain in Fig. 4.2 (where the signals $u[k]$ and $d[k]$ play the same role of $s[k]$ and $n[k]$ in Fig. 4.5). The expected

value of the vector of the estimated gains $\mathbf{h}$ converges to $\mathbf{r}$:

$$\mathrm{E}\{[h_0, h_1, \ldots, h_{M-1}]\} \rightarrow [r_0, r_1, \ldots, r_{M-1}]\,, \tag{4.14}$$

under the same hypotheses formulated in the previous section (i.e., $n[k]$ uncorrelated to the N sequences $x_i[k]$, and $h_i[k]$ slower than $x_i[k]$).

The one-hot encoding of $\mathbf{x}[k]$ guarantees that just one of the N adaptive filters in parallel is active at the k-th sample. Hence, only one output will be effectively subtracted from $y[k]$ at a time and the branches do not interfere each other. On the basis of this consideration, we can apply the theory discussed in the previous section for the estimation of a linear gain and the same fundamental results about convergence speed and accuracy of the estimated gains hold even for the multipath configuration. Assuming for instance the DAC input $s[k]$ uniformly distributed between 0 and $N-1$, each filter is exerted on average one time out of N. Thus, every sequence $x_i[k]$ has a mean square value $\overline{x^2} = 1/N$ and each of the N adaptive filters has a time constant given by Eq. (4.7), where $\overline{x^2}$ replaces $\overline{u^2}$:

$$\tau \simeq N \cdot \frac{T_\mathrm{S}}{\gamma}\,. \tag{4.15}$$

This result is consistent with intuition: since N coefficients need to be estimated and just one of the N filters is exerted at a time, the convergence time increases linearly as N. Regarding the accuracy of the N estimated gains, the expression of the mean square value of the error follows from (4.8)

$$\overline{(h_i - r_i)^2} \simeq \frac{1}{2}\gamma\overline{n^2}\,. \tag{4.16}$$

Finally, let us note that the digital hardware complexity required to implement the multipath adaptive filter is moderate and it increases linearly as N. Since the N sequences $x_i[k]$ are one-bit signals, all the multipliers in Fig. 4.5 will be realized as simple digital multiplexers. Thus, just accumulators and adders are required.

4.5 Adaptive linearization of DAC characteristic

The algorithm for the estimation of the DAC non-linear characteristic introduced in the previous section can be slightly modified in order to cancel the errors arising from nonlinearity and to get a linear conversion characteristic

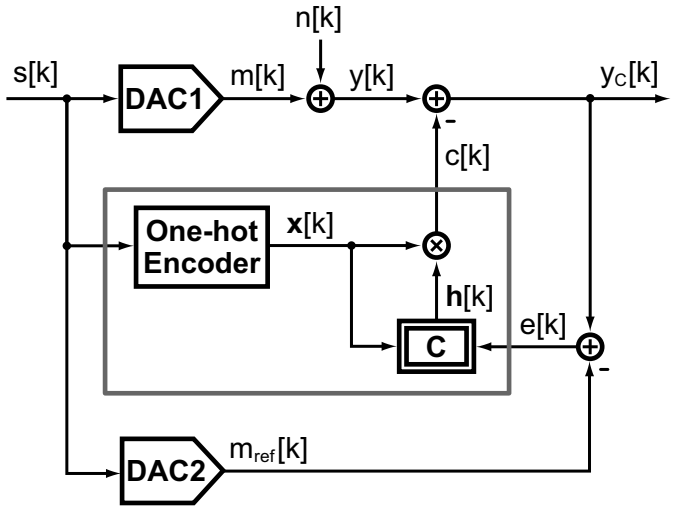

Figure 4.6 Concept of multipath adaptive filter for DAC linearization.

independently on the origin of the static errors.

4.5.1 Concept of adaptive DAC linearization

The system in Fig. 4.5 can be modified to estimate the only non-linearity errors in place of the whole DAC characteristic. This result is obtained by two steps: (i) introducing an ancillary DAC (denoted as DAC2), with high linearity, driven by the same input sequence $s[k]$ as the DAC to be linearized (denoted hereinafter as DAC1); (ii) feeding the same multipath LMS adaptive filter introduced in the previous section with an error signal $e[k]$, given by the difference between the corrected output of DAC1 and the output of DAC2, i.e.

$$e[k] = y_{\mathrm{C}}[k] - m_{\mathrm{ref}}[k] \tag{4.17}$$

The resulting system is drawn in Fig. 4.6. The adaptive filter (inside the gray line) is drawn in a compact form, relying on the definition of $\mathbf{x}[k]$ and the vector of the estimated coefficients $\mathbf{h}[k] = [h_0[k], h_1[k], \ldots, h_{N-1}[k]]$. As we demonstrated in the previous section, the adaptive filter tends to cancel on average the error signal $e[k]$. Thus:

$$\mathrm{E}\{y_{\mathrm{C}}[k]\} \to m_{\mathrm{ref}}[k]\,, \tag{4.18}$$

which means that the whole system tends to make DAC1 as linear as DAC2, as desired.

The corrected output of the system in Fig. 4.6 can be written as $y_C[k] = m[k] + n[k] - c[k]$, where $c[k]$ is the correction sequence provided by the LMS filter and $n[k]$ an uncorrelated sequence representing for instance DAC1 random noise. Hence the expected value of $c[k]$ tends to:

$$\mathrm{E}\{c[k]\} \rightarrow m[k] - m_{\mathrm{ref}}[k]\,, \tag{4.19}$$

which is simply the difference between the outputs of DAC1 and DAC2. If we now denote as $\mathbf{l} = [l_0, l_1, \ldots, l_{N-1}]$ the vector representing the characteristic of DAC2 (similarly to what we did for DAC1), (4.19) allows us to conclude that

$$\begin{aligned}\mathrm{E}\{\,[h_0[k], h_1[k], \ldots, h_{N-1}[k]]\,\} \rightarrow &[r_0, r_1, \ldots, r_{N-1}] + \\ &- [l_0, l_1, \ldots, l_{N-1}]\,.\end{aligned} \tag{4.20}$$

In practice, the vector of the correction coefficients tends on average to the difference between the characteristics of DAC1 and DAC2. Thus, if DAC2 is much more linear than DAC1, the vector $\mathbf{h}[k]$ of the LMS filter estimates the departure of DAC1 characteristic from an ideally-linear one.

The block diagram in Figure 4.6 shows the concept of the proposed adaptive linearization technique. To make this solution effective in improving DAC nonlinearity and to implement the proposed LMS filter entirely in the digital domain, three major issues must still be faced: (i) if $c[k]$ is a digital signal, a third DAC is necessary at the output of the adaptive filter itself to allow the subtraction of $c[k]$ from $m[k]$ in the analog domain; (ii) an ADC is needed to convert the analog error $e[k]$ into the digital domain. Both the third DAC and the ADC would complicate unacceptably the system. (iii) A practical method to design DAC2 with much better linearity than DAC1 must be illustrated. In the following, we will describe step by step how we can modify the proposed system to remove all those practical impairments.

4.5.2 Implementation in digital domain

Instead of introducing a third DAC to convert $c[k]$, we can rely on the assumption that the nonlinearity of DAC1 is mainly determined by its most-significant bits (MSBs), while its least-significant bits (LSBs) are less influential in terms of both element mismatch and harmonic distortion [14]. Thus, the adaptive linearization can be applied to the MSBs only of DAC1 and its LSBs can be used to correct the MSBs. Obviously, the LSBs need to account for the additional dynamic range to perform the correction.

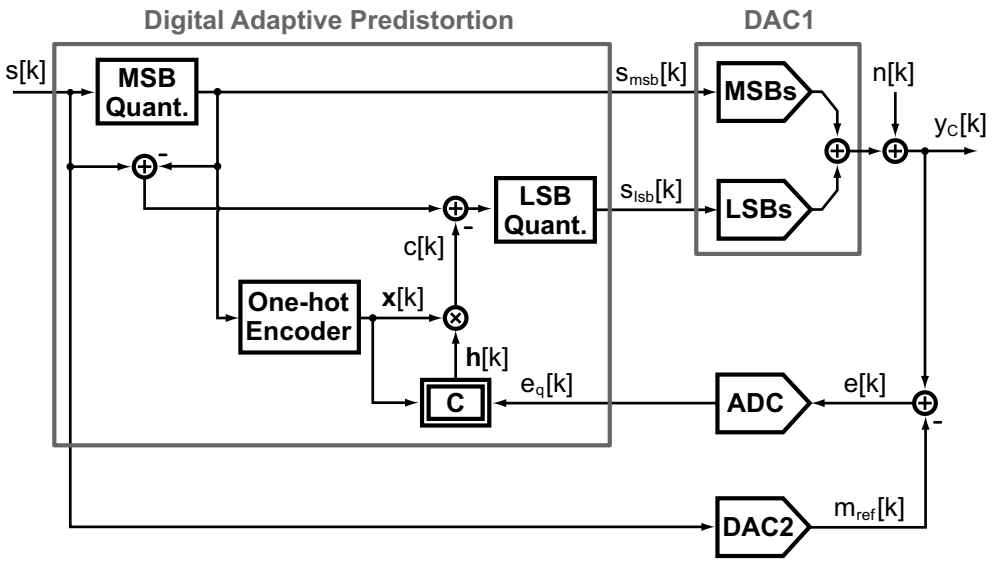

Figure 4.7 Implementation of the adaptive DAC linearization in the digital domain.

In practice, DAC1 can be implemented as a *digitally*-segmented DAC with a coarse section and a fine section, where the latter has a dynamic range larger than the LSB of the former. This solution not only avoids the use of an additional DAC for the correction, but has also the additional advantage of reducing the hardware required by the multipath adaptive filter. In fact, the latter depends linearly on the number of DAC levels to be corrected, thus exponentially on the DAC resolution.[1]

The resulting correction scheme with the digitally-segmented DAC is shown in Fig. 4.7. The adaptive linearization of the MSB section of DAC1 is obtained by feeding the MSB's of the input code $s_{\mathrm{msb}}[k]$ to the LMS multipath filter, and subtracting the correction term $c[k]$ directly from the quantization error of the MSB quantizer, which is then fed to the LSB quantizer. The dynamic range of the fine section of DAC1 must be extended to include the maximum nonlinearity error of the coarse section.

From a different point of view, the architecture in Fig. 4.7 can be regarded as a digital predistortion scheme that performs an adaptive compensation of the non-linear transfer characteristic of the DAC. The same method without modifications can be applied to binary-coded, thermometer-coded or segmented

[1] The sub-radix-2 DAC architecture adopted in [54], in which each DAC element is nominally less in value than the sum of the lower elements, may be used alternatively in DAC1 to accommodate the correction signal.

DACs. In contrast to other linearization techniques [45]–[47], which aim at correcting just the DAC element mismatches, the proposed technique linearize the DAC, regardless of the source of non-linearity. This is achieved by exploiting the correlation existing between the error $e[k]$ and the selection vector $\mathbf{x}[k]$, that picks out a specific level of the DAC characteristic at every k.

4.5.3 Elimination of multi-bit ADC

In the scheme in Fig. 4.7, a multibit ADC is added to convert the error signal back to the digital domain. However, in a practical implementation, a linear ADC would result critical for design and power consumption.

The simplest and most efficient solution consists in employing a simple comparator (or single-bit ADC) rather than a multibit ADC. The LMS algorithm in the multipath adaptive filter would be in this case based on the sign of the error signal. This algorithm which is commonly referred to as *sign-error* LMS [49] has been successfully employed in the context of fractional-N PLLs to cancel fractional spurs [55]. Although the sign-error LMS algorithm trades simplicity and efficiency of hardware with convergence speed, this is not a limiting factor in the case of our interest, as it will be clearer in section 4.7.

4.5.4 Realization of reference DAC

The last practical issue to be faced is the realization of the linear DAC2 for the determination of the nonlinearity errors of DAC1. However, DAC2 can be made much more linear than DAC1, only if DAC2 operates at much slower rate than DAC1. A trade-off between linearity and speed always exists in DAC design. Thus, the lower rate allows the improvement of DAC2 linearity. If N_{down} stands for the down-sampling factor, i.e. the ratio between the sampling frequencies of DAC1 and DAC2, the error $e[k]$ can be detected only one out of N_{down} samples. So, it follows that the update rate of the multipath LMS adaptive filter described above will be operated at slower rate $f_{\text{S}}/N_{\text{down}}$, being $f_{\text{S}} = 1/T_{\text{S}}$.

The final architecture of the digital linearization scheme is shown in Fig. 4.8, in which the combination of a comparator and a slow accurate DAC (DAC2) eliminates the problems of linearity and power consumption of a multibit ADC. A digital subsampler reduces the data rate of DAC2 input. The DAC1 output subsampling is performed by means of a sample-and-hold circuit operating at $f_{\text{S}}/N_{\text{down}}$. This solution allows a low-speed comparator, but, on the other hand, it may add a contribution to harmonic distortion which is not corrected

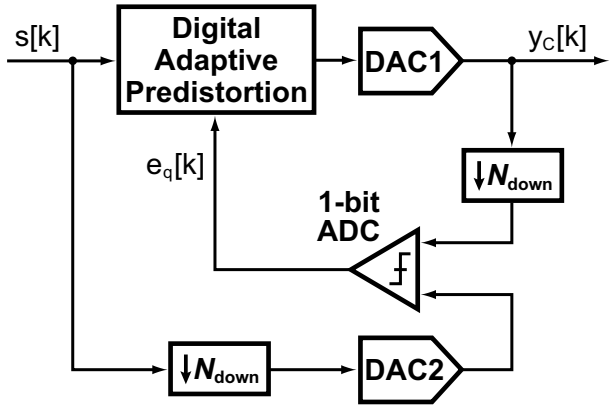

Figure 4.8 Final architecture of the adaptive linearization scheme.

by the proposed algorithm. Anyway, as we will see in the next chapter this source of non-linearity can be sufficiently reduced by a proper design. Finally, a digital upsampler is present inside the digital predistortion block to apply the correction sequence $c[k]$ at the full rate of DAC1.

4.6 Practical linearization of current-steering DACs

As a first step, we have introduced so far the new adaptive linearization technique taking into account, for simplicity, a DAC described only by its static characteristic. In other words, referring to the DAC behavioral model introduced in Chapter 3, we have focused our analysis on static non-linearity only, neglecting the effects due to dynamic current and output impedance submodels.

However, in order to apply the proposed LMS multipath adaptive filter to the practical case of current-steering DACs, dynamic non-linearity errors must be inevitably considered. In particular, we will focus in the following on two essential aspects. First, an equalization technique must be developed in order to compensate the actual finite output bandwidth of DAC1. Second, the effects of current dynamic errors on the linearization of static characteristic must be verified, so as they do not prevent the correct convergence of the LMS algorithm.

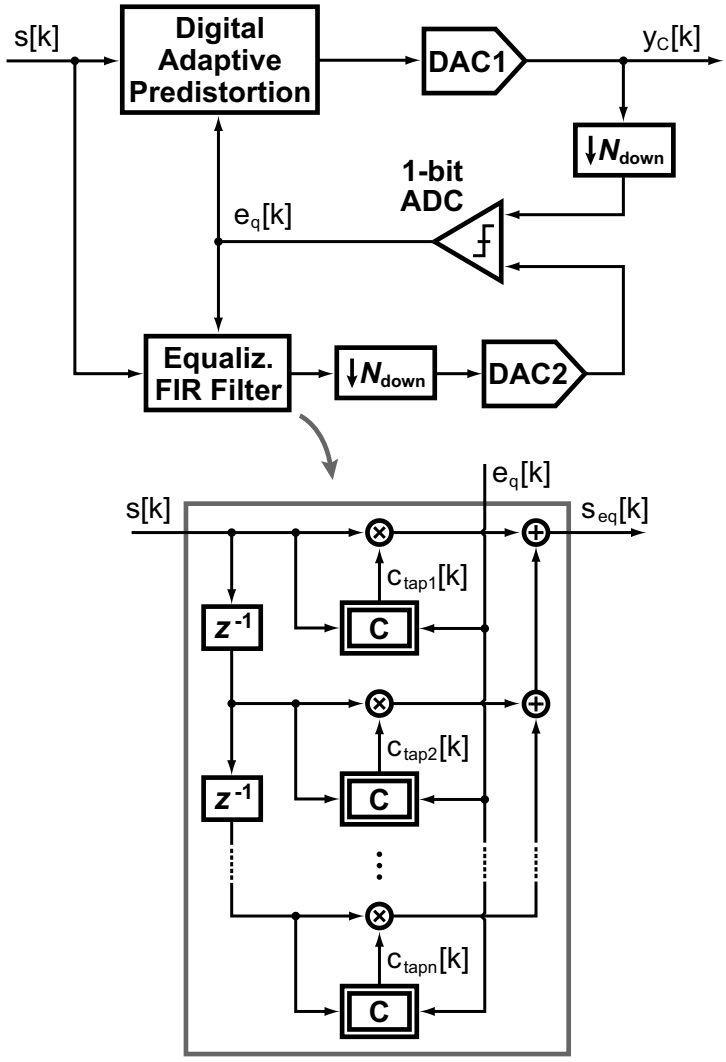

Figure 4.9 Implementation of the adaptive FIR equalization filter.

4.6.1 Equalization of DAC finite output bandwidth

In the algorithm description carried out in section 4.5 we have implicitly assumed that signal transients at the output of both DAC1 and DAC2 settle within a sampling period T_S. Only under this hypothesis, the comparator effectively detects the *static* non-linearity error of DAC1 with respect to DAC2. However, in practice, the finite bandwidth of DAC1 can prevent the output signal to reach its final value by the end of the sampling period T_S. This means that in the actual case the DAC output at the instant k will depend

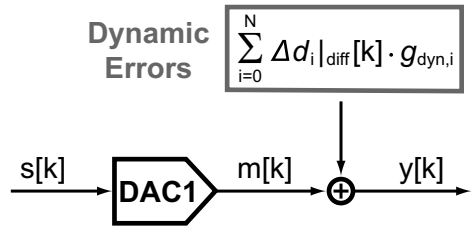

Figure 4.10 Modeling of dynamic errors components at DAC1 output.

not only on the present digital input sample, but even on some of the previous ones. Clearly, this memory effect due to the finite bandwidth of DAC1 output impedance can lead to a malfunctioning of the linearization algorithm.

To solve the problem, an equalization technique must be developed so as to compensate the output bandwidth impairment between DAC1 and DAC2. The simplest way consists in inserting an equalization FIR filter on the reference DAC2 path, so as to replicate the analog filter represented by DAC1 output impedance, but in the digital domain. The resulting scheme is depicted in Fig. 4.9. Since DAC1 output bandwidth depends on many uncontrollable factors (such as unit cells parasitic capacitances, variable external loads, etc.) the FIR taps coefficients can be adjusted in an adaptive way, as shown in details in the gray box of Fig. 4.9. The LMS algorithm exploits in this case the correlation between the different delayed versions of the digital input code and the quantized error signal $e_q[k]$. Obviously, the number of taps must be chosen according to the ratio between the sampling frequency f_S and the estimated bandwidth that has to be compensated.

Finally, let us underline once again that the aim of the proposed equalization filter is not the output impedance non-linearity cancellation (which can be easily achieved by proper sizing of transistors, as seen in Chapter 2), but only the compensation of DAC1 output bandwidth.

4.6.2 Effect of dynamic errors

In order to guarantee a proper functioning of the linearization of DAC static characteristic, we must ensure that dynamic non-linearity errors originating from current cells switchings (let us refer to the dynamic current model in Chapter 3) do not impact on convergence behavior of the LMS algorithm. To analyze the problem, we can simply proceed by intuition. Once the memory effect due to output impedance is compensated by the FIR equalization filter as described above, then we can consider the dynamic DAC output components as

uncorrelated with digital input code. In fact, dynamic non-linearity errors at a given instant k are related to the N differentiation signals $\Delta d_i|_{\text{diff}}[k]$ instead to the digital input level $s[k]$ (which in turn determines the selection vector $\mathbf{b}[\mathbf{k}]$). This is well explained in Fig. 4.10, where the sum of dynamic components can be seen as playing the same role of the uncorrelated noise $n[k]$ in Fig. 4.6. In other words, since dynamic errors are correlated to the time-derivative of input signals instead of the digital input level $s[k]$, the convergence of the LMS multipath adaptive filter is guaranteed.

Although it is not straightforward to get analytical evidence of the LMS convergence dynamics, simulation results confirm the validity of the proposed approach, as it will be shown in the next section.

4.7 Simulation results

The proposed algorithm is first validated relying on Matlab simulations. The digital linearization technique has been applied to the behavioral model of the 10-bit 2.5 GS/s 28 nm CMOS DAC whose design will be presented in Chapter 5. Its segmented architecture nominally consists of a coarse thermometer-coded section with the 4 MSBs (i.e. 15 x64 elements) and a fine binary-coded section with the 6 LSBs (x32, x16,...,x1 elements). However, in practice, the implementation of the proposed technique requires some modifications of fine section dynamic range as discussed in the following and shown in Fig. 4.11.

The estimation of the non-linearity characteristic of DAC1 coarse section (comprising random mismatch, harmonic distortion and offset) is performed by the multipath LMS adaptive filter as described above, with $N = 16$ paths. Therefore, in order to accommodate the generated correction sequence $c[k]$, the dynamic range of the fine section must be increased and must overlap the one of the coarse section. Instead of adding larger elements which would worsen non-linearity, extra elements with the same weight can be inserted into the DAC fine section. For instance, in the level corresponding to the x32 weight, three elements, instead of the nominal one, are used (let us refer to Fig. 4.11).

In order to achieve an extremely accurate linearization of static characteristic, the residual mismatch errors of the fine section are in turn corrected as in [47], that is exploiting the correlation between the error and the individual selection of each element. For the additional correction sequences $c_{\text{x32}}[k], c_{\text{x16}}[k], \ldots, c_{\text{x2}}[k]$ (one for every level except the last one) the same considerations already done for $c[k]$ still hold. Since each level correction sequence is added to the input of the successive (finer) level, the dynamic range of each

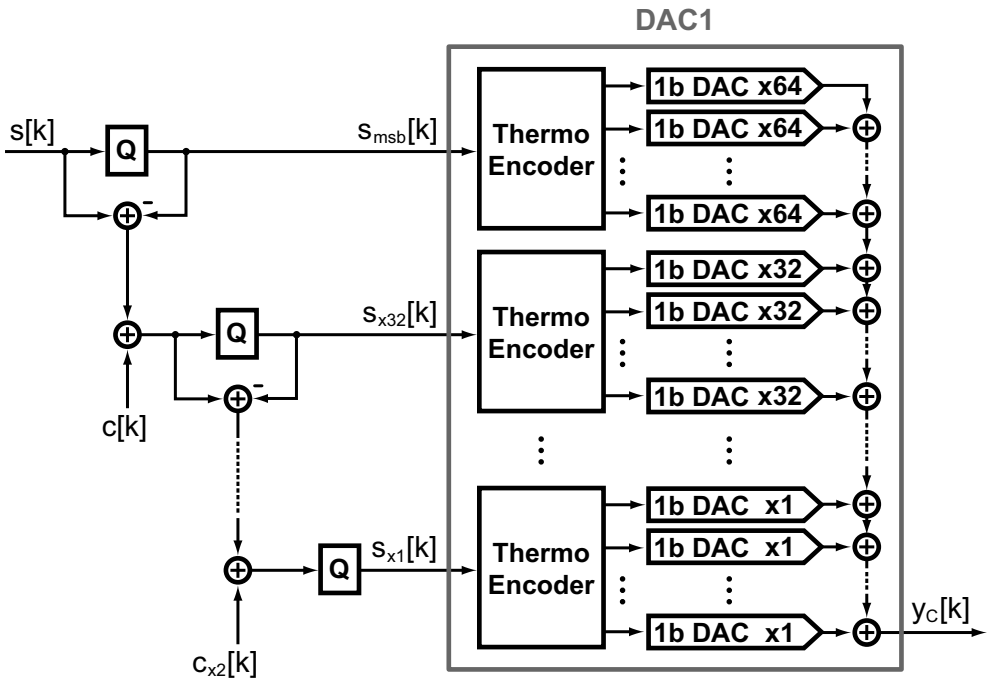

Figure 4.11 Complete architecture of DAC1.

level must be extended to include these errors. The designed DAC has an overall over-range of about 19% of the nominal 10-bit dynamic range.

In the behavioral model we built, DAC2, used as reference DAC, has the same resolution and Least-Significant Bit value ($V_{\text{lsb}} = 500\,\mu\text{V}$) as DAC1, but a sampling frequency $N_{\text{down}} = 100$ times lower. Its characteristic is assumed to be perfectly linear, in order to be able to focus only on performance limits of the proposed linearization technique. In addition, the equalization of DAC output bandwidths is performed by an adaptive 4-taps FIR filter, so as to be able to compensate bandwidth limitations (in a first-order approximation) down to 790 MHz.

Finally, we modeled the comparator offset (assuming a standard deviation of $10{\cdot}V_{\text{lsb}}$) and the output thermal noise. As we will see in Chapter 5, employing a sample-and-hold circuit with sampling capacitor $C_{\text{S}} = 10\,\text{fF}$, the resulting noise standard deviation at the comparator input is $\sigma_n \simeq 1.26 \cdot V_{\text{lsb}}$.

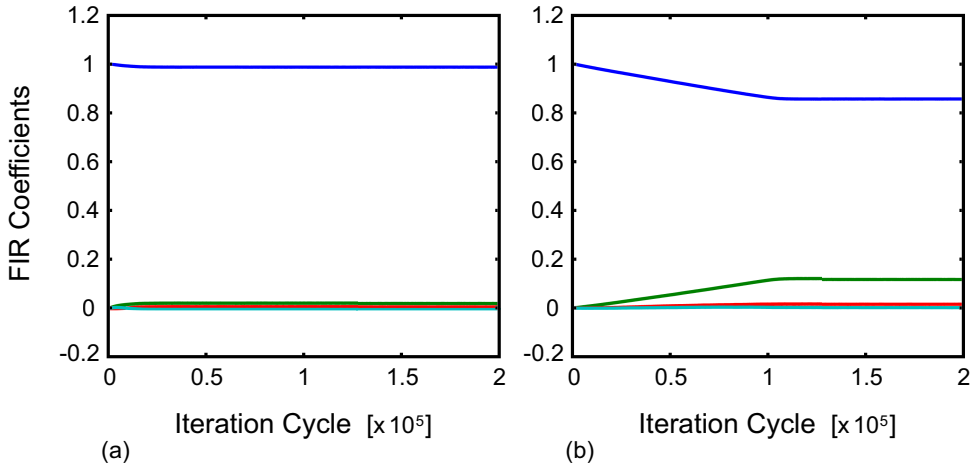

Figure 4.12 Convergence of equalization FIR filter in the case of large (a) and narrow (b) DAC output bandwidth.

4.7.1 Accuracy and convergence speed

First of all, we have seen that equalization of DAC1 and DAC2 output bandwidths is a necessary condition for a proper functioning of the adaptive linearization technique. Fig. 4.12 shows the convergence transients of the 4-taps FIR equalization filter coefficients. As expected, in the case of a large DAC1 output bandwidth [Fig. 4.12(a)], all signal transient settle by the end of a sampling period T_S and hence c_{tap1} converges to 1 while the other coefficients remain at zero. On the other hand, in the case of a narrower DAC1 bandwidth [Fig. 4.12(b)], taps coefficients correctly converge to different values because of the dependency on previous samples.

For what concerns the LMS multipath adaptive filter coefficients, we have already discussed the importance of the update parameter γ in setting their convergence time and accuracy. However, referring to the scheme in Fig. 4.7, in which we introduced additional blocks, we should note that the update parameter of the adaptive filter must be replaced by

$$\gamma' = \gamma \cdot g_{adc} \cdot g_{dac} \,, \tag{4.21}$$

where γ is the gain coefficient in the integrators inside the block C, g_{adc} the ADC gain and g_{dac} the gain of the fine section of DAC1 (denoted as LSBs in Fig. 4.7). All three blocks are in the LMS feedback loop. In these simulations, the update parameter γ' is set to 2^{-11}. This choice guarantees a fluctuation of

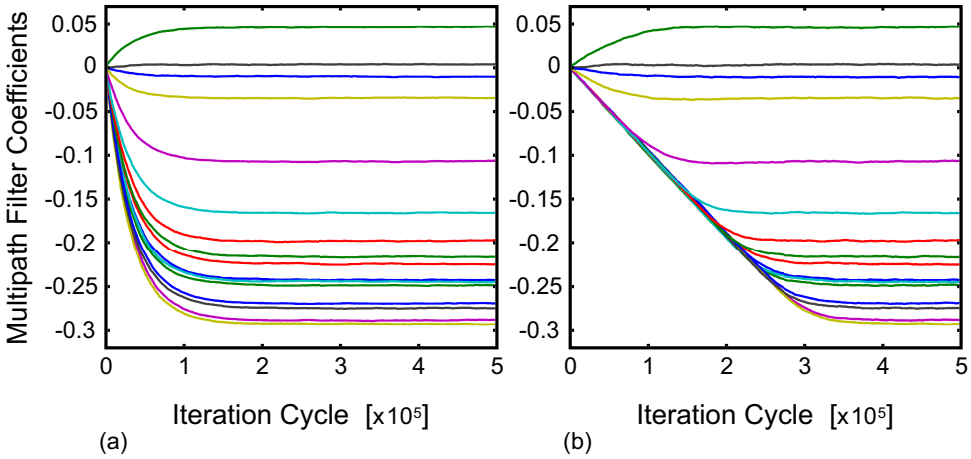

Figure 4.13 Convergence of multipath LMS adaptive filter coefficients: (a) standard LMS and (b) sign-error LMS.

the correction coefficients averaged over the 16 $\{h_i\}$ of about $0.31 \cdot 10^{-3}$, that corresponds to $0.02 \cdot V_{\text{lsb}}$ transferred at the output, and a negligible degradation of DAC1 dynamic range. In fact the standard deviation of the error between DAC1 and DAC2 is dominated by thermal noise $\sigma_e = 1.3 \cdot V_{\text{lsb}} \simeq \sigma_n$.

As a first test, the scheme employing the multibit ADC is simulated and the LMS algorithm relying on the multibit $e[k]$ signal is used. In this case, the 10-bit ADC gain is $g_{\text{adc}} = 1/(2^9 \cdot V_{\text{lsb}})$, assuming an ADC output range between -1 and $+1$. The gain of the fine section of DAC1 (correcting for the coarse section errors) is $g_{\text{dac}} = 2^6 \cdot V_{\text{lsb}}$. Thus, the gain γ of the integrators to employ in the 16 paths of the adaptive filters is found inverting Eq. (4.21): $\gamma = 2^{-8}$. The transients of the 16 coefficients $h_i[k]$, with $i = 0, \ldots, 15$, achieved from simulations are shown in Fig. 4.13(a). Focusing on the initial transients at start-up, the average time-constant is about $33 \cdot 10^3$ iteration cycles of DAC2 clock, which is very close to the result $(32.768 \cdot 10^3)$ given from Eq. (4.15) (in which γ is replaced by γ').

As a second test, we simulated the convergence in the case of the system in Fig. 4.8 with the sign-error LMS algorithm and the single-bit ADC, which is the practical implementation of the proposed method. Although the single-bit ADC having the characteristic of sign$(\cdot)$ function is highly nonlinear, it is possible to derive an equivalent linear gain under the presence of random noise around $e[k] = 0$. Assuming $e[k]$ a random Gaussian noise with variance σ_e^2, it is $g_{\text{adc}} \simeq 0.8/\sigma_e$ over a linear range of about $2\sigma_e$ [56]. As numerical simulations show that $\sigma_e \simeq 1.3 \cdot V_{\text{lsb}}$, it follows that $g_{\text{adc}} \simeq 0.6/V_{\text{lsb}}$, which is much higher

than in the case of the multibit ADC. In order to get the same $\gamma' = 2^{-11}$ and the same accuracy of the estimated coefficients, as in the previous example, the gain of the integrators in the LMS filter is set to $\gamma = 2^{-16}$, in this case. The transients of the coefficients shown in Fig. 4.13(b) exhibit a slew-rate regime at start-up, because of the limited dynamic-range of the single-bit ADC. Settling time in this case obviously depends on the final values of the coefficients $h_i[k]$. In the simulation of Fig. 4.13 all the coefficients settle in about $3.5 \cdot 10^5$ iteration cycles, corresponding to 14 ms.

Although the sign-error LMS has a speed/accuracy trade-off worse than the standard LMS, this is not a limiting factor in our case. What counts is the convergence speed in the presence of small perturbations occurring during normal operation. In fact, both in the case of standard and sign-error LMS, if perturbations are sufficiently small, convergence transients will be approximately the same. The reason is that the *average* behavior of the single-bit ADC is equivalent to that of a linear gain, in the presence of a sufficient level of noise dithering the ADC input. In our case, since the tracking capability of the sign-error algorithm is approximately the same as the one of the standard LMS for perturbations less than $1.3 \cdot V_{\text{lsb}}$, in many cases, the former can be preferred given its greater simplicity and efficiency.

4.7.2 Linearity

In order to get a measurement of the impact of the proposed LMS multipath adaptive filter on DAC linearity, the output spectrum in the case of a one-tone test has been simulated in Matlab, using for DAC1 the overall behavioral model presented in Chapter 3. Fig. 4.14 compares the DAC output spectra with a full-scale sinusoid input signal at frequency $f_{\text{IN}} = 100\,\text{MHz}$, before and after the application of the proposed technique. Without any correction applied [Fig. 4.14(a)] the combination of static and dynamic non-linearity errors produces an SFDR = 52 dB. When the LMS multipath adaptive filter is enabled [Fig. 4.14(b)], static non-linearity is canceled out, leading to an SFDR improvement of about 23 dB (SFDR = 75 dB). The same comparison in the case of a higher input signal frequency ($f_{\text{IN}} = 1.1\,\text{GHz}$) is shown in Fig. 4.15. Even in this case, the proposed adaptive linearization technique cancels the effects of static non-linearity errors, making the DAC limited only by the uncorrected dynamic ones. The SFDR is increased from 50 dB [Fig. 4.15(a)] to 66 dB [Fig. 4.15(b)].

For the sake of completeness, Fig. 4.16 shows the DAC SFDR as a function

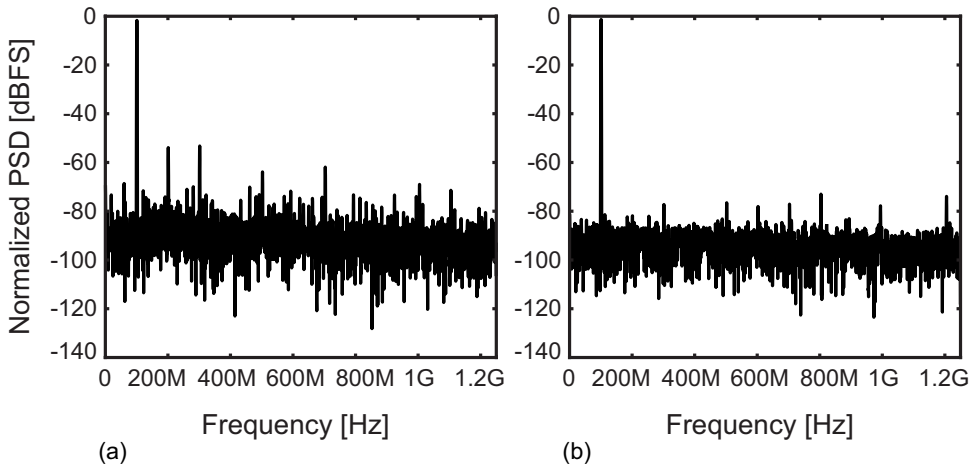

Figure 4.14 DAC output spectra in the case of a low-frequency input (f_{IN} = 100 MHz): (a) without corrections and (b) with the proposed adaptive linearization technique.

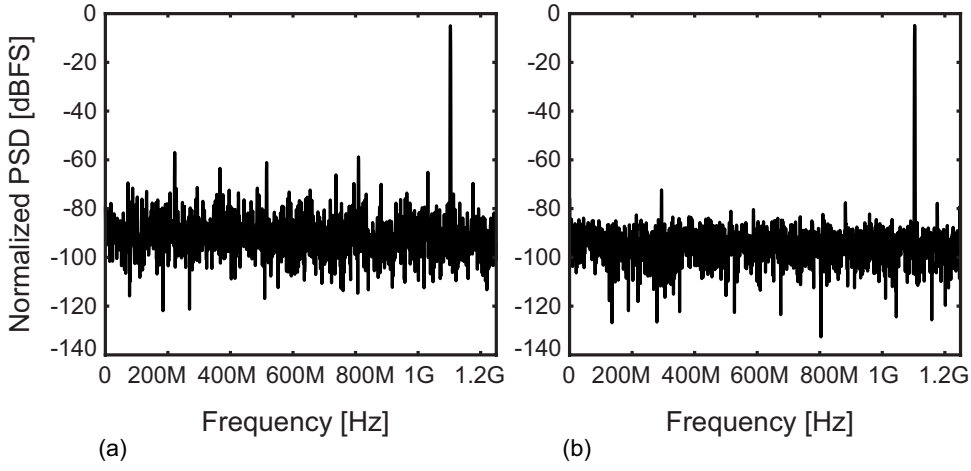

Figure 4.15 DAC output spectra in the case of a high-frequency input (f_{IN} = 1.1 GHz): (a) without corrections and (b) with the proposed adaptive linearization technique.

of input frequency f_{IN} before (gray plot) and after (black plot) the application of the proposed technique. Once again, even though the linearization operates on static non-linearity only, the significant SFDR improvement demonstrates its effectiveness over the entire Nyquist bandwidth. Furthermore, the SFDR trend confirms that the presence of uncorrected dynamic errors does not prevent the exact convergence of the LMS algorithm, as anticipated in section

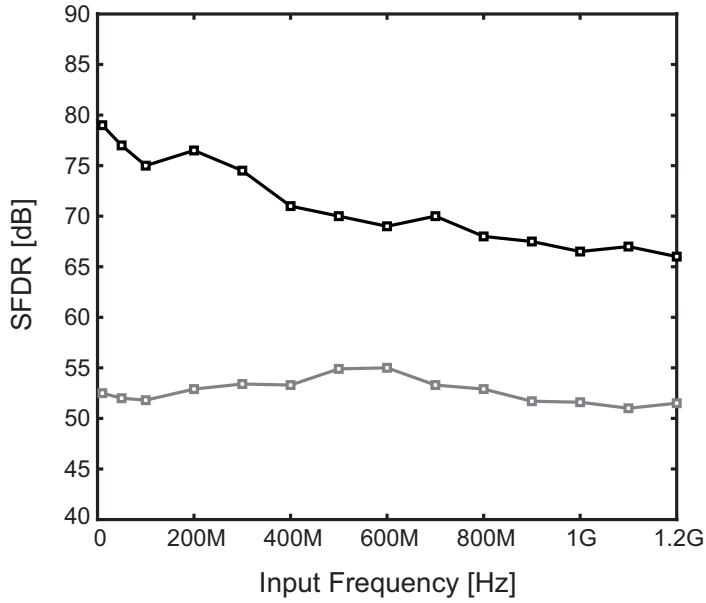

Figure 4.16 SFDR vs. input frequency: comparison between DAC without corrections (gray plot) and DAC with the proposed adaptive linearization technique.

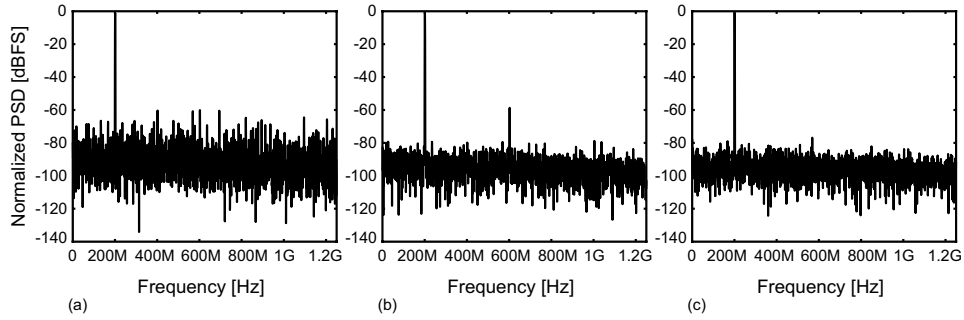

Figure 4.17 Comparison of DAC output spectra with a static third-order harmonic distortion applied: (a) without corrections, (b) with mismatch correction as in [47], (c) with the proposed multipath adaptive filter.

4.6.2.

Finally, in order to highlight the difference of the proposed technique with that one in [47], the DAC output spectrum has been simulated in the case of a one-tone test ($f_{\mathrm{IN}} = 200\,\mathrm{MHz}$) with a third-order static non-linearity added at the DAC model output. Modeling the hypothetical gain compression of a buffer or amplifier cascaded to the DAC, it has been expressed as $f(x) = \alpha_1 x + \alpha_3 x^3$ ($\alpha_1 = 1$, $\alpha_3 = -0.1$). The results are shown in Fig. 4.17. In the case of no corrections applied [Fig. 4.17(a)] the SFDR is 59 dB. With the adoption of the algorithm in [47] [Fig. 4.17(b)] static mismatches are canceled but third-order harmonic survives in the output spectrum confirming that this method is unable to compensate harmonic distortion, because of the randomization required for elements selection. On the contrary, Fig. 4.17(c) shows that our proposed adaptive linearization technique completely eliminates static non-linearity errors, including harmonic distortion, regardless of their source, leading to a significant SFDR improvement.

Chapter 5

Circuit Design of a 10-bit 2.5-GS/s DAC in 28-nm CMOS

Contents

5.1 Introduction

The digital adaptive linearization technique we introduced in the previous chapter has been implemented in a 28 nm CMOS chip prototype aimed at demonstrating the practical effectiveness of the proposed approach. Being the target application the baseband section of a 60 GHz transmitter, DAC specifications in terms of resolution and sampling frequency have been set to 10-bit and 2.5 GS/s, respectively, with a required SFDR greater than 60 dB over the entire Nyquist bandwidth. In particular, the DAC has been designed to achieve a differential peak-to-peak output swing of about 500 mV ($V_{\mathrm{lsb}} = 500\,\mu\mathrm{V}$) over

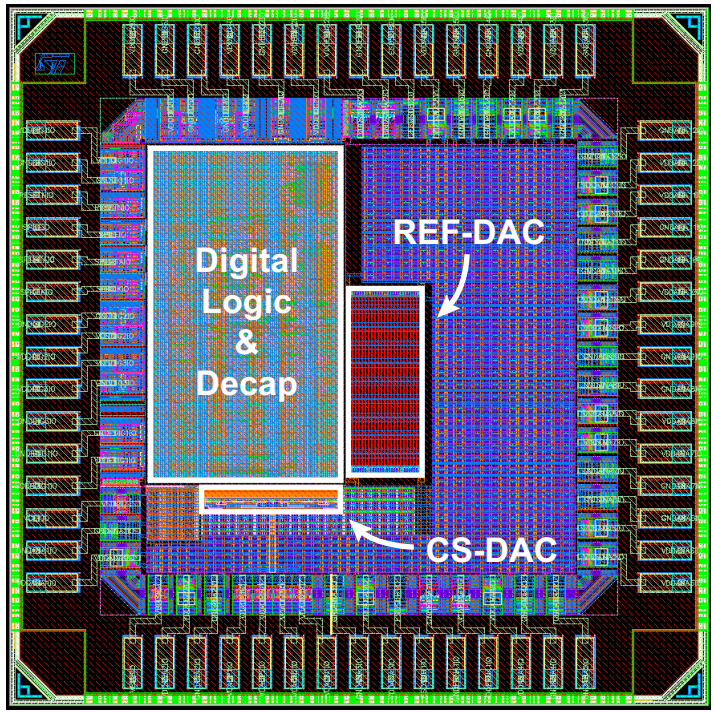

Figure 5.1 Layout of the overall designed DAC in 28 nm CMOS.

an external 50 Ω load. A nominal supply voltage of 1 V has been used for both analog and digital circuits.

The complete layout of the first chip prototype is shown in Fig. 5.1. The overall die measures 1.4 mm x 1.4 mm. Most of the area is occupied by wire-bonding pads and decoupling capacitors (about 1.8 nF and 2.9 nF for digital and analog supply voltages, respectively), which are essential in order to suppress the effects of supply noise. This first prototype version is aimed at off-line off-chip detection of the error signal ($e_q[k]$) required for the estimation of the LMS multipath filter coefficients. To this purpose, the chip incorporates all the digital adaptive predistortion logic, the current steering DAC and the reference DAC (i.e. DAC1 and DAC2, respectively, in Chapter 4). The next chip version also includes the sample-and-hold circuit needed for the on-chip background error signal detection.

In this chapter we will deal with circuit implementation aspects of each block of the system. In addition to the current-steering DAC, circuit design of a passive resistor-string DAC (used as the reference DAC2) and of a differential sample-and-hold circuit will be presented. Then, the main issues associated

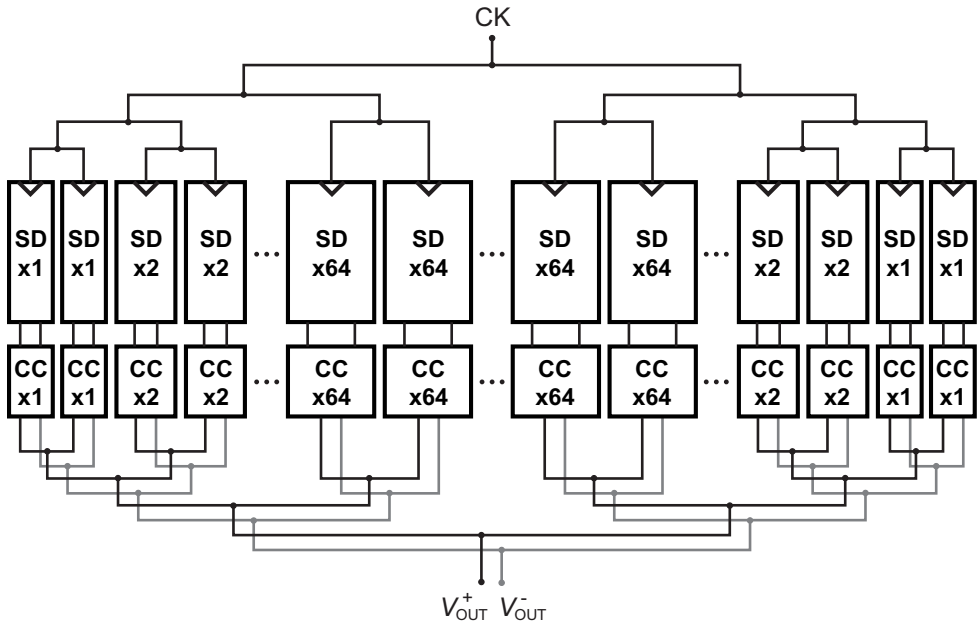

Figure 5.2 Conceptual floorplan of current-steering DAC. SD and CC stand for switch drivers and current cells, respectively.

with the synthesis of a 2.5 GHz digital logic will be briefly discussed. Finally, a performance summary will be provided, highlighting pros and cons of the proposed solution with respect to other state-of-the-art design. Since at the time of writing this Ph.D. dissertation the chip prototype was not available yet for experimental measurements, only simulation results will be considered. Also, potential phenomena degrading measured performances will be sketched.

5.2 Current-steering DAC

As already anticipated in previous chapters, the 10-bit 2.5 GS/s current-steering DAC has been implemented according to a segmented architecture in order to conjugate intrinsic advantages of thermometer-coded DACs (glitch energy, monotonicity) with those of binary-coded DACs (compactness, area) [14]. In particular, the overall DAC consists of a coarse thermometer-coded section with the 4 MSBs combined with a fine binary-coded section with the 6 LSBs. To accommodate the non-linearity correction terms, the fine sub-DAC dynamic range is further extended. As described in Chapter 4, a 16-paths LMS filter

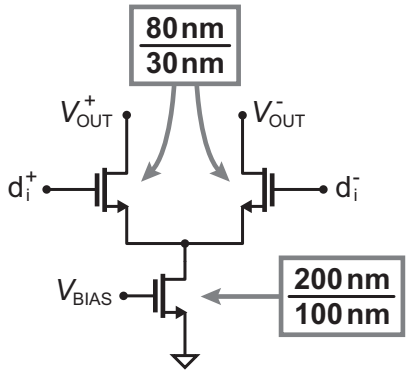

Figure 5.3 Unit current cell with near-minimum sized transistors.

linearizes the coarse static characteristic while the residual mismatch errors of the fine section are corrected as in [47].

Being the static characteristic linearized in digital domain, DAC circuit design has been fully oriented at optimizing dynamic performances. This is highlighted in Fig. 5.2, which shows a conceptual floorplan of the DAC. Instead of a traditional matrix-style layout a single-line configuration has been used, so as to improve compactness and minimize parasitic capacitances, which are detrimental for high-frequency performances. Furthermore, to ensure equal delays along the whole signal processing chain a binary tree configuration has been used for both clock distribution to switch drivers and differential signal paths from current cells to the outputs.

According to what seen in Chapter 2, circuit design of both unit current cells and switch drivers has been focused on optimization of speed and dynamic linearity.

5.2.1 Unit current cell

Without any requirement on static accuracy, the only objective of unit current cell design is to obtain proper values of switching resistance ΔR and switching capacitance ΔC, so as to pull down to a tolerable level output impedance and switched capacitance distortions.

Due to the small supply voltage ($V_{DD} = 1\,V$), the non-cascoded topology shown in Fig. 5.3 has been used. Given the LSB current $I_{lsb} = 10\,\mu A$, a current source length $L_{gen} = 100\,nm$ is needed to get a sufficiently high output resistance ($R_{on} \simeq 1.8\,M\Omega$). The optimum value of switch overdrive voltage (see Fig. 2.16 in Chapter 2) is achieved with $W_{gen} = 200\,nm$ and minimum-

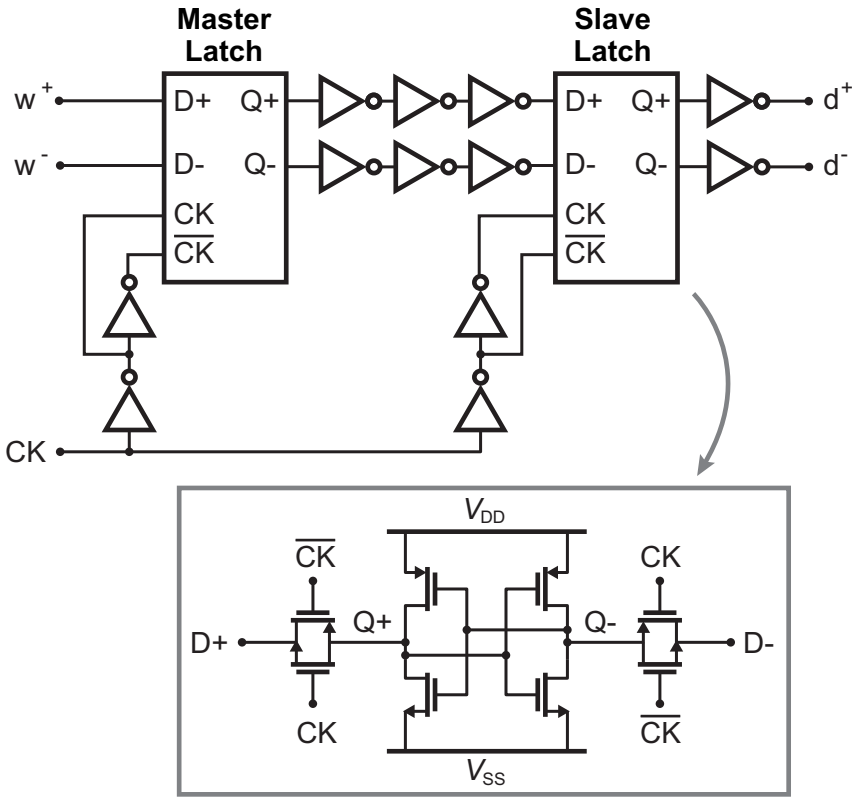

Figure 5.4 Switch driver circuit.

sized switches (80 nm/30 nm). In this way, the resulting switch capacitance $\Delta C < 20\,\text{aF}$ ensures an SFDR $> 60\,\text{dB}$ up to 1.2 GHz.

Current cells of different weights are simply obtained by properly scaling transistors widths.

5.2.2 Switch driver

The fundamental purpose of switch driver circuits is to accurately synchronize the current cells digital control signals, eliminating any spurious feed-through from digital logic to DAC output. In this design, the switch driver circuit depicted in Fig. 5.4 has been employed. It consists of a simple master-salve configuration in which two CMOS latches operate on opposite clock phases.

We have seen in Chapter 2 that, in order to lower distortion due to driver mismatches, both fast transitions of driving signals and good matching of driver transistors are needed. Unfortunately, this would lead to increased power consumption and dimensions of driver circuits. Therefore, in order to save power

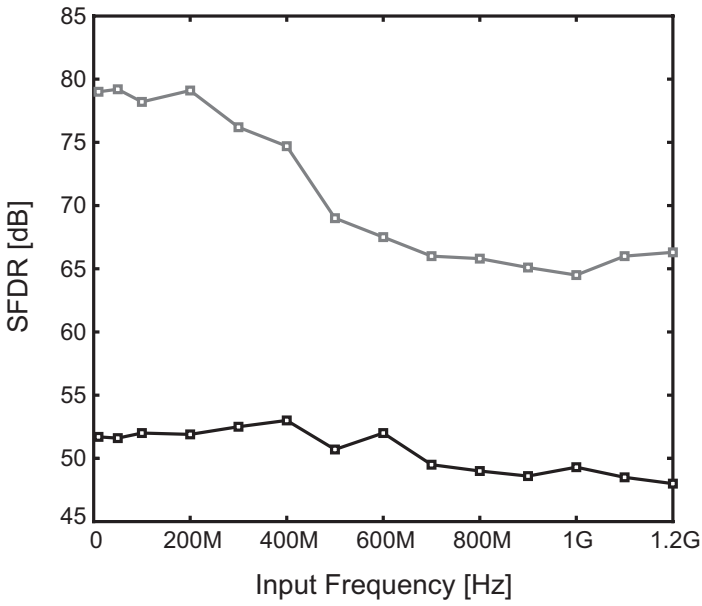

Figure 5.5 SFDR vs. input frequency resulting from circuit simulations: all the errors (black plot) and only dynamic errors (gray plot).

and area a progressively scaled CMOS buffer is inserted between master and slave latches and an further driver stage (i.e. a simple inverter) is added just before the switches. In this way, less sensitive blocks can be scaled down in size, leading to tapered design [8].

Each of the two latches is realized by means of the simple transmission-gate latch topology highlighted inside the gray box in Fig. 5.4. In fact, it is well known from literature that latch signal transients have to be kept as short as possible in order to minimize DAC sensitivity to driver mismatches, clock jitter, device noise, etc. To this purpose, the implemented CMOS configuration guarantees transitions steeper than any other CML latch.

Finally let us underline that local clock buffers are used inside every driver circuit to cancel out effects of data-dependent clock-loading on dynamic performances.

5.2.3 Simulation results

First of all, the overall power consumption of the designed current-sterring DAC resulting from circuit simulations is about 34 mW (including clock buffer, driving circuits and current cells) in the worst case of $f_S = 2.5\,\mathrm{GS/s}$ and $f_{IN} = 1.2\,\mathrm{GHz}$ (i.e. maximum switching activity).

Static and dynamic linearity performances have been simulated with a one-tone test for different input signal frequencies. The results are shown in Fig. 5.5. The SFDR when all the errors are accounted for (black plot) is approximately constant, as expected, going from 51 dB at DC to 48 dB at 1.2 GHz. This confirms that by means of the proposed DAC design we have effectively pulled down dynamic non-linearity errors below the static ones. This is further verified by the gray plot, which represents the SFDR when static mismatches are *disabled* by substituting current source transistors with their Norton equivalent circuits. The SFDR improvement over the entire bandwidth goes from a maximum of 27 dB at DC to a minimum of 17 dB at Nyquist.

5.3 Reference DAC

Having set $N_{\text{down}} = 100$, the reference DAC has been designed to operate at a down-sampled frequency $f_{\text{S,down}} = f_{\text{S}}/N_{\text{down}} = 25\,\text{MS/s}$. Because of its inherently monotonicity and low power consumption, the differential resistor-string DAC topology shown in Fig. 5.6 has been chosen [4]. Each of the two strings consists of $N = 2^{10}$ unit resistors R, so as to create a 1024-taps voltage divider between $V_{\text{DD}} = 1\,\text{V}$ and the externally provided $V_{\text{ref,bias}} = 0.75\,\text{V}$. A *zero-hot* encoder generates the digital control signals driving gates of simple *p*MOS switches. This means that, for both sides of the converter, at every sample all the switches are off except one which connects the selected tap of voltage divider to the corresponding output.

The only limitation to conversion speed is given by the finite convergence time constant due to DAC load capacitance. The most stringent situation occurs at mid-scale transitions, when the equivalent differential DAC output resistance is maximum ($R_{\text{eq}}|_{\text{diff}} = NR/2$). In this design, on the basis of considerations in terms of matching and power consumption, a unit poly-silicon resistor with $R = 25\,\Omega$ has been used. It follows that, in order to avoid any output finite settling effect even in the worst case (i.e. $\tau_{\text{eq}} \ll T_{\text{S,down}}/10$) a differential output capacitance $C_{\text{L}}|_{\text{diff}} \ll 300\,\text{fF}$ is required. As we will see in the next section, this requirement can be easily met.

The overall reference DAC consumes only 20 µA and occupies a 150 µm x 380 µm area. Monte-Carlo simulations of the static characteristic have been carried out in order to account for the effects of unit resistances random mismatches. An example is shown in Fig. 5.7. Maximum values of INL and DNL remain well below 1-LSB confirming a proper functioning of the designed DAC as reference for the linearization of the current-steering one.

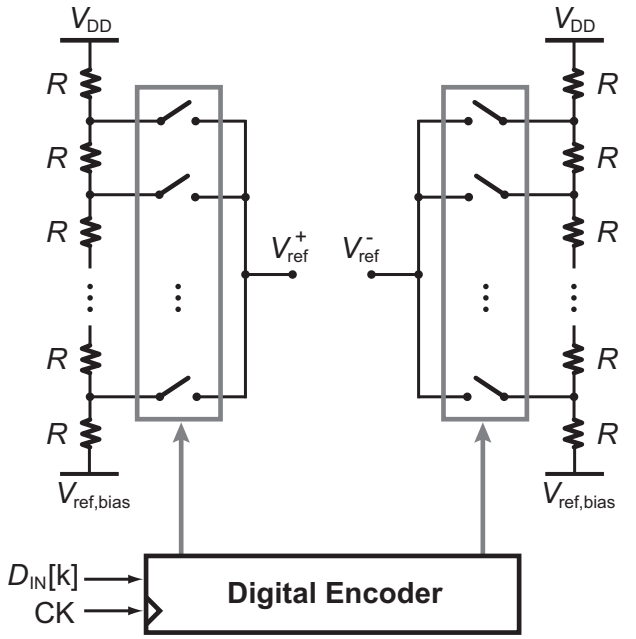

Figure 5.6 Differential resistor-string DAC.

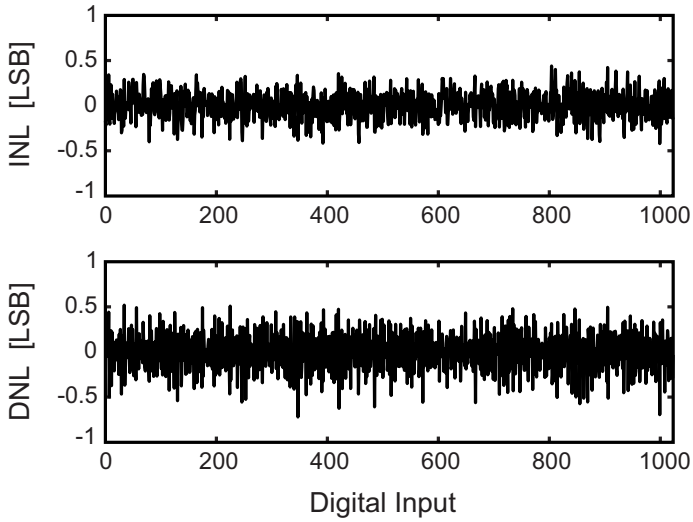

Figure 5.7 Reference DAC INL and DNL obtained by circuit simulations.

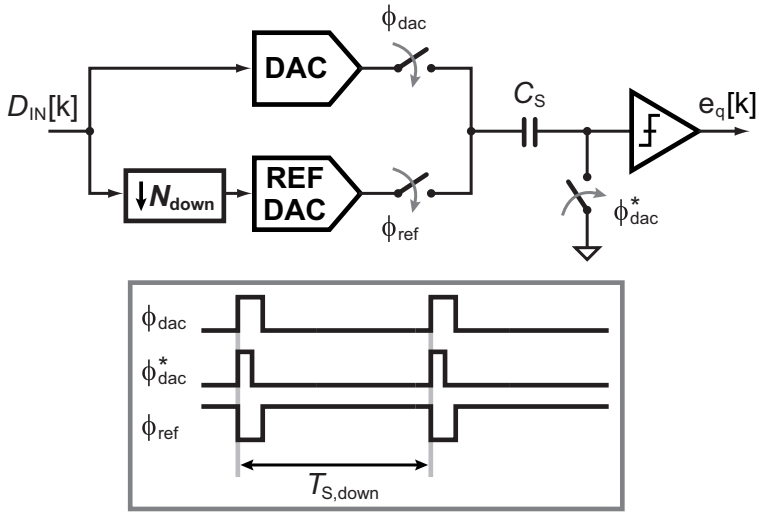

Figure 5.8 Conceptual scheme of sample-and-hold circuit and comparator chain. For simplicity, the single-ended version is depicted.

5.4 Sample-and-hold circuit

To complete the analog section of the overall system, the only remaining block is a sample-and-hold circuit which must be able to accurately sample the current-steering DAC output in a sampling period T_S, once out of N_{down} samples, and then to compare it with the reference DAC output. Even though the remarkable difference between $T_S = 400\,ps$ (i.e. the duration of the sampling phase of the current-steering DAC) and $T_{S,down}$ (which approximately corresponds to the comparing phase), this operation can be accomplished by a simple two-phases circuit, as clearly shown in the conceptual scheme of Fig. 5.8. Let us note that circuit is drawn single-ended for simplicity, even though it is fully differential in practice.

Circuit operation is based on the use of two non-overlapping clock phases: ϕ_{dac} (with duration T_S, once out of N_{down} sampling periods) and ϕ_{ref} (which covers the remaining part of the down-sampled period $T_{S,down}$), while ϕ^*_{dac} is a replica of ϕ_{dac} turning off slightly before. This technique, known as *bottom-plate sampling* [57], minimizes signal-dependent charge injection. When the sampling phase ϕ_{dac} is active, the current-steering DAC output voltage V_{dac} is acquired on sampling capacitor C_S. Then, during the comparison phase ϕ_{ref}, the reference DAC is connected in series to C_S, while all the other switches are

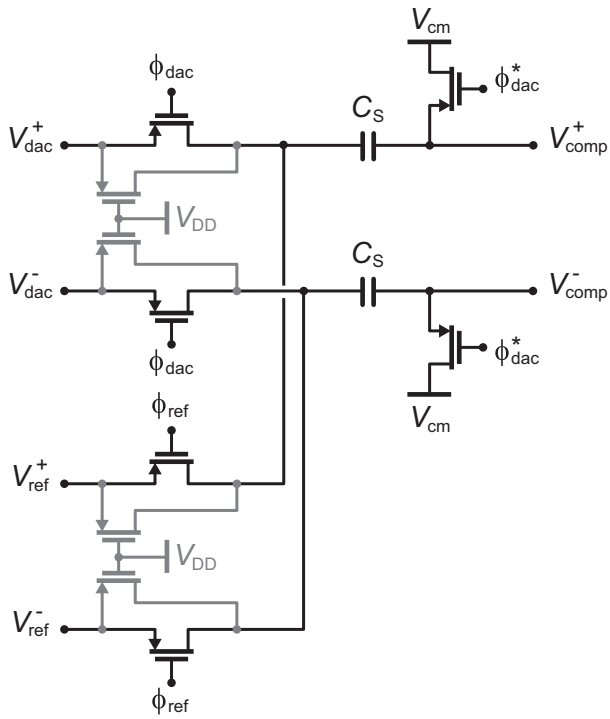

Figure 5.9 Differential sample-and-hold circuit.

off. It results that the voltage at comparator input is given by:

$$V_{\text{comp}}[k] = V_{\text{ref}}[k] - V_{\text{dac}}[k]\,, \tag{5.1}$$

and hence the value of quantized error $e_q[k]$ effectively depends on the sign of the difference between DACs output voltages.

The design of such circuit in terms of speed and accuracy can be extremely simplified if we remember basic concepts on LMS algorithm convergence. We have indeed seen in Chapter 4 that any noise uncorrelated with DAC digital input code has no effect on convergence of the linearization technique, except for the accuracy of estimated coefficients, which however can be improved by properly setting the update parameter γ. It follows that we can reduce the sampling capacitor value, without totally caring of kT/C noise. This leads to a great advantage in terms of both circuit sampling speed and disturbances injected into current-steering DAC output nodes. The resulting differential circuit is depicted in Fig. 5.9, where we used two sampling Metal-Oxide-Metal (MOM) capacitors of value $C_S = 5\,\text{fF}$. Dummy transistors (always off) are

drawn in gray, which are used to compensate feed-through effects.

In order to verify the impact of the proposed sample-and-hold circuit on overall DAC performances, the spectra of both the current-steering DAC output and the sampled voltage have been simulated in the case of a one-tone test. Fig. 5.10 shows the results obtained with $f_{IN} = 1.1\,\text{GHz}$, $f_S = 2.5\,\text{GS/s}$ and $N_{down} = 4$ instead of 100, so as to lower simulation time. Focusing on DAC output spectrum [Fig. 5.10(a)], even though spurs at a frequency offset equal to $f_S/N_{down} = 625\,\text{MHz}$ appear, because of disturbances produced by the sample-and-hold circuit, they still are below the third-order harmonic due to the switched capacitance effect and, hence, the SFDR degradation is negligible (SFDR = 66 dB). SFDR of the sampled voltage is further better, since dynamic effects are mostly died at the end of the sampling phase, as evident from Fig. 5.10(b). Finally, Fig. 5.11 shows the SFDR of DAC output (with mismatches disabled) when connected to the sample-and-hold circuit, as a function of the input frequency, compared with the results we have obtained in section 5.2.3 for the current-steering DAC only. The figure clearly demonstrates that sample-and-hold circuit operation does not degrades substantially spectral performances of the overall system, except for the low-frequency range, where the penalty still remains below 5 dB.

5.5 Digital logic

In addition to the 1.8 nF supply voltage decoupling capacitance, digital section of the system mostly consists of the digital adaptive predistortion scheme performing the DAC static characteristic linearization, as described in the previous chapter. Furthermore, in order to allow chip testing without the need of driving high-speed digital signals from the outside, two Direct Digital Frequency Synthesizers (DDFSs) have been included for one-tone and two-tone linearity tests. Then, all the digital control signals and parameters are set by means of a standard Serial-to-Parallel Interface.

The implementation of such complex digital logic has been carried out by following the traditional automatic standard cells flow. Starting from the VHDL description of the system, CAD tools have been used to synthesize, place, route and verify all the digital logic. In particular, in order to meet the extremely stringent speed requirement ($f_{clk} = 2.5\,\text{GHz}$), a digital pipeline implementation has been required. This approach permits to reduce register-to-register paths length (and hence their corresponding propagation delay) at the cost of an increased latency of the overall system. As an example Fig. 5.12

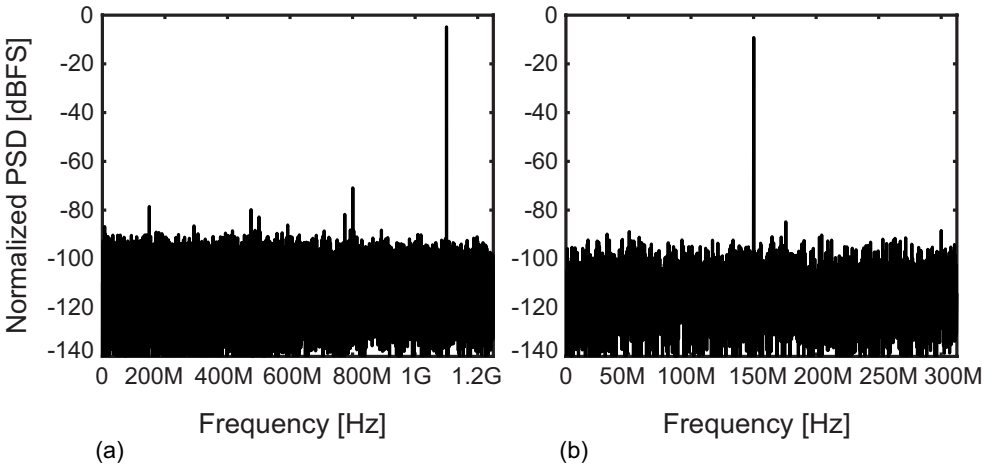

Figure 5.10 Spectra of (a) Current-steering DAC output and (b) down-sampled signal in the case of a one-tone test with $f_{\mathrm{IN}} = 1.1\,\mathrm{GHz}$, $f_{\mathrm{S}} = 2.5\,\mathrm{GS/s}$ and $N_{\mathrm{down}} = 4$.

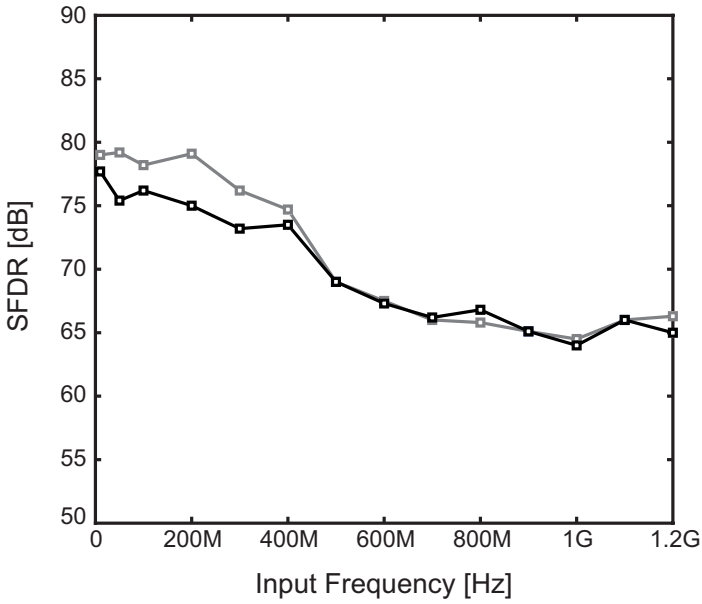

Figure 5.11 SFDR vs. input frequency resulting from circuit simulations. Comparison between DAC without (gray plot) and with (black plot) the sample-and-hold circuit.

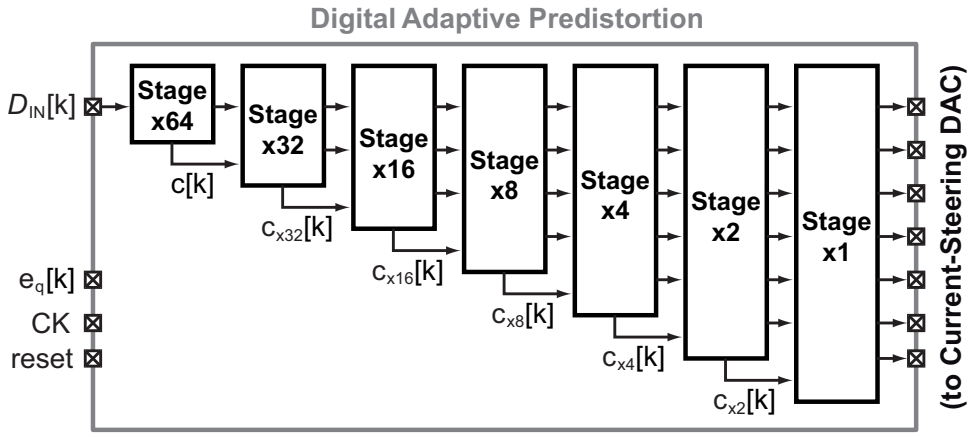

Figure 5.12 Pipeline implementation of the digital adaptive predistortion scheme.

shows the pipeline arrangement of the digital predistortion scheme. In this architecture, each stage of the pipeline is realized by more than one register stages and corresponds to a certain level of the current-steering DAC.

The pipeline depth of the overall digital section (including DDFSs, control logic, predistortion scheme and encoders) is about 50 stages and the total gate count is approximately 16000 (except for decoupling capacitors, which are not accounted for).

5.6 Performance summary

Main data and characteristics of the overall design are summarized in Tab. 5.1, where simulation results of the proposed DAC are compared with measured performances of the most recently published CMOS Digital-to-Analog Converters with sampling frequencies in the GS/s range, which have been already analyzed in Chapter 1 and 2. Although not totally fair, because relying on simulations instead of measurement data, this kind of comparison can be useful to evaluate the potential extent of advantages and/or drawbacks of the proposed technique with respect to the ones reported in open literature.

As previously discussed, the proposed 10-bit 2.5 GS/s current-steering DAC has been designed in a 28 nm CMOS process using a single supply voltage $V_{\mathrm{DD}} = 1\,\mathrm{V}$. Providing a 10 mA full-scale current onto a 50 Ω differential load, it achieves a peak-to-peak output voltage swing of about 500 mV. Even though the lower supply voltage, the resulting power delivered to the load ($P_{\mathrm{load}} = -2\,\mathrm{dBm}$), is in line with the state-of-the-art, except for the high-voltage DACs

	This Work	[8]	[9]	[10]	[11]	[12]	[13]
Process [nm]	28	65	130	65	90	180	40
Supply [V]	1	1.1/2.5	1.2/1.8	1.2	1.2/2.5	1.8/3.3	1.2
$\boldsymbol{I_{\text{load}}}$ **[mA]**	10	50	10	8	16	20	16
$\boldsymbol{P_{\text{TOT}}}$ **[mW]**	N/A	188	27	60	128	600	40
$\boldsymbol{P_{\text{load}}}$ **[dBm]**	-2	12	-2	-1	-7	4	-4
Res. [bits]	10	12	10	9	12	14	12
$\boldsymbol{f_{\text{S}}}$ **[GS/s]**	2.5	1.6/2.9	1.6	3	1.25	3/6	1.6
$\textbf{SFDR}\boldsymbol{\vert_{\text{DC}}}$ **[dB]**	78	74	74	61	75	84	74
$\textbf{SFDR}\boldsymbol{\vert_{\text{Nyq}}}$ **[dB]**	65	52	50	53	66	57.5	70

Table 5.1 Performance summary of the designed DAC, compared with the most recently published state-of-the-art DACs, which have been already shown in Tab. 1.1 in Chapter 1.

[8], [12] and Return-to-Zero DACs [11], [13], which achieve much higher and much lower output powers, respectively.

For what concerns spectral performances, compared to the other state-of-the-art methods, the proposed digital adaptive linearization technique promises better, or at least comparable, linearity. While the Spurious-Free Dynamic Range at low frequency ($\text{SFDR}|_{\text{DC}} = 78\,\text{dB}$) is approximately at the same level as other designs, the most substantial advantage can be found in the high-frequency range, as expected. Linearity at Nyquist ($\text{SFDR}|_{\text{Nyq}} = 65\,\text{dB}$) is indeed better than almost all the other state-of-the-art DACs, and only comparable to RZ DAC designs [11], [13], which however are characterized by a considerably lower output power level. Furthermore, remembering that the proposed DAC has a lower nominal resolution than the others (except [10], 10-bits against 12/14-bits), linearity data suggest an interesting insight: high resolution is not only useless in the high-frequency range, but even detrimental. In other words, dynamic linearity benefits from circuit simplicity and minimum dimensions.

Finally, to complete the comparison with literature, in particular with [11] and [13] which provide slightly better linearity even though at a lower f_{S}, the overall power consumption must be accounted for. Unfortunately, during the design process, only the estimation of the *analog* power (i.e. the power of

current-steering and resistor-string DACs) has been achieved (36 mW at the maximum input frequency). On the contrary, it has not been possible to get a realistic estimation of the digital core power consumption, that has to be expected a significant contribution in the overall term P_{TOT}, because of the high clock frequency. For this reason a fair comparison with state-of-the-art will be possible only on the basis of experimental results in terms of power consumption measurements.

Other phenomena potentially degrading DAC performances are supply noise, inductive coupling at the interface with the external load and accuracy of on-chip current and voltage references. Once again, evaluation of the effective impact of all these factors will be allowed only by experimental measurements.

Conclusions

This Ph.D. dissertation has focused on definition and development of new design methodologies and techniques for the implementation of high-speed high-performance DACs suitable for the integration in ultra-scaled CMOS technologies, allowing to overcome the fundamental trade-offs between static linearity, dynamic linearity and power efficiency. In particular, a novel digital technique for the linearization of the DAC static characteristic has been introduced, which proves suitable for Digital-to-Analog Converters with sampling frequencies in the GS/s range and medium-to-high resolutions. To demonstrate its effectiveness, the proposed method has been applied to the design and the implementation of a 10-bit 2.5 GS/s DAC in 28 nm CMOS.

The digital linearization algorithm is based on the use of a new multipath LMS adaptive filter that continuously measures and cancels static non-linearity errors in the background of normal operation. Since analog circuits impairments are canceled out in the digital domain, a design full-oriented at optimizing dynamic performances is allowed, overcoming in this way the typical trade-off between low-frequency and high-frequency linearity. The proposed scheme includes an additional voltage comparator and an ancillary slow rate, yet linear, DAC, resulting in an extremely simple and low-power overall DAC architecture. Behavioral simulations confirm the effectiveness of algorithm in increasing the linearity across the full bandwidth, with an improvement ranging from 26 dB at DC to 15 dB at the Nyquist frequency. Theoretical aspects of this linearization technique have been published at an IEEE conference [52].

A 10-bit 2.5 GS/s current-steering DAC including the digital calibration scheme has been designed and implemented in 28 nm CMOS. Using a single supply voltage $V_{DD} = 1$ V, it provides a 10 mA full-scale current onto a 50 Ω differential load, resulting in a -2 dBm output power. While the current-steering circuit consumes 36 mW power at the maximum operating frequency, the ancillary 10-bit 25 MS/s resistor-string DAC draws only about 20 µA. Although at the time of writing this Ph.D. dissertation the chip prototype was not available

yet for experimental measurements, simulation results showed a DAC SFDR greater than 65 dB across the entire Nyquist bandwidth ($\mathrm{SFDR}|_{\mathrm{DC}} = 78\,\mathrm{dB}$ and $\mathrm{SFDR}|_{\mathrm{Nyq}} = 65\,\mathrm{dB}$), revealing the potential effectiveness of the proposed linearization technique to advance the state-of-the-art.

In conclusion, the present work has demonstrated that the extensive use of digital adaptive calibration algorithms can make high-speed DACs suitable for the application to modern multi-carrier multi-band transmitters to be integrated in low-cost ultra-scaled CMOS processes. With respect to the results reported in this dissertation, further benefits in this field will come from future research aimed at increasingly simplifying the required digital hardware complexity for the implementation of such techniques, leading to a further improvement in terms of both area and power efficiency.

References

[1] IEEE 802.15.3c Standard. [Online]. Available: http://ieeexplore.ieee.org/-xpl/mostRecentIssue.jsp?punumber=5284442

[2] B. Razavi, *RF Microelectronics*, 2nd ed. Prentice Hall, 2011.

[3] M. Gustavsson, J. Wikner, and N. Tan, *CMOS Data Converters for Communications*. Kluwer Academic Publishers, 2000.

[4] B. Razavi, *Principles of Data Conversion System Design*. John Wiley & Sons, 1995.

[5] IEEE 802.3an Standard. [Online]. Available: http://ieeexplore.ieee.org/-xpl/mostRecentIssue.jsp?punumber=11160

[6] S. Spiridon, J. van der Tang, H. Yan, H.-F. Chen, D. Guermandi, X. Liu, E. Arslan, F. van der Goes, and K. Bult, "A 375 mW Multimode DAC-Based Transmitter with 2.2 GHz Signal Bandwidth and In-Band IM3 < -58 dBc in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1595–1604, July 2013.

[7] R. Farjad, F. Gerfers, M. Brown, A. Tavakoli, D. Nguyen, H. Sedarat, R. Shirani, and H.-T. Ng, "A 48-Port FCC-Compliant 10GBASE-T Transmitter with Mixed-Mode Adaptive Echo Canceller," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3261–3272, December 2012.

[8] C.-H. Lin, F. van der Goes, J. Westra, J. Mulder, Y. Lin, E. Arslan, E. Ayranci, X. Liu, and K. Bult, "A 12 bit 2.9 GS/s DAC with IM3 < -60 dBc Beyond 1 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3285–3293, December 2009.

[9] P. Palmers and M. Steyaert, "A 10-bit 1.6-GS/s 27-mW Current-Steering D/A Converter with 550-MHz 54-dB SFDR Bandwidth in 130-nm CMOS,"

IEEE Trans. Circuits Syst. I, vol. 57, no. 11, pp. 2870–2879, November 2010.

[10] S. Le Tual, P. Singh, A. Bal, and C. Garnier, "A 3GS/s, 9b, 1.2V Single Supply, Pure Binary DAC with >50dB SFDR up to 1.5GHz in 65nm CMOS," in *IEEE Symp. VLSI Circuits*, 2011, pp. 64–65.

[11] W.-H. Tseng, C.-W. Fan, and J.-T. Wu, "A 12-Bit 1.25-GS/s DAC in 90 nm CMOS with > 70dB SFDR up to 500 MHz," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2845–2856, December 2011.

[12] G. Engel, S. Kuo, and S. Rose, "A 14b 3/6GHz Current-Steering RF DAC in 0.18 µm CMOS with 66dB ACLR at 2.9GHz," in *IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 458–460.

[13] W.-T. Lin and T.-H. Kuo, "A 12b 1.6GS/s 40mW DAC in 40nm CMOS with >70dB SFDR Over Entire Nyquist Bandwidth," in *IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 474–475.

[14] C.-H. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm^2," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1948–1958, December 1998.

[15] A. Van Den Bosch, M. Borremans, M. Steyaert, and W. Sansen, "A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 315–324, March 2001.

[16] K. Doris, "High-Speed D/A Converters: from Analysis and Synthesis Concepts to IC Implementation," Ph.D. dissertation, Eindhoven University of Technology, 2004.

[17] J. Bastos, A. Marques, M. Steyaert, and W. Sansen, "A 12-bit Intrinsic Accuracy High-Speed CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1959–1969, December 1998.

[18] G. Van Der Plas, J. Vandenbussche, W. Sansen, M. Steyaert, and G. Gielen, "A 14-bit Intrinsic Accuracy Q^2 Random Walk CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1708–1718, December 1999.

[19] A. Bugeja and B.-S. Song, "A Self-Trimming 14-b 100-MS/s CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1841–1852, December 2000.

[20] M. Tiilikainen, "A 14-bit 1.8-V 20-mW 1-mm^2 CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1144–1147, July 2001.

[21] K. O'Sullivan, C. Gorman, M. Hennessy, and V. Callaghan, "A 12-bit 320-MSample/s Current-Steering CMOS D/A Converter in 0.44-mm^2," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1064–1072, July 2004.

[22] T. Chen and G. Gielen, "A 14-bit 200-MHz Current-Steering DAC with Switching-Sequence Post-Adjustment Calibration," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2386–2394, November 2007.

[23] W. Schofield, D. Mercer, and L. Onge, "A 16b 400MS/s DAC with <-80dBc IMD to 300MHz and <-160dBm/Hz Noise Power Spectral Density," in *IEEE ISSCC Dig. Tech. Papers*, 2003, pp. 126–482.

[24] B. Schafferer and R. Adams, "A 3V CMOS 400mW 14b 1.4GS/s DAC for Multi-Carrier Applications," in *IEEE ISSCC Dig. Tech. Papers*, 2004, pp. 360–532.

[25] K. Doris, J. Briaire, D. Leenaerts, M. Vertreg, and A. van Roermund, "A 12b 500MS/s DAC with >70dB SFDR up to 120MHz in 0.18 µm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2005, pp. 116–588.

[26] K. Chan and I. Galton, "Dynamic Element Matching to Prevent Nonlinear Distortion from Pulse-Shape Mismatches in High-Resolution DACs," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2067–2078, September 2008.

[27] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching Properties of MOS Transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, October 1989.

[28] M. Clara, W. Klatzer, B. Seger, A. Di Giandomenico, and L. Gori, "A 1.5V 200MS/s 13b 25mW DAC with Randomized Nested Background Calibration in 0.13 µm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 250–600.

[29] X. Wu and M. Steyaert, "Output Impedance Analysis of Digital-to-Analogue Converters," *Electronics Letters*, vol. 47, no. 24, pp. 1314–1316, 2011.

[30] A. Bugeja, B.-S. Song, P. Rakers, and S. Gillig, "A 14-b, 100-MS/s CMOS DAC Designed for Spectral Performance," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1719–1732, December 1999.

[31] P. Larsson, "Resonance and Damping in CMOS Circuits with On-Chip Decoupling Capacitance," *IEEE Trans. Circuits Syst. I*, vol. 45, no. 8, pp. 849–858, August 1998.

[32] J. Vandenbussche, G. Van der Plas, G. Gielen, and W. Sansen, "Behavioral Model of Reusable D/A Converters," *IEEE Trans. Circuits Syst. II*, vol. 46, no. 10, pp. 1323–1326, October 1999.

[33] M. Naoues, D. Morche, C. Dehos, R. Barrak, and A. Ghazel, "Novel Behavioral DAC Modeling Technique for WirelessHD System Specification," in *IEEE Int. Conf. on Electronics, Circuits and Systems*, 2009, pp. 543–546.

[34] C. Su and R. Geiger, "Dynamic Calibration of Current-Steering DAC," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2006, pp. 4–120.

[35] B. Catteau, P. Rombouts, and L. Weyten, "A Digital Calibration Technique for the Correction of Glitches in High-Speed DAC's," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2007, pp. 1477–1480.

[36] A. Oppenheim and R. Schafer, *Discrete-Time Signal Processing*, 3rd ed. Prentice Hall, 2009.

[37] C.-H. Hsu, M. Straayer, and M. Perrott, "A Low-Noise Wide-BW 3.6-GHz Digital $\Delta\Sigma$ Fractional-N Frequency Synthesizer with a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2776–2786, December 2008.

[38] M. Zanuso, S. Levantino, C. Samori, and A. L. Lacaita, "A Wideband 3.6 GHz Digital $\Delta\Sigma$ Fractional-N PLL with Phase Interpolation Divider and Digital Spur Cancellation," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 627–638, March 2011.

[39] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. Lacaita, "A 2.9-4.0-GHz Fractional-N Digital PLL with Bang-Bang Phase Detector and $560 - \mathrm{fs}_{\mathrm{rms}}$ Integrated Jitter at 4.5-mW Power," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2745–2758, December 2011.

[40] G. Marzin, S. Levantino, C. Samori, and A. Lacaita, "A 20 Mb/s Phase Modulator Based on a 3.6 GHz Digital PLL with -36 dB EVM at 5 mW Power," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2974–2988, December 2012.

[41] Y. Chiu, C. Tsang, B. Nikolic, and P. Gray, "Least Mean Square Adaptive Digital Background Calibration of Pipelined Analog-to-Digital Converters," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 1, pp. 38–46, January 2004.

[42] B. Murmann and B. Boser, "A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, December 2003.

[43] A. Panigada and I. Galton, "A 130 mW 100 MS/s Pipelined ADC with 69 dB SNDR Enabled by Digital Harmonic Distortion Correction," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3314–3328, December 2009.

[44] A. Verma and B. Razavi, "A 10-bit 500-MS/s 55-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3039–3050, November 2009.

[45] I. Galton, "Digital Cancellation of D/A Converter Noise in Pipelined A/D Converters," *IEEE Trans. Circuits Syst. II*, vol. 47, no. 3, pp. 185–196, March 2000.

[46] X. Wang, U. Moon, M. Liu, and G. Temes, "Digital Correlation Technique for the Estimation and Correction of DAC Errors in Multibit MASH $\Delta\Sigma$ ADCs," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2002, pp. IV–691–IV–694.

[47] B. Catteau, P. Rombouts, J. Raman, and L. Weyten, "An On-Line Calibration Technique for Mismatch Errors in High-Speed DACs," *IEEE Trans. Circuits Syst. I*, vol. 55, no. 7, pp. 1873–1883, August 2008.

[48] S. Haykin, *Adaptive Filter Theory.* Prentice Hall Ed., 2002.

[49] A. Sayed, *Adaptive Filters.* John Wiley & Sons, 2008.

[50] C. Daigle, A. Dastgheib, and B. Murmann, "A 12-bit 800-MS/s Switched-Capacitor DAC with Open-Loop Output Driver and Digital Predistortion," in *IEEE Asian Solid-State Circuits Conf. Dig.*, 2010, pp. 1–4.

[51] A. Panigada and I. Galton, "Digital Background Correction of Harmonic Distortion in Pipelined ADCs," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 9, pp. 1885–1895, September 2006.

[52] A. Fenaroli, S. Levantino, C. Samori, and A. Lacaita, "Background Adaptive Linearization of High-Speed Digital-to-Analog Converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2013, pp. 582–585.

[53] B. Widrow, J. McCool, M. Larimore, and C. Johnson, "Stationary and Nonstationary Learning Characteristics of the LMS Adaptive Filter," *Proc. IEEE*, vol. 64, no. 8, pp. 1151–1162, August 1976.

[54] W. Liu, P. Huang, and Y. Chiu, "A 12-bit, 45-MS/s, 3-mW Redundant Successive-Approximation-Register Analog-to-Digital Converter with Digital Calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2661–2672, November 2011.

[55] A. Swaminathan, K. Wang, and I. Galton, "A Wide-Bandwidth 2.4 GHz ISM Band Fractional-N PLL with Adaptive Phase Noise Cancellation," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2639–2650, December 2007.

[56] N. Da Dalt, "Markov Chains-Based Derivation of the Phase Detector Gain in Bang-Bang PLLs," *IEEE Trans. Circuits Syst. II*, vol. 53, no. 11, pp. 1195–1199, November 2006.

[57] K.-L. Lee and R. Mayer, "Low-Distortion Switched-Capacitor Filter Design Techniques," *IEEE J. Solid-State Circuits*, vol. 20, no. 6, pp. 1103–1113, December 1985.