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ANALYSIS AND MINIMIZATION OF FLICKER NOISE UP-CONVERSION IN RADIO-FREQUENCY LC-TUNED OSCILLATORS

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Abstract

THE world cell phones market experienced a steady growth in latest years, driven by the increasing number of applications available on smartphones, tablet computers and PDAs. Today's portable devices integrate multiple communication capabilities with ever-increasing data transfer rates. In this scenario, the implementation of single-chip radio transceivers capable of operating over multiple standards is of great interest. The need for a higher integration level to reduce board size and cost led CMOS processes to fast become the technology of choice in RFIC development. However, to take full advantage of the switching characteristics of MOS transistors in CMOS, a digital approach started to be adopted in the RFIC design. On the contrary, the analog section of transceivers must cope with the limitations imposed by the adoption of scaled CMOS processes, for example the large flicker noise corner frequencies.

In this context, the design of local oscillators (LOs) for signal (de)modulation is becoming a highly-demanding task. This is due to the need of oscillators with an increasingly-broad tuning range to comply with different radio-communication standards. In the traditional design approach, however, this generally leads to a non-optimum sizing of the active devices of the oscillators. This further exacerbates the impact of flicker noise, eventually resulting into unacceptable phase noise performances.

The main purpose of this doctoral thesis is to provide a detailed quantitative analysis of the flicker noise up-conversion mechanisms, filling the gap towards a complete understanding of this phenomenon. In particular, it

will be shown that harmonic distortion is the major $1/f^3$ phase noise source in voltage-biased oscillator topologies, while the modulation of parasitics is the dominant effect in the current-biased counterparts. A detailed analysis is carried out in the framework of the so-called impulse sensitivity function.

Basing on theoretical results, several techniques to mitigate or suppress the flicker noise up-conversion are presented, together with measurements results carried out on three different test chips which confirm the validity of the proposed analyses. Furthermore, a new accurate simulation technique to compute the impulse sensitivity function in oscillators is presented, which is easier and faster to be implemented with respect to the traditional method.

Riassunto

Il mercato mondiale dei telefoni cellulari ha assistito negli ultimi anni ad una crescita esplosiva, guidata dal crescente numero di funzioni disponibili negli "smartphone" e nei computer "tablet". I moderni dispositivi portatili integrano molteplici standard di comunicazione con velocità di trasmissione dei dati sempre maggiore. In questo scenario è di grande interesse la possibilità di implementare trasmettitori radio su singolo chip capaci di operare su diversi sistemi di comunicazione. D'altra parte, la necessità di ottenere un'elevata integrazione, per ridurre l'ingombro ed il costo della scheda, ha consentito alle tecnologie CMOS scalate di diventare ben presto le tecnologie principali nell'ambito della progettazione dei circuiti integrati a radiofrequenza. Ciò ha comportato l'impiego sempre maggiore di circuiti digitali, per poter beneficiare a pieno delle caratteristiche di buoni interruttori dei transistori MOS scalati. La sezione analogica del ricetrasmettitore, invece, deve adattarsi alle limitazioni imposte dell'adozione di tecnologie CMOS scalate, ad esempio l'elevata presenza di rumore flicker prodotto dai transistori.

In questo contesto la progettazione di oscillatori locali per la (de)modulazione dei segnali diventa un'attività molto complessa. Ciò è dovuto in maniera determinante anche alla necessità di realizzare oscillatori capaci di sintetizzare ampi intervalli di frequenza, in modo da operare su diversi standard di comunicazione. Tuttavia, adottando un approccio di progetto tradizionale, questa richiesta comporterebbe un dimensionamento non ottimale dei dispositivi attivi dell'oscillatore. Ciò determina un ulteriore innal-

zamento dell'impatto del rumore flicker, che si traduce infine in prestazioni di rumore inaccettabili.

Lo scopo principale di questa tesi di dottorato è fornire un'analisi quantitativa dettagliata dei meccanismi di conversione del rumore flicker in rumore di fase, basata su una profonda comprensione fisica del fenomeno. In particolare, sarà dimostrato che la distorsione armonica è l'origine principale del rumore di fase con andamento $1/f^3$ nelle topologie di oscillatore polarizzate in tensione, mentre la modulazione dei parassiti capacitivi è l'effetto dominante in quelle polarizzate in corrente. L'analisi di entrambi i fenomeni viene effettuata adottando il concetto di funzione di sensitività all'impulso.

Sulla base dei risultati teorici sono presentate diverse tecniche circuitali per ridurre l'impatto del rumore flicker, la cui validità è stata verificata attraverso tre diversi circuiti integrati di test. Le misure effettuate confermano inoltre la bontà dell'analisi di rumore. Infine, viene presentata una nuova accurata tecnica di simulazione per ricavare la funzione di sensitività all'impulso negli oscillatori. L'impiego di tale metodologia si rivela più veloce e semplice da implementare rispetto a quella tradizionale.

Acknowledgement

I am indebted to Andrea Bonfanti, who served as a second de facto advisor. The theory and the test chips presented in this thesis were developed under his constant guidance.

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List of abbreviations

2G second generation 1

4G fourth generation 1

AGC automatic gain control 7

AM amplitude modulation 6, 8, 9, 20, 36, 38–41, 43, 44, 46, 48, 49, 52, 95, 105, 107, 119, 122, 125–127, 137–141, 143, 147, 150, 153–155, 161, 166

BER bit error rate 2

BiCMOS bipolar complementary metal-oxide-semiconductor 1, 2

BSIM Berkeley Short-channel IGFET Model 23, 24, 32, 33, 57–59, 75, 96, 150, 151, 160, 162, 167

CAD computer-aided design 85

CM-PM common mode voltage to phase modulation 46

CMOS complementary metal-oxide-semiconductor 1, 2, 5, 9, 21, 41, 46, 54, 55, 57, 73, 83, 93, 96, 105, 110, 117, 120, 142, 154, 159

EDGE enhanced data rates for GSM evolution 1

FCW frequency control word 107, 110–112, 115, 165

FM frequency modulation 9, 11, 38, 41, 43, 44, 139, 140, 143, 154, 155

FoM figure of merit 75, 79, 81–83, 128, 141

GR generation-recombination 147

GSM global system for mobile communications 1, 3

ISF impulse sensitivity function 7, 8, 16–18, 29–31, 33, 35, 36, 38, 39, 49, 50, 52, 56, 60, 62–64, 70, 72, 73, 83, 86, 88, 89, 91–96, 98–103, 117, 122, 139, 154, 161–164

ITRS International Technology Roadmap of Semiconductor 4

LTE long term evolution 1

LTV linear time-variant 9, 14, 86

MIM metal-insulator-metal 74, 107, 142

MIMO multiple-input and multiple-output 14

MOS metal-oxide-semiconductor 2, 4, 5, 44, 74, 96, 143, 159

MOSFET MOS field-effect transistor 4, 6, 8, 30, 32, 37, 43, 49, 50, 54, 55, 68–70, 73, 74, 79, 83, 96, 102, 108, 120, 122, 127–129, 139, 149, 154, 163–165

NMF noise modulating function 32, 35, 67, 72, 92, 100, 111, 117, 120, 125, 145–147, 154

NMOS n-channel MOS 20–22, 34, 35, 37, 38, 41, 49, 51, 55, 57, 68, 69, 71, 80, 163

PLL phase-locked loop 2–5, 159

PM phase modulation 6, 8, 11, 20, 36–41, 46, 48, 49, 52, 81, 95, 105, 107, 119, 122, 123, 127, 137–139, 141, 143, 147, 150, 153, 154, 161, 166

PMOS p-channel MOS 20–22, 34, 35, 37, 41, 49, 51, 55, 57, 69, 71, 80, 93, 95, 107, 163, 164

PNOISE periodic noise 49, 70, 100, 150, 163

PSD power spectral density 4, 5, 12, 101, 159

PSS periodic steady-state 27, 41, 64, 91, 96, 130, 131, 166

PXF periodic transfer function 64, 86, 88, 89, 91, 93–98, 103, 164

RF radio-frequency 1, 64, 88, 120, 146, 147, 149, 150

RFIC radio-frequency integrated circuit 1, 2

RMS root mean square 4, 73, 98

SFDR spurious-free dynamic range 11, 12

SiGe silicon germanium 1

SOI silicon-on-insulator 1

SSCR single-sideband-to-carrier ratio 3–5, 12, 22, 49, 56, 102, 110–113, 121, 127, 128, 143–145, 147, 148, 150, 151, 159, 161, 165, 167, 168

TCW transconductance control word 107, 110, 111

THD total harmonic distortion 22, 27–29, 123, 124, 160

VCO voltage-controlled oscillator 2–7, 21, 23, 35, 45, 46, 54, 73–77, 79–83, 95, 110, 115, 116, 121, 154, 159–161, 163, 165

Contents

CHAPTER 1

Introduction and background

1.1 Introduction

The world cell phones market experienced a steady growth in latest years, driven by the increasing number of applications available on smartphones and tablet computers. Today's portable devices integrate multiple communication capabilities with ever-increasing data transfer rates. In particular, they have to support cellular standards from second generation (2G), namely global system for mobile communications (GSM) and enhanced data rates for GSM evolution (EDGE), to fourth generation (4G) long term evolution (LTE) together with the WiFi/WiMAX connectivity. In this scenario, the implementation of single-chip radio-frequency (RF) transceivers capable of operating over multiple standards is of great interest.

The need for a higher integration level to reduce board size and cost led complementary metal-oxide-semiconductor (CMOS) processes to fast become the technology of choice in radio-frequency integrated circuit (RFIC) development. In the not-too-distant past, bipolar complementary metal-oxide-semiconductor (BiCMOS) process technologies, such as silicon germanium (SiGe) and silicon-on-insulator (SOI), were more suitable for ana-

log and RFIC design than CMOS. This transition is driven primarily by the fact that CMOS processes are less expensive and more conducive to large-scale integration than BiCMOS. To take full advantage of the switching characteristics of metal-oxide-semiconductor (MOS) transistors in CMOS, a digital approach started to be adopted in the RFIC design. The analog section of transceivers, however, must cope with the limitations imposed by the adoption of scaled CMOS processes. One of these limitations is the increasing flicker noise corner frequency of minimum channel-length transistors [1]. This can lead to a severe degradation of the spectral purity of LC-tuned voltage-controlled oscillators (VCOs), which in turn also affects the frequency synthesizers for signal (de)modulation, eventually impairing the overall bit error rate (BER) of the communication system.

In the next section, a numerical example of the impact of technology scaling on the output phase jitter [2] of a 2.5-GHz phase-locked loop (PLL) is presented to give some reference numbers.

Standard	Frequency band [MHz]	Phase noise [dBc/Hz]
GSM 900/1800	880-960 1710-1880	-122 @ 0.6 MHz -132 @ 1.6 MHz -139 @ 3 MHz
UMTS	1920-2170 1900-2025	-132 @ 3 MHz -132 @ 10 MHz -144 @ 15 MHz
Bluetooth	2402-2480	-84 @ 1 MHz -114 @ 2 MHz -129 @ 3 MHz
WiFi	2412-2472 5150-5350 5470-5825	-102 @ 1 MHz -125 @ 25 MHz
WiMAX	2300-2400 2305-2320 2469-2690 3300-3400 3400-3800	Phase jitter $< 1^\circ$ rms

Table 1.1: *Operating carrier frequencies and phase noise requirements of major wireless communication standards.*

Table 1.1 reports the operating frequencies and the phase noise specifications of major communication standards, the former spanning from

800 MHz to nearly 6 GHz. A brief review of the concepts of phase noise and jitter in oscillators can be found in Section 1.5. Even if the most stringent phase noise requirements are dictated by the GSM and WiMAX standards, the design of voltage-controlled oscillators is still a challenging issue due to the need for broad intervals of frequency to be synthesized. This requirement further exacerbates the impact of flicker noise, because it generally leads to a non-optimum sizing of the active devices of the oscillator, as it will be more clear in Chapters 2 and 6.

1.2 The impact of scaling on phase jitter in frequency synthesizers

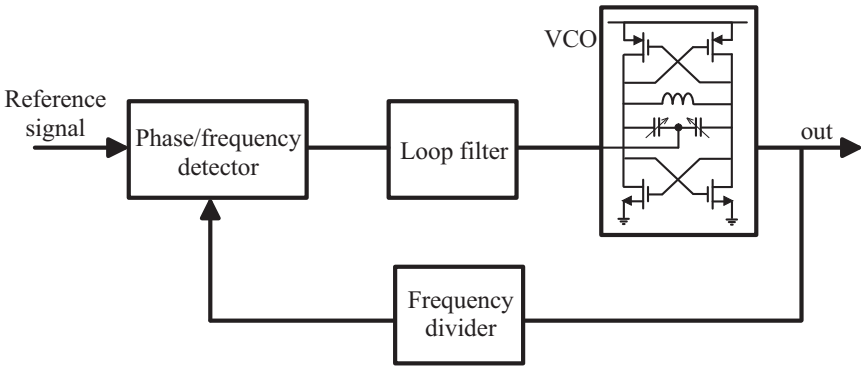


Figure 1.1: *Simple PLL block model, where the VCO is implemented in a voltage-biased topology.*

Consider the simple block model of a PLL in Fig. 1.1, where the VCO is implemented in a voltage-biased topology and is the only noisy block of the system. In this case, a type-II third-order PLL is considered, its bandwidth being set equal to 500 kHz. Fig. 1.2(a) plots the magnitude of the loop gain $G_{loop}(s)$ (solid line) and of the transfer function of VCO phase noise to output (dash-dotted line), given by $\left|(1 - G_{loop})^{-1}\right|$. The feedback provides a high-pass filtering action on the VCO noise that is transferred the output node out, implying that most of the close-in phase noise of the oscillator is suppressed. However, since the PLL bandwidth is typically in the 100-to-500-kHz range to minimize the noise contributions of charge-pump, reference, and Σ-Δ modulator [3, 4], its output phase jitter is still dominated by the oscillator phase noise. A comparison between the phase noise of free-running and phase-locked oscillator, quoted as single-sideband-to-

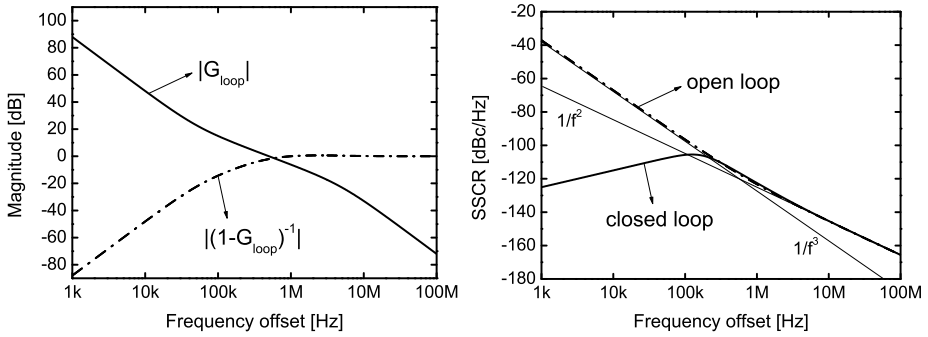


Figure 1.2: *(a) Magnitude of loop gain $G_{loop}(s)$ (solid line) and of transfer function of VCO noise to output (dash-dotted line). (b) SSCR at PLL output (solid line) and SSCR of the free-running oscillator (dash-dotted line) for $L_{min} = 65$ nm.*

carrier ratio (SSCR) [5], is shown in Fig. 1.2(b).

The VCO has been designed with minimum-length transistors to achieve a large tuning range, while the other parameters were set to typical reference values: excess gain [6] of 2.5, tank quality factor $Q = 10$, and tank capacitance $C = 1$ pF. The flicker noise of oscillator MOS field-effect transistors (MOSFETs) has been scaled as reported by the International Technology Roadmap of Semiconductor (ITRS) [7]. Figure 1.3 shows the gate-referred power spectral density (PSD) of flicker noise of a minimum-area MOS transistor as a function of technology node. The PSD has been normalized to a L_{min}^2 gate area and a 1-Hz frequency.

By means of Leeson's formula [8] and of (2.65) that will be derived in Chapter 2, it is possible to compute the phase noise induced by thermal and flicker noise, respectively. The corresponding root mean square (RMS) phase jitter contributions at the PLL output have been then obtained by integrating phase noise over the frequency bandwidth between 1 kHz and 100 MHz. The two contributions are plotted in Fig. 1.4 as function of the technology node.

Below a minimum length of 90 nm, the output phase jitter is mostly due to flicker noise. For instance, in the 65-nm case, the $1/f^3$- and $1/f^2$-shaped phase noise cross at a corner frequency equal to 600 kHz. Even if the PLL bandwidth is set to about the same value, the high-pass filtering action of the loop does not provide an effective reduction of the flicker-induced phase noise, its contribution to the output jitter being larger than the one due to

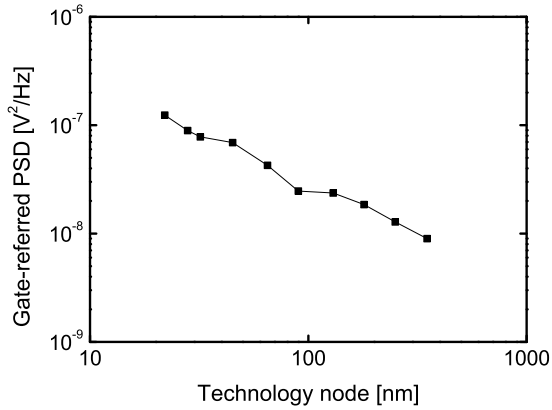


Figure 1.3: *Gate-referred power spectral density of flicker noise of a minimum-area MOS transistor as a function of technology node. The PSD has been normalized to a L_{min}^2 area and a 1-Hz frequency.*

white noise [9]. The SSCR at the PLL output and the SSCR of the free-running oscillator in a 65-nm CMOS process are shown in Fig. 1.2(b) as solid and dash-dotted line, respectively.

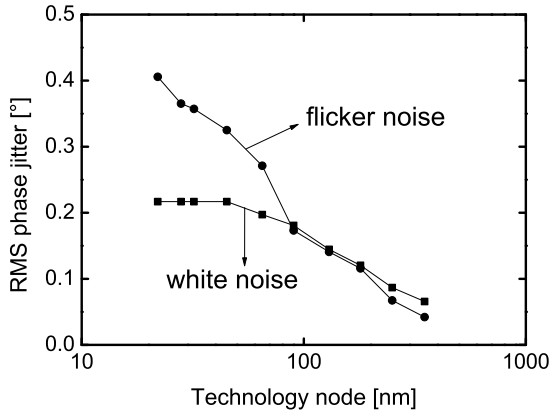


Figure 1.4: *Dependence on technology node of the integral phase noise expected from a 2.5-GHz PLL with a 500-kHz bandwidth. In the VCO design, a voltage-biased topology with minimum-length planar bulk CMOS transistors has been adopted.*

1.3 Review of technical literature

In the last decades, extensive efforts have been devoted to understanding and minimizing mechanisms of flicker noise up-conversion [10–36]. Four

major up-conversion mechanisms have been identified so far, namely:

1. conversion of amplitude modulation (AM)-to-phase modulation (PM) due to non-linear varactors [11–13, 15];
2. modulation of the current flowing through the tail capacitance in a current-biased VCO topology [16, 19, 30, 36];
3. modulation of parasitic capacitances of the transconductor stage [20, 21, 30]
4. modulation of the harmonic content of the output voltage waveform [17, 19, 22–28].

The first up-conversion mechanism has been well clarified and can be minimized by employing smaller analog varactors for a finer frequency tuning and a bank of digitally-controlled capacitors for a coarse tuning. This can drastically reduce the AM-to-PM conversion due to the non-linear capacitances, without impairing the overall VCO tuning range [32].

The second and third up-conversion mechanisms, on the contrary, have been investigated more from a qualitative perspective and a detailed quantitative explanation has not been given yet. Moreover, though being closely related to each other, they have been studied independently and no comparison has been provided showing which one of these two effects is dominant in current-biased oscillators. Since the up-conversion cause is the presence of a tail node oscillating at even harmonics, one possible solution is to resort to a voltage-biased topology [13, 32–34]. Another solution is the adoption of a tail LC resonant filter tuned at twice the oscillation frequency [29]. The main drawback of this technique is the non-negligible silicon real-estate needed to integrate the filter inductor. Moreover, since the efficiency of this technique is highly sensitive to the variation of oscillation frequency, a tuning mechanism is required. This introduces further noise, which can eventually impair the effectiveness of this solution, especially if the VCO has to cover a large frequency band.

The third mechanism started to be analyzed only in a few recent works [20, 21]. In those works, however, the effect of the modulation of parasitic capacitances was quantified by means of circuit simulations, taking into account only the parasitics of the MOSFET switching pair. Moreover, an explicit relationship with oscillator phase noise was not derived.

Regarding the last up-conversion mechanism, the concept that harmonic distortion may cause phase noise degradation in oscillators has been high-

lighted many times in literature. For example, Vittoz *et al.* [25], describing the adoption of an automatic gain control (AGC) circuit in a crystal oscillator, state that non-linearity has a "devastating effect on stability" and propose "to limit the amplitude of oscillation" to reduce the effect of distortion. The same idea can be found in the work of Gavra and Ermolenko [26] and Margarit [24], where the authors adopt an AGC loop to make possible a quasi-linear operation of the VCO, thus reducing harmonic distortion and improving phase noise performance.

Among most recent papers, Jerng and Sodini [22] propose to reduce the device width of the differential-pair transistors in a current-biased oscillator to increase the overdrive voltage and to extend the linear range of the switching devices. In this way the harmonic distortion is reduced with benefits in terms of phase noise arising from both the switching pair and the flicker noise up-conversion of the bias current. These authors refer to the effect as a form of "indirect frequency modulation". Another solution has been presented where damping resistors are placed at the source side of the differential pair transistors in order to linearize the transconductor and to suppress $1/f$ noise up-conversion [23]. This solution reduces harmonic generation and therefore the Groszkowski effect but at the expenses of excess gain and start-up margin.

1.4 Scope of this thesis

The main purpose of this doctoral dissertation is to provide a detailed quantitative analysis of the up-conversion mechanisms discussed in Section 1.3 and to take into account for the first time the cyclostationary flicker noise, thus filling the gap towards a complete understanding of this phenomenon. In particular, it will be shown that the harmonic distortion is the major $1/f^3$ phase noise source in voltage-biased oscillator topologies, while the modulation of parasitics is the dominant effect in the current-biased counterparts.

A detailed analysis is carried out basing on the model of Hajimiri and Lee [37,38], since it provides an acceptable trade-off between accuracy and complexity. By means the concept of ISF it is possible:

- to account for the non-stationary nature of noise sources
- to derive closed-form expressions which describe how the phase noise generation mechanism acts

The latter point, in particular, helps gaining insights into up-conversion

phenomena from a circuit designer perspective [39–41]. A review of the two most important models of phase noise oscillators can be found in Section 1.6.

Basing on the theoretical results, several techniques to mitigate or suppress the flicker noise up-conversion are presented, together with measurements results carried out on three different test chips which confirm the validity of the proposed analyses. Furthermore, a new accurate simulation technique to compute the ISF in oscillators is presented, which is easier and faster to be implemented with respect to the traditional method.

The thesis is organized as follows.

Chapter 2 is devoted to the analysis of the flicker noise up-conversion mechanisms in voltage-biased LC oscillators. A quantitative model based on the framework of Hajimiri's impulse sensitivity function is provided and is validated against circuit simulations. It will be shown that the flicker noise up-conversion is mainly due to the distortion generated by the active element. A closed-form expression of $1/f^3$ phase noise is derived which accurately matches simulations, also providing quantitative links to key design parameters of the oscillator. In particular, it will be demonstrated that two mechanisms play a fundamental role in the conversion of flicker noise into phase noise: i) the direct injection into the tank of PM tones since the current flowing through active devices lags with respect to the voltage and ii) an AM-to-PM conversion effect due to the dependence of the oscillation frequency on the harmonic content of the output voltage. It will be highlighted that flicker noise up-conversion is reduced in case of low excess gain, which translates into low distortion of the voltage output, and high tank quality factor (for a fixed excess gain), providing a strong attenuation of higher-order harmonics.

Chapter 3 is dedicated to the analysis of an alternative topology which is able to suppress the flicker noise up-conversion. The insertion of resistors in series to the drain nodes of the transistors allows the circuit to reach remarkable phase noise reduction, avoiding the adoption of resonant LC filters and the corresponding area penalty. Moreover, since the resistors are at the MOSFET drains, the start-up margin is not degraded. A quantitative framework is introduced to explain the peculiar up-conversion mitigation reached in the circuit by properly tailoring the resistor values.

In **Chapter 4**, a fast and accurate simulation technique to evaluate the impulse sensitivity function of an oscillator is presented. The knowledge of the impulse sensitivity function allows the designer not only to calculate

the phase noise arising from a specific noise source, but also to gain insight in the phase-noise generation mechanisms. However, despite its usefulness in circuit design, commercially-available circuit simulators do not yet automatically calculate the impulse sensitivity function, which needs instead to be determined via repeated transient analyses. The proposed method, based on the linear time-variant (LTV) analysis of oscillators, computes the impulse phase response by means of periodic steady-state and periodic transfer function simulations available in commercial simulators (Spectre, Eldo, etc.). This technique overwhelms the traditional simulation method in terms of both speed and precision and can be easily extended in order to compute also the noise modulating function and the phase noise induced from cyclostationary noise sources.

In **Chapter 5**, a wide-band voltage-biased oscillator is presented where the excess gain value is kept low as the frequency spans between 1.6 and 2.6 GHz by adopting a segmented transconductor. Such a technique breaks the conflicting link between tuning range and $1/f^3$ phase-noise performance. The circuit, fabricated in a 65-nm CMOS technology, demonstrates a reduction of 10 dB of the flicker noise up-conversion over a 47% tuning range without impairing the $1/f^2$ phase noise performance. Moreover, measurement results are in good agreement with simulations, thus proving the validity of the phase noise generation model adopted.

In **Chapter 6**, flicker noise up-conversion mechanisms in current-biased oscillators are discussed and clarified. In particular, it is shown that the $1/f^3$ phase noise is mostly due a conversion of amplitude modulation to frequency modulation (FM) due to the presence of non-linear parasitic capacitances of the transconductor stage. A quantitative insight into this phenomenon is carried out, highlighting that the amplitude-to-frequency sensitivity term associated to the tail capacitance is the dominant contribution to the overall sensitivity. The impact of the tail capacitance is further investigated, pointing out its dependence on oscillation amplitude and width of switching transistors. In particular, it is clarified why the AM-to-FM sensitivity is null for a particular value of bias current, which can be adjusted by the circuit designer adopting a sufficiently-small transistors width.

In **Chapter 7**, the validity of the phase noise analysis presented in Chapter 6 is verified by means of measurements carried out on a few test chips. Two current-biased oscillators have been fabricated on the same die with different size of the transistors of the differential pair. Measurements results confirms a reduction of flicker noise up-conversion of about 7 dB in

case of smaller width with no impairment of the $1/f^2$ phase noise. A further investigation will also be carried out in order to explain the discrepancy between measured and simulated values of $1/f^3$ phase noise. A revised model of flicker noise up-conversion is proposed, which captures the effect of partial correlation between noise side-bands by taking into account the non-instantaneous response of noise to variation of bias conditions.

Finally, in **Chapter 8**, a summary of conclusions and original contribution of this thesis is provided.

1.5 Review of the concepts of phase noise and jitter

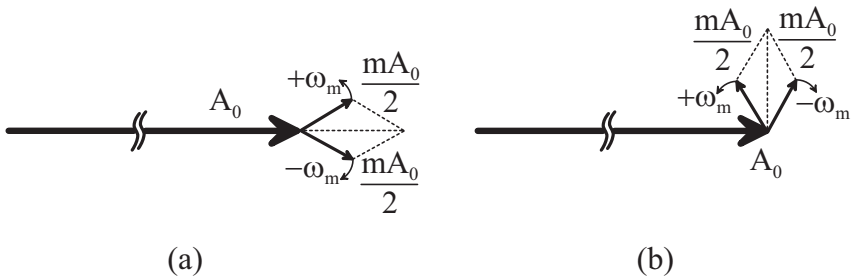


Figure 1.5: *Phasor representation of (a) amplitude-modulated carrier and (b) phase-modulated carrier.*

Ideally, an oscillator generates a sinusoidal or harmonic signal $V(t) = A_0 \cos(\omega_0 t + \phi_0)$, where A_0, ω_0 and ϕ_0 are the oscillation amplitude, angular frequency and initial phase, respectively, and are constant over the time. In an actual oscillator, however, due to the unavoidable presence of noise sources, these quantities become modulated and, thus, time-dependent. In case of amplitude modulation, the oscillator output voltage becomes:

$$V(t) = A_0 [1 + m \cdot \cos(\omega_m t)] \cos(\omega_0 t + \phi_0),$$

where typically $m \ll 1$ and $\omega_m \ll \omega_0$. The output spectrum now consists of a Dirac Delta function at ω_0 and a couple of side-tones at angular frequencies $\omega_0 \pm \omega_m$. A phasor representation of the amplitude-modulated carrier is shown in Fig. 1.5(a).

In case of frequency modulation, on the other hand, the frequency can be written as: $\omega(t) = \omega_0 + \omega_m(t)$. Since the phase is the integral of the frequency, the output signal can be written as:

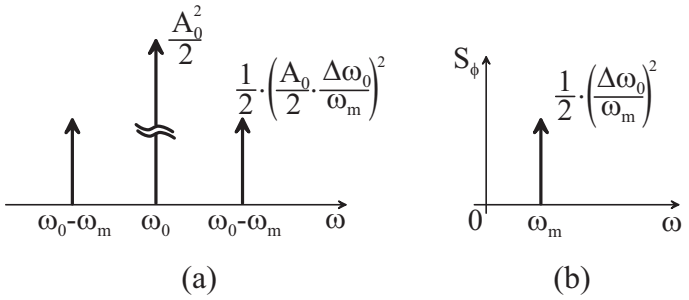


Figure 1.6: *Frequency spectra of the modulated output voltage $V(t)$ (a) and of the modulated phase $\Delta\phi(t)$ (b).*

$$V(t) = A_0 \cos\left[\omega_0 t + \phi_0 + \tfrac{\Delta\omega_0}{\omega_m} \sin(\omega_m t)\right].$$

A corresponding phase modulation also occurs in this case, with modulation index $m = \frac{\Delta\omega_0}{\omega_m}$. The resulting phase is:

$$\phi(t) = \Delta\phi \cdot \sin(\omega_m t), \tag{1.1}$$

where $\Delta\phi = \frac{\Delta\omega_0}{\omega_m}$. If the following inequality holds:

$$\Delta\phi \ll 1\,\text{rad}, \tag{1.2}$$

which is the case of small-angle modulation ("narrow-band" FM), the signal $V(t)$ can be approximated as:

$$\begin{aligned} V(t) &\cong A_0 \cos(\omega_0 t + \phi_0) - A_0 \sin(\omega_0 t + \phi_0) \cdot \frac{\Delta\omega_0}{\omega_m} \sin(\omega_m t) \\ &= A_0 \cos(\omega_0 t + \phi_0) - \frac{A_0}{2} \cdot \frac{\Delta\omega_0}{\omega_m} \cos[(\omega_0 - \omega_m) t] \\ &- \frac{A_0}{2} \cdot \frac{\Delta\omega_0}{\omega_m} \cos[(\omega_0 + \omega_m) t]. \end{aligned}$$

A phasor representation of the two PM side-tones is visible in Fig. 1.5(b), while the spectrum of the modulated output signal is shown in Fig. 1.6(a).

The ratio between the power of each side-tone and the power of the carrier is denoted as spurious-free dynamic range (SFDR) and is given by:

$$SFDR = \frac{\frac{1}{2}\left(\cdot\frac{A_0}{2} \cdot \frac{\Delta\omega_0}{\omega_m}\right)^2}{\frac{A_0^2}{2}} = \frac{1}{4} \cdot \left(\frac{\Delta\omega_0}{\omega_m}\right)^2 = \left(\frac{\Delta\phi}{2}\right)^2, \tag{1.3}$$

It is interesting to note that the SFDR is equal to half the power of the modulated phase $\phi(t)$, whose spectrum, S_ϕ, is depicted in Fig. 1.6(b). The SFDR is usually expressed in dBc, i.e. dB with respect to the carrier.

An undesired phase modulation can also occur due to the presence of a noise source whose power spreads over a certain frequency interval. The phase perturbations induced by noise sources are referred to as "phase noise". Since S_ϕ is inversely proportional to the square of the frequency offset ω_m, it exhibits a $1/\omega_m^2$ tail (-20 dB/decade slope) in case of white noise, while a $1/\omega_m^3$ dependence (-30 dB/decade slope) arises in presence of $1/f$ noise. Such a spectrum of $\phi(t)$ is shown in Fig. 1.7(a).

Similarly to the previous case of sinusoidal modulation, the corresponding spectrum of the output voltage is a scaled replica of S_ϕ folded around both sides of the carrier, as depicted in Fig. 1.7(b). This assumption is valid if (1.2) holds. The power spectral density at $\omega_0 \pm \omega_m$ of the output voltage is given by $S_V(\omega_0 \pm \omega_m) \cong \frac{S_\phi(\omega_m)}{2} \cdot \frac{A_0^2}{2}$. The noise level is now expressed by the ratio between the noise power in a 1-Hz bandwidth at offset ω_m and the power of the carrier. This figure quantifying the amount of phase noise is defined single-sideband-to-carrier ratio (SSCR) and can be also denoted with $\mathcal{L}$:

$$SSCR(\omega_m) = \frac{S_V(\omega_0 \pm \omega_m)}{A_0^2/2} \cong \frac{S_\phi(\omega_m)}{2} \text{ [dBc/Hz]}. \tag{1.4}$$

Clearly, an equivalence between the SSCR and the SFDR can be found once $\Delta\phi$ in (1.3) is set equal to:

$$\Delta\phi = \sqrt{2S_\phi(\omega_m) \cdot 1\,\text{Hz}}, \tag{1.5}$$

i.e. if the power of the sinusoid in (1.1) is equal to the noise PSD integrated over a 1-Hz bandwidth.

It it worth noting that while the power spectrum of the phase, S_ϕ, diverges to ∞ at zero offset frequency, the spectrum of the output voltage, S_V, does not. This is because the small-angle approximation in (1.2) is no longer valid as ω_m approaches zero. As a result, if only white noise is considered, the voltage spectrum tapers off with a Lorentzian shape and its integral is equal to the power of the ideal carrier [42].

However, in practical applications it is sometimes more useful to provide a characterization of the phase/time deviation (also referred to as "jitter") rather than the voltage spectrum. Hence, it necessary to overcome the difficulty arising due to S_ϕ approaching ∞. Demir *et al.* show that in case

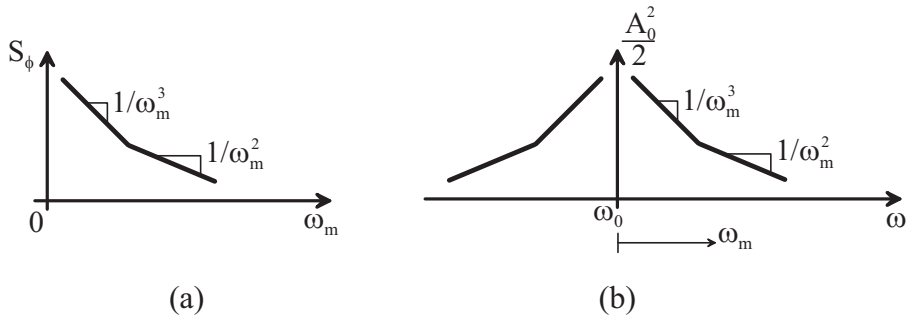


Figure 1.7: *Phase (a) and voltage (b) spectrum of an actual oscillator.*

of white noise the phase deviation becomes a Gaussian random variable with a variance that linearly increases with the observation time T [43], . A simple proof can be given by taking $S_\phi(\omega_m) = \frac{c}{\omega_m^2}$, where c is a constant:

$$\Delta\phi_{rms}^2 = \int_{\omega_{min}=\frac{1}{T}}^{\infty} S_{\phi(\omega_m)}\, d\omega_m = \int_{\omega_{min}=\frac{1}{T}}^{\infty} \frac{c}{\omega_m^2}\, d\omega_m = cT.$$

The jitter expressed as time deviation is simply given by $\frac{\Delta\phi_{rms}}{\omega_0}$. Thus, one of the possible solution for jitter calculation [9], which is commonly used in practice, is excluding the interval of frequencies below a minimum value f_{min} from the integral. The value of f_{min} is dictated by the duration of observation or by the speed of the phase-correction algorithm.

1.6 Review of oscillator phase noise models

In the last two decades, an intense research has been carried out by many authors on oscillator phase noise. Different models have been proposed for the description of this phenomenon, which are far more complex than the Leeson's empirical formulation [8]. In particular, two major frameworks have been developed and implemented by widely-used circuit simulators, namely:

- Hajimiri's model, based on the so-called impulse sensitivity function
- Demir's model, based on decomposition of perturbations into phase- and orbital-deviation components

In the following, the two models will be briefly reviewed, highlighting their strengths and weaknesses.

1.6.1 Hajimiri's model

This model was first presented in the form of a general theory for phase noise in electrical oscillators [37]. It is a LTV model that describes the oscillating circuit as a multiple-input and multiple-output (MIMO) system. In particular, the inputs are the different noise sources, while the outputs are the oscillation amplitude, $A_0(t)$, and the oscillation phase, $\phi(t)$.

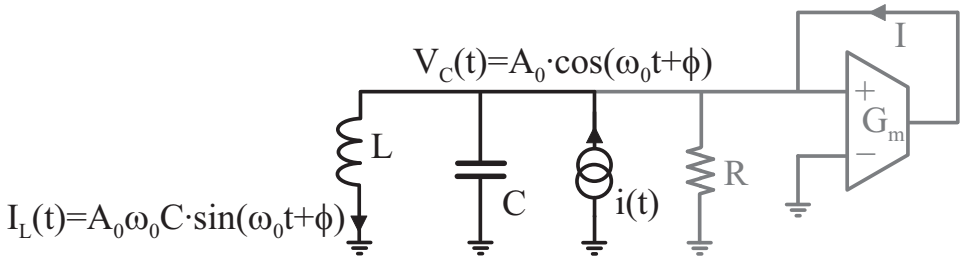


Figure 1.8: *Equivalent circuit of a LC oscillator.*

It is then possible to define two impulse response functions for each noise source, namely $h_{A_0}(t,\tau)$ and $h_\phi(t,\tau)$, the former being associated to amplitude perturbations, the latter to phase perturbations. The impulse response associated to A_0 is usually of little interest, since it tends to asymptotically fade with time due to the unavoidable presence of an amplitude-limiting mechanism of the oscillator amplifying stage. On the contrary, the impulse response associated to the phase, h_ϕ, is of greater interest and it is necessary to quantify the contribution of each noise source to the overall oscillator noise.

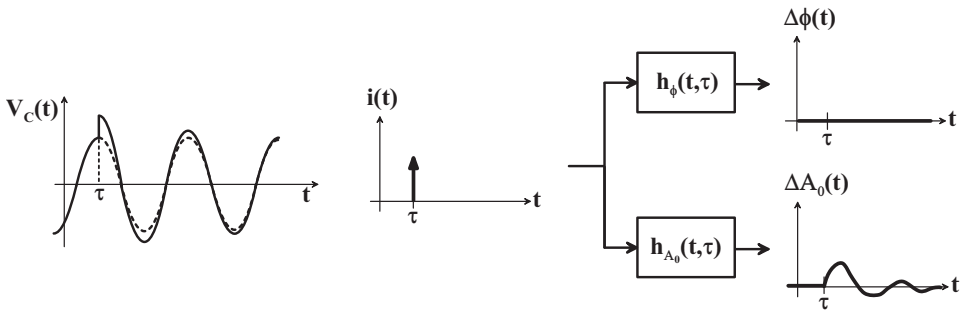


Figure 1.9: *Impulse response of oscillator output waveform to a charge pulse injected during the peak of the sinusoidal voltage across the tank capacitor. In this case, no phase perturbation occurs, while the amplitude variation is recovered in a few oscillation cycles.*

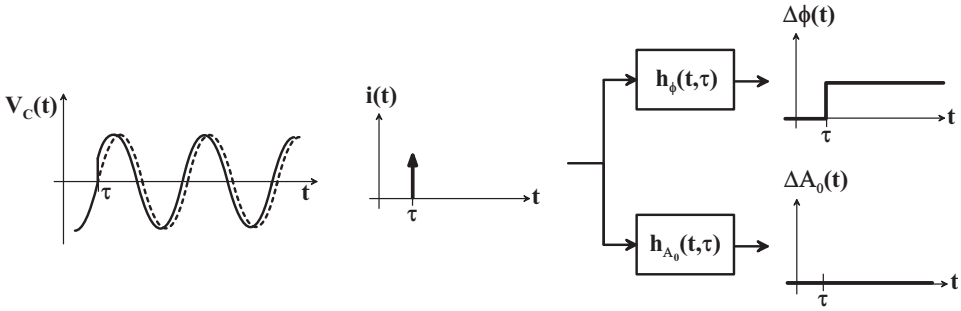


Figure 1.10: *Impulse response of oscillator output waveform to a charge pulse injected during the zero crossing of the sinusoidal voltage across the tank capacitor. In this case, the phase perturbation reaches its maximum value, while no amplitude variation is induced.*

Consider, as an example, a parallel LC resonating tank, shown in Fig. 1.8, the voltage across the capacitor and the current flowing through the inductor being given by $V_C(t) = A_0 \cos(\omega_0 t + \phi)$ and $I_L(t) = A_0 \omega_0 C \sin(\omega_0 t + \phi)$, respectively. The injection of a charge pulse $i(t) = \Delta q \cdot \delta(t - \tau)$ at time $t = \tau$ results into an instantaneous variation of the voltage across the tank equal to $\Delta V_C = \Delta q / C$. As shown in Fig. 1.9, if the charge pulse is injected at the peak of the voltage, no phase perturbation occurs and $h_\phi(t, \tau) = 0$. On the other hand, if the injection happens during the zero crossing, this situation being depicted in Fig. 1.10, the phase error reaches its maximum value, given by $\Delta\phi = \Delta q / q_{max}$, where $q_{max} = A_0 C$ is the maximum charge stored in the tank capacitor. Since the oscillator has no time references, such an induced phase error is permanent and cannot be recovered. On the contrary, the amplitude perturbation is progressively attenuated by the transconductor non-linearity.

The impulse phase response, $h_\phi = \Delta\phi / \Delta q$, is given by:

$$h_\phi(t, \tau) = \frac{\Gamma(\tau)}{A_0 C} \cdot u(t - \tau), \tag{1.6}$$

where $\Gamma(t)$ is the so-called impulse sensitivity function, taking into account the periodic dependence of the induced phase shift on the charge injection time, and $u(t)$ is the unity-step function. More in general, given a current disturbance $i_n(t)$ between two nodes, the corresponding phase perturbation $\Delta\phi(t)$ can be calculated by using (1.6), resulting:

$$\Delta\phi(t) = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\tau) i_n(\tau) \, \mathrm{d}\tau, \tag{1.7}$$

where q_{max} is the maximum charge across the capacitor placed between the nodes of interest.

Hajimiri's model is applicable to all classes of oscillators and can be further extended to take into account the cyclostationary nature of noise processes. This point will be discussed in Section 2.4.2. One of the limitation of the ISF-based approach is that it is not able to predict the Lorentzian shape of the oscillator output voltage, as this method fails when a sinusoidal perturbation is injected whose frequency is close enough to the oscillation frequency. As a consequence, Hajimiri's method is unable to capture injection-locking phenomena [44, 45].

1.6.2 Demir's model

The phase noise model proposed by Demir *et al.* adopts a non-linear perturbation analysis [43] that was first introduced by Kärtner [46]. Unlike Hajimiri's model, in the work by Demir the perturbation is not decomposed into phase and amplitude noise components. Instead, the perturbation is decomposed into a phase-deviation component and an additive component that Demir calls orbital deviation. According to the original notation, the unperturbed oscillation is described by a vector $x_s(t)$ consisting of the capacitor voltage and the inductor current. When an external noise injection occurs, the oscillator response is modified to $x_s(t+\alpha(t))+y(t)$, where $\alpha(t)$ is the time-dependent time shift or phase deviation and $y(t)$ is the orbital deviation. The main difference between $\alpha(t)$ and $y(t)$ is that while the former increases with time, even if the perturbation is small, the latter always remain small. To better clarify these concepts, it is useful to make use of a graphical representation in state-space or phase plane.

Figure 1.11 plots the current through the inductor against the voltage across the capacitor. The solid-line curve is the trajectory corresponding to the unperturbed state. In case of small perturbation, the trajectory changes with time but its points fall inside the region delimited by the two dashed lines. At a given time instant, the oscillator was at point A on the unperturbed trajectory. As a result of a disturbance, the state of the oscillator can be changed to point B. A third point, B', can be found on the unperturbed limit cycle such that the perturbation effect can be equivalently viewed as the combination of a phase shift α and a small additive component y.

By means of a complex mathematical description, featuring Floquet theory and stochastic differential equations, Demir is able to derive the statistical properties of both phase and orbital deviations and to compute

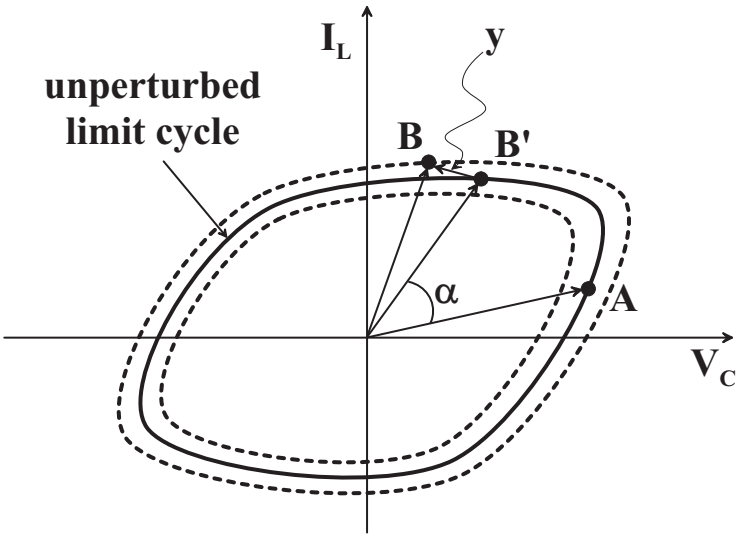


Figure 1.11: *Limit cycle and excursion due to perturbation.*

the output spectrum of the oscillator in case of white and colored noise sources [47]. The analysis starts from describing the oscillator by means of a set of differential equations in the form:

$$\dot{x} = f(x),$$

which is first numerically solved to find the unperturbed solution $x_s(t)$. The system is then linearized around the steady-state solution and a perturbation component $b(t)$ is added. After major elaborations, the differential equation describing the behaviour of the phase deviation α is derived as:

$$\frac{d\alpha}{dt} = v_1^T \left[t + \alpha(t)\right] B \left[x_s \left(t + \alpha(t)\right)\right] b(t), \tag{1.8}$$

where $v_1^T(t)$ plays a similar role to Hajimiri's ISF and $B(t)$ is a function mapping the effect of the circuit time-variance onto the perturbation vector $b(t)$ [48]. It is worth noting that (1.8) is basically a more refined version of (1.7) rewritten in a differential form.

Demir's models is the most generic and accurate model and can be applicable to all classes of oscillators. A higher accuracy is achieved with respect to the ISF-based method since the dependence of v_1^T and B on the induced phase shift α is taken into account in (1.8). As a consequence, it correctly predicts the Lorentzian shape of the output spectrum, since it does not collapse in case the frequency of the perturbation approaches the

frequency of oscillation. On the other hand, the main drawback of this mathematical model is that it does not provide the circuit designer a physical insight into the phase noise generation mechanism.

CHAPTER 2

Flicker noise up-conversion in voltage-biased LC oscillators

2.1 Introduction

This chapter is devoted to the analysis of the flicker noise up-conversion mechanisms in voltage-biased LC oscillators. Quantitative results will be provided, showing that in this oscillator topology the $1/f^3$ phase noise arises due to modulation of the harmonic content of the output voltage.

The effect is known since 1933 when Janusz Groszkowski published his pioneering work on frequency stability in oscillators [49]. Groszkowski found that the steady-state oscillation frequency does not perfectly match the resonance frequency of the tank. Since the active element drives the tank with a non-harmonic current signal, a frequency shift of the oscillation frequency arises. The shift is needed to guarantee that the average reactive power delivered to the resonant tank in the oscillation period is zero. In fact, the high-frequency harmonics of the current signal flow into the tank capacitor, which is a low-impedance load on the high-frequency side of the resonance, delivering a net capacitive reactive power. The first harmonic of

the current should therefore lag the voltage in order to deliver the inductive power needed to keep the balance. In [49], the oscillation frequency was found to be:

$$\omega_0^2 = \omega_R^2 \cdot \frac{\sum_{k=1}^{+\infty} V_k^2}{\sum_{k=1}^{+\infty} k^2 \cdot V_k^2}, \tag{2.1}$$

where $\omega_R/(2\pi)$ is the tank resonance frequency and V_k is the amplitude of the *k*-th voltage harmonic. According to (2.1), any time noise modulates the amplitude of the voltage harmonics, a frequency modulation is generated, ultimately resulting into phase noise.

Despite distortion has been always considered a fundamental cause of phase noise generation, only recently Bevilacqua and Andreani [27, 28] started to develop quantitative frameworks by studying the $1/f$ noise up-conversion of the bias current due to non-linearity in both Colpitts and differential-pair LC-tuned oscillators. Moving further along this investigation path, this chapter provides a quantitative analysis of the flicker noise up-conversion arising from the cross-coupled pair in a voltage-biased oscillator. For the first time a quantitative link between $1/f$ noise up-conversion and non-linearity is addressed taking also into account the cyclostationary nature of the noise sources.

2.2 The case study

Figure 2.1 shows a differential LC-tuned oscillator implementing a voltage-biased topology that has been taken as case study in this chapter. With respect to the well-known current-biased differential topology, the circuit does not feature a bias current generator, thus removing dominant contributions to both $1/f^2$ and $1/f^3$ phase noise [12, 50]. Moreover, the varactors have been replaced by a linear capacitor to avoid further AM-to-PM conversion. Since the topology has very few noise sources, it provides the proper environment to study the up-conversion mechanism only due to non-linearity of the switching active elements without the presence of other terms.

In designing the circuit, n-channel MOS (NMOS) and p-channel MOS (PMOS) transistors have been sized to set the output nodes to half the supply voltage. This choice maximizes the oscillation swing. By assuming

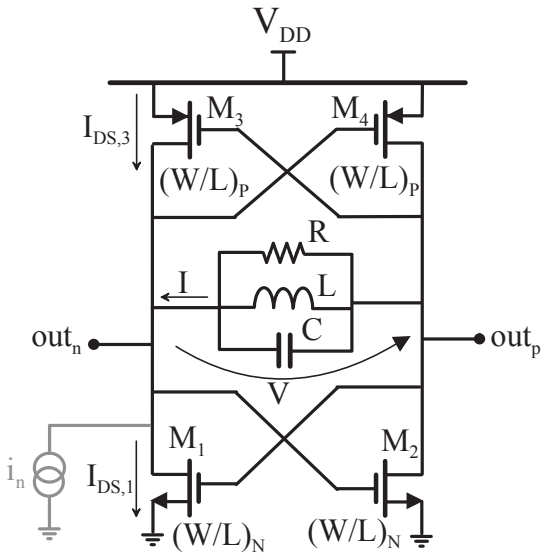


Figure 2.1: *Differential double cross-coupled oscillator implementing a voltage-biased VCO.*

the same threshold voltage for both types of transistor ($V_{TH,n} = |V_{TH,p}| = V_{TH}$), the condition leads to set the same transconductance for both NMOS and PMOS transistors, which translates into $W_p/W_n = \mu_n/\mu_p = 2.2$. In the following, the width W will always refer to the width of the NMOS transistors, while the width of the PMOS transistors will be always considered accordingly adjusted to retain the 2.2-ratio.

The circuit was simulated in a 65-nm CMOS technology with 1.2-V supply. The oscillator central frequency was set to $2\,$GHz by using a tank with $L = 1.2\,$nH, $C = 5.3\,$pF and a quality factor $Q = 10$ (i.e. $R = 150\,\Omega$). Once the tank has been sized, the only free parameter left to the designer is the small-signal loop gain, or excess gain [24, 51], defined as:

$$G_X = g_m \cdot R, \tag{2.2}$$

g_m being the small-signal transconductance of the double cross-coupled transconductor.

The excess gain is usually set between 2 and 4 to guarantee oscillator start-up even in presence of process spread and variability of the tank quality factor [24]. In practice, when this topology is adopted to implement a VCO, the excess gain is set by choosing the transistors widths, while the lengths may be kept at the minimum value not to narrow the achievable

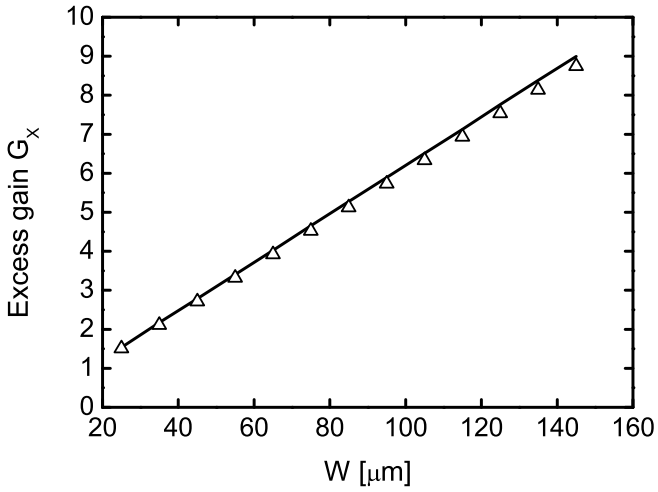


Figure 2.2: *Excess gain $G_X = g_m R$ as a function of transistor width. Triangles refer to g_m evaluated as in (2.3) and considering $\frac{\mu C'_{ox}}{L}\left(\frac{V_{DD}}{2} - V_{TH}\right) \cong 0.4\,mA/\left(V \cdot \mu m\right)$.*

tuning range. Assuming a square-law transistor characteristic and considering that at the start-up the overdrive voltage is $V_{DD}/2 - V_{TH}$, the overall transconductance is given by the sum of the NMOS and the PMOS pair transconductance, that is:

$$g_m = \frac{g_{m,n} + g_{m,p}}{2} \cong \mu C'_{ox} \left(\frac{W}{L}\right)_n \left(\frac{V_{DD}}{2} - V_{TH}\right). \qquad (2.3)$$

It follows that the excess gain varies linearly with the transistor width, as shown in Fig. 2.2. As W ranges from $25\,\mu$m to $145\,\mu$m, the excess gain spans from 1.5 to about 9. On the other hand, the larger the transistor width, the larger the excess gain and the higher the voltage harmonic distortion.

Figure 2.3 shows the simulated total harmonic distortion (THD) [51,52] of the differential output voltage, together with the oscillation frequency, as a function of the excess gain. By increasing the harmonic distortion of the output voltage, the oscillation frequency shifts down with respect to the resonance frequency, in agreement with the Groszkowski effect. In Fig. 2.3 triangles refer to the estimate derived from (2.1), having care to take into account also the slight dependence of the resonance frequency on transistor width due to the variations of the gate and drain parasitic capacitances.

Let us now consider the phase noise of the circuit, quoted as SSCR in the following. Figure 2.4 shows the dependence of the $1/f^2$ and the $1/f^3$ phase noise on the excess gain, G_X, evaluated at $10\,$MHz and $1\,$kHz, re-

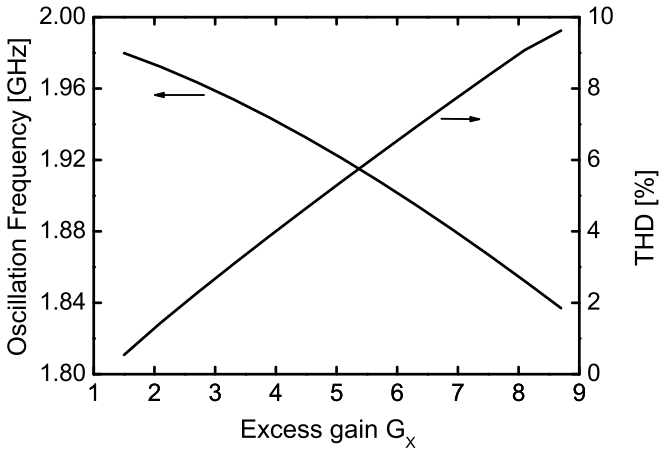


Figure 2.3: *Oscillation frequency and total harmonic distortion for the VCO in Fig. 2.1 varying the excess gain G_X.*

spectively. While at 10-MHz frequency offset the phase noise is dominated by contributions of the stationary noise source (i.e. the tank loss resistance) and of the cyclostationary white noise sources of the transistors, at 1-kHz offset their contributions are negligible, independently of the excess gain, thus making possible to isolate the term due to flicker noise up-conversion. Results using both Berkeley Short-channel IGFET Model (BSIM) and SPICE2 flicker noise model are shown in Fig. 2.4(b).

It turns out that the larger the transistors and thus the excess gain G_X, the higher both $1/f^2$ and $1/f^3$ phase noise contributions. Now the question is whether the rise of the phase noise is due to an increase of noise sources intensity and/or to an increasing efficiency of folding and conversion mechanisms pumping up noise within the oscillator bandwidth.

As far as the $1/f^2$ phase noise is considered, its dependence on G_X has been ascribed to the increasing loading effect provided by the transistors to the tank. As their width gets larger, the devices operate in the linear region for a larger portion of the oscillation cycle, loading the resonator and leading to "a degradation of the resonator quality factor" [53]. In other terms, the rise of the $1/f^2$ phase noise is mainly ascribed to an increase of the noise power. On the other hand, the steeper rise ($+20$ dB in Fig. 2.4(b)) of the $1/f^3$ phase noise has been so far qualitatively attributed to the growing oscillator non-linearity [22]. The aim of the following sections will be to provide a quantitative justification of this idea.

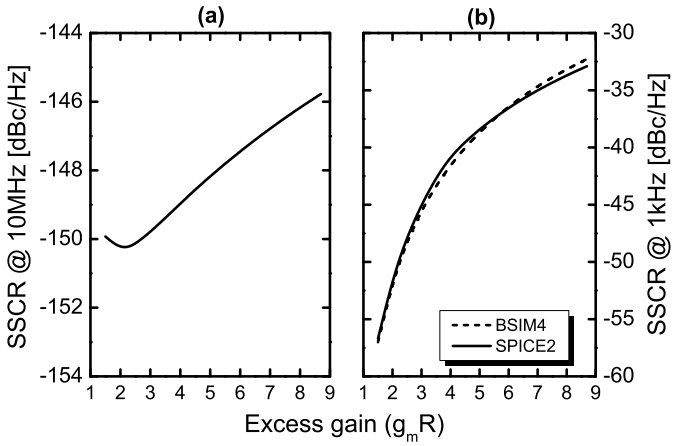


Figure 2.4: *Phase noise at* 10*-MHz (a) and* 1*-kHz (b) frequency offset as a function of the excess gain* G_X*.* $1/f^3$ *phase noise at* 1 *kHz was evaluated adopting both BSIM and SPICE2 flicker noise model.*

2.3 Steady-state solution of Van der Pol oscillator

This section is devoted to the computation of the steady-state solution of the voltage-biased oscillator in Fig. 2.1 when no external perturbation is present. A simplified yet accurate analysis is carried out, deriving closed-form expressions for the main quantities of the circuit, which will later prove useful for calculating phase noise.

Any LC-tuned oscillator can be schematically represented as a LC tank with a loss resistor R and a non-linear transconductor providing the energy to balance, at steady state, its losses. This schematic representation is shown in Fig. 2.5. For the sake of simplicity, the analytic description of transconductor non-linearity is limited to a third-order polynomial function. Moreover, this function is odd due to the differential nature of the oscillator in Fig. 2.1. The I-V characteristic of the active stage is thus given by:

$$I(V) = g_1 V - g_3 V^3 \tag{2.4}$$

and the voltage-biased topology resorts to a Van der Pol oscillator [54]. In the following, it will shown that this approximation leads to accurate results.

In the circuit in Fig. 2.1, the transconductor is synthesized by means of a double cross-coupled pair. Its non-linear I-V curves are reported in Fig. 2.6 for two different values of the transistor width together with the fitting third-order polynomial curves. The first coefficient in (2.4), g_1, is

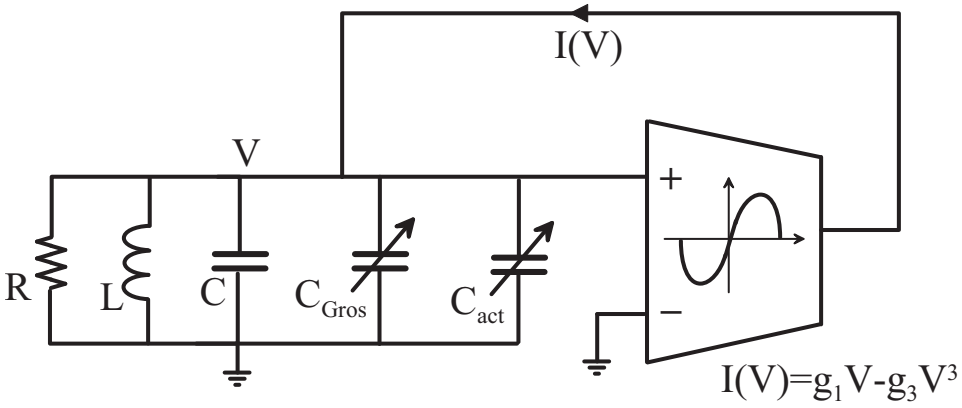


Figure 2.5: *Behavioral model of a voltage-biased oscillator.*

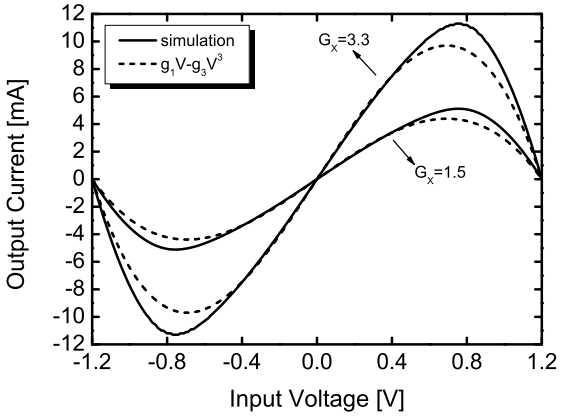


Figure 2.6: *I-V characteristic of the double cross-coupled pair LC oscillator sketched in Fig. 2.1 for $G_X = 1.5$ ($W = 25\ \mu m$) and $G_X = 3.3$ ($W = 55\ \mu m$). Dashed lines refer to third-order polynomial approximations.*

the small-signal transconductance at DC, that is $g_1 = g_m$. It can be also shown that $g_3 = g_m/V_{DD}^2$.

In order to simplify the analysis, let us consider only the first and third harmonic of output voltage. The voltage waveform will therefore be taken as:

$$V(t) \cong \underbrace{A_1 \cos(\omega_0 t)}_{V_1(t)} - \underbrace{A_3 \sin(3\omega_0 t)}_{V_3(t)}, \tag{2.5}$$

where A_1 and A_3 are both positive. The phase relationship between V_1 and V_3 will be justified in the following. Starting from (2.5), the output current of the transconductor at the fundamental frequency is computed as:

$$I_1(t) \cong \underbrace{\left[g_1 A_1 - \frac{3}{4} g_3 A_1^3\right]}_{I_1^I} \cos(\omega_0 t) + \underbrace{\left[\frac{3}{4} g_3 A_1^2 A_3\right]}_{I_1^Q} \sin(\omega_0 t), \tag{2.6}$$

where I_1^I e I_1^Q are the in-phase and in-quadrature terms. Due to the presence of the I_1^Q component, a phase shift ϑ is generated between the phasors $\overrightarrow{I_1}$ and $\overrightarrow{V_1}$ associated to $I_1(t)$ and $V_1(t)$, respectively. More precisely, since the higher-order harmonics of the transconductor current mainly flow through the tank capacitor, which is a low-impedance path for such harmonics, it follows that the frequency of the fundamental harmonic must shift on the low-frequency inductive side of the resonance to cancel out their capacitive reactive power. The oscillation frequency ω_0 deviates from resonance, thus becoming:

$$\omega_0 = 1/\sqrt{LC} + \Delta\omega_0, \tag{2.7}$$

$\Delta\omega_0$ being negative. Balancing both the in-phase and in-quadrature currents of the resonant tank and of the transconductor at the fundamental frequency, we get:

$$\begin{cases} g_1 A_1 - \dfrac{3}{4} g_3 A_1^3 = \dfrac{A_1}{R} & (2.8) \\ \dfrac{3}{4} g_3 A_1^2 A_3 = \left(\dfrac{1}{\omega_0 L} - \omega_0 C\right) A_1. & (2.9) \end{cases}$$

The oscillation amplitude A_1 and the frequency deviation $\Delta\omega_0$ can be de-

rived from (2.8) and (2.9), respectively, as:

$$\begin{cases} A_1 = \sqrt{\frac{4}{3}\frac{(g_1 - 1/R)}{g_3}} = \sqrt{\frac{4}{3}\frac{(G_X - 1)}{g_3 R}} & (2.10) \\ \Delta\omega_0 \cong -\frac{3}{8}\frac{g_3 A_1 A_3}{C}, & (2.11) \end{cases}$$

the latter being derived by means of the approximation $1-\omega_0^2 LC \cong -2\frac{\Delta\omega_0}{\omega_0}$. Note that this is a simplified version of the rigorous analysis already performed by Groszkowski [49].

In order to derive a closed form expression for A_3, the transconductor output current at $3\omega_0$ is needed. By taking $A_3 \ll A_1$, this term turns out to be:

$$I_3 \cong \left[-\frac{1}{4} g_3 A_1^3\right] \cos(3\omega_0 t). \tag{2.12}$$

Equation (2.12) justifies the approximation of the output voltage given in (2.5). Since the third harmonic of the current flows mainly into the tank capacitor, whose impedance is $1/(j3\omega_0 C)$, V_3 is a sine function at $3\omega_0$. The complete balance equation for A_3 reads:

$$-\frac{1}{4} g_3 A_1^3 = -3\omega_0 C A_3 + \frac{A_3}{3\omega_0 L}, \tag{2.13}$$

resulting:

$$A_3 \cong \frac{3}{32}\frac{g_3}{\omega_0 C} A_1^3. \tag{2.14}$$

From (2.10) and (2.14), it follows that the THD of the oscillator is:

$$THD \cong \frac{A_3}{A_1} \cong \frac{1}{8}\frac{(G_X - 1)}{Q}. \tag{2.15}$$

Equation (2.15) suggests that the harmonic distortion is a function of excess gain and quality factor. Note that the term $(G_X - 1)/Q$ is equal to $\epsilon/4$, ϵ being the voltage-biased parameter [54].

Finally, the phase ϑ of the first harmonic of the current flowing through the tank can be linked to the frequency shift $\Delta\omega_0$. By means of the approximation $1 - \omega_0^2 LC \cong -2\frac{\Delta\omega_0}{\omega_0}$, the tank impedance Z_1 can be written as $Z_1 = R + j2\Delta\omega_0 L$. Since $\vartheta = \angle Z_1$, it is:

$$\vartheta \cong \arctan\left(\frac{2\Delta\omega_0 L}{R}\right), \tag{2.16}$$

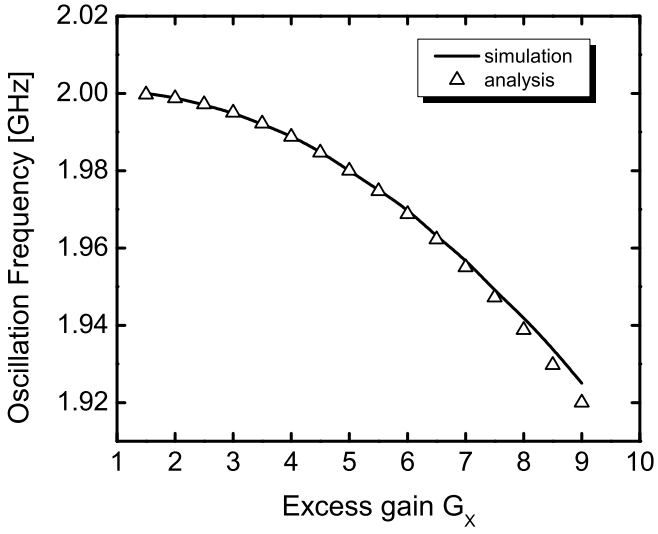


Figure 2.7: *Oscillation frequency as a function of the excess gain. Triangles refer to the oscillation frequency estimated with (2.1) taking into account the effect of distortion.*

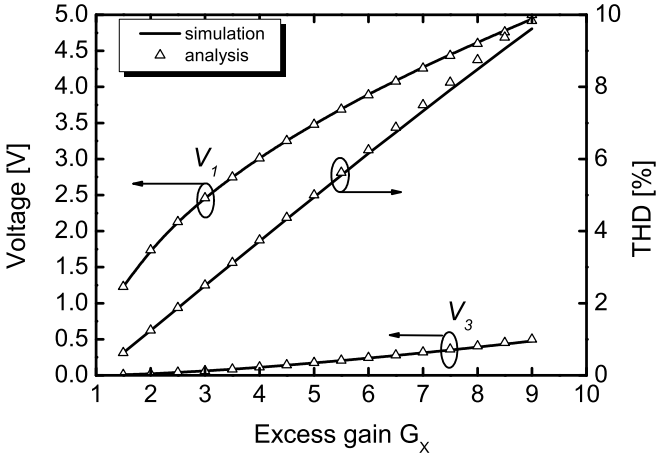


Figure 2.8: *Dependence on the excess gain of the THD and of the magnitude of first and third harmonic of the voltage. Triangles refer to expressions (2.10), (2.14), and (2.15).*

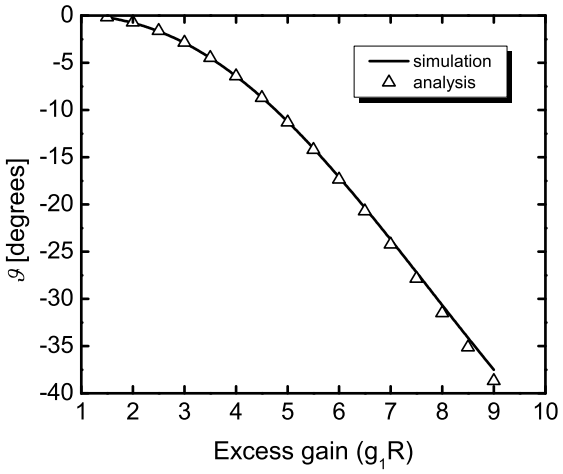


Figure 2.9: *Phase ϑ of the first harmonic of the current flowing through the tank as a function of the excess gain. Triangles refer to the approximation given by (2.16).*

clearly being $\vartheta < 0$.

The compact equations derived above have been compared to the steady-state solution of the behavioral model in Fig. 2.5 obtained by a periodic steady-state (PSS) simulation with SpectreRF in a Cadence environment. Figures 2.7, 2.8 and 2.9 show the oscillation frequency, the amplitudes A_1 and A_3 together with the total harmonic distortion and the phase ϑ, respectively, as functions of the excess gain. The small-signal transconductance, g_1, has been changed from $10\,\text{mA/V}$ to $60\,\text{mA/V}$, while the other model parameters have been taken as: $g_3 = 3\,\text{mA/V}^3$, $L = 1.2\,\text{nH}$, $C = 5.3\,\text{pF}$ and $R = 150\,\Omega$[1]. Note that although the analysis was carried out only considering the first and the third harmonic of the output voltage, the accuracy is very good even up to an excess gain of 9.

2.4 Phase noise induced from cyclostationary noise sources

2.4.1 The ISF: a closer look

The contribution of each noise source to the oscillator phase noise may be computed using the impulse sensitivity function [37, 38], introduced in Section 1.6.1. Although the ISF was originally defined as the $\Gamma(t)$ function

[1] In a real oscillator the parameter g_3 is function of g_1 while it was kept constant in the behavioral simulations. However, this does not invalidate the obtained results, since simulations confirm that THD and current phase are only function of the excess gain and thus of g_1.

in (1.7), in this dissertation it will be denoted as its scaled replica:

$$h(t) = \frac{\Gamma(t)}{q_{max}}, \tag{2.17}$$

q_{max} being the maximum charge across the capacitor placed between the nodes of interest. This choice has the advantage to allow:

- to directly compare phase responses associated to current sources located in different points of the circuit
- to avoid determining the value of q_{max} and, thus, the value of the equivalent capacitor "seen" by the current source, which can result into a tedious operation

Under this frame, the phase fluctuation generated by a noise source, $i_n(t)$, can be written as:

$$\Delta\phi(t) = \int_{-\infty}^{t} h(\omega_0\tau) \cdot i_n(\tau)\, d\tau, \tag{2.18}$$

Let us now refer to the circuit in Fig. 2.1. The noise injected by each switching transistor (e.g. the n-type MOSFET at the bottom left) will affect the oscillator phase noise via $h_{DS}(\omega_0 t)$, the latter being the ISF for the noise generator i_n applied between its drain node and ground.

Before deriving both functions by circuit simulations, some simplified arguments may help in highlighting some of their key features that will be then confirmed by numerical results. Let us assume that the differential output voltage waveform is given by:

$$V(t) \cong A_1 \cos(\omega_0 t). \tag{2.19}$$

In this case, the ISF of a noise source placed across the tank can be well approximated by a harmonic function in quadrature with respect to $V(t)$ [37, 41]:

$$h_T(\omega_0 t) \cong \frac{1}{A_1 C} \cos\left(\omega_0 t + \frac{\pi}{2}\right). \tag{2.20}$$

On the other hand, a current noise pulse injected by the noise generator across the n-type MOSFET M_1 at the bottom left in Fig. 2.1 will cause some signal to flow through the tank. More precisely, since the tank capacitor behaves as a short-circuit and the impedances of the two branches (M_1-M_3 and M_2-M_4) are almost the same for any operating bias point along the

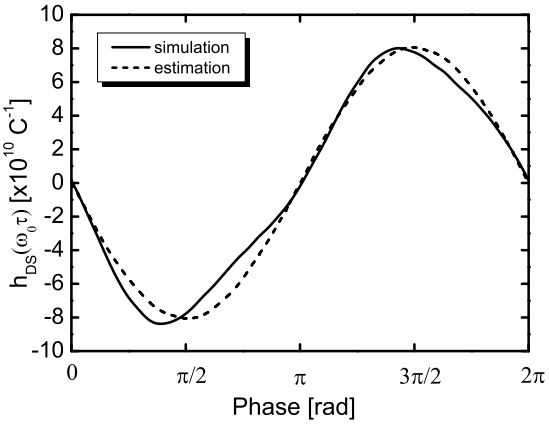


Figure 2.10: *Simulated and estimated ISF, $h_{DS}(\omega_0 t)$, over a single oscillation cycle for a current noise generator at the node out_n as in Fig. 2.1 derived for $W = 55\,\mu m$.*

oscillator cycle, about half of current pulse injected at the drain node is expected to flow through the tank. It follows that $h_{DS}(\omega_0 t)$ should be well approximated by half the ISF across the tank, that is:

$$h_{DS}(\omega_0 t) \cong \frac{1}{2A_1 C} \cos\left(\omega_0 t + \frac{\pi}{2}\right). \tag{2.21}$$

Figure 2.10 shows the ISF derived by simulating the circuit in Fig. 2.1 for a particular value of the excess, $G_X = 3.3$. A detailed explanation of the adopted ISF simulation methodology can be found in Chapter 4. The comparison with the approximation given by (2.21) is good. However, some slight discrepancies may be noticed. First of all, the simulated function is distorted. This result is not surprising since any distortion of the output voltage waveform will also reflect on the ISF [55]. In addition, it can be seen that the simulated ISF slightly leads the harmonic estimate given by (2.21). The same phase shift appears on $h_T(\omega_0 t)$ (not shown). A better approximation for the first harmonic of $h_{DS}(\omega_0 t)$ can therefore be given by:

$$h_{DS}(\omega_0 t) \cong h_1 \cos\left(\omega_0 t + \varphi_h^{(1)}\right), \tag{2.22}$$

where $h_1 = \frac{1}{2A_1 C}$ and $\varphi_h^{(1)} > \pi/2$ are to be determined. This term is by far the most dominant one. However, in Section 2.7.3 the impact of the higher-order harmonics arising from distortion will be also addressed.

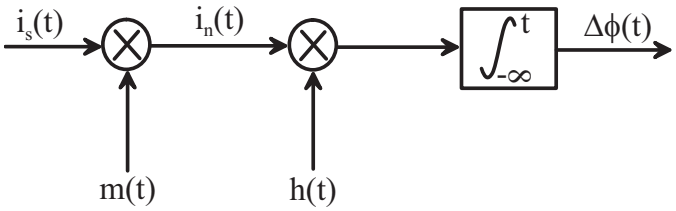


Figure 2.11: *Block diagram describing the generation of* $1/f^3$ *phase noise from the modulation through* $m(t)$ *of a stationary source* $i_s(t)$.

2.4.2 Modeling cyclostationary noise sources

Let us now consider the noise generator, $i_n\,(t)$, in (2.18). As far as the transistor operates in small-signal regime, noise processes are described by means of a power spectral density that depends on some device parameters.

A simple model equation for the $1/f$ noise has been provided [56] and adopted by the SPICE2 flicker noise model. According to this model, the power spectral density of the $1/f$ current noise may be written as:

$$S_I\,(\omega) = \frac{K_F |I_{DS}|^{\alpha}}{C'_{ox} L^2_{MOS}} \frac{2\pi}{\omega}, \tag{2.23}$$

where K_F is a process-dependent constant, I_{DS} the transistor channel current, L_{MOS} the MOSFET channel length and the exponent α a constant typically ranging between 1 and 2. More refined models, such as BSIM [57], are numerically implemented in circuit simulators. In all cases, the power spectral density varies according to some device parameters whose value depends on the transistor bias point.

In a large signal time-variant regime, these parameters are periodically modulated and the noise processes become cyclostationary. From the viewpoint of second-order statistics, the calculation of transfer functions from such noise generators can be greatly simplified if their noise processes are described starting from a stationary noise and then considering the intermixing of the noise components arising from the large signal variations of the device parameters [58–60]. Basing on the latter consideration, a cyclostationary process $i_n(t)$ can be written as the product of a stationary process $i_s(t)$ with unilateral power spectral density $S(\omega)$ and a deterministic noise modulating function (NMF) $m(t)$, resulting:

$$i_n\,(t) = m\,(t) \cdot i_s\,(t)\,, \tag{2.24}$$

This description is schematically depicted in Fig. 2.11. For the flicker

noise of transistor M_1 modeled as in (2.23), it is straightforward to choose:

$$\begin{cases} S(\omega) = \dfrac{K_F}{C'_{ox} L^2_{MOS}} \dfrac{2\pi}{\omega} & (2.25) \\ m(t) = \sqrt{|I_{DS,1}|^{\alpha}}. & (2.26) \end{cases}$$

In this frame, relying on Rice's noise theory [61], each single tone of the stationary process will be written as:

$$i_s(t) = i_s \cos\left(\omega_m t + \varphi_n\right), \tag{2.27}$$

where φ_n is a random phase uniformly distributed over the 0-2π interval and the magnitude i_s is given by $i_s = \sqrt{2S\left(\omega_m\right) \cdot 1\,\mathrm{Hz}}$. Basing on (2.24), each single tone translates into a set of correlated tones around each harmonic of the spectrum, as shown in Fig. 2.12, eventually resulting into a phase perturbation.

Even if this approach seems to work well to describe the behavior of cyclostationary white noise sources (shot or thermal noise) in linear time-variant circuits, there is a general belief that for long-term correlation noises, like flicker noise, this approach may be questionable [58]. Moreover, experimental measurements have demonstrated that stationary-based noise models, like SPICE2 and BSIM, are not accurate enough in cyclostationary regime [62–64]. However, since the purpose of this chapter is to grasp a physical insight of the up-conversion mechanism and to quantitatively justify the SpectreRF simulation results, we follow the procedure described above sticking to the simple model in (2.23).

2.4.3 The induced phase noise

Referring to the noise generator in Fig. 2.1, the contribution to the output phase arising from the low-frequency tone $i_s\left(t\right)$ can therefore be written as:

$$\Delta\phi\left(t\right) = \int_{-\infty}^{t} h_{DS}\left(\omega_0 \tau\right) \underbrace{m\left(\tau\right) i_s\left(\tau\right)}_{i_n(\tau)} d\tau. \tag{2.28}$$

Note that the product $m\left(t\right) \cdot i_s\left(t\right)$ generates correlated noise components i_n at frequencies $k\omega_0 \pm \omega_m$ as schematically depicted in Fig. 2.12. These components translate via the ISF, $h_{DS}\left(\omega_0 t\right)$, to phase noise.

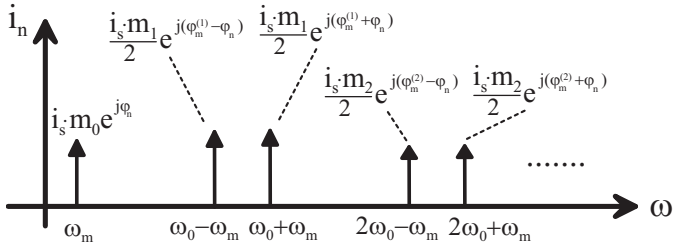


Figure 2.12: *Cyclostationary current noise tones resulting from a slow-frequency tone* $i_s(t) = i_s \cdot \cos(\omega_m t + \varphi_n)$.

Let us now try to gain a more quantitative insight into the outcome of (2.28). Since $I_{DS}(t)$ is a periodic function, $m\,(t)$ can be expanded into a Fourier series as:

$$m\,(t) = \sum_{k=0}^{+\infty} m_k \cdot \cos\left(k\omega_0 t + \varphi_m^{(k)}\right). \tag{2.29}$$

Taking for $h_{DS}\,(\omega_0)$ the first dominant harmonic term given by (2.22), it turns out that the current tones significantly contributing to phase modulation are only those at $\omega_0 \pm \omega_m$:

$$\begin{cases} i_n\,(\omega_0 + \omega_m) \Rightarrow \frac{i_s \cdot m_1}{2} \cdot \cos\left[(\omega_0 + \omega_m)\,t + \varphi_m^{(1)} + \varphi_n\right] \\ i_n\,(\omega_0 - \omega_m) \Rightarrow \frac{i_s \cdot m_1}{2} \cdot \cos\left[(\omega_0 - \omega_m)\,t + \varphi_m^{(1)} - \varphi_n\right] \end{cases}, \tag{2.30}$$

since only the slow-varying term of the product $h_{DS}\,(\omega_0) \cdot m\,(\omega_0)$ in (2.28) survives after the integration.

The two tones in (2.30) eventually result into a phase modulation and the output voltage in (2.19) can be rewritten adding the perturbation term as:

$$V\,(t) \cong A_1 \cos\left[\omega_0 t + \Delta\phi(t)\right], \tag{2.31}$$

$\Delta\phi(t)$ being given by:

$$\Delta\phi(t) = \frac{h_1 m_1 i_s}{2\omega_m} \cos\left(\varphi_h^{(1)} - \varphi_m^{(1)}\right) \cos\left(\omega_m t + \varphi_n\right), \tag{2.32}$$

where (2.21) has been used. The amplitude of the phase modulation is therefore written as:

$$\Delta\phi = \frac{h_1 m_1 i_s}{2\omega_m} \left|\cos\left(\varphi_h^{(1)} - \varphi_m^{(1)}\right)\right|. \tag{2.33}$$

According to (1.4) and (1.5), the single sideband to carrier ratio is given by $\left(\frac{\Delta\phi}{2}\right)^2 \cdot \frac{1}{1\,\mathrm{Hz}}$, resulting:

$$\mathcal{L}\left(\omega_m\right) = \frac{S\left(\omega_m\right)}{2} \cdot \left[\frac{h_1 m_1 \cos\left(\varphi_h^{(1)} - \varphi_m^{(1)}\right)}{2\omega_m}\right]^2 . \tag{2.34}$$

To account for the contribution of both PMOS and NMOS transistors, the power spectral density $S(\omega)$ in (2.25) and (2.34) can be extended to:

$$S_{1/f}\left(\omega_m\right) = 2\left(\frac{K_F^n}{C'_{ox}L_n^2}\frac{2\pi}{\omega_m} + \frac{K_F^p}{C'_{ox}L_p^2}\frac{2\pi}{\omega_m}\right), \tag{2.35}$$

where the factor 2 derives from adding the uncorrelated $1/f$ noise contributions of the two transistors within each cross-coupled pair.

Thus, the overall phase noise can be written as:

$$\mathcal{L}\left(\omega_m\right) = \frac{S_{1/f}\left(\omega_m\right)}{8\omega_m^2} \cdot \left[h_1 m_1 \cos\left(\varphi_h^{(1)} - \varphi_m^{(1)}\right)\right]^2 . \tag{2.36}$$

Equations (2.35) and (2.36) assume that the NMF $m\left(t\right)$ is the same for NMOS and PMOS transistors. The extension to a more general case can be easily derived. From a conceptual standpoint, (2.36) highlights that the $1/f$ noise up-conversion depends on the values of two key phase shifts:

- the phase $\varphi_h^{(1)}$ resulting from the first harmonic of ISF being not precisely in quadrature to the voltage waveform
- the phase $\varphi_m^{(1)}$ of the first harmonic of the modulating function, $m\left(t\right)$, with respect to the voltage waveform.

A quantitative evaluation of the two phase shifts will be carried out in Section 2.5 and compared to simulation results.

2.5 The up-conversion mechanisms

2.5.1 Phase noise decomposition

In the following, a phasor interpretation of the result gained so far will be provided. To this purpose, it is vital noting that (2.36) basically indicates that the dominant contribution to $1/f^3$ phase noise depends on the scalar

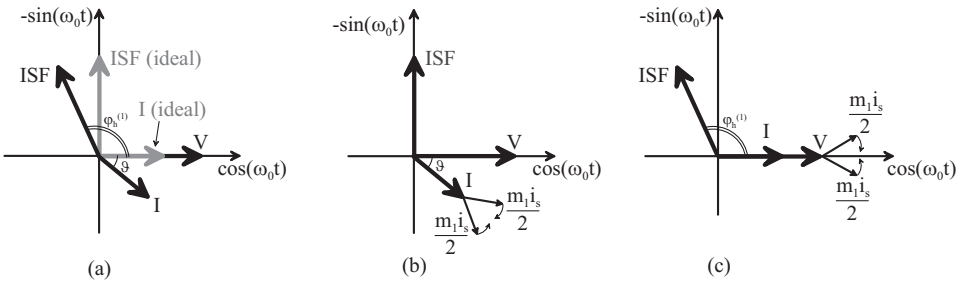


Figure 2.13: *(a) Phasor plot of the first harmonics of output voltage, transistor current and its related ISF. Grey and black arrows refer to the ideal and real case, respectively. (b) Phasor plot corresponding to direct contribution arising from injection of small current tones. (c) Phasor plot associated to AM-to-PM conversion phenomenon.*

product between the first harmonics of the ISF and the modulating function $m(t)$, i.e.:

$$\mathcal{L}\left(\omega_m\right) \propto \left(\overrightarrow{h_1} \cdot \overrightarrow{m_1}\right)^2 . \tag{2.37}$$

Any time these phasors are orthogonal, the dominant term of low-frequency noise up-conversion vanishes with the obvious benefit that $1/f^3$ phase-noise is nulled.

The phasor plot in Fig. 2.13(a) shows this ideal situation for the current noise generator of the transistor M_1 in Fig. 2.1. The output voltage of the VCO is taken as a cosine function, thus its corresponding phasor is placed along the x-axis, while the ISF is in quadrature. On the other hand, the first harmonic of the NMF, due to the mild dependence of $m(t)$ on $I_{DS,1}$ in (2.26), follows approximately the first harmonic of the transistor current, which is in phase with the voltage V. If both conditions apply, (2.36) gives nil and the conversion of $1/f$ noise into phase noise will be determined only by weaker terms caused by higher-order harmonics of both ISF and $m(t)$. However, in the more general case, depicted in Fig. 2.13(a), the ISF leads by more than 90 degrees, and the current slightly lags by an angle ϑ with respect to the output voltage, the latter effect being explained in Section 2.3. As it will be shown in the following sections, $\varphi_h^{(1)} - \frac{\pi}{2}$ and $\varphi_m^{(1)}$ are in the order of a few degrees for typical values of excess gain. Thus, the following approximations can be adopted: $\cos\varphi_m^{(1)} \cong 1$ and $\sin\varphi_h^{(1)} \cong 1$

and (2.36) can be rewritten as:

$$\mathcal{L}(\omega_m) \cong \left[\underbrace{\xi(\omega_m) h_1 m_1 \sin \varphi_m^{(1)}}_{\text{direct contribution}} + \underbrace{\xi(\omega_m) h_1 m_1 \cos \varphi_h^{(1)}}_{\text{AM-to-PM contribution}} \right]^2, \tag{2.38}$$

where $\xi(\omega_m) = \frac{\sqrt{2S_{1/f}(\omega_m)}}{4\omega_m}$. Thus, the $1/f^3$ phase noise results from the sum of two correlated contributions. These terms can be linked to specific up-conversion mechanisms that will be explained in the following sections.

2.5.2 Direct contribution

The first up-conversion mechanism is due to the phase $\varphi_m^{(1)}$ being different from zero. This term corresponds to the first contribution in (2.38) and derives from the Groszkowski effect. Fig. 2.13(b) shows the two correlated noise current tones in (2.30). They generate a phase modulation, with amplitude equal to $\frac{h_1 m_1 i_s}{2\omega_m} \sin \varphi_m^{(1)}$, arising from the injection into the tank of their components orthogonal to the voltage (PM components), as indicated by the factor $\sin \varphi_m^{(1)}$. This term is thus referred to as a *direct contribution* to $1/f^3$ phase noise.

The question is how to link $\varphi_m^{(1)}$ to the phase shift ϑ derived in Section 2.3. To this purpose, it is first useful to establish the relationship between the phase of the tank current ϑ and the phase $\varphi_{I,1}$ of the first harmonic of the current $I_{DS,1}$ flowing through the transistor M_1 in Fig. 2.1. This step is very simple to be performed since two conditions hold:

- NMOS and PMOS transistors are sized to be electrically equivalent
- ϑ is only due to harmonic distortion, other sources of delay being negligible.

As a result, the first harmonics of $I_{DS,1}$ and $I_{DS,3}$, flowing through M_1 and M_3 respectively, have same magnitude $I_{DS}^{(1)}$ and opposite phase. Since the current flowing through the tank is given by $I_{DS,1} - I_{DS,3}$, it immediately follows:

$$\begin{cases} \varphi_{I,1} \cong \vartheta & (2.39) \\ I_{DS}^{(1)} = \dfrac{A_1}{2R}, & (2.40) \end{cases}$$

the latter resulting from (2.8) and (2.6), neglecting the in-quadrature part.

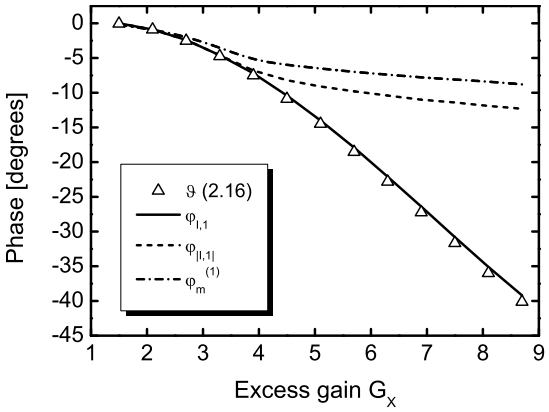


Figure 2.14: *Phases of the first harmonics of $I_{DS,1}(t)$, $|I_{DS,1}(t)|$ and modulating function, $m(t)$. Triangles refer to the value of ϑ calculated by using (2.16).*

Unfortunately, it is not possible to find a closed-form expression of $\varphi_m^{(1)}$, since the modulating function $|I_{DS,1}(t)|^{\alpha/2}$ is related to MOSFET channel current by two non-linear operators: absolute value and power raising. However, the phase $\varphi_m^{(1)}$ has been computed by means of circuit simulations. Figure 2.14 shows ϑ, $\varphi_{I,1}$ and $\varphi_m^{(1)}$ versus the oscillator excess gain. The phase of the first harmonic of $|I_{DS,1}(t)|$, denoted as $\varphi_{|I,1|}$ is also plotted. For low excess gain, i.e. for quasi-harmonic current, $\varphi_m^{(1)}$ is well approximated by $\varphi_{I,1}$, as evident in Fig. 2.14, eventually resulting:

$$\varphi_m^{(1)} \cong \vartheta. \tag{2.41}$$

For an excess gain greater than 4, corresponding to an NMOS transistor width larger than $65\ \mu$m, the oscillation amplitude is higher than the power supply, thus making the drain current of M_1 to be negative for a fraction of the period (the current flows from source to drain). This is why the phase of the first harmonic of $|I_{DS,1}|$ deviates from the one corresponding to $I_{DS,1}$, while the power raising operator has a minor effect. The following analysis will therefore be limited to small values of excess gain, that are adequate for most applications.

2.5.3 AM-to-PM contribution

The second contribution in (2.38) results from the phase of the ISF that is not perfectly in quadrature with the output voltage. The corresponding phasor plot is shown in Fig. 2.13(c). To consider the second term in (2.38),

we now assume $\varphi_m^{(1)} = 0$. In this case, the two noise current tones in (2.30) are generating an amplitude modulation of the current, and thus of the output voltage, at the fundamental frequency. They eventually result into phase noise due to the ISF phase shift. The term is therefore recognized as due to AM-to-PM conversion. This up-conversion mechanism is usually quoted referring to an AM-to-FM sensitivity, k_{AM-FM}, defined as:

$$k_{AM-FM} = \frac{\partial \omega_0}{\partial A_1}, \tag{2.42}$$

where A_1 is the oscillation amplitude of the voltage first harmonic. Let us now derive the link between the ISF phase shift $\varphi_h^{(1)}$ and the coefficient k_{AM-FM} to bridge the two descriptions. In case of small perturbation ΔA_1 of the voltage amplitude, the derivative in (2.42) can be approximated by the finite difference:

$$\frac{\partial \omega_0}{\partial A_1} \cong \frac{\Delta \omega}{\Delta A_1}. \tag{2.43}$$

On the other hand, the amplitudes of frequency and phase modulations, $\Delta\omega$ and $\Delta\phi$ respectively, are linked by:

$$\Delta\phi = \frac{\Delta\omega}{\omega_m}, \tag{2.44}$$

ω_m being the modulation frequency. Therefore, from (2.42), (2.43) and (2.44), it turns out that:

$$\Delta\phi = \frac{k_{AM-FM}\Delta A_1}{\omega_m}. \tag{2.45}$$

The magnitude ΔA_1 depends on the amplitude modulation of the current and on the resistive impedance, R_{AM}, "seen" by the AM current tones [53]. Its value for the oscillator model in Fig. 2.5 will be explicitly derived in the following. Here the analysis is kept still more general. At this stage we may write:

$$\Delta A_1 = m_1 i_s R_{AM}. \tag{2.46}$$

The value of $\Delta\phi$ given by (2.45) must be equal to the one resulting from (2.33) evaluated for $\varphi_m^{(1)} = 0$, i.e.:

$$\Delta\phi = \frac{h_1 m_1 i_s}{2\omega_m} \cos\varphi_h^{(1)}. \tag{2.47}$$

From (2.47), using (2.46) and (2.45), it is now possible to link the additional ISF phase shift $\varphi_h^{(1)}$ to k_{AM-FM}:

$$h_1 \cos \varphi_h^{(1)} = 2k_{AM-FM} R_{AM}. \tag{2.48}$$

Finally, since $h_1 \cong \frac{1}{2CA_1}$, the phase $\varphi_h^{(1)}$ is thus given by:

$$\varphi_h^{(1)} \cong \frac{\pi}{2} - 4CA_1 k_{AM-FM} R_{AM}. \tag{2.49}$$

Equation (2.49) is general and it is valid for any harmonic oscillator. It links the phase shift of the impulse sensitivity function to any AM-to-PM conversion mechanism of a low-frequency noise source. Thus, we will refer to the second term of $1/f^3$ phase noise given by (2.38) as *AM-to-PM contribution*. The next section will be devoted to analyze more in depth the AM-to-PM conversion effects taking place in a voltage-biased oscillator.

2.6 AM-to-PM conversion effects

Three main AM-to-PM conversion mechanisms have to be taken into account when dealing with a harmonic oscillator:

- the modulation of the voltage amplitude across tank varactors;
- the modulation of the harmonic content of the output voltage;
- the modulation of the voltage amplitude across non-linear parasitic capacitances of the transconductor.

The first contribution can be drastically reduced if frequency tuning is achieved by using a bank of switched capacitors and a small analog varactor [32], thus featuring a low sensitivity to AM noise. The impact of the other terms will be instead estimated in the following subsections in the case of voltage-biased oscillators.

2.6.1 Modulation of the harmonic content

Since the Groszkowski effect links the frequency shift $\Delta\omega_0$ in (2.11) to the harmonic content of the voltage waveform [49], it can be a source of AM-to-PM conversion. Any change of the voltage amplitude may cause a variation of its harmonic distortion. The balance between the reactive power delivered to the tank by the fundamental harmonic and by the higher-order

harmonics is perturbed and the oscillation frequency has to shift accordingly to recover it. This effect, induced by amplitude modulation, may be referred to as *incremental* Groszkowski effect [27].

The presence of a frequency shift, $\Delta\omega_0$, can be modeled by adding to the circuit model in Fig. 2.5 an equivalent non-linear capacitance C_{Gros} [30], which is function of the oscillation amplitude A_1. Its value can be linked to the frequency shift by writing:

$$C_{Gros} \cong -2\frac{\Delta\omega_0}{\omega_0}C \tag{2.50}$$

and, using (2.10), (2.11) and (2.14):

$$C_{Gros} = \frac{3}{4}\frac{g_3 A_1 A_3}{\omega_0} = \frac{9}{128}\frac{g_3^2 A_1^4}{\omega_0^2 C}. \tag{2.51}$$

The Groszkowski capacitance can be eventually related to the excess gain, resulting:

$$C_{Gros} = \frac{C}{8}\frac{(G_X - 1)^2}{Q^2}, \tag{2.52}$$

being $Q = \omega_0 RC$ the tank quality factor.

Equation (2.51) highlights that any amplitude change of the voltage harmonics leads to a variation of the equivalent capacitance, C_{Gros}, resulting into an AM-to-PM conversion. In particular, a modulation of A_1 reflects into a modulation of A_3, and thus of the harmonic distortion, determining a frequency modulation via the Groszkowski effect. The corresponding AM-to-FM sensitivity can be derived from:

$$k_{AM-FM}^{(\text{Gros.})} \cong \frac{\partial\omega_0}{\partial A_1} = \frac{\partial\omega_0}{\partial C_{Gros}} \cdot \frac{\partial C_{Gros}}{\partial A_1}. \tag{2.53}$$

By using (2.51) and (2.10), it turns out:

$$k_{AM-FM}^{(\text{Gros.})} = -\frac{9}{64}\frac{g_3^2 A_1^3}{\omega_0 C^2} = -\frac{1}{4}\frac{\omega_0 (G_X - 1)^2}{A_1 Q^2}. \tag{2.54}$$

Thus, the AM-to-PM sensitivity $k_{AM-FM}^{(\text{Gros.})}$ is a function of the excess gain. As G_X is increased, the modulation of the harmonic content grows causing an increase of the AM-to-PM conversion effect.

2.6.2 Modulation of non-linear parasitic capacitances

Let us now consider the AM-to-PM conversion effect arising from the non-linear parasitic capacitances of the transconductor. Recently, the effect has

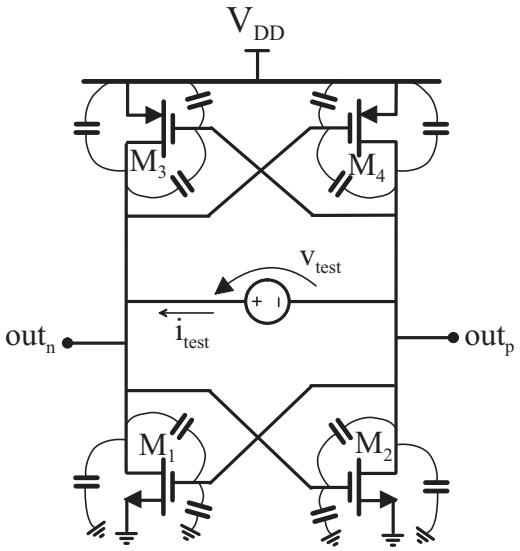


Figure 2.15: *Circuit schematic for the evaluation of the effective parasitic capacitance connected to the tank.*

been analyzed referring to a current-biased topology [21]. Here we address the impact in a voltage-biased oscillator as a function of the transistors width, which sets the g_m-value and thus the excess gain. Since parasitic capacitances scale with CMOS technology, this term is expected to be abated by scaling. Let us denote as C_{act} the effective parasitic capacitance in parallel to the tank due to active devices, shown in Fig. 2.5. Basing on (2.42), the corresponding frequency sensitivity can be written as:

$$k_{AM-FM}^{(\text{Act.})} \cong \frac{\partial \omega_0}{\partial A_1} = \frac{\partial \omega_0}{\partial C_{act}} \cdot \frac{\partial C_{act}}{\partial A_1} \cong -\frac{\omega_0}{2C} \cdot \frac{\partial C_{act}}{\partial A_1}, \tag{2.55}$$

To get a realistic estimate of the factor $\frac{\partial C_{act}}{\partial A_1}$, detailed simulations of the circuit in Fig. 2.1 were performed. The tank was sized to have $L = 1.2\,\text{nH}$, $C = 5.3\,\text{pF}$ and $Q = 10$. The transistors were designed with minimum length while the width of the NMOS transistors was swept from $20\,\mu\text{m}$ to $150\,\mu\text{m}$ in order for the excess gain to range from 1.4 to about 10. The width of the PMOS transistors was always twice the width of the NMOS devices. PSS analyses were first run to obtain the oscillation amplitude values A_1 corresponding to the different sizing choices. Then, periodic steady-state simulations were run on the circuit schematic in Fig. 2.15 where the LC tank is replaced by a harmonic voltage source, $v_{test} = A_1 \cos(\omega t)$. In this way, only the physical MOSFETs capacitances are taken into account since

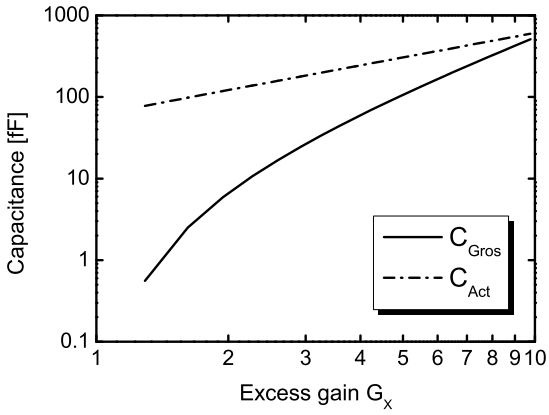


Figure 2.16: *Equivalent non-linear capacitances C_{act} and C_{Gros} for the oscillator in Fig. 2.1 as functions of the excess gain. The oscillator has been sized with minimum length (65 nm) transistors, $L = 1.2\,nH$, $C = 5.3\,pF$ and $Q = 10$ for an oscillation frequency of 2 GHz.*

the Groszkowski effect does not take place. The effective capacitance C_{act} can be derived as [15]:

$$C_{act} = \frac{1}{\pi\omega A_1^2} \oint i_{test} dv_{test}. \tag{2.56}$$

The derivative $\frac{\partial C_{act}}{\partial A_1}$ in (2.55) is obtained by setting $\omega = 2\pi \cdot 2$ Grad/s and sweeping A_1 around the closed-loop amplitude value computed for each transistor width. Figure 2.16 compares the values derived for both C_{act} and C_{Gros}, the latter being estimated by means of (2.52). C_{act} is almost linearly dependent on transistor width, and therefore on excess gain, and is always larger than C_{Gros}. The corresponding AM-to-FM sensitivity, $k_{AM-FM}^{(\text{Act.})}$, is plotted in Fig. 2.17 (solid line) showing an almost linear dependence on the excess gain.

The sensitivity of the transconductor input capacitance on the oscillation amplitude can be qualitatively explained taking into account the contribution of each transistor to the differential tank capacitance. Regarding the transistor M_1 in Fig. 2.1, its contribution can be estimated as:

$$C_{act,M_1}(t) \cong C_{gd,1}(t) + \frac{1}{2} C_{gs,1}(t) + \frac{1}{2} C_{dsub,1}(t), \tag{2.57}$$

where C_{gd}, C_{gs} and C_{dsub} are the gate-drain, gate-source and drain-substrate parasitic capacitances, respectively. Even if the parasitic capacitances are

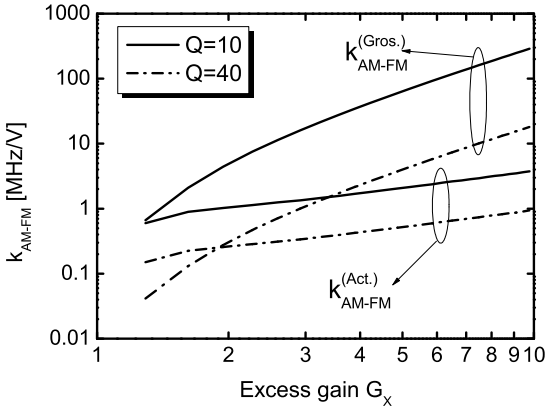


Figure 2.17: *Estimated $k_{AM-FM}^{(Gros.)}$ and simulated $k_{AM-FM}^{(Act.)}$ of the oscillator in Fig. 2.1 for $Q = 10$ (solid lines) and $Q = 40$ (dashed lines).*

time-variant, the effective contribution of the transistor M_1 to the differential tank capacitance can be approximated by the average value of C_{act,M_1} [13, 21]. Analogue considerations apply for the other transconductor devices.

For the sake of simplicity, let us consider in the model represented in Fig. 2.15 an increase of the differential voltage A_1 around the time-varying operating point. As far the oscillation amplitude increases, M_1 operates in ohmic region for a larger portion of the oscillation period. The average value of the gate-drain parasitic capacitance increases since C_{gd} is equal to a gate-drain overlap capacitance, $C_{ov}^{'}W$, in saturation and off regions ($C_{ov}^{'}$ is the specific overlap capacitance per unit channel width), while it approaches $\frac{1}{2}C_{ox}^{'}WL$ when it is ohmic, being $C_{ov}^{'}W \ll \frac{1}{2}C_{ox}^{'}WL$. The gate-source capacitance is much less sensitive to the operating point being equal to $\frac{2}{3}C_{ox}^{'}WL$ or $\frac{1}{2}C_{ox}^{'}WL$ as far the transistor is in saturation or ohmic region. Also the drain-substrate capacitance is less susceptible to a variation of the oscillation amplitude since it is associated to a reverse-biased *p-n* junction.

Thus, the derivative of the effective transconductor parasitic capacitance, C_{act}, with respect to the oscillation amplitude is positive, its behavior being determined by the MOS gate-drain capacitances. Moreover, $\frac{\partial C_{act}}{\partial A_1}$ increases with the excess gain, since transistor C_{gd} is proportional to the transistor width. This results into a negative sensitivity $k_{AM-FM}^{(\text{Act.})}$, featuring a linear dependence on the excess gain.

However, as shown in Fig. 2.17 (solid lines), the incremental Groszkow-

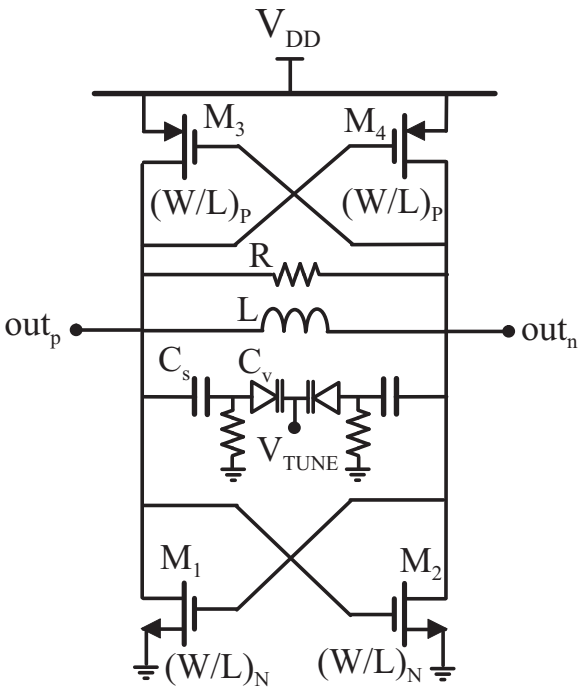


Figure 2.18: *Voltage-biased VCO with variable capacitors.*

ski effect is always more relevant than the contribution due to the non-linear transconductor parasitic capacitances. In fact, even if the parasitic input capacitance is even two orders of magnitude larger than the Groszkowski capacitor for small/moderate excess gain and comparable for large value of G_X, its sensitivity to amplitude modulation, $\frac{\partial C_{act}}{\partial A_1}$, is much lower with respect to $\frac{\partial C_{Gros}}{\partial A_1}$ and thus $k_{AM-FM}^{(\text{Act.})}$ is negligible with respect to $k_{AM-FM}^{(\text{Gros.})}$.

Finally, the reader may wonder if this conclusion changes when a tank quality factor larger than 10 is considered. In fact, the incremental Groszkowski contribution decreases being $k_{AM-FM}^{(\text{Gros.})} \propto 1/Q^2$. On the other hand, once the excess gain is fixed, a higher quality factor allows to adopt small-width transistors since $R = \omega_0 LQ$. This means that the parasitic capacitance scales down by the same Q-factor and the same happens for the $k_{AM-FM}^{(\text{Act.})}$ sensitivity. Figure 2.17 also shows the two estimated AM-to-FM sensitivities for $Q = 40$ (dashed lines). Even in this case, $k_{AM-FM}^{(\text{Gros.})}$ is larger than $k_{AM-FM}^{(\text{Act.})}$ for $G_X > 2$.

2.6.3 Modulation of non-linear varactors

Finally, it is worth investigating whether the flicker noise up-conversion mechanisms discussed in this chapter are dominant or not in a real oscillator that makes use of varactors to tune the oscillation frequency. The AM-to-PM conversion due to non-linear capacitances may be quantified by using a conversion coefficient, K_{AM-FM}, representing the sensitivity of the oscillation frequency to amplitude variations of the output voltage [11–13]. The phase noise resulting from this AM-to-PM conversion mechanism can be written as:

$$SSCR\left(\omega_m\right) = \frac{K_{AM-FM}^2 S_{AM}\left(\omega_m\right)}{2\omega_m^2}, \tag{2.58}$$

where $S_{AM}\left(\omega_m\right)$ is the power spectral density of the amplitude noise at an offset ω_m from the carrier. This amplitude noise is mainly due to current flicker noise that is up-converted around the fundamental frequency by the time-varying operating point of the transistors. The value of the conversion coefficient can be estimated for both CMOS and bipolar varactors [11–13]. In both cases, the K_{AM-FM} coefficient is proportional to the oscillator gain, $K_{VCO} = |\partial\omega_0/\partial V_{TUNE}|$, where V_{TUNE} is the control voltage of the VCO.

It turns out that the AM-to-PM conversion due to varactors is expected to be dominant for large VCO gains. Figure 2.18 shows a voltage-biased VCO using diode varactors to tune the frequency. The C_S capacitors are adopted in order to remove another $1/f^3$ phase noise generation mechanism, i.e. the common mode voltage to phase modulation (CM-PM) effect [13].

The VCO gain is changed by varying the voltage V_{TUNE}. For a fair comparison, the oscillation frequency is always kept at 2 GHz. Figure 2.19 shows the simulated phase noise at 1-kHz offset for two different values of VCO gain as a function of the excess gain. The up-converted flicker noise is now determined by both AM-to-PM conversion due to varactors and harmonic content modulation. The former contribution is dominant for small values of G_X and large oscillator gains, and it decreases for high excess gain since amplitude noise is reduced. Moreover, the presence of non-linear capacitances in the tank slightly increases the voltage harmonic distortion causing a small increment of $1/f^3$ phase noise also for large excess gains. However, while the varactor contribution may be reduced by minimizing the varactor sensitivity (K_{VCO}) and using a bank of digitally-switched capacitors not to impair the tuning range, the contribution arising from the transconductor non-linearity is unavoidable since it is intrinsically related to the non-linear nature of oscillators.

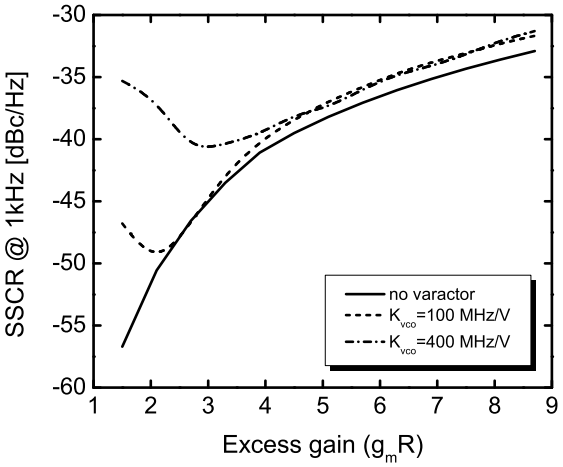


Figure 2.19: *Phase noise at* 1*-kHz offset for two different values of the oscillator gain* (K_{VCO}) *as function of the excess gain.*

2.7 Quantitative assessment of $1/f^3$ phase noise contributions

2.7.1 The impact of the excess gain

Let us now link the phase shifts $\varphi_m^{(1)}$ and $\varphi_h^{(1)}$ to the excess gain. The approximation in (2.41) is used. Plugging (2.11) into (2.16) leads to:

$$\varphi_m^{(1)} \cong \vartheta \cong -\arctan\left[\frac{(G_X-1)^2}{8Q}\right]. \tag{2.59}$$

It is therefore expected that, by increasing the excess gain G_X, the first harmonic of the transistor current increasingly lags with respect to the voltage waveform, following almost a quadratic dependence on G_X.

Regarding $\varphi_h^{(1)}$, in order to compute (2.49), the estimate of R_{AM} is needed. Following [53], R_{AM} is given by:

$$R_{AM} = \frac{1}{2}\left[R \parallel \left(-G_0 - \frac{1}{2}G_2\right)^{-1}\right], \tag{2.60}$$

where the factor $\frac{1}{2}$ takes into account that each noise source at the transistor drain causes a single-ended noise injection, while G_0 and G_2 are the Fourier coefficients of $G[V(t)] = \frac{\partial I(t)}{\partial V(t)}$. Taking (2.4), $G[V(t)] = g_1 - 3g_3V(t)^2$

and considering $V(t) \cong A_1 \cos(\omega_0 t)$, it is:

$$\begin{cases} G_0 = g_1 - \frac{2(G_X-1)}{R} \\ G_2 = -\frac{2(G_X-1)}{R} \end{cases} \tag{2.61}$$

Using (2.60) and (2.61), R_{AM} reads:

$$R_{AM} = \frac{R}{4(G_X - 1)}. \tag{2.62}$$

Note that R_{AM} is not simply given by the tank loss resistance R due to the presence of an amplitude-limiting mechanisms. Equation (2.62) represents the effect of the non-linearity on the amplitude variation. The larger the excess gain the larger the non-linearity and the smaller the amplitude variation due to the injected current tones.

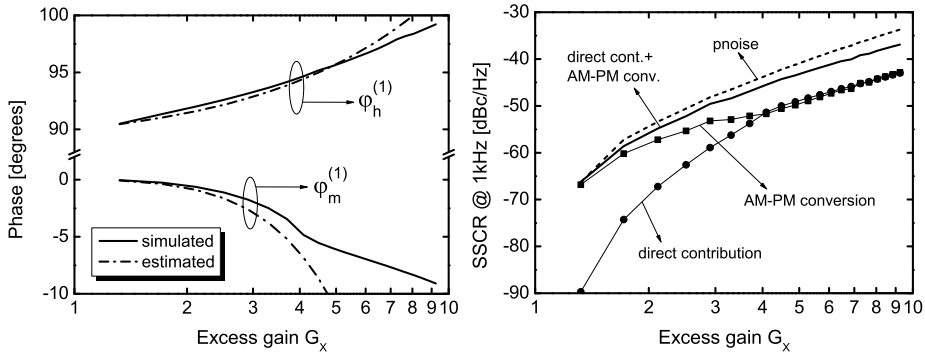
By assuming that the modulation of the harmonic content is the dominant mechanism of AM-to-PM conversion and by using (2.49), (2.54) and (2.62), $\varphi_h^{(1)}$ can be written as:

$$\varphi_h^{(1)} \cong \frac{\pi}{2} + \frac{G_X - 1}{4Q}. \tag{2.63}$$

Equations (2.59) and (2.63) suggest that both $1/f^3$ phase noise contributions in (2.38) are only function of the excess gain G_X and the tank quality factor Q and rise as the excess gain is increased.

As a matter of fact, the oscillator in Fig. 2.1 sized as in Section 2.2 has been simulated varying the transistor width and thus the excess gain. In Fig. 2.20(a), the simulated $\varphi_h^{(1)}$ and $\varphi_m^{(1)}$ phases are plotted as functions of the excess gain and compared with the estimates given by (2.59) and (2.63), showing a good agreement. The discrepancy between the simulated and estimated $\varphi_m^{(1)}$ at high excess gain is due to the approximation adopted in Section 2.5.2, where $\varphi_m^{(1)}$ has been taken as the phase of current flowing through the transistor, basically neglecting the impact of the absolute value and power raising operators.

As G_X is increased, the two phases rapidly depart from their ideal value, i.e. 0 and $\frac{\pi}{2}$, and consequently, both direct and AM-to-PM contributions increase, as shown in Fig. 2.20(b). Clearly, being correlated, the two contributions have to be linearly summed up to get the overall $1/f^3$ phase noise. Note that, being $\varphi_m^{(1)} < 0$ and $\varphi_h^{(1)} > \frac{\pi}{2}$, both terms in (2.38) are negative, thus summing up in phase.



(a) (b)

Figure 2.20: *(a) Simulated and estimated $\varphi_h^{(1)}$ and $\varphi_m^{(1)}$ of the voltage-biased oscillator in Fig. 2.1 as functions of the excess gain and (b) simulated direct and AM-to-PM contributions to $1/f^3$ phase noise quoted as SSCR at 1-kHz offset. Their sum is also plotted, together with the SpectreRF PNOISE analysis result.*

The estimate of $1/f^3$ phase noise closely matches the simulation result given by the SpectreRF periodic noise (PNOISE) analysis. The $1/f$ noise coefficients in (2.35) are $K_F^n = 10^{-27}$ AF and $K_F^p = 2{\cdot}10^{-28}$ AF for NMOS and PMOS transistors, respectively, and $C'_{ox} \cong 19\,\text{fF}/\mu\text{m}^2$. The small discrepancy (less than $1.5\,\text{dB}$) between simulated and estimated phase noise has to be ascribed to higher-order harmonics of the ISF, that so far have been neglected. In Section 2.7.3, it will be shown that the contribution of the third harmonic of the ISF and of the modulating function, thus of the current tones around the third harmonic of the transistor current, is sufficient to bridge the gap between the PNOISE simulation result and the estimate given by (2.38).

2.7.2 A closed-form expression of $1/f^3$ phase noise

Let us now try to derive a closed form expression of the $1/f^3$ phase noise starting from (2.36) and considering an excess gain not larger than 4, which is almost always verified in practice. In this range, the approximation $\varphi_m^{(1)} \cong \vartheta$ holds well. Thus, the only parameter in (2.36) still lacking of an analytic expression is the magnitude of the first harmonic of the modulating function, m_1. Since the purpose of this Section is to derive an approximate yet simple formula to compute the $1/f^3$ phase noise, it useful to consider the currents flowing through the MOSFETs in the oscillator in Fig. 2.1 as

square waves with 50% duty cycle. In other words, the transistors work as perfect switches and the current flowing through the LC tank is commutated between the M_1-M_4 and M_2-M_3 branches. Since the on-resistances of MOSFETs channel are smaller then R, the current flowing in M_1 during the triode region is given by $I_p \cong \frac{V_{DD}}{R}$. Since $\alpha = 1$ in the considered technology, the modulating function is then a square wave between 0 and $\sqrt{\frac{V_{DD}}{R}}$. By means of the approximation $2/\pi \cong 1/\sqrt{2}$, m_1 can be written as:

$$m_1 \cong \sqrt{\frac{V_{DD}}{2R}}. \tag{2.64}$$

Finally, by plugging (2.64), (2.59) and (2.63) into (2.36), the up-converted flicker noise can be estimated as:

$$SSCR\left(\omega_m\right) = \left(\frac{K_F^n}{C'_{ox}L_n^2} + \frac{K_F^p}{C'_{ox}L_p^2}\right)\left(\frac{2\pi}{\omega_m}\right) \cdot \frac{\left(G_X^2 - 1\right)^2 \omega_0}{2 \cdot 32^2 V_{DD}\omega_m^2 Q^3 C}. \tag{2.65}$$

By increasing the excess gain from 1.5 to 4, the phase noise of the reference oscillator is expected to increase from -62.4 dBc/Hz to -40.85 dBc/Hz. This estimate matches very closely with simulation results and is shown in Fig. 2.21). Equation (2.65) also suggests that $1/f^3$ phase noise can be reduced by decreasing the excess gain and/or improving the quality factor.

Note that the phase noise is proportional to $1/Q^3$ even if both φ_ϵ and $\varphi_m^{(1)}$ are proportional to $1/Q$, thus suggesting a $1/Q^2$-dependence of phase noise. The reason for this additional dependence on $1/Q$ is that also the transistor channel current depends on the tank loss resistance $R = \omega_0 LQ$. The larger the tank quality factor, the smaller the current and also the flicker noise intensity. Equation (2.65) explicitly indicates the dependence of $1/f^3$ phase noise on excess gain and it will be used in Chapter 5 to quantify the improvement of flicker-induced phase-noise performance achieved in the proposed oscillator topology.

2.7.3 The impact of higher-order harmonics

In order to refine the estimate, (2.21) can be extended to take into account all the harmonic components of the ISF. The Fourier series of h_{DS} can thus be written as [65]:

$$h_{DS}\left(\omega_0 t\right) = \frac{h_0}{2} + \sum_{k=1}^{+\infty} h_k \cos\left(k\omega_0 + \varphi_h^{(k)}\right), \tag{2.66}$$

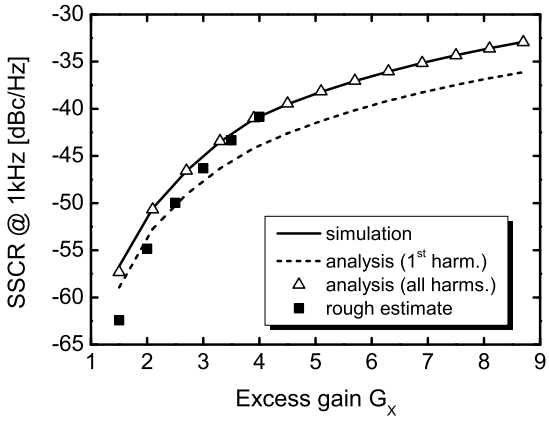


Figure 2.21: $1/f^3$ *phase noise at* 1*-kHz offset. Dashed line and triangles refer to the analyses based on first harmonic (see (2.36)) and all harmonics of* h_{DS}*, respectively. Diamonds refer to the rough estimate given by (2.65).*

where $h_1 = \frac{1}{2CA_1}$. As a consequence, the $1/f^3$ phase noise expression given by (2.36) can be accordingly extended to:

$$SSCR(\omega_m) = \frac{S_{1/f}(\omega_m)}{8\omega_m^2} \cdot \left[\sum_{k=0}^{+\infty} h_k m_k \cos\left(\varphi_h^{(k)} - \varphi_m^{(k)}\right)\right]^2 . \quad (2.67)$$

The magnitudes and the phases of $h_{DS}(t)$ and $m(t)$ can be evaluated by means of the simulation method described in Chapter 4.

Figure 2.21 (triangles) shows the $1/f^3$ phase noise estimation taking into account all the harmonic terms of h_{DS} and the contribution of both NMOS and PMOS pairs. The discrepancy is now reduced to less than 0.5 dB with respect to the simulated phase noise at 1-kHz offset. Figure 2.22 shows the contribution to the output noise due to the most relevant terms in (2.67). In addition to the dominant term generated by the first harmonic of h_{DS}, the contribution due to the third harmonic is also important. Its rising dependence is not due to the phase $\varphi_h^{(3)} - \varphi_m^{(3)}$, which is always around zero degrees thus giving $\cos\left(\varphi_h^{(3)} - \varphi_m^{(3)}\right) \cong 1$. It is instead the amplitude of the third harmonic of h_{DS} that changes by a factor of 10 as the excess gain ranges from 1.5 to 9 and the oscillator is driven in a highly non-linear regime.

The contributions due to the DC and the 2^{nd} harmonic of h_{DS} are more than one order of magnitude lower and negative. This result is not surprising. Since low frequency noise is up-converted around the oscillation

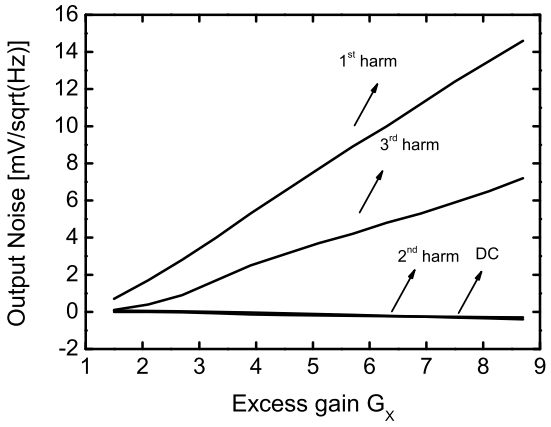


Figure 2.22: *Contributions to output noise due to different harmonics of the drain-referred ISF, h_{DS}.*

frequency and its harmonics, all the contributions are correlated and they may lead to a partial cancellation.

2.8 Conclusions

In this chapter, the up-conversion of flicker noise due to voltage harmonic content variation in voltage-biased oscillator has been discussed and quantitatively assessed. The phase noise up-conversion mechanisms have been quantified and linked to the oscillator non-linearity. Design equations have been derived and compared to simulation results adopting a stationary-based flicker noise model. In particular, it has been demonstrated that two mechanisms play a fundamental role in the conversion of flicker noise into phase noise:

- the direct injection into the tank of PM tones since the current through active devices lags with respect to the voltage
- an AM-to-PM conversion effect due to the dependence of the oscillation frequency on the harmonic content of the output voltage.

Equations (2.59), (2.63) and (2.65) highlight that flicker noise up-conversion is reduced in case of low excess gain, which translates into low distortion of the voltage output, and high tank quality factor (for a fixed excess gain), providing a strong attenuation of higher-order harmonics.

CHAPTER 3

Suppression of flicker noise up-conversion in voltage-biased oscillators

3.1 Introduction

In recent years, a few techniques have been presented to mitigate the effect of harmonic distortion in oscillators. Jerng and Sodini propose to reduce the device width of the differential-pair transistors in a current-biased oscillator to increase the overdrive voltage and to extend the linear range of the switching devices [22]. In this way, the harmonic distortion is reduced with benefits in terms of flicker noise up-conversion arising from both the switching pair and the bias circuit . These authors refer to the effect as a form of "indirect frequency modulation". Also in [23] the traditional topology shown in Fig. 3.1(a) is modified to include damping resistors at the source side of the differential pair transistors, introduced to linearize the transconductor and to suppress $1/f$ noise up-conversion. Both solutions reduce harmonic generation and therefore the Groszkowski effect but at the expenses of excess gain and start-up margin.

To circumvent these limitations, an alternative topology was proposed

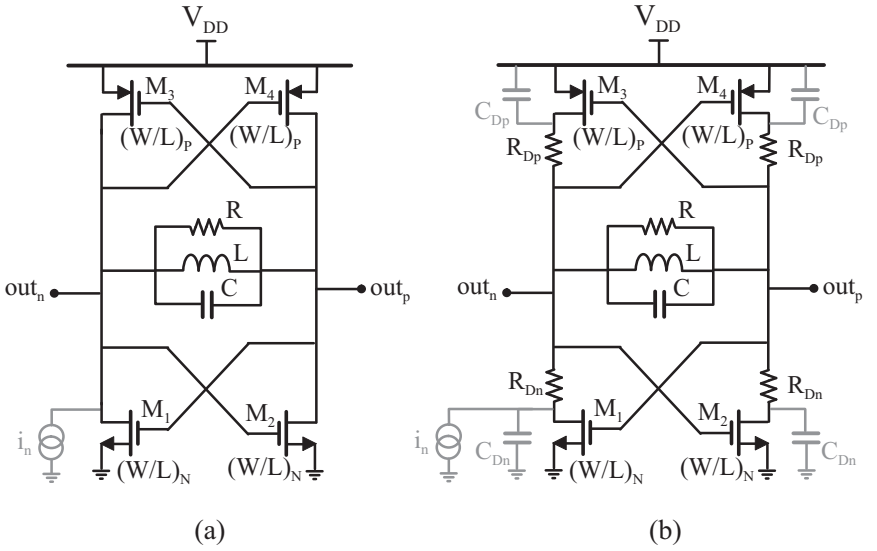


Figure 3.1: *Double cross-coupled voltage-biased oscillator: (a) traditional implementation and (b) topology with added drain resistances.*

in [33] where resistors are inserted at the transistor drains, as depicted in Fig. 3.1(b). It has been shown that the circuit reaches remarkable phase noise suppression, avoiding resonant solutions and the corresponding area penalties. Moreover, since the resistors are at the MOSFET drains, the start-up margin is not degraded. In addition, numerical simulations showed the potential to highly suppress the $1/f$ noise up-conversion by tailoring the resistor values. As the resistances are increased, the $1/f^3$ phase noise first decreases, reaching a minimum, and then it rises again. In [33], an intuitive and heuristic justification of this behavior was proposed. In this chapter, the analysis is revised and a quantitative framework is introduced to explain the peculiar up-conversion mitigation reached in the circuit.

The chapter is organized as follows. In Section 3.2 the proposed oscillator topology is presented and an analysis of $1/f^3$ phase noise generation is applied to the circuit. The explanation for the phase-noise dependence on the resistance value is provided in Section 3.3. Section 3.4 is devoted to comparing theory, simulations and experimental results for the 65-nm CMOS VCO previously reported in [33], while Section 3.5 provides the design guidelines to implement a VCO with reduced flicker-induced phase noise. In Section 3.6 a figure of merit is introduced to compare the effectiveness of different solutions. Finally, the conclusions are drawn in Section 3.7.

3.2 VCO with suppressed $1/f^3$ phase noise

The voltage-biased oscillator topology, analyzed in detail in Chapter 2 and shown in Fig. 3.1(a), can be improved by adding resistors in series to the MOSFETs drains, thus resorting to the circuit presented in [33] and depicted in Fig. 3.1(b). Under the assumption that the threshold voltage is the same for both NMOS and PMOS transistors ($V_{TH,n} = |V_{TH,p}| = V_{TH}$), if the voltage drop due to the resistors is lower than the threshold voltage, V_{TH}, when the circuit is balanced (i.e. at the oscillator start-up), the transistors are in saturation and the small-signal transconductance of the differential pair is not affected in practice. In fact, considering $R_{Dn} = R_{Dp}$, the overall transconductance of the double-coupled pair results:

$$g_m \cong \mu_n C'_{ox} \left(\frac{W}{L}\right)_n \left(\frac{V_{DD}}{2} - V_{TH}\right) \left[1 + \lambda \left(\frac{V_{DD}}{2} - \Delta V_R\right)\right], \quad (3.1)$$

being λ the channel-length modulation factor and ΔV_R the ohmic drop across the drain resistors, once $\Delta V_R < V_{TH}$.

Thus, the excess gain of the proposed oscillator in Fig.3.1(b) mildly depends on the added resistors, its dependence being limited to the channel-length modulation[1]. For the 1.2-V supply 65-nm CMOS process considered in this chapter, $V_{TH} \cong 0.4V$ and $\lambda \cong 1\ V^{-1}$. Thus, even considering a voltage drop as large as the threshold voltage, the reduction of excess gain is limited to a factor of about 1.3.

As far as the phase noise induced from $1/f$ noise concerns, it is first important to notice that due to the presence of the resistor the impulse sensitivity function h_{DS} associated to the current source i_n in Fig. 3.1(b) is no longer simply equal to half the tank-referred one, h_T. As a consequence, while (2.20) is still valid, its magnitude and phase, h_1 and $\varphi_h^{(1)}$ in (2.22), are not simply equal to $\frac{1}{2A_1C}$ and $\frac{\pi}{2} + \frac{G_X - 1}{4Q}$, respectively, the latter value given by (2.63).

However, linking h_{DS} to h_T is still very useful. To this aim, following the approach described in Section 2.4, the output phase shift $\Delta\phi(t)$ induced by the cyclostationary $1/f$ current noise $i_n(t)$ of transistor M_1 in Fig. 3.1(b)

[1] In the case of resistors added at the transistor source nodes, the overall transconductor g_m can be estimated as $\frac{g_{m0}}{1+g_{m0}R_S}$, g_{m0} being the transconductance without source degeneration. This approximation is valid if the ohmic drop across the resistor is much lower then the transistor overdrive voltage without source degeneration, i.e. $\frac{V_{DD}}{2} - V_{TH}$.

can be written as:

$$\Delta\phi(t) = \int_{-\infty}^{t} h_{DS}(\omega_0\tau)\, i_n(\tau) d\tau = \\ = \int_{-\infty}^{t} h_T(\omega_0\tau)\, \frac{i_{n,eq}(\tau)}{i_n(\tau)} i_n(\tau)\, d\tau. \tag{3.2}$$

In (3.2), $i_{n,eq}(t)$ is the equivalent current noise source that must be placed across the tank to account for the same phase contribution of $i_n(t)$. This approach allows to evaluate the phase perturbation once the tank-referred ISF, $h_T(\omega_0 t)$, is known. The ratio $i_{n,eq}(t)/i_n(t)$ in (3.2) is a periodic small-signal transfer function and will be denoted as $\Pi(\omega_0 t)$. Moreover, from (3.2) it immediately follows that:

$$h_{DS}(\omega_0 t) = \Pi(\omega_0 t) \cdot h_T(\omega_0 t). \tag{3.3}$$

Now the question is how the equivalent current noise $i_{n,eq}(t)$ can be evaluated. For the noise current generator $i_n(t)$, the system is linear although time-variant. Thus, the equivalent current can be evaluated as the current flowing in the equivalent Norton short-circuit between the output nodes. Since the circuit has a periodic steady state and being the output voltage harmonic for relative high-Q oscillator, the short-circuit can be replaced by a sinusoidal voltage generator with the same oscillation amplitude. Clearly, in the traditional voltage-biased oscillator topology, $\Pi(\omega_0 t)$ is a constant approximately equal to $1/2$, following the arguments in Section 2.4.1.

Let us now apply the phase noise analysis to the oscillator in Fig. 3.1(b) with resistors at the transistor drains. Also in this topology, as it will be shown in the following, the main contribution to $1/f^3$ phase noise derives from the first harmonic of h_{DS}. Furthermore, being h_T almost sinusoidal, it results from (3.3):

$$h_{DS}(\omega_0 t) \cong \Pi_0 \cdot h_T(\omega_0 t) \cong \Pi_0 \cos\left(\omega_0 t + \frac{\pi}{2} + \varphi_{\epsilon,DS}\right), \tag{3.4}$$

Π_0 being the average value of the function $\Pi(\omega_0 t)$ and $\varphi_{\epsilon,DS}$ the excess phase of h_{DS} with respect to quadrature.

The block diagram describing the phase noise generation mechanisms through Π and h_T is depicted in Fig. 3.2. It is useful to recall from Section 2.4.3 that the SSCR can be written as:

$$\mathcal{L}(\omega_m) = \frac{S_{1/f}(\omega_m)}{8\omega_m^2} \cdot \left[h_1 m_1 \sin\left(\varphi_{\epsilon,DS} - \varphi_m^{(1)}\right)\right]^2, \tag{3.5}$$

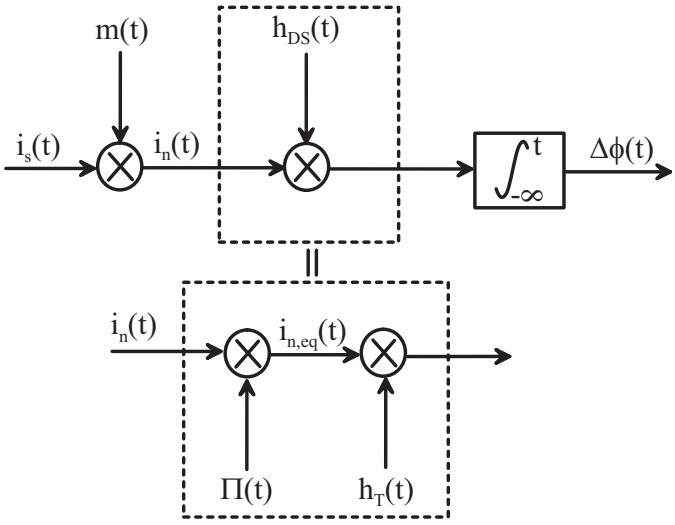


Figure 3.2: *Block diagram describing the generation of $1/f^3$ phase noise from the modulation through $m(t)$ of a stationary process $i_s(t)$.*

which is a slightly-modified version of (2.36).

From (3.4), it is likely that the amplitude of h_{DS} is a function of the drain resistor value. In fact, during the oscillation cycles, when the voltage at the node out_n approaches the negative rail, M_1 enters the ohmic region. If the drain resistor is larger than the transistor channel resistance, most of the current noise of the device is expected to re-circulate within the channel, not reaching the tank, with beneficial impact on phase noise. On the other hand, these resistors together with the transistor stray capacitances may cause signal delays within the oscillator loop that can affect the $1/f$ noise up-conversion mechanisms by changing the phase shifts in (3.5).

In order to have reference values, phase noise simulations were performed on the circuit in Fig. 3.1(b) designed in a 65-nm CMOS technology. The resonance frequency was set to 3.6 GHz by using $L = 4.6$ nH, $C = 400$ fF and $R = 1040\,\Omega$, leading to a quality factor of 10. The transistors were sized to have an excess gain, $g_m R$, of 2.8, enough to guarantee a safe start-up. Since $W_p = 2W_n$, the stray capacitance at the drain of the NMOS transistors, C_{Dn}, is half the capacitance of PMOS transistors, C_{Dp}. Therefore, to equalize the two delays the choice was to set $R_{Dn} = R_D$ and $R_{Dp} = R_D/2$. The delay $R_{Dn}C_{Dn} = R_{Dp}C_{Dp}$ will be denoted in the following as $R_D C_D$.

Figure 3.3 shows the phase noise at 1-kHz offset computed by using both SPICE and BSIM4 flicker noise models for different values of R_D.

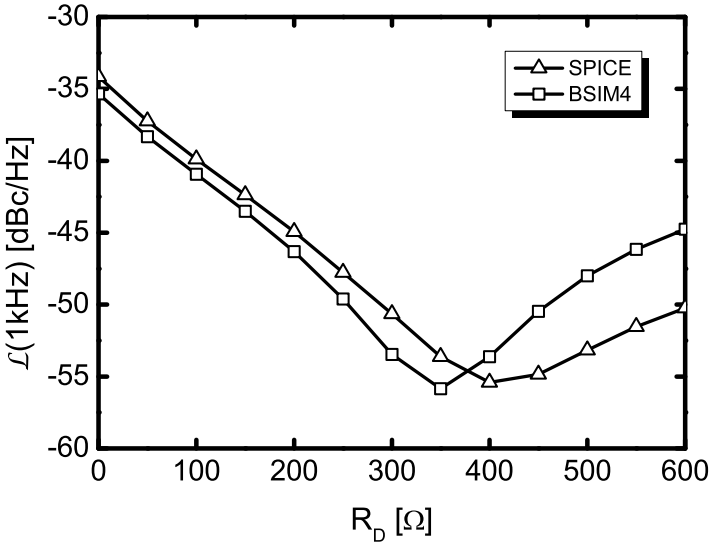


Figure 3.3: *Phase noise induced from* $1/f$ *noise evaluated at* 1*-kHz offset from the carrier. The simulation results with both SPICE and BSIM4 models are shown.*

At 1-kHz offset, flicker-induced phase noise is the dominant contribution. For both $1/f$ noise models, by increasing R_D the phase noise decreases reaching a minimum at $R_D \cong 400\,\Omega$ (SPICE) or at $R_D \cong 345\,\Omega$ (BSIM4) corresponding to the white noise floor of about -56 dBc/Hz.

It is evident that the specific noise model slightly shifts the optimum resistance value of $1/f^3$ noise suppression but the general feature of the phase noise trend is retained and deserves to be better understood. In fact, it is unlikely that a complete noise cancellation can be explained only by Π_0. This value is expected to decrease as R_D increases but there is no clear reason why, in some cases, it should become nil. The sine function in (3.5) suggests instead that a cancellation may occur when the phase shifts within its argument cancel out. Their values as a function of the drain resistor are shown in Fig. 3.4 (solid lines). For $R_D \cong 290\,\Omega$, the excess phase $\varphi_{\epsilon,_{DS}}$ and $\varphi_m^{(1)}$ in the SPICE flicker noise model are equal. For this resistor value, the phase noise resulting from the flicker current noise tones folded around the fundamental frequency is expected to be nil. Indeed, the flicker-induced phase noise suppression in Fig. 3.3 happens for a slightly-larger value of R_D.

Moreover, once the resistor has been sized, the reduction of $1/f^3$ phase noise is effective even if the oscillation frequency is changed. Fig. 3.5 shows the phase noise at 1-kHz and 1-MHz offset for the novel oscillator

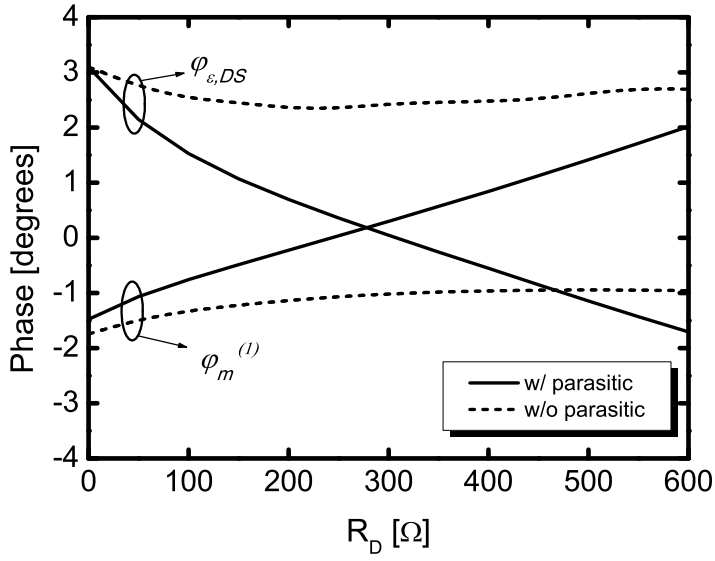


Figure 3.4: *$\varphi_{\epsilon,DS}$ and $\varphi_m^{(1)}$ as functions of the drain resistance R_D for the circuit in Fig. 3.1(b). Dashed lines refer to the case without parasitic drain capacitances.*

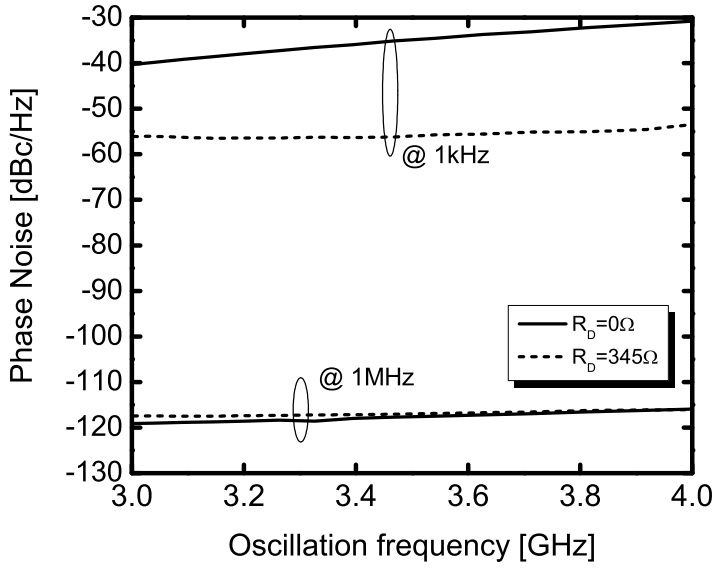


Figure 3.5: *Phase noise at 1-kHz and 1-MHz offset for the oscillator in Fig. 3.1(b) when tuned between 3 and 4 GHz for $R_D = 0$ and $R_D = 345\,\Omega$. The BSIM4 flicker noise model is adopted.*

topology in Fig. 3.1(b) when its oscillation frequency is tuned between 3 and $4\,$GHz, corresponding to a tuning range equal to 28%. The phase noise at 1-kHz offset is close to $-55\,$dBc/Hz along the whole tuning range. Figure 3.5 also shows that the proposed technique is not detrimental in terms of $1/f^2$ phase noise, since it causes an increase always lower than $2\,$dB. The following section will be therefore devoted to analyzing more in depth the circuit and the impact of the component values on both flicker-induced and $1/f^2$ phase noise. In addition, a quantitative explanation for the opposite trends of $\varphi_{\epsilon,DS}$ and $\varphi_m^{(1)}$ versus R_D will be presented.

3.3 Circuit analysis

3.3.1 Effect of loop delay on ISF

First, let us consider the transistor M_1 at the bottom-left side in Fig. 3.1(b). When the differential output voltage $V_{out} = out_p - out_n$ is positive (i.e. the voltage at the node out_p is larger than the voltage at the node out_n), the device enters the ohmic region. The larger R_D, the larger is the voltage drop at the drain node and the deeper is the ohmic region. Fig. 3.6(a) shows the dependence of h_{DS} on the phase $\omega_0 t$ compared to $h_T(\omega_0 t)$. Since the oscillation amplitude is reduced by R_D, the magnitude of both ISFs increases. However, it is interesting to note that as M_1 becomes ohmic, $h_{DS}(\omega_0 t)$ approaches zero, in agreement with the idea that the resistance R_D forces most of the M_1 current noise to re-circulate within the transistor. This consideration is confirmed by looking at the function $\Pi(\omega_0 t)$ shown in Fig. 3.6(b) for different values of the resistance R_D: for $\omega_0 t \cong \pi$, when the transistor M_1 is in deep triode region, the value of $\Pi(\omega_0 t)$ tends to reduce, preventing the current noise to reach the tank.

By increasing R_D, the effect becomes stronger and the magnitude of the first harmonic of h_{DS} increases less than h_T (Fig. 3.7(a)), their ratio changing from 0.5 for $R_D = 0$ to 0.38 for $R_D = 600\,\Omega$. On the other hand, the drain resistance has an impact also on the phase of both h_{DS} and h_T. Fig. 3.7(b) shows the excess phase of the first harmonics of the two sensitivity functions, the one associated to h_T being $\varphi_{\epsilon,T}$. The zero phase value corresponds to the perfect quadrature with respect to the output voltage. The two phases start from a positive value determined by the nonlinearity of the system, as shown in Chapter 2. For $R_D = 0$,$\varphi_{\epsilon,DS} = \varphi_{\epsilon,T}$ is

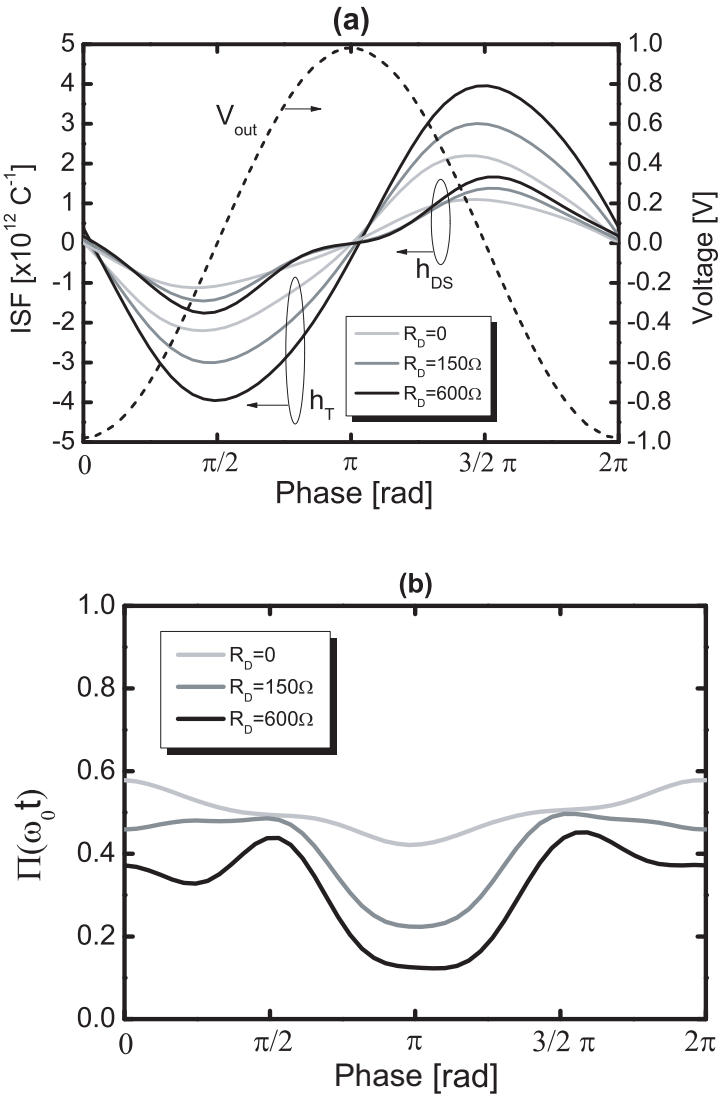


Figure 3.6: *$h_{DS}(\omega_0 t)$ and $h_T(\omega_0 t)$ (a) and function $\Pi(\omega_0 t)$ (b) referred to the bottom-left transistor M_1 in Fig. 3.1(b) as functions of the output voltage phase for three different R_D values. V_{out} refers to the differential output voltage V_{out_p}-V_{out_n}.*

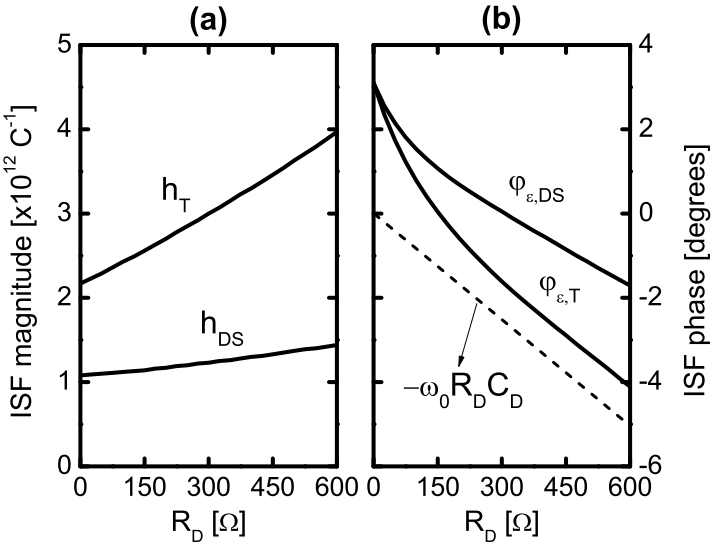


Figure 3.7: *Magnitude (a) and excess phase (b) of first harmonics of $h_T(\omega_0 t)$ and $h_{DS}(\omega_0 t)$ as functions of R_D. Dashed lines refers to the added delay phase, $-\omega_0 R_D C_D$.*

equal to:

$$\varphi_{\epsilon,DS} \cong \frac{G_X - 1}{4Q}. \tag{3.6}$$

However, as R_D increases both the first harmonics of h_T and h_{DS} begin to lag, thus suggesting that, by increasing R_D, an additional delay due to R_D and stray capacitances on the transistor drain nodes comes into play, thus modifying the $\varphi_{\epsilon,DS}$ term appearing in (3.5). To strengthen this theory, the phases $\varphi_{\epsilon,DS}$ and $\varphi_m^{(1)}$ have been computed removing the parasitic capacitance at the drain node of the transconductor transistors. The results are shown in Fig. 3.4 (dashed lines). The two phases weakly depend on R_D, thus confirming that the oscillator non-linearity is mildly dependent on the added drain resistors.

A more quantitative insight can be gained by studying the oscillator model in Fig. 3.8, where the transconductor is followed by a delay block $e^{-j\theta} = e^{-j\omega\tau}$. A simplified analysis may be performed by decoupling the effects of the added delay and transconductor non-linearity.

The first step is to consider the transconductor linear, thus taking $V(t) \cong V_1 \cos(\omega_0 t)$ and $I(t) \cong I_1 \cos(\omega_0 t - \theta)$, and compute the ISF across the tank, $\Gamma_T(\omega_0 t) = \cos\left(\omega_0 t + \frac{\pi}{2} + \varphi_{\epsilon,T}\right)$, relating the phase $\varphi_{\epsilon,T}$ to the loop

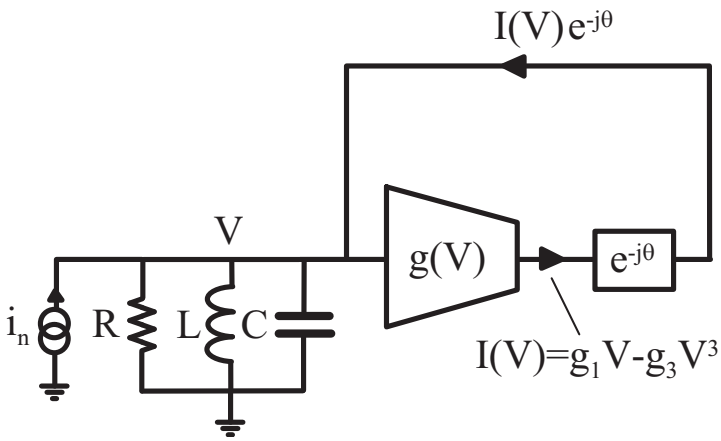


Figure 3.8: *Behavioral model of the oscillator with added delay block, $e^{-j\theta}$, in the feedback path.*

delay.

To this purpose, Fig. 3.9(a) shows the phasors of the fundamental harmonic of the voltage waveform across the tank and of the current delivered by the transconductor. In addition, it highlights two current noise tones injected across the tank at an offset $\pm\omega_m$ from the carrier ω_0 with a φ initial phase. Due to noise injection, the phase of the output voltage is modulated at a frequency ω_m according to:

$$\begin{aligned}\Delta\phi\left(t\right) = \Bigg[\int_{-\infty}^{t} i_n \cos\left[\left(\omega_0+\omega_m\right)\tau+\varphi\right]\cdot h_T\left(\omega_0\tau\right)d\tau \; + \\ + \int_{-\infty}^{t} i_n \cos\left[\left(\omega_0-\omega_m\right)\tau+\varphi\right]\cdot h_T\left(\omega_0\tau\right)d\tau\Bigg] = \\ = i_n\omega_m \sin\left(\varphi-\varphi_{\epsilon,T}\right)\sin\left(\omega_m t\right). \qquad (3.7)\end{aligned}$$

Equation (3.7) emphasizes that for $\varphi = \varphi_{\epsilon,T}$ the two current tones do not modulate the phase of the output voltage. The same condition of no output voltage modulation can be identified referring to Fig. 3.9(b). In fact, if $\varphi = -\theta$ the noise tones do not modulate the phase of the current and therefore no phase modulation of the output voltage arises, if AM-to-PM contribution is neglected. By equating the two conditions, $\varphi = \varphi_{\epsilon,T}$ and $\varphi = -\theta$ it follows that the ISF excess phase $\varphi_{\epsilon,T}$ follows the loop delay $-\theta$.

Regarding the impact of transconductor non-linearity, (3.6) suggests that they cause a positive phase shift between the first harmonic of the ISF and the output voltage. Therefore, by adding the two contributions, $\varphi_{\epsilon,T}$ may

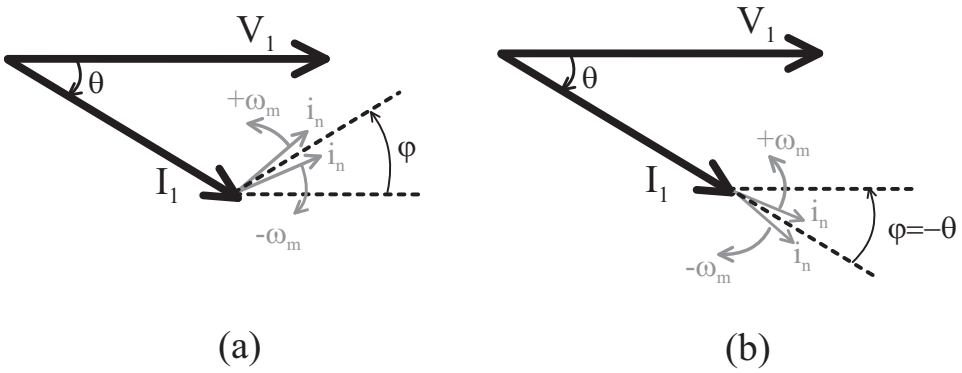


Figure 3.9: *Injection of two current tones at an offset $\pm\omega_m$ from the carrier in the case of loop delay, θ, and linear transconductor (a). The phase of the current is left unchanged if the small tones are applied with initial phase equal to -θ (b)*

be taken as:

$$\varphi_{\epsilon,T} \cong \frac{G_X - 1}{4Q} - \theta. \tag{3.8}$$

The approximation has been verified by means of behavioral simulations. The model in Fig. 3.8 has been implemented in a Cadence environment and linear time-variant simulations (PSS and periodic transfer function (PXF) analyses) have been performed in order to evaluate the phase of the ISF first harmonic. The transconductor was taken with a third-order non-linearity, i.e. $I(V) = g_1 V - g_3 V^3$. In agreement with parameter values met in realistic RF circuits, the tank quality factor and the excess gain, $G_X = g_1 R$, have been set equal to 10 and 3, respectively.

Figure 3.10 shows the dependence of $\varphi_{\epsilon,T}$ on the phase delay θ, which is in good agreement with (3.8). The excess phase, $\varphi_{\epsilon,T}$, is approximately 3° for $\theta = 0^\circ$ and decreases almost linearly as the added delay increases as predicted by (3.8) (dashed line in Fig. 3.10). The dependence of the excess phase on added delay given by (3.8) holds well also if applied to the oscillator in Fig. 3.7(b). In fact, both $\varphi_{\epsilon,_{DS}}$ and $\varphi_{\epsilon,_T}$ decrease following the increasing loop delay, which can be quantified in a first order approximation as $\theta = \omega_0 R_D C_D$.

3.3.2 Effect of loop delay on noise modulating function

Let us now analyze the impact of R_D on the noise modulating function $m(t)$ and on the phase shift of its first harmonic. $\varphi_m^{(1)}$ shows the opposite dependence on drain resistor value with respect to $\varphi_{\epsilon,_{DS}}$, as depicted in

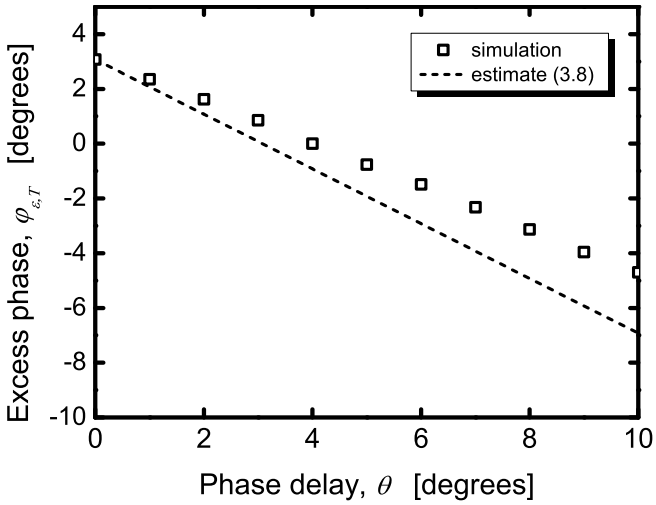


Figure 3.10: *$\varphi_{\epsilon,T}$ as function of added phase delay, θ, for the behavioral oscillator of Fig. 3.8. The dashed line refers to the estimate of $\varphi_{\epsilon,T}$ given by (3.8).*

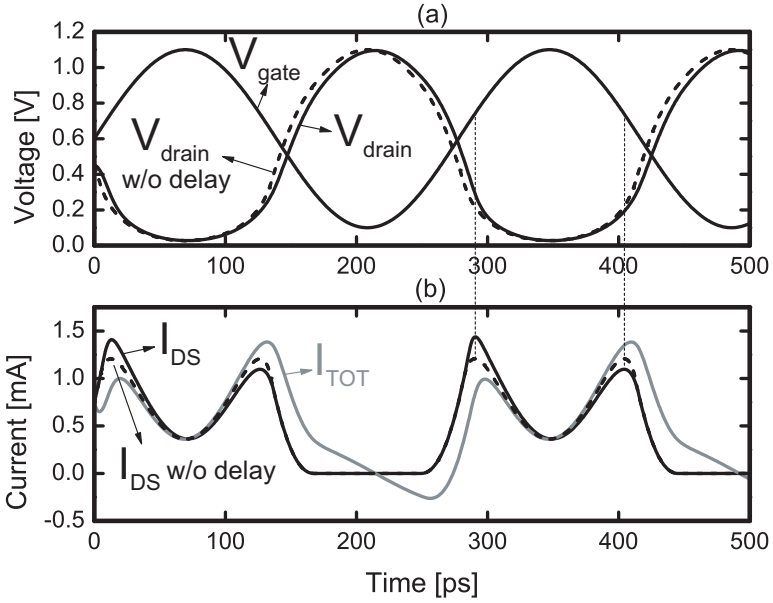


Figure 3.11: *Voltage (a) and current (b) waveforms of M_1 in Fig. 3.1(b). The dashed lines refer to the case without delay, i.e. $C_D = 0$.*

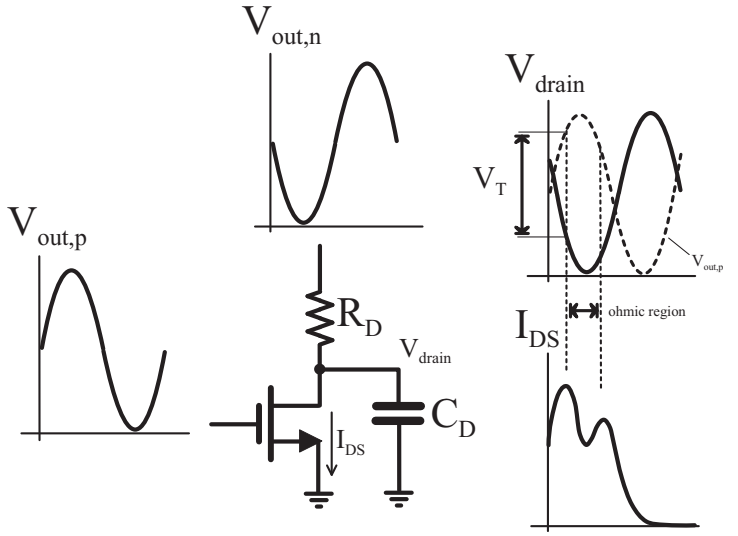


Figure 3.12: *Simplified voltage and current waveforms of the transistor M_1 in Fig. 3.1(b). The transistor current peak occurs at the boundary of the ohmic region. Due to the delay of the voltage waveform at the drain node, the condition $V_{GD} = V_{out,p}$-$V_{drain} = V_{TH}$ is reached for two different gate voltage values: the first occurs at a larger gate voltage, thus implying a larger current.*

Fig. 3.4. By increasing R_D, the first harmonic of $m(t)$ progressively leads the voltage waveform even if the current flowing through the M_1 branch of the transconductor features an increasing phase delay. A qualitative explanation of this trend can be derived by looking at the simulated voltage and current waveforms in Fig. 3.11. Fig. 3.11(a) shows the voltage waveforms at the drain and gate nodes of the transistor M_1 in Fig. 3.1(b), while Fig. 3.11(b) shows the transistor channel current, I_{DS} and the total current, I_{TOT}, flowing through the drain resistor. The latter also includes the current flowing through the stray capacitance. The voltage and current waveforms for $C_{Dn} = 0$ are also shown for reference.

Due to the $R_D C_D$ delay at the drain node, the drain voltage V_{drain} and I_{TOT} are delayed with respect to the case $C_{Dn} = 0$. Note also that by increasing the C_{Dn} value, the transistor channel current I_{DS}, which has a symmetric waveform for $C_{Dn} = 0$, shows a first peak higher than the second one. In fact, the current peak is reached at the boundary of the saturation region, i.e. when the transistor enters or leaves the ohmic region (see Fig. 3.12). This happens when the gate-drain voltage is close to the threshold voltage, i.e. when $V_{GD} = V_{out,p}$-$V_{drain} = V_{TH}$. Thus, due to the delay at the drain node, the condition is verified for two different gate

voltage values and the first current peak is higher since corresponds to a slightly-larger gate voltage. It follows that by increasing the delay, the first harmonic of I_{DS} leads the driving voltage at the gate node. As a result, $\varphi_m^{(1)}$, which can be approximated by the phase of the first harmonic of the transistor channel current according to (2.41), moves towards more positive values as shown in Fig. 3.4, eventually reaching the crossover with $\varphi_{\epsilon,_{DS}}$.

The phase $\varphi_m^{(1)}$ can be quantified resorting to first-order approximations:

- $\varphi_m^{(1)} \cong \varphi_{I_{DS}}^{(1)}$, being $\varphi_{I_{DS}}^{(1)}$ the phase of the first harmonic of the transistor channel current, I_{DS};
- the phase of the transistor channel current is determined when the MOS is in ohmic region, as depicted in Fig. 3.11(b);
- the gate and drain voltages can be expressed as:

$$V_{gate}(t) = \frac{V_{DD}}{2} - A_1 \cos(\omega_0 t) \tag{3.9}$$

$$V_{drain}(t) \cong \left(\frac{V_{DD}}{2} - V_{TH}\right) - A_1 \cos(\omega_0 t - \theta), \tag{3.10}$$

  θ being the phase delay at the drain node equal to $\omega_0 R_D C_D$. Thus, in the expression of the drain voltage we neglect the ohmic drop across the resistance R_D.

Under these approximations, the transistor channel current when M_1 is ohmic can be expressed as:

$$I_{DS} \cong \mu_n C'_{ox} \left(\frac{W}{L}\right)_n (V_{gate} - V_{TH}) V_{drain} \tag{3.11}$$

From (3.9), (3.10) and (3.11) the phase of the first harmonic of I_{DS} can be easily derived as:

$$\varphi_{I_{DS}}^{(1)} \cong \theta \cdot \left(\frac{\frac{V_{DD}}{2} - V_{TH}}{V_{TH}}\right). \tag{3.12}$$

For the considered technology, being $V_{DD} = 1.2\,\mathrm{V}$ and $V_{TH} \cong 0.4\,\mathrm{V}$, it results $\varphi_{I_{DS}}^{(1)} \cong \frac{1}{2}\theta = \frac{1}{2}\omega_0 R_D C_D$.

Finally, taking into account the effect of the transconductor non-linearity, which sets the phase of the transistor current also in the case $R_D = 0$, the phase of the NMF can be approximated as:

$$\varphi_m^{(1)} \cong -\frac{(G_X - 1)^2}{8Q} + \frac{1}{2}\omega_0 R_D C_D, \tag{3.13}$$

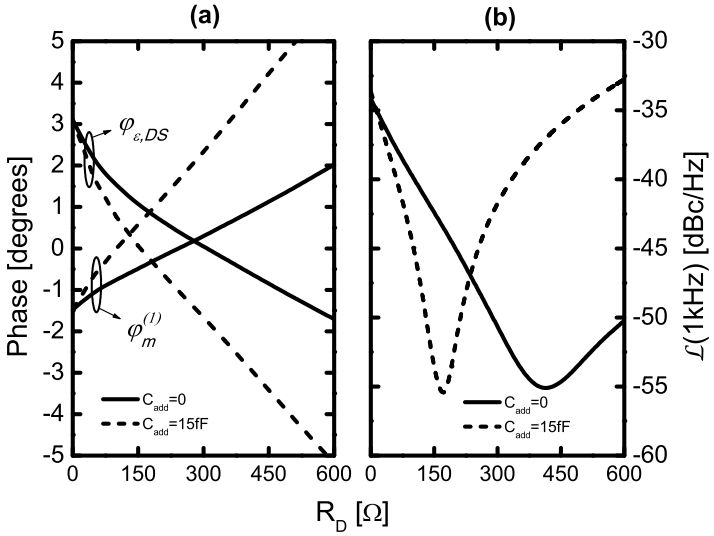


Figure 3.13: *$\varphi_{\epsilon,_{DS}}$ and $\varphi_m^{(1)}$ (a) and phase noise at 1-kHz offset (b) for an added capacitance of 15 fF at NMOS transistor drains (30 fF at p-MOSFET drains), as functions of R_D. For comparison, also the case without added capacitance is shown.*

where (2.59) has been used. Equation (3.13) suggests that the phase of the modulating function depends on the added loop delay. As R_D increases, $\varphi_m^{(1)}$ departs from the negative value set by the Groszkowski effect, eventually becoming positive. For R_D ranging from 0 to $600\,\Omega$ and considering a parasitic capacitance at the n-MOSFET drain node of 7 fF, the estimated phase $\varphi_m^{(1)}$ increases by $2.7°$, in good agreement with the simulation result of $3.5°$ (see Fig. 3.4).

3.3.3 Drain resistor sizing

The analysis reported in the previous sections shows that both phase shifts $\varphi_{\epsilon,_{DS}}$ and $\varphi_m^{(1)}$ depend on the added delay $\omega_0 R_D C_D$. By assuming $\varphi_{\epsilon,DS} \cong \varphi_{\epsilon,T}$ and approximating the modulating function with the transistor channel current, from (3.8) and (3.13) the condition $\varphi_{\epsilon,DS} - \varphi_m^{(1)} = 0$ can be expressed in terms of added loop delay and excess gain:

$$\underbrace{\left[\frac{G_X - 1}{4Q} - \omega_0 R_D C_D\right]}_{\varphi_{\epsilon,DS}} - \underbrace{\left[-\frac{(G_X-1)^2}{8Q} + \frac{1}{2}\omega_0 R_D C_D\right]}_{\varphi_m^{(1)}} = 0 \qquad (3.14)$$

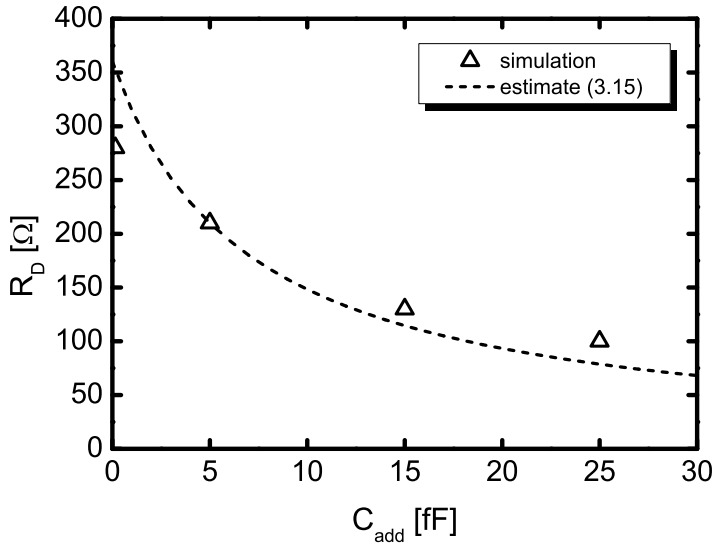


Figure 3.14: *Drain resistance corresponding to $\varphi_{\epsilon,DS}$-$\varphi_m^{(1)} = 0$ for a capacitance C_{add} added at the n-MOSFET drain nodes. For the PMOS transistors $2C_{add}$ is added at the drain terminals. A drain parasitic capacitance of 7 fF is considered for the NMOS transistors (14 fF for p-channel MOSFETs).*

It results that the drain resistance value that allows to suppress the flicker noise up-conversion is:

$$R_D \cong \frac{G_X^2 - 1}{12Q\omega_0 C_D}. \tag{3.15}$$

For the considered oscillator with $G_X = 2.8$, $\omega_0 = 2\pi \cdot 3.6$ Grad/s, $Q = 10$ and $C_D = 7$ fF, the optimum drain resistance results $360\,\Omega$, close to the simulated value (see Fig. 3.4). Other simulations were run by adding extra capacitances of 15 fF at the drain of NMOS transistors and 30 fF at the drain of p-MOSFETs. Fig. 3.13(a) shows the two simulated curves of $\varphi_{\epsilon,DS}$ and $\varphi_m^{(1)}$ as functions of R_D, compared to the two phases in the circuit without extra capacitances. It turns out that by increasing the capacitance value, the phase $\varphi_{\epsilon,DS}$ drops more rapidly and, on the opposite, $\varphi_m^{(1)}$ grows faster, as predicted by (3.8) and (3.13), respectively. The condition $\varphi_{\epsilon,DS} - \varphi_m^{(1)} = 0$ is reached for $R_D \cong 130\,\Omega$, while the estimated optimum resistance is very close and equal to $\cong 115\,\Omega$. This shift of the noise minimum towards lower R_D values is confirmed by the simulated phase noise at 1-kHz offset, shown in Fig. 3.13(b).

Figure 3.14 shows the drain resistance value satisfying the condition $\varphi_{\epsilon,DS}$-$\varphi_m^{(1)} = 0$ as function of added capacitance C_{add}. In this case, C_D

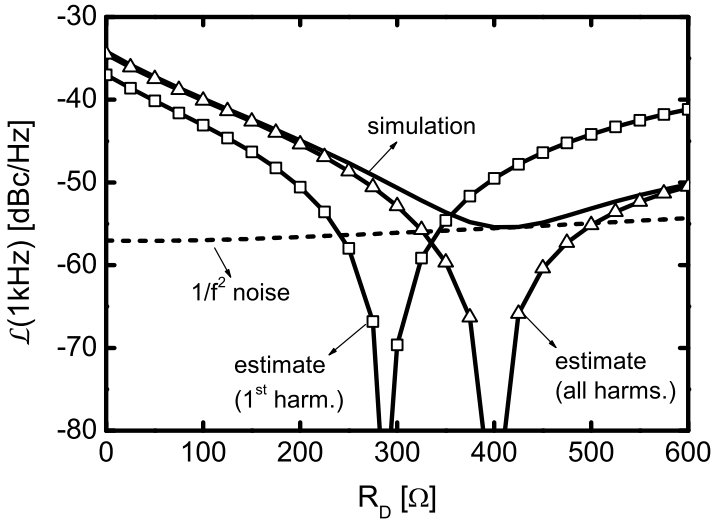


Figure 3.15: *Phase noise at 1-kHz offset as function of the drain resistance R_D. Solid line refers to the SpectreRF PNOISE simulation while dashed line refers to the $1/f^2$ contribution. Triangles and squares refer to the phase noise estimated considering only the first harmonic and all the harmonic terms of the ISF, respectively.*

refers to the total capacitance at the n-MOSFET drain node, being $C_D \cong 7\,\text{fF} + C_{add}$. For comparison, Fig. 3.14 also shows the curve corresponding to the estimated optimum resistance given by (3.15) that confirms the validity of the quantitative analysis so far reported.

Actually, the dependence of the optimum value of R_D on excess gain is less than quadratic. This happens since the phase of the modulating function depends more weakly on G_X with respect to the prediction given by (3.13). Thus, if the oscillation frequency is changed, both the added loop delay $\omega_0 R_D C_D$ and $G_X = g_m R$ vary, being $R = \omega_0 LQ$. This consideration suggests a slight dependence of the optimum resistance value on the oscillation frequency and explains why the proposed method works over a wide tuning range, as shown in Fig. 3.5.

3.3.4 The effect of ISF higher-order harmonics

Figure 3.15 shows the comparison between the simulated $1/f^3$ phase noise at 1-kHz frequency offset (solid line) and its estimate (squares) using (3.5) and considering the simulated phases $\varphi_{\epsilon,DS}$ and $\varphi_m^{(1)}$ in Fig. 3.4. As already pointed out, the minimum of the phase noise occurs at a slightly-larger resistance value. As discussed in Section 2.7.3, the numerical results can

be fully explained by taking into account the impact of higher-order harmonics, since also in this case h_{DS} is not perfectly sinusoidal due to the distortion introduced by the function $\Pi(\omega_0 t)$. Thus, the $1/f^3$ phase noise can be written as:

$$SSCR(\omega_m) = \frac{S_{1/f}(\omega_m)}{8\omega_m^2} \cdot \left[\sum_{k=0}^{+\infty} h_k m_k \cos\left(\varphi_h^{(k)} - \varphi_m^{(k)}\right)\right]^2. \quad (3.16)$$

In (3.16), the $h_{DS}(\omega_0 t)$ functions for NMOS and PMOS transistors have been taken the same. This assumption is reasonable since all transistors are electrically equivalent and the added delay on each drain node has been tailored to be equal. Fig. 3.15 (triangles) shows the $1/f^3$ phase noise at 1-kHz offset obtained by properly summing up all the contributions as in (3.16). The correlated contributions arising from the higher-order harmonics shift the $1/f^3$ phase noise suppression at $R_D = 400\,\Omega$ (for SPICE flicker noise model) where the overall phase noise becomes limited by the $1/f^2$ contribution (dashed line in Fig. 3.15) equal to -55.5 dBc/Hz. The estimate compares very well with the simulation results.

3.3.5 Impact of drain resistors on $1/f^2$ phase noise

The adoption of resistors at the transistor drain nodes is not detrimental in terms of the $1/f^2$ phase noise. In fact, the added drain resistors reduce the oscillation amplitude and are sources of white noise, but, at the same time, they prevent the transistors to load the tank. Their impact on $1/f^2$ phase noise will be quantitatively addressed in the following.

As far the oscillation amplitude concerns, it can be estimated in the proposed oscillator as [33]:

$$A_1 \cong V_{DD} \frac{R}{R + r_{on,p} + r_{on,n} + R_{Dp} + R_{Dn}}, \quad (3.17)$$

where $r_{on,p}$ and $r_{on,n}$ are the resistances of the transistors in deep ohmic region. Clearly, the oscillation amplitude is reduced with respect to the traditional oscillator by a factor of

$$\frac{R + r_{on,p} + r_{on,n} + R_{Dp} + R_{Dn}}{R + r_{on,p} + r_{on,n}}, \quad (3.18)$$

Considering $r_{on,p} = r_{on,n} \cong 80\,\Omega$, $R = 1040\,\Omega$, $R_{Dn} = 345\,\Omega$ and $R_{Dp} = R_{Dn}/2$, this factor is equal to 1.4 and would cause an increase of $1/f^2$ phase

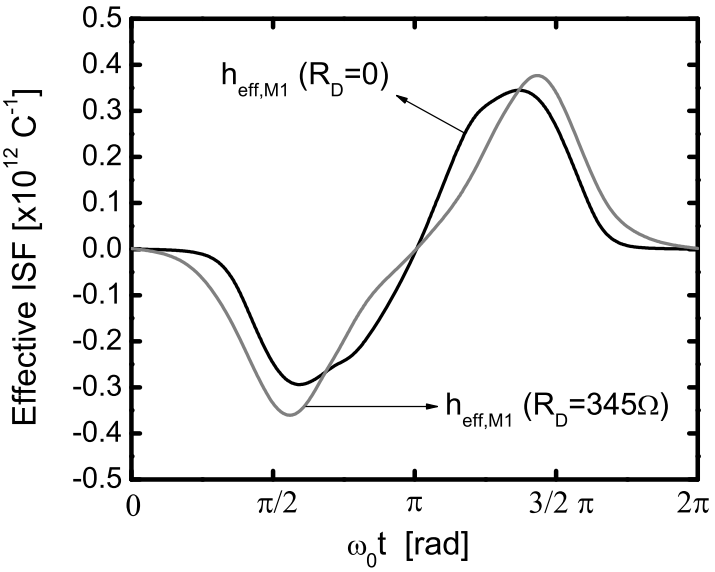


Figure 3.16: *Effective impulse sensitivity functions for the thermal noise current generator of M_1 in the oscillator in Fig. 3.1(a) and in the improved topology of Fig. 3.1(b).*

noise of about $3\,$dB. Additionally, the drain resistors contribute to phase noise with their noisy current. However, this noise is injected only when the corresponding transistor is in deep ohmic region. When this happens, the ISF associated to a generator placed across the resistor terminals is low since it occurs at the negative peak of the differential output voltage. At the zero crossing of the output voltage, instead, the transistors are in saturation and no current noise is injected into the tank.

On the other hand, the drain resistor has a positive effect on transistor noise, since it makes the transistor current noise to re-circulate into the transistor itself when it is ohmic. In other words, the R_D resistor prevents the transistor "to load" the resonator and the noise current to reach the tank. This qualitative analysis is confirmed by observing Fig. 3.16 that shows the effective ISFs corresponding to the white noise current generator of the transistor M_1 in the oscillator of Fig. 3.1(a) and in the improved topology of Fig. 3.1(b). The effective ISF, $h_{eff,M1}$, is the ISF multiplied by the NMF of cyclostationary noise (denoted as $\alpha(t)$ in [37]), i.e. $\sqrt{g_m(t)+g_{ds}(t)}$ in the case of white current noise, divided by the peak value of $\alpha(t)$. In this case, both the effective impulse sensitivity functions have been normalized with respect to the maximum value of the function $\alpha(t)$ corresponding to the transistor M_1 for $R_D = 0$. When the resistor is added at the transistor drain

	$R_D = 0$	$R_D = 345\Omega$
A_1	$1.12\,\mathrm{V}$	$0.791\,\mathrm{V}$
Tank noise	$2.68 \cdot 10^{-13}\,\mathrm{V^2/Hz}$	$2.67 \cdot 10^{-13}\,\mathrm{V^2/Hz}$
NMOS output noise	$4.58 \cdot 10^{-13}\,\mathrm{V^2/Hz}$	$1.98 \cdot 10^{-13}\,\mathrm{V^2/Hz}$
PMOS output noise	$3.85 \cdot 10^{-13}\,\mathrm{V^2/Hz}$	$1.67 \cdot 10^{-13}\,\mathrm{V^2/Hz}$
R_{DN} noise	–	$4.54 \cdot 10^{-14}\,\mathrm{V^2/Hz}$
R_{DP} noise	–	$1.5 \cdot 10^{-14}\,\mathrm{V^2/Hz}$
$\mathcal{L}(1\mathrm{MHz})$	$-117\,\mathrm{dBc/Hz}$	$-116.4\,\mathrm{dBc/Hz}$

Table 3.1: *Output voltage noise contributions at* 1*-MHz offset from carrier with and without the drain resistors.*

node, $h_{eff,M1}$ has a larger peak due to the smaller oscillation amplitude, but is lower when the MOSFET is in ohmic region (for a phase around π, being the differential output voltage a cosine), thus preventing $\mathrm{M_1}$ to load the tank and to inject its current noise. A a result, both effective ISFs have almost the same RMS value, which translates into the same $1/f^2$ phase noise.

To strengthen this theory, Table 3.1 shows the oscillation amplitude, the contributions to the output noise of both active and passive devices and the overall phase noise at 1-MHz frequency offset for the oscillators in Fig. 3.1(a) and Fig. 3.1(b) with $R_D = 345\,\Omega$. Simulation results show that the oscillation amplitude is reduced once the drain resistors are added at the drain nodes by a factor 1.4, as predicted by (3.18). This would lead to an increase of phase noise of about $2.7\,\mathrm{dB}$. However, the output voltage noise due to the transistor is almost halved, thus balancing the voltage amplitude reduction. Moreover, the noise added by the drain resistors is about one order of magnitude lower than the noise due to the active devices and tank loss resistor. This justifies the worsening of $1/f^2$ phase noise limited to only $0.6\,\mathrm{dB}$.

3.4 Measurement results

The proposed technique has been adopted in a 65-nm CMOS VCO, already presented in [33], covering the Italian 3.5-GHz WiMAX frequency band (3.4-$3.6\,\mathrm{GHz}$). The VCO tank features a 4.55-nH inductor while the capac-

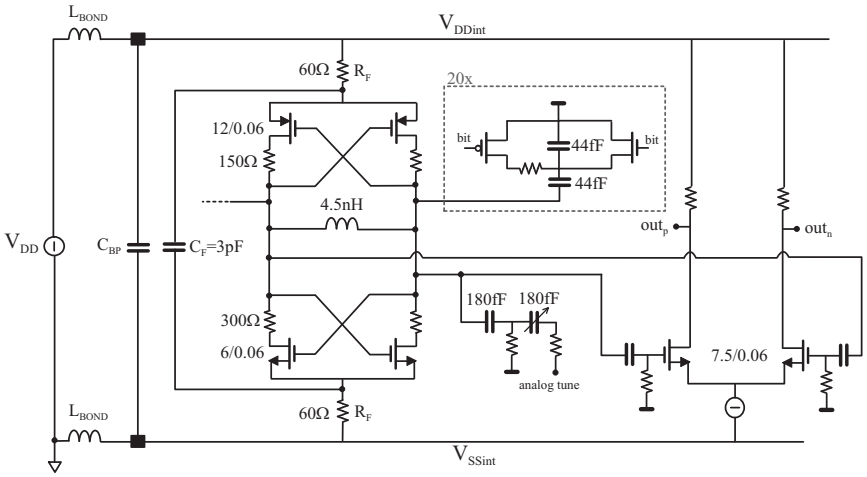


Figure 3.17: *Schematic of the implemented voltage-biased oscillator with drain resistors together with the output buffer.*

itance consists of two banks of 20 switched metal-insulator-metal (MIM) capacitors and two thick-oxide MOS varactors. The tank quality factor is approximately set to 10 by the small-area inductor. In order to bias the oscillation voltage at the middle of the supply rails, the widths of the p- and n-MOSFETs have a ratio of 2. The same ratio applies between their drain parasitic capacitances. As a result, the drain resistors have been scaled accordingly. The transistor width ($W_n = 6\,\mu$m, $W_p = 12\,\mu$m) was chosen to guarantee an excess gain larger than 2 over the whole tuning range. The drain resistors were sized to $R_{Dp} = 150\,\Omega$ and $R_{Dn} = 300\,\Omega$ to equalize the delays at the transistor drain nodes. The simplified schematic is depicted in Fig. 3.17. The VCO core is followed by a differential output buffer, which creates a disturbance at $2\omega_0$ on the supply rail. Note that the $1/f$ noise from the buffer transistors could be up-converted as supply noise around $2\omega_0$, then further down-converted at ω_0 by the VCO switching as $1/f$ amplitude noise across the tank, finally giving rise to $1/f^3$ phase noise. Thus, the network R_F-C_F-R_F was added to filter out the signal at $2\omega_0$, avoiding any residual $1/f^3$ phase-noise contribution. The measured tuning range spans between 3.0 and 3.6 GHz with a maximum power consumption of 0.7 mW from the 1.2-V supply (excluding buffers). A VCO with identical topology but with no drain resistors was also fabricated as reference on the same die. The microphotograph of the die is shown in Fig. 3.18, where VCO1 and VCO2 refer to traditional and modified voltage-biased oscillators, respectively. Note that the resistors R_F have a positive impact in terms of $1/f^3$

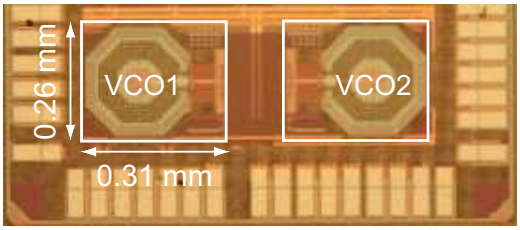


Figure 3.18: *Die microphotograph. VCO1 and VCO2 refer to traditional and modified voltage-biased oscillators, respectively.*

phase noise due to transconductor transistors, since they slightly reduce the oscillator non-linearity lowering the effective power-supply. However, the reduction of flicker-induced phase noise due to these resistors is of about 4 dB. Both the implemented oscillators feature the network R_F-C_F-R_F.

Figure 3.19 shows the phase noise spectra of the two free-running VCOs at 3.57-GHz oscillation frequency. The modified voltage-biased oscillator outperforms the standard topology by about 9 dB at 1-kHz offset. Furthermore, as expected, the $1/f^2$ phase noise of about -114 dBc/Hz at 1-MHz offset is not significantly degraded by the added resistors, leading to a figure of merit (FoM) [66] of about 186 dB.

Figure 3.20 compares the measured and simulated phase noise at 1-kHz and 1-MHz frequency offset along the tuning range in order to quantify both $1/f^3$ and $1/f^2$ contributions. Noise simulations have been run using BSIM4 model for both flicker and thermal noise and the parameters set by the technology specs. Simulation results compare reasonably well with experimental values over the extended 3.0-3.6 GHz range. The experimental trend of the $1/f^3$ phase noise is well captured by simulations from 3.2 to 3.6 GHz even if the actual improvement ranges from 5 to 9 dB, about 3-4 dB less than the numerical expectations. In the frame of flicker-induced phase-noise analysis, the agreement shown in Fig. 3.20 may be considered good taking into account the sensitivity of $1/f^3$ phase noise on the specific flicker noise model and the parameters spread. In fact, even adopting the same noise model, simulations performed on different corners show a 6-dB variation of the phase noise at 1-kHz frequency offset for both the standard and the improved topology. However, the reduction of flicker noise up-conversion is confirmed also varying the process corner.

Finally, the adoption of the drain resistor has a slight benefit in terms of reduction of low-frequency noise from power supply. In fact, the measured sensitivity from power supply, $k_{supply} = \frac{\Delta\omega_0}{\Delta A_1}$ [13], varies from 10 MHz/V

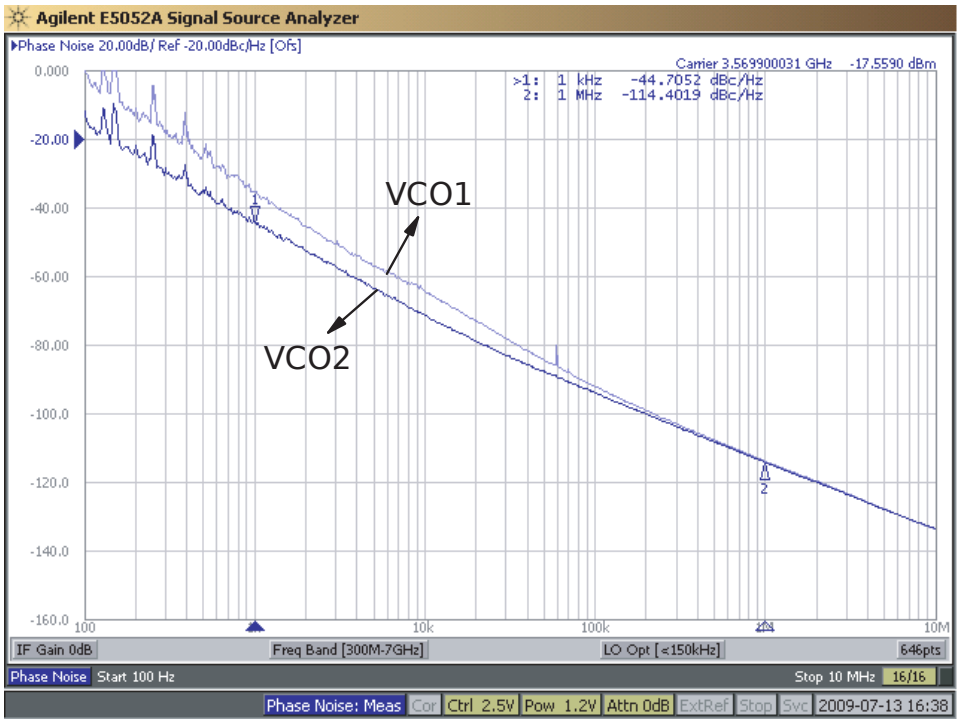


Figure 3.19: *Measured phase noise of VCO1 (upper curve) and VCO2 (lower curve) at the upper-side of tuning range. A noise reduction of about 9 dB is achieved at 1-kHz frequency offset.*

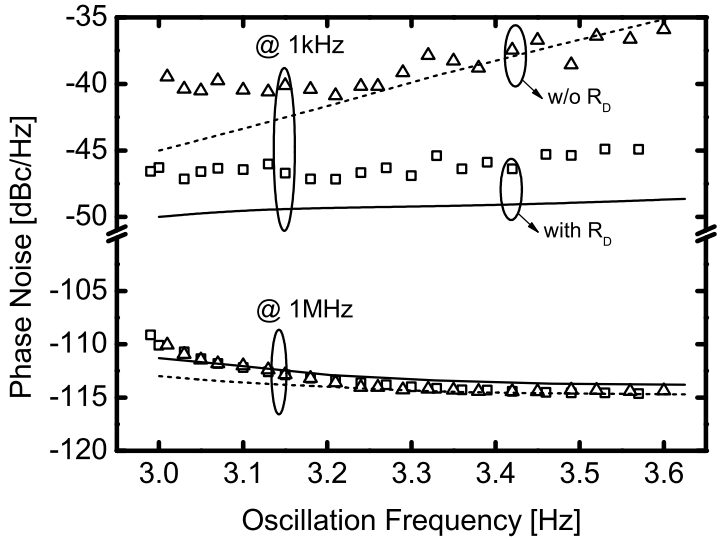


Figure 3.20: *Measured phase noise at* 1*-kHz and* 1*-MHz offset over tuning range for the standard topology (triangles) and the proposed one (squares). Solid and dashed lines refer to the phase noise estimated by post-layout simulations on the oscillator with and without drain resistors, respectively.

to 20 MHz/V along the tuning range for the implemented traditional VCO, while the sensitivity is slightly lower for the improved topology, being in the range 7-15 MHz. In fact, the low-frequency noise from power supply modulates the output voltage common mode and is up-converted by modulating the non-linear capacitances at the output nodes and the bias voltage of the transconductor, thus its non-linearity. Since the non-linear capacitances have been drastically reduced in both oscillators and the non-linearity is only slightly affected by adding the drain resistors, it is likely that the improved oscillator features a mildly lower power-supply sensitivity.

Parameter	[10]	[12]	[16]	[22]	[23]	[14]	this work
Technology	0.13 μm	0.25 μm	0.35 μm [a]	0.18 μm [a]	0.18 μm	0.35 μm	0.065 μm
Frequency (GHz)	5.3	5.15	1.54	5.32	2.22	0.7	3.3
Tuning Range (%)	22.6	21.3	13.7	7.5	0	13.6	18.2
Power Supply (V)	1.2	2.5	2.7	1.8	1.8	1.5	1.2
Power consumption (mW)	24	7.25	16.2	13.5	18.5 [b]	2.55 [c]	0.72
$\mathcal{L}$(1kHz) (dBc/Hz)	-38/-28	-40/-29	-60/-55	-38 [d]	-47	-77/-60	-47/-45
$FoM^{(1/f^3)}$ (dB)	120/112	130/121.5	137/133	126	126	153/137	140.8/141.1
$\mathcal{L}$(1MHz) (dBc/Hz)	-123/-120	-122.5/-118.5	-131/-129	-124 [d]	-122	-142	-110/-114
$FoM^{(1/f^2)}$ (dB)	183/180	189/185	182	188	176	195.4	181/186

[a] BiCMOS
[b] including buffers (VCO core power not available)
[c] off-chip inductor
[d] not available over tuning range

Table 3.2: *Measured performance summary and comparison with recently published low $1/f^3$ phase noise VCOs*

Table 3.2 compares the performance of recently-published oscillators that aim to minimize $1/f^3$ phase noise by means of a new FoM whose definition is theoretically justified in Section 3.6:

$$FoM^{(1/f^3)} = \frac{\omega_0^2}{\mathcal{L}(\omega_m)\,\omega_m^3 I_{DC}}, \tag{3.19}$$

I_{DC} being expressed in mA. The presented VCO shows the best $FoM^{(1/f^3)}$. Only the VCO in [14] has a higher $FoM^{(1/f^3)}$ but it features an off-chip high-Q inductor and the suppression of $1/f$ noise up-conversion is obtained by means of a tail resonant filter, thus making the $1/f^3$ phase noise and its related FoM varying along the oscillator tuning range.

3.5 Design criteria

The analysis reported in the previous sections suggests the criteria to design an oscillator with reduced flicker noise up-conversion without degrading start-up margin and $1/f^2$ phase noise. The oscillator design can be based on the following steps:

- The minimum tank capacitance, C_{min}, is chosen in order to satisfy the requirements on $1/f^2$ phase noise, i.e. $\mathcal{L}(\omega_m)$, [5]

$$C_{min} \cong \frac{kT}{\mathcal{L}(\omega_m)} \frac{\omega_{0_{max}}}{Q} \frac{1+F}{\omega_m^2} \frac{1}{V_{DD}^2}, \tag{3.20}$$

  being $\omega_{0,max}$ the maximum oscillation frequency and F the transconductor noise factor ($F \cong 1$).

- The minimum parallel loss resistance of the tank is determined as:

$$R_{min} = \omega_{0_{min}} LQ, \tag{3.21}$$

  $\omega_{0_{min}}$ being the minimum oscillation frequency, and the overall transconductor g_m is set to assure a reliable start-up at $\omega_{0_{min}}$:

$$g_m = \frac{G_X}{R_{min}} \geq \frac{2}{R_{min}} \tag{3.22}$$

- Assuming n- and p-channel MOSFETs sized in order to balance their different mobility ($\mu_n(W/L)_n = \mu_p(W/L)_p$), the n-MOSFETs can be designed with aspect ratio equal to:

$$\left(\frac{W}{L}\right)_n \cong \frac{g_m}{\mu_n C'_{ox}\left(\frac{V_{DD}}{2} - V_{TH}\right)}. \tag{3.23}$$

- After determining the value of the parasitic capacitance, C_D, at the drain of the NMOS transistors, the drain resistance is derived from (3.15) as:

$$R_D \cong \frac{G_X^2 - 1}{12Q\omega_{0_{min}}C_D}. \tag{3.24}$$

  which minimizes flicker noise up-conversion.

  Clearly, it must be $R_{Dn} = R_D$ and $R_{Dp} = \frac{1}{2}R_D$ in order to have the same delay at NMOS and PMOS drain nodes.

- The value of R_D given by (3.24) must fulfill the condition $\Delta V_R \leq V_{TH}$, ΔV_R being the ohmic drop across the drain resistor at DC bias, which assures the transistor to be in the saturation region. If this condition is not verified, C_D has to be increased in order to accommodate a smaller value of R_D.

As $1/f^3$ phase noise minimization is obtained thanks to a proper value of the delay R_DC_D introduced in the oscillator loop, the resistor value can always be kept low by choosing the appropriate value of C_D. This option may be useful when high current consumption and low $1/f^2$ phase-noise oscillators is required. In this case, there may be no need of extra capacitances at drain nodes. In fact, the equivalent parallel tank loss resistance scales and transistor widths have to be accordingly increased to achieve the same excess gain, resulting into larger parasitics.

To further demonstrate this point, we adopted the proposed technique to design a 3.6-GHz voltage-biased oscillator featuring 10 times higher power consumption with respect to the reference oscillator but with the same tank quality factor Q of 10. The drain resistors were sized as $R_{Dn} = 35\,\Omega$ and $R_{Dn} = R_{Dn}/2$, preventing the transistors to enter the ohmic region at the start-up. Due to the higher current drawn by the VCO, the transistors were sized with $W_n = 60\,\mu$m and $W_p = 2W_n$. Thus, there was no need to add a capacitor at the drain nodes of the devices since the parasitic capacitance itself is sufficient to create the proper delay with the adopted resistors. The simulated phase noise at 1-MHz offset is -127 dBc/Hz for both the classical voltage-biased oscillator and the proposed topology. In the $1/f^3$ region, the conventional oscillator features -42 dBc/Hz at 1-kHz offset, while it reduces to -62 dBc/Hz in the improved topology.

3.6 Definition of a figure of merit for $1/f^3$ phase noise

In this chapter, a theoretical framework is provided to the definition of the figure of merit for flicker-induced phase noise, $FoM^{(1/f^3)}$, adopted in Section 3.4. Although flicker-induced phase noise is of great concern in oscillators and can worsen the performance of the whole synthesizer, such a FoM has never been introduced in literature to compare different VCOs to the best of our knowledge. However, it is reasonable to assume that such a figure of merit has to be similar for the classical FoM derived for $1/f^2$ noise [66]. In fact, the $1/f^3$ phase noise is still a phase fluctuation, so it is expected to scale as ω_0^2 and with the power absorbed by the tank. On the other hand, flicker-induced phase noise is proportional to current, while white-induced one depends only on tank losses [41].

Equation (3.5), which expresses the $1/f^3$ phase noise in a general case, suggests that:

- $1/f^3$ phase noise is proportional to the flicker noise current tones upconverted around the fundamental carrier, i.e.,

$$S_I\left(\omega_0 \pm \omega_m\right) \propto \frac{K_F^n}{C_{ox}' L_{MOS}^2} \frac{I_1}{\omega_m}, \tag{3.25}$$

  I_1 being the magnitude of the first harmonic of the transistor current. For simplicity, we have considered the exponent α in SPICE flicker noise model in (2.23) equal to 1.

- Only a small fraction of these noise components gives rise to a phase modulation of the output voltage, this fraction being proportional to the term $\sin\left(\varphi_m^{(1)} - \varphi_\epsilon\right)$ in (3.5). Thus, the PM current noise components around the carrier have a power spectral density given by:

$$S_I^{PM}\left(\omega_0 \pm \omega_m\right) = S_I\left(\omega_0 \pm \omega_m\right) \cdot \sin^2\left(\varphi_m^{(1)} - \varphi_\epsilon\right). \tag{3.26}$$

- The PM current tones determine a phase modulation of the output voltage being multiplied by the lossless tank impedance,

$$\left|Z\left(j\left(\omega_0 \pm \omega_m\right)\right)\right| = \frac{1}{2\omega_m C}, \tag{3.27}$$

  resulting in:

$$V_n^2\left(\omega_0 \pm \omega_m\right) \propto S_I\left(\omega_0 \pm \omega_m\right) \cdot \left(\frac{1}{2\omega_m C}\right)^2. \tag{3.28}$$

- The amplitude of the carrier is proportional to the tank loss resistance, $R = \frac{Q}{\omega_0 C}$, and I_1, i.e.,

$$A_1 \propto \frac{QI_1}{\omega_0 C}. \tag{3.29}$$

Taking into account the above mentioned considerations, the flicker-induced phase noise can be written as:

$$\mathcal{L}(\omega_m) = \frac{2V_n^2(\omega_0 \pm \omega_m)}{A_1^2} \propto \frac{\omega_0^2}{\omega_m^3 Q^2 |I_1|}. \tag{3.30}$$

The current I_1 flowing into the transistors and in the tank is proportional to the average current drawn by the power-supply, I_{DC}, i.e.,

$$I_1 = \gamma I_{DC}, \tag{3.31}$$

γ being the current efficiency of the oscillator which quantifies how much the oscillator is prone to convert the average power-supply current into a first-harmonic current to be delivered to the tank. Note that a similar argument has been adopted in [66] to derive the figure of merit for the $1/f^2$ phase-noise. In this case, the phase noise is inversely proportional to the power absorbed by the resonator, RI_1^2 which is linked to the overall power consumption through the oscillator power efficiency. Note that this analysis is also valid for a current-biased VCO. In such oscillator topology, the flicker noise current from the tail generator is mixed by the switching action of the transconductor resulting into correlated current tones around the carrier, as well in a voltage-biased oscillator it is the cyclostationary operating point of the coupled-pair transistors that up-converts the flicker noise current around the carrier.

In conclusion, these considerations suggest a dependence of $1/f^3$ phase noise on current consumption rather than on power consumption, differently to $1/f^2$ phase noise. Finally, like for the $1/f^2$ phase noise, the dependence of the phase noise on tank quality factor is not taken into account. Thus, the FoM for $1/f^3$ phase noise can be defined as:

$$FoM^{(1/f^3)} = \frac{\omega_0^2}{\mathcal{L}(\omega_m)\,\omega_m^3} \cdot \frac{1\,\text{mA}}{I_{DC}}. \tag{3.32}$$

3.7 Conclusions

By adopting resistors in series to the drain nodes of the transconductor transistors, the up-conversion of flicker noise in a voltage-biased oscilla-

tor can be effectively reduced. The resistors, together with the parasitic drain capacitance, introduce a delay in the loop gain shifting both the ISF and the current waveform of the MOSFETs. It follows that $1/f$ noise up-conversion can be properly reduced by judiciously tailoring the component values without degrading the start-up margin or adopting resonant filters. In this chapter, a theoretical explanation and a quantitative analysis have been carried out addressing in details the different effects and a comparison has been made between numerical results and experimental measurements on a 65-nm CMOS VCO. Finally, the figure of merit for the flicker-induced phase noise, $FoM^{(1/f^3)}$, is introduced allowing to compare oscillators featuring different oscillation frequency and current consumption. Adopting this FoM, the presented oscillator outperforms other integrated VCOs with reduced flicker noise up-conversion.

CHAPTER 4

An efficient simulation technique to compute the impulse sensitivity function in oscillators

4.1 Introduction

The knowledge of the impulse sensitivity function $h(t)$ allows the designer not only to calculate the phase noise arising from a specific noise source, but also to gain insight in the phase-noise generation mechanisms [41, 67–71].

Despite the usefulness of this function in circuit design, commercial circuit simulators do not automatically calculate the $h(t)$ yet, which needs instead to be determined via repeated transient analyses [37]. Numerical techniques to compute the $h(t)$ components have been studied in the literature [55, 72] and developed in specialized software codes. However, to the best of our knowledge, they are not implemented in widely-employed commercial computer-aided design (CAD) tools.

This chapter presents a fast and accurate simulation technique to evaluate the impulse sensitivity function of an oscillator. The proposed method,

based on the LTV analysis of oscillators, computes the impulse phase response by means of periodic steady-state and periodic transfer function simulations available in commercial simulators (Spectre, Eldo, etc.). This technique overwhelms the classical simulation method based on transient analysis and injection of charge pulses both in terms of speed and precision. The good accuracy of the proposed method has been verified in several oscillator topologies, namely a voltage-biased, a ring and a current-biased oscillator.

The simulation method can be further extended to compute also the noise modulating function and, thus, the phase noise induced from cyclostationary noise sources.

This chapter briefly reviews the traditional transient-based simulation method proposed by Hajimiri and Lee. Section 4.3 describes the proposed method to simulate the ISF by means of periodic small-signal analysis. Section 4.4 shows the comparison between the PXF and transient analysis-based methods in terms of implementation simplicity and simulation speed in a voltage-biased LC and a ring oscillator, highlighting the advantages of the proposed technique. Finally, conclusions are drawn in Section 4.6.

4.2 The traditional method

The simulation method reported in [37] is directly derived from the theoretical background developed in the same paper. Let $V_0(t)$ be the unperturbed output voltage of the oscillator. According to theory presented in Section 1.6.1, when a charge pulse $i_n(t) = \Delta q \cdot \delta(t - \tau)$ is injected at instant $t = \tau$ within the circuit, a perturbation of both oscillation amplitude and phase occurs. $h(\tau)$ is given by $\frac{\Delta\phi(\tau)}{\Delta q}$, where $\Delta\phi$ is the asymptotic output phase shift. The required steps for computing $h(\tau)$ are the following:

1. Run a transient simulation of the unperturbed oscillator and annotate a time instant t_{ref} when the output voltage crosses an arbitrarily-chosen value V_{ref}, once the initial transient has faded. Referring to Fig. 4.1, V_{ref} has been chosen equal to 0.

2. Apply a short current pulse of area Δq at instant τ at the nodes where the current noise source is located and run a new transient simulation. Once the oscillation amplitude has returned to the steady-state value, if the induced phase shift is much smaller than 2π, the output voltage will cross V_{ref} at the instant t_1 close to t_{ref} (see Fig. 4.1).

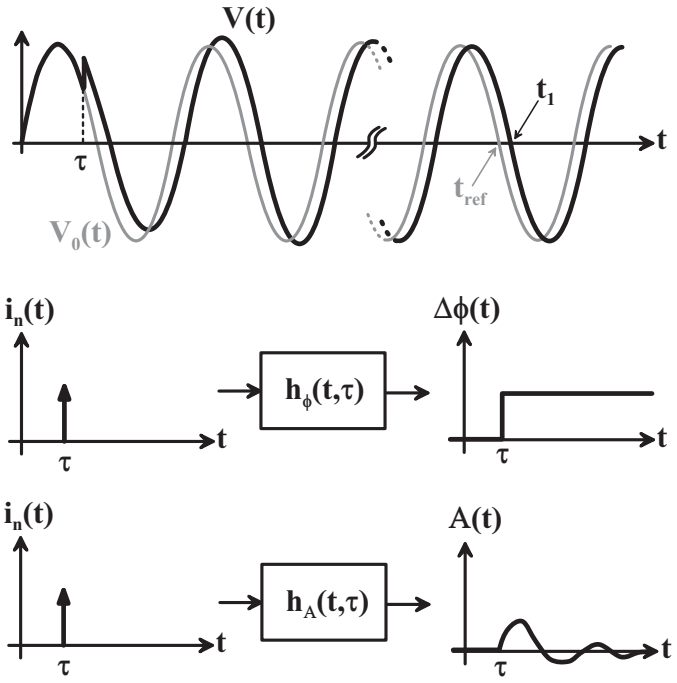


Figure 4.1: *Waveforms of perturbed and unperturbed output voltage, $V_0(t)$ and $V(t)$, respectively.*

3. The phase shift $\Delta\phi$ is obtained as $\Delta\phi = \omega_0 (t_{ref} - t_1)$, resulting in $h_\phi(\tau) = \frac{\Delta\phi}{\Delta q}$.
4. By sweeping the injection time instant τ over one oscillation period, the time waveform of $h(t)$ can be obtained. The more accuracy is needed, the more transient simulations must be run.

Despite its simplicity, this procedure has several drawbacks. The most important is that it is hard to be performed in a completely-automatic way. This is because a manual calibration of several parameters occurs before simulation. As it will be more clear in Section 4.4, these parameters are the amount of the injected charge Δq and the time accuracy of transient analyses.

In [37], an analytical method to compute the above mentioned phase shift and thus the phase sensitivity function is proposed. A current impulse applied to the *i*-th node of the oscillator causes an initial change $\Delta V_i = \Delta q / C_i$ of the node voltage and an excess phase equal to:

$$\Delta\phi_i = \omega_0 \frac{\Delta q}{C_i} \frac{\dot{v}_i}{|\overrightarrow{\dot{v}_i}|^2}, \tag{4.1}$$

being Δq the excess charge on the node capacitor C_i, ω_0 the oscillation frequency, $\dot{v}_i$ the time derivative of the *i*-th node voltage and $|\dot{\vec{v}_i}|^2$ the norm of the first derivative of the waveform vector.

Equation (4.1) refers to oscillators where state variables are node voltages, while the reader can find in [73] how (4.1) can be applied in the case of an LC oscillator whose state variables are capacitor voltage and inductor current. It should be noted that (4.1) is not correct in general, since it assumes that noise perpendicular to state-space trajectory of the oscillator does not generate any phase noise [73, 74]. In particular, (4.1) leads to incorrect determination of the ISF each time amplitude to phase noise conversion takes place in the oscillator, as verified in Section 4.4 by an appropriate simulation.

4.3 The proposed method

The method proposed in this chapter derives the oscillator impulse phase response in the frequency domain by means of a PXF analysis available in commercial RF circuit simulators. Let us consider the output voltage of the unperturbed oscillator at the fundamental frequency as:

$$V(t) = A_0 \cos(\omega_0 t + \theta),$$

θ being the initial phase of the sinusoid. The ISF to be evaluated can be expanded into a Fourier series:

$$h(t) = \frac{h_0}{2} + \sum_{k=1}^{+\infty} h_k \cos(k\omega_0 t + \varphi_k), \tag{4.2}$$

where h_k and φ_k are the magnitude and the phase of the k-th harmonic term, respectively. In (4.2), h_0 is the DC component of the impulse sensitivity function that can be either a positive or a negative value.

In this frame, a small current tone at an offset $-\omega_m$ around the k-th harmonic of the output voltage, that is:

$$i_n(t) = i_n \cos\left[(k\omega_0 - \omega_m)\, t\right], \tag{4.3}$$

causes a phase modulation at ω_m of the output voltage. In fact, from (2.18), (4.2) and (4.3), the corresponding output phase can be approximated by the slow-frequency component:

$$\Delta\phi(t) \cong \frac{h_k i_n}{2\omega_m} \sin(\omega_m t + \varphi_k). \tag{4.4}$$

Note that only the k-th harmonic term of the ISF contributes to determine the output phase $\Delta\phi(t)$. Thus, the output voltage around the fundamental frequency, $V(t) = A_0 \cos[\omega_0 t + \theta + \Delta\phi(t)]$, shows two correlated terms at $\omega_0 \pm \omega_m$, that is:

$$\begin{cases} V(t) \cong A_0 \cos(\omega_0 t + \theta) + v_u(t) + v_l(t) & (4.5) \\ v_u(t) = v_k^{PM} \cos\left[(\omega_0 + \omega_m)\, t + \Phi_k^+\right] & (4.6) \\ v_l(t) = v_k^{PM} \cos\left[(\omega_0 - \omega_m)\, t + \Phi_k^-\right], & (4.7) \end{cases}$$

where:

$$\begin{cases} v_k^{PM} = \dfrac{A_0 h_k i_n}{4\omega_m} & (4.8) \\ \Phi_k^+ = \theta + \varphi_k & (4.9) \\ \Phi_k^- = \pi + \theta - \varphi_k. & (4.10) \end{cases}$$

These equations pose the basis of the numerical methodology to derive the ISF function by means of a PXF simulation, which computes the magnitude and the phase of the periodic small-signal transfer function from the single current tone in (4.3) at frequency $k\omega_0 - \omega_m$ to the output voltage at frequency $\omega_0 + \omega_m$. Denoting with $\overrightarrow{i_n}$ the phasor associated to the input current in (4.3) and with $\overrightarrow{v_u}$ and $\overrightarrow{v_l}$ those associated to the upper and lower side-tones in (4.6) and (4.7), respectively, the PXF analysis computes the transfer functions:

$$\begin{cases} \overrightarrow{X_u} = \dfrac{\overrightarrow{v_u}}{\overrightarrow{i_n}} = \dfrac{A_0 h_k}{4\omega_m} e^{j\Phi_k^+} & (4.11) \\ \overrightarrow{X_l} = \dfrac{\overrightarrow{v_l}}{\overrightarrow{i_n}} = \dfrac{A_0 h_k}{4\omega_m} e^{j\Phi_k^-}, & (4.12) \end{cases}$$

where (4.8) has been used.

Finally, from (4.9) and (4.11), the magnitude and the phase of the *k*-th harmonic term of $h(t)$ can be derived as:

$$\begin{cases} h_k = \dfrac{4\omega_m}{A_0} \cdot \left|\overrightarrow{X_u}\right| & (4.13) \\ \varphi_k = \angle\overrightarrow{X_u} - \theta. & (4.14) \end{cases}$$

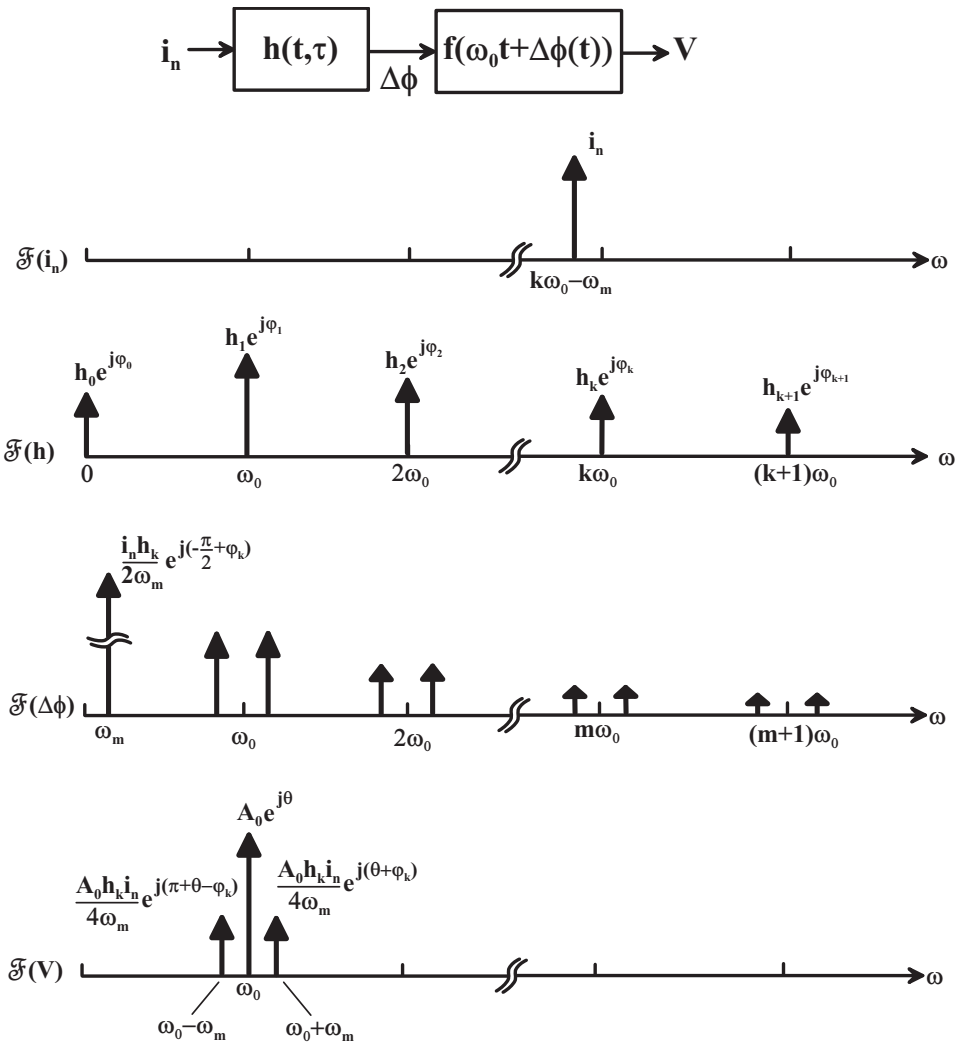


Figure 4.2: *Spectra of injected current tone, impulse sensitivity function, output phase and output voltage.*

In the case of the $h\,(t)$ DC component, φ_0 can be either 0 or π. The index k is an integer number automatically swept by the simulator between 0 and N, where N can be limited to 5-6 for sinusoidal oscillators. In the above mentioned equations, A_0 and θ are the magnitude and the initial phase of the first harmonic of the output voltage, respectively, and can be estimated through a single PSS simulation.

Finally, note that the PXF simulation is a linear analysis, meaning that the circuit is linearized around the time-varying operating point, thus avoiding the problem of large injected signal occurring when performing transient analysis. Figure 4.2 shows the spectra of the injected current tone $i_n\,(t)$, $h\,(t)$, output phase $\Delta\phi\,(t)$ and modulated output voltage $V(t)$.

The computation of the ISF is greatly simplified for both conventional and proposed method using a simulation environment that supports scripting, such as Cadence OCEAN [75]. However, it must be pointed out that while adopting the PXF-based technique the results can be achieved in a completely-automatic way, the transient analysis-based method requires a careful setting of the simulation parameters to get accurate results. In particular:

- the injected charge must be chosen in order to be sufficiently large to avoid the numerical error to become significant and sufficiently small to assure a linear relationship between charge and phase;

- a sufficient number of periods must be simulated to allow the amplitude transient to be over after the injection of the pulse;

- a minimum number of samples per period and a maximum tolerance (*strobeperiod* and *errpreset* parameters in Spectre simulator) are required to achieve the desired accuracy.

Such parameters, however, can hardly be determined *a priori*, thus implying the need for a manual calibration. The error arising from these issues will be quantitatively addressed in Sections 4.4.1 and 4.4.2.

```
PI=3.141592653589793
f0=1G ;Oscillation frequency
fm=1k ;Offset frequency
wm=2*PI*fm

;Set up the two analyses
analysis('pss ?fund sprintf( nil "%g" f0) ?harms "10" ?errpreset "
    conservative"
    ?tstab "80n" ?p "/outp" ?n "/outn")
analysis('pxf ?p "/outp" ?n "/outn" ?sweeptype "relative"
    ?relharmnum "1" ?start sprintf(nil "%g" fm) ?stop "" ?maxsideband
        "20" )

run()

;Compute oscillation amplitude and initial phase
A0 = mag(harmonic((v("/outp" ?result "pss_fd") - v("/outn" ?result "pss_fd
    ")) '(1)))
theta = phaseDegUnwrapped(harmonic(v("/outp" ?result "pss_fd") '(1)))

;Compute harmonic coefficients of ISF
h0 = mag(harmonic(getData("in" ?result "pxf") '(-1)))*4*wm/A0
phih0 = mag(phaseDegUnwrapped(harmonic(getData("in" ?result "pxf") '(-1)))
    -theta)

h1 = mag(harmonic(getData("in" ?result "pxf") '(0)))*4*wm/A0
phih1 = -phaseDegUnwrapped(harmonic(getData("in" ?result "pxf") '(-2)))-
    theta-theta

h2 = mag(harmonic(getData("in" ?result "pxf") '(1)))*4*wm/A0
phih2 = -phaseDegUnwrapped(harmonic(getData("in" ?result "pxf") '(-3)))-
    theta-theta*2

...
```

Listing 1: *Lines of Cadence OCEAN code for the simulation of the ISF.*

Listing 1 shows sample lines of Cadence OCEAN code to implement the proposed method. The simulation of the ISF is achieved by computing magnitude and phase of each Fourier coefficients by means of (4.13) and (4.14). By subtracting $k \cdot \theta$ from each phase φ_k allows to refer the ISF to an output voltage whose first harmonic is a cosine function. This can be particularly useful when the noise modulating function is also needed for phase noise computation, and thus synchronization between the two functions must be guaranteed. This is not straightforward, since the NMF is obtained by means of a different simulation method, as it will be shown in Section 4.5.

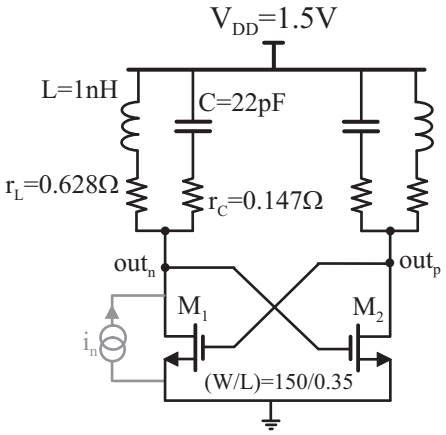


Figure 4.3: *The simulated voltage-biased LC oscillator.*

4.4 Simulation results

4.4.1 The impact of the amount of injected charge

The proposed computation method for the derivation of $h(t)$ has been verified by means of a comparison with the Hajimiri's technique in two oscillator topologies. The impact of the value of the injected charge in the transient-based method is also highlighted. The benchmark topologies are the voltage-biased LC and the ring oscillator shown in Fig. 4.3 and Fig. 4.4, respectively. Both oscillators are designed in a 0.35-μm CMOS technology and run at 1-GHz frequency.

In the voltage-biased LC oscillator the ISF is simulated for a current noise source connected between one of the output and ground, as shown in Fig. 4.3. Figure 4.5 shows a comparison between the results obtained with the PXF and transient analysis-based methods, the latter being performed with three different values of the ratio between the injected charge Δq and the maximum charge q_{max} stored in each tank capacitor. In particular, a perfect matching between the results of the two methods is achieved for a $\Delta q/q_{max}$ ratio equal to 10^{-2}. As the injected charge approaches q_{max} (ratio equal to 0.5 in Fig. 4.5), the resulting ISF is distorted, while, as the ratio is lowered to 10^{-5}, the resulting waveform is affected by numerical error.

In order to verify that phase sensitivity function resulting from (4.1) can lead to an incorrect result, the oscillator in Fig. 4.3 has been simulated adopting as tank capacitors two accumulation PMOS varactors with the same capacitance value (22 pF). Thus, due to the non linear C-V charac-

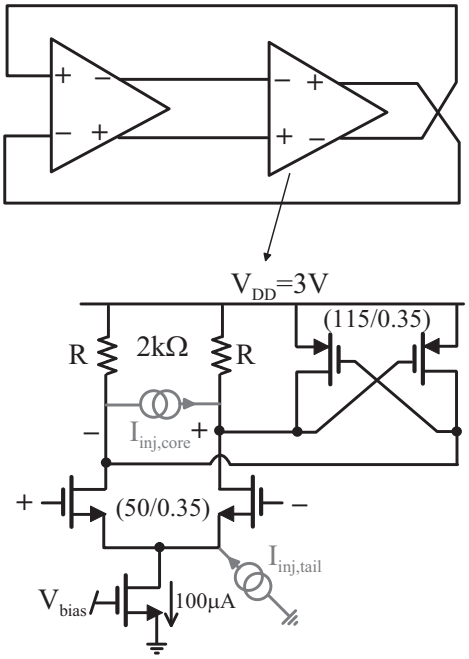


Figure 4.4: *The simulated ring oscillator.*

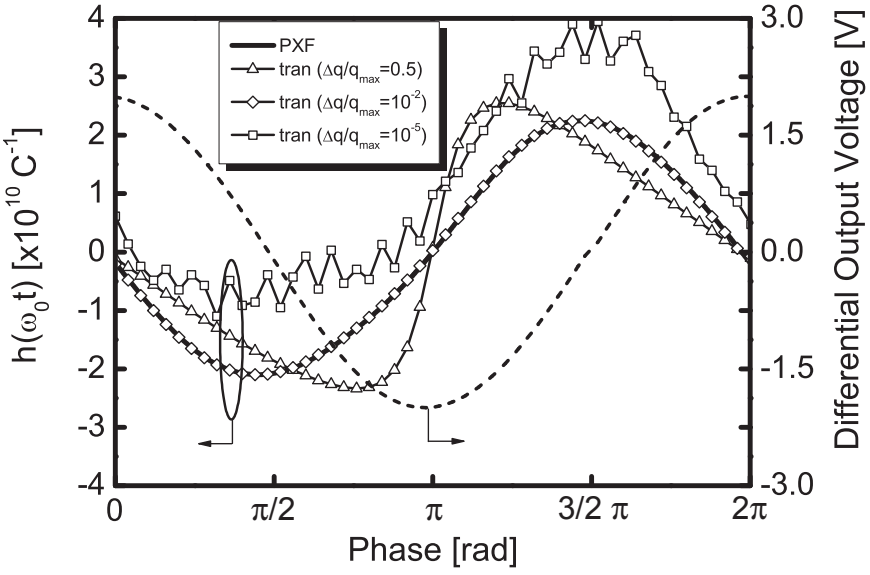


Figure 4.5: *Simulated ISF of the voltage-biased LC-tuned oscillator in Fig. 4.3 using the proposed PXF and transient analysis-based methods.*

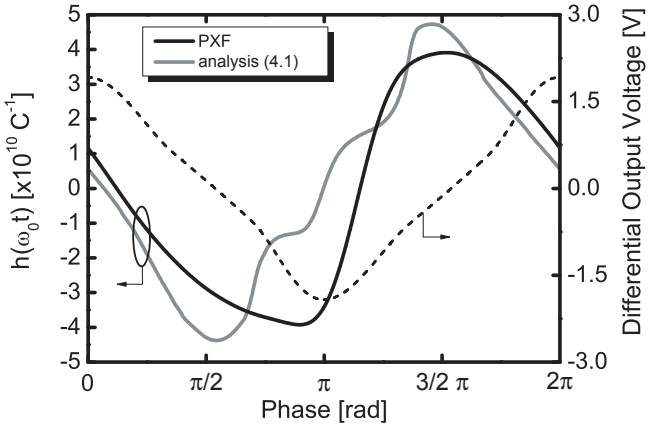


Figure 4.6: *Simulated ISF of the voltage-biased LC oscillator in Fig. 4.3 adopting as tank capacitor an accumulation PMOS varactor featuring a gain of* $500\,MHz/V$*. Equation (4.1) leads to an incorrect estimation of the sensitivity function.*

Topology	Simulation Time (transient)	Simulation Time (PXF)
Voltage-biased LC	6m 41s	5s
Ring	7m 40s	6s

Table 4.1: *ISF simulation time*

teristic of the varactors, the VCO is affected by an AM-to-PM conversion mechanism [11]. Fig. 4.6 shows the phase sensitivity evaluated via the PXF-based method and by means of (4.1). The latter estimation confirms the incorrect prediction of the closed-form formula reported in [37].

Finally, the ring oscillator of Fig. 4.4 has been considered as case study. The ISF has been evaluated for the tail current noise source and for a noise source across the differential output, namely $I_{inj,tail}$ and $I_{inj,core}$. The results, plotted in Fig. 4.7, suggest a perfect matching between the ISF waveforms obtained with the two above mentioned methods.

Table 4.1 reports a comparison between the ISF simulation times for the two methods in both oscillators. The simulations have been performed in the Cadence OCEAN environment with a 3-GHz Pentium Xeon featuring a 4-Gbyte main memory. A total of 50 ISF samples over one oscillation period have been computed by means of transient analyses. Each analysis has been run for 200 oscillation periods, injecting the current pulse in the middle of the simulation time, with the following accuracy parameters: *reltol*$= 10^{-6}$ and *errpreset*='conservative' [76]. Regarding the PXF-based

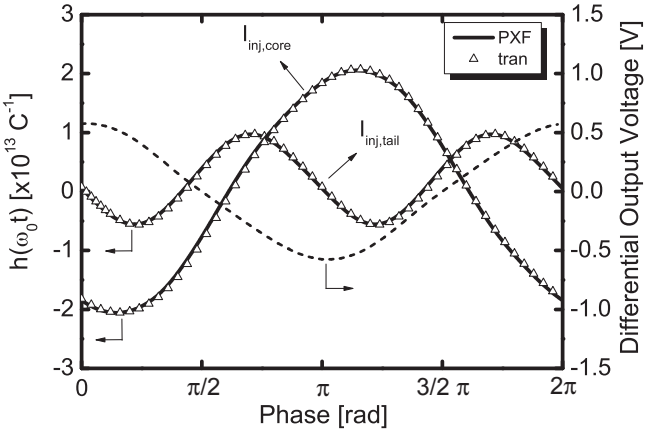


Figure 4.7: *Simulated ISFs of the ring oscillator in Fig. 4.4 using the proposed and transient analysis-based simulation method.*

method, the PSS stabilization time (*tstab*) has been set equal to 100 periods (with the same accuracy parameters) and 20 harmonic terms have been computed. The computation time with the transient analysis-based method is approximately 80 times larger than adopting the proposed simulation technique.

4.4.2 The impact of the simulated points per period

In this section, the trade-off between speed and accuracy affecting the method based on transient analyses is highlighted. As a benchmark circuit, the current-biased LC oscillator shown in Fig. 4.8 is adopted. The oscillator is designed in a 65-nm CMOS technology with the following parameters: $L = 2\,\text{nH}$, $C = 1.6\,\text{pF}$ and variable MOS capacitance C_v spanning from $0.2\,\text{pF}$ to $0.6\,\text{pF}$, so that the oscillation frequency f_0 can be tuned from $2.45\,\text{GHz}$ to $2.65\,\text{GHz}$. The resonator quality factor is $Q = 5$ at $2.5\,\text{GHz}$, the current drawn from the voltage supply $V_{DD} = 2.5\,\text{V}$ is $5\,\text{mA}$ and the voltage waveform across the LC tank $out_p(t) - out_n(t)$ has a peak-to-peak value of about $2.0\,\text{V}$. The MOSFET devices are described by BSIM4 models with parameters of an existing technology process.

In this circuit, the ISF functions related to the input current $i_1(t)$ and $i_2(t)$ in Fig. 4.8 are first computed by means of the two methods. The $h(t)$ functions resulting by adopting a PSS/PXF analysis are shown as solid lines in Fig. 4.9. The CPU time required by the proposed method to derive each ISF curve is of the order of $10\,\text{s}$. These results are validated by means of

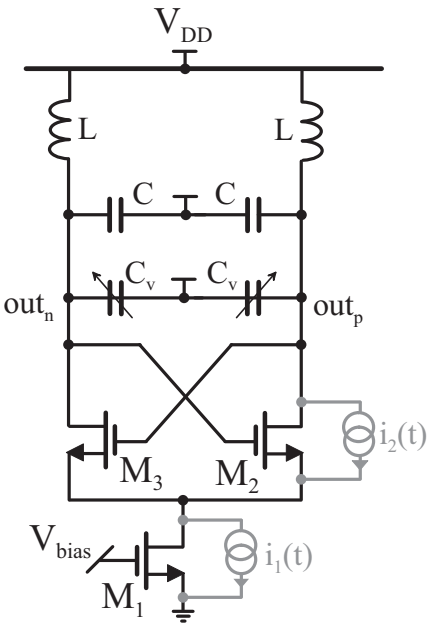


Figure 4.8: *Simulated current-biased LC oscillator.*

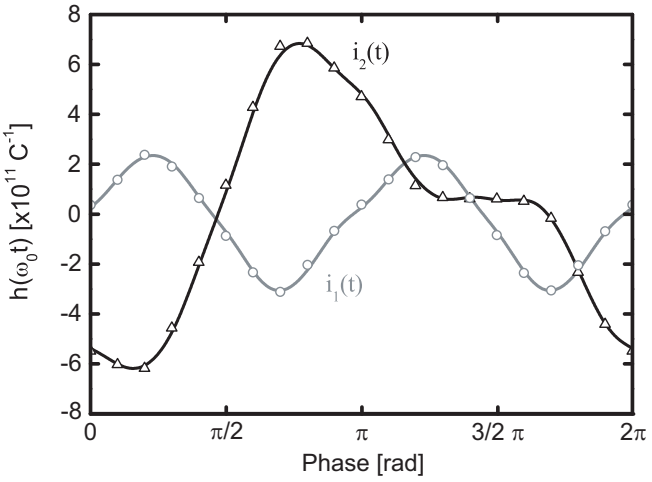


Figure 4.9: *Impulse sensitivity functions for the input signal $i_1(t)$ and $i_2(t)$ in the LC oscillator: from transient analysis (circles and triangles), from PXF analysis (solid line).*

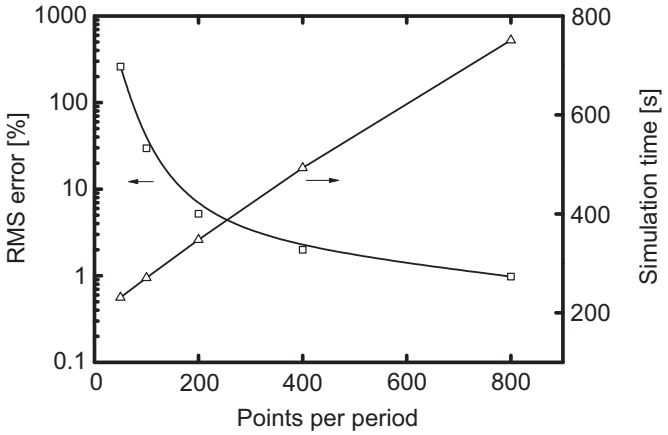


Figure 4.10: *Accuracy and simulation time for the conventional method applied to $i_2(t)$ current generator in Fig. 4.8 as a function of the number of simulated samples per period.*

a comparison with the curves obtained with the conventional time-domain method. In this case, single charge pulses are injected in 21 equally-spaced time instants along the oscillation period. The corresponding $h(t)$ functions are reported in Fig. 4.9 (circles and triangles).

Transient simulation have been performed setting the ratio $\Delta q/q_{max}$ equal to 10^{-2}, as emerged from Section 4.4.1. The amplitude damping follows a simple exponential decay whose time constant is proportional to RC, R being the equivalent parallel loss resistance of each half tank. Since $RC = Q/\omega_0$, the number of oscillation periods to simulate after the injection is in the order of $10RC \approx 2Q$. In this case, a total of 20 periods have been simulated. With regard to the tolerance, the SpectreRF default setting *errpreset*=‘conservative’ was used and the number of samples per period was varied in order to achieve a good matching with the results given by the PXF-based method.

Figure 4.10 shows the simulation time and the root mean square error between waveforms resulting from PXF- and transient-based methods, the latter being performed with a different number of samples per period. The error affecting results of time-domain simulations is referred to as “warping” [77]. A RMS error equal to 1% between the two ISFs is achieved with a total of 800 samples per period, leading to a simulation time of about $750\,\mathrm{s}$, i.e. 75 times higher with respect to the PXF-based method. The proposed technique is even more efficient if the oscillator quality factor is

increased. Considering for the oscillator in Fig. 4.8 a Q of 50, a similar accuracy is obtained with the same number of samples per period but simulating a larger number of periods (200), leading to a simulation time of about 10000 s.

```
Tsim=80n
analysis('tran ?stop sprintf(nil "%g" Tsim) ?finalTimeOp nil)

Tstart=75n
Tstop=76n

Nsample=500
Tsample=(Tstop-Tstart)/Nsample

times=sprintf( nil "%g" Tstart)
for( idxtimes 1 Nsample
optime=Tstart+idxtimes*Tsample
times=strcat( times sprintf( nil " %g" optime))
)

analysis('tran ?stop sprintf(nil "%g" Tsim) ?infotimes list(times) )

run()

ids=getData("M1:ids" ?result "tran_info")
m=sqrt(ids)
```

Listing 2: *Lines of Cadence OCEAN code for the simulation of the modulating function.*

4.5 Simulation of the noise modulating function

The method proposed in Section 4.3 can be extended to perform the overall computation of phase noise induced from a cyclostationary noise source. According to the theory discussed in Section 2.4, the knowledge of the noise modulating function $m(t)$ is required. The computation of this function generally requires to access to some device electrical parameters along a single oscillation period. This can be performed in SpectreRF only by means of a transient analysis, by setting the simulation parameter *infotimes*. This parameter lists the time instants when the operating point of the device must be sampled. The initial phase of the output voltage of the oscillator θ must be also calculated, to ensure the synchronization with the ISF previously derived. Before setting *infotimes*, it is convenient to run a prior transient simulation to accurately annotate the oscillation period and the time necessary for the start-up dynamics of the oscillator to be over.

A sample OCEAN script to simulate the noise modulating function is

shown in Listing 2. The T_{start} and T_{stop} time instants define the oscillation period during which $m(t) = \sqrt{I_{DS}}$ is sampled. The *for* cycle generates the string *times*, which sets the value of *infotimes*, by concatenating 500 equally-spaced time instants. The value of 500 has been derived in an empirical way by means of a comparison between the results provided by the proposed method and by SpectreRF PNOISE analysis.

```
PI=3.141592653589793
Tsim=80n

analysis('tran ?stop sprintf(nil "%g" Tsim) ?finalTimeOp nil)

run()

selectResults( 'tran )

;Select two zero-crossing time instants
Tstart=cross( v("/outp")-v("/outn") 0 -1 'rising nil nil)
Tstop=cross( v("/outp")-v("/outn") 0 -2 'rising nil nil)

f0=1.0/(Tstop-Tstart)
w0=2.0*PI*f0

out=v("/outp")-v("/outn")
time=xval(out)

;Compute in-phase and quadrature component of output voltage
outI=2*average(out*cos(w0*time))
outQ=-2*average(out*sin(w0*time))

;Compute initial phase of first harmonic of output voltage
phi0=atan(outQ/outI)

;Shift Tstart and Tstop
DT=-phi0/w0
Tstart=Tstart+DT
Tstop=Tstop+DT
```

Listing 3: *Additional lines of Cadence OCEAN code computing T_{start} and T_{stop} to synchronize the modulating function with the ISF provided by Listing 1.*

The time instants T_{start} and T_{stop} can be also automatically computed by the simulator. This results into an improved accuracy and can be useful in order to synchronize the NMF with the ISF, the latter obtained by means of Listing 1 and referred to an output voltage whose first harmonic is a cosine function. The additional lines of OCEAN code to perform this operation are provided in Listing 3. This script basically runs a prior transient simulation, selects a reference oscillation period, computes the initial phase of the first

harmonic of the output voltage $out_p - out_n$ and accordingly shifts T_{start} and T_{stop}.

The validity of the proposed phase noise computation method has been verified also for phase noise induced by cyclostationary thermal noise of the transistor M_2 of the LC oscillator in Fig. 4.8. The noise analysis presented in Section 2.4 is revised in order to account for the wide-band nature of such a noise source. A simple expression of its power spectral density is given by:

$$S_w(f) = 4kT\gamma \left[g_m(t) + g_{ds}(t)\right], \tag{4.15}$$

where g_{ds} is drain-source output conductance. Unlike the case involving flicker noise only, the stationary process $i_s(t)$ associated to the PSD in (4.15) consists of noise distributed over the entire frequency spectrum. The single tone of the stationary process can be conveniently written extending (2.27) as:

$$i_s(t) = i_{s,k} \cos\left[\left(k\omega_0 + \omega_m\right) t + \phi_n\right], \tag{4.16}$$

where ϕ_n is a random phase uniformly distributed over the $0 - 2\pi$ interval while the magnitude $i_{s,k}$ is given by:

$$i_{s,k} = \sqrt{2S_w\left(k\omega_0 + \omega_m\right) \cdot 1\,\text{Hz}} = \sqrt{8kT\gamma \cdot 1\,\text{Hz}}.$$

In this case, it is convenient to define an "effective" ISF $h_{eff}(t)$ [37] such that the contribution to the output phase arising from the single-frequency tone in (4.16) can be written as:

$$\Delta\phi_k(t) = \int_{-\infty}^{t} \underbrace{h\left(\omega_0\tau\right) m\left(\omega_0\tau\right)}_{h_{eff}(\omega_0\tau)} i_{s,k}\left(\tau\right) d\tau. \tag{4.17}$$

The Fourier expansion series of $h_{eff}(t)$ is given by:

$$h_{eff}(t) = \frac{h_{eff,0}}{2} + \sum_{k=1}^{+\infty} h_{eff,k} \cdot \cos\left(k\omega_0 t + \varphi_{eff,k}\right). \tag{4.18}$$

According to (1.4) and (1.5), the corresponding single-sideband-to-carrier ratio is given by $\left(\frac{\Delta\phi_k}{2}\right)^2 \cdot \frac{1}{1\,\text{Hz}}$ and the total phase noise results from summing up noise contributions generated by uncorrelated tones at offset $\pm\omega_m$ around each harmonic of the output spectrum. By using (4.17) and (4.18), the SSCR induced from thermal noise of transistor M_2 is therefore given

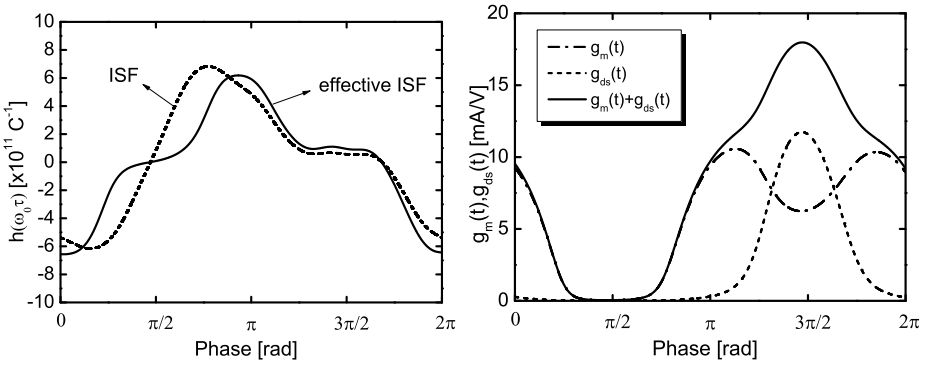


Figure 4.11: *Comparison between ISF for the input signal $i_2(t)$ in the LC oscillator in Fig. 4.8 and efffective ISF associated to thermal noise of MOSFET M_2 (a). $g_m(t)$ and $g_{ds}(t)$ functions of M_2 (b).*

by:

$$SSCR\left(\omega_m\right) \cong \frac{S_w(\omega_m)}{2}\left[\frac{h_{eff,0}}{2\omega_m}\right]^2 + \\ + \sum_{k=1}^{+\infty} \frac{S_w(k\omega_0+\omega_m)+S_w(k\omega_0-\omega_m)}{2}\left[\frac{h_{eff,k}}{2\omega_m}\right]^2. \tag{4.19}$$

By plugging (4.15) into (4.19), the latter reduces to:

$$SSCR\left(\omega_m\right) \cong 8kT\gamma\left[\frac{h_{eff,RMS}}{2\omega_m}\right]^2, \tag{4.20}$$

where $h_{eff,RMS}$ is the root mean square of the effective ISF.

The resulting effective ISF associated to the thermal noise of M_2 is shown in Fig. 4.11(a) as solid line, while the original ISF is plotted as a dashed line. The simulated functions $g_m(t)$ and $g_{ds}(t)$ are instead plotted in Fig. 4.11(b) together with their sum, the latter being related to the modulating function by (4.15).

Finally, Table 4.2 reports the $1/f^2$ phase noise contributions of M_1 and M_2 of the oscillator in Fig. 4.8. The phase noise is quoted as SSCR at 10-MHz frequency offset from carrier and has been calculated by means of the proposed simulation technique. A comparison with the results of the SpectreRF periodic noise analyses is also provided, confirming the validity of the proposed computation method.

Noise Source	Simulated $\mathcal{L}(10\,\text{MHz})$ (Proposed)	Simulated $\mathcal{L}(10\,\text{MHz})$ (PNOISE)
M_2 (Thermal)	-147.56	-147.04
M_1 (Thermal)	-153.21	-152.67

Table 4.2: *Simulated phase noise in LC oscillator.*

4.6 Conclusions

In this chapter, a fast and accurate simulation method based on PXF analysis for the impulse phase response in oscillators has been presented. The proposed technique overwhelms the traditional simulation method based on transient analysis in terms of both computation time and accuracy. In particular, the method is helpful every time the magnitude and phase of each ISF component is of interest and can be easily extended in order to compute the noise modulating function and the phase noise induced from cyclostationary noise sources.

CHAPTER 5

A wide-band voltage-biased LC oscillator with reduced flicker noise up-conversion

5.1 Introduction

In Chapter 2 it has been shown that the up-conversion of flicker noise in voltage-biased oscillators is due to two mechanisms, namely the direct injection into the tank of PM tones since the current troughs active devices lags with respect to the voltage and an AM-to-PM conversion effect due to the dependence of the oscillation frequency on the harmonic content of the output voltage. It has been also pointed out that both effects are reduced in case of low excess gain, which translates into low distortion of the voltage output, and high tank quality factor (for a fixed excess gain), providing a strong attenuation of higher-order harmonics. This result has therefore inspired the design of a novel voltage-biased topology where the excess gain is kept almost constant and close to 2 as the frequency spans the whole tuning range, thus breaking the conflicting link between tuning range and $1/f^3$ phase-noise performance. The circuit has been fabricated in a 65-nm CMOS technology, demonstrating a reduction of 10 dB of the $1/f^3$ phase

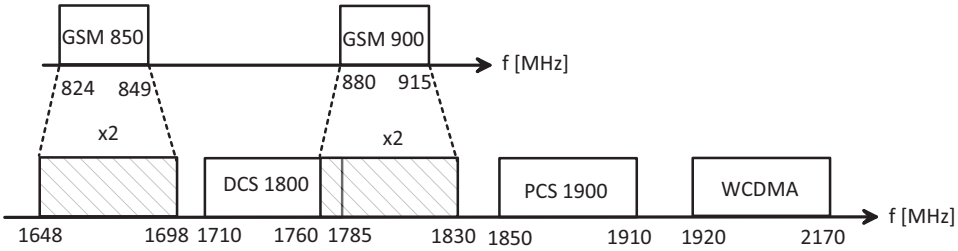


Figure 5.1: *Frequency bands of cellular standards.*

noise over a 47% tuning range, without impairing the $1/f^2$ phase noise performance.

5.2 The proposed topology

In Chapter 2 it has been shown that the two dominant $1/f^3$ phase-noise contributions rise by increasing the excess gain, thus suggesting that oscillator design should be accomplished by limiting the excess gain values. However, in practical applications this requirement is conflicting with the increasing tuning range width. Since frequency tuning is implemented by changing the value of a tunable capacitor, the equivalent parallel loss resistance of the tank R does not remain constant. If tank losses are determined by the inductor series resistance, r_s, it is:

$$R \cong \frac{(\omega_0 L)^2}{r_s}. \tag{5.1}$$

In this case, an oscillation frequency ranging from 1.6 to 2.6 GHz is considered, in order to cover most cellular bands, shown in Fig. 5.1, and to comply also with Bluetooth and 2.5-GHz WiMAX.

In the traditional voltage-biased topology, the small-signal transconductance g_m is therefore chosen to guarantee a reliable oscillation start-up, i.e. $G_X \geq 2$, at the minimum frequency, where the equivalent parallel loss resistance is the lowest. As a consequence, by increasing the oscillation frequency the excess gain increases, thus degrading the $1/f^3$ phase-noise performance. To avoid this trend, a mechanism is therefore needed to adjust the value of g_m to the corresponding R-value given by (5.1), thus keeping G_X approximately equal to 2 over the whole tuning range. To this aim, Fig. 5.2 shows a novel voltage-biased topology where the transconductor

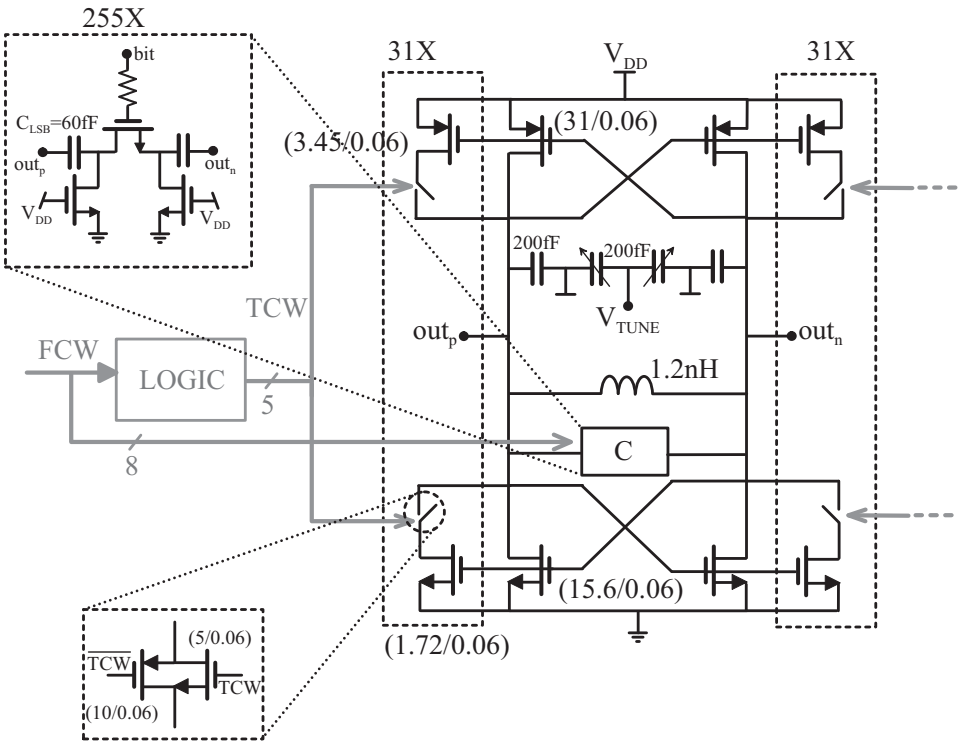


Figure 5.2: *Schematic of the fabricated oscillator implementing the proposed topology.*

is split into a main part that provides the minimum g_m-value required at the maximum frequency and a set of 31 cells, digitally-controlled by a transconductance control word (TCW). This signal can be set externally or by a digital circuit to track the tank capacitance.

The tank capacitance consists on 255 MIM capacitor-based cells connected as shown in Fig. 5.2 and controlled by a frequency control word (FCW). This 8-bit digital word is used to switch-on the capacitive cells needed to synthesize the required oscillation frequency, thus FCW=0 and FCW=255 correspond to the maximum and the minimum oscillation frequency, respectively. A fine tuning of the oscillation frequency is obtained by using a pair of accumulation-PMOS varactors with a sensitivity k_{VCO} lower than 8 MHz/V. Such a small tuning gain has been chosen not to further worsen the AM-to-PM conversion mechanism and to prevent low-frequency noise from 1.2-V supply to be converted into phase noise [13].

The FCW range $(0{:}255)$ has been divided into 16 equally-spaced intervals. While in the first interval $(0{:}15)$ only the transconductor core is active,

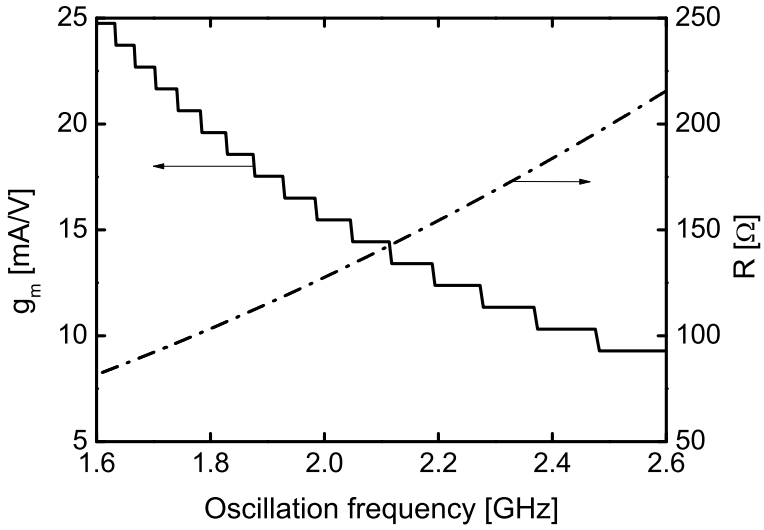


Figure 5.3: *Equivalent parallel loss resistance R and optimum value of small-signal transconductance g_m as functions of the oscillation frequency.*

in each of the following intervals an additional g_m-cell is turned on to compensate the decrease of the parallel resistance. The cells have been sized in order to keep the excess gain approximately constant and equal to 2 as the frequency spans along the tuning range. A larger number of cells have been integrated either to verify the theory on a broad interval of the excess gain values and to eventually compensate a lower quality factor of the inductor at the maximum frequency.

Figure 5.3 shows the overall transconductance g_m together with the estimated values of the equivalent parallel loss resistance as functions of the oscillation frequency. The product $g_m R$ is always in the range 1.9-2.1 assuring a reliable and fast oscillation start-up and, in the meantime, a low flicker noise up-conversion. The switches connecting the transconductance cells to the rest of the circuit are placed in series to the drain of the transistors. To ensure a low series resistance along the whole oscillation period, they have been implemented by using pass-transistors. Their noise contribution is expected to be negligible since their MOSFETs work either in deep triode or in off region.

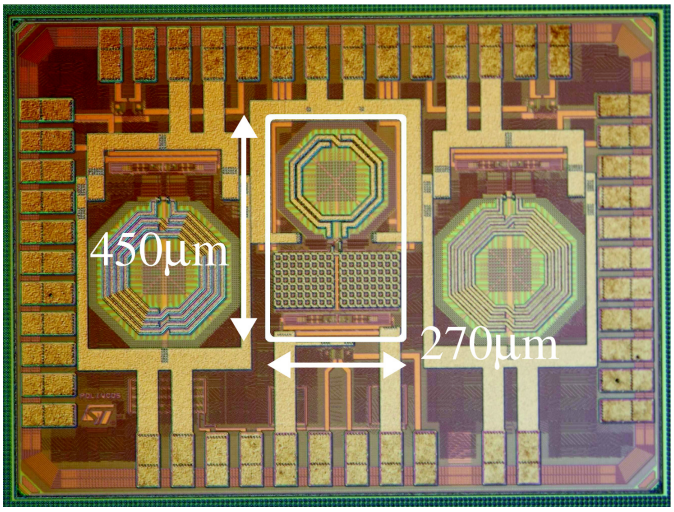


Figure 5.4: *Die photograph.*

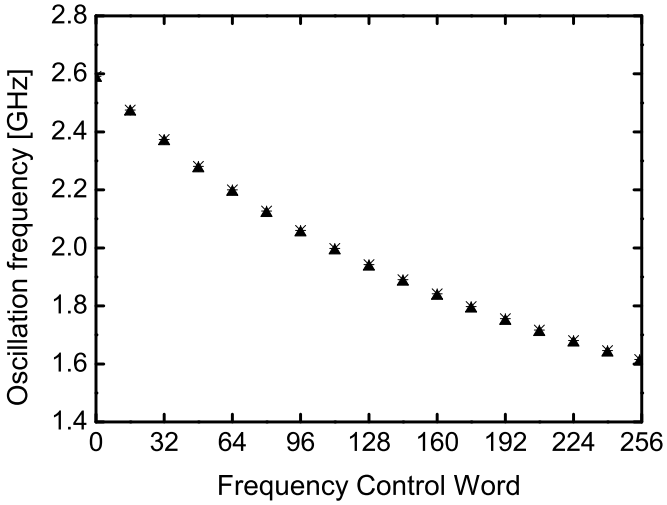


Figure 5.5: *Measured oscillation frequency of two different oscillator samples.*

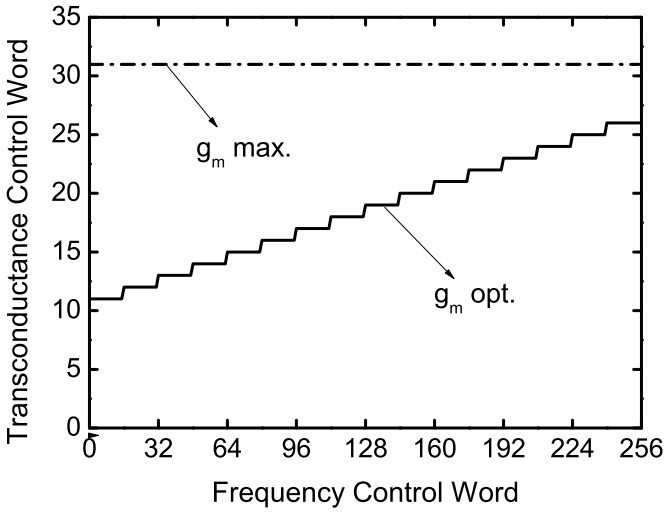


Figure 5.6: *Transconductance control word vs. frequency control word in the two measurement conditions, i.e. with $g_m\ max.$ and $g_m\ opt.$*

5.3 Measurement results

The proposed topology has been integrated in a 1.2-V 65-nm CMOS technology. The microphotograph of the oscillator die is shown in Fig. 5.4. The VCO covers the 1.6-2.6 GHz band and the measured oscillation frequency as a function of the FCW is reported in Fig. 5.5. Phase-noise measurements have been performed by using an Anritsu MS2690A signal analyzer running the phase-noise measurement option while the circuit has been powered by a battery. The $1/f^3$ phase noise has been quoted as SSCR at 1-kHz offset from the carrier. The measurements have been carried out in two different operative conditions:

1. by keeping on all the transconductance cells, thus guaranteeing the oscillation start-up over the whole tuning range ($g_m\ max.$);

2. by changing the number of active transconductance cells according to the FCW ($g_m\ opt.$).

These experimental conditions corresponds to set the TCW as in Fig. 5.6. Note that in the latter case, for FCW=0 the number of the transconductance cells on is not 0, which would correspond to leave active only the core transconductor. In fact, the inductor quality factor has been estimated to be approximately 6 at 2.6 GHz, instead of about 10.5 as predicted from post-

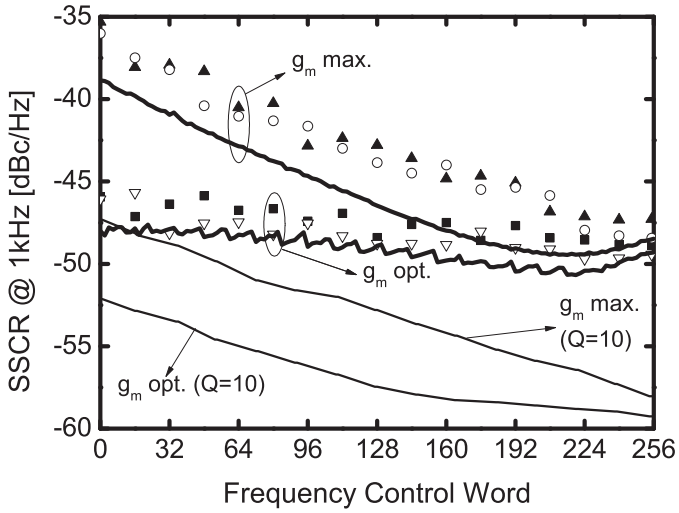


Figure 5.7: *SSCR at* 1*-kHz frequency offset of two different oscillator samples. Symbols refer to measured phase noise, while solid lines to simulated values. Also the simulated results obtained with Q=*10 *are shown.*

layout simulations, thus the condition $G_X \cong 2$ is reached only turning on 11 g_m-cells.

The measured $1/f^3$ phase noise on two oscillators samples is shown in Fig. 5.7. As predicted, by following the traditional design, the $1/f^3$ phase noise rapidly rises as the oscillation frequency is increased due to the growing excess gain. Instead, the segmented topology reduces the flicker noise up-conversion over the whole tuning range and by almost 10 dB at the highest oscillation frequency (FCW=0). A residual increase of the $1/f^3$ noise may be still noticed as the oscillation frequency increases due to the decreasing value of the tank capacitance. Figure 5.7 also shows the comparison with SpectreRF simulation results. The good agreement between measured and simulated results, achieved by assuming a tank quality factor equal to 6, proves the validity of the NMF-based phase noise generation model adopted. For comparison, the projected performances achievable by a tank with the nominal Q of 10 are also shown.

Figure 5.8 shows the measured SSCR at 1-kHz offset from carrier as function of the TCW for two values of FCW. Once the FCW is set, as the TCW is increased the transconductance of the active element and thus the oscillator excess gain increase, leading to a rapid growing of the $1/f^3$ phase noise.

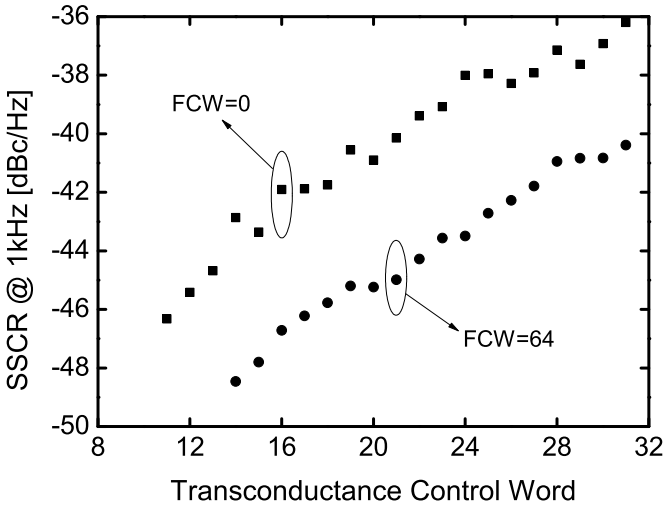


Figure 5.8: $1/f^3$ *phase noise at* 1*-kHz offset from carrier as a function of the transconductance control word for two values of FCW.*

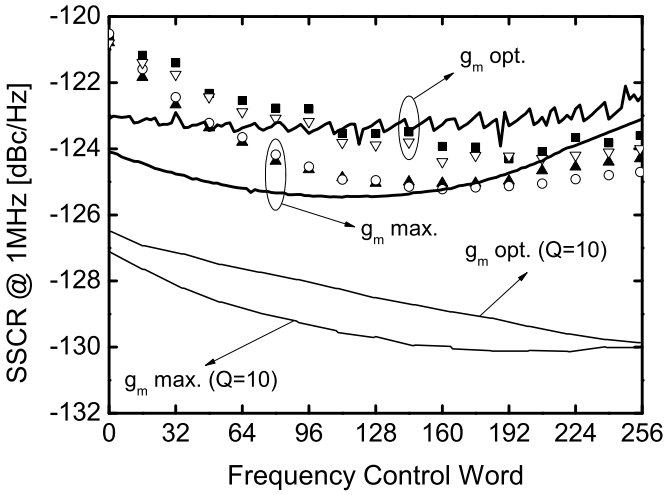


Figure 5.9: *SSCR at* 1*-MHz frequency offset of two different oscillator samples. Symbols refer to measured phase noise, while solid lines to simulated values. Also the simulated results obtained with* Q=10 *are shown.*

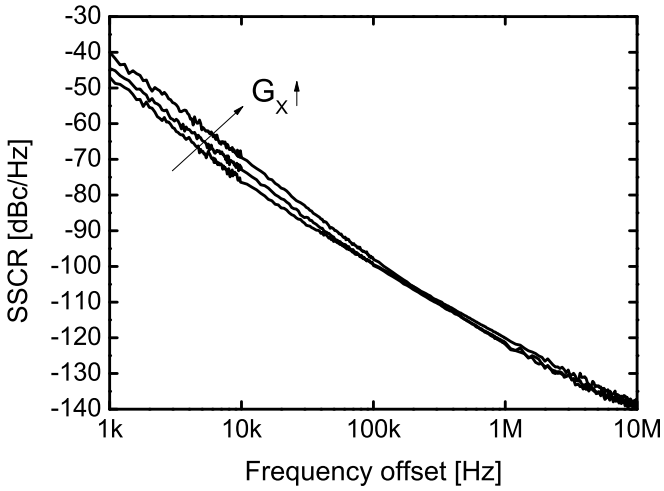


Figure 5.10: *Measured SSCR vs offset frequency at* $2.6\,GHz$ *for different values of the excess gain.*

As far as the $1/f^2$ phase noise is concerned, Fig. 5.9 plots the measurement results performed in the same two conditions described before. An increase of only 1 dB is observed, meaning that the proposed topology is not detrimental neither in terms of smaller oscillation amplitude nor in terms of additional noise due to switches. The full measured phase noise spectrum at $f_0 = 2.6\,\text{GHz}$ for different values of the excess gain is plotted in Fig. 5.10.

With respect to the traditional design, the proposed solution features also a lower power consumption and a reduced sensitivity to voltage supply variations. Figure 5.11 shows a comparison of the current drawn from the 1.2-V supply when the transconductor size is always set to be maximum and when it is tailored to adaptively keep the excess gain constant. In the latter case, increasing the oscillation frequency a growing number of g_m-cells are switched off with a beneficial impact on the current consumption.

Regarding the supply sensitivity, it is:

$$k_{supply} = \frac{\partial \omega_0}{\partial V_{DD}} \cong \frac{\partial \omega_0}{\partial A_1} \cdot \frac{\partial A_1}{\partial V_{DD}}.$$

Since $A_1 \cong V_{DD}$, the supply noise is converted due to modulation of the common-mode voltage across the analog varactors [13] and the incremental Groszkowski effect. However, the sensitivity associated to the first term is given by $\frac{k_{VCO}}{2}$, which is negligible with respect to $k_{AM-FM}^{(\text{Gros.})}$ that is about

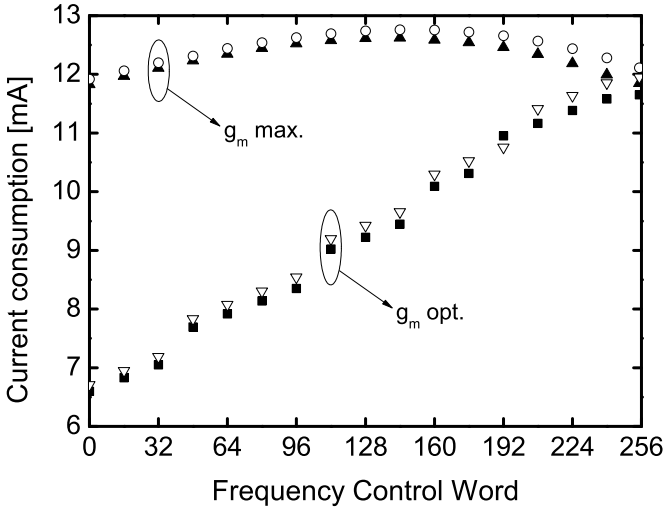


Figure 5.11: *Measured DC current drawn from the* 1.2*-V supply of two different oscillator samples.*

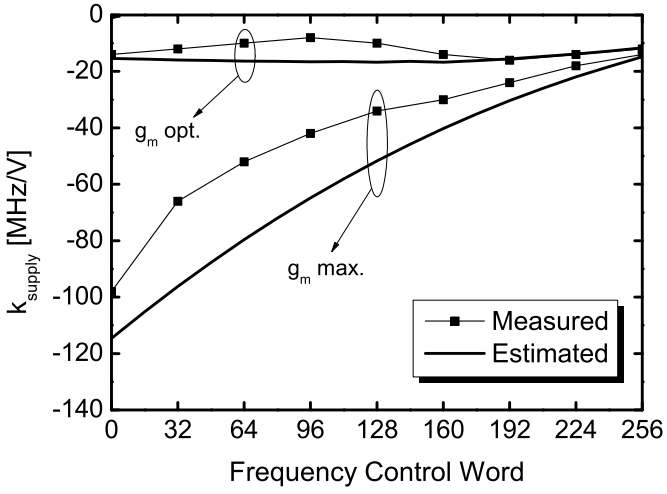


Figure 5.12: *Measured and estimated sensitivity of oscillation frequency on supply voltage.*

15 MHz/V for $G_X \cong 2$ and $Q = 6$ and depends quadratically on the excess gain. Fig. 5.12 shows the experimental values of measured k_{supply} as a function of FCW. Note that the experimental values are in good agreement with the theoretical frequency sensitivity resulting from (2.54). At the maximum frequency of 2.6 GHz, the segmented transconductor guarantees a reduction of the k_{supply} sensitivity by a factor of 5.

Finally, Table 5.1 reports a comparison of recently-published wide-band VCOs. In this work, the oscillator performance is evaluated by using the figure of merit $FoM^{(1/f^3)}$ defined in Section 3.6, normalized to take into account also the broad frequency interval of operation. The resulting $FoM_T^{(1/f^3)}$ is normalized with respect to the tuning range as in [78] and is given by:

$$FoM_T^{(1/f^3)} = -\mathcal{L}(\omega_m) + 20\log\left(\frac{\omega_0}{\omega_m^{1.5}} \cdot \frac{TR}{10}\right) - 10\log\left(\frac{I_{DC}}{1\,\text{mA}}\right),$$

where TR is the tuning range expressed as percentage. When compared to the state-of-the-art VCOs, the proposed oscillator shows an average $1/f^3$ phase noise of -48 dBc/Hz at 1-kHz frequency offset, which translates into the best average figure of merit over the frequency span. Only the oscillator in [21] outperforms the presented VCO, albeit it was designed in a less-scaled technology. Moreover, this result was obtained with a higher power consumption and a narrower tuning range, thus the oscillator in [21] features a lower $FoM_T^{(1/f^3)}$.

In summary, the comparison shows that the presented design achieves both wide tuning range and low flicker noise up-conversion over the whole frequency range.

Parameter	[10]	[79]	[21]	[80]	this work
Technology	$0.13\,\mu$m	$0.13\,\mu$m	$0.25\,\mu$m	65 nm	65 nm
Frequency [GHz]	5.3	2.15	2.7	4.01	2.1
Tuning Range [%]	22.6	92.6	28.6	75	47.6
Power Supply [V]	1.2	1.5	2.0	0.6	1.2
Power consumption [mW]	24	30	20	9.8/14.2	8/14.5
$\mathcal{L}$(1kHz) [dBc/Hz]	-38/-28	-52/-35	-54/-44	-44/-32	-50/-46
$FoM_T^{(1/f^3)}$ [dB]	136.5/126.5	149/141	150.7/142.6	145.7/142.1	146.2/149.2
$\mathcal{L}$(1MHz) [dBc/Hz]	-123/-120	-124/-120	-135/-133	-130/-125.7	-124/-120.5

Table 5.1: *Performance comparison of recently-published wide-band VCOs*

5.4 Conclusions

In Chapter 2, it has been shown that the major contribution to up-conversion in voltage-biased oscillator topologies arises by the non-perfect quadrature between the first harmonic of the ISF and the current flowing through the transistors. This effect has been recognized as due to the Groszkowski effect and to the variation of the voltage waveform harmonics induced by amplitude modulation. The strength of both mechanisms increases with larger values of excess gain. This result has inspired the design of a novel voltage-biased topology where the excess gain is kept almost constant and close to 2 as the frequency spans the whole tuning range, thus breaking the conflicting link between tuning range and $1/f^3$ phase-noise performance. The circuit has been fabricated in a 65-nm CMOS technology, demonstrating a reduction of 10 dB of the $1/f^3$ phase noise over a 47% tuning range, without impairing the $1/f^2$ phase noise performance. Moreover, measurement results are in good agreement with simulations, thus proving the validity of the NMF-based model adopted.

CHAPTER 6

Analysis and reduction of flicker noise up-conversion in current-biased LC oscillators

6.1 Introduction

In the previous chapters, the differential voltage-biased LC oscillator has been extensively analyzed since it is an interesting solution as the supply voltage keeps decreasing with technology scaling. In this chapter, the flicker noise up-conversion theory developed in Chapter 2 is applied to current-biased oscillators, which have been widely used so far owing to the possibility to precisely set the power consumption of the circuit.

In the last decades, many papers have been devoted to investigate the generation mechanisms of close-in phase noise in this oscillator topology. Four major up-conversion mechanisms have been identified so far, namely:

1. conversion of AM-to-PM due to non-linear varactors [11–13, 15];
2. modulation of the current flowing through the tail capacitance [16, 19, 30, 36];

3. modulation of differential pair device capacitances [20, 21, 30]

4. modulation of the harmonic content of the output voltage waveform [17, 19, 22–28].

The first up-conversion mechanism has been well clarified and can be drastically reduced by employing smaller analog varactors and a coarse digital tune. Regarding the other effects, in most papers the phase noise analysis has been carried out in a more qualitative rather than quantitative perspective and a complete explanation of these phenomena has not been provided yet.

On the one hand, it has not been pointed out whether the main $1/f^3$ phase noise contribution is the current noise of the biasing circuit or of the switching pair. In most papers, only the stationary noise from tail current source was taken into account, although this contribution can be minimized by adopting non-minimum channel length transistors. On the other hand, it is still not clear which one of the aforementioned mechanisms is dominant in current-biased oscillators. In fact, despite being closely related to each other, those effects have been studied independently and no numerical comparison between their impact has been provided. In particular, the modulation of differential pair device capacitances started to be analyzed only recently [20, 21]. However, in those papers only the parasitics of the MOSFET switching pair were considered in performing circuit simulations, neglecting the presence of a tail capacitance.

In this chapter, the cyclostationary nature of noise of the switching pair is taken into account for the first time by adopting the NMF-approach. Up-conversion mechanisms are quantitatively evaluated, eventually showing that the induced $1/f^3$ phase noise is mostly generated by modulation of the non-linear capacitance placed at the tail node. Based on this analysis, some important design insights will be drawn, whose validity has been verified by means of measurements on a test chip, described in Chapter 7.

6.2 $1/f^3$ phase noise analysis in current-biased LC oscillators

Figure 6.1 shows a differential LC-tuned oscillator implementing a current-biased topology that has been taken as case study in this chapter.

The circuit has been simulated in a 0.13-μm CMOS technology with 1.2-V nominal supply and RF technology options. The circuit is biased with $V_{DD} = 1\,\text{V}$, while the current I_B spans between 1 and $4\,\text{mA}$. The

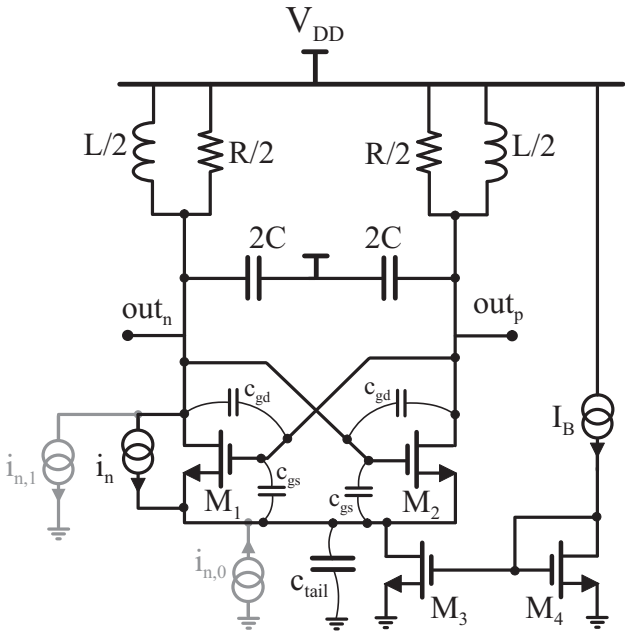


Figure 6.1: *Schematic of a differential cross-coupled oscillator implementing a current-biased VCO.*

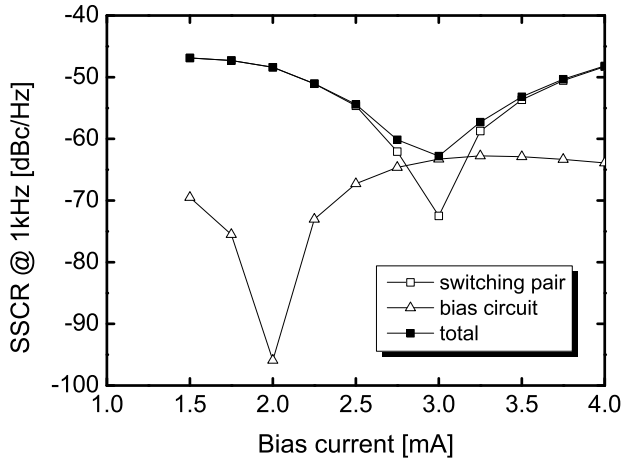


Figure 6.2: *Simulated contributions of SSCR at 1-kHz frequency offset from switching pair and bias circuit (M_3-M_4) for $W = 15\,\mu m$. The overall $1/f^3$ phase noise resulting from their sum is also plotted.*

width W of the MOSFETs M_1 and M_2 of the switching pair has been also varied, in order to investigate its impact on $1/f$ noise up-conversion. Their length, instead, has been set equal to the minimum value of 130 nm in order to guarantee a broad tuning range. Transistors M_3 and M_4 have been instead sized with $(W_{tail}/L_{tail}) = (150/3)$, the length being chosen for the $1/f^3$ phase noise contribution of biasing circuit to be negligible, while at the same time avoiding to introduce a large tail capacitance c_{tail}. The oscillator frequency spans from 1.9 to 2.6 GHz by using a tank with $L = 3.75$ nH, $C = 1 \div 1.87$ pF and a quality factor $Q = 10$. The $1/f^3$ phase noise contributions of switching pair and biasing circuit are plotted in Fig. 6.2 together with their sum as function of bias current for $W = 15\,\mu$m.

In this circuit, the current noise source i_n in Fig. 6.1 is considered, since only the flicker noise of M_1 and M_2 is relevant. With respect to the voltage-biased topology so far investigated, the ISF associated to i_n, h_{DS}, is far from being a pure sinusoid, since the source node of M_1 is no more connected to ground. As a consequence, also the DC component and the second harmonic of h_{DS} in (2.66) have to be taken into account. A sample waveform of h_{DS} can be found in Fig. 4.9. Basically, h_{DS} is almost zero when M_1 is ohmic, while it resembles the traditional sinusoid during the other working regions.

To grasp an intuitive insight into the up-conversion mechanism, it is useful to split i_n into two ground-referred current sources, $i_{n,0}$ and $i_{n,1}$ [81]. These two sources feature the same frequency content of i_n, consisting of $1/f$ noise folded around each harmonic of the output spectrum. However, owing to their location in the circuit, only a limited number of their noise side-bands are of interest. In particular, the noise from $i_{n,1}$ is directly injected into the LC tank, similarly to the case of the voltage-biased oscillator. Thus, according to the theory developed in Chapter 2, only noise components folded around the fundamental frequency are of interest. On the other hand, the current noise $i_{n,0}(t)$ is injected into the tank after being modulated by the switching action of M_1 and M_2. As a consequence, only the noise folded around even harmonics is converted around the oscillation frequency f_0, eventually translating into phase noise [36].

In the general case, both direct injection and AM-to-PM conversion discussed in Sections 2.5.2 and 2.5.3 are responsible for the $1/f^3$ phase noise generation. However, it must be pointed out that in the current-biased topology the Groszkowski effect is much less relevant than in the voltage-biased counterpart, resulting into a much smaller direct contribution and AM-to-

PM conversion due to modulation of harmonic content. In order to prove this statement, it is useful to compare the two topologies in terms of total harmonic distortion [27, 28].

By taking the output voltage $V(t) = out_p(t) - out_n(t)$ as a cosine function, the current $I_1(t)$ flowing through the transistor M_1 can be approximated as a square wave between 0 and I_B, thus resulting:

$$I_1(t) = I_B \cdot s(t), \tag{6.1}$$

where

$$s(t) = \frac{s_0}{2} + \sum_{k=1}^{+\infty} s_k \cos(k\omega_0 t) = \frac{1}{2} + \sum_{k=1}^{+\infty} \frac{2}{k\pi} \sin\left(\frac{k\pi}{2}\right) \cos(k\omega_0 t). \tag{6.2}$$

The current flowing through M_2, $I_2(t)$, can be instead calculated by considering a square wave shifted by 180 degrees. Denoting with R the equivalent differential loss resistance of both LC tanks, the magnitude of each Fourier component of the differential output voltage $V(t)$ is given by:

$$A_k = \begin{cases} I_B s_1 R & \text{if } k = 1 \\ I_B s_k \left| \frac{1}{jk\omega_0 C} \right| & \text{if } k = 3, 5, 7, ... \\ 0 & \text{elsewhere.} \end{cases} \tag{6.3}$$

By using (6.3), the resulting total harmonic distortion is equal to:

$$THD = \sqrt{\frac{\sum_{k=2}^{+\infty} A_k^2}{A_1^2}} \cong \frac{1}{8Q}. \tag{6.4}$$

In (6.4), the approximation $\sqrt{\frac{1}{3^4} + \frac{1}{5^4} + \frac{1}{7^4} + ...} = \sqrt{\frac{\pi^4}{96} - 1} \cong \frac{1}{8}$ has been used.

With respect to the voltage-biased oscillator, (6.4) does not feature the term $G_X - 1$ (see Eq. (2.15)), implying that in the current-biased topology the THD is independent on excess gain and intrinsically smaller than in the Van der Pol oscillator. By limiting the analysis to the third harmonic and using the approximation $1 - \omega_0^2 LC \cong -2\frac{\Delta\omega_0}{\omega_0}$, the frequency shift due to the Groszkowski effect can be written according to (2.1) as:

$$\Delta\omega_0 \cong -\frac{1}{2}\omega_0 \left(1 - \frac{A_1^2 + A_3^2}{A_1^2 + 9A_3^2}\right) \cong -\frac{1}{2} \cdot \frac{8A_3^2}{A_1^2} \cdot \omega_0. \tag{6.5}$$

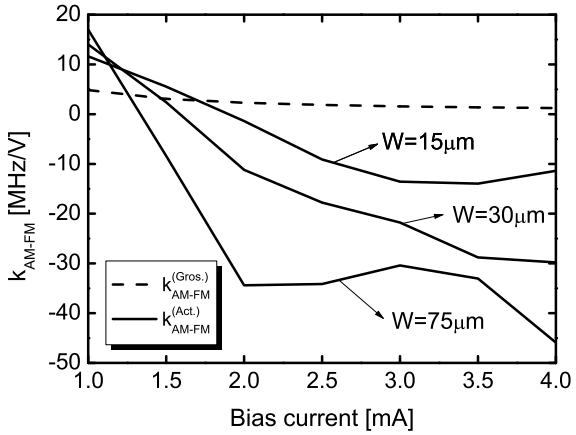


Figure 6.3: *Comparison among frequency sensitivity associated to Groszkowski effect given by (6.7) (dashed line) and simulated $k_{AM-FM}^{(Act.)}$ (solid lines) for different sizes of switching pair transistors as function of bias current.*

In (6.5), the last approximation is valid since the ratio $\frac{A_3}{A_1}$ is equal to $\frac{1}{9Q}$ according to (6.3). The condition $A_1^2 \gg 9A_3^2$ thus holds for $Q > 1$.

The equivalent Groszkowski capacitance defined in Section 2.6.1 corresponding to the frequency shift in (6.5) can be thus expressed as function of THD as:

$$C_{Gros} \cong -2\frac{\Delta\omega_0}{\omega_0}C = 8 \cdot THD^2 \cdot C. \tag{6.6}$$

Due to the quadratic dependence of C_{Gros} on THD, the Groszkowski capacitance is reduced by about a factor of 10 with respect to the voltage-biased topology, since the excess gain G_X typically ranges between 2 and 4. The same holds for the frequency sensitivity $k_{AM-FM}^{(\text{Gros.})}$, which can be expressed as:

$$k_{AM-FM}^{(\text{Gros.})} = \frac{\partial\omega_0}{\partial C_{Gros}} \cdot \frac{\partial C_{Gros}}{\partial THD} \cdot \frac{\partial THD}{\partial A_1} \cong \frac{\omega_0}{A_1} \cdot \frac{1}{8Q^2} \tag{6.7}$$

by using (6.4) and (6.6). With respect to the sensitivity of a voltage-biased oscillator given by (2.54), $k_{AM-FM}^{(\text{Gros.})}$ in (6.7) is reduced by a factor of $2\,(G_X - 1)^2$. This frequency sensitivity has been compared with the term associated to the modulation of parasitics, $k_{AM-FM}^{(\text{Act.})}$, including tail and differential pair device capacitances. The latter sensitivity has been computed by means of SpectreRF simulations performed on the circuit in Fig. 6.1 with the following parameters: $L = 3.75\,\text{nH}$, $C = 1.87\,\text{pF}$ and $R = 610\,\Omega$, corresponding

to an oscillation frequency f_0 equal to $1.9\,\text{GHz}$ and a tank quality factor Q equal to 10. The bias current I_B has been swept between 1 and $4\,\text{mA}$, the oscillation amplitude varying from 0.2 to $1\,\text{V}$. The results are plotted in Fig. 6.3 for three values of W, namely 15, 30 and $75\,\mu\text{m}$.

Unlike the voltage-biased topology, $k_{AM-FM}^{(\text{Gros.})}$ is negligible with respect to the sensitivity $k_{AM-FM}^{(\text{Act.})}$. On the one hand, $k_{AM-FM}^{(\text{Gros.})}$ is reduced by about a factor of 20 in this topology. On the other hand, $k_{AM-FM}^{(\text{Act.})}$ is much larger than in the voltage-biased counterpart due to the presence of a large tail capacitance, as it will be shown in Section 6.3. This effect also results into a major flicker-noise up-conversion mechanism.

Based on this analysis, the phase noise can be computed by first evaluating the impact of noise sources on the oscillation amplitude A_1 and then considering the corresponding modulation of non-linear parasitic capacitances of the transconductor. The noise side-bands to be taken into account are only those around the fundamental frequency of $i_{n,1}$ and that around DC of $i_{n,0}$. To a first approximation, the side-bands around even harmonics of $i_{n,0}$ can be neglected since the transistor current resembles a square wave and features almost no power at their frequencies. The two noise side-bands around the fundamental can be also neglected, since they yield a common-mode disturbance which does not appear at the differential output.

Following the approach adopted in Chapter 2, the cyclostationary noise of i_n can be described starting from a generic current tone i_s of a stationary process and then considering the mixing with the NMF. Being the Groszkowski effect negligible, the two current tones around ω_0 of $i_{n,1}$ can be written as in (2.30) by taking $\varphi_m^{(1)} = 0$. They are directly injected into the tank, eventually resulting into AM side-tones of output voltage after multiplication by $R/2$. These tones can be thus written as:

$$i_{n1} \Rightarrow \begin{cases} \dfrac{Rm_1 i_s}{4} \cos\left[(\omega_0 - \omega_m)\, t\right] \\ \dfrac{Rm_1 i_s}{4} \cos\left[(\omega_0 + \omega_m)\, t\right]. \end{cases} \tag{6.8}$$

On the other hand, the low-frequency tone associated to $i_{n,0}$ is first multiplied by the square wave $s(t)$ in (6.2), which models the switching action of M_1 and M_2. The resulting AM voltage side-tones can be easily derived

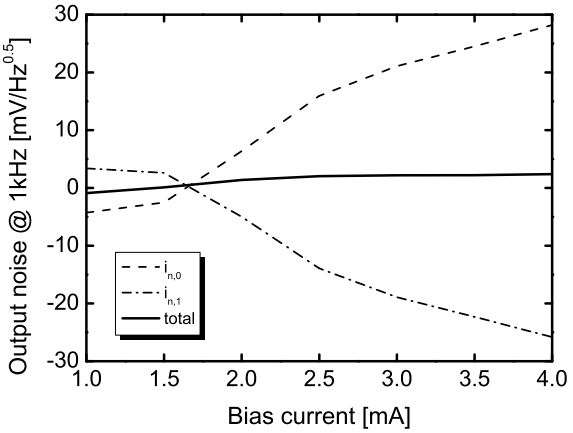


Figure 6.4: *Contributions to output voltage noise at 1-kHz offset from carrier induced from $i_{n,0}$ and $i_{n,1}$ as function of bias current for $W = 75\ \mu m$.*

as:

$$i_{n0} \Rightarrow \begin{cases} -\dfrac{4}{\pi} \cdot \dfrac{Rm_0 i_s}{4} \cos\left[(\omega_0 - \omega_m)\, t\right] \\ -\dfrac{4}{\pi} \cdot \dfrac{Rm_0 i_s}{4} \cos\left[(\omega_0 + \omega_m)\, t\right]. \end{cases} \tag{6.9}$$

As suggested by (6.8) and (6.9), $i_{n,1}$ and $i_{n,0}$ have opposite effects on the oscillation amplitude, the former increasing A_1, the latter diminishing it during the positive swing. This is not surprising since the the two noise sources are correlated. Figure 6.4 shows the contributions to output voltage noise at 1-kHz offset from the 1.9-GHz carrier induced by $i_{n,0}$ and $i_{n,1}$ as function of the bias current I_B. Summing the cosine functions in (6.8) and (6.9) and taking into account that $m_1 = \frac{4}{\pi} m_0$, the overall AM should be nil. However, only a partial cancellation occurs and a residual $1/f^3$ phase noise component is still present, which is about one order of magnitude smaller than the two original contributions. This is generally due to two reasons:

- the current is not exactly a square wave, especially if M_1 and M_2 operate in deep triode region
- the sensitivity $k_{AM-FM}^{(\text{Act.})}$ associated to $i_{n,0}$ features an additional term which relates the modulation of parasitic capacitances to the modulation of bias current for a constant oscillation amplitude.

However, simulations performed on the circuit in Fig. 6.1 show that the first source of imperfect cancellation is dominant and results into a scale factor

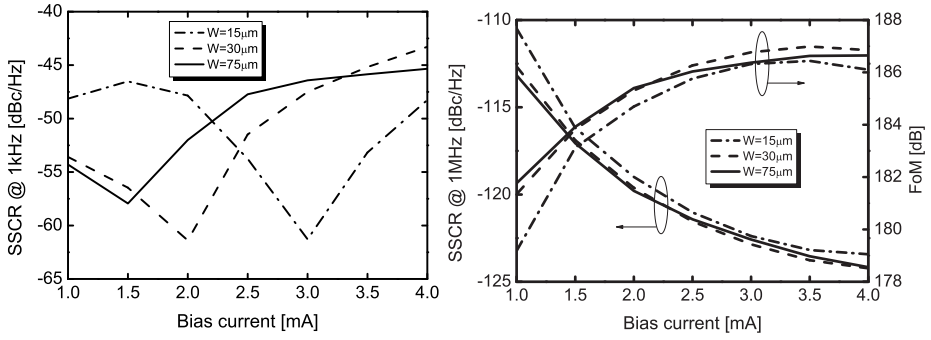


Figure 6.5: *Simulated SSCR at 1-kHz (a) and 1-MHz (b) frequency offset from carrier of the current-biased oscillator in Fig. 6.1 corresponding to different sizes of the MOSFET switching pair.*

between the two phase noise contributions which is almost constant over the bias current range.

Deriving analytical expressions to quantitatively describe these two aspects is impracticable and the general view of flicker noise up-conversion mechanisms in current-biased oscillator would be hardly retained. Instead, since the purpose of this chapter is to derive general design criteria, the phase noise analysis is carried out based from the following statement: the $1/f^3$ phase noise in the topology in Fig. 6.1 is the sum of two correlated AM-to-PM contributions which partially cancel out each other. As a consequence, the overall phase noise can be written as an attenuated replica of the SSCR arising from $i_{n,0}$ or $i_{n,1}$.

As an example, by plugging (2.49) into (2.38), it is possible to derive the phase noise induced from $i_{n,0}$ as:

$$SSCR_0(\omega_m) = \frac{S_{1/f}(\omega_m)}{2\omega_m^2}\left(m_0 k_{AM-FM}^{(\text{Act.})}\frac{2}{\pi}R\right)^2, \tag{6.10}$$

where the equalities $h_1 = \frac{1}{2CA_1}$ and $R_{AM} = \frac{2}{\pi}R$ have been used.

The overall phase noise can be thus written as:

$$SSCR(\omega_m) \cong \varepsilon^2 \cdot SSCR_0(\omega_m), \tag{6.11}$$

where the factor $\varepsilon \approx 0.1$ accounts for the small fraction of phase noise surviving the destructive interference.

As shown in Fig. 6.4, the two contributions of $1/f^3$ output voltage noise are null for a particular value of the bias current I_B. By examining (6.10),

this can be justified only by the sensitivity $k_{AM-FM}^{(\text{Act.})}$ being equal to zero, since m_1 is always positive and the other parameters are constant. In Section 6.3, a detailed explanation for the nulling of $k_{AM-FM}^{(\text{Act.})}$ is carried out.

However, it is useful to determine the general trend of $1/f^3$ phase noise also as a function of the transistors width, being a free parameter. Figure 6.5(a) shows the simulated SSCR at 1-kHz frequency offset from carrier of the oscillator corresponding to three different sizes of the MOSFET switching pair. It turns out that for smaller W the $1/f^3$ phase noise is nulled at larger bias currents.

This is useful in designing the oscillator since W can be chosen in order to achieve, for same the value of I_B, both minimum flicker noise up-conversion and maximum figure of merit for $1/f^2$ phase noise, the latter occurring at the cross-over between current- and voltage-limited regime [30]. In fact, the $1/f^2$ phase noise features a negligible dependence on the width of the switching transistors, as confirmed by simulation results. The $1/f^2$ phase noise computed by SpectreRF is plotted in Fig. 6.5(b) quoted as SSCR at 1-MHz frequency offset from carrier. In this case, the largest value of FoM, also shown in Fig. 6.5(b), is reached for $I_B = 3.5\,\text{mA}$, corresponding to the plateau region of SSCR at 1-MHz offset, and suggests to choose $W = 15\,\mu\text{m}$ to minimize the flicker noise contribution.

6.3 AM-to-PM conversion due to non-linear capacitances

In this section, the sensitivity $k_{AM-FM}^{(\text{Act.})}$ of the oscillator in Fig. 6.1 is investigated by means of circuit simulations. The evaluation of the modulation of parasitics has to face a twofold complexity, consisting in the time-varying nature of both the devices capacitances and their transfer functions toward the LC tank, indicating their effective impact on the oscillation frequency. In the circuit in Fig. 6.1, three main classes of parasitics exist, namely:

- the gate-drain capacitances of M_1 and M_2, c_{gd}
- the gate-source capacitances of M_1 and M_2, c_{gs}
- the tail capacitance, c_{tail}, including the source-substrate junction capacitance of M_1 and M_2 and the gate-drain and drain-substrate capacitances of M_3

In the following, the sensitivity term associated to each class will be computed.

The first term associated to both c_{gd} can be easily derived, since these capacitances are placed differentially across the tank. Their overall effective value setting the oscillation frequency is thus given by $c_{gd,eff} = 2c_{gd,0} - c_{gd,2}$, where $c_{gd,0}$ is the time-average of each capacitance and $c_{gd,2}$ is the second-order Fourier coefficient of the waveform of $c_{gd}(t)$ [11,15]. A circuit simulation is needed only to extract the two harmonic components $c_{gd,0}$ and $c_{gd,2}$.
As a first approximation, this method can extended to the second class of parasitics, c_{gs}. Since the voltage of the source node of the switching pair is almost constant, exhibiting only minor fluctuations, the gate-source capacitances can be ascribed as single-ended tank-referred capacitances, their effective value being thus given by $c_{gs,eff} = c_{gs,0} - \frac{1}{2}c_{gd,2}$.

With regard to the tail capacitance, a more refined method must be adopted. First, it is worth defining the harmonic components of $c_{tail}(t)$ that are of interest. To this purpose, denoting with $v_{tail}(t)$ the voltage at the source node of M_1 and M_2, the current flowing through the tail capacitance can be written as:

$$i_{tail}(t) = \frac{d}{dt}c_{tail}(t) \cdot v_{tail}(t) + c_{tail}(t) \cdot \frac{d}{dt}v_{tail}(t).$$

Since this current is injected into the tank after multiplication with the square wave in (6.2), only even harmonics of i_{tail} are significant. The voltage v_{tail} is almost a sinusoid at frequency $2f_0$ superimposed to a constant value, implying that also for the tail capacitance the the zeroth- and second-order Fourier coefficients, $c_{tail,0}$ and $c_{tail,2}$, are of interest in computing the effective value.

The time-waveforms of c_{gd}, c_{gs} and c_{tail} are obtained by means of transient analyses sampling the MOSFET operating point along an oscillation period by setting the parameter *infotimes*, similarly as described in Chapter 4. Simulation results, however, show that the second-order terms $c_{x,2}$, c_x indicating the generic class of parasitics, are in all cases more than one order of magnitude smaller than the corresponding $c_{x,0}$ and they have thus been discarded. The frequency sensitivity can be computed as the finite difference $\frac{\Delta\omega_0}{\Delta A_1}$, which approximates the derivative $\frac{\partial\omega_0}{\partial A_1}$ if ΔA_1 is sufficiently small. The oscillation amplitude can be varied by slightly changing the bias current in simulations, thus resulting:

$$k_{AM-FM,x} \cong \frac{\Delta\omega_{0,x}}{\Delta I_B} \cdot \frac{\Delta I_B}{\Delta A_1} = \frac{\Delta\omega_{0,x}}{\Delta I_B} \cdot \frac{1}{\frac{2}{\pi}R}, \tag{6.12}$$

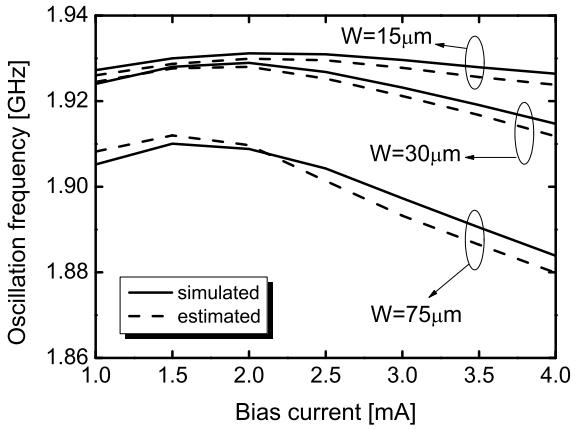


Figure 6.6: *Oscillation frequency as function of bias current for different sizes of switching pair transistors. Solid lines refer to the results provided by PSS analyses carried out at* 1.9 *GHz, while dashed lines to those obtained at* 19 *MHz modeling parasitics by means of additional capacitances whose value had been previously determined by transient simulations.*

where $\Delta\omega_{0,x}$ is the frequency deviation from resonance induced by the presence of parasitics. For c_{gd} and c_{gs}, the term $\frac{\Delta\omega_{0,x}}{\Delta I_B}$ is simply equal to $-\frac{\omega_0}{2C}\cdot\frac{\Delta c_{0,x}}{\Delta I_B}$.

In order to compute the effective capacitance "seen" by the tank due to c_{tail}, a more refined method is adopted. The circuit in Fig. 6.1 has been simulated at a much smaller frequency in order to neutralize the impact of other parasitics. A 100-times smaller oscillation frequency can be accomplished by setting $L = 375$ nH, $C = 187$ pF, keeping the same tank quality factor, bias current and transistors size. A PSS analysis is first performed in order to derive the oscillation frequency, determined only by the Groszkowski effect. An additional capacitance is then placed, whose value is $100c_{tail,0}$, to model the effect of c_{tail}. A second PSS analysis has been then run and the frequency deviation with respect to the previous case, $\Delta\omega_{0,tail}$, is computed. The frequency sensitivity can be instead calculated by using (6.12), while the effective capacitance is given by $c_{tail,eff} = -2C\cdot\frac{\Delta\omega_{0,tail}}{\omega_0}$.

The validity of this technique has been verified by comparing the oscillation frequency values resulting from PSS analyses carried out at 1.9 GHz, plotted in Fig. 6.6 as solid lines, with those resulting from the method discussed above, taking into account the overall effect of c_{gs}, c_{gd} and c_{tail}. The resulting curves are plotted in Fig. 6.6 as dashed lines, confirming the good

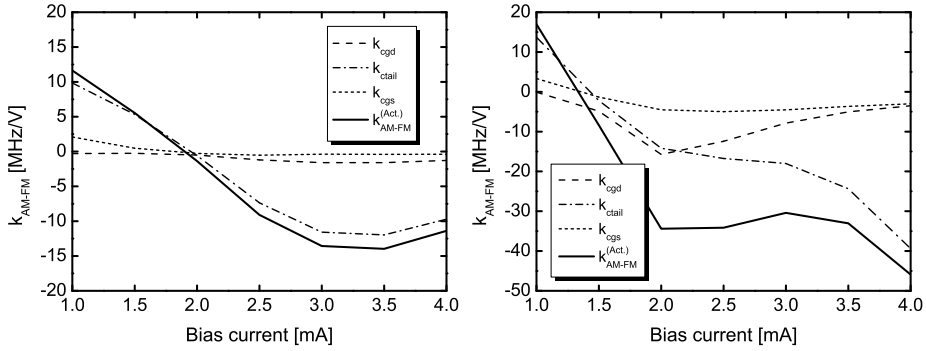


Figure 6.7: *Simulated contributions of $k_{AM-FM}^{(Act.)}$ as function of bias current I_B for $W = 15\,\mu$m (a) and $W = 75\,\mu$m (b).*

accuracy of the simulation method.

The single contributions to the frequency sensitivity associated to the different class of parasitics are instead shown in Fig. 6.7(a) and Fig. 6.7(b) for $W = 15\,\mu$m and $W = 75\,\mu$m , respectively. These simulation results confirm that the null of $k_{AM-FM}^{(\text{Act.})}$ occurs at a larger I_B for a smaller transistor width. The corresponding curves of oscillation frequencies in Fig. 6.6 show a maximum value corresponding to the zero-crossing of $k_{AM-FM}^{(\text{Act.})}$. By comparing Fig. 6.7(a) and Fig. 6.7(b), two observations must be pointed out:

- for both values of W, the dominant contribution is the sensitivity term related to the modulation of c_{tail}, although relatively-small transistors (M_3 and M_4) were used for the biasing circuit. This term is responsible for the $k_{AM-FM}^{(\text{Act.})}$ to cross the zero value, since it is positive for smaller bias current and then diminishes as I_B increases.

- for a larger transistors width W, the term related to c_{gd} is also significant. Since this term is always negative, the null of $k_{AM-FM}^{(\text{Act.})}$ is reached for a lower value of the bias current.

In the following, the impact of the three classes of parasitics will be discussed more in detail.

Figure 6.8(a) shows the simulated values of $c_{gd,0}$ as function of oscillation amplitude. In this case, being both c_{gd} directly connected between the two output nodes, the effective capacitance is simply given by $2c_{gd,0}$.

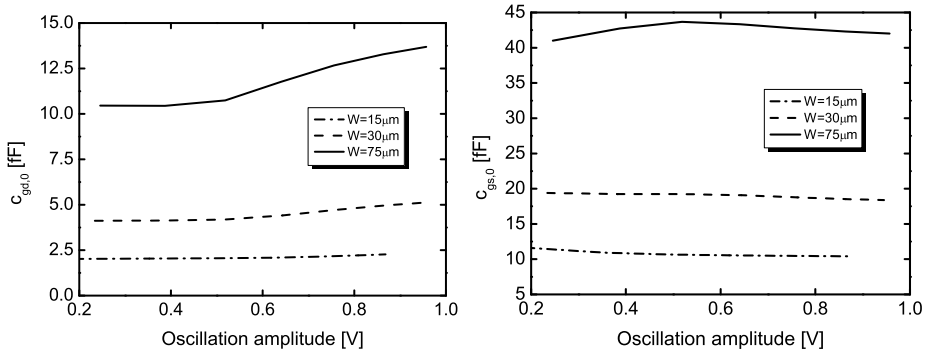


Figure 6.8: *Simulated average values of gate-drain capacitance $c_{gd}(t)$ (a) and gate-source capacitance $c_{gs}(t)$ (b) of M_1 as function of oscillation amplitude.*

As discussed in Section 2.6.2, the average value of the gate-drain parasitic capacitance increases with A_1 since M_1 operates in ohmic region for a larger portion of the oscillation period. As a consequence, the contribution given by the gate oxide capacitance tends to dominate with respect to the one given by the overlap capacitance. Moreover, since $c_{gd,0}$ monotonically increases with A_1, the sensitivity term associated to c_{gd} is always negative.

On the other hand, the gate-source capacitance is much less sensitive to the operating point since it approximately varies from $\frac{2}{3}C'_{ox}WL$ when M_1 works in saturation region to $\frac{1}{2}C'_{ox}WL$ when it enters the ohmic region. The time-average value $c_{gs,0}$ is plotted in Fig. 6.8(b). As far as the effective capacitance is concerned, its value is almost given by $2c_{gs,0}$.

6.4 The impact of the tail capacitance

As far as the tail capacitance concerns, its contribution to the effective tank capacitance is also strongly dependent on the working regions of the switching pair transistors. In [18], an analysis of the impact of c_{tail} on the oscillation frequency is carried out in case of M_1 and M_2 working in saturation or off region, i.e. for small oscillation amplitude. In this section, the analysis is refined and extended to the case when the two switching transistors enter the ohmic region.

The equivalent circuit to compute the effective c_{tail} in case of small oscillation amplitude in shown in Fig. 6.9. The output voltages can be taken

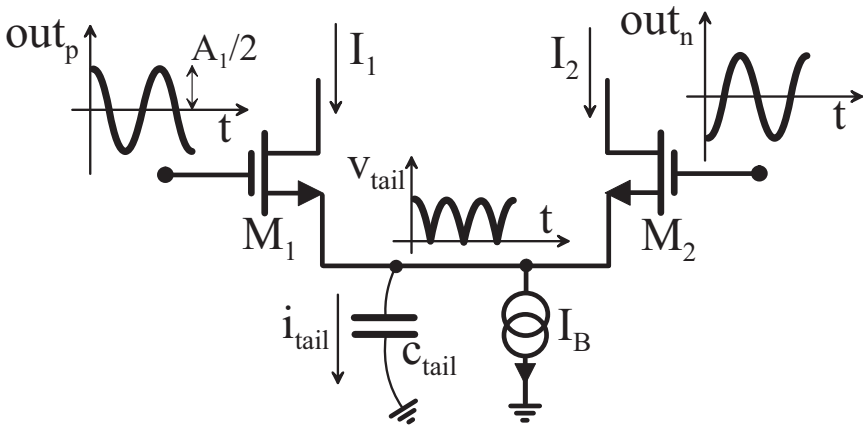


Figure 6.9: *Equivalent circuit to compute the effective c_{tail} in case of M_1 and M_2 working in saturation region, i.e. for small oscillation amplitude.*

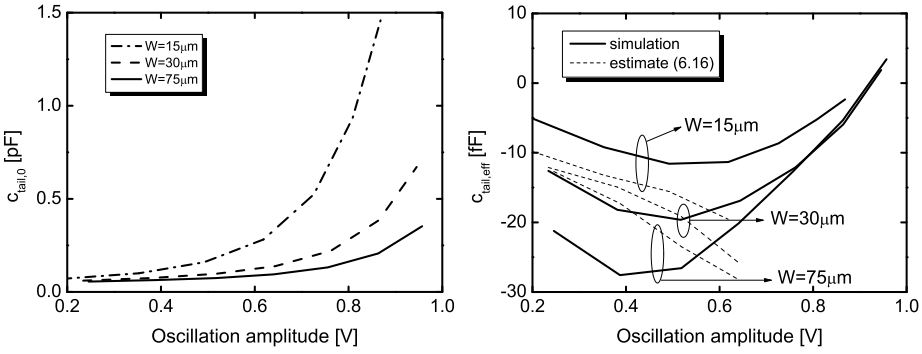


Figure 6.10: *Simulated average values of tail capacitance as function of oscillation amplitude (a). Effective capacitance "seen" by the tank due to c_{tail} obtained by means of simulations (solid lines) and by approximated analytical expression given by (6.16) (dashed lines) (b).*

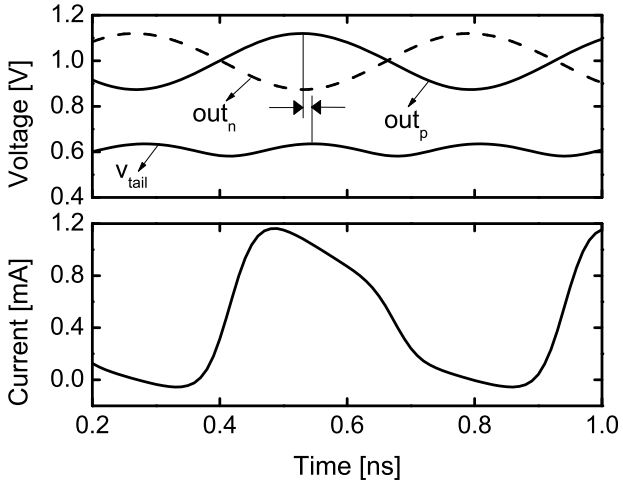


Figure 6.11: *Simulated waveforms of out_p, out_n, v_{tail} and I_1 flowing through M_1 for $I_B = 1\,mA$, corresponding to a small oscillation amplitude of about $300\,mV$.*

as:

$$\begin{cases} out_p = \frac{A_1}{2}\cos(\omega_0 t) \\ out_n = -\frac{A_1}{2}\cos(\omega_0 t) \end{cases} . \tag{6.13}$$

The time-average tail capacitance has been computed by means of circuit simulation and is plotted in Fig. 6.10(a) as function of oscillation amplitude for different values of W. The increase of c_{tail} with A_1 can be explained noting that a larger oscillation amplitude reduces the average drain-source voltage of the transistor M_3, increasing its c_{gd}, which is a major component of c_{tail}.

Since the circuit acts as a source-follower stage, the tail node voltage resembles a rectified cosine wave, being pulled up twice per oscillation period. This is confirmed by transient simulation results reported in Fig. 6.11. In general, denoting with $z_{tail} = \frac{1}{j2\omega_0 c_{tail,0}}$ the impedance of c_{tail} at $2\omega_0$ and with g_m the DC small-signal transconductance of M_1 and M_2, the phasor associated to the second harmonic of the tail node voltage can be written as:

$$\overrightarrow{v_{tail}} = \frac{A_1}{4}\left|\frac{z_{tail}}{z_{tail}+1/g_m}\right| e^{-j\arctan\left(\frac{1}{g_m|z_{tail}|}\right)}.$$

The phasor associated to the current at $2\omega_0$ flowing through the tail capacitance can be thus derived as:

$$\overrightarrow{i_{tail}} = \frac{A_1\omega_0 c_{tail,0}}{2\sqrt{1+\left(\frac{2\omega_0 c_{tail,0}}{g_m}\right)^2}} e^{j\arctan\left(\frac{g_m}{2\omega_0 c_{tail,0}}\right)}.$$

Due to the presence of c_{tail}, the current at the fundamental frequency flowing through M_1 and M_2 has an additional term, resulting from i_{tail} mixed with the first and third harmonic of the square wave in (6.2). As an example, the quadrature component at ω_0 of I_1 flowing through M_1 is given by:

$$I_{1,Q} = \frac{2}{3\pi} \cdot \frac{A_1\omega_0 c_{tail,0}}{\sqrt{1+\left(\frac{2\omega_0 c_{tail,0}}{g_m}\right)^2}} \sin\left[\arctan\left(\frac{g_m}{2\omega_0 c_{tail,0}}\right)\right], \tag{6.14}$$

where the factor $\frac{2}{3\pi}$ derives from $\frac{s_1-s_3}{2}$.

By equating $I_{1,Q}$ with the quadrature component flowing through the left half of the tank, it results:

$$\left(\frac{1}{j\omega_0 L/2} + j\omega_0 2C\right)\frac{A_1}{2} = j\frac{2}{3\pi} \cdot \frac{A_1\omega_0 c_{tail,0}}{\sqrt{1+\left(\frac{2\omega_0 c_{tail,0}}{g_m}\right)^2}} \sin\left[\arctan\left(\frac{g_m}{2\omega_0 c_{tail,0}}\right)\right].$$

It is evident that c_{tail} results into an effective negative capacitance. If placed differentially across the two outputs, its value is given by:

$$c_{tail,eff} \cong -\frac{2}{3\pi} \cdot \frac{c_{tail,0}}{\sqrt{1+\left(\frac{2\omega_0 c_{tail,0}}{g_m}\right)^2}} \sin\left[\arctan\left(\frac{g_m}{2\omega_0 c_{tail,0}}\right)\right]. \tag{6.15}$$

In the case when $2\omega_0 c_{tail,0} < g_m$, (6.15) can be simplified to:

$$c_{tail,eff} \cong -\frac{2}{3\pi} \cdot \frac{c_{tail,0}}{1+\left(\frac{2\omega_0 c_{tail,0}}{g_m}\right)^2}. \tag{6.16}$$

Note that (6.16) is a more refined version of the expression given in [18], where the factor $\frac{2}{3\pi}$ was not taken into account. The validity of (6.16) has been verified for the oscillator under test. The resulting curves of estimated $c_{tail,eff}$ are shown in Fig. 6.10(b) as dashed lines and fairly compare with the results obtained by means of simulations (solid lines).

By increasing the bias current, i.e. the oscillation amplitude, the effective capacitance first becomes more negative and then it increases, eventually becoming positive. The first trend derives from (6.16) and is due to the increase of $c_{tail,0}$, visible in Fig. 6.10(a). This can be explained noting the a

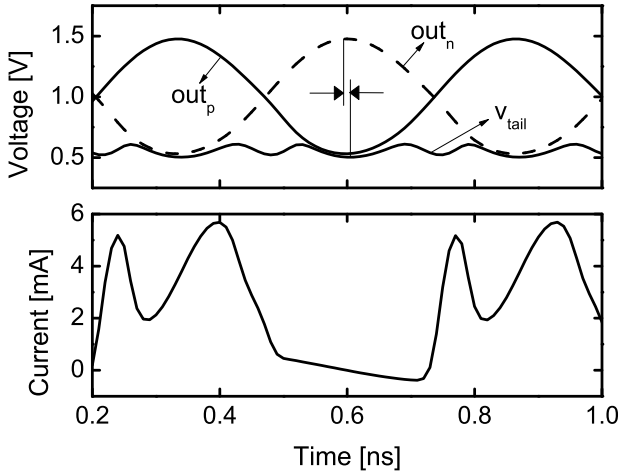


Figure 6.12: *Simulated waveforms of out_p, out_n, v_{tail} and I_1 flowing through M_1 for $I_B = 4\,mA$, corresponding to an oscillation amplitude of about $1\,V$.*

larger oscillation amplitude reduces the average drain-source voltage of the transistor M_3, increasing its c_{gd}, which is a major component of $c_{tail,0}$.

The rise of $c_{tail,eff}$, instead, requires a further investigation, since the approximation in (6.16) is no longer valid as far as the oscillation amplitude A_1 is larger than the threshold voltage of switching transistors. In such a condition, M_1 and M_2 start working either in ohmic or off region for most of the oscillation period. As a consequence, the circuit in Fig. 6.9 no more acts as a source follower, the tail node voltage being determined by drain nodes rather than by gate nodes. In particular, if their on-resistance is sufficiently small, the tail node voltage follows the negative swings of the drain nodes of M_1 and M_2, as confirmed by transient simulation results shown in Fig. 6.12. By taking out_p and out_n as in (6.13), v_{tail} approximately results a rectified cosine wave which is 180 degrees out of phase with respect to the previous case of small oscillation amplitude. The amplitude of the second harmonic of the tail node voltage is now dictated by the partition between z_{tail} and the on-resistance r_{on} of M_1 and M_2, rather than $1/g_m$.

Following the same procedure as before and taking into account these two aspects, the quadrature component of I_1 induced by c_{tail} can be written as:

$$I_{1,Q} \cong -\frac{2}{3\pi} \cdot \frac{A_1 \omega_0 c_{tail,0}}{1 + (2\omega_0 c_{tail,0} r_{on})^2}, \tag{6.17}$$

resulting into a positive $c_{tail,eff}$ given by:

$$c_{tail,eff} \cong \frac{2}{3\pi} \cdot \frac{c_{tail,0}}{1 + \left(2\omega_0 c_{tail,0} r_{on}\right)^2}. \tag{6.18}$$

Thus, the effective capacitance due to c_{tail} becomes positive for large oscillation amplitude and shows a minimum value, visible in Fig. 6.10(b), for $A_1 \approx V_{TH}$, where V_{TH} is the threshold voltage of the transistors, equal to $0.4\,\mathrm{V}$ in the considered technology. However, a smaller transistor width W results into a smaller variation of $c_{tail,eff}$ and hence of $k_{AM-FM}^{(\mathrm{Act.})}$, even if $c_{tail,0}$ is larger (see Fig. 6.10(a)). In fact, a smaller W translates into a smaller g_m and a larger r_{on}, thus decoupling tail and tank capacitances and resulting into a lower partition factor.

6.5 The direct contribution: a final remark

In Section 6.4 it has been shown that the presence of c_{tail} is responsible for the current of M_1 to slightly lead or lag with respect to the output voltage. This is due to the presence of the quadrature component expressed by (6.14) or (6.17), depending on the oscillation amplitude. The reader may thus wonder if a significant direct contribution to $1/f^3$ phase noise arises due to the tail capacitance. In general, the answer is affirmative. However, it must be pointed out that the direct contribution undergoes the same partial cancellation occurring for the AM-to-PM conversion effect. This is because a direct injection into the tank of PM current component arises from both noise sources $i_{n,1}$ and $i_{n,0}$, the latter contributing with the noise folded around the second harmonic. Similarly to the case of AM-to-PM conversion discussed in Section 6.2, the two current sources are correlated and their effects on output voltage tend to cancel out each other.

By means of (1.4) and (2.67), the power spectral density of output voltage noise due to direct injection induced by $i_{n,1}$ and $i_{n,0}$ can be written as:

$$\begin{cases} i_{n1} \Rightarrow \sqrt{S_V\left(\omega_0 \pm \omega_m\right)} = \xi\left(\omega_m\right) A_1 m_1 h_1 \sin\left(\varphi_m^{(1)}\right) & (6.19) \\ i_{n0} \Rightarrow \sqrt{S_V\left(\omega_0 \pm \omega_m\right)} = \xi\left(\omega_m\right) A_1 m_2 h_2 \cos\left(\varphi_h^{(2)} - \varphi_m^{(2)}\right), & (6.20) \end{cases}$$

where $\xi\left(\omega_m\right) = \frac{\sqrt{S_{1/f}(\omega_m)}}{2\omega_m}$. It can be easily shown that right-hand sides of (6.19) and (6.20) have same magnitude but opposite phase. In (6.20),

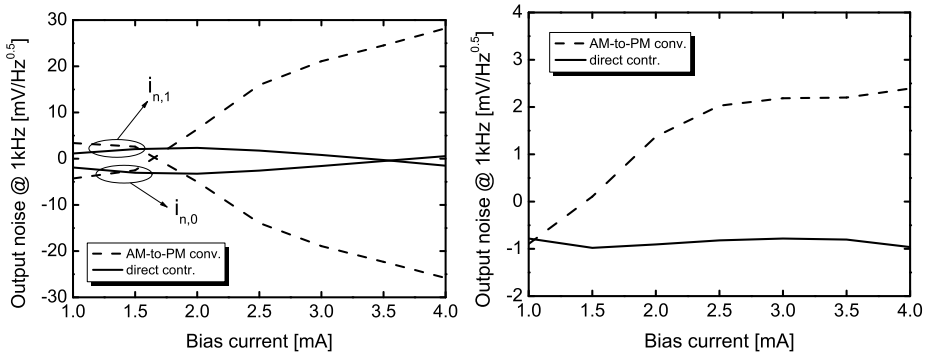


Figure 6.13: *Simulated output voltage noise contributions due to AM-to-PM conversion and direct injection induced by $i_{n,1}$ and $i_{n,0}$ for $W = 75\,\mu$m (a). Total noise components resulting from summing the contributions of both noise sources (b).*

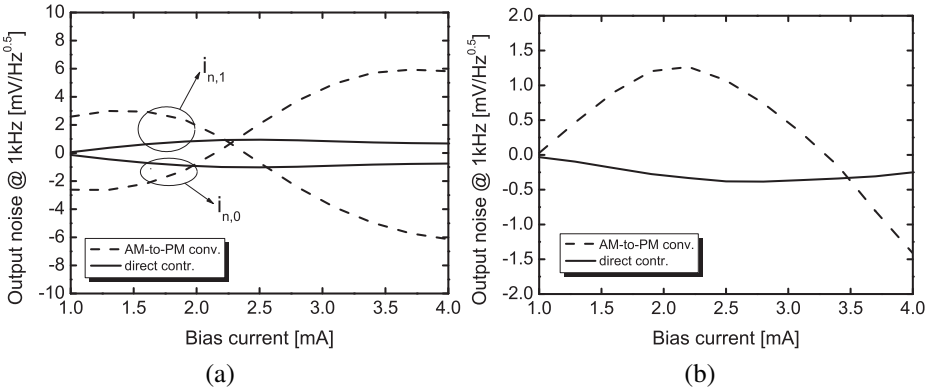


Figure 6.14: *Simulated output voltage noise contributions due to AM-to-PM conversion and direct injection induced by $i_{n,1}$ and $i_{n,0}$ for $W = 15\,\mu$m (a). Total noise components resulting from summing the contributions of both noise sources (b).*

$m_1 \sin\varphi_m^{(1)} \cong m_2 \sin\varphi_m^{(2)}$, since both quadrature components at ω_0 and $2\omega_0$ of the MOSFET current arise due to the current flowing through c_{tail} mixed by the the square wave in (6.2). On the other hand, $h_2 \cong h_1$ and $\varphi_h^{(2)} \cong -\frac{\pi}{2}$. The first and second harmonic components of the ISF, in fact, are associated to same phase noise generation mechanism but phase perturbations induced from $i_{n,0}$ and $i_{n,1}$ have opposite sign, similarly to the case of AM-to-PM conversion described in Section 6.2.

This analysis is confirmed by circuit simulations. Figure 6.13(a) shows the simulated output voltage noise contributions due to AM-to-PM conversion and direct injection induced by $i_{n,1}$ and $i_{n,0}$ for $W = 75\,\mu$m. The total noise components resulting from summing the contributions of both noise sources are instead shown in Fig. 6.13(b).

As expected, the two phase noise contributions due to direct injection reach their peaks when the magnitude of the effective tail capacitance reach its maximum value. On the other hand, for the same value of bias current the two AM-to-PM contributions drop to zero, as the derivative $\frac{\partial c_{tail,eff}}{\partial A_1}$ is null, as visible in Fig. 6.10(b). In practice, the presence of a direct contribution term results into the minimum of phase noise to occur for a slightly-different value of I_B.

However, since the strength of direct injection increases with $c_{tail,eff}$, this component is reduced by adopting smaller widths of switching transistors, with obvious benefit in terms of overall $1/f^3$ phase noise. The noise decomposition has been performed also on the oscillator featuring a W equal to $15\,\mu$m and the simulation results are plotted in Fig. 6.14(a) and (b). In this case, the impact of the direct injection is completely negligible, the $1/f^3$ phase noise being determined only by the AM-to-PM component.

6.6 Conclusions

In this chapter, the flicker noise up-conversion mechanisms in current-biased oscillators have been discussed and clarified. In particular, it has been shown that the $1/f^3$ phase noise is mostly due to an AM-to-PM conversion arising from modulation of non-linear parasitic capacitances of the transconductor stage. A quantitative insight into this phenomenon has been carried out, highlighting that the AM-to-FM sensitivity term associated to the tail capacitance is the dominant contribution to the overall sensitivity. The impact of the tail capacitance has been further investigated, pointing out its dependence on oscillation amplitude and width of switching tran-

sistors. In particular, it has been clarified why the AM-to-FM sensitivity is null for a particular value of bias current, which can be adjusted by the circuit designer by adopting a sufficiently small transistors width.

CHAPTER 7

Measurement results

7.1 Introduction

In Chapter 6, the $1/f^3$ phase noise generation in differential current-biased LC oscillator has been analyzed in detail. It has been pointed out that the AM-to-PM conversion due to the presence of a large tail capacitance is the dominant mechanism. This noise component is null for a particular value of bias current which can be adjusted in order to achieve also a larger FoM for the $1/f^2$ phase noise. This can be accomplished by simply adopting smaller transistor width for the switching pair. In this chapter, the validity of the proposed analysis is verified by means of measurements carried out on a few test chips. Two current-biased oscillators have been fabricated on the same die with different size of the transistors of the differential pair.

Measurements results confirms a reduction of flicker noise up-conversion of about 7 dB in case of smaller width with no impairment of the $1/f^2$ phase noise. However, since the measured values of $1/f^3$ phase noise are larger than those predicted by simulations, the model describing phase noise generation has been revised. A more accurate model of flicker noise up-conversion is proposed, which captures the effect of partial correlation

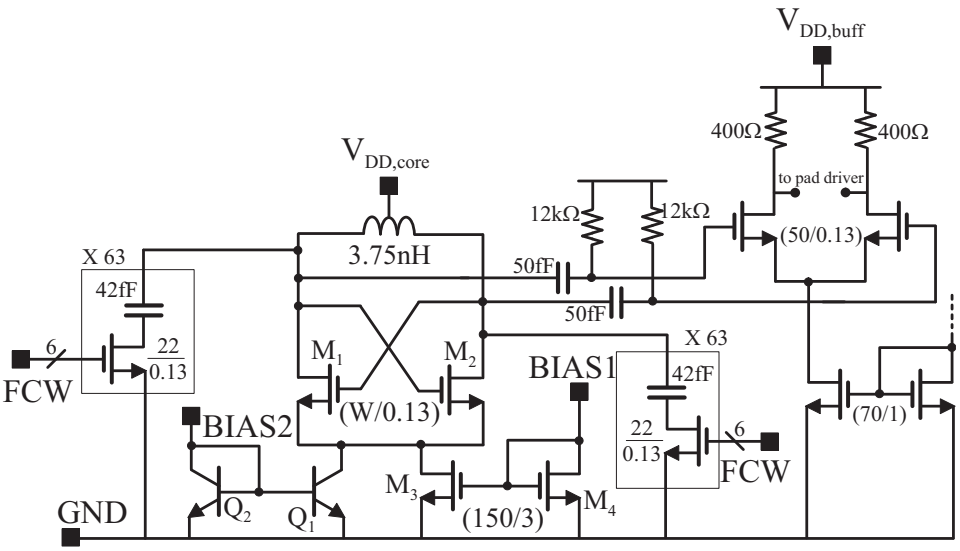


Figure 7.1: *Schematic of the fabricated oscillator. Two versions have been implemented on the same die employing $W = 15\,\mu m$ and $W = 75\,\mu m$.*

between noise side-bands by taking into account the non-instantaneous response of noise to variation of bias conditions.

7.2 The fabricated oscillators

The circuit analyzed in Chapter 6 has been fabricated in a 0.13-μm CMOS technology with 1.2-V nominal voltage supply. The complete schematic is shown in Fig. 7.1. The voltage supply of the core part of the circuit was set equal to $V_{DD,core} = 1\,\text{V}$. The oscillator also features a bipolar transistors biasing circuit, in order to provide reference numbers of measured $1/f^3$ phase noise which is free of noise induced from the tail transistors. The bias current I_B injected at nodes BIAS1 or BIAS2 ranges between 1 and $4\,\text{mA}$. Two versions of the same oscillators have been implemented on the same die, namely OSC1 and OSC2, employing $W = 15\,\mu\text{m}$ and $W = 75\,\mu\text{m}$, respectively. The microphotograph of the die is shown in Fig. 7.2. Transistors M_3 and M_4 of biasing circuit have been sized with $(W/L)_{3,4} = (150/3)$ for their $1/f^3$ phase noise contribution to be negligible, while at the same time avoiding to introduce a large tail capacitance c_{tail}. The tank inductance was set equal to $L = 3.75\,\text{nH}$. A discrete tuning scheme employing 63 MIM-based capacitance cells allows to vary the os-

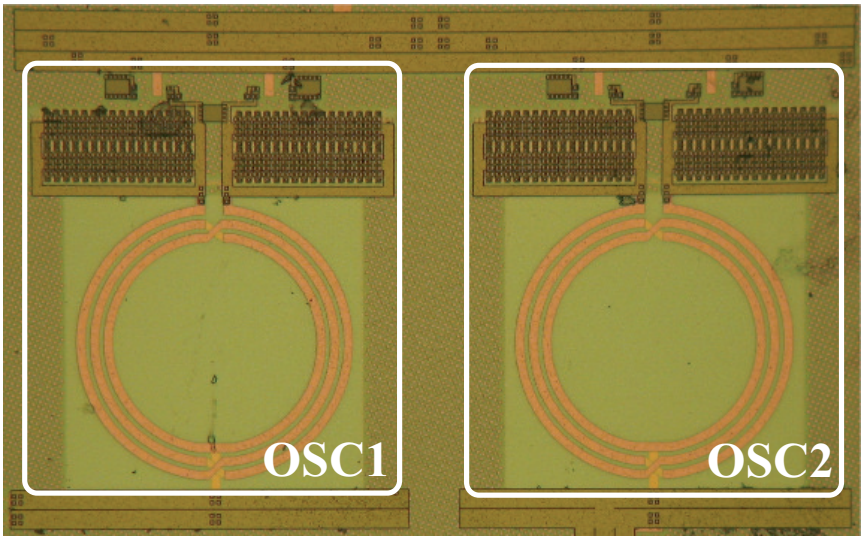


Figure 7.2: *Die microphotograph of the fabricated oscillators. OSC1 and OSC2 refer to the oscillators featuring $W = 15\,\mu m$ and $W = 75\,\mu m$, respectively.*

cillation frequency between 1.9 to $2.6\,\text{GHz}$. The measured quality factor Q is about 7 at $2.5\,\text{GHz}$.

7.3 Measurement results

Phase noise measurements have been carried out by employing an Anritsu MS2690A signal analyzer running the phase noise measurement option. The measured $1/f^3$ phase noise of both oscillators is shown in Fig. 7.3(a) and (b), quoted as SSCR at 1-kHz frequency offset from the 1.9-GHz and 2.6-GHz carrier, respectively. Since exactly the same phase noise is obtained biasing the circuit with bipolar and MOS transistors, it is possible to conclude that flicker noise from tail devices results into a negligible contribution, the overall $1/f^3$ phase noise being only due to the switching pair.

Since the minimum of SSCR at 1-kHz offset occurs at the peak of the measured oscillation frequency, plotted in Fig. 7.4(a) and (b), the flicker noise up-conversion is due to the AM-to-PM conversion effect described in Section 6.3. As expected, the minimum AM-to-FM sensitivity of OSC1 occurs at a larger bias current with respect to OSC2, which is closer to the cross-over region between current- and voltage-limited regime. This is confirmed by observing the curves of $1/f^2$ phase noise, quoted as SSCR

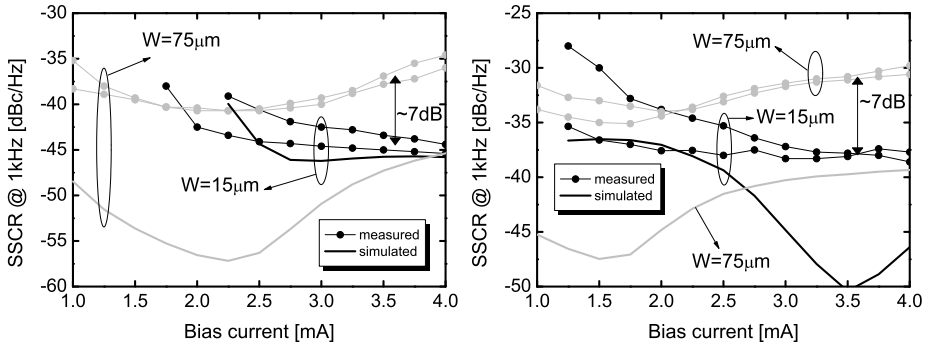


Figure 7.3: *SSCR at 1-kHz frequency offset from the 1.9-GHz (a) and 2.6-GHz (b) carrier of two samples of the fabricated oscillators.*

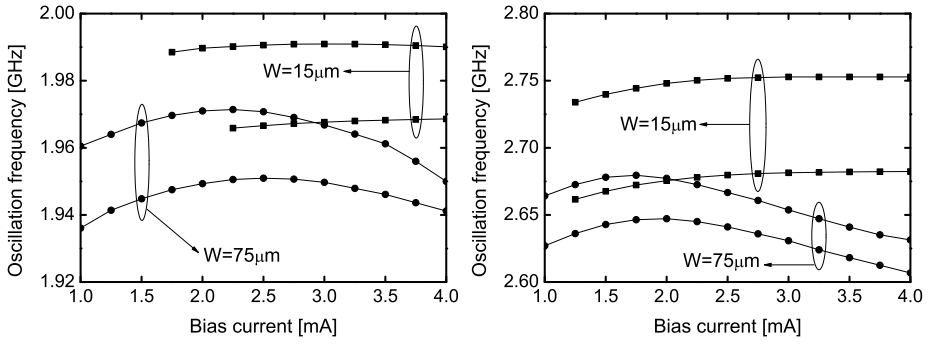


Figure 7.4: *Oscillation frequency of two samples of the fabricated oscillators as function of bias current at lower (a) and higher (b) end of the tuning range.*

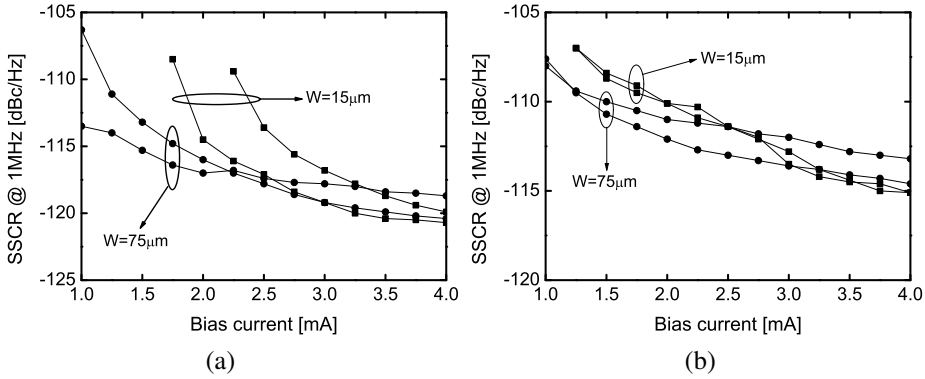


Figure 7.5: *SSCR at 1-MHz frequency offset from the 1.9-GHz (a) and 2.6-GHz (b) carrier of two samples of the fabricated oscillators.*

at 1-MHz frequency offset and shown in Fig. 7.5(a) and (b), their plateau region corresponding to $I_B \cong 3.5\,\text{mA}$.

Moreover, the $1/f^2$ phase noise is almost the same for OSC1 and OSC2, confirming that it is not affected by the adoption of smaller transistors for the switching pair. On the other hand, a reduction of more than $7\,\text{dB}$ of flicker noise up-conversion is achieved in OSC1 with respect to OSC2 at both lower and upper end of the frequency span. The reduction is obtained for a bias current $I_B = 3.5\,\text{mA}$, which maximizes the figure of merit. However, the measured $1/f^3$ phase noise is larger than predicted by SpectreRF simulator, whose results are plotted in Fig. 7.3(a) and (b) as solid lines. A discrepancy of about $10\,\text{dB}$ exists between measured and simulated values, except for OSC1 running at $1.9\,\text{GHz}$, where it is limited to a few dB.

At this point, the reader may thus wonder why the phase noise generation model so far adopted fails to accurately predict flicker noise up-conversion in the current-biased oscillator while it succeeds in the case of voltage-biased topology, as demonstrated in Chapter 5. The difference between the two circuits lies in correlation between noise side-bands playing a crucial role in determining the $1/f^3$ phase noise of current-biased oscillator, as discussed in Chapter 6. On the contrary, only the flicker noise folded around the first harmonic is responsible for $1/f^3$ phase noise in the voltage-biased counterpart.

The limitations of the NMF-approach starting from a single modulated noise process have been discussed in several papers [82–88], where various authors have investigated the generation of noise side-bands from low-

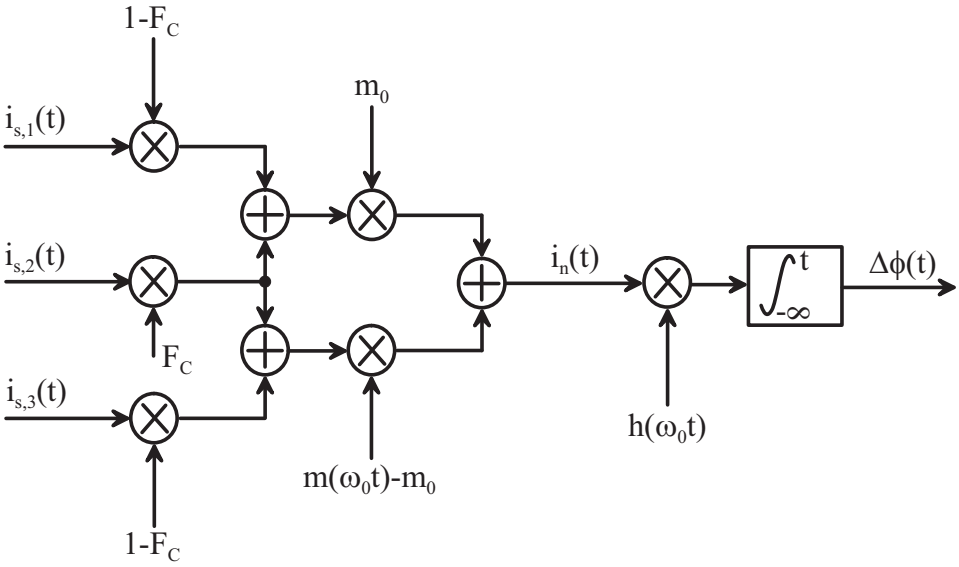


Figure 7.6: *Phase noise generation scheme accounting for partial correlation between up-converted flicker noise side-bands.*

frequency noise sources using physical device simulations. In [82], Bonani *et al.* claim that it is not clear *a priori* whether noise resulting from modulation of a slow stationary process can be ascribed as a pure low-frequency noise, a fully-correlated cyclostationary process or a mixture of both. This is due to the presence of a large number of microscopic noise sources within the device, which, in general, undergo different modulating functions. As a consequence, it is sometimes difficult to describe their overall effect by means of a single equivalent lumped source at the terminals of the device.

The NMF-based approach adopted so far can thus lead to an overestimated correlation between baseband noise and RF noise side-bands [87]. In Section 7.4, based on the work of Bonani and Rudolph, the phase noise generation model is revised and extended to take into account the partial correlation between noise side-bands, eventually justifying the discrepancy between measurement and simulation results for the current-biased oscillator topology.

7.4 An accurate phase noise generation model

Partial correlation of up-converted flicker noise side-bands results from low-frequency noise due to traps being affected by a different strength of modulation. In [83], it has been observed that the relative contribution of generation-recombination (GR) noise to the collector current noise in a bipolar device depends on the spatial location of GR centres. In [85], physical device simulations on a *p-n* junction diode show that traps located in the proximity of ohmic contacts yield terminal fluctuations whose frequency conversion is milder than in the case of traps in the depletion region.

A model to describe the noise of device operating in large-signal regime is presented in [87], which allows to control the amount of the inter-harmonic cross-correlation. To resort to this description, the phase noise generation block scheme in Fig. 2.11 so far adopted can be redrawn as depicted in Fig. 7.6, where $i_{s,1}$, $i_{s,2}$ and $i_{s,3}$ are three independent stationary processes with a $1/f$-shaped frequency spectrum. The factor F_C controls the correlation between baseband and RF noise side-bands and is thus referred to as *correlation factor*. In the case $F_C = 1$, the block schemes in Fig. 2.11 and Fig. 7.6 are equivalent and the non-stationary process $i_n(t)$ is simply derived by multiplying $i_{s,2}(t)$ by the NMF $m(t)$. On the other hand, when $F_C = 0$, the baseband part of $i_n(t)$ is due to $i_{s,1}$ multiplied by the DC component of $m(t)$, m_0, and is completely uncorrelated with noise side-bands around the harmonics, which instead result from $i_{s,3}(t)$ multiplied by the RF part of $m(t)$.

This description has been employed to compute the $1/f^3$ phase noise of OSC2 running at $1.9\,\text{GHz}$. No further refinement of the simulation technique proposed in Chapter 4 is necessary. The resulting SSCR at 1-kHz frequency offset is plotted in Fig. 7.7 as function of the correlation factor and compared to measurements results. Even though the reduction of correlation can lead to more accurate results, especially for values of F_C close to 0.75, the description in [87] is still not able to predict the phase noise plateau occurring for I_B around $2.5\,\text{mA}$. Referring to the analysis carried out in Chapter 6, as far as the correlation factor approaches zero, the $1/f^3$ phase noise contributions due to AM-to-PM conversion from flicker noise around DC and fundamental frequency no more cancel out each other but rather sum up in power, resulting into a larger $1/f^3$ phase noise. Its null, however, is still present, since the two contributions cross zero for the same value of bias current.

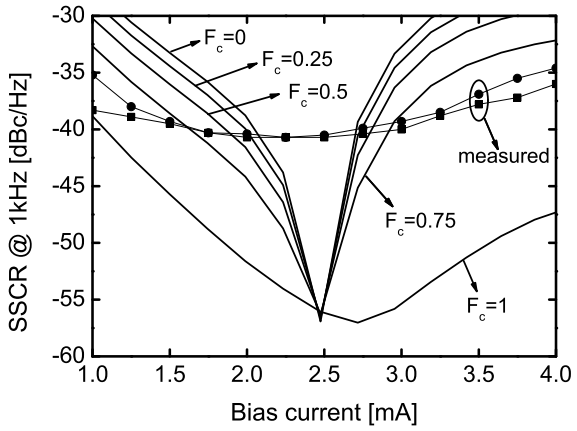


Figure 7.7: *SSCR of OSC2 at 1-kHz frequency offset from the 1.9-GHz carrier as function of the bias current. Symbols refer to measured values, while lines refer to those predicted by Rudolph and Bonani's model depicted in Fig. 7.6 as function of the correlation factor F_C.*

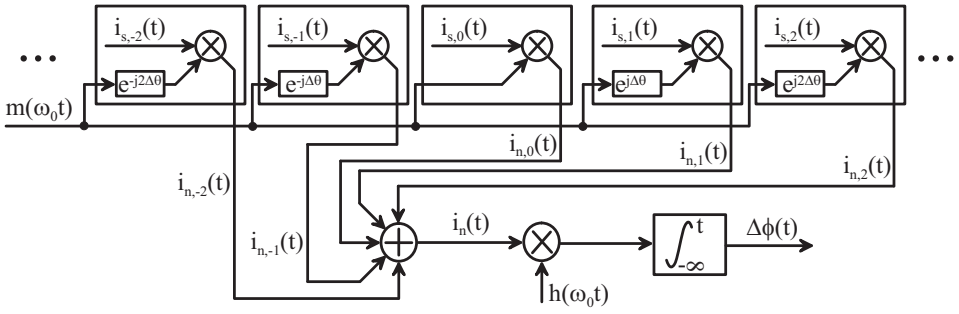


Figure 7.8: *Phase noise generation scheme accounting for non-instantaneous dependence of low-frequency microscopic sources within the device on bias conditions.*

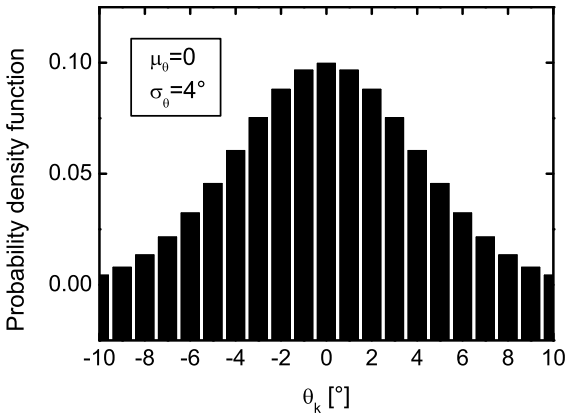


Figure 7.9: *Discrete probability density function of phase shift θ_k .*

In the following, a new model is proposed, where the assumption of instantaneous response of each trap to variation of bias condition is removed. Instead, it is postulated that low-frequency microscopic noise contributions are up-converted by different modulating functions. These functions are delayed or anticipated replicas of $m(t) = \sqrt{I_{DS}(t)}$, the former case occurring for traps with larger time constants and vice versa. Thus, the RF noise at MOSFET terminals results from summation of uncorrelated terms. Each of these contributions is given by the product of a stationary process $i_{s,k}$ multiplied by a different modulating function $m\left(\omega_0 t + \theta_k\right)$. Being output fluctuations due to trapping phenomena independent of each other, the low-frequency process $i_{s,m}$ is uncorrelated with $i_{s,n}$ if $m \neq n$.

Since the phase shift θ_k is a random variable, the power spectral density of $i_{s,k}$ is properly scaled accounting for its statistical distribution. It is expected that θ_k spreads around 0, meaning that the simple SPICE2 flicker noise model adopted so far only describes an "average" response of microscopic sources to modulation.

The proposed phase noise generation mechanism is depicted in Fig. 7.8, which features a discrete number of delay blocks. The two parameters N and θ_k of the scalable model can be derived from measurement results.

However, simulation show that the discretization has a negligible impact on final result, as far as $N > 10$. In this case, $N = 21$ is taken. With regard to θ_k, a Gaussian distribution is assumed with zero mean and variance equal to 4°. The corresponding probability density function is plotted in Fig. 7.9. The proposed model was slightly extended in order to take into account

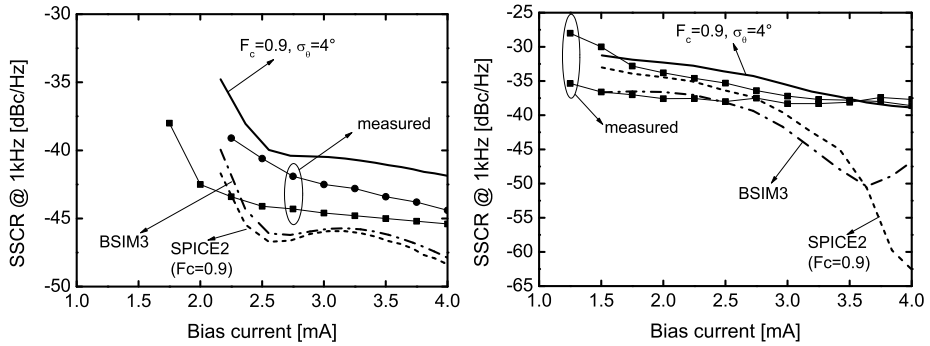


Figure 7.10: *SSCR at 1-kHz frequency offset from the 1.9-GHz (a) and 2.6-GHz (b) carrier of the fabricated oscillator with $W = 15\ \mu$m. Symbols refer to measured values, while lines refer to simulation performed with BSIM3.3 model (full correlation, dash-dotted line), SPICE2 adopting a correlation factor equal to 0.9 (Bonani's model, dashed line) and SPICE2 model with $F_C = 0.9$ and $\sigma_\theta = 4°$ (proposed model, solid line).*

also the presence of almost-stationary noise from traps located near ohmic contacts, as in the model of Bonani. However, this refinement only results into a minor improvement of accuracy, since a correlation factor close to unity, $F_C = 0.9$, was found to provide the best fitting.

The overall description is able to accurately predict the $1/f^3$ phase noise for both OSC1 and OSC2 running at 1.9 and 2.6 GHz. Figures 7.10 and 7.11 compares the SSCR at 1-kHz frequency offset obtained by chip measurements (symbols), SpectreRF PNOISE simulation with BSIM3.3 model (full correlation, dash-dotted lines) and simulation method described in Chapter 4 with Bonani's model with $F_C = 0.9$ (dashed lines) and proposed model (solid lines).

Clearly, also the phase noise generation scheme in Fig. 7.8 provides a reduction of the inter-harmonic correlation, although in this case it is not limited to baseband and RF noise. Regarding flicker noise up-conversion, the dominant mechanism is still the AM-to-PM conversion effect due to the presence of tail capacitance for both oscillators. However, the different phase shift of modulating functions associated to each microscopic source leads to a different direct contribution, which can even results into a non-negligible term for negative values of θ_k. Since the main effect of the direct contribution is to "move" the minimum of phase noise towards a different bias current value, as explained in Section 6.5, the destructive interference

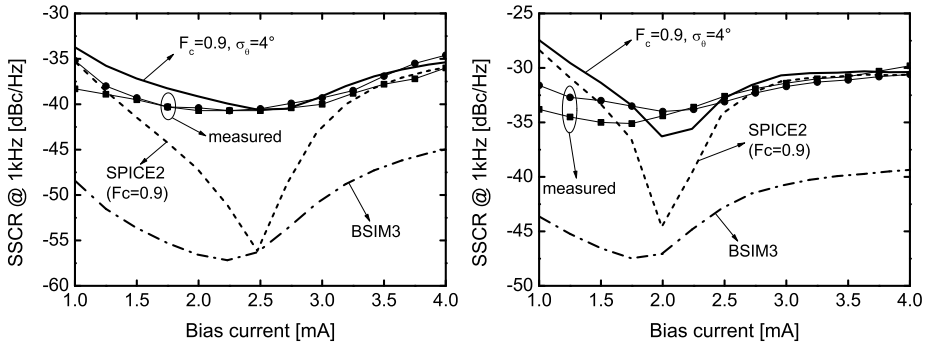


Figure 7.11: *SSCR at 1-kHz frequency offset from the 1.9-GHz (a) and 2.6-GHz (b) carrier of the fabricated oscillator with $W = 75\ \mu$m. Symbols refer to measured values, while lines refer to simulation performed with BSIM3.3 model (full correlation, dash-dotted line), SPICE2 adopting a correlation factor equal to 0.9 (Bonani's model, dashed line) and SPICE2 model with $F_C = 0.9$ and $\sigma_\theta = 4°$ (proposed model, solid line).*

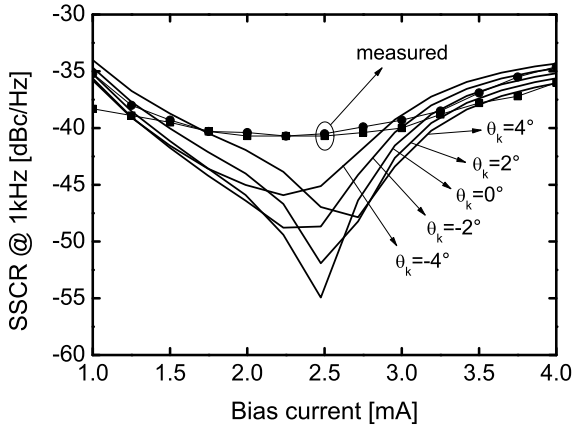


Figure 7.12: *SSCR of OSC2 at 1-kHz frequency offset from the 1.9-GHz carrier as function of the bias current. Symbols refer to measured values, while lines refer to contributions associated to different values of phase shift affecting the modulating function in the proposed model.*

no more occurs. This situation is depicted more clearly in Fig. 7.12, which shows a set of $1/f^3$ phase noise curves induced from non-stationary processes $i_{n,k}$ of OSC2 running at $1.9\,\text{GHz}$.

7.5 Conclusions

In this chapter, the validity of the phase noise analysis presented in Chapter 6 has been verified by means of measurements carried out on a few test chips. Two current-biased oscillators have been fabricated on the same die with different size of the transistors of the differential pair. Measurements results confirms a reduction of flicker noise up-conversion of about 7 dB in case of smaller width with no impairment of the $1/f^2$ phase noise. A further investigation has also been carried out in order to explain the discrepancy between measured and simulated values of $1/f^3$ phase noise. A revised model of flicker noise up-conversion was proposed, which captures the effect of partial correlation between noise side-bands by taking into account the non-instantaneous response of noise to variation of bias conditions.

CHAPTER 8

Conclusions

A summary of the most important original contributions of this thesis is given below.

Regarding flicker noise up-conversion in voltage-biased oscillators, it is shown that modulation of harmonic content is the main cause of $1/f^3$ phase noise generation. This effect has been quantitatively assessed and linked to the oscillator non-linearity. In particular, it has been demonstrated that two mechanisms play a fundamental role in the conversion of flicker noise into phase noise:

- the direct injection into the tank of PM tones since the current through active devices lags with respect to the voltage
- an AM-to-PM conversion effect due to the dependence of the oscillation frequency on the harmonic content of the output voltage.

Design equations have been derived which highlight that flicker noise up-conversion is reduced in case of low excess gain, translating into low distortion of the voltage output, and high tank quality factor (for a fixed excess

gain), providing a strong attenuation of higher-order harmonics.

The up-conversion can be mitigated by adopting resistors in series to the drain nodes of the transconductor transistors. The resistors, together with the parasitic drain capacitances, introduce a delay in the loop gain shifting both the ISF and the current waveform of the MOSFETs. It follows that $1/f$ noise up-conversion can be reduced by judiciously tailoring the component values without degrading the start-up margin or adopting resonant filters. A theoretical explanation and a quantitative analysis have been carried out, addressing in details the different effects. The analysis has been verified by means of experimental measurements on a 65-nm CMOS VCO.

Regarding the simulation of the impulse sensitivity function, a fast and accurate method based on periodic transfer function analysis for the impulse phase response in oscillators has been presented. The proposed technique overwhelms the traditional simulation method based on transient analysis in terms of both computation time and accuracy. In particular, the method is helpful every time the magnitude and phase of each ISF component is of interest.

An alternative solution to reduce the flicker noise up-conversion has been presented, where a segmented transconductor is adopted in order to keep the excess gain almost constant and close to 2 as the frequency spans over the broad 1.6-to-2.6-GHz interval, thus breaking the conflicting link between tuning range and $1/f^3$ phase-noise performance. The circuit has been fabricated in a 65-nm CMOS technology, demonstrating a reduction of $10\,\mathrm{dB}$ of the $1/f^3$ phase noise over a 47% tuning range, without impairing the $1/f^2$ phase noise performance. Moreover, measurement results are in good agreement with simulations, thus proving the validity of the NMF-based phase noise model adopted.

Regarding flicker noise up-conversion in current-biased oscillators, it has been shown that the $1/f^3$ phase noise is mostly due to an AM-to-PM conversion arising from modulation of non-linear parasitic capacitances of the transconductor stage. A quantitative insight into this phenomenon has been carried out, highlighting that the AM-to-FM sensitivity term associated to the tail capacitance is the dominant contribution to the overall

sensitivity. The impact of the tail capacitance has been further investigated, pointing out its dependence on oscillation amplitude and width of switching transistors. In particular, it has been clarified why the AM-to-FM sensitivity is null for a particular value of bias current, which can be adjusted by the circuit designer by adopting a sufficiently small transistors width. Measurements results confirms a reduction of flicker noise up-conversion of about $7\,\mathrm{dB}$ in case of smaller width with no impairment of the $1/f^2$ phase noise.

Regarding the validity of phase noise model in current-biased oscillators, a further investigation has also been carried out in order to explain the discrepancy between measured and simulated values of $1/f^3$ phase noise. A revised model of flicker noise up-conversion was proposed, which captures the effect of partial correlation between noise side-bands by taking into account the non-instantaneous response of noise to variation of bias conditions.

List of Publications

- **F. Pepe**, A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita. Suppression of flicker noise up-conversion in a 65-nm CMOS VCO in the 3.0-to-3.6 GHz band. *IEEE J. Solid-State Circuits*, 48(10):2375–2389 , October 2013.
- **F. Pepe**, A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita. Analysis and minimization of flicker noise up-conversion in voltage-biased oscillators. *IEEE Trans. Microw. Theory Tech.*, 61(6):2382–2394, June 2013.
- A. Bonfanti, **F. Pepe**, C. Samori, and A. L. Lacaita. Flicker noise up-conversion due to harmonic distortion in Van der Pol CMOS oscillators. *IEEE Trans. Circuits Syst. I: Reg. Paper*, 59(7):1418–1430, July 2012.
- P. Maffezzoni, **F. Pepe**, and A. Bonfanti. A unified method for the analysis of phase and amplitude noise in electrical oscillators. *IEEE Trans. Microw. Theory Tech.*, 61(9):3277–3284, September 2013.
- S. Levantino, P. Maffezzoni, **F. Pepe**, A. Bonfanti, and A. L. Lacaita. Efficient calculation of the impulse sensitivity function in oscillators. *IEEE Trans. Circuits Syst. II: Exp. Briefs*, 59(10):628–632, October 2012.
- **F. Pepe**, A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita. A wideband voltage-biased LC oscillator with reduced flicker noise up-

conversion. *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, pages 27–30, 2013.

- **F. Pepe**, A. Bonfanti, S. Levantino, P. Maffezzoni, C. Samori, and A. L. Lacaita. Simulating phase noise induced from cyclostationary noise sources. *Proc. IEEE Int. Symp. on Circ. and Syst. (ISCAS)*, pages 2686–2689, 2013.

- **F. Pepe**, A. Bonfanti, S. Levantino, P. Maffezzoni, C. Samori, and A. L. Lacaita. An efficient linear-time variant simulation technique of oscillator phase sensitivity function. *Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), International Conference on*, pages 17–20, 2012.

- **F. Pepe**, A. Bonfanti, and A. L. Lacaita. A fast and accurate simulation method of impulse sensitivity function in oscillators. *Proc. of MIPRO International Convention*, pages 66–71, 2012.

- **F. Pepe,** A. Bonfanti and S. Levantino and C. Samori and A. L. Lacaita. Reducing flicker noise up-conversion in a 65nm CMOS VCO in the 1.6 to 2.6 GHz band. *Proc. SPIE*, pages 876403–876403-9, 2013.

- **F. Pepe,** A. Bonfanti and S. Levantino and P. Maffezzoni and C. Samori and A. L. Lacaita. A simulation technique to compute phase noise induced from cyclostationary noise sources in RF oscillators. *Proc. SPIE*, pages 87640B–87640B-8, 2013.

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