POLITECNICO DI MILANO
DEPARTMENT OF PHYSICS
DOCTORAL PROGRAMME IN PHYSICS

DEVELOPMENT OF GRAPHENE-BASED INTEGRATED CIRCUITS FOR RADIO-FREQUENCY APPLICATIONS

Doctoral Dissertation of:
Erica Guerriero

Supervisor:
Prof. Roman Sordan

Tutor:
Prof. Franco Ciccacci

The Chair of the Doctoral Program:
Prof. Paola Taroni

2015 – XVII Cycle

To my grandmother

Acknowledgements

First of all I would like to express my gratitude to my supervisor, professor Roman Sordan, for the opportunity of working in his group. I am sincerely thankful for the patience demonstrated the thousands of times in which I came to the office asking for some obvious explanation, for being capable of transmit me the passion for electronics (or black magic) and for the help throughout this PhD.

I am really grateful to professor Herbert Zirath for the great opportunity to join his group in Chalmers and for the time dedicated to help me and teach me the basics of device modelling. I have really appreciated the helpful teachings and inspiring discussions.

A special thanks goes to all the Chalmers people, in particular to prof. Niklas Rorsman, prof. Omid Habibpour and Micheal Winters for the useful discussions and collaboration. Thanks to all the friends for the wonderful welcome (and welcome back), for moral (and practical) support, for the lots of 3p.m-fika, for the help with measurements (and with Christmas shopping) and for the fridays afterworks: Olle, César, David, Sebastian, Andreas, Mustafa, Helena, Marcus, Evgeni, James, Ankur, William, Koen, Anna, Christian and my officemate Per Åke. I had a really great time, thank you!

Grazie a tutti i miei graphene-colleghi: Max, Laura e Laura in primis per tutti i buoni insegnamenti, Marco, Paolo, Aida, Luca per aver condiviso con me e col grafene gioie (poche) e dolori (quelli non si fanno mai mancare). Grazie ai miei ex coinquilini: SCC (come te nessuno mai), generale Aghionski (l'unico vero signore, degno di tale nome, di via per brunate), e Fabio-fagiano-Isa (per avermi ceduto il suo posto!). Grazie a tutti i colleghi LNESS, primo su tutti l'indispensabile, saggio e onnipresente Marco Leone. Grazie anche a Luca, Ballabiò, Sergio, Daniela, Christian, Edo, Jacopo, Valeria, Monica, Danny, Alexey, il Profeta, Giovanni e chiunque mi sia rimasto tra le righe.

Una menzione speciale a quelli-del-fundedì: Tommy, Davi, Ciccio, Gighen, Campo, Casati e Ste.. posso riassumere quello che voglio (anzi no, hai ragione Tommy, che vorrei) dirvi con un "GRAZIE DELLA PRESENZA!".

E infine ma non meno importante un grazie alla mia famiglia, mamma, papà, Lele, zio e nonna.. e alla mia seconda famiglia: Raffa, Emilio, Tommy e Davide (ancora!). Grazie per la pazienza, per il supporto, per avermi lasciato partire e per avermi aspettata.

Contents

List of abbreviations and chemical compounds

2-D two-dimensional
AC alternate current
ADC analog to digital converter
ADS advanced design system
AFM atomic force microscopy
ALD atomic layer deposition
Al_2O_3 Aluminum oxide (alumina)
BASK binary-amplitude-shift keying
BJT bipolar junction transistor
BN boron nitride
CMOS complementary metal oxide semiconductor
CNT carbon nanotube
CVD chemical vapour deposition
DC direct current
DOS density of states
DUT device under test
ECL emitter coupled logic
EOT equivalent oxide thickness
FET field effect transistor
GFET graphene FET
HBT heterojunction bipolar transistors
HEMT high electron-mobility transistor
HfO_2 Hafnium oxide (hafnia)
HHMT high hole-mobility transistor
HOPG highly oriented pyrolitic graphite
FO fan-out
FOM figure of merit
IC integrated circuit
IF intermediate frequency
ITRS international roadmap of semiconductors

LCAO linear combination of atomic orbitals
GFET graphene field effect transistor
MOSFET metal-oxide-semiconductor field effect transistor
MOS-C metal-oxide-semiconductor capacitor
MoS_2 Molybdenum disulfide
OOK on-off keying
PFET p-type field effect transistor
PMMA poly-methil-metacrylate
NFET n-type field effect transistor
RF radio-frequency (3 kHz-300 GHz)
RO ring oscillator
SEM scanning electron microscope
SOI silicon-on-insulator
TiO_2 Titanium oxide (titania)
TLM transmission line method
TMAH tetramethylammonium hydroxide
VNA vector network analyzer

Abstract

Graphene is an attractive two-dimensional material that possesses peculiar mechanical, electrical and thermal properties. Motivated by the scaling limitations in conventional silicon technology, it was not long after graphene ultra-high mobility was measured in pioneering experiments, that the electronics community started an intensive research to demonstrate the possibilities of graphene to become the material of future electronics era. In the ten years that followed graphene rediscovery, dated 2004, enormous progresses have been done in the field of graphene electronics. Single transistors and more complex circuits performing analog and digital functions have been demonstrated. However, together with progresses, the physical limitations of graphene became more apparent and the bright future seems far to come.

This work represents a contribution to the research on graphene devices for high-frequency applications. Introducing an ultra-thin, high-$\varkappa$ oxide in the fabrication process, exfoliated-graphene FETs with exceptionally good performances have been demonstrated. Based on the GFETs, more complex devices were demonstrated, such as the first graphene inverter that exhibits significant voltage gain in ambient conditions. The great improvements in graphene CVD-growth have made it possible to implement this scalable material in the fabrication process, opening up new perspectives for industrial applications. With CVD-graphene, the control over size and shape permitted to obtain channels with homogeneus characteristics, leading to a great performance improvement, and inverters exhibiting DC and AC voltage gain above 20 dB were demonstrated. These high-gain devices could be cascaded to perform multiple logic operations. Demonstration of device cascading led to the fabrication of the first graphene integrated ROs, with highest oscillation frequency of 4.3 GHz with 0.9 µm gate length, surpassing silicon ROs speed at the same gate length. To improve the performance of these circuits, a sistematic study on the scaling of intrinsic parameters of GFETs has been done through S-parameters measurements. A small-signal model of the GFETs have been tested and used to extract the intrinsic parameters. GFETs with exceptionally good saturation have been fabricated, exhibiting highest f_{T} of about 10 GHz, f_{max} of 21 GHz and intrinsic AC gain above 30 dB at 10 MHz for devices with 1 µm gate length, this being the highest value reported in literature. This research reveals that the main limiting factors affecting device performances are the large contact resistance, the poor interface quality between graphene and top oxide and the large sensitivity of graphene to environment, that should be addressed to achieve a real breaktrough.

Chapter 1

Introduction and motivation

In the last decade graphene has been addressed by the scientific community as the material of wonders, capable of replacing silicon in the next generation of electronics. This great excitement have mostly been raised by graphene exceptional mobility, higher than 100,000 $cm^2V^{-1}s^{-1}$at room temperature [1], which is almost equal between holes and electrons [2, 3]. The absence of a bandgap in graphene results in bipolar conduction, namely the possibility to switch continuosly between electrons and holes [2, 4], a peculiarity that can ease the circuit complexity and could represent an advantage for graphene with respect to conventional semiconductors which require extrinsic doping to modify the type of conduction [5]. However, despite the huge research efforts, there are no graphene-based electronic devices yet available on the market. The lack of a bandgap prevents graphene-based transistors to be turned off, with consecutively low on-off ratios and high static power consumption representing huge obstacles for the development of graphene-based devices for logic applications [6]. In the field of high-frequency analog electronics, however, the situation is different since the complete switching-off of transistors is not required, thus making graphene an attractive option thanks to its ultra-high mobility (even though not fully preserved in top-gated devices [7]]) that could allow to access the terahertz operation. In the following introduction I will try to review the main characteristics that led to the enourmous popularity of graphene.

1.1 Beyond Moore's law

Since the invention of Si MOSFET in 1960, the semiconductor electronics has experienced a constant progress. Following the Moore's Law, the MOSFET integration density in ICs has increased by a factor of almost 1.4 per year, with the advantage of reduced fabrication costs and increased speed of operation [8]. This miniaturization has been accomplished through an aggressive scaling of transistor dimensions, but nowadays this trend is approaching its technological limits. Today Si MOSFETs with 20-nm gate length [1] are in mass production and for 2020 the ITRS roadmap requires to reach a 10-nm node [9]. At this scale length

[1] Physical gate length for 20-nm node is about 30 nm.

the MOSFET operation is degraded by the increasing influence of short channel effects [10]. When the gate length L is scaled down, one of the main issues that has to be faced is the reduction of gate control on the drain current. Moreover, when source and drain are brought in too close proximity, a diffusion leakage current flows through the bulk to the surface, significantly changing device characteristics. The easiest approach to counteract short channel effects consists in a simultaneous reduction of all the characteristic dimensions of the device. Thus, a shorter gate length should be accompanied by a reduction of the source and drain dimensions, with a simultaneous increase in their doping concentration to keep the channel access resistance as low as possible. However, this task is difficult to accomplish since it requires a control at the atomic scale that is highly demanding from a technological point of view, since even few atoms can make a difference in the doping profile, leading to unavoidable device-to-device fluctuations [10].

One of the crucial parameters involved in the scaling process is the reduction of gate oxide thickness. In order to preserve a good gate control, the SiO_2 thickness in past nanoMOSFETs has been reduced to few atomic layers, demanding a strict control of homogeneity over millions of devices to avoid hot spots and ensure standard performances. Since a further gate scaling would be physically limited by the tunnelling current, a higher dielectric constant should be preferred to a reduced oxide thickness to provide increased gate capacitance. In this perspective there is an ongoing research focused on high-$\varkappa$ oxides like ZrO_2 or HfO_2 [11] and a new parameter has been introduced to define vertical scaling: the equivalent oxide thickness $EOT = t_{ox}\varepsilon_{SiO_2}/\varepsilon_{ox}$, namely the oxide thickness that a generic gate stack with a certain capacitance would exhibit if it were made of SiO_2. Despite the benefits that this change seems to promise, the introduction of new types of dielectrics faces some technological challenges, e.g. the presence of defective interfaces and dopants diffusion that can severely degrade mobility and affect device performances [12, 13, 14].

While both oxide thickness and channel doping scaling were approaching physical limits, increasing efforts have been directed to the development of new device architectures. The introduction of SOI substrates has opened the way to multi-gate architectures and is at the basis of FinFET technology. In FinFETs the channel is embedded in a thin silicon fin that constitutes the body of the device, and is surrounded on three sides by the gate. With this approach the thickness of the channel can be reduced to $< 1/4$ of the channel length [15], resulting in an improved gate control that led to the recent commercial push to Si FinFETs at the 22 nm node [16, 17]. However, all these technological improvements represent just temporary solutions, while the continuous development of RF electronics requires new materials with higher mobility than Si for faster operations.

The HEMT technology cannot be considered strictly "new" since the first HEMTs have been described in 1980 [18]. In these structures, based on III-V semiconductors, a quantum well confines the carriers, separating them from the ionized donor atoms to prevent scattering, thereby leading to high intrinsic mobility, tipically about 10^4 $cm^2V^{-1}s^{-1}$ for InP and GaAs HEMTs at room tmperature [19, 18]. Among the variety of systems belonging to this category, the most notable are InAlAs/InGaAs HEMTs on InP and InAlAs/InGaAs

metamorphically grown on GaAs, showing extremely high frequency capability and low-noise operation for low power applications, while AlGaN/GaN HEMTs, having a larger bandgap, offer unique solution for high voltage and power applications [19]. However the HEMT technology is limited to RF applications and seems not suitable for mainstream highly integrated electronics, due to the high-costs and the technological difficulties related to the fabrication process.

Against this background it should not surprise that the isolation of graphene in 2004 [2], with the cheap and perhaps naïve technique of scotch tape exfoliation, raised a great excitement in the electronics community. Thanks to its intrinsic 2-D nature, graphene allows to reduce the channel dimension to a greater extent, with a strong improvement of vertical scaling. Its high mobility makes it a good candidate for RF applications. The ambipolar transport allows the fabrication of electron and hole-type FETs without the need of extrinsic doping. Moreover, the hole and electron mobilities in graphene are almost equal, while in Si the ratio $\mu_{\mathrm{p}}/\mu_{\mathrm{n}}$ is around 0.3, 0.05 in GaAs, and approaches 0.01 in the narrow bandgap compounds InAs and InSb. Therefore, high hole-mobility devices represent a challenge for conventional semiconductor industry [18]. However, the lack of a band gap in graphene represents a serious problem that limits the applications of this material, and demystification is needed to discern between realistic applications and speculations. Nowadays it is commonly accepted opinion that graphene cannot compete with III-V materials in terms of speed and power consumption, but it retains promising perspectives in the flexible electronics arena, where its flexibility and transparency, together with high mobility, can offer great advantages over the conventional organic electronics [20, 21].

This PhD work has been devoted to the fabrication and characterization of graphene FETs and more complex graphene ICs. The realization of the first graphene audio voltage amplifier showing a real voltage gain in ambient conditions [22] has set the basis for further developments, such as the demonstration of device cascading [23], and the fabrication of the first integrated graphene ring oscillators, operating in the gigahertz range [24]. The influence of parasitic resistances and capacitances on the overall device performance have been investigated. A study upon device scaling has allowed to identify the main limitations related to the current graphene technology that should be addressed to guarantee further developments.

Chapter 2

Graphene electronic properties

This chapter is devoted to the description of graphene properties that are relevant for electronic applications. Beginning with the derivation of graphene band structure it is possible to derive all its fundamental properties. The origins of high mobility and ambipolarity, introduced in chapter 1, will be discussed in details.

2.1 Band structure

All physical properties of materials can be directly inferred from their band structure. Graphene is a two-dimensional sheet of carbon atoms arranged in a hexagonal lattice.

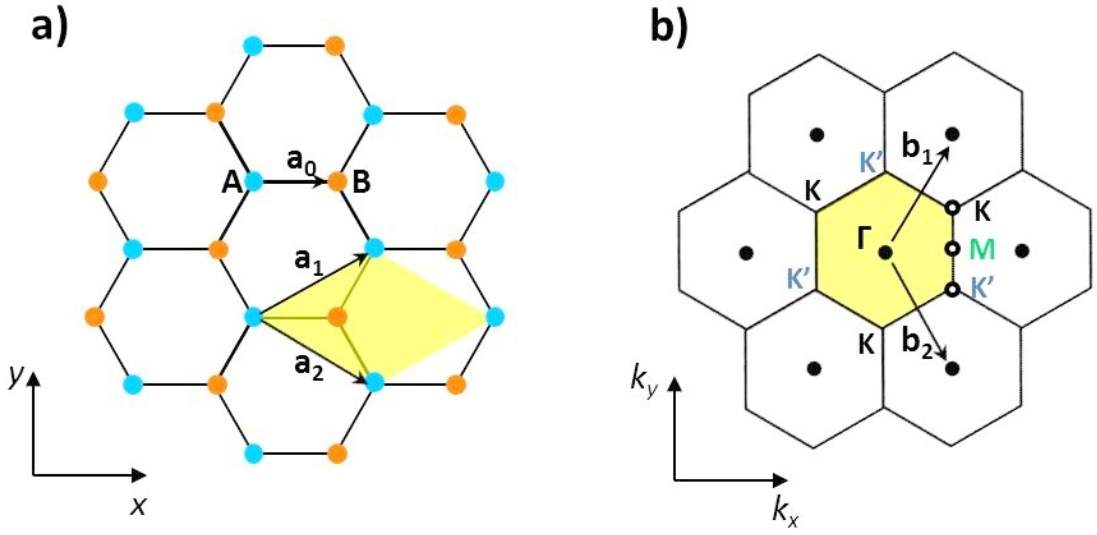

Figure 2.1: a) Lattice of graphene in real space with atomic positions A and B and lattice vectors $\mathbf{a}_1$ and $\mathbf{a}_2$ forming the primitive unit cell (shaded); b) first Brillouin zone (shaded) with reciprocal lattice vectors $\mathbf{b_1}$ and $\mathbf{b_2}$ and high symmetry points K, K', Γ and M.

The lattice structure of graphene contains two carbon atoms per unit cell which form

two sublattices. Each Bravais lattice is given by the basis vectors connecting the next to nearest neighbors: $\mathbf{a}_1 = \mathbf{a}_0\left(\sqrt{3}/2; 1/2\right)$and $\mathbf{a}_2 = \mathbf{a}_0\left(\sqrt{3}/2; -1/2\right)$ where $\mathbf{a_0}$=1.42 Å is the carbon-carbon distance in graphene (figure 2.1a). Any physical property of the lattice $f(\mathbf{r})$ will inherit its periodicity, which means that $f(\mathbf{r})$ is invariant under translation along the primitive lattice vectors: $f(\mathbf{r}) = f(\mathbf{r}+\mathbf{r_n})$, where the translation vector $\mathbf{R}$ is the integer sum of the primitive lattice vectors: $\mathbf{R} = \sum_n m\mathbf{a}_n$, with m integer.

The vectors $\mathbf{b_1}$ and $\mathbf{b_2}$ (figure 2.1b) are known as the reciprocal lattice vectors. Their magnitudes have units of inverse length and their direction is perpendicular to the crystal planes defined by the primitive lattice vectors. As the primitive lattice vectors define the lattice in direct space in terms of the distances between atoms, the reciprocal lattice vectors define a reciprocal lattice in terms of the spacing of crystal planes in the momentum space (k-space). The reciprocal lattice is also invariant under translation such that for any physical property in k-space $g(\mathbf{k})$, $g(\mathbf{k}) = g(\mathbf{k}+\mathbf{G})$ where the translation vector $\mathbf{G}$ is the integer sum of the reciprocal lattice vectors.

The band structure of graphene can be derived with the aid of Bloch theorem, used to describe the motion of particles subjected to the periodic potential of a crystal lattice. Since the length scales of periodicity in crystals are on the order of Angstroms, a quantum mechanical approach is needed to describe the motion of electrons. The time-independent Schrödinger equation that expresses the classical energy conservation in a quantum mechanical context takes the following form:

$$\mathcal{H}\Psi(\mathbf{r}) = \left[\frac{p^2}{2m} + V(\mathbf{r})\right]\Psi(\mathbf{r}) = E\Psi(\mathbf{r})$$

where $p = -i\hbar\nabla$ is the quantum momentum operator, and $\Psi(\mathbf{r})$ is the eigenfunction of an electron.

The solutions of the Schrödinger equation for a free electron are plane waves. When electrons move in a periodic potential the plane wave solutions are subjected to the periodicity of that potential. This can be translated in the periodicity of wave functions describing the density of probability to find an electron in the periodic environment.

In the graphene lattice each carbon atom has 4 electrons available, one in the s orbital an the other three in p_x, p_y and p_z orbitals. For simmetry reasons the p_z orbital is orthogonal to the others, meaning that their wavefunctions cannot overlap (i.e., an electron that has a certain probability to lie in an s orbital has a zero probability to be found in a p_z orbital). Therefore the p_z electrons forming the π-bonds can be treated independently from the other valence electrons, and each carbon atom can be modeled just as a single p_z orbital centered in the atomic position $\mathbf{r_n}$. According to this description the wave functions $\Psi(\mathbf{k}, \mathbf{r})$ can be expressed as a linear combination of atomic wave functions on each sublattice within the LCAO formalism [25]:

$$\Psi(\mathbf{k}, \mathbf{r}) = c_A(\mathbf{k})\Phi_A(\mathbf{k}, \mathbf{r}) + c_B(\mathbf{k})\Phi_B(\mathbf{k}, \mathbf{r}) \tag{2.1}$$

with

$$\Phi(\mathbf{k},\mathbf{r}) = \frac{1}{\sqrt{N}} \sum_n \mathrm{e}^{i\mathbf{k}\cdot\mathbf{r}_n} p_{z,\mathrm{A}}(\mathbf{r}-\mathbf{r}_n) \tag{2.2}$$

representing the periodicity of sublattice n (either A or B), where N is the number of unit cells in the sublattice and $\mathbf{r_n}$ is a lattice point. Schrödinger equation, $\mathcal{H}\Psi(\mathbf{k},\mathbf{r}) = E(k)\Psi(\mathbf{k},\mathbf{r})$, can be written as:

$$\begin{bmatrix} \mathcal{H}_{\mathrm{AA}} & \mathcal{H}_{\mathrm{AB}} \\ \mathcal{H}_{\mathrm{BA}} & \mathcal{H}_{\mathrm{BB}} \end{bmatrix} \begin{bmatrix} c_{\mathrm{A}}(\mathbf{k}) \\ c_{\mathrm{B}}(\mathbf{k}) \end{bmatrix} = E(\mathbf{k}) \begin{bmatrix} c_{\mathrm{A}}(\mathbf{k}) \\ c_{\mathrm{B}}(\mathbf{k}) \end{bmatrix} \tag{2.3}$$

where

$$\mathcal{H}_{\mathrm{AA}} = \langle \Phi_{\mathrm{A},m}(\mathbf{k}) | \, \mathcal{H} \, | \Phi_{\mathrm{A},n}(\mathbf{k}) \rangle = \int \Phi^*_{\mathrm{A},m}(\mathbf{k}) \mathcal{H} \Phi_{\mathrm{A},n}(\mathbf{k}) d\mathbf{r} = \frac{1}{N} \sum_{m,n} \mathrm{e}^{i\mathbf{k}\cdot(\mathbf{r}_n - \mathbf{r}_m)} \langle p_{z,\mathrm{A},m} | \mathcal{H} | \, p_{z,\mathrm{A},n} \rangle$$

$$\mathcal{H}_{\mathrm{AB}} = \langle \Phi_{\mathrm{A},m}(\mathbf{k}) | \, \mathcal{H} \, | \Phi_{\mathrm{B},n}(\mathbf{k}) \rangle = \int \Phi^*_{\mathrm{A},m}(\mathbf{k}) \mathcal{H} \Phi_{\mathrm{B},n}(\mathbf{k}) d\mathbf{r} = \frac{1}{N} \sum_{m,n} \mathrm{e}^{i\mathbf{k}\cdot(\mathbf{r}_n - \mathbf{r}_m)} \langle p_{z,\mathrm{A},m} | \mathcal{H} | \, p_{z,\mathrm{B},n} \rangle$$

with $\mathcal{H}_{\mathrm{AA}} = \mathcal{H}_{\mathrm{BB}}$ representing the onsite energies and $\mathcal{H}_{\mathrm{BA}} = \mathcal{H}^*_{\mathrm{AB}}$ representing the hopping energies.

An explicit calculation of $\mathcal{H}_{\mathrm{AB}}$ by restricting the sum over the first nearest-neighbors gives:

$$\mathcal{H}_{\mathrm{AB}} = \frac{1}{N} \left(1 + \mathrm{e}^{\mathbf{i}\mathbf{k}\cdot\mathbf{a}_1} \langle \mathrm{p_{z,A,0}} | \mathcal{H} | \, \mathrm{p_{z,B,a_1}} \rangle + \mathrm{e}^{i\mathbf{k}\cdot\mathbf{a}_2} \langle p_{z,A,0} | \mathcal{H} | \, p_{z,B,a_2} \rangle \right) = \gamma_0 \alpha(\mathbf{k})$$

where γ_0 is the transfer integral between the first neighbor orbitals, with typical values comprised between -2.9 and -3.1 eV [26].

Setting the reference value for energy, $\mathcal{H}_{\mathrm{AA}} = 0$, the Hamiltonian becomes:

$$\mathcal{H}(\mathbf{k}) = \begin{bmatrix} 0 & \gamma_0\alpha(\mathbf{k}) \\ \gamma_0\alpha(\mathbf{k})* & 0 \end{bmatrix}$$

Solving the secular equation $|\mathcal{H} - IE(\mathbf{k})| = 0$, gives the energy dispersion relation [25]:

$$E(\mathbf{k}) = \pm |\gamma_0 \alpha(\mathbf{k})| = \pm\gamma_0 \sqrt{3 + 2\cos(\mathbf{k}\cdot\mathbf{a_1}) + 2\cos(\mathbf{k}\cdot\mathbf{a_2}) + 2\cos(\mathbf{k}\cdot(\mathbf{a_2}-\mathbf{a_1}))} = \tag{2.4}$$

$$= \pm\gamma_0 \sqrt{3 + 4\cos\left(\frac{\sqrt{3}}{2}\mathrm{a}_0 k_x\right)\cos\left(\frac{\mathrm{a}_0 k_y}{2}\right) + 2\cos(\mathrm{a}_0 k_y)}$$

where the plus sign is associated with the conduction band and the minus sign with the valence band. Since there are two π-electrons in the unit cell the valence band is fully occupied, while the conduction band is empty. The two bands touch at the K and K' points, where the energy goes to zero, so the Fermi level E_{F} is the zero-energy reference

and the Fermi surface contains all the K and K' discrete points.

Now consider the condition for elastic reflection of waves from a periodic structure. According to Bragg's law the reflection from a periodic structure only occurs when the incident wave $\mathbf{k}$ and reflected wave $\mathbf{k}$' interfere constructively, a condition fulfilled when the difference between the incident and reflected waves is equal to a reciprocal lattice vector $\mathbf{G}$: $\Delta\mathbf{k} = \mathbf{k}-\mathbf{k}' = \mathbf{G}$. Furthermore, an elastic scattering event requires that the direction of the momentum is changed, while the magnitude remains constant: $|\mathbf{k}| = |\mathbf{k}'|$.

From these two conditions the expression of elastic reflection of a wave from a periodic structure can be derived as [27]:

$$\mathbf{k} \cdot \mathbf{G} = \frac{1}{2}|\mathrm{G}|^2$$

The scattering condition enlights a fundamental difference between the points labeled K and K'. The points labeled by K are considered to be equivalent since they can be reached by a translation via reciprocal lattice vector. Therefore any physical property of the lattice will be equivalent at the K points. However, one cannot translate from K to K' via a reciprocal lattice vector, and therefore these points are inequivalent giving rise to the possibility of different physics at K and K'. This difference between the points K and K' will ultimately build a degeneracy into the band structure of graphene, known as valley isospin. Furthermore, it is important to remember that an electron can live in two spin states giving rise to an additional twofold spin degeneracy.

The plot of E($\mathbf{k}$) is by definition, the band structure. The band structure around the special points in the Brillouin zone K and K' is approximately conical (see figure 2.2).

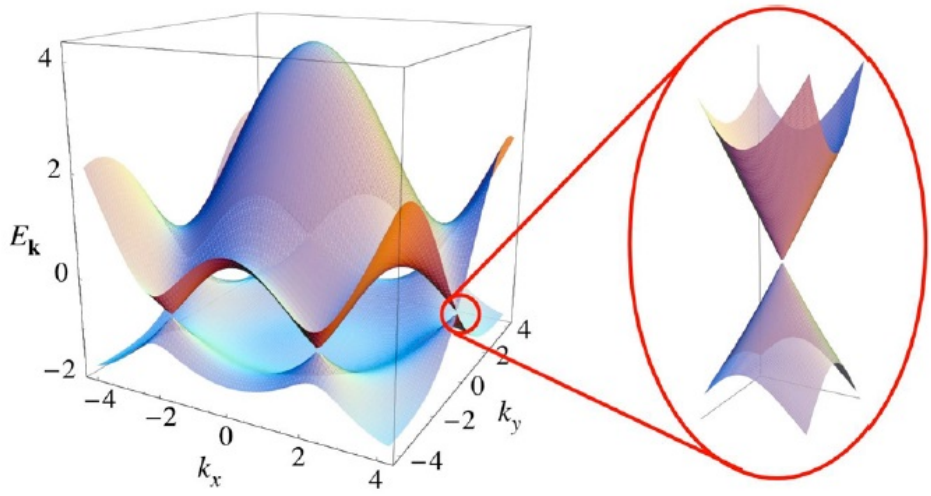

Figure 2.2: Energy band diagram derived trough a tight binding approximation, inset shows the energy dispersion close to the Dirac point [26].

A linearization around a(K+$\delta\mathbf{k}$) (see 3.9) gives the behavior of the band structure near

the Dirac points.

$$E_{\pm}(\delta\mathbf{k}) = \pm\frac{3\gamma_0 a_0}{2}\,|\delta\mathbf{k}| = \pm v_{\mathrm{F}}\hbar\,|\delta\mathbf{k}| = \pm v_{\mathrm{F}}\,|\mathbf{p}| \tag{2.5}$$

Here v_{F} is the Fermi velocity which has a value of approximately 10^8cm/s [3, 26].

In even the most heavily doped graphene the highest electron energies are tipically less than 300 meV. Since the Dirac cones have an extent of ± 1 eV around the Fermi level [26], electrons in graphene occupy the Dirac cones at equilibrium [28]. The low-energy physiscs just introduced becomes important in all calculations regarding electronic properties at equilibrium or near equilibrium.

The density of states per energy is related to the density of states in k-space by the expression: $\rho(E) = \rho(k)dk/dE$. Taking the linear expression for energy close to the Dirac point results in [29]:

$$\rho(E) = \frac{2\,|E|}{\pi(\hbar v_{\mathrm{F}})^2} \tag{2.6}$$

According to (2.6) close to the Dirac point, where E=0, the DOS goes to zero. This unique linear dependence, a direct consequence of graphene linear spectrum, differs from conventional semiconductors, where $\rho(E) \propto \sqrt{E}$, and also from 2-D electron gas, where DOS is constant with energy [27].

2.2 Massless Dirac fermions and electron-hole simmetry

The motion of charged carrier in the crystal lattice is usually described by the effective mass tensor, defined as [27]:

$$(m_{ij}*)^{-1} = \frac{1}{\hbar^2}\frac{\partial^2 E(\mathbf{k})}{\partial k_i \partial k_j}$$

Since for graphene the first derivative of energy with respect of momentum is a discontinuos function, this expression turns out to be meaningless. Instead, a relativistic approach is needed to relate mass and energy of the particles. The relativistic expression for energy is:

$$E = \sqrt{m_0^2 c^4 + c^2 p^2} \tag{2.7}$$

with $m_0$being the rest mass of the particle. To obtain expression (3.2) from (2.7), with Fermi velocity taking the place of speed of light in graphene lattice, the rest mass should be set to zero at K and K' points. It is for this reason that electrons near the K and K' points are termed massless Dirac fermions and the K and K' points themselves are known as Dirac Points.

As discussed above, in the proximity of Dirac points the energy-momentum relation is linear. An alternative way to write the linear Hamiltonian around K points involves the use of Pauli matrices:

$$\mathcal{H}_K = v_{\mathrm{F}}\hat{\sigma}\cdot\mathbf{p} \tag{2.8}$$

with $\hat{\sigma} = (\sigma_x, \sigma_y, \sigma_z)$, where

$$\sigma_x = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}, \quad \sigma_y = \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix}, \quad \sigma_z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}$$

are the Pauli matrices.

For the inequivalent K' point, the Hamiltonian is the transposed of (2.8) :$\mathcal{H}_{K'} = \mathcal{H}_K^t$. Equation (2.8) has the same form of a Dirac equation with rest mass of the particle equal to zero and electron Fermi velocity v_{F} which is almost 300 times smaller than the speed of light. These Pauli matrices do not operate on the spin, but on the sublattice degree of freedom, that takes the name of pseudospin. The Hamiltonian is proportional to the helicity operator, namely the projection of the pseudospin on the momentum direction, defined as $\hat{h} = \hat{\sigma} \cdot \frac{\mathbf{p}}{|\mathbf{p}|}$. This quantity can be either positive or negative, stating that pseudospin and momentum are parallel or antiparallel one to each other (see figure 2.3). Since the Hamiltonian is proportional to $\hat{\sigma}^t$ at the point K' , the helicity is inverted when passing from K to K'. We can write once more the Hamiltonian of equation (2.8) as:

$$\mathcal{H}_\xi = v_{\mathrm{F}} |\mathbf{p}| \begin{pmatrix} 0 & \mathrm{e}^{i\xi\theta} \\ \mathrm{e}^{-i\xi\theta} & 0 \end{pmatrix} \tag{2.9}$$

where $\mathbf{p} = |\mathbf{p}| \, \mathrm{e}^{i\theta}$, $\theta = \arctan(p_x/p_y)$ and ξ=1 (point K) or -1 (point K'). The eigenstates of (2.9) can be written as:

$$|\Psi_{\xi,s}\rangle = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 \\ s\mathrm{e}^{+i\xi\theta} \end{pmatrix}$$

where $s = \pm 1$ is the band index (plus sign stands for conduction, minus for valence band), and ξ is the valley index which indicates the sublattices located in K and K' [25].

Around the K point the pseudospin is parallel to the momentum in the conduction band and antiparallel in the valence band. In the K' point the situation is reversed. This peculiarity has serious consequences on the transport properties of graphene. In the absence of pseudospin-flip processes (for which we need to take into account perturbation theory), an electron moving to the right can be scattered only to a right-moving electron state or left-moving hole state, in other words backscattering is strictly forbidden due to the pseudospin conservation.

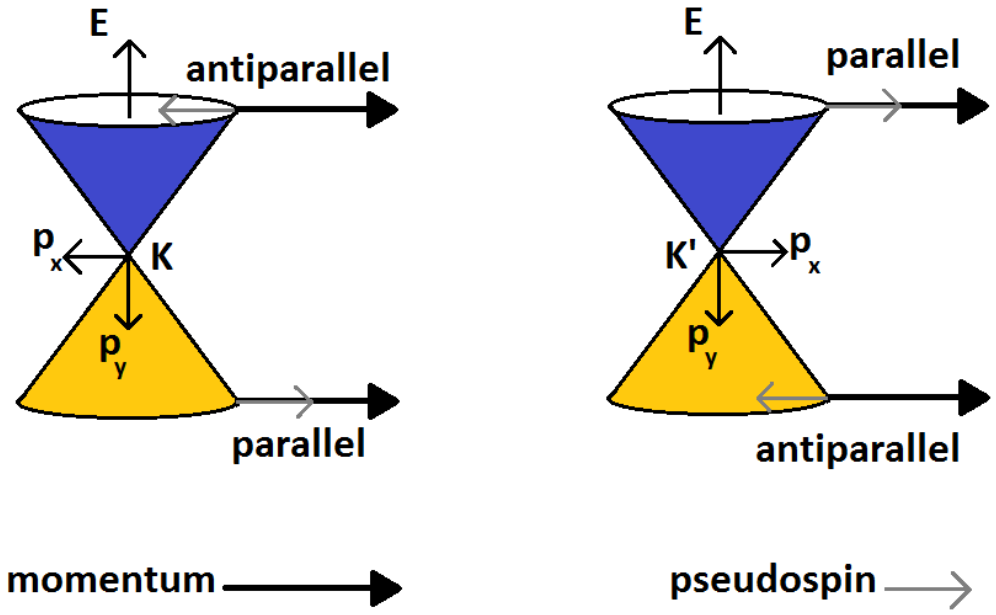

Figure 2.3: Momentum and pseudospin direction in the valence and conduction band at points K nd K' in the first Brillouin zone.

This peculiarity leads to an interesting relativistic process, named Klein paradox, in which a potential barrier exceeding the electron's rest energy becomes transparent to electron penetration. In such a case, the transmission probability, T, depends only weakly on the barrier height, with very high barriers approaching the perfect transparency. For single-layer graphene, an electron wavefunction at the barrier interface perfectly matches the corresponding wavefunction for a hole with the same direction of pseudospin, yielding T =1 [30]. This anomalous tunnelling is expected to play an important role in the transport properties, in particular for low carrier concentration regime, where disorder induces significant potential barriers and the systems are likely to break up into a random distribution of p-n junctions [31]. In conventional 2-D systems, strong enough disorder causes electronic states to be separated by potential barriers with exponentially small transparency, leading to the Anderson localization [32]. In contrast, in graphene all potential barriers are relatively transparent, preventing charge carrier confinement. Therefore, the so-called different electron and hole "puddles" induced by disorder are not isolated but percolate, therefore suppressing localization [33].

2.3 Carrier density and quantum capacitance

Carrier density n is defined as the number of charge carriers available in a certain volume (or surface in case of graphene) of material and as such it depends on the position of the Fermi level inside the band structure, related to the DOS through the Fermi-Dirac distribution f(E):

$$n = \int_{E_0}^{\infty} \rho(E) f(E) dE \tag{2.10}$$

Several experiments [34, 35], have demonstrated that the actual carrier density differs from that predicted by theory for Fermi energies close to the Dirac point. The minimum carrier density of an ideal graphene layer should come from the thermally generated carriers, $n_{\mathrm{th}} = (\pi/6)(k_{\mathrm{B}}T/\hbar v_{\mathrm{F}})^2 \approx 8 \cdot 10^{10} cm^{-2}$ at $T = 300$ K [36]. However, in any real 2-D graphene sample extrinsic random-charged impurity centers are invariably present causing the nonideal system to break up into spatially inhomogeneous conductive 2-D electron and hole puddles [31], i.e., regions with a Fermi level above (electron) or below (hole) the Dirac point. These electron and hole puddles lead to a minimum residual carrier density that can be expressed as [36]:

$$n_0 = \sqrt{\left(\frac{n^*}{2}\right)^2 + n_{\mathrm{th}}^2}$$

where $n^*$is the residual carrier puddle density that induce a surface potential distribution in the graphene sheet.

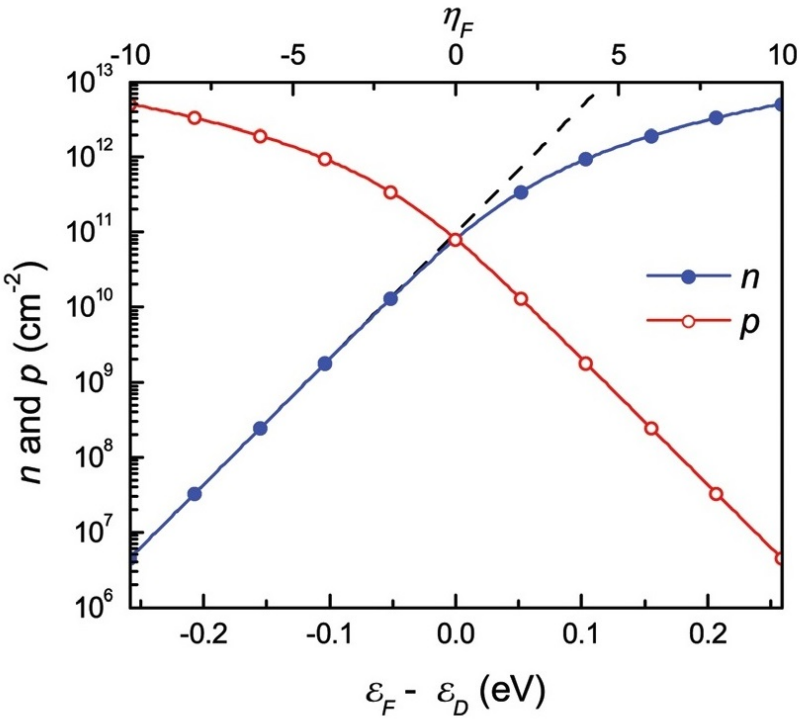

Figure 2.4: Electron (n) and hole (p) carrier densities as a function of the Fermi level position relative to the dirac point ϵ_{F}-ϵ_{D}. From reference [4].

Typical values of n_0 are 10^{11}-10^{12}cm^{-2} for graphene on SiO_2 substrate [37] and 10^{13}cm^{-2}

for epitaxial graphene on SiC [38], comparable with the sheet carrier density of Si MOSFET and HEMT channels [21].

The charge density of graphene can be modulated through electrostatic doping by placing an oxide/metal gate stack on top of it, to build a parallel plate capacitor (see section 3.1). This kind of structure resembles a MOS-C and is of fundamental importance because it constitutes the basics of any graphene field-effect device. The capacitance of the metal-oxide-graphene system cannot be simply calculated as the oxide capacitance itself, namely $C_G \neq C_{\rm ox} = \varepsilon_0 \varepsilon_{ox} A/t_{\rm ox}$, where $\varepsilon_{\rm ox}$ and $t_{\rm ox}$are the dielectric constant and thichkness of the oxide layer and A is the gate area. Since graphene is a 2-D system, the effect of quantization in the vertical direction (out of plane) plays an important role in determining its physical behavior, thus a correct estimation of the capacitance should take into account the quantum capacitance of graphene, $C_Q = e^2\rho(E)$, that can be regarded as the additional energy cost of inducing carriers in the limited-DOS material. An explicit form derived on the basics of a 2-D, free-electron gas model and taking into account the residual carrier density gives for the quantum capacitance [35]:

$$C_Q = \frac{2e^2}{\hbar v_{\rm F}\sqrt{\pi}}\sqrt{|n_{\rm G}| + |n^*|} \tag{2.11}$$

where

$$n_{\rm G} = \left(\frac{eV_{\rm ch}}{\hbar v_{\rm F}\sqrt{\pi}}\right)^2$$

is the gate-induced carrier concentration in the channel depending on the channel potential $V_{\rm ch}$. Expression (2.11) gives values that are in good agreement with measurements, and that are usually much larger than the predicted value for minimum quantum capacitance of $C_{\rm q,min} \approx 0.8$ μF/cm^2, attributed to thermal induced carriers [35].

The total capacitance of the metal-oxide-graphene system results from the series connection of the oxide capacitance and the quantum capacitance of graphene, with the smaller of the two dominating the other. Thus, when studying graphene-oxide-metal systems with a large oxide capacitance (provided by thin, high-κ dielectrics), it should be taken into account that the total capacitance can be significantly lower than what would be expected for a MOS-C equivalent structure.

2.4 Transport properties

Mobility is the fundamental transport property that describes the motion of carriers subjected to an external electric field, from which conductivity (or sheet resistance) and carrier density can be derived as [27]:

$$\sigma = \frac{1}{R_{\rm sh}} = ne\mu$$

Within the Boltzmann theory, valid for carrier density much larger than scattering-center density (i.e., for energy far from the Dirac point) the mobility can be expressed as:

$$\mu = \frac{e v_{\mathrm{F}}^2 \langle \tau \rangle}{E_{\mathrm{F}}}$$

where $\langle \tau \rangle$ is the energy-averaged finite-temperature scattering time that sums up all contributions arising from different scattering sources. In pristine free-standing graphene at very low temperatures the mobility can take extremely high values, up to 100,000 $\mathrm{cm^2V^{-1}s^{-1}}$, because the carriers can only scatter with lattice acoustic phonons due to the absence of backscattering [1]. However, when graphene is transferred on a dielectric substrate and/or covered with a gate dielectric, mobility drops dramatically. The dielectric surface introduces several additional sources of scattering, like lattice defects, charged impurities located at the interfaces and surface optical phonons of the lattice that couple to the external electric field. At low temperatures the main scattering contribution comes from acoustic phonons and charged impurities (so-called Coulomb scattering). The mobility limited by acoustic phonon scattering is found to be inversely proportional to the carrier density, because a larger number of carriers leads to a larger number of collisions. The mobility limited by Coulomb scattering does not depend on the carrier density, but just on the density of scattering centers [39]. At room temperature the carriers acquire enough kinetic energy to scatter with surface and substrate optical phonons [34, 40]. The optical-phonon scattering limited mobility has found to decrease monotonically as $\mu \propto 1/\sqrt{n}$ [41]. Moreover, the activation of this phonon scattering mechanism leads to a degradation of mobility with increasing temperature [39]. It should be mentioned that the substrate plays an important role on the extent of mobility damping. It has been demonstrated that high-$\varkappa$ dielectric substrates such ZrO_2 and HfO_2 improve the mobility at low temperature by screening the charged impurities, but this effect is washed out at higher temperatures by the increased rate of optical phonon scattering compared to SiO_2 substrate [41]. In this perspective, the ideal dielectric material should possess both high static dielectric constant (to screen charged-impurities) and high-energy phonons that are not activated in low-field transport.

Another important transport property, that defines the ultimate speed of any electronic device, is the carrier's drift velocity v_{drift}. At low fields the velocity-field dependence is linear, with $v_{\mathrm{drift}} = \mu E$ [5]. At high fields the drift velocity tends to saturate, limited by the scattering of carriers with the optical phonons, which is modeled by [42]:

$$v_{\mathrm{drift}} = \frac{\mu E}{1 + \mu E / v_{\mathrm{sat}}} \tag{2.12}$$

The saturation velocity v_{sat} at low temperatures and low carrier densities is a constant, $v_{\mathrm{sat,low}} = (2/\pi) v_{\mathrm{F}}$, while at higher carrier density it scales as $v_{\mathrm{sat}} = \frac{2}{\pi} v_{\mathrm{F}} \hbar\Omega / E_{\mathrm{F}} = 2\Omega/\sqrt{\pi^3 n}$, where $\hbar\Omega$ is the energy of graphene optical phonons [36]. On SiO_2 substrate the saturation velocity is degraded because the dominant scattering mechanism is related to substrate low-energy phonons ($\hbar\Omega = 55$ meV) rather than graphene zone-edge phonons ($\hbar\Omega = 160$

meV). Thus, in order to achieve a high saturation velocity, a condition that is necessary for high-speed devices, substrates with higher phonon energies are required. Moreover, high-field saturation velocity can only occur in highly-ordered samples showing little defects and impurities concentration so that the elastic scattering events are minimized and optical phonon scattering prevails. If this condition is not satisfied the drain current continues to increase monothonically with the drain bias [43].

It is worth to point out that electronic devices are far from being ideal systems. As already mentioned, the extremely high mobility of suspended graphene cannot be achieved in real devices, since the unavoidable presence of a substrate introduces several scattering sources. High intrinsic mobility (after extraction of contact resistance) up to 24,000 $cm^2V^{-1}s^{-1}$has been demonstrated for exfoliated-graphene top gated devices and CVD-graphene buried gated GFETs [44, 7], still far from the record values for suspended graphene. However a lot of research efforts have been done to face this issue, and depositing graphene on h-BN has shown promising results. The h-BN can be used both as a substrate and as a gate dielectric, completely embedding the graphene channel. This approach has proved to be effective in reducing the roughness of graphene sheets, while the high dielectric constant improves the screening of charge impurities. The result is graphene exhibiting low doping, low hysteresis and high mobility up to 40,000 $cm^2V^{-1}s^{-1}$ for bilayer graphene devices on h-BN at room temperature and 100,000 $cm^2V^{-1}s^{-1}$ in top gated devices embedded in h-BN at 1.6 K [45, 46]. However, this technique is not yet mature to deliver the longed-for technological breakthrough. The main drawback is represented by the lack of scalability, since high-quality BN is obtained through exfoliation [1], h-BN crystals are quite expensive and the device processing requires several transfer steps that introduce contaminations and lead to a random device-to-device variation. For these reasons, despite the possible improvements, the use of h-BN has not been considered in this thesis.

[1] Although h-BN can be growth with CVD on Cu, similarly to graphene, the quality is lower compared to exfolited material. [47]

Chapter 3

GFETs and voltage amplifiers

This chapter is a review of GFETs characteristics. The influence of graphene physical properties on devices operation will be discussed and compared to standard Si MOSFETs. The possibility to achieve good performance by careful parameter-design tuning will be investigated.

The chapter is organized as follows: first a brief introduction to Si MOSFETs will be given, to enlight the main differences between semiconductor-based and graphene-based devices. Then, some important small-signal FOMs, like transconductance and output resistance, will be introduced and their dependence on material properties will be discussed. The last section will be devoted to graphene-based inverters, covering theory of operation, device fabrication and characterization.

3.1 The basic unit: GFET

The MOSFET is the most commonly used Si-based device. It comprises a conductive channel connected to three terminals: the source from which carriers are injected in the channel, the drain from which carriers leave the channel and the gate that modulates the channel doping through capacitive coupling [48]. Different techniques, such as ion implantation, are used to introduce dopants in the Si substrate to realize either p-type or n-type FETs [5]. The characteristic of PFETs and NFETs differ due to the different electron and hole mobilities in Si, related to different effective masses. In contrast, GFETs are ambipolar devices, so they exhibit both hole and electron conduction tunable through electrostatic doping [2]. Moreover the electron and hole mobilities in graphene are almost equal (deviations from this behavior will be discussed in section 4.2.2), making the transfer characteristics of GFETs symmetric.

3.1.1 Current-voltage characteristics

The analysis of the current dependence on drain-to-source and gate-to-source voltage enlights the differences between a MOSFET and a GFET.

Consider as an example a graphene sheet n-doped by external impurities, connected between two electrodes labelled as source and drain. Adding an oxide/metal stack on top of the graphene layer results in the formation of a GFET. The *I-V* and transfer characteristics of a GFET differ from that of the MOSFET. In a MOSFET the channel formation depends on the voltage applied between the gate metal and the substrate. Only if this voltage is above the treshold value V_{th} (that is constant) an inversion layer is formed and the MOSFET turns on. In a GFET the treshold voltage V_{th} has a different meaning since its value is not fixed, but is rather a function of the V_{DS}.

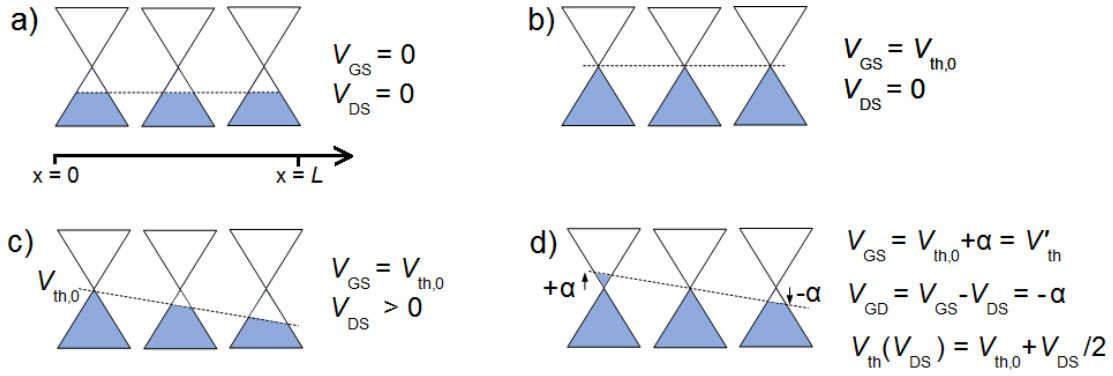

Figure 3.1: Doping profile of the GFET channel extending from source (x = 0) to drain (x = *L*). a) When no bias applied. b) Applying $V_{\mathrm{GS}} = V_{\mathrm{th},0}$ the potential of the channel reaches the value at the Dirac point. c) Applying $V_{\mathrm{DS}} > 0$ the potential at the drain increases. d) To restore the charge neutrality of the channel at fixed V_{DS}, the V_{GS} should be increased of an amount α, so that the potential $V_{\mathrm{GD}} = V_{\mathrm{GS}} - V_{\mathrm{DS}} = -\alpha$ and the Dirac point is in the middle of the channel. This condition is satisfied when $\alpha = V_{\mathrm{DS}}/2$. The new treshold voltage, $V_{\mathrm{th}} = V_{\mathrm{th},0} + \alpha$, is then a function of V_{DS} : $V_{\mathrm{th}}(V_{\mathrm{DS}}) = V_{\mathrm{th},0} + V_{\mathrm{DS}}/2$.

Figure 3.1a shows the channel potential of a GFET with no bias applied. A voltage $V_{\mathrm{GS}} = V_{\mathrm{th},0}$ should be applied between gate and source terminals (see figure 3.1b) to shift the Fermi level of graphene channel to the Dirac point. When a positive V_{DS} is applied the potential at drain side decreases (figure 3.1c) and therefore, to restore the charge neutrality of the channel, V_{GS} should be increased of an amount α, so that the potential at the drain $V_{\mathrm{GD}} = V_{\mathrm{GS}} - V_{\mathrm{DS}} = -\alpha$ and the Dirac point is in the middle of the channel (figure 3.1d). This condition is satisfied when $\alpha = V_{\mathrm{DS}}/2$, so the treshold voltage is a function of V_{DS} and can be expressed as $V_{\mathrm{th}}(V_{\mathrm{DS}}) = V_{\mathrm{th},0} + V_{\mathrm{DS}}/2$ [1]. Thus, at larger V_{DS}, larger V_{GS} are required to restore channel neutrality.

[1] This treatise is valid in the assumption that the electron and hole conduction are symmetric.

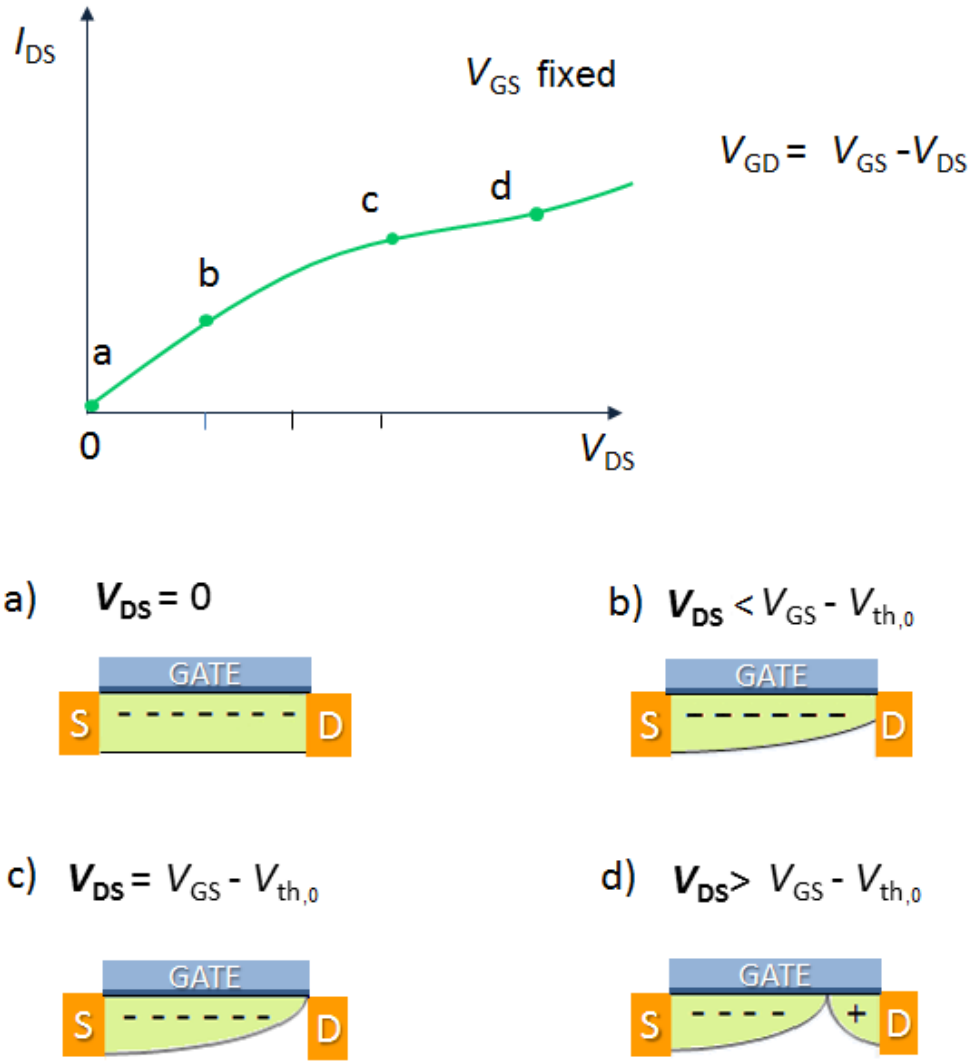

Figure 3.2: The output *I-V* characteristic and corresponding doping profile of an intrinsically n-doped GFET biased at a fixed V_{GS}. a) When $V_{DS} = 0$ the channel is not conductive. b) Increasing V_{DS} to positive values an electron current flows between source and drain. c) When the channel potential at the drain equals $V_{th,0}$ the channel pinches off at the drain side, exhibiting pseudosaturation in the *I-V* curve. d) At higher V_{DS} the Dirac point enters in the channel that becomes ambipolar and current increases.

The output *I-V* characteristic of the GFET at a fixed V_{GS} is shown in figure 3.2. When no voltage is applied between the electrodes, i.e. $V_{DS} = 0$, the channel is not conductive (figure 3.2a). If the source is kept to ground potential and a positive V_{DS} is applied, an electron current flows in the channel (figure 3.2b). Increasing V_{DS} the channel pinches off at the drain side (figure 3.2c). The pinch-off occurs when the potential at the drain,

V_{GD} , equals the treshold value $V_{th,0}$ so that the reduced DOS limits the carrier injection. While in Si MOSFETs the pinch-off leads to current saturation, in GFETs this phenomenon causes only a pseudosaturation, because a further increase of V_{DS} would directly switch the channel below drain from n to p-type resulting in a mixed electron-hole conduction (figure 3.2d).

To examine the transfer characteristics of the GFET consider figure 3.3, where the V_{DS} is fixed at a positive value. If $V_{GS} < V_{th,0}$ is applied, a hole current will flow in the channel (figure 3.3a). When $V_{GS} = V_{th,0}$ the channel pinches off at the source (figure 3.3b) and increasing V_{GS} further will cause the Dirac point to move inside the channel resulting in mixed electron-hole conduction (figure 3.3c). The current minimum is found at $V_{GS} = V_{th}(V_{DS})$, when the Dirac point is in the middle of the channel so that electron and hole currents are equal and the carrier density is at its minimum value (figure 3.3d) [4]. At higher V_{GS} the channel conduction will experience a transition from a majority hole to a majority electron carriers figure (3.3e) until pinch-off at the drain side occurs when the $V_{GD} = V_{th,0}$ (figure 3.3f). In contrast with Si MOSFETs, the channel in GFETs is always conductive, and the gate voltage cannot switch the transistor between the on and off states, but rather between p and n-type, passing trough a state of maximum resistance. For this reason while the typical current on-off ratio, I_{on}/I_{off}, of MOSFETs is between 10^4 and 10^7, in GFETs it is usually below 10 in air ambient, limiting GFETs potentiality in digital electronics [21]. There is an extensive research concerning bandgap opening in graphene in order to increase the current on/off ratio. This can be accomplished by patterning of graphene in nanoribbons, application of high perpendicular electric fields to A-B graphene bilayers [49], or fabrication of heterostructures with other 2-D materials [50]. However all these approaches exhibit drawbacks. In graphene nanoribbons the edge roughness and the bandgap opening result in a reduced mobility and consequently low on current. In bilayer graphene, the bandgap opened with perpendicular electric fields can be as high as 250 meV, a value still too small to fabricate good transistors [21]. Heterostructures with MoS_2 and h-BN are currently under investigation, but their fabrication still involves exfoliation and transfer methods, thereby limiting these structures to a proof of principle devices [51].

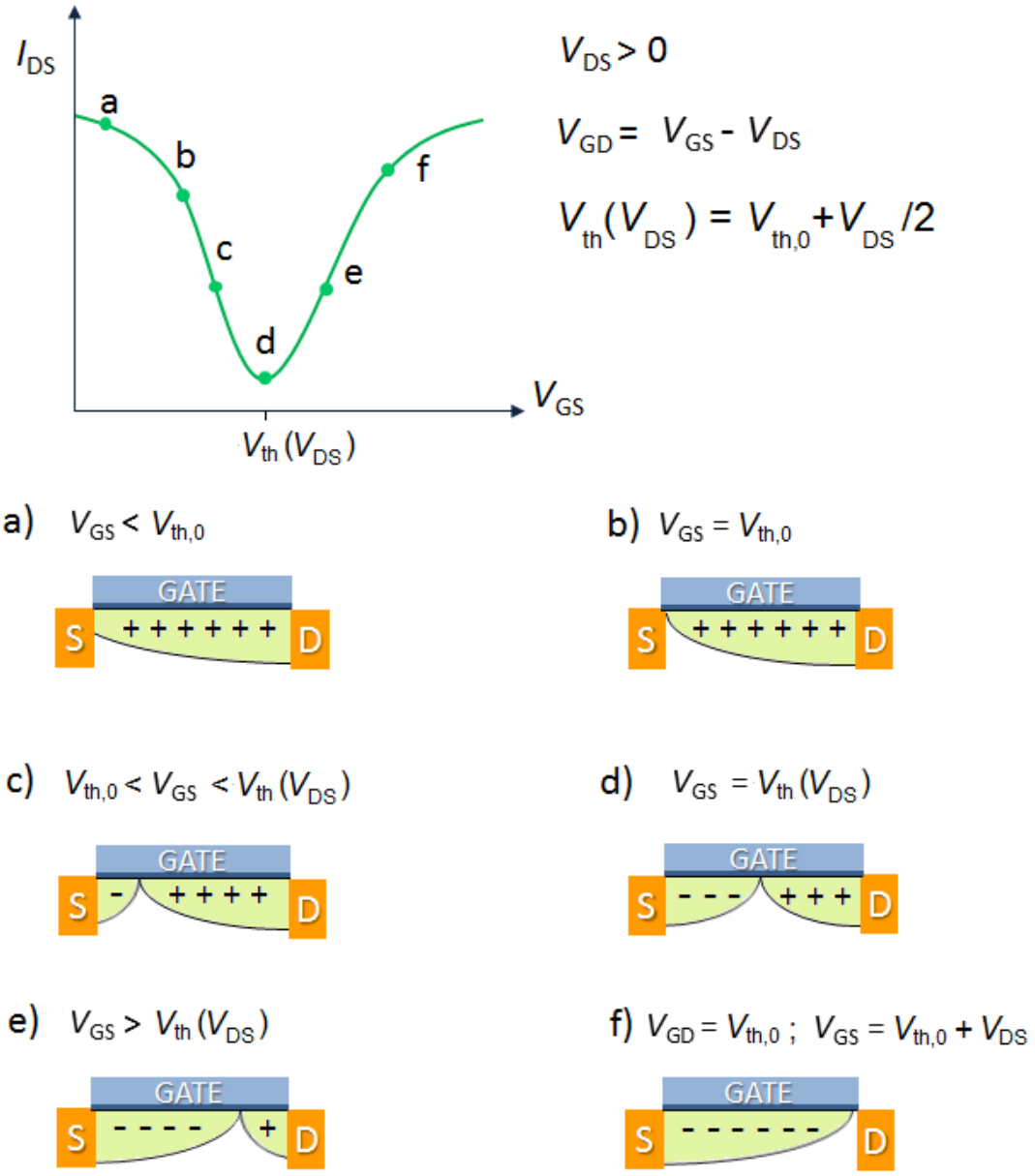

Figure 3.3: Transfer characteristic and corresponding doping profile of a GFET when a fixed $V_{DS} > 0$ is applied. a) At $V_{GS} < V_{th,0}$ the channel experience hole conduction. b) When $V_{GS} = V_{th,0}$ the channel pinches off at the source. c) Increasing V_{GS} the Dirac point enters the channel. d) When $V_{GS} = V_{th}(V_{DS})$ the Dirac point is in the middle of the channel resulting in a current minimum. e) At higher V_{GS} the majoritary carriers are electrons. f) When the potential below the drain, V_{GD}, goes to $V_{th,0}$ the channel pinches off at the drain side.

3.1.2 Intrinsic gain

The intrinsic gain A_0 is an important parameter, defined as the maximum gain that is available from a single transistor, and corresponds to the open-circuit voltage gain of the GFET shown in figure 3.4 [52]:

$$A_0 = \frac{v_{\text{out}}}{v_{\text{in}}} = g_{\text{m}} r_{\text{d}}$$

where r_{d} is the output resistance and g_{m} is the transconductance of the GFET (the derivation of the small-signal model is provided in section 5.3).

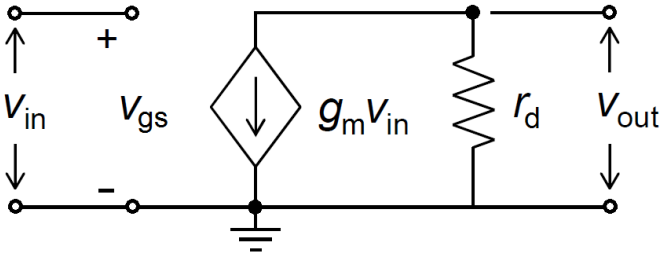

Figure 3.4: Small-signal equivalent circuit of an ideal GFET valid at low frequencies. The parameter g_{m} is the transconductance and r_{d} is the output resistance of the GFET.

The output resistance can be derived from the DC characteristics as the inverse of channel current derivative with respect of the voltage drop along the channel:

$$r_{\text{d}} = \left(\frac{\partial I_{\text{D}}}{\partial V_{\text{DS}}} \right)^{-1} \tag{3.1}$$

As discussed in section 3.1.1, current saturation in standard MOSFETs arises from pinch-off. The conductive channel of a MOSFET is created when the potential difference between the gate and the substrate is above a threshold value V_{th}, so that an inversion layer connecting source and drain is formed. When a V_{DS} is applied, current flows between the drain and source. When the gate-to-drain voltage difference is below the threshold, $V_{\text{GD}} < V_{\text{th}}$, the MOSFET enters in pinch-off mode characterized by the lack of channel region near the drain. Although the channel does not extend the full length of the device, the high electric field existing between the drain and the channel allows conduction, with the drain current showing a weak dependence upon drain voltage and controlled primarily by the gate-source voltage [5]. In graphene there is no threshold voltage for conduction, thus current saturation can only occur as pseudosaturation when electron and hole conduction equals or as velocity saturation in high-field regime (see section 2.4) [42].

The achievement of a good current saturation is one of the main issues of GFETs technology. One option is to look for high saturation velocity in ultra-clean samples with low-defectivity on high-phonon energy substrates like h-BN. However this technology is

not yet mature to be applied to a large-scale production, and is limited by the high cost and complicate processing. Similarly, patterning graphene into nanoribbons reduces current and mobility, washing out the advantage of higher saturation (see section 2.4). A different approach consists in using thinner gate oxide, to increase the depletion rate of the channel and reduce the effect of intrinsic carriers and interfacial traps, with a consistent improvement in saturation characteristics [53].

A thinner oxide has the other important advantage of improving the gate voltage control on the current, the parameter defined as transconductance:

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{GS}}} \tag{3.2}$$

Assuming an approximated large-signal model valid in the linear region [22] to describe a single GFET as a simple voltage-controlled resistor, the drain current can be modeled as:

$$I_{\mathrm{D}}(V_{\mathrm{DS}},V_{\mathrm{GS}}) = \frac{W}{L}\left(\sigma_0 + \frac{\varepsilon_0\varepsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}}\mu\left|V_{\mathrm{GS}} - V_{\mathrm{th}}\right|\right)V_{DS} \tag{3.3}$$

where σ_0 is the conductance of the channel at Dirac point [2]. An explicit calculation of (3.1) and (3.2) from (3.3) gives for transconductance an output resistance the following expressions:

$$g_{\mathrm{m}} = \frac{W}{L}\frac{\varepsilon_0\varepsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}}\mu V_{\mathrm{DS}} \tag{3.4}$$

$$r_{\mathrm{d}} = \left[\frac{W}{L}\left(\sigma_0 + \frac{\varepsilon_0\varepsilon_{\mathrm{ox}}}{\mathrm{t}_{ox}}\mu\left(V_{\mathrm{GS}} - V_{\mathrm{th}}\right)\right)\right]^{-1} \tag{3.5}$$

The expressions show that high-$\varkappa$, thin oxides (large $\varepsilon_{\mathrm{ox}}/t_{\mathrm{ox}}$) can provide both a higher transconductance and a higher output resistance compared to conventional SiO_2 dielectric. This solution has been investigated in the current work to develop devices with high intrinsic gain for a wide range of applications.

3.2 Graphene inverters

The CMOS inverter is the main device based on MOSFET structure. It consists of a PFET and an NFET connected in series, sharing a common drain electrode. A digital signal applied to the input terminal (the gate) comes to the output (the common drain) with its phase shifted by 180°, i.e. inverted. In digital electronics, several CMOS logic gates can be connected together and cascaded to perform multiple logic operation. The Si CMOS technology offers extremely low static power consumption, fast on/off switching rate and higher packing density compared to BJT-based devices, leading this technology to dominate the market [54]. In this section graphene inverters fundamentals will be presented

[2] Note that this oversimplified expression does not take into account the shift of the drain voltage dependence of V_{th}.

and compared with Si CMOS inverters, and details on fabrication and performances will be given.

3.2.1 Operating principle

Since graphene is a bipolar conductor, a single GFET can be either p-type or n-type depending on the bias condition. Thus, in principle, graphene inverters can be simply fabricated by connecting two GFETs in series on the same graphene channel, sharing a common electrode, see figure 3.5.

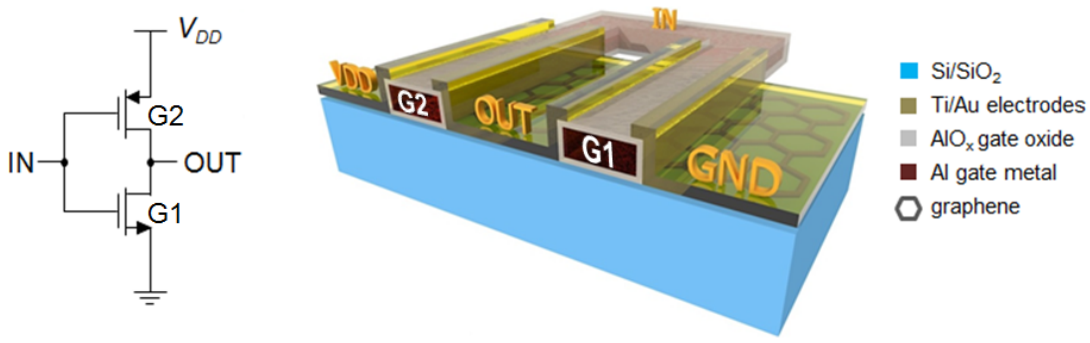

Figure 3.5: Graphene inverter (right) and circuit schematic (left). From reference [22].

When no bias V_{DD} is applied, the two GFETs have the same average doping level. When $V_{\mathrm{DD}} > 0$ is applied, the channel would be depleted from electrons, thus a more positive input voltage will be needed to restore the charge neutrality. The voltage drop occurs all along the channel, but the potential of the channel in G2 increases with respect to that in G1, shifting the Dirac point of G2 to higher input voltages. Indeed the average potential of G1 varies from V_{th} to $(V_{\mathrm{OUT}}+V_{\mathrm{th}})/2$, while the average potential of G2 varies from V_{th} to $(V_{\mathrm{DD}}+V_{\mathrm{OUT}})/2$. Complementary operation is obtained applying an input voltage between the Dirac points of the two GFETs, with one GFET biased in the p-type-operation region and the other one in the n-type, figure 3.6b.

The output voltage of the inverter is obtained from the voltage divider shown in figure 3.5:

$$V_{\mathrm{OUT}} = \frac{V_{\mathrm{DD}}}{R_1 + R_2} R_2 = \frac{V_{\mathrm{DD}}}{\frac{R_1}{R_2} + 1} \tag{3.6}$$

where R_1 and R_2 are the resistances of GFETs G1 and G2, see figure 3.5. Note that in graphene inverters, differently from conventional CMOS inverters, rail-to-rail operation is not possible, i.e., the output voltage never reaches zero or V_{DD} because GFETs cannot be turned off. The maximum voltage swing, $V_{\mathrm{p-p}} = V_{\mathrm{out,max}} - V_{\mathrm{out,min}}$, is related to the resistance on-off ratio γ:

$$V_{\mathrm{p-p}} = \frac{\gamma - 1}{\gamma + 1} V_{\mathrm{DD}}.$$

If we assume that the GFETs are identical, so that their on and off resistances are the same, then V_{OUT} varies between $V_{DD}/(1+\gamma)$ and $\gamma V_{DD}/(1+\gamma)$. Typical values for γ are between 2 and 5, so in the best case of $\gamma = 5$ the maximum swing is $\approx 66\%$ of V_{DD}.

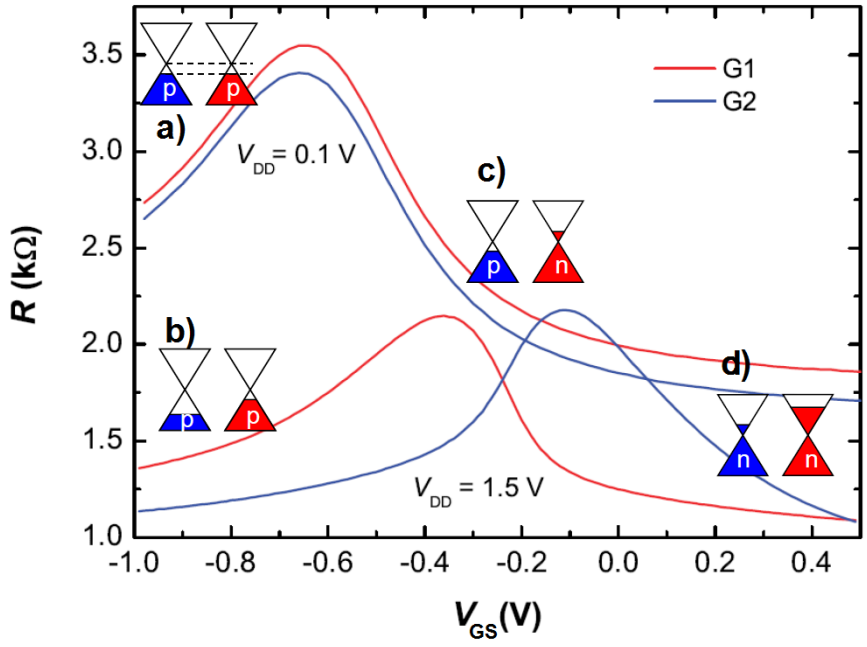

Figure 3.6: Transfer curves of single GFETs in inverter configuration. (a) At low bias (V_{DD} = 0.1 V) GFETs have the same doping level. The application of a large bias to the inverter (V_{DD} =1.5 V) causes the Dirac points of the GFETs to split. (b) When V_{GS} is lower than the Dirac points of the two GFETs ($V_{\mathrm{GS}} < V_{\mathrm{th},1} < V_{\mathrm{th},2}$), both GFETs are p-type; (c) between the two Dirac points they exhibit complementary operation ($V_{\mathrm{th},1} < V_{\mathrm{GS}} < V_{\mathrm{th},2}$); (d) at $V_{\mathrm{th},1} < V_{\mathrm{th},2} < V_{\mathrm{GS}}$ both GFETs are n-type. Adapted from reference [22].

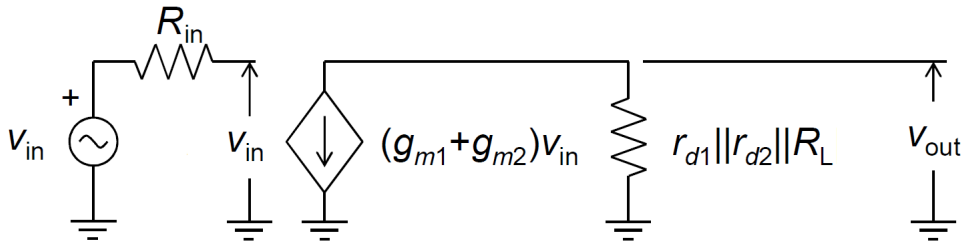

Figure 3.7: Small-signal equivalent circuit for an inverter in complementary configuration, valid at low frequencies (where capacitances can be neglected). Here R_{in} and R_{L} represent input and load impedence related to the measurements setup.

Since almost all electronic circuits comprise multiple stages, each stage must provide voltage amplification in order to preserve the signal integrity during transmission. A circuit is an amplifier if the output voltage swing is larger than the input voltage swing, the amount of the amplification being equal to the voltage gain:

$$v_{\mathrm{out}} = A_v v_{\mathrm{in}} \tag{3.7}$$

The voltage gain of an inverter can be derived from the small-signal circuit shown in figure 3.7 as:

$$A_v = \frac{v_{\mathrm{out}}}{v_{\mathrm{in}}} = -(g_{\mathrm{m1}} + g_{\mathrm{m2}})(r_{\mathrm{d1}} || r_{\mathrm{d2}} || R_{\mathrm{L}}).$$

This model is valid at low frequency, where the value of ac voltage gain approaches the DC value $A_{\mathrm{v}}(0) = dV_{\mathrm{OUT}}/dV_{\mathrm{IN}}$. Assuming that GFETs have identical characteristics so that $r_{\mathrm{d1}} = r_{\mathrm{d2}} = r_{\mathrm{d}}$ and $g_{\mathrm{m1}} = g_{\mathrm{m2}} = g_{\mathrm{m}}$, the expression simplifies to:

$$A_v = -2g_{\mathrm{m}}(r_{\mathrm{d}}/2 || R_{\mathrm{L}}) \tag{3.8}$$

With $R_{\mathrm{L}} \to \infty$ the voltage gain assumes the maximum value of:

$$A_v = -g_{\mathrm{m}} r_{\mathrm{d}} \tag{3.9}$$

that is equal to the intrinsic gain of a single GFET derived in section 3.1.2, $A_v = -A_0$ (minus sign stems for signal inversion).

3.2.2 Experimental background

Pioneering works on graphene transistors have been based on graphene flakes exfoliated on top of Si/SiO_2 substrate [2]. The production of graphene flakes through mechanical exfoliation is a very cheap technique that can be used at laboratory scale to obtain monolayers up to hundreds microns of size. It consists of peeling-off the surface of HOPG with a scotch tape, pressing the tape on top of the silicon chip and peeling it off again to release the material [55]. Among the debris transferred on the substrate, having different thickness distribution, there will be also a certain probability to find graphene monolayers. Usually these mechanically exfoliated flakes exhibit much better physical properties compared to graphene obtained through physical growth or chemical synthesis, because they are free of defects and grain boundaries. Despite the great advantages in terms of cost and performances offered by this technique, it is limited to the laboratory scale, where it has been extensively used to demostrate early proof of principle devices. Nowadays growth techniques like CVD on Cu and epitaxy on SiC are mature enough to provide good quality material, compatible with industrial processes, that is extensively supplanting exfoliated graphene [56].

In the early reports, GFETs exhibited a very poor transconductance mainly due to the low-$\varkappa$ ($\varepsilon_{\mathrm{ox}}$= 3.9) and the high thickness (tipically 300 nm) of the silicon oxide covering the substrate and providing a back gate dielectric [57]. The choice of such substrates was

forced by practical considerations, since in this case the optical interference allows one to see even a monolayer with optical microscope under white light, providing an easy method to identify graphene flakes [58]. However, with poor transconductance, voltage gain was very low (much less than one) and high back gate voltages (up to hundred volts) were needed to tune the channel doping [57].

In 2010 Tsukagoshi and co-workers demonstrated that aluminum evaporated on top of the graphene channel not only oxidizes at the outer surface, but also at the interface with graphene, thereby providing a very thin layer of a gate dielectric of 4 nm in thickness [59]. The dielectric constant of this native oxide, even though lower that that of stoichiometric Al_2O_3, is around 7, higher than that of SiO_2. This oxide not only improves the transconductance, but allows to operate the device with much smaller gate voltages, making it possible to achieve input/output signal matching.

3.2.3 Fabrication of exfoliated-graphene amplifiers

The technique based on spontaneous formation of AlO_x has been adopted to fabricate high performances amplifiers. Graphene flakes were obtained through the scotch-tape method and transferred on top of highly As-doped (n-type) Si chips. The top side of the chips is covered by a 300 nm thick layer of thermally grown SiO_2, while the bottom side is covered by a 3 nm of Cr, 5.5 nm of Sb and 200 nm of Ag conductive layer. Graphene crystallites can be visualized by the use of optical microscopy and the optical contrast gives an indication on the thickness. The selected flakes were specifically identified as mono, bi or multilayers with the aid of Raman spectroscopy, which allows a precise measurement of the flake height. The typical distance between two graphene planes in bulk graphite is known to be around 0.4 nm [2]. However, the thickness measured with AFM is usually higher, an evidence commonly attributed to the presence of a layer of adsorbed water between the substrate and graphene layers deposited on top. Thus, thicknesses of the order of 1-1.4 nm were commonly attributed to monolayer graphene, while higher values up to 2 nm, to bilayers. The randomness of exfoliation process is responsible of the irregular shape and variable size distribution of the flakes, preventing the use of a standard device design. Thus, all the fabricated GFETs differ in terms of channel shape and size, preventing a collection of a good statistics on the device performance.

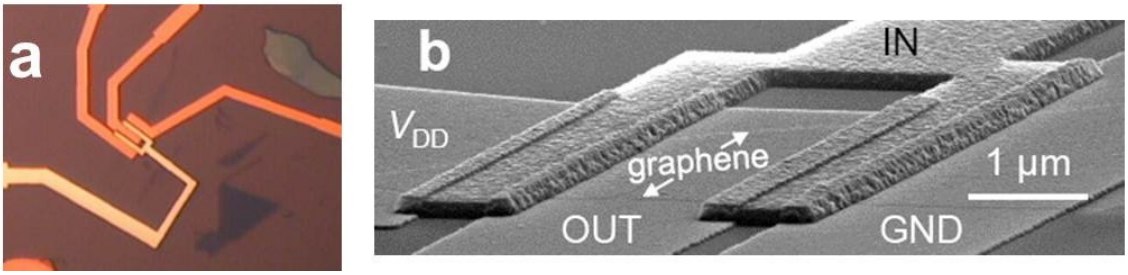

Figure 3.8: Optical image (a) and SEM image (b) of a graphene voltage amplifier. From reference [22].

Source, drain and top gate contacts were fabricated through an e-beam lithography process with PMMA as positive resist, followed by e-beam evaporation and lift off. Top gates were fabricated in the first step by direct evaporation of 100 nm of Al on the patterned area. The metal oxidizes all around the contacts as described previously, providing an insulating layer of AlO_x. In order to eliminate access resistances, the 5 nm Ti/ 50 nm Au electrodes were overlapped with the gates, assuring a complete channel coverage, as shown in figure 3.8,b. This procedure resulted in an improved channel stability compared to standard non-overlapped devices, since the coverage prevents the contamination of channel by enviromental doping, thereby reducing hysteresis in the I-V characteristics.

With this approach the first graphene amplifier showing a room temperature voltage gain higher than 10 dB has been demonstrated [22]. The characterization of these high-gain amplifiers will be further investigated in the following section since these devices represented the starting point of this research.

3.2.4 Characterization of high gain amplifiers

Figure 3.9 shows the circuit diagram of the fabricated inverter in the complementary push-pull configuration used to perform the AC measurements. In this setup the gate terminal (IN) was biased with a sinusoidal signal $v_{\mathrm{IN}} = V_{\mathrm{IN}} + V_{\mathrm{in}}\sin(2\pi ft)$ applied by a Tektronix AFG 3022B function generator, while input and output signals were measured by an Agilent infiniium 54832D mixed-signal oscilloscope. The output resistance of the function generator ($R = 50\ \Omega$) is small compared to the input impedence of the oscilloscope ($Z = 1\ \mathrm{M}\Omega\ ||13$ pF), thus it can be neglected in the series connection. Figure 3.10 shows the transfer curve V_{OUT} vs. V_{IN} of the amplifier biased with V_{DD}= 1.5 V. The largest value of the voltage gain obtained with this supply voltage was $|A_{\mathrm{v}}|_{\mathrm{max}}$= 2.1 at the DC operating point Q. The expression for the low-frequency voltage gain can be derived from (3.9), (3.4) and (3.5), see section 3.2.1:

$$A_v = -\frac{V_{\mathrm{DS}}}{V_{\mathrm{GS}} - V_{\mathrm{th}} + \sigma_0 t_{\mathrm{ox}} / (\varepsilon_0 \varepsilon_{\mathrm{ox}} \mu)} \tag{3.10}$$

Assuming that at point Q the two GFETs exhibit the same resistance (see figure 3.6,b), then the voltage drop on each GFET should be approximately $|V_{\mathrm{DS}}| \approx V_{\mathrm{DD}}/2$, and the quantity $(V_{\mathrm{GS}} - V_{\mathrm{th}}) \approx (V_{\mathrm{th},2} - V_{\mathrm{th},1})/2 = \Delta V_{\mathrm{IN}}$, since the Q point corresponds to the input voltage that lies between the Dirac voltages of the two GFETs. Therefore the expression for the maximum voltage gain becomes [22]:

$$|A_v|_{\mathrm{max}} = \frac{V_{\mathrm{DD}}}{\Delta V_{\mathrm{IN}} + 2\sigma_0 t_{\mathrm{ox}} / (\varepsilon_0 \varepsilon_{\mathrm{ox}} \mu)} \tag{3.11}$$

where the quantity ΔV_{IN} depends on V_{DD}. Expression (3.11) shows that a higher gain can be found at higher supply voltages.

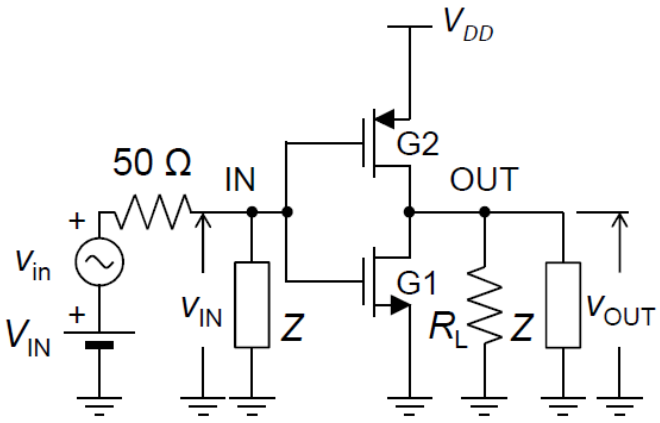

Figure 3.9: A circuit diagram of the amplifier. Z =1 MΩ||13 pF is the input impedance of the oscilloscope used to measure input and output signals while 50 Ω is the output resistance of the input voltage source. Since $|Z|>>50$ Ω the input signal fully drops across Z, i.e., $v_{\mathrm{IN}}(\mathrm{t}) = V_{\mathrm{IN}} + v_{\mathrm{in}}(\mathrm{t})$, where V_{IN} is the DC bias voltage and $v_{\mathrm{in}}(\mathrm{t})$ is the AC component of the input signal. The load resistance R_{L} simulates the input resistance of the next amplifying stage. In the measurements presented here this resistance was infinite.

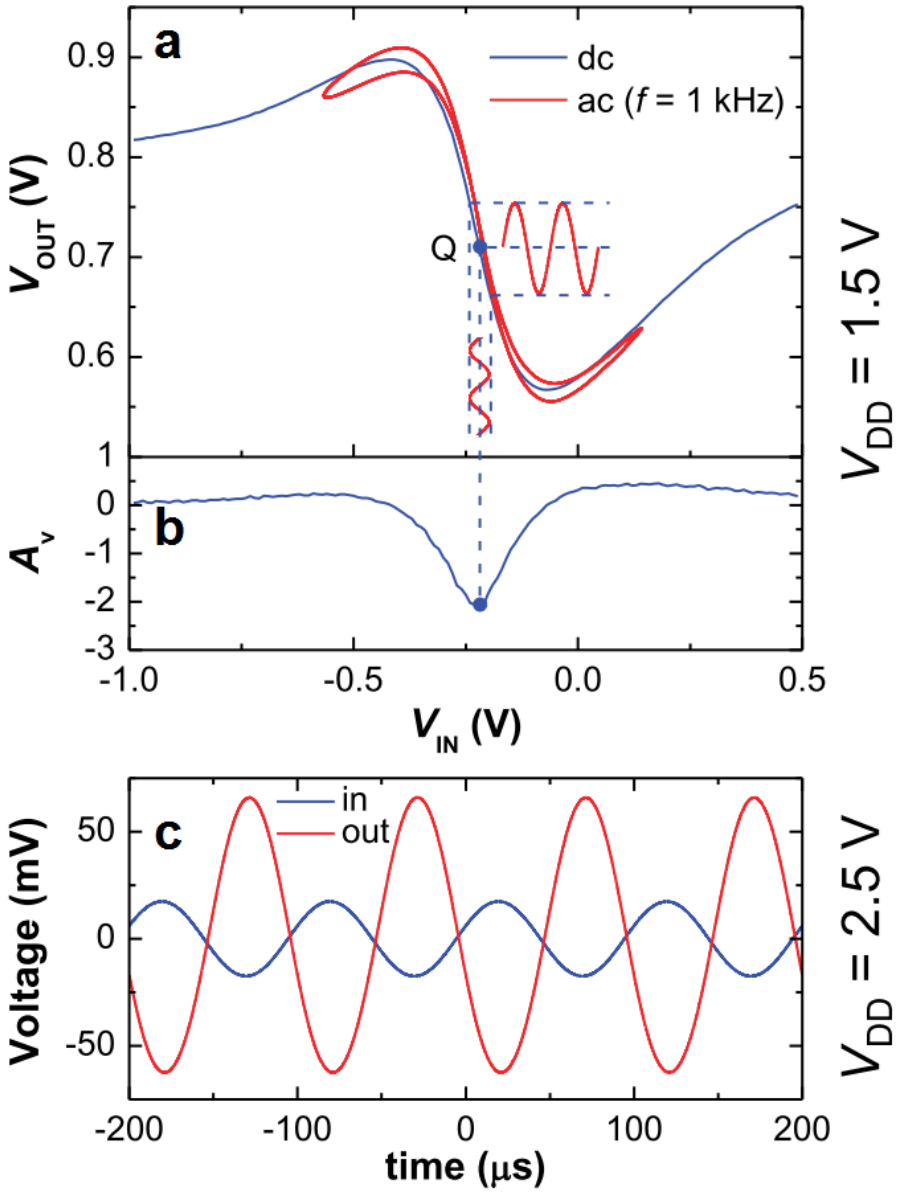

Figure 3.10: Principle of voltage amplification. a) Static (DC) transfer curve of the amplifier is shown in blue. Dynamic (AC) transfer curve is shown in red and was obtained by plotting output voltage v_{OUT} vs. input voltage $v_{\mathrm{IN}} = V_{\mathrm{IN}} + V_{\mathrm{in}}\sin(2\pi ft)$, with $f = 1$ kHz. b) Low-frequency voltage gain $A_v = dV_{\mathrm{OUT}}/dV_{\mathrm{IN}}$. A small signal superposed to the DC operating point Q is amplified at the output. c) AC components of the input and output voltage signals at a frequency $f = 10$ kHz. From reference [22].

The fabricated GFETs at high supply voltages exhibit a transconductance of $g_{\mathrm{m}}/W \sim 500$ mS/mm [22], that combined with relatively large output resistance $r_{\mathrm{d}}W \sim 10.5$ kΩ μm (see figure3.11) results in measured DC and AC voltage gains above 10 dB.

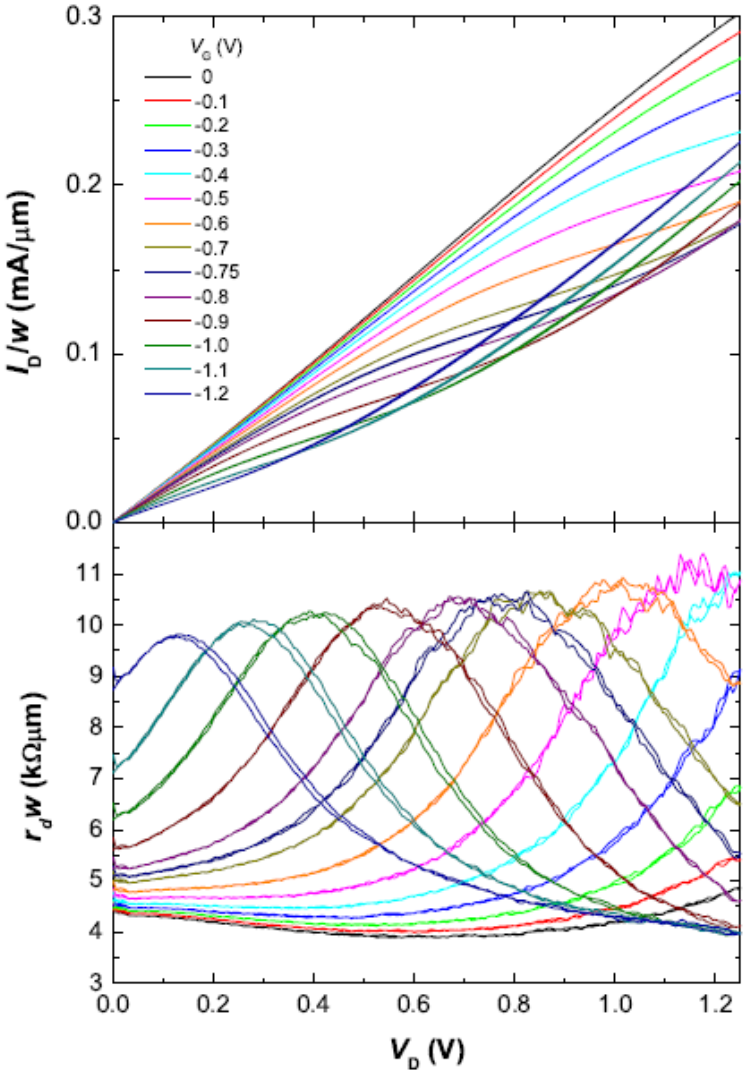

Figure 3.11: Static (DC) characteristics of one of the fabricated GFETs whose Dirac point is at $V_{\rm th} = -1.12$ V. a) Current-voltage characteristics. b) Output resistance. From reference [22].

Figure 3.10c shows measured ac components of the input and output voltage signals of the amplifier biased at $V_{\rm DD} = 2.5$ V (DC components have been removed from the plot for clarity). At this supply voltage a maximum voltage gain of $|A_{\rm v}|_{\rm max}$=3.7 was measured at an input frequency of 10 kHz. As discussed above a higher gain could be obtained at higher voltage supplies. The maximum applicable bias is set by the maximum current density that can be sustained by the flake (∼1.2 mA/μm [60], five times higher than the current flowing in our devices at 2.5 V) and by the maximum voltage drop sustained by the gate oxide. Since the upper part of the channel is at a potential $V_{\rm DD}$, the voltage drop on the gate oxide is given by $V_{\rm DD}$ -$v_{\rm IN}$. Here $v_{\rm IN} = V_{\rm IN} + V_{\rm in}\sin(2\pi ft)$, where $V_{\rm IN}$ = -0.22 V and $V_{\rm in}$

= 0.35 V, giving -0.57 < v_{IN}< 0.13 V, so for V_{DD} > 2.5 V the voltage drop on the gate would be higher than 2.35 V, a value that is close to the breakdown voltage of the oxide $V_{B,ox}$= 2.5 V.

The frequency response of the fabricated amplifiers has been investigated and results are shown in figure 3.12a. The amplifier is biased at V_{DD} = 2.5 V and a small AC signal is superposed to the DC Q point-voltage, giving the maximum signal amplification $|A_v|_{max}$ = 3.7 (11.4 dB). The gain remains constant up to about 20 kHz, and then decreases as the frequency is increased, dropping by 3 dB at the higher cutoff frequency $f_{-3\ dB}$ = 70 kHz which also defines the bandwidth of the amplifier. The amplifier is capable of signal amplification up to a unity-gain frequency f_1 = 360 kHz. At this frequency, the amplifier operates as a unity-gain amplifier (buffer), while for $f > f_1$ it attenuates the input signal. The signal phase shift φ introduced by the amplifier is 180° at low frequencies (signal inversion), decreasing to 90° at high frequencies, see figure 3.12b.

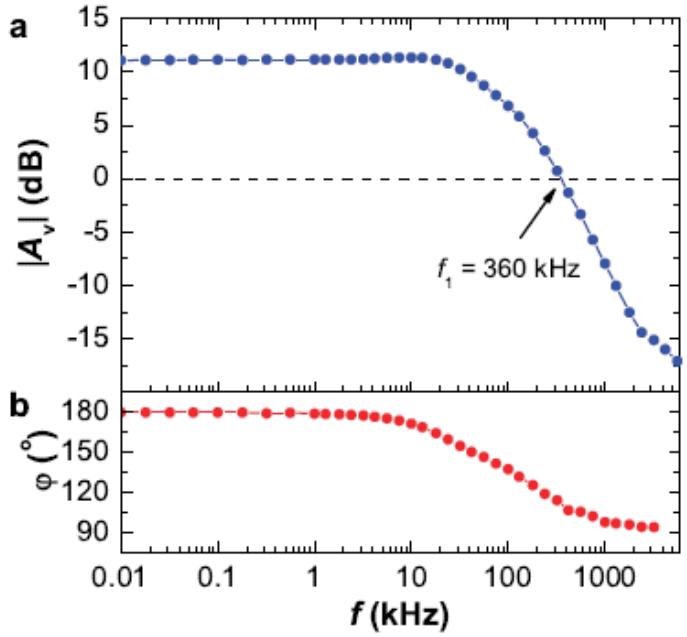

Figure 3.12: Frequency response of the amplifier. a) Gain magnitude. b) Phase shift between input and output signals as a function of frequency. From reference [22].

Both amplitude and phase characteristics of the voltage gain indicate a typical dominant-pole (at f_{-3dB}) behavior. However, this pole does not originate from the amplifier but from the capacitances of the cables used to connect the amplifier to the measurement equipment. The cables have a total conductor-to-ground capacitance $C_c \approx 0.5$ nF which introduces a pole at a frequency $f_p = (2\pi(r_d/2 + R_c)C_c)^{-1} \approx 100$ kHz, where $R_c \approx 1.5$ kΩ is the contact resistance of the output line. The obtained value is consistent with the measured f_{-3dB}. As

no other poles were observed, the fabricated amplifier has cutoff and unity-gain frequencies above 5 MHz which may extend its application to high-frequency circuits [3].

3.3 Cascading of stages

The discussed GFETs, despite representing a huge step forward to fully-integrated graphene circuits, were not scalable and exhibited wide performance variations from one sample to another due to the randomness of exfoliation procedure. This fundamental issue had to be addressed in order to realize more complex electronic circuits. This section is devoted to discussion on the advancement that allowed to demonstrate cascaded devices, beginning with an introduction of the fundamental characteristics that a single stage should exhibit in order to provide cascading capability.

3.3.1 Operating principle

In order to fabricate more complex circuits the issue of signal matching is of fundamental importance, because it represents one of the requirements for device cascading. To cascade two identical inverters the output and the input DC offsets must be equal at the highest gain point, so that one stage can drive the other in the amplifying mode to propagate the signal without loosing its amplitude. The highest voltage gain is reached at the DC operating point that lies approximately between the Dirac points of the two complementary GFETs, labeled as Q point. When a negligibly small V_{DD} is applied, the DC offset of V_{OUT} is almost zero according to (3.6), and the offset of V_{IN} is set equal to V_{th} to operate the device in the Q point (see figure 3.6a). By increasing V_{DD} the splitting between Dirac points of the two GFETs increases, and the DC component of V_{IN} should be increased to $V_{\mathrm{th}} + V_{\mathrm{DD}}/\left(1 + R_1/R_2\right)$, while the DC component of V_{OUT} shifts to $V_{\mathrm{DD}}/\left(1 + R_1/R_2\right)$, where $R_1/R_2 \approx 1$ in Q (see figure 3.6c). It follows that, in ideal condition of undoped graphene such that $V_{\mathrm{th}} = 0$, $V_{\mathrm{IN}} = V_{\mathrm{OUT}} \approx V_{\mathrm{DD}}/2$. The matching is possible because the input voltage V_{IN} has the same order of magnitude of the bias voltage V_{DD}. With a lower capacitive oxide, such as the thick SiO_2 back gate, the V_{IN} required to reach the Dirac voltage is almost one order of magnitude higher than V_{DD}, so V_{OUT} is not enough to drive the next stage in the highest gain point [57, 59].

Voltage gain and signal matching are the two requirements that must be fulfilled for cascading, togheter with homogeneus devices characteristics (on-off ratio, channel resistance, doping level), thus an efficient gate oxide and high quality graphene with low doping level are necessary.

The voltage amplifiers described in section 3.2.4 did not show signal matching (see figure 3.10a), thus were not suitable to fabricate more complex circuits. A breakthrough was achieved through the implementation of CVD grown graphene as GFET channel material. The joint efforts of several research groups in developing the growth process resulted in an improved quality of CVD graphene, that despite being still more defective than exfoliated

[3] An intrinsic unity-gain frequency can be estimated to be ~ 8.6 GHz [22].

graphene can deliver sufficiently high mobilities (up to $\sim$ 5,000 $cm^2V^{-1}s^{-1}$) to fabricate GFETs with good performances.

3.3.2 Fabrication of CVD-graphene amplifiers

In this stage of the project we have employed CVD-grown graphene provided by the group of Eric Pop at the University of Urbana-Champaign, IL. Graphene CVD-growth has undergone large improvements recently, thanks to the intensive research to understand the impact of the initial nucleation and growth dynamics on the final film quality. It has been shown that the growth from CH_4 precursor on Cu(111) surface at high temperatures (T = 1000 °C) promotes monolayer formation thanks to a high cracking and diffusion efficiency of carbon atoms [56]. The quality of the material employed in this work has been confirmed by Raman analysis. The G/2D peak ratio suggests the presence of primarily monolayer graphene, while the small integrated D/G ratio (< 0.2) implies relatively good quality of graphene grown by CVD, see figure 3.13.

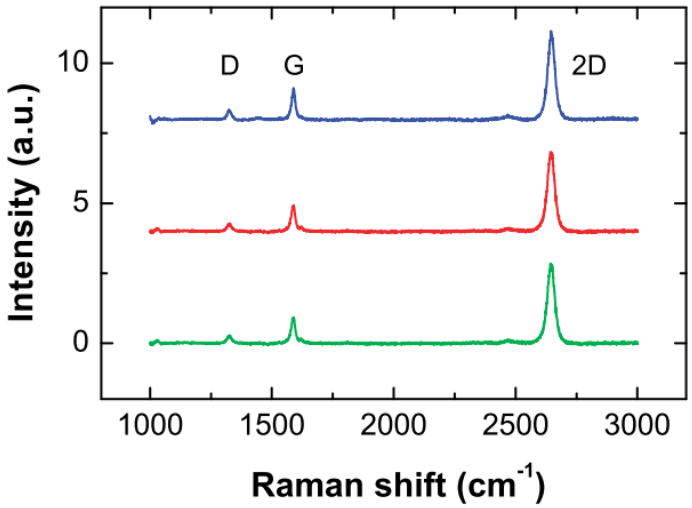

Figure 3.13: Raman spectra of typical graphene films used in this study. From reference [23].

After growth the material was wet-transferred on top of conventional silicon substrates [23]. The wet transfer method involves the use of a dual stack of PMMA (60 nm of 495 A2 and 250 nm of 950 A4) deposited on top of graphene for support and protection. The copper substrate is dissolved with an etchant ($FeCl_3$ solution) and the graphene-stand layer stack can be transferred in solution on top of another substrate. After transfer the substrate is gently heated to promote graphene adhesion and the stand layer is dissolved in acetone. This process introduces some unwanted contaminations in graphene, because PMMA residues are left on the film even after cleaning.

The device fabrication process starts with an etching step to define the channels. PMMA

positive resist is exposed in the 1 mm^2 area surrounding the channel. After development the sample is treated with oxygen plasma reactive ion etching to remove graphene from the exposed areas, while channels are protected by the PMMA mask. The described procedure provides the desired number of channels with equal shape and size troughout the sample, making it possible to standardize design for all devices and leading to a more reliable statistics compared to exfoliated samples. The fabrication of gates and electrodes proceeds as described in section 3.2.3. Figure 3.14a shows a magnified image of the active part of the device (excluding pads and connections). Six GFETs (corresponding to three inverters) where patterned in series, with $W = 20$ µm and $L = 2$ µm. In order to cascade devices the connection between input and output is externally made during measurements trough coaxial cables.

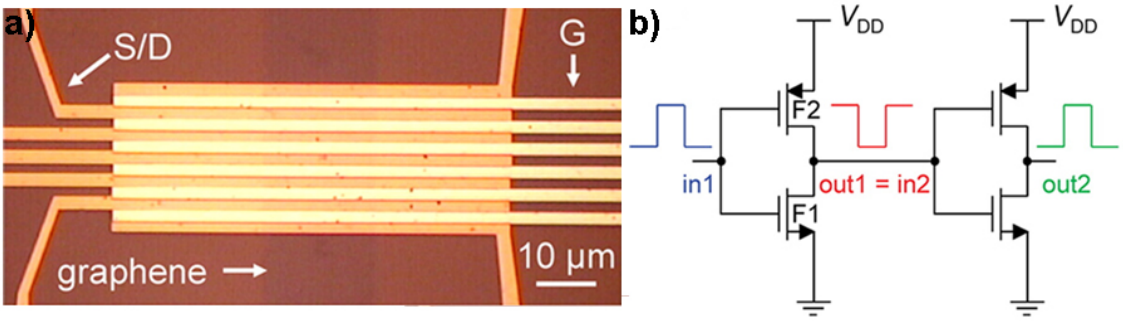

Figure 3.14: a) Optical image of six GFETs in series with $W = 20$ µm; $L = 2$ µm. b) Circuit schematic of cascaded inverters. From reference [23].

3.3.3 Characterization of amplifiers and device cascading

As fabricated, inverters can be individually characterized, see figure 3.14, through independent pads that can be accessed with multicontact probes. Figure 3.15a shows the DC transfer curves of one of the fabricated inverters at several V_{DD}. The voltage gain increases at larger supply voltages, thanks to the increased transconductance, and the largest value obtained under ambient conditions is tipically $A_v \sim -5$ at $V_{DD} = 2.5$ V, figure 3.15b. Moreover, the highest gain is found at the DC operating point Q, where $V_{OUT} \approx V_{IN}$, allowing signal matching.

Digital signals exhibit two well distinguished logic states (0 and 1) corresponding to precise DC voltage levels. The difference between these voltages, also known as voltage swing $V_{p\text{-}p}$, corresponds to the signal amplitude, and voltage gain is needed to preserve the amplitude during transmission. The maximum swing $V_{p-p,in}$ that can be applied at the input so that $V_{p-p,in} = V_{p-p,out}$ can be determined from figure 3.15a by taking the intersection between the transfer curve and the unity-gain line passing through point Q. If the channel is intrinsically doped so that a $V_{IN} = V_{th}$ is needed to move the Fermi level at the Dirac point, the operating point should be shifted from Q to match input and output, however by moving left or right from the Q point the maximum input swing is reduced.

When V_{th} is too large, the input swing should be reduced so much that it ultimately becomes too small to be reliably distinguished from thermal voltage $V_{\mathrm{T}} = k_{\mathrm{B}}T/e$. In this condition the signal cannot be trasmitted.

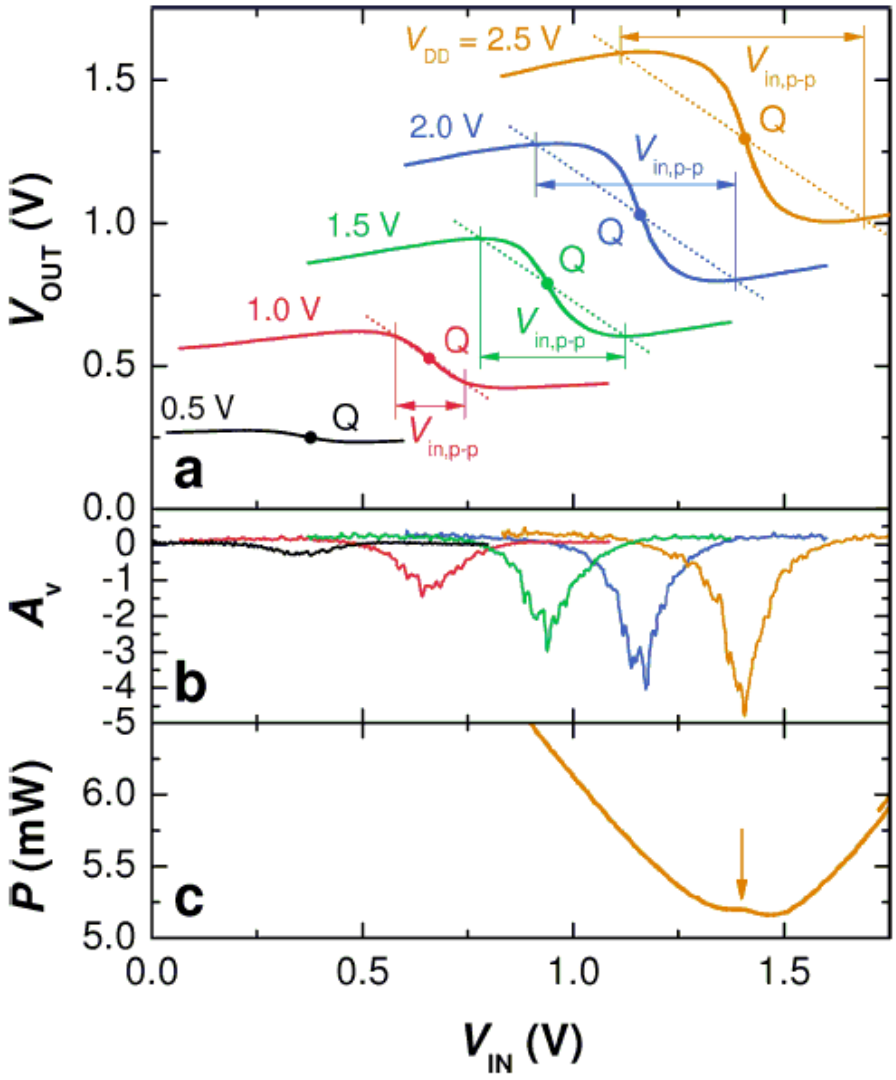

Figure 3.15: Transfer characteristics of CVD graphene inverters showing signal matching (a) and high gain (b). Power dissipated at the operating point shows a minimum (c). From reference [23].

Figure 3.15c shows the power dissipated by the inverter, $P = I_{\mathrm{DD}}V_{\mathrm{DD}}$, as a function of the input voltage, with the current in the inverter defined as $I_{\mathrm{DD}} = V_{\mathrm{DD}}/(R_1 + R_2)$. At the Q point there is a small local maximum of the dissipated power. In conventional Si CMOS this corresponds to a global maximum since both the PFET and the NFET are on (in correspondance of the switching event). On either sides of the operating point one of the FETs turns off while the other goes to saturation mode, the sum of resistances,

$R_1 + R_2$, goes to infinity and the current drops to zero leading to zero dissipated power. However, since GFETs cannot be turned off, static power dissipation cannot be eliminated. To diminish the dissipated power it is would be necessary to reduce the bias, but this leads to a reduced voltage swing, representing a trade-off in device operation.

Figure 3.16 shows the input and output voltage signals of two cascaded inverters, with the output of the first one connected to the input of the second. The signal matching was obtained at the DC operating point Q which lies between the highest-gain points of the two inverters. Since both the inverters show gain $|A_v| > 4$, their over-unity voltage gain is preserved in Q point, allowing cascading. The output signal of the second inverter is amplified with respect to the input, but this does not represent a problem for digital operation, since in order to correctly interprete a signal as 0 (1) it is sufficient that the voltage level is equal or lower (higher) than the input value. The transient behavior observed (rising and falling edges of the signals are not straight as in an ideal square wave) is a consequence of the reduced bandwidth of the setup. The external connections through coaxial cables introduce series resistances and capacitances. Parasitic resistances added in series to channel resistance reduce the transconductance and together with parasitic capacitances play a significant role at high frequency, introducing a low-pass filter that limits the response of the device to the overall response of the circuit (see also 4.1.2).

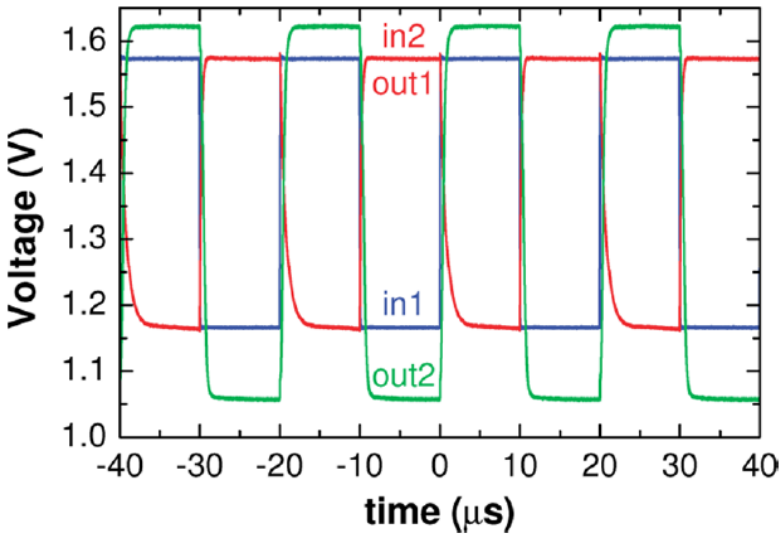

Figure 3.16: Digital waveforms measured under ambient conditions in a cascade connection of two graphene inverters (connected as in figure 3.14b). The supply voltage is $V_{DD} = 2.5$ V and frequency $f = 50$ kHz. Transient behavior observed in this plot is a consequence of the limited bandwidth of the setup. From reference [23].

To explain why the CVD-graphene-based inverters show better performance compared to the exfoliated-graphene-based inverters we should take into account the scalability of this technique. The exfoliated flakes have irregular shapes and random sizes, thus making it difficult to fabricate two equal GFETs on different channels, while CVD technique combined

with reactive ion etching provides identical channels increasing the probability of matching characteristics. Moreover, the use of a standard design and the possibility to pattern as many channels as desired, lead to a larger number of devices fabricated in less time.

3.4 Improvements on graphene amplifiers

Recently, new record performances have been achieved. Inverters have been patterned on a highly-insulating Si substrate on which CVD graphene from Bluestone Global Tech®has been prevously transferred [61]. Fabrication proceeded as described in this chapter. A record DC voltage gain of $|A_{\mathrm{v,DC}}| = 13$, correspondng to 22 dB, has been measured for an inverter with L= 2 μm, W= 10 μm biased at V_{DD}= 2 V, see figure 3.17a[4]. Moreover, this high gain is preserved in AC operation. The same device biased at V_{DD}= 3 V has been tested as small-signal amplifier. An input signal with f =1 kHz and $V_{\mathrm{p\text{-}p}}$= 30 mV has been applied to the gate, superposed to the DC offset providing the highest amplification. The measured AC voltage gain is $|A_{\mathrm{v,AC}}|$= 11.3, corresponding to 21 dB, see figure 3.17b.

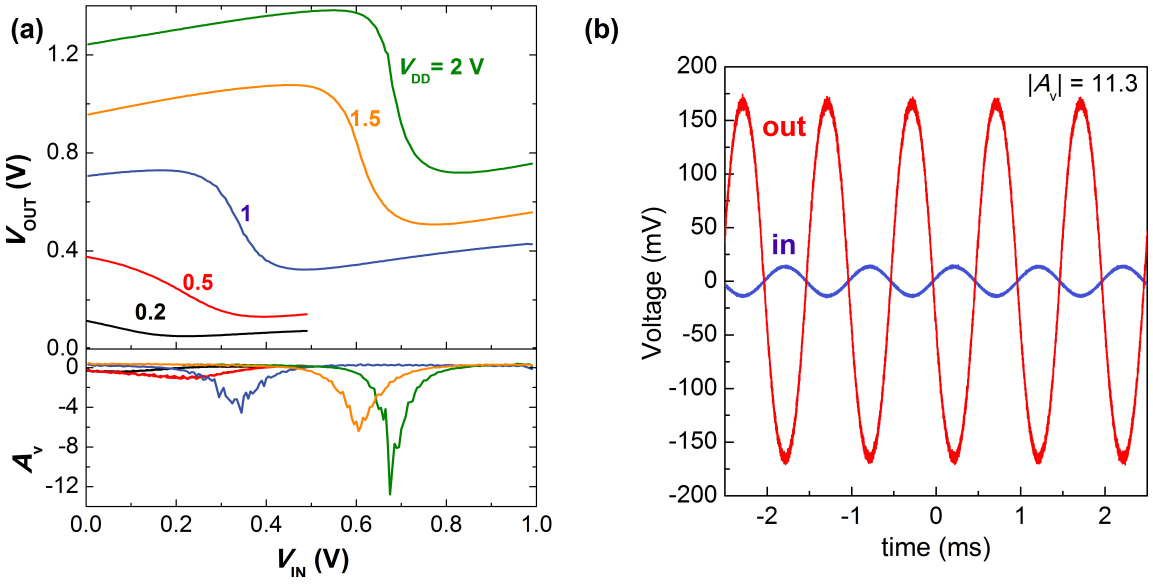

Figure 3.17: a) DC voltage gain for an inverter with L= 2 μm, W= 10 μm at different V_{DD}. The highest DC gain was $A_{\mathrm{v,DC}}$= -12.77 at V_{DD}= 2 V. b) AC response of the same inverter biased at V_{DD}= 3 V . Input signal has f =1 kHz and $V_{\mathrm{p\text{-}p}}$= 30 mV. The AC voltage gain is $A_{\mathrm{v,ac}}$= -11.3.

[4]Larger voltage gain values have been reported, but for much longer channels. [62]

Chapter 4

Graphene ROs and more complex circuits

After demonstrating the cascading of devices the next step consists of the fabrication of more complex integrated graphene circuits, like ROs. Oscillators are circuits capable of signal generation and are required for several applications such as timing in computer and control systems and for carrying information in communication systems [63]. Moreover, these circuits provide a direct estimation of the inverter propagation delay in a real circuit in which its input and output are loaded by other devices. This chapter will be devoted to the description of the operating principle of ROs and will provide both fabrication and characterization details. The scaling of these devices has been investigated and will be discussed.

4.1 Graphene ROs

A RO consists of an odd number of inverters, at least three, cascaded in a loop. At low frequency the loop provides a negative feedback because the output signal is fed back in the input with a phase shift of 180°, each stage introducing a phase shift of 180°. On top of this, each stage introduces an additional frequency-dependent shift, that can lead to a positive feedback and trigger oscillations.

In order to be implemented in ROs, graphene inverters must satisfy stringent criteria. First of all they must have identical characteristics in terms of total resistance, on/off ratio and doping level. They must exhibit a voltage gain $|A_{\mathrm{v}}| \geq 2$ and input-output signal matching to allow cascading. Moreover, in order to achieve high oscillation frequencies, the output resistance should be low. The three-stage ROs are the simplest to fabricate, because they require the lowest number of inverters, and they are also the fastest in this class of circuits.

4.1.1 Operating principle

The figure 4.1a represents a simplified schematic of the input impedence of one stage (i.e., an inverter) of the RO, with the input resistance modeled as $R_{\mathrm{IN}} \approx r_{\mathrm{d}} + R_{\mathrm{g}}$ where r_{d} is the output resistance of the loading inverter and R_{g} is the resistance of the gate metal.

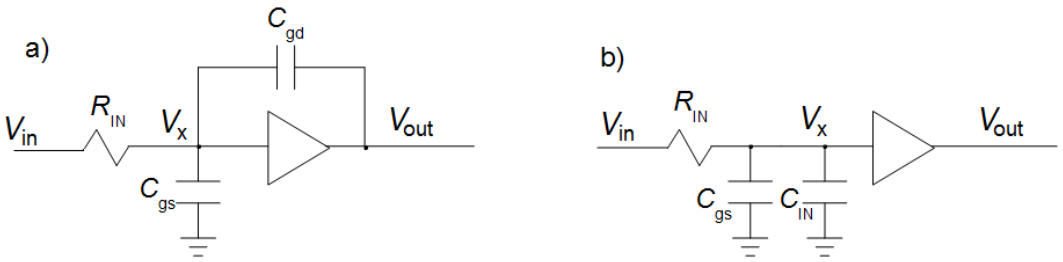

Figure 4.1: a) Schematic circuit of the input impedence of a single stage. The triangular symbol represents the voltage amplifier. b) Circuit after application of Miller's theorem. Here C_{gs} and C_{gd} are the gate to source and gate to drain capacitances, while $R_{\mathrm{IN}} \approx r_{\mathrm{d}} + R_{\mathrm{g}}$ where r_{d} is the output resistance of the loading inverter and R_{g} is the gate resistance.

According to the Miller's theorem the floating capacitance between gate and drain, C_{gd}, can be substituted by two equivalent grounded capacitances at the two ports of the inverter, with $C_{\mathrm{IN}} = C_{\mathrm{gd}}(1 + |A_v|)$ connected at the input, and $C_{\mathrm{OUT}} = C_{\mathrm{gd}}(1 + |A_v^{-1}|)$ connected at the output. Assuming $|A_v| \gg 1$, $C_{\mathrm{IN}} \gg C_{\mathrm{OUT}}$, and therefore C_{OUT} can be neglected which simplifies the circuit to that of figure 4.1b. Solving for the open-loop transfer function of a single stage $H_{\mathrm{i}}(s)$, with $s = \mathrm{j}\omega$, gives:

$$H_i(s) = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{x}}} \frac{V_{\mathrm{x}}}{V_{\mathrm{in}}} = A_{v,i} \frac{1}{1 + sR_{\mathrm{IN}}C_{\mathrm{T}}}$$

and

$$H_i(\omega) = \frac{A_i(0)}{1 + j\frac{\omega}{\omega_{0,i}}}$$

with $C_{\mathrm{T}} = C_{\mathrm{gs}} + C_{\mathrm{IN}}$ and $A_{\mathrm{v,i}}$ approximated by $A_{\mathrm{i}}(0)$ (the DC voltage gain of the inverter), the characteristic frequency is $\omega_{0,i} = (R_{\mathrm{IN}}C_{\mathrm{T}})^{-1}$. The open-loop transfer function of the three stages cascaded is the product of the transfer functions of each stage, resulting in:

$$H(\omega) = \frac{V_{\mathrm{out}}(\omega)}{V_{\mathrm{in}}(\omega)} = \frac{A_i^3(0)}{\left(1 + \frac{j\omega}{\omega_{0,i}}\right)^3} \tag{4.1}$$

Equation (4.1) represents the gain of a three-stage circuit, defined as the ratio between input and output voltage phasors. From this expression we note that, in addition to the 180° phase-shift introduced by the three inverters at low frequencies, there is a frequency-dependent shift added to the signal. The RO (i.e., the closed-loop circuit) will oscillate if

the output signal is fed back into the input with a 360° (or zero) phase-shift. This occurs at the frequency of signal (or of a noise component) at which each stage provides additional 60° phase-shift. The frequency that fulfills this condition can be obtained from:

$$\tan^{-1}\frac{\omega_{\mathrm{osc}}}{\omega_{0,i}} = 60^{\circ} \tag{4.2}$$

which results in:

$$\omega_{\mathrm{osc}} = \sqrt{3}\omega_{0,i} \tag{4.3}$$

where $\omega_{0,i} = f_{-3\mathrm{dB,i}}$, i.e. the frequency at which the voltage gain of each stage drops of 3 dB from the DC value $A_{\mathrm{i}}(0)$ [64]. From (4.1) it is possible to calculate the minimum voltage gain per stage which provides that $H(\omega) = 1$, that is $|A_i(0)| = 2$ for a three-stage RO (and $|A_{\mathrm{i}}(0)| = 1$ for larger number of stages). According to this derivation, if the gain of each stage is $|A_i(0)| = 2$, a noise component at frequency ω_{osc} at the input would be transmitted with the same amplitude at the output.

The closed-loop transfer function of the RO (that takes into account the feedback) is then expressed as [64]:

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{H(\omega)}{1 - H(\omega)} = \frac{A_i^3(0)}{\left(1 + \frac{j\omega}{\omega_{0,i}}\right) - A_i^3(0)}$$

From which the output voltage, i.e. the noise component amplified within the loop, can be derived [64]:

$$V_{\mathrm{out}}(t) \approx \exp\left(\frac{|A_{\mathrm{v}}| - 2}{2}\omega_0 t\right)\cos\left(\frac{|A_{\mathrm{v}}|\sqrt{3}}{2}\omega_0 t\right). \tag{4.4}$$

The expression (4.4) describes a growing sinusoidal waveform arising from a noise component with frequency $\omega_{osc} = |A_v|\sqrt{3}\omega_0/2$. In the case of $|A_v| = 2$ this simply reduces to $V_{\mathrm{out}}(t) = \cos\left(\sqrt{3}\omega_0 t\right)$ at the frequency calculated in (4.3). However, this is a very unlikely situation. It is more realistic to consider $|A_v| > 2$, thus, according to equation (4.4), the amplitude of the oscillation can exponentially grow to infinity. In reality, the amplitude is limited by the saturation of the amplifying stages. Figure 4.2 helps to explain this concept. Consider the amplified noise component fed back at the input of the RO (i.e., in the first inverter of the loop). If the amplitude of the wave is large the linear model fails and the wave is cut and distorted by nonlinear effects. The maximum amplitude in a CMOS inverter-based RO is set by the rail-to-rail operation, but in a graphene inverter we have seen (in section 3.2.1) that the highest voltage swing is limited to about 66% of V_{DD}.

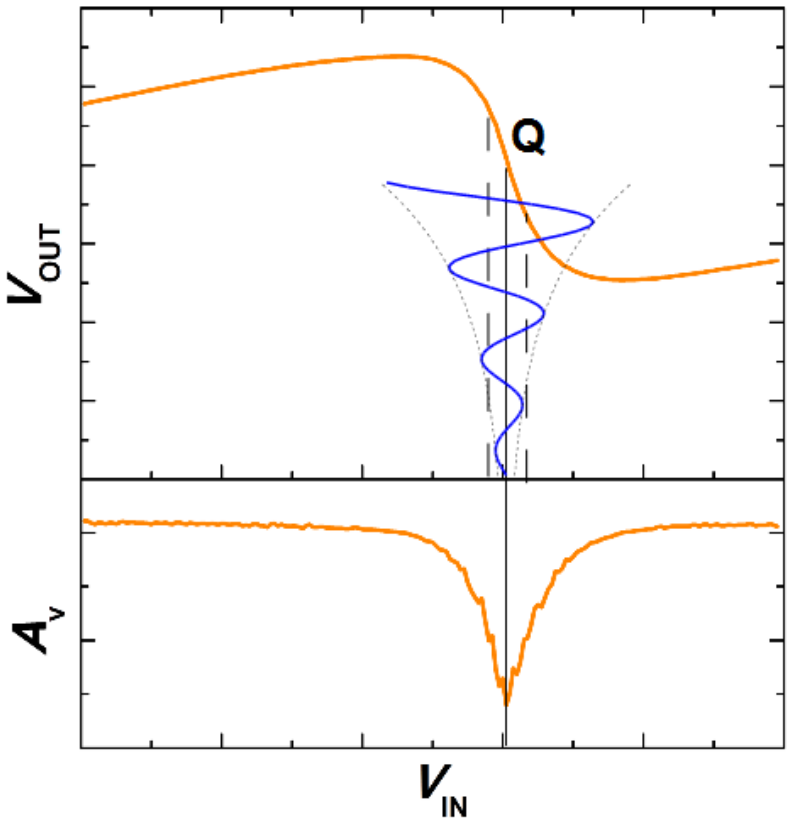

Figure 4.2: Transfer curve (orange) of an inverter representing one of the stages of a RO. When the noise component (blue signal) is superposed to the DC offset of the inverter, it exceeds the linear range of operation and its amplitude is limited by the gain of the inverter.

This small-signal analysis can predict the conditions at which oscillation begins. This model can be applied to the system as long as the signal amplitude is small enough to justify the linear approximation. When the signal starts to propagate in the loop, it grows in amplitude until it saturates and reaches a "steady state" (an AC steady state). In this regime a large signal model is required to correctly describe the RO operation. Derivation of large signal model for graphene ROs can be found in Appendix A.

4.1.2 Fabrication of graphene ROs

There are some important aspects that should be taken into account in order to design a RO operating at high frequency. The measurement setup, such as the external coaxial cables connecting input and output described in section 3.3, introduce an extra capacitive load that severely limits the frequency response of the ciruit. In general, every transmission line is associated with extra resistances, capacitances and inductances that are not negligible at high frequencies because they introduce a signal-delay that causes reflections and distortions

[65]. Moreover the length of the cables, being much longer than the wavelength of the signal, slows down the transmission. These problems can be solved by replacing the cables with internal connections, as shown in the schematic and in the corresponding optical image of the circuit with colored dashed lines, figure 4.3.

The gates are fabricated with a tilted evaporation process of an Al/Ti/Au stack (32/1.4/9 nm). The angle between the surface of the sample and the direction of evaporation is 45° to ensure the formation of a slope on one side of the gates (see figure 4.4, in violet). Electrodes are fabricated with standard evaporation of Au (100 nm), i.e. with the surface of the sample perpendicular to the direction of evaporation, and this results in almost vertical edges on all sides (figure 4.4, in yellow). The desired input/output connection is provided by the gold-terminated sloping edge of the gates which allows a good ohmic contact. In order to implement this step inside the process, it was not possible to overlap gates and electrodes, as this would result in short circuits.

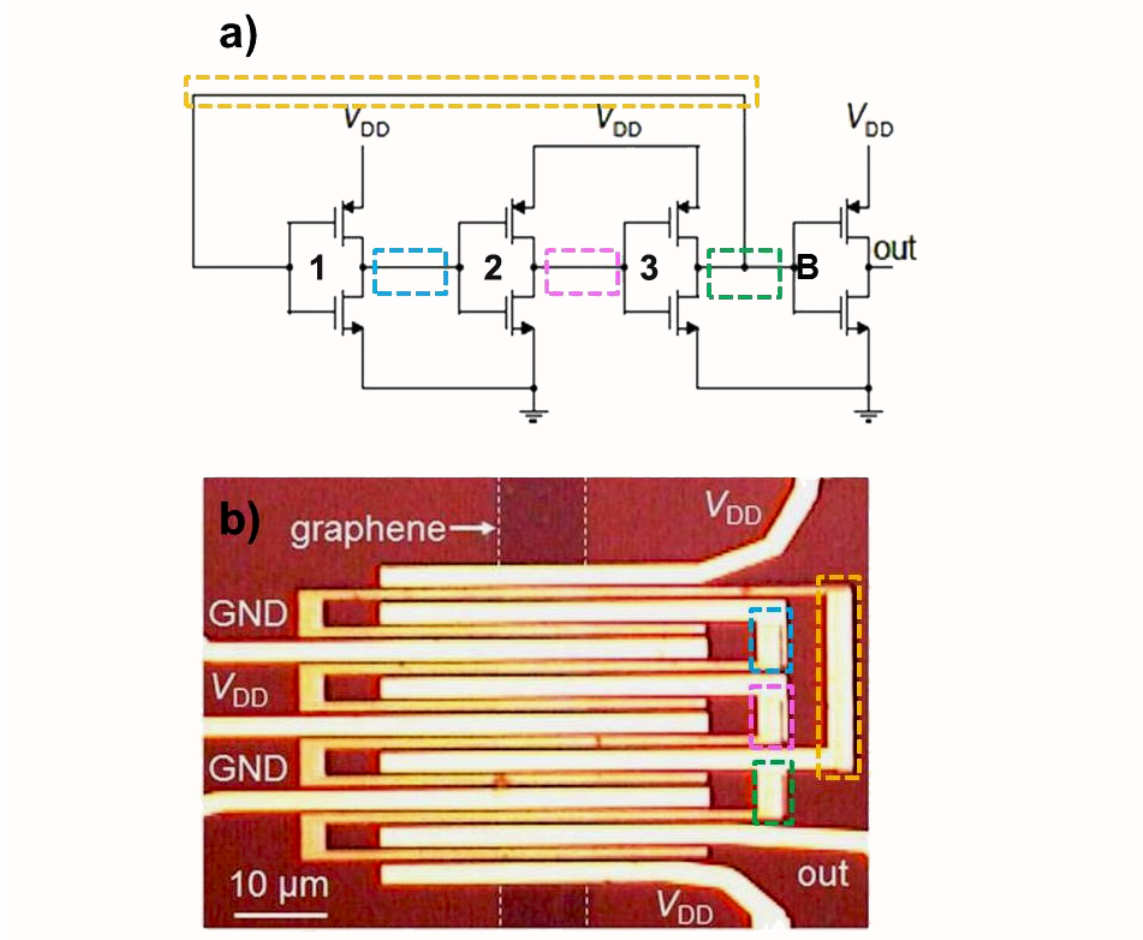

Figure 4.3: a) Circuit schematic of a three stage RO with an additional buffer stage B. b) Optical image of the RO. The dashed lines indicate respectively: blue) out 1-in 2, pink) out 2- in 3, yellow) out 3- in 1, green) out 3-in B connections.

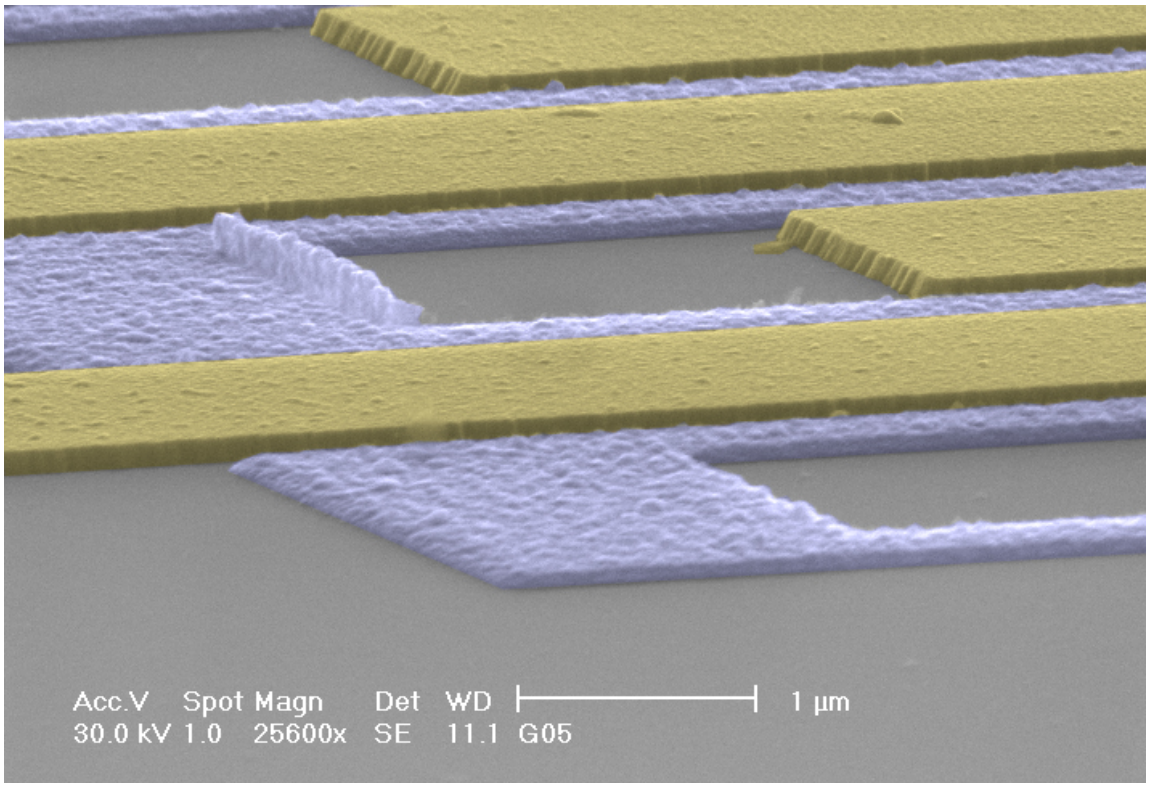

Figure 4.4: SEM image (in false colors) of gates (violet) and electrodes (yellow). The gates have a slope in the direction of the tilt (from left to right) while the profile of electrodes is more abrupt.

Apart from the inverters connected in a loop, the design presented here has an additional stage, labelled by B in figure 4.3a), which is a buffer stage connected to the output of the last inverter of the loop. The third inverter will consequently have a FO of 2. The increased FO slows down the ring, but this additional capacitive load is lower compared to the load of the measurements setup, thus the buffer stage allows faster operation. Both buffered and unbuffered ROs have been fabricated [24]. For comparison an unbuffered RO with $W = 10$ µm, $L = 3$ µm and $t_{ox} = 75$ nm oscillates at $f_o \sim 20$ MHz while a buffered RO with same characteristics oscillates at $f_o \sim 200$ MHz. Since unbuffered ROs show worse performances, only buffered ROs will be discussed here.

4.1.3 Characterization of ROs

To reduce parasitic capacitances and gate resistance, graphene ROs have been fabricated without gate pads, see figure 4.3. However, when the voltage supply V_{DD} is large enough to provide $|A_v| > 2$ for each stage, oscillations can start (a large signal model to describe the oscillation mechanism is presented in Appendix A). If devices show intrinsic doping, a common back gate voltage can be applied to restore GFETs neutrality, allowing signal matching. In order to characterize a RO, a suitable V_{DD} (i.e., large enough to provide $|A_v|$

> 2) is applied to the inverters, and the back gate voltage is swept to tune the inverters and initiate oscillations.

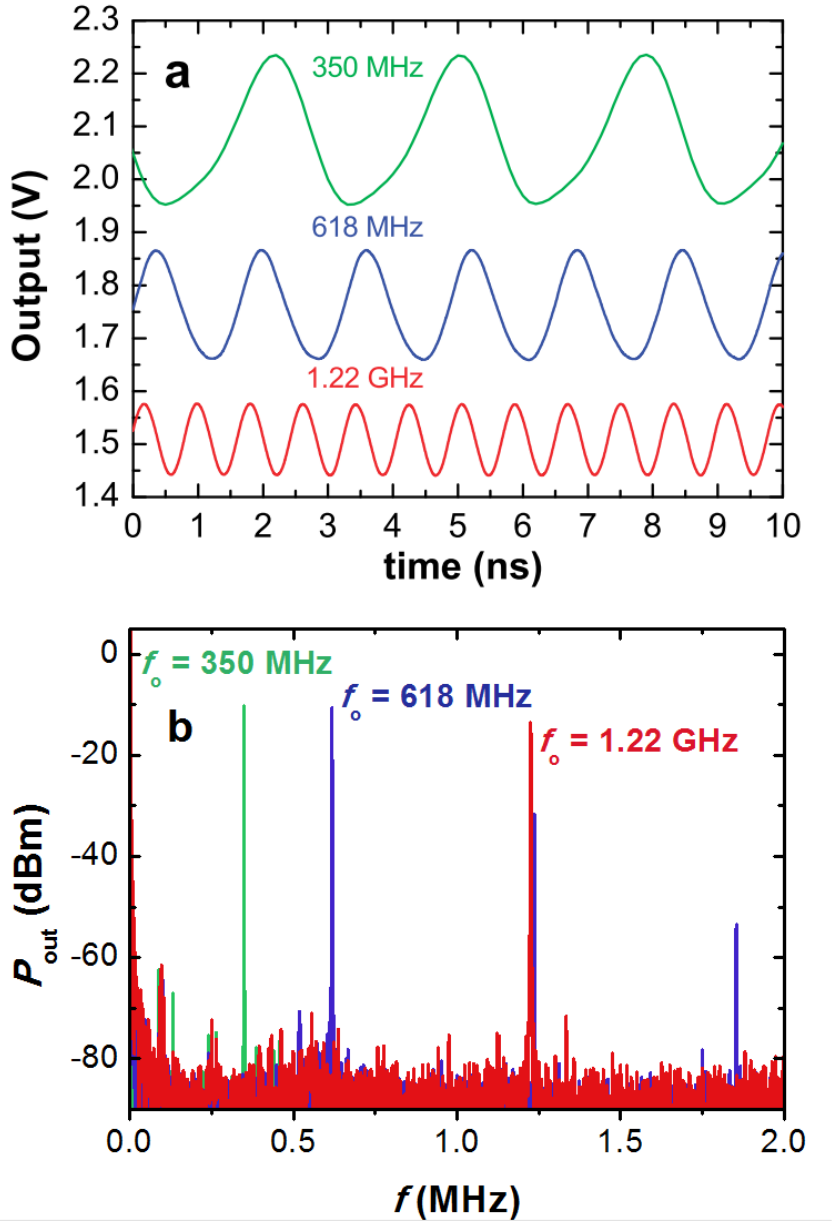

Figure 4.5: a) Signal and b) Fourier transform of ROs with different gate lengths. From reference [24].

The output signal is acquired by Agilent Infiniium DSO9404A (4 GHz bandwidth) through a high input impedance Agilent 1158A (100 kΩ||0.8 pF) active probe connected to the output pad. A high input impedence probe is required because the standard 50-ohm terminated AC probes would load the output, interfering with the device characteristics (see Appendix B). Figure 4.5 shows the signals recorded for three ROs having different gate

lengths.

The scaling of oscillation frequency with the gate length is shown in figure 4.6. The oscillation frequency is the inverse of the total delay time obtained by summing delays of each stage in the loop, for which the expression is given in Appendix A, equation (A.14). The delay time is related to the time constant of the circuit (A.1) which, taking into account the parasitic resistances of the circuit, can be expressed as:

$$\tau_i \propto R_{\mathrm{O}} C_{\mathrm{G}} = \left(\rho_{\mathrm{ch}} \frac{L}{W} + 2\frac{\rho_{\mathrm{ch}} L_{\mathrm{a}}}{W} + \frac{\rho_C}{W} + \rho_{\mathrm{M}} \frac{l'}{w' t_{\mathrm{M}}} \right) LWC_{\mathrm{OX}} \tag{4.5}$$

where ρ_{ch} is the channel resistivity, ρ_{C} is the contact resistivity, L_{a} is the acces length (the distance between gate and electrodes), ρ_{M}, t_{M}, l' and w' are respectively the metal resistivity, thickness, the length and width of the electrodes from the contact (the point of carrier injection in the channel) to the pads. The first term in brackets corresponds to the channel resistance, second, third and fourth represent respectively the access, contact and interconnection resistances.

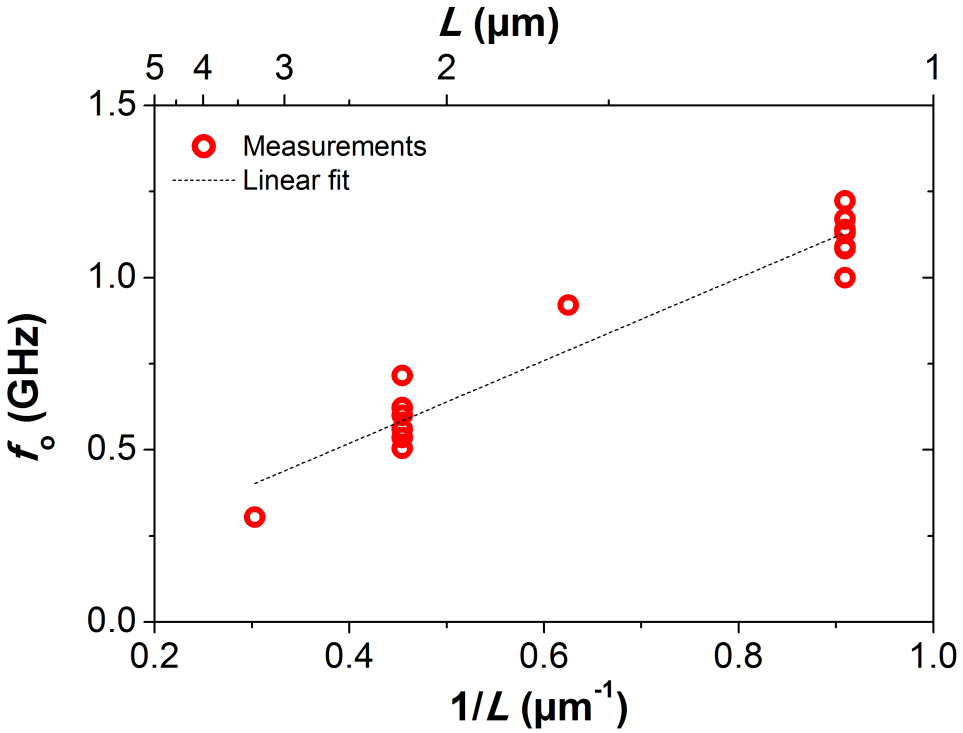

Figure 4.6: Scaling of oscillation frequency with actual gate length for ROs with W = 10 µm and L_{a}= 0.5 µm.

The interpolation of data collected for ROs with gate legth from 0.9 to 3.3 µm (figure 4.6) shows that in this range the oscillation frequency scales linearly with L^{-1}. At first

sight, since both channel resistance and geometric gate capacitance scale down with L, a L^{-2} dependence is expected. However the additional components of the total resistance, such contact and interconnection resistances, do not scale with L. Moreover the gate delay is influenced by other parasitic components, such gate fringe capacitances and capacitances between source/drain contacts and the substrate, that do not depend on L, thus the gate delay scales slower, tipically $\tau \propto L$ as found from data interpolation.

The dependence of the oscillation frequency on the bias has been investigated. For devices with $L > 1$ µm it is possible to demonstrate that the oscillation frequency increases by increasing V_{DD}. This behavior is expected because at higher biases the output conductance of the inverter increases (output resistance decreases). This dependence, however, is weaker compared to Si CMOS, because the output conductance in graphene has a weaker dependence on the voltage bias (in graphene the output conductance never drops to zero, being limited to the minimum value of conductance at the Dirac point). The voltage swing increases with V_{DD}, because at higher bias the voltage gain is higher. For the RO shown in figure 4.7, the change of oscillation frequency with supply voltage is $\sim 5.6\ \% \ f_{\mathrm{o}}/V_{\mathrm{DD}}$ on average. This is about 7, 21, and 51 times smaller than that of ROs based on Si CMOS [24], MoS_2 [44], and CNTs [66], respectively. In applications requiring dynamic frequency and voltage scaling[1] to throttle down digital circuits, such a weak dependence could be a disadvantage. However, the insensitivity of graphene ROs to power supply noise could represent an important advantage in applications in which frequency stability is required, e.g., for clock generation in high-speed digital systems.

[1] Dynamic frequency and voltage scaling is a technique used to preserve the dissipated power, especially in mobile devices. The transient dissipated power is defined as $P_{\mathrm{tr}} = C_{\mathrm{out}} V_{\mathrm{DD}}^2 f$ where $\mathrm{C_{out}}$ is the output capacitance of the inverter and f is the switching frequency. By reducing either V_{DD} or f the transient power decreases proportionally[67].

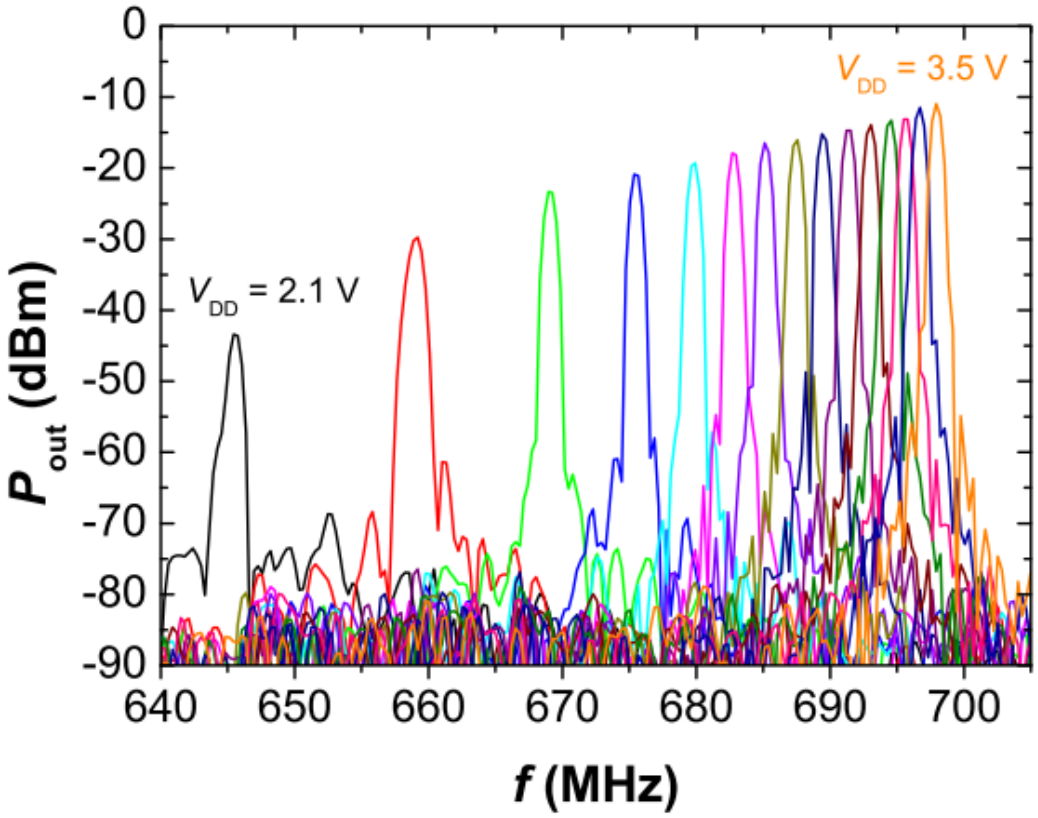

Figure 4.7: Dependence of oscillation frequency on the supply voltage V_{DD} of the inverters comprising the RO (L =2 μm and W =10 μm) at V_{BG} = 89 V. From left to right: V_{DD} = 2.1 to 3.5 V in steps of 0.1 V. From reference [24].

In short-gate devices the oscillation frequency is relatively unstable, exhibiting time variation. This drift, usually towards lower frequencies, is superposed to the bias-related drift that becomes undetectable. In small devices L is reduced but L_{a} is kept constant, leading to a greater influence of the ungated acces region on device characteristics. These ungated regions of the channel are more sensitive to the external impurities, that are attracted towards graphene surface when the back gate voltage is increased. This dynamical doping is responsible for the drift of the Dirac point of the GFETs that changes the gain of the inverters and modify the oscillation frequency (see figure 4.8).

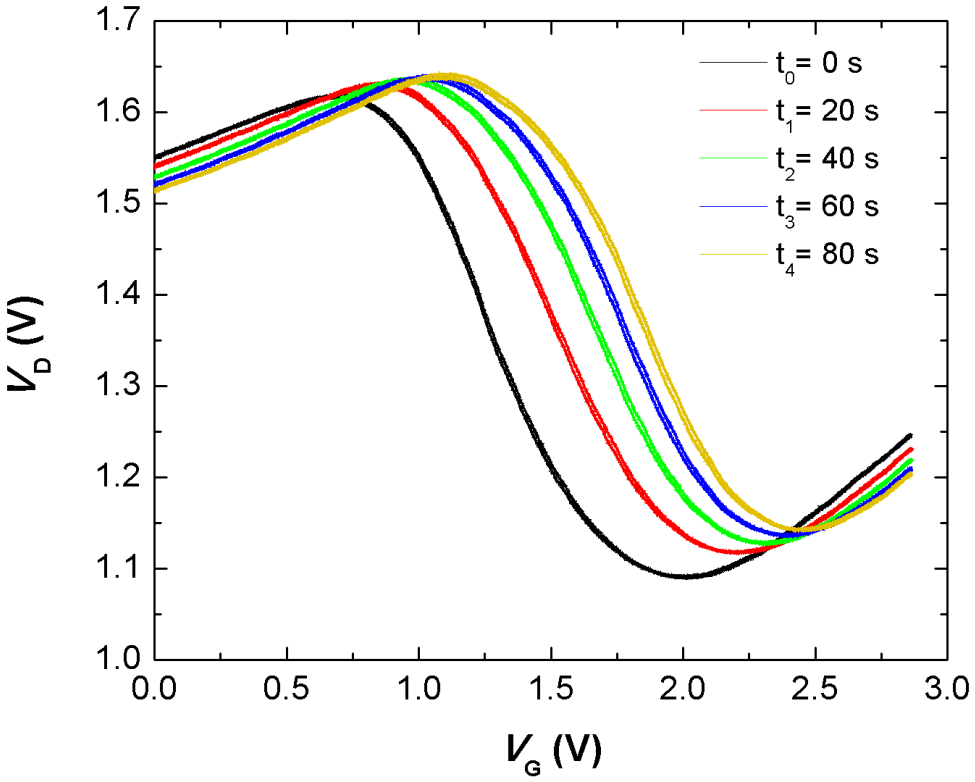

Figure 4.8: Drift of the transfer curves of a graphene inverter with time at $V_{\mathrm{BG}} = 160$ V and $V_{\mathrm{DD}} = 2.5$ V. After the first curve (black; 0 s) was measured, subsequent curves were measured at 20 s intervals. The drift is a consequence of the drift of the Dirac point to larger gate voltages, which is more prominent at large back-gate voltages. The drift detunes the RO by introducing in/out mismatch, which stops the RO from oscillating after some time.

4.2 Design improvements and device scaling

The access, contact and interconnects resistances represent parasitic elements that introduce a voltage drop between the bias injection point on the pad and the channel end, leading the actual voltage drop on the channels to be lower than V_{DD}. The expression (4.5) shows that, apart from reducing the gate length L, there are several parameters that is possible to tune in order to reduce the output resistance and capacitance, and therefore to increase device speed. The most intuitive is a "geometrical approach" that consists in modifying the design to minimize access length and metal line resistance. A second issue is related to the reduction of contact resistance, which involves a deeper investigation because this resistance is influenced by several factors, including material quality and interfaces [68, 69], and thus requires to perform several tests to determine which metal combination is more

suitable for CVD graphene on Si/SiO_2 substrate.

4.2.1 Design optimization

Regarding the geometrical approach several design improvements have been considered. The initial design shown in figure 4.9a has been modified increasing the contacts width (figure 4.9b) and decreasing the output pad size (figure 4.9c) to reduce the resistance of interconnects and the output capacitance (see Appendix B). The influence of these modification is expected to be minor, thus has not been quantified directly. However, from a simple analysis of (4.5), it is expected that the new design (figure 4.9c) leads to better performances than (figure 4.9a).

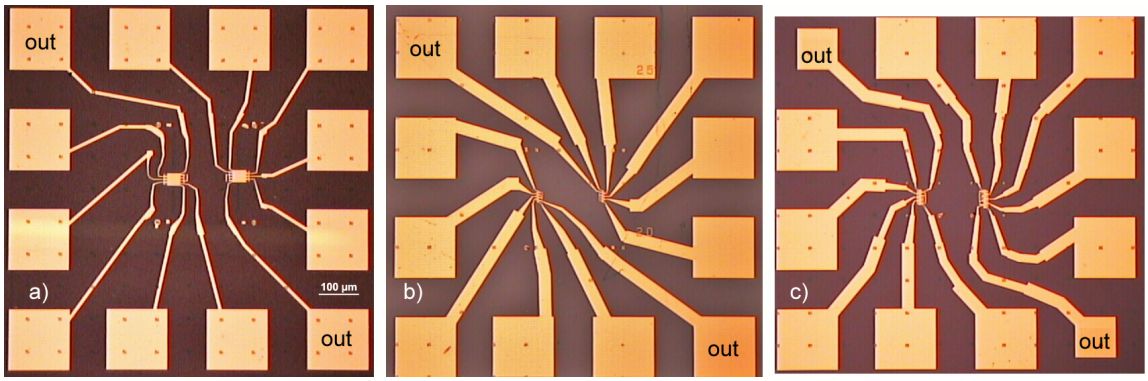

Figure 4.9: Optical images of two graphene ROs: a) design with narrow electrodes, b) design with wide electrodes, c) design with wide electrodes and small output pads.

To further improve the design, the access length have been reduced from 0.5 µm (figure 4.10a), to 0.25 µm (figure 4.10b). Note that these values refer to the designed access length, which is larger than the actual L_a, due to the proximity effect that causes the exposed electrodes to be wider (see figure 4.11). Moreover the contact length has been reduced to the minimum size compatible with channel dimensions (figure 4.10c).

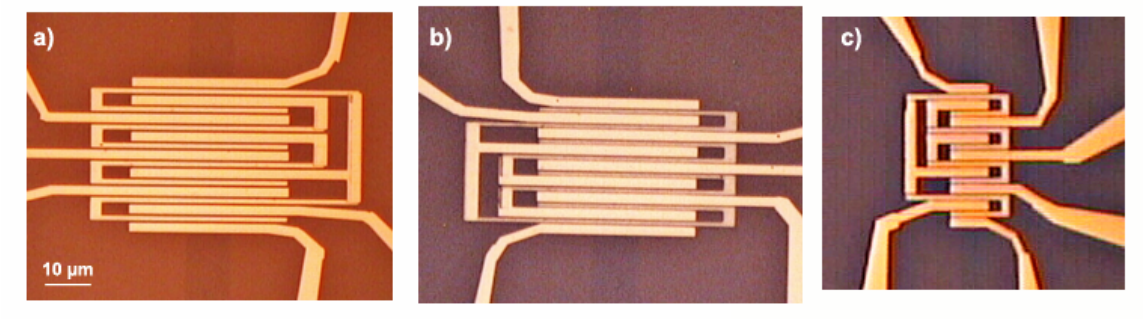

Figure 4.10: Optical image of RO channels with $L = 1$ µm: a) $W = 10$ µm, $L_a = 0.5$ µm; b) $W = 10$ µm, $L_a = 0.25$ µm; c) $W = 5$ µm, $L_a = 0.25$ µm and shrinked connections.

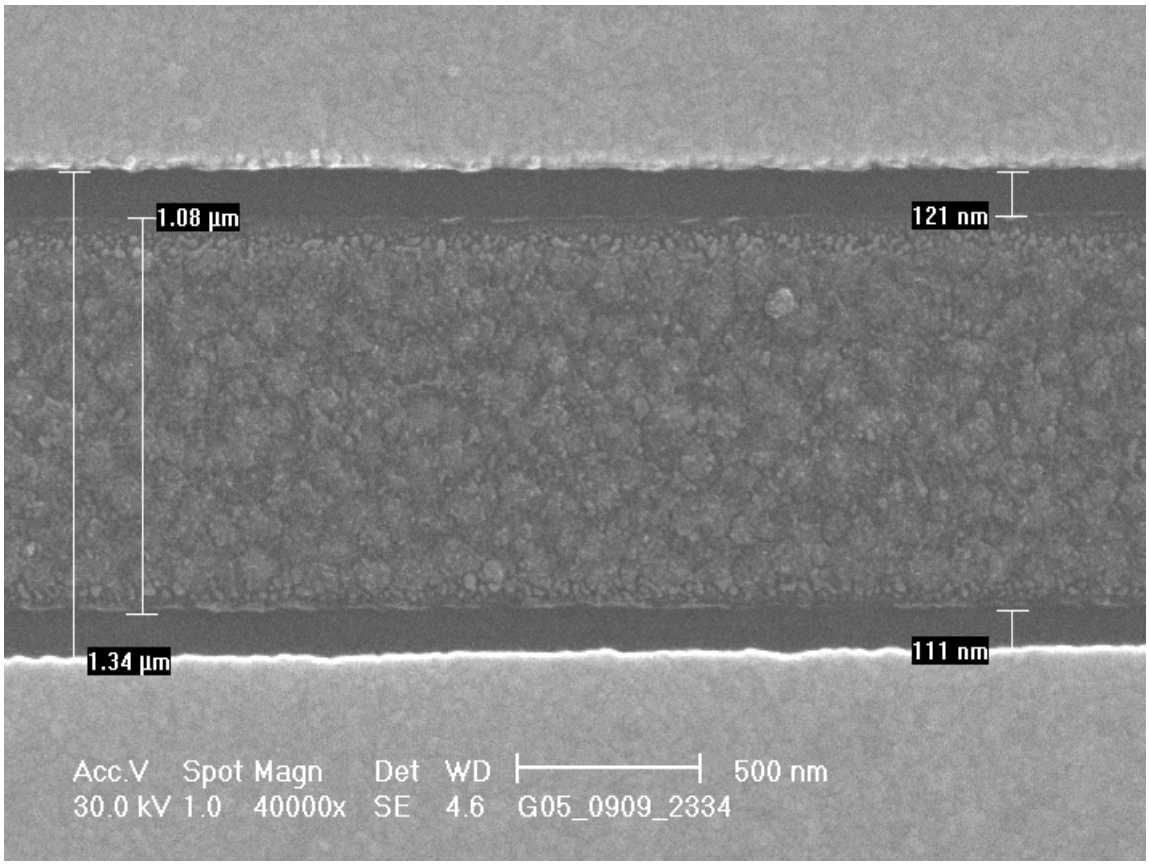

Figure 4.11: SEM image of a RO with nominal $L = 0.9$ µm and $L_a = 0.25$ µm. Actual dimensions are written on scale bars.

The effect of access length scaling will be discussed in section 4.2.3.

4.2.2 Investigation of contact resistance

Graphene-metal contact is similar to the ohmic contact that occurs between two metals, but limited DOS of graphene implies that the charge transfer occurring to balance the Fermi level at the equilibrium extends along the channel for some extent. The nature of graphene-metal contact has been deeply investigated because it represents one of the major issues in the development of high performance GFETs, since the contact resistance is about an order of magnitude higher than in conventional Si CMOS, thus becoming the crucial parameter for device optimization [70, 21].

When a metal and a semiconductor are put in contact, a Schottky barrier builds up, with height corresponding to the difference between the metal work function and the electron affinity of the semiconductor, namely $\Phi_B = \phi_M - \chi$. A depletion layer with a certain extention is formed in the semiconductor due to its limited carrier density. In contrast to this, a contact between two metals shows no potential barriers. The work functions difference causes the electrons to be transferred directly through the interface, but the

small redistribution of the electron cloud can screen the potential difference due to the high carrier density. In turns the vacuum level changes abruptly at the interface [5].

The contact between graphene and metal represents an intermediate situation. Graphene has no bandgap, but as semiconductors it has a limited DOS. This means that even a very small amount of electrons transferred through the interface can shift the Fermi level of graphene significantly (figure 4.12b), forming a dipole layer with a large screening length. Moreover it has been demonstrated that the carrier injection from metal to graphene occurs through the contact edge and not through the whole contact area [71]. The reason for this behavior is that, despite the high charge carrier mobility in graphene, its limited DOS causes a high-resistance path for the electrons, which move easier inside the metal rather than in the channel (figure 4.12c).

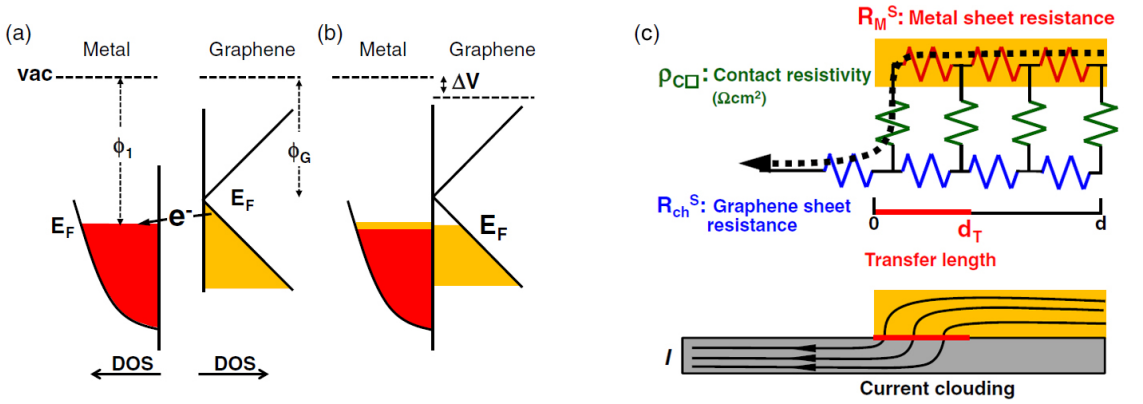

Figure 4.12: Graphene-metal interface a) before the contact; b) after the contact. c) Transmission line model for graphene-metal contact. Taken from reference [71].

Several works have reported that graphene-metal contact properties cannot be directly inferred from the simple calculation of the work function difference, since factors like substrate-induced or process-induced doping of graphene have a fundamental impact on the resulting DOS below the contact [68]. Graphene transferred on Si/SiO_2 substrate has a different doping level (tipically much lower) than graphene grown directly on SiC. This substrate-induced doping determines the Fermi level position in graphene, influencing the nature of graphene-metal contact that will result either in a p-n junction characterized by an extra resistance or in a p-p or n-n type of contact with a resistance proportional to the DOS below the contact [72]. It is important to notice that even the gate voltage can influence the contact resistance, despite some works reporting otherwise [73], because it varies the position of the Fermi level in graphene, thereby changing the density of states available for carrier injection. This variation, however, is minor compared to the channel resistance modulation and in first approximation contact resistance can be treated as a constant term added in series to the channel.

Since it is difficult to determine a priori the best metal for contact, TLM stuctures have been fabricated with several material combinations to test their performances. All contacts

have been fabricated by e-beam lithography on PMMA followed by e-beam evaporation of the metals, in order to identify the material that better fits this specific process. It has been shown that the process itself represents another important source of variability. The lithography step introduces the variable which is the resist (different for optical and e-beam lithography) that leaves some residues on the channel even after development, doping the channel. Moreover, the metal deposition with different processes (sputtering, ALD, evaporation) leads to contacts with different cristallinity and thus different work functions [69].

Au has one of the lowest resistivity value ($\rho = 2.4 \cdot 10^{-8}$ Ωm) and is a highly inert material that does not oxidize in air, so it has been used in all tests as protective metal layer. Several combinations of Au, Ti/Au, Ni/Au, Pd/Au and Pt/Au have also been investigated. Ti is often used as adhesion layer below Au (because it easily oxidize providing a stronger interaction with the substrate), deposited in a thin layer of 1-10 nm thickness. However we found that contacts made of pure Au have the lowest resistance of all tested combinations, providing a contact resistivity of $\rho_c \approx 190$ $\Omega\mu$m extracted from two-probe and four-probe measurements on TLM structures. The TLM structures consist of a pattern of electrodes, with increasing spacing between two consecutive contacts, on which it is possible to make two and four-probe measurements. From the formula:

$$R_{ch} = R_{TOT} - 2R_c$$

where R_{TOT} is the value obtained from two-probe and R_{ch} the value obtained from four-probe measurements, it is possible to extract directly the contact resistance. Figure 4.13 shows contact resistance values, normalized by channel width, extracted at the Dirac point. Since different metals introduce different doping in graphene, the Dirac point value has been chosen as a reference for meaningful comparision. With Ni contacts it has been difficult to obtain a relevant statistic, thus ROs have been fabricated to directly compare their performances with that of ROs having Au-electrodes, as discussed in the following section.

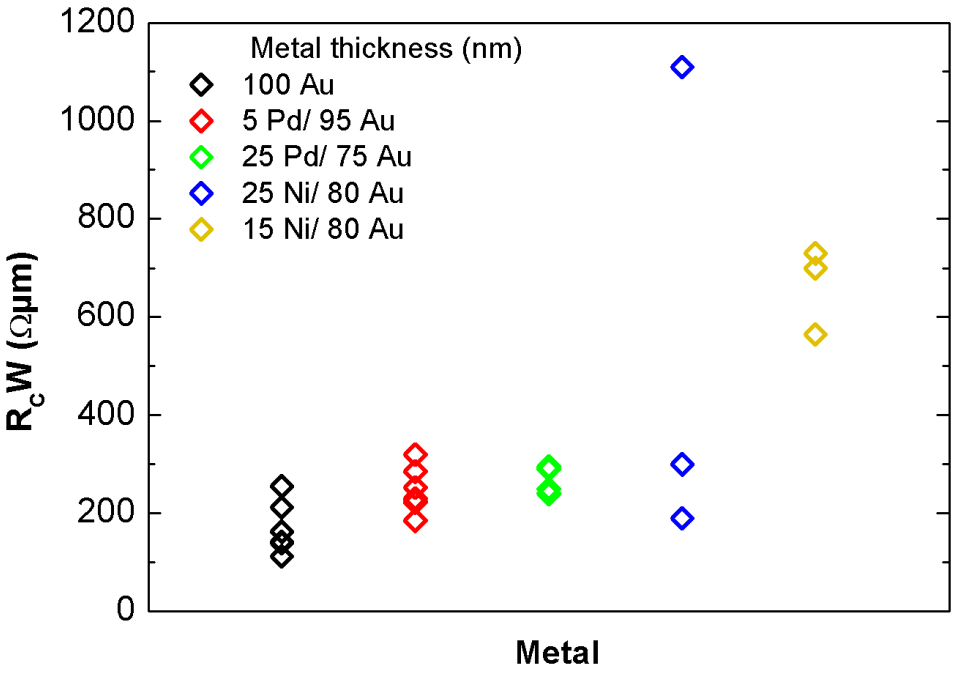

Figure 4.13: Contact resistance at the Dirac point for different metals.

4.2.3 Scaling of lateral dimensions

The dimensions of graphene ROs have been scaled to study the influence of parasitics on the oscillation frequency. Since the gate dielectric is formed from spontaneous oxidation and its thickness is not controllable, the vertical dimensions of the GFETs have been kept constant, with a EOT = $t_{AlO_x}(\varepsilon_{SiO_2}/\varepsilon_{AlO_x})$ ≈2.5 nm. The metal line thickness, t_M, has been increased to reduce the parasitic resistance of interconnects. The effect of larger thickness can be seen by comparing blue with purple circles in figure 4.14, corresponding to a set of devices in which t_M was varied from 75 to 100 nm while the other parameters were kept constant. Despite the large scattering in purple circles dataset, they also exhibit the largest f_o for any gate length tested, as expected.

The lateral scaling has involved channel length L, width W and access length L_a (see figure 4.10c), data are plotted in figure 4.14. By keeping the other parameters constant the frequency scales as $1/L$, as discussed in section 4.1.3, a trend that has been confirmed for all investigated samples. At smaller access lengths the total resistance is smaller, see (4.5), and thus the oscillation frequency is higher, as confirmed by comparison of black and red circles in figure 4.14, where the only parameter changed is L_a. Measurements also demonstrate that channel width reduction leads to an increase in the oscillation frequency. The effect of this operation may be not so evident from (4.5), because a decreased channel (i.e., gate) width reduces gate capacitance but at same time increases channel resistance, so the two contributions are expected to counterbalance. However, the resistance associated with metal contacts is not affected by the scaling of channel width, so that the contribution

of capacitance on this term cannot be neglected. We found from experiments that by reducing channel width from 10 to 5 µm the oscillation frequency increases, as can be seen comparing black and blue circles in figure 4.14. However, further reduction down to 2 µm (light blue circle) leads to worse performances (only one data point is reported on the plot, corresponding to the only RO with $W = 2$ µm exhibiting oscillations). This behavior may depend on the fact that CVD graphene contains a lot of domains and a minimum channel size is required to preserve conduction, but this phenomenon has not been further investigated. Finally the performance of Ni/Au contacts have been compared to those of pure Au contacts, keeping constant the total t_M . The comparison between blue and green circles and between yellow and purple circles confirm the results obtained by TLM investigations, with pure Au electrodes providing the lowest contact resistance and consequently the highest device speed.

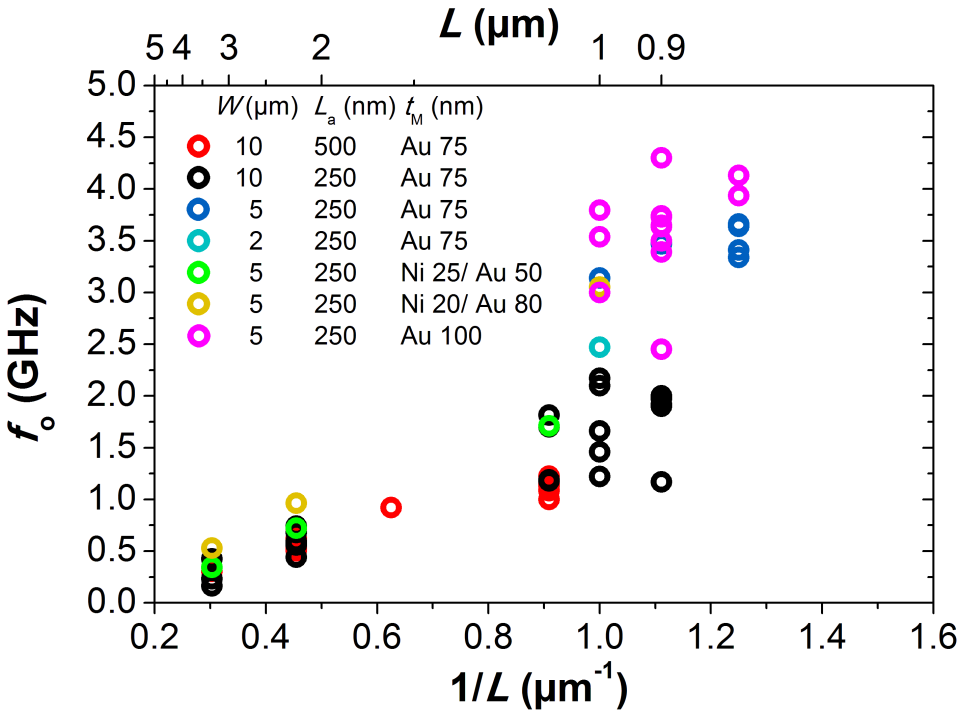

Figure 4.14: Oscillation frequency vs. actual gate length for ROs made of different metal S/D contacts.

In chapter 5 the small-signal FOMs f_T and f_{max} will be introduced as typical standards for evaluating device performances. It is worth to point out that those FOMs are measured in idealized conditions and valid only in the small-signal regime. An estimation of signal propagation delay in a real device, which is valid also in the large-signal regime, can be provided by the CV/I intrinsic gate delay metric. The intrinsic gate delay represents the

time required to increase the voltage of the gate capacitor through the large-signal voltage swing $V_{\text{p-p}}$ when charged at a constant drain current [74]. This metric has been widely used to demonstrate the scaling of Si CMOS, reaching a value below 1 ps at the 22 nm node [75]. However CV/I cannot be directly measured but only calculated and, as f_{T} and f_{max}, is only a single-transistor metric that does not reflect the real transistor delay in a circuit. Therefore, the FO1 inverter delay τ_{FO1} in ROs has been introduced by the ITRS roadmap since 2009 as main speed metric for circuit scaling. The FO1 gate delay represents the delay of an inverter that is loaded with another identical inverter. Its value for Si CMOS is currently 2.2 ps at the 22 nm node [75]. Figure 4.15 shows the scaling of FO1 gate delay for the highest-performances graphene devices (dataset represented with purple circles in figure 4.14) and Si CMOS (from Intel [75]). τ_{FO1} for graphene ROs can be determined from the oscillation frequency f_{o} as $\tau_{\text{FO1}} = 1/f_{\text{o,FO1}} = 0.82/f_{\text{o}}$, where $f_{\text{o,FO1}}$ is the oscillation frequency of a corresponding unbuffered RO, i.e. with FO = 1. The factor 0.82 takes into account the FO2 of the third inverter in buffered ROs [24]. Note that we are not able to measure $f_{\text{o,FO1}}$ without loading the RO with the measurement setup.

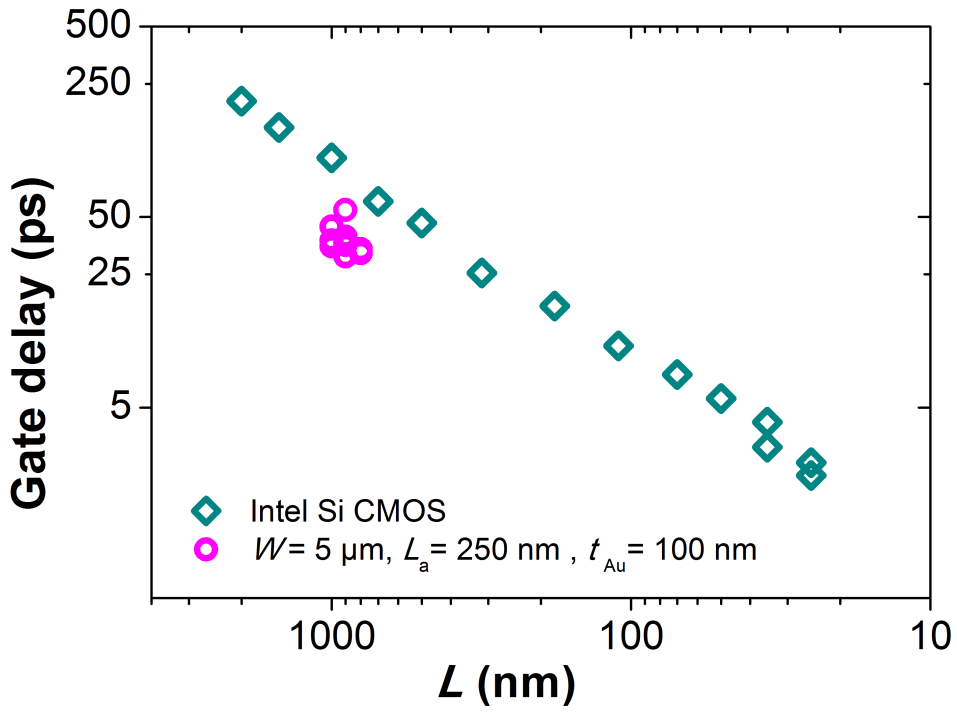

Figure 4.15: Gate delay per stage: comparison between current Si CMOS technology and the best graphene ROs fabricated.

Figure 4.15 demonstrates that graphene ROs have the capability to scale faster than Si CMOS at the same gate length, due to the larger charge carrier mobility in graphene.

However, while the scaling in Si CMOS has been demonstrated down to the 22 nm node (corresponding to $L = 34$ nm [17]), the current study has shown scaling only down to 0.7 µm design length (corresponding to $L = 0.8$ µm), where the highest f_o reported was 4.3 GHz, corresponding to a FO1 delay of 31 ps.

The scaling is currently limited by the high contact resistance that rapidly reduces the voltage gain in short-channel devices, becoming the dominant contribution on total resistance. This evidence has been demonstrated by measuring the transfer characteristics of graphene inverters with actual $L = 0.8$ µm, exhibithing a voltage gain $|A_v| \approx 2$, which is not enough to provide working ROs if device-to-device variations are taken into account.

4.3 Applications of graphene ROs

ROs can be used to perform analog and digital operations such as signal mixing and amplitude modulation, functionalities that are used in common applications.

Several demostrations of graphene-based analog modulators and mixers have been performed [76, 77, 20, 78], aiming to show the potential of graphene in high-frequency analog electronics. The disadvantages of using a semimetal like graphene in digital circuits have been acknowledged at the beginning of this work, however, it is a common opinion [21, 6] that graphene can suit analog electronics demand. For analog operations like signal mixing and modulation, transistors do not have to exhibit an off-state, and voltage gain is not strictly required. However, the gain is necessary both for signal transmission and for signal generation. Thereby the target of this section is the demostration of fully-integrated graphene circuits for applications in analog electronics.

4.3.1 Graphene analog mixers

A mixer is a circuit capable of frequency conversion that is used for transmitters (where it performs up-conversion) and receivers (performing down-conversion). In case of up-conversion operation the two inputs are a high frequency carrier or local oscillator (LO) and an information signal at an intermediate frequency (IF). The output comprises two RF signals, one at an upper sideband ($f_{LO} + f_{IF}$) and one at a lower sideband ($f_{LO} - f_{IF}$) centered around the high-frequency carrier [65].

The mixer circuit demonstrated here is depicted in figure 4.16. This is the first example of a graphene mixer with a built-in local oscillator, since all graphene mixers demonstrated so far have required an external oscillator to generate the signal [76, 78]. The core of the mixer is the buffer inverter. The high-frequency input signal is determined by the output of the RO (note that the RO operation is almost unaffected by the buffer since the former is outside the loop): $v_{IN,B}(t) = v_{LO}(t) = V_{OUT} + V_{p-p}\sin(2\pi f_{LO}t)$ where V_{OUT} is the DC offset of the output signal of the RO. The low frequency input is a small IF signal $v_{IF}(t) = V_{IF}\sin(2\pi f_{IF}t)$ superimposed to the DC bias of the buffer: $v_{DD,B}(t) = V_{DD} + v_{IF}(t)$, that leads the voltage gain of the buffer to vary with a periodicity determined by $f_{IF} = 25$ MHz. Choosing a small V_{IF} we can assume the voltage gain variation to be linear (linear

expansion of the gain around the DC offset) and express it as:

$$A_{\mathrm{v,B}}(t) = A_{\mathrm{v,B}}(V_{\mathrm{DD}}) + kv_{\mathrm{IF}}(t) \tag{4.6}$$

with k being a proportionality constant that can be determined experimenally ($k \approx 2$ V^{-1})[24]. The output voltage, according to (3.7) is

$$v_{\mathrm{OUT,B}} = A_{\mathrm{v,B}}(t)v_{\mathrm{IN,B}}(t) = A_{\mathrm{v,B}}(V_{\mathrm{DD}})v_{\mathrm{LO}}(t) + kv_{\mathrm{IF}}(t)v_{\mathrm{LO}}(t)$$

The first term gives rise to a component at a frequency f_{LO}= 292 MHz, while the second term is the product of two sines, $\sin(2\pi f_{\mathrm{LO}}t)\sin(2\pi f_{\mathrm{IF}}t)$ and generates the two components at frequencies $f_{\mathrm{LO}} \pm f_{\mathrm{IF}}$. In figure 4.17 the output signal (a) and the power spectrum (b) of the mixer are shown.

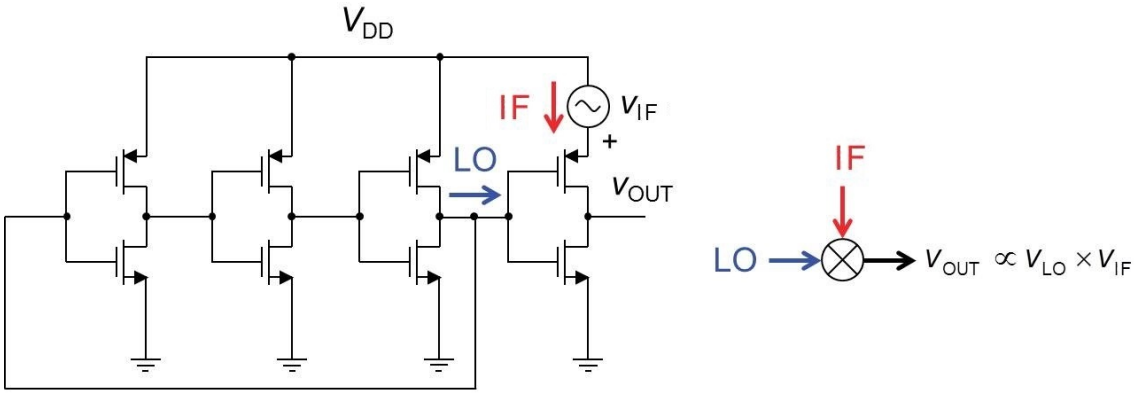

Figure 4.16: Graphene analog mixer circuit schematic. From reference [24].

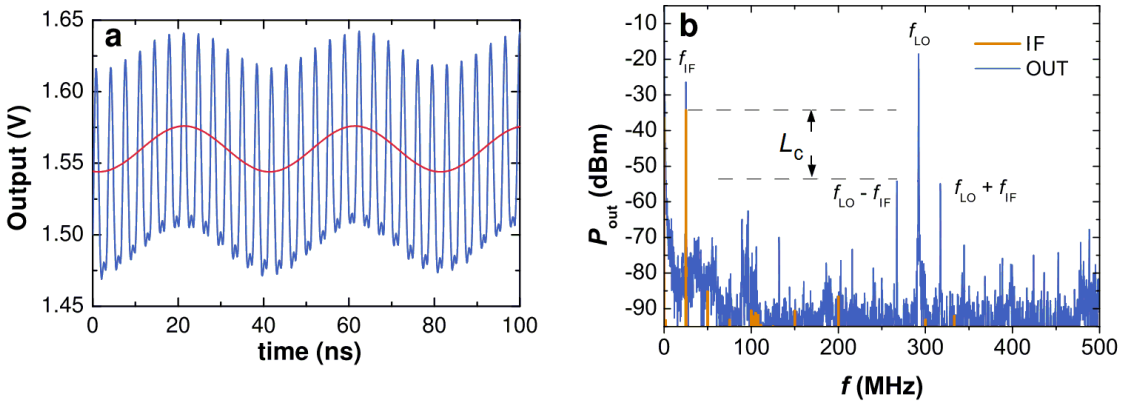

Figure 4.17: a) Output signal of the graphene analog mixer generated by the superposition of the high frequency LO signal $f_{\mathrm{LO}} = 292$ MHz and the low-frequency IF signal $f_{\mathrm{IF}} = 25$ MHz (red signal). b) Power spectrum of the input (IF) and of the output (OUT) of the mixer at $V_{\mathrm{DD}} = 2.5$ V. From reference [24].

For larger amplitudes of V_{IF} the gain variation is not linear anymore. The nonlinear intermodulation of the two input signals generates output signals at frequencies given by the sum of the harmonic multiples of the inputs: $nf_{\mathrm{LO}} \pm mf_{\mathrm{IF}}$, where n and m are integers. When this occurs the mixer is said to operate as harmonic or subharmonic mixer.

A performance metric for the mixer is the conversion loss, a measure of the efficiency in converting energy from the input to the output frequency, defined as the difference between the IF intput power and the available RF output power (from one of the sidebands): $L_{\mathrm{c}} = 10\log(P_{\mathrm{in,IF}}) - 10\log(P_{\mathrm{out,RF}}) \geq 0$ dB [65]. Conversion loss depends on the LO power, because it influences the mixer input impedence and the related resistive losses. The conversion loss obtained for the graphene mixer from figure 4.17 is 19.6 dB at an LO power of -18.5 dBm and IF power of -34.3 dBm, which is better than in early graphene mixers [79, 76], but worse than in recent graphene mixers [78, 80]. Another relevant performance metric is the port isolation, that defines the power leakages between each two of the three ports of the mixer. Considering the analyzed mixer, the isolation between the mixer ports is insufficient since the IF input port is not isolated from the LO signal. However, this problem could be addressed by connecting the IF source to the input of an amplifier (an inverter), and feeding the signal to the buffer through the output of this amplifier, thereby suppressing the feedback. In general, conversion loss is not a critical parameter for low-gain mixers that usually exhibit better noise figures and linearity (less power dissipated through the harmonics) than high-gain mixers. Required signal levels in the former case are often obtained by filtering the output before passing it to an additional low-noise amplifier stage [24].

4.3.2 Graphene digital modulators

The just described analog mixer can be used to perform the transmission of analog data in form of analog signals. If instead a digital information, such as computer data, has to be transmitted over channels that require analog signals (like fiber optic networks, computer modems, cellular phone networks, and satellite systems) a different encoding method should be involved. In these hybrid digital/analog systems an electromagnetic carrier wave is used to carry the information over great distances, while the digital data is used to modulate one or more parameters of the carrier wave, namely amplitude, frequency or phase [63]. The amplitude-shift keying techniques are characterized by the variation of carrier wave amplitude between discrete levels at a rate defined by the digital data. On-off keying (OOK) and binary amplitude-shift keying (BASK) are two types of amplitude modulation techniques. Usually OOK refers to a modulation between signal/noise states, whereas BASK is a more general term that refers to modulation between high-amplitude and low-amplitude states.

The circuit used to perform BASK modulation is depicted in figure 4.16 and resembles the analog mixer described above. The buffer inverter is fed with two input signals, a high-frequency LO signal (f_{LO}= 1.18 GHz) generated by the RO at the gate port and a digital IF signal (f_{IF}= 3 MHz) superimposed to the drain bias: $v_{\mathrm{IF}}(t) = V_{\mathrm{IF,ON}}$ for $0 < t < T/2$ and $v_{\mathrm{IF}}(t) = V_{\mathrm{IF,OFF}}$ for $T/2 < t < T$ where T defines the period. The voltage gain of the buffer depends on $v_{\mathrm{DD,B}}(t)$ as in (4.6), but in this case it can assume only two discrete values:

$$A_{\mathrm{v,B}}(t) = \begin{cases} A_{\mathrm{v,B}}(V_{\mathrm{DD}}) + A_v(V_{\mathrm{IF,ON}}) & \text{for} \quad 0 < t < T/2 \\ A_{\mathrm{v,B}}(V_{\mathrm{DD}}) + A_v(V_{\mathrm{IF,OFF}}) & \text{for} \quad T/2 < t < T \end{cases}$$

thereby the output signal of the RO alternates between a low amplitude and a high amplitude state with a time period defined by f_{IF} (see figure 4.18).

The amplitude ratio between the on and off output signals is about 9.2, thereby providing two well distinguished states. Note that the DC offset that has been substracted from the plot can also be removed from measurements through appropriate filtering.

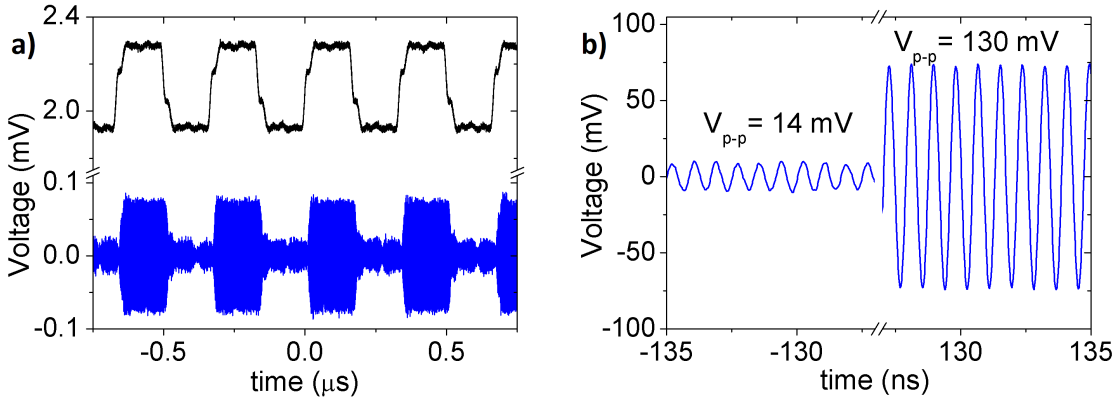

Figure 4.18: a) RF (black) signal, f_{RF} = 3 MHz, and output (blue) signal of the ring; b) zoomed output signal: in the off state f_{LO}=1.19 GHz, $V_{\mathrm{p\text{-}p}}$= 14 mV, and in the on state f_{LO}= 1.18 GHz, $V_{\mathrm{p\text{-}p}}$= 130 mV.

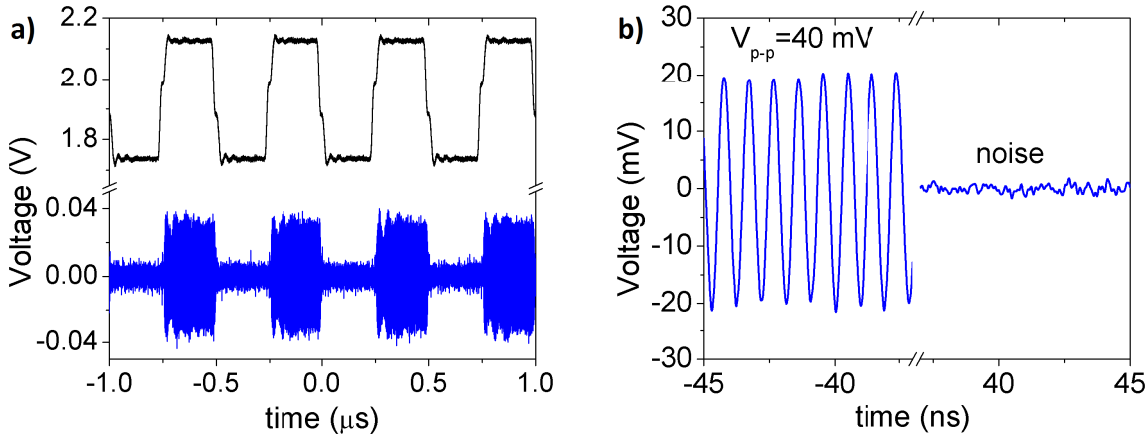

Figure 4.19: a) RF (black) signal, f_{RF} = 2 MHz, and output (blue) signal of the RO; b) zoomed output signal: in the on state f_{LO}=1.05 GHz, $V_{\mathrm{p\text{-}p}}$ = 40 mV, and in the off state (noise).

The circuit for OOK modulation is depicted in figure 4.19. A low-frequency IF square wave signal is superimposed to the drain bias of the first inverter within the RO's loop. The amplitude of this IF signal must be chosen such that in the on state the gain of the inverter is $|A_{v,1}| > 2$ and the RO can oscillate, while in the off state $|A_{v,1}| < 2$ and the oscillation is suppressed, see (4.1). If this happens the output signal (measured at the buffer output port) will alternate between an off noise state and an on state with signal amplitude given by $A_{\mathrm{v,B}} v_{\mathrm{LO}}(t)$ and frequency f_{LO} (see figure 4.19).

From the operational point of view there is no difference between these two techniques because both produce two well-defined states that can be demodulated at the receiver end to retrieve the digital information. Compared to the graphene-based amplitude modulators

demonstrated so far [20], the graphene ROs used in this work provide the capability of operation with a higher frequency LO carrier wave ($f > 1$ GHz). Since high frequency encoding is needed for fast and efficient transmission, this demonstration represent a step-forward through real applications of graphene devices.

Chapter 5

RF study of GFETs

The successful demonstration of complex integrated circuits brings up a further question: what can be done to sistematically improve the performances of these devices? An investigation of the single device unit, the GFET, from the circuit level to a physical level, can provide a useful tool to understand the phyiscs of the device and to find the most important factors influencing the scaling to submicron legths.

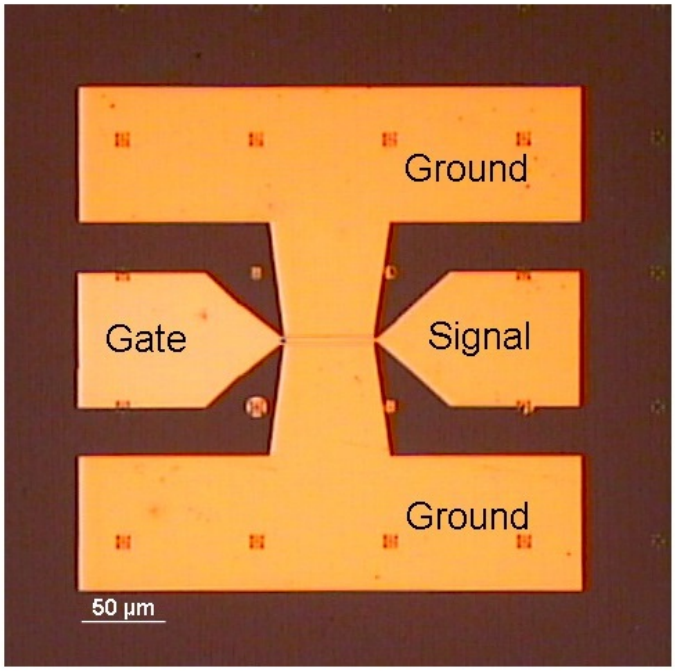

Figure 5.1: Optical image of a GFET in GSG configuration. The GFET comprises two parallel channels of $W = 50$ µm each, corresponding to a single channel of $W = 100$ µm. The gate length is $L = 1$ µm.

By studying the frequency response of GFETs through S-parameter measurements it is

possible to determine f_T and f_{MAX} and to develop a small-signal model of the circuit. For this purpouse GFETs in ground-signal-ground (GSG) configuration, as in figure 5.1, have been fabricated on different substrates and with different CVD-grown graphene (details are given in table 5.1).

SAMPLE	S1	S2	S3-S4
GRAPHENE	CVD Urbana	CVD Bluestone GT	CVD Urbana
$t_{substrate}$	510 µm	470 µm	470 µm
$\rho_{substrate}$	0.001-0.01 Ωcm	5000 Ωcm	5000 Ωcm
$t_{BG,ox}$	300 nm	1 µm	1 µm

Table 5.1: List of the investigated samples. $t_{substrate}$ is substrate thickness, $\rho_{substrate}$ is the substrate resistivity and $t_{BG,ox}$ is the thickness of the back gate oxide.

This chapter will introduce some importants FOMs that are commonly used to determine the performances of GFETs and FETs in general. These FOMs can be determined with the aid of S-parameter measurements, that allow also the extraction of intrinsic device parameters such transconductance and output resistance. A small-signal model that simulates the GFET operation at any bias point will be presented, and the outcome of scaling investigations will be discussed.

5.1 Important FOMs in small-signal regime

Different FOMs have been adopted in the past to compare the performances of GFETs to Si CMOS and III-V HEMTs and define the real potential of graphene technology. The main performance metric for this investigation has been the transistor cutoff frequency f_T, corresponding to the frequency at which the small-signal current gain, defined as $h_{21} = i_{out}/i_{in}$, goes to unity. The circuit configuration that allows to measure cutoff frequency has a current source directly connected to the input port (the gate) of the FET and the output port (the drain) shorted to ground (the source) as in figure 5.2a.

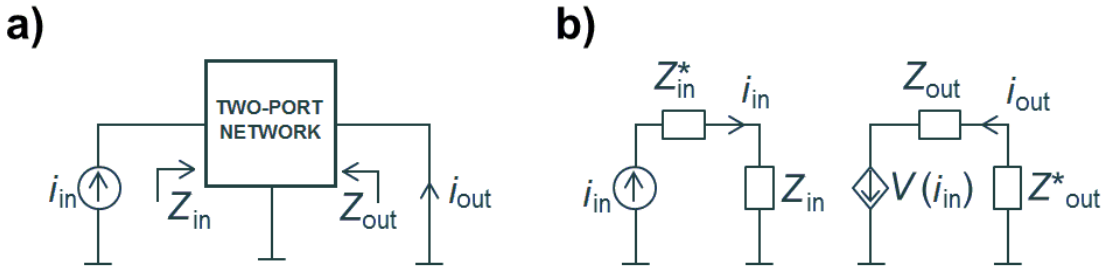

Figure 5.2: General schematic of the circuits used to measure current gain (a) and unilateral power gain (b). In (a) the i_{in} is the input current from an ideal current source, i_{out} is the output current (source and drain are shorted) and Z_{in} and Z_{out} are the input and output impedances of the device. Circuit (b) is unilateral (no feedback) and input and output ports are conjugated-matched with Z^*_{in} and Z^*_{out} to provide the highest gain. The voltage $V(i_{in})$ between source and drain depends on the input current.

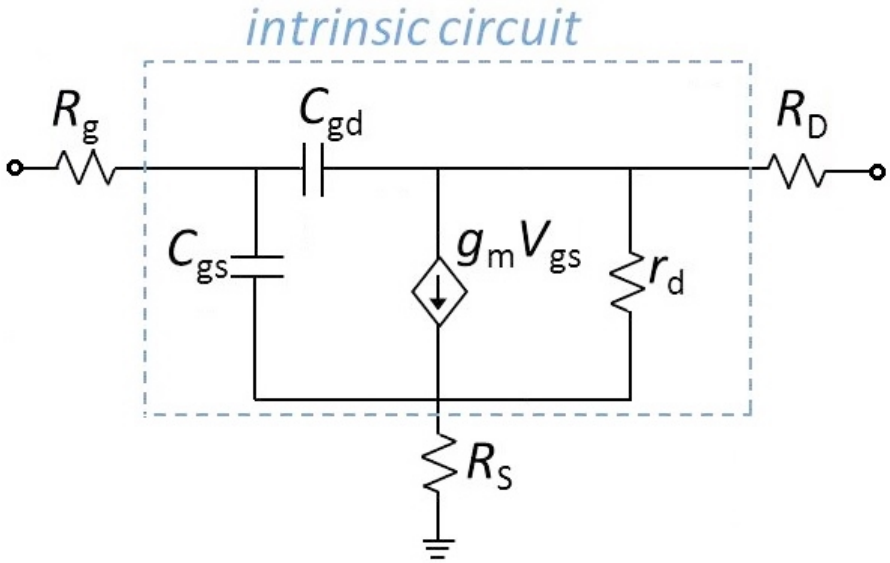

Figure 5.3: Small-signal equivalent circuit of a GFET comprising an intrinsic core, and series contact (R_S, R_D) and gate (R_g) resistances.

The expression for the intrinsic cutoff frequency of a GFET can be derived by the analysys of the equivalent small-signal intrinsic circuit of the transistor (see figure 5.3):

$$f_{T,int} = \frac{g_{m,int}}{2\pi(C_{gs} + C_{gd})} \tag{5.1}$$

The extrinsic cutoff frequency that includes the contribution from gate, source and drain resistances is given by:

$$f_{\mathrm{T,ext}} = \frac{g_{\mathrm{m,int}}}{2\pi(C_{\mathrm{gd}} + C_{\mathrm{gs}})} \frac{1}{1 + \frac{R_{\mathrm{S}}+R_{\mathrm{D}}}{\mathrm{r}_{\mathrm{d,int}}} + \frac{C_{\mathrm{gd}} g_{\mathrm{m,int}} (R_{\mathrm{S}}+R_{\mathrm{D}})}{C_{\mathrm{gs}}+C_{\mathrm{gd}}}} \tag{5.2}$$

where R_{g}, R_{S} and R_{D} are the gate, source and drain contact resistances. The presence of a current source at the input in the circuit of figure 5.2, makes the current gain independent on the extent of R_{g}. This fact has important consequencies, in particular at high frequencies at which R_{g} and C_{gs} would otherwise act as a RC filter, slowing down the circuit response. Another important characteristic of the circuit of figure 5.2 is the short-circuit between source and drain, that result in the expression for $f_{\mathrm{T,int}}$ being independent on the output resistance $r_{\mathrm{d,int}}$, i.e. on the extent of current saturation (that is usually poor for GFETs, as discussed in chapter 3). Therefore, in this setup framework and thanks to the high carrier mobility of graphene, GFETs can exhibit extremely high cutoff frequencies, above 400 GHz for devices with $L = 100$ nm [81, 82], close to the values exhibited by the InP HEMT (the fastest technology) at the same technological node [21]. Moreover, the scaling trend of $f_{\mathrm{T}} \propto L^{-1}$ follows that of conventional semiconductor FETs [21]. However, as anticipated in section 4.2.3, the cutoff frequency is not the most suitable parameter to judge device performances, since it is a measure of the transit time of carriers in the channel rather than of the real transistor functionality at high frequency.

A more realistic figure of merit is the maximum frequency of oscillation, f_{max}, representing the frequency at which the unilateral power gain (see Appendix C), also called Mason's gain [83], $U = P_{\mathrm{out}}/P_{\mathrm{in}}$, falls to unity. The intrinsic maximum frequency of oscillation is:

$$f_{\mathrm{max,int}} = \frac{g_{\mathrm{m,int}}}{4\pi C_{\mathrm{gs}} \sqrt{R_{\mathrm{g}}/r_{\mathrm{d,int}}}} \tag{5.3}$$

Note that to calculate this expression the gate resistance should be included in the intrinsic circuit in figure 5.3, otherwise $f_{\mathrm{max,int}}$ would go to infinity. By adding the source and drain parasitic resistances, extrinsic $f_{\mathrm{max,ext}}$ can be expressed as [21]:

$$f_{\mathrm{max,ext}} = \frac{g_{\mathrm{m,int}}}{4\pi C_{\mathrm{gs}} \sqrt{\frac{(R_{\mathrm{g}}+R_{\mathrm{S}}+R_{\mathrm{D}})}{r_{\mathrm{d,int}}} + \frac{g_{\mathrm{m,int}} R_{\mathrm{g}} C_{\mathrm{gd}}}{C_{\mathrm{gs}}}}} \tag{5.4}$$

In the circuit used to measure f_{max}, shown in figure 5.2b, the impedance of the input voltage source and the load impedance are finite, resulting in both R_{g} and $r_{\mathrm{d,int}}$ influencing the power gain. This severely limits the extent of f_{max} in GFETs, that turns out to be much smaller than in conventional transistors, typically only ~ 50 GHz [21], with a maximum value of 105 GHz recently reported for a 100 nm gate length device [84]. By comparison, $f_{\mathrm{max}} > 1$ THz has been obtained both in InP HEMT [85] and HBTs [86]. Moreover, f_{max} of GFETs was found to scale only weakly with the inverse gate length, thereby offering less perspectives for improvements [21]. Of the two FOMs, f_{T} and f_{max}, the latter is certainly the more important, since it is an invariant quantity which represents a benchmark to compare different transistor technologies and accounts for real signal amplification. However, it is defined in conditions of device unilateralization and impedance matching (see Appendix C)

which cannot be performed in realistic circuits. Therefore it can be convenient to provide an additional FOM, to describe the power delivered by the transistor in a realistic circuit, and this parameter is the transducer power gain that will be defined in section 5.2.1.

5.2 *S*-parameters

Scattering parameters are reflection and transmission coefficents defined as the ratios between reflected and transmitted normalized voltage waves at the two ports of the device. They are widely used in microwave electronics where they represent a useful tool to study the frequency response of amplifiers (and other circuits in general), being preferred to current and voltage measurements that require open and short circuits difficult to obtain at high frequencies (due to the parasitic capacitances and inductances) [87].

A transistor is a two-port network, with gate-source as input and drain-source as output port (source is usually grounded). *S*-parameter measurements are performed applying a small power signal superposed to the DC bias at both ports to measure reflection and propagation coefficients as a function of frequency (see figure 5.4).

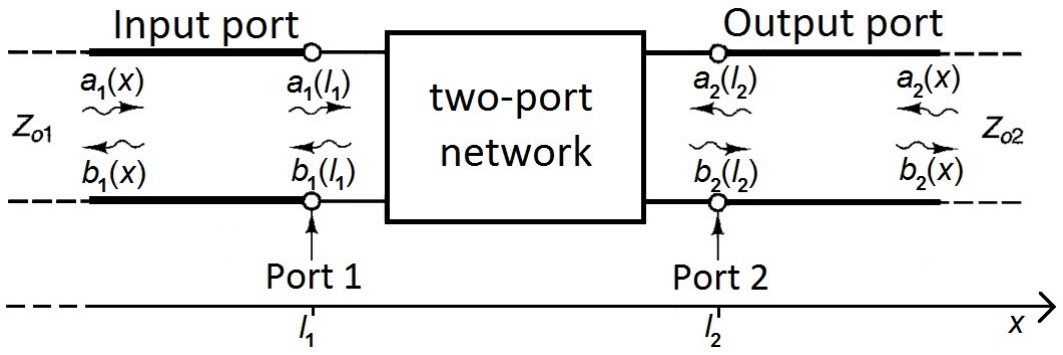

Figure 5.4: Schematic of travelling waves in a two-port network. $a_i\,(x)$ is the incident and $b_i\,(x)$ the reflected voltage wave (where i is an integer that indicates the port number) defined as a function of the position along the transmission line. Taken from [87].

A voltage wave travelling through a transmission line can be represented as a superposition of an incident and a reflected wave forming a standing wave pattern, which can be written as:

$$V(x) = V^+(x) + V^-(x) = A\mathrm{e}^{-j\beta x} + B\mathrm{e}^{j\beta x} \tag{5.5}$$

where $\beta = \omega\sqrt{LC}$ is the characteristic propagation constant of the transmission line that depends on the inductance L and on the capacitance C of the transmission line. The incident and reflected voltages, normalized with respect to the characteristic impedence of the transmission line Z_0 (tipically 50 Ω for coaxial cables), can be written respectively as:

$$a(x) = \frac{V^+(x)}{\sqrt{Z_0}} \quad \text{and} \quad b(x) = \frac{V^-(x)}{\sqrt{Z_0}}$$

According to these expressions S-parameters are defined as follows [87]:

$$S_{11} = \frac{b_1(l_1)}{a_1(l_1)}\Big|_{a_2(l_2)=0} \quad \begin{array}{c}\text{input reflection coefficient}\\ \text{(with output properly terminated)}\end{array}$$

$$S_{21} = \frac{b_2(l_2)}{a_1(l_1)}\Big|_{a_2(l_2)=0} \quad \begin{array}{c}\text{forward transmission coefficient}\\ \text{(with output properly terminated)}\end{array}$$

$$S_{22} = \frac{b_2(l_2)}{a_2(l_2)}\Big|_{a_1(1_1)=0} \quad \begin{array}{c}\text{output reflection coefficient}\\ \text{(with input properly terminated)}\end{array}$$

$$S_{12} = \frac{b_1(l_1)}{a_2(l_2)}\Big|_{a_1(1_1)=0} \quad \begin{array}{c}\text{backward transmission coefficient}\\ \text{(with input properly terminated)}\end{array}$$

The term "properly terminated" implies that the transmission line is loaded with an impedence equal to its own impedence to avoid any signal reflection. The extent of transmission or reflection of the incident wave depends on the input and output impedances of the device. The parameter S_{11}, for example, is related to the input impedance Z_{IN} through the following expression [87]:

$$S_{11} = \frac{Z_{\mathrm{IN}} - Z_0}{Z_{\mathrm{IN}} + Z_0} = \Gamma_{\mathrm{IN}}$$

and similarly:

$$Z_{\mathrm{IN}} = Z_0 \frac{1 + \Gamma_{\mathrm{IN}}}{1 - \Gamma_{\mathrm{IN}}}$$

The S-parameters can be easily converted into Z or Y-parameters directly related to capacitances, resistances and inductances of the device that can be described through a physical model.

5.2.1 Extraction of small-signal FOMs

S-parameter measurements give direct acces to the main small-signal FOMs, such g_{m}, g_{d}, A_0, h_{21} and U .

Transconductance and output conductance are given by: $g_{\mathrm{m}} = \mathrm{Re}(Y_{21})$ and $g_{\mathrm{d}} = \mathrm{Re}(Y_{22})$, where Y_{21} and Y_{22} are the admittance parameters that are directly available from the measurements as well as S-parameters and Z-parameters to which they are related. Knowing the transconductance and the output conductance values, the intrinsic gain of the GFET, A_0, can be calculated (see equation 3.9).

Similarly, the current gain h_{21} can be extracted from measurements as [87]:

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}$$

The unilateral power gain U is defined as the maximum power gain that can be obtained from the two port system, after it has been made unilateral with the help of a lossless and reciprocal embedding network which provides the required feedback (see Appendix C) [88]. It can be expessed as a function of Y, Z or S-parameters as:

$$U = \frac{|Y_{21} - Y_{12}|^2}{4\left(\mathrm{Re}\left(Y_{11}\right)\mathrm{Re}\left(Y_{22}\right) - \mathrm{Re}\left(Y_{12}\right)\mathrm{Re}\left(Y_{21}\right)\right)} = \frac{|S_{12} - S_{21}|^2}{\det(\mathbf{I} - \underline{S}\underline{S}^*)}$$

where $\underline{S}$ is the scattering matrix and $\mathbf{I}$ is the identity matrix.

Another important parameter is the transducer power gain, defined as the fraction of power available from the source, P_{avs}, that is delivered to the load, P_{L} :

$$G_{\mathrm{T}} = \frac{P_{\mathrm{L}}}{P_{\mathrm{avs}}} = \frac{|S_{21}|^2\left(1 - |\Gamma_{\mathrm{L}}|^2\right)\left(1 - |\Gamma_{\mathrm{S}}|^2\right)}{|1 - \Gamma_{\mathrm{IN}}\Gamma_{\mathrm{S}}|^2\,|1 - S_{22}\Gamma_{\mathrm{L}}|^2} \tag{5.6}$$

where Γ_{L} and Γ_{S} are the load and the source reflection coefficients, respectively. If source and load are matched (i.e. $\Gamma_{\mathrm{L}} = \Gamma_{\mathrm{S}} = 0$) the expression simplifies to $G_{\mathrm{T}} = |S_{21}|^2$.

The transducer power gain is often the more important parameter for circuit designers, since it represents the effective power efficiency of a device in real conditions, because unilateralization and impedance matching can be difficult to achieve, especially over a wide frequency range.

5.3 Small-signal model of GFETs

A general small-signal circuit model has been proposed for GFETs, based on the conventional MOSFET model [89, 90]. The model includes an intrinsic GFET core comprised of bias dependent parameters, the contacts and gate resistances that are considered part of the extrinsic circuit and the additional parasitic components related to pads and interconnects, see figure 5.5. The small-signal model is used to describe the device response to small variations of drain and gate bias. A linear expansion of the current around a bias point defined by the DC voltages $\mathrm{Q}(V_{\mathrm{GS}}, V_{\mathrm{DS}})$ gives:

$$i_{\mathrm{D}} = i_{\mathrm{D}}(Q) + \left.\frac{\partial i_{\mathrm{D}}}{\partial v_{\mathrm{DS}}}\right|_{\mathrm{Q}}(v_{\mathrm{ds}}) + \left.\frac{\partial i_{\mathrm{D}}}{\partial v_{\mathrm{GS}}}\right|_{\mathrm{Q}}(v_{\mathrm{gs}}) = I_{\mathrm{D,DC}} + g_{\mathrm{d}}v_{\mathrm{ds}} + g_{\mathrm{m}}v_{\mathrm{gs}}$$

Within superposition theory the DC and AC components of the current can be treated separately. Then, the AC circuit response can be modeled by a voltage-controlled current source, $g_{\mathrm{m}}v_{\mathrm{gs}}$, in parallel with a resistor r_{d}. This small-signal circuit has general validity at low frequency, but the values of g_{m} and r_{d} should be determined at a given DC point.

A high frequency model of the GFET should take into account the charging and discharging of the gate capacitance that affects the dynamic response of the device. The source-to-drain and source-to-gate capacitances in a standard MOSFET describe the coupling between the gate and the channel and are bias dependent. In ohmic (or linear) region, with $V_{\mathrm{DS}} \approx 0$, the charges are equally distributed in the channel, and C_{gs} and C_{gd} can be expressed as [91]:

$$C_{\mathrm{gs,lin}} = C_{\mathrm{gd,lin}} = \frac{C_{\mathrm{ox}}LW}{2} \tag{5.7}$$

assuming that no overlap exists between the electrodes and the gate oxide (if that would be the case additional overlap capacitances should be included in the model). In saturation regime, the channel is pinched-off at the drain. Since no mobile carriers are accumulated at the drain side, the capacitances can be modeled as:

$$C_{\mathrm{gs,sat}} = \frac{2C_{\mathrm{ox}}LW}{3}, \quad C_{\mathrm{gd,sat}} \approx 0 \tag{5.8}$$

As discussed in the previous chapters GFETs never exhibit a real saturation, thus mobile charges are always present at either drain or source side. For this reason we could expect C_{gs} to be higher than C_{gd} when channel pinches-off at the drain due to a lower DOS, and C_{gd} higher than C_{gs} when the pinch-off occurs at the source side. When the Dirac point is in the middle of the channel, the capacitances should be equal because the charge distribution in the channel becomes symmetric.

Capacitance C_{ds} describes the coupling between source and drain mainly occurring through the substrate. In long channel devices its value is small and turns out to be negligible if compared to the intrinsic gate capacitances.

The extrinsic GFET model comprises gate, source and drain resistances. The gate resistance, R_{g}, is a bias-independent parameter that describes the resistance of the gate metal considering the small-signal operating conditions [92]:

$$R_{\mathrm{g}} = \frac{R_{\mathrm{g,DC}}}{3} = \frac{\rho_{\mathrm{g}} W_{\mathrm{g}}}{3 L_{\mathrm{g}} t_{\mathrm{g}}} \tag{5.9}$$

where $R_{\mathrm{g,DC}}$ is the geometric gate resistance, ρ_{g} is the resistivity of the gate metal, W_{g}, L_{g} and t_{g} are the width, length and thickness of the gate metal line (not to be confused with W and L, the width and length of the channel below the gate). Contact resistances comprise several contributions such as probe-to-pad contact resistance, interconnects resistance and carrier injection resistance from metal to graphene. While the first two terms are bias-independent, the carrier-injection resistance depends on the DOS of graphene below the contact, that is determined by the graphene and metal work functions, the intrinsic doping of the channel and, ultimately, by the gate-voltage induced channel potential in the contacts proximity (see section 4.2.2). Clearly, the choice to model these contributions as single resistances R_{S} and R_{D}, as in figure 5.5, is an oversimplification. However, it is reasonable to start from the simplest model capable to provide a good description of device physics and add corrections if the agreement with the measurements is not satisfactionary. A different model for contacts is proposed in Appendix D (based on the paper work [93]).

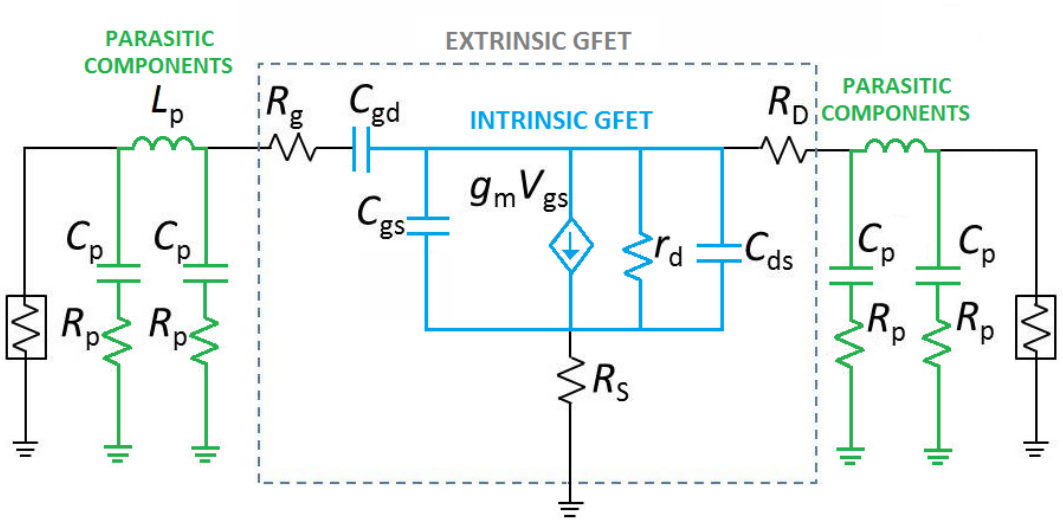

Figure 5.5: Equivalent small-signal circuit for the GFET. It comprises an intrinsic core, series resistances of the contacts that, added to the intrinsic part, complete the extrinsic circuit, and parasitic resistances inductances and capacitances associated with pads and interconnects.

To complete the model, parasitic capacitances arising between pads and the substrate through the back gate oxide, C_{p}, and resistances and inductances of the metal lines, R_{p} and L_{p}, should be included as bias-independent parasitic components [94]. The procedure to extract the contribution of these parameters from the measurements is called de-embedding and will be described in the next section.

5.4 Experimental

5.4.1 Measuring *S*-parameters

The S-parameters are measured in matched conditions, i.e. with ports terminated with an impedence that equals the impedence of the transmission lines of 50 Ω. When the output is properly teminated the travelling wave incident on the load is totally absorbed, so the conditon $a_2(l_2) = 0$ is satisfied and the same holds for the input. S-parameter measurements have been performed with a probe-station Cascade Microtech Summit 12561B controlled by a Nucleus software. Input and output signals were applied by an Anritsu Vectorstar MS4647A VNA. The DC bias to gate and drain ports was applied through 2600 Keithley source-metres. The devices were probed with (GSG) Cascade Microtech 110-A probes with 100 µm-pitch. The external ground pins were connected to the sources of the GFETs and the signal pins were connected respectively to the gate at the input and to the drain at the output port.

The main components of the VNA are the stimulus sources and the response receivers. The stimulus sources (one at each port) comprise a frequency synthesizer that generates a

power wave (of -25 dBm corresponding to $\sim$3 µW) that is split into the incident wave sent to the DUT and in a reference wave. The reference and scattered waves are down-converted by a tuned receiver into a lower IF signal and filtered trough a 100 Hz bandwidth to reduce noise components before ADC processing [95].

Since a travelling wave experiences a delay which depends on the characteristic impedence Z_0 and propagation constant β of the transmission line, S-parameters assume different values as a function of position along the transmission line. Hence, a calibration with a reference substrate should be performed prior to the measurements to correct the phase-shift up to the probe tips. The calibration substrate contains standard open, short and 50 Ω-load structures whose S-parameters are known and recorded in the calibration software WinCal. The real S-parameters of these circuits are measured by the VNA and the difference between the measured values and the nominal values stored in the software is related to the delay introduced by transmission line and connections. WinCal computes this difference and stores it as a baseline. If this procedure is done correctly, when the real device is tested all the parasitic impedances from VNA source to the probe tips are substracted from the measurements, thereby giving access to the circuit model parameters of figure 5.5.

The VNA provides S-parameters that, being complex reflection coefficients, are usually plotted in polar form. Knowing the direct relation between reflection coefficient and impedance, $\Gamma = (Z-1)/(Z+1)$, it could be of more practical use to extract directly from the plots the impedance values of the circuits. This can be accomplished through Smith charts, often normalized by the characteristic impedance Z_0, that can map Z on the same polar plots just by changing the axis value, see figure 5.6. Vertical lines on the polar plot map to circles of constant resistance on the Smith Chart, and horizontal lines map to arcs of constant reactance.

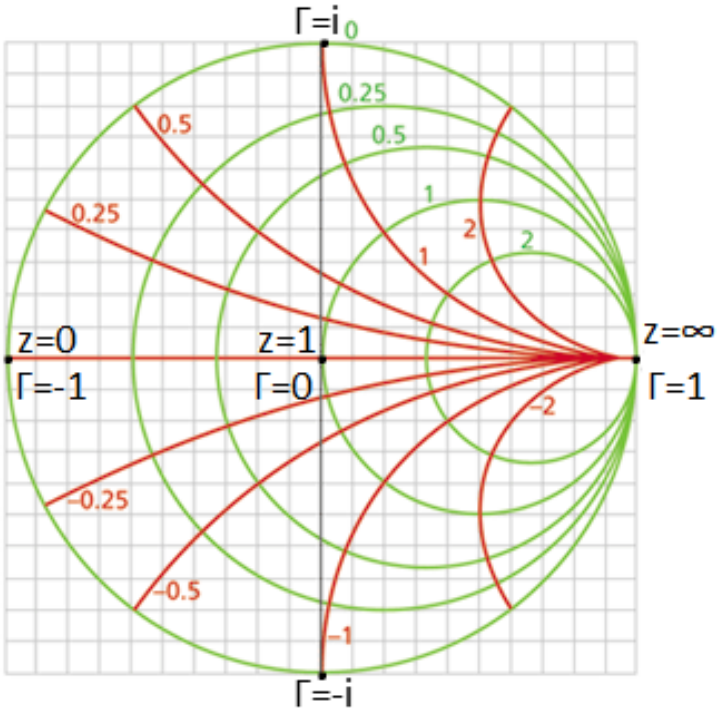

Figure 5.6: Smith chart with constant reactance curves (red) and constant resistance circles (green). Special points on the real and imaginary axes are marked.

5.4.2 De-embedding

When testing the RF performances of a device, it may be useful to extract the contribution of the parasitic components of pads and interconnects, not being part of the extrinsic circuit. This extraction is accomplished through the de-embedding procedure.

In order to perform de-embedding open, short and through standards, which are exact copy of the real device without the graphene channel, have been fabricated. Open structure has no connection (open circuit) between the two ports, short has input and output ports shorted together to ground, and through is characterized by a short between the two ports. Without a graphene channel there are no contact resistances, so these standards only represent the parasitics associated with interconnects, pads and substrate. To extract the parasitic components it is necessary to define in advance an equivalent circuit that correctly models the test structures, as shown in figure 5.7. The value of the parasitic components is calculated through an optimization process performed by the software ADS by minimizing the difference between the measured S-parameters and those simulated from the modeled circuit (this procedure will be described in section 5.5.3). The parasitic components extracted can be substracted from the measurements to access the extrinsic-device behaviour.

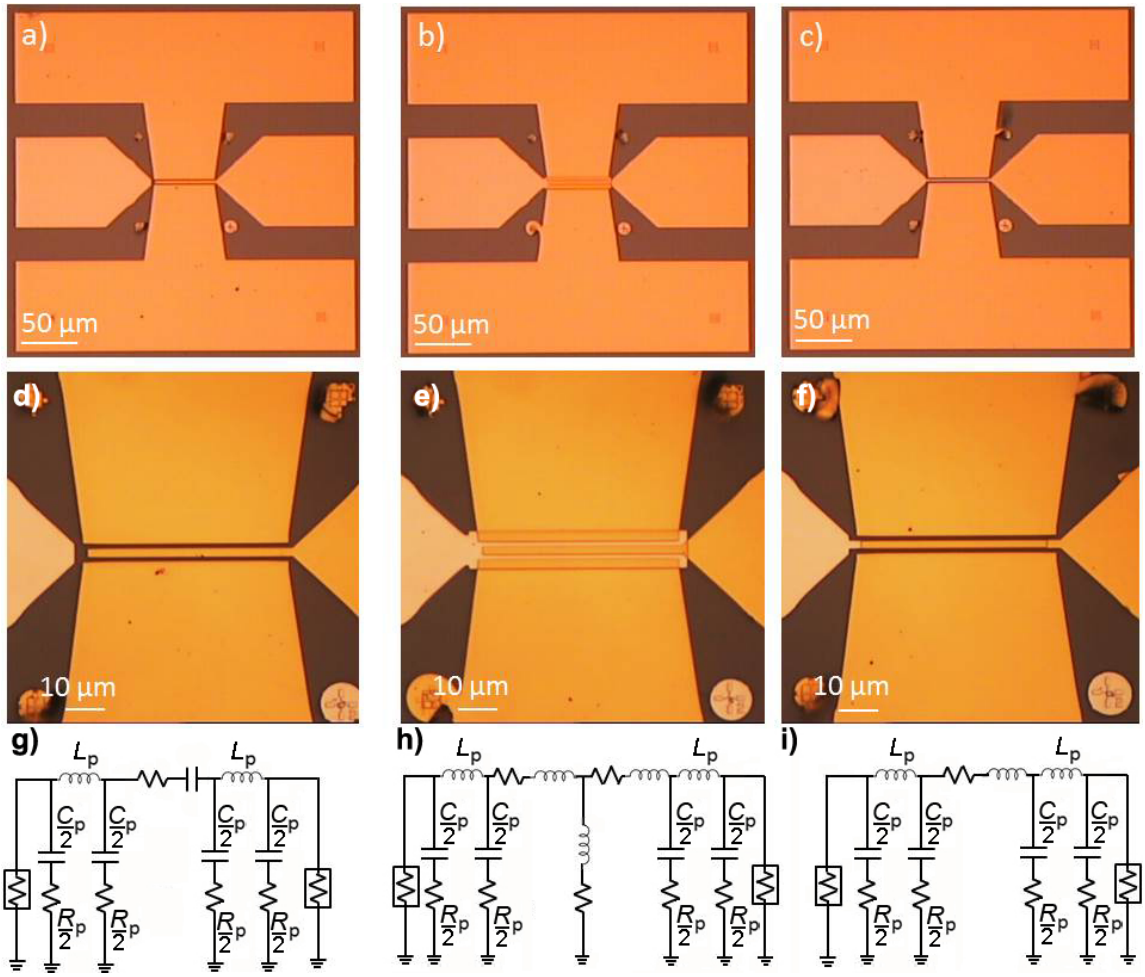

Figure 5.7: Optical image of a) open, b) short and c) through structure. Zoomed-in of the same structures (d,e,f) and corresponding equivalent circuit (g,h,i).

5.5 Results and discussion

5.5.1 Determination of the parasitic components of different substrates

A first investigation on samples S1 and S2 has been focused on the influence of the substrate on GFETs performance. Sample S1 is fabricated on the conventional substrate used throughout this work. As shown in Table 1, S1 substrate is made by low-resistivity Si covered with 300 nm of SiO_2 on the top side and a metal back gate on the bottom side, while S2 substrate is formed by highly-resistive Si covered by 1 µm of SiO_2 on the top, without back gate. Therefore S1 should exhibit higher parasitic capacitances C_p arising from pads and substrate through the relatively thin oxide (the low resistivity of the As-doped Si increases both capacitive and resistive losses) compared to S2. Capacitive losses reduce the speed of signal transmission, hence insulating substrates like S2 represent the ideal choice in the microwave field. This preliminary study had the purpouse to determine

the effective properties of the two different substrates and show their effect on the operation speed through deembedding.

The test structures shown in figure 5.7 have been fabricated on both substrates and S-parameters of unbiased devices have been measured to extract the parasitic resistances, inductances and capacitances [94]. While the parasitic resistance is negligible in both cases ($R_{\mathrm{p}}\sim$ 1 Ω) and L_{p} depends on the metal lines so it is equal for the two substrates, simulations give $C_{\mathrm{p}}\sim$ 50 pF/cm^2 on S2 and $C_{\mathrm{p}}\sim$ 200 pF/cm^{2}on S1. Taking into account the effect of parasitic capacitances, the expression for the cutoff frequency becomes [5]:

$$f_{\mathrm{T}} = \frac{g_{\mathrm{m,int}}}{2\pi((C_{\mathrm{gs}}+C_{\mathrm{gd}})(1+(R_{\mathrm{S}}+R_{\mathrm{D}})/r_{\mathrm{d,int}})+C_{\mathrm{gd}}g_{\mathrm{m,int}}(R_{\mathrm{D}}+R_{\mathrm{S}})+C_{\mathrm{p}})}.$$

This expression shows that higher parasitic capacitances reduce the f_{T} and therefore f_{max}. For this reason the following investigation has been performed only on devices fabricated on S2, S3 and S4 that provide better device performances than S1.

5.5.2 DC characterizations

Before investigating the AC response of the devices a DC characterization has been performed to determine the optimum bias condition, i.e. the voltages at the Q point (for which the intrinsic gain is maximum).

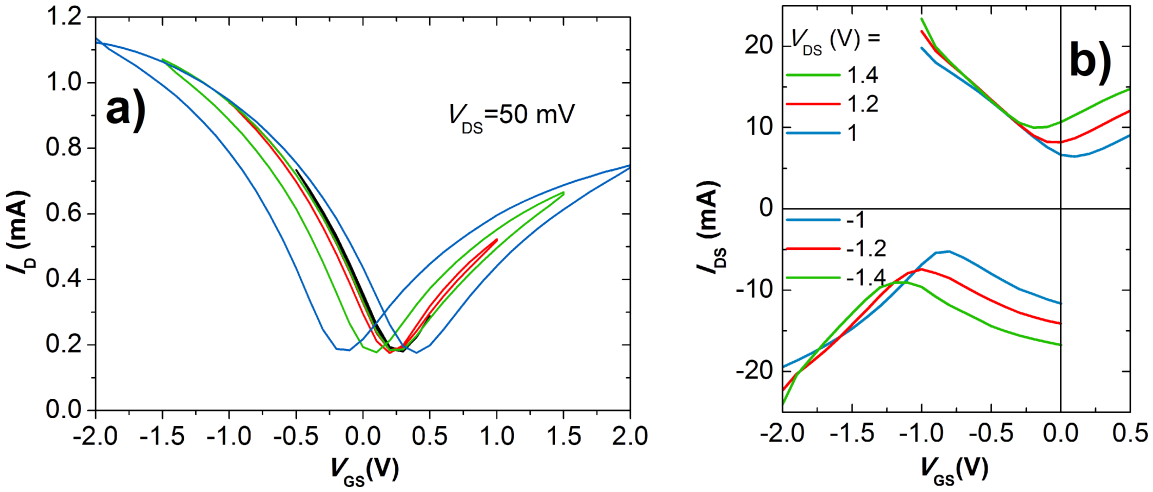

Figure 5.8: DC characterization of a typical device. a) Transfer characteristics at V_{D}=50 mV showing low doping level ($V_{\mathrm{th}}\sim$ 0 V) and hysteresis. b) Transfer characteristics at positive and negative bias. The hole branch (left from the Dirac point) is steeper then the electron branch and shows less drain bias dependence, i.e. the current variation with respect to the drain voltage at a fixed gate voltage is smaller on the left from the Dirac point, implying better saturation.

Figure 5.8a shows the DC transfer curve of a typical device from sample S3, measured by increasing the amplitude of double (forward and backward) gate voltage sweep. The

hysteresis observed here has been subject of several studies [96, 97], and is commonly attributed to the presence of charges trapped at the interface between graphene and the top gate oxide that dope the graphene layer, thereby changing the effective potential. Hysteresis phenomenon occurs in a timescale of seconds, and can be suppressed by faster sweep rates that prevent the accumulation of mobile charges. At larger sweep amplitudes the hysteresis increases (from black to blue curve). This behaviour can been explained considering that interface traps are filled continuosly as the gate voltage is tuned, so that at larger sweeps there is a larger traps density N_{tr} responsible of a larger split in the Dirac points of the up and down sweeps. The split of the Dirac voltages is: $\triangle V_{\mathrm{np}} = 2\mathrm{e}N_{\mathrm{tr}}/C_{\mathrm{q}}$ where C_{q} is the quantum capacitance arising from graphene limited DOS [96].

During S-parameters measurements the high sweep frequency (above 10 MHz) and the sweep amplitude given by the small RF power applied to the input port (-25 dBm corresponding to about 35 mV) allow to neglect the effect of charge trapping on device operation. This is because the dynamic of the traps response is too slow to follow the sweep frequency.

Figure 5.8b shows two transfer curves of the same device measured at negative and positive drain bias. Two interesting features should be highlighed. First, in the majoritary-hole transport region (left side from the Dirac point) the transfer curves are steeper, corresponding to a larger transconductance. This behaviour can be attributed to the formation of p-n-p junction between p-type contacts and the channel on the right-hand side of the Dirac point, in the majoritary-electron transport regime, causing an increase in the contact resistance in the right branch [98, 99]. A second feature, that may be less obvious, is that moving along the drain bias sweep at a fixed gate voltage (i.e. following the current variation between the curves at the same gate voltage) the output conductance is lower in the left branches, where curves overlap. Both characteristics, high trasconductance and low output conductance, are beneficial for high gain operation. Thereby the Q point for this device has been set at negative drain and gate biases, in the deep hole conduction region. Since all devices exhibit similar doping levels and transfer characteristics they have all been measured under these conditions. The choice to investigate all devices within a limited voltage range around Q point allows to minimize the scattering of measured values and extract a better scaling statistics.

5.5.3 S-parameter-based scaling study

S-parameters were measured in a frequency range from 10 MHz to 50 GHz. The variables were extracted through the optimizations performed in the frequency range from 10 MHz to 20 GHz. Optimizations are performed by the ADS software through an iterative procedure that allows to determine the values of the parameters of the small-signal model. Such values are those for which the quantity: $\underline{S}_{\mathrm{error}} = |\underline{S}_{\mathrm{meas}} - \underline{S}_{\mathrm{model}}|$ is minimized, with $\underline{S}_{\mathrm{meas}}$ defining the matrix of measured S-parameters and $\underline{S}_{\mathrm{model}}$ the matrix of S-parameters simulated for the small-signal model, see figure 5.9.

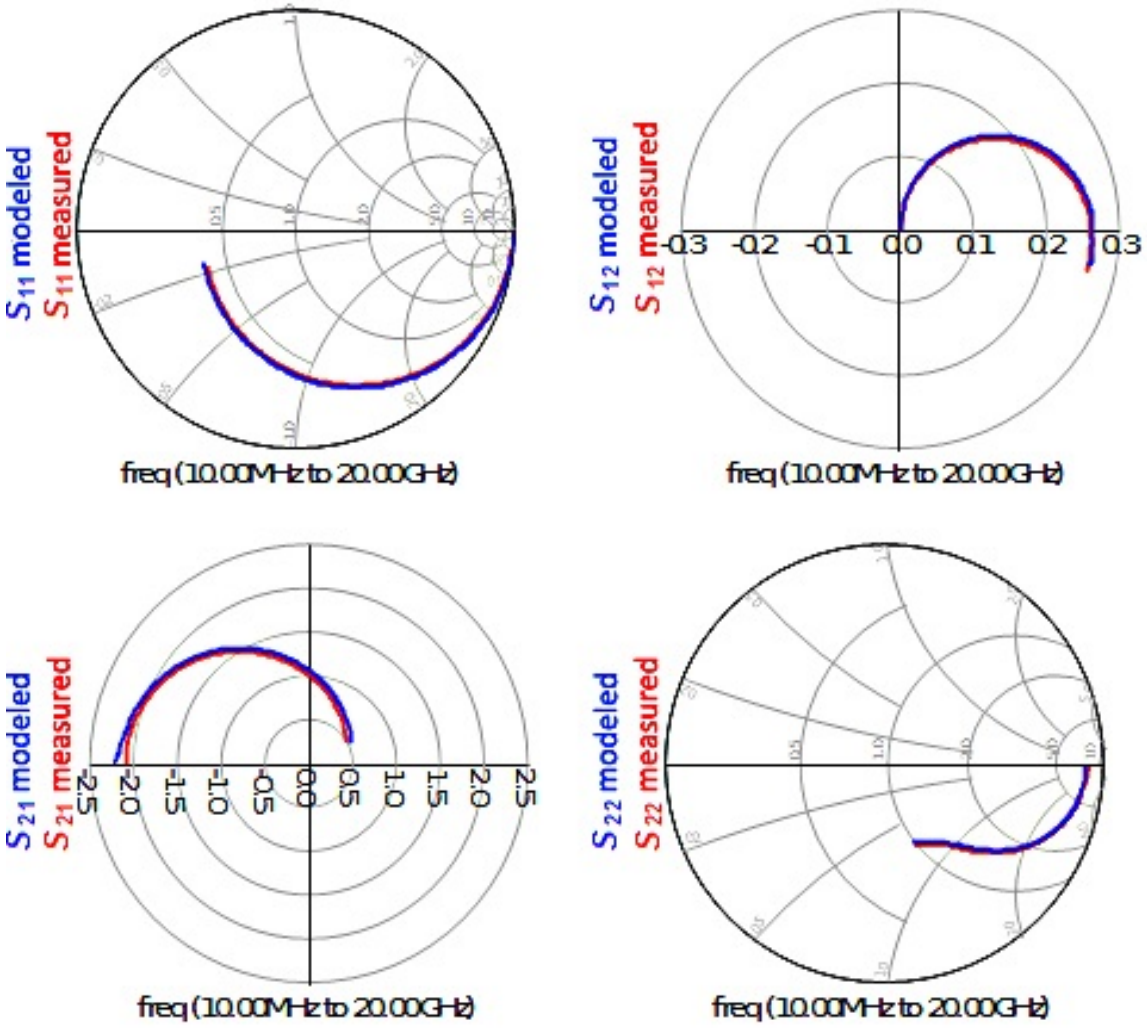

Figure 5.9: Comparison between measured and modeled S-parameters at V_{DS}= -1.5 V and V_{GS}= -1.3 V for a device with L = 1 µm and W= 40 µm (sample S3).

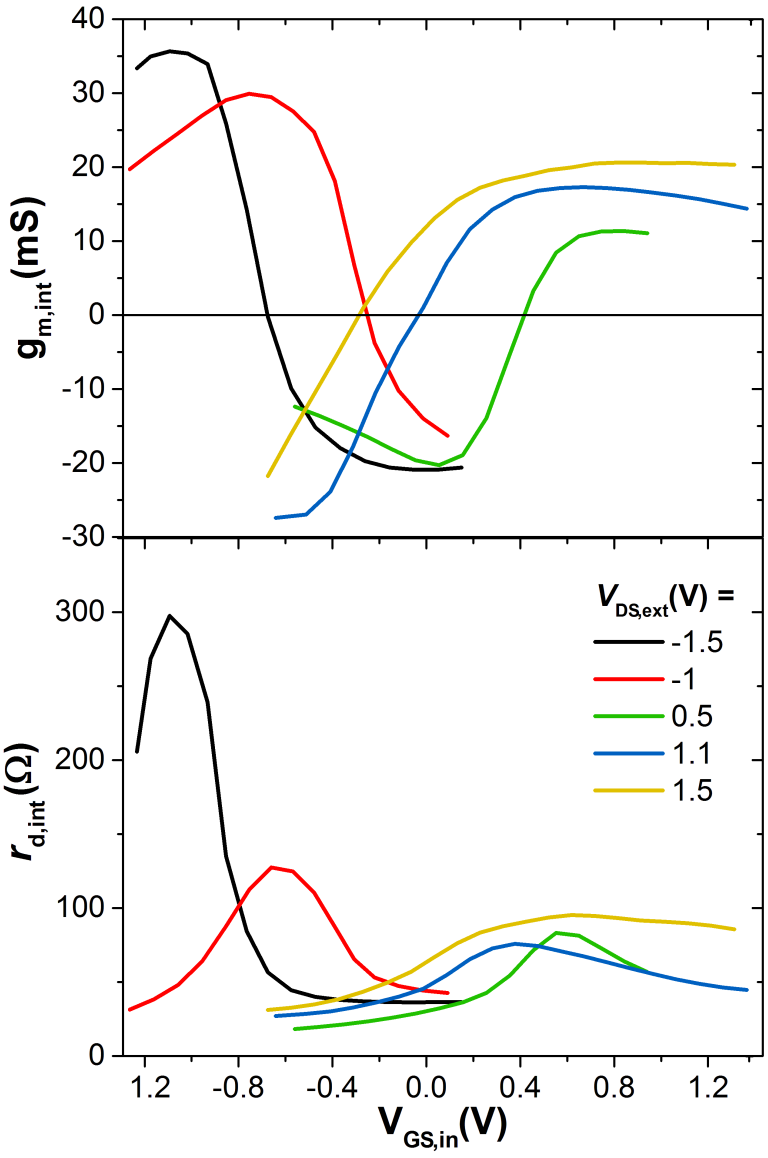

Figure 5.10: Simulated intrinsic transconductance and output resistance plotted as a function of intrinsic gate voltage at different V_{DS} for a device with $L = 1$ µm and $W = 40$ µm (sample S3).

The intrinsic values of $g_{\mathrm{m,int}}$ and $r_{\mathrm{d,int}}$ can be plotted as a function of the intrinsic voltages. The intrinsic drain voltage corresponds to the effective voltage drop along the channel after extraction of contact resistances: $V_{\mathrm{DS,int}} = V_{\mathrm{DS,ext}} - I_{\mathrm{D}}(R_{\mathrm{S}} + R_{\mathrm{D}})$. The intrinsic transconductance is higher (and the output resistance lower) compared to the extrinsic values due to the extraction of contact resistances whose contribution is bias-independent.

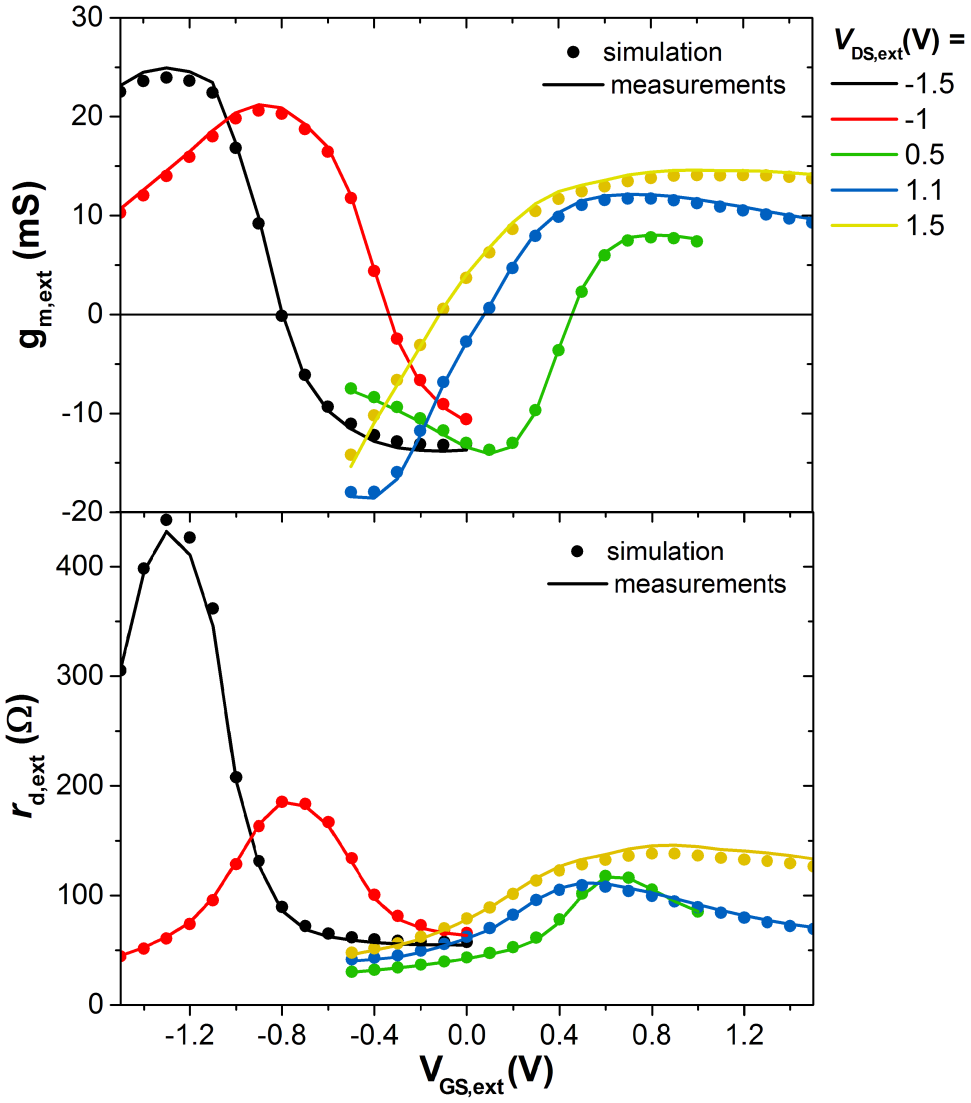

Figure 5.11: Comparison between measured and simulated extrinsic transconductance and output resistance plotted as a function of the extrinsic gate voltage at different V_{DS} corresponding to intrinsic values shown in figure 5.10. The data extracted from simulations are converted into extrinsic adding the contribution of contact resistances. Measured data correspond to low frequency $\mathrm{Re}(Y_{21})$ and $\mathrm{Re}(Y_{22})^{-1}$.

The intrinsic values can be converted into extrinsic with the following formula [100]:

$$g_{\mathrm{m,ext}} = \frac{g_{\mathrm{m,int}}}{1 + g_{\mathrm{m,int}} R_{\mathrm{S}} + \frac{(R_{\mathrm{S}}+R_{\mathrm{D}})}{r_{\mathrm{d,int}}}}$$

$$r_{\mathrm{d,ext}} = r_{\mathrm{d,int}} \left(1 + g_{\mathrm{m,int}} R_{\mathrm{S}} + \frac{(R_{\mathrm{S}} + R_{\mathrm{D}})}{r_{\mathrm{d,int}}} \right)$$

and then compared to the extrinsic values recorded from measurements at each bias point. The extrinsic values used for comparison correspond to $g_{\mathrm{m,ext}} = \mathrm{Re}(Y_{21})$ and $r_{\mathrm{d,ext}} = \mathrm{Re}(Y_{22})^{-1}$ at the lowest frequency of 10 MHz . The agreement between measurements and simulations indicates that the model used for the extraction is good. The extrinsic values could also be extracted from DC values that are recorded before each frequency sweep. However the devices instability make them sensitive to the bias sweep order. When sweeping V_{GS} at different V_{DS} only $g_{\mathrm{m,ext}}$ could accurately be extracted, while by sweeping V_{DS} at different V_{GS} only $r_{\mathrm{d,ext}}$ could accurately be extracted. However, since only one type of sweep is used in measurements, the two data are not simoultaneusly available.

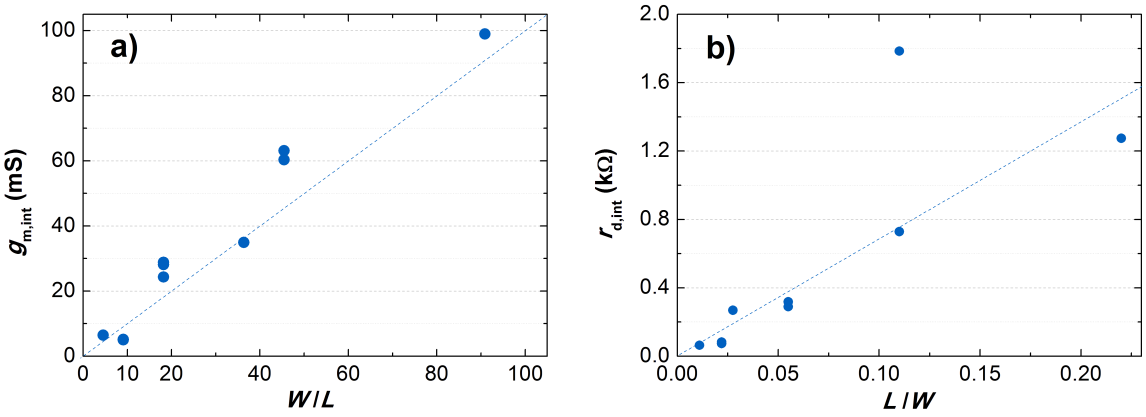

Figure 5.12: Scaling of intrinsic transconductance (a) and output resistance (b) extracted from simulations. Each point corresponds to a single device (sample S3) measured at the bias point for which the f_{max} reaches maximum.

Following model validation, the scaling of intrinsic parameters with gate length has been investigated. The choice to analyse intrinsic instead of extrinsc parameters depends on the fact that contact resistances are independent of the gate lenght while the resistance of interconnects are constant. Thus both resistances have a larger effect on the performances of smaller devices. Recalling the equations (3.4) and (3.5) that describe the transconductance and output resistance derived in the linear regime, the transconductance is expected to scale like W/L and the output resistance like L/W. This trend is confirmed in the plots shown in figure 5.12.

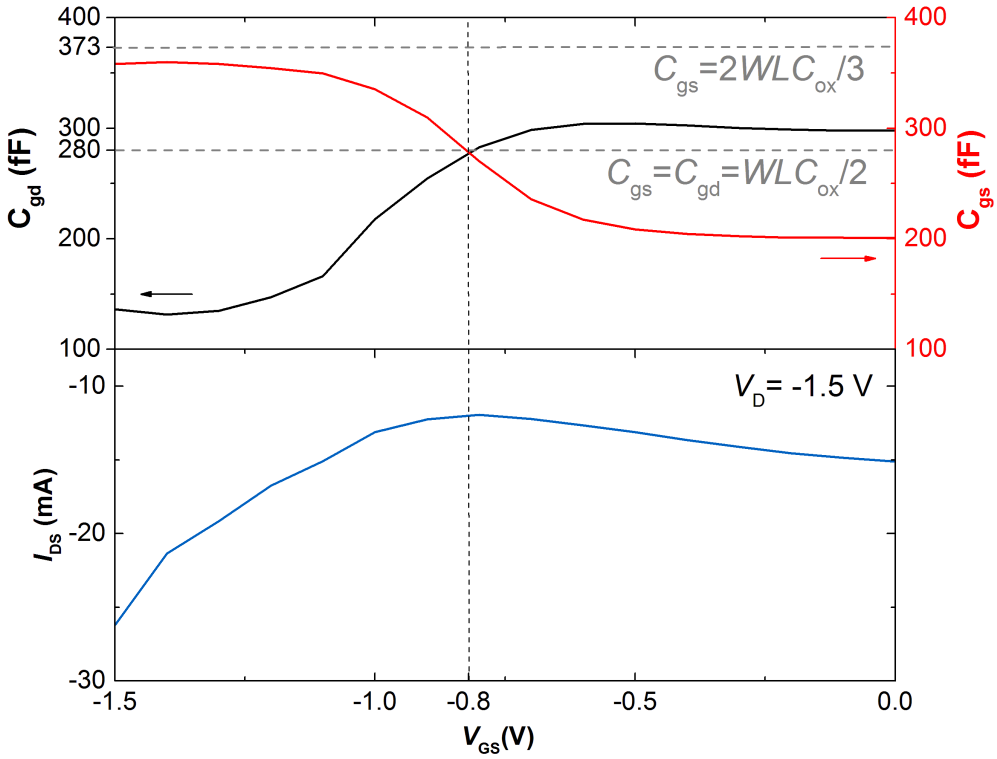

Figure 5.13: C_{gs} and C_{gd} extracted from device simulations, at the drain bias providing the highest f_{max}, as a function of the gate bias for a device with $L = 1$ µm and $W = 40$ µm. The lines showing the trend expected for an equivalent MOSFET in linear operation and deep saturation. Drain current versus gate voltage is also plotted. At the Dirac point the capacitances switches.

As described in section 5.3, the intrinsic capacitances of GFETs cannot be described as in standard MOSFETs. Considering the charge profile in the channel at different bias conditions the capacitances should be equal, following equation (5.7), whenever the charge distribution in the channel is symmetric, corresponding to the gate bias at which resistance peak occurs. When the device is in the pseudosaturation the formula (5.8) does not hold, because the carrier density in the pinch-off region, even though very small, never vanishes so that the capacitance below the contact cannot be neglected. Figure 5.13 shows the extracted intrinsic capacitances versus gate voltage and the corresponding drain current for a representative device. When channel exhibits majority-hole conduction, we observe a large current and a large difference between capacitances, a trend that approaches the MOSFET limits. At the Dirac point the capacitances are equal, as expected. In the majority-electron conduction region, the current modulation is lower and the total current does not reach the highest values reached in the hole branch, possibly because a larger part of the applied voltage drops on the p-n junction of the contact. The effect of reduced current is a lower total capacitance $C_T = C_{\mathrm{gs}} + C_{\mathrm{gd}}$.

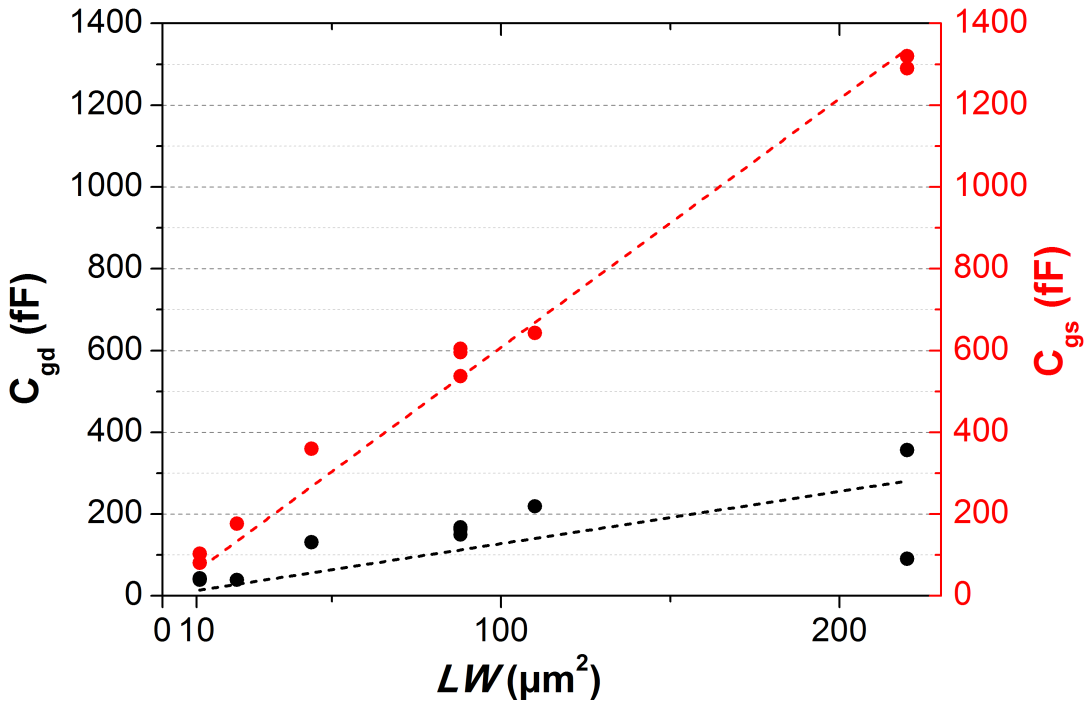

Figure 5.14: Scaling of intrinsic $C_{\rm gs}$ and $C_{\rm gd}$ capacitance, extracted from simulations, as a function of channel area. Each point corresponds to a single device (from sample S3) measured at the bias point for which the $f_{\rm max}$ reaches its maximum.

Figure 5.14 shows the capacitances of all measured devices plotted as a function of the gate area. The values were extracted from the optimized device model at the bias point at which $f_{\rm max}$ was the highest. The slope of the C vs. LW plot should be proportional to $C_{\rm ox}$/n with $C_{\rm ox}$=14 fF/μm^2. The values extracted from the plot are n = 7/3 for $C_{\rm gs}$ and n = 11 for $C_{\rm gd}$, leading to the following empirical expressions for capacitances observed in the pseudosaturation regime:

$$C_{\rm gs,ps} \approx \frac{3C_{\rm ox}LW}{7} \quad \text{and} \quad C_{\rm gd,ps} \approx \frac{C_{\rm ox}LW}{11} \ .$$

This result is in contrast with that of reference [101] that predicts n = 1 for $C_{\rm gs}$ and n = 2 for $C_{\rm gd}$ when $V_{\rm GS} > V_{\rm DS}/2$ as in the present case. However, this would make the total capacitance larger than the oxide capacitance, which is unphysical. Instead, the measured trend is more similar to that of conventional MOSFETs, equation (5.8).

Gate and contact resistances have been extracted from the small-signal model. The gate resistance extracted from the model is higher than what is predicted by the theory (section 5.3). Theoretical values have been calculated with the expression (5.9), where $W_{\rm g}$ has been substituted by $W_{\rm eff}$ that represents the effective length of the gate-metal finger from the pad to the channel end. The $W_{\rm eff}$, for narrow devices, is much larger than $W_{\rm g}$, because the

channel is patterned in the middle of the gate fingers. The resistance associated with the large pads has not been taken into account in calculations, and this can underestimate the real gate resistance. Despite some deviations, the scaling trend is uphold by the model and the predicted values are reasonable.

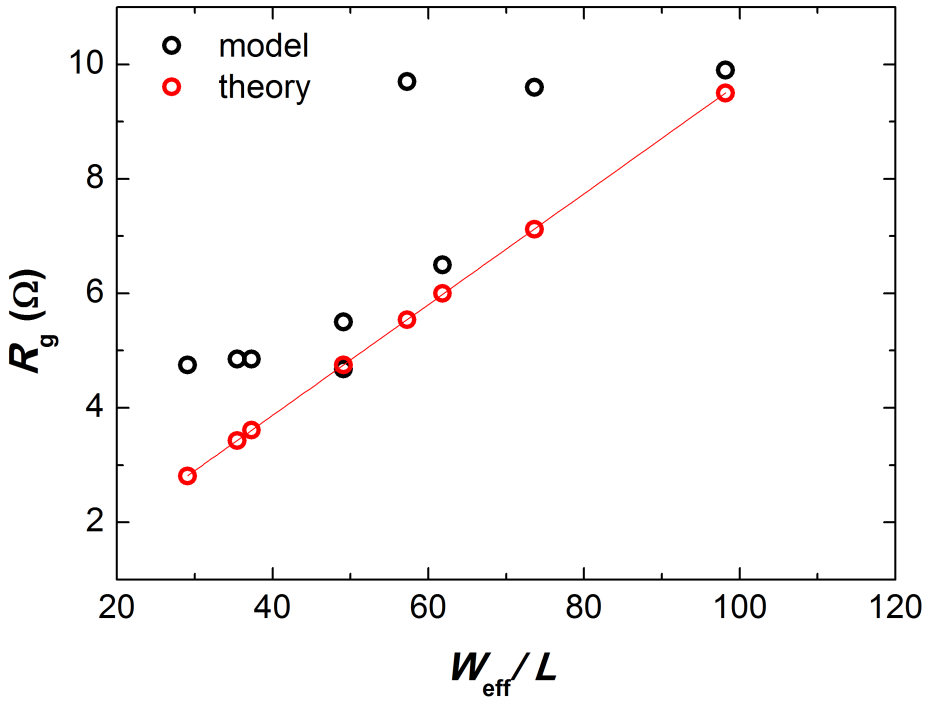

Figure 5.15: Modeled and theoretical gate resistance versus W_{eff}/L. The effective gate width considered in the calculations is larger than the channel width and corresponds to the length of the gate metal line from the pad to the end of the channel. This is an underestimation of the real gate resistance that comprises a contribution from the pad (although the difference is expected to be small).

The contact resistance profile resulting from this model is rather unexpected. In all simulations (that have been performed for ten different devices) the drain resistance is almost twice the source resistance in both positive and negative bias ranges. Considering that the contact resistivity is purely dependent on the contact width rather than on the contact area [71], this result has no proper physical explanation. Indeed, if the difference is caused by the formation of p-n-p junctions in the contact area, it would be largely bias dependent, and for negligibly small V_{DS} the contacts should be equal [72], which is not the case. However, if the carrier injection depends on the contact area, it is reasonable to expect a larger contact resistance for the smaller drain contact because the ratio between source and drain contact areas is $A_{\text{S}}/A_{\text{D}} = (L_{\text{S}}W_{\text{S}})/(L_{\text{D}}W_{\text{D}}) = L_{\text{S}}/L_{\text{D}} = 50$.

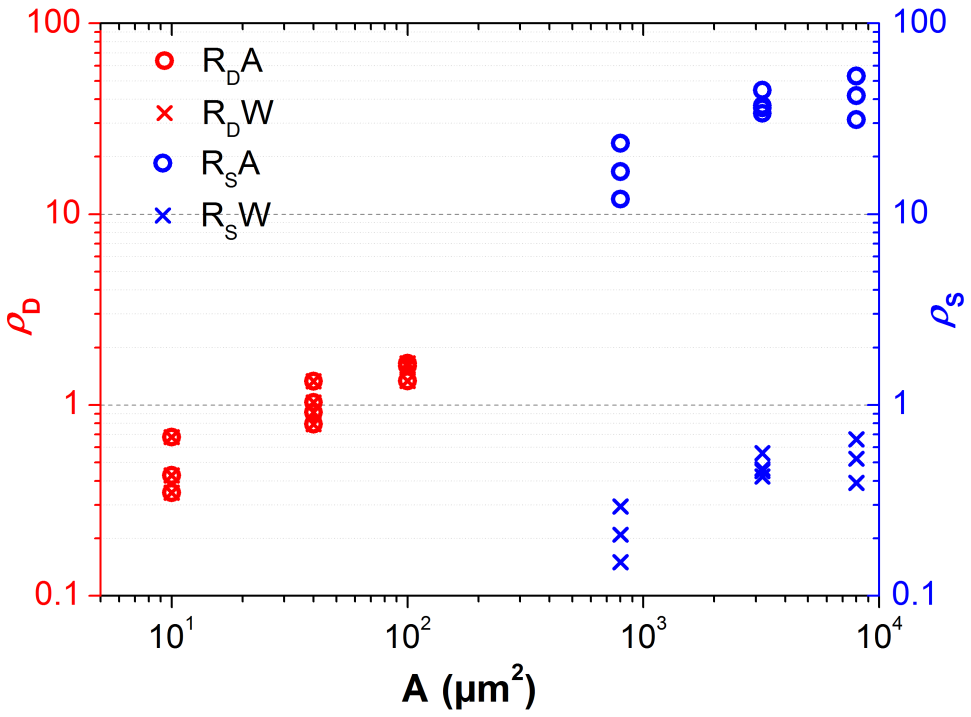

Figure 5.16: Drain (red) and source (blue) contact resistivity calculated as RW (Ωμm) and as RA (Ωμm^2).

The current gain h_{21} and Mason's gain U have been measured to extract the small-signal FOMs f_{T} and f_{max}. Open-circuit voltage gain A_{v}, $|S_{21}|$ and the transducer power gain G_{T}, directly proportional to S_{21}, were investigated. Unlike the Mason's gain, defined for a unilateral matched-circuit, the transducer gain is a measure of the real power amplification of the device and it depends on the measurement conditions. In order to have $G_{\mathrm{T}} > 1$ it is not sufficient to provide $|S_{21}| > 1$ (that would be the case if the device is perfectly-matched, see equation (5.6)). From a simple intrinsic model of the GFET (and considering $C_{\mathrm{gs}} >> C_{\mathrm{gd}}$) the expression for $|S_{21}|$ can be approximated as [100]$|S_{21}| \approx -2Z_0 g_{\mathrm{m,ex}}/(1 + Z_0 g_{\mathrm{d,ex}})$. Since both g_{m} and g_{d} increase linearly with gate width W, the $|S_{21}|$ increases monothonically with W. We found in experiments that all devices with $W = 10$ μm exhibit $|S_{21}| < 0$ dB. The highest measured $|S_{21}|$ is 12.5 dB for a ten times larger device. This value is also the highest reported in literature [100].

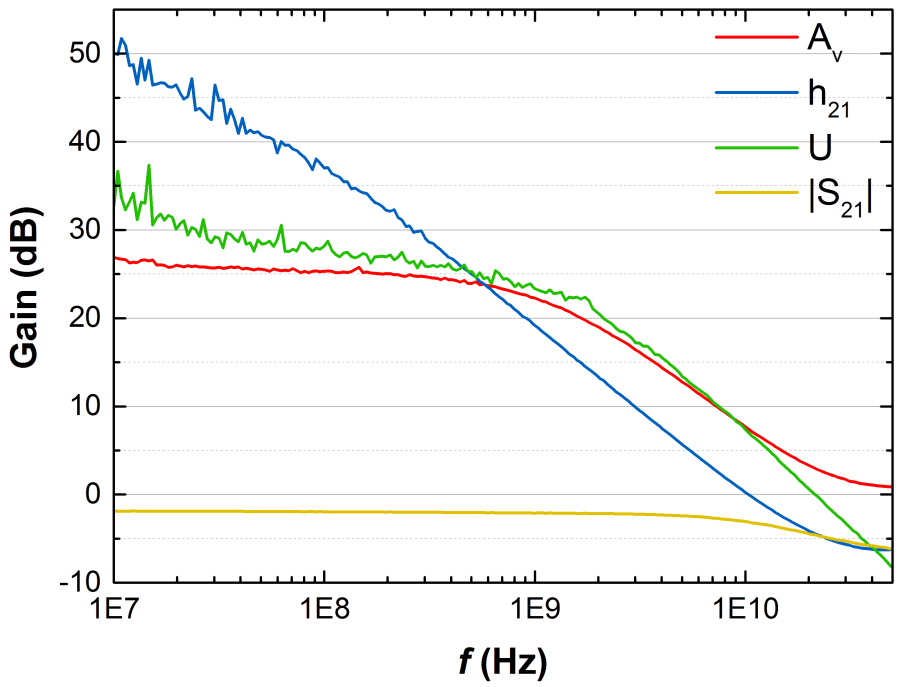

Figure 5.17: Measured extrinsic current gain h_{21}, Mason's gain U, intrinsic voltage gain A_{v} and $|\mathrm{S}_{21}|$ as a function of frequency for a device with L= 1 µm and W= 10 µm (sample S4).

The intrinsic gain, $A_0 = g_{\mathrm{m}} r_{\mathrm{d}}$, of the GFET is equal to the open-circuit voltage gain $A_v = |z_{21}| / |z_{11}|$ at low frequencies, and therefore can be extracted from S-parameter measurements. The largest intrinsic AC gain measured is above 30 dB for a device with L = 1 µm and W = 10 µm, and it is also the highest value reported in literature for devices with comarable gate length [81, 53, 62].

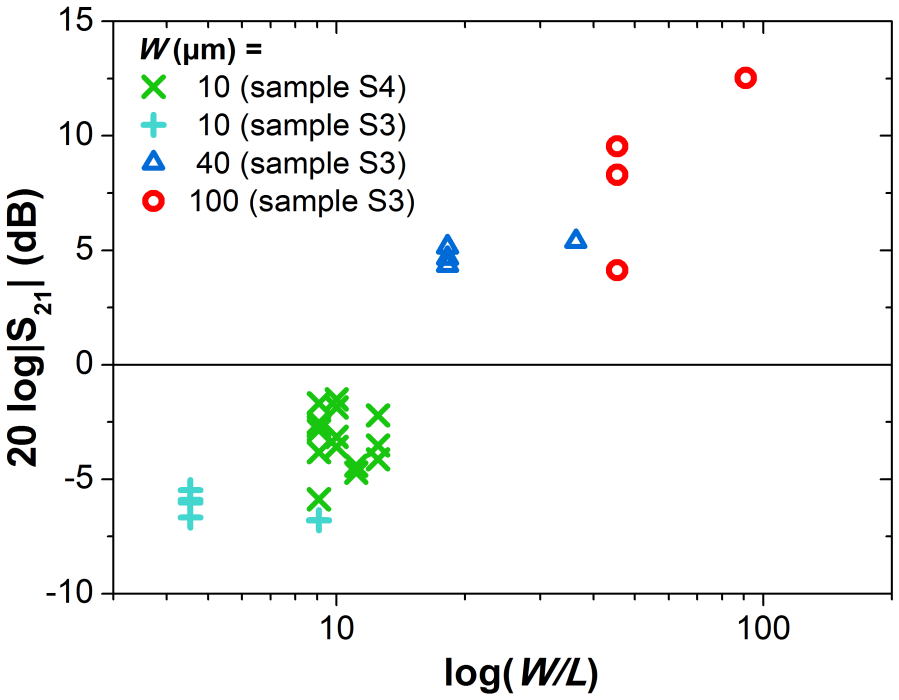

Figure 5.18: Plot of log|S21| vs. log(W/L) showing a linear dependence.

f_T and f_{max} have been extracted for all devices at the bias point in which they reach the maximum value. The choice of comparing the maximum values instead of chosing a reference bias point equal for all devices has been dictated by the large performance variability that is usually exhibited by CVD GFETs. At an arbitrary bias point the devices are likely to have different doping profiles and charge distributions, therefore a comparison of their properties would be meaningless. In order to limit the dispersion of values, all devices have been tested only in the negative V_{GS} and V_{DS} range. The highest measured f_T is 10.3 GHz in the device with W = 10 µm and actual L = 1 µm, that is about forty times smaller than the highest value reported in literature, 427 GHz for a device with W = 5 µm and L = 67 nm [82]. The scaling trend $1/L$ indicates that to obtain a similar value it would not be sufficient to preserve the scaling of all other intrinsic parameters, but also a higher channel mobility would be required. The feature that mostly affect post-processing mobility is the oxide/graphene interface quality, suggesting that better results could be possibly obtained with a better control on the oxidation process, pheraps using ALD oxides.

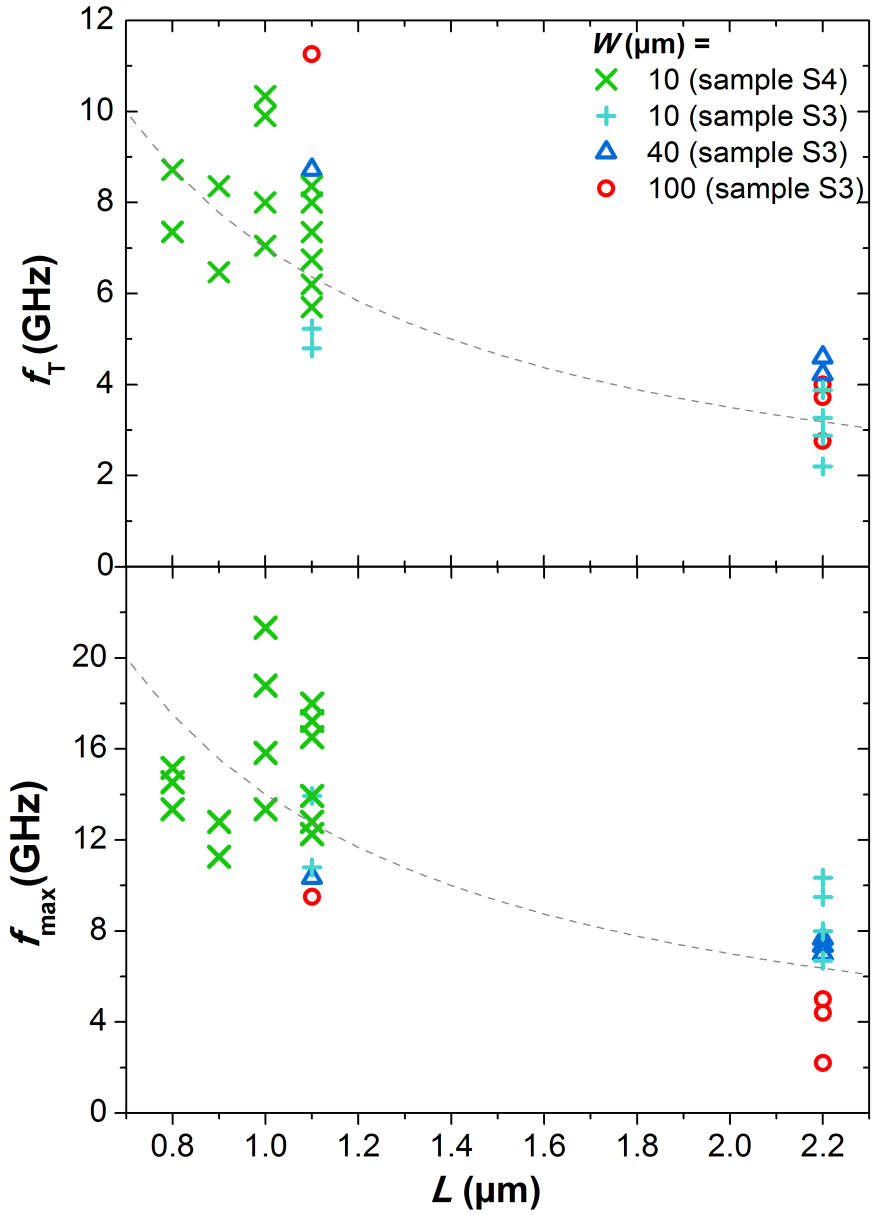

Figure 5.19: Measured f_T and f_{max} for devices with different gate lengths (samples S3 and S4). f_{max} and f_T are the maximum values measured for each device (the bias point providing this condition varies from device to device). A hyperbola L^{-1} suggests the scaling trend expected for f_T and f_{max} as a function of gate length L.

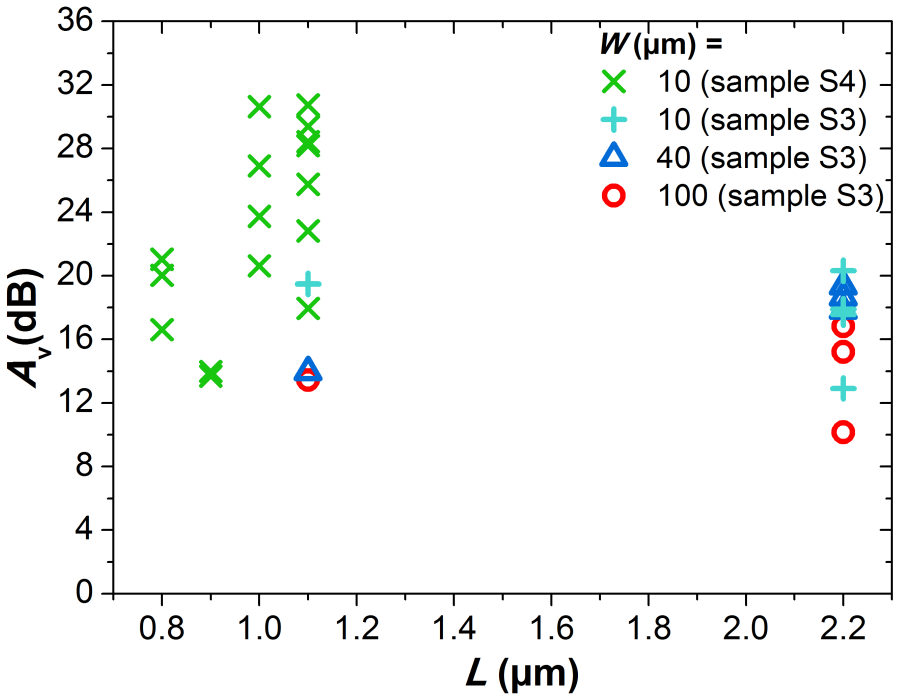

Figure 5.20: The low-frequency open-circuit voltage gain measured for devices with different gate lengths (samples S4 and S5). The values correspond to the maximum values measured for each device (the bias point providing this condition varies for each device). Since $|A_v| = g_m r_d$ at low frequency, the gain should not scale with gate length and width.

The highest measured $f_{\max}$ is 21.3 GHz in a device with $W = 10$ µm and $L = 1$ µm, that is about 5 times smaller than the record value of 105 GHz obtained in a device with $W = 14$ µm and $L = 100$ nm [84]. In this case the performance comparison is better, although it has been reported that $f_{\max}$ does not seem to scale with length in graphene devices [21], therefore a further reduction of gate resistance, with a possible implementation of T-gate structure [102], and contact resistance reduction should be considered for further performance improvements.

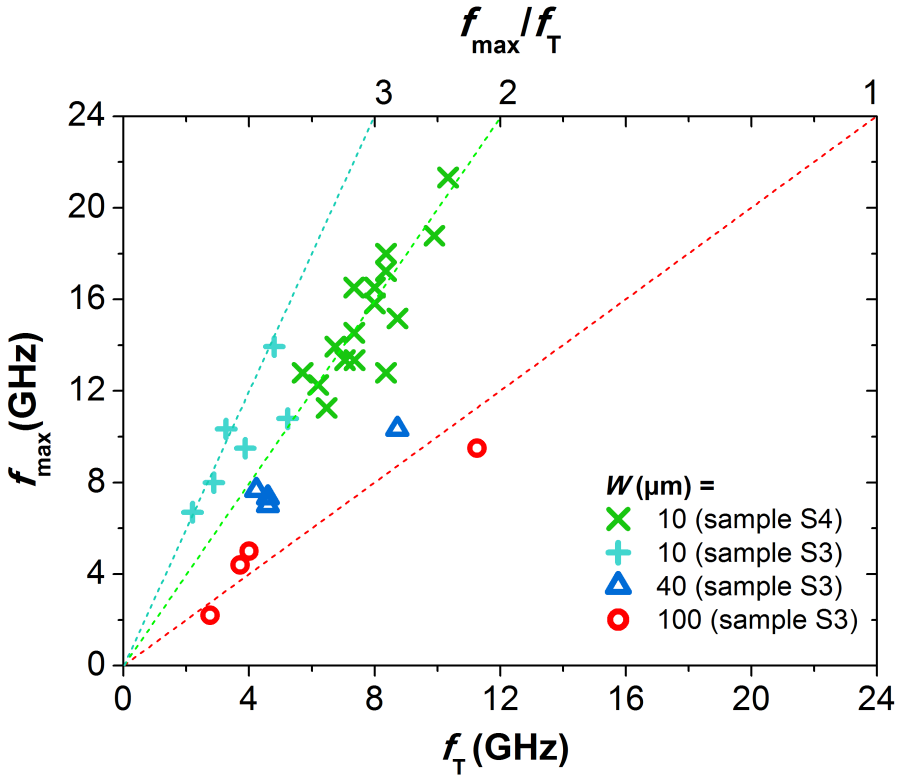

Figure 5.21: Measured $f_{\max}/f_{\mathrm{T}}$ ratio for devices with different gate sizes (from S3 and S4). $f_{\max}$ and f_{T} are the maximum values measured for each device (the bias point providing this condition varies for each device).

An important parameter to consider is $f_{\max}/f_{\mathrm{T}}$. In standard InP and GaAs HEMTs, the fastest technology available, this ratio is about 2 [21]. In GFETs, however, $f_{\max}$ is usually smaller than f_{T} [103, 104], and the highest ratio reported in literature is 1.5 attributed to the low intrinsic capacitances and gate resistance arising from an embedded T-gate structure [102]. In the present work the highest measured $f_{\max}/f_{\mathrm{T}}$ was 3.1, with an average of 2 for sample S4, see figure 5.21, considerably outperforming the state of the art for graphene technology. Considering the formula (5.2) and (5.4) $f_{\max}$ can be expressed as a function of as f_{T} [102]:

$$f_{\max} = \frac{f_{\mathrm{T}}}{2\sqrt{g_{\mathrm{d}}(R_{\mathrm{g}} + R_{\mathrm{S}}) + 2\pi f_{\mathrm{T}} R_{\mathrm{g}} C_{\mathrm{gd}}}}.$$

This expression enlights the impact of a large r_{d} on $f_{\max}$. Hence, a possible explanation for the record $f_{\max}/f_{\mathrm{T}}$ exhibited by these GFETs can be attributed to the good saturation, that explains also why standard GFETs, having poor saturation, show much lower $f_{\max}$. A DC analysis of the devices, shown in figure 5.22, has confirmed the exceptional saturation of these devices, that can be attributed to the ultra-small EOT, about 2 nm, allowing a better gate control on the drain current, together with a good material quality [53].

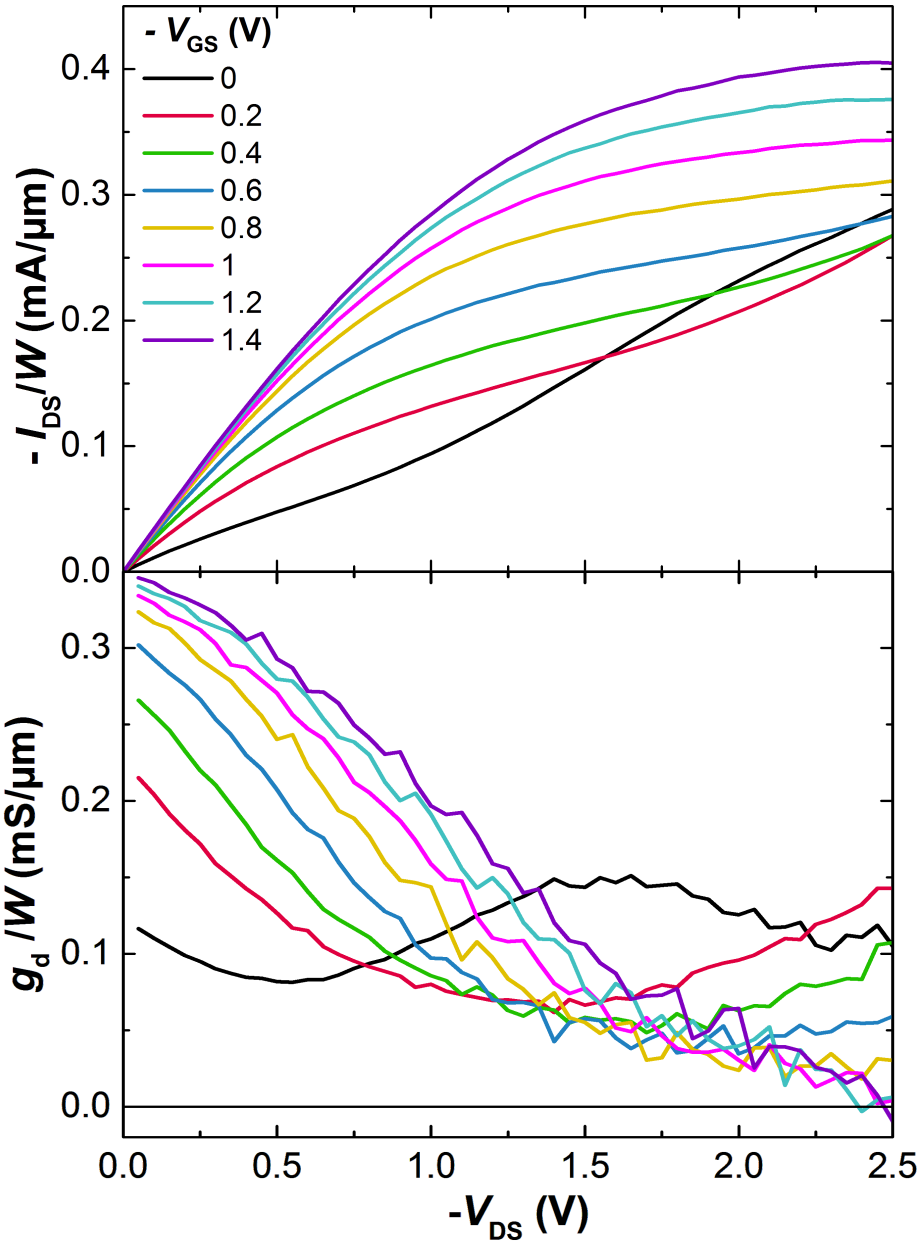

Figure 5.22: I-V characteristics for one of the best measured devices (sample S4, $L = 1$ µm, $W = 10$ µm) exhibiting $|A_v| = 26.9$ dB at low frequencies. At high $|V_{DS}|$ and V_{GS}<<-1 V the device shows good saturation confirmed by the output conductance that goes to zero.

The mechanism responsible of an improved saturation with thinner oxide can be explained as an effect of quantum capacitance. The channel capacitance is given by the series

connection of oxide and graphene capacitance. In pinch-off conditions the limited graphene DOS strongly limits the total capacitance, and this effect is larger for larger C_{ox}. Limited capacitance results in a limited carrier density, thus in current saturation [53].

The same plot shows that at very large drain and gate biases the GFET exhibits negative differential resistance (NDR). This phenomenon has been previously reported [53, 105] and has been attributed to the ambipolar nature of graphene. The theory states that current decreases after pseudosaturation reaching a minimum when Dirac point is in the middle of the channel [105]. In figure 3.3 the shift was caused by gate bias sweep producing qualitatively the same effect. In order to detect the NDR, a low contact resistance and small EOT, like those in samples S3 and S4, are required. Theoretical studies have focused on the possible exploitation of this effect to enhance the voltage gain in RF application, revealing that NDR is obtained at the expense of a reduced transconductance [106]. However, the increase of voltage gain above the intrinsic value is limited to only extremely small AC input voltages and therefore the use of NDR in realistic applications is not feasible [106].

Chapter 6

Conclusion and outlook

In this PhD work high performance graphene inverters based on high-$\varkappa$, thin dielectric, have been demonstrated. These inverters show a record AC gain above 11 dB at 1 kHz. The good and homogeneus performance obtained with these CVD-graphene devices led to the demonstration of first gigahertz integrated ROs. ROs with a gate length of 0.9 µm exhibited the highest oscillation frequency of 4.3 GHz, with signal amplitude primarly limited by the bandwidth of the setup rather than by intrinsic device characteristics. The effect of scaling on device performance has been investigated, showing that this technology is not efficient when gate length is scaled below 500 nm, due to detrimental effect of contact resistances that do not scale. Different metals have been tested to reduce contact resistance. Tests have been performed in parallel, with direct implementation of metal contacts in ROs and with fabrication of TLM structures for two-probe and four-probe measurements. Experiments have shown that pure Au contacts (without adhesion layer) provide the lowest contact resistance ~ 200 Ωµm. The fabricated ROs have been tested as analog mixers and amplitude modulators, operating in the gigahertz frequency range, to demonstrate some possible applications. Among the noticeable results it should be mentioned that this is the first demonstration of a graphene mixer with bult-in graphene-made local oscillator.

Aiming to further improve the performances of these complex circuits and to extend their frequency capability, single GFETs have been fabricated and characterized by S-parameter measurements. A small-signal model of GFETs has been proposed and tested, and the investigation has enlightened the dynamics of small-signal device operation. The model exhibited good agreement with measurements, at least for wide GFETs, while the uncertanty on narrow GFETs is larger, probably due to the weaker signal leading to lower signal/noise ratio. The small-signal FOMs extracted from these devices reveal an exceptionally high $f_{\max}/f_{\mathrm{T}}$ ratio above 3. Moreover, high intrinsic open circuit gain $A_{\mathrm{v}} > 30$ dB (with $W = 10$ µm, $L = 1$ µm) and high $|\mathrm{S21}| > 12.5$ dB (with $W = 100$ µm, $L = 1.1$ µm) have been reported, outperforming the state of the art to the best of our knowledge. A comparison with current III-V technology in terms of cutoff and oscillation frequency is shown in figures 6.1 and 6.2, updated from reference [21].

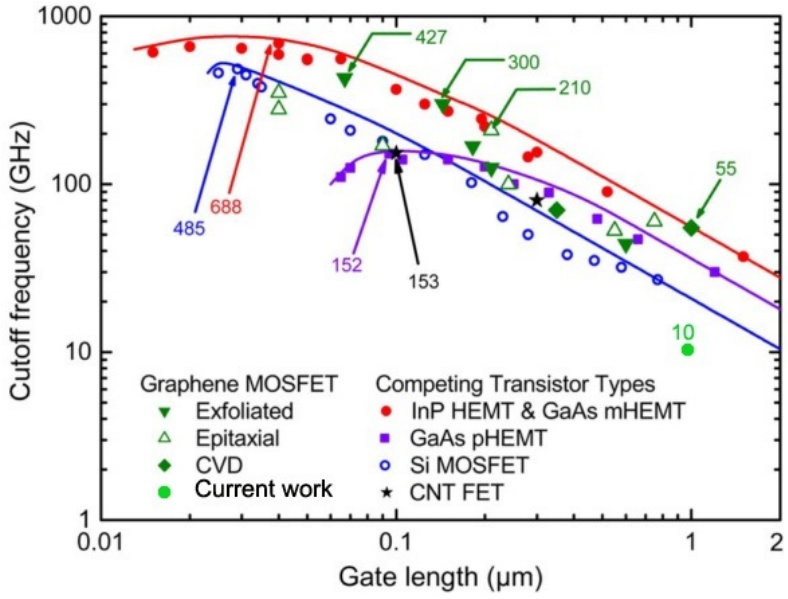

Figure 6.1: State of the art of GFETs cutoff frequency vs. gate lenght compared with competing technology: carbon nanotubes FETs, InP HEMTs and GaAs metamorphic HEMTs, GaAs pseudomorphic HEMTs and Si MOSFETs. The plot is taken from reference [21] and updated with the present results.

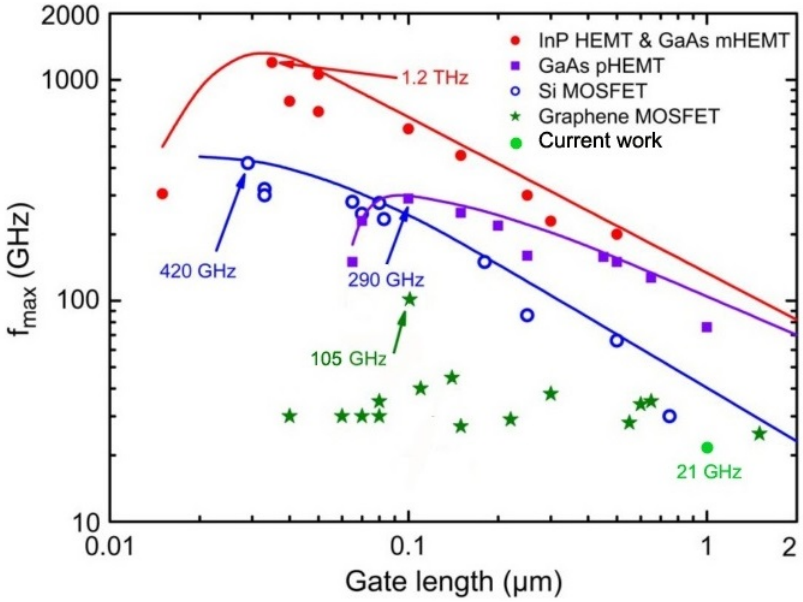

Figure 6.2: State of the art of GFETs maximum oscillation frequency vs. gate lenght compared with competing technology: carbon nanotubes FETs, InP HEMTs and GaAs metamorphic HEMTs, GaAs pseudomorphic HEMTs and Si MOSFETs. Taken from reference [21] and updated with the present results.

While in terms of cutoff frequency the devices demonstrated in this work are outperformed by the state of the art of GFETs, in which f_T is about five times higher than here, the f_{max} follows the trend exhibited by graphene MOSFETs. However, the plot shows clearly that GFETs performance in terms of f_{max} poorly compare with other technologies, in particular with the high-frequency InP HEMTs and GaAs mHEMTs, capable to reach THz operation. The low f_{max} values stem from the poor current saturation of GFETs, although the exceptionally good saturation observed in the investigated devices suggests a possible improvement if other parameters are adequately controlled.

The main characteristics affecting device performances have been discussed through the thesis and will be briefly highlighted here. One of the main tasks is to reduce the contact resistance below 100 Ωμm. Such ultra-low contact resistance values have been demonstrated with heavily-doped graphene on SiC [107], but not yet with low-doping CVD-grown graphene. On CVD graphene, protecting the graphene channel from resist contamination through the deposition of a sacrificial Al layer has resulted in low-contact resistance values down to 200 Ωμm [108]. We have tested this process in the fabrication of our devices, but without appreciable results. The Al removal through a TMAH solution represented a critical step since it also promotes graphene detachment from the substrate damaging the channels. Another strategy to improve contact quality is based on thermal annealing, although the output of these processes severely depends on the pressure/temperature conditions, on the contact metal, resist type and deposition method [109, 110]. Thermal annealing in vacuum at different temperatures have been tested on our conventional GFETs, with no evidence of improvements. It should be noted that post-deposition annealing is expected to be beneficial because it promotes the formation of better quality metal interfaces. Very small and regular metal grains are known to provide lower contact resistance [69]. However, SEM imaging of our Au contacts show regular grains with an average diameter of about 50 nm, indicating that annealing is not necessary (figure 6.3). A more promising solution [111] that is currently under investigation consists of holes-patterning in the graphene channel below the contacts to increase the interfacial edges useful for carrier injection. This method has already demonstrated some promising results, currently under evaluation, but it needs to be implemented with back gate tuning of the channel doping level below contacts.

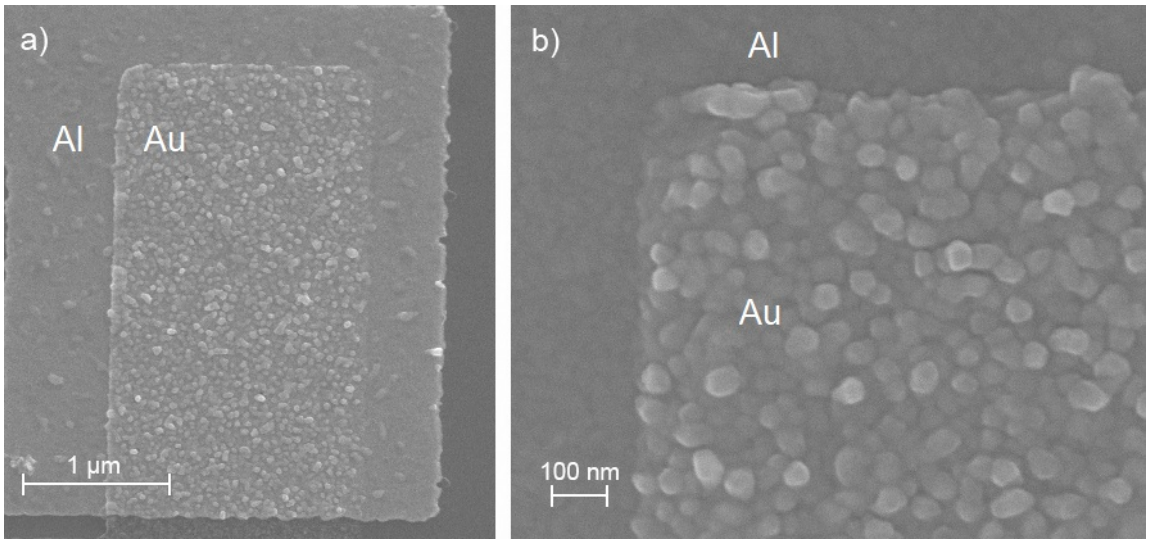

Figure 6.3: a) SEM image of an e-beam evaporated Au electrode overlapped to an Al contact. b) Zoom-in on the contacts showing the Au grain size.

Another fundamental task is the improvement of dielectric quality. Graphene-dielectric interface is of a great importance since dielectric roughness causes scattering phenomena that affect mobility. Dielectrics also introduce new charge-trapping sites causing hysteretical behaviour of device I-V characteristics. Evaporation method allows only a limited control on the oxide properties, since oxidation of Al occurs as a spontaneous process after metal deposition. A possible solution to improve interfaces could be the use of different deposition methods (e.g., ALD) that rely upon self-limited chemical reactions to control the ultimate oxide thickness and the kinetics of oxide formation. A further opportunity is to switch to novel dielectris, like the high-$\varkappa$ HfO_2 ($\varkappa$=25) or TiO_2 ($\varkappa$=80) [112], currently under investigation in our research group, or the two dimensional hexagonal-BN that provides flat surfaces [45, 113, 114, 115, 47]. However, the high-$\varkappa$ oxides are tipically characterized by defective surfaces and large phonon scattering, while the main limitation of h-BN is related to the lack of high-quality material by CVD growth, and to the integration of the transfer methods in a scalable industrial process.

Concerning device stability it has been observed that the channel doping profile, when not properly passivated, change with time. High biases and high currents anneal the device resulting in a shift of the Dirac point. It has been proved that flowing nitrogen on the devices during measurements helps to keep the devices more stable [24]. Hence, we have inferred that, during measurements, the high voltages applied to the channel, in particular across the back gate oxide (biased up to 200 V), attracts the charged impurities present in the enviroment and dope graphene. This problem affects in particular the devices with uncovered access regions of the channel, like ROs. Therefore a different design providing a full channel coverage (that is actually hindered by the need to avoid short circuits, as described in chapter 4) could be beneficial in improving device stability.

To conclude, even if researches would be capable to address all the problems enlightened, there are still fundamental issues that restrain graphene applications in the mainstream electronics. As mentioned, monolayer GFETs exhibit intrinsically high static power dissipation, therefore they are not feasible for digital electronics. Therefore, unless the attempts to open a bangap through nanopatterning or electric fields can bring satisfactory outcomes, an effective solution to this limitation seems still far to come.

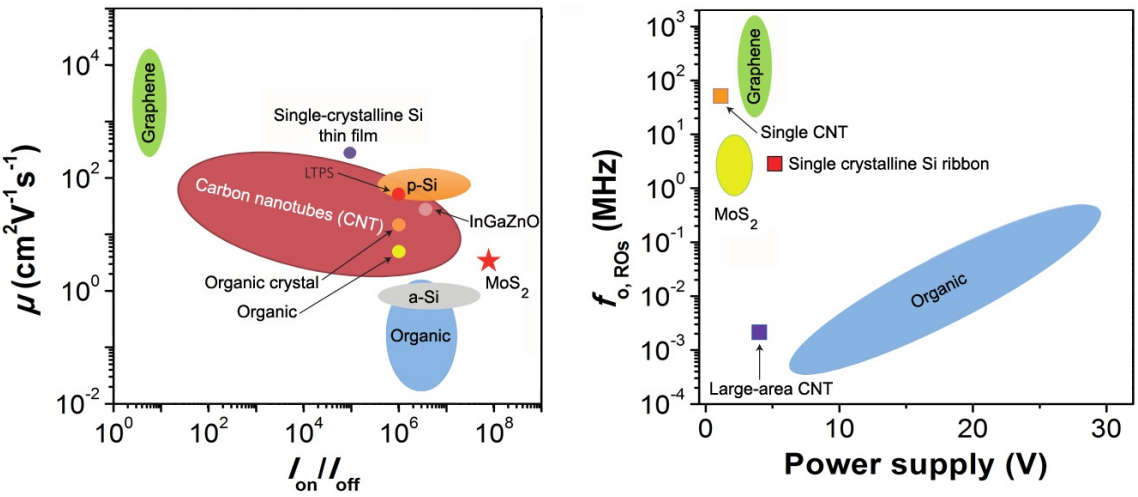

Figure 6.4: a) Tradeoff between carrier mobility and on-off ratio (bandgap related) for graphene and other relevant technologies. b) ROs oscillation frequency versus power supply for different technologies. Plots taken from reference [6].

Regarding graphene industrial applicability, the field of flexible and analog electronics is among the most promising. Indeed, compared to organic-based electronics, graphene offers superior transport properties, like a mobility two orders of magnitude higher than the best organic semiconductors [6, 116]. However, the fabrication of completely bendable electronic devices requires all components (including the battery) to be flexible, and the path to develop such a technology on industrial scale is perhaps not mature yet.

Interesting possibilities are ultimately offered by novel heterostructures, combining the unique properties of different 2-D materials like graphene, BN and MoS_2, where graphene has been either employed as material for interconnects or as a channel for field-effect Shottky barrier or tunnelling transistors [117, 118, 119, 120]. The research on 2-D materials represents a hot topic, so we believe that the we will witness great progresses in the near future.

Appendix A

Large signal model of ROs

As discussed in the main text, the oscillations of the RO are triggered by a noise component at a certain frequency that introduces a positive feedback in the loop. Once the oscillations are initiated, the signal waveform grows in amplitude until it settles to a saturated value and the small-signal model is not valid anymore to describe the system. To model the transmission of the large signal in the circuit, the delays introduced by each stage should be taken into account. A single stage can be modeled as the output resistance of an inverter in series with the input capacitance of the next stage. Signal transmission involves the charging of the capacitors trough the discharge of the resistors by the signal voltage swing. The time constant of the stage, τ_{RC}, is:

$$\tau_{\mathrm{RC}} = (R_{\mathrm{ON}}||R_{\mathrm{OFF}})(C_{\mathrm{M}} + C_{\mathrm{gs}}) \approx (R_{\mathrm{ON}}||R_{\mathrm{OFF}})C_{\mathrm{G}}(2 + A_v) \tag{A.1}$$

where the approximation that $C_{\mathrm{gs}} = C_{\mathrm{gd}} = C_{\mathrm{G}}$ has been introduced, thereby neglecting the gate dependence of capacitances.

The voltage of the charging inverter varies in time according to:

$$v_{\mathrm{o}}(t) = V_{\mathrm{OFF}}^{\infty} + (V_{\mathrm{ON}}^{\infty} - V_{\mathrm{OFF}}^{\infty})\mathrm{e}^{-\frac{t}{\tau_{\mathrm{RC}}}} \tag{A.2}$$

for $0 < t < \frac{T}{2}$, where V_{ON}^{∞} and $V_{\mathrm{OFF}}^{\infty}$ are the steady-state upper and lower voltage levels of the inverter.

Using the formula for a voltage divider, when the grounded FET is turned off the output voltage is:

$$V_{\mathrm{ON}}^{\infty} = V_{\mathrm{DD}} \frac{R_{\mathrm{OFF}}}{R_{\mathrm{ON}} + R_{\mathrm{OFF}}},$$

and when it is turned on the output becomes:

$$V_{\mathrm{OFF}}^{\infty} = V_{\mathrm{DD}} \frac{R_{\mathrm{ON}}}{R_{\mathrm{ON}} + R_{\mathrm{OFF}}},$$

then the voltage swing of the oscillation is:

$$V_{\mathrm{p-p}} = V_{\mathrm{ON}}^{\infty} - V_{\mathrm{OFF}}^{\infty} = V_{\mathrm{DD}} \left(\frac{R_{\mathrm{OFF}} - R_{\mathrm{ON}}}{R_{\mathrm{OFF}} + R_{\mathrm{ON}}} \right) \tag{A.3}$$

Assuming that R_{OFF} is equal to the resistance of the GFET at the Dirac point, R_0, then from (A.1) and (A.3) the time constant of each stage can be expressed as a function of known parameters:

$$\tau_{\mathrm{RC}} = \frac{R_0}{2} \left(1 - \frac{V_{\mathrm{p-p}}}{V_{\mathrm{DD}}} \right) C_{\mathrm{G}} (2 + A_v) \tag{A.4}$$

The inverter rise delay τ_i is defined as the time in which the voltage is at the treshold value: $V_{\mathrm{th}} = (V_{\mathrm{ON}}^{\infty} - V_{\mathrm{OFF}}^{\infty})/2$, hence substituting $v_{\mathrm{o}}(t)$ with V_{th} and t with τ_i in (A.2) gives:

$$\tau_i = \ln(2) \tau_{\mathrm{RC}} \tag{A.5}$$

The oscillation frequency is given by the sum of the delays per each stage, $f_{\mathrm{o}} = \frac{1}{2 \sum_i \tau_i}$ where the factor 2 takes into account both the rise and the fall time. For an unbuffered RO this leads to the simple expression $f_{\mathrm{o}} = \frac{1}{2n\tau}$ where n is the number of stages (i.e. inverters).

This simple steady-state model [24] is based on the assumption that the signal propagation in the loop is slow enough to allow the inverters to reach the steady-state before they are triggered again. Assuming that the steady-state is reached within 3 times constant this is equivalent to:

$$2 \sum_i \tau_i \geq 3 \tau_{\mathrm{RC}}$$

expressing it in a more general form valid both for buffered and unbuffered ROs, with N_{i} representing the inverter FO (N_{i}=1), and N_{n} the FO of the n-th inverter (that can be equal to 1 for unbuffered and to 2 for buffered ROs), gives the condition:

$$(n-1)\tau_i + N_n \tau_i \geqslant 3 \frac{N_i \tau_i}{\ln(2)}$$

that for the explicit case of a buffered ROs with $N_{\mathrm{n}} = 2$ and $N_{\mathrm{i}} = 1$ leads to the condition $n > 3.3$, which is not fulfilled for 3-stages buffered ROs. Since the inverters do not reach the steady-state the oscillation frequency is underestimated by this model. A better description of the system can be provided by a transient model.

In a transient model V_{ON}^{∞} should be replaced with V_{ON} in (A.2), leading to a new expression for the threshold voltage, that is:

$$V_{\mathrm{th,i}} = \frac{V_{\mathrm{ON,i}} - V_{\mathrm{OFF,i}}}{2} \tag{A.6}$$

with

$$V_{\mathrm{OFF,i}} = V_{\mathrm{OFF}}^{\infty} + (V_{\mathrm{ON,i}} - V_{\mathrm{OFF}}^{\infty})\mathrm{e}^{-\frac{T_i}{2\tau_{\mathrm{RC},i}}} \tag{A.7}$$

From (A.6) and (A.7) the following expression is obtained[24]:

$$1 + \mathrm{e}^{-\frac{T}{2\tau_{\mathrm{RC,i}}}} = 2\mathrm{e}^{-\frac{\tau_i}{2\tau_{\mathrm{RC},i}}} \tag{A.8}$$

which leads to:

$$1 + \mathrm{e}^{-\frac{T}{2\tau_{\mathrm{RC}}}} = 2\mathrm{e}^{-\frac{\tau}{2\tau_{\mathrm{RC}}}} ;\text{for} \quad 0 < i < n \tag{A.9}$$

$$1 + \mathrm{e}^{-\frac{T}{2N_{\mathrm{n}}\tau_{\mathrm{RC}}}} = 2\mathrm{e}^{-\frac{\tau_{\mathrm{n}}}{2N\tau_{\mathrm{nRC}}}} ;\text{for} \quad i = n \tag{A.10}$$

Since half of the period is equal to the sum of all the inverter delays (this corresponds to consider just the propagation of the signal in the forward direction) $\frac{T}{2} = (n-1)\tau_i + \tau_{\mathrm{n}}$, introducing the expressions for τ_i and τ_n derived from (A.9) and (A.10) yields to:

$$\frac{T}{2} = (n-1)\tau_{\mathrm{RC}}\ln\left(\frac{2}{1+\mathrm{e}^{-\frac{T}{2\tau_{\mathrm{RC}}}}}\right) + N_{\mathrm{n}}\tau_{\mathrm{RC}}\ln\left(\frac{2}{1+\mathrm{e}^{-\frac{T}{2N_{\mathrm{n}}\tau_{\mathrm{RC}}}}}\right) \tag{A.11}$$

substituting $\frac{T}{2\tau_{\mathrm{RC}}} = x$ in (A.11) gives:

$$x = (n-1)\ln\left(\frac{2}{1+\mathrm{e}^{-x}}\right) + N_{\mathrm{n}}\ln\left(\frac{2}{1+\mathrm{e}^{-N_{\mathrm{n}}x}}\right) \tag{A.12}$$

which can be solved for x to find f_{o}. For $n = 3$ it yields:

$$x = \begin{cases} \ln(2+\sqrt{5}); & \text{for} N_{\mathrm{n}} = 1 \\ \ln(3+2\sqrt{2}); & \text{for} N_{\mathrm{n}} = 2 \end{cases} \tag{A.13}$$

Therefore, for a buffered RO with N_{n}= 2, the oscillation frequency can be calculated as:

$$f_{\mathrm{o}} = \frac{1}{2\tau_{\mathrm{RC}}x} = \frac{1}{2\tau_{\mathrm{RC}}\ln(3+2\sqrt{2})} = \frac{1}{3.5\tau_{\mathrm{RC}}}. \tag{A.14}$$

Supporting information in reference [24] show a comparison between measured values and numerical simulation with the presented model.

Appendix B

Influence of probe impedence on the measurements setup

Some evidences of the importance of the measurement setup for a correct interpretation of device characteristics have been shown throughout this thesis. Metal contacts, interconnects and coaxial cables have a strong influence on device performances both at low frequencies, where they add extrinsic resistances, and at high frequencies where parasitic capacitances dephase the signal. Not only signal transmission, but also signal probing represents a critical procedure. Two practical examples of the impact of active probe impedance on the measured signal amplitude and on the output bandwidth will be given in this Appendix.

To show how the probe resistance affects the signal amplitude the ac transfer characteristics of an inverter have been measured with two different setups. A small sinusoidal signal $v_{\mathrm{IN}} = V_{\mathrm{IN}} + \mathrm{V_{in}}\sin(2\pi ft)$ with DC offset V_{IN} corresponding to the highest-gain operating point Q is applied to the gate terminal. The input and output signals are measured with an oscilloscope with high (13 pF||1 MΩ) input impedence. The output of the inverter is additionally loaded either with the high input-impedence of a Picoprobe Model 35 with Z_{IN}= (0.05 pF||1.25 MΩ), or with a 500 Ω resistor shown in figure B.1.

Recalling equation (3.8), the voltage gain of the inverter is given by

$$A_v = -2g_{\mathrm{m}}(r_{\mathrm{d}}/2||R_{\mathrm{L}}||R)$$

where R is the input resistance of the oscilloscope, that can be neglected since it is in parallel with small $r_{\mathrm{d}} \approx 500\ \Omega$. When measuring the output voltage with the active probe, the high resistance R_{L}= 1.25 MΩ can also be neglected, and the voltage gain is simply given by equation (3.9), $A_v = -g_{\mathrm{m}}r_{\mathrm{d}}$.

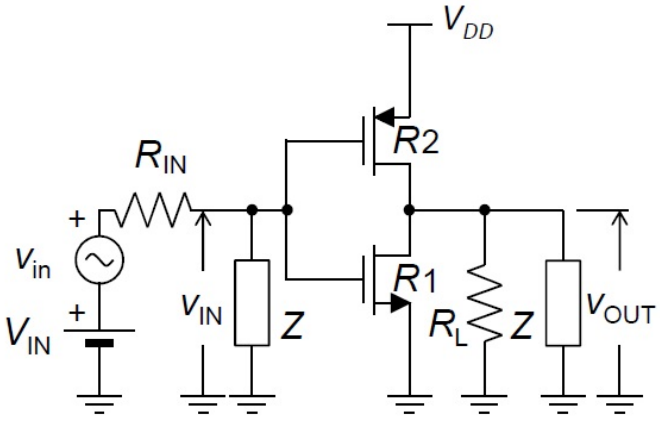

Figure B.1: Schematic of the inverter at low frequencies. $Z = R||C$, where $R = 1$ MΩ and $C = 13$ pF, is the input impedance of the oscilloscope used to measure input and output signals. The output is additionally loaded with a resistance R_{L} that can be either the high-impedence active probe (1.25 MΩ) or a resistor (500 Ω).

However, when the output is loaded with a smaller resistance, e.g. R_{L}= 500 Ω , the effect of the load cannot be neglected because it is comparable to the resistance of the device r_{d}. In this case $R_{\mathrm{L}} \approx r_{\mathrm{d}}$, and the gain reduces to $A_v = -g_{\mathrm{m}} r_{\mathrm{d}}/2$, half of the intrinsic gain of the device.

Figure B.2 shows the impact of different loads on the AC gain of the inverter. The input and ouput signal offsets have been substracted from the plots for clarity. The input voltage amplitude is V_{in}= 40 mV at $f = 1$ kHz. With high impedence load the output voltage amplitude is V_{out}= 90 mV, corresponding to an AC gain $|A_v| = V_{\mathrm{out}}/V_{\mathrm{in}} = 2.25$. With low impedence load the output amplitude is V_{out}= 34 mV, corresponding to an AC gain of $|A_v| = V_{\mathrm{out}}/V_{\mathrm{in}} = 0.85 < 1$.

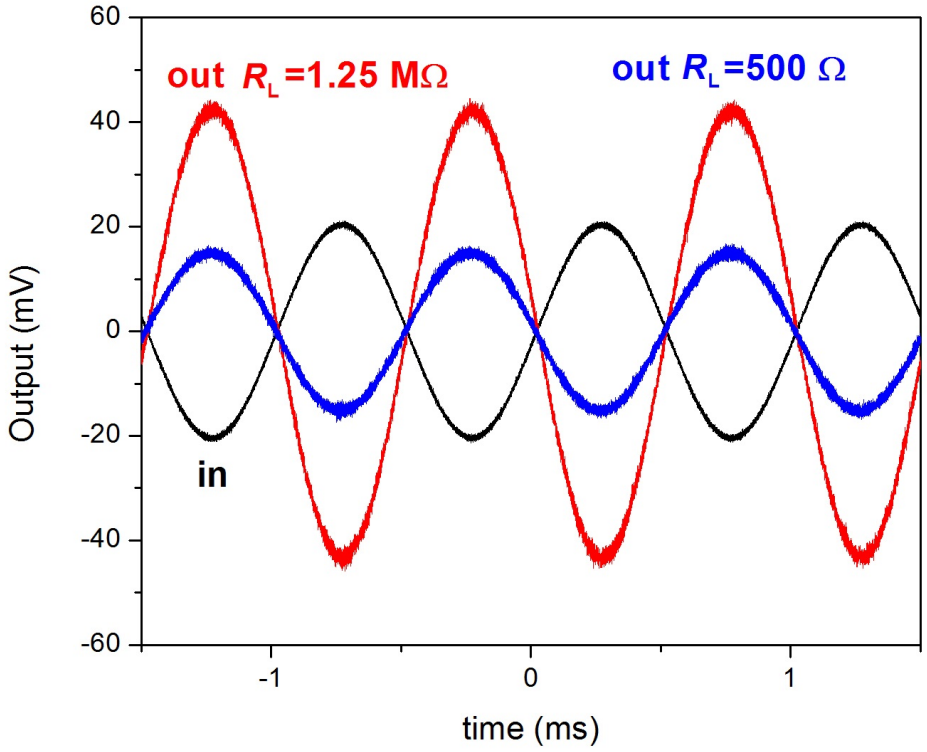

Figure B.2: Input signal with $V_{\text{p-p}}$= 40 mV, f = 1 kHz (black); output signal measured with a high-input impedence probe (R_{L}= 100 kΩ) in red; output signal measured with a resistor (R_{L}= 500 Ω) in blue. Signal offsets are shifted to zero for clarity.

Another serious issue concerning measurements is related to the maximum signal freqeuncy that can be detected, ultimately limited by the output bandwidth of the setup. The bandwidth can be determined with the circuit model shown in figue B.3, where the output resistance of the inverter, R_{o}, is connected in parellel to the high resistance of the active probe (R_{A}= 100 kΩ). The output capacitance is determined by the coupling between the output pad and the conductive substrate through the back gate oxide, connected in parallel to the negligibly small capacitance of the active probe (C_{A} = 0.08 pF).

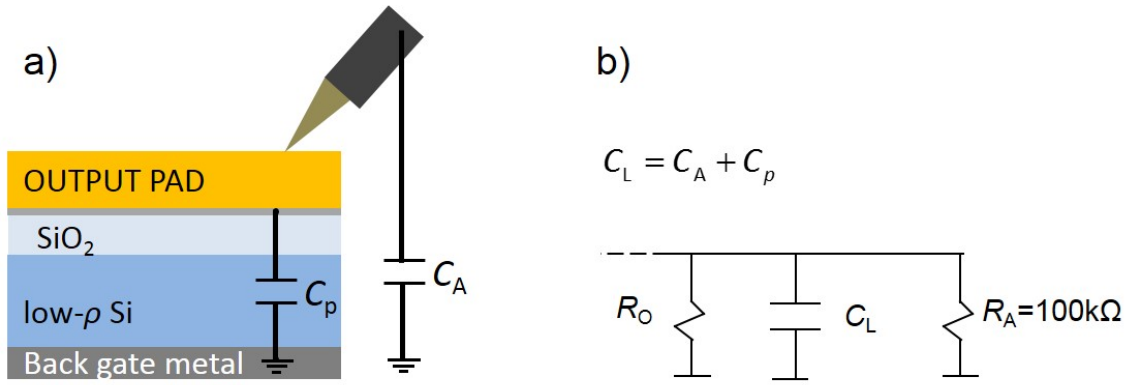

Figure B.3: a) Schematic of the measurement setup with active probe connected to the output pad coupled with the conductive substrate. b) Equivalent circuit to determine the output bandwidth of the setup.

The output resistance of the inverter is given by (4.5) and is the relevant term in the parallel connection, while the output capacitance can be expressed as:

$$C_{\mathrm{O}} = LWC_{\mathrm{BG,ox}}$$

where A is the area of the output pad. The output bandwidth is then given by:

$$f_{-3\mathrm{dB}} = \frac{1}{(R_{\mathrm{O}}||R_{\mathrm{A}})\,(C_{\mathrm{O}}||C_{\mathrm{A}})} \approx \frac{1}{R_{\mathrm{O}}||C_{\mathrm{O}}} \tag{B.1}$$

The circuit output acts as a low-pass filter that attenuates the signals of frequencies higher than $f_{-3\mathrm{dB}}$ at a rate of 20 dB/dec. The ultimate consequence is that high-frequency signals cannot be detected because their amplitude is too small (figure B.4).

The simplest solution to reduce output capacitance is to shrink the area of the output connection, as shown in figure 4.9c. However, a more efficient approach consists in replacing the conducting substrate with an insulating substrate. This modification was introduced in the process. The former substrate was 510 µm thick, heavily-doped (ρ = 0.001-0.01 Ωcm), Si wafer with 300 nm of SiO_2, while the latter substrate employed was a 480 µm thick, high-resistivity ($\rho = 5 \cdot 10^3$ Ωcm), Si wafer with 1µm of SiO_2. The drawback of using an insulating substrate results in a lack of back gate control, requiring graphene with ultra-low doping level in order to achieve signal matching. However, the recent progresses in material growth have provided a high quality material with very low doping levels (once transferred on Si substrate) that made the fabrication of working ROs possible without the need of a back gate. The oscillation frequency of these ROs is sligthly lower compared to that of backgated ROs, but this can easily be explained by the fact that the ROs can oscillate within a certain input/output voltage range in which gain and matching conditions are satisfied. The back gate can adjust the doping and tune the oscillation at the highest frequency, while this control is not possible in samples without back gate.

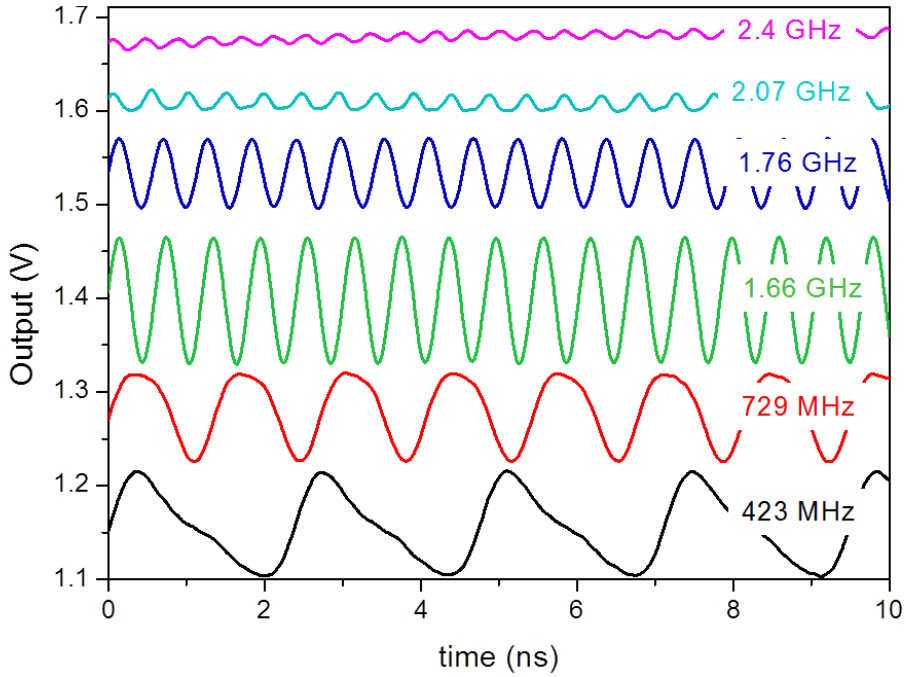

Figure B.4: Output signal at different oscillation frequencies. Fast signals have lower amplitude and detection can be difficult.

Appendix C

Unilateralization and impedence matching

Recalling sec.5.1 the $f_{\max}$ is defined as the frequency at which the unilateral power gain, U, falls to unity. The unilateral power gain measurements requires device unilateralization and impedance matching. Unilateralization means that the power gain is measured in a circuit without feedback, i.e. in a circuit in which there is only a signal transmission from input to output so that $Y'_{12} = 0$.

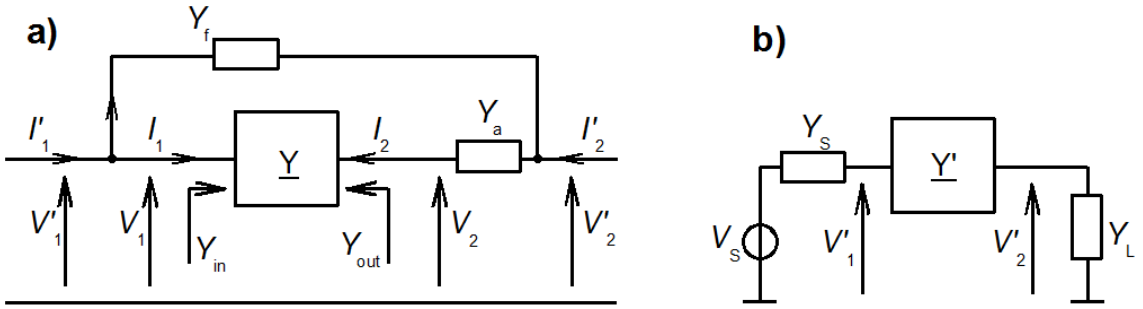

Figure C.1: Two-port network embedded in a lossless passive network providing unilateralization. Y_{a} and Y_{f} are the reactive components of the network. V and V ' are the voltages and the I and I ' are the currents of the circuit before and after unilateralization, respectively. $\underline{\mathrm{Y}}$ represents the active device impedance matrix.

The circuit can be made unilater by the insertion in a lossless network, such that shown in figure C.1a. This new circuit can be analyzed to determine the values of $Y_{\mathrm{a}} = jb_{\mathrm{a}}$ and $Y_{\mathrm{f}} = jb_{\mathrm{f}}$ that provide unilateralization.

Solving for the left node in figure C.1a gives:

$$I'_1 = I_1 + Y_{\mathrm{f}}\left(V'_1 - V'_2\right) = Y_{11}V_1 + Y_{12}V_2 + Y_{\mathrm{f}}\left(V'_1 - V'_2\right) = Y'_{11}V'_1 + Y'_{12}V'_2$$

Noting that $V'_1 = V_1$ we can rewrite the above expression as a function of V'_1 and V'_2. First

we need to solve the expression for $I_2$to find V_2:

$$I_2 = Y_\mathrm{a} + \left(V'_2 - V_2\right) = Y_{21}V_1 + Y_{22}V_2$$

that gives $V_2 = \left(Y_\mathrm{a}V'_2 - Y_{21}V'_1\right) / \left(Y_{22} - Y_\mathrm{a}\right)$. Hence we have:

$$I'_1 = \left(Y_{11} - \frac{Y_{21}Y_{12}}{Y_{22}+Y_\mathrm{a}} + Y_\mathrm{f}\right)V'_1 + \left(\frac{Y_{12}Y_\mathrm{a}}{Y_{22}+Y_\mathrm{a}} - Y_\mathrm{f}\right)V'_2 = Y'_{11}V'_1 + Y'_{12}V'_2.$$

Since unilateralization requires $Y'_{12} = 0$, we derive $Y_\mathrm{f} = Y_{12}Y_\mathrm{a}/\left(Y_{22}+Y_\mathrm{a}\right) = jb_\mathrm{f}$. Solving separately for the real and the complex part gives: $b_\mathrm{f} = b_{12} - b_{22}g_{12}/g_{22}$ and $b_\mathrm{a} = b_{12}g_{22}/g_{12} - b_{22}$.

Signal matching is accomplished by terminating the two ports of figure C.1a with complex-conjugated of the input Y'_in and output Y'_out admittances, so that $Y_\mathrm{S} = Y'^{*}_\mathrm{in} = Y'^{*}_{11}$ and $Y_\mathrm{L} = Y'^{*}_\mathrm{out} = Y'^{*}_{22}$, thereby providing the highest gain possible. The complex power is defined as: $S = P + jQ$. The input power in conditions of unilateralization and impedance matching can be calculated from the resulting circuit of figure C.1b as:

$$S_\mathrm{in} = S_1 = V'_1 I'^{*}_{11} = V'_1(V'_1 Y'_{11})^*$$

Then the input power becomes:

$$P_\mathrm{in} = \mathrm{Re}\left\{S_\mathrm{in}\right\} = \mathrm{Re}\left\{Y'_{11}\right\}\left|V'_1\right|^2 = g'_{11}\left|V'_1\right|^2$$

And the output power is:

$$P_\mathrm{out} = \mathrm{Re}\left\{S_\mathrm{out}\right\} = \mathrm{Re}\left\{S_\mathrm{L}\right\} = \mathrm{Re}\left\{Y_\mathrm{L}\right\}\left|V_\mathrm{L}\right|^2 = g_\mathrm{L}\left|V'_2\right|^2$$

The unilateral power gain is defined as:

$$U = \frac{P_\mathrm{out}}{P_\mathrm{in}} = \frac{g_\mathrm{L}}{g'_{11}}\frac{\left|V'_2\right|^2}{\left|V'_1\right|^2} = \frac{g_\mathrm{L}}{g'_{11}}\frac{\left|Y'_{21}\right|^2}{\left|Y'_{22}+Y_\mathrm{L}\right|^2} = \frac{\left|Y'_{21}\right|^2}{4g'_{11}g'_{22}}.$$

The Mason's gain is the only invariant parameter of the device, hence[83]:

$$U = \frac{\left|Y'_{21}\right|^2}{4g'_{11}g'_{22}} = \frac{\left|Y_{21}-Y_{12}\right|^2}{4\left(g_{11}g_{22}-g_{21}g_{12}\right)}.$$

It can be extracted from S-parameters measurements of the device in any condition and corresponds to the maximum power gain that could be obtained if unilateralization and impedance matching conditions are satisfied [88].

Appendix D

Alternative small-signal model for contact resistances

The contact resistance values extracted from the model in figure 5.5 show a large asymmetry between source and drain, that can hardly be explained by the physical properties of the contacts. A more accurate description of the contacts is shown in figure D.1. Here the contact resistance is modeled as the sum of three main contributions: a constant term representing the metal line resistance, a DOS-dependent term representing the resistance of graphene channel below the contact and a third term representing the impedance associated with the interface, that can be considered as an "injection" resistance. This contact resistance model [93], has been implemented in ADS and a simulation has been run to compare results with figure 5.9. Plots in figure D.2 show a good agreement between meaurements and model, with values of intrinsic parameters extracted that are in agreement with the first model. However, this is just a preliminary result and further investigations are needed to provide a thorough understanding of contact resistance scaling.

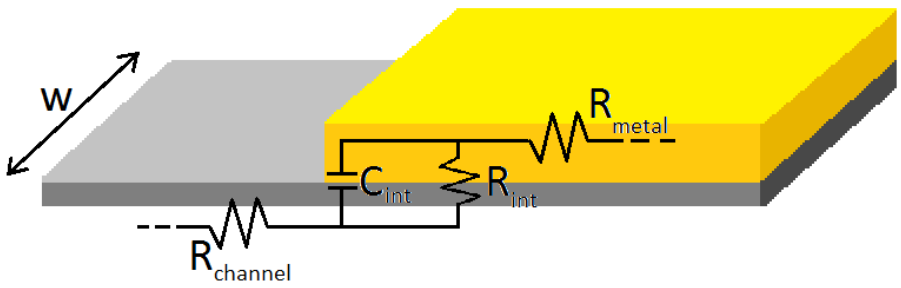

Figure D.1: Model for the contact resistance based on [93]. It comprises a contrbution from the metal line R_{metal} in series with the interface impedence ($R_{\text{int}}//C_{\text{int}}$) and with the channel resistance below the contact R_{channel}.

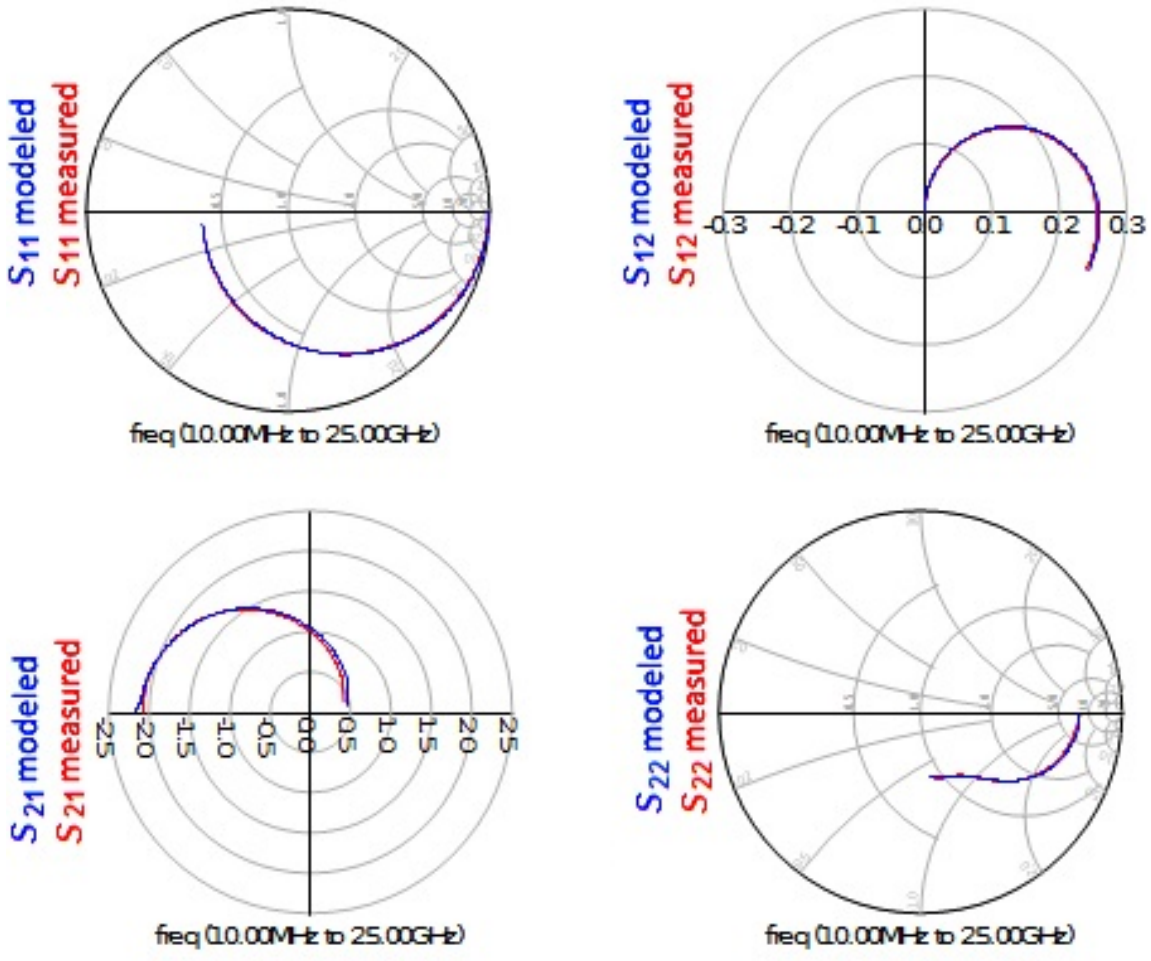

Figure D.2: Comparison between measured and modeled S-parameters at V_{DS}= -1.5 V and V_{GS}= -1.3 V for a device with L = 1 µm and W= 40 µm (sample S3). Contact resistances are modeled based on [93].

Bibliography

[1] A.S. Mayorov, R.V. Gorbachev, S.V. Morozov, L. Britnell, R. Jalil, L. A. Ponomarenko, P . Blake, K. S. Novoselov, K. Watanabe, T. Taniguchi, and Geim A.K. Micrometer-scale ballistic transport in encapsulated graphene at room temperature. *Nano Letters*, 11(6):2396–2399, 2011.

[2] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jing, Y. Zhang, S.V. Dubonos, I. V. Grigorieva, and Firsov A.A. Electric field effect in atomically thin carbon films. *Science*, 22:2–6, 2004.

[3] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, M.I. Katsnelson, I.V. Grigorieva, S.V. Dubonos, and Firsov A. A. Two-dimensional gas of massless dirac fermions in graphene. *Nature*, 438(7065):197–200, November 2005.

[4] J. G. Champlain. A first principles theoretical examination of graphene-based field effect transistors. *Journal of Applied Physics*, 109(8):084515, 2011.

[5] S. M Sze. *Semiconductor devices physics and technology.* Wiley, 2002.

[6] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D . Neumaier, D. Seabaugh, S.K. Banerjee, and Colombo L. Electronics based on two-dimensional materials. *Nature Nanotechnology*, 9:768–779, 2014.

[7] L. Liao, J. Bai, Y. Qu, Y.-C. Lin, Li, Y. Huang, and X. Duan. High-k oxide nanoribbons as gate dielectrics for high mobility top-gated graphene transistors. *PNAS*, 107(5):6711–6715, 2010.

[8] G. Moore. Cramming more components onto integrated circuits. *Electronics*, 38(8):114–117, 1965.

[9] The international technology roadmap for semiconductors. http://www.itrs.net.

[10] S. Galdin-Retailleau, A. Bournel, and P. Dollfus. *Nanoscience Nanotechnologies and nanophysics*, chapter 11-Ultimate electronics, pages 392–400. Springer, 2004.

[11] C. Dupas, P. Houdy, and M. Lahmani. *Nanoscience Nanotechnologies and nanophysics.* Springer, 2004.

[12] A. Toriumi and K. Kita. *Dielectric Films for Advanced Microelectronics*, chapter 7, pages Material Engineering of High–k Gate Dielectrics. Wiley, 2007.

[13] M. V. Fischetti, D.A. Neumayer, and E. A. Cartier. Effective electron mobility in si inversion layers in metal-oxide-semiconductor systems with a high-k insulator: The role of remote phonon scattering. *Journal of Applied Physics*, 90(9):4587, 2001.

[14] G. Lucovsky and J.L. Whitten. *High Dielectric Constant Materials: VLSI MOSFET Applications*, chapter 11, pages Electronic Structure of Alternative High–k Dielectrics. Springer, 2005.

[15] R. Doering and Y. Nishi. *Handbook of Semiconductor Manufacturing Technology*. CRC Press, 2007.

[16] C.-H. Jan et al. 22nm soc platform technology featuring 3-d tri-gate and high-k/ metal gate, optimized for ultra low power, high performance and high density soc applications. In *Int. El. Devices Meet. an Francisco, CA, USA*, 2012.

[17] C. Auth et al. 22 nm high performance and low-power cmos technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density mim capacitors. In *Symp. VLSI Technology*, pages 131–132, 2012.

[18] S. Oktyabrsky and P.D. Ye. *Fundamentals of III-V Semiconductor MOSFETs*. Springer, 2010.

[19] J. A. Alamo. The high electron mobility transistor at 30 : Impressive accomplishments and exciting prospects. In *International Conference on Compound Semiconductor Manufacturing Technology*, 2011.

[20] S. Lee, K. Lee, C.H. Liu, G.S. Kulkarni, and Zhong. Z. Flexible and transparent all-graphene circuits for quaternary digital modulations. *Nature communications*, 3:1018, 2012.

[21] F. Schwierz. Graphene Transistors: Status, Prospects, and Problems. *Proceedings of the IEEE*, 101(7):1567–1584, July 2013.

[22] E. Guerriero, L. Polloni, L. G. Rizzi, M. Bianchi, G. Mondello, and R. Sordan. Graphene audio voltage amplifier. *Small*, 8(3):357–361, 2012.

[23] L. G. Rizzi, M. Bianchi, A. Behnam, E. Carrion, E. Guerriero, L. Polloni, E. Pop, and R. Sordan. Cascading wafer-scale integrated graphene complementary inverters under ambient conditions. *Nano letters*, 12(8):3948–53, August 2012.

[24] E. Guerriero, L. Polloni, M. Bianchi, A. Behnam, E. Carrion, L. G. Rizzi, E. Pop, and R. Sordan. Gigahertz integrated graphene ring oscillators. *ACS nano*, 7:5588, 2013.

[25] L.E.F. Foa Torres, S. Roche, and J.-C. Charlier. *Introduction to Graphene-Based Nanomaterials*. Cambridge University Press, 2014.

[26] A. H. Castro Neto, F. Guinea, N.M.R. Peres, K.S. Novoselov, and A.K. Geim. The electronic properties of graphene. *Reviews of Modern Physics*, 81:109, 2009.

[27] G. Parravicini G. Grosso. *Solid State Physics*. Academic Press, 2000.

[28] A. K. Geim and K. S. Novoselov. The rise of graphene. *Nature Materials*, 6(3):183–191, 2007.

[29] E. H. Hwang and S.D. Sarma. Screening-induced temperature-dependent transport in two-dimensional graphene. *Physical Review B*, 79:165404, 2009.

[30] M. I. Katsnelson. Graphene: carbon in 2 dimensions. *Materials Today*, 10(1):20–27, 2007.

[31] J. Martin, N. Akerman, G. Ulbricht, T. Lohmann, J.H. Smet, K. von Klitzing, and A. Yacoby. Observation of electron-hole puddles in graphene using a scanning single-electron transistor. *Nature Physics*, 4(2):144–148, 2007.

[32] P. A. Lee and D. S. Fisher. Anderson localization in two dimensions. *Physical Review Letters*, 47(12):882–885, 1981.

[33] M. I. Katsnelson, K. S. Novoselov, and A. K. Geim. Chiral tunnelling and the Klein paradox in graphene. *Nature Physics*, 2(9):620–625, 2006.

[34] K. Nagashio, T. Nishimura, and A. Toriumi. Estimation of residual carrier density near the dirac point in graphene through quantum capacitance measurement. *Applied Physics Letters*, 102:173507, 2013.

[35] J. Xia, F. Chen, J. Li, and N. Tao. Measurement of the quantum capacitance of graphene. *Nature nanotechnology*, 4:505–509, 2009.

[36] V. E. Dorgan, M.-H. Bae, and E. Pop. Mobility and saturation velocity in graphene on SiO2. *Applied Physics Letters*, 97:082112, 2010.

[37] Y. Yin, Z. Cheng, L. Wang, K. Jin, and W. Wang. Graphene, a material for high temperature devices-intrinsic carrier density, carrier drift velocity, and lattice energy. *Scientific reports*, 4:5758, 2014.

[38] S. Forti and U. Starke. Epitaxial graphene on SiC: from carrier density engineering to quasi-free standing graphene by atomic intercalation. *Journal of Physics D: Applied Physics*, 47(9):094013, 2014.

[39] W. W. Zhu, V. Perebeinos, M. Freitag, and P. Avouris. Carrier scattering, mobilities, and electrostatic potential in monolayer, bilayer, and trilayer graphene. *Physical Review B*, 80:235402, 2009.

[40] S. Fratini and F. Guinea. Substrate-limited electron dynamics in graphene. *Physical Review B*, 77(19):195415, 2008.

[41] A. Konar, T. Fang, and D. Jena. Effect of high-κ gate dielectrics on charge transport in graphene-based field effect transistors. *Physical Review B*, 82(11):115452, 2010.

[42] I. Meric, M.Y. Han, A.F. Young, B. Ozyilmaz, P. Kim, and K.L. Shepard. Current saturation in zero-bandgap, top-gated graphene field-effect transistors. *Nature nanotechnology*, 3(11):654–9, 2008.

[43] A. Barreiro, M. Lazzeri, J. Moser, F. Mauri, and A. Bachtold. Transport Properties of Graphene in the High-Current Limit. *Physical Review Letters*, 103(7):076601(4), 2009.

[44] Y. Wang, B.-C. Huang, M. Zhang, C. Miao, Y.-H. Xie, and J. C. S. Woo. High performance graphene FETs with self-aligned buried gates fabricated on scalable patterned Ni-catalyzed graphene. *Dig. Symp. Very Large Scale Integr. (VLSI) Technol.*, 1(1):116–117, 2011.

[45] I. Meric, C. Dean, A. Young, J. Hone, P. Kim, and K.L. Shepard. Graphene field-effect transistors based on boron nitride gate dielectrics. In *Electron Devices Meeting (IEDM)*, 2010.

[46] S. Masubuchi, S. Morikawa, M. Onuki, K. Iguchi, K. Watanabe, T. Taniguchi, and T. Machida. Fabrication and characterization of high-mobility graphene p-n-p junctions encapsulated by hexagonal boron nitride. *Japanese Journal of Applied Physics*, 52:110105, 2013.

[47] K.K. Kim, A. Hsu, X. Jia, S.M. Kim, Y. Shi, M. Dresselhaus, T. Palacios, and J. Kong. Synthesis and characterization of hexagonal boron nitride film as a dielectric layer for graphene devices. *ACS Nano*, 6(10):8583–90, 2012.

[48] D. Kahng. Electric field controlled semiconductor device, u. s. patent no. 3,102,230, 1963.

[49] F. Xia, D. B. Farmer, Y.-M. Lin, and P. Avouris. Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature. *Nano Letters*, 10(2):715–718, 2010.

[50] M. A. Bisset, M. Tsuji, and A. Hiroki. Strain engineering the properties of graphene and other two-dimensional crystals. *Physical Chemistry Chemical Physics*, 16:11124, 2014.

[51] G.-H. Lee, Y.-J. Yu, X. Cui, N. Petrone, C.-H. Lee, M.S. Choi, D.-Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, T. Taniguchi, C. Nuckolls, P. Kim, and J. Hone. Flexible and Transparent MoS2 Field-Effect Transistors on Hexagonal Boron Nitride-Graphene Heterostructures. *ACS*, 7(9):7931–7936, 2013.

[52] A. S. Sedra and K. C. Smith. *Microelectronic Circuits*. Oxford University press, 2009.

[53] S.-J. Han, D. Reddy, G.D. Carpenter, A.D. Franklin, and K.A. Jenkins. Current Saturation in Submicrometer Graphene Transistors with Thin Gate Dielectric: Experiment, Simulation and Theory. *ACS Nano*, 6(6):5220–5226, 2012.

[54] J. E. Ayers. *Digital Integrated Circuits*. Taylor & Francis e-Library, 2005.

[55] M.J. Allen, V.C. Tung, and R.B. Kaner. Honeycomb carbon: a review of graphene. *Chemical reviews*, 110(1):132–145, 2010.

[56] J.D. Wood, S.W. Schmucker, A.S. Lyons, E. Pop, and J.W. Lyding. Effects of polycrystalline Cu substrate on graphene growth by chemical vapor deposition. *Nano Letters*, 11:4547–4554, 2011.

[57] F. Traversi, V. Russo, and R. Sordan. Integrated complementary graphene inverter. *Applied Physics Letters*, 94(22):223312, 2009.

[58] P. Blake, E.W. Hill, A.H. Castro Neto, K. S. Novoselov, D. Jiang, R. Yang, and A.K. Booth, T. J. andGeim. Making graphene visible. *Applied Physics Letters*, 91(6):063124, 2007.

[59] S.-L. Li, H. Miyazaki, A. Kumatani, A. Kanda, and K. Tsukagoshi. Low operating bias and matched input-output characteristics in graphene logic inverters. *Nano Letters*, 10:2357–2362, 2010.

[60] A.D. Liao, J.Z. Wu, X. Wang, K. Tahy, D. Jena, H. Dai, and E. Pop. Thermal limited current carrying ability of graphene nanoribbons. *Physical review letters*, 106:256801, 2011.

[61] E. Guerriero, M. Fiocco, A. A. Sagade, D. Neumaier, and R. Sordan. Integrated graphene high-gain voltage amplifiers and high-frequency ring oscillators. In *Graphene Week 2014, 23-27 June, Gothenburg, Sweden*, 2014.

[62] L. Tao, J. Lee, H. Li, R. D. Piner, R. S. Ruoff, and D. Akinwande. Inductively heated synthesized graphene with record transistor mobility on oxidized silicon substrates at room temperature. *Applied Physics Letters*, 103:183115, 2013.

[63] J. R. Barry. *Digital communication- Third Edition*. Kluwer Academic Publishers, 2004.

[64] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. Mcgraw Hill Higher Education, 2001.

[65] D. M. Pozar. *Microwave engineering*. Wiley, 4th edition, 2012.

[66] Z. Chen, J. Appenzeller, Y.-M. Lin, J. Sippel-Oakley, A.G. Rinzler, J. Tang, S.J. Wind, P.M. Solomon, and P. Avouris. An integrated logic circuit assembled on a single carbon nanotube. *Science*, 311:1735, 2006.

[67] J. P. Uyemura. *CMOS logic circuit design*. Kluwer Academic publisher, 2002.

[68] P. A. Khomyakov, G. Giovannetti, P.C. Rusu, G. Brocks, and P.J. Kelly. First-principles study of the interaction and charge transfer between graphene and metals. *Physical review. B*, 79:195425, 2009.

[69] E. Watanabe, A. Conwill, D. Tsuya, and Y. Koide. Low contact resistance metals for graphene based devices. *Diamond and Related Materials*, 24:171–174, 2012.

[70] S. M. Song and B. J. Cho. Contact resistance in graphene channel transistors. *Carbon letters*, 14(3):162–170, 2013.

[71] K. Nagashio and A. Toriumi. Density-of-states limited contact resistance in graphene field-effect transistors. *Japanese Journal of Applied Physics*, 50(7):070108, 2011.

[72] Z. Chen and J. Appenzeller. Gate modulation of graphene contacts - on the scaling of graphene fets. *Symposium on VLSI Technology Digest of Technical Papers*, 1:128–129, 2009.

[73] S. Russo, M. F. Craciun, M. Yamamoto, A. F. Morpurgo, and S. Tarucha. Contact resistance in graphene-based devices. *Physica E: Low-dimensional Systems and Nanostructures*, 42(4):677–679, 2010.

[74] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic. Benchmarking nanotechnology for high-performance and low-power logic transistor applications. *IEEE Transactions on Nanotechnology*, 4:153–158, 2005.

[75] K.J. Kuhn, U. Avci, A. Cappellani, M. D. Giles, M. Haverty, S. Kim, R. Kotlyar, S. Manipatruni, D. Nikonov, C. Pawashe, M. Radosavljevic, R. Rios, S. Shankar, R. Vedula, R. Chau, and I. Young. The ultimate cmos device and beyond. In *Int. E. Devices Meet.*, 2012.

[76] H. Wang, A. Hsu, J. Wu, J. Kong, and T. Palacios. Graphene-Based Ambipolar RF Mixers. *IEEE Electron Device Letters*, 31(9):906–908, 2010.

[77] H. Wang, D. Nezich, J. Kong, and T. Palacios. Graphene Frequency Multipliers. *IEEE Electron Device Letters*, 30(5):547–549, 2009.

[78] O. Habibpour and S. Cherednichenko. A Subharmonic Graphene FET Mixer. *IEEE Electron*, 33(1):71–73, 2012.

[79] Y.-M. Lin, A. Valdes-Garcia, S.-J. Han, D.B. Farmer, I. Meric, Y. Sun, Y. Wu, C. Dimitrakopoulos, A. Grill, and P. Avouris. Wafer-scale graphene integrated circuit. *Science*, 332:1294–1297, 2011.

[80] J. S. Moon, H.-C. Seo, M. Antcliffe, D. Le, C. McGuire, A. Schmitz, L.O. Nyakiti, D.K. Gaskill, P.M. Campbell, K.-M. Lee, and P. Asbeck. Graphene FETs for Zero-Bias Linear Resistive FET Mixers. *IEEE Electron Device Letters*, 34(3):465–467, 2013.

[81] Y. Wu, K.A. Jenkins, A. Valdes-Garcia, D.B. Farmer, Y. Zhu, A.A. Bol, C. Dimitrakopoulos, W. Zhu, F. Xia, P. Avouris, and Y.-M. Lin. State-of-the-art graphene high-frequency electronics. *Nano letters*, 12(6):3062–7, 2012.

[82] R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y.-C. Lin, S. Jiang, Y. Huang, and X. Duan. High-frequency self-aligned graphene transistors with transferred gate stacks. *Proceedings of the National Academy of Sciences of the United States of America*, 109(29):11588–92, 2012.

[83] S. Mason. Power gain in feedback amplifier. *Transactions of the IRE Professional Group on Circuit Theory*, CT-1(2):20–25, 1954.

[84] Z.H. Feng, C. Yu, J. Li, and X.B. Song J.J. Wang S.J. Cai Q.B. Liu, Z.Z. He. An ultra clean self-aligned process for high maximum oscillation frequency graphene transistors. *Carbon*, 75:249–254, 2014.

[85] R. Lai, X. Mei, W. Deal, W. Yoshida, Y.M. Kim, P.H. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier, L. Samoska, and A. Fung. Sub 50 nm InP HEMT device with Fmax greater than 1 THz. *Int. El. Devices Meet.*, 1:609–611, 2007.

[86] J. Hacker, M. Urteaga, M. Seo, A. Skalare, and R. Lin. InP HBT amplifier MMICs operating to 0.67 THz. In *Proc. IEEE MTT-S Int. Microwave Symp.*, 2013.

[87] G. Gonzalez. *Microwave Transistor Amplifiers: Analysis and Design*. Prentice-Hall. Inc., 1996.

[88] M. S.Gupta. Power gain in feedback amplifiers,a classic revisited. *IEEE Transactions on Microwave Theory and Techniques*, 40(5):864–879, 1992.

[89] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez. A new method for determining the fet small-signal equivalent circuit. *IEEE Transactions on Microwave Theory and Techniques*, 36(7):1151–1159, 1988.

[90] S. Lee, C.-S. Kim, and H.-K. Yu. A small-signal RF model and its parameter extraction for substrate effects in RF MOSFETs. *IEEE Transactions on Electron Devices*, 48(7):1374–1379, 2001.

[91] M. Golio. *The RF and Microwave Handbook*. CRC Press LLC, 2001.

[92] F. Schwierz and J. Liou. *Modern Microwave Transistors: Theory, Design and Performance.* Hoboken, New Jersey, 2003.

[93] H.H. Berger. Models for contacts to planar device. *Solid-state electronics*, 15(2):145–158, 1972.

[94] N. Rorsman, M. Garcia, C. Karlsson, and H. Zirath. Accurate Small-Signal modmodel of HFET's for millimiter-wave applications. *IEEE Transactions on Microwave Theory and Techniques*, 44(3):432–437, 1996.

[95] Keysight Network Analyzer basics Application notes.

[96] H. Wang, Y. Wu, C. Cong, J. Shang, and T. Yu. Hysteresis of electronic transport in graphene transistors. *ACS nano*, 4(12):7221–8, 2010.

[97] E. Carrion, A.Y. Serov, S. Islam, A. Behnam, A. Malik, F. Xiong, M. Bianchi, R. Sordan, and E. Pop. Hysteresis-free nanosecond pulsed electrical characterization of top-gated graphene transistors. *IEEE Transactions on electron devices*, 61:1583–1589, 2014.

[98] J. Knoch, Z. Chen, and J. Appenzeller. Properties of Metal-Graphene Contacts. *IEEE Transactions on Nanotechnology*, 11(3):513–519, 2012.

[99] W. Liu, J. Wei, X. Sun, and H. Yu. A Study on Graphene-Metal Contact. *Crystals*, 3(1):257–274, 2013.

[100] O. Habibpour. *Graphene FETs in Microwave Applications.* PhD thesis, Chalmers University of Technology, 2012.

[101] S. Rodriguez, S. Vaziri, A. Smith, S. Fregonese, M. Ostling, M. Lemme, and A. Rusu. A Comprehensive Graphene FET Model for Circuit Design. *IEEE Transactions on Electron Devices*, 61(4):1199–1206, 2014.

[102] S.-J. Han, S. Oida, K.A. Jenkins, and D. D. Lu. Multifinger Embedded T-Shaped Gate Graphene RF Transistors With High fMAX/fT Ratio. *IEEE Electron Device Letters*, 34:1340–1342, 2013.

[103] Z. Guo, R. Dong, P.S. Chakraborty, N. Lourenco, J. Palmer, Y. Hu, M. Ruan, J. Hankinson, J. Kunc, J.D. Cressler, C. Berger, and W.A. de Heer. Record maximum oscillation frequency in c-face epitaxial graphene transistors. *Nano Letters*, 13:942–947, 2013.

[104] Y. Lin, C. Dimitrakopoulos, K. A. Jenkins, D.B. Farmer, H. Chiu, A. Grill, and A. Avouris. 100-GHz Transistors from wafer-scale epitaxial graphene. *Science*, 327:100, 2010.

[105] Y. Wu, D.B. Farmer, W. Zhu, S.-J. Han, C.D. Dimitrakopulos, A.A. Bol, P. Avouris, and Y.-M. Lin. Three-terminal graphene negative differential resistance devices. *ACS Nano*, 6(3):2610–2616, 2012.

[106] R. Grassi, A. Gnudi, V. Di Lecce, E. Gnani, S. Reggiani, and G. Baccarani. Exploiting negative differential resistance in monolayer graphene fets for high voltage gains. *IEEE Transactions on electron devices*, 61(2):617–624, 2014.

[107] J. S. Moon, M. Antcliffe, H. C. Seo, D. Curtis, S. Lin, A. Schmitz, I. Milosavljevic, A. A. Kiselev, R. S. Ross, D. K. Gaskill, P. M. Campbell, R. C. Fitch, K.-M. Lee, and P. Asbeck. Ultra-low resistance ohmic contacts in graphene field effect transistors. *Applied Physics Letters*, 100:203512, 2012.

[108] A. Hsu, H. Wang, K.K. Kim, J. Kong, and T. Palacios. Impact of Graphene Interface Quality on Contact Resistance and RF Device Performance. *IEEE Electron Device Letters*, 32(8):1008–1010, 2011.

[109] O. Balci and C. Kocabas. Rapid thermal annealing of graphene-metal contact. *Applied Physics Letters*, 101(24):243105, 2012.

[110] A. D. Franklin, S.-J. Han, A. A. Bol, and V. Perebeinos. Double Contacts for Improved Performance of Graphene Transistors. *IEEE Electron Device Letters*, 33(1):17–19, 2012.

[111] J. T. Smith, A. D. Franklin, D. B. Farmer, and C. D. Dimitrakopoulos. Reducing Contact Resistance in Graphene Devices through Contact Area Patterning. *ACS nano*, 7(4):3661–7, 2013.

[112] A. Chaudhry. *Fundamentals of Nanoscaled Field Effect Transistors*. Springer, 2013.

[113] C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K. L. Shepard, and J. Hone. Boron nitride substrates for high quality graphene electronics. *Nature Nanotechnology*, 5:722–726, 2010.

[114] J. Bai, L. Liao, H. Zhou, R. Cheng, L. Liu, Y. Huang, and X. Duan. Top-Gated Chemical Vapor Deposition Grown Graphene Transistors with Current Saturation. *Nano Letters*, 11(6):2555–2559, 2011.

[115] H. Wang, T. Taychatanapat, A. Hsu, K. Watanabe, T. Taniguchi, P. Jarillo-Herrero, and T. Palacios. BN/Graphene/BN Transistors for RF Applications. *IEEE Electron Device Letters*, 32(9):1209–11, 2011.

[116] S. Cataldo and B. Pignataro. Polymeric thin films for organic electronics: Properties and adaptive structures. *Materials*, 6(3):1159–1190, 2013.

[117] L. Britnell, R. V. Gorbachev, R. Jalil, B. D. Belle, F. Schedin, A. Mishchenko, T. Georgiou, M. I. Katsnelson, L. Eaves, S. V. Morozov, N. M. R. Peres, J. Leist,

A. K. Geim, K. S. Novoselov, and L. A. Ponomarenko. Field-effect tunneling transistor based on vertical graphene heterostructures. *Science*, 335(6071):947–950, 2012.

[118] X. Cui N. Petrone C.H. Lee M.S. Choi D.Y. Lee C. Lee W.J. Yoo K. Watanabe T. Taniguchi C. Nuckolls P. Kim J. Hone G.H. Lee, Y. J. Yu. Flexible and transparent mos2 field-effect transistors on hexagonal boron nitride-graphene heterostructures. *ACS Nano*, 7(9):7931–6, 2013.

[119] H. Tian, Z. Tan, C. Wu, X. Wang, M. A. Mohammad, D. Xie, Y. Yang, J. Wang, L.-J. Li, J. Xu, and T.-L. Ren. Novel field-effect schottky barrier transistors based on graphene-mos2 heterojunctions. *Scientific reports*, 4:5951, 2014.

[120] L. Yu, Y.-H. Lee, X. Ling, E. J. G. Santos, Y. C. Shin, Y. Lin, M. Dubey, E. Kaxiras, J. Kong, H. Wang, and T. Palacios. Graphene/MoS2 Hybrid Technology for Large-Scale Two-Dimensional Electronics. *Nano Letters*, 14(6):3055–3063, 2014.