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VARIABILITY, ENDURANCE AND NOVEL APPLICATIONS OF RESISTIVE SWITCHING DEVICES

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Abstract

In recent years there has been a huge increase in the storage capacity of integrated memories, still the technological solutions remained almost the same. The continuous demand of new portable, low-cost, low-power devices has forced a huge effort in R&D pushing the limits of the current technology. Flash memory, representing the main stream memory technology and experienced an impressive development, that has led this technology to a 16 nm node and to the implementation of 3D architectures. As we approach the scaling limit imposed by physics to Flash technology, the research is making more and more efforts towards the development of new devices that are able to combine the characteristics of Flash technology with the performances of faster memories, overcoming the scaling limits that will soon afflict the floating gate devices. At the same time, it is emerging the need of a new family of memory, called storage class memory, that combines the benefits of a solid-state memory, like high speed and robustness and the archival capabilities and low cost of conventional HDD.

Among many competitors, oxide based resistive switching memories represent a strong candidate for next generation solid state non-volatile memory technology. In particular, the extreme ease of fabrication, the low power and energy consumption and the high write/erase speed suggest that this technology may became a valid alternative to Flash memories and an optimal choice for storage class memory.

This Doctoral Dissertation will be focused on Hafnium Oxide-based Resistive-switching Random Access Memory (RRAM). The work describes working principles, physical/numerical modeling, reliability issues and innovative applications. Experimental characterization has been a crucial step in this task, being the starting point of physical understanding and thus modeling.

The first Chapter will briefly describe the non-volatile memory scenario, explaining the Flash technology basics showing its limits and presenting several new solutions. A first introduction on RRAM technology will be discussed, presenting the basic working principle, the array architecture and the scaling perspectives.

The second Chapter will briefly present the different devices studied and will give a deep insight into the switching mechanism. After the description of the bipolar program operations, we will focus on a new switching characteristic, discussing the physics mechanism and a possible application for increase the memory density.

The third chapter will focus on program variability, the cycle-to-cycle fluctuation of the set state resistance. Starting from the experimental results obtained under DC condition we will present an analytical model and a Monte Carlo model capable of describe variability and its dependence on programming current.

The fourth Chapter will focus on switching in pulsed regime. In particular will be described the dependence of program variability and endurance on pulse-amplitude and pulse-width. For the the endurance will be presented an Arrhenius model, capable of account for the dependence on the pulse-amplitude and pulse-width.

The fifth Chapter will focus on the random telegraph noise (RTN) affecting low resistance states. Starting from a detailed electrical characterization, we will present a physics based numerical model that can describe the dependence of the RTN switching-rates and the RTN switching-amplitude on the applied voltage and temperature. We will demonstrate that the key parameter is the local temperature and the voltage impact the switching frequency, through the Joule heating.

The sixth Chapter will focus on a completely different aspects of resistive-switching memory, a innovative logic based on RRAM. We will introduce the fundamental logic gates, like AND, IMP, OR and NOT, all logic functions are enabled by the conditional switching in serially-connected RRAM. We will focus also on the logic circuits and on different crossbar architectures. Finally a 1-bit full adder will be demonstrate by simulations and experiments.

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Resistive-switching memory technology

The increasing demand for high density, low cost and low power storage devices has lead the development of today's non-volatile market leader Flash technology. To overcame the limits of Flash memory new technologies are emerging as interesting solutions. In this chapter, after a brief introduction of non-volatile memory market, a first overview to resistive-switching technology will be done.

1.1 Introduction to Non Volatile Memory

The incredible growing of the market of portable devices, such as smartphones, tablets, music player has driven the developments of low power and high performances solid-state memories.

The fast adoption of electronic low-volume portable devices with low power consumption and high performances is pushing up the demand of non-volatile solid-state memories. Smart phones, music players, tablets and Solid State Disks (SSDs) are only few examples of the ubiquitousness and the ever increasing role played by non-volatile memory (NVM) in changing our lifestyle. From a simple concept in the early 80's, Flash memory, the actual market leader of NVMs, grew up and generated close to $ 23 billion in worldwide revenue in 2007 [1], representing one of the many success stories in the semiconductor industry.

This incredible growth was essentially driven by the Moore's Law that lead to dramatic reductions in unit cost over the past few decades for the entire semiconductor industry. This enables NVM to fulfill the requirement for products of ever higher density while continuously pulling down market prices. As can be seen in Fig. 1.1, the cost of Flash memory has fallen from $10000 per gigabyte of the mid 90's, approaching $1 per gigabyte in 2010 [2]. This continuous reduction of the memory price enabled creation of new markets that in turn largely repaid the efforts devoted for the manufacturing of memory chips with increased performances and functionality. All these improvements were made possible by the innovation of the industry along different fronts, first

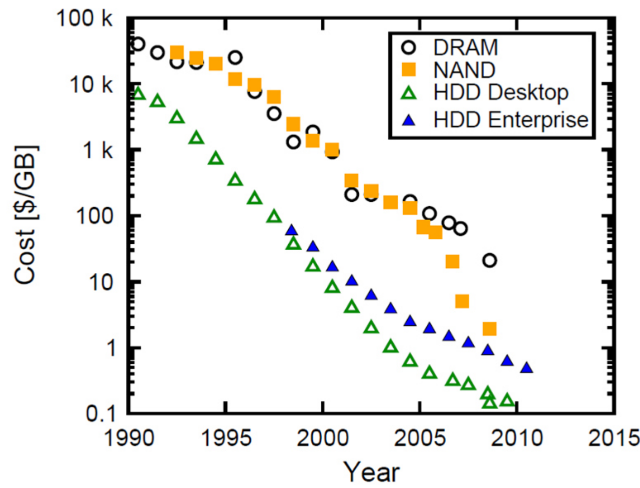

Figure 1.1: Cost per GigaByte (GB) of Desktop and Enterprise hard disk drives (HDD) compared to the cost reduction trend in DRAM and NAND memory (recom- piled from [2])).

of all the great advances in lithography which is fundamental for the area scaling. A great contribution was also provided by innovative self-aligned technologies, the introduction of NAND memory to reduce memory cell size, the introduction of multi-level cell technology and wafer size increasing from 150 mm in 1987 to 300 mm in recent years 1.1. Despite their still high cost per bit with respect to magnetic hard disk drives, semiconductor memories resulted the winning solution in all the consumer products requiring light weight, low size, low power consumption and high reliability.

In this frame, Fig. 1.2 reports the significant developments in NAND flash memory over the past few years, as extracted from the works presented at the ISSCC 2014. Continuous scaling of the memory cell has resulted in an exponential increase of the memory density per chip. In order to guarantee an ever increase in memory density and and ever decrease in memory costs, something more than the mere scaling of feature size will be necessary, due to the intrinsic physical limits that Flash technology will face in the next years. In the last decade several emerging memory technologies have been proposed as possible alternatives to Flash memory. Such technologies may be classified into two big categories, that is evolutionary memories, that essentially rely on the continuation of the existing ones, and completely new storing concepts. In the following sections, the traditional Flash memory cell, its working principle and the main scaling limitations will be briefly described, then the main direction in the non-volatile panorama will be presented and discussed. A particular attention will be devoted to Resistive-switching Random Access Memory (RRAM) technology and its fundamentals, as it will be the main topic of this Doctoral dissertation.

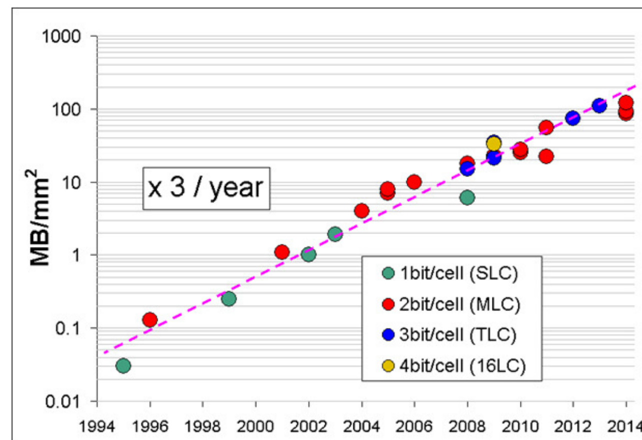

Figure 1.2: Observed trend in NAND Flash memory capacities presented at ISSCC in the past years (data from ISSCC 2014 documentation).

1.2 Mainstream FLASH memory

The outstanding improvements in Flash technology have been achieved by the practical scaling methodologies allowed by the CMOS technology and by the simple structure of the floating-gate cell today representing the mainstream non-volatile storage element. Flash memory essentially consists in a MOSFET transistor with tunable threshold voltage. Respect to a conventional transistor, the structure presents a floating gate (FG), in which it is possible to store charge, typically electrons. There are two kinds of Flash memories, NOR and NAND. In NOR memory architectures, each cell in a two-dimensional array is directly connected to its word-line and bit-line input lines, whereas in NAND memory architectures, small blocks of cells are connected in series between a high input signal and ground. Thus, due to its smaller unit cell size and being in perspective well suitable for the exploitation of new enhanced optical lithographic techniques [3], NAND Flash can inherently be packed more densely than NOR Flash, attaining the minimum cell area of $4\mathrm{F}^2$ respect to the $10\mathrm{F}^2$ occupied by the NOR counterpart. The sensing mechanism consists in applying a positive bias to the control gate (CG) and subsequently reading of the resulting current that can be high or low as a function of threshold-voltage (V_T), hence function of the stored charge in the FG. On the other hand, the programming mechanism consists of a controlled shift of the threshold voltage, achieved by injecting or removing charge in the floating gate. This operation can exploit Channel Hot Electrons injection (CHE) or Fowler- Nordheim tunneling (FN) mechanism [4]. The former approach needs a relatively high drain to source current and is used in NOR Flash, where each cell has its drain contact connected to the bit-line. FN programming is instead employed in NAND Flash, where the drain contact is not available, and provides slower single bit operation; however, the much smaller value of the tunneling current allows for parallel programming of several cells in the same array and largely enhances the overall write throughput. As a consequence, NOR memory are mainly used for applications such as embedded logic

that require fast access to data that is modified only occasionally. In contrast, NAND memory is a high-density, block-based architecture with slower random access which is mainly used for mass storage applications. In both NOR and NAND architectures, the erase operation is achieved by means of FN tunneling from the FG to the channel. As already mentioned, the success of Flash technology has been guaranteed by the complete compatibility with the CMOS technology, and Flash cell has been profitably scaled in a similar way as conventional transistors. However, major scaling challenges mine Flash scalability for next generations, originating from both physical scaling constraints (lithography and the cell layout design) and severe reliability issues [1, 2, 5]. Among them we can cite [6]: (i) oxide traps, contributing threshold-voltage (V_T) instability issues such as stress-induced leakage current (SILC) [7], trapping/detrapping [8] and random telegraph signal noise (RTN) [9], (ii) edge field-enhancement and discrete-dopant effects, which collaborate with oxide-trap effects to enhance the V_T spread in the array, (iii) few-electron effects [3] and (iv) cell-cell electrostatic coupling in the array [10].

1.3 Evolutionary scenario and paradigm shift

The impressive performance growth rate of the traditional system memory and storage hierarchy that we are experiencing in the memory market since the last 30 years is facing serious problems and main challenges in the design of large-scale, high-performance systems. The gap between the performance of disks and the rest of the system - which is already five orders of magnitude - continues to widen rapidly [11,12]. In addition, the energy consumption, the space usage and cost of the memory and storage systems pose major doubts on the feasibility of even higher performing, although low-cost, devices. Naturally, the continuous challenge toward lower costs and higher performances has driven a strong innovation in the existing technologies but it has also led to the development of alternative memory technologies as well, in anticipation of scaling limitations of existing Flash memory [1].

To overcome the several obstacles and maintain the historic growth rate we have experienced so far two possible may apply. The most conservative strategy is the so-called evolutionary scenario: major efforts are currently underway to develop the capability to integrate device chips by stacking them vertically and using through-silicon vias (TSV) [13] to connect them or, even more challenging and economically interesting, stacking several layer of circuits on the same wafer [14, 15]. Such 3D integration is faced by hard technical challenges regarding design, fabrication, bonding, test, reliability, yield and overall cost. A second, more demanding possibility, is the exploration of a wide variety of entirely new approaches. This strategy is called paradigm shift and has been carried out in the last years by both industries and research centers all over the world: important examples of novel concepts are Ferroelectric RAM, Magnetic RAM, and resistive memories (Phase-Change Memory, Oxide-based RAM and Electrochemical Metallization Memory) [2, 16]. Among these, Oxide-based RAM and Electrochemical Metallization Memory are the most promising technologies. Fig. 1.3 reports the density achieved in products and/or demonstrators for several technologies, including NAND flash, Oxide-RRAM, Phase Change Memory (PCM), Ferroelectric Memory (FeRAM), and Magnetic Memory (MRAM). RRAM recently achieved a ca-

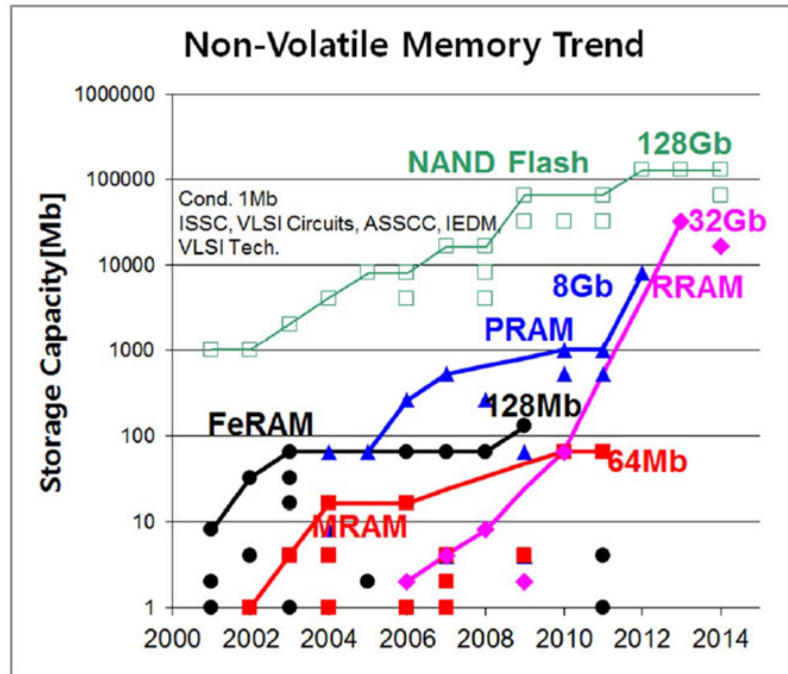

Figure 1.3: Comparison between memory density achieved in conventional NAND flash and emerging memory technologies (data from ISSCC 2014 documentation).

pacity of 32 Gb [17], which is close to the density typically available in commercial NAND products.

1.4 RRAM technology

Among the candidates for NVM applications RRAM represents a very promising competitor in the challenge for the post-Flash scenario. The first report about it is dated 1960s [18], but only recently this technology is attracting a serious interest both in academy and industry. The basic principle of this kind of memory is the so called resistive switching, *i.e.* the peculiar property of an active layer material of changing its resistivity after the application of an external voltage or current. Starting from a high resistive value, typical of insulators, the material can switch to a low resistive value, typical of metals. This change in conduction is reversible and the two resistance states can be easily used to store a bit of information.

RRAM devices include a wide range of different materials used as resistive oxide switching layer and electrodes. A summary is reported in Fig. 1.4, where the elements used for electrodes are highlighted in blue while in yellow are colored the metals corresponding to the binary oxide used for the switching [19]. In literature several kinds of resistive memory, based on different physics mechanisms are contemplated. To clarify this complex zoology, a useful taxonomy has been provided by Waser and

Figure 1.4: Summary of the materials that have been used for binary metal-oxide RRAM. Metals of the corresponding binary oxides used for the resistive switching layer are colored in yellow, while metals used for the electrodes are colored in blue [19].

Aono [16], introducing a classification of nine different basic switching mechanisms and devices: (i) Nanomechanical Memory, (ii) Molecular Memory, (iii) Phase Change Memory, (iv) Thermochemical Memory, (v) Valence Change Memory, (vi) Electrochemical Metallization Memory, (vii) Electrostatic/Electronic Effects Memory, (viii) Magnetoresistive Memory and (ix) Ferroelectric Memory. Devices from (iii) to (viii) are the most promising NVMs for future post-Flash replacement where the resistive-switching effect can be obtained by the application of electrical stimuli able to generate thermal, chemical, electronic/electrostatic effects inside the active layer material. More precisely, the physical mechanism for switching resistance states in the Phase Change Memory is purely thermal and for the Electrostatic/ Electronic Effects Memory the switching mechanism is purely electronic. However, the physical switching mechanisms for the Thermal Chemical Memory (TCM), the Valence Change Memory Cell (VCM), and the Electrochemical Metallization Cell (ECM) are all based on reduction/ oxidation (Redox)-related chemical effects. Due to similarity of their physical mechanisms they are also known with the name of Redox RAM.

The Doctoral Dissertation here reported is focused on the electrical characterization and physical modeling of VCM cells. A preliminary introduction to this kind of RRAM technology is here reported. In a VCM cell the resistive-switching requires a change of bias polarity between the set and the reset operations. This is thus referred to as bipolar switching. The first operation is the forming: the creation of a conductive filament (CF) that connect the two electrodes through a soft breakdown. After the creation of the CF, it is dissolved by migration of ions toward the electrodes, namely positive ions (*e.g.* metallic ions or oxygen vacancies) drift toward the cathode and negative ions (oxygen ions) drift toward the anode (see Fig. 1.5). The CF is recovered by migration of the ions back to the previous position (see Fig. 1.5a). This allows a low-resistance connec-

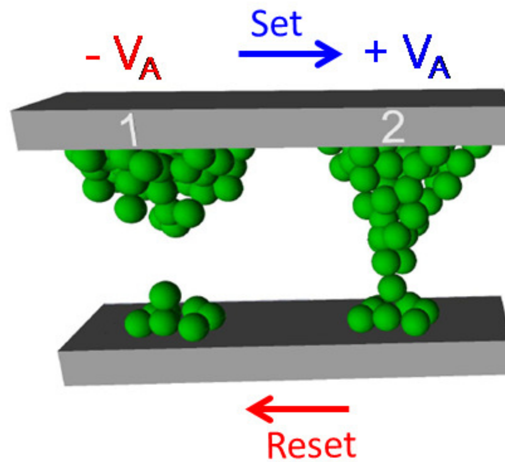

Figure 1.5: Schematic representation of a VCM cell in the high resistive state (1) and in the low resistive state (2). Different polarity is applied for the creation and dissolution of the CF.

tion between the electrodes by a continuous metal-rich (or oxygen-vacancy rich) CF. Several transition metal oxides have been shown to display bipolar VCM switching. Examples are ZrO_x [20], $SrTiO_x$ [21], Nb_2O_5 [22], TiO_x [23] and HfO_x [24]. The preliminary forming operation is generally required to initiate the resistance switching, but the reset and set parameters generally vary depending on the materials and the cell structures. Moreover in some VCM devices is possible to observe the uniform switching of the active layer material instead of the filamentary switching. This cells are based on complex oxides such as PrCaMnO (PCMO) and other perovskites [25]. In this case the memory show an area-dependent switching, where the both high resistance and low resistance state are inversely proportional to the device area, contrary. to TCM. Ion migration in these materials is probably uniform, leading to an increase of the oxygen concentration to the anode side and a resulting oxidation. The formation of an interface layer with a high potential barrier for electrons causes the increase of resistance in the uniform switching VCM. This kind of VCM is attracting a growing interest since the reset current can be reduced linearly with the device area, in contrast to filamentary switching RRAM where the reset current is area independent. However, the deposition and control of complex ternary/quaternary oxides is generally not straightforward and the reliability issues and mechanisms are still not clear, thus these devices appear to be not yet sufficiently mature as compared to filamentary RRAM.

1.5 Architectures and scaling perspectives

RRAM technology has attracted a strong interest in particular for its intrinsic scalability potentials. The particular simplicity of the cell, as a matter of fact a simple two terminal capacitor, witch allow for an integration in crossbar array, reported in Fig. 1.6. In this approach each cell is located at the crossing point between a vertical and a horizontal

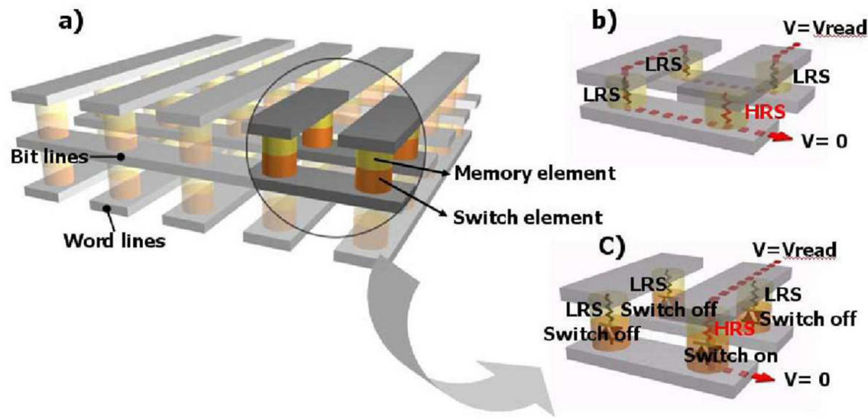

Figure 1.6: Double stack, cross-point RRAM array (a), demonstrated by Samsung in 2007 [39]. In order to prevent reading interferences (b) it is necessary to have a rectifying element, *e.g.* a diode (c).

line. The resulting area dimension of each cell is very small, equal to $4F^2$, where F is the minimum line width/intermetal distance. This dimension is comparable with the dimension of NAND Flash and smaller than DRAM. As reported in Fig. 1.6b, this solution suffers from the so-called sneakpath current issue. To read the resistance it is necessary bias the selected top/bottom lines while all other unselected lines are unbiased, *i.e.*, floating. Measuring the flowing current allows recognizing the state of the cell. The measured current is the sum of the selected cell current and the current flowing through unselected cells in the set state, the sneak path in Figure 1.6b. To solve this problem a selector device must be connected in series to the cell in the so-called one selector/one resistor (1S1R) structure, Fig. 1.6.

In literature are present several kind of selectors, the three most relevant approach are: (i) unipolar diode, (ii) bipolar diode and (iii) threshold switches [26]. The first solution , the unipolar diode, applies only to unipolar switching RRAM because a significant current can only be achieved in one voltage polarity. The most basic example of unipolar diode is a pn diode, using both monocrystalline Si and polycrystalline Si capable of 3-D stacking [27, 28]. Also Schottky-type diodes, such as Ag-ZnO [29], were proposed as unipolar selectors. However unipolar diodes have two big drawback: a low the current density and the fact that only unipolar switching is allowed [26]. For the bipolar diode the most simply solution is back-to-back connection of two Si-based p-n diodes, thus achieving a symmetric pnp structure capable of bipolar rectification [30]. The major problem of this solution is related to the integration in vertical 3D RRAM, which requires materials with low deposition temperature. Another bipolar diode is the mixed electronic-ionic conduction (MIEC), based on the doping of migrating Cu ions show steep I-V characteristics and low voltage operation, while being compatible with back-end-of-line process [31]. Finally the threshold switches are based on a reversible switching of an insulating material into a conductive state, which is preserved only until the voltage is reduced below the threshold condition, the so-called threshold switching. Threshold switching has been extensively observed in metal oxides and

chalcogenides. Typically threshold switching is bipolar, with an on/off ratio of the current dictated by an abrupt transition from on to off conduction states. More recent alternative switches include the threshold vacuum switch (TVS), based on threshold switching in void layers between two electrodes [32].

Electrical characterization and filament morphology

This chapter presents the memory structures of RRAM devices object of this Doctoral Dissertation and gives a deeper insight into different program operations. The morphology of the conductive filament and its dependence on the switching operation is investigated through electrical characterizations and numerical simulations.

2.1 Introduction

In resistive switching memory set/reset operations are achieved through electrical pulses, which can have the same or opposite polarity, corresponding to unipolar or bipolar switching modes, respectively [33]. In unipolar switching, the set and reset processes are interpreted in terms of local chemical reduction (*e.g.*, NiO $\rightarrow$ Ni + O in the prototypical NiO-based unipolar RRAM [34]) and local chemical oxidation, respectively, where the local joule heating developed by the electrical pulse accelerates the chemical reaction in the desired time range [35]. On the other hand, bipolar switching is explained by the thermally activated ion migration of conductive ions (e.g., oxygen vacancies or metal cations, such as Hf ion in HfO_x based bipolar RRAM), where the alternate polarities of set and reset pulses result in ion migration in opposite directions, thus allowing for the growth and the dissolution of the CF, respectively [36, 37]. The interest in bipolar switching devices has grown in the recent few years, due to the insufficient stability of unipolar switching [38].

In this Chapter, after an introduction on the experimental samples, we focus on the switching mechanisms. The starting point is the bipolar switching, then we describe the concept of complementary switching and finally we explain a special application of complementary switching that allows a doubling of the resistance levels for multi-level memory(that means an increase of 1 bit in the stored information, *e.g.* 3 bits instead 2 for 4 resistance levels). In this Chapter, as well as in the all Chapters, we present a complete work, that includes electrical characterization, modeling and simulation. This is the result of the work of a team where I contributed for the firsts two parts,

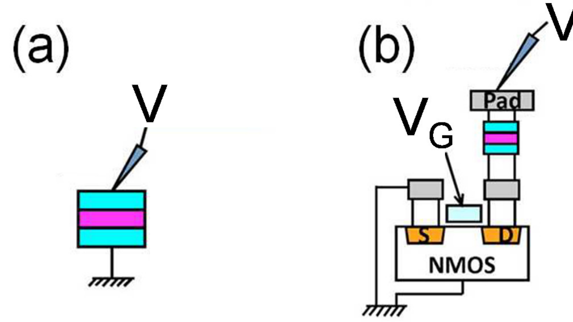

Figure 2.1: Qualitative sketches of the two types of analytical cells object of the electrical characterization in this Doctoral Dissertation, namely 1R (a) and 1T1R (b) structures.

namely electrical characterization and physical modeling. Therefore I designed and realized each experiments and I provided a physical explanation of the experimental results, clearly under the guidance of the advisor and discussing with the entire team.

2.2 Experimental samples and electrical characterization

The memory devices object of this Doctoral Dissertation belong to the group of VCM already presented in Chapter 1. In order to access a deeper comprehension of the physical mechanisms involved in the resistive-switching phenomenon, the electrical characterization dealt only with single analytical cells. As already mentioned in Chapter 1, the simplest RRAM cell is the so called Metal-Insulator-Metal (MIM) structure reported in Fig. 2.1a. This memory device consists of an active switching layer interposed between two metal electrodes. A more complex memory cell is the 1-transistor/1-resistor structure (1T1R) obtained by the integration of a MIM device with a MOS field effect transistor (see Fig. 2.1b). The cell structure presents a memory element (1R) and also a selection element (1T).

Basically three different samples were characterized and modeled, all based on Hafnium-Oxide HfO_2, but with a different stack. The first device used is a simply 1R device, where an amorphous HfO_x (with $x < 2$) switching layer is interposed between two TiN electrodes. Two different thickness of the HfO_x layer were used, namely 5 and 20 nm, while the device active area was $1\mu m^2$ [**?**]. The other two devices considered are both 1T1R RRAM. One consisted of a TiN/HfO_2/Ti/TiN RRAM, where the amorphous HfO_2 switching layer had a thickness of about 5 nm and the Ti buffer layer at the top electrode (TE) acted as oxygen exchange layer (OEL) to induce oxygen deficiency in the switching layer, finally leading to a HfO_x composition with $x < 2$ [39]. The RRAM had dimensions of 50 nm x 50 nm with crossbar geometry. The last device that we studied consist of a TiN bottom electrode (BE), a silicon doped amorphous HfO_x ($HfSiO_x$) switching layer, deposited through ALD technique, and a Ti top electrode (TE) [40]. Also these RRAM has an active area of 50 nm x 50 nm.

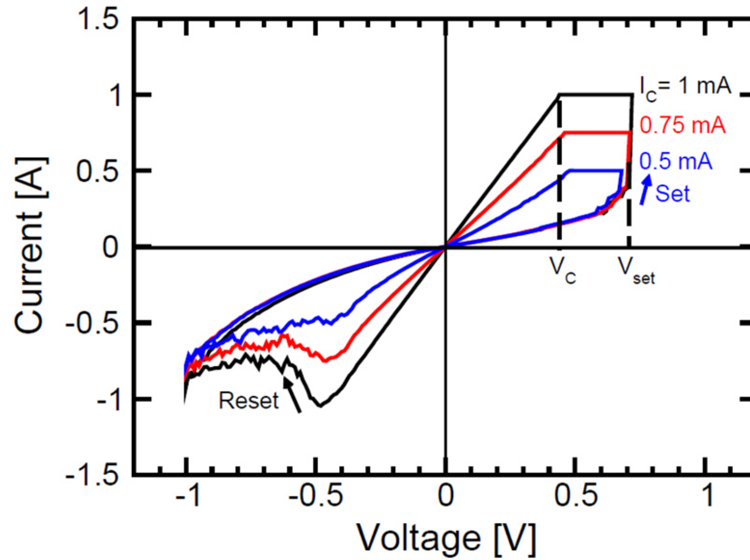

Figure 2.2: Measured I-V curves for bipolar RRAM device with TiN-HfO_x-TiN structure. Set and reset operations are reported for different I_C = 0.5, 0.75 and 1 mA. The constant corner voltage V_C is evidenced.

2.3 Bipolar Switching

Fig. 2.2 shows measured current-voltage (I-V) curves for a HfO_x RRAM device. The I-V curves were measured in DC conditions by a Semiconductor Parameter Analyzer. The figure shows set/reset processes under positive and negative polarity, respectively, for increasing I_C, namely, 0.5, 0.75, and 1 mA. Set state resistance and reset current are controlled by the I_C: as I_C increases, R decreases and I_{reset} increases. This behavior can be attributed to the dependence of the CF size on the I_C: a large I_C causes a filament with a larger cross-section, characterized by a lower resistance. Since the reset voltage is almost constant, a lower resistance leads to a higher I_{reset} [37].

Bipolar switching in Fig. 2.2 can be qualitatively understood by the schematic illustration in Fig. 2.3, showing the evolution of the CF from the high-resistance (reset) state to the low resistance (set) state during the set transition. In the figure, blue dots represent conductive defects, such as oxygen vacancies and/or excess Hf atoms, which are generated at Bipolar switching can be qualitatively understood by the schematic illustration in Fig. 2.3, showing the evolution of the CF from the high-resistance (reset) state to the low resistance (set) state during the set transition. In the figure, blue dots represent conductive defects, such as oxygen vacancies and/or excess Hf atoms, which are generated at the initial forming (breakdown) operation. These conductive defects are initially accumulated at the top electrode (TE), where they migrated in response to the negative voltage applied to the TE in the preceding reset process. The CF is disconnected due to the presence of a depleted gap with low defect-concentration, hence high resistivity. The application of a positive voltage to the TE during the set operation results in the migration of the positively-ionized defects from the top reservoir into the

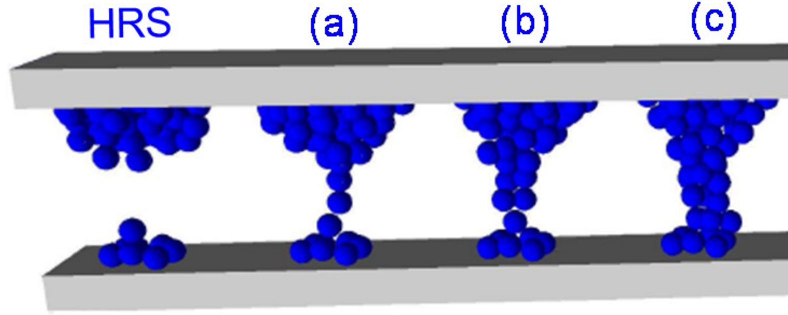

Figure 2.3: Schematic illustration of the ion migration phenomena at a CF during the set transition. Starting from the reset state, obtained by reset under a negative voltage, the application of a positive voltage results in the migration of positively-ionized defects (the blue dots in the sketch) from the top reservoir into the gap.

depleted gap, thus leading to a decrease of resistance. The abrupt set transition can be understood by noting that, as the depleted gap length Δ first decreases from (a) to (b) in Fig. 2.3 due to ion migration, the field across the remaining gap increases. This accelerates ion migration even further, causing the abrupt closure of the depleted gap and the corresponding increase of the current in Fig. 2.2. The reset transition proceeds right to left in Fig. 2.3, in that the depleted gap gradually opens due to ion migration toward the TE. Opposite to the set transition, the migration induced opening of the gap causes the decrease of the electric field and of the temperature at the two tips of the CF [41]. Due to such self-limited reset transition, the voltage must be increased to achieve effective opening of the gap within the timescale of the experiment [42].

The resistance R in the set state is controlled by I_C through the equation

$$R = \frac{V_C}{I_C}, \tag{2.1}$$

where V_C is a constant of about 0.4 V, corresponding to the value of the voltage drop across the device at the end of the set transition, usually in the timescale of 1 s [51]. V_C can be recognized as the corner voltage where the linear I-V curve of the set-state RRAM crosses the constant current region at I = I_C in Fig. 2.2. The constant V_C is also supported by the comparison with literature data for similar oxide MIM devices, as summarized in Fig. 2.3. The figure collects data for unipolar switching NiO [46], [47], [48] and various materials displaying bipolar switching, including HfO_2 [49], CuO [45], ZrO_x/HfO_x [43], and TiO_x [44]. All data align on the same line represented by eq. 2.3 with V_C of about 0.4 V, irrespective of the composition of the switching layer and of the electrodes [27]. Such material independence of V_C was explained by the small impact of the ion migration parameters on the set/reset kinetics [27], [32]. In addition, V_C appears to be almost completely insensitive to the experimental parameters, such as the (i) initial resistance, which spanned from full reset states to intermediate states with a resistance only slightly larger than the set state; the (ii) applied voltage, which also spanned between 0.4 V to a few volts; and the (iii) compliance I_C, which is in a relatively broad range between a few microamperes to

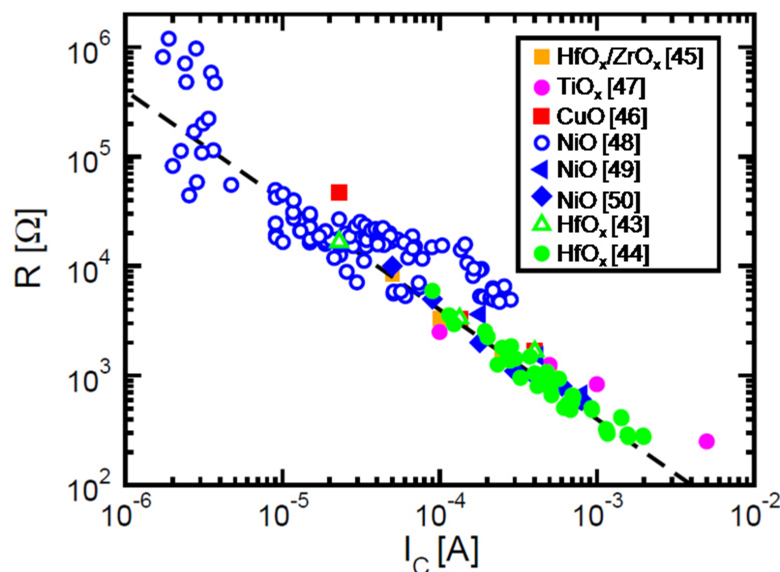

Figure 2.4: Scatter plot of set resistance R as a function of I_C. Several metal oxides from literature are compared, including ZrO_x/HfO_x [43], TiO_x [44], CuO [45], NiO [46], [47], [48], HfO_2 [49], [50]. All data roughly obey Eq. (2.3) relating R and I_C with V_C = 0.4 V.

more than 1 mA.

2.4 Complementary Switching

Complementary resistive switch (CRS) has been recently proposed as a promising memory element able to solve the sneakpath problem for future RRAM crossbar arrays [52]. Fig. 2.5 schematically shows the structure of the CRS (a) and the I-V characteristics (b) that can be obtained biasing this device with positive/negative voltage sweeps. From the architectural point of view the CRS basically consists of a stack of two conductive bridging RRAM (CBRAM) cells antiserially-connected. The result is a memory device with one inert top electrode (TE) and bottom electrode (BE), e.g. Pt, and two solid-electrolyte switching layers separated by a common active electrode, e.g. Cu. The two binary logic states necessary to store a bit of information corresponds to the conductive filament (CF) shunting either (1) the top switching layer, or (2) the bottom switching layer (see sketches in Fig. 2.5b). It is noteworthy that the overall device, at the end of a program operation shows always a high resistance thus avoiding the presence of leaky paths during the successive reading operation [52]. To switch the memory element from the high resistive state (1) to the high resistive state (2) of Fig. 2.5b a positive voltage sweep must be applied to the top electrode. This program operation causes first of all (i) a set process, *i.e.* formation of a CF in the bottom layer by Cu^+ migration toward the bottom electrode, and then (ii) a reset process, i.e. consumption of the CF in the top layer by Cu^+ migration back to the Cu common electrode.

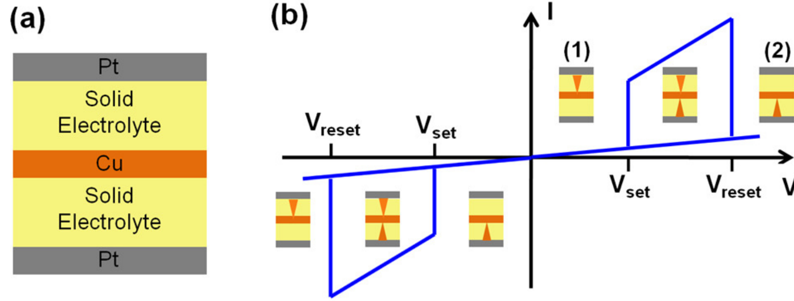

Figure 2.5: Schematic structure (a) and I âĹŠ V characteristics (b) of the conventional CRS based on an anti-serial connection of two CBRAMs [52]. Sketches of CF's evolution during voltage sweep are also shown.

In this way we succeeded in moving the CF from the up layer, i.e. state (1), to the bottom layer, i.e. state (2). In the same way a negative bias can be applied to switch the cell from state (2) to state (1) in Fig. 2.5b. The reading operation is performed applying a positive TE voltage above the set voltage V_{set} [52]. The fabrication of a CRS was also shown for Pt/ZrO_X/HfO_x/metal/HfO_x/ZrO_X/Pt and Pt/ZrO_X/HfO_x/ZrO_X/Pt stacks, indicating that not only CBRAMs but also oxide-RRAMs can be used for the realization of this kind of memory element [43].

The CRS shown in Fig. 2.5a or the ones proposed in [43] require a complex stacking of metal-oxide/metal layers thus resulting in a delicate fabrication process and in the fast degradation of the common active internal electrode [43, 52]. The integration complexity may be reduced by the introduction of complementary switching (CS), a new program operation that can be performed in single-stack nonpolar-RRAM devices [53]. CS can be obtained thanks to the natural asymmetry of reset state, where a depleted gap can be selectively created close to the BE or the TE by the application of a positive or negative voltage respectively. Fig. 2.6a shows the evolution of calculated CF shape obtained by simulations with a numerical model for unipolar/bipolar switching [41]. The initial shape (I) is obtained by the application of a negative reset inducing a depletion of conductive defects (*e.g.* excess Hf or O-vacancies in HfO_x) close to the BE. An applied positive voltage causes defects migration toward the BE, resulting first of all in CF reconnection (II), followed by depletion of the CF at the TE side (III). In the same way, a negative TE voltage can be applied to state (III) resulting first of all again in CF reconnection (IV), and then in gap formation (V). Anyway this time the depleted region is close to the BE thus leading to state (V) analogous to the initial state (I). It is noteworthy that each program sequence ends up with a reset operation which leaves the memory element always in a high resistive state. In this way, like in CRS, we are able to avoid the presence of leaky paths during the successive reading operation. Using the same numerical model for unipolar/bipolar switching [41] used to represent the evolution of CF under CS programming in Fig. 2.6a, it is possible to obtain the calculated I-V curves shown in Fig. 2.6b. It is here evidenced the intrinsically symmetric set/reset switching between low resistive states (II, IV) and high resistive states (I $\rightarrow$ V, III) under positive and negative voltage. The experimental validation of CS in

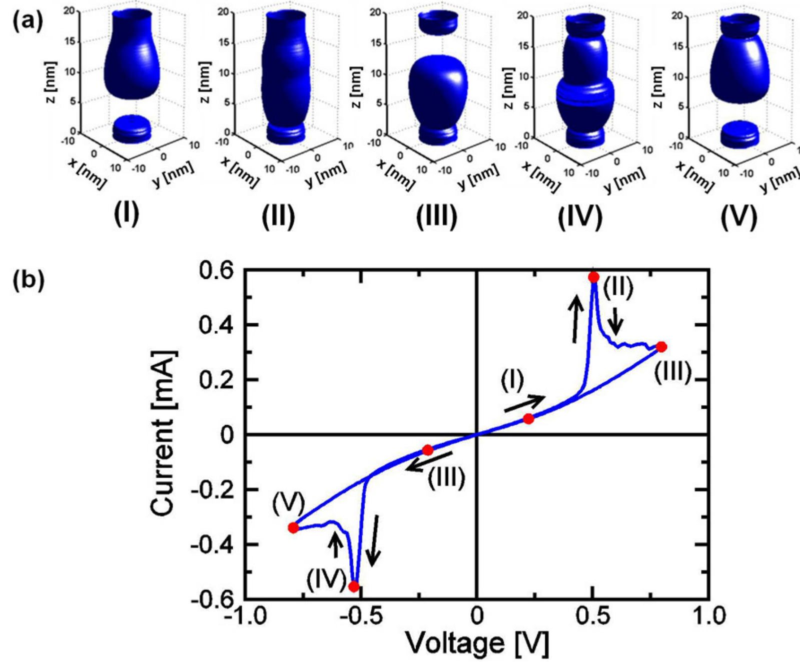

Figure 2.6: Calculated CF's shape (a) and corresponding I-V characteristics (b) for applied positive (I-III) and negative (III-V) ramped voltage. The broken CF (I) reforms as the gap is refilled by migrating positive ions (II), then a new gap is opened at the positive TE (III). Similarly, under V < 0 the gap is refilled (IV), then reopened at the BE [state (V), same as (I)]. The I-V curves evidence set (I $\rightarrow$ II) and reset (II $\rightarrow$ III) transitions under positive voltage, then set (III $\rightarrow$ IV) and reset (IV $\rightarrow$ V) transitions under negative voltage.

a single-stack nonpolar- RRAM device is shown in Fig. 2.7. This oxide-RRAM structure is a simple TiN-HfO_x-TiN stack with 5 nm-thick HfO_x as active layer material. The uniform Hf concentration profile allowed for a fully symmetric nonpolar- RRAM device. As a result, CS operation is possible and the voltage levels for both set (V_{set} ≈ 0.5 V) and reset ($V_{reset} \approx 0.7$ V) show only a minor asymmetry while changing the polarity of the applied bias.

It should be pointed out that CS cannot be generally observed in all bipolar-switching devices, but only in a subset of them. To highlight this point, Fig. 2.8 shows the measured I-V curves for two different RRAM devices with 20 nm-thick HfO_x, one device featuring a Hf-rich HfO_x buffer layer at the top electrode interface (asymmetric, solid curve), while the other has a uniform composition profile (symmetric, dashed curve). Under a positive voltage sweep without compliance limit, the symmetric device shows CS behavior, while the asymmetric device only shows a set transition followed by destructive breakdown. This is due to the Hf-rich layer acting as a virtually-unlimited reservoir for ion supply, thus hindering the complete migration of the ion reservoir from the top to the bottom electrode. These results suggest that CS cannot be observed in oxides with strongly asymmetric oxygen distribution.

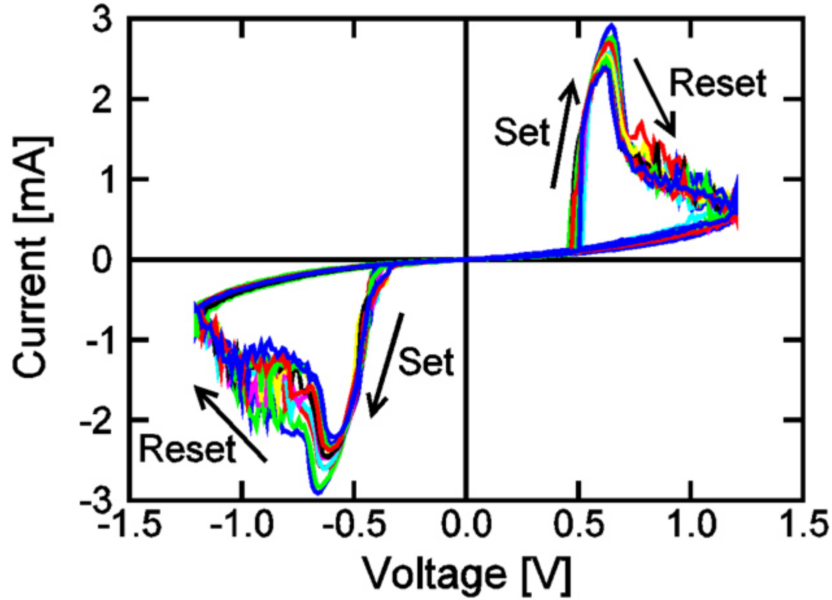

Figure 2.7: Measured I-V characteristics for complementary switching. In complementary switching, the current during set transition is not limited and the positive voltage sweep induces set followed by reset. The initial reset state with high resistance is recovered by a similar sweep under negative polarity.

2.5 A novel multilevel approach

Figure 2.9a shows the current-voltage (I-V) characteristics for a RRAM device, with 20 nm-thick HfO_x. The RRAM displays bipolar switching (BS), in that opposite voltage polarities are needed to activate/deactivate the CF. During the reset transition at negative voltage, the depleted gap is formed in the CF resulting in the negative high-resistance state (NHRS), which is sketched as state 1 in Figure 2.10c. The asymmetric shape of the CF is due to the positively ionized defects being attracted toward the top electrode during the negative-voltage reset transition. In the set transition at positive voltage, defects migrate from the top reservoir into the depleted gap, leading to the positive low-resistance state (PLRS). The amount of defects entering the gap, thus the resistance, R, of the PLRS, is controlled by the compliance current, I_C ,(1 mA in Figure 2.9a) [50]. The switching characteristic changes from BS to complementary switching (CS) when no current limitation is introduced during the set transition, [53] as shown in Figure 2.9b. Due to the absence of any current compliance, the CF growth in the gap region is only limited by the available conductive defects, thus reaching a minimum resistance at about 0.8 V, corresponding to state 2 in Figure 2.9c. A further voltage increase after set leads to the reset transition, caused by ion migration and accumulation at the bottom electrode. The positive high-resistance state (PHRS) is thus obtained, corresponding to state 3 in Figure 2.9c. Similar set and reset transitions are achieved under negative voltage, thus allowing to achieve the minimum resistance (state 4) and the NHRS (state 5), which is equivalent to the initial NHRS (state 1).

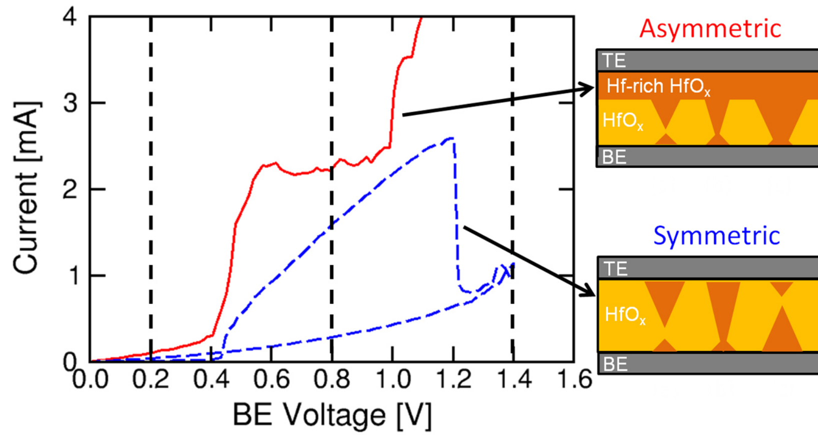

Figure 2.8: Measured I-V characteristics for asymmetric (solid curve) and symmetric (dashed curve) 20 nm-thick HfO_x RRAM device. CS is observed only for the symmetric device, while in the asymmetric device unlimited supply of migrating ions prevents reset. A uniform composition profile is therefore needed for CS.

Figure 2.9c indicates that PHRS (state 3) and NHRS (state 1 or 5) differ by the location of the accumulated defects at the bottom or top electrode, respectively, although the two states share the same value of R. This allows a duplication of the number of RRAM states corresponding to any given R: in this level-duplication scheme, two states with the same R differ by the orientation of the CF determined by the polarity of the voltage inducing ion migration, similar to the multibit operation of charge-based memory with localized carrier injection at the source or drain side of the transistor [54]. The duplication scheme results in a dramatic enhancement of data storage density: for instance, four R levels, equivalent to 2 bits, are duplicated to 8 states, or 3 bits, which corresponds to a 50% increase of information stored in the array. Figure 2.10 illustrates the extension of the level duplication scheme to any R level. Starting from the NHRS (Figure 2.10e), a positive set operation is carried out in Figure 2.10a with I_C = 0.625 mA (solid line), thus achieving the PLRS (Figure 2.10f). The compliance current dictates the PLRS resistance according to R = $V_C/I_C \approx 0.35$ V/0.625 mA ≈ 0.56 kΩ , where V_C is the final voltage across the RRAM at the compliance level I_C [37]. The same value of R is obtained by applying a negative voltage sweep to the PHRS (Figure 2.10i) with the same I_C , as shown in Figure 2.10a (dashed line). The negative low- R state (NLRS in Figure 2.10j) is thus achieved with the same R as the PLRS in Figure 2.10f, but with opposite defect profile in the CF. The two states can be distinguished by the positive read operation shown in Figure 2.10b: NLRS undergoes a BS reset transition under positive voltage with $I_{reset} \approx I_C$ [37], while PLRS displays CS with $I_{reset} \approx 4$ mA $\gg I_C$. This is because a positive voltage to the PLRS (Figure 2.10f) leads to ion migration toward the bottom electrode, causing the transition to PHRS (Figure 2.10i) through CS. In general, PLRS and NLRS display almost identical I - V curves in the reset transition, except for the opposite polarity. These results support the picture of identical defect profiles along the CF in PLRS and NLRS, except for the opposite direction as described in Figure 2.10f and j. Similar positive read characteristics are

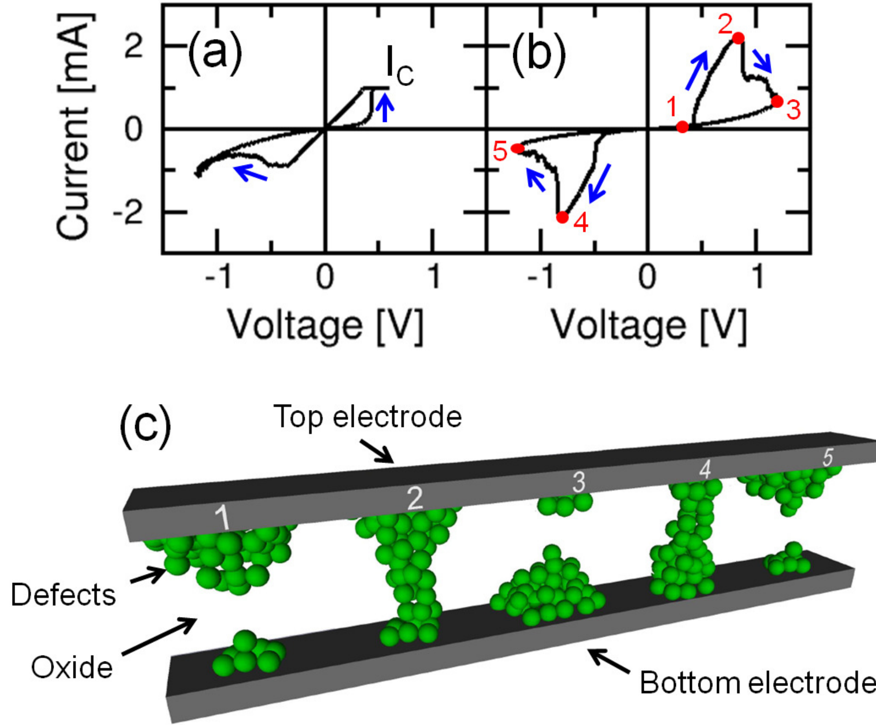

Figure 2.9: a) Measured bipolar switching (BS), and b) complementary switching (CS) characteristics for a RRAM with 20-nm-thick HfO_x , and c) CF shapes in states 1-5 along a full CS cycle. In BS, the set transition under positive voltage is limited to a compliance current (I_C) which controls the resistance (R), and the reset current (I_{reset}) during the negative-bias reset transition. No I_C limit is instead used during CS, resulting in a large CF growth during the positive-bias set transition (state 2), followed by reset transition to positive high-resistance state (PHRS) (state 3). Application of a negative bias results in similar set transition to state 4 and reset transition to NHRS (state 5, equal to state 1).

shown in Figure 2.10c for PLRS and NLRS with a larger CF size, due to an increased I_C = 1.25 mA. Similar data are shown in Figure 2.10d for I_C = 2.5 mA. The corresponding PLRS/NLRS are schematically shown in Figure 2.10g,k (I_C = 1.25 mA) and Figures 2.10h,l I_C = 2.5 mA). The defect concentration in the depleted gap increases in PLRS and NLRS for increasing I_C from left to right in Figure 2.10e-l. Figures 2.10c,d further demonstrate that NLRS and PLRS display BS and CS, respectively, thus can be discriminated by their respective I_{reset} although having the same resistance.

Figure 2.11 shows the measured R and I_{reset} for PLRS and NLRS at increasing I_C . PLRS displays a constant $I_{reset} \approx 4$ mA since I_{reset} depends on the minimum resistance state 2 in Figure 2.9c, which is solely dictated by the amount of available defects in the CF. These are pre-determined by the current compliance at electroforming and do not depend on the set operation [55]. On the other hand, I_{reset} is inversely proportional to R in NLRS, since the reset voltage V_{reset} in BS remains approximately constant ($V_{reset} \approx 0.4$ V) due the voltage-driven nature of BS, thus leading to I_{reset} = V_{reset}/R $\propto$ 1/R [37]. As a result, 3 bits are stored with only 4 resistance levels and 8

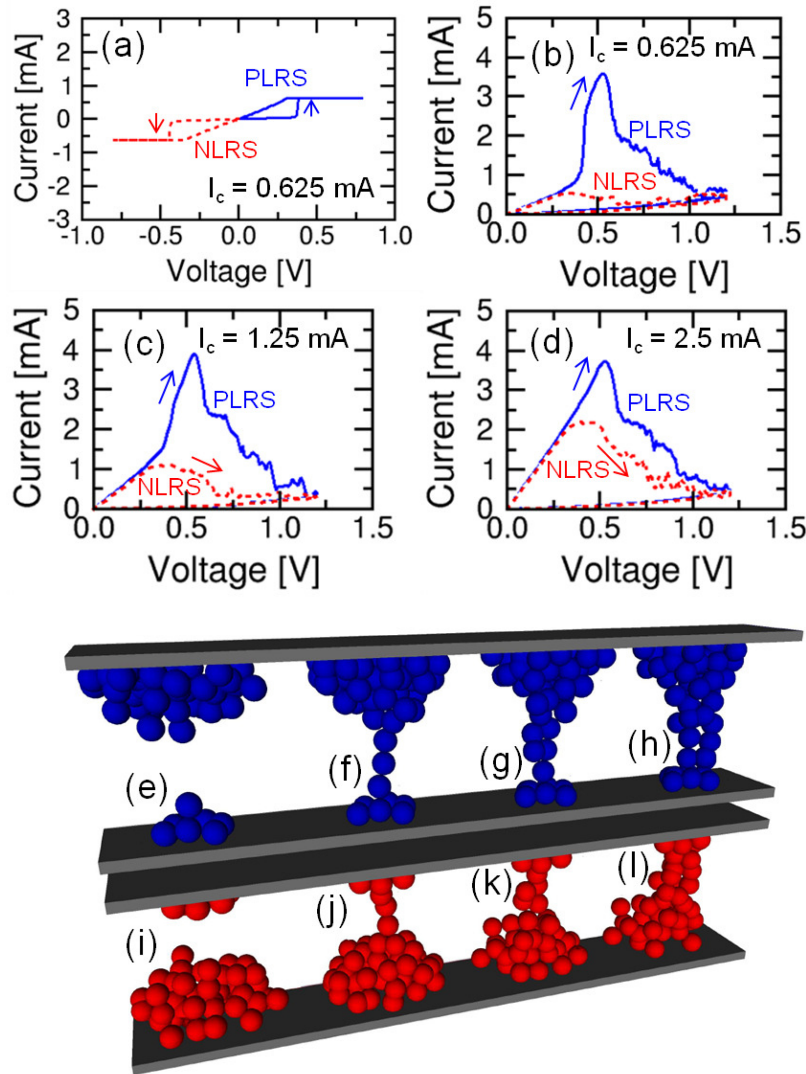

Figure 2.10: a) Measured I-V curves during positive and negative set transitions at a current compliance I_C = 0.625 mA for programming PLRS and NLRS, respectively, and b-d) measured response to a positive read voltage, for increasing I_C , namely 0.625 mA (b), 1.25 (c), and 2.5 mA (d). e) Schematic illustration of the CF shape in the NHRS, and f-h) CF shape in the PLRS at increasing I_C , thus leading to more defects in the depleted gap close to the bottom electrode. i) Schematic illustration of the CF shape in the PHRS, and j-l) CF shape in the NLRS at increasing I_C.

different CF states, namely 3 PLRS, 3 NLRS, 1 PHRS and 1 NHRS. For any given R , e.g. , the values R_1 , R_2 , and R_3 of programmed states in Figure 2.10b-d, NLRS and PLRS can be discriminated by their I_{reset} in response to a positive voltage, namely a low or high I_{reset} reveals NLRS or PLRS, respectively. On the other hand, for high-R states, a high I_{reset} corresponds to NHRS, displaying CS under a positive voltage,

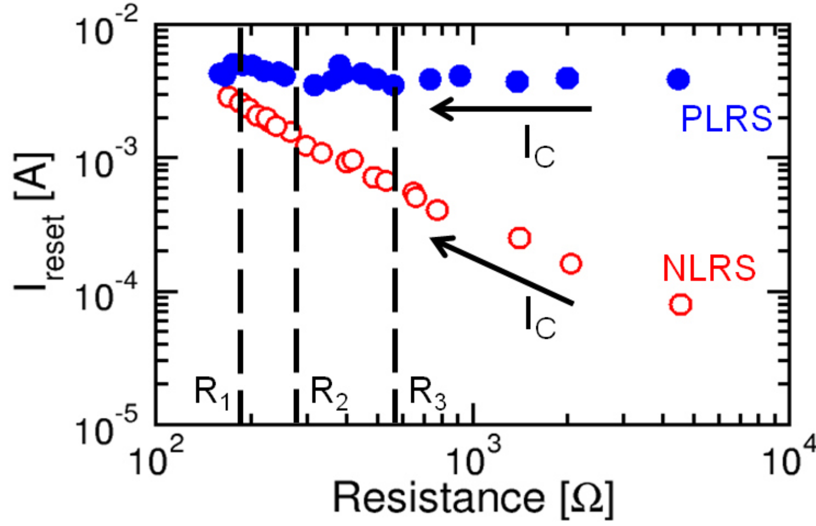

Figure 2.11: Scatter plot of R and I reset for PLRS and NLRS at increasing I_C . Two states with the same R can be discriminated by I_{reset} under positive read, thus allowing the duplication of RRAM states.

while PHRS do not show any significant resistance change, since the positive voltage would push ionized defects toward the bottom electrode, where they are already accumulated. Note that the positive read operation is destructive, in that the PLRS/NLRS must be restored from the PHRS after read.

The physical concept of PLRS/NLRS is further clarified by simulation results in Figure 2.12, obtained by a numerical model for set/reset transitions in metal-oxide RRAM [41]. The model relies on the solution of the drift/diffusion equation for ions with temperature-dependent mobility and diffusivity. Since oxygen vacancies act as doping in metal oxides, [56–58] a higher local defect concentration enhances the electrical conductivity. Therefore, migration-induced depletion and filling of a CF gap in the model account for the reset and set transitions, respectively [41]. Figure 2.12a shows the calculated I- V curves during the positive/negative set transitions to achieve PLRS and NLRS respectively. Figure 2.12b shows the positive read characteristics for PLRS and NLRS, displaying CS and BS, respectively, in agreement with the experimental results in Figure 2.10b-d. Figure 2.12c shows the calculated map of defect concentration, n_D , in the radial coordinates, for the initial NHRS, the PLRS after positive set transition and the final PHRS after positive read. Defects are accumulated at the top electrode in NHRS, with a depleted gap close to the bottom electrode. The gap is partially filled after the set transition in the PLRS, while the positive read voltage finally induces CS and a consequent inversion of the orientation of the doping profile, resulting in the PHRS. Figure 2.12d shows similar maps of n_D for the initial PHRS, the NLRS state after negative set transition and the final PHRS, recovered after read under positive voltage. Calculations agree well with the experimental characteristics and with the physical picture in Figure 2.10 , thus supporting this multilevel scheme as a robust storage approach for extreme scaling of information density in RRAM.

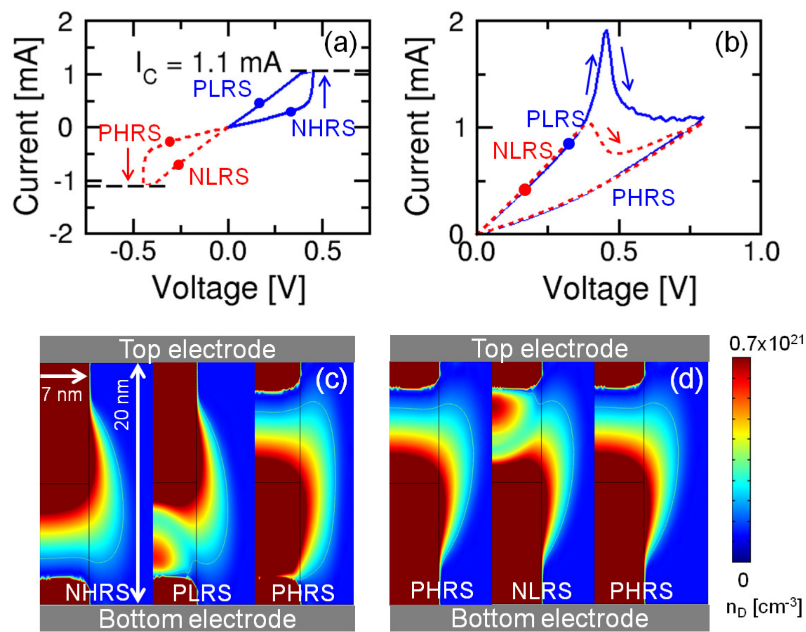

Figure 2.12: a) Calculated I-V curves during positive/negative set transition at I_C = 1.1 mA, and b) the corresponding response of NLRS and PLRS under a positive voltage read. c) Calculated defect distributions for NHRS, for PLRS obtained after positive set transition and for PHRS achieved in response to a positive read voltage, resulting in CS. d) Calculated defect distributions for PHRS, for NLRS obtained after negative set transition and for PHRS at the end of the reset transition under positive read voltage.

Switching variability and set failure in 1T1R RRAM

This chapter is dedicated to program variability. Starting from the experimental evidences two different models are presented to explain switching variability and its dependence on programming current. A new failure mechanism for set process is also discussed.

3.1 Introduction

To be competitive with Flash NAND, resistive-switching memory must reduce the power consumption. Low-power operation is possible by limiting the size of the conductive filament (CF) that is activated/deactivated during switching operation of the RRAM. This is generally achieved by limiting the current during the set operation, the reconnection of the CF. To demonstrate low power operation of RRAM, one-transistor/one-resistor (1T1R) structures were used where the integrated MOS transistor limited the current during the set process [39,46,59,60]. Through this approach, the reset current was successfully reduced below 10 μA [46,60].

In the low-current regime, however, reliability issues arises due to the small size of the CF. Atomic-size CFs are prone to accelerated diffusion at elevated temperature [61, 62] and enhanced random telegraph noise (RTN) [63]. In addition, size-dependent variability issues arise due to the small number of defects involved in the CF [64, 65]. For instance, it was shown that single-defect generation/migration may lead to significant fluctuation of the resistance during the reset transition. To control and predict reliability of RRAM in the low power regime, variability of set/reset processes must be evaluated and modeled.

Set-reset characteristics were studied on 1T1R structures described in Chapter 1 and sketched in Fig. 3.1. The integrated select transistor served as current limiter during the set transition. The current compliance I_C in the set transition was controlled by the gate voltage V_G.

To initialize the RRAM operation, electrical forming was achieved by the application of a positive TE voltage while I_C was kept to a small value (I_C = 10 μA) by the

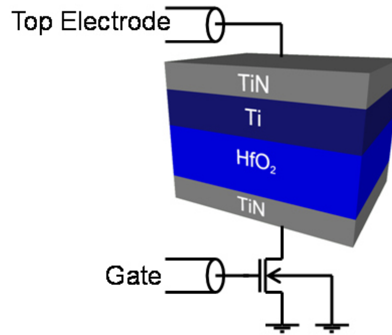

Figure 3.1: Schematic layout of 1T1R structure, highlighting the stack composition in the RRAM device.

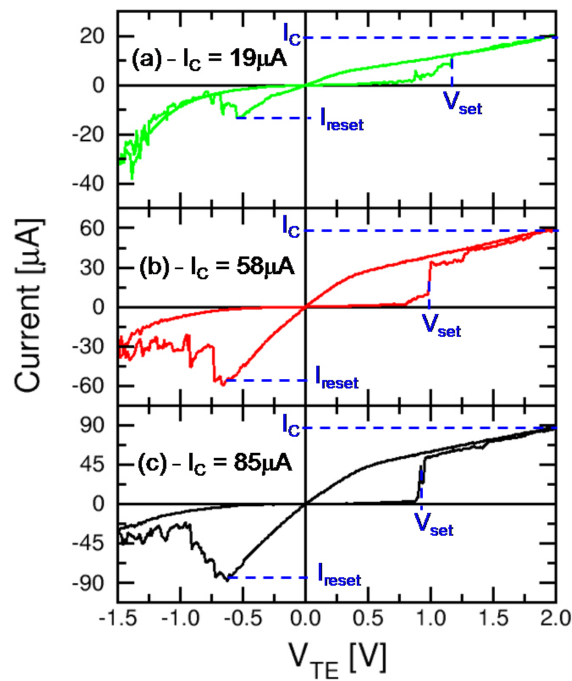

Figure 3.2: Measured I-V curves for increasing I_C = 19 μA (a), 58μA (b) and 85 μA (c). The definitions of switching parameters V_{set}, I_C and I_{reset} are also shown.

gate voltage. After forming, the RRAM was switched to the high-resistance state, or reset state, by the reset transition, consisting of a negative V_{TE} sweep while a high gate voltage (V_G = 1.5 V) was applied to minimize the transistor resistance. The set transition was induced by the application of a positive voltage V_{TE} sweep while the compliance current I_C was limited by a suitable value of the gate voltage V_G. Fig. 3.2 shows the measured I-V curves for current compliance values I_C = 19 μA (a), 60 μA

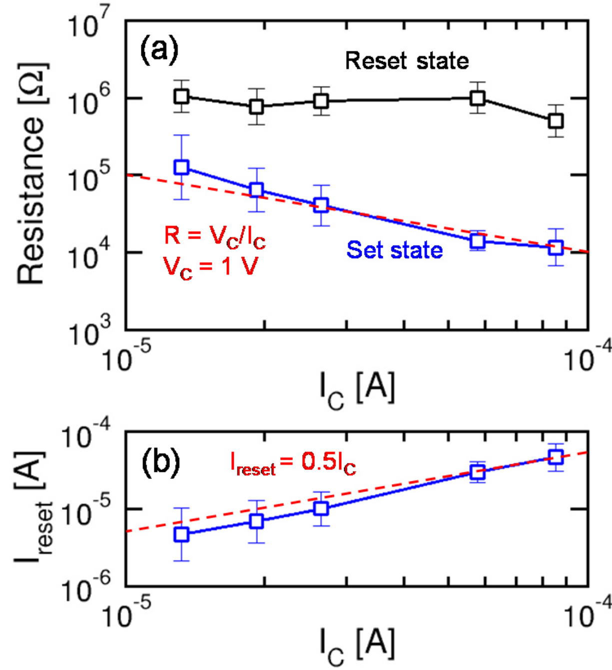

Figure 3.3: Measured R for the set and reset states (a) and measured I_{reset} as a function of I_{reset} (b). The I_C-dependence of set-state R and I_{reset} are well described by the universal switching laws R = V_C/I_C and $I_C \propto I_{reset}$.

(b) and 85 μA (c). As already discussed in the previous Chapter the set transition takes place at positive V_{TE} as an abrupt decrease of the resistance R at the set voltage V_{set}, while the reset transition appears as a more gradual increase of R under negative V_{TE}. The reset current I_{reset} is defined as the onset of the reset transition to larger resistance. Note that the current may even increase over I_{reset} during the reset sweep, particularly for low I_C, due to the leaky reset state. As I_C is increased, the set-state resistance R decreases while I_{reset} decreases [51].

Fig. 3.3 shows the measured R in the set and reset states (a) and I_{reset} (b) as a function of I_C. The results agree with the universal behavior of set and reset transitions previously reported in [51]. In particular, the set-state resistance follows the equation R = V_C/I_C with V_C = 1 V, as expected from the voltage controlled dynamics of ion migration [37]. On the other hand, the reset-state resistance remains approximately constant in our I_C range, due to the constant reset conditions used in our work (same V_G, same maximum V_{TE} along the negative sweep). Finally, the reset current I_{reset} is proportional to I_C, due to the set/reset processes relying on the same physical mechanism, that is ion migration from/to a reservoir at the TE [37]. As a result, the characteristic voltages and currents for set and reset transitions are approximately the same. The slightly asymmetric switching, where I_{reset} is smaller than I_C, might be due to the different activation energies for CF activation and deactivation, as previously observed for conductive bridge RAM (CBRAM) devices [41].

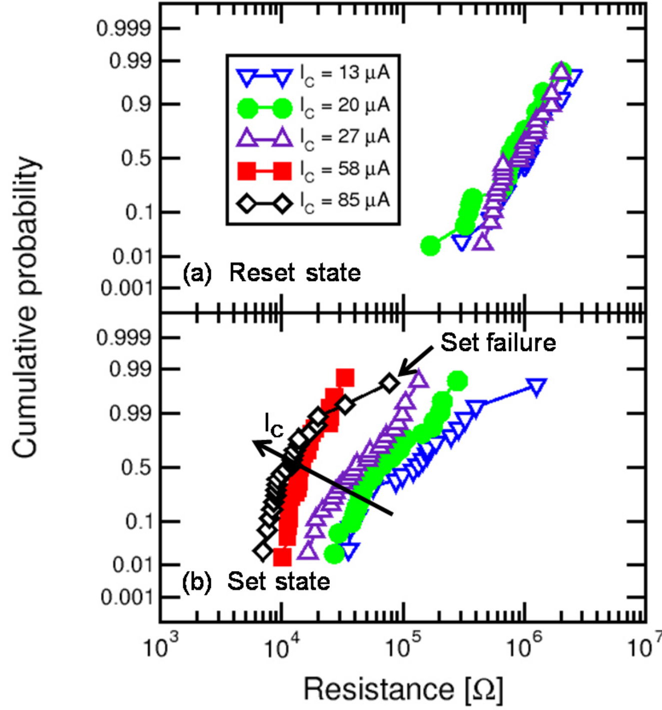

Figure 3.4: Cumulative distributions of R for the reset state (a) and for the set state (b) at increasing I_C. Note the high-R distribution tail for I_C= 85 μA, causing set failure.

3.2 Set state variability

As I_C is decreased in Figs. 3.2 and 3.3, the variability of set state parameters, namely R and I_{reset}, clearly increases. The reset transitions features random steps and fluctuations, which can be explained by individual defects or defect clusters migrating across the depleted gap during the reset transition [41]. As the CF size decreases, the number of individual migrating defects decreases, thus causing less current fluctuations in the reset transition. On the other hand, the amplitude of each fluctuation increases compared to I_{reset}, thus causing the increasing reset noise at small CF size. Also, the occurrence of each current fluctuation becomes more randomly distributed along the reset transition and the resistance increase with voltage becomes less predictable for decreasing I_C.

We studied the variability of programmed states through a statistical analysis of R at increasing set/reset cycling and for variable I_C. To this purpose, set/reset switching cycles were repeated 30 times for I_C = 13, 19, 27, 58 and 85 μA. Fig. 3.4 shows the cumulative distributions of R for the reset state (a) and the set state (b) at increasing I_C. All measurements were carried out on the same device and for repeated DC cycles. The reset state R shows almost no dependence on I_C, which might be explained by the reset parameters (maximum negative V_{TE} = -1.5 V and V_G = 1.5 V) being the same

irrespective of I_C. Also, the maximum negative V_{TE} was sufficiently large to prevent excessive R variability due to the random current fluctuations in the reset transitions of Fig. 3.2.

3.2.1 Analytical model for cycle-to-cycle variability

We focus our attention on the variability of the set-state resistance in Fig. 3.4b. The cumulative distributions of set-state R show a clear dependence on I_C, with an increase of the distribution spread on the logarithmic scale for decreasing I_C [66]. The resistance variability was monitored by the relative spread σR/R, where σR is the standard deviation of resistance and R is the distribution average. The I_C-dependent variability is more evident in Fig 3.5a, showing the experimental σR/R as a function of I_C. For I_C < 70 μA, σR/R increases for decreasing I_C with a slope of about -0.65 on the logarithmic scale. The I_C-dependent variability can be explained by the fluctuation of the number of defects contributing to the CF. As the CF becomes smaller at decreasing I_C, the number of defects in the CF decreases, as shown by the schematic illustration of a large CF in Fig. 3.5b and a small CF in Fig. 3.5c. Correspondingly, the relative spread of the injected defects during the set transition increases, resulting in a larger relative spread of CF size, hence resistance.

To describe the size-dependent set-state variability, we developed an analytical model for few-defect fluctuation during the set transition. Assuming an ohmic-conduction model for the set state, R can be estimated as [67]:

$$R = \rho \frac{t_{ox}}{A}, \tag{3.2}$$

where ρ is the resistivity of the CF, t_{ox} is the HfO_x layer thickness and A is the area of the CF cross section, given by A = $\pi\phi^2/4$ where ϕ is the effective CF diameter. The number of defects N in the CF is expected to be proportional to the CF volume, hence to the CF area A since t_{ox} is kept fixed by the stack geometry and does not depend on I_C. Based on the ohmic model of Eq. 3.2, we thus conclude the following proportionality between R and the microscopic parameters of the CF:

$$R \propto A^{-1} \propto N^{-1}, \tag{3.3}$$

We then assume a Poisson statistics for the defect-number fluctuation in the CF in the set state. According to the Poisson statistics, the standard deviation σN of the number of defects in the set state is given by:

$$\sigma_N \propto A^{-1} \propto N^{-1}, \tag{3.4}$$

Eq. 3.4 should be viewed as a first order approximation, since the number of injected defects might be sub-Poissonian as a result of the negative feedback in the set transition at constant current I_C [37]. The relative spread of R thus reads:

$$\frac{\sigma_R}{R} \propto \frac{\sigma_A}{A} \propto \frac{\sigma_N}{N} \propto N^{-0.5} \propto I_C^{-0.5}, \tag{3.5}$$

which predicts a slope -0.5 in the logarithmic plot of Fig. 3.5a. The slightly larger slope (-0.65) in the experimental data might be due to the limited validity of the ohmic model,

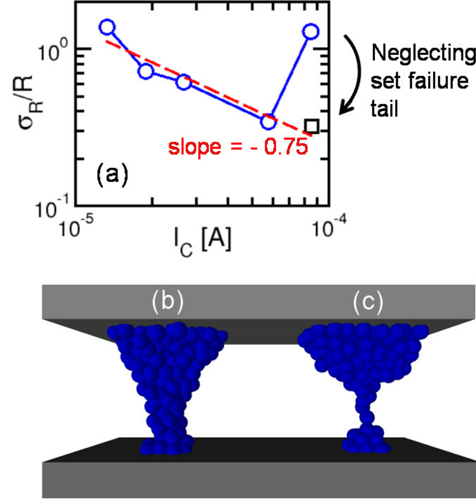

Figure 3.5: Relative spread σ_R/R for the set state as a function of I_C (a) and schematic illustration of large (b) and small CF (c), corresponding to large and small I_C, respectively. The open red square in (a) was obtained by neglecting states affected by CS, *i.e.* tail states in Fig. 3.4

particularly for small CF characterized by a relatively high R. In the high-R range, the transport regime changes from ohmic to thermally-activated hopping at localized defects [68], as a result of the smaller density of defects in the CF. In this conduction regime, an additional source of variability is the random defect position, while our model in Eqs. 3.2-3.5 only considers random number fluctuation. Nevertheless, our analytical model can provide a simple yet accurate estimation of the I_C-dependent variability of programmed state in RRAM.

The variability analysis repeated on different devices shows similar results, highlighting that the device-to-device variability is smaller or comparable to the cycle-to-cycle variability, as also reported in literature [69].

3.2.2 Failure of set operation

For I_C > 60 μA Fig. 3.5a shows that the relative spread unexpectedly increases in contrast to Eq. 3.5. This is because of the tail (marked at set failure) at high R in Fig. 3.4a for relatively high I_C. Set failure negatively impacts RRAM reliability, particularly for multilevel cell operation. To better understand the set-failure mechanism, Fig. 3.6a shows the measured I-V curve in correspondence of set failure in the high-R tail of Fig. 3.4a. For positive voltage above V_{set}, an unusual reset event occurs at V_{reset}. This can be explained in terms of CS [53], as shown in Fig. 3.6b: in the initial reset state (A), defects are accumulated at the TE because of the previous negative reset operation, while a depleted gap causes a large R. The drift of positively ionized defects into the gap results in the transition to the set state (B) at V_{set}. A further increase of voltage, however, can induce ion accumulation toward the bottom electrode (BE), causing a gap opening close to the TE and a consequent transition to a new reset state (C) [66].

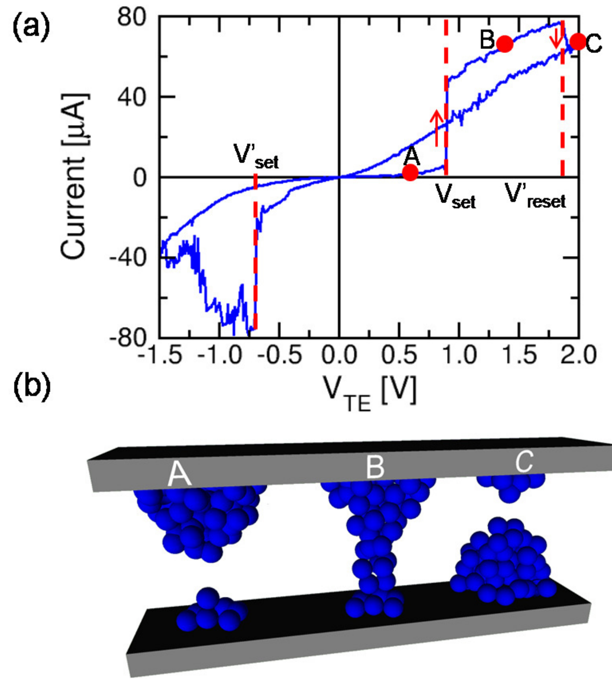

Figure 3.6: Measured I-V curve for a set/reset cycle in the high-R tail of Fig. 3.4b, showing the set-failure mechanism (a), and schematic illustration of the CS process responsible for set failure (b). A reset transition at positive voltage is seen at V_{reset}, due to the transition from B to C.

Note that the voltage V_C across the RRAM after ~ 1 s from the set transition is shown to remain approximately constant for variable current compliance I_C, *e.g.*, $V_C \approx 0.4$ V in HfO_x RRAM [37, 65, 70]. However, the CS effect evidences an increase of V_C with current, allowing self-limited current followed by reset transition because of the excessive voltage stress inducing ion migration within the CF [71]. The voltage stress at high current can explain the reset transition at V_{reset} in Fig. 3.6b.

Further evidence for CS in Fig. 3.6b is given by the device behavior at negative voltage in Fig. 3.6a; as the voltage is swept to negative values, a set transition is first observed at $V_{set} \approx$ -0.7 V because of gap filling close to the TE [transition from C to B in Fig. 3.6b]. Then R increases for V < V_{set} because of ion migration to the TE and gradual increase of the depleted gap (transition from B to A in Fig. 3.6b). The sharp set transition followed by the reset transition is a clear signature of CS according to previous results for one resistor RRAM devices [71]. The observed CS can also explain previously observed unipolar switching, causing reset during set pulses at relatively large voltage in HfO_x RRAM [72]. Fig. 3.7a shows that the frequency of CS approaches 30% for I_C = 85 μA, while CS is almost negligible for smaller values of I_C. This can be explained by Fig. 3.7b, schematically showing the I-V curve of the RRAM alone, thus corrected by the voltage drop at the transistor, during the set transition. The figure also shows the expected behavior of V_C (R = V_C/I_C as reported in

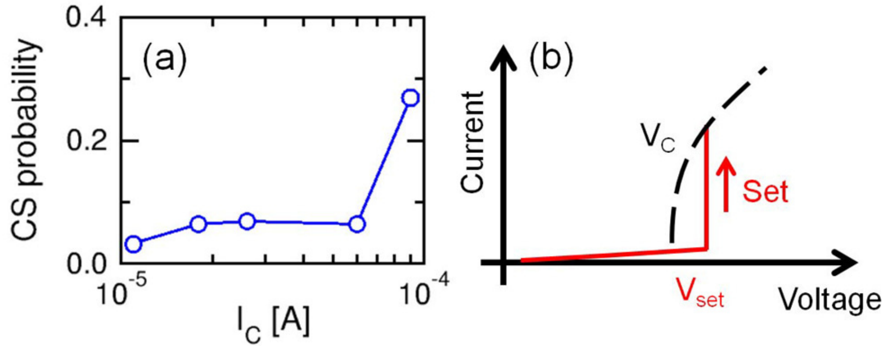

Figure 3.7: (a) Probability of CS as a function of I_C and (b) schematic I-V curve during (solid line) set transition and (dashed line) current dependent V_C. V_C increases at increasing current as evidenced by self-compliance in CS experiments.

Chapter 2), namely the voltage across the CF after a given time (e.g., 1 s in typical dc measurements) from the set transition. The voltage V_C is generally below V_{set}, thus causing a voltage snap-back at the set transition. As the current increases, however, V_C increases as evidenced by the self-compliance effect during CS experiments [71]. The V_C increase might be due to the increased effective energy barrier E_{ion} for CF growth because of mechanical stress and/or absence of grain boundaries or other defects acting as migration channel. For large I_C, the enhanced voltage stress on the RRAM causes reset transition, where migration of defects from the CF to the BE is energetically preferred with respect to defect migration from the TE reservoir to enlarge the CF size. Voltage stress might not be the only driving force for set failure. Other possible explanations include current stress, where the higher current density at high I_C might cause additional stress through Joule heating and electromigration. Set failure might be avoided by a thoughtful choice of the set pulse amplitude V_P and/or pulse duration. Based on Fig. 3.6a, V_P might be chosen within the window between V_{set} and V_{reset}, to minimize the probability of failure because of incomplete set (caused by $V_P < V_{set}$) or CS (caused by $V_P > V_{reset}$). Note that both V_{set} and V_{reset} have statistical nature arising from the energy landscape of E_{ion} at the CF. In addition, the reset state induced by the reset transition above V_{reset} cannot be recovered at positive voltage, rather a negative set/reset operation is needed for re-initialization [72]. Therefore, program-verify schemes with a gradual increase of V_P seem most appropriate for a reliable set operation. In addition, set failure may be suppressed by a careful engineering of the oxygen exchange layer or of the forming process, aimed at avoiding CF rupture at the TE side due to CS [66].

3.2.3 Monte Carlo model

The set and reset transitions can be described as the change of shape and size of the CF resulting from the migration of ionized defects, such as oxygen vacancies and excess metal atoms. A numerical model based on temperature- and field-accelerated ionic drift-diffusion was recently reported [41]. Fig. 3.8 shows numerical simulation results

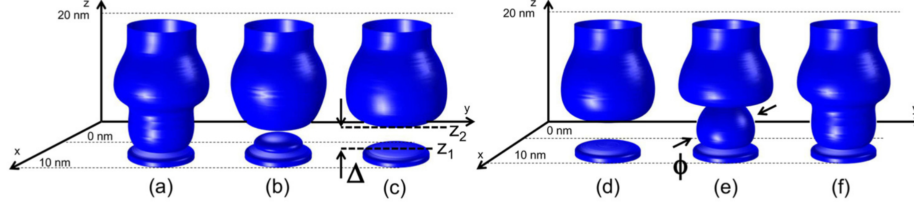

Figure 3.8: Contour plots of the calculated defect concentration for a reset transition (a, b, c) and a set transition (d, e, f). The defect concentration was calculated by a numerical model for set/reset processes due to ion migration. The gap length Δ increases during the reset transition, while the CF diameter ϕ in the gap region increases during set transition.

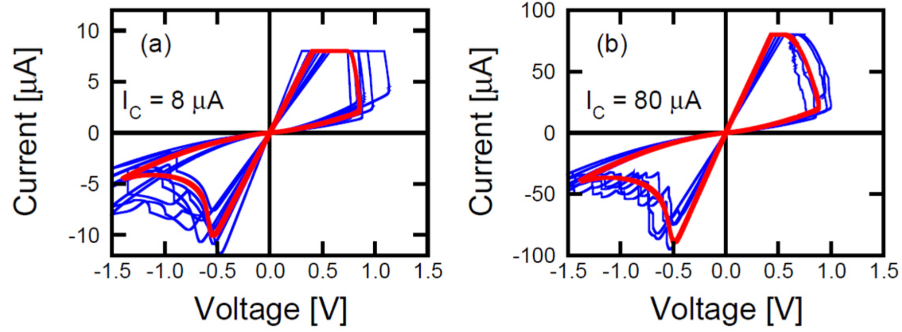

Figure 3.9: Calculated I-V curves obtained by the analytical model (thick line) and repeated I-V curves obtained by the Monte Carlo variability model (thin line) for I_C = 8μA (a) and 80μA (b). The statistical fluctuation of resistance, switching current and switching voltage increases for decreasing I_C.

for the contour plot of the defect density during reset transition (a, b, c) and set transition (d, e, f). Starting from a continuous conductive filament (Fig. 3.8a), the reset transition results in the gradual opening of a depleted gap due to the ion migration toward the negatively-biased top electrode (Fig. 3.8b and c) [73]. The depleted gap has a high resistivity, therefore can account for the resistance increase during reset. To analytically describe the reset transition, the growth rate of the gap length Δ can be written as:

$$\frac{d\Delta}{dt} = Ae^{-\frac{E_A - \alpha qV}{kT}} \tag{3.6}$$

where A is a pre-exponential coefficient [ms^1], E_A is the energy barrier for ion migration, α is a barrier lowering coefficient, V is the voltage drop across the gap, k is the Boltzmann constant and T is the local temperature at the injecting edge z_1 (see Fig. 3.8c). Eq. 3.6 relies on reset transition being controlled by ion hopping which is a thermally activated process with energy barrier E_A [74, 75]. It is thus assumed that the gap depletion rate increases proportional to the defect migration velocity, described by the Arrhenius law in Eq. 3.6. Starting from the reset state in Fig. 3.8d (same as the final state in Fig. 3.8c), the set transition causes defect migration toward the bottom electrode as a result of the positive voltage applied to the top electrode. Defects are

therefore injected into the gap leading to an increase of defect concentration which appears as an increase of CF diameter ϕ within the gap region (Fig. 3.8e and f). Defect migration is sustained by the CF reservoir at the top electrode side. Similar to Eq. 3.6, we can therefore describe the diameter growth rate by:

$$\frac{d\phi}{dt} = Ae^{-\frac{E_A - \alpha qV}{kT}} \tag{3.7}$$

where the same parameters as in Eq. 3.7 were used, except for T which is now evaluated at the injecting top boundary at z_2. The same coefficient A as Eq. 3.5 was used in Eq. 3.6 for simplicity [73].

The resistance R of the device was calculated as the series of three CF regions, namely (i) a stub at the top-electrode side, (ii) a gap region and (iii) a stub at the bottom electrode side. The two stubs were assumed to have a fixed diameter, dictated by I_C during the forming operation. The gap region was assumed to have length Δ, dictated by the reset operation, and a filament diameter ϕ, dictated by the set operation. This allowed for the calculation of the CF resistance for any set/reset state. Fig. 3.9 shows the I-V characteristics, thick line, obtained by the analytical model for I_C = 8 μA (a) and I_C = 80 μA (b). In the model, I_C controls the set state R and I_{reset}, similar to experimental results in Fig. 3.2. This is further confirmed in Fig. 3.10, showing measured and calculated R for the set state (a), I_{reset} (b) and V_{reset} (c) as a function of I_C. Experimental results were obtained as the median value over a statistics of 50 cycles for the same RRAM device. In Fig. 3.10 data are reported for undoped [66] and doped [76] HfO_x showing the same behavior. Calculations were obtained for E_A = 1.2 eV, α = 0.05 and A = 300 ms^1. The resistance decreases at increasing I_C as a result of the larger diameter ϕ achieved during set transition [37]. The product of R and I_C is approximately constant and equal to $V_C \approx 0.5$ V, which describes the voltage needed to activate ion migration in the timescale of the experiment (about 1 s in this work) [37]. In fact, the voltage across the device decreases due to CF growth at a constant I_C, therefore the growth process stops when the voltage equals the critical value V_C for ion migration. The reset current I_{reset} increases according to I_{reset} $approx$ I_C in Fig. 3.10b, while V_{reset} is approximately constant in Fig. 3.10c [51]. Calculated results from the analytical model show good agreement with data, supporting our analytical model for set/reset processes.

To account for switching variability, random migration of discrete defects was introduced in the analytical model by a Monte Carlo approach. Fig. 3.11 shows a schematic for the discrete migration of ionized defects during set transition (a) and reset transition (b). In the Monte Carlo model, each defect (or defect cluster) has a characteristic energy barrier E_A describing its hopping mobility. The CF or gap growths therefore follow a sequence of discrete defect events, each characterized by a random value of E_A and a corresponding migration rate. The energy barrier was extracted randomly from a uniform distribution between 0.7 and 1.7 eV, which is centered around the average value of 1.2 eV used in the calculations of Figs. 3.9 and 3.10. The random E_A allows to describe the structural change of the HfO_x material in the gap region, due to change of the composition profile resulting from the growth of the CF during set transition and the growth of a depleted gap during reset transition. As a result, the structure of the migration channel changes with time during the transition, resulting in a random change of the energy barrier for defect migration. A constant volume of 0.6

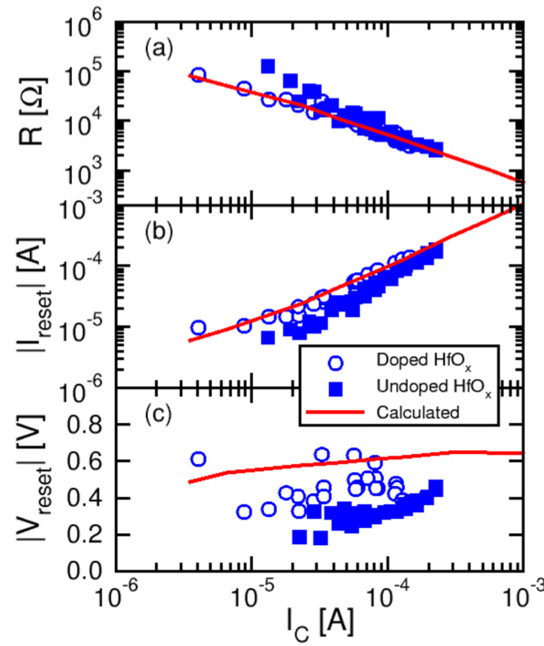

Figure 3.10: Average of measured and calculated set state resistance R (a), reset current I_{reset} (b) and reset voltage V_{reset} (c) as a function of I_C. The absolute values of current and voltage are reported. The average values were obtained over 50 cycles at each I_C. Resistance (a) and V_{reset} (b) are corrected by the voltage drop across the select MOSFET in the 1T1R structure. Data for undoped HfO_x RRAM samples from [66] and for doped HfO_x [73] are reported for comparison.

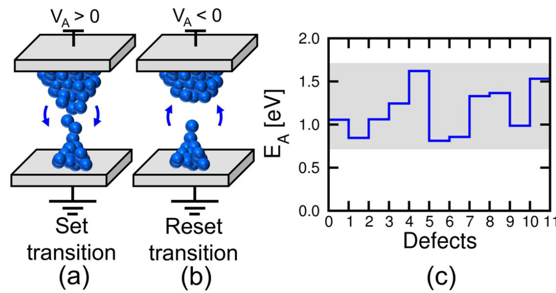

Figure 3.11: Schematic illustration of the discrete defect migration in the Monte Carlo model for variability. Set transition is described as the migration of discrete defects, resulting in the CF diameter growth (a) while reset transition is described as the migration of discrete defects, resulting in the gap length increase (b). Energy barriers for the injection of individual defects, or defect clusters, are randomly extracted within a uniform distribution between 0.7 eV and 1.7 eV (c)

nm^3, corresponding to about 13 point defects in HfO_x, was attributed to each defect cluster with a certain value of E_A [73]. Fig. 3.11c shows the randomly extracted E_A for 11 groups of defects during a set transition calculated by the Monte Carlo model.

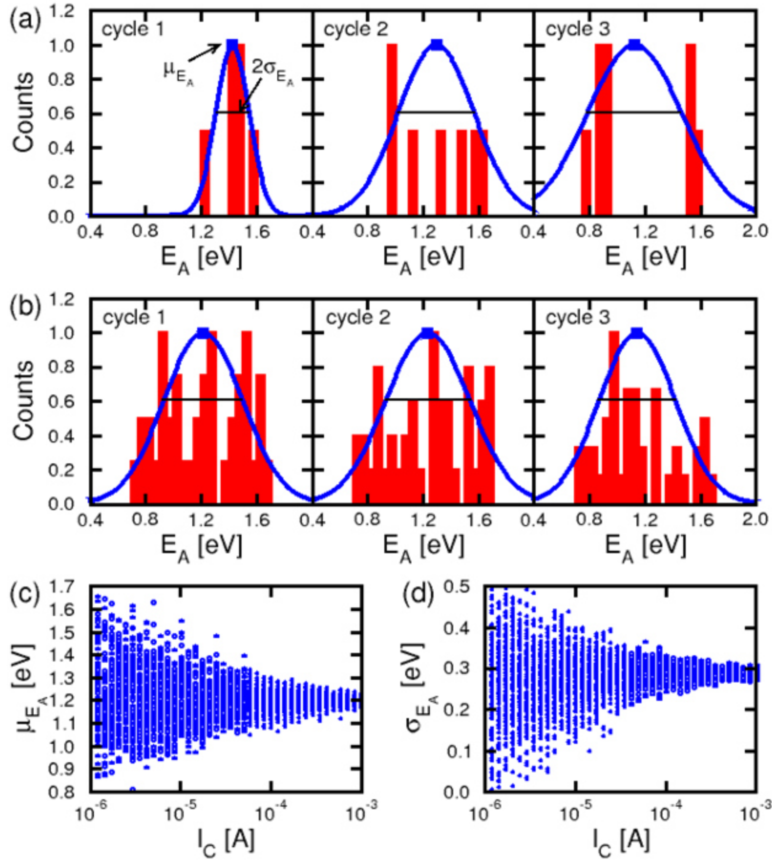

Figure 3.12: Distributions of E_A for three set/reset cycles and the corresponding gaussian fits obtained from the Monte Carlo model for I_C = 8μA (a) and 80μA (b). Both the average value μ_{E_A} and the standard deviation σ_{E_A} display more fluctuation from cycle to cycle in the case of I_C = 8μA, as summarized by μ_{E_A} (c) and σ_{E_A} (d) as a function of I_C.

Fig. 3.9 shows typical I-V characteristics (thin line), obtained by the Monte Carlo model for I_C = 8 μA (a) and I_C = 80 μA (b). Random migration events appear as step changes of resistance during both set and reset transitions. Most importantly, random defect migration induces cycle-to-cycle variations of switching parameters, such as R of the set and reset states, V_{set}, V_{reset} and I_{reset}. The switching variability is significantly higher for I_C = 8 μA as compared to I_C = 80 μA. The enhanced statistical fluctuation at decreasing I_C is explained in Fig. 3.12, showing the histograms of the extracted E_A during three complete I-V curves including set and reset transitions at I_C = 8 μA (a) and I_C = 80 μA (b). The gaussian fitting curve is also shown for each histogram: the average value μ_{E_A} and the standard deviation σ_{E_A} of the E_A distribution change from cycle to cycle for I_C = 8 μA in Fig. 3.12a, as a result of the small number of injection events. On the other hand, the Gaussian distributions are highly stable in terms of μ_{E_A} and σ_{E_A} for I_C = 80 μA in Fig. 3.12b, thanks to the large number of

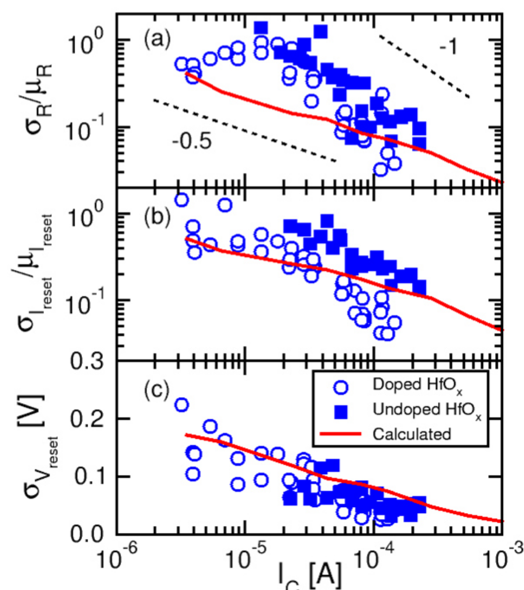

Figure 3.13: Relative spread of set state resistance σR/μR (a), relative spread of I$_{reset}$ (b) and standard deviation of V$_{reset}$ (c) as a function of I$_C$, from both data and calculations. Data were collected from a statistics of 50 cycles for a single 1T1R structure. Data for undoped HfO$_x$ RRAM samples from [66] and doped HfO$_x$ from [73] are reported for comparison.

defects involved in the set/reset transitions. To further highlight the dependence on I$_C$, Fig. 3.11 also shows μ_{E_A} (c) and σ_{E_A} (d) of individual I-V curves as a function of I$_C$. As I$_C$ increases, the distributions of both μ_{E_A} and σ_{E_A} become narrower, indicating the decrease of the cycle-to-cycle variations for increasing size of the CF. Clearly, the large fluctuation of E$_A$ at small I$_C$ clearly results in the enhanced switching variability in Fig. 3.9a.

To highlight the I$_C$-dependence of switching variability, Fig. 3.13a shows the relative spread of R for the set state as a function of I$_C$. The relative spread was evaluated for both data and calculations as the ratio between the standard deviation σ_R and the median value μ_R of the distribution of R over 50 cycles on the same device. Both data and calculations show a decrease of σ_R/μ_R for increasing I$_C$, due to the averaging effect of discrete ion migration in large CFs. Similar behaviors are found for the relative spread of the reset current $\mu_{I_{reset}}/\sigma_{I_{reset}}$ in Fig. 3.12b and for the standard deviation $\sigma_{V_{reset}}$ of the reset voltage in Fig. 3.12c. The calculated relative spread of the resistance in Fig. 3.12a shows a slope of -0.5, which is consistent with the Poisson statistics that controls the number of defects in the CF after set transition [66]. However, the experimental data show a larger slope of about -1, which can be interpreted by the additional contribution of random position of defects, as schematically shown in Fig. 3.14. In fact, our model only accounts for the variable number of injected defects as a result of the random E$_A$, while defect position within the gap region is not considered. Fig. 3.14 schematically shows a CF with only 4 defects A, B, C, D in the gap region.

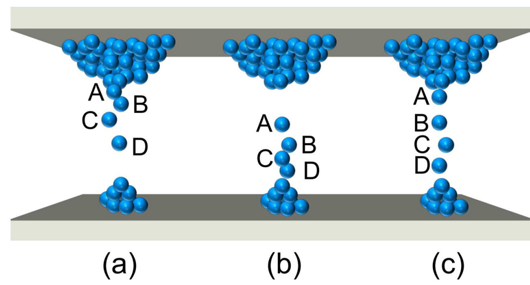

Figure 3.14: Schematic picture of the fluctuation of the defect position in small CF, possibly contributing to the I_C-dependent variability in Fig. (3.13). The CF is assumed to consist of only four defects A, B, C and D in the gap region. For instance, defects can be located at the top side of the gap (a), at the bottom side of the gap (b) or be uniformly distributed (c), thus impacting the measured resistance for the same nominal size of the CF.

The position of these defects is randomly changed from cycle to cycle, *e.g.*, the defects can be located at the top electrode side (a), at the bottom electrode side (b) or evenly distributed (c). Depending on the local defect arrangement, different band structures and transport properties are obtained, thus resulting in different values of the set state R. This additional variability source might account for the slope in Fig. 3.13a being higher than the theoretical value of 0.5.

Pulsed regime: variability and cycling failure

This Chapter is focused on switching in pulsed regime. Different aspects are investigated, such as the impact of pulse-amplitude and pulse-width on the switching, the variability and the endurance. An Arrhenius model capable of describe endurance and its dependence on pulse-amplitude and pulse-width is also described.

4.1 Pulsed characterization

In Chapter 2 and 3 we focused on set/reset operations and switching variability in DC conditions. In this Chapter we focus on the pulse regime, where the pulse-width is in the range from 100 ns up to 1 ms. The study start with a first pulse characterization, then we consider the switching variability and the failure mechanism. Finally we present an Arrhenius model capable of describe the dependence of endurance on pulse-width and pulse-amplitude.

For the pulsed regime we studied RRAM devices consisting of a TiN bottom electrode (BE), an amorphous $HfSiO_x$ switching layer and a Ti top electrode (TE) [77]. An on-chip integrated select transistor was used to limit the current during the set transition to a maximum compliance value I_C, as schematically shown in Fig. 4.1a. The setup for real-time monitoring of pulsed set/reset characteristics is reported in Fig. 4.1b: an arbitrary waveform generator applies a voltage pulse to the TE and to the gate of the transistor while an oscilloscope reads the voltage at the TE and the current flowing in the device [39]. Fig. 4.2a shows a typical waveform applied to the TE, consisting of a sequence of 4 triangular pulses, including (i) positive set, (ii) positive read, (iii) negative reset and (iv) negative read [78]. Positive and negative voltages were used for the read pulses after set and reset, respectively, to avoid possible disturb. A pulse-width t_P of 1 μs was used in the figure for all program/read pulses. A relatively low gate voltage V_G was used during set to control the compliance current I_C = 50 μA, while a high V_G was used during read and reset pulses to minimize the transistor resistance.

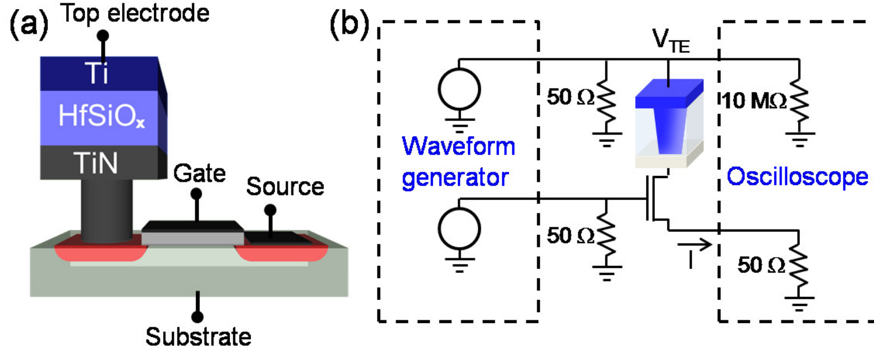

Figure 4.1: Schematic of the 1T1R cell (a) and of the experimental setup (b) used in this work. The RRAM stack includes a $HfSiO_x$ switching layer, a Ti cap layer and TiN BE.

From the voltage/current in Fig. 4.2a, it is possible to obtain the I-V curve in Fig. 4.2b, indicating a RW of about 10x between low-resistance state (LRS) and high-resistance state (HRS). The figure also shows the definition of the main parameters of the switching characteristics namely V_{set}, defined in correspondence of a current increase above 25 μA during the set transition, V_{reset}, defined in correspondence of the maximum current I_{reset} during the reset transition, and V_{stop}, namely the maximum negative voltage along the reset sweep.

Set and reset operations in Fig. 4.2 are controlled by I_C and V_{stop}, respectively. Limiting the current during the set transition allows to control the size of the conductive filament (CF) and the consequent I_{reset}, whereas the V_{stop} controls the HRS [79]. While I_C is kept as low as possible to limit the power consumption for high-density

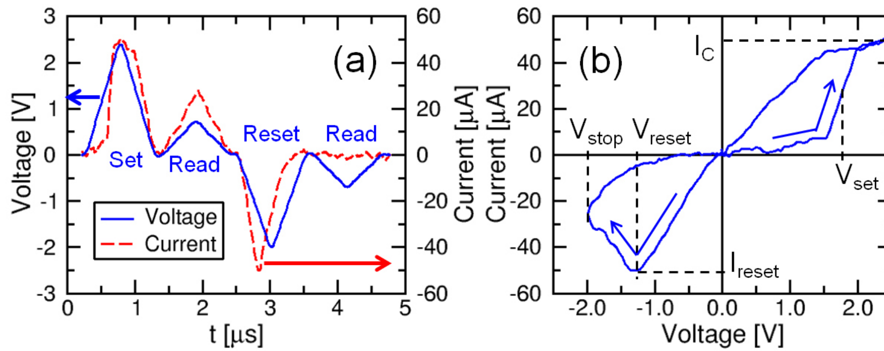

Figure 4.2: Measured TE voltage V and current I (a) and typical I-V characteristic (b) obtained from the measured V and I. Parameters are defined as follows: V_{set} is the set voltage marking the current crossing 25 μA, I_C = 50 μA is the compliance current, R_{LRS} is the resistance of the low resistance state (LRS), V_{reset} is the reset voltage marking the first decrease of R_{LRS}, I_{reset} is the corresponding reset current, R_{HRS} is the resistance of the high-resistance state (HRS).

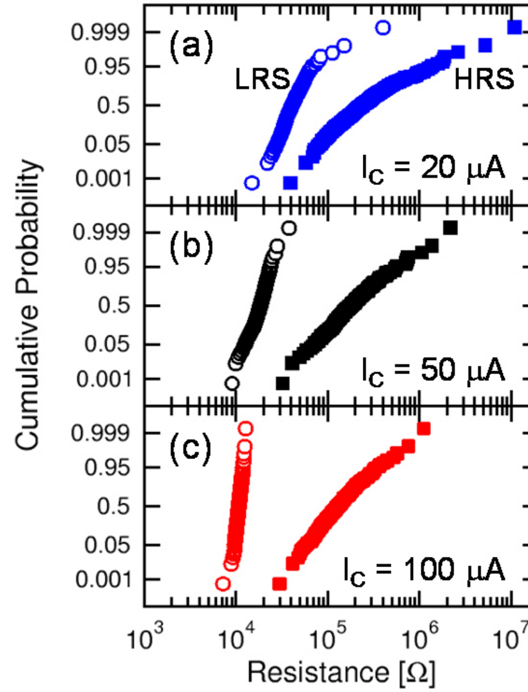

Figure 4.3: Distributions of the measured R for HRS (square) and LRS (circle) at I_C = 20μA (a), 50μA (a) and 100μA (c) for V_{stop} = 1.7 V and t_P = 1 μs.

applications, V_{stop} can be tuned to optimize RW, switching variability and endurance.

4.2 Cycle-to-cycle variability

Fig. 4.3 shows the cycle-to-cycle distributions of measured resistance R in the low-resistance state (LRS) and the high-resistance state (HRS) at increasing I_C = 20μA (a), 50μA (b) and 100μA (c). Distributions were obtained for one single cell operated at fixed stop voltage V_{stop} = 1.7 V with set/reset pulse-width t_P = 1μs. LRS distribution spread increases for decreasing I_C, while for the HRS the spread is almost independent on I_C, in agreement with the results for DC-type cycling discussed in the previous Chapter. The CF size increases with I_C, thus resulting in a decrease of LRS resistance and of its relative spread, which is mainly controlled by defect-number variation in the CF. The HRS behavior is similar to LRS, although with weaker dependence on I_C. The strong increase of σ_R/R for both HRS and LRS at small I_C is the origin of large program noise for low-current, low-power operation, undermining RRAM reliability.

To reduce the switching variations of HRS and LRS, we studied the impact of V_{stop} on cycle-cycle distributions. Fig. 4.4 shows the distributions of HRS (a) and LRS (b) at increasing V_{stop}. Constant I_C = 20μA and t_P = 1μs were used in the pulsed cycling, while V_{stop} was increased from 1.2 V to 1.9 V. Fig. 4.5 shows the median value (a)

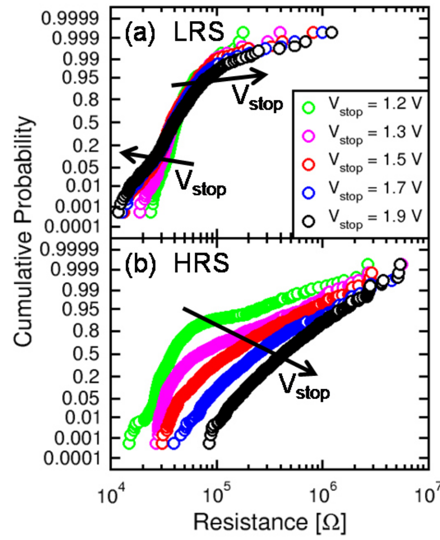

Figure 4.4: Distribution of LRS (a) and HRS (b) resistance for different V_{stop}. Increasing of V_{stop} results in a worsening of LRS tails and in a tightening of the HRS distributions.

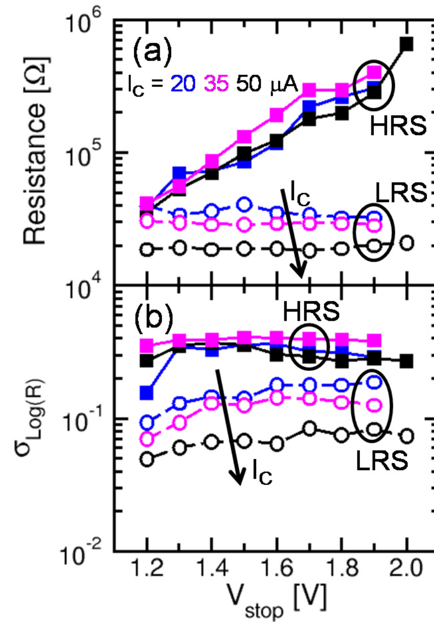

Figure 4.5: Median values (a) and standard deviation $\sigma_{Log_{10}(R)}$ (b) of resistance as a function of V_{stop} for different I_C.

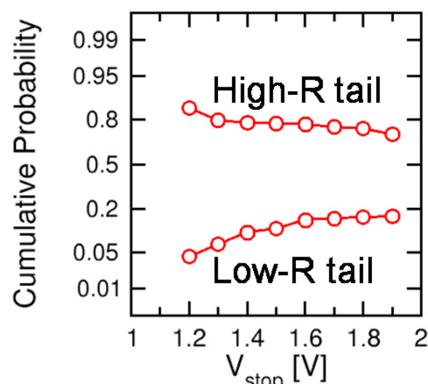

Figure 4.6: Percentile resistance tails defined as the variation of $\pm 25\%$ respect to the median value as function of V_{stop}.

and σLog$_{10}$(R) (b) for LRS and HRS as a function of V_{stop} at increasing I_C. Due to the deeper reset, HRS resistance increases and its distribution becomes tighter at increasing V_{stop}. These results indicate that a large V_{stop} plays a beneficial role for HRS distributions. On the other hand, LRS median value shows no dependence on V_{stop}, since the size of the CF is only dictated by I_C. The LRS distribution display tails at both low and high R in Fig. 4.4b, which increase their size at increasing V_{stop}. This causes an increase of $\sigma_{Log_{10}(R)}$ for LRS in Fig. 4.5b, particularly at small I_C.

To better understand the origin of LRS variability degradation at increasing V_{stop}, we evaluated the tail size as the percentile corresponding to $\pm 25\%$ change with respect to the median value in each distribution. Fig. 4.6 shows the tail percentile in LRS distributions at increasing V_{stop}, clearly indicating the increase of tails at both high and low resistance. The strongest amplitude and increase is shown by the low-R tail, which we attribute to the CF overgrowth due to the capacitive current overshoot at large V_{set}. This is described by the comparison of I-V curves in Fig. 4.7 for typical V_{set} (a) and for large V_{set} (b). In the latter case, a smaller LRS resistance is achieved after set transition, as a result of the larger current reached in the set transient caused by the parasitic capacitance C_P at the transistor drain in the 1T1R structure (Fig. 4.7c) [47]. This is further evidenced by the correlation between LRS resistance and V_{set} in Fig. 4.8, where R is constant at low V_{set}, then decreases at large V_{set} due to the increasing impact of C_P. Changing I_C results in change of the R plateau in Fig. 4.8, but not in the I_C-independent decaying-R region controlled by C_P. Simulation results with our analytical model [80] and assuming C_P = 50 fF are also shown, in good agreement with data. The increasing low-R tail in Fig. 4.6 is thus due to the deeper reset having statistically large V_{set}, causing increasing low-R tail due to the C_P overshoot.

We found that the high-R tail in Fig. 4.4b and 4.6 is due to incomplete set of deep HRS, which can be solved by increasing the voltage of the set pulse and/or increasing the set pulse width t_P. For instance, Fig. 4.9 shows measured LRS distributions at increasing t_P, where a large t_P is clearly seen to suppress high-R tails. From these results, the LRS variations can be reduced by suppressing high V_{set} and reducing C_P.

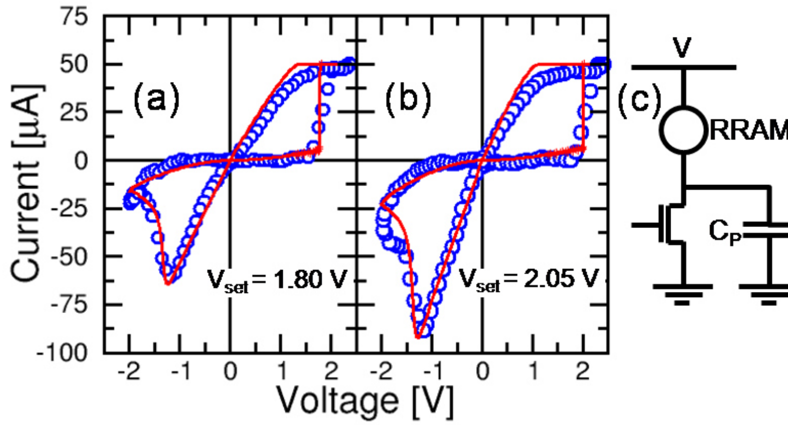

Figure 4.7: Measured and calculated I-V curves for typical set/reset (a) and deep reset (b), inducing set overshoot and filament overgrowth due to the parasitic capacitance C_P (c).

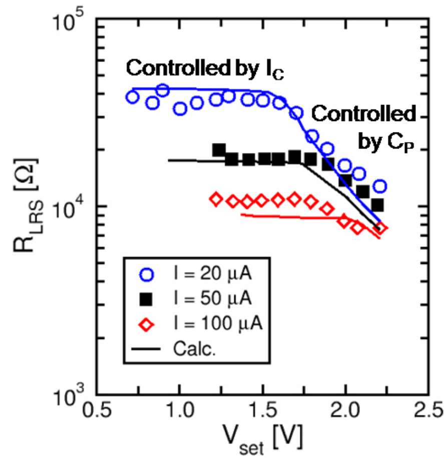

Figure 4.8: Measured and calculated LRS resistance as a function of V_{set} for different I_C.

4.3 Endurance failure

Cycling endurance was studied by monitoring the LRS and HRS as in Fig. 4.2 along several set/reset cycles. Fig. 4.10a shows R_{LRS} and R_{HRS} measured during a typical cycling experiment for V_{stop} = 1.9 V. Both R_{LRS} and R_{HRS} slightly decrease with cycling keeping a constant RW, then collapses around N_C = 1.7x10^5 cycles due to an increase of the R_{LRS} and a decrease of the R_{HRS}. The collapse of the RW is highlighted in Fig. 4.10b, showing a gradual decrease of RW across about 50 cycles. Note that failure mode differs from the usual high-resistance (open) or low resistance (short) failure modes which were previously reported [81,82]. Fig. 4.10a clearly shows

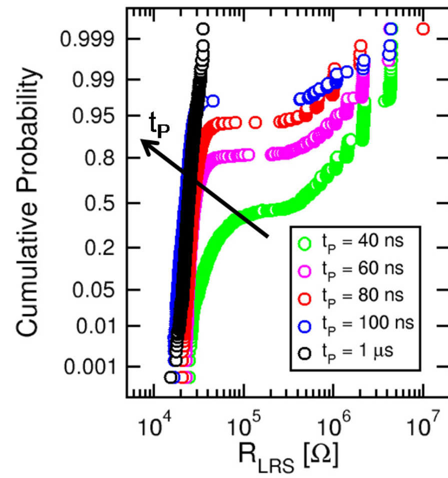

Figure 4.9: LRS resistance distributions for different t_P. Increasing of t_P results in a tightened distribution with a smaller high-R tail.

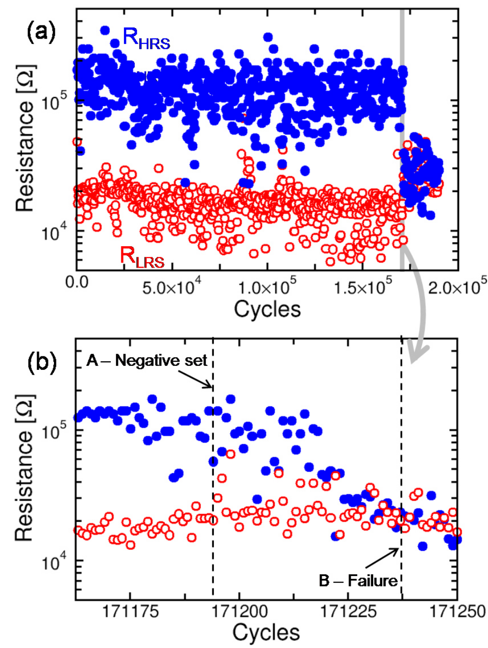

Figure 4.10: Measured R as a function of the number of cycles (a) and highlighted region in correspondence of failure around $1.7\text{x}10^5$ (b). Two characteristic cycles are marked, corresponding to the negative-set event (A) and final failure due to RW collapse (B).

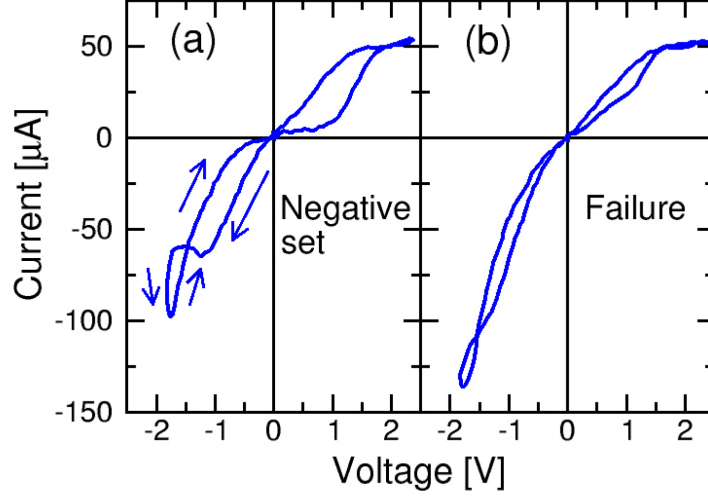

Figure 4.11: Measured I-V curves corresponding to the marked locations in Fig. 4.10, namely negative-set event (a) and failure (b). Negative set causes an excess current of about $2I_C$, initiating filament overgrowth which finally leads to the NS state with no RW in (b).

that the final state after the failure is neither HRS nor LRS but an intermediate state, with a resistance of about 30 kΩ.

We found that failure is always triggered by a negative set event as shown in Fig. 4.11a: reporting the I-V curve collected in correspondence of cycle A in Fig. 4.10b. After a typical positive set operation, the application of the negative pulse, causes a reset transition followed by an anomalous increase of the current. During the reset pulse the transistor gate is biased with a high voltage, to minimize the series resistance, therefore the unlimited current can freely rise to a high value, e.g., about $2I_C$ in Fig. 4.11a. We believe that the negative set transition consists of an injection of defects from the BE toward the TE , where the resulting filament largely overgrows due to the lack of a current compliance. As a result, R_{HRS} decreases due to the larger cross section of the depleted gap in the CF. The leaky HRS also inhibits the set operation: in fact, due to the relatively low R_{HRS}, there is no sufficient voltage drop across the RRAM to reach V_{set} and induce set transition. Fig. 4.11b shows the I-V curve corresponding to cycle B in Fig. 4.10b, after failure induced by the negative set transition. The I-V curve clearly shows no hysteresis, as a result of the lack of set transition in the leaky HRS. The state resulting from negative set will be therefore referred to as non-switching (NS) state in the following.

4.3.1 Endurance dependence on V_{stop}

Cycling endurance was studied for different pulse amplitude V_{stop}. Fig. 4.12 shows the endurance N_C as a function of V_{stop} for t_P = 1 μs, showing a maximum N_{fail} around V_{stop} = 1.7 V. Different failure modes are also indicated: NS state due to negative set is the main failure mode at high V_{stop}, while no-reset (NR) mode dominates at low

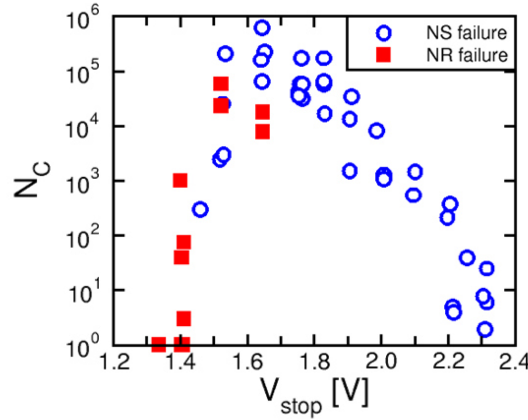

Figure 4.12: Measured number of cycles before failure N_C as a function of V_{stop} for t_P = 1 μs. Failure occurs by NS mode at high V_{stop}, while at low V_{stop} the device cannot reset properly.

V_{stop}, where the voltage is insufficient to induce reset. For V_{stop} larger than 1.7 V, the endurance decreases due to an acceleration of the degradation with V_{stop}. As shown in Fig. 4.11, the failure is due to a negative set and the probability of negative set increases with V_{stop}. For V_{stop} decreasing below 1.7 V, the voltage is not enough to induce a reset transition, therefore the N_C sharply collapse to zero. This is shown by the measured R_{LRS} and R_{HRS} in Fig. 4.13 for a low V_{stop} = 1.4 V: while R_{LRS} is almost constant, R_{HRS} fluctuates because of random failure of the reset transition Fig. 4.13a. This is explained in Fig. 4.13 b and c showing I-V curves with normal (b) and NR behavior (c). Note that in this range of voltage (V_{stop} < 1.7 V), the failure is due to the insufficient voltage to reset the device, thus should not be viewed as a true failure event. These results show that, although beneficial for RW and variability, the use of a large V_{stop} might be a concern from the viewpoint of endurance failure.

4.3.2 Endurance dependence on t_P

We studied the dependence of cycling endurance on pulse width t_P in the range from 100 ns to 1 ms. Fig. 4.14 shows the I-V curves for $t_P = 100$ ns (a) and 1 ms (b) at V_{stop} = 1.7 V. The figure also shows calculations by our analytical model [80]. In Fig. 4.14 is reported also the summary of measured and calculated switching parameters, namely V_{set}, V_{reset} (c), R_{LRS} and R_{HRS} (d) for V_{stop} = 1.7 V. Fig. 4.14c clearly shows the voltage-accelerated nature of the switching where both set and reset voltages decrease with t_P since less voltage is needed to trigger the set/reset transition at increasing time [83].

Fig. 4.15 shows the measured N_C as a function of V_{stop} for increasing t_P. As the pulse-width increases, the N_C curve shifts to lower V_{stop} following to the behavior of V_{reset} in Fig. 4.14a. Strikingly, however, the maximum $N_C \approx 4\text{x}10^5$ does not change with t_P.

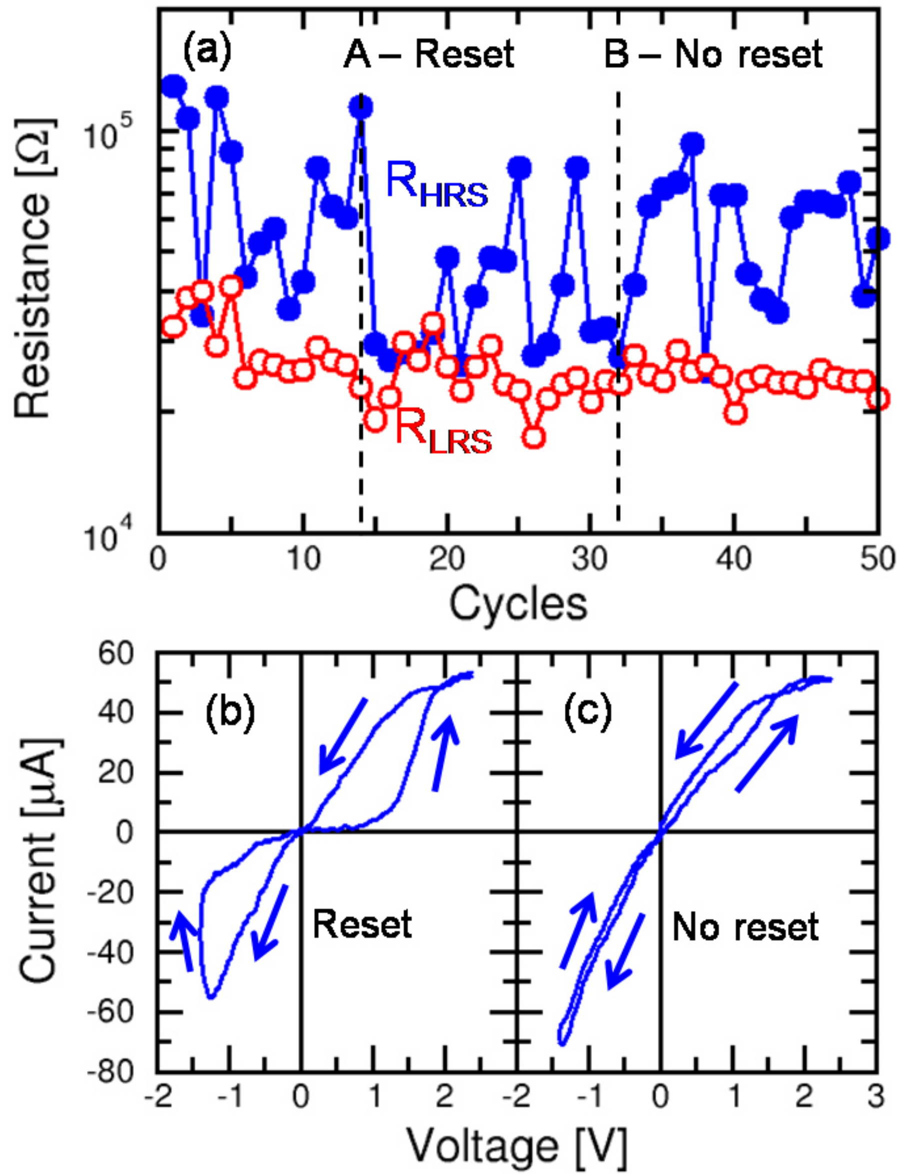

Figure 4.13: Measured R as a function of cycles for low V_{stop} = 1.4 V (a) and measured I-V curves corresponding to successful reset (b) and no reset due to insufficient V_{stop} (c) as marked in (a). The noisy RW indicates NR failure due to insufficient V_{stop}.

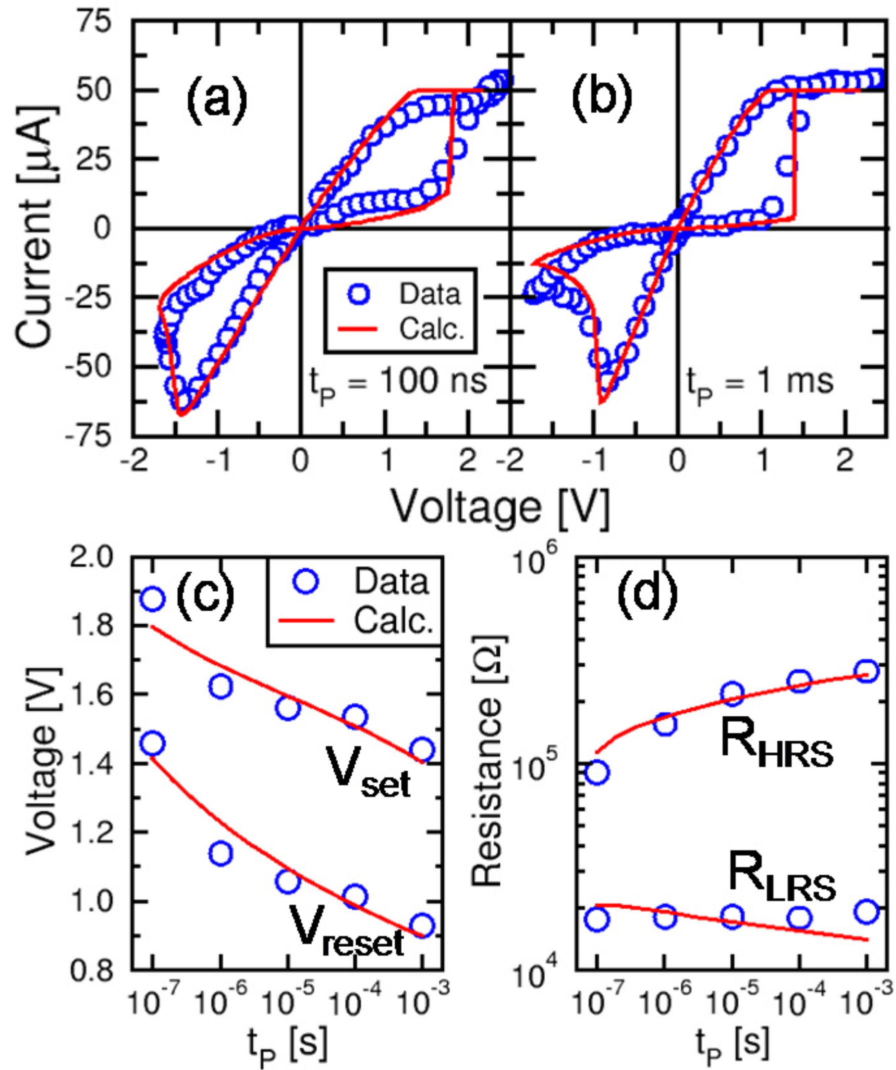

Figure 4.14: Measured and calculated I-V curves for t_P = 100 ns (a) and 1 ms (b). Measured and calculated V_{set}, V_{reset} (c), R_{HRS} and R_{LRS} (d) as a function of t_P. Note the decrease of set/reset voltages at increasing t_P, due to the voltage-accelerated nature of switching.

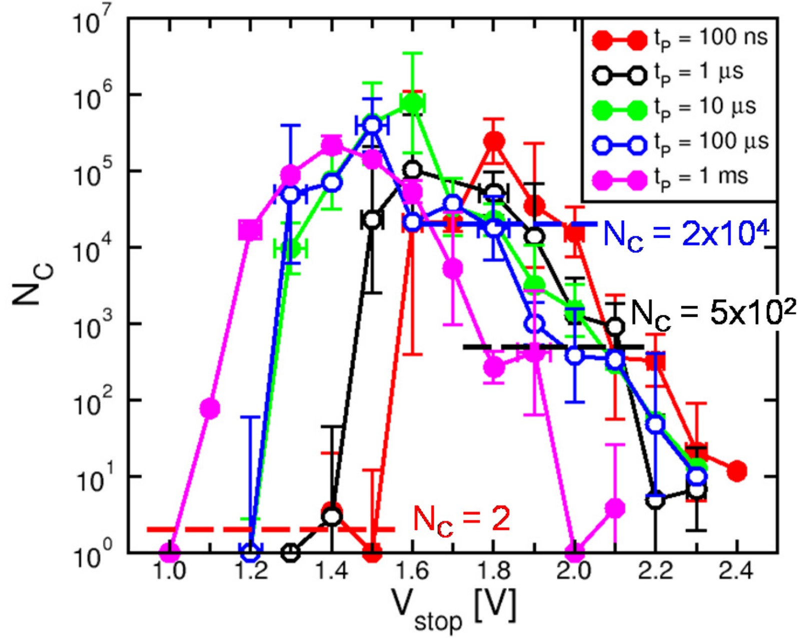

Figure 4.15: Measured N_C as a function of V_{stop} for increasing t_P. The curves shift to lower V_{stop} at increasing t_P, in agreement with the t_P-dependence of switching voltages in Fig. 4.14c.

4.3.3 Endurance model

To understand the V-acceleration law of endurance, we extracted V_{stop} at constant N_C in Fig. 4.15 for the rising-N_C side (N_C = 2) and the decaying-N_C side (N_C = 5x10^2 and N_C = 2x10^4). The extracted V_{stop} is shown in Fig. 4.16a as a function of t_P: the 2 different acceleration slopes for the rising and decaying regions can be understood by different mechanisms controlling N_C, namely incomplete reset at small V_{stop} and negative set at large V_{stop}. The 2 processes are reproduced by a Joule-heating model with activation energies E_A = 1.2 eV (same as reset process [76]) and 2.7 eV, respectively. The larger barrier of the negative set process can be understood by the harder defect injection from the TiN BE, featuring no oxygen-exchange layer. To further confirm the T-accelerated law of negative-set failure, we calculated the degradation function f = $\int e^{-\frac{E_A}{kT}} dt$, where T is the local temperature at the CF controlled by V(t) through the Joule heating formula : T = $T_0 + \frac{V_{stop}^2}{8\rho k_{th}} = T_0 + \alpha V_{stop}^2$. Two different values of α were used, namely α = 434 K/V^2 for N_C = 2, which corresponds to a formed CF representing the set state, and α = 52 K/V^2 for N_C = 5x10^2 and 2x10^4, representing the reset state. The degradation function accounts for the increasing device degradation due to cycling. Plotting N_C as a function of f in Fig. 4.16b shows a universal behavior for all t_P, thus supporting the Arrhenius-acceleration of failure with E_A = 2.7 eV. This means that the failure is controlled by the degradation, and the degradation depends on both V_{stop} and t_P. Fig. 4.16c shows the computed N_C using the Arrhenius acceleration

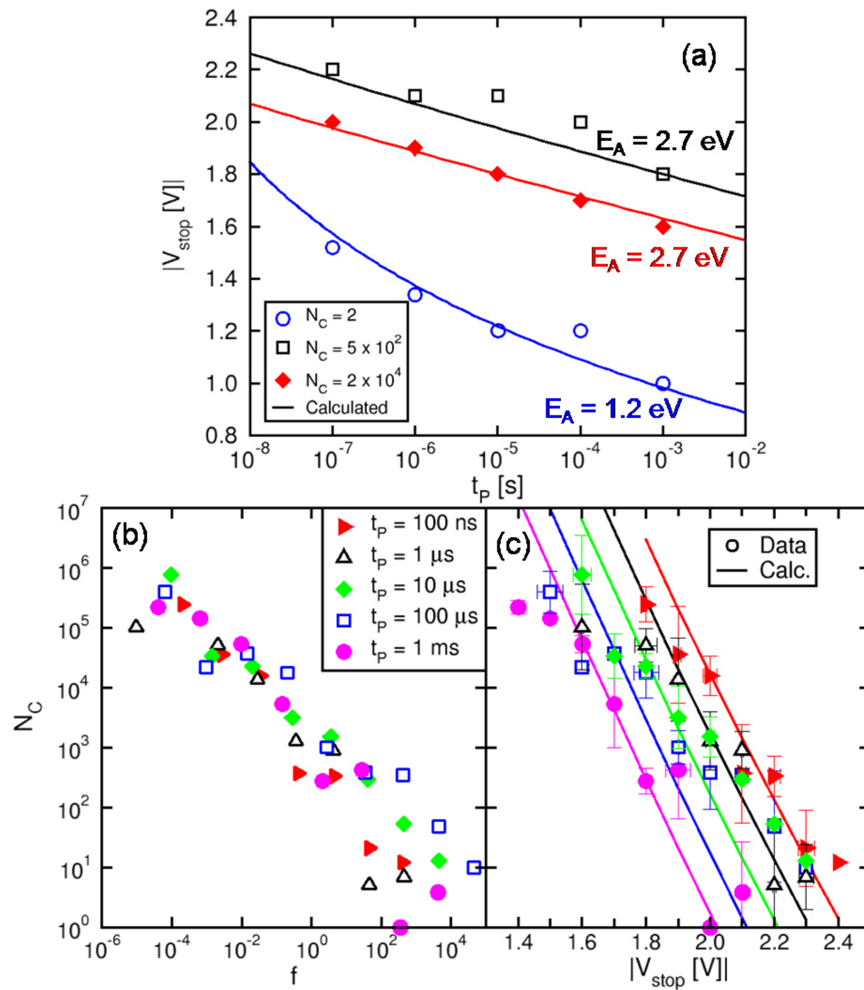

Figure 4.16: Extracted V_{stop} from Fig. 4.15 as a function of t_P (a), measured N_C as a function of the degradation function f shows an universal behavior for all t_P (b) and measured and calculated N_C as a function of V_{stop} (c). Two different E_A in (a) point out two different failure mechanisms at small and large V_{stop}, respectively no reset and negative set. Calculations display a good agreement with data for relatively large V_{stop} where endurance is limited by negative set.

function: calculations agree with data in the negative set region, thus further supporting the Arrhenius-based endurance model [84].

Random telegraph noise in RRAM

This chapter is dedicated to the study of the random telegraph noise (RTN). The two levels current fluctuations affect set and reset states of RRAM and causes a worsening of the resistance distributions. The chapter presents a detailed electrical characterization of the phenomena, performed as a function of the bias voltage, the operating temperature and the programming current and a physics-based model.

5.1 RTN characterization

High-density application requires operation at low current below 10 μA, where the cell might be affected by program variability [69, 72, 85] and random telegraph noise (RTN) [63, 72, 76, 86–92]. While program variability might be controlled by proper program/verify procedures, read current fluctuations due to low-frequency noise can hardly be avoided. Therefore, a comprehensive characterization of the dependence of RTN on program/read parameters (voltage, current, temperature) and a detailed understanding of RTN physics is essential.

We carried out experiments on bipolar RRAM devices based on doped HfO_X as active switching layer. The device stack consist of the usual TiN/$HfSiO_X$/Ti described in Chapter 2 [40]. Fig. 5.1 shows typical I-V curves showing set and reset transitions at positive and negative voltage, respectively. The compliance current I_C, namely the maximum current in the set operation, was changed from $I_C = 70$ μA (a) to 3.5 μA (b), allowing the control of the set-state resistance R = V_C/I_C, with $V_C \approx 0.4$ V, and the reset current $I_{reset} \approx I_C$ [51]. As shown in Fig. 5.1b, the set state obtained with a low I_C might feature RTN, namely a 2-level current fluctuation [93]. This noise can affect the read current and consequently the read distribution in the cell array.

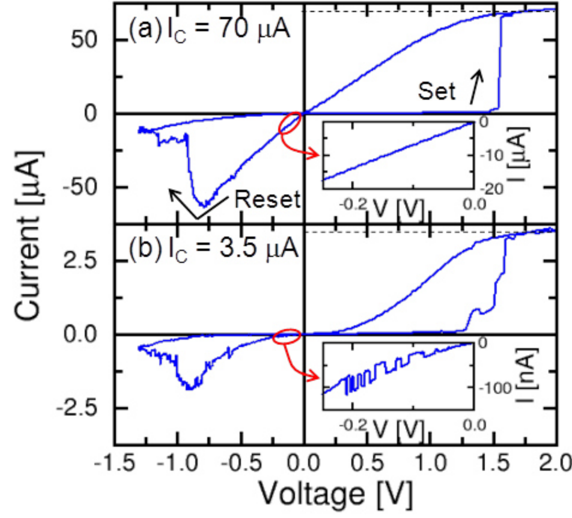

Figure 5.1: Measured I-V curves for $I_C = 70\ \mu$A (a) and $I_C = 3.5\ \mu$A (b). The insets is a magnification of the I-V curve at low field, indicating RTN fluctuations at low I_C.

5.2 Numerical model of RTN

RTN is due to a metastable defect close to the CF boundary, fluctuating between two charged states, e.g., neutral (0) and negative (-) state, as schematically reported in Fig. 5.2a [63, 92, 94]. While the neutral state does not affect the conduction in the CF, the negative charge causes carrier depletion in the CF and a consequent R increases from R_{on} to R_{off} [63]. To understand the properties of RTN at low I_C, we developed a physics-based model by solving semiconductor transport equations in the CF [94].

5.2.1 Transport and kinetic model

The potential φ was calculated through the Poisson equation,

$$\vec{\nabla} \cdot (-\epsilon \vec{\nabla} \varphi) = q[N_D - n + \chi(x, y, z)], \tag{5.8}$$

where N_D is the concentration of dopant atoms, assumed totally ionized, n is the electron density and χ(x, y, z) describes the fixed charge. The drift-diffusion current density was calculated by:

$$\vec{J} = qn\mu_n \vec{F} + kT\mu_n \vec{\nabla} n, \tag{5.9}$$

where μ_n is the electron mobility and $\vec{F}$ is the electric field. Drift-diffusion current continuity was described by:

$$\vec{\nabla} \cdot \vec{J} = 0, \tag{5.10}$$

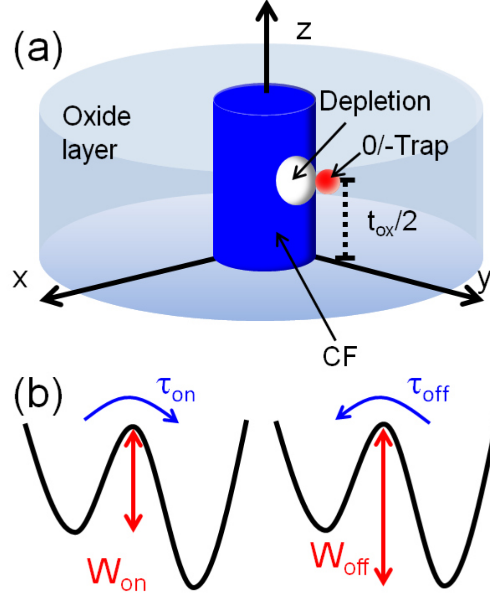

Figure 5.2: Sketch of the RTN model. Fluctuations of a bistable defect close to CF cause RTN (a). When the defect is negatively charged, the CF is depleted from carriers within approximately a Debye length. Energy diagram for bistable defect switching (b). The transition from low to high resistance requires thermal excitation over a barrier W_{on} in an average time τ_{on}, while the transition from high to low resistance requires excitation over a barrier W_{off} in an average time τ_{off}.

and, finally, the electric field $\vec{F}$ was linked to the electrostatic potential φ through the equation:

$$\vec{F} = -\vec{\nabla}\varphi. \tag{5.11}$$

An n-doped CF was assumed since O-vacancies generate localized states close to the conduction band in HfO_2 [95]. The Fourier equation was solved in the model to account for localized Joule heating. Defect switching kinetics was described by thermally-activated time constants

$$\tau_{on} = \tau_0 e^{\frac{W_{on}}{kT}}, \tag{5.12}$$

$$\tau_{off} = \tau_0 e^{\frac{W_{off}}{kT}}, \tag{5.13}$$

respectively for on $\rightarrow$ off and off $\rightarrow$ on transitions, as shown in Fig. 5.2b. The fluctuation amplitude was evaluated considering the depletion from free electrons of the CF: when a defect is negatively charged the CF is depleted approximately within a Debye length λ_D [63] given by:

$$\lambda_D = \sqrt{\frac{\varepsilon kT}{q^2 n}} \tag{5.14}$$

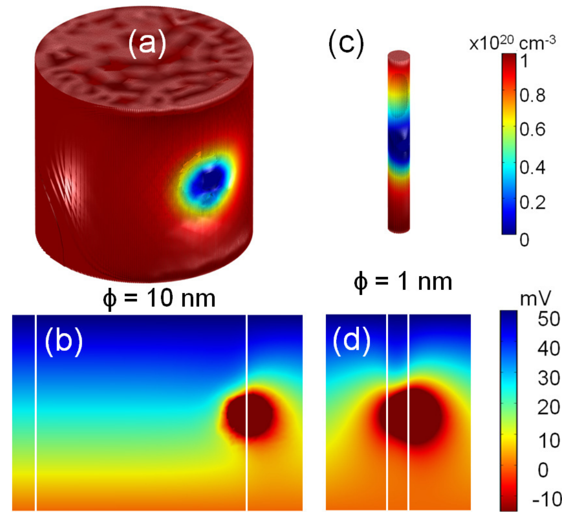

Figure 5.3: Simulation results of the RTN model indicating the map of calculated electron density for a CF with $\phi = 10$ nm (a) and the corresponding electrostatic potential profile (b). Calculations were carried out assuming a negatively charged defect at the CF surface in correspondence of $t_{ox}/2$. The negative defect causes depletion of carrier concentration (a) and a local potential decrease (b). Similarly for $\phi = 1$ nm the map of calculated electron density (c) and the corresponding electrostatic potential profile (d). Electrons depletion can be partial (a) or full (c) depending on the CF size.

where ϵ is the CF permittivity, k is the Boltzmann constant, T is the temperature, n is the carrier density in the CF and q is the electron charge.

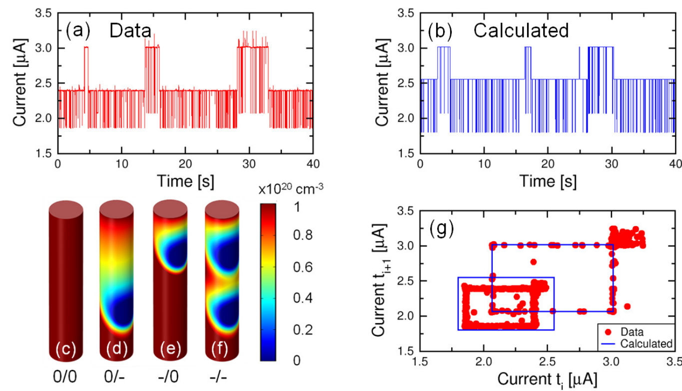

Figure 5.4: Measured (a) and calculated (b) four levels RTN. The four levels can be attribute to two defects that can be both neutral (c), one negative (d-e) or both negative (f). Two different squares appear in the read current correlation plot as result of four levels RTN (g).

5.2.2 Simulation results

To quantitatively describe RTN the model was implemented through the finite-element method (FEM) using COMSOL. Fig. 5.3a shows the calculated electron density n within a cylindrical CF with diameter $\phi = 10$ nm and doping density $N_D = 10^{20}$ cm^{-3}. A negatively-charged trap was assumed at the CF surface, leading to a local depletion within a characteristic range close to the Debye length $\lambda_D = 1.2$ nm [63]. Fig. 5.3b shows the calculated profile of the electrostatic potential during read at $V_{read} = 50$ mV, showing a potential dip in correspondence of the negative charge. The carrier depletion is limited to the surface region, therefore negligibly affecting the measured R. Fig. 5.3c and d show similar calculations for a smaller CF with ϕ = 1 nm, obtained with a lower I_C. Carriers are fully depleted close to the charged defect, since ϕ is comparable to λ_D [63].

The model allows to calculate dynamic RTN switching under various trap configuration, CF size and voltage/temperature conditions. For instance, Fig. 5.4a shows RTN data with 4 discrete resistance levels, which can be attributed to two independently-fluctuating defects along the CF [91]. Fig. 5.4b shows the calculated R over time, assuming two RTN defects as shown in the calculated carrier map of Fig. 5.4c-f. The two trap configurations are indicated, namely 0/0 (c), 0/- (d), -/0 (e) and -/- (f). These states correspond to the four RTN levels from the highest current (state 0/0) to the lowest current (state -/-). Fig. 5.4 shows the correlation plot of read current I_{n+1} at time t_{n+1} as a function of the current I_n measured at the previous read time t_n [91,96]. Two squares appear in the correlation plot, consistently with the two traps contributing to RTN [96]. The square areas are different since δI_0, namely the current change between states 0/0 and -/0, is larger than δI_-, namely the current change between states 0/- and -/-. This is because the depletion regions induced by the two negative defects overlap in Fig. 5.4f, thus resulting in non-additive depletion effects.

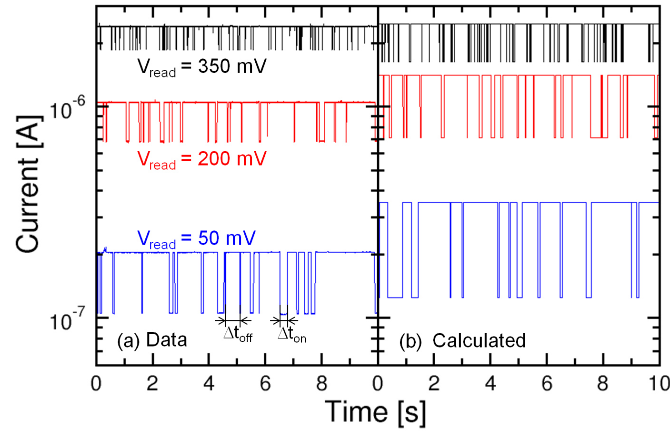

Figure 5.5: Measured (a) and calculated (b) RTN traces for the same state at increasing read bias $V_{read} =$ 50 mV, 200 mV and 350 mV. The RTN switching times Δt_{on} and Δt_{off} decrease with V_{read}.

5.3 Voltage-dependent RTN

A close inspection of the I-V curve in Fig. 5.1b reveals that the RTN switching kinetics increases at higher voltage while the ΔR, namely the difference between the resistance values in correspondence of the two RTN levels, decreases at higher voltage. To understand the dependence on applied voltage we measured the same RTN for increasing bias $V_{read} = 50$ mV, 200 mV and 350 mV.

5.3.1 Impact on switching rates

Fig. 5.5 confirms that the switching time decreases for increasing applied V_{read}, revealing a voltage-dependent RTN kinetics.

This can be understood by the localized Joule heating in the CF, where the applied voltage causes a parabolic temperature profile along the filament, with maximum temperature given by:

$$T_{max} = T_0 + \frac{R_{th}}{R} V^2 \tag{5.15}$$

where T_0 is the ambient temperature, R_{th} is the equivalent thermal resistance of the CF and R is the electrical resistance [94].

To confirm this voltage-dependent RTN, Fig. 5.5b shows the calculated resistance as function of time for $V_{read} = 50$, 200 and 350 mV. The simulation shows that the RTN switching frequency increases for increasing bias voltage. In the model, energy barriers $W_{on} = 0.71$ eV and $W_{off} = 0.88$ eV were used for the RTN defect, which was assumed to be located at $t_{ox}/2$ from the electrode (see Fig 5.5a).

Fig. 5.6 shows the simulated temperature maps for V_{read} = 50 mV (a), 200 mV (b) and 350 mV (c) while Fig. 5.6d reports the maximum temperature along the CF and the temperature of the trap as function of V_{read}. The defect is assumed to be localized at $t_{ox}/2$ from both electrodes and at 0.5 nm from the CF surface (see Fig. 5.6). For V_{read} = 50 mV the Joule heating effect is negligible therefore the temperature is almost equal to the ambient temperature T_0 = 303 K. Increasing the bias the Joule heating increases, the temperature of the filament increases up to 352 K at 400 mV while the the trap temperature reaches 325 K. From Fig. 5.6b and 5.6c it is clear that the impact of the Joule heating on the RTN kinetics depends also on the distance between the CF and the trap.

To better understand the switching kinetics and the impact of applied voltage we defined Δt_{on} and Δt_{off} as the times for which the current stays high and low, respectively, (see Fig 5.6). Fig. 5.7 shows the distribution of Δt_{on} and Δt_{off} for $V_{read} =$ 50 (a), 200 (b) and 350 mV (c). The exponential distributions reveal fully uncorrelated switching events, the characteristic slope providing the time constants τ_{on} and τ_{off}, that is the average value for the exponential distribution. The agreement between calculations and data strongly supports the Joule heating model for the voltage-dependent RTN.

Further support to the Joule heating model for RTN comes from a temperature variable experiments, where the same device was measured with different V_{read} at variable ambient temperature, from $T_0 = 30°$C to $T_0 = 70°$C. The device was initially set at a compliance current I_C = 5 μA and was characterized by a RTN with a relatively large amplitude. Fig. 5.8, showing RTN measured (a) and calculated (b) at $V_{read} = 10$

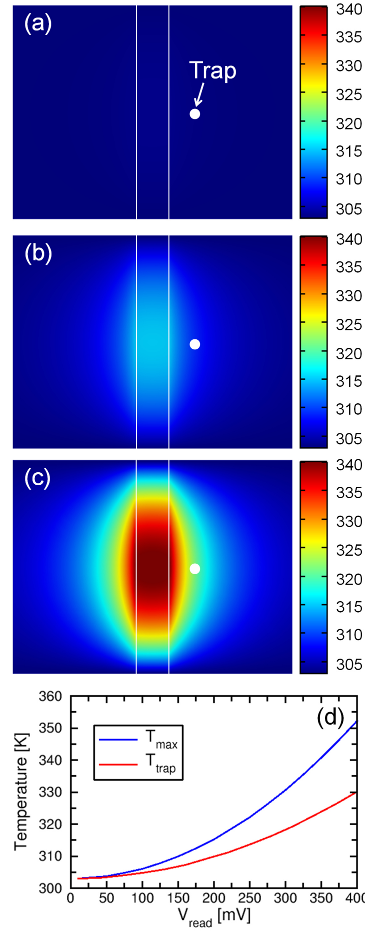

Figure 5.6: Simulated CF temperature for increasing bias, V_{read} = 50 mV (a), 200 mV (b) and 350 mV (c). The maximum temperature increases from 303 K up to 352 K in the CF at V_{read} = 400 mV while the temperature of the trap achieves 325 K (d). The trap is assumed to be located at $t_{ox}/2$ and far 0.5 nm from the CF surface.

mV for increasing temperature $T_0 = 30$, 50 and 70°C. Comparing traces at different temperature it is clear that RTN switching times decrease for increasing temperature, thus supporting the temperature activation model of Fig. 5.2b.

To better understand the impact of temperature and bias on switching kinetics we considered the time constants τ_{on} and τ_{off} for the different conditions. Fig. 5.9 shows measured and calculated τ_{on} (a) and τ_{off} (b) as a function of V_{read}, for increasing T_0 from 30°C to 70°C. For a fixed temperature the switching times decreasing with V_{read} while for a fixed V_{read} the switching times decreasing with temperature. These behaviors can be explained by the equations 5.12 and 5.13, where switching kinetics is controlled by local temperature that increase with Joule heating effect and the ambient temperature. Calculations by the numerical model are shown on the same figures,

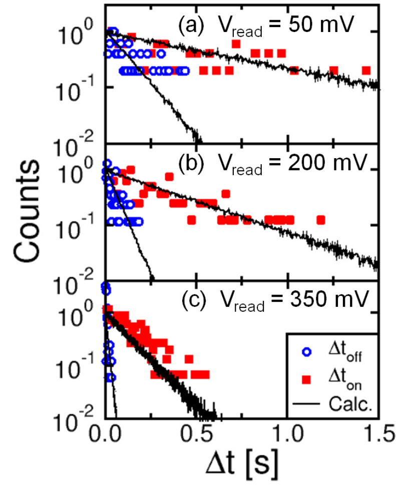

Figure 5.7: Distributions of measured and calculated Δt_{on} and Δt_{off} for $V_{read} = 50$ (a), 200 (b) and 350 mV (c). Both Δt_{on} and Δt_{off} show an exponential shape which is consistent with the random switching in RTN and the slopes of the distribution are the average values for transition times τ_{on} and τ_{off}.

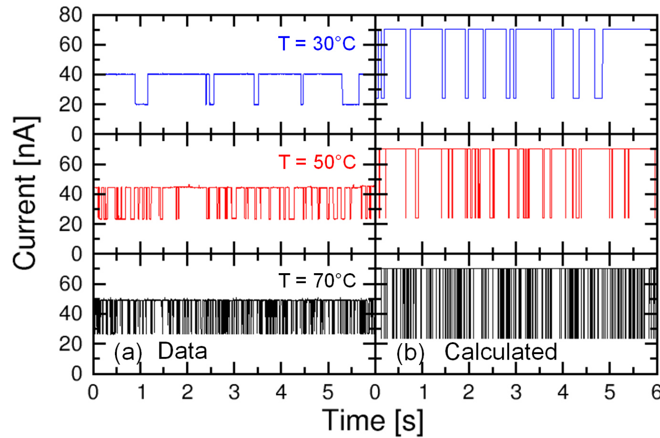

Figure 5.8: Measured (a) and calculated (b) RTN traces for the same state at $V_{read} = 10$ mV for increasing ambient temperature $T_0 = 30°C$ (a), 50°C (b) and 70°C (c).

demonstrating a good agreement with data.

5.3.2 Impact on ΔR

Fig. 5.1b also shows that the resistance change ΔR decreases for increasing V_{read}. This is particularly evident for relatively small I_C, as shown by the measured R as a function of V_{read} for I_C = 6 μA in Fig. 5.10a. Note the symmetric and non-linear

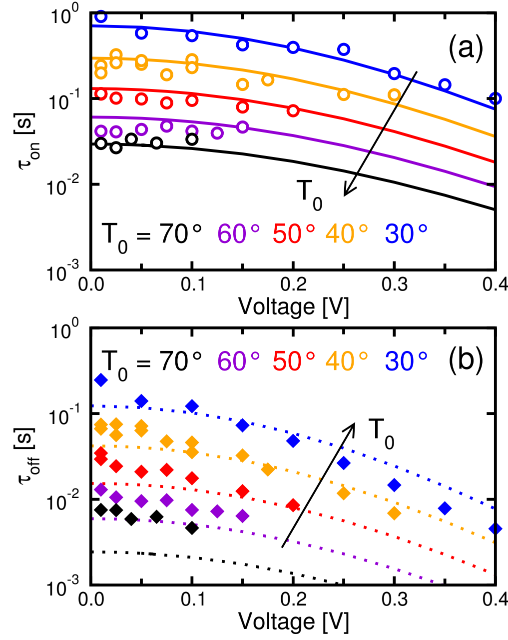

Figure 5.9: Calculated τ_{on} (a) and τ_{off} (b) for increasing ambient temperature from $T_0 = 30°C$ to $T_0 = 70°C$. The model for T-accelerated RTN and Joule heating can reproduce the observed V-dependence of switching times.

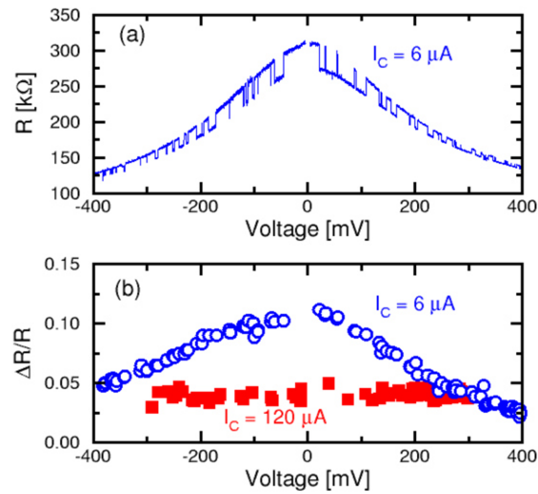

Figure 5.10: Measured R for I_C = 6 μA (a) and ΔR/R for I_C = 6 μA and I_C = 120 μA (b) as a function of V_{read}. The decrease of R and of ΔR/R with V_{read} for I_C = 6 μA is consistent with PF conduction and its response to a fluctuating charge as shown in Fig. 5.11. The relative resistance change δR/R remains constant for I_C = 120 μA due to metallic transport in large CFs.

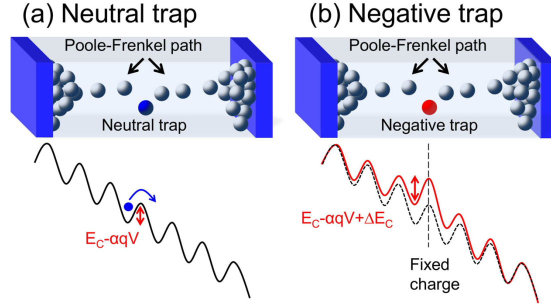

Figure 5.11: Schematic illustration of the PF transport in a few-defect CF. For a neutral defect, R is controlled by an energy barrier E_C (b), while the transition to a negative charge causes an increase of energy barrier by ΔE_C.

behavior of R, which is consistent with PF transport in the CF. Also, the switching rates display the same dependence for positive and negative V_{read}, since T only depends on the absolute value of V_{read}. Fig. 5.10b shows the corresponding ΔR/R for I_C = 6 μA (from Fig. 5.10a) and I_C = 120 μA. Data at I_C = 6 μA clearly show a decrease of ΔR/R with V_{read}, while ΔR/R negligibly depends on V_{read} for I_C = 120 μA. This behavior can be understood by the different conduction regimes taking place in small and large CFs. A small CF can consist of only few defects, acting as localized states for PF hopping of electrons, while a large CF contains many more defects resulting in a doped-semiconductor behavior or even a metallic-like conduction for extremely large defect concentration, *e.g.*, $N_D = 10^{21}$ cm^{-3}. Fig. 5.11 schematically shows the PF conduction picture and the impact of a RTN switching defect close to the CF. When the RTN defect is in the neutral state (Fig. 5.11a), electrons migrate in response to the applied voltage V_{read}, and the CF resistance can be written as:

$$R = R_0 e^{\frac{E_C - \alpha q V}{kT}} \tag{5.16}$$

where R_0 is a pre-exponential factor, α is the barrier lowering coefficient and E_C is the characteristic energy barrier for electron hopping [97]. For a negatively-charged defect (Fig. 5.11b), the defect potential influences the electrostatic potential in the CF, thus enhancing the hopping barrier by an additional contribution ΔE_C. Therefore, the resistance increases according to:

$$R = R_0 e^{\frac{E_C + \Delta E_C - \alpha q V}{kT}} \tag{5.17}$$

From Eqs. (5.16) and (5.17), the ratio ΔR/R reads:

$$\frac{\Delta R}{R} = \frac{R' - R}{R} = e^{\frac{\Delta E_C}{kT}} - 1 \tag{5.18}$$

where an increase of T, due to a larger Vread, leads to a decrease of ΔR/R. Fig. 5.12 shows the 1 + ΔR/R from Fig. 5.11b for both I_C = 6 μA and I_C = 120 μA [97].

Data at small I_C in Fig. 5.12 display an Arrhenius behavior with slope ΔE_C = 4.1 meV for V_{read} < 0 and 5.6 meV for V_{read} > 0, which is consistent with Eq. (5.18).

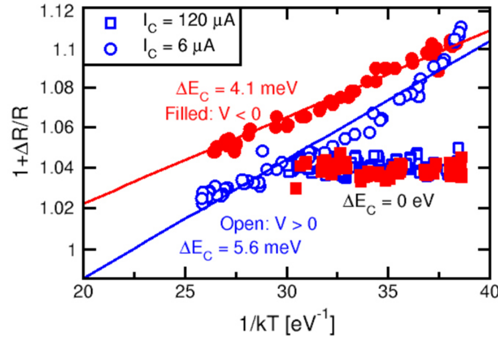

Figure 5.12: Arrhenius plot of 1+ΔR/R for I_C = 6 μA and I_C = 120 μA, for both positive and negative V_{read}. The defect temperature was estimated from Eq. (5.15). The straight line for I_C = 6 μA is in agreement with the PF model of Eq. (11), while the constant ΔR/R for I_C = 120 μA can be explained by metallic conduction in the CF.

The polarity-dependent ΔE_C might be due to different position of the energy maximum between two localized state with respect to the RTN defect for positive and negative V_{read}. For I_C = 120 μA, ΔR/R is almost constant, which can be explained by conduction being due to doped semiconductor or metallic transport. For PF-type CFs achieved at low I_C, the immunity to RTN increases for increasing V_{read}. This is due to the increased switching rate, which allows for a better averaging between the two resistance levels, and to the reduced RTN amplitude. Therefore, reading at relatively large V_{read} may considerably reduce read error in RRAM.

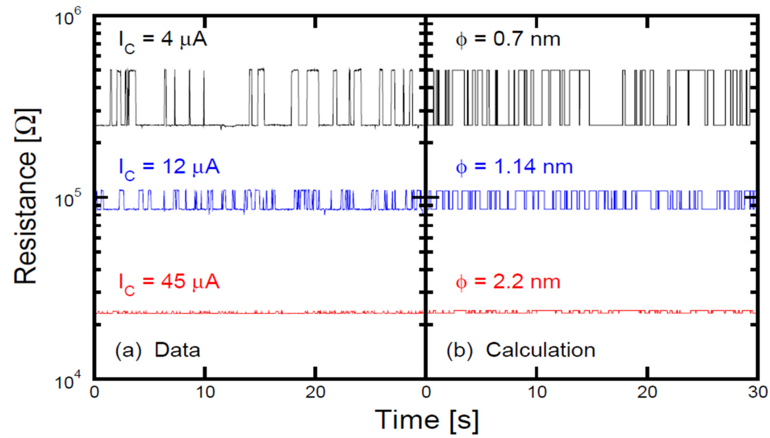

Figure 5.13: Measured (a) and calculated (b) resistance as a function of time for variable size of the CF. RTN shows a dependence on CF size, where the relative amplitude ΔR/R increases at increasing R, thus decreasing CF size.

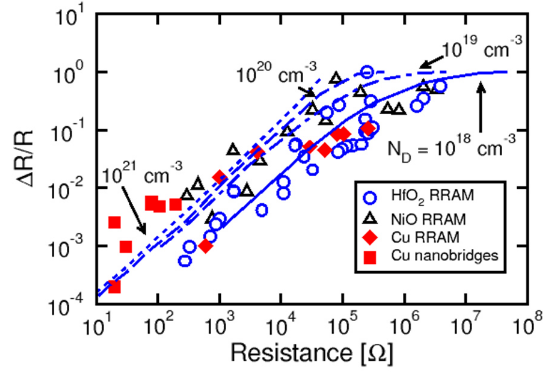

Figure 5.14: Measured and calculated ΔR/R as a function of R. Data for NiO based RRAM [93], Cu-based electrochemical RRAM [98] and Cu nanobridges [99] are also shown for comparison with HfO_x-RRAM data. All data display an universal dependence on R, which can be understood by size-dependent depletion. Calculations were carried out at variable N_D.

5.4 Size-dependent RTN

Fig. 5.13a shows the measured resistance as a function of time for variable resistance, obtained by changing I_C during the set transition. The resistance change ΔR increases with the resistance levels, as shown by the measured relative resistance change ΔR/R as a function of the average resistance R in Fig. 5.14. The figure also reports data from NiO RRAM [93], Cu-based conductive-bridge RAM [98] and Cu nanobridges [99]. All data display an increase of ΔR/R with R below about 100 kΩ, with a saturation at higher R. The RTN dependence on R was previously explained by the size-dependent carrier depletion within the CF [93]. For small R, corresponding to a large CF where the CF diameter ϕ is much larger than λ_D, the trap-induced depletion impacts only partially on the carrier concentration. As ϕ decreases, the depleted region increases, resulting in an increasing ΔR/R. For $\phi < \lambda_D$, full depletion occurs, accounting for the saturated ΔR/R at increasing R. The slope of ΔR/R in Fig. 5.13 at low R is approximately 1 in the bi-logarithmic plot, indicating a linear dependence on resistance. This is because R is inversely proportional to the CF area A_{CF}, thus $|\frac{\Delta R}{R}| \approx |\frac{\Delta A_{CF}}{A_{CF}}| \propto R$ where $\Delta A_{CF} \approx \lambda_D^2$ is the depleted area [93].

Logic based on resistive memory

This Chapter is dedicated to logic computation. An innovative logic, based on RRAM, is presented. Logic computation is obtained through conditional switching in RRAM circuits with serially-connected switches. Same basic gates, like AND, IMP, NOT and bit transfer are demonstrated, each using a single clock pulse, while other functions (OR and XOR) are achieved in multiples step. To support the high functionality of this logic, a 1-bit full adder is demonstrated by simulations and experiments

6.1 Introduction

Moore's law has driven the scaling of CMOS technology for logic and memory applications for almost 40 years. Today, CMOS scaling is becoming increasingly hard mainly due to the increase of the subthreshold leakage current, which raises the static and stand-by power consumptions in digital circuits. To suppress the leakage-induced power, novel device technologies, such as the tunnel field-effect transistor (TFET) [100] and the nanoelectromechanical switch (NEMS) [101] with improved subthreshold slope, have been proposed. A more radical approach consists of adopting materials-based switching, such as spintronic [102–106] and resistive switching [107–110]. In most cases, the switching states of the material are nonvolatile, which allows for storing the input/output states of a logic gate even without any power supply. This approach allows for normally-off logic circuits having two major benefits: (i) the suppression of the static power and (ii) the storage of the computed states in the logic circuit, which may thus be capable of instant boot.

Among the nonvolatile logic concepts, those based on resistive (or memristive) switching have received strong interest due to the scalable operation current [46, 59], the high switching speed [111, 112], and the simple 2-terminal structure, which makes it possible to integrate a switch in crossbar circuit with individual device area of $4F^2$, where F is the minimum feature size allowed by the lithography. Resistive switching is nonvolatile, thus providing the basis for the resistive switching memory (RRAM) for high-density and embedded storage [113–115]. RRAM was initially proposed for application as a reconfigurable switch in field-programmable gate array (FPGA), to

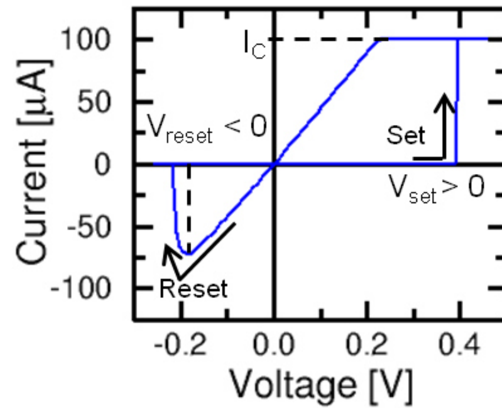

Figure 6.1: Measured I-V curve for the RRAM device showing set and reset transitions under positive and negative voltages, respectively.

reduce the area usually occupied by SRAM-based switches [116–119]. Material implication (IMP) has been demonstrated in RRAM circuits with two parallel-connected switches [107, 108]. IMP allows for functionally-complete logic through the iteration of multiple computing steps, however achieving other logic functions such as AND or NOT in a single clock pulse would allow for greatly reduced computation time and simplified logic operation.

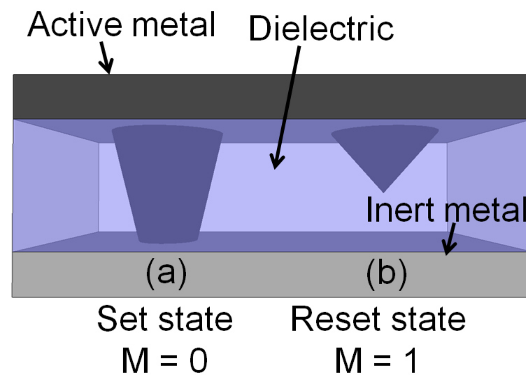

Figure 6.2: Schematic illustration of the RRAM switch in the set (M = 0, a) and reset (M = 1, b) states. Active metal is Ag, while the dielectric is GeS_2.

6.2 RRAM characteristics

To demonstrate logic operations with resistive switching, we used electrochemical RRAM devices provided by Adesto Technologies [113]. The device stack consisted of a W bottom electrode, a GeS_2 solid electrolyte and a Ag top electrode (TE). Resistive switching in these devices is due to the voltage-induced migration of Ag cations within the solid electrolyte, causing the formation/disruption of a conductive filament (CF), or conductive bridge [120, 121]. Fig. 6.1 shows the I-V characteristics of the RRAM device used in our work. Application of a positive voltage above the set voltage V_{set} leads to set transition from high to low resistance, as a result of the formation of the CF. The maximum current is fixed by the measurement setup to a compliance current I_C = 100 μA, to allow control of the CF size, hence of the resistance R. After set transition, the voltage snaps back to a value V_C of about 0.15 V, which identifies the characteristic voltage to induce migration in the CF on the 1-s timescale of the experiment [50]. Application of a negative voltage above the reset voltage V_{reset} results in the reset transition from low to high resistance, revealing the dissolution of the CF by Ag migration back to the TE.

Fig. 6.2 schematically shows the two states of the RRAM devices, namely set state (a) and reset state (b). In the set state, the RRAM has a low resistance R due to the CF connecting top and bottom electrodes. After disconnection of the CF in the reset state, the RRAM displays a high resistance. The shape of the CF in the set and reset states may vary depending on the RRAM concept, material and type of operation, however the details of the CF geometry are not relevant for the resistance switching and logic operation discussed in this work. Electrochemical RRAM devices are considered in this work because of their extremely low power operation, which was demonstrated in the few-nA range [122, 123] and few-ns timescale [124]. In addition, the large resistance window of about 6 decades [123] and the abrupt reset transition in Fig. 6.2, compared to the gradual resistance increase in bipolar oxide-based RRAM devices [41], support Ag-GeS_2 as an ideal device for logic operation.

6.3 RRAM logic gates

Logic computing in RRAM devices can be achieved by first assigning two logic values to the device states in Fig. 6.2. The set and reset states are defined as states M = 0 and 1, respectively, where M is the state variable reflecting the value of V_{set} in the I-V curve [109]. In a RRAM logic gate, the switching devices (or switches) both store the input/output states, and operate in response to an applied driving pulse. Different logic functions are achieved by different values of the pulse voltage, *e.g.*, high/low voltages [109], or positive/negative voltages. This is different from the conventional CMOS logic gates, where each logic function has a specific circuit topology, *e.g.*, a NAND gate differs from a NOR gate by the connection of pull-up and pull-down transistors. The lack of topology in RRAM logic allows for standardization of the circuit architecture, by using, *e.g.*, the crossbar array with extremely high density achieved by the small device size of $4F^2$ [125]. Another key difference from CMOS logic is that the output states are stored in the logic gate even after the supply is turned off, as a result of the nonvolatile behavior of the switch. This allows normally-off operation of the logic circuit with a consequent suppression of the static and stand-by power.

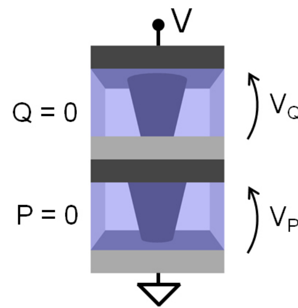

Figure 6.3: Schematic layout of a RRAM-based logic gate. Two switches are connected in series and the logic operation depends on the applied voltage.

Fig. 6.3 schematically shows the structure of a switch-based logic gate. Two RRAM devices P (bottom switch) and Q (top switch) are connected in series. Both switches can be accessed individually, *e.g.*, to write the input state or for reading, by application of a voltage V_P or V_Q as shown in Fig. 6.3. To drive the logic operation, however, the switches must be biased together in the serial configuration, by applying a driving voltage V to the top electrode while leaving the intermediate electrode floating and the bottom electrode grounded. Depending on the states of P and Q and on the polarity of V, conditional switching can take place in either switch, thus resulting in a compute operation. Application of a positive V can result in a set transition of P or Q, while a negative V can induce reset transition in either switch. Finally, the output can be obtained as the final states P' and Q' of the switches, which can then be used as new input states in the same switch or can be transferred to other switches for further operations [109].

6.3.1 AND gate and bit transfer

Fig. 6.4 schematically describes the operation of an AND gate, showing, from left to right, the initial (input) states of the switches, the I-V characteristics with the corresponding RRAM switching, the final (ouput) states and the experimental demonstration of the logic gate. The input states may be directly written in the two RRAM switches, or be transferred there from other switches, or be the result of a previous operation in the switches. The logic operation is enabled by application of a driving pulse of positive voltage ($2V_C < V < 2V_{set}$) across the two serially-connected switches. The applied voltage is positive, thus the switching can only induce set transition in either switch. If P = Q = 0 (a), no switching can take place since the switches are both in the set state, thus the final states are the same as the initial states, namely P' = Q' = 0. For P = 0 and Q = 1 (b), most of the applied voltage drops across Q, causing set transition to Q' = 0. Similarly, for P = 1 and Q = 0 (c), the large voltage drop across P induces set transition to P' = 0. Finally, if both P and Q are equal to 1 (d), the voltage divides equally across P and Q, resulting in no switching in either P or Q, since $V < 2V_{set}$. As a result of this conditional switching, both output states P' or Q' provides the AND function of the input states P and Q, as summarized in Tab. 6.1. As a special case of the AND operation for Q = 1, the state of P is automatically transferred to Q', serving

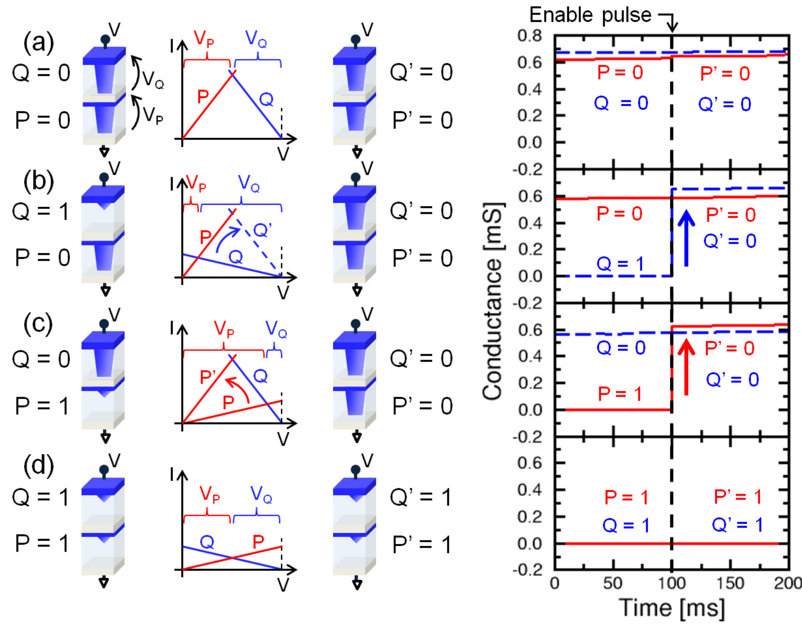

Figure 6.4: Schematic of the RRAM-based AND gate showing (from left to right) the initial (input) states P and Q, the I-V curves for RRAM devices, the final (output) states and the experimental demonstration. The four initial states of P and Q are considered, namely P = Q = 0 (a), P = 0 and Q = 1 (b), P = 1 and Q = 0 (c) and P = Q = 1 (d). A positive voltage is applied, resulting in AND operation (Tab Ia).

P	Q	P' = P·Q	Q' = P·Q
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

Table 6.1: Truth table for AND operation, highlighting the special cases of bit transfer Q' = P·1.

as a scheme for bit transfer between two switches.

The AND function P·Q is experimentally demonstrated for 2 wire-bonded conductive-bridge RRAM switches, as shown by the measured conductance $G = I/V$ in Fig. 6.4. A 100 ms enable pulse with voltage 0.8 V was applied to drive the logic operation, resulting in a set transition from 1 to 0 for P = 0 and Q = 1 (b) and P = 1 and Q = 0 (c). No switching takes place for P = Q in (a) and (d). the conductance for state 0 was around 0.6 mS, corresponding to a resistance of about 1.65 kΩ. This state was achieved by limiting the current to I_C = 100 μA during the initial writing and logic operation. The compliance current was maintained by properly-biased transistors in series with the switches in the so-called one-transistor/one-resistor (1T1R) configuration [46, 59].

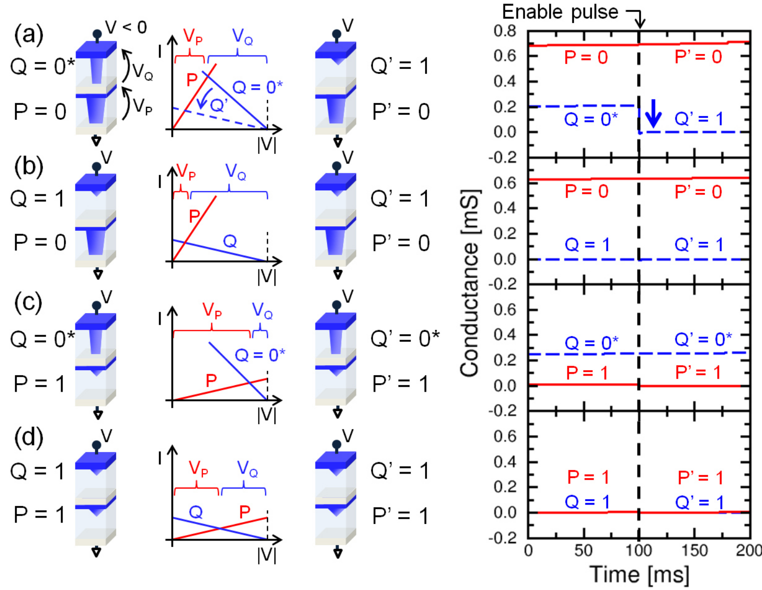

Figure 6.5: Schematic of the RRAM-based IMP logic gate showing (from left to right) the initial (input) states P and Q, the I-V curves for RRAM devices, the final (output) states and the experimental demonstration of logic switching. The four initial states of P and Q are considered, namely P = Q = 0 (a), P = 0 and Q = 1 (b), P = 1 and Q = 0 (c) and P = Q = 1 (d). A negative voltage is applied, resulting in IMP operation.

6.3.2 IMP, NOT and regeneration

Fig. 6.5 shows the material implication (IMP) gate, consisting of the same structure as the AND gate but operated under a negative voltage |V| < $2V_{reset}$. Similar to Fig. 6.4, Fig. 6.5 shows, from left to right, the initial (input) states, the I-V curves with RRAM switching, the final (output) states and the measured conductance before/after application of the enable pulse. For P = Q = 0, the voltage divides equally across P and Q, thus reset occurs in neither P nor Q since |V| < $2V_{reset}$. To allow for switching in this case, Q is prepared in the set state with a smaller compliance current I_C^*, *e.g.*, I_C^* = 30 μA in Fig. 6.6, thus resulting in a smaller CF and in a smaller conductance (about one third of P in Fig. 6.6). This will be referred to as state Q = 0^* in the following. The imbalance between the two states results in more voltage drop across Q, thus forcing transition to Q' = 1 with no disturb to P, as shown by the measured conductance of Q decaying to a small value after the enable pulse in Fig. 6.5a. For P = 0 and Q = 1 (b), the voltage drop across P is negligible, thus preventing any reset transition to occur in P. On the other hand, the large voltage across Q cannot lead to any reset transition, since Q is already in the reset state. Similarly, for P = 1 and Q = 0^* (c), reset transition is inhibited in Q due to the low voltage drop, while P is already in the reset state. Finally, for P = Q = 1 (d), no reset is possible as both RRAMs are already in the reset state. After conditional switching, the output Q' corresponds to the IMP function Q' = P $\rightarrow$ Q, as summarized in Tab. 6.2. For the special case with Q = 0^*, the output Q' provides the function Q' = NOT(P), thus working as a bit inverter.

P	Q	P' = P	Q' = P→Q
0	0*	0	1
0	1	0	1
1	0*	1	0*
1	1	1	1

Table 6.2: Truth table for IMP operation, highlighting the special cases of bit inverter Q' = NOT(P) = P→0*.

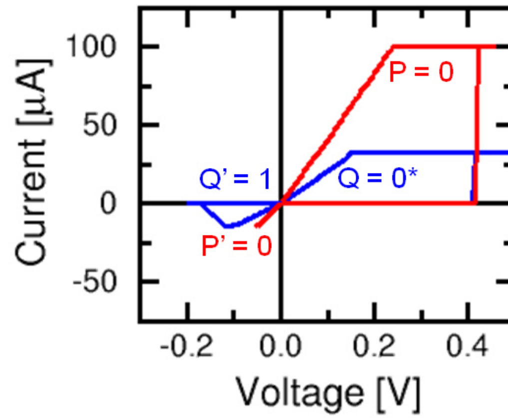

Figure 6.6: Measured I-V curves during preliminary write (V > 0) and compute (V < 0) for IMP with P = 0 and Q = 0*. For controlled switching to Q' = 1, Q must be set to a higher R (state Q = 0*) with lower I_C.

Fig. 5 also shows the measured conductance G before and after the application of the enable pulse, indicating the reset transition from Q = 0* to 1 in (a). Transistors in the 1T1R structures were biased to high conductance to minimize the voltage drop across them.

The introduction of the third state 0* makes regeneration steps necessary, whenever an output state 0 must serve as the second operand in an IMP operation, where 0* is instead expected. In this case, the state 0 can be transferred to an auxiliary switch initially in state 1 by an AND operation with reduced compliance I_C^*. The auxiliary switch can then be used as second input in the IMP operation. The opposite case is also possible, namely an output state 0* is needed as first operand in an IMP operation. In this case, the switch can be straightforwardly regenerated by a set operation at a voltage V between V_C and V_{set} in Fig. 6.1. In fact, state 0* will switch to 0 by CF growth accelerated by the voltage being higher than V_C, while state 1 is not disturbed since $V < V_{set}$. Fig. 6.7 shows the measured I-V curves for state 0 (a), 0* (b) and 1 (c), indicating regeneration of state 0* in Fig. 6.7b with no disturb on 0 and 1. Finally, note that 0 and 0* can both appear as input states in AND operation, since the output is always 0, except for both initial states being P = Q = 1.

Another approach to achieve different reset behaviors for P and Q in Fig. 6.5a is to use different RRAM materials for P and Q. For instance, the Ag-GeS_2 RRAM used

in this work shows a remarkable asymmetry between the set and the reset processes, where the I_{reset} can be significantly smaller than I_C [126]. The ratio I_{reset}/I_C can be as small as 0.1 for Ag-GeS_2 RRAM devices and was shown to depend on I_C, namely an increasingly smaller I_{reset}/I_C is obtained at decreasing I_C [126]. The set/reset asymmetry was attributed to the compressive stress affecting the CF after set transition and contributing to the CF retraction during reset transition. On the other hand, RRAM based on metal oxides, such as HfO_x [41,50,59] and TaO_X [127], usually display symmetric set/reset processes with $I_{reset} \approx I_C$. No significant stress effects are expected in this case, due to the presence of both cations, *e.g.*, ionized Hf in HfO_2, and anions, i.e., O^{2-}. The opposite migration of cations and anions might minimize accumulation of impurities and stress buildup. A logic gate where P has symmetric switching ($I_{reset} \approx I_C$) and Q has asymmetric set/reset switching ($I_{reset} < I_C$) can intrinsically allow for the IMP behavior in Fig. 6.5.

6.3.3 OR gate

Other logic functions can be achieved by combining IMP, NOT and AND functions discussed above. OR can be simply obtained through the DeMorgan theorem, namely A+B = NOT(NOT(A)·NOT(B)). This translates into three pipelined operations, namely (i) inversion of both inputs A and B, which can be operated in parallel, (ii) AND operation and (iii) inversion of the previous output. This sequence is summarized in Tab 6.3, showing the 5 switches used for the operation, namely the 2 input switches P1 = A, P2

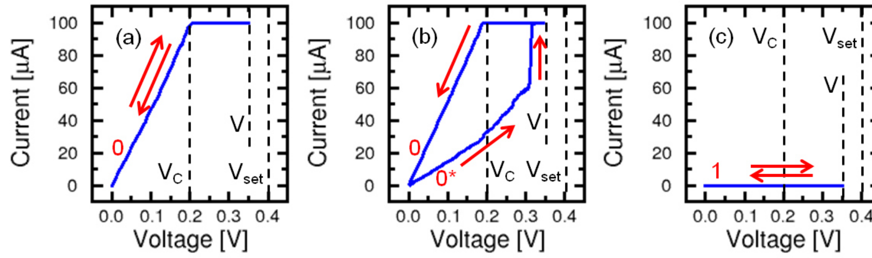

Figure 6.7: Measured I-V curves during regenerate operation for the state 0 (a), 0* (b) and 1 (c). Applying a voltage between V_C and V_{set} state 0* switches to state 0 (b) while state 1 (c) is not disturbed since $V < V_{set}$

Clock =	1	2	3
P1=A			
P2=B			
P3=0*	P1→P3	P3·P4	
P4=0*	P2→P4	P3·P4	
P5=0*			P4→P5

Table 6.3: Implementation of OR gate in 3-pulses sequence with 5 switches. IMP operations are highlighted in gray while the output result is highlighted in green.

= B, the output switch P5 = A OR B, and 2 auxiliary switches P3 and P4. Switches P3 and P4 are initially prepared in state 0^*, since they must operate in IMP operations aimed at inversion (see Tab. 6.2). In the first clock pulse, P3 receives the inverted value of P1, while P4 receives the inverted value of P2. Then, AND of P3 and P4 is performed at the second clock pulse. Note that any state 0^* <would be regenerated to 0 in the second stage, since AND is operated at a compliance current $I_C > I_C^*$. In the third stage, P4 is inverted and transferred into the output switch P5. The output state can be either 0^* or 1, thus can be readily used as second operand in a subsequent IMP operation. In case of read or other types of operation (*e.g.*, AND, or first operand in IMP), the output must be regenerated from 0^* to 0, as shown in Fig. 6.7.

Fig. 6.8 demonstrates the OR operation by showing the measured current during the three stages of OR operation in Tab. 6.3, namely NOT, AND and final NOT. Input states A = 0 and B = 1 were chosen to exemplify the logic operation. For the experimental demonstration, RRAM devices with 1T1R structures were wire-bonded for serial connection in the logic-gate architecture of Fig. 6.3. P3 first shows reset transition at the beginning of clock pulse #1, then undergoes set transition during the AND operation in the second clock pulse. Finally, a reset transition appears in P5 due to P4 = 0^*. The final state P5 = 1 provides the output of the OR operation. The functionality of the logic gate can be similarly demonstrated for other states of the inputs A and B.

6.3.4 XOR gate

The XOR operation A $\oplus$ B can be achieved in 3 steps by cascading NOT, IMP and AND, namely:

$$A \oplus B = (A \to B') \cdot (B' \to A), \tag{6.19}$$

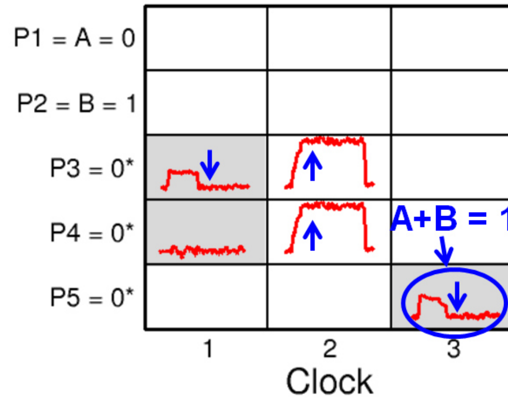

Figure 6.8: Measured switching current for an OR gate with input A = 0 and B = 1. Switches are indicated as P1 through P5, with P1 and P2 serving as input, P3 and P4 serving as auxiliary switches, and P5 serving as output. Three clock pulses are used for the OR operation. Arrows indicate set and reset transitions, IMP operations are highlighted in grey.

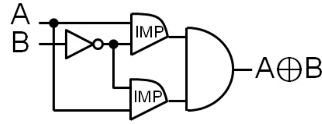

Figure 6.9: Schematic layout of XOR gate achieved using NOT, IMP and AND.

which is schematically shown in Fig. 6.9. Tab. 6.4 shows the 4-pulse sequence to complete XOR operation in a circuit of 5 RRAM switches. First, A is copied from P1 to P5 with reduced compliance I_C^* to change 0 into 0*, while B is inverted in P3. In the second pulse, the inverted B is regenerated to change 0* into 0, while another inverted B is transferred into P4. These 2 pulses complete the preliminary NOT operations in Fig. 6.9. IMP operations are carried out in the third pulse, with output in P4 = A→B' and in P5 = B'→A. Finally, the AND product P4·P5 is performed in the fourth pulse. Fig. 6.10 shows the measured (a) and calculated current (b) as a function of time during the operation of the XOR sequence of Tab. 6.4. The demonstration was done for input A = 0 and B = 1, resulting in an output P4 = P5 = A ⊕ B = 1. Calculations were achieved by simulating the 2-RRAM switches with current limitation to describe the effect of the select transistors. Simulations were done by using an analytical model for RRAM set/reset temperature- and field-assisted migration of ionized defects [37].

Clock =	1	2	3	4
P1=A	P1·P5			
P2=B				
P3=0*	P2→P3	P3=P3		
P4=0*		P2→P4	P1→P4	P4·P5
P5=1	P1·P5		P3→P5	P4·P5

Table 6.4: Implementation of XOR gate in 4-pulses sequence with 5 switches. IMP operations are highlighted in gray while the output result is highlighted in green.

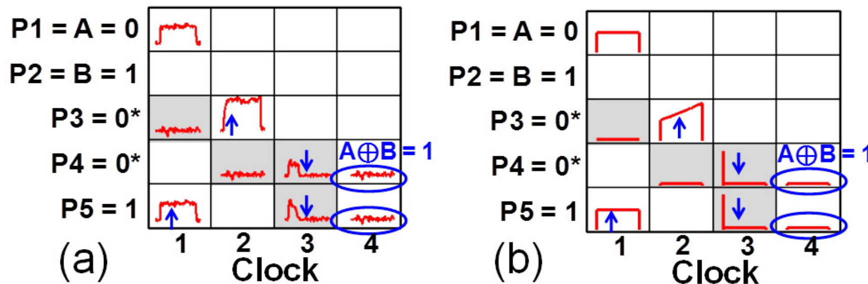

Figure 6.10: Measured (a) and calculated (b) switching current for a XOR gate with input A = 0 and B = 1. Arrows indicate set and reset transitions.

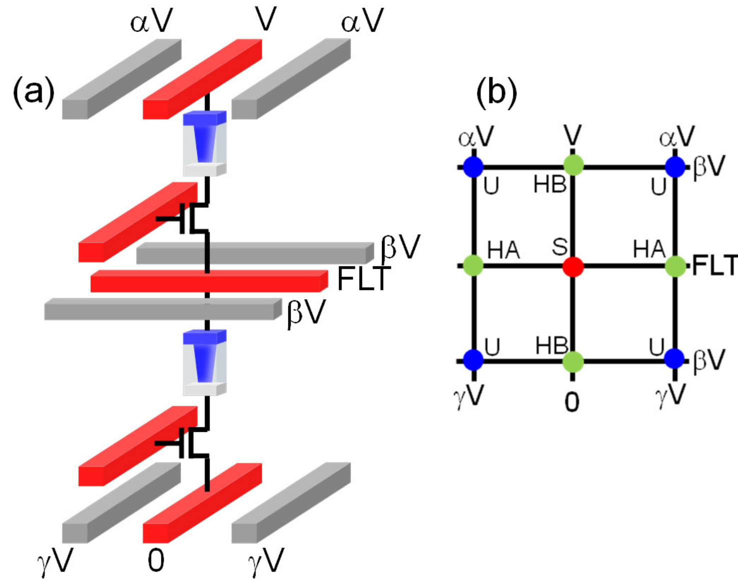

Figure 6.11: Schematic view of 2 stacked arrays with 1T1R architecture (a) and corresponding plan view (b). The selected columns are biased at V and 0 while the unselected at αV and γV. The selected row is floating and the unselected rows are biased at βV. Depending on its position in the array a cell can be selected (S), unselected (U) or half selected (HA and HB).

XOR operation is essential to achieve more complex functions, such as addition [128].

6.4 1T1R crossbar implementation

Our general implementation consists of 2 stacked crossbar arrays, each array being a periodic sequence of rows and columns with a RRAM switch located between each row and column. The intermediate rows are shared between the top and the bottom crossbar arrays [125]. The stacked structure allows to naturally implement the serial-RRAM structure of the logic gate [110]. Here it is possible to either independently access individual cells within each crossbar array, *e.g.*, for the write operation, or access any given logic gate by applying a voltage V to the top column with grounded bottom column and floating intermediate row, to perform any given logic operations [110].

Fig. 6.11a illustrates one possible array implementation of RRAM logic, where RRAMs in both the top and bottom crossbars are accompanied by a select transistor in the so-called one-transistor/one-resistor (1T1R) structure. Only the selected RRAM gate is shown in all schemes, where a simple logic operation, *e.g.*, AND, is carried out. While the scheme in Fig. 6.11a is totally agnostic with respect to the specific integration approach, the select transistor might be thought as a vertical gate-all-around (GAA) transistor, similar to the upper select gate and bottom select gate in 3D flash architectures [129] and one-transistor/one-capacitor DRAM [130]. With respect to the conventional crossbar approach with passive selector elements (*e.g.*diode), the 1T1R

with a vertical GAA transistor would require a row/column pitch of 3F instead of 2F, to accommodate the channel width (1F), the gate line space surrounding the channel (1F) and the spacer (1F). Therefore, the estimated single device area is $9F^2$, instead of $4F^2$ of an ideal passive crossbar.

Fig. 6.11a also shows a generic bias scheme for logic operation in the selected gate, where a voltage V is applied to the top column, while the bottom column is grounded and the intermediate row remains floating. The voltage V is positive for AND (or transfer) operations, while V is negative for IMP (and NOT) operations. For the sake of simplicity, we assumed that the top and bottom RRAM in the logic gate are located at the same coordinates on the array, although they also might be located at different positions, provided that they share the same intermediate floating row. The input states (set state 0 or reset state 1) are initially stored in the two switches at the selected position in the array. In the following, we will assume that IMP operation takes place by different reset voltages in the top and bottom RRAM switches, namely the bottom RRAM switch (P) has a relatively large reset voltage V_{reset}, while the top RRAM switch (Q) has a small reset voltage $V^*_{reset} < V_{reset}$ [110]. The small value of V^*_{reset} causes Q to reset first in the IMP gate, thus allowing to achieve IMP functionality. As discussed in [110], different reset voltages can be obtained by different materials in the RRAM device, *e.g.*, using an electrochemical-type RRAM with Ag or Cu electrode to achieve asymmetric switching with relatively small reset voltage [50].

The logic operation takes place in the selected RRAM switches by applying positive/negative V with appropriate voltages V_{G1} and V_{G2} to the gate of the select transistors to activate the current path across the selected RRAMs. Note that the transistor gate lines are parallel to the columns, and unselected gate lines are left at low voltage to avoid any disturb to the unselected RRAM elements during either write or logic computation. To unselect all other RRAMs in the crossbar arrays, the unselected top columns, intermediate rows and bottom columns must be biased to an appropriate voltage. As shown in Fig. 6.11a, voltage values αV, βV and γV, with α, β and γ being positive and less than 1, are used to bias the unselected top columns, intermediate rows and bottom columns, respectively. To study the disturb conditions for α, β and γ, four cases can be considered depending on the position of the logic gate as shown in the top-view of the crossbar circuit in Fig. 6.11b. Each of these cases will be considered in the following subsections.

6.4.1 Selected gate.

The selected gate (S in Fig. 6.11b) is located at the crossing between the top column biased at V and the floated row. The grounded column is assumed exactly below the top column biased at V. Logic switching occurs in S according to the AND and IMP operations [110]. To induce the logic operation the applied voltage must satisfy the following conditions:

$$V_{set} < V < 2V_{set}, \tag{6.20}$$

for AND operation, and:

$$V > 2V^*_{reset} + 2V_{MOS}, \tag{6.21}$$

for IMP operation, where the voltage V_{MOS} across the transistor depends on the current I through the equivalent transistor resistance R_{MOS}, namely $V_{MOS} = R_{MOS}I^*_{reset}$.

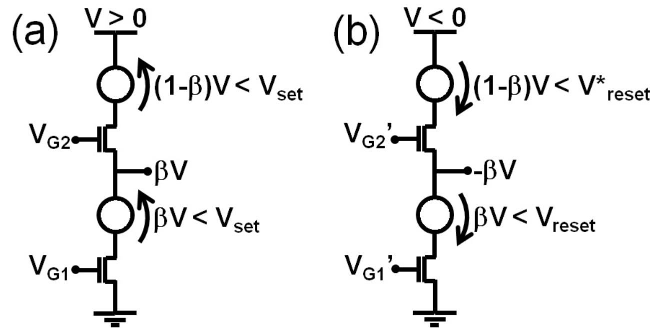

Figure 6.12: Generic half-selected gates HB during AND (a) and IMP (b) operation. Note the different gate voltages in (a) and (b), where V_{G1} and V_{G2} are smaller than V'_{G1} and V'_{G2} to properly control the current during the set transition.

Note that there is no maximum limit for V in Eq. (6.21): in fact, as soon as reset transition of Q occurs at I^{*}_{reset}, almost the entire applied voltage drops across Q due to its high resistance, thus protecting P against any disturb. A practical maximum limit of V in Eq. (6.21) is therefore the breakdown voltage for Q. On the other hand V_{MOS} can be neglected for AND operation in Eq. (6.20) because I is approximately zero.

6.4.2 Unselected gates.

The unselected gates (U in Fig. 6.11b) do not share any row or column with the selected gate. The transistors of these logic gates are non-conducting since the gate voltage is low on all unselected gate lines. Therefore, no disturb can take place on these logic gates.

6.4.3 Half-selected gate of type A.

The half-selected gate of type A (HA in Fig. 6.11b) is located at the crossing between a generic unselected column and the selected row. These are not affected by any disturb, since the select transistors are switched off.

6.4.4 Half-selected gate of type B.

The half selected gate of type B (HB in Fig. 6.11b) is located at the crossing between the selected column and a generic unselected row. The transistors of these logic gates are conducting since they share the high voltage of the selected logic gates in the top and bottom arrays, respectively. Fig. 6.12 shows a generic HB gate during AND operation (a) and IMP operation (b), differing by the polarity of the voltage applied to the top column. The gate voltages are also different to ensure proper biasing of the transistors for set (a) and reset (b) operations during AND and IMP, respectively. In the case of AND, disturb should be avoided by ensuring that the voltages across the RRAM

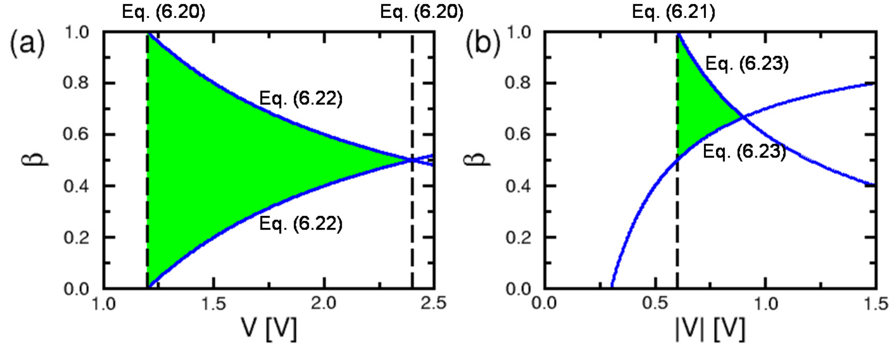

Figure 6.13: Range of allowed values of parameter β as function of applied voltage for AND (a) and IMP (b) operations. The range is limited by conditions described in Eqs. (6.20-6.22).

Table 6.5: Parameter values used to evaluate the allowed range of α, β and γ in Fig. 6.13 and Fig. 6.16.

Parameter	**Value**
V_{set}	1.2 V
V^*_{reset}	0.2 V
V_{reset}	0.4 V
V_C	0.4 V
I_C	10 μA
R_{MOS}	20 kΩ
R_S	20 kΩ

switches are both below the set voltage V_{set}. Based on Fig. 6.12a, this condition reads:

$$1 - \frac{V_{set}}{V} < \beta < \frac{V_{set}}{V}, \tag{6.22}$$

for AND operation. The condition in Eq. (6.22) is represented in Fig. 6.13a as the range of suitable values of β as a function of the applied voltage V during AND operation. In these calculations, the values of V_{set} and V_C shown in Tab. 6.5 were assumed. The figure also includes the conditions expressed by Eq. (6.20) about the minimum and maximum voltages necessary to operate the AND logic gate [110]. Clearly, a large difference between V_C and V_{set} is beneficial to broaden the window of β. The other parameters α and γ, which do not impact the disturb analysis, can be conveniently chosen to be around 0.5.

For IMP operation, both βV and (1-β)V must be smaller than the reset voltage to avoid reset transition in either the top or bottom device of HB. The acceptable β must thus comply with the condition:

$$1 - \frac{V^*_{reset}}{V}(1 + \frac{R_{MOS}}{R}) < \beta < \frac{V_{reset}}{|V|}(1 + \frac{R_{MOS}}{R}), \tag{6.23}$$

which is shown in Fig. 6.13b as the allowed range of parameter β as a function of the absolute value of the voltage V applied in the IMP operation. Also the minimum

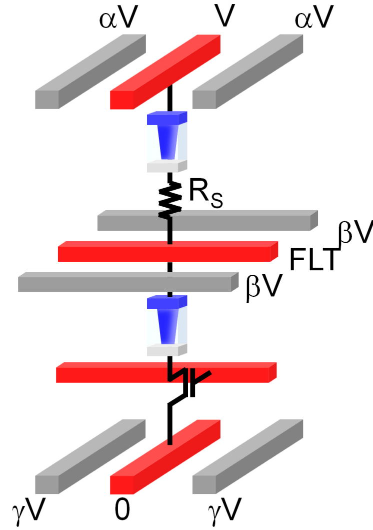

Figure 6.14: Schematic view of the alternative structure 1T1R/1R1R. With respect to the 1T1R structure in Fig. 6.11a, the transistor of the top RRAM is replaced by a resistor R_S for selection and current limitation.

voltage in Eq. (6.21) to operate the IMP logic gate is shown in the figure. Assuming the values of V_{set}, V^{*}_{reset} and V_{reset} in Tab. 6.5, β can be conveniently chosen within the range from 0 to 1 during AND operation and from 0.5 to 1 during IMP operations, depending on the applied voltage. On the other hand, coefficients α and γ are not relevant for disturb, thus a convenient value of α = γ = 0.5 can be assumed.

6.5 Hybrid 1T1R/1R1R architecture

A simple alternative to the 1T1R structure is the hybrid structure schematically shown in Fig. 6.14, where RRAM switches are accompanied by a select transistor in the bottom layer, while a passive resistance R_S is used in the top layer for the purpose of cell selection and current limitation. The transistors in the bottom layer can thus be fabricated as front-end transistors with either horizontal (conventional) or vertical geometry. No transistors in the top layer are needed, thus alleviating the complexity of the crossbar fabrication. The gate lines are parallel to the intermediate rows for convenience of the biasing scheme. As in the full 1T1R architecture, the selected top and bottom columns are biased at V and 0, respectively, while the intermediate row is left floating to allow for conditional switching during AND or IMP operations. Write of input states is allowed by independently biasing either the top cell or the bottom cell within their respective crossbar, leaving all columns of the other crossbar floating. Selection in the 1R1R (top) crossbar is possible by using a V/2 biasing scheme, where only the selected cell is biased to sufficient voltage for set/reset operation. Current limitation, which is needed to achieve a given value of resistance in RRAM, is obtained by using the select transistor with proper gate bias in the bottom layer, or the load

resistance R_S in the top layer. In fact, application of a voltage V_S for setting the RRAM switch results in a current $I_C = (V_S - V_C)/R_S$ after set, where V_C is the characteristic voltage capable of activating ionic migration in the RRAM switch in the timescale of the set operation [50]. The current I_C then controls the set-state resistance of the RRAM according to $R = V_C/I_C$. To read the content of any RRAM switch in the bottom crossbar array, the 1T1R structure can be used to selectively activate the current path along the selected cell. On the other hand, reading a cell in the top crossbar, is possible by first transferring the bit value to the bottom crossbar through a modified AND operation [110], then reading the corresponding bottom RRAM switch. A similar procedure can be used for writing input states in the top crossbar, in case the V/2 scheme is inappropriate due to excessive spread of the set/reset voltages.

To study the disturb effect during logic operation in the crossbar array, we considered all cases of unselected and half-selected logic gates as indicated in Fig. 6.11b.

6.5.1 Selected gate (S):

To induce the logic operation the applied voltage must satisfy the conditions:

$$V_{set} < V < 2V_{set}, \tag{6.24}$$

for AND operation, and

$$V > 2V^*_{reset} + V_{R_S} + V_{MOS}, \tag{6.25}$$

where V_{R_S} is the voltage across the series resistance, namely $V_{R_S} = R_S I_{*reset}$, similarly to Eq. (6.21).

6.5.2 Unselected gate (U):

First, we consider the U gates, sharing neither the row nor the column with the selected gate. The bias of the U gate is shown in Fig. 6.15a: the low gate voltage protects the bottom RRAM from any possible disturb, while the top RRAM case must be studied in detail. To rule out any disturb, the voltage drop across the top cell must be lower than V_{set} and higher than $-V^*_{reset}$, where V^*_{reset} is assumed positive. This condition can be generally expressed as:

$$-V^*_{reset} < (\alpha - \beta)V - R_S I < V_{set}, \tag{6.26}$$

for IMP operation where V is positive for AND operation and negative for IMP operation, or the current I is assumed positive if it flows from top to bottom. In cases $\alpha > \beta$ for AND operation ($V > 0$) and $\alpha < \beta$ for IMP operation ($V < 0$), the voltage across the cell is positive, which may induce a set transition. Since set transition can only take place in state 1, the current I can be neglected, thus Eq. (6.26) becomes $(\alpha - \beta)V < V_{set}$, which considering positive and negative V becomes:

$$\alpha - \beta < \frac{V_{set}}{V} \tag{6.27}$$

for AND operation, and

$$\beta - \alpha < \frac{V_{set}}{|V|} \tag{6.28}$$

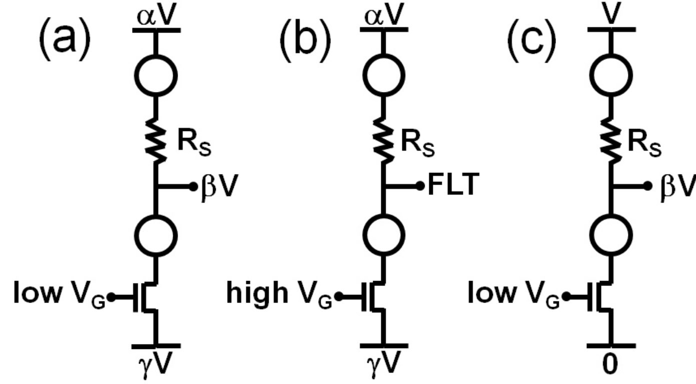

Figure 6.15: Bias configuration during logic operation for unselected cell U (a), half-selected cell HA (b) and half-selected HB defined according to Fig. 6.11b.

for IMP operation. On the other hand, assuming $\alpha < \beta$ for AND operation (V > 0) and $\alpha > \beta$ for IMP operation (V < 0), the disturbing voltage is negative, thus may possibly induce reset transition in state 0, where the current is not negligible anymore. Therefore, Eq. (6.26) becomes $(\beta - \alpha)V < V^*_{reset} - R_S I$, which, by noting $I = (\alpha-\beta)V/(R + R_S)$ and distinguishing between positive and negative V, becomes:

$$\beta - \alpha < \frac{V^*_{reset}}{V}(1 + \frac{R_S}{R}) \tag{6.29}$$

for AND operation, and:

$$\alpha - \beta < \frac{V^*_{reset}}{|V|}(1 + \frac{R_S}{R})\ (IMP\ operation) \tag{6.30}$$

for IMP operation.

6.5.3 Half-selected gate of type A (HA):

Cells sharing the same row and the same gate voltage as the selected device are biased according to the scheme in Fig. 6.15b. Disturb might take place in both the top and bottom RRAM, and all possible values of the floating node potential (FLT) should be considered. As worst cases, we consider FLT = 0 and FLT = V in the following, namely the minimum and maximum potential for the floating node. In the case FLT = 0, the voltage across the top RRAM switch should not exceed the set voltage during AND operation or the reset voltage during the IMP operation, which reads:

$$-V^*_{reset} < \alpha V - R_S I < V_{set} \tag{6.31}$$

which, after considering the different values of the current for set and reset disturbs, becomes:

$$\alpha < \frac{V_{set}}{V} \tag{6.32}$$

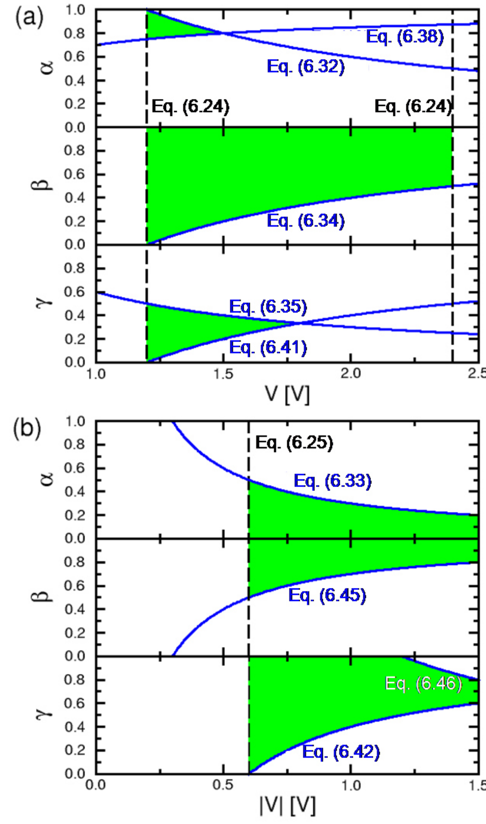

Figure 6.16: Range of allowed values of parameters α, β and γ for AND (a) and IMP (b) operations.

for AND operation, and:

$$\alpha < \frac{V^*_{reset}}{|V|}(1 + \frac{R_S}{R}) \tag{6.33}$$

for IMP operation. For the bottom RRAM switch, similar conditions apply to prevent disturb, namely:

$$-V_{set} < \gamma V - R_{MOS} I < V_{reset} \tag{6.34}$$

which, after considering the different operations can be rewritten as:

$$\gamma < \frac{V_{reset}}{V}(1 + \frac{R_{MOS}}{R}) \tag{6.35}$$

for AND operation, and:

$$\gamma < \frac{V_{set}}{|V|} \tag{6.36}$$

for IMP operation.

Similar equations are obtained for the case FLT = V. First, the top-RRAM voltage should not exceed either the set or reset voltages according to:

$$-V_{set} < (1-\alpha)V - R_S I < V^*_{reset} \quad (6.37)$$

where the set and reset disturb conditions apply to IMP (V < 0) or AND (V > 0) operations, respectively. Eq. (6.37) can be thus restated as:

$$\alpha > 1 - \frac{V^*_{reset}}{V}(1 + \frac{R_S}{R}) \quad (6.38)$$

for AND operation, and:

$$\alpha > 1 - \frac{V_{set}}{|V|} \quad (6.39)$$

for IMP operation. For the bottom RRAM switch, similar conditions apply to prevent disturb, namely:

$$-V_{reset} < (1-\gamma)V - R_{MOS} I < V_{set} \quad (6.40)$$

where the set and reset disturb conditions apply to AND (V > 0) or IMP (V < 0) operations, respectively. Eq. (6.40) can be thus rewritten as:

$$\gamma > 1 - \frac{V_{set}}{V} \quad (6.41)$$

for AND operation, and:

$$\gamma > 1 - \frac{V_{reset}}{|V|} * (1 + \frac{R_{MOS}}{R}) \quad (6.42)$$

for IMP operation. Conditions on α and γ in Eqs. (6.32-6.42) are included in Fig. 6.16 for AND operation (a) and for IMP operation (b).

6.5.4 Half-selected gate HB:

Cells sharing the same column as S are biased according to the scheme in Fig. 6.15c. The select transistor in the bottom RRAM is in an off state, thus disturb can only take place in the top cell. For this RRAM switch, the voltage should not exceed either the set or reset voltages according to:

$$-V^*_{reset} < (1-\beta)V - R_S I < V_{set} \quad (6.43)$$

where the set and reset conditions apply to the AND and IMP operation, respectively. These two conditions can be distinguished as follows:

$$\beta > 1 - \frac{V_{set}}{V} \; (AND\ operation) \quad (6.44)$$

$$\beta > 1 - \frac{V^*_{reset}}{|V|}(1 + \frac{R_S}{R}) \; (IMP\ operation) \quad (6.45)$$

which are represented in Fig. 6.16 for AND operation (a) and IMP operation (b).

6.5.5 Operating window of α, β and γ:

Fig. 6.16 shows the allowed range of parameters α, β and γ as function of V for AND (a) and IMP (b) operations. Using the values reported in Tab. 6.5, the conditions expressed by Eqs. (6.27-6.30) are satisfied irrespective of the applied voltage.

From Fig. 6.16, the most strict condition is on α during AND operation, where the parameter is limited by V_{set}, V_{reset} and R_S. The window can be increased using a larger value for R_S. This causes also an increase of the other parameters β and γ, although V shift to high voltage for IMP operation due to Eq. (6.25).

6.6 1-bit adder

To fully support RRAM logic, complex functions such as the 1-bit full adder must be demonstrated [102, 131, 132]. Fig. 6.17 schematically shows the input/output flow diagram of a 1-bit adder, where input bits A and B are summed with carry-in C_{in}, to yield the output S given by:

$$S = A \oplus B \oplus C_{in}, \tag{6.46}$$

where $\oplus$ indicates the XOR function. The carry-out bit C_{out} is given by:

$$C_{out} = (A \cdot B) + C_{in} \cdot (A \oplus B), \tag{6.47}$$

where the AND and OR operations can be replaced by IMP functions, thus leading to:

$$C_{out} = ((A \oplus B) \rightarrow C_{in}) \rightarrow (A \cdot B). \tag{6.48}$$

Eqs. 6.46 and 6.48 can be implemented with RRAM logic relying on the AND, IMP, OR and XOR functions already described in [110]. Tab. 6.6 reports the sequence of operations in the proposed RRAM adder at each clock signal. In this implementation, we adopted a general RRAM-logic approach [110], where IMP is operated by the use of three states, namely 0, 0^* and 1. This allowed us to experimentally demonstrate the scheme of Tab. 6.6, since the RRAM devices with different reset currents I_{reset} and I^*_{reset} were not available.

Addition in Tab. 6.6 is completed in 7 clock pulses with 11 RRAM switches. Input states A and B are initially stored in switches P1 and P2, respectively, while the C_{in} is

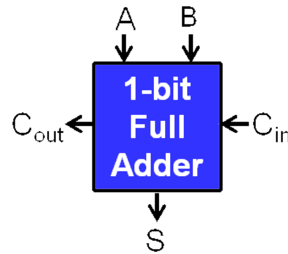

Figure 6.17: Flow diagram of a 1-bit adder with input A and B, output S, carry-in C_{in} and carry-out C_{out}.

Table 6.6: Sequence of operations in the 1-bit addition with 7 clock pulses and 11 switches. IMP and regeneration (*e.g.*, P3 = P3) are reported in the output switch only, while AND is reported for both switches. Input states are located in P1 = A, P2 = B, output state in P6 = P11 = S, carry-in in P7 = C_{in} and carry-out in P10 = C_{out}.

Clock=	1	2	3	4	5	6	7
P1 = A	P1·P5			P1·P2			
P2 = B				P1·P2	P1·P10		
P3 = 0*	P2→P3	P3=P3					
P4 = 0*		P2→P4	P1→P4	P4·P5			
P5 = 1	P1·P5		P3→P5	P4·P5	P5·P6		
P6 = 1					P5·P6	P8→P6	S=P6·P11
P7 = C_{in}							
P8 = 0*	P7→P8	P8=P8					
P9 = 0*		P7→P9			P4→P9	P9=P9	
P10 = 1					P2·P10		C_{out}=P9→P10
P11 = 0*			P7→P11			P5→P11	S=P6·P11

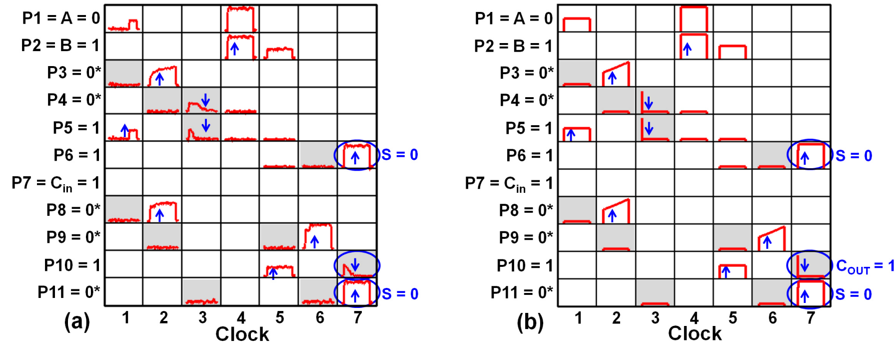

Figure 6.18: Experimental (a) and simulated (b) current in RRAM gates for demonstrating the 1-bit adder according to the scheme in Tab. II. The current is shown only in the output RRAM for IMP (highlighted in gray), and in both RRAMs for AND operations. The blue arrows indicate set (1 to 0) or reset (0 to 1) transitions in the logic switch. The operation current was I_C = 80 μA, pulse time = 100 ms.

stored in P7. Other auxiliary switches are initially prepared in either state 0^* or state 1, depending on their use. The output S finally appears in switch P6 at clock 7, while the C_{out} is located in P10. In the first 4 clock pulses, the XOR operation A $\oplus$ B is completed through AND and IMP operations according to the algorithm:

$$A \oplus B = (A \to B') \cdot (B' \to A), \tag{6.49}$$

in agreement with Tab. 6.4 [110]. The result of the XOR operation is found in P4 and P5 at clock #4, and is further replicated in P6 at clock #5. During this initial phase, the negated C_{in} is replicated in three auxiliary switches, namely P8 (clock #1 and #2), P9 (clock #2) and P11 (clock #3). At clock #6, the operations $C'_{in} \to A \oplus B$ and $A \oplus B \to C'_{in}$ which are needed to complete the second XOR operation in Eq. (6.46), are completed in P6 and P11, respectively, then their respective outputs are used as inputs for the final AND operation providing the output S at clock #7. To compute the carry out, the operations $(A \oplus B) \to C'_{in}$ and $A \cdot B$ are performed at clock #5 in P9 and P10, respectively, then their output are combined through the final IMP operation at clock #7 in P10, according to Eq. (6.48).

The RRAM adder requires a relatively small area consumption of only 11 switches, which would correspond to areas of $44F^2$ or $22F^2$, in the case of an ideal crossbar with one or 2 layers, respectively. Assuming the 1T1R architecture in Sec. 2 with a vertical transistor and $9F^2$ area of the individual switch, the ideal area consumption would rise to about $100F^2$ or $50F^2$, in the case of one or 2 layers. These results suggest a huge area saving consumption with respect to the 28-transistor adder in CMOS logic requiring few-thousands of F^2 in CMOS technology [102, 131]. The switch count and area consumption of the RRAM adder are also advantageous compared to adder circuits based on alternative technologies, such as magnetic or domain wall logic [106].

6.6.1 Experimental demonstration

The RRAM adder in Tab. 6.6 was experimentally demonstrated by wire-bonded RRAM devices with 1T1R architecture [128]. The integrated select transistors was used to control the operation current to values I_C = 80 μA and I_C^* = 30 μA for states 0 and 0^*, respectively. As a representative case, Fig. 6.18a shows the measured current in the serially connected RRAM switches during a 1-bit addition according to Tab. 6.6, for initial input states A = 0 and B = 1 with carry-in C_{in} = 0. Each clock pulse lasted 0.1 s. Grey boxes indicate IMP operation (V < 0), while all other boxes contain AND operations (V > 0). The current is shown for both RRAM switches for AND operations. For instance, the current shown in P1 and P5 at clock #1, representing the operation P1·P5, shows a steep increase at about 2/3 of the pulse-width, due to the transition of P5 from state 1 to state 0, indicated as a blue arrow in P5. A reduced compliance current I_C^* was used during this operation since P5 must serve as second operand in the IMP operation P3 $\to$ P5 at clock #3. Similar set transitions during AND operations take place in P1·P2 at clock #4, P2·P10 at clock #5 and P6·P11 at clock #11. Confirm transitions from 0^* to 0 were carried out in P3 and P8 at clock #2 and P9 at clock #6. The current during a generic IMP operation P $\to$ Q is shown for the second operand (Q) only. For instance, the current during the operation P2 $\to$ P3 with P2 = B = 1 at clock #1 is shown for P3 only. Since P2 remains in the off state, only a low, off-state

current can be seen with no switching. Reset transitions $0^* \rightarrow 1$ during IMP operations are seen in P4 and P5 at clock $\#3$ and P10 = C_{out} at clock $\#7$.

Fig. 6.18b shows the calculated current response for the same addition as in Fig. 6.18a. Simulations were achieved with an analytical model for RRAM based on filament growth/dissolution activated by the local field and temperature [37]. Set and reset transitions well agree with the experimental switching behavior in Fig. 6.18a.

6.6.2 Energy consumption

The energy consumption in Fig. 6.18 can be estimated by the formula:

$$\begin{aligned} E_{add} =& N_{1\rightarrow 0}V_+I_C\frac{t_P}{2} + N_{1\rightarrow 0^*}V_+I_C^*\frac{t_P}{2} + N_0V_+I_Ct_P \\ &+ N_{0^*\rightarrow 0}V_+(I_C + I_C^*)\frac{t_P}{2} + N_{0^*\rightarrow 1}V_-I_C^*\frac{t_P}{2}, \end{aligned} \tag{6.50}$$

where $N_{1\rightarrow 0}$, $N_{1\rightarrow 0^*}$, N_0, $N_{0^*\rightarrow 0}$ and $N_{0^*\rightarrow 1}$ are the number of transitions $1 \rightarrow 0$ (full set), $1 \rightarrow 0^*$ (partial set), $0 \rightarrow 0$ (no transition during AND operation), $0^* \rightarrow 0$ (confirm) and $0^* \rightarrow 1$ (reset), respectively. The voltages V_+ and V_- are those appearing across the 2 serially-connected RRAM switches during AND and IMP operations, respectively, while t_P is the clock pulse-width. Each transition was assumed to take place in correspondence of $t_P/2$ for simplicity in Eq. (6.50). Fig. 6.19 shows the number of transitions in Eq. (6.50) as a function of the input states A, B and C_{in}, and the estimated energy consumption for a practical case, assuming t_P = 10 ns, $I_C = 2I_C^* = 10\ \mu$A, $V_+ = 1.3$ V and $|V_-| = 0.6$ V. This is the 'dynamic' energy consumption of the RRAM adder, while there is no static power component given the nonvolatile nature of RRAM switches. On the other hand, the static power consumption in a CMOS microprocessor might be even larger than the dynamic contribution [100]. These results suggest that, besides a smaller circuit area, RRAM logic may allow saving a significant power through the normally-off operation of non-volatile switches.

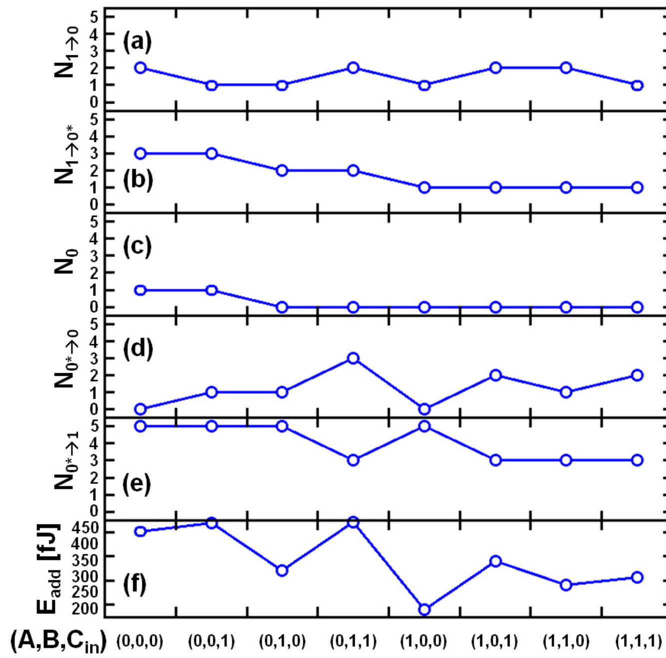

Figure 6.19: Number of transitions from 1 to 0 (a), from 1 to 0^* (b), from 0^* to 0 (c), from 0^* to 1 (d), number of no-transitions in the set state (e) and energy dissipation as a function of the input configuration (A,B,C_{in}). The total dissipated energy (f) is evaluated by Eq. (6.50).

Summary of results

A short summary of results and several concluding remarks are reported in the following.

Oxide based resistive switching memories represent a strong candidate for next generation solid state non-volatile memory technology. In particular, the extreme ease of fabrication, the relative low operating voltages and high write/erase speed suggest that this technology may became a valid alternative to Flash memories.

Starting from the concept of complementary switching, a concept recently proposed to solve the sneak-path in crossbar-array, an innovative multilevel scheme for oxide RRAM was developed. The new scheme relies on the storage of two different states for any resistance level, where the two states differ by the orientation of the CF. The defect concentration and orientation can be independently controlled by the current compliance and voltage polarity, respectively. Storage and discrimination of 8 states (*i.e.* , 3 bits) is demonstrated by experiments and numerical simulations. These results support the high functionality of nanoionics in storing and elaborating information in metal oxides.

The switching variability of the set state was characterized and two different models where provided, an analytical model, for the Poisson fluctuation of the defect number in the conductive filament and a Monte Carlo model, which describes the discrete injection of defects. Both models can capture the dependence of variability on the compliance current. It was also evidenced a new set-failure phenomenon induced by complementary switching. Set failure might be suppressed by accurate choice of the programming voltage, time and pulse shape, as well as by a careful RRAM stack engineering.

It was studied pulsed operation of oxide RRAM, showing that the reset pulse-amplitude V_{stop} controls resistance window and switching variability, the hight resistance state distribution improves for increasing V_{stop}, while low resistance state is degraded due to capacitive overshoot and incomplete set. Endurance failure at high V_{stop} is due to negative set, inducing a non switching state with low high resistance state preventing set transition. Changing the set/reset pulse-width causes a negligible change of maximum endurance, which is explained by an Arrhenius model of failure.

Starting from a detailed electrical characterization random telegraph noise (RTN) was studied. The random fluctuation between two levels is explained by the change of charge state in a bistable defect close to the CF. The model provides a physical quantitative description of both the electron transport in presence of a fluctuating defect

and the temperature-dependent switching kinetics. The model accounts for the size dependence of RTN amplitude, which is due to the partial or full depletion of carriers depending on the CF diameter, and for bias dependence of RTN switching.

It was demonstrated nonvolatile logic operation in RRAM through conditional switching in serially-connected devices. The RRAM state variable can be 0 (low-resistance set state) or 1 (high-resistance reset state). The state variable is used both as input or output of the logic operations. AND, IMP, NOT and transfer can be achieved in a single clock pulse, while OR, XOR and all other operations (*e.g.*, NAND and NOR) are achieved in multiple computation steps. The new nonvolatile logic approach allows to suppress the static leakage power dissipation, while reducing the area consumption thanks to the scalable 2-terminal structure of the RRAM switch. RRAM logic was studied also from the circuit viewpoint, discussing the implementation architecture, the select/unselect scheme to prevent disturb and the implementation of a 1-bit adder. Two architectures were considered, namely a 1T1R architecture, where RRAM in both the top and the bottom crossbar arrays are selected by a transistor, and a hybrid 1T1R-1R1R architecture, where only RRAM in the bottom crossbar requires a select transistor. Both architectures show a window of possible operating voltages for both AND and IMP operations hence for all other logic operations. Finally, a 1-bit adder is designed and demonstrated by experiments and simulations, allowing for a prediction of energy consumption. RRAM logic appears as a promising alternative to CMOS technology for area and energy scaling thanks to the reduced area and nonvolatile behavior of RRAM devices.

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Best Poster Award for the paper "Voltage-Dependent Random Telegraph Noise (RTN) in HfOx Resistive RAM" by S. Balatti, S. Ambrogio, A. Cubeta, A. Calderoni, N. Ramaswamy, D. Ielmini, presented by S. Balatti at IEEE International Reliability Physics Symposium, June 1-5, 2014

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