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Power converter cell design using IGCTs for HVDC and FACTS application

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FIGURE INDEX:

ABSTRACT

Electronic power converter is used to refer to a power electronic circuits that converts voltage and current from one from to another form. A switch mode power supply can be step down switch mode power supply (Buck converter), step up chopper (Boost converter), flyback converter and resonant converter. Either a IGBT, IGCT or power MOSFET is normally used in such a converter and this converter is called a switch mode power supply. For power electronic converter applications in general, there are many possibilities in using semiconductors as a switch. The switching mode power conversion gives high efficiency, but the disadvantage is that due to the nonlinearity of switches, harmonics are generated at both the supply and load sides. In this thesis we just consider the IGBT and the IGCT, due to the fact that these semiconductors have the most suitable characteristics for high power converter applications. Low on-state voltages and fast switching transients offer minimal semiconductor losses and the highest silicon utilization in medium voltage applications. Due to that IGCTs have a great potential for power systems converter applications. The following thesis gives at first a general view into IGCTs, shows advantages and disadvantages and compares the characteristics and performance of an IGCT with the ones of an IGBT. The existing IGCTs (asymmetric, conducting and reverse blocking) cover a huge range of application at medium voltage levels (medium voltage drives, static circuit breaker, DVRs, DUPS, SMES, BESS, etc.) with different conversion structures. Dual gate principle consists on the use of a second gate driver to control the IGCT gate-anode voltage (the base emitter voltage of the PNP equivalent in the thyristor type structure).

A part of the thesis consists in a PSPICE model implementation description. This has been performed in order to get a better view into the switching progresses, by using the basic converter cell with all parasitic elements and the influence of them. The effect of using a snubber system by a simulation platform has been then evaluated with a clamp circuit. The main parameter in the clamping circuit design is the characteristics of the derivative limiting inductor current, which may depend both on the converter topology and the modulation strategy. The clamping circuit designed for a full bridge converter with Bipolar and Unipolar modulation. In Bipolar modulation only two switching states are available and thus the converter is operated as a single phase two level voltage sources ($\pm V_{bus}$). Clamp current varies between $\pm I_{max}$ during each switching event, while semiconductor current only varies between I_{max} and zero (clamp current slope is twice the slope of the semiconductors). The Unipolar modulation is based on four available switching states and converter is operated single phase three level voltage source ($\pm V_{bus}$ and 0). The derivative limiting circuit also acts only in case of positive clamp current slope. Both, clamp and semiconductor current vary between I_{max} and 0 and with the same slope. A PSPICE and MATLAB model was implement for Bipolar and Unipolar switching technique.

An illustrated mechanical design of half bridge and full bridge converter was presented which consists of IGCTs, DC-link capacitor, clamping resistor and clamping inductor. In order to find the dimensioning factors of a Modular Multilevel Converter (MMC), an understanding of its basic operational principles is essentials. MMC converter consists of three phase (A,B,C), each phase has one upper arm and one lower arm connected in series between the dc terminals. The AC terminal was located at the midpoint between two arms. Each arm consists of one arm inductor and N number of series connected full bridge converter with dc capacitors. There are two loss calculation methods used in the literature. One is based on instantaneous

semiconductor or submodule current waveform where the semiconductor conduction and switching losses are derived from the current waveform. The other one is based on analytical equations of the semiconductor and submodule currents. The semiconductor losses are derived from the analytical current equations. The advantage of analytical loss calculation method is straightforward calculation without the need of specific converter modulation and control. In this thesis, the analytical loss calculation method for MMC High Voltage Direct Current (HVDC) converter with full-bridge module is used. The total losses in the converter comprise mainly of **switching losses**, **conduction losses** and **clamping loss** for IGCT full bridge converter**.** The diode turns on rapidly and hence the switching energy of the diode during turn-on can be neglected. But due to reverse recovery characteristics, the turn-off energy of the diode has to be considered.

Power semiconductor device such as IGBT/IGCT, both turn-on and turn-off was controlled and used to make self- commutated voltage source converters. The concept of modular multilevel converter topology based on the converters arm act as a controllable voltage source with a high number of possible discrete voltage steps which allows forming an approximate sine wave in terms of adjustable magnitude of the voltage to the AC terminal. Model and simulation of MMC was performed. The purpose of the simulation was to predict the dynamic response of the modular multilevel converter during normal and fault conditions. The MMC model was built using Simulink/SimPowerSystem Toolbox. The converter Pulse Width Modulation (PWM) modulation and control are implemented using standard Simulink blocks The Matlab S-funtion are used for programming the capacitor voltage balancing control algorithm which generate the actual IGCT switching signal for the submodules of the converter main circuits in the SimPowerSystem. A level- shifted sinusoidal pulse width strategy is used for the modulation of MMC. Level shifted PWM technique requires twelve carrier waves displaced symmetrically with respect to zero-axis.

CHAPTER 1

INTRODUCTION

1.1 Transmission System

New power system transmission infrastructures will require substantially higher capacity than today and higher reliability for massive fluctuation to incorporate renewable energy sources. A solution based on upgrading of the existing High Voltage Alternating Current (HVAC) grid is challenging in densely populated areas because of public opposition, narrow transmission corridors and limited availability of right of way (ROW). High power electronic converters find their use to control load flow, to reduce transmission losses and to avoid congestion, loop flows and voltage problems.

High Voltage Direct Current (HVDC) systems and Flexible Alternative Current Transmission System (FACTS) provide essential supports to avoid various AC system related problems and concerns in the power systems. They can increase the transmission capacity and system stability in a very efficient way and assist in prevention of cascaded disturbances. HVDC and FACTS installation provides economic solution for special transmission application. HVDC is well-suited for long-distance, bulk-power transmission, long submarine cable crossings and asynchronous interconnections. In earlier 1970s, HVDC systems used only line-commutated solid state devices, in most cases, thyristor valves. FACTS based on VSV concept has been the first VSC application for power transmission system. While VSC applications may have different topologies, the first converters realized with VSC HVDC applications had been based all on 2-3 level technology. This concept enables to switch respectively two or three different voltage levels at the AC terminals of the converter.

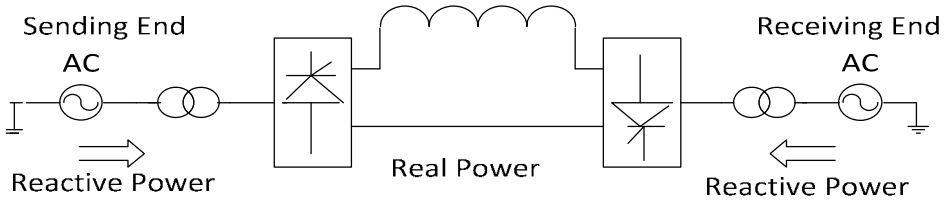


Fig: 1.1 LCC thyristor based HVDC system

HVDC using thyristor valves are known as line-commutated converters (LCC) **fig: 1.1** HVDC. ABB uses HVDC Classic as trademark name for LCC HVDC. LCC HVDC can transmit high volume of power up to 8 GW with a state-of-the-art ultra-high DC voltage of +/- 800kV. It provides high efficiency with converter station loss of only 0.8%. However, LCC HVDC does not well suit for meshed DC grid connection as the voltage must be reversed if the direction of power is reversed. LCC HVDC also needs reactive power compensation for the connected AC systems which are normally provided by HVDC passive filters. When connecting to weak AC systems, LCC HVDC may experience communication failure during power system fault conditions.

1.2 Converter System

Power electronics is the study of switching electronic circuits in order to control the flow of electrical energy. Power electronics is the technology behind switching power supplies, power converters, ower inverter, motor drives and motor soft starters. Power electronics has appliactions that span the whole field of electrical power systems, with the power range of these applications extending from a few VA/Watts to several MVA/MW. Electronic power converter is the term that used to refer to a power electronic circuits that converters voltage and current from one from to another form. These converters can be classified as:

- AC to DC converter (Rectification) – An AC to DC converter circuit can convert AC voltage into a DC voltage. The DC output voltage can be controlled by varying the firing angle of the thyristors. The AC input voltage could be a single phase or three phase. Rectifiers can be classified as uncontrolled and controlled rectifiers, and the controlled rectifiers can be further divided into semi controlled and full controlled rectifiers. Uncontrolled rectifier circuits are built with diodes, and fully controlled rectifier circuit are built with SCRs. Both diodes and SCRs are used in semi controlled rectifier circuits. There are many applications for rectifiers as in variable speed DC drives, battery charges, and DC power supplies and power supply for a specific application like electroplating.
- DC to AC converter (Inverter) — The converter that changes a DC voltage to an alternative voltage, AC is called an inverter. Earlier inventers were built with SCRs. Since the circuit required turning the SCR off tends to be complex, other power semiconductor devices such as bipolar junction transistor (BJT), power MOSFESTs, insulated gate bipolar transistor (IGBT), and insulated gate – commutated thyristor (IGCT) are used today. There are many inverter circuits and the techniques for controlling an inverter vary in complexity. Some of the applications of an inverter are emergency lighting systems, AC variable speed drives, uninterrupted power supplies and frequency converters.
- DC to DC converter (Chopper) -- These converters can convert a fixed DC input voltage into variable DC voltage or vice versa. The DC output voltage is controlled by varying of duty cycle. When the SCR came into use , a DC to DC converter circuit was called a chopper. Nowadays, an SCR is rarely used in a DC to DC converter. Either a IGBT, IGCT or power MOSFET is normally used in such a converter and this converter is called a switch mode power supply. A switch mode power supply can be step down switch mode power supply (Buck converter), step up chopper (Boost converter), flyback converter and resonant converter. The typical applications for a switch mode power supply or a chopper are DC drive, battery charger and DC power supply.
- AC to AC converter (Cycloconverter) — A convertor that changes an AC supply to the AC supply with alternative voltage, frequency, phase or shape is called an AC to AC converter. These converters can convert from a fixed AC voltage into variable AC output voltage. The output voltage is controlled by varying firing angle of TRIAC. These type converters are known as AC voltage regulator. A cyccloconvertor or a Matrix converter converts an AC voltage. The amplitude and the frequency of input voltage to a cycloconverter tend to be fixed values, whereas both the amplitude and the frequency of output voltage of a cycloconverter tend to be variable specially in adjustable speed drivers (ASD)

1.3 Switching Techniques

In electrical engineering, a switch is an electrical component that can break an electrical circuit, interrupting the current or diverting it from one conductor to another. The most familiar form of switch is manually operated electromechanical device with one or more sets of electrical contacts, which are connected to external circuits. Each set of contacts can be in one of two stated : either 'closed' meaning the contacts are touching and electricity can flow between them, or 'open ' meaning the contacts are separated and the switch is no conducting. Make a flexible power electronic switch-mode converter for general usage; it can operate as a half bridge, full bridge or three-phase converter in four quadrants, leading to a wide range of usage: DC-DC converter, DC-AC converter single phase or three phase inverter, in a DC or AC motor drive. The most basic concept of a switch mode power converter is the bi-positional switch and pulse width modulation (PWM) switch. **Fig 1.2** shows different power electronics switch with respect to their power rating.

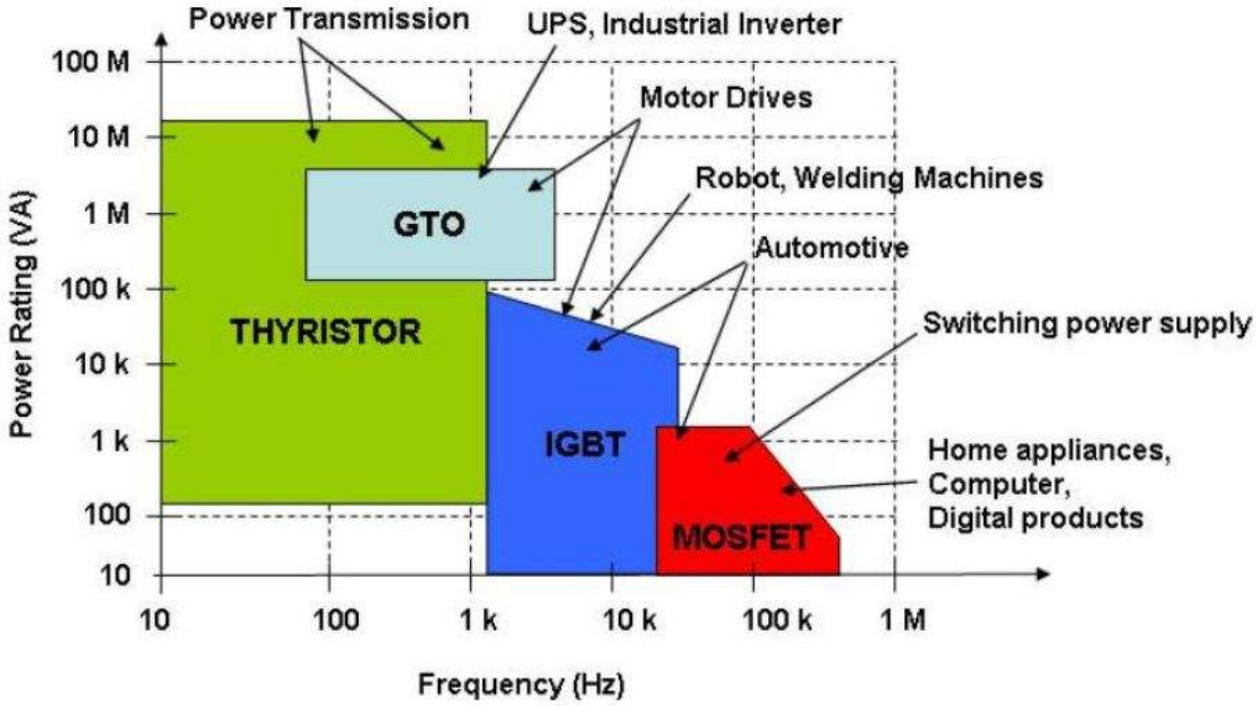


Fig: 1.2 switching power rating for power electronics

1.4 Purpose of Thesis

The thesis focuses on high power converter submodule / cell design of multilevel converters for HVDC and FACTS applications. The basic building blocks for the multilevel converters are Half Bridge (HB) and Full Bridge (FB) submodules. The semiconductors used in the high power converter submodules are Integrated Gate Bipolar Transistor (IGBTs) or Integrated Gate Commutated Thyristor (IGCTs). A first contribution of this thesis is the analysis of the IGCT switching characteristics including turn-off overvoltage, turn-on over-current, clamp circuit, derived semiconductor current for converter applications and IGBT and IGCT

converter loss calculations by analytical method. A second contribution is the simulation of Modular Multilevel Converter (MMC) for half bridge with IGCT also part of thesis.

1.5 Work Place at ABB

Completing my master's thesis I got chance in ABB- Vasteras,Sweden Corporate Research Center(CRCSE) for nine month. This thesis evaluates the potential application of IGCTs for Voltage Source Converter (VSC) HVDC applications based on modular multilevel converters. The reference semiconductor component is a ABB StakPak IGBT 5SNA200045K0301. As alternate components, a ABB HiPak IGBT 5SNA 1200G450300 and Asymmetric IGCT 5SHY 55L4500 are used, which are all available in the ABB portfolio. The IGCT converter cell designs for MMC HVDC application are performed in the thesis.

1.6 Definitions

IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
HVDC	High Voltage Direct Current
FACTS	Flexible Alternative Current System
SOA	Safe Operating Area
VSC	Voltage Source Converter
MMC	Module Multilevel Converter

1.7 Structure

This thesis has the following structure.

Section 1 describes the purpose and scope for this report as well as terms, abbreviations and acronyms which are used.

Section 2 gives a comparison of semiconductor characteristics of IGBTs and IGCTs.

Section 3 describes the design requirement and actual designs of IGCT for use in half- and full-bridge cells.

Section 4 summarizes the IGCT design work and presents the contribution of the thesis.

Section 5 proposes the future work of IGCT converter cells application.

1.8 History of Semiconductor

Power semiconductor devices constitute the heart of modern power electronic apparatus. There is no doubt that semiconductors changed the world and will continue to be the key technology for enabling integration of renewable energy sources to make a better green world. Power electronic converters in the form of a matrix of on-off switches are used to

convert power from ac-to-dc (rectifier), dc-to-dc (chopper), dc-to-ac (inverter), and ac-to-ac at the same (ac controller) or different frequencies (cycloconverter). The switching mode power conversion gives high efficiency, but the disadvantage is that due to the nonlinearity of switches, harmonics are generated at both the supply and load sides. The switches are not ideal, and they have conduction and turn-on and turn-off switching losses. The power electronics converter technology has experienced fast developments during the past 20 years that high power semiconductor switches and novel multilevel converter topology converters have been invented to solve these issues. The advances in power electronic converters have been revolutionized various applications such as heating and lighting controls, ac and dc power supplies, electrochemical processes, dc and ac motor drives, static VAR generation, high voltage DC transmission, etc.

For power electronic converter applications in general, there are many possibilities in using semiconductors as a switch. In this thesis we just consider the IGBT and the IGCT, due to the fact that these semiconductors have the most suitable characteristics for high power converter applications. Today's power semiconductor devices are almost exclusively based on silicon material and can be classified as follows:

- Diode
- Thyristor or silicon-controlled rectifier (SCR)
- Triac
- Gate turn-off thyristor (GTO)
- Bipolar junction transistor (BJT or BPT)
- Power MOSFET
- Static induction transistor (SIT)
- Insulated gate bipolar transistor (IGBT)
- MOS-controlled thyristor (MCT)
- **Integrated gate-commutated thyristor (IGCT)**

1.9 HVDC System

Forced-commutated Voltage Source converters (VSC) HVDC systems using IGBT (Insulated Gate Bipolar Transistors) were first introduced to the market by ABB since the late 1990's with the trademark name HVDC Light (**fig 1.3)**. The VSC HVDC systems can change power flow through the reversal of current direction rather than voltage polarity which makes DC grid connection straightforward. They can provide reactive power support without using AC filters. The VSC HVDC transmissions based on two- and three-level VSC HVDC systems were introduced. In the late 2010's, modular multilevel converter (MMC) VSC (**fig 1.4**) topology were introduced which further reduces converter harmonics and converter losses. Now the state-of-the-art MMC VSC HVDC converter has a typical station loss of 1% which is very close to that of the HVDC Classic. Other advantages of MMC VSC converters include improved reliability and availability and reduced the converter cost.

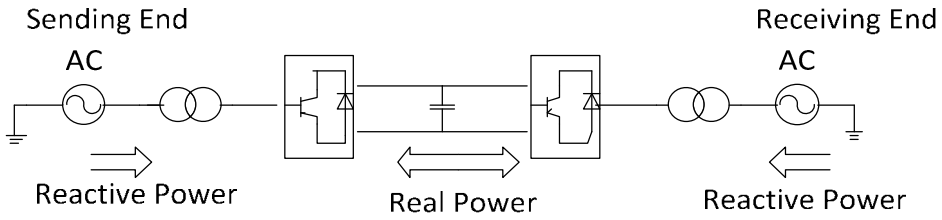


Fig: 1.3 VSC based HVDC system with IGBTs

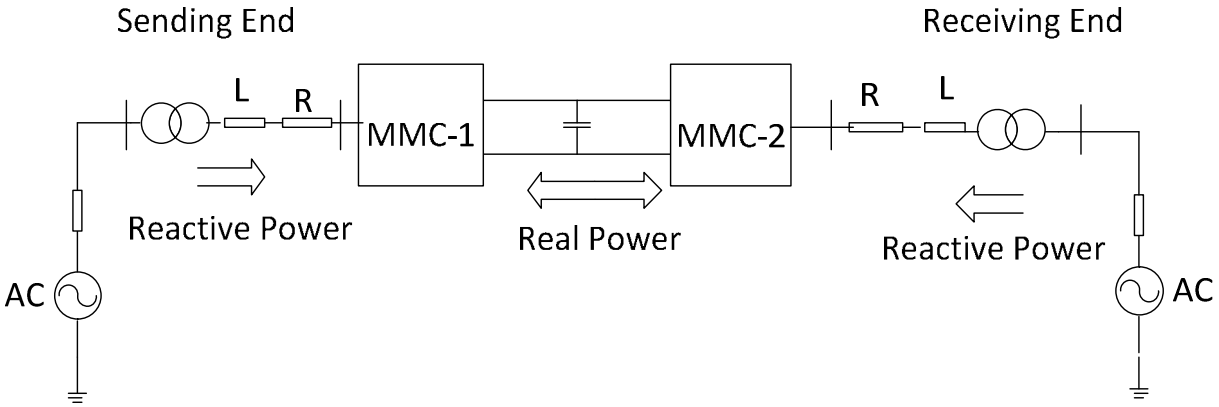


Fig: 1.4 VSC based MMC HVDC system with IGBT/IGCT

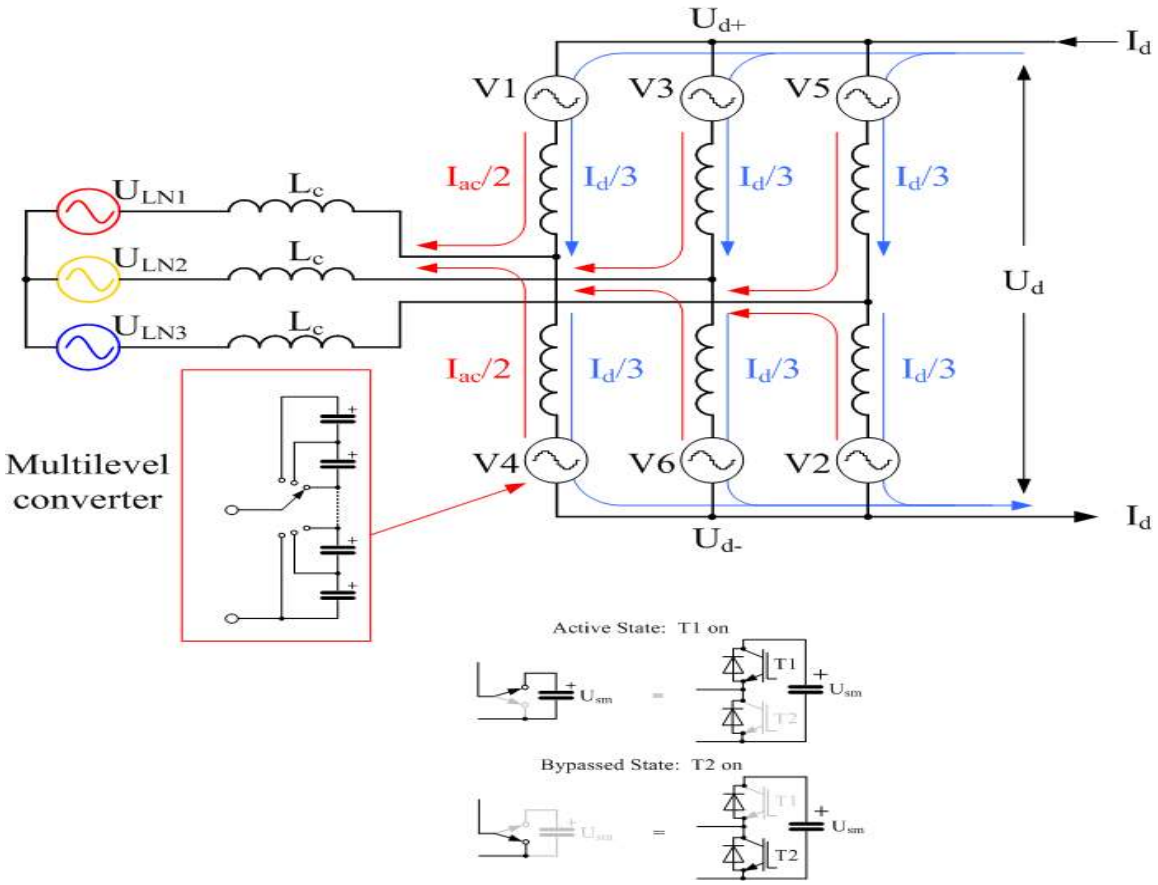


Fig: 1.5 MMC HVDC Converters

VSC based MMC (Modular Multilevel Converter) HVDC converter (**fig 1.5**) arm acts as a controllable voltage source with a high number of possible discrete voltage steps which allow forming an approximate sine wave in terms of adjustable magnitude of the voltage to the AC terminal. HVDC converter consists of freely chosen number of identical submodules. In principle a converter arm, which consist of many submodules, represents a voltage source converter. A voltage source converter which is able to control the AC- voltages (multilevel) and the DC-side voltage (Vd) fast and simultaneously via the switching states of the submodules.

CHAPTER 2

Semiconductor Device

2.1 IGBT (Insulated Gate Bipolar Transistor)

MOSFET and Bipolar junction transistor compose the main IGBT structure (**fig 2.1**), which leads to a high speed, voltage controlled device with low on-state voltage and low switching loss or energy. IGBT is a minority-carrier device with high input impedance and large bipolar current-carrying capability .Tail current at turn off (Bipolar) and sensitivity to electrostatic charges (MOS) are the drawbacks for that kind of device technology.

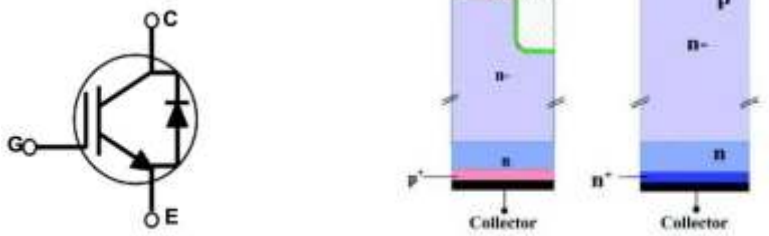


Fig:2.1 IGBT cross sectional diagram

An IGBT has a significantly lower forward voltage drop compared to a conventional MOSFET in higher blocking voltage devices. As the blocking voltage rating of both MOSFET and IGBT devices increases, the depth of the n-drift region must increase and the doping must decrease, resulting in roughly square relationship decrease in forward condition versus blocking voltage capability of the device. To inject minority carrier (holes) from the collector p+ region into the n-drift region during forward conduction, the resistance of the n-drift region during forward conduction, the resistance of the n-drift region is considerably reduced.

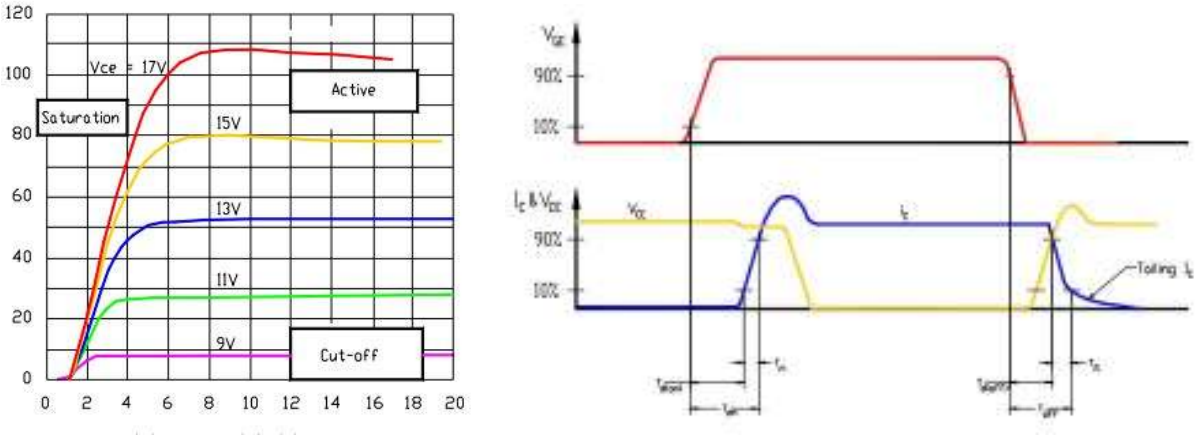


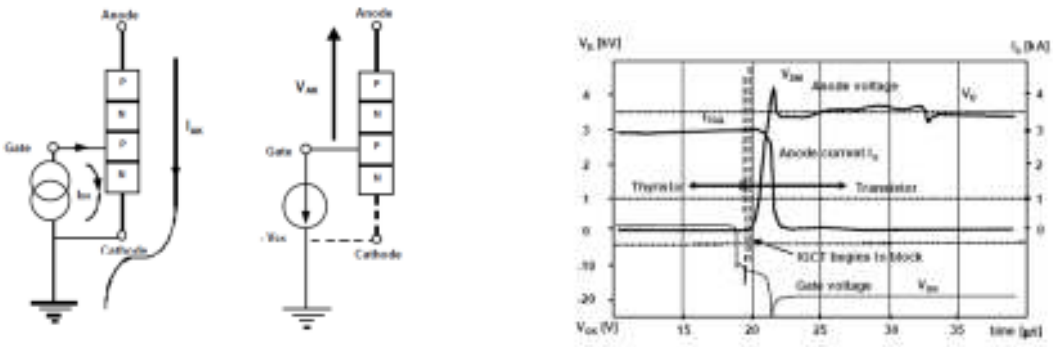
Fig:2.2 IGBT I-V characteristic & current and voltage turn-On & turn-off waveform [14]

Transistor has reverse current flow. This means that unlike a MOSFET, IGBTs cannot conduct in the reverse direction. This reverse current flow is needed an additional diode (called a freewheeling diode) is placed in parallel with the IGBT to conduct current in the opposite direction (**fig 2.2**). Problem of using diode is not severe, because at the higher voltages where IGBT usage dominates. Diodes are significantly higher performance as the body diode of a MOSFET.

Reverse bias rating of the N-drift region to collector P+ diode is usually few volts. A additional series diode is using when the circuit application applies a reverse voltage to the IGBT. The minority carriers injected into the N-drift region take time to enter and exit or recombine at turn on and turn off. These results in longer switching time and hence higher switching loss compared to a power MOSFET.

2.2 Introducing the IGCT (Integrated Gate Commutated Thyristor)

IGCT is a four-layer thyristor structure **(fig 2.3a)** device similar to a Gate Turn-off Thyristor (GTO). It is mounted into its gate driving unit which results in an extremely low inductance coupling between semiconductor and gate-unit. This low inductance connection allows the thyristor or GCT to be turned off with unity gain via a low voltage source (20V **fig 2.3b**). the vertical structure of the GCT, through derived from the GTO, has benefited from high voltage IGBT developments and incorporates such loss reduction techniques as the buffer layer and the transparent emitter. These techniques lead to thinner wafer design than was possible for GTOs which further allows the monolithic integration of an anti-parallel diode onto the same wafer for revered conduction, which was not optimally feasible with GTOs . the result is a switch which behaves like an IGBT at turn-off (open-base pnp transistor) and generates the same turn-off losses. In conduction however, the IGCT is a thyristor and as such it generate substantially lower losses than an IGBT. This is due to the fact that a thyristor operates at much higher charge density than a transistor due to charge injection from its two emitters (pnp and npn transistors). The design of the IGCT gate-unit allows a short but high value of turn-on gate current (typically 5times higher than in GTO) which drives on GCT as an npn transistor (short delay time, monotonic voltage collapse, negligible losses). Thus the IGCT is a thyristor in conduction, a pnp transistor at turn-off and during blocking and an npn transistor at turn-on. Like the transistor, the IGCT requires no dv/dt limitation at turn-off but unlike the transistor (**fig 2.3c**), it is not possible to control neither turn-on nor turn-off speed.



a) b) c)

Fig. 2.3 a) Conducting (Thyristor) b) Blocking (Transistor)
c) IGCT turn-off like a transistor [12]

The rate of change of the drive is critical for the operation of the GCT. The anode current has to be turned off in less than 1us otherwise the device comes into the unstable part of the characteristics. The voltage needed results for a given inductance of the gate circuit, respectively the inductance for a given gate voltage. In the other hand, a simple, reliable and cost effective drive unit is only possible at low voltages. An ideal voltage for 3.3kA IGCT (**fig 2.4**) is 20V because of the gate can withstands, this voltage after turn-off. The permissible leakage inductance of interrupting 3kA is 6nH or less [13].

Fig 2.4: IGCT [14]

The Integrated Gate Commutated Thyristor (IGCT) has become the power semiconductor of choice in medium voltage industrial application, also in energy management and the traction markets. IGCTs have many advantages not only on the silicon wafer itself, but in the way it is driven by the integrated gate drive. The 'hard-drive' concept at the heart of IGCT operation requires the mechanical integration of gate driver and semiconductor into one single unit with low circuit inductors. It also implies a number of new converter features, which makes IGCT converters different from GTO or IGBT converters.

IGCT or GCT refers to the gate commutated thyristor with press-pack semiconductor package. Further distinctions can be made to distinguish RC-IGCTs (reverse-conducting), RB-IGCTs (reverse blocking) and AS-IGCTs (asymmetric with neither reverse blocking nor reverse- conducting capability) (**fig 2.5**). ABB sells only IGCTs whereas other manufactures may offer the GCT and gate-unit separately. The term 'SGCT' is also used some suppliers to designate a 'symmetric blocking' device, known here as RB-IGCT per the above definition.

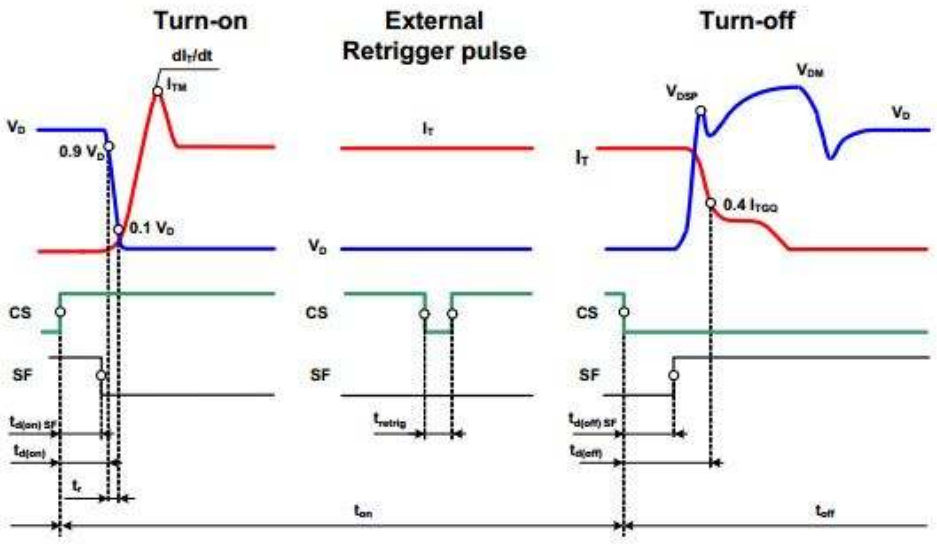


Fig. 2.5: IGCT I-V characteristic & current and voltage turn-On & turn-off waveform [15]

IGCT is characterized by a high current capability and low on-state voltages. In the beginning of turn-off, the gate-cathode junction is reverse-biased and the cathode emitter is turned off before the voltage at the main blocking junction rises, resulting in an extremely fast commutation of the cathode current to the gate.

2.3 VSC Based HVDC Converter Topology

Converters with the capability to synthesize voltage waveforms with more than three levels are called multilevel converter. Increasing number of voltage levels in the converter station, the size of the voltage steps is shorten and the voltage gradients are minimized, reducing significantly the harmonic content of the output voltage and therefore the size of the bulky passive AC filters. Usually their energy is stored in a set of series connected capacitors with the same voltage. The interest over multilevel converters in high power and high voltage applications has grown due to the low voltage distortion on the AC line, introduced by these converters. When the number of levels increases, the synthesized output voltage is a staircase wave with more steps, which approaches more accurately a sinusoidal waveform.

Several multilevel topologies have been proposed in the literature: Diode-Clamped Multilevel converter (DCMC), Flying-Capacitor Multilevel converter (FCMC) and Module Multilevel Converters (MMC). The MMC (**fig 2.6**) topology has been suggested 2003 by A. Marquardt and A. Lesincar [16]. It consist of the six arms, each connecting one AC terminal to one DC terminal, where each arm consisting of a large number of IGBT/IGCT converter submodules or converter cell. In submodules, half bridge or full bridge consists of two or four IGBTs connected in series across the capacitor, with the midpoint connection and one of the two capacitors terminal brought out as external connections.
Depending on which of the two IGBTs / IGCTs in each submodule is turned on, the capacitor is either bypassed or inserted into the circuit. Each submodule therefore acts as an independent two-level converter generating a voltage of either 0 or V_{cap} (where V_{cap} is the submodule capacitor voltage). With a suitable number of submodules connected in series, the arm can synthesize a stepped voltage waveform that approximates very closely to a sine-

wave and contains very low levels of harmonic distortion. Therefore, each arms of a MMC is a separate controllable voltage source.

The MMC differs from other types of converter in that current flows continuously in all six arms of the converter throughout the mains-frequency cycle. As a result, concepts such as "on-state" and "off-state" have no meaning in the MMC. The direct current splits equally into the three phases and the alternating current splits equally into the upper and lower arm of each phase.

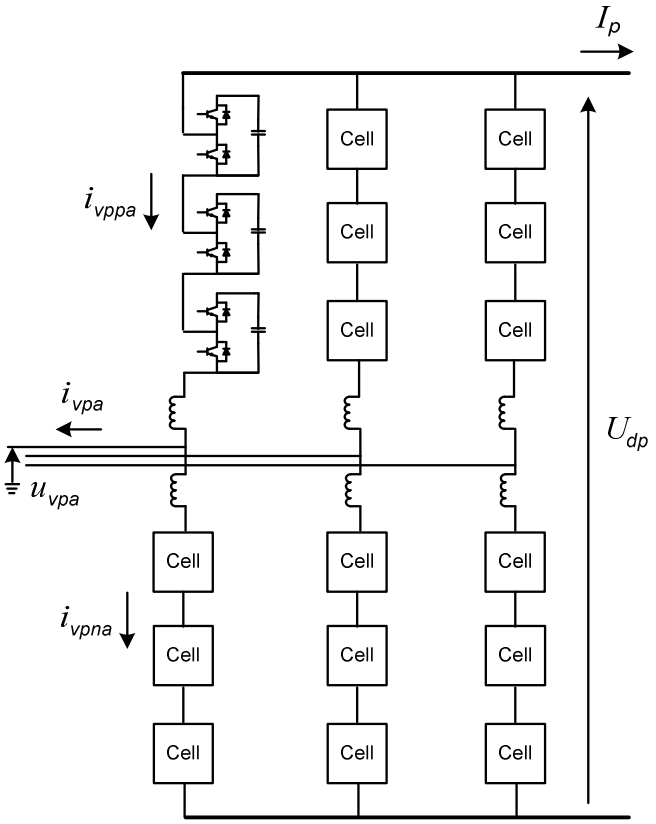


Fig. 2.6: MMC converter for HVDC application

2.4 Half and Full Bridge Converter Submodules Using IGCT

The basic converter cells using IGCT semiconductors for MMC HVDC application are shown in Fig. 2.6 . The half-bridge (**fig 2.7**) submodules are normally used for MMC converter to synthesize sinusoidal output AC voltages with low converter loss. The full-bridge submodule can also be used in MMC converter for DC side pole to pole and pole to ground fault blocking since it can provide reverse voltage during DC faults. However, the converter loss with full-bridge (**fig 2.7**) cells is much higher compared with the half-bridge version.

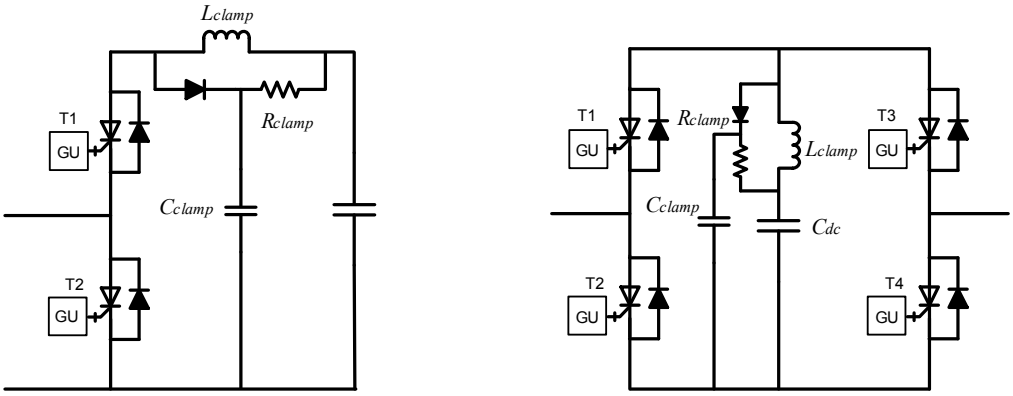


Fig:2.7 Half- and Full-Bridge Converter with IGCT with clamp circuit

IGCT has great potential for MMC HVDC application due to its lower on-state loss compared with IGBT. However, its main disadvantage of the use of IGCTs is the clamp circuit, which is always needed to limit the $\frac{\partial i}{\partial t}$ at the free-wheeling diode turn off and the IGCT turn-off overvoltage. The diode turn-off is caused by an IGCT turn-on and the diode's turn-off $\frac{\partial i}{\partial t}$ capability is, in most cases, lower than the turn-on $\frac{\partial i}{\partial t}$ capability of the IGCT. This is especially true in common applications without a turn-off clamp. Hence a $\frac{\partial i}{\partial t}$ limiting choke L_L must be large enough to allow operation within the $\frac{\partial i}{\partial t}$ range of the diode even at the highest DC link voltage. The $\frac{\partial i}{\partial t}$ limiting inductor is dimensioned to limit the current derivative to the maximum allowed value specified in the datasheet, at the maximum DC voltage at which the cell will be operated [5]. Typical values for ABB diodes are between 200 and 1000 A/µs depending on diode wafer size and switching voltage.

Compared with conventional GTO snubber circuit, the dV/dt snubber capacitors are not needed for the IGCTs. Furthermore, due to the very low storage and fall times, the minimum on and off time can be reduced below 10µs. The turn-on characteristic by hard positive gate drive of the device is also improved and only the IGCT associated freewheeling diode is subject to turn-on di/dt (**fig 2.8**) limitations. Due to its thyristor nature, the GCT cannot provide such a di/dt control. Instead, di/dt control must be provided by means of an external inductor, which also requires a small low inductance clamp circuit (RCD circuit) for over-voltage limitation at IGCTs turn-off. Clamp circuit required to limit di/dt at turn-on (diode turn-off di/dt limitation) and over-voltage at turn off.

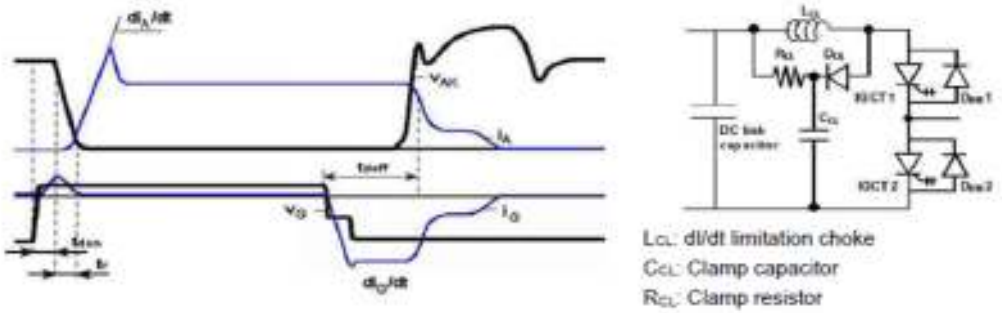


Fig:2.8 IGCT characteristic waveform and clamp circuit for freewheeling diode di/dt turn-off limitation [1]

2.4.1 Inductor current & Clamp Circuit design for Converter

The purpose of using the clamping circuit (**fig 2.9**) is to limit the di/dt of the diode turn-off current and the turn-off overvoltage of the IGCT. There are plenty of literatures in which the clamp circuit and parameter sizing are discussed. Some methodologies have been used in the thesis and summarized below. In all of them, the proper size of the clamping inductor is calculated according to the following expression:

$$L = \frac{V_{BUSmax}}{di/dt_{max}}$$

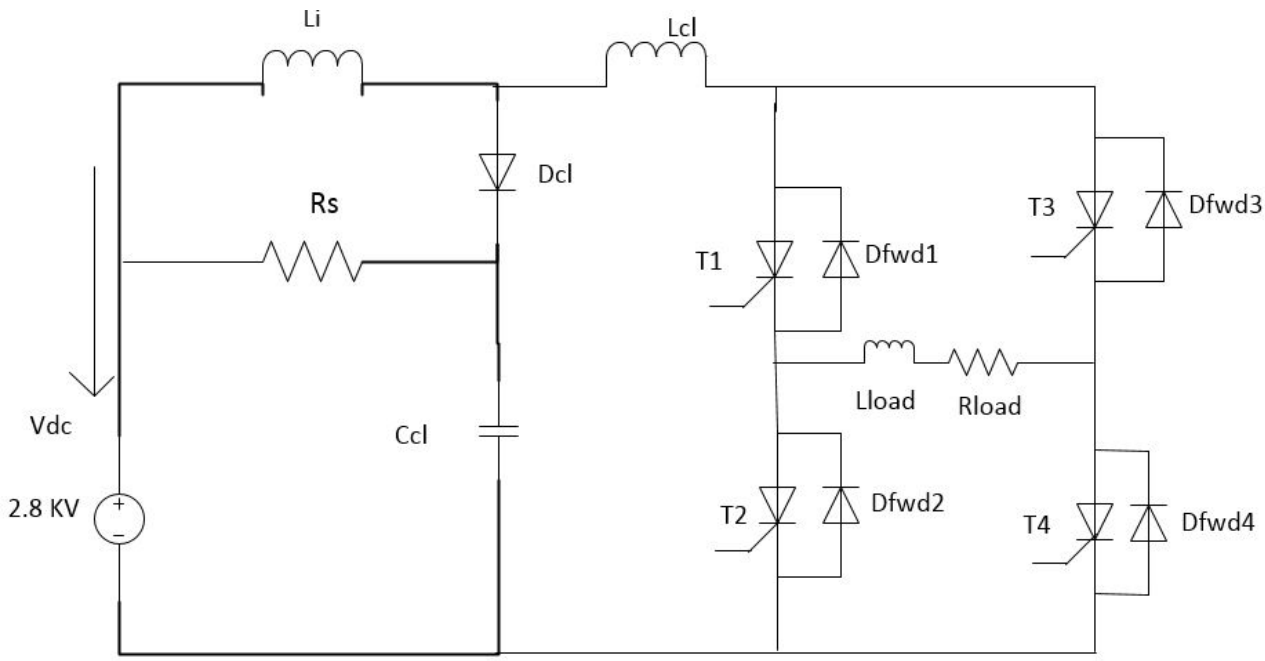


Fig: 2.9 Full bridge IGCT with clamp components

Concerning the RCD clamping components design, two main methods can be used as follows:

Iterative method based on simulations: Using an equivalent circuit for considering the switching events occurring in a VSC converter circuit (2 or 3-level topologies), and ideal switching elements. The values of *L*, *C* and *R* given in the "conditions" column of the IGCT datasheet are used as a starting point for the design, and they are then iteratively adjusted to meet the previously mentioned design criteria (using estimated values of stray inductances).

Analytical expression based method derived from the differential equations that describe the current limiting and clamping circuit:

$$\Delta V_c'' + \frac{1}{RC} Vc' + \frac{1}{LC} Vc = 0 \quad (1)$$

$$I_c'' + \frac{1}{RC} Ic' + \frac{1}{LC} Ic = 0 \quad (2)$$

By solving these equations, expressions for the maximum achieved voltage ($\Delta Vmax$) and the clamp current cancellation time (Tb) can be obtained.

$$T_b = \frac{1}{\beta}\left[\pi - \tan^{-1}\left(\frac{\beta}{\alpha}\right)\right] \quad (3)$$

$$\Delta V_{max} = \frac{I\circ}{C\omega\circ} e^{-\frac{\alpha}{\beta}\tan^{-1}\left(\frac{\beta}{\alpha}\right)} \quad (4)$$

With $\alpha = \frac{1}{2RC}$ $\omega\circ = \frac{1}{\sqrt{LC}}$ $\beta = \sqrt{\omega^2\circ - \alpha^2}$

A graphical method is proposed for solving equation. 3 and 4 and calculating the optimal set of *R*, *L* and *C* values that permit to fulfill the clamp circuit design criteria. In other papers some simplified expressions are proposed in order to calculate these parameters using some empirical coefficients in **fig 2.10 and 2.11**

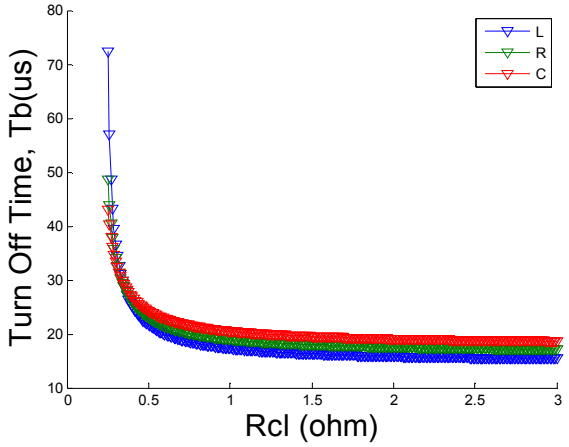


Fig:2.10 Current cancellation time Tb vs Rcl

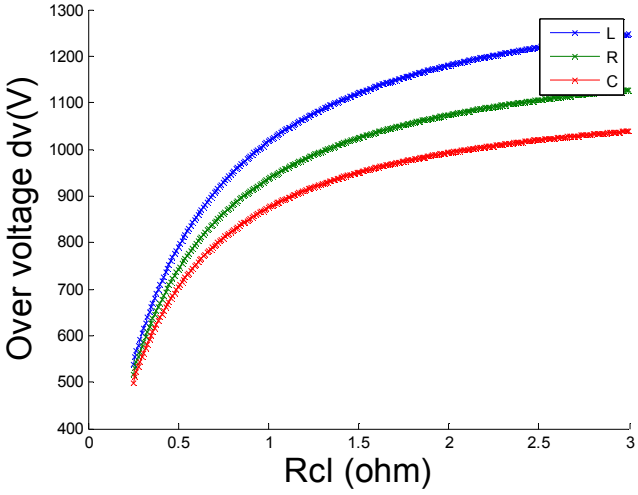


Fig: 2.11 Overvoltage for various clamping parameters values

The main parameter to be considered in the clamping circuit design is the characteristics of the semiconductor switching modes which may depend both on the converter topology and the chosen modulation strategy. In this section the clamping circuit design will be analyzed for a full bridge converter with bipolar and unipolar mode modulation. The bipolar switching mode is defined in a way that the output of the full-bridge converter voltage is from Vdc to –Vdc or from –Vdc to Vdc. The unipolar switching mode is defined such that the output voltage of the full-bridge converter is from Vdc to 0 or from 0 to –Vdc and vice versa.

2.5 Bipolar Switching for Full Bridge Converter Submodule

With this modulation only two switching states are available, and thus the converter is operated as a single phase 2-level voltage sources (± *Vbus*). One example bipolar switching operations is that the IGCT switches (**fig 2.12**) T2 and T3 are turned on while the IGCT switches T1 and T4 are turned off. The converter current is commutated from the IGCTs T1 and T4 to the antiparallel diodes D2 and D3.

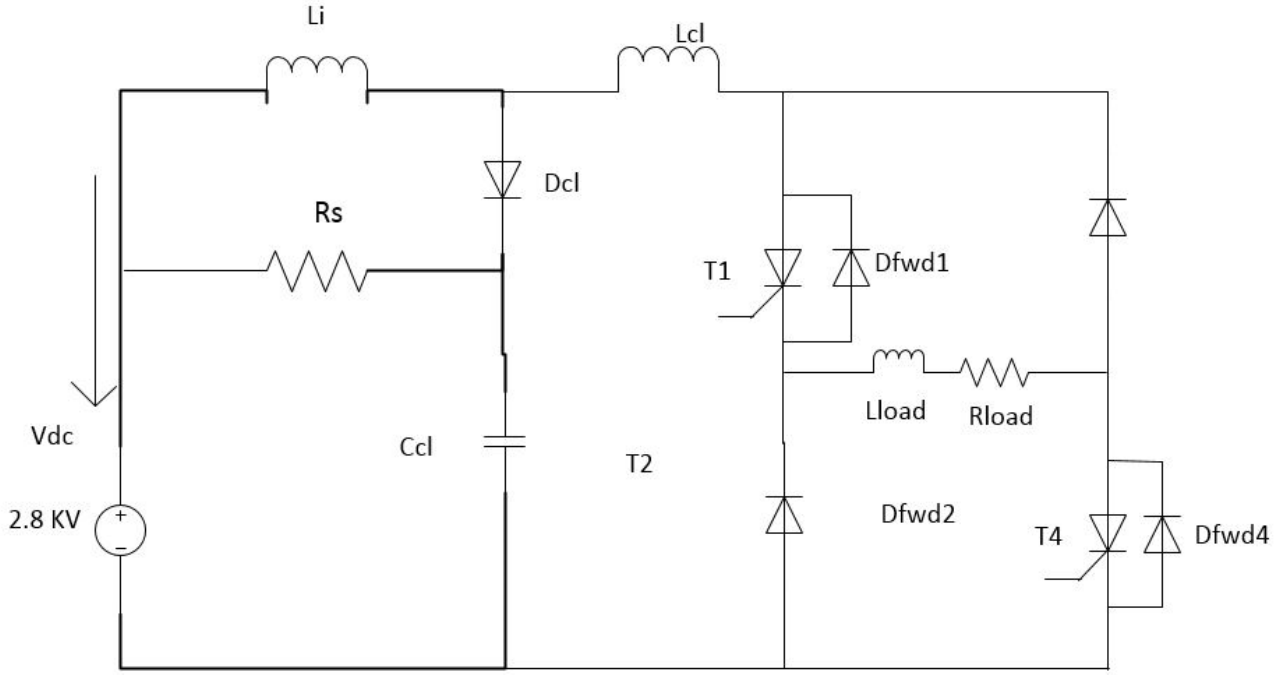


Fig: 2.12 Bipolar modulation (case 1) mode

2.5.1 Dimensioning of the data of Li

The stray inductance L_i(4.41µH) is the combination of L_{i1}+ L_{i2} = 4.36µH+50nH. This inductance has to limit the $\frac{\partial i}{\partial t}$in the clamp circuit, thus avoiding the destruction of the diode. Fig 2.15 shows the whole cell including the clamp, like it is shown in the datasheets of IGCTs. The maximum decay rate of on-state current defines the minimum value of (L_{i1}+ L_{cl}) according to:

$$(L_i + L_{CL}) = \frac{V_{DClink}}{\frac{\partial i}{\partial t}}$$

Where

- V_{DClink} is the voltage drop across (L_i + L_{CL}) during turn-off of the diode;
- L_i is the $\frac{\partial i}{\partial t}$ limiting inductance, which is normally divided in two parts:

  L_{i1}: clamping inductor to achieve the required $\frac{\partial i}{\partial t}$

  L_{i2}: stray inductance of the DC-link capacitor; this part is not damped by R_s and therefore strongly contributes to the voltage overshoot V_{dm} should be minimized.
- L_{CL}(0.3µH) is the inductance of the clamp circuit. Should be minimized.
- R_S(0.35Ω) is the damping resistor, L_s(50nH) is the stray inductance are used to dissipate the clamp circuit energy;
- C_{CL}(20µF) is the capacitor, used to clamp the IGCT over-voltage; it also initially absorbs some of the energy stored in the $\frac{\partial i}{\partial t}$;
- $R_{load} = 0.933\Omega$ L_{load} = 0.1mH.
- D_{CL} is the clamp diode, should have a small forward recovery V_{FR}.

2.5.2 Detailed View in Pspice & Matlab simulation

Bipolar switching for full bridge converter submodel simulations (**fig 2.13 & 2.14**) were developed by using a voltage controlled switch (V_2), with a turn-on and turn-off resistance. Model IGCT V Switch $\mathbf{R_{on}= 10e^{-3}}$, $\mathbf{R_{off=}\ 1e^{4}}$, $\mathbf{V_{on=}\ 0.1V}$, $\mathbf{V_{off=}0.0V}$ but disregarded the parameters of the gate signal, which are given by the datasheet.

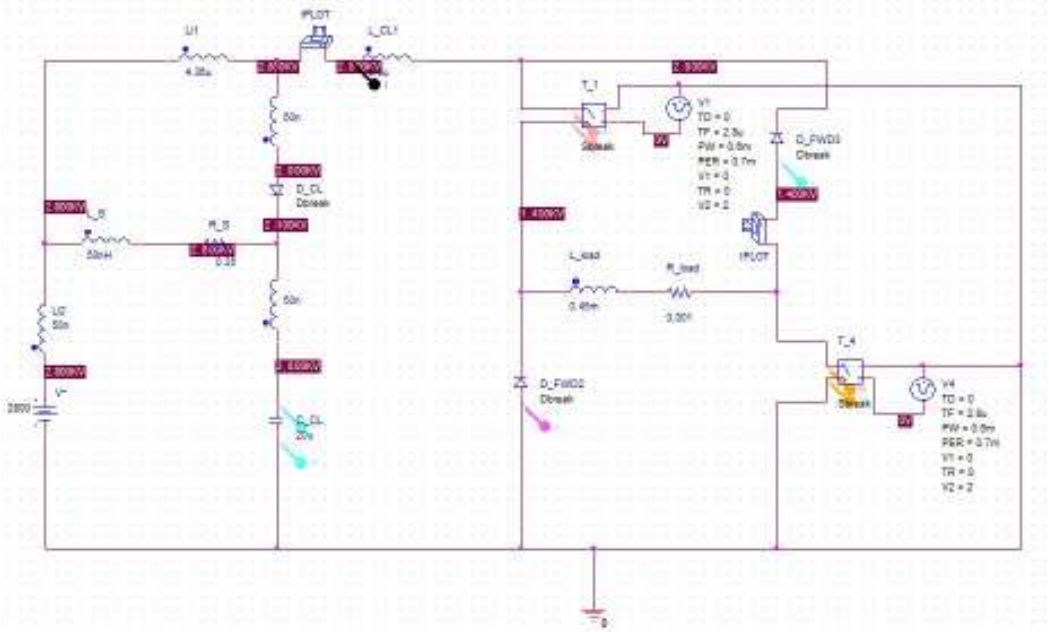


Fig: 2.13 Bipolar modulation Pspice model

- ✓ **TD (Time delay) = 0s TF (Fall time) = 2.8µS TR (Rise time)= 0s**

- ✓ **PW(Pulse Width) = 0.6mS PER (Period) = 1.2m V1 = 0V V2=0V**
- ✓ **Run time = 1.2mS Step Size = 1µS**

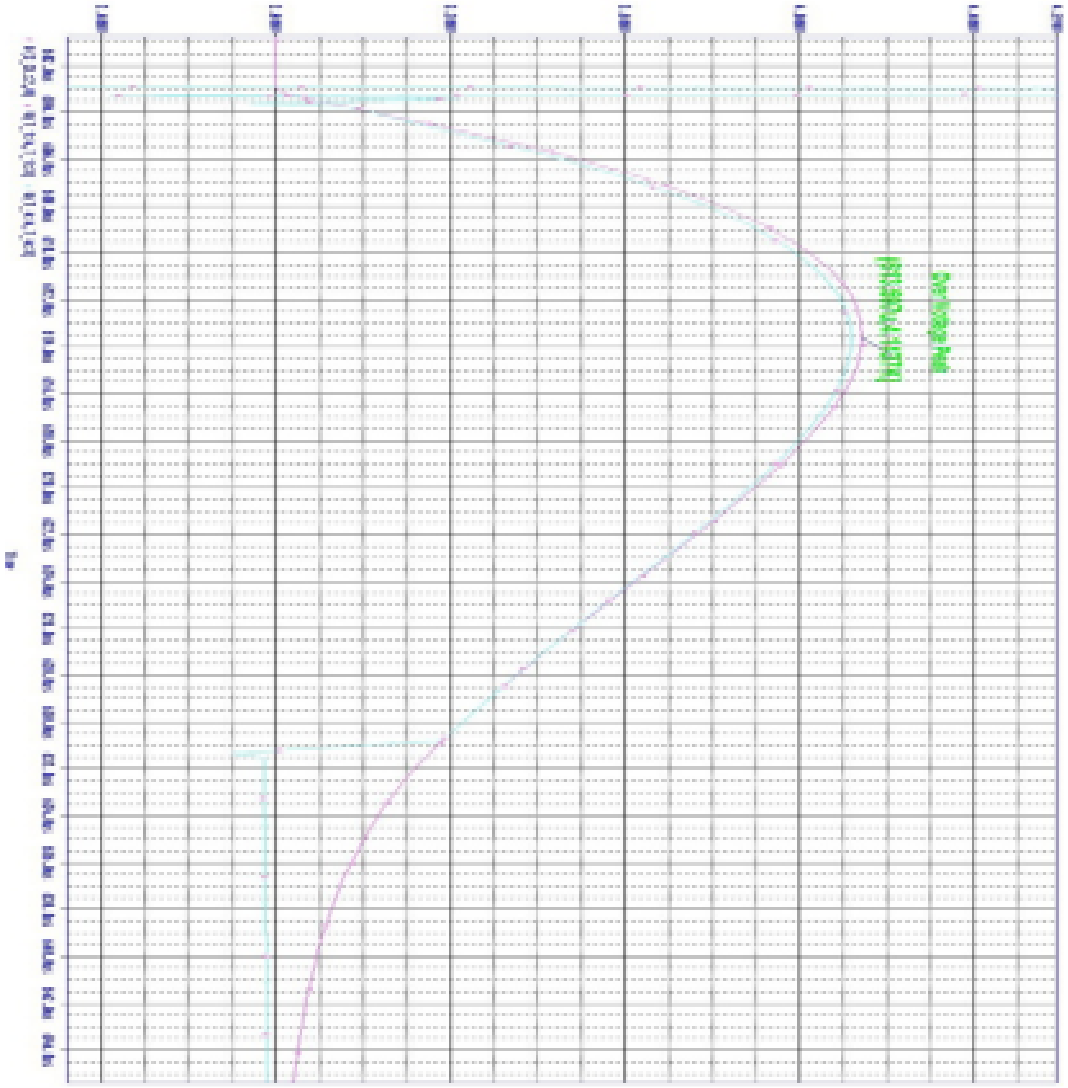


Fig: 2.14 Overvoltage @IGCT turn off for bipolar case in Pspice simulation

Using below data when did simulation in Pspice:

- V_{DC} = 2800 V
- $\frac{\partial i}{\partial tmax}$ = 600 $\frac{A}{\mu s}$ (given in the datasheet. That is the total maximum)
- Typical value of $\frac{\partial i}{\partial t}$ (L_i = 4.41 µH, L_{CL} = 0.3 µH)

  $\rightarrow \frac{\partial i}{\partial t} = \frac{2800\,V}{4.71\mu H} = 594.48\ \frac{A}{\mu s}$

  In most equalization the stray inductance of the clamp inductance is disregarded, so that we get:

$$\rightarrow \frac{\partial i}{\partial t} = \frac{2800\ V}{4.41\ \mu H} = 634.492\ \frac{A}{\mu s}$$

$$\rightarrow L_i = \frac{V_{DClink}}{\frac{\partial i}{\partial t}} = \frac{2800\ V\mu s}{600\ A} = 4.67\ \mu H \quad \text{(for } L_{CL} \rightarrow 0\text{)}$$

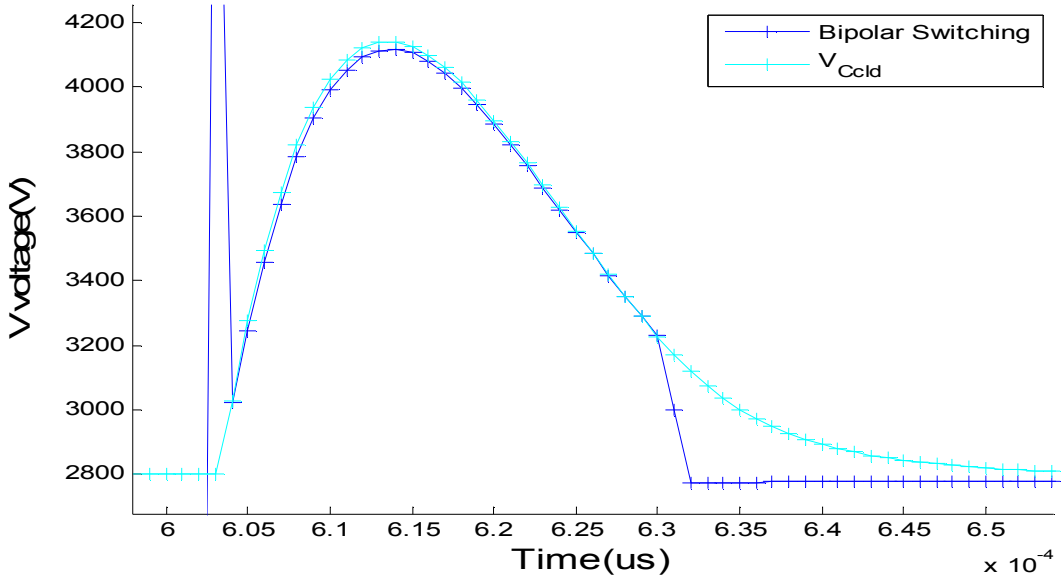


Fig : 2.15 Zoom view of Overvoltage @IGCT turn off for Bipolar case in Matlab

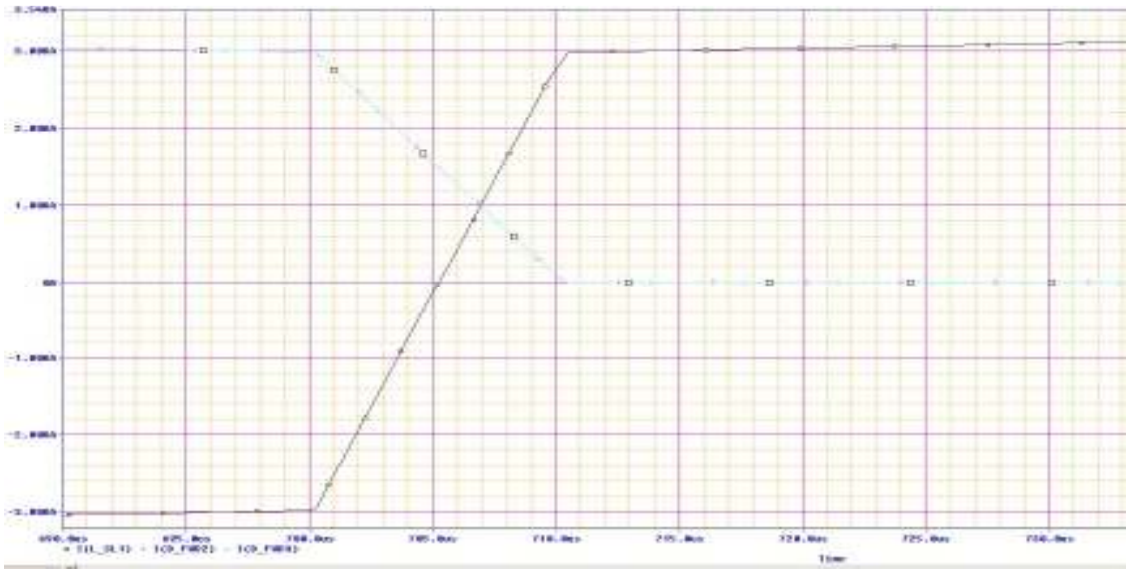


Fig : 2.16 Zoom view of current slopes @IGCT turn on for Bipolar case in Pspice simulation

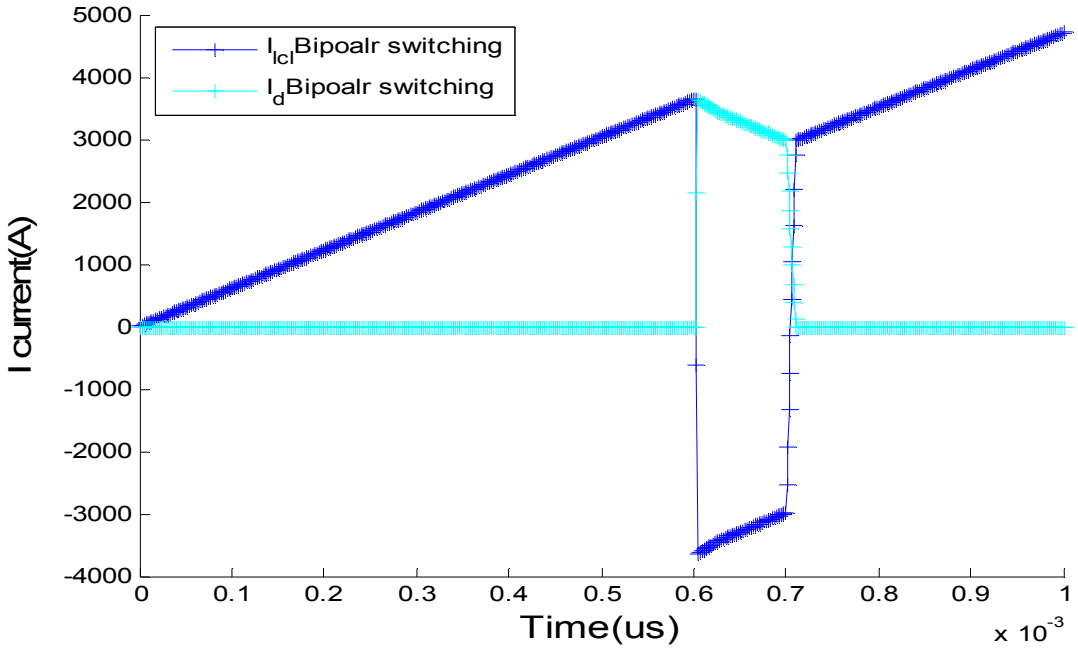


Fig: 2.17 Submodule and clamping inductor current for Bipolar case in Matlab

From these characteristics, some conclusions can be drawn as follows.

- The clamp current varies between ± *Imax* during each switching event, while semiconductor current only varies between *Imax* and zero. The clamp current slope is twice the slope of that of the semiconductors.
- There is a relatively high overvoltage during IGCT turn-off which is double of the unipolar switching overvoltage or half bridge submodule overvoltage when the free-wheeling diodes are turned-on.

2.6 Unipolar Switching for Full Bridge Converter Submodule

The Unipolar modulation (**fig 2.18**) is based on four available switching states, and the converter is operated as a single phase three level voltage source (± *Vbus* and 0). The main characteristics of a unipolar modulated IGCT full-bridge are shown below. One example case is that the IGCT switches T2 and T3 are turned on initially, assuming the current flows through T2 and T3. By turning off IGCT switch T2 and turning on IGCT switch T1, the current is commutated from the IGCT T2 to the free-wheeling diode D1. By observing the unipolar switching pattern, it is essentially the same as the switching pattern of the half-bridge submodule.

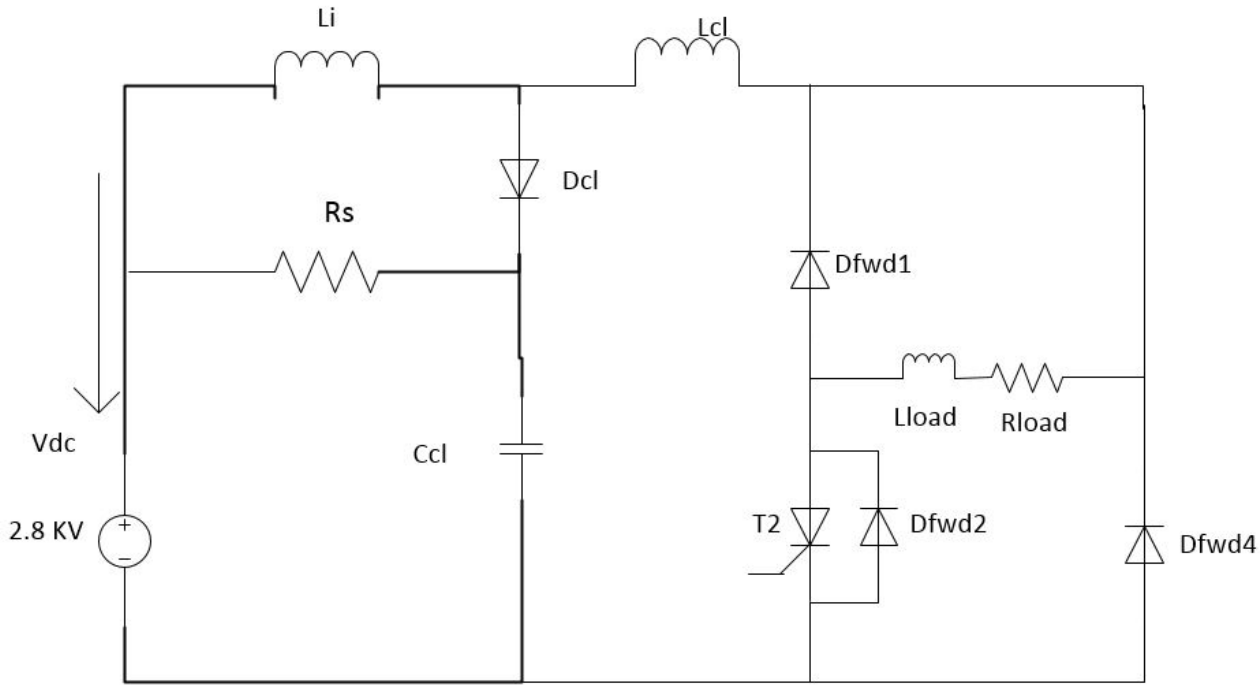


Fig: 2.18 Unipolar Modulation (case 2) model

- L_{CL}(0.3μH) is the stray inductance of the IGCT converter stack. It should be minimized to reduce switching overvoltage and losses.
- R_S(0.35Ω) is the damping resistor which is used to dissipate the clamp circuit energy, L_s(50nH) is the stray inductance of the clamping resistor;
- C_{CL}(20μF) is the clamping capacitor which is used to clamp the IGCT over-voltage: It also initially absorbs some of the energy stored in the $\frac{\partial i}{\partial t}$ inductor clamp;
- D_{CL} is the clamp diode, should have a small forward recovery V_{FR}

2.6.1 Detailed View in Pspice & Matlab simulation

Unipolar switching for full bridge submodel (**fig 2.19**) simulations are done in pspice (fig: 2.20) and also in matlab (fig: 2.21) were developed by using a voltage controlled switch(V_1/4), with a turn-on and turn-off resistance. Model IGCT V Switch $\mathbf{R_{on}= 10e^{-3}}$, $\mathbf{R_{off=}\ 1e^{4}}$, $\mathbf{V_{on=}\ 0.1V}$, $\mathbf{V_{off=}0.0V}$ but disregarded the parameters of the gate signal, which are given by the datasheet.

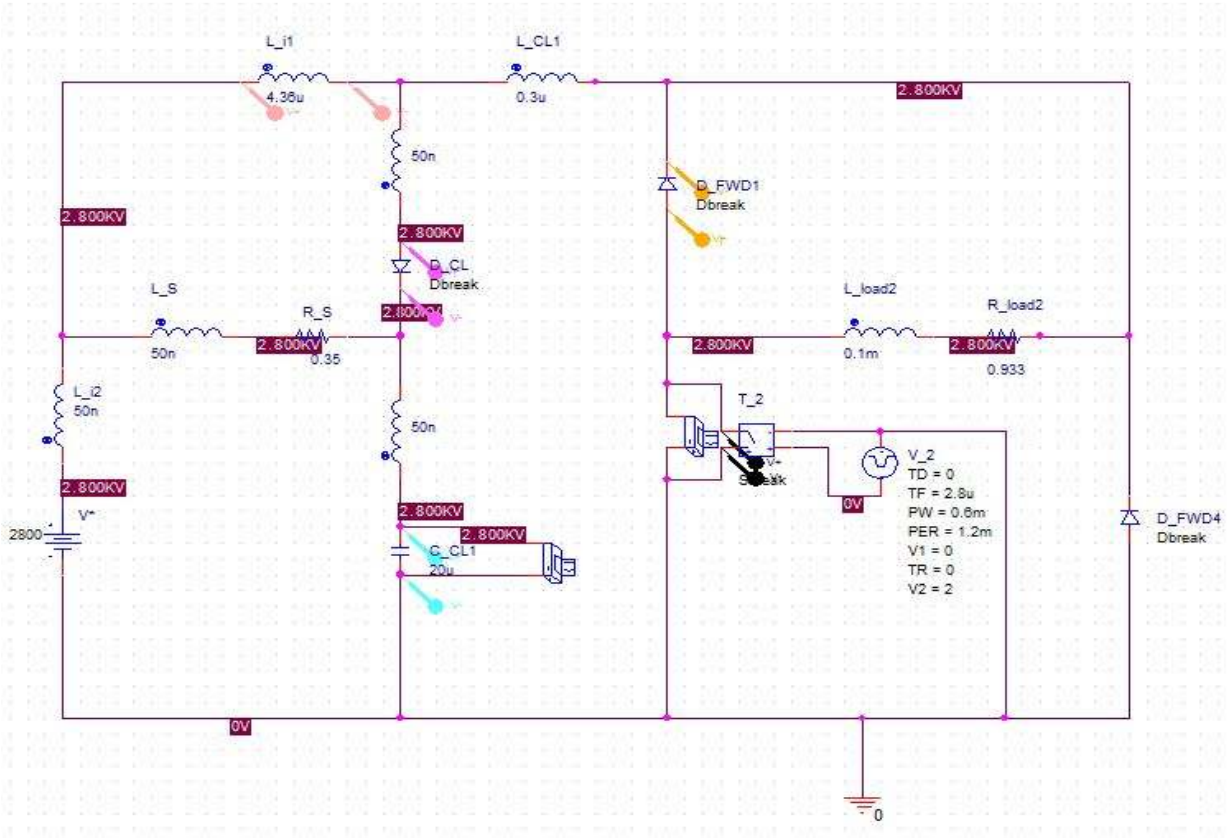


Fig: 2.19 Pspice model of unipolar switching mode

- ✓ **TD (Time delay) = 0s TF (Fall time) = 2.8µS TR (Rise time)= 0s**
- ✓ **PW(Pulse Width) = 0.6mS PER (Period) = 1.2m V1 = 0V V2=0V**
- ✓ **Run time = 1.2mS Step Size = 1µS**

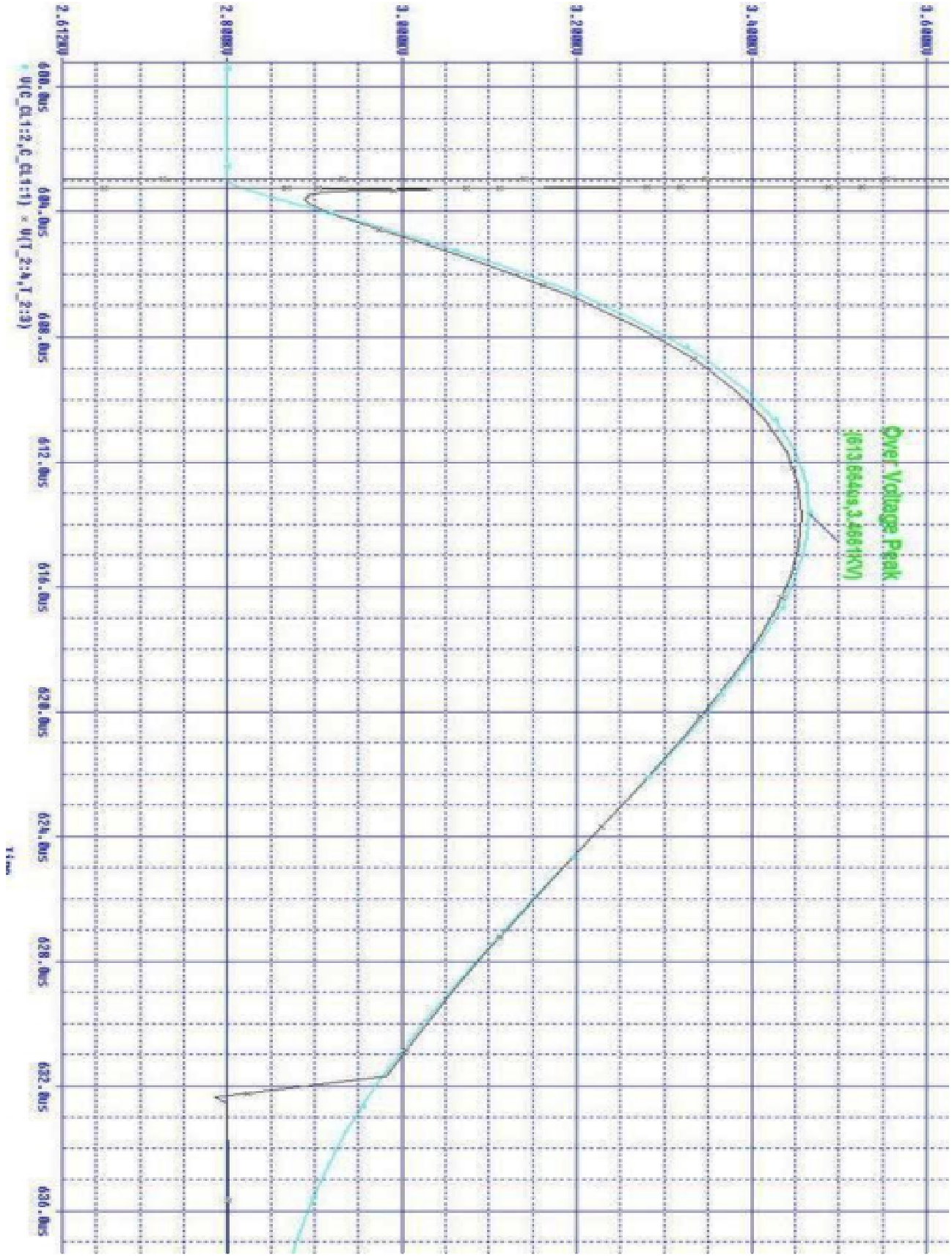


Fig: 2.20 Overvoltage @IGCT turn off for unipolar mode

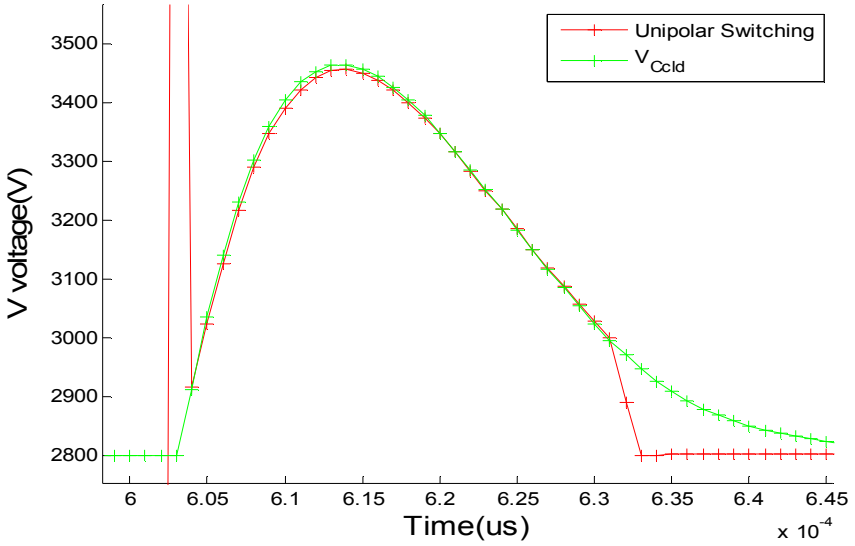


Fig: 2.21 Zoom view of Overvoltage @IGCT turn off for unipolar mode

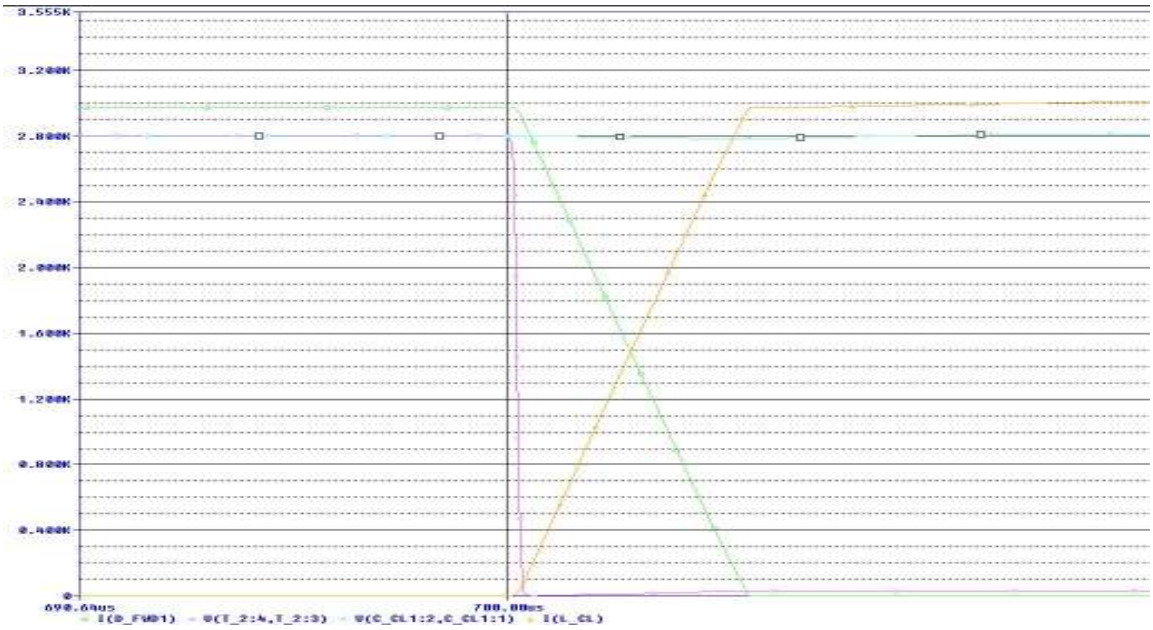


Fig: 2.22 Zoom view of current @IGCT turn on for unipolar mode

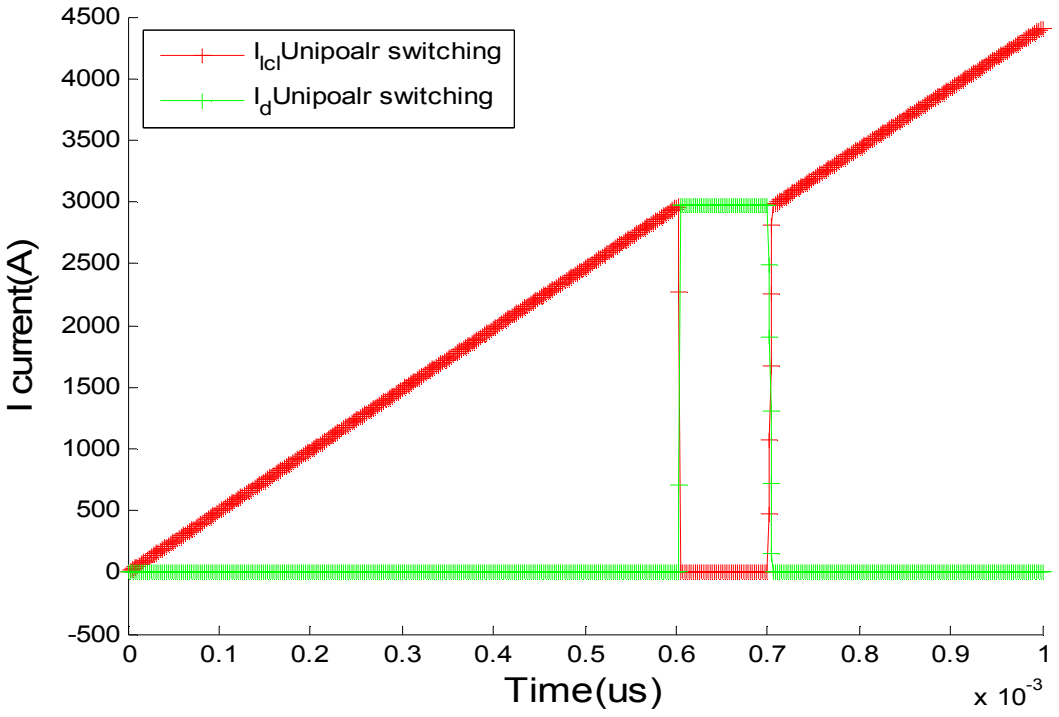


Fig: 2.23 Diode and clamp current for unipolar mode operation

From Pspice simulation of full-bridge unipolar operation, some conclusions can be drawn as follows:

- Both clamp and semiconductor current vary between *Imax* and 0 and with the same slope which is in contrast to the bipolar operation mode where the clamp current slope (di/dt) is two times of the semiconductor slope.
- The overvoltage during IGCT's turn-off is only half of the overvoltage of the bipolar case when the same clamping circuit parameters are used.

It is noted that the design of IGCT clamping circuit should consider these two operating modes. For MMC HVDC converters with full-bridge cells, the unipolar switching mode is used during normal operation. However, when DC side fault occurs, the IGCTs in the full-bridge submodules are blocked to provide reverse submodule voltage to block the DC side fault. Therefore, the bipolar operating mode may occur during DC side fault blocking operation. The design of the submodule clamp circuit should ensure that the IGCT semiconductor maximal rating should not be violated during normal and faulty transient operations.

2.7 Mechanical design of Full bridge submodule

The mechanical design of half- and full-bridge cells are illustrated in **fig 2.24** and **2.25**. The mechanical designs of the submodules are based on modular concept. The half-bridge and full- bridge converter submodules are composed of IGCT, DC-link capacitor, clamping

inductor, clamping resistors, clamping capacitors. Snubber circuit are required to limit $\frac{di}{dt}$ and over voltage during IGCT turn- on and turn-off.

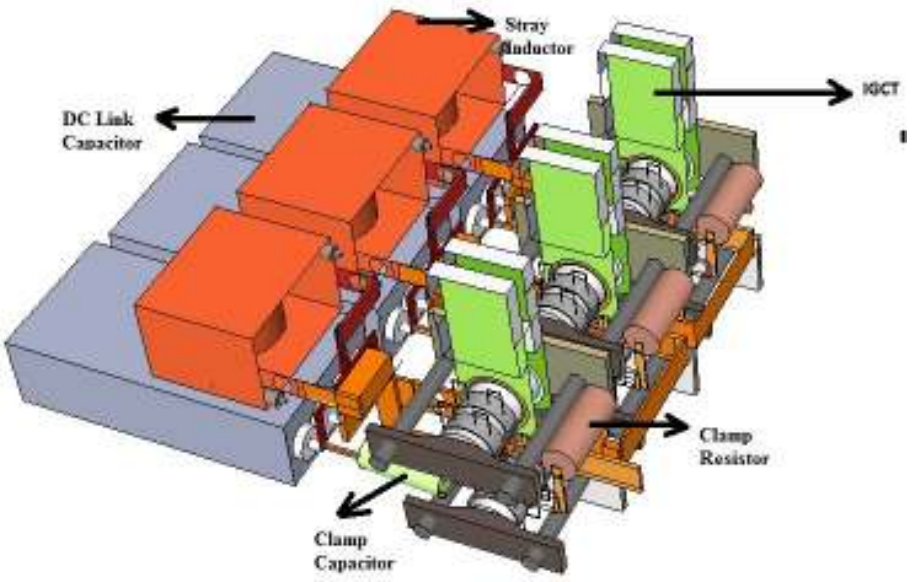


Fig 2.24: Illustration of half bridge converter with IGCT submodule

IGCT needs $\frac{di}{dt}$ protection during turn-on and overvoltage protection during turn-off. Snubber capacitor is needed for minimized overvoltage. Overvoltage usually occurs during turn-off process. The snubber resistor R is used to discharge clamping inductor energy during IGCT switching on and off.

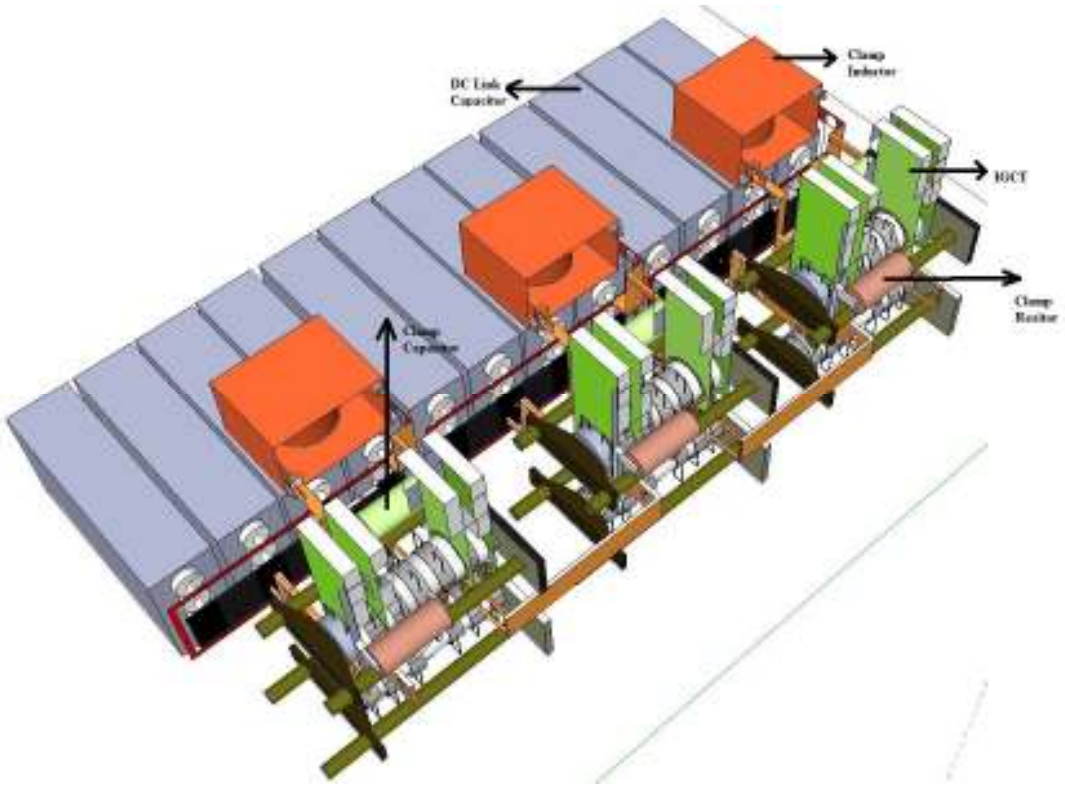


Fig 2.25: Illustrate of full bridge converter with IGCT submodule

CHAPTER 3

Loss Calculation

3.1 MMC LOSS CALCUALTION for Full-Bridge submodule

In order to find the dimensioning factors of a Modular Multilevel Converter (MMC), an understanding of its basic operational principles is essentials. The schematic of one phase leg of a MMC is shown in (**fig: 3.1**). Each phase leg consists of two arms, one upper arm and one lower arm, connected in series between the dc terminals. The ac terminals is located at the midpoint between the two arm are shown in (**fig 3.1**). Each arm consists of one arm inductor and N series connected half/full bridge with dc capacitors, termed submodules. The resistive losses in the converter are modeled with resistor R connected in series with each arm inductor. The purpose of arm inductors is to limit parasitic currents and fault currents In order to limit the parasitic current, the required arm inductors are typically very small.

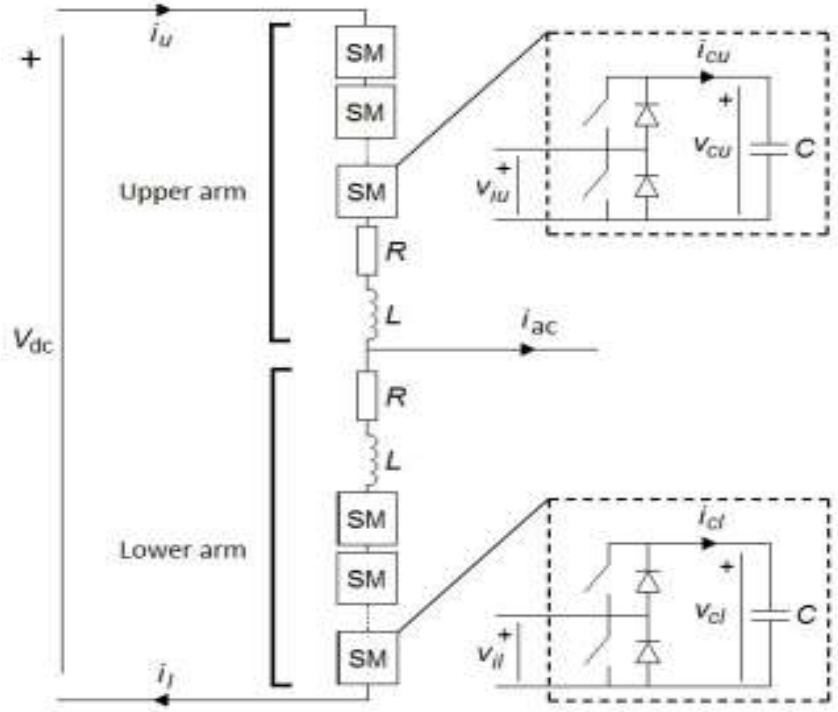


Fig: 3.1 One phase leg of the modular multilevel converter

The purpose of loss calculation is to estimate the converter efficiency and to design proper cooling system for the converter. There are two loss calculation methods used in the literature. One is based on instantaneous semiconductor or submodule current waveform where the semiconductor conduction and switching losses are derived from the current waveform. The other one is based on analytical equations of the semiconductor and submodule currents. The semiconductor losses are derived from the analytical current equations. The advantage of analytical loss calculation method is straightforward calculation without the need of specific converter modulation and control. In this thesis, the analytical loss calculation method for MMC HVDC converter with full-bridge (**fig: 3.2**) module is used.

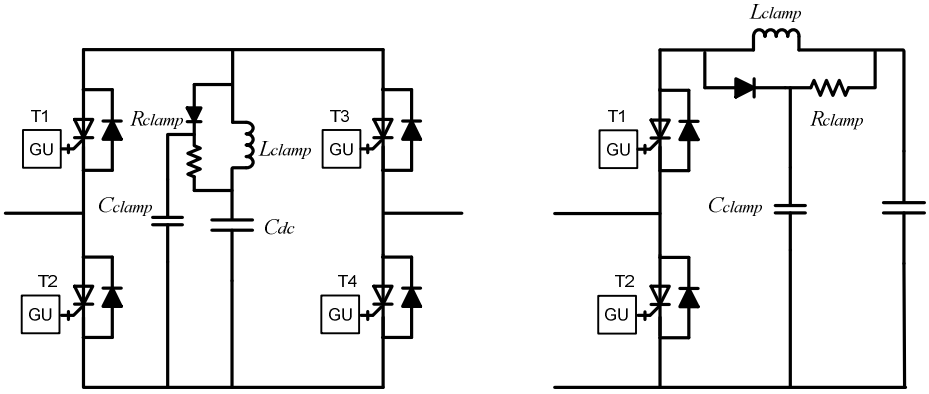


Fig: 3.2 MMC converter cell Full Bridge IGCT & Half Bridge IGCT

For consistency purpose, this part of the thesis same notation using as like **fig 2.6** . Among three phase (A, B, C) in MMC HVDC converter. One single(A) phase current detonated by i_{vpa} . Each phase has two arm (positive & negative). For one phase(A) positive –arm current denoted as i_{vppa}, negative – arm denoted as i_{vpna} and the DC current represented as I_p. Therefore, one single phase (A) positive –arm current i_{vppa} can be represented as

$$i_{vppa} = \frac{i_{vpa}}{2} - \frac{I_p}{3} \text{ (two arm \& three phase)}$$

One single phase (A) negative-arm current

$$i_{vpna} = -\frac{i_{vpa}}{2} - \frac{I_p}{3}$$

Assuming the phase (A) voltage is represented as :

$$U_{vpa} = \sqrt{2}U_{vp}\cos(\omega t + \delta_{vp})$$

Where U_{vpa} is the phase voltage RMS value and δ_{vp} is the phase voltage angel. The phase (A) current is represented as

$$i_{vpa} = \sqrt{2}U_{vp}\cos(\omega t + \delta_{vp} - \varphi)$$

Where φ is the load angel. Single phase (A) positive arm current can be written as

$$i_{vppa} = \frac{\sqrt{2}U_{vp}\cos(\omega t+\delta_{vp}-\varphi)}{2} - \frac{I_p}{3}$$

Similarly the negative arm current for phase (A) can be written as

$$i_{vpna} = -\frac{\sqrt{2}U_{vp}\cos(\omega t+\delta_{vp}-\varphi)}{2} - \frac{I_p}{3}$$

The DC current I_p can be represented as

$$I_p = -\frac{P_{vp}}{U_{dp}} = -\frac{3U_{vp}I_{vp}\,cos\varphi}{U_{dp}}$$

Here, we define the modulation index m_p as

$$m_p = \frac{\sqrt{2}U_{dp}}{U_{dp}/2} = \frac{2\sqrt{2}U_{dp}}{U_{dp}}$$

Substituting m_p intoI_p, it can be represented as

$$I_p = -\frac{P_{vp}}{U_{dp}} = -\frac{3m_pI_{vp}cos\varphi}{2\sqrt{2}}$$

Thus, the positive and negative arm currents can be represented as

$$i_{vppa} = \frac{\sqrt{2}I_{vp}\cos(\omega t+\delta_{vp}-\varphi)}{2} + \frac{m_pI_{vp}cos\varphi}{2\sqrt{2}}$$

and

$$i_{vpna} = -\frac{\sqrt{2}I_{vp}\cos(\omega t+\delta_{vp}-\varphi)}{2} + \frac{m_pI_{vp}cos\varphi}{2\sqrt{2}}$$

The total losses in the converter comprise mainly of **switching losses**, **conduction losses** and **clamping loss** for IGCT full bridge converter**.** The diode turns on rapidly and hence the switching energy of the diode during turn-on can be neglected. But due to reverse recovery characteristics, the turn-off energy of the diode has to be considered. For calculating losses we consider negative current passes through each cell, denoted by the scenario ($\boldsymbol{i_{vppa} < 0}$). Insert or bypass are making though T4 switch. That means T4 is always active condition.

3.2 Cell operating Mode

For easier loss calculation taking upper arm operating mode analysis, converter arm current should be identified. Semiconductor losses are divided into four parts, the upper- leg (inserting-leg, **fig 3.3b**) IGCT T1 and diode D1 losses, the lower-leg (bypassing-leg, **fig 3.3a**) IGCT T2 and diode D2 losses. The on and off states of the semiconductor devices or cell operating mode depend on the directions of converter arm current (upper arm i_{vppa} or lower arm i_{vpna}) flowing through the MMC cells.That is, the zero crossing of the converter arm current should be calculated from i_{vppa} and i_{vpna}. An illustration of upper arm current i_{vppa} is given in **fig. 3.3** .The zero crossing points $\theta_1, \theta_2, \theta_3$ are in **fig: 3.4** solved from

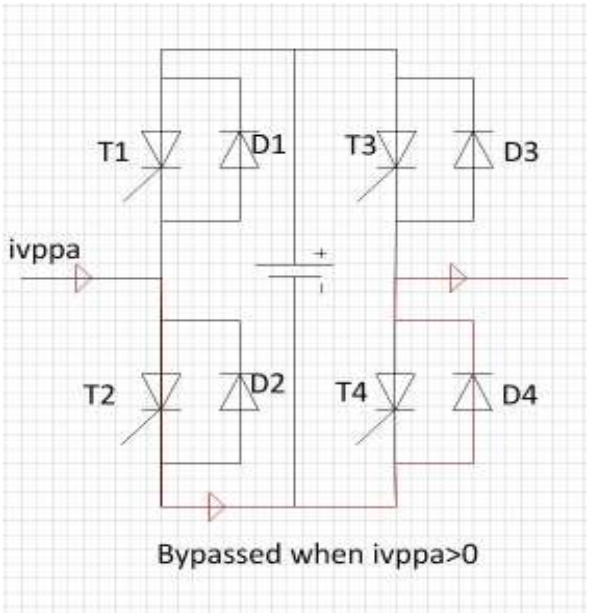
$$i_{vpna} = -\frac{\sqrt{2}U_{vp}\cos(\omega t+\delta_{vp}-\varphi)}{2} + \frac{m_p I_{vp} cos\varphi}{2\sqrt{2}} = 0$$

which gives

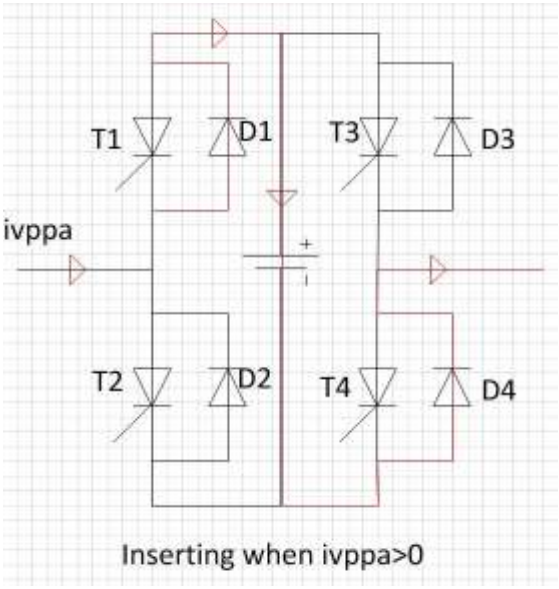
$$\theta_{1,} = \varphi - cos^{-1}(-\frac{m_p}{2}cos\varphi)$$

$$\theta_{2,} = \varphi + cos^{-1}(-\frac{m_p}{2}cos\varphi)$$

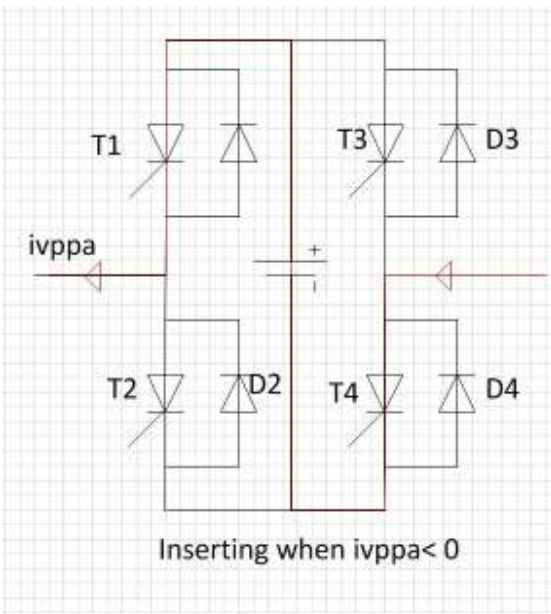
$$\theta_{3,} = 2\pi + \theta_1$$



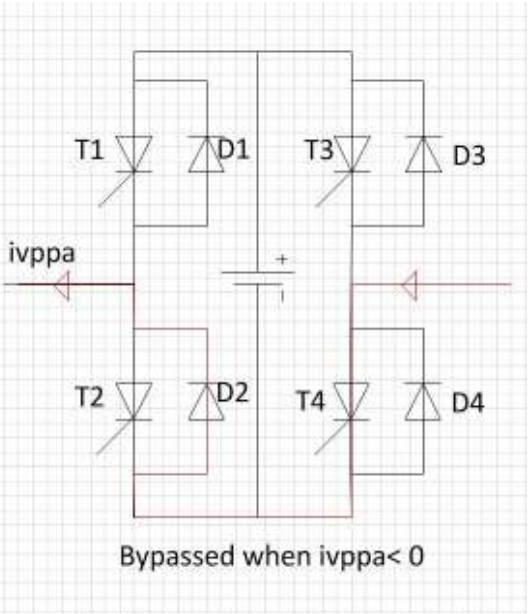
a) bypassing i_{vppa} >0



b) inserting i_{vppa} >0



c) inserting $i_{vppa} < 0$



d) bypassing $i_{vppa} < 0$

Fig: 3.3 Upper –arm MMC converter cell operating mode

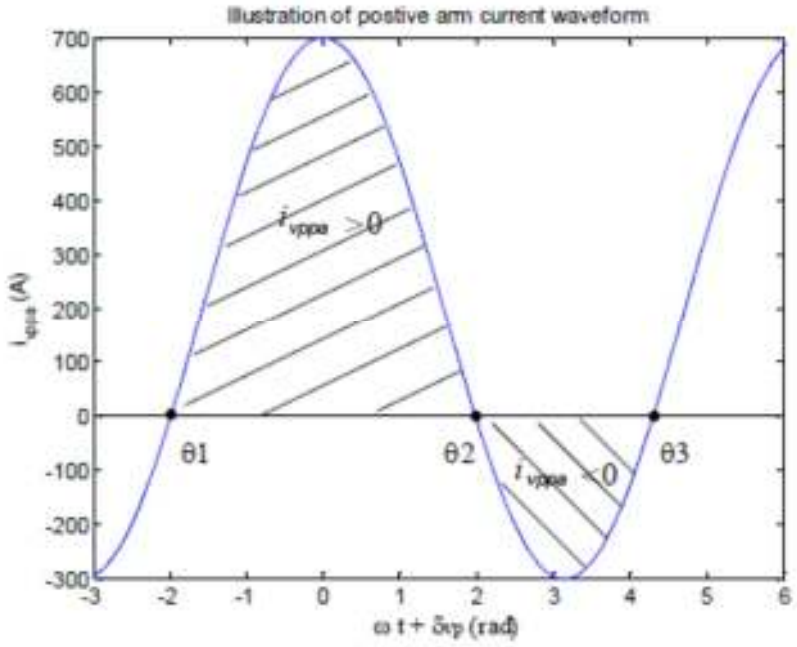


Fig :3.4 Zero crossing of MMC converter arm current

The number of cells in the positive arm that are inserted (N_{ins}) and bypassed (N_{byp}) at a given time instant can be calculated. The total number of cell in positive arm is given by N = U_{dp}/U_{cell} where $U_{cell}$is the rated converter cell DC-link voltage. The number of cells inserted N_{ins} is calculated as

$$N_{ins} = \frac{\frac{U_{dp}}{2} - U_{vpa}(t)}{U_{cell}}$$

$$N_{byp} = N - N_{ins} = N - \frac{\frac{U_{dp}}{2} - U_{vpa}(t)}{U_{cell}}$$

Substituting $U_{vpa}(t)$ and m_p into the above equation, the inserted and bypassed cell number are given as

$$N_{ins} = \frac{N}{2}(1 - m_p \cos(\theta))$$

$$N_{byp} = \frac{N}{2}(1 + m_p \cos(\theta))$$

The percentages of inserted and bypassed cells with respect to the total positive arm cells *N* are given as

$$n_{ins} = \frac{1}{2}(1 - m_p \cos(\theta))$$

$$n_{byp} = \frac{1}{2}(1 + m_p \cos(\theta))$$

Where $\theta = \omega t + \delta_{vp}$

3.3 Analytical loss calculation method

The loss analysis is performed only for converter positive arm (positive arm currenti_{vppa}) in this thesis. The negative arm MMC cells has the same loss profile as the positive-arm cells since the converter upper and lower arms are symmetrical.

3.4 Conduction losses estimation

The conduction losses for MMC HVDC cell are calculated by the flowing equations.

Upper-leg IGCT T4

The conduction loss of the upper-leg IGCT T4 (**fig 3.3c**), inserting with negative arm current) is given as. Where r_{ce} and v_{ce} are IGCT T4 on state characterizes.

$$P_{cond,T4} = \frac{1}{2\pi}\int_{\theta 2}^{\theta 3}(r_{ce}\ i_{vppa}^2(\theta) - v_{ce}\, i_{vppa}(\theta))d\theta$$

$$= \frac{1}{2\pi}\int_{\theta 2}^{\theta 3}(r_{ce}\ \frac{I_{vp}^2}{4}(\frac{m_p}{2}\cos\varphi + \cos(\theta-\varphi))^2\, d\theta - \frac{1}{2\pi}\int_{\theta 2}^{\theta 3} v_{ce}\frac{I_{vp}}{\sqrt{2}}(\frac{m_p}{2}\cos\varphi + \cos(\theta-\varphi))d\theta$$

$$= \frac{1}{2\pi}\int_{\theta 2}^{\theta 3}(r_{ce}\ \frac{I_{vp}^2}{4}(\frac{m_p^2}{4}\ cos^2\varphi + m_p\ cos\varphi\cos(\theta-\varphi) + cos^2(\theta-\varphi))d\theta - \frac{1}{2\pi}\int_{\theta 2}^{\theta 3} v_{ce}\frac{I_{vp}}{\sqrt{2}}(\frac{m_p}{2}\cos\varphi + \cos(\theta-\varphi))d\theta$$

$$= \frac{1}{2\pi}\int_{\theta 2}^{\theta 3}(r_{ce}\ \frac{I_{vp}^2}{4}(\frac{m_p^2}{4}\ cos^2\varphi + m_p\ cos\varphi\cos(\theta-\varphi) + \frac{1+\cos(2\theta-2\varphi)}{2})\, d\theta - \frac{1}{2\pi}\int_{\theta 2}^{\theta 3} v_{ce}\frac{I_{vp}}{\sqrt{2}}(\frac{m_p}{2}\cos\varphi + \cos(\theta-\varphi))d\theta$$

$$= \frac{1}{2\pi}\frac{I_{vp}^2 r_{ce}}{2}\left[\frac{m_p^2}{4}\ cos^2\varphi[\theta_3-\theta_2] + m_p\ cos\varphi\sin[(\theta_3-\theta_2)-\varphi] + \frac{1}{2}[\theta 3-\theta 2]\ \frac{1}{4}\sin[2(\theta_3-\theta_2)-\varphi]\right] - \frac{1}{2\pi}\frac{I_{vp}v_{ce}}{\sqrt{2}}\left[(\frac{m_p}{2}\cos\varphi[\theta_3-\theta_2] + \sin[(\theta_3-\theta_2)-\varphi]\right]$$

Where

$$\theta_1 = \varphi - \cos^{-1}\left(-\frac{m_p}{2}\ cos\varphi\right)$$

$$\theta_2 = \varphi + \cos^{-1}\left(-\frac{m_p}{2}\ cos\varphi\right)$$

$$\theta_3 = 2\pi + \theta_1$$

Upper-leg Diode D4 :

The conduction loss of the upper-leg IGCT D4 (**fig 3.3b**), inserting with positive arm current) is given as, where $r_{f_\circ}$ and $v_{f_\circ}$ are upper –leg diode D4 on-state characteristics.

$$P_{cond,D4} = \frac{1}{2\pi}\int_{\theta 1}^{\theta 2}(r_{f_\circ}\, i_{vppa}^2(\theta) + v_{f_\circ}\, i_{vppa}(\theta))d\theta$$

$$= \frac{1}{2\pi}\int_{\theta 1}^{\theta 2}(r_{ce}\ \frac{I_{vp}^2}{4}(\frac{m_p}{2}\cos\varphi + \cos(\theta-\varphi))^2\, d\theta$$

$$+ \frac{1}{2\pi}\int_{\theta 1}^{\theta 2} v_{ce}\frac{I_{vp}}{\sqrt{2}}(\frac{m_p}{2}\cos\varphi + \cos(\theta-\varphi))d\theta$$

$$= \frac{1}{2\pi}\int_{\theta 1}^{\theta 2}(r_{ce}\ \frac{I_{vp}^2}{4}(\frac{m_p^2}{4}\ cos^2\varphi +\ m_p\ cos\varphi\cos(\theta-\varphi) + cos^2(\theta-\varphi))d\theta$$

$$+ \frac{1}{2\pi}\int_{\theta 1}^{\theta 2} v_{ce}\frac{I_{vp}}{\sqrt{2}}(\frac{m_p}{2}\cos\varphi + \cos(\theta-\varphi))d\theta$$

$$= \frac{1}{2\pi}\int_{\theta 1}^{\theta 2}(r_{ce}\ \frac{I_{vp}^2}{4}(\frac{m_p^2}{4}\ cos^2\varphi +\ m_p\ cos\varphi\cos(\theta-\varphi) + \frac{1+\cos(2\theta-2\varphi)}{2})\, d\theta$$

$$+ \frac{1}{2\pi}\int_{\theta 1}^{\theta 2} v_{ce}\frac{I_{vp}}{\sqrt{2}}(\frac{m_p}{2}\cos\varphi + \cos(\theta-\varphi))d\theta$$

$$= \frac{1}{2\pi}\frac{I_{vp}^2}{2}\left[\frac{m_p^2}{4}\ cos^2\varphi[\theta_2-\theta_1] +\ m_p\ cos\varphi\sin[(\theta_2-\theta_1)-\varphi] + \frac{1}{2}[\theta_2-\theta_1] + \frac{1}{4}\sin[2(\theta_2-\theta_1)-\varphi]\right] + \frac{1}{2\pi}\frac{I_{vp}}{\sqrt{2}}\left[(\frac{m_p}{2}\cos\varphi[\theta_2-\theta_1] + \sin[(\theta_2-\theta_1)-\varphi]\right]$$

$$\theta_1 = \varphi - \cos^{-1}\left(-\frac{m_p}{2}\ cos\varphi\right)$$

$$\theta_2 = \varphi + \cos^{-1}\left(-\frac{m_p}{2}\ cos\varphi\right)$$

$$\theta_3 = 2\pi + \theta_1$$

The conduction losses switch T1, diodeD1, switchT2, diode D2

$$P_{cond,T1} = \frac{1}{2\pi}\int_{\theta 2}^{\theta 3}(r_{ce}\ i_{vppa}^2(\theta) + v_{ce}\, i_{vppa}(\theta))\, N_{ins}\, d\theta$$

$$P_{cond,D1} = \frac{1}{2\pi}\int_{\theta 1}^{\theta 2}(r_{f_\circ}\ i_{vppa}^2(\theta) + v_{f_\circ}\, i_{vppa}(\theta))\, N_{ins}\, d\theta$$

$$P_{cond,T2} = \frac{1}{2\pi}\int_{\theta 1}^{\theta 2}(r_{ce}\ i_{vppa}^2(\theta) + v_{ce}\, i_{vppa}(\theta))\, N_{byp}\, d\theta$$

$$P_{cond,D2} = \frac{1}{2\pi}\int_{\theta 2}^{\theta 3}(r_{f_\circ}\ i_{vppa}^2(\theta) - v_{f_\circ}\, i_{vppa}(\theta))\, N_{ins}\, d\theta$$

So, total power loss for conduction will be calculating from below formulas:

$$P_{cond,switch} = P_{cond,T4} + P_{cond,T1} + P_{cond,T2}$$

$$P_{cond,diode} = P_{cond,D4} + P_{cond,D1} + P_{cond,D2}$$

$$P_{cond,Total} = P_{cond,diode} + P_{cond,switch}$$

3.5 Switching losses estimation

In this thesis MMC simulation work used for full bridge converter. Each full bridge converter has four switches & four freewheeling diode. The switching losses, diodes and controlled semiconductors should be characteristed for the turn-on and turn-off switching transients. When there is inserting & bypassing happen through switch & diode. In equation we assuming f_p is switching frequency, W_{on} and W_{off} are switching on and off energy for IGCT respectively. V_{ref} and I_{ref} are the reference point where the switching energy is measured, V_c is the actual DC link voltage. m_p is modulation index and i_{ap}, i_{an} are expressing postive & negative arm current.

$$P_{switch,T1} = f_p * \left(\frac{W_{on}+W_{off}}{V_{ref}I_{ref}}\right) * V_c * i_{an}$$

$$P_{switch,D1} = f_p * \left(\frac{W_{on}+W_{off}}{V_{ref}I_{ref}}\right) * V_c * i_{ap}$$

$$P_{switch,T2} = f_p * \left(\frac{W_{on}+W_{off}}{V_{ref}I_{ref}}\right) * V_c * i_{ap}$$

$$P_{switch,D2} = f_p * \left(\frac{W_{on}+W_{off}}{V_{ref}I_{ref}}\right) * V_c * i_{an}$$

Where

$$i_{ap} = \frac{I_v}{2\sqrt{2\pi}} \left(m_p * cos\varphi * \cos(-\frac{m_p}{2} cos\varphi) + 2 * \sin(-\frac{m_p}{2} cos\varphi)\right)$$

$$i_{an} = \frac{I_v}{2\sqrt{2\pi}} \left(m_p * cos\varphi * \cos(\left(-\frac{m_p}{2} cos\varphi\right) - \varphi) + 2 * \sin(-\frac{m_p}{2} cos\varphi)\right)$$

$$P_{switch.T} = P_{switch,T1} + P_{switch,T2}$$

$$P_{switch,D} = P_{switch,D1} + P_{switch,D2}$$

$$P_{switching,Total} = P_{switch,D} + P_{switch,T}$$

3.6 Clamping losses estimation for IGCT

Hard switching IGCT switching cells must contain an IGCT turn –on inductor (snubber) to limit diode turn-off di/dt, the energy stored in the inductor is discharged and clamped by means of an RCD circuit. Not all of the magnetizing energy is evaluated over the RCD circuit, certain amount of energy is dissipated on the semiconductors and restore to the input power supply.

The clamp circuit power losses are evaluated to identify the amount of magnetizing energy dissipated on the clamp circuit components. The calculation of clamping circuit loss is given as follows.

$$I_{cl}^2 = \frac{I_{vp}^2 m_p^2}{8} cos^2\varphi + \frac{I_{vp}^2}{4}$$

Where I_{cl} is the RMS value of the clamping inductor current. Taking the positive arm for example, I_{cl}^2 is calculated as following

$$P_{clamping} = f_p \left(\frac{1}{2} * L_{cl} * I_{cl}^2\right)$$

The higher the DC input voltage, the smaller the turn-off switching time and higher the clamp circuit over voltage. Higher DC input voltage, the IGCT turn-off behavior becomes more ideal and more energy is dissipated over the clamp circuit components.

3.7 Verification of Analytical loss calculation method

The analytical loss calculation method is used for the follow case study, assuming 320kV DC side voltage and 1GW transmitted active power. The typical data value given by datasheet of IGCT is as following.

- $V_{tTo} = 1.10$ V, $V_{tDo} = 1.9$ V
- $r_{T1} = r_{T2} = 0.26e^{-3}$, $r_{D1} = r_{D2} = 0.79e^{-3}$
- $W_{onT1} = 1.8$ J, $W_{offT2} = 26.5$ J
- $W_{rec} = 10.91$ J, $V_{ref} = 2.8$ kV
- $I_{ref} = 4$ kA

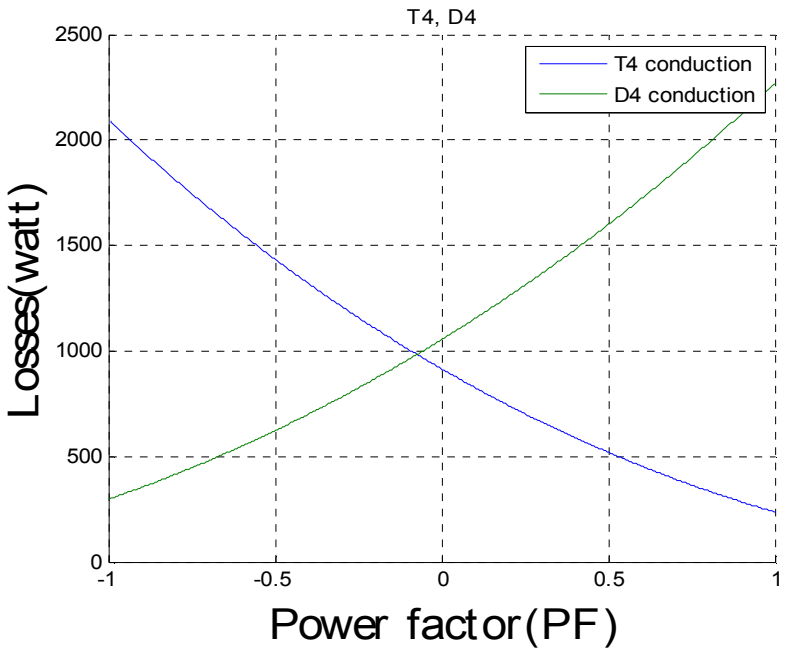


Fig: 3.5 SwitchT4 & diode D4 conducting when T3 always switched off

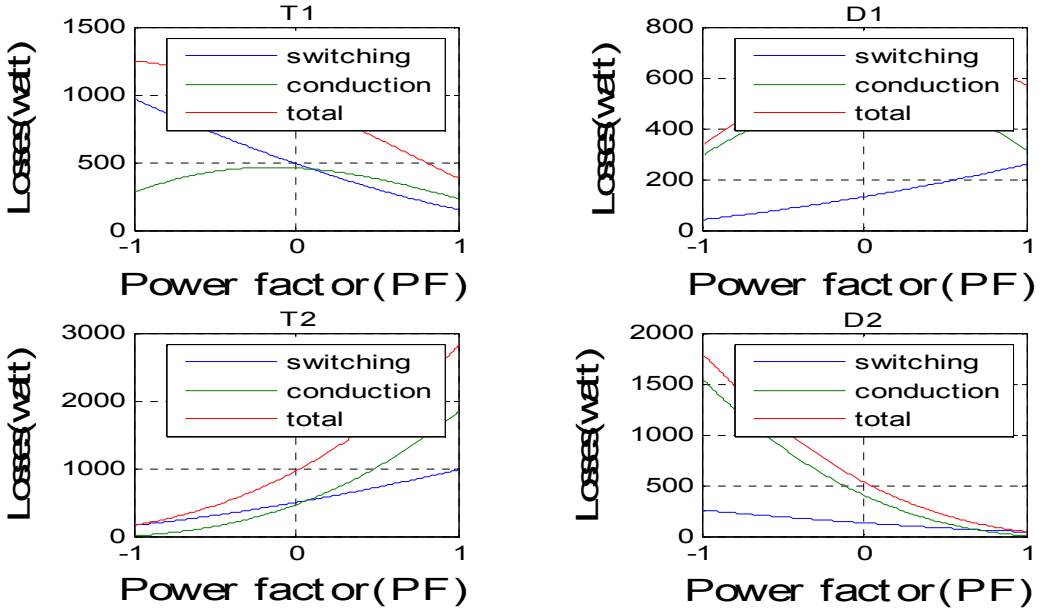


Fig: 3.6 Losses in switches & diodes

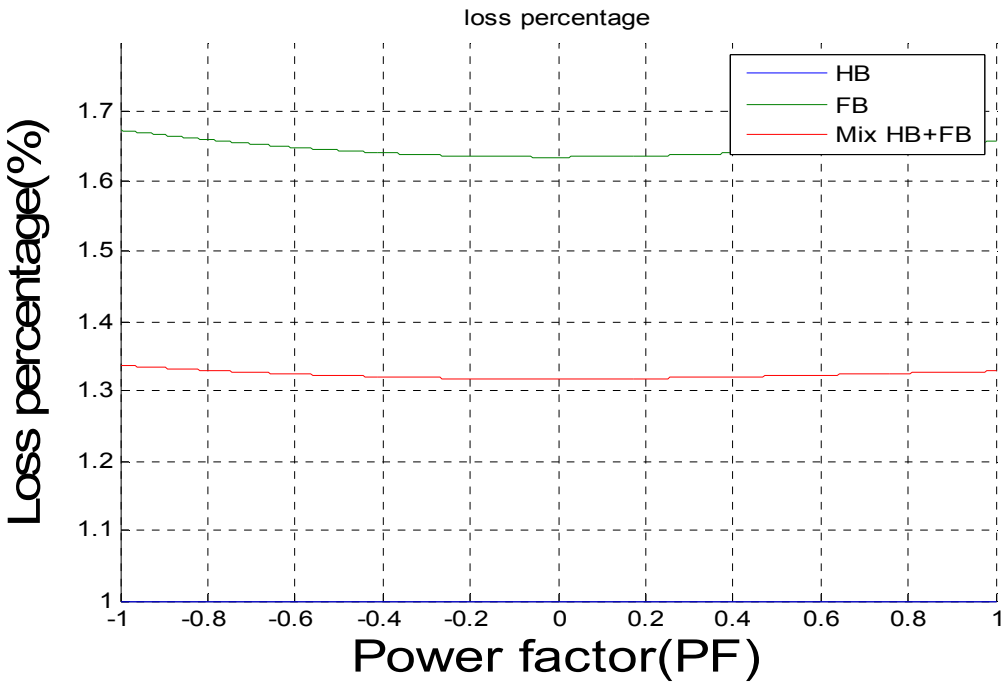


Fig: 3.7 Fifty percent HB and fifty percent FB in M2C Converter

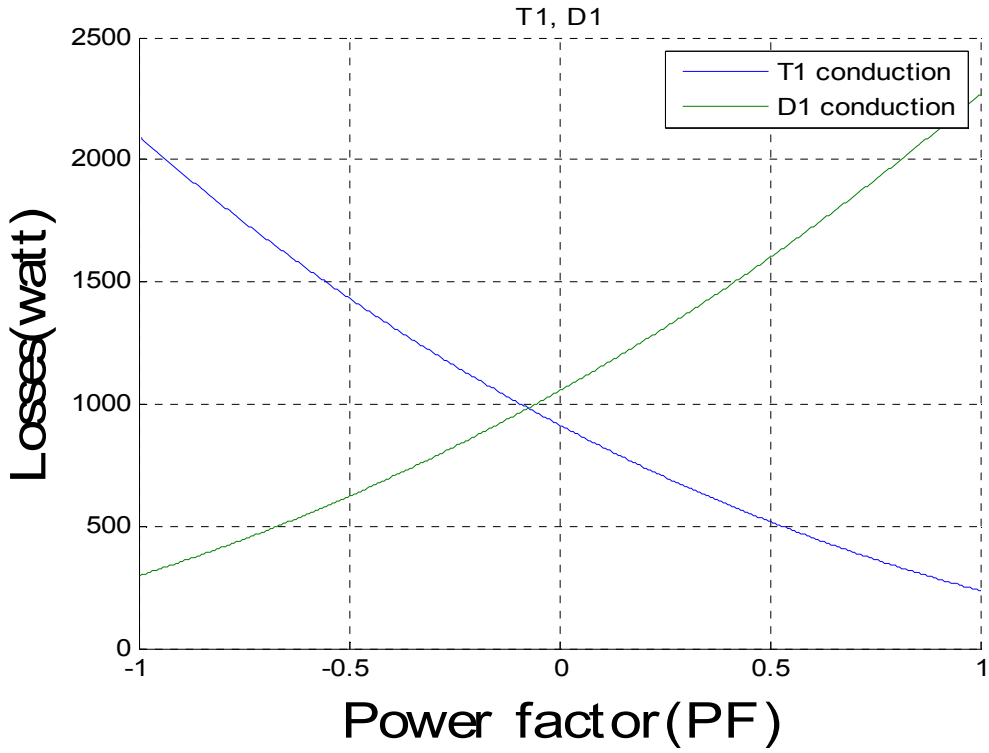


Fig: 3.8 SwitchT4 & diode D4 conducting when T2 always switched off

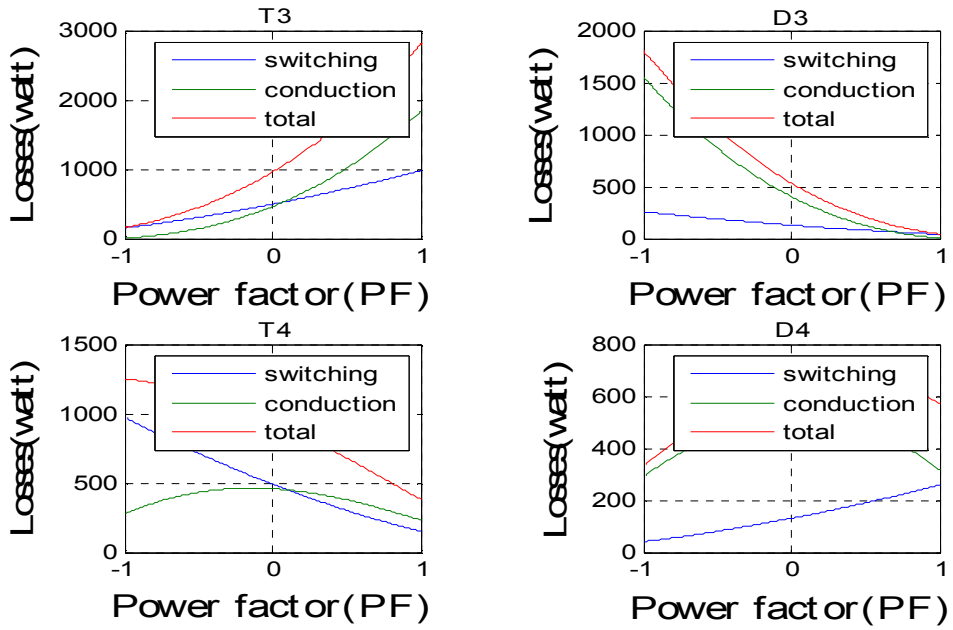


Fig: 3.9 Losses in switches & diodes

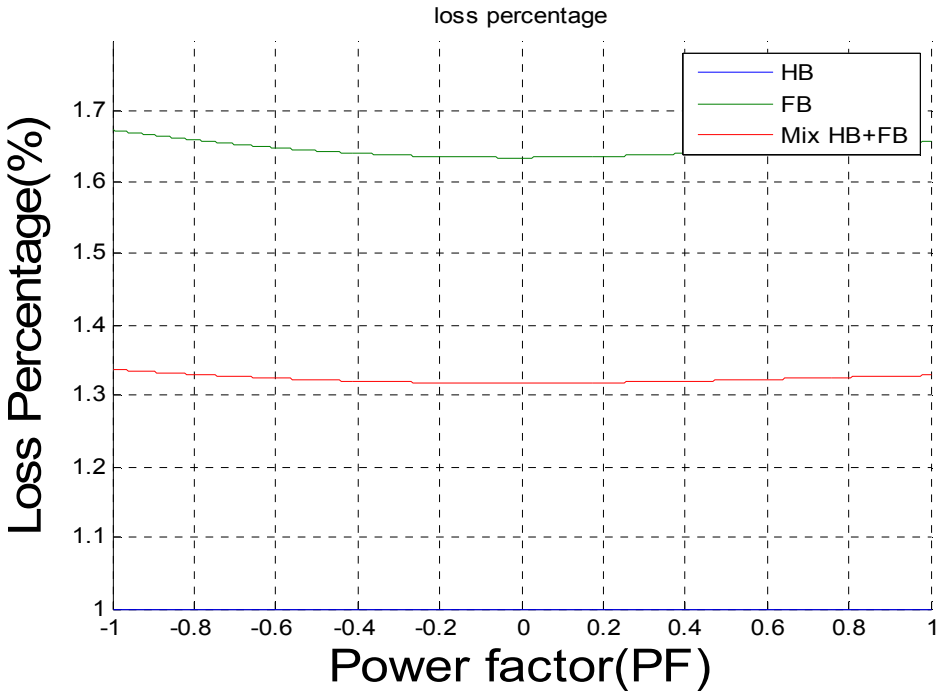


Fig: 3.10 Fifty percent HB & fifty percent FB in M2C Converter

CHAPTER 4

Modular Multilevel Converter

4.1 VSC BASED MODULAR MULTILEVEL CONVERTER

For power semiconductor device such as IGBT/IGCT, both turn-on and turn-off can be controlled. Therefore, they can be used to make self-commutated voltage source converters. In such converters, the polarity of DC voltage is usually fixed. For this reason, an HVDC converter using IGBT/IGCT is usually referred to as a voltage-source converter. The additional controllability of power semiconductors gives many advantages, notably the ability to switch the IGBTs on and off many times per cycle in order to improve the harmonic performance. The voltage source converter no longer relies on synchronous machines in the AC system for its operation which provides many advantages compared with the line commutated thyristor-based current source converter. A voltage-sourced converter can therefore feed power to an AC network consisting only of passive loads, something which is impossible with LCC HVDC [10]. Voltage-source converters are also considerably more compact than line-commutated converters (mainly because much less harmonic filtering is needed) and are preferable to line-commutated converters in locations where space is at a premium, for example on offshore platforms. Unlike the line-commutated HVDC converters, voltage-source converters maintain a constant polarity of DC voltage and power reversal is achieved instead by reversing the direction of current. This makes voltage-source converters much easier to connect into a Multi-terminal HVDC system or "DC Grid" [09]. HVDC systems based on voltage-source converters traditionally use the six-pulse 2-level connection because the converter produces much less harmonic distortion with PWM modulation than a comparable LCC and the twelve-pulse connection is unnecessary. This simplifies the construction of the converter transformer. However, there are several different configurations of voltage-source converter and research is continuing to take place into new alternatives for example modular multilevel converter.

The concept modular multilevel converter topology based on the converters arm act as a controllable voltage source with a high number of possible discrete voltage steps, which allow forming a approximate sine wave in terms of adjustable magnitude of the voltage to the AC terminal which shown in Figure 4.1. Each of the variable voltage sources are designed with a number of identical but individually controllable submodules. Each submodule is a two-terminal component which can be switched between a state with full module voltage and as state with zero module voltage in both current direction. Dependent on the current direction, the capacitor can be charged or discharged. Besides auxiliary components and electronics, each submodule consists of an IGBT/IGCT half-bridge submodule. Series connection of submodules can be control individually and selectively. In each single phase, there are two arm which are noted by upper arm and lower arm connected in series between the dc terminals. The AC terminals located at the midpoint between the two arms shown in Figure 5.2. Each arm has twelve submodules of half -bridge converters. In each arm, an inductor is used to limit the common 2-order harmonic current and fault current during DC side pole-to-pole or pole-to-ground fault.

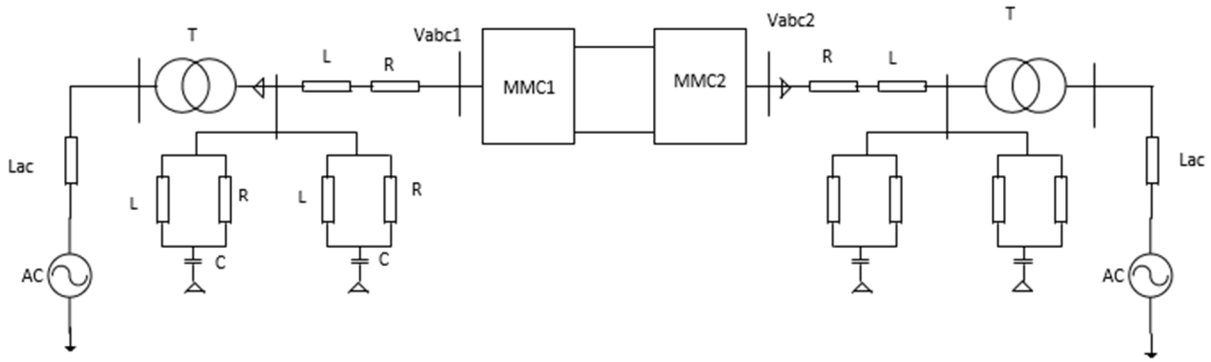


Fig: 4.1 Single line diagram of MMC HVDC [11]

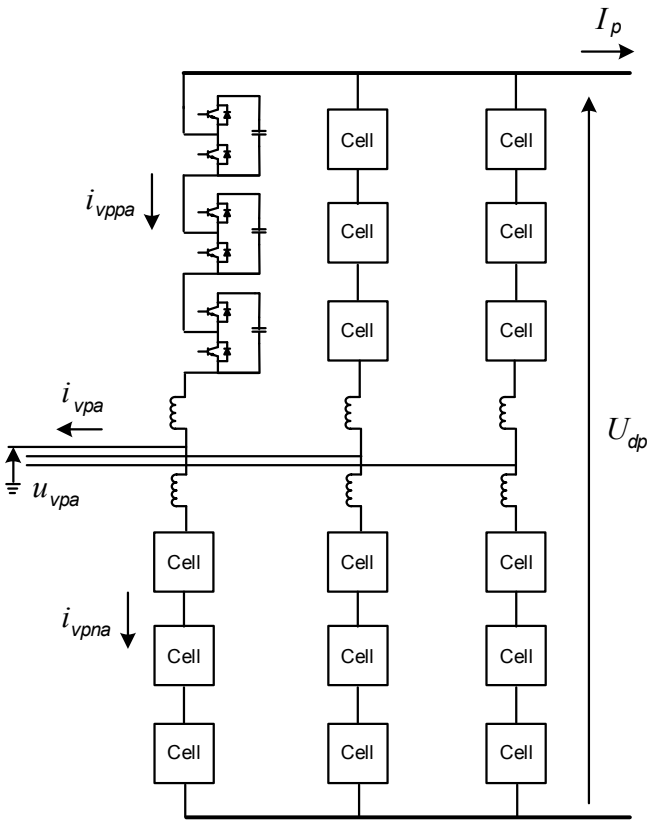


Fig: 4.2 Three-phase diagram of one sending/receiving end of MMC HVDC converter

The modeling and simulation of modular multilevel converter is performed in this chapter. Matlab/Simulink models of modular multilevel converter is built as shown in Figure 5.3 and Figure 5.4. The purpose of the simulation is to predict the dynamic response of the modular multilevel converter during normal and fault conditions. It is assumed that there are twelve submodules in each converter arm of the three phase converter system. Each submodule has a 15mF DC link capacitor with a DC voltage of 800V. The arm inductor in each arm is assumed to be 5mH. The total DC pole-to-pole voltage is 9.6kV.

4.2 Simulation model with half bridge submodule in MMC

The MMC model is built using Simulink/SimPowerSystem Toolbox. The electrical circuits are simulated by SimPowerSystem. The converter PMW modulation and control are implemented using standard Simulink blocks. The Matlab S-Funtion (discuss later) is used for programming the capacitor voltage balancing control algorithm which generates the actual IGBT switching signals for the submodules of the converter main circuits in the SimPowerSystem subsystem as shown in Figure 4.4.

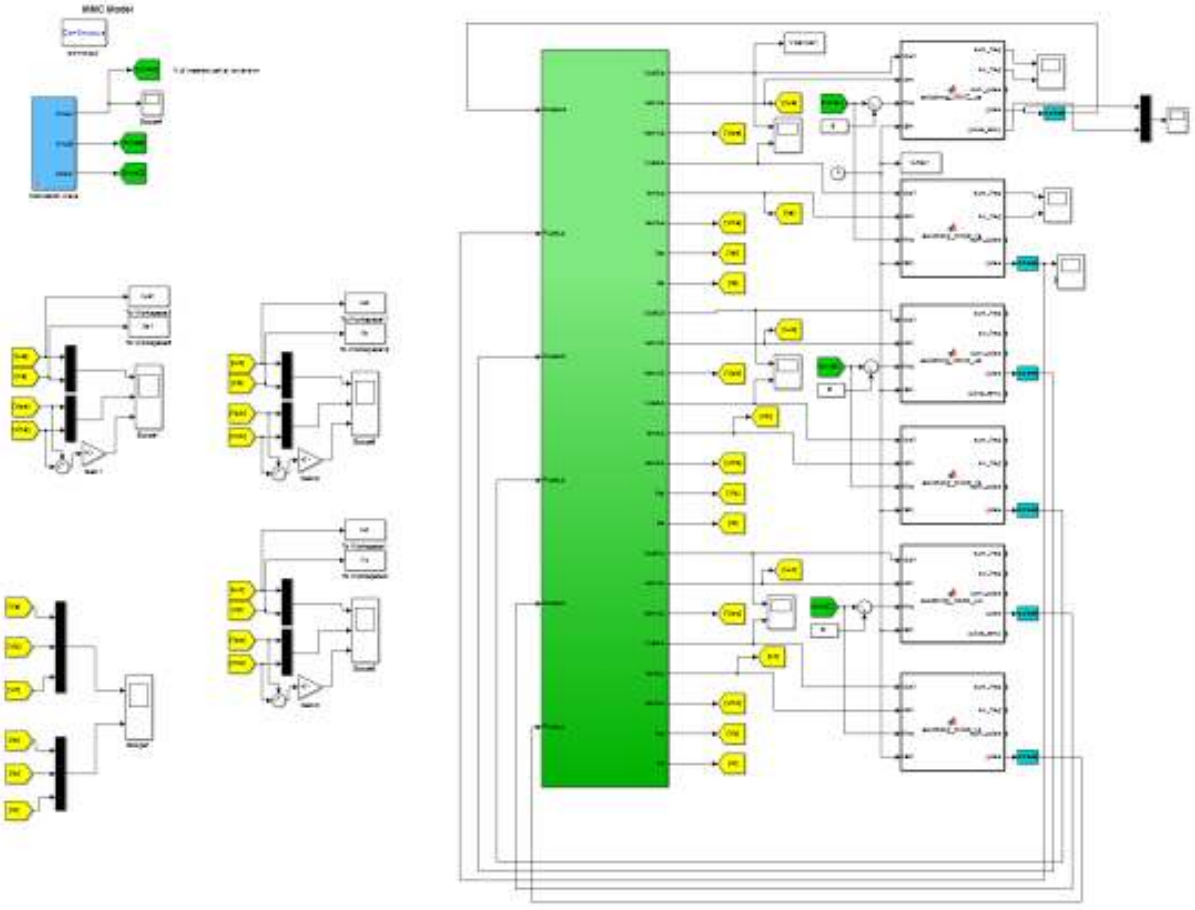
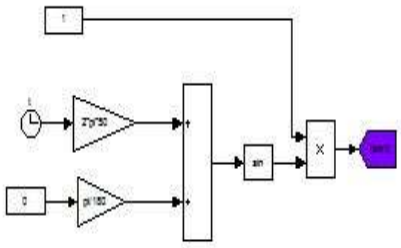


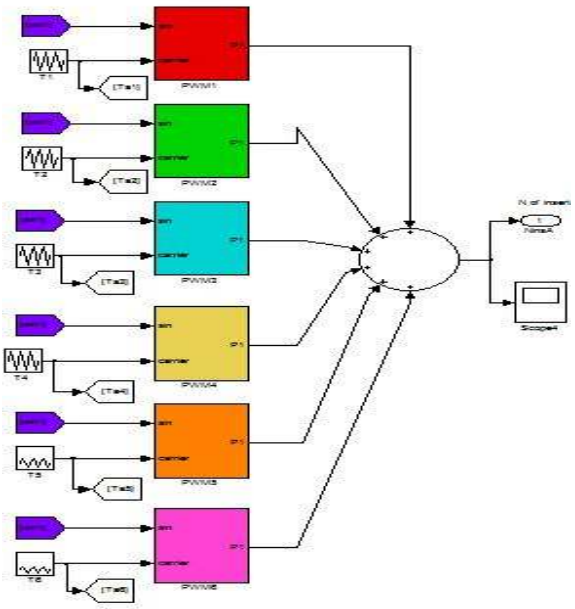
Fig: 4.3 Complete MMC model with three phase in Matlab/Simulink using SimPowerSystems

4.2.1 SPWM (Sinusoidal Pulse Width Modulation) Strategy

A level-shifted sinusoidal pulse width strategy is used for the modulation of modular multilevel converter. Level shifted PWM technique requires twelve carrier waves displaced symmetrically with respect to zero-axis as shown in Figure 4.6. The three-phase voltage references are compared with the twelve carrier waves to generate the required PWM signals as shown in Figure 4.6. The 3rd harmonic injection which is normally used for increasing the linear modulation range is not used here in the SPWM for simplicity purpose. The detailed view of the SPWM strategy is shown in Figure 4.7. In fig 4.5 showing the details view of SPWM generating with Matlab symbol.

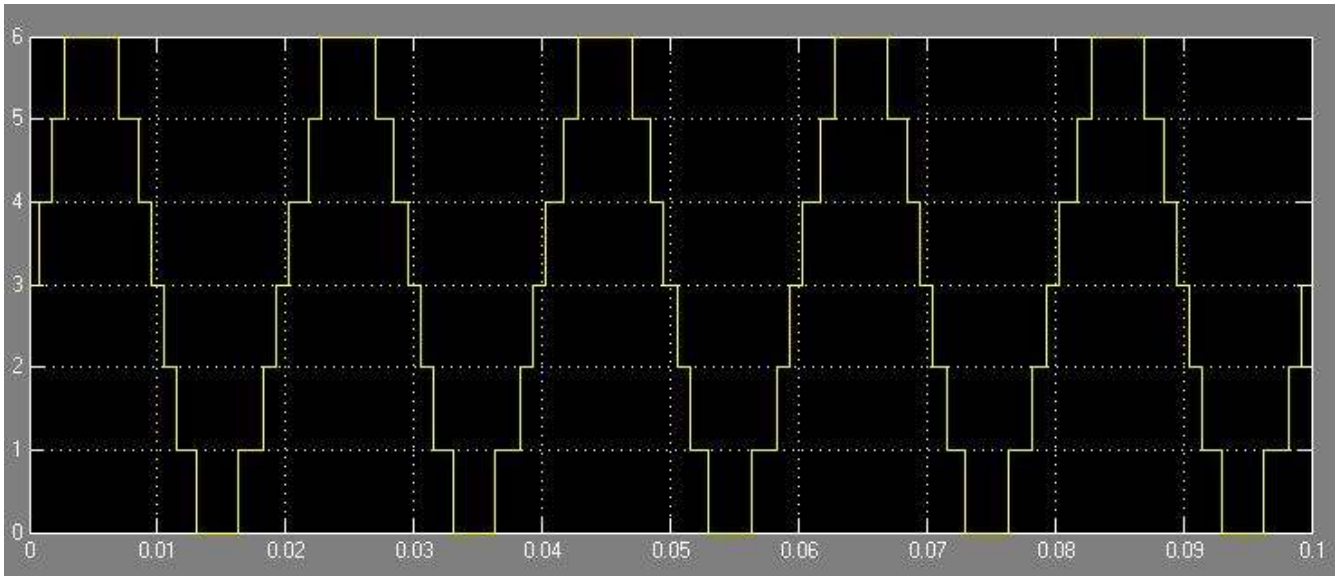


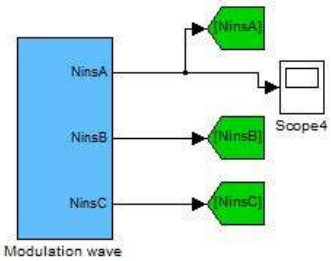
a)



b)

c)





d)

Fig: 4.4 a) Generating Sine wave, b) SPWM generating, c) Single line SPWM output, d) Modulation Wave block in Simulink

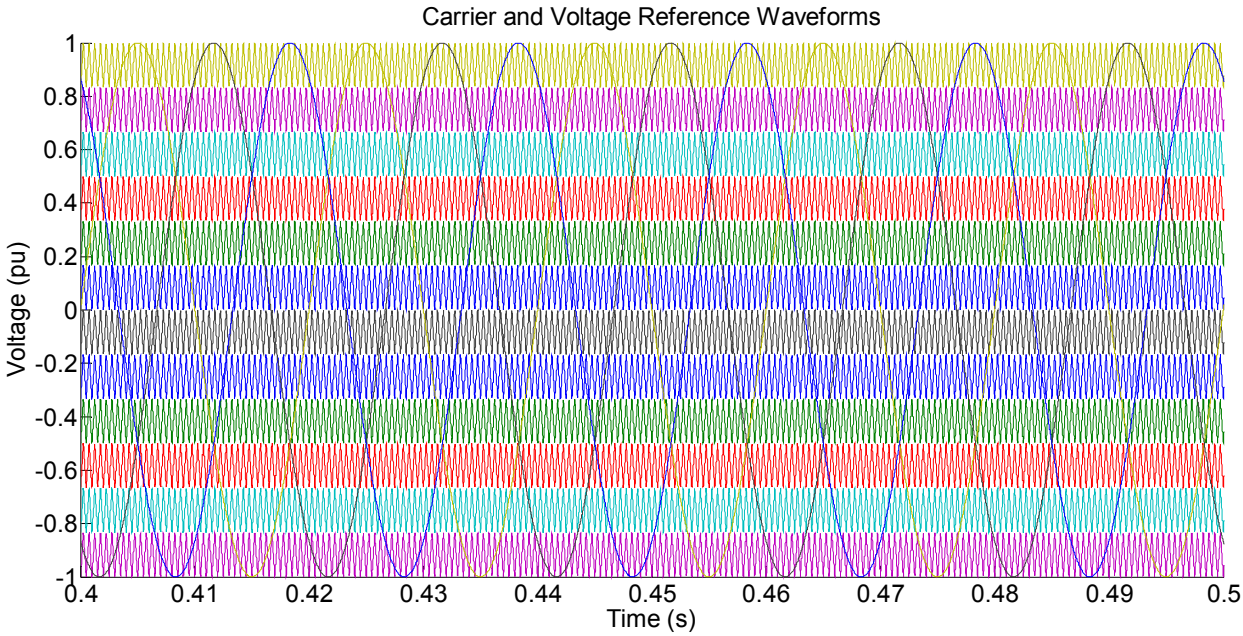


Fig: 4.5 Carrier signal and reference signal in Matlab

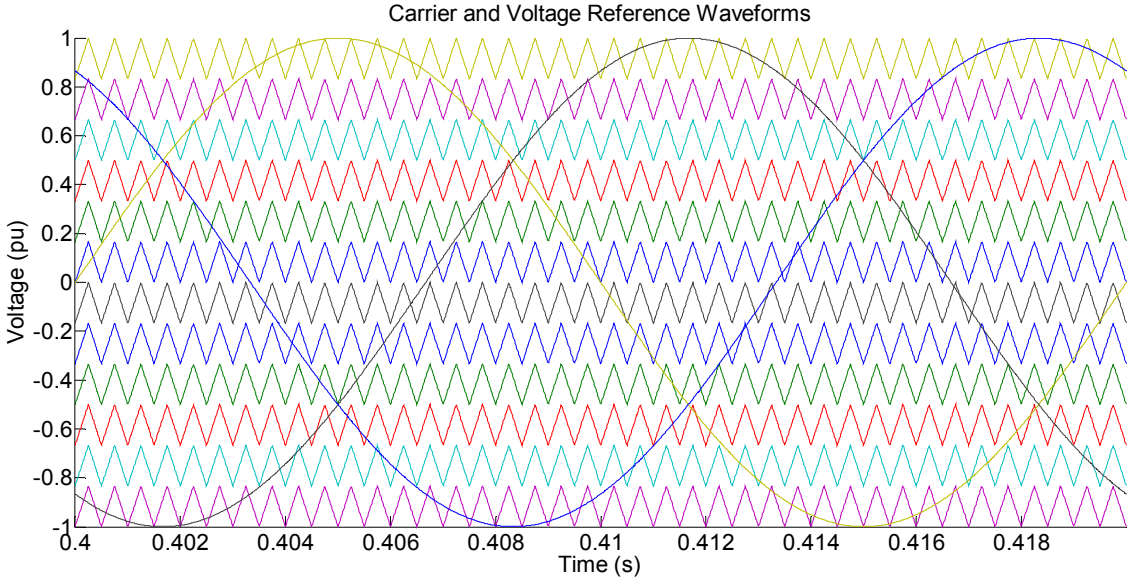


Fig: 4.6 Zoom view of carrier signal & reference signal in Matlab

The SPWM generates the numbers of submodules that needs to be inserted in the lower arms of three phases as shown in Figure 4.7. The numbers of submodules that needs to be inserted in the upper arms of the responding phases are then calculated by the total numbers of the submodules per arm subtracting the numbers of submodules inserted in the lower arms. This PWM operation strategy makes the DC pole-to-pole voltage constant if the 2-order harmonic common-mode voltage ripple is ignored. The submodule capacitors will be charged and discharged to transferred energy from DC side to AC side or vice verse. In order to void the submodule DC capacitor voltages from diverging, the converter submodule voltage balancing control is required for an MMC-based HVDC system. This is done by

sorting the submodule voltages and selectively inserting or bypassing the DC capacitors according to the arm current directions.

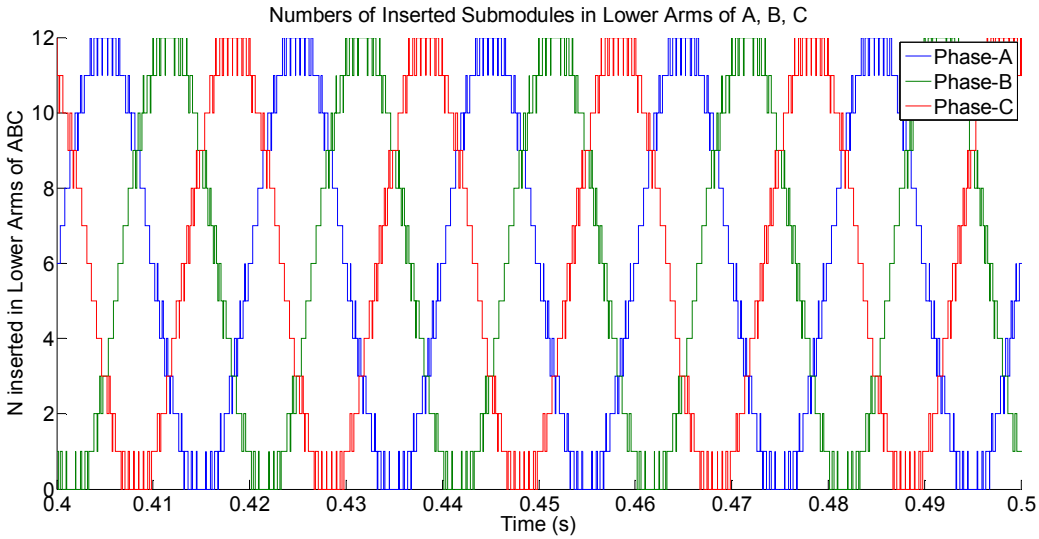
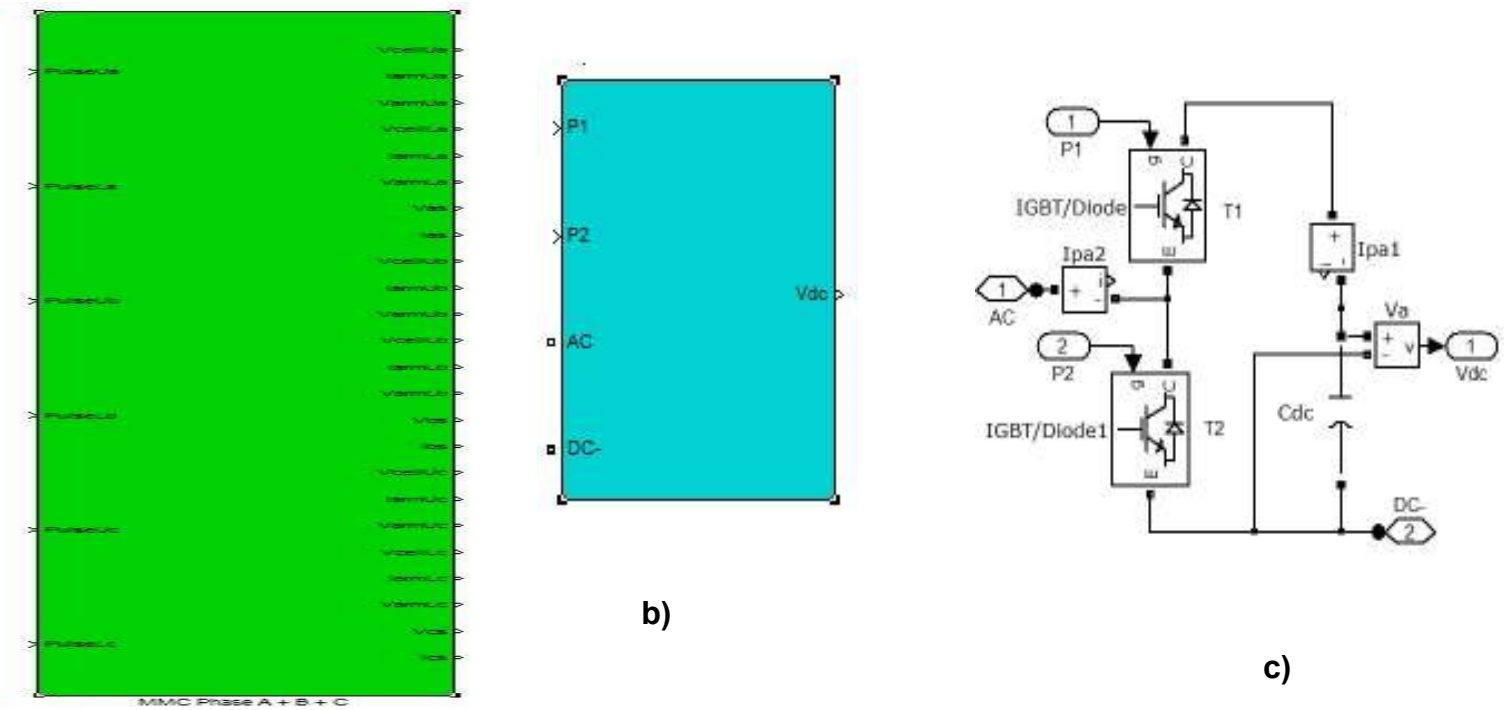


Fig: 4.7 Numbers of submodules inserted in lower arms of three phases

4.2.2 Converter Block

Inside the MMC phase subsystem, there are three phase line. Each phase consists of twelve converter cell, six cell in upper arm & six cell in lower arm.



a) **b)** **c)**

Fig: 4.8 a) MMC subsystem, b) Converter block, c) Half bridge converter with IGBT

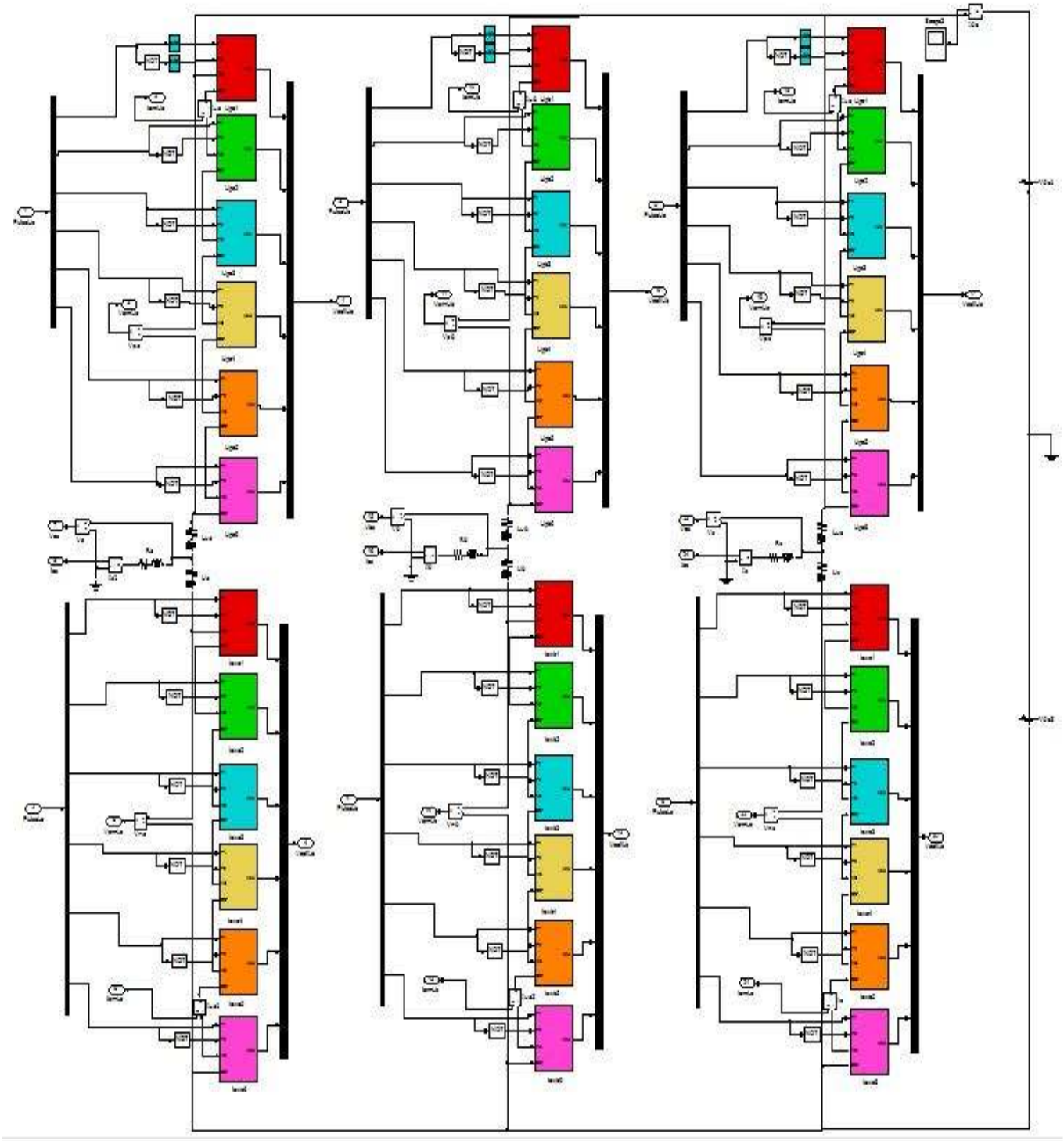


Fig: 4.9 Three phase circuit with submodule, inside of a MMC model Converter

4.2.3 S- function block

Fig 4.1 shows a single-line diagram of the study system and fig 4.2 depicts a schematic representation of the MMC based HVDC system. MMC consists of six arms where each arm includes n = 6 series –connected nominally identical, half bridge submodules. For current control & limit fault currents using a reactor in phase arms (fig 4.2 & fig 4.10). AC terminal of MMC is connected to a utility grid through RL . Basically the S-block is using for controlling the capacitor voltage & switching states. The half bridge cell where it's

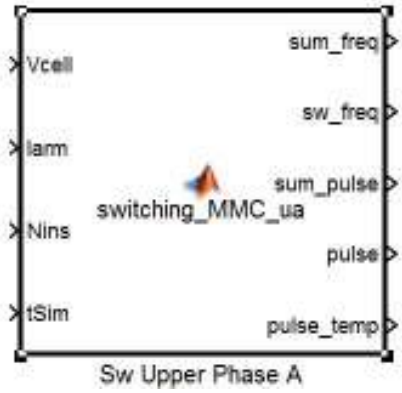


Fig: 4.10 S-function block

Output voltage equal to its capacitor voltage or zero, depending on the switching states. The switching states and the resultant voltage at the output of each submodules depend on state of switch. When switch T1 (fig 4.9c) is ON, T2 is OFF, that time resultant voltage is capacitor voltage. And when switch T1 is ON, T2 is OFF , the resultant voltage is zero.

Switching function from S-block to control which converter will be select and which one unselect. In a single phase among twelve converter cell (fig: 4.9b & fig 4.10) each time six cell will be selected. The values of upper cell & lower cell of each arm are determined by desired voltage level of phase (fig 4.7) using PD-SPWM (phase detection sinusoidal Pulse width modulation) modulator. Assuming that each SM (Sub Module) capacitor is regulated at Vc(t) = Vdc/6 a seven –level waveform at midpoint of ac-side. v_t denoted at mid-point voltage

- Level 1 : $v_t = -\frac{V_{dc}}{2}$, all of the six upper (lower) SMs are off (on) upper six is on, lower six zero.
- Level 2 : $v_t = -\frac{V_{dc}}{3}$, out of six SMs , one is on and out of six lower SMs, five are on.
- Level 3 : $v_t = -\frac{V_{dc}}{6}$, out of six SMs, two are on and out of six lower SMs, four are on.
- Level 4 : $v_t = 0$, out of six SMs, three are on and out of six lower SMs, three are on
- Level 5 : $v_t = \frac{V_{dc}}{6}$, out of six SMs, four are on and out of six lower SMs, two are on
- Level 6 : $v_t = \frac{V_{dc}}{3}$,out of six SMs, five are on and out of six lower SMs, one are on
- Level 7 : $v_t = \frac{V_{dc}}{2}$,out of six SMs are on and out of six lower SMs are zero

4.3 Simulation Results

Given the mentioned SPWM and submodule voltage balancing control method, the MMC HVDC converter was simulated. The phase-A upper and lower arm voltages are shown in Figure 5.8. The arm voltages have DC components superimposed with AC components. When adding the two arm voltages, the resulted common-mode voltage is equal to the DC pole-to-pole voltage subtracting the arm inductor voltage. When subtracting the two arm voltages, the differential mode voltage is equal to two folds of the AC phase voltage. Compared with Figure 5.7, it is shown that the simulated arm voltages are consistent with the numbers of submodules generated the SPWM strategy. It is also noticed from Figure 5.8 that the levels of the arm voltages are thirteen which is corresponding to the total numbers of the submodules in one arm. Due to the submodule capacitor voltage variation, the DC voltage levels are slightly drifted as shown in Figure 5.8. The higher converter voltage outputs from the arm, the more pronounced the arm voltage drifting. The voltage drifting is characterized by 2rd order harmonics and is caused by the capacitor energy exchange between the submodules. Therefore, it is typical for modular multilevel converters. More advanced modulation methods can be used to reduce the submodule capacitor voltage ripples and thus the size of the submodule capacitors.

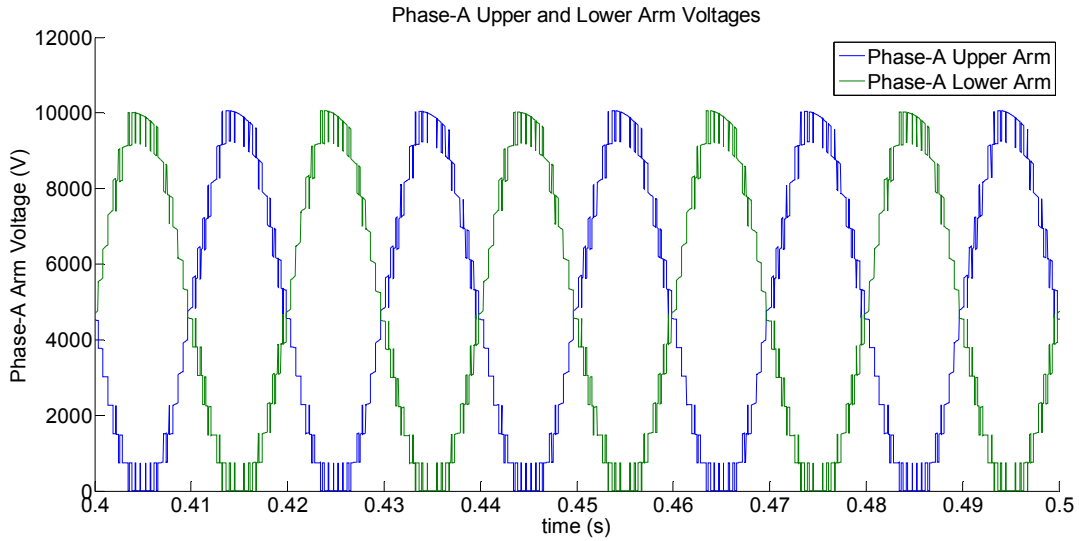


Fig: 4.11 Upper and lower arm voltages of phase-A

The arm currents of phase-A is shown in Figure 4.9. It is observed from Figure 4.9 that the upper and lower arm currents include DC and fundamental frequency AC current. It can be derived that the arm currents are composed of one third of the total DC current and half of the AC phase current. The 2rd harmonic circulating currents also exist in the arm currents which are generated by the 2rd harmonic voltages of the capacitor voltage ripples.

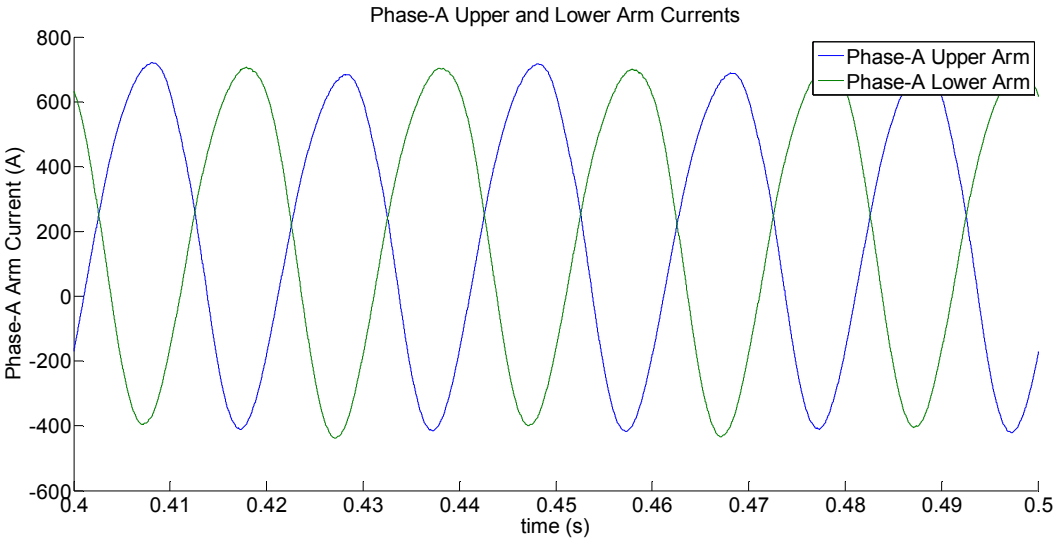


Fig: 4.12 Upper and lower arm currents of phase-A

The three-phase AC line-to-line output voltages are shown in Figure 4.10. It is observed in Figure 4.10 that the output voltage is very much sinusoidal with low harmonic distortion which is one of the main benefits of MMC converter. The three-phase output currents are shown in Figure 4.11. Due to the relatively large inductive loading, the phase currents are much smoother than the phase voltages without noticeable switching side-band harmonics.

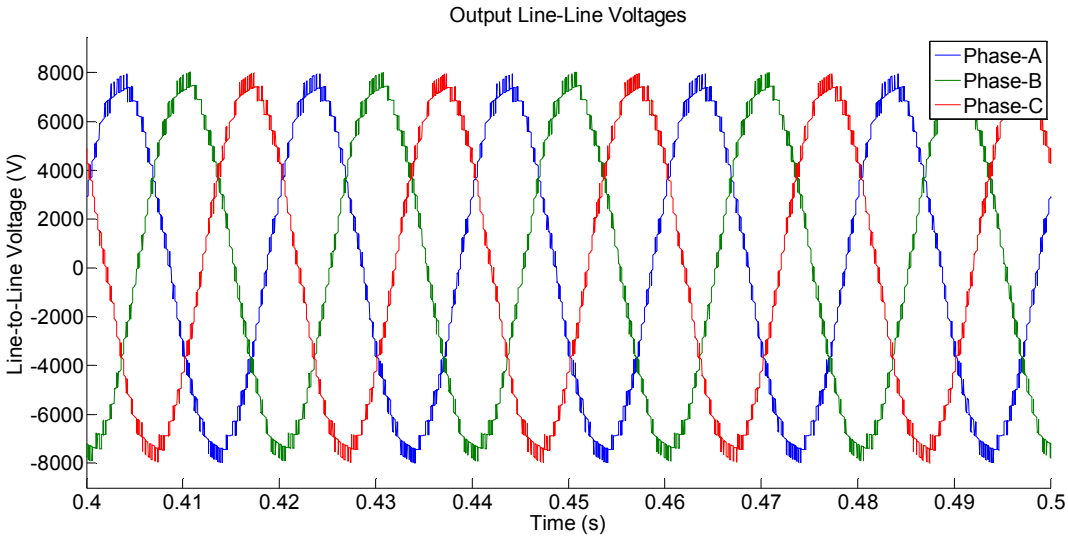


Fig: 4.13 Three-phase line-to-line voltages of MMC converter

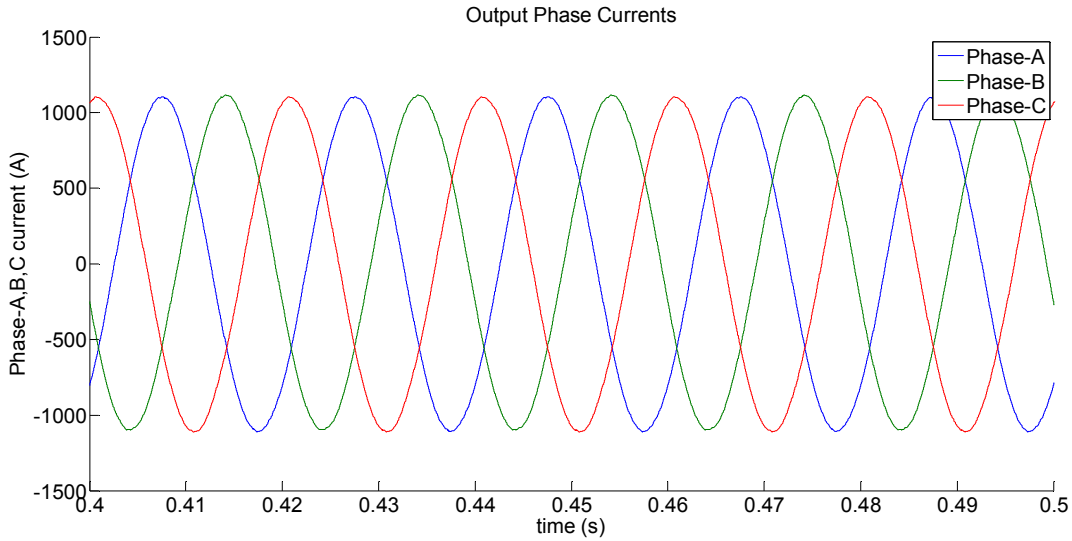


Fig: 4.14 Three-phase currents of MMC converter

The total phase-A arm voltage is shown in Figure 4.12, As it is stated earlier, it represents the common-mode voltage that is characterized by the DC pole-to-pole voltage together with the 2rd order harmonic voltage of the arm inductor. This 2rd order harmonic voltage generates 2rd harmonic circulating currents in the converter arm that should be filtered out or mitigated by advanced modulation and control schemes.

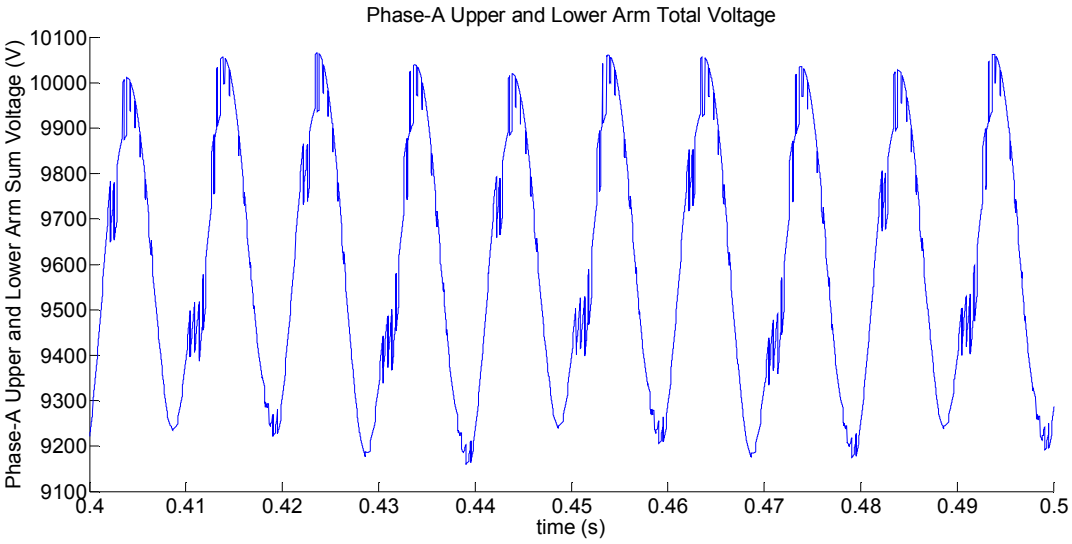


Fig: 4.15 Phase-A upper and lower arm total voltage

The converter submodule voltages of Phase-A are shown in Figures 4.13 and 4.14. It is observed from Figures 4.13 and 4.14 that the capacitors are charged and discharged where the capacitor energy of each submodule maintains constant. Therefore, the capacitor voltages are well balanced which verifies the effectiveness of the capacitor balancing control.

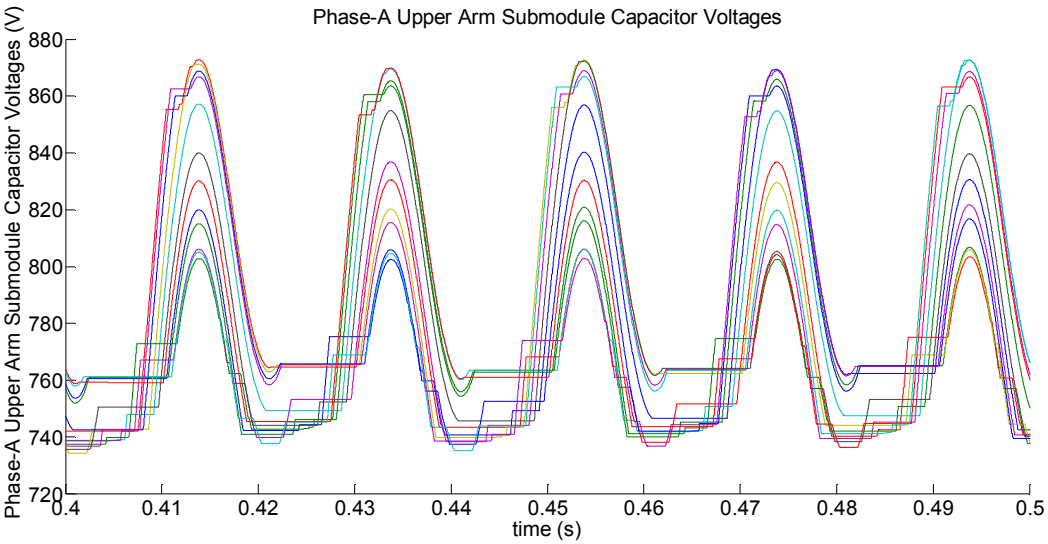


Fig: 4.16 Phase-A upper arm submodule capacitor voltages

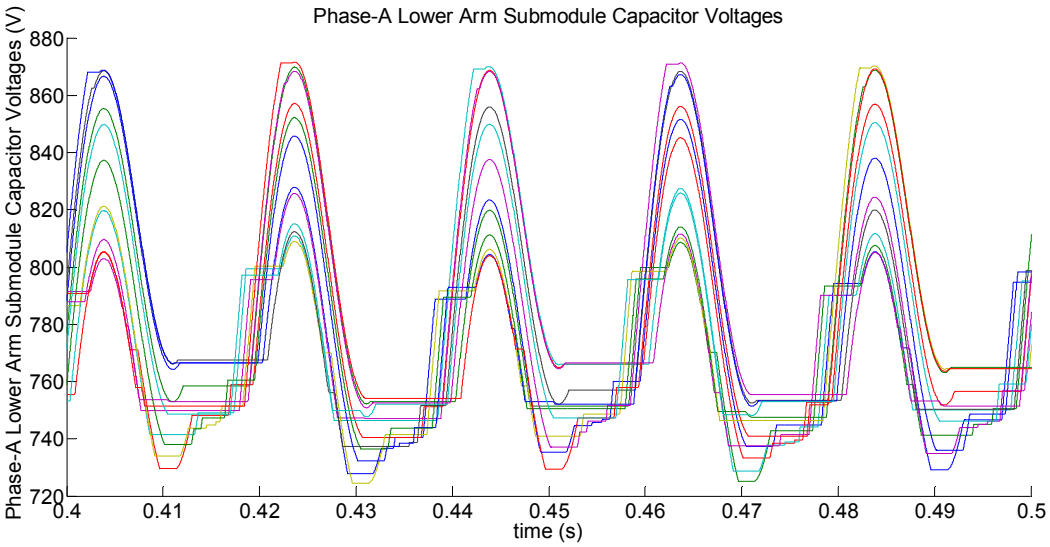


Fig: 4.17 Phase-A lower arm submodule capacitor voltages

The semiconductor currents of the two IGBT positions inside one half-bridge submodule are shown in Figure 4.15 and 4.16. In Figure 4.15, it is observed that the switching frequency for one submodule is very low which results in low switching losses. This is one of the main advantage of MMC converter compared with 2- or 3-level converters that use a few kHz switching frequency and thus induce high switching losses.

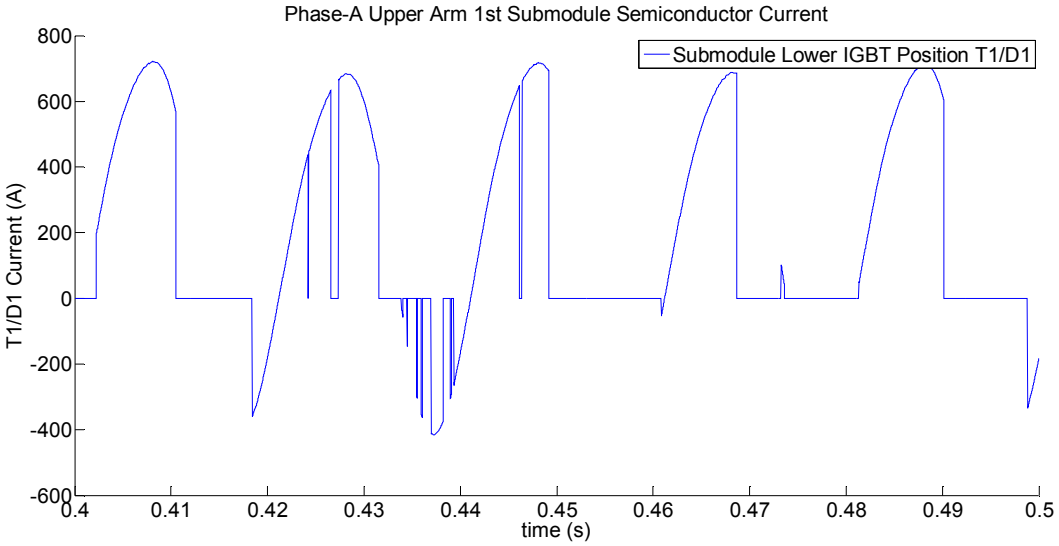


Fig: 4.18 Semiconductor switch T1/D1 current

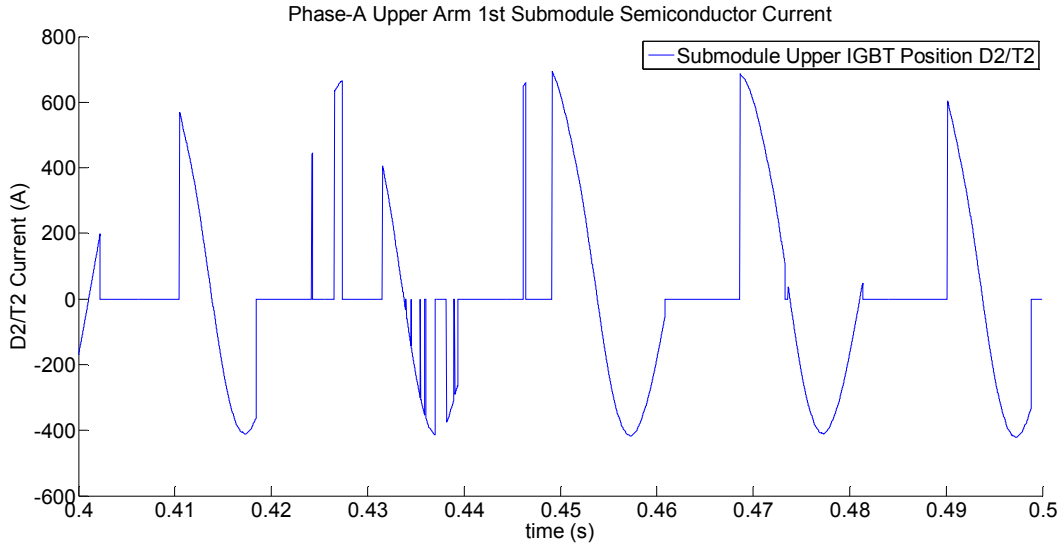


Fig: 4.19 Semiconductor switch T2/D2 current

5 CONCLUSIONS

This thesis presents the converter cell design with IGCTs for HVDC applications. Half- and full-bridge cells, which are the basic building blocks of MMC converters, are used. The IGCT semiconductor static and dynamic switching behaviors are investigated together with their clamping circuit. The semiconductor losses for MMC converters with half- and full-bridge cells are evaluated. The converter cell mechanical designs are illustrated based on modular concept. The MMC converter is simulated in Matlab/Simulink. The detailed modulation and control methods of MMC converter are analyzed and presented.

6 FUTURE WORK

The existing IGCTs (asymmetric, conducting and reverse blocking) cover a huge range of application at medium voltage levels (medium voltage drives, static circuit breaker, DVRs, DUPS, SMES, BESS, etc.) with different conversion structures. Future research & development efforts are carried on to improve the IGCTs performance and to expand their field of application. Dual gate principle [17] consists on the use of a second gate driver to control the IGCT gate-anode voltage (the base emitter voltage of the PNP equivalent in the thyristor type structure). The second gate driver will be able to eliminate the IGCT tail current at turn-off, considerably reducing the switching losses of the component, whereas using a symmetric structure can also provide a considerable reduction of the on-state losses. Anode gate control may offer additional degree of freedom for series connection and reduction of snubber requirement could be achieved. The reduction of the switching losses provided by dual gate principle if we applied to future more than 10kV IGCTs.

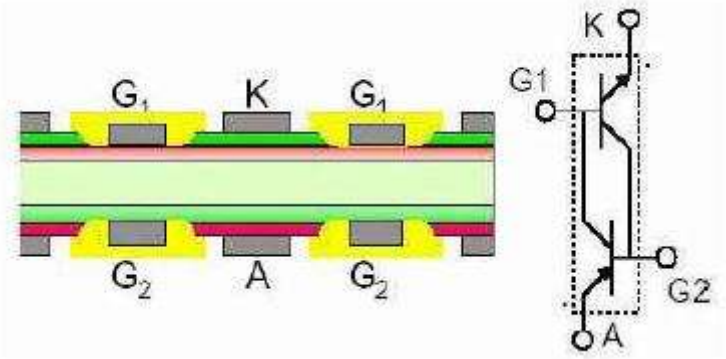


Fig: 6 Semiconductor structure of a ‘symmetrical Dual Gate IGCT’

The MMC converter with full-bridge submodules should be simulated for normal condition and DC side pole-to-pole or pole-to-ground fault condition. The use of full-bridge submodule can block the DC side fault therefore increasing the reliability of the converter operation.

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