School of Industrial and Information Engineering

POLITECNICO DI MILANO

Three-level Neutral-Point-Clamped Voltage Source Converters for Renewable Energy Systems: Modeling, Operation and Control

Master's Thesis in Electrical Engineering

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Mahdi Fakharmanesh

Abstract

Renewable energy sources are attracted a great deal of interest in recent years since they are clean, endless and always available. Widely used power converters in renewable energy sources are back-to-back converters included a AC-DC side, a DC-link capacitor and a DC-AC side. Multilevel voltage source inverters are used in the DC-AC side that can reach high voltages with low harmonics. By using appropriate modulation schemes, they can provide higher performance and higher efficiency than the traditional converters.

Power losses are a serious subject in voltage source inverter. In order to improve the efficiency of systems, we should decrease the power losses in the semiconductor devices.

The thesis finds a mathematical model of conduction and switching power losses in diodes, IGBTs and MOSFETs. Afterwards, we give an overview on two-level and three-level neutral point clamped converter topologies and try to model properly these converters.Then, instantaneous power losses in both inverters are investigated. The next step is to give an overview of modulation schemes such as pulse width modulation (PWM) and space vector modulation (SVM). Then we try to improve SVM to reduce switching power losses by finding the time intervals that the phase currents reach their maximum values and prevent switching during these time intervals. At the end, the models are simulated and the results are compared with each other.

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Chapter 1

Introduction

1.1 Introduction

Energy plays an important role in our life. As the world's populations is growing, the energy consumption increases. Research shows the total demand for energy will increase by 21% by 2030 [6].

Nowadays, fossil fuels such as natural gas and oil are usual energy sources. They are non-renewable energy sources formed by natural processes. This means that these sources take billion of years to be formed. Therefore, the rate of energy use is considerable more than the fossil energy formations. In addition to this, when the fossil fuels burn, they contribute largely to greenhouse gas emissions. To tackle the energy shortage and the pollution problem, we can use renewable energy sources. Therefore, the renewable energy sources are of concern for researchers. The renewable energy sources are more sustainable, reliable and more stable sources. The most interesting renewable sources are supplied by the sun such as wind energy or the solar energy.

Changes in the amount of sunlight arriving to different areas cause the temperature to change. The temperature variations cause changes in atmospheric pressure. Differences in atmospheric pressure create wind energy. Therefore, wind is an indirect type of solar energy. Wind turbines convert the wind into electrical energy. Wind turbines are mounted on tall towers where the wind is faster and less turbulent. The generator is connected to blades by a gear. The generator produces electricity energy when the blades turn. This energy is converted into the desirable AC energy by back to back converters (see Fig. 1.1 and Fig. 1.2) and filters.

Photovoltaics are other energy source. In this way, photo-voltaic panels convert light into electricity. If the intensity of the light is increased, the power is generated by the photo-voltaic panels. The photo-voltaic panels produce DC electricity. Therefore, a converter is also needed to convert DC voltage to AC voltage to be connected to the electrical grid. In practice, photo-voltaic can be connected to voltage source inverters to supply AC electricity or be connected to a battery to store the energy.

Wind turbines produce the electricity. The frequency and voltage, which are produced by the generator, can not be directly connected to the grid system. Moreover, the photovoltaic panels generate DC electricity. Therefore, it is essential to have some strategies in order to improve the power quality of the power system and be able to connect renewable energy sources to the power system. Thus, modern power electronic technology plays an important role in the integration of the renewable energy sources to the AC grid. Therefore, it is necessary to find out the effective technologies for the renewable generation systems. The conversion of either an input DC power or an input AC power at a given frequency and voltage to an output power at desired frequency and voltage can be obtained with power converters. Various power converters have been developed to fulfil the requirements of the renewable energy generation. Each of them has some benefits and some drawbacks.

Widely used power converters in renewable energy systems are back-to-back converters. It is composed of a controlled rectifier and a controlled inverter. The controlled rectifier has a bidirectional power flow capability. The decoupling capacitor between rectifier side and inverter side provides independent control capability of the two converters. The traditional converter is back-to-back connected two-level converter (see Fig. 1.1). It converts the input voltage into the two-level output voltage. Other type of the back-to-back converter is the three-level back-to-back converter (see Fig. 1.2). The output voltage of this converter is smoother due to the three output voltage levels.

For an efficiency point of view, a comparison of power losses in the two-level versus the three-level inverter is included. The total power losses of semiconductor devices are divided into the conduction losses and the switching losses [3]. The conduction losses can be obtained based on the voltage-current characteristics (v-i) of the semiconductor devices. The switching losses are calculated by using the switching energy losses given in the datasheets. Moreover, the modulation schemes in both converter should be investigated to find the best solution.

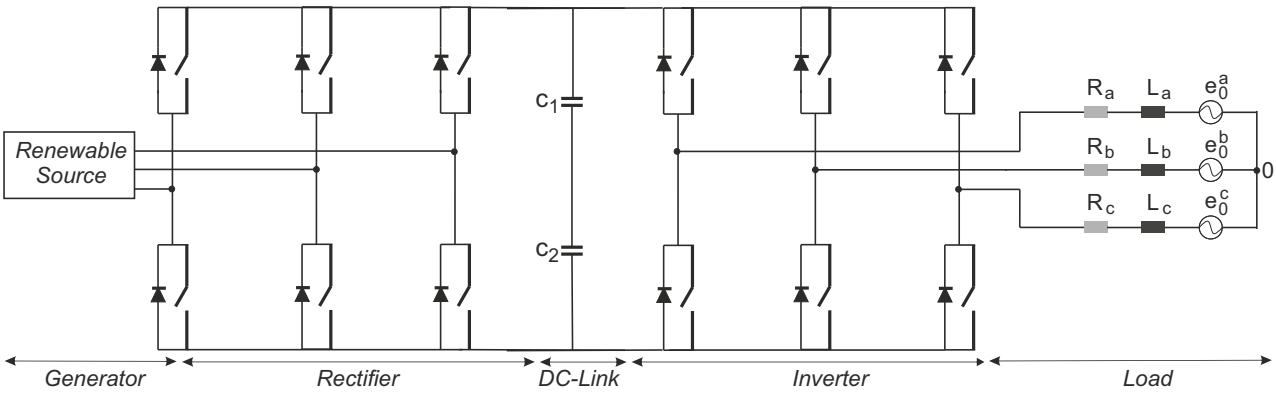


Figure 1.1: Schematic circuit of two-level back-to-back converter.

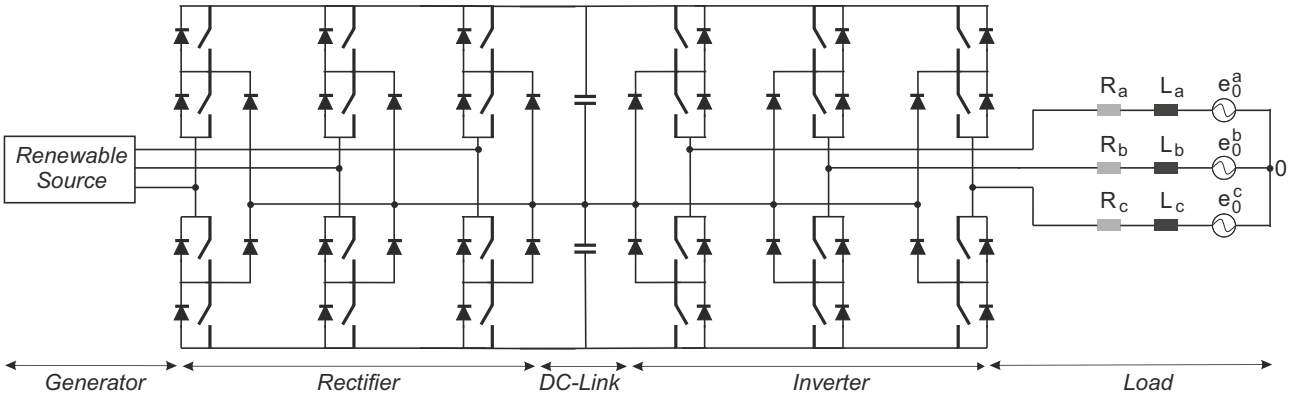


Figure 1.2: Schematic circuit of three-level back-to-back converter.

1.1.1 Thesis Objectives

The objectives of the thesis can be summarised as follows:

1. Overview of the semiconductors devices and their power losses (Chapter 2).
2. Model of both the two-level voltage source inverter and three-level neutral point clamped voltage source inverter (Chapter 3).
3. Model of the power losses of both the 2-level voltage source inverter and three-level neutral point clamped voltage source inverter (Chapters 3).
4. Investigatation of modulation techniques for three-level neutral point clamped voltage source inverter (Chapter 4).
5. Simulatation of the performance and comparison of the efficiencies (Chapter 5).

1.1.2 Thesis Organization

This thesis is organized by chapters in the following way.

1. Chapter one introduces the motivation of this thesis.
2. Chapter two focuses on the power losses in the power diodes, the IGBTs and the MOSFETs, along with their features and applications.
3. Chapter three gives a mathematical model of the two-level VSI and three-level NPC VSI and their losses.
4. Chapter four gives an overview on the modulation techniques such as pulse width modulation (PWM) and space vector modulation (SVM) for 3-level NPC VSI.

5. Chapter five focuses on the simulation and comparison of the efficiency in 2-level VSI and 3-level NPC VSI.

6. Chapter six concludes the results obtained from the previous chapters.

Chapter 2

Modeling of Conduction and Switching Losses

Nowadays, inverters are used to convert DC waveform to AC waveform. An ideal inverter provides the desirable voltage\current waveform by turning the switches on and off. During each switching period T_s $[s]$, the switch conducts for a time up to t_{ON} $(0 \leq t_{ON} \leq T_s)$ and remains off for the rest of the period. Fig. 2.1 shows one leg of two types of voltage source inverters. They are composed of a set of switches and diodes. In an ideal power semiconductor device, the voltage drop across the switch is zero when it conducts, therefore, there are no power losses. Correspondingly, during off-state, the leakage current in the ideal power switch is zero. Therefore, the switch has no off-state power losses. Besides, it is assumed that the power switch makes the transition between the on-state and off-state instantaneously. Hence, there are no switching power losses either. However in practice, due to the semiconductor's physical structure, the semiconductor devices have power losses during both on-state and off-state, and the switching performances.
In this chapter, the conduction and the switching losses of diodes, MOSFETs and IGBTs are discussed. Afterwards, the model of losses are found from the voltage-current characteristics (v-i) of the semiconductor devices.

2.1 Power Diode

In the voltage source inverters (VSIs), we use diodes for many reasons. The most important reason is to protect the switch from the reverse current damage caused by inductive loads. In power electronics, there are two important types of power diodes, one of them is the Schottky diode and the other is the P-i-N diode. The Schottky diode is composed of a metal and a semiconductor drift region. It is a uni-polar device with fast switching behavior. It is used in low voltage applications, because the conduction resistance will be increased for higher break down voltage. Hence, for high voltage it is substituted by a P-i-N diodes [3]. The P-i-N

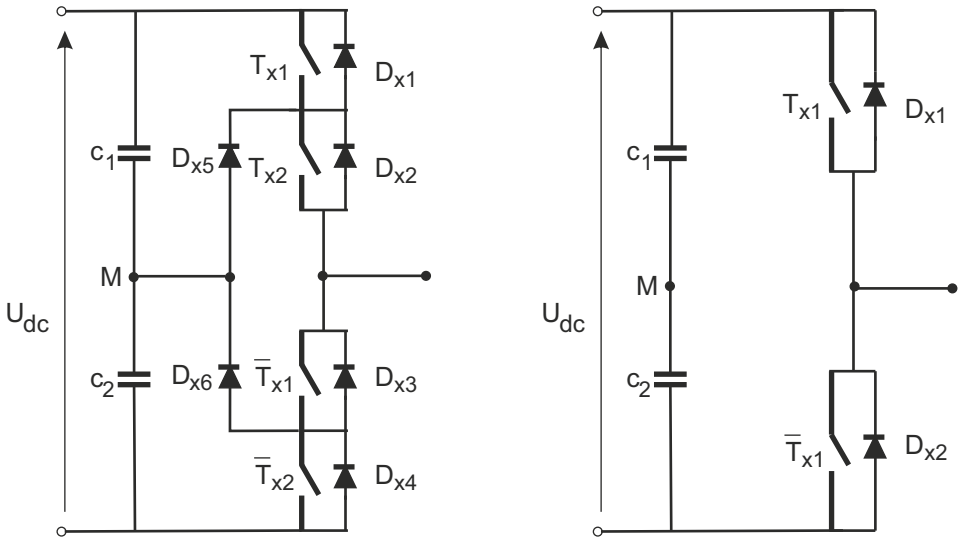


Figure 2.1: One leg of 2-L VSI and 3-L NPC VSI typologies.

diode is composed of the anode, the N-drift region and the cathode. The cathode is a highly N doped region; the N-drift is a low doped concentration N region, N-drift is grown over the cathode and the anode is a highly P doped region. The N-drift region allows the P-i-N diode to block large reverse voltages depending on its low doping and width. Therefore, the P-i-N diode is used for the high voltage converters, because it is lightly doped in the N-drift region. The P-i-N diode drawback is its significant switching losses. Fig. 2.2 shows the schematic symbol of a diode during on-state,where $i_f(t)$ $[A]$ and $u_f(t)$ $[V]$ are the current and the voltage during conduction respectively.

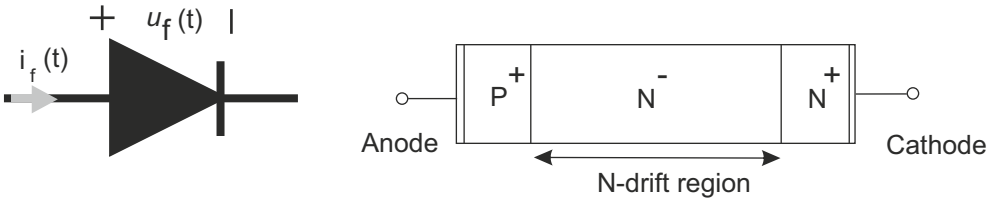


Figure 2.2: Schematic symbol of a diode.

In a power diode, we have four types of power losses. They are on-state power loss, off-state power loss, forward recovery loss, and reverse recovery loss [3]. The first one is on-state power loss. It occurs because of the voltage drop during the conduction. Secondly, power loss appears due to the leakage current in the reverse mode. The leakage current is small, therefore, it is considered insignificant [3]. Third and fourth, the switching losses arise when turning the diode on and off. In these cases, the diode is faced with transients called switching performances. At these stages, the diode has two situations; one of them is when

the diode must be rapidly switched from the blocking state to the on-state. In this case, there is a jump in the voltage across the diode. This is because, in the N-drift region, there is no extra charge. Therefore, the impedance of the diode is high, hence the maximum forward voltage drop U_{FP} $[V]$ across the diode is very high [3]. When the drop voltage across the diode reaches the turn-on voltage U_{on} $[V]$ the forward current reaches the turn-on current I_f $[A]$. This phenomenon is referred to as the forward recovery (Fig. 2.3). The forward recovery occurs in very small interval time. Therefore, we can consider it insignificant [3].

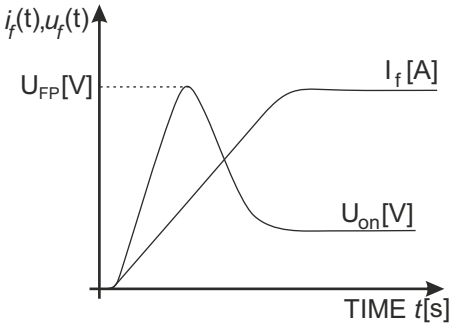


Figure 2.3: Forward recovery in a power diode (based on Fig. 1 in [1]).

The last type of loss occurs when the stored charges within the N-drift region of the diode must be extracted before the diode is able to support the reverse voltage U_R $[V]$. Reverse recovery time t_{rr} $[s]$ is defined as the time between the zero crossing of the forward current to the time. This produces a large reverse current for a short reverse recovery time duration called the reverse recovery. Fig. 2.4 shows the reverse recovery procedure in the diode.

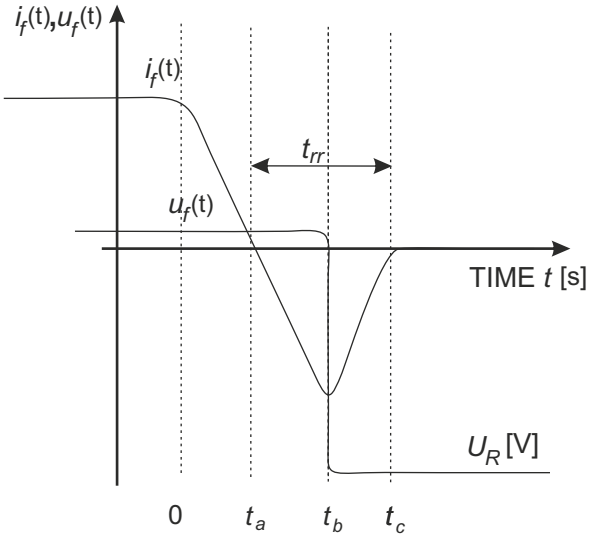


Figure 2.4: Reverse recovery in a power diode (based on Fig. 5 in [2]).

Both the reverse recovery and the forward recovery occur during a very short time, however both of them are large. These are caused the big losses referred to as the switching losses.

An ideal v-i characteristic of a P-i-N diode is depicted in Fig. 2.5. The diode has no voltage drop across when it conducts. Moreover, there is no leakage current flowing through the diode when it is in the off-state mode. In addition to these, electrons and holes are instantaneously depleted from the N-drift regions resulting to no switching losses in the diode.

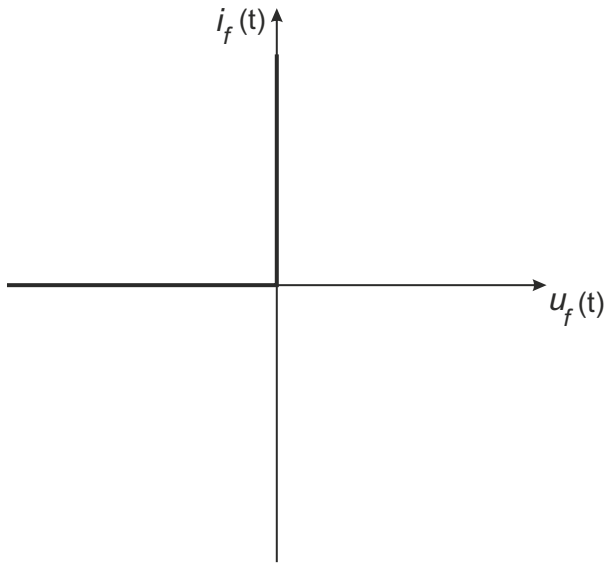


Figure 2.5: An ideal characteristic of power diode.

In practice, the diode has non-ideal behavior which means the diode has the voltage drop during the conduction mode and the reverse current during the off-state. Similarly, the diode has the switching losses when the diode is turning on or off (see Fig. 2.6). The overall power losses $p_{tl-D}\left(\vartheta_J(t), t\right)$ are given by [3]

$$p_{tl-D}\left(\vartheta_J(t), t\right) = p_{on-D}\left(\vartheta_J(t), t\right) + \underbrace{p_{off-D}\left(\vartheta_J(t), t\right)}_{\approx 0} + p_{rr-D}\left(\vartheta_J(t), t\right) + \underbrace{p_{fr-D}\left(\vartheta_J(t), t\right)}_{\approx 0}. \tag{2.1}$$

where $p_{on-D}\left(\vartheta_J(t), t\right)$ $[W]$ is the power loss during the on-state mode, $p_{off-D}\left(\vartheta_J(t), t\right)$ $[W]$ is the power loss during the off-state mode, $p_{rr-D}\left(\vartheta_J(t), t\right)$ $[W]$ is the switching loss during reverse recovery of the diode, $p_{fr-D}\left(\vartheta_J(t), t\right)$ $[W]$ is switching loss during the forward recovery, ϑ_J $[K]$ refers to the junction temperature (see appendix A) and t $[s]$ stands for time .

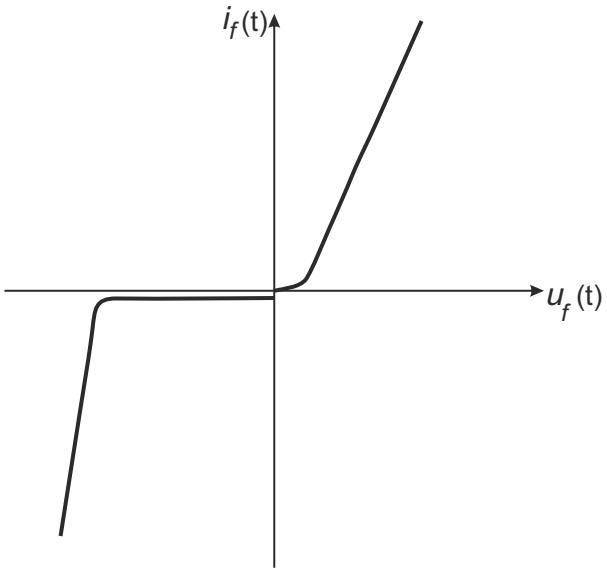


Figure 2.6: Characteristics of a typical power diode (based on Fig. 1 in [2]).

2.1.1 Conduction Losses of the Diode ($p_{on-D}\left(\vartheta_J(t), t\right)$)

When the diode is in the forward mode, the on-state loss appears in a diode due to the on-state voltage drop U_{on}. We use the v-i characteristic of the diode to model the on-state power loss. Fig. 2.7 shows the relationship between the forward voltage $u_f(t)$ $[V]$ and the current density $j_f(t)$ $[\frac{A}{cm^2}]$ of the diode based on the injection levels. The forward density current increases in the three stages. At very low current density phase, the recombination process within the space-charge layer of the P–N junction makes the current. In this phase, the on-state current density is exponentially proportional to the voltage, i.e. $j_f \propto e^{(\frac{qu_f}{2k\vartheta_J})}$, where q $[C]$ is the electron charge, k $[\frac{J}{K}]$ is the Boltzmann's constant (Its unit is joule over kelvin) and ϑ_J $[K]$ is the absolute junction temperature . Under the low-level injection phase, the diffusion of minority carriers injected into the N-drift region is dominating. Therefore, the current density occurs by the diffusion. In this condition, the on-state current density is exponentially proportional to the forward voltage, i.e. $j_f \propto e^{(\frac{qu_f}{k\vartheta_J})}$. With further increase in the on-state current density, the presence of a high concentration of both electrons and holes in the N-drift region makes high-level injection current density. The current density becomes exponentially proportional to the voltage, i.e. $j_f \propto e^{(\frac{qu_f}{2k\vartheta_J})}$ [3].

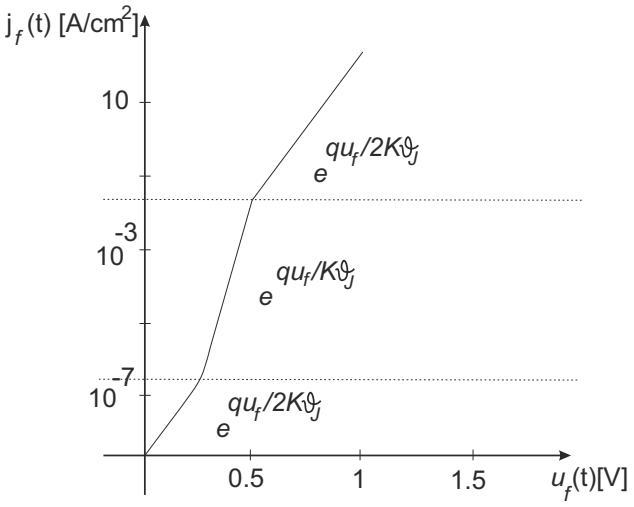


Figure 2.7: An ideal characteristic of power diode (based on Fig. 5.7 in [3]).

The on-state loss is the main part of the total power losses. Therefore, it is important to accurately estimate the on-state loss. The exact model of the on-state losses can be found by calculating the precise relationship between the forward current and the on-state voltage. However, the intrinsic parameters of the diode are not available in the datasheets. The v-i characteristic of the diode is available in the datasheets. Therefore, the on-state losses can be calculated with the approximation between the on-state current and the on-state voltage. Fig. 2.8 shows this approximation by linearization.

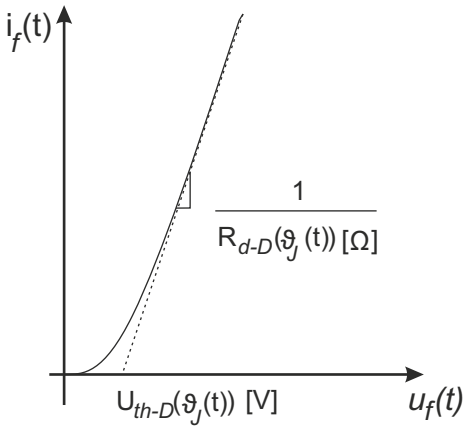


Figure 2.8: Forward characteristic of a typical diode.

As it can be seen, the forward characteristic of the diode can be linearized by the dy-

namic resistance $R_{d-D}(\vartheta_J(t))$ $[\Omega]$ and the threshold voltage $U_{th-D}(\vartheta_J(t))$ $[V]$ for the diode. The dynamic resistance is the inverse slope of the v-i characteristic of the diode and the threshold voltage is where the diode starts conducting. Both of these parameters are dependent on the junction temperature, which means by increasing the junction temperature, the threshold voltage decreases while the dynamic resistance increases. These relationships can be expressed by [7], [8]

$$U_{th-D}\left(\vartheta_J\left(t\right)\right) = \frac{U_{th-D}(\vartheta_{J-max})\vartheta_{J-min} - U_{th-D}(\vartheta_{J-min})\vartheta_{J-max}}{\vartheta_{J-min} - \vartheta_{J-max}} + [\frac{U_{th-D}(\vartheta_{J-min}) - U_{th-D}(\vartheta_{J-max})}{\vartheta_{J-min} - \vartheta_{J-max}}]\vartheta_J(t), \tag{2.2}$$

and

$$R_{d-D}\left(\vartheta_J\left(t\right)\right) = \frac{R_{d-D}(\vartheta_{J-max})\vartheta_{J-min} - R_{d-D}(\vartheta_{J-min})\vartheta_{J-max}}{\vartheta_{J-min} - \vartheta_{J-max}} + [\frac{R_{d-D}(\vartheta_{J-min}) - R_{d-D}(\vartheta_{J-max})}{\vartheta_{J-min} - \vartheta_{J-max}}]\vartheta_J(t). \tag{2.3}$$

where ϑ_{J-min} $[K]$ and ϑ_{J-max} $[K]$ are the minimum temperature and the maximum temperature of v-i characteristics given in the datasheet respectively, $U_{th-D}(\vartheta_{J-min})$ $[V]$ and $U_{th-D}(\vartheta_{J-max})$ $[V]$ are the threshold voltage at the junction temperature ϑ_{J-min} and ϑ_{J-max} respectively. $R_{d-D}(\vartheta_{J-min})$ and $R_{d-D}(\vartheta_{J-max})$ are the dynamic resistance of the diode at the junction temperature ϑ_{J-min} and ϑ_{J-max} respectively (see Fig. 2.9). It should be mentioned that the junction temperature $\vartheta_J(t)$ changes with the time (see (A.14)).

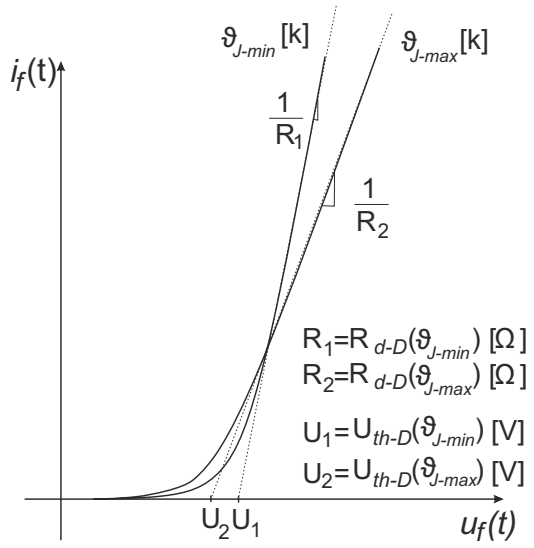


Figure 2.9: Typical diode forward characteristics based on the junction temperature.

The forward characteristic is therefore linearized by $U_{th-D}\left(\vartheta_J\left(t\right)\right)$ and $R_{d-D}\left(\vartheta_J\left(t\right)\right)$. It is given by [9]

$$u_f\left(t\right) = R_{d-D}\left(\vartheta_J\left(t\right)\right)\left|i_f\left(t\right)\right| + U_{th-D}\left(\vartheta_J\left(t\right)\right). \tag{2.4}$$

where $\left|i_f\left(t\right)\right|$ $[A]$ is the amplitude of the forward current through the diode (in voltage source inverters the forward current can be negative, therefore, the amplitude of forward current should be considered.) and $u_f\left(t\right)$ $[V]$ is the voltage across the diode during the conduction.

The conduction power loss of the diode $p_{on-D}\left(\vartheta_J(t), t\right)$ $[W]$ is the product of the voltage and the current, i.e.

$$p_{on-D}\left(\vartheta_J(t), t\right) = \left|i_f\left(t\right)\right| u_f\left(t\right), \tag{2.5}$$

By inserting (2.4) into (2.5)

$$p_{on-D}\left(\vartheta_J(t), t\right) = R_{d-D}\left(\vartheta_J(t)\right)\left(i_f(t)\right)^2 + U_{th-D}(\vartheta_J(t))\left|i_f\left(t\right)\right|. \tag{2.6}$$

The above equation is therefore defined as the conduction losses in the power diodes.

2.1.2 Reverse Recovery Power Losses in Diode ($p_{rr-D}\left(\vartheta_J(t), t\right)$)

When the diode conducts, the minority charges Q $[C]$ are stored in the N-drift region. These minority charges must be depleted before the diode becomes reverse biased. Removal of these charges is possible by two mechanisms [4]. The first one occurs by recombination inside the diode called passive removal. The amount of minority charges recombined are dependent on $\frac{di_f(t)}{dt}$. Other mechanism is active removal. It occurs by the negative diode current. The remaining stored charge in the active removal is called reverse recovery charge Q_{rr} $[C]$. Active removal depletes the reverse recovery charges in N-drift region. If $\frac{di_f(t)}{dt}$ is large enough, the minority charges have no time to recombine inside the diode. In power electronics $\frac{di_f(t)}{dt}$ is equal to $-\frac{U_R}{L}$ [10], where U_R $[V]$ is the reverse voltage across the diode and L $[H]$ is the inductance of the load . This value is large enough. Therefore we can say that the minority charges in the conduction mode are almost equal to the reverse recovery charges. The process of switching from the on-state to the off-state is called reverse recovery (see Fig. 2.4). Energy loss during reverse recovery is given by

$$E_{rr-D}\left(\vartheta_J(t), t\right) = \int_{t_a}^{t_c} i_{rr}\left(t\right) u_{rr}\left(t\right) dt. \tag{2.7}$$

where $u_{rr}(t)$ $[V]$ and $i_{rr}(t)$ $[A]$ are both the voltage and the current during the reverse recovery mode, and t_a $[s]$ is the time that the forward current $i_f(t)$ $[A]$ starts to become negative inside the diode and t_c $[s]$ is the time when $i_f(t)$ becomes the leakage current. The $u_{rr}(t)$ is equal to the on-state voltage drop across the diode from t_b to t_a $[s]$ (this part can be considered insignificant due to the small voltage drop) in addition to the reverse bias voltage U_R from t_b to t_c. Therefore the reverse recovery energy loss $E_{rr-D}\left(\vartheta_J(t), t\right)$ is

$$E_{rr-D}\left(\vartheta_J(t),t\right) = \underbrace{U_{on}\int_{t_a}^{t_b} i_{rr}(t)dt}_{\approx 0} + U_R\int_{t_b}^{t_c} i_{rr}\left(t\right)dt. \tag{2.8}$$

Since $i_{rr}(t)$ during the reverse recovery time $t_{rr} := t_c - t_a$ is the time rate of reverse recovery charges, the area under the current-time is the reverse recovery charge (see Fig. 2.10) [11] .

$$Q_{rr} = \int_{t_a}^{t_c} i_{rr}(t)dt, \tag{2.9}$$

If we assumed that $t_a - t_b$ is approximately equal to $t_c - t_b$, the right integral (2.8) can be therefore approximated by $\frac{1}{4}$ of the reverse recovery charges, i.e [12].

$$E_{rr-D}\left(\vartheta_J(t),t\right) = \frac{U_R Q_{rr}}{4}. \tag{2.10}$$

$E_{rr-D}\left(\vartheta_J(t),t\right)$ $[J]$ is a function of the forward current $i_f(t)$, the junction temperature $\vartheta_J(t)$ and the reversed bias voltage U_R [13], [14], [15].

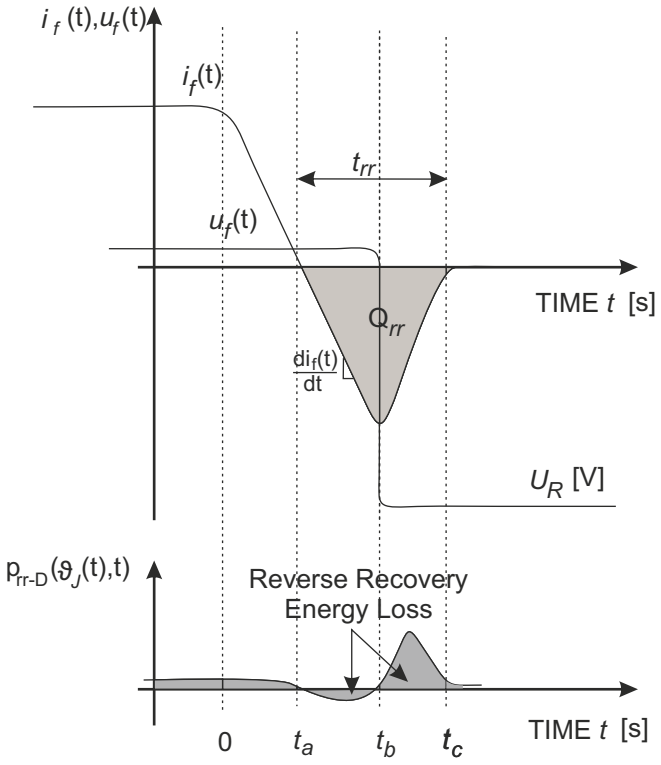


Figure 2.10: Diode reverse recovery loss.

In the previous pages we see that the forward current passing through the diode is divided into three regions. If we assume the rate of the forward current $-\frac{di_f}{dt} = \frac{U_R}{L}$ is high enough, active procedure depletes the minority charge stored in the N-drift region (the recombination procedure does not occur inside the diode) [13]. Therefore the reverse recovery charges Q_{rr} are equal to the minority stored charges Q when the diode conducts. Since over the normal operating range of the power diode, the diffusion current is dominating, the reverse recovery charges are proportional to the square root of the forward current [4], [16] (see Fig. 2.11).

$$Q_{rr} \propto \sqrt{i_f(t)}. \tag{2.11}$$

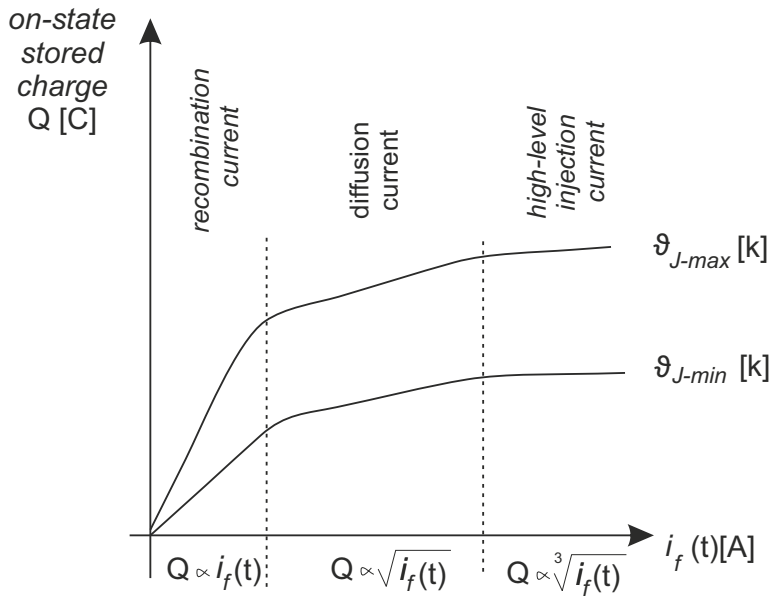


Figure 2.11: Diode stored charge Q in the N-drift region with on-state current (based on Fig. 2 in [4]).

In addition to these, the energy is proportional to the voltage applied across the diode [14]. Finally, the reverse recovery charge is proportional to the junction temperature [13], [15]. In the datasheet, the reverse recovery charges is given under the test conditions; therefore it needs to be changed to the operation mode. The final equation for the energy losses during the reverse recovery is given by [17], [14]

$$E_{rr-D}(\vartheta_J(t), t) = \frac{U_R Q_{rr}}{4} \sqrt{\left(\frac{|i_f(t)|}{I_{f-rated}}\right)} \left(\frac{U_R}{U_{R-rated}}\right)^{0.6}. \tag{2.12}$$

where $|i_f(t)|$ $[A]$ is the amplitude of current's diode in conduction mode, $I_{f-rated}$ $[A]$ is the forward current given in the datasheet for a specified reverse recovery charges Q_{rr}, U_R $[V]$ is the reversed bias voltage and $U_{R-rated}$ $[V]$ is the voltage given in the datasheet for a specified reverse recovery charges Q_{rr}.

The reverse recovery energy of the diode is dependent on the junction temperature. It is given by [18], [13]

$$E_{rr-D}(\vartheta_J(t), t) = E_{rr-D}(\vartheta_J(t_0), t_0)[1 + \alpha_{\vartheta-D}(\vartheta_J(t) - \vartheta_J(t_0))]. \tag{2.13}$$

where $\alpha_{\vartheta-D}$ is the temperature coefficient of the reverse recovery losses of the diode.

This value can typically be calculated using data from the diode manufacturer. A good approximation is 0.006 $[\frac{1}{K}]$ for the power diode [18].

The reverse recovery charge Q_{rr} given in the datasheet is obtained from one switching period T_s $[s]$ under the conditions test. If we want to find the reverse recovery power loss $p_{rr-D}(\vartheta_J(t), t)$, we should calculate it in one switching period.

$$p_{rr-D}(\vartheta_J(t), t) = \frac{1}{T_s} \underbrace{\int_{t_a}^{t_b} u_{rr}(t) i_{rr}(t) dt}_{E_{rr-D}(\vartheta_J(t), t)}, \tag{2.14}$$

and if switching frequency f_s $[Hz]$ is equal to

$$f_s = \frac{1}{T_s}, \tag{2.15}$$

Therefore, the power reverse recovery loss is

$$p_{rr-D}(\vartheta_J(t), t) = E_{rr-D}(\vartheta_J(t), t) f_s. \tag{2.16}$$

2.2 Power MOSFET

A power MOSFET (Metal–Oxide–Semiconductor Field Effect Transistor) is a specific type of transistor controlled by a voltage. Its main advantages are high input impedance that makes it easy to drive and fast switching speed operating in the 10–50 $[kHz]$. At high breakdown voltages the on-state voltage drop of the power MOSFET increases. Therefore, the power MOSFET is usually used in applications where the operating voltages are below 200 $[V]$. Fig. 2.12 shows a schematic circuit diagram of the power MOSFET [3].

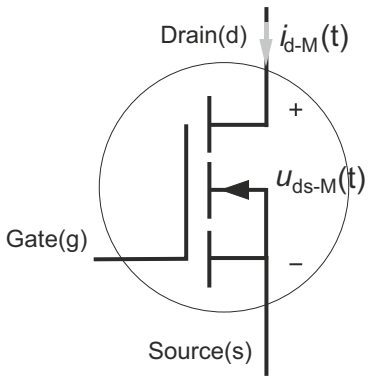


Figure 2.12: Schematic circuit diagram of an n-channel power MOSFET.

In a power MOSFET, just like in all semiconductors, power losses come from four sources. First, on-state power loss occurs when a voltage drop is across the MOSFET during conduction. Second, power loss appears due to leakage current in the reverse mode, but it is considered insignificant due to the low leakage current. Third and fourth, the switching losses occur when the MOSFET is turning on or off. In these two latter cases, the voltage and the current must pass through the active region. Thus, the voltage and the current of the MOSFET are causing the switching losses.

Fig. 2.13 shows the output voltage-current (v-i) characteristics for an ideal power MOSFET. v-i characteristics of the MOSFET is based on the drain current $i_{d-M}(t)$ $[A]$ versus drain-source voltage $u_{ds-M}(t)$ $[V]$ as a function of the gate-source voltage $u_{g-M}(t)$ $[V]$. An ideal MOSFET conducts current with zero voltage drop during the on-state and it blocks the voltage with zero leakage current during off-state. Moreover, the ideal MOSFET can switch between the on-state mode and the off-state mode instantaneously. Thus, the ideal MOSFET does not have any power losses. However, in practice, the MOSFET does not behave in this way. As the Fig 2.14 shows, the MOSFET has a voltage drop during conduction and the leakage current during off-state. Moreover, it does not switch instantaneously. Therefore, the overall power losses of the MOSFET $p_{tl-M}(\vartheta_J(t), t)$ $[W]$ are given by [3]

$$p_{tl-M}(\vartheta_J(t), t) = p_{on-M}(\vartheta_J(t), t) + \underbrace{p_{off-M}(\vartheta_J(t), t)}_{\approx 0} + p_{sw-M-on}(\vartheta_J(t), t) + p_{sw-M-off}(\vartheta_J(t), t). \tag{2.17}$$

where $p_{on-M}(\vartheta_J(t), t)$ $[W]$ is the conduction loss of the MOSFET , $p_{off-M}(\vartheta_J(t), t)$ $[W]$ is the off-state loss of the MOSFET, $p_{sw-M-on}(\vartheta_J(t), t)$ $[W]$ is the turn-on switching loss of the MOSFET, $p_{sw-M-off}(\vartheta_J(t), t)$ $[W]$ is the turn-off switching loss of the MOSFET, and $\vartheta_J(t)$ $[K]$ is the junction temperature.

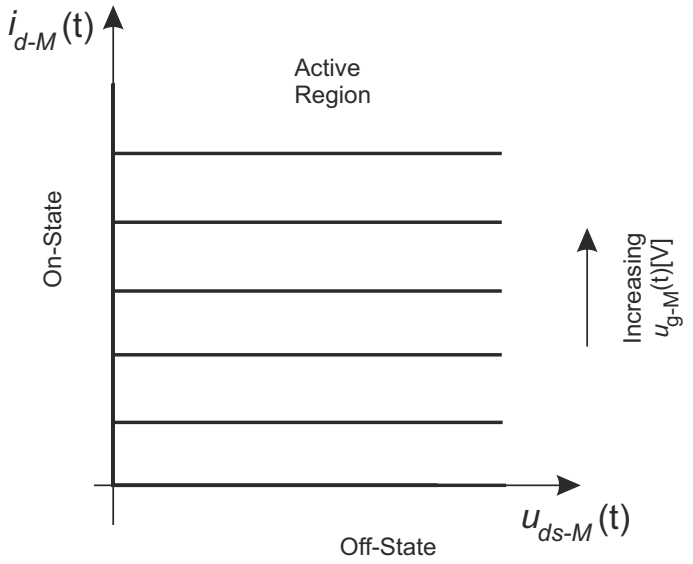


Figure 2.13: An ideal characteristic of power MOSFET.

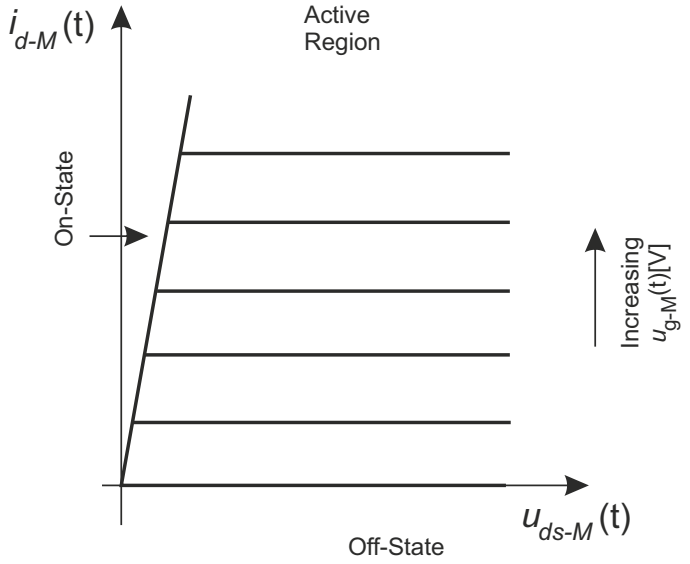


Figure 2.14: V-I characteristics of a typical power MOSFET

2.2.1 Conduction Losses of Power MOSFET ($p_{on-M}(\vartheta_J(t), t)$)

Conduction loss of the power MOSFET is often calculated by a dynamic resistance $R_{d-M}(\vartheta_J(t))$ [Ω]. Fig. 2.15 shows how we can find the dynamic resistance from v-i characteristics of the MOSFET.

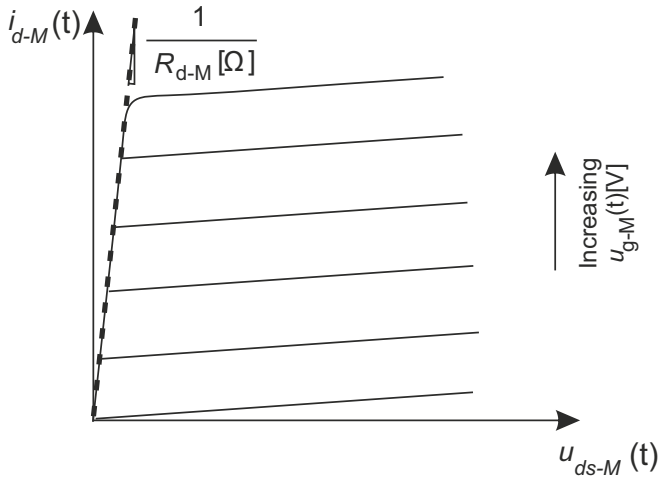


Figure 2.15: Output characteristics of a typical power MOSFET.

Just like the diode, the dynamic resistance is dependent upon the junction temperature. (A.14) shows that the junction temperature is a function of time. Moreover, Fig. 2.16 illustrates that by increasing temperature the dynamic resistance increases. The dynamic resistance based on the junction temperature is therefore calculated by [7]

$$R_{d-M}\left(\vartheta_J\left(t\right)\right) = \frac{R_{d-M}(\vartheta_{J-max})\vartheta_{J-min} - R_{d-M}(\vartheta_{J-min})\vartheta_{J-max}}{\vartheta_{J-min} - \vartheta_{J-max}} + \left[\frac{R_{d-M}(\vartheta_{J-min}) - R_{d-M}(\vartheta_{J-max})}{\vartheta_{J-min} - \vartheta_{J-max}}\right]\vartheta_J(t). \tag{2.18}$$

where ϑ_{J-min} $[K]$ and ϑ_{J-max} $[K]$ are the minimum and the maximum junction temperature of v-i characteristics given in the datasheet respectively and $R_{d-M}(\vartheta_{J-min})$and $R_{d-M}(\vartheta_{J-max})$ are the dynamic resistances of the MOSFET at the junction temperature ϑ_{J-min} and ϑ_{J-max} respectively.

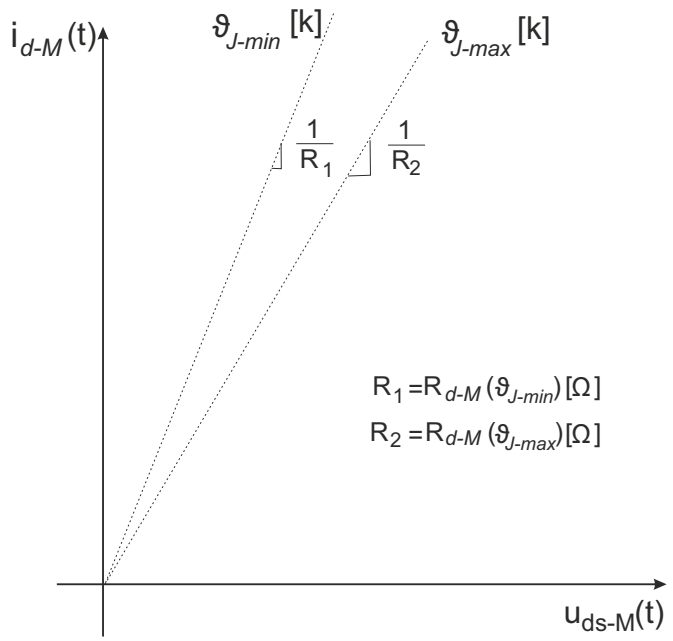


Figure 2.16: Typical MOSFET forward characteristics based on the junction temperature.

The forward characteristic of MOSFET are approximated by using $R_{d-M}\left(\vartheta_J\left(t\right)\right)$

$$u_{ds-M}(t) = R_{d-M}(\vartheta_J(t))|i_{d-M}(t)|. \tag{2.19}$$

where $|i_{d-M}(t)|$ $[A]$ is the amplitude of the drain current flowing through the MOSFET and $u_{ds-M}(t)$ $[V]$ is voltage drop across drain-source in the conduction mode.

Now, the conduction power loss in the MOSFET is given by

$$p_{on-M}(\vartheta_J(t), t) = |i_{d-M}\left(t\right)|u_{ds-M}\left(t\right), \tag{2.20}$$

and it is equal to

$$p_{on-M}(\vartheta_J(t), t) = R_{d-M}(\vartheta_J(t))(i_{d-M}(t))^2. \tag{2.21}$$

2.2.2 MOSFET Switching Losses ($p_{sw-M-on}(\vartheta_J(t), t)$ & $p_{sw-M-off}(\vartheta_J(t), t)$)

The switching losses of the MOSFET are created by the parasitic capacitances between the terminals of the MOSFET. Fig. 2.17 illustrates the parasitic gate-source C_{gs} $[F]$, the gate-drain C_{gd} $[F]$ and the drain-source C_{ds} $[F]$ capacitances. C_{gs} is the capacitance due to the overlap of the source and the gate. It is a constant capacitance independent of the operation voltage. C_{gd} consists of three parts, the first part is the capacitance associated with the overlap of the gate and the P-region. The second part is the capacitance associated with the N-region under the gate, and the last one is the capacitance between the gate and the

source. This is a nonlinear function of gate-drain voltage of the power MOSFET $u_{gd-M}(t)$. Finally the capacitance C_{ds} is between the P-region and the N-region. It is dependent on $u_{ds-M}(t)$ [19].

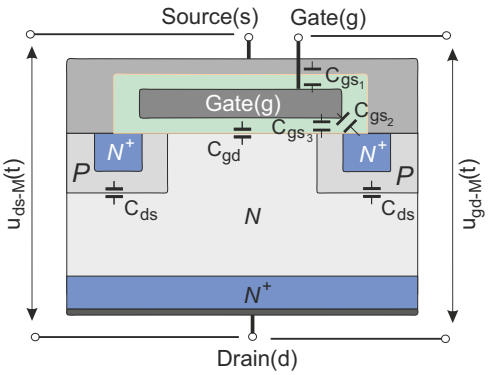


Figure 2.17: Cross-section of a power MOSFET with parasitic capacitances (based on fig 4 in [5]).

The capacitances are often named C_{iss} $[F]$, C_{oss} $[F]$, and C_{rss} $[F]$ in the datasheets. C_{iss} is the input capacitance and it is equal to C_{gd} in addition to C_{gs}. C_{rss} is called Miller capacitance and it is equal to C_{gd}. C_{oss} is also referred to the output capacitance and it is equal to C_{gd} in addition to C_{ds} [20]. All of these capacitances play an important role in determining the switching performance for the power MOSFET. Fig. 2.18 shows the equivalent circuit for the capacitances between the terminals of the power MOSFET [19], [21].

$$C_{iss} = C_{gd} + C_{gs}, C_{rss} = C_{gd}, C_{oss} = C_{gd} + C_{ds}. \tag{2.22}$$

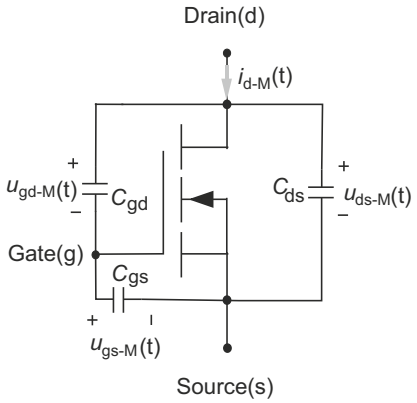


Figure 2.18: Capacitances for the power MOSFET structure.

The parasitic capacitances can explain the switching losses in the power MOSFET. The switching losses are dependent upon how the parasitic capacitances of the gate are charged. These parameters are also weakly dependent upon the drain current, the supply voltage, and the junction temperature. Fig. 2.19 shows the test circuit to determine the switching's waveform. There are two switches. The switch S_1 is for the analysis of the turn-off behavior and S_2 is for the turn-on behavior.L $[H]$ is an inductive load in parallel with a power diode D. I_D $[A]$ is the maximum current flowing through the load. Resistance R $[\Omega]$ is used to drive the MOSFET.

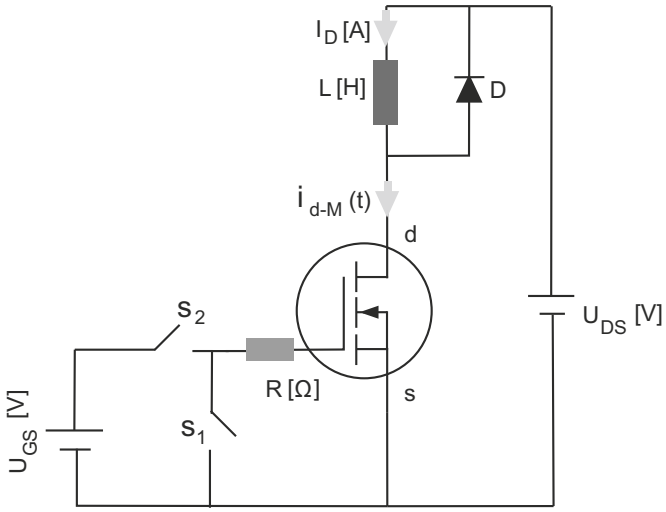


Figure 2.19: Inductive switching Loss Test Circuit.

Fig. 2.20 shows the turn-on behavior of the MOSFET. Before the gate current is turned on, the gate-source voltage $u_{gs-M}(t)$ $[V]$ and the drain current $i_{d-M}(t)$ are zero. When $i_{g-M}(t)$ $[A]$ flows, C_{gs} and C_{gd} start to be charged and $u_{g-M}(t)$ increases. During charging C_{gs}, C_{gd} remains constant because the drain-source voltage $u_{ds-M}(t)$ is constant. The MOSFET is off until $u_{gs-M}(t)$ is less than threshold voltage U_{TH} $[V]$ of the MOSFET. Once the voltage $u_{gs-M}(t)$ reaches U_{TH} , drain current $i_{d-M}(t)$ starts to flow through the MOSFET. Since the diode is parallel with the MOSFET, the $u_{ds-M}(t)$ remains constant, because the diode can not bear any voltage until all of the load current is passed through the power MOSFET. $u_{g-M}(t)$ continues to rise to the plateau voltage U_{GP} $[V]$, while the entire $i_{d-M}(t)$ has transferred from the diode to the power MOSFET. When $i_{d-M}(t)$ is equal to I_D $[A]$, $u_{ds-M}(t)$ starts to reduce. In this time, the gate current I_{g-M} $[A]$ is used to charge C_{gd}. Therefore, $u_{g-M}(t)$ remains constant at the plateau voltage until $u_{ds-M}(t)$ reduces to the on-state voltage [22] . After this time, $u_{g-M}(t)$ increases until it reaches the gate supply voltage U_{GS} $[V]$. During the time interval $[t_1 - t_3]$, the switching losses occur. The gate charge during the time intervals

$[t_1 - t_3]$ is defined as the gate switching charge Q_{sw} $[C]$. Q_{sw} is considered the most significant parameter for the power MOSFET performance and it is given in the datasheets.

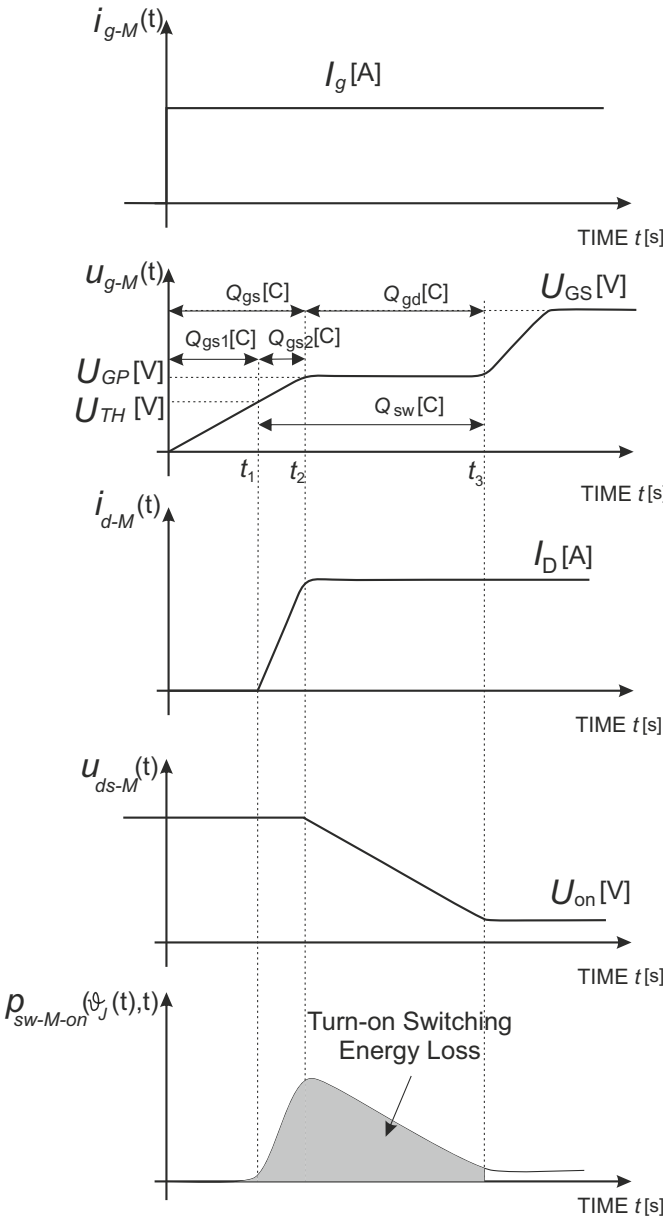


Figure 2.20: Gate charge waveform of the power MOSFET during turn-on transition.

Fig. 2.21 illustrates the turn-off behavior of the MOSFET. The MOSFET is operating in the on-state before it is turned off. The gate of the power MOSFET is connected to the

source via the gate resistance R to discharge its capacitances and turns the MOSFET off. $i_{d-M}(t)$ and $u_{ds-M}(t)$ do not change until $u_{g-M}(t)$ reaches to the plateau voltage U_{GP}. During the time interval $[0-t_4]$, C_{gd} remains constant because $u_{ds-M}(t)$ is constant. $u_{ds-M}(t)$ starts to increase at time t_4, In this time, $i_{d-M}(t)$ is equal to I_D, because the current cannot be transferred to the diode until the $u_{ds-M}(t)$ exceeds the supply voltage U_{DS} $[V]$. Since $i_{d-M}(t)$ remains constant, $u_{g-M}(t)$ also is constant at the gate plateau voltage. At time t_5, I_D starts to transfer from the power MOSFET to the power diode. Since $u_{ds-M}(t)$ is constant, the C_{gd} can also be assumed to remain constant during this phase. After this time, the $u_{g-M}(t)$ decreases until it becomes zero.

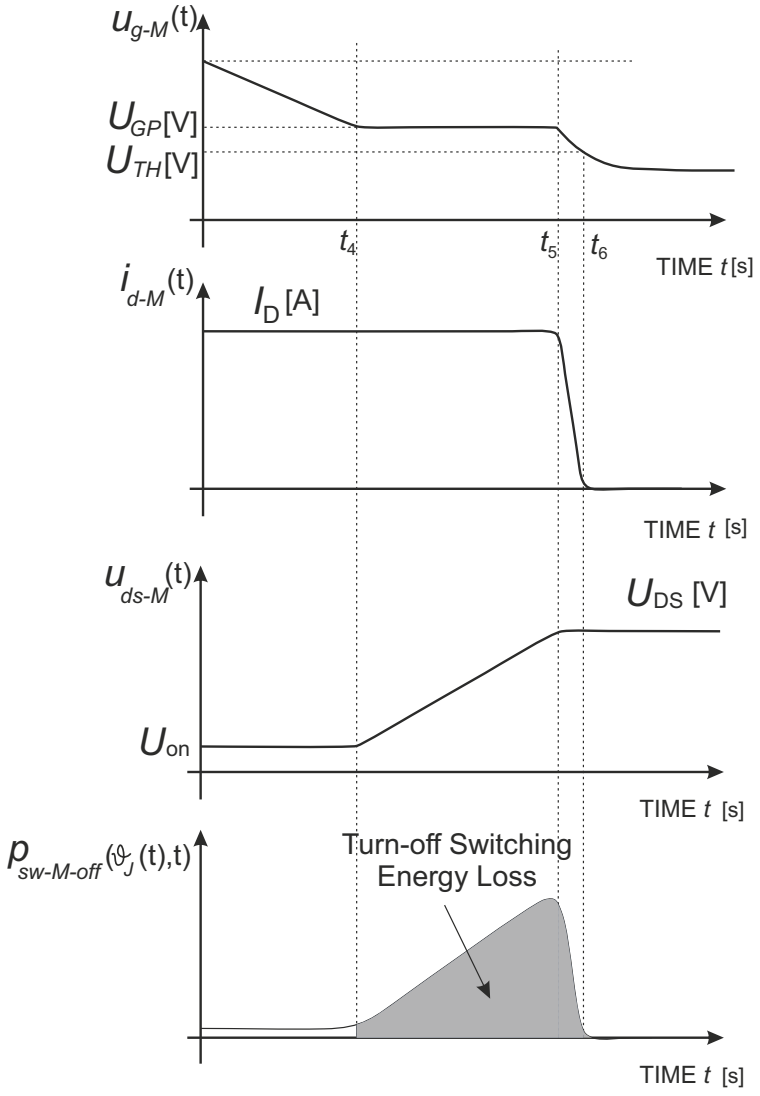


Figure 2.21: The power MOSFET during turn-off transition.

A simple method of calculating the switching energy loss of the power MOSFET based on datasheet is desirable. As these can be seen from Fig. 2.20 and Fig. 2.21, an equation for estimating the energy loss of the power MOSFET is given by

$$E_{sw-M}(\vartheta_J(t),t) = E_{sw-M-on}(\vartheta_J(t),t) + E_{sw-M-off}(\vartheta_J(t),t). \tag{2.23}$$

where $E_{sw-M-on}(\vartheta_J(t),t)$ $[J]$ is the energy loss during turn-on MOSFET and $E_{sw-M-off}(\vartheta_J(t))$ $[J]$ is the energy loss during turn-off MOSFET.

Since in practice, a free-wheeling diode is parallel to the MOSFET, the turn-on switching loss in the worst is the sum of the turn-on switch energy loss without taking the reverse recovery of the diode into account and the turn-on switch energy loss caused by the reverse-recovery of the free-wheeling diode. It is given by [18]

$$E_{sw-M-on}(\vartheta_J(t),t) = \frac{1}{2}|i_{d-M}(t)|U_{DS}\,(t_{on}+t_{off}) + Q_{rr}U_{DS}. \tag{2.24}$$

where $|i_{d-M}(t)|$ $[A]$ is the amplitude of drain current flowing through the MOSFET when the MOSFET is on, U_{DS} $[V]$ is the drain-source voltage across the MOSFET when the MOSFET is off , t_{on} $[s]$ and t_{off} $[s]$ are the interval time $[t_1 - t_3]$ (see Fig. 2.20) and the interval time $[t_4 - t_6]$ (see Fig. 2.21) respectively and Q_{rr} $[C]$ is the reverse recovery of the diode parallel with the MOSFET.

$E_{sw-M-off}(\vartheta_J(t),t)$ is the energy loss during the MOSFET turn-off and is given by [18]

$$E_{sw-M-off}(\vartheta_J(t),t) = \frac{1}{2}|i_{d-M}(t)|U_{DS}\,(t_{on}+t_{off})\,. \tag{2.25}$$

Moreover, the energy is proportional to the voltage drop across the MOSFET and the current passing through the MOSFET. Therefore, (2.23) becomes [23]

$$E_{sw-M}(\vartheta_J(t),t) = (E_{sw-M-on}(\vartheta_J(t),t) + E_{sw-M-off}(\vartheta_J(t),t))\frac{|i_{d-M}(t)|}{I_{D-rated}}(\frac{U_{DS}}{U_{DS-rated}})^{1.49}. \tag{2.26}$$

where $I_{D-rated}$ $[A]$ and $U_{DS-rated}$ $[V]$ are the rated load current and the rated drain-source voltage given in the datasheet.

The turn-on interval time $|t_{on}|$ and turn-off interval time $|t_{off}|$ can be obtained with a good approximation by [20]

$$|t_{off}| = |t_{on}| = \frac{Q_{sw}}{I_g}. \tag{2.27}$$

where I_g $[A]$ is the gate drive current and Q_{sw} $[C]$ is the gate switch charge provided in the power MOSFET datasheets.

Finally, the temperature dependency should be applied to the energy loss. It is given by [18]

$$E_{sw-M}(\vartheta_J(t),t) = E_{sw-M}(\vartheta_J(t_0),t_0)[1+\alpha_{\vartheta-M}(\vartheta_J(t)-\vartheta_J(t_0))]. \tag{2.28}$$

where $\alpha_{\vartheta-M}$ is the temperature coefficient of the switching loss. This is equal to 0.003 $[\frac{1}{K}]$ for the MOSFET.

Just like power diode, all the switching data in the MOSFET's datasheet are found in one period of switching T_s $[s]$. The switching power losses $p_{sw-M}(\vartheta_J(t),t)$ $[W]$ in one period of switching can be therefore calculated by

$$p_{sw-M}(\vartheta_J(t),t) = \frac{1}{T_s}\underbrace{\int_{T_s} u_{ds-M}(t)i_{d-M}(t)dt}_{E_{sw-M}(\vartheta_J(t),t)}, \tag{2.29}$$

and if switching frequency f_s $[Hz]$ is equal to

$$f_s = \frac{1}{T_s}, \tag{2.30}$$

Therefore, the switching power losses are

$$p_{sw-M}(\vartheta_J(t),t) = \underbrace{E_{sw-M-off}(\vartheta_J(t),t)f_s}_{p_{sw-M-off}(\vartheta_J(t),t)} + \underbrace{E_{sw-M-on}(\vartheta_J(t),t)f_s}_{p_{sw-M-on}(\vartheta_J(t),t)} = E_{sw-M}(\vartheta_J(t),t)f_s. \tag{2.31}$$

2.3 Power IGBT

An IGBT (Insulated Gate Bipolar Transistor) is a three-terminal power semiconductor device. The IGBT combines the advantage of the MOSFET input characteristics and bipolar junction transistor (BJT) output characteristics that makes it a voltage-controlled bipolar device. The advantages of the IGBT are the low saturation voltage drop and a simple drive circuit due to the high input impedance of the MOSFET. In case of IGBT, the on-resistance decreases with the breakdown voltage in comparison to the power MOSFET. The IGBT is used therefore in the high voltage breakdown (more than 200 $[V]$) [3]. Fig. 2.22 shows the schematic symbol of the IGBT. Its terminals are called Emitter (E), Collector (C) and Gate (G).

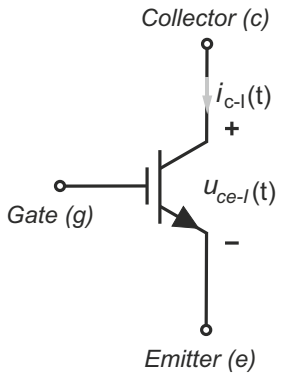


Figure 2.22: IGBT circuit diagram symbol.

In the IGBT, the losses are divided into four regions. First region is the on-state power loss. It occurs when the IGBT is on. There is therefore a voltage drop across the IGBT. Second, the power loss appears due to the leakage current in the reverse mode. It can be considered insignificant because the leakage current is very small. Third and fourth are the switching losses. They occur when the IGBT is turning on or off. In these two latter cases, the voltage or current of the IGBT can not instantaneously become zero. The switching losses happen therefore in these cases.

Fig. 2.23 shows the v-i characteristics of an ideal IGBT. The ideal IGBT conducts current in the on-state mode with zero voltage drop. It blocks voltage in the off-state mode with zero leakage current. In addition, the ideal IGBT can turn on or off instantaneously.

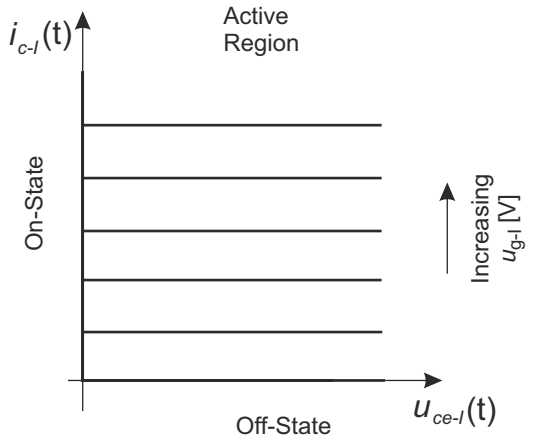


Figure 2.23: An ideal characteristics of the IGBT.

In practice, the IGBT has non-ideal behavior. The Fig. 2.24 shows the IGBT has the voltage drop during the conduction mode and has the reverse current during the off-state mode. Moreover, it has the switching losses when the IGBT becomes on or off. The total power losss $p_{tl-I}(\vartheta_J(t), t)$ are given by [24]

$$p_{tl-I}(\vartheta_J(t), t) = p_{on-I}(\vartheta_J(t), t) + \underbrace{p_{off-I}(\vartheta_J, t)}_{\approx 0} + p_{sw-I-on}(\vartheta_J(t), t) + p_{sw-I-off}(\vartheta_J(t), t). \tag{2.32}$$

where $p_{on-I}(\vartheta_J(t), t)$ $[W]$ is the power loss during the conduction, $p_{off-I}(\vartheta_J, t)$ $[W]$ is the power loss during the off-state mode, $p_{sw-I-on}(\vartheta_J(t), t)$ $[W]$ is the turn-on switching loss and $p_{sw-I-off}(\vartheta_J(t), t)$ $[W]$ is the turn-off switching loss.

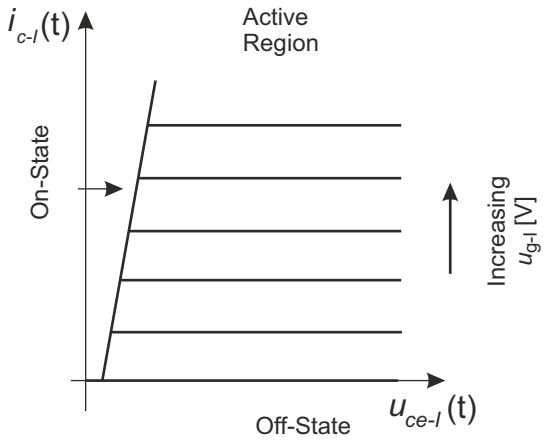


Figure 2.24: The characteristics of a typical IGBT.

2.3.1 IGBT Conduction Losses ($p_{on-I}(\vartheta_J(t), t)$)

The forward characteristic of an IGBT can be linearized by the threshold voltage $U_{th-I}(\vartheta_J(t))$ $[V]$ and the dynamic resistance $R_{d-I}(\vartheta_J(t))$ $[\Omega]$ [25], [24]. The equation of the emitter-collector voltage $u_{ce-I}(t)$ $[V]$ based on the collector current $i_{c-I}(t)$ $[A]$ is given therefore by [26]

$$u_{ce-I}(t) = U_{th-I}(\vartheta_J(t)) + R_{d-I}(\vartheta_J(t))\,|i_{c-I}(t)| \tag{2.33}$$

where $|i_{c-I}(t)|$ $[A]$ is the amplitude of the collector current passing through the IGBT.

Fig. 2.25 shows how we can find the dynamic resistance and the threshold voltage from the output characteristic of the IGBT .

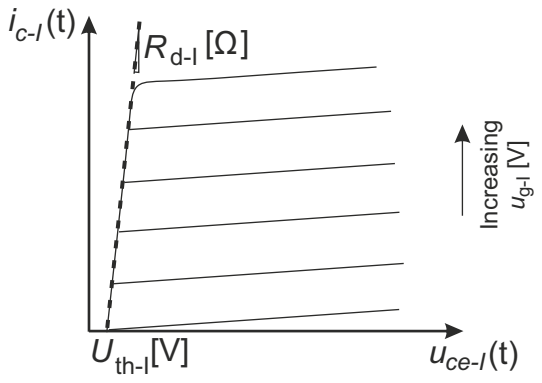


Figure 2.25: Output Characteristics of a typical power IGBT.

Similar to the diode, the dynamic resistance and the threshold voltage are dependent on the junction temperature. These dependencies are given by [7]

$$U_{th-I}\left(\vartheta_J\left(t\right)\right) = \frac{U_{th-I}(\vartheta_{J-max})\vartheta_{J-min} - U_{th-I}(\vartheta_{J-min})\vartheta_{J-max}}{\vartheta_{J-min} - \vartheta_{J-max}} + [\frac{U_{th-I}(\vartheta_{J-min}) - U_{th-I}(\vartheta_{J-max})}{\vartheta_{J-min} - \vartheta_{J-max}}]\vartheta_J(t), \tag{2.34}$$

and

$$R_{d-I}\left(\vartheta_J\left(t\right)\right) = \frac{R_{d-I}(\vartheta_{J-max})\vartheta_{J-min} - R_{d-I}(\vartheta_{J-min})\vartheta_{J-max}}{\vartheta_{J-min} - \vartheta_{J-max}}] + [\frac{R_{d-I}(\vartheta_{J-min}) - R_{d-I}(\vartheta_{J-max})}{\vartheta_{J-min} - \vartheta_{J-max}}]\vartheta_J(t). \tag{2.35}$$

where $\vartheta_J(t_1)$ $[K]$ and $\vartheta_J(t_2)$ $[K]$ are the minimum and maximum junction temperature of v-i characteristics given in the datasheet (see Fig. 2.26), $U_{th-I}(\vartheta_{J-min})$ and $U_{th-I}(\vartheta_{J-max})$ are the threshold voltages at the junction temperature ϑ_{J-min} and ϑ_{J-max} respectively and $R_{d-I}(\vartheta_{J-min})$ and $R_{d-I}(\vartheta_{J-max})$ and the dynamic resistances of the IGBT at the junction temperature ϑ_{J-min} and ϑ_{J-max} respectively.

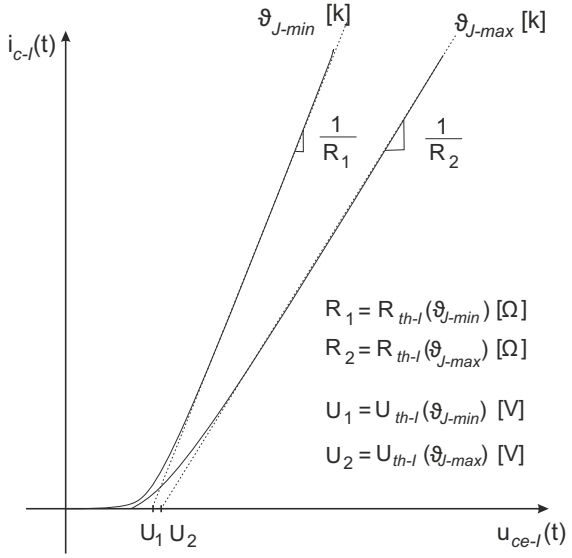


Figure 2.26: Typical IGBT forward characteristics based on the junction temperature.

Now, the power loss in the IGBT is given by

$$p_{on-I}(\vartheta_J(t), t) = |i_{c-I}\left(t\right)|u_{ce-I}\left(t\right). \tag{2.36}$$

and it is equal to

$$p_{on-I}(\vartheta_J(t), t) = U_{th-I}\left(\vartheta_J\left(t\right)\right)\left|i_{c-I}\left(t\right)\right| + R_{d-I}\left(\vartheta_J\left(t\right)\right)\left(i_{c-I}\left(t\right)\right)^2. \tag{2.37}$$

2.3.2 IGBT Switching Losses ($p_{sw-I-on}(\vartheta_J(t), t)$ & $p_{sw-I-off}(\vartheta_J(t), t)$)

Fig. 2.27 illustrates the test circuit. This test circuit is used to obtain the switching waveforms. This test circuit is similar to the MOSFET's test circuit. The IGBT's turn-on and turn-off switching waveforms are very similar to the MOSFET's switching waveforms.

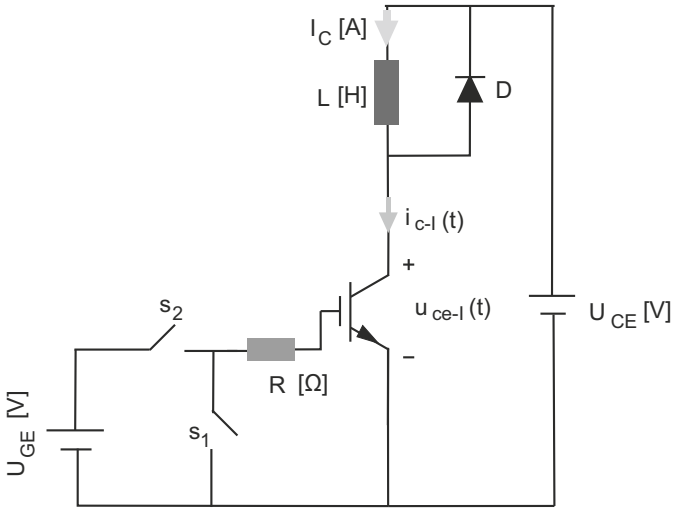


Figure 2.27: The IGBT Switching Test Circuit.

Fig. 2.28 shows the IGBT's turn-on waveforms obtained from the test circuit in Fig. 2.27. When $u_{g-I}(t)$ increases to the threshold voltage U_{TH} $[V]$, the gate current $i_{g-I}(t)$ charges the parasitic capacitances C_{ge} and C_{gc}. In the time interval $[0 - t_1]$, $u_{ce-I}(t)$ and $i_{c-I}(t)$ do not change. When $u_{g-I}(t)$ passes the threshold voltage U_{TH}, $i_{c-I}(t)$ starts to conduct. In this region, $i_{c-I}(t)$ increases to the maximum load current I_C $[A]$. At the same time, $u_{ce-I}(t)$ reduces compared with the reverse bias voltage U_{CE} $[V]$. This is because $i_{c-I}(t)$ passes through the inductive load L $[H]$. The voltage across the inductive load (see Fig. 2.27) increases, therefore $u_{ce-I}(t)$ decreases a little. During the time interval $[t_1$-$t_3]$, the diode current $i_D(t)$ decreases. Therefore, there is a reverse recovery. This current $i_D(t)$ is added to $i_{c-I}(t)$. In the time t_2 $[s]$, all the minority stored charges in the N-drift region is depleted and the diode can bear the reverse voltage. Therefore, the collector-emitter voltage $u_{ce-I}(t)$ reduces rapidly. After the time t_4 $[s]$, the IGBT turns on. The collector current is equal to maximum turn-on current I_C and the turn-on voltage drop across the collector-emitter is equal to U_{on}.

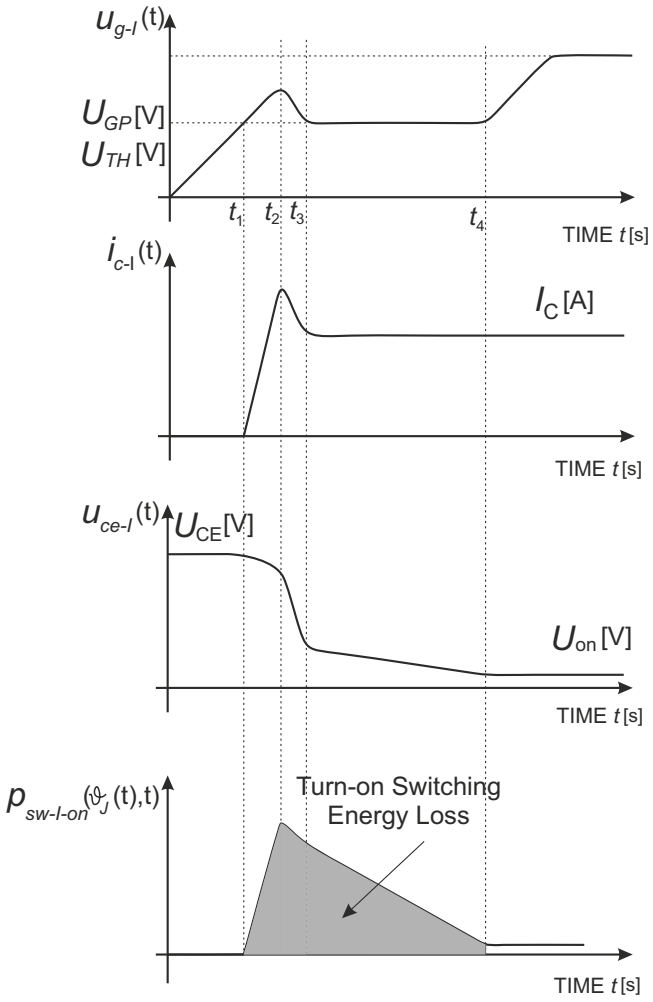


Figure 2.28: The turn-on waveforms of an IGBT.

Fig. 2.29 shows the IGBT's turn-off waveforms obtained from the test circuit in Fig. 2.27. Before t_4, $u_{g-I}(t)$ decreases to the plateau voltage U_{GP} $[V]$. At this time, the values of $u_{ce-I}(t)$ and $i_{c-I}(t)$ do not change. $u_{ce-I}(t)$ starts to increase at time t_4. In this interval time, $i_{c-I}(t)$ is equal to I_C, because the current cannot be transferred to the diode until the $u_{ce-I}(t)$ exceeds the supply voltage U_{CE}. Since $i_{c-I}(t)$ is constant, $u_{g-I}(t)$ also is constant at the gate plateau voltage. At time t_5, $i_{c-I}(t)$ starts to transfer from the IGBT to the power diode. Therefore, the value of $u_{ce-I}(t)$ is maintained at U_{CE}, while $i_{c-I}(t)$ decreases. Finally, when the IGBT is ready to bear the reverse voltage, $i_{c-I}(t)$ transfers to the diode and becomes zero.

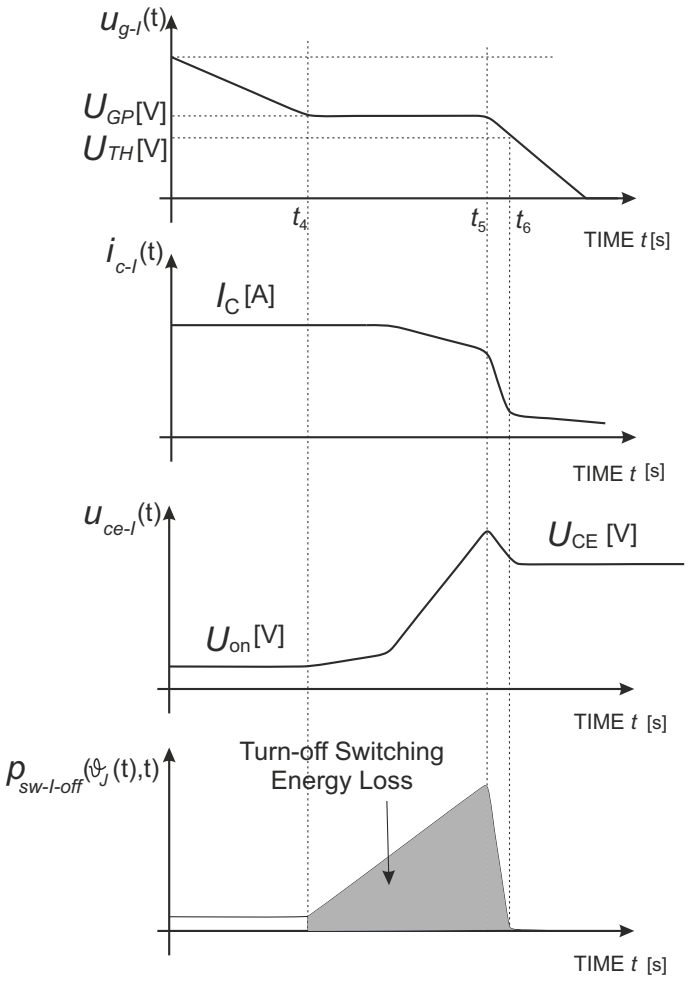


Figure 2.29: The turn-off waveforms of an IGBT.

The switching losses of the IGBT based on the datasheet can be calculated by [18], [23]

$$E_{sw-I}(\vartheta_J(t),t) = [E_{sw-I-on}(\vartheta_J(t),t) + E_{sw-I-off}(\vartheta_J(t),t)](\frac{|i_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}. \quad (2.38)$$

where $E_{sw-I-on}(\vartheta_J(t),t)$ $[J]$ and $E_{sw-I-off}(\vartheta_J(t),t)$ $[J]$ are the turn-on and turn-off energies of the IGBT at the rated current $I_{C-rated}$ $[A]$ and the rated voltage $U_{CE-rated}$ $[V]$ respectively, U_{CE} $[V]$ is the reverse voltage across the IGBT when it is off and $|i_{c-I}(t)|$ $[A]$ is the amplitude of the collector current when the IGBT is off.

The below equation can be applied to (2.38) which yields [18]

$$E_{sw-I}(\vartheta_J(t),t) = E_{sw-I}(\vartheta_J(t_0),t_0)[1 + \alpha_{\vartheta-I}(\vartheta_J(t) - \vartheta_J(t_0))] \quad (2.39)$$

where $\vartheta_J(t)$ $[K]$ is the junction temperature at time t and $\alpha_{\vartheta-I}$ is the temperature coefficient the IGBT. This parameter is equal to 0.003 $[\frac{1}{K}]$ for the IGBT.

At the end, just like the diode and the MOSFET, the switching energy losses given in the datasheet are found in one period of switching. Therefore, the switching power losses $p_{sw-I}(\vartheta_J(t), t)$ in one period of switching can be therefore calculated by [27], [24]

$$p_{sw-I}(\vartheta_J(t), t) = \frac{1}{T_s} \underbrace{\int_{T_s} u_{ce-I}(t) i_{c-I}(t) dt}_{E_{sw-I}(\vartheta_J(t), t)} . \tag{2.40}$$

and if switching frequency f_s $[Hz]$ is equal to

$$f_s = \frac{1}{T_s}, \tag{2.41}$$

Therefore, the switching power losses are [28]

$$p_{sw-I}(\vartheta_J(t), t) = E_{sw-I}(\vartheta_J(t), t) f_s. \tag{2.42}$$

$$p_{sw-I-on}(\vartheta_J(t), t) = E_{sw-I-on}(\vartheta_J(t), t) f_s. \tag{2.43}$$

$$p_{sw-I-off}(\vartheta_J(t), t) = E_{sw-I-off}(\vartheta_J(t), t) f_s. \tag{2.44}$$

Chapter 3

Modeling of Voltage Source Inverters

An inverter is basically a converter that converts DC to AC power. The inverter circuits can be mainly divided into two classes based on their operation, current source inverters (CSIs) and voltage source inverters (VSIs) [29]. Voltage source inverters are divided into several topologies. The most important topologies are the two-level voltage source inverters and the three-level neutral point clamped voltage source inverters. The main reasons to choose a desired configuration for our circuit are various advantages such as lower common mode voltage, reduced Electromagnetic Interference (EMI) generation, lower $\frac{du(t)}{dt}$ to supply and lower harmonic contents in the output voltage [30].

In this section, the structure of two-level voltage source inverter and three-level neutral point clamped (NPC) voltage source inverter are investigated, then the losses in these inverters are modeled.

3.1 Two Level Voltage Source Inverter (2-L VSI)

The three-phase two-level voltage source inverter is shown in Fig. 3.1. The inverter contains six switches $S_a(t)$, $S_b(t)$, $S_c(t)$, $\bar{S}_a(t)$, $\bar{S}_b(t)$ and $\bar{S}_c(t)$. Each switches $S_x(t)$ and $\bar{S}_x(t)$ ($x \in \{a, b, c\}$) is composed of a transistors $T_x(t)$ (IGBT or MOSFET) with a P-i-N diode $D_x(t)$ in parallel with each switch (see Fig. 3.2).

The $S_a(t)$, $S_b(t)$ and $S_c(t)$ are upper switches while $\bar{S}_a(t)$, $\bar{S}_b(t)$ and $\bar{S}_c(t)$ are lower switches. The upper and the lower power switches of the same leg are complementary in operation. This means if the upper switch is turned on, the lower switch must be turned off. The output voltage of the inverter depends only upon the switching states $S_{abc}(t)$ and the DC-link voltage U_{dc} $[V]$. Therefore, the output voltages of the two-level inverter is independent of the direction of the phase currents $i^{abc}(t)$ $[A]$ and they are equal to $+\frac{U_{dc}}{2}$ $[V]$ and $-\frac{U_{dc}}{2}$ $[V]$.

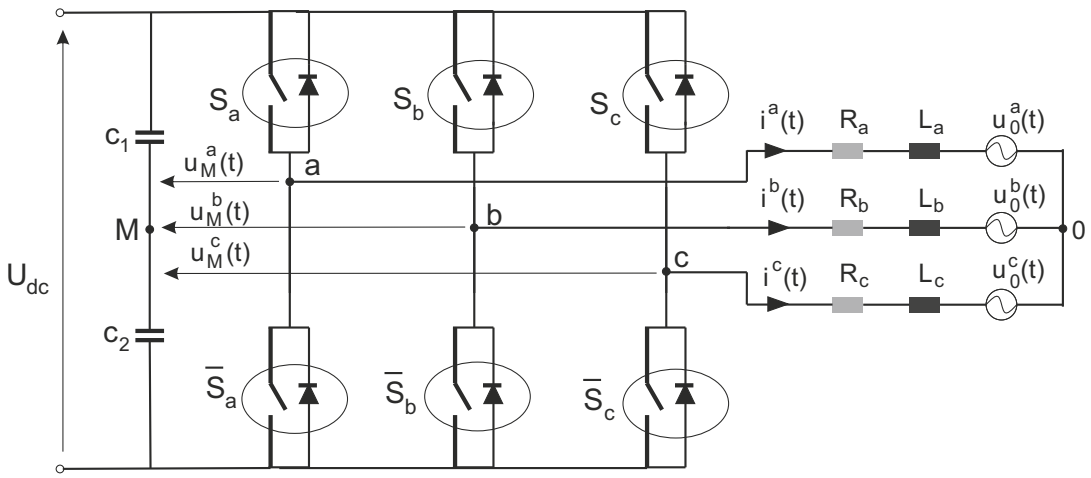


Figure 3.1: Simplified two-level voltage source inverter.

3.1.1 Switching States and Commutations

Fig. 3.1 shows that the upper switches connect the AC terminals of the inverter (a, b, or c) to the positive DC-link voltage while the AC terminals of the inverter (a, b, or c) can be connected to the negative DC-link voltage by the lower switches. Therefore, the number of switching states are $2^3 = 8$.

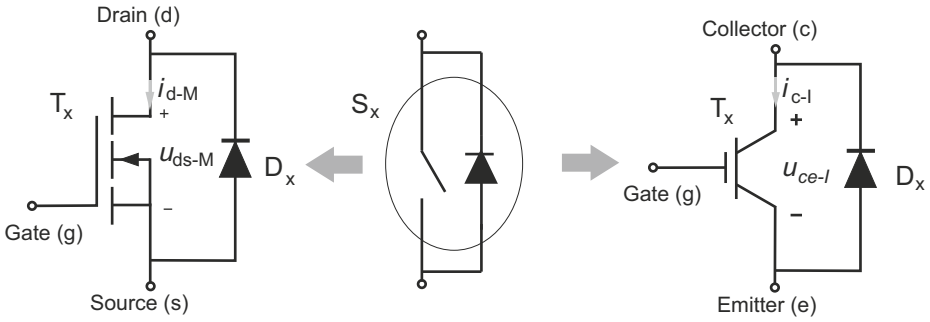


Figure 3.2: A switch of an inverter.

Tab. 3.1 gives the switching positions of each phase leg where 1 and 0 denote the on and off state of the switch respectively. For example, if $S_a(t)$ is on then the leg of a is connected to positive DC-link voltage and the voltage between leg of a and the mid-point M of two capacitors is equal to $u^a_M(t) = +\frac{U_{dc}}{2}$. The phase current paths through the semiconductors are shown in Fig. 3.3. The switching losses are created by the commutation processes between

$S_x(t)$	$u_M^x(t)$, $x \in \{a,b,c\}$
1	$+\frac{U_{dc}}{2}$
0	$-\frac{U_{dc}}{2}$

Table 3.1: Switching positions for each phase of the two-level voltage source inverter.

$S_x(t)$	$T_x(t)$	$\bar{T}_x(t)$	$D_x(t)$	$\bar{D}_x(t)$
$i^x(t) > 0$, $x \in \{a,b,c\}$				
1	On	-	-	-
0	-	-	-	On
$i^x(t) < 0$, $x \in \{a,b,c\}$				
1	-	-	On	-
0	-	On	-	-

Table 3.2: Conduction losses in the two-level voltage source inverter.

the different switching states. The distribution of the switching losses and the conduction losses are given in Tab. 3.2 and Tab. 3.3 respectively.

For a positive phase current $i^x(t) > 0$ ($x \in \{a,b,c\}$), the conduction losses occur in the $T_x(t)$ when the $S_x(t)$ is on or in the $\bar{D}_x(t)$ when the $S_x(t)$ is off. The commutation from $S_x(t) = 1$ to $S_x(t) = 0$ occurs by turning $T_x(t)$ off and turning $\bar{D}_x(t)$ on. In this way, the turn-off switching power losses arise. The commutation from $S_x(t) = 0$ to $S_x(t) = 1$ occurs by turning $\bar{D}_x(t)$ off and turning $T_x(t)$ on. In this way, the reverse recovery power losses arise in the diode and the turn-off switching power losses occur in $T_x(t)$. Fig. 3.3 shows the paths of the positive phase current. As it can be seen, the conduction loss and the switching losses occur in the $T_x(t)$ or $\bar{D}_x(t)$ when the phase current is positive.

For a negative phase current $i^x(t) < 0$ ($x \in \{a,b,c\}$), the conduction losses occur in the $D_x(t)$ when the $S_x(t)$ is on or in the $\bar{T}_x(t)$ when the $S_x(t)$ is off. The commutation from $S_x(t) = 1$ to $S_x(t) = 0$ occurs by turning $D_x(t)$ off and turning $\bar{T}_x(t)$ on. In this way, the turn-on switching power losses arise in $\bar{T}_x(t)$ and reverse recovery power losses occur in $D_x(t)$. The commutation from $S_x(t) = 0$ to $S_x(t) = 1$ occurs by turning $D_x(t)$ on and turning $\bar{T}_x(t)$ off. Therefore, the turn-off switching power losses occur in $\bar{T}_x(t)$. Fig. 3.3 shows the paths of the negative phase current. In these situations, the conduction loss and the switching losses occur in the $D_x(t)$ or $\bar{T}_x(t)$.

$S_x(t)$	$T_x(t)$	$\bar{T}_x(t)$	$D_x(t)$	$\bar{D}_x(t)$
$i^x(t) > 0,\ x \in \{a, b, c\}$				
$1 \longrightarrow 0$	Off	-	-	On
$0 \longrightarrow 1$	On	-	-	Off
$i^x(t) < 0,\ x \in \{a, b, c\}$				
$1 \longrightarrow 0$	-	On	Off	-
$0 \longrightarrow 1$	-	Off	On	-

Table 3.3: Switching losses in the two-level voltage source inverter.

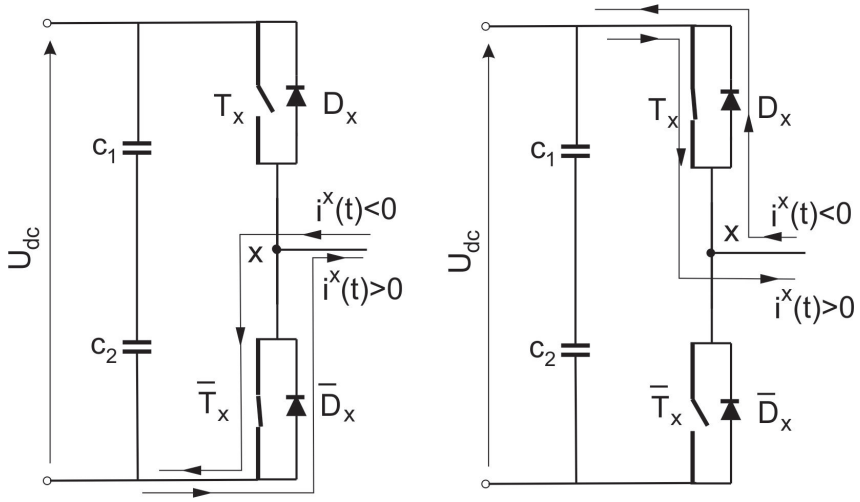


Figure 3.3: Load current paths of the two-level voltage source inverter.

3.1.2 Modeling of Two-Level Voltage Source Inverters

Mathematical models are an important tool to analyze the dynamic performance of a voltage source inverter. A mathematical model of the inverter must be established based on the switching states and the DC-link voltage. A schematic diagram of the two-level inverter is shown in Fig. 3.1.

The following assumptions are made in order to model the two-level inverter:

(A1). All semiconductor devices are identical and ideal with identical characteristics.

(A2). All parasitic elements of circuit are considered insignificant.

(A3). AC side is modelled by voltage sources $u_0^x(t)$ ($x \in \{a, b, c\}$): hence voltage sources are symmetrical. The three voltage sources are connected in star with a neutral connection (0 point). Fig. 3.4 shows the model of the AC side. The AC side also has an internal resistive-inductive impedance (R_x - L_x) [31]. (3.1) describes the sinusoidal voltage sources in the AC side. They are an ideal symmetrical three-phase source with constant amplitude $\widehat{U_0}$

$[V]$ and constant frequency f_0 $[Hz]$.

$$u_0^{abc}(t) = \begin{bmatrix} u_0^a(t) \\ u_0^b(t) \\ u_0^c(t) \end{bmatrix} = \widehat{U_0} \begin{bmatrix} \sin(2\pi f_0 t + \varphi_0) \\ \sin(2\pi f_0 t + \varphi_0 - \frac{2\pi}{3}) \\ \sin(2\pi f_0 t + \varphi_0 - \frac{4\pi}{3}) \end{bmatrix}. \tag{3.1}$$

where φ_0 $[rad]$ is initial phase shift.

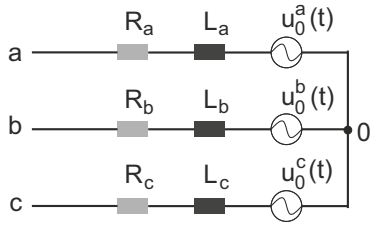


Figure 3.4: AC side model for three-phase system.

(A4). The values for R_x $[\Omega]$ and L_x $[H]$ are identical for all three phases, i.e. $R_a = R_b = R_c = R$ and $L_a = L_b = L_c = L$.

As it can be seen from Fig. 3.5, $S_x(t)$ and $\bar{S}_x(t)$ can be considered as a two-pole switch $S_i(t)$ which may be connected to the positive or the negative voltage according to the modulation strategy used.

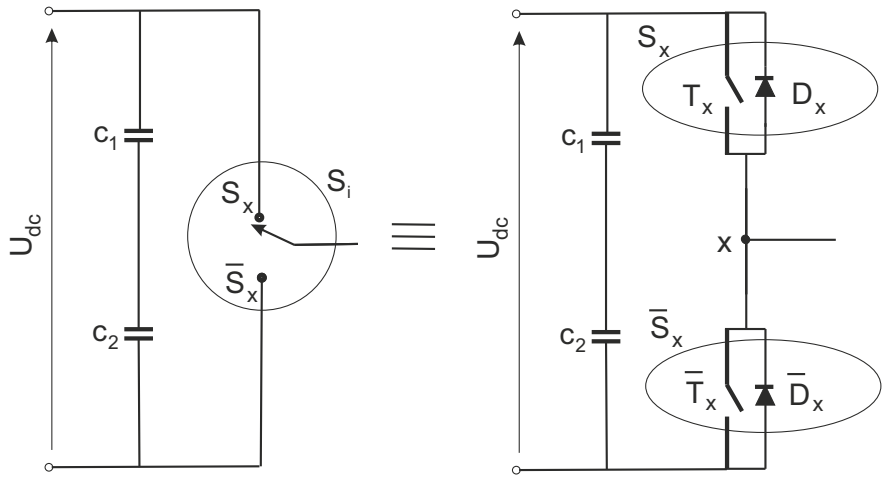


Figure 3.5: One leg of a two-level voltage source inverter.

Therefore, Fig. 3.1 turns into Fig. 3.6.

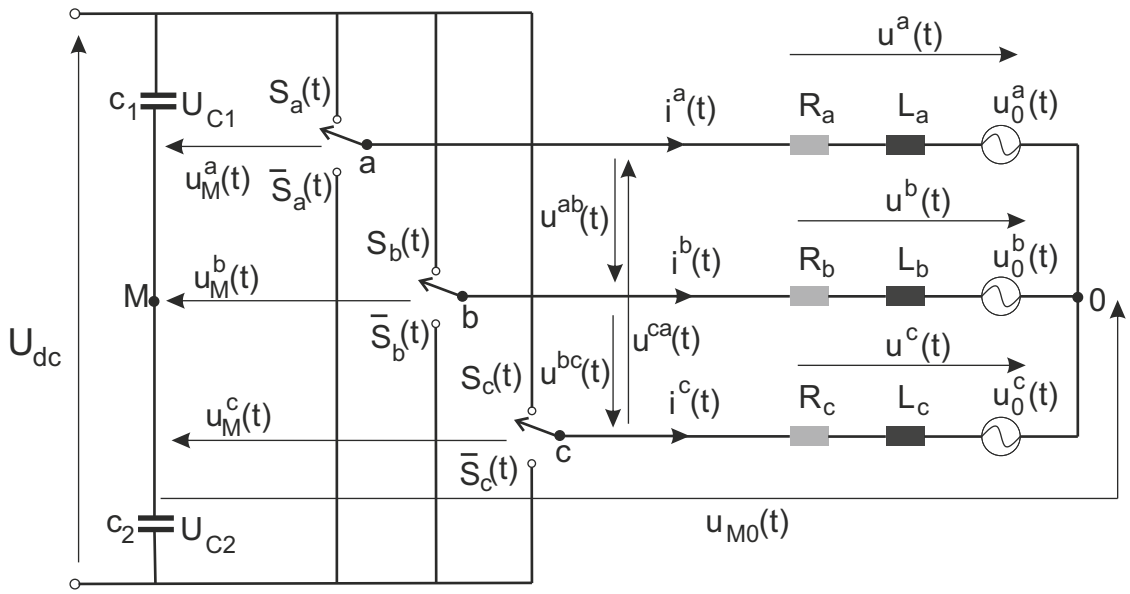


Figure 3.6: Schematic circuit of the three-phase two-level VSI.

The two-pole switch $S_i(t)$ $(i \in \{a, b, c\})$ is defined as

$$S_i(t) = \begin{cases} 1, & \text{if } S_i(t) \text{ is on} \\ 0, & \text{if } S_i(t) \text{ is off.} \end{cases}$$

$S_i(t)$ can be splitted into $S_x(t)$ and $\bar{S}_x(t)$. There are two switches in the each leg that are complementary. Thus, either $S_x(t)$ or $\bar{S}_x(t)$ is on (see Fig. 3.5).

$$S_i(t) = S_x(t) + \bar{S}_x(t). \tag{3.2}$$

Tab. 3.4 shows the relation between the two-pole switches and the switching state.

Two-pole Switch		
$S_i(t)$	$S_x(t)$	$\bar{S}_x(t)$
1	1	0
1	0	1

Table 3.4: Switching functions.

where

$$S_x(t) + \bar{S}_x(t) = 1. \tag{3.3}$$

Therefore, the model of the three-phase two-level VSI can be described by using the following equations:

$$\begin{cases} L_a \dfrac{di^a(t)}{dt} = u^a(t) - u_0^a(t) - R_a i^a(t) \\ L_b \dfrac{di^b(t)}{dt} = u^b(t) - u_0^b(t) - R_b i^b(t) \\ L_c \dfrac{di^c(t)}{dt} = u^c(t) - u_0^c(t) - R_c i^c(t) \end{cases} \tag{3.4}$$

where the phase voltages are given by

$$\begin{cases} u^a(t) = u_M^a(t) + u_{M0}(t), \\ u^b(t) = u_M^b(t) + u_{M0}(t), \\ u^c(t) = u_M^c(t) + u_{M0}(t). \end{cases} \tag{3.5}$$

where $u_{M0}(t)$ $[V]$ is the common-mode voltage between the mid-point of capacitors and the neutral point of star connection.

The voltage between the phase a,b and c and the mid-point (M) of the two capacitors are

$$\begin{cases} u_M^a(t) = S_a(t)U_{C1} - \bar{S}_a(t)U_{C2}, \\ u_M^b(t) = S_b(t)U_{C1} - \bar{S}_b(t)U_{C2}, \\ u_M^c(t) = S_c(t)U_{C1} - \bar{S}_c(t)U_{C2}. \end{cases} \tag{3.6}$$

where U_{C1} $[V]$ and U_{C2} $[V]$are the voltage across the capacitors C_1 and C_2 respectively.

If the sinusoidal voltage sources are assumed ideal and balanced (assumption (A3)), then the following holds

$$\begin{cases} \forall t > 0 : u^a(t) + u^b(t) + u^c(t) = 0, \\ \forall t > 0 : i^a(t) + i^b(t) + i^c(t) = 0. \end{cases} \tag{3.7}$$

by summation of the phase voltages of (3.5) and using (3.7), $u_{M0}(t)$ is given by

$$u_{M0}(t) = -\frac{u_M^a(t) + u_M^b(t) + u_M^c(t)}{3}. \tag{3.8}$$

By combining (3.6), (3.8) and (3.5) the following expressions are obtained

$$\begin{cases} u^a(t) = [S_a(t) - \dfrac{S_a(t)+S_b(t)+S_c(t)}{3}]U_{C1} - [\bar{S}_a(t) - \dfrac{\bar{S}_a(t)+\bar{S}_b(t)+\bar{S}_c(t)}{3}]U_{C2}, \\ u^b(t) = [S_b(t) - \dfrac{S_a(t)+S_b(t)+S_c(t)}{3}]U_{C1} - [\bar{S}_b(t) - \dfrac{\bar{S}_a(t)+\bar{S}_b(t)+\bar{S}_c(t)}{3}]U_{C2}, \\ u^c(t) = [S_c(t) - \dfrac{S_a(t)+S_b(t)+S_c(t)}{3}]U_{C1} - [\bar{S}_c(t) - \dfrac{\bar{S}_a(t)+\bar{S}_b(t)+\bar{S}_c(t)}{3}]U_{C2}. \end{cases} \tag{3.9}$$

If constant DC-link voltage U_{dc} and identical capacitances ($C_1 = C_2$) are used, then

$$U_{C1} = U_{C2} = \frac{U_{dc}}{2}. \tag{3.10}$$

The phase voltages $u^{abc}(t)$ based on the input DC-link voltage and the switching states are obtained ($\bar{S}_x(t) = 1 - S_x(t)$) [32]

$$u^{abc}(t) = \begin{bmatrix} u^a(t) \\ u^b(t) \\ u^c(t) \end{bmatrix} = \frac{U_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} S_{abc}(t). \tag{3.11}$$

where switching states are

$$S_{abc}(t) = \begin{bmatrix} S_a(t) \\ S_b(t) \\ S_c(t) \end{bmatrix}. \tag{3.12}$$

and can have $2^3 = 8$ different states.

Line-to-line voltages $u_{ltl}^{abc}(t)$ can be calculated directly from (3.6) and (3.10) such that [33]

$$u_{ltl}^{abc}(t) = \begin{bmatrix} u_{ltl}^{ab}(t) \\ u_{ltl}^{bc}(t) \\ u_{ltl}^{ca}(t) \end{bmatrix} = \begin{bmatrix} u_M^a(t) - u_M^b(t) \\ u_M^b(t) - u_M^c(t) \\ u_M^c(t) - u_M^a(t) \end{bmatrix} = U_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} S_{abc}(t). \tag{3.13}$$

The phase currents $i^{abc}(t)$ can be calculated by using (3.11) and (3.1)

$$\begin{cases} \dfrac{di^a(t)}{dt} = \dfrac{1}{L_a}[u^a(t) - u_0^a(t) - R_a i^a(t)], \\ \dfrac{di^b(t)}{dt} = \dfrac{1}{L_b}[u^b(t) - u_0^b(t) - R_b i^b(t)], \\ \dfrac{di^c(t)}{dt} = \dfrac{1}{L_c}[u^c(t) - u_0^c(t) - R_c i^c(t)]. \end{cases}$$

3.1.3 Instantanous Power Losses in Two-Level VSI ($p^{abc}_{tot-2l-VSI}(\vartheta_J(t),t)$)

The total power losses in the power semiconductor devices of a two-level inverter are composed of the on-state and the switching losses. If the switches are composed of an IGBT and an inverse power diode, the conduction losses are found by (2.37) and (2.6).

$$p^{abc}_{on-I}(\vartheta_J(t),t)=\begin{bmatrix}p^a_{on-I}(\vartheta_J(t),t)\\ p^b_{on-I}(\vartheta_J(t),t)\\ p^c_{on-I}(\vartheta_J(t),t)\end{bmatrix}=\begin{bmatrix}U_{th-I}\left(\vartheta_J\left(t\right)\right)\left|i^a_{c-I}\left(t\right)\right|+R_{d-I}\left(\vartheta_J\left(t\right)\right)\left(i^a_{c-I}\left(t\right)\right)^2\\ U_{th-I}\left(\vartheta_J\left(t\right)\right)\left|i^b_{c-I}\left(t\right)\right|+R_{d-I}\left(\vartheta_J\left(t\right)\right)\left(i^b_{c-I}\left(t\right)\right)^2\\ U_{th-I}\left(\vartheta_J\left(t\right)\right)\left|i^c_{c-I}\left(t\right)\right|+R_{d-I}\left(\vartheta_J\left(t\right)\right)\left(i^c_{c-I}\left(t\right)\right)^2\end{bmatrix}, \tag{3.14}$$

$$p^{abc}_{on-D}\left(\vartheta_J(t),t\right)=\begin{bmatrix}p^a_{on-D}\left(\vartheta_J(t),t\right)\\ p^b_{on-D}\left(\vartheta_J(t),t\right)\\ p^c_{on-D}\left(\vartheta_J(t),t\right)\end{bmatrix}=\begin{bmatrix}U_{th-D}(\vartheta_J(t))|i^a_f(t)|+R_{d-D}\left(\vartheta_J(t)\right)\left(i^a_f(t)\right)^2\\ U_{th-D}(\vartheta_J(t))|i^b_f(t)|+R_{d-D}\left(\vartheta_J(t)\right)\left(i^b_f(t)\right)^2\\ U_{th-D}(\vartheta_J(t))|i^c_f(t)|+R_{d-D}\left(\vartheta_J(t)\right)\left(i^c_f(t)\right)^2\end{bmatrix}. \tag{3.15}$$

As it can be seen from Tab. 3.2, the conduction losses depend on the switching states and the direction of currents. This means that we have the conduction power losses in the IGBT if the switching state is one and the current direction is positive or the switching states is zero and the current direction is negative; the conduction power losses in the diode if the switching state is one and the current direction is negative or the switching states is zero the and current direction is positive. The current direction and the switching states determine which transistor or diode is on . The current direction can be found by appling the Heaviside Step Function. Heaviside Step function is

$$H(x)=\begin{cases}1, & \text{if } x>0\\ 0, & \text{if } x<0.\end{cases}$$

If we define matrix of $A(t)$ as a diagonal matrix such that

$$\forall t\in\mathbb{R}: A(t)=\begin{bmatrix}S_a(t) & 0 & 0\\ 0 & S_b(t) & 0\\ 0 & 0 & S_c(t)\end{bmatrix}, \tag{3.16}$$

matrix of $B(t)$ as a column matrix such that

$$\forall t\in\mathbb{R}: B(t)=\begin{bmatrix}H(i^a(t))\\ H(i^b(t))\\ H(i^c(t))\end{bmatrix}, \tag{3.17}$$

matrix of $U(t)$ as a unit column matrix such that

$$\forall t\in\mathbb{R}: U(t)=\begin{bmatrix}1\\ 1\\ 1\end{bmatrix}, \tag{3.18}$$

and finally, matrix of $I(t)$ as an identity matrix such that

$$\forall t \in \mathbb{R} : I(t) = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}. \tag{3.19}$$

The instantanous conduction power losses $p^{abc}_{on-2L-ID}(\vartheta_J(t), t)$ $[W]$ are given by

$$\begin{aligned} p^{abc}_{on-2L-ID}(\vartheta_J(t), t) = [p^{abc}_{on-I}(\vartheta_J(t), t)]^T (& \underbrace{A(t)B(t)}_{S_x(t)=1 \text{ and } i^x(t)>0.} + \underbrace{[I(t) - A(t)][U(t) - B(t)]}_{S_x(t)=0 \text{ and } i^x(t)<0.}) \\ + [p^{abc}_{on-D}(\vartheta_J(t), t)]^T (& \underbrace{A(t)[U(t) - B(t)]}_{S_x(t)=1 \text{ and } i^x(t)<0.} + \underbrace{[I(t) - A(t)]B(t)}_{S_x(t)=0 \text{ and } i^x(t)>0.}). \end{aligned} \tag{3.20}$$

where $[p^{abc}_{on-I}(\vartheta_J(t), t)]^T$ and $[p^{abc}_{on-D}(\vartheta_J(t), t)]^T$ are transpose of (3.14) and (3.15) respectively.

The switching power losses can be calclated from Tab. 3.3, (2.44) or (2.31) and (2.16). The turn-on and turn-off switching power losses of the IGBT and the reverse recovery of the diode are given by

$$\begin{aligned} p^{abc}_{sw-I-on}(\vartheta_J(t), t)) &= \begin{bmatrix} p^a_{sw-I-on}(\vartheta_J(t), t)) \\ p^b_{sw-I-on}(\vartheta_J(t), t)) \\ p^c_{sw-I-on}(\vartheta_J(t), t)) \end{bmatrix} \\ &= \begin{bmatrix} E_{sw-I-on}(\vartheta_J(t), t)(\frac{|i^a_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}[1 + \alpha_{\vartheta-I}(\vartheta_J(t) - \vartheta_J(t_0))]f_s \\ E_{sw-I-on}(\vartheta_J(t), t)(\frac{|i^b_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}[1 + \alpha_{\vartheta-I}(\vartheta_J(t) - \vartheta_J(t_0))]f_s \\ E_{sw-I-on}(\vartheta_J(t), t)(\frac{|i^c_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}[1 + \alpha_{\vartheta-I}(\vartheta_J(t) - \vartheta_J(t_0))]f_s \end{bmatrix}, \end{aligned} \tag{3.21}$$

$$\begin{aligned} p^{abc}_{sw-I-off}(\vartheta_J(t), t)) &= \begin{bmatrix} p^a_{sw-I-off}(\vartheta_J(t), t)) \\ p^b_{sw-I-off}(\vartheta_J(t), t)) \\ p^c_{sw-I-off}(\vartheta_J(t), t)) \end{bmatrix} \\ &= \begin{bmatrix} E_{sw-I-off}(\vartheta_J(t), t)(\frac{|i^a_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}[1 + \alpha_{\vartheta-I}(\vartheta_J(t) - \vartheta_J(t_0))]f_s \\ E_{sw-I-off}(\vartheta_J(t), t)(\frac{|i^b_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}[1 + \alpha_{\vartheta-I}(\vartheta_J(t) - \vartheta_J(t_0))]f_s \\ E_{sw-I-off}(\vartheta_J(t), t)(\frac{|i^c_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}[1 + \alpha_{\vartheta-I}(\vartheta_J(t) - \vartheta_J(t_0))]f_s \end{bmatrix}, \end{aligned} \tag{3.22}$$

$$p_{rr-D}^{abc}\left(\vartheta_J(t),t\right) = \begin{bmatrix} p_{rr-D}^{a}\left(\vartheta_J(t),t\right) \\ p_{rr-D}^{b}\left(\vartheta_J(t),t\right) \\ p_{rr-D}^{c}\left(\vartheta_J(t),t\right) \end{bmatrix}$$
$$= \begin{bmatrix} \frac{U_R Q_{rr}}{4}\sqrt{\left(\frac{|i_f^a(t)|}{I_{f-rated}}\right)}\left(\frac{U_R}{U_{R-rated}}\right)^{0.6}[1+\alpha_{\vartheta-I}(\vartheta_J(t)-\vartheta_J(t_0))]f_s \\ \frac{U_R Q_{rr}}{4}\sqrt{\left(\frac{|i_f^b(t)|}{I_{f-rated}}\right)}\left(\frac{U_R}{U_{R-rated}}\right)^{0.6}[1+\alpha_{\vartheta-I}(\vartheta_J(t)-\vartheta_J(t_0))]f_s \\ \frac{U_R Q_{rr}}{4}\sqrt{\left(\frac{|i_f^c(t)|}{I_{f-rated}}\right)}\left(\frac{U_R}{U_{R-rated}}\right)^{0.6}[1+\alpha_{\vartheta-I}(\vartheta_J(t)-\vartheta_J(t_0))]f_s \end{bmatrix}. \quad (3.23)$$

As it can be seen from Tab. 3.3, the switching power losses are dependent upon change in the switching vector $S_{abc}(t)$ and the direction of phase current $i^{abc}(t)$. When the switching vector $S_{abc}(t)$ goes from one to zero or vice versa, the switching power losses occur. We use the discrete space to find these changes. Therefore, the switching vector, the phase currents and the switching power losses are mapped from continuous space to discrete space such that

$$\forall t \in \mathbb{R} : S_{abc}(t) \rightarrow \forall k \in \mathbb{Z} : S_{abc}[k], \quad (3.24)$$
$$\forall t \in \mathbb{R} : i^{abc}(t) \rightarrow \forall k \in \mathbb{Z} : i^{abc}[k], \quad (3.25)$$
$$\forall t \in \mathbb{R} : p_{rr-D}^{abc}\left(\vartheta_J(t),t\right) \rightarrow \forall k \in \mathbb{Z} : p_{rr-D}^{abc}[\vartheta_J[k],k], \quad (3.26)$$
$$\forall t \in \mathbb{R} : p_{sw-M-on}^{abc}(\vartheta_J(t),t) \rightarrow \forall k \in \mathbb{Z} : p_{sw-M-on}^{abc}[\vartheta_J[k],k], \quad (3.27)$$
$$\forall t \in \mathbb{R} : p_{sw-M-off}^{abc}(\vartheta_J(t),t) \rightarrow \forall k \in \mathbb{Z} : p_{sw-M-off}^{abc}[\vartheta_J[k],k], \quad (3.28)$$
$$\forall t \in \mathbb{R} : p_{sw-I-on}^{abc}(\vartheta_J(t),t) \rightarrow \forall k \in \mathbb{Z} : p_{sw-I-on}^{abc}[\vartheta_J[k],k], \quad (3.29)$$
$$\forall t \in \mathbb{R} : p_{sw-I-off}^{abc}(\vartheta_J(t),t) \rightarrow \forall k \in \mathbb{Z} : p_{sw-I-off}^{abc}[\vartheta_J[k],k]. \quad (3.30)$$

We compare the switching vector of $S_{abc}[k-1]$ with $S_{abc}[k]$ to find when the changes occur at switching vector. Then, the direction of the phase currents $i^{abc}[k]$ are used to find which switches or diodes have the switching power losses. Just like the conduction power losses, some matrices are introduced. The matrix of $A[k]$ as a diagonal matrix such that

$$\forall k \in \mathbb{Z} : A[k] = \begin{bmatrix} S_a[k] & 0 & 0 \\ 0 & S_b[k] & 0 \\ 0 & 0 & S_c[k] \end{bmatrix}, \quad (3.31)$$

matrix of $B[k]$ as a column matrix such that

$$\forall k \in \mathbb{Z} : B[k] = \begin{bmatrix} H(i^a[k]) \\ H(i^b[k]) \\ H(i^c[k]) \end{bmatrix}, \quad (3.32)$$

matrix of $U[k]$ as an unit column matrix such that

$$\forall k \in \mathbb{Z} : U[k] = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}, \quad (3.33)$$

and finally, matrix of $I[k]$ as an identity matrix such that

$$\forall k \in \mathbb{Z} : I[k] = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}. \tag{3.34}$$

The total switching power losses $p^{abc}_{sw-2L-ID}[\vartheta_J[k], k]$ are given by

$$\begin{aligned} p^{abc}_{sw-2L-ID}[\vartheta_J[k], k] = (p^{abc}_{rr-D}[\vartheta_J[k], k])^T \\ (\underbrace{(I[k-1] - A[k-1])A[k]B[k]}_{S_x[k-1]=0 \text{ and } S_x[k]=1 \text{ and } i^x[k]>0.} + \underbrace{A[k-1](I[k] - A[k])(U[k] - B[k]))}_{S_x[k-1]=1 \text{ and } S_x[k]=0 \text{ and } i^x[k]<0.} \\ + (p^{abc}_{sw-I-on}[\vartheta_J[k], k])^T \\ (\underbrace{(I[k-1] - A[k-1])A[k]B[k]}_{S_x[k-1]=0 \text{ and } S_x[k]=1 \text{ and } i^x[k]>0.} + \underbrace{A[k-1](I[k] - A[k])(U[k] - B[k]))}_{S_x[k-1]=1 \text{ and } S_x[k]=0 \text{ and } i^x[k]<0.} \\ + (p^{abc}_{sw-I-off}[\vartheta_J[k], k])^T \\ (\underbrace{(A[k-1])(I[k] - A[k])B[k]}_{S_x[k-1]=1 \text{ and } S_x[k]=0 \text{ and } i^x[k]>0.} + \underbrace{(I[k-1] - A[k-1])A[k](U[k] - B[k]))}_{S_x[k-1]=0 \text{ and } S_x[k]=1 \text{ and } i^x[k]<0.}. \end{aligned} \tag{3.35}$$

where $(p^{abc}_{rr-D}[\vartheta_J[k], k])^T$, $(p^{abc}_{sw-I-on}[\vartheta_J[k], k])^T$ and $(p^{abc}_{sw-I-off}[\vartheta_J[k], k])^T$ are transpose of (3.23), (3.21) and (3.22) respectively.

Then, a low pass filter is used to reconstruct the continuous switching power losses from the discrete switching power losses [34].

$$p^{abc}_{sw-2L-ID}[\vartheta_J[k], k] \rightarrow p^{abc}_{sw-2L-ID}(\vartheta_J(t), t). \tag{3.36}$$

Finally, the total instantaneous power losses for a two-level voltage source inverter is given by

$$p^{abc}_{tot-2l-VSI}(\vartheta_J(t), t) = p^{abc}_{sw-2L-ID}(\vartheta_J(t), t) + p^{abc}_{on-2L-ID}(\vartheta_J(t), t). \tag{3.37}$$

If the switches are composed of a MOSFET and an inverse power diode, we should only replace the MOSFET's equations with the IGBT's equations.

3.2 Three-Level NPC Voltage Source Inverter (3-L NPC VSI)

Fig. 3.7 shows the schematic circuit of a three-phase three-level neutral point clamped voltage source inverter. The inverter leg a consists of four transistors $T_{a1}(t)$, $T_{a2}(t)$, $\bar{T}_{a1}(t)$ and $\bar{T}_{a2}(t)$ with four anti-parallel diodes $D_{a1}(t)$ to $D_{a4}(t)$. The transistors are switched in pairs, the complement transistors are $\bar{T}_{a1}(t)$ and $\bar{T}_{a2}(t)$. The switches $S_{a1}(t)$ and $\bar{S}_{a2}(t)$ ($S_x(t)$ is a switch and it is composed of a transistor $T_x(t)$ and an anti-parallel diode $D_x(t)$) are outer switches while the switches $S_{a2}(t)$ and $\bar{S}_{a1}(t)$ are inner switches. On the DC side of the inverter, the DC-link capacitor is split into two capacitor C_1 and C_2, providing a neutral point M. $D_{a5}(t)$ and $D_{a6}(t)$ are connected to the neutral point and are called the clamping diodes. When the transistors $T_{a2}(t)$ and $\bar{T}_{a1}(t)$ are on, the phase a is connected to the neutral point M through either $D_{a5}(t)$ or $D_{a6}(t)$.

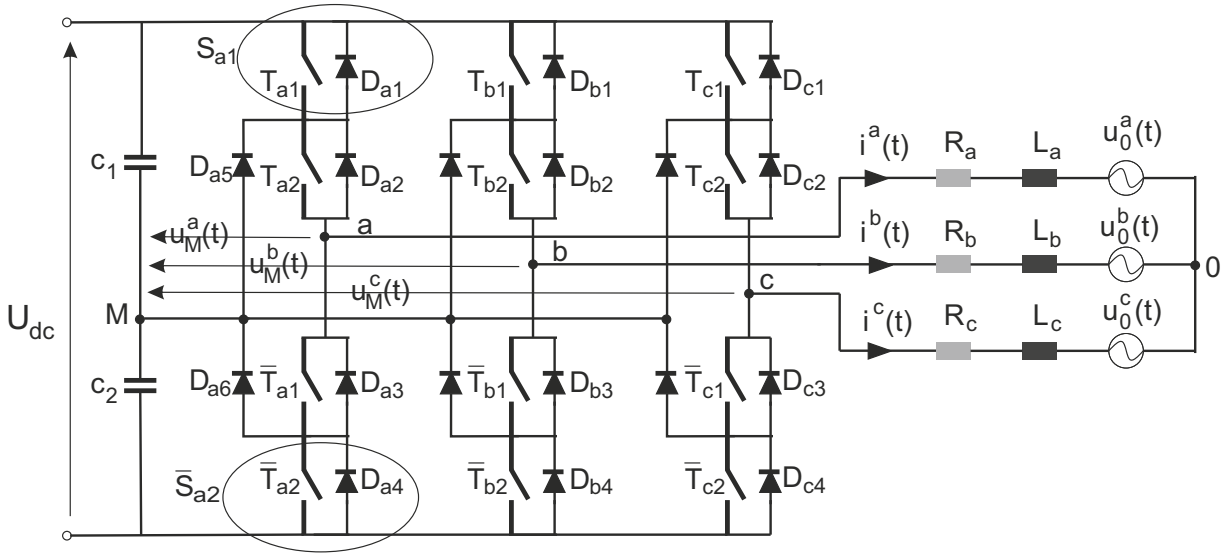


Figure 3.7: Schematic circuit of the three-phase three-level NPC VSI.

3.2.1 Switch States and Commutations

Tab. 3.5 shows the switching states in the NPC inverter. In order to produce three-levels voltage, only two of four switches in each phase leg are turned on at any time. Thus, the total number of different switch states are $2^3 = 27$. Because we have four switches and two of them are switched in pairs ($\bar{S}_{x1}(t)$ and $\bar{S}_{x2}(t)$), the switching vector can be defined as a

$S_{x1}(t)$	$S_{x2}(t)$	$\bar{S}_{x1}(t)$	$\bar{S}_{x2}(t)$	$u_M^x(t)$, $x \in \{a, b, c\}$
1	1	0	0	U_{C1} $[V]$
0	1	1	0	0
0	0	1	1	$-U_{C2}$ $[V]$

Table 3.5: Definition of switching states of three-level NPC VSI.

matrix such that

$$S_{abc}^{1,2}(t) = \begin{bmatrix} S_{a1}(t) & S_{a2}(t) \\ S_{b1}(t) & S_{b2}(t) \\ S_{c1}(t) & S_{c2}(t) \end{bmatrix}. \tag{3.38}$$

In Tab. 3.5, if the upper switches $S_{x1}(t)$ and $S_{x2}(t)$ are turned on, $u_M^x(t)$ is equal to U_{C1}, where $u_M^x(t)$ is the voltage at terminal x ($x \in \{a, b, c\}$) with respect to the neutral point M and U_{C1} is the voltage across the capacitor C_1. If $\bar{S}_{x1}(t)$ and $\bar{S}_{x2}(t)$ are on $u_M^x(t) = -U_{C2}$, where U_{C2} is the voltage across the capacitor C_2. If the inner two switches $\bar{S}_{x1}(t)$ and $S_{x2}(t)$ are on, $u_M^x(t)$ is zero through the clamping diodes $D_{x5}(t)$ or $D_{x6}(t)$. Depending on the direction of phase current $i^x(t)$, one of the two clamping diodes is turned on. For instance, if $i^x(t) > 0$, $D_{x5}(t)$ should be turned on and the terminal x is connected to the neutral point M through the conduction of $D_{x5}(t)$ and $T_{x2}(t)$. Therefore, $u_M^x(t)$ has three voltage levels U_{C1}, 0, and $-U_{C2}$.

Fig. 3.8 illustrates the phase current paths $i^x(t)$ ($x \in \{a, b, c\}$) in three-level NPC VSI. Either the upper switches or the lower switches are on, two transistors or two diodes lie within the phase current path. If the inner switches are on, the direction of $i^x(t)$ determines whether $\bar{T}_{x1}(t)$ or $T_{x2}(t)$ conducts. In this state, one transistor and one diode conduct. Tab. 3.6 summarizes the on-state losses, where $[S_{x1}(t)\ \ S_{x2}(t)\,]$ shows which one of the switches $S_{x1}(t)$ and $S_{x2}(t)$ are on. For example, [1 0] means $S_{x1}(t)$ is on, while $S_{x2}(t)$ is off.

Commutation processes make the switching losses. The switching losses occur when the switches are turning on or off. Here, for example, a commutation process from $S_x^{1,2}(t) = [0\ 1]$ to $S_x^{1,2}(t) = [1\ 1]$ is considered. Fig. 3.9 shows the schematic circuit diagram of the inverter leg x ($x \in \{a, b, c\}$) during commutation process when $i^x(t) > 0$. The direction of the phase current $i^x(t)$ determines which switches should be turned on or off. In switching state $S_x^{1,2}(t)$ = [0 1], the switches $T_{x2}(t)$ and $\bar{T}_{x1}(t)$ are on while the switches $T_{x1}(t)$ and $\bar{T}_{x2}(t)$ are off. The clamping diode D_{x5} is turned on by the positive phase current $i^x(t) > 0$. When $\bar{T}_{x1}(t)$ is turned off and $T_{x1}(t)$ is turned on, the clamping diode $D_{x5}(t)$ is reverse-biased. Therefore, D_{x5} is turned off and the path of load current $i^x(t)$ is forced to pass through $T_{x1}(t)$.

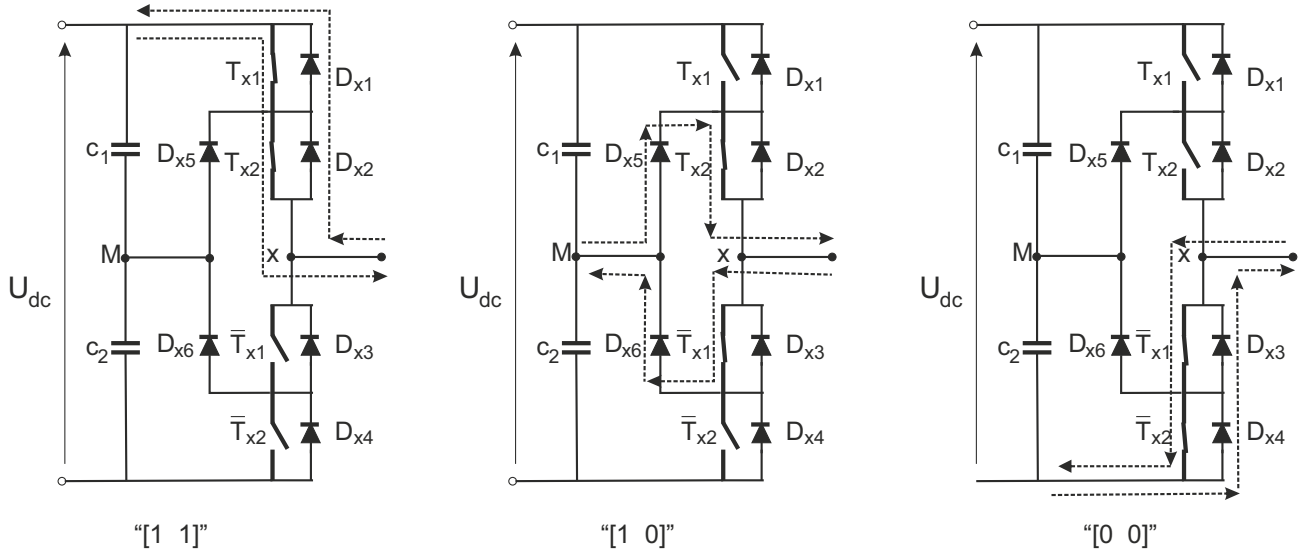


Figure 3.8: The conduction current paths of three-level NPC VSI.

$S_x^{1,2}(t)$	$T_{x1}(t)$	$D_{x1}(t)$	$T_{x2}(t)$	$D_{x2}(t)$	$\bar{T}_{x1}(t)$	$D_{x3}(t)$	$\bar{T}_{x2}(t)$	$D_{x4}(t)$	$D_{x5}(t)$	$D_{x6}(t)$
$i^x(t) > 0$, $x \in \{a, b, c\}$										
[1 1]	On	-	On	-	-	-	-	-	-	-
[0 1]	-	-	On	-	-	-	-	-	On	-
[0 0]	-	-	-	-	-	On	-	On	-	-
$i^x(t) < 0$, $x \in \{a, b, c\}$										
[1 1]	-	On	-	On	-	-	-	-	-	-
[0 1]	-	-	-	-	On	-	-	-	-	On
[0 0]	-	-	-	-	On	-	On	-	-	-

Table 3.6: Conduction losses in three-level NPC VSI.

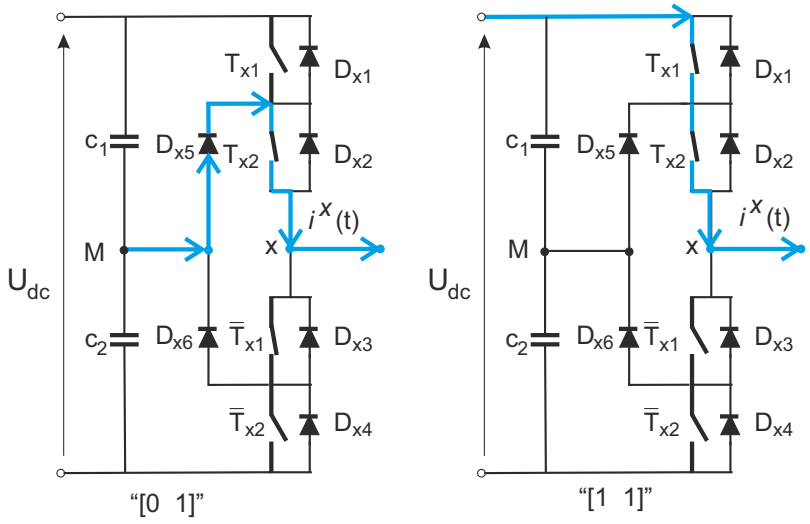


Figure 3.9: Commutations in the three-level NPC VSI for positive current.

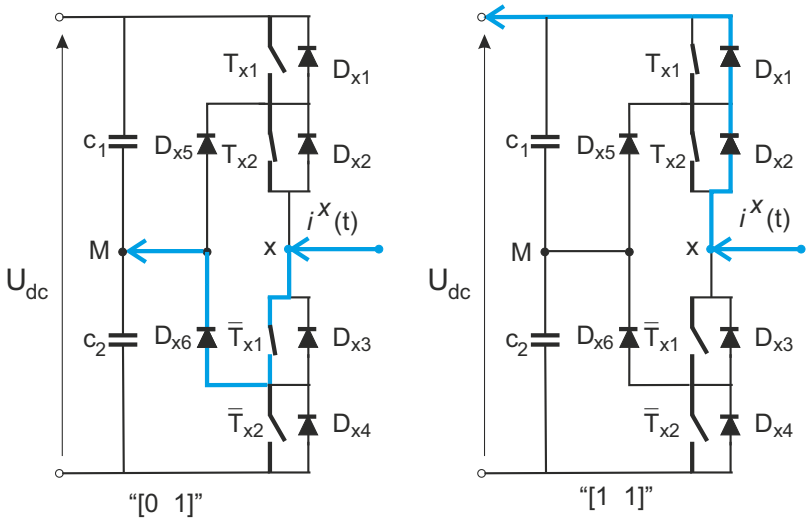


Figure 3.10: Commutations in the three-level NPC VSI for negative current.

Fig. 3.10 shows the commutation process when $i^x(t) < 0$. In $S_x^{1,2}(t) = [0\ 0]$, $T_{x2}(t)$ and $\bar{T}_{x1}(t)$ are turn-on and the clamping diode $D_{x6}(t)$ provides the path for the negative phase current $i^x(t)$. When $S_x^{1,2}(t) = [1\ 1]$, $\bar{T}_{x1}(t)$ is turned off and the phase current forces diodes

$D_{x1}(t)$ and $D_{x2}(t)$ to be turned on. The current $i^x(t)$ is commutated from $\bar{T}_{x1}(t)$ and $D_{x6}(t)$ to the diodes $D_{x1}(t)$ and $D_{x2}(t)$. Tab. 3.7 summarizes the switching losses.

$S_x^{1,2}(t)$	$T_{x1}(t)$	$D_{x1}(t)$	$T_{x2}(t)$	$D_{x2}(t)$	$\bar{T}_{x1}(t)$	$D_{x3}(t)$	$\bar{T}_{x2}(t)$	$D_{x4}(t)$	$D_{x5}(t)$	$D_{x6}(t)$
$i^x(t) > 0,\ x \in \{a, b, c\}$										
[1 1] $\longrightarrow$ [0 1]	Off	-	-	-	-	-	-	-	On	-
[0 1] $\longrightarrow$ [1 1]	On	-	-	-	-	-	-	-	Off	-
[0 1] $\longrightarrow$ [0 0]	-	-	Off	-	-	On	-	On	Off	-
[0 0] $\longrightarrow$ [0 1]	-	-	On	-	-	Off	-	Off	On	-
$i^x(t) < 0,\ x \in \{a, b, c\}$										
[1 1] $\longrightarrow$ [0 1]	-	Off	-	Off	On	-	-	-	-	On
[0 1] $\longrightarrow$ [1 1]	-	On	-	On	Off	-	-	-	-	Off
[0 0] $\longrightarrow$ [0 1]	-	-	-	-	-	-	Off	-	-	On
[0 1] $\longrightarrow$ [0 0]	-	-	-	-	-	-	On	-	-	Off

Table 3.7: Switching losses in three-level NPC VSI.

3.2.2 Modeling of the Three-Level NPC VSI

The three-phase three-level NPC VSI is composed of a DC-link capacitor, switches and diodes which has been connected to the load. First the switches and load are modeled. Afterwards, the modeling of the three-level NPC VSI is presented.

(3.1) can be used to model three-phase AC side. Moreover, the VSI is composed of the power switches. All the switches in one leg of the three-level NPC VSI can be considered as a three-pole switch which can connect the phase to any DC-link voltage according to the modulation strategy. Therefore, the three-pole switchs $S_i(t)$ ($i \in \{a, b, c\}$) are introduced. Tab. 3.8 represents the three-pole switch. $S_i(t)$ is defined as [35]

$$S_i(t) = \begin{cases} \mathrm{S}_i^U(t), & \text{if } S_x^{1,2}(t) = [1\ 1] \\ \mathrm{S}_i^M(t), & \text{if } S_x^{1,2}(t) = [0\ 1] \\ \mathrm{S}_i^L(t), & \text{if } S_x^{1,2}(t) = [0\ 0]. \end{cases}$$

where $S_i^U(t)$ means the upper switches are on or $S_x^{1,2}(t) = [1\ 1]$, $S_i^M(t)$ means the inner switches are on or $S_x^{1,2}(t) = [0\ 1]$, and $S_i^L(t)$ means the lower switches are on or $S_x^{1,2}(t) = [0\ 0]$. Moreover, (3.39) shows that at any time only one of the $S_i^U(t)$, $S_i^M(t)$ and $S_i^L(t)$ is one [35].

$$i \in \{a, b, c\}, S_i^U(t) + S_i^M(t) + S_i^L(t) = 1. \tag{3.39}$$

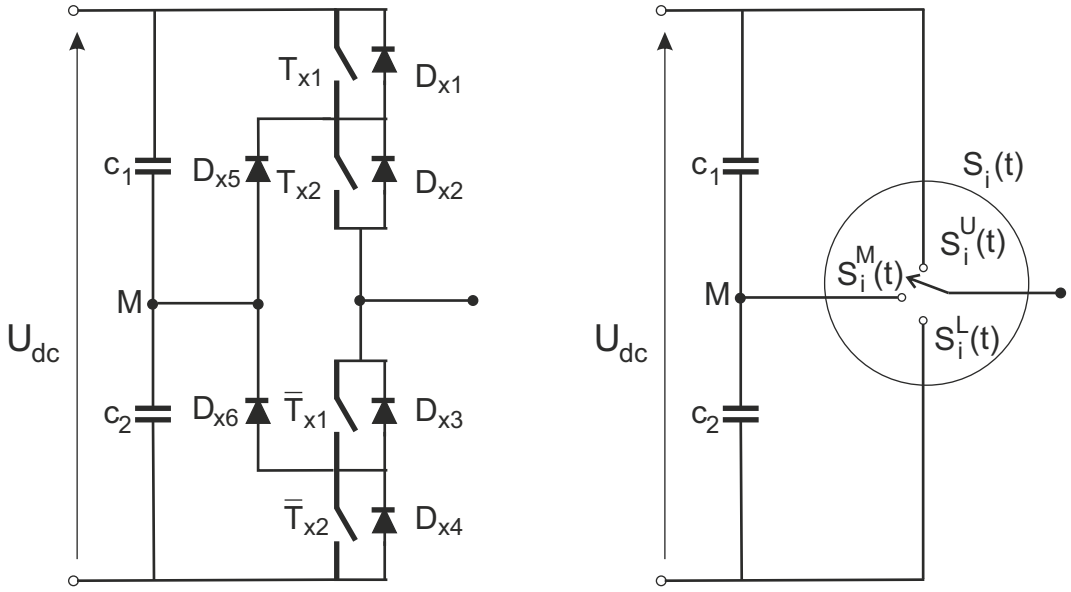


Figure 3.11: Power swtiches model.

The relationship between switching states and the three-pole switch shows in Tab. 3.8 .

Switching States				Three-pole Switch			
$S_{x1}(t)$	$S_{x2}(t)$	$\bar{S}_{x1}(t)$	$\bar{S}_{x2}(t)$	$S_i(t)$	$S_i^U(t)$	$S_i^M(t)$	$S_i^L(t)$
1	1	0	0	$S_i^U(t)$	1	0	0
0	1	1	0	$S_i^M(t)$	0	1	0
0	0	1	1	$S_i^L(t)$	0	0	1

Table 3.8: Relationship between switching states and the three-pole switch.

Now, the modeling of the three-level NPC VSI is represented mathematically. Before modeling two assumptions are taken.

(A1). All switching devices are ideal with identical characteristics.

(A2). All parasitic elements of circuit components are considered insignificant.

Fig. 3.12 shows the schematic diagram model of the three-phase three-level NPC VSI. Therefore, the modeling of the three-phase three-level NPC VSI can be described by using the following equations.

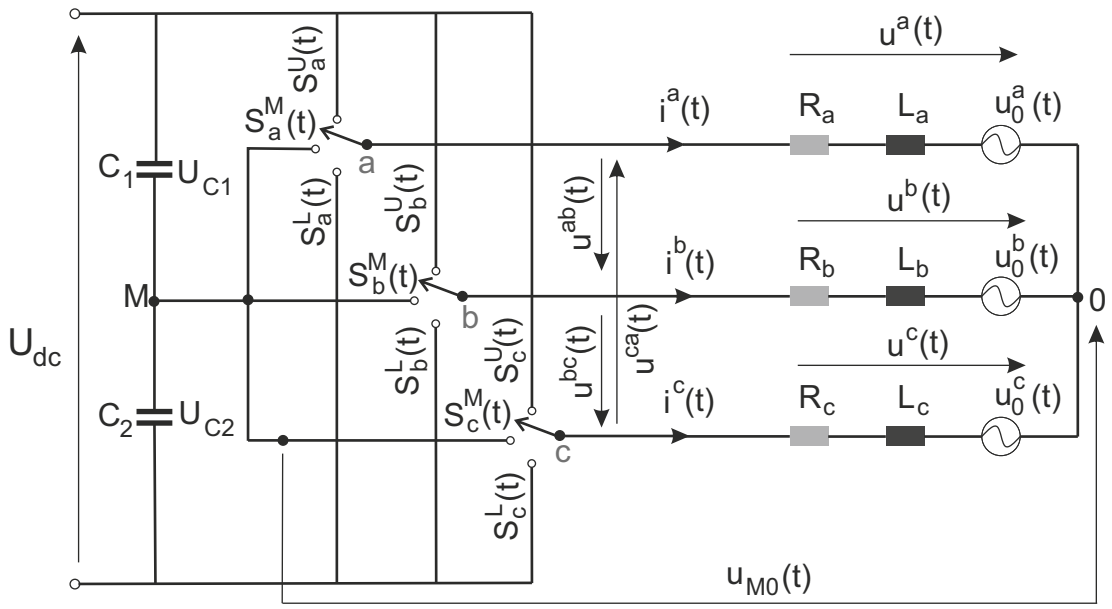


Figure 3.12: Schematic circuit of the three-phase three-level NPC VSI.

$$\begin{cases} L_a \dfrac{di^a(t)}{dt} = u^a(t) - u_0^a(t) - R_a i^a(t), \\ L_b \dfrac{di^b(t)}{dt} = u^b(t) - u_0^b(t) - R_b i^b(t), \\ L_c \dfrac{di^c(t)}{dt} = u^c(t) - u_0^c(t) - R_c i^c(t). \end{cases} \tag{3.40}$$

where the phase voltages are given by

$$\begin{cases} u^a(t) = u_M^a(t) + u_{M0}(t), \\ u^b(t) = u_M^b(t) + u_{M0}(t), \\ u^c(t) = u_M^c(t) + u_{M0}(t). \end{cases} \tag{3.41}$$

where $u_{M0}(t)$ is the voltage between the mid-point M of the capacitors and the neutral point 0 of star connection.

The voltage between the phase a,b and c and the mid-point of the two capacitors (M) are

$$\begin{cases} u_M^a(t) = S_a^U(t)U_{C1} - S_a^L(t)U_{C2} + S_a^M(t)\cdot 0, \\ u_M^b(t) = S_b^U(t)U_{C1} - S_b^L(t)U_{C2} + S_b^M(t)\cdot 0, \\ u_M^c(t) = S_c^U(t)U_{C1} - S_c^L(t)U_{C2} + S_c^M(t)\cdot 0. \end{cases} \tag{3.42}$$

where U_{C1} and U_{C2} are the voltage across the capacitors C_1 and C_2 respectively.

If the sinusoidal voltage sources are assumed ideal and balanced

$$\begin{cases} u^a(t) + u^b(t) + u^c(t) = 0, \\ i^a(t) + i^b(t) + i^c(t) = 0, \end{cases} \tag{3.43}$$

then, by summation of the phase voltages of (3.41) and using (3.43), $u_{M0}(t)$ is given by

$$u_{M0}(t) = -\frac{u_M^a(t) + u_M^b(t) + u_M^c(t)}{3}. \tag{3.44}$$

By combining (3.42), (3.44) and (3.41) the following expressions are obtained

$$\begin{cases} u^a(t) = [S_a^U(t) - \dfrac{S_a^U(t) + S_b^U(t) + S_c^U(t)}{3}]U_{C1} - [\bar{S}_a^L(t) - \dfrac{\bar{S}_a^L(t) + \bar{S}_b^L(t) + \bar{S^L}_c(t)}{3}]U_{C2}, \\ u^b(t) = [S_b^U(t) - \dfrac{S_a^U(t) + S_b^U(t) + S_c^U(t)}{3}]U_{C1} - [\bar{S}_b^L(t) - \dfrac{\bar{S}_a^L(t) + \bar{S}_b^L(t) + \bar{S}_c^L(t)}{3}]U_{C2}, \\ u^c(t) = [S_c^U(t) - \dfrac{S_a^U(t) + S_b^U(t) + S_c^U(t)}{3}]U_{C1} - [\bar{S}_c^L(t) - \dfrac{\bar{S}_a^L(t) + \bar{S}_b^L(t) + \bar{S}_c^L(t)}{3}]U_{C2}. \end{cases} \tag{3.45}$$

If constant DC-link voltage U_{dc} and identical capacitances $C_1 = C_2$ are assumed, i.e.

$$U_{C2} = U_{C1} = \frac{U_{dc}}{2}, \tag{3.46}$$

thus, the phase voltages $u^{abc}(t)$ based on the input DC-link voltage and the switching states are obtained

$$u^{abc}(t) = \begin{bmatrix} u^a(t) \\ u^b(t) \\ u^c(t) \end{bmatrix} = \frac{U_{dc}}{6} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \left(\begin{bmatrix} S_a^U(t) \\ S_b^U(t) \\ S_c^U(t) \end{bmatrix} - \begin{bmatrix} S_a^L(t) \\ S_b^L(t) \\ S_c^L(t) \end{bmatrix} \right). \tag{3.47}$$

where $S_a^U(t)$, $S_b^U(t)$ and $S_c^U(t)$ are the upper switches and $S_a^L(t)$, $S_b^L(t)$ and $S_c^L(t)$ are the lower switches that are complementary to the upper switches.

Line-to-line voltages $u_{ltl}^{abc}(t)$ can be calculated directly from (3.42) and (3.46) such that

$$u_{ltl}^{abc}(t) = \begin{bmatrix} u_{ltl}^{ab}(t) \\ u_{ltl}^{bc}(t) \\ u_{ltl}^{ca}(t) \end{bmatrix} = \begin{bmatrix} u_M^a(t) - u_M^b(t) \\ u_M^b(t) - u_M^c(t) \\ u_M^c(t) - u_M^a(t) \end{bmatrix} = \frac{U_{dc}}{2} \begin{bmatrix} 1 & -1 & 0 \\ -0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \left[\begin{bmatrix} S_a^U(t) \\ S_b^U(t) \\ S_c^U(t) \end{bmatrix} - \begin{bmatrix} S_a^L(t) \\ S_b^L(t) \\ S_c^L(t) \end{bmatrix} \right]. \tag{3.48}$$

At the end, the relationship beween three-pole switch matrix and switching vector can be presented by the Heaviside Step Function. The Heaviside Step Function is defined as

$$H(t-\alpha) = \begin{cases} 1, & t > \alpha \\ 0, & t \leqslant \alpha. \end{cases}$$

where α is a constant. Thus,

$$S_{abc}^U(t) = \begin{bmatrix} S_a^U(t) \\ S_b^U(t) \\ S_c^U(t) \end{bmatrix} = H\left(\begin{bmatrix} S_{a1}(t) & S_{a2}(t) \\ S_{b1}(t) & S_{b2}(t) \\ S_{c1}(t) & S_{c2}(t) \end{bmatrix} \begin{bmatrix} 1 \\ 1 \end{bmatrix} - \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \right) = \underbrace{\begin{bmatrix} H(S_{a1}(t) + S_{a2}(t) - 1) \\ H(S_{b1}(t) + S_{b2}(t) - 1) \\ H(S_{c1}(t) + S_{c2}(t) - 1) \end{bmatrix}}_{\text{If } S_{x1}(t) = 1 \text{ and } S_{x2}(t) = 1 \text{ then } S_x^U(t) = 1.}, \tag{3.49}$$

and

$$S_{abc}^L(t) = \begin{bmatrix} S_a^L(t) \\ S_b^L(t) \\ S_c^L(t) \end{bmatrix} = H\left(\begin{bmatrix} \bar{S}_{a1}(t) & \bar{S}_{a2}(t) \\ \bar{S}_{b1}(t) & \bar{S}_{b2}(t) \\ \bar{S}_{c1}(t) & \bar{S}_{c2}(t) \end{bmatrix} \begin{bmatrix} 1 \\ 1 \end{bmatrix} - \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \right) = \underbrace{\begin{bmatrix} H(\bar{S}_{a1}(t) + \bar{S}_{a2}(t) - 1) \\ H(\bar{S}_{b1}(t) + \bar{S}_{b2}(t) - 1) \\ H(\bar{S}_{c1}(t) + \bar{S}_{c2}(t) - 1) \end{bmatrix}}_{\text{If } S_{x1}(t) = 0 \text{ and } S_{x2}(t) = 0 \text{ then } S_x^L(t) = 1.}. \tag{3.50}$$

3.2.3 Instantaneous Power Losses in Three-Level Neutral Point Clamped Voltage Source Inverter ($p^{abc}_{tot-3l-NPC-VSI}(\vartheta_J(t),t)$)

The total power losses in the power semiconductor devices of a three-level NPC VSI are composed of the on-state and the switching losses. If the switches are composed of an IGBT and an inverse power diode, the conduction losses are found by (2.37) and (2.6).

$$p^{abc}_{on-I}(\vartheta_J(t),t) = \begin{bmatrix} p^a_{on-I}(\vartheta_J(t),t) \\ p^b_{on-I}(\vartheta_J(t),t) \\ p^c_{on-I}(\vartheta_J(t),t) \end{bmatrix} = \begin{bmatrix} U_{th-I}\left(\vartheta_J\left(t\right)\right)\left|i^a_{c-I}\left(t\right)\right| + R_{d-I}\left(\vartheta_J\left(t\right)\right)\left(i^a_{c-I}\left(t\right)\right)^2 \\ U_{th-I}\left(\vartheta_J\left(t\right)\right)\left|i^b_{c-I}\left(t\right)\right| + R_{d-I}\left(\vartheta_J\left(t\right)\right)\left(i^b_{c-I}\left(t\right)\right)^2 \\ U_{th-I}\left(\vartheta_J\left(t\right)\right)\left|i^c_{c-I}\left(t\right)\right| + R_{d-I}\left(\vartheta_J\left(t\right)\right)\left(i^c_{c-I}\left(t\right)\right)^2 \end{bmatrix}, \tag{3.51}$$

$$p^{abc}_{on-D}\left(\vartheta_J(t),t\right) = \begin{bmatrix} p^a_{on-D}\left(\vartheta_J(t),t\right) \\ p^b_{on-D}\left(\vartheta_J(t),t\right) \\ p^c_{on-D}\left(\vartheta_J(t),t\right) \end{bmatrix} = \begin{bmatrix} U_{th-D}(\vartheta_J(t))|i^a_f(t)| + R_{d-D}\left(\vartheta_J(t)\right)\left(i^a_f(t)\right)^2 \\ U_{th-D}(\vartheta_J(t))|i^b_f(t)| + R_{d-D}\left(\vartheta_J(t)\right)\left(i^b_f(t)\right)^2 \\ U_{th-D}(\vartheta_J(t))|i^c_f(t)| + R_{d-D}\left(\vartheta_J(t)\right)\left(i^c_f(t)\right)^2 \end{bmatrix}. \tag{3.52}$$

As it can be seen from Tab. 3.6, the conduction losses depend on the switching vector and the direction of currents. This means that we have the conduction power losses in the IGBT if $S^{1,2}_{abc}(t)$= [1 1] and the $i^x(t) > 0$ or $S^{1,2}_x(t)$= [0 1] and $i^x(t) > 0$ or $S^{1,2}_x(t)$= [0 0] and $i^x(t) < 0$ or $S^{1,2}_x(t)$= [0 1] and $i^x(t) < 0$, and the conduction power losses in the diode if $S^{1,2}_x(t)$= [0 0] and $i^x(t) > 0$ or $S^{1,2}_x(t)$= [0 1] and $i^x(t) > 0$ or $S^{1,2}_x(t)$= [1 1] and $i^x(t) < 0$ or $S^{1,2}_x(t)$= [0 1] and $i^x(t) < 0$. Therefore, the phase current direction and the switching vector determine which transistor or diode is on . The current direction can be found by appling the Heaviside Step Function. Heaviside Step function is

$$H(x) = \begin{cases} 1, & t > 0 \\ 0, & t < 0. \end{cases}$$

Matrices of $A_1(t)$ and $A_2(t)$ are defined as the diagonal matrices such that they split the switching vector $S^{1,2}_{abc}(t)$ into two matrices.

$$\forall t \in \mathbb{R} : A_1(t) = \begin{bmatrix} S_{a1}(t) & 0 & 0 \\ 0 & S_{b1}(t) & 0 \\ 0 & 0 & S_{c1}(t) \end{bmatrix}, A_2(t) = \begin{bmatrix} S_{a2}(t) & 0 & 0 \\ 0 & S_{b2}(t) & 0 \\ 0 & 0 & S_{c2}(t) \end{bmatrix}, \tag{3.53}$$

matrix of $B(t)$ as a column matrix such that

$$\forall t \in \mathbb{R} : B(t) = \begin{bmatrix} H(i^a(t)) \\ H(i^b(t)) \\ H(i^c(t)) \end{bmatrix}, \tag{3.54}$$

matrix of $U(t)$ as a unit column matrix such that

$$\forall t \in \mathbb{R} : U(t) = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}, \tag{3.55}$$

and finally, matrix of $I(t)$ as an identity matrix such that

$$\forall t \in \mathbb{R} : I(t) = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}. \tag{3.56}$$

The instantanous conduction power losses $p^{abc}_{on-3L-ID-NPC-VSI}(\vartheta_J(t), t)$ are given by

$$\begin{aligned} p^{abc}_{on-3L-ID-NPC-VSI}(\vartheta_J(t), t) = [p^{abc}_{on-I}(\vartheta_J(t), t)]^T \\ (\quad \underbrace{2(A_1(t)A_2(t)B(t))}_{S_{x1}(t)=1 \text{ and } S_{x2}(t)=1 \text{ and } i^x(t)>0.} \\ + \quad \underbrace{[I(t) - A_1(t)]A_2(t)B(t)}_{S_{x1}(t)=0 \text{ and } S_{x2}(t)=1 \text{ and } i^x(t)>0.} \\ + \underbrace{[I(t) - A_1(t)][A_2(t)][U(t) - B(t)]}_{S_{x1}(t)=0 \text{ and } S_{x2}(t)=1 \text{ and } i^x(t)<0.} \\ + \underbrace{2([I(t) - A_1(t)][I(t) - A_2(t)][U(t) - B(t)])}_{S_{x1}(t)=0 \text{ and } S_{x2}(t)=0 \text{ and } i^x(t)<0.} \\ + [p^{abc}_{on-D}(\vartheta_J(t), t)]^T \\ (\underbrace{2(A_1(t)A_2(t)[U(t) - B(t)])}_{S_{x1}(t)=1 \text{ and } S_{x2}(t)=1 \text{ and } i^x(t)<0.} \\ + \underbrace{[I(t) - A_1(t)]A_2(t)[U(t) - B(t)]}_{S_{x1}(t)=0 \text{ and } S_{x2}(t)=1 \text{ and } i^x(t)<0.} \\ + \underbrace{2([I(t) - A_1(t)][I(t) - A_2(t)]B(t))}_{S_{x1}(t)=0 \text{ and } S_{x2}(t)=0 \text{ and } i^x(t)>0.} \\ + \quad \underbrace{[I(t) - A_1(t)]A_2(t)B(t)}_{S_{x1}(t)=0 \text{ and } S_{x2}(t)=1 \text{ and } i^x(t)>0.} \quad). \end{aligned} \tag{3.57}$$

where $[p^{abc}_{on-I}(\vartheta_J(t), t)]^T$ $[W]$ and $[p^{abc}_{on-D}(\vartheta_J(t), t)]^T$ $[W]$ are transpose of (3.51) and (3.52) respectively.

The switching power losses can be calculated from Tab. 3.7, (2.44) or (2.31) and (2.16). The turn-on and turn-off switching power losses of the IGBT and the reverse recovery of the

diode are given by

$$p^{abc}_{sw-I-on}(\vartheta_J(t),t)) = \begin{bmatrix} p^{a}_{sw-I-on}(\vartheta_J(t),t)) \\ p^{b}_{sw-I-on}(\vartheta_J(t),t)) \\ p^{c}_{sw-I-on}(\vartheta_J(t),t)) \end{bmatrix}$$
$$= \begin{bmatrix} E_{sw-I-on}(\vartheta_J(t),t)(\frac{|i^a_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}[1+\alpha_{\vartheta-I}(\vartheta_J(t)-\vartheta_J(t_0))]f_s \\ E_{sw-I-on}(\vartheta_J(t),t)(\frac{|i^b_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}[1+\alpha_{\vartheta-I}(\vartheta_J(t)-\vartheta_J(t_0))]f_s \\ E_{sw-I-on}(\vartheta_J(t),t)(\frac{|i^c_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}[1+\alpha_{\vartheta-I}(\vartheta_J(t)-\vartheta_J(t_0))]f_s \end{bmatrix}, \tag{3.58}$$

$$p^{abc}_{sw-I-off}(\vartheta_J(t),t)) = \begin{bmatrix} p^{a}_{sw-I-off}(\vartheta_J(t),t)) \\ p^{b}_{sw-I-off}(\vartheta_J(t),t)) \\ p^{c}_{sw-I-off}(\vartheta_J(t),t)) \end{bmatrix}$$
$$= \begin{bmatrix} E_{sw-I-off}(\vartheta_J(t),t)(\frac{|i^a_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}[1+\alpha_{\vartheta-I}(\vartheta_J(t)-\vartheta_J(t_0))]f_s \\ E_{sw-I-off}(\vartheta_J(t),t)(\frac{|i^b_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}[1+\alpha_{\vartheta-I}(\vartheta_J(t)-\vartheta_J(t_0))]f_s \\ E_{sw-I-off}(\vartheta_J(t),t)(\frac{|i^c_{c-I}(t)|}{I_{C-rated}})(\frac{U_{CE}}{U_{CE-rated}})^{1.49}[1+\alpha_{\vartheta-I}(\vartheta_J(t)-\vartheta_J(t_0))]f_s \end{bmatrix}, \tag{3.59}$$

$$p^{abc}_{rr-D}(\vartheta_J(t),t) = \begin{bmatrix} p^{a}_{rr-D}(\vartheta_J(t),t) \\ p^{b}_{rr-D}(\vartheta_J(t),t) \\ p^{c}_{rr-D}(\vartheta_J(t),t) \end{bmatrix}$$
$$= \begin{bmatrix} \frac{U_R Q_{rr}}{4}\sqrt{(\frac{|i^a_f(t)|}{I_{f-rated}})}(\frac{U_R}{U_{R-rated}})^{0.6}[1+\alpha_{\vartheta-I}(\vartheta_J(t)-\vartheta_J(t_0))]f_s \\ \frac{U_R Q_{rr}}{4}\sqrt{(\frac{|i^b_f(t)|}{I_{f-rated}})}(\frac{U_R}{U_{R-rated}})^{0.6}[1+\alpha_{\vartheta-I}(\vartheta_J(t)-\vartheta_J(t_0))]f_s \\ \frac{U_R Q_{rr}}{4}\sqrt{(\frac{|i^c_f(t)|}{I_{f-rated}})}(\frac{U_R}{U_{R-rated}})^{0.6}[1+\alpha_{\vartheta-I}(\vartheta_J(t)-\vartheta_J(t_0))]f_s \end{bmatrix}. \tag{3.60}$$

As it can be seen, the switching power losses are dependent upon change in the switching vector $S^{1,2}_{abc}(t)$ and the direction of phase current $i^{abc}(t)$. The switching power losses occur when the switching vector $S^{1,2}_{abc}(t)$ goes from one to zero or vice versa. We use the discrete space to find these changes. Therefore, the switching vector, the phase currents and the switching power losses are mapped from continuous space to discrete space such that

$$\forall t \in \mathbb{R} : S_{abc}^{1,2}(t) \rightarrow \forall k \in \mathbb{Z} : S_{abc}^{1,2}[k], \tag{3.61}$$

$$\forall t \in \mathbb{R} : i^{abc}(t) \rightarrow \forall k \in \mathbb{Z} : i^{abc}[k], \tag{3.62}$$

$$\forall t \in \mathbb{R} : p_{rr-D}^{abc}\left(\vartheta_J(t), t\right) \rightarrow \forall k \in \mathbb{Z} : p_{rr-D}^{abc}[\vartheta_J[k], k], \tag{3.63}$$

$$\forall t \in \mathbb{R} : p_{sw-M-on}^{abc}(\vartheta_J(t), t) \rightarrow \forall k \in \mathbb{Z} : p_{sw-M-on}^{abc}[\vartheta_J[k], k], \tag{3.64}$$

$$\forall t \in \mathbb{R} : p_{sw-M-off}^{abc}(\vartheta_J(t), t) \rightarrow \forall k \in \mathbb{Z} : p_{sw-M-off}^{abc}[\vartheta_J[k], k], \tag{3.65}$$

$$\forall t \in \mathbb{R} : p_{sw-I-on}^{abc}(\vartheta_J(t), t) \rightarrow \forall k \in \mathbb{Z} : p_{sw-I-on}^{abc}[\vartheta_J[k], k], \tag{3.66}$$

$$\forall t \in \mathbb{R} : p_{sw-I-off}^{abc}(\vartheta_J(t), t) \rightarrow \forall k \in \mathbb{Z} : p_{sw-I-off}^{abc}[\vartheta_J[k], k]. \tag{3.67}$$

We compare the switching vector of $S_{abc}^{1,2}[k-1]$ with $S_{abc}^{1,2}[k]$ to find when the changes occur at switching vector. Then, the direction of the phase currents $i^{abc}[k]$ are used to find which switches or diodes make the switching power losses. Just like the conduction power losses, some matrices are introduced. The matrices of $A_1[k]$ and $A_2[k]$ are defined as the diagonal matrices such that they split the switching vector $S_{abc}^{1,2}[k]$ into two matrices.

$$\forall k \in \mathbb{Z} : A_1[k] = \begin{bmatrix} S_{a1}[k] & 0 & 0 \\ 0 & S_{b1}[k] & 0 \\ 0 & 0 & S_{c1}[k] \end{bmatrix}, A_2[k] = \begin{bmatrix} S_{a2}[k] & 0 & 0 \\ 0 & S_{b2}[k] & 0 \\ 0 & 0 & S_{c2}[k] \end{bmatrix}, \tag{3.68}$$

matrix of $B[k]$ as a column matrix such that

$$\forall k \in \mathbb{Z} : B[k] = \begin{bmatrix} H(i^a[k]) \\ H(i^b[k]) \\ H(i^c[k]) \end{bmatrix}, \tag{3.69}$$

matrix of $U[k]$ as a unit column matrix such that

$$\forall k \in \mathbb{Z} : U[k] = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}, \tag{3.70}$$

and finally, matrix of $I[k]$ as an identity matrix such that

$$\forall k \in \mathbb{Z} : I[k] = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}. \tag{3.71}$$

The total switching power losses $p^{abc}_{sw-3L-ID-NPC-VSI}[\vartheta_J[k],k]$ are given by

$$
\begin{aligned}
p^{abc}_{sw-3L-ID-NPC-VSI}[\vartheta_J[k],k] = (p^{abc}_{rr-D}[\vartheta_J[k],k])^T \\
&(\underbrace{(I[k-1]-A_1[k-1])A_1[k]A_2[k]B[k]}_{S^{12}_x[k]\text{: } [0\ 1] \longrightarrow [1\ 1] \text{ and } i^x[k]>0.} \\
&+ \underbrace{(I[k]-A_1[k])A_2[k-1](I[k]-A_2[k])B[k]}_{S^{12}_x[k]\text{: } [0\ 1] \longrightarrow [0\ 0] \text{ and } i^x[k]>0.} \\
&+ \underbrace{2((I[k]-A_1[k])(I[k-1]-A_2[k-1])A_2[k]B[k])}_{S^{12}_x[k]\text{: } [0\ 0] \longrightarrow [0\ 1] \text{ and } i^x[k]>0.} \\
&+ \underbrace{2(A_1[k-1](I[k]-A_1[k])A_2[k](U[k]-B[k]))}_{S^{12}_x[k]\text{: } [1\ 1] \longrightarrow [0\ 1] \text{ and } i^x[k]<0.} \\
&+ \underbrace{(I[k-1]-A_1[k-1])A_1[k]A_2[k](U[k]-B[k])}_{S^{12}_x[k]\text{: } [0\ 1] \longrightarrow [1\ 1] \text{ and } i^x[k]<0.} \\
&+ \underbrace{(I[k]-A_1[k])A_2[k-1](I[k]-A_2[k])(U[k]-B[k])}_{S^{12}_x[k]\text{: } [0\ 1] \longrightarrow [0\ 0] \text{ and } i^x[k]<0.} \\
&+ (p^{abc}_{sw-I-on}[\vartheta_J[k],k])^T \\
&(\underbrace{(I[k-1]-A_1[k-1])A_1[k]A_2[k]B[k]}_{S^{12}_x[k]\text{: } [0\ 1] \longrightarrow [1\ 1] \text{ and } i^x[k]>0.} \\
&+ \underbrace{(I[k]-A_1[k])(I[k-1]-A_2[k-1])A_2[k]B[k]}_{S^{12}_x[k]\text{: } [0\ 0] \longrightarrow [0\ 1] \text{ and } i^x[k]>0.} \\
&+ \underbrace{A_1[k-1](I[k]-A_1[k])A_2[k](U[k]-B[k])}_{S^{12}_x[k]\text{: } [1\ 1] \longrightarrow [0\ 1] \text{ and } i^x[k]<0.} \\
&+ \underbrace{(I[k]-A_1[k])A_2[k-1](I[k]-A_2[k])(U[k]-B[k]))}_{S^{12}_x[k]\text{: } [0\ 1] \longrightarrow [0\ 0] \text{ and } i^x[k]<0.} \\
&+ (p^{abc}_{sw-I-off}[\vartheta_J[k],k])^T \\
&(\underbrace{(A_1[k-1])(I[k]-A_1[k])A_2[k]B[k]}_{S^{12}_x[k]\text{: } [1\ 1] \longrightarrow [0\ 1] \text{ and } i^x[k]>0.} \\
&+ \underbrace{(I[k]-A_1[k])A_2[k-1](I[k]-A_2[k])B[k]}_{S^{12}_x[k]\text{: } [0\ 1] \longrightarrow [0\ 0] \text{ and } i^x[k]>0.} \\
&+ \underbrace{(I[k-1]-A_1[k-1])A_1[k]A_2[k])(U[k]-B[k])}_{S^{12}_x[k]\text{: } [0\ 1] \longrightarrow [1\ 1] \text{ and } i^x[k]<0.} \\
&+ \underbrace{(I[k]-A_1[k])(I[k-1]-A_2[k-1])A_2[k])(U[k]-B[k]))}_{S^{12}_x[k]\text{: } [0\ 0] \longrightarrow [0\ 1] \text{ and } i^x[k]<0.}.
\end{aligned}
\tag{3.72}
$$

where $(p^{abc}_{rr-D}[\vartheta_J[k],k])^T$ $[W]$, $(p^{abc}_{sw-I-on}[\vartheta_J[k],k])^T$ $[W]$ and $(p^{abc}_{sw-I-off}[\vartheta_J[k],k])^T$ $[W]$ are transpose of (3.60), (3.58) and (3.59).

Then, a low pass filter is used to reconstruct the continuous switching power losses from the discrete switching power losses.

$$p^{abc}_{sw-3L-ID-NPC-VSI}[\vartheta_J[k],k] \rightarrow p^{abc}_{sw-3L-ID-NPC-VSI}(\vartheta_J(t),t). \tag{3.73}$$

Finally, the total instantaneous power losses for a two-level voltage source inverter is given by

$$p^{abc}_{tot-3l-NPC-VSI}(\vartheta_J(t),t) = p^{abc}_{sw-3L-ID-NPC-VSI}(\vartheta_J(t),t) + p^{abc}_{on-3L-ID-NPC-VSI}(\vartheta_J(t),t). \tag{3.74}$$

If the switches are composed of a MOSFET and an inverse power diode, we should only replace the MOSFET's equations with the IGBT's equations.

Chapter 4

Modulation Techniques for Three-level NPC VSI

In all configurations of VSIs, semiconductor devices should be switched between on and off to control the amplitude and frequency of the output voltage. Several different modulation schemes based on switching frequency have been proposed for three-level NPC VSIs. First group is when modulation schemes work with low switching frequencies. This means that these types of schemes turn the switches on or off for a limited number during one cycle of the output voltages. Selective harmonic elimination (SHE) and the space-vector control (SVC) are modulation schemes that work with low switching frequencies. Second group is when modulation schemes work with mixed switching frequencies. The mixed switching frequencies allow a group of the switches operate at low switching frequencies while other group of the switches to operate at high frequencies. Hybrid modulation scheme is from this type. The last group is when the switches are turned on or off with high switching frequencies. This means that these modulation turn the switches on or off many times in one period of the fundamental output voltage [30]. Very interesting methods at high frequencies are space vector modulation (SVM), phase shifted PWM and level shifted PWM. Fig. 4.1 shows the classification of multilevel modulation schemes. In this chapter, PWM and SVM for a three-level NPC VSIs are defined and explained.

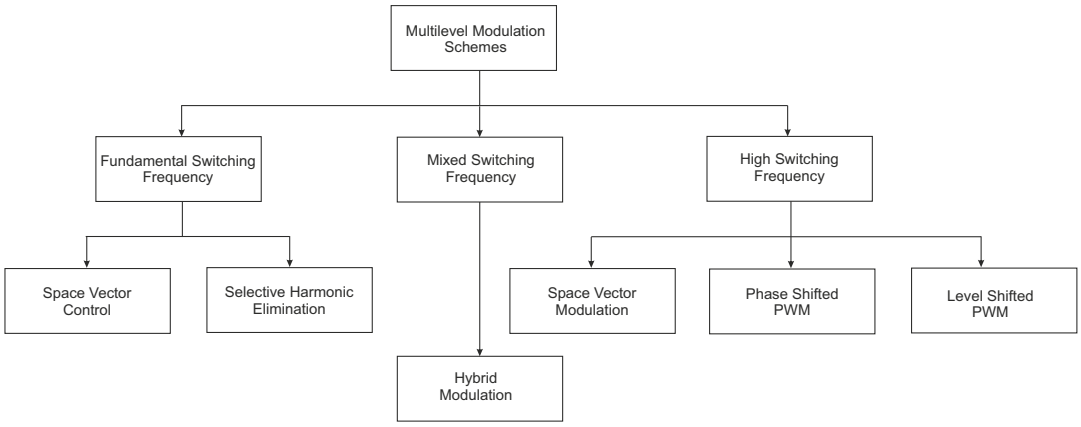


Figure 4.1: Classification of multilevel modulation methods.

4.1 Pulse Width Modulation

As it can be seen from Fig. 4.2, sinusoidal PWM schemes can be divided into two groups at high frequencies. The first group is phase shifted PWM technique. The second one is level shifted PWM or carrier disposition modulation (CD). The level shifted PWM is also categorized into Phase Disposition (PD), Phase Opposite Disposition (POD) and Alternative Phase Opposite Disposition (APOD) [36].

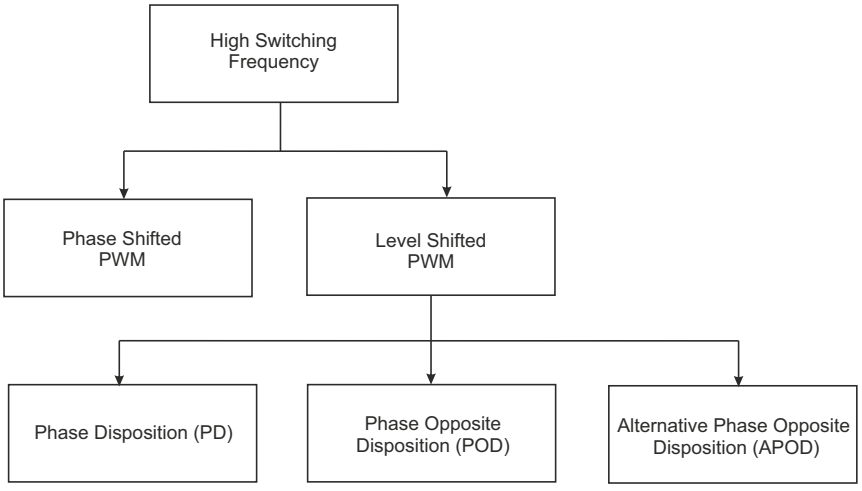


Figure 4.2: Sinusoidal modulation schemes for Multilevel VSIs at high frequency.

In general, pulse width modulation is composed of n reference waveforms and m carrier waveforms where n is determined by the number of phases and m depends on the number of

levels of inverter.
The reference waveforms are usually sinusoidal waveforms with amplitude $\widehat{U}_r$ $[V]$ and frequency f_r $[Hz]$. In three-phase system, three reference sinusoidal waveforms are used that are shifted of 120 electrical degrees from each other.

$$u_{ref}^{abc}(t) = \begin{bmatrix} u_{ref}^{a}(t) \\ u_{ref}^{b}(t) \\ u_{ref}^{c}(t) \end{bmatrix} = \widehat{U}_r \begin{bmatrix} \cos(2\pi f_r t + \varphi_r) \\ \cos(2\pi f_r t + \varphi_r - \frac{2\pi}{3}) \\ \cos(2\pi f_r t + \varphi_r - \frac{4\pi}{3}) \end{bmatrix}. \tag{4.1}$$

where φ_r $[rad]$ is initial phase shift of reference waveform.
Moreover, one reference sinusoidal waveform can be used, afterwards this is shifted two times with an appropriate electrical shift.
Any types of carrier waveforms can be used in PWM, like saw-tooth carrier, inverted saw-tooth carrier, triangle carrier ,etc (see Fig. 4.3).

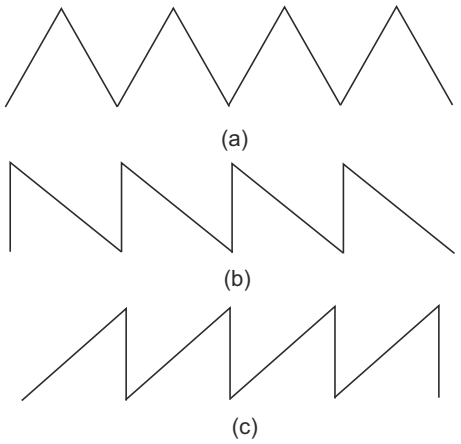


Figure 4.3: (a) Triangle carrier (b) Inverted sawtooth carrier (c) Sawtooth carrier.

However, certain harmonics are eliminated when triangle carrier waveforms are used with the reference sinusoidal waveforms. Therefore, triangle carrier waveforms are used for inverters [37]. For a three-level NPC inverter, two triangle carrier waveforms are required. All carriers have the same peak-to-peak amplitude $\widehat{U}_c$ $[V]$ and frequency f_c $[Hz]$. (4.2) gives the Fourier series of triangle carrier waveform shown in Fig. 4.4.

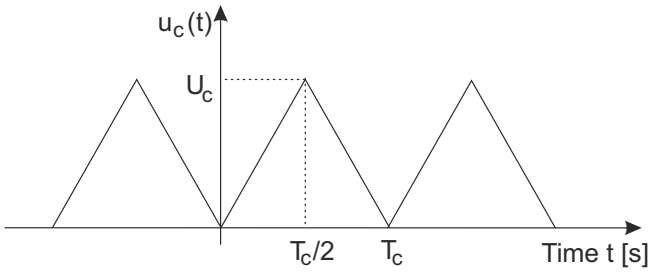


Figure 4.4: Triangle waveforms.

$$u_c(t) = \frac{\widehat{U}_c}{2} - \frac{4\widehat{U}_c}{\pi^2}\sum_{i=1}^{\infty}\frac{1}{(2i-1)^2}\cos\frac{2(2i-1)\pi t}{T_c}. \tag{4.2}$$

where T_c $[s]$ is the period of the triangle carrier waveform.

Different types of modulation schemes are obtained by changing the place of triangle carrier waveforms. The zero reference sinusoidal waveforms are placed in the middle of the carrier waveforms. At every instant, carrier waveforms are compared with the references waveforms. These can be mathematically described by using the Heaviside step function .

$$H(x) = \begin{cases} 1, & \text{if } x > 0 \\ 0, & \text{if } x < 0. \end{cases}$$

Thus, the states of the switching vector for PWM are given by

$$S_{abc}^{1,2}(t) = \begin{bmatrix} S_{a1}(t) & S_{a2}(t) \\ S_{b1}(t) & S_{b2}(t) \\ S_{c1}(t) & S_{c2}(t) \end{bmatrix} = \begin{bmatrix} H(u_{ref}^a(t) - u_{c1}(t)) & H(u_{ref}^a(t) - u_{c2}(t)) \\ H(u_{ref}^b(t) - u_{c1}(t)) & H(u_{ref}^b(t) - u_{c2}(t)) \\ H(u_{ref}^c(t) - u_{c1}(t)) & H(u_{ref}^c(t) - u_{c2}(t)) \end{bmatrix}. \tag{4.3}$$

The output voltage and the content of harmonics depend on the amplitudes and frequencies of carrier and reference waveforms. Therefore, two indices are introduced to measure the ability of a PWM schemes to deliver AC power. The amplitude ratio r_A is defined as the ratio of the reference amplitude $\widehat{U}_r$ to the amplitude of peak-to-peak carrier band $\widehat{U}_c$

$$r_A = \frac{\widehat{U}_r}{\widehat{U}_c}. \tag{4.4}$$

Moreover, frequency ratio r_f is given by

$$r_f = \frac{f_c}{f_r}. \tag{4.5}$$

Other important thing in the sinusoidal PWM is total harmonic distortion of voltage (THD_v) and it is defined by

$$THD_v = \sqrt{\sum_{n=2}^{\infty}(\frac{V_n}{V_1})^2}. \tag{4.6}$$

THD_v is the summation of all harmonic of the voltage waveforms compared against the fundamental waveform of the voltage.

In this section, Phase Shifted, Phase Disposition (PD), Phase Opposite Disposition (POD) and Alternative Phase Opposite Disposition (APOD) modulation schemes are analyzed.

4.1.1 Phase Shifted PWM

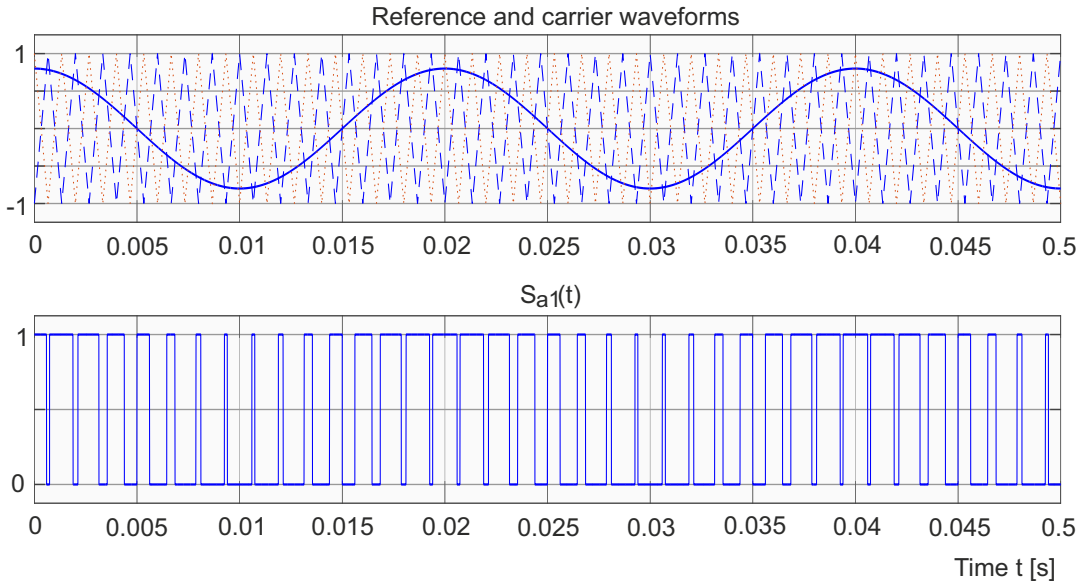
In three-level NPC VSI, two carrier signals are required in phase shifted pwm. Two triangular carriers have the same peak to peak amplitude $\widehat{U}_c$ $[V]$ and same frequency f_c $[Hz]$, but the carrier waveforms are shifted from each other. For three-level NPC VSI, the carriers are phase shifted with an angle of π $[rad]$. In phase shifted PWM, the amplitude ratio r_A and frequency ratio r_f are

$$r_A = \frac{\widehat{U}_r}{\widehat{U}_c}. \tag{4.7}$$

Moreover,

$$r_f = \frac{f_c}{f_r}. \tag{4.8}$$

Fig. 4.5 shows sinusoidal reference waveform and two triangular waveforms, the switching waveforms and the line-to-live voltage in the three-level NPC VSI respectively. Fig. 4.6 illustrates THD_v and line-to-line voltage in three-level NPC VSI.



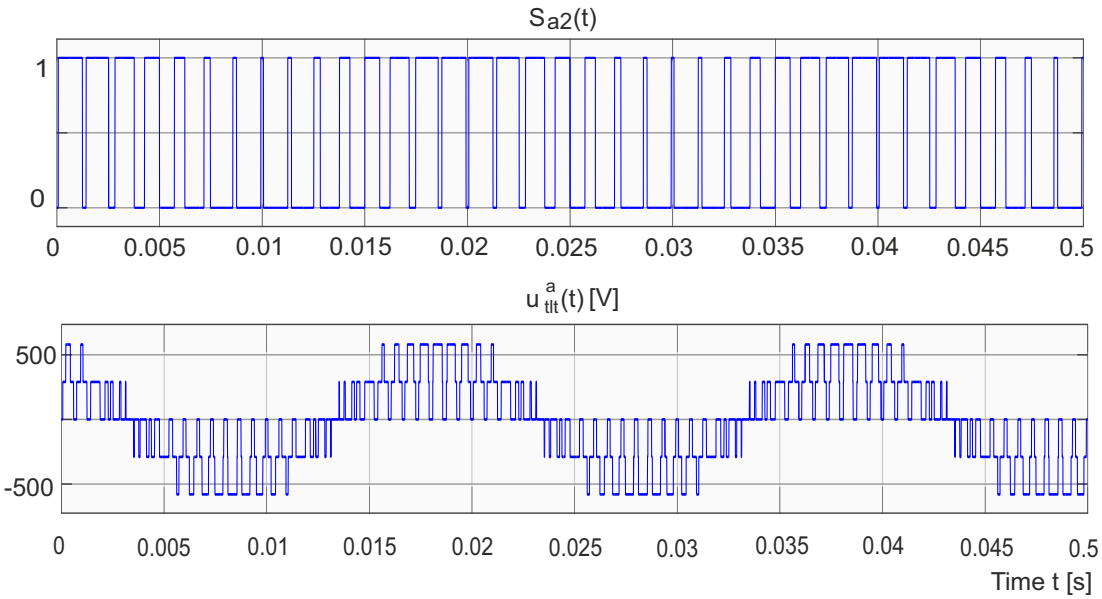


Figure 4.5: Simulated waveforms in the three-level NPC VSI using phase shifted PWM (f_r = 50 $[Hz]$, f_c = 750 $[Hz]$, r_A = 0.8, and r_f = 15).

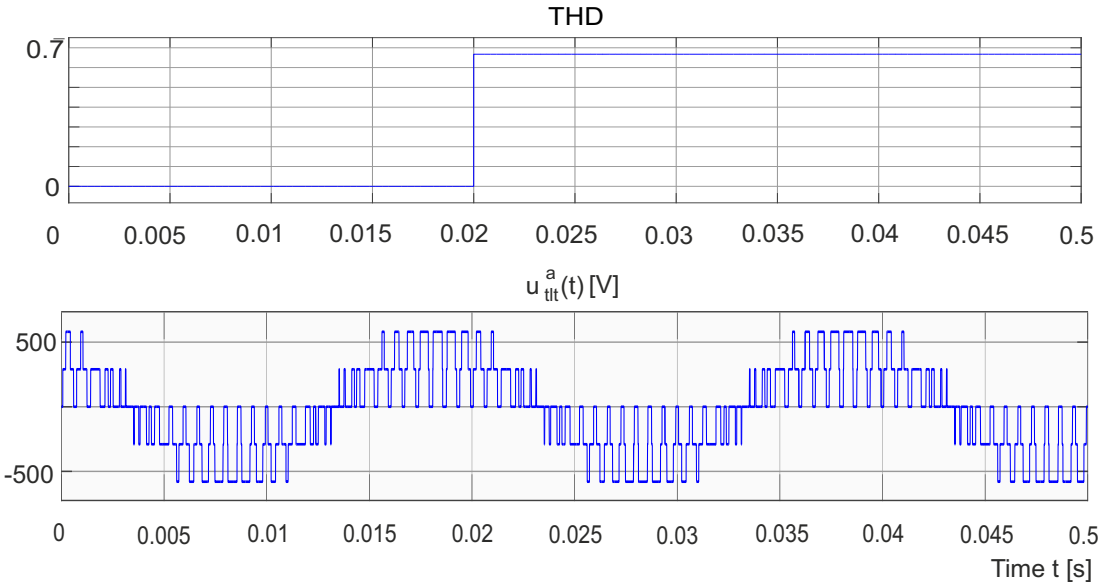


Figure 4.6: Line-to-line voltage total harmonic distortion (THD_v = 67%) and line to line voltage in the three-level NPC VSI using phase shifted PWM (f_r = 50 $[Hz]$, f_c = 750 $[Hz]$, r_A = 0.8, and r_f = 15).

4.1.2 Phase Disposition PWM

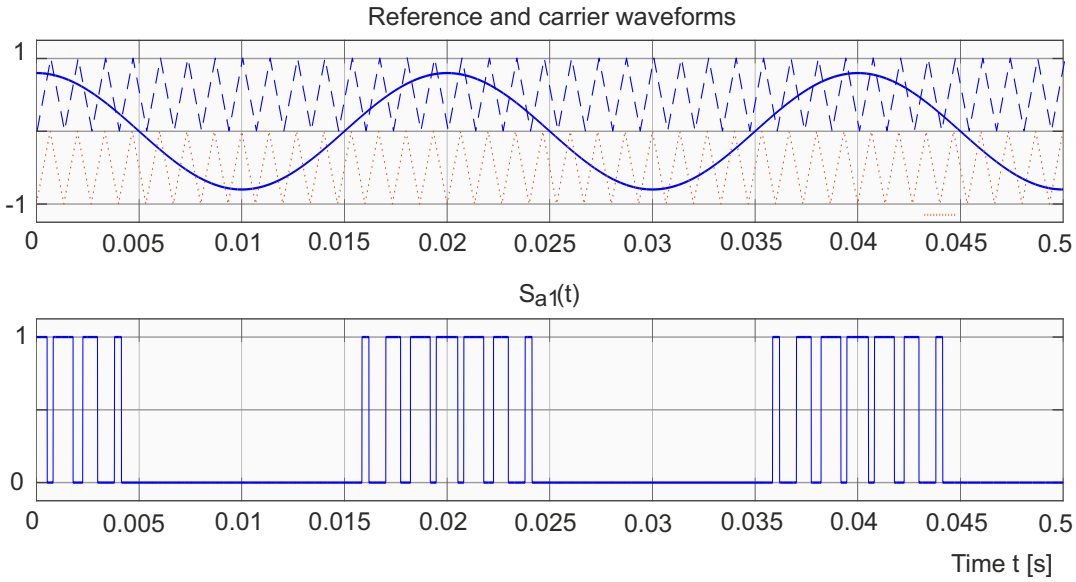
In three-level NPC VSI, two triangular carrier waveforms are in phase with same amplitude $\widehat{U}_c$ $[V]$ and frequency f_c $[Hz]$. The phase disposition (PD) technique has only odd harmonics for odd r_f and yields odd and even harmonics for even r_f. In phase disposition PWM, the amplitude ratio r_A and frequency ratio r_f are

$$r_A = \frac{\widehat{U}_r}{2\widehat{U}_c}. \tag{4.9}$$

Moreover,

$$r_f = \frac{f_c}{f_r}. \tag{4.10}$$

Fig. 4.7 shows sinusoidal reference waveform and two triangular waveforms, the switching waveforms and the line-to-live voltage in the three-level NPC VSI respectively. Fig. 4.8 illustrates THD_v and line-to-line voltage in three-level NPC VSI.



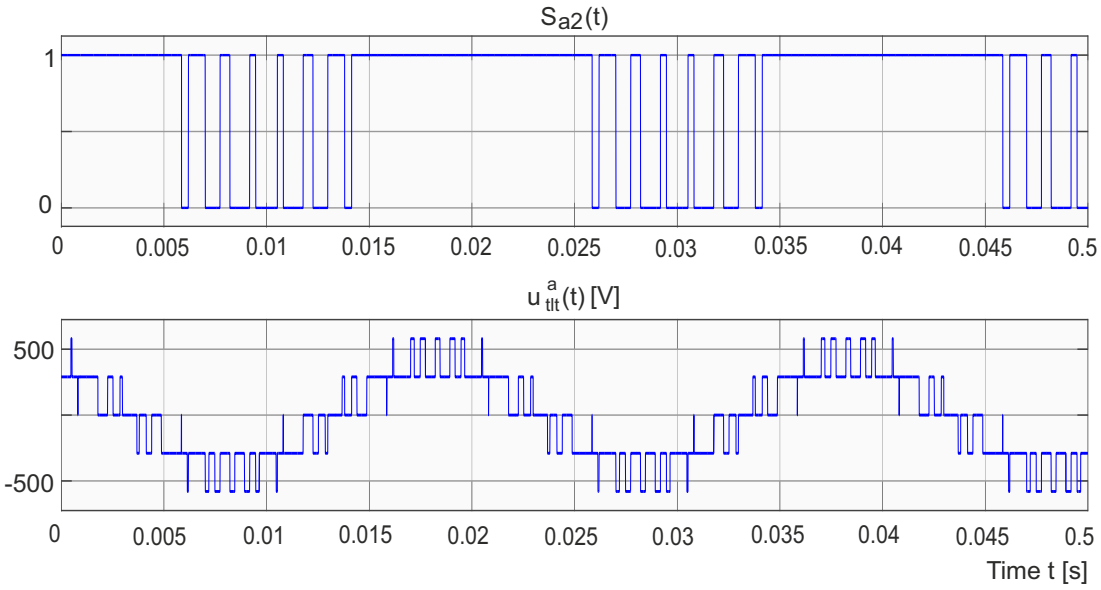


Figure 4.7: Simulated waveforms in the three-level NPC VSI using phase disposition PWM ($f_r = 50$ $[Hz]$, $f_c = 750$ $[Hz]$, $r_A = 0.8$, and $r_f = 15$).

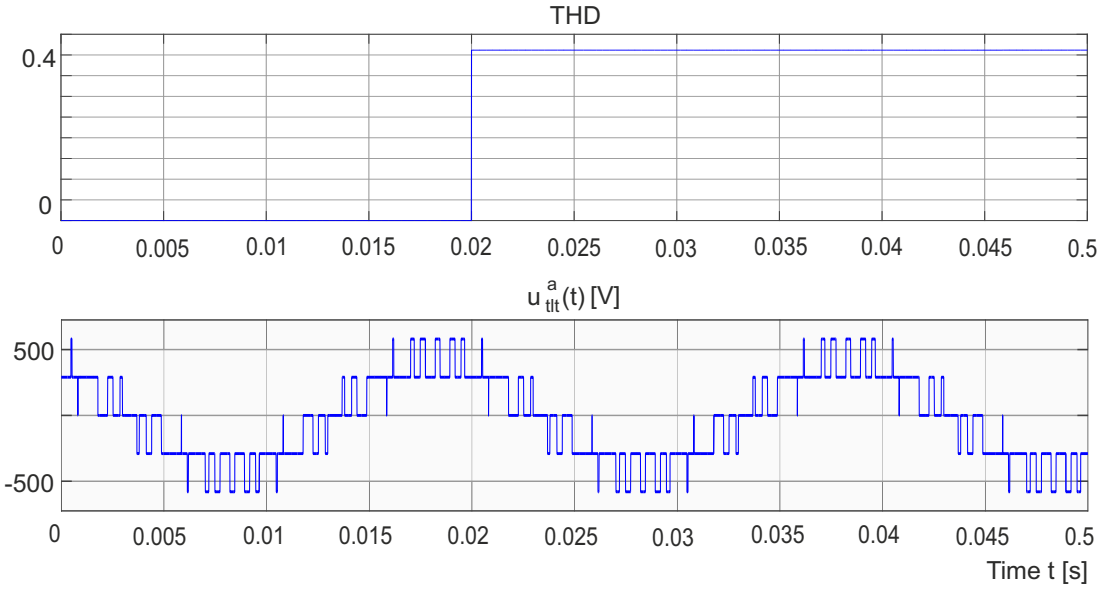


Figure 4.8: Line-to-line voltage total harmonic distortion ($THD_v = 41\%$) and line to line voltage in the three-level NPC VSI using phase disposition PWM ($f_r = 50$ $[Hz]$, $f_c = 750$ $[Hz]$, $r_A = 0.8$, and $r_f = 15$).

4.1.3 Phase Opposite Disposition PWM

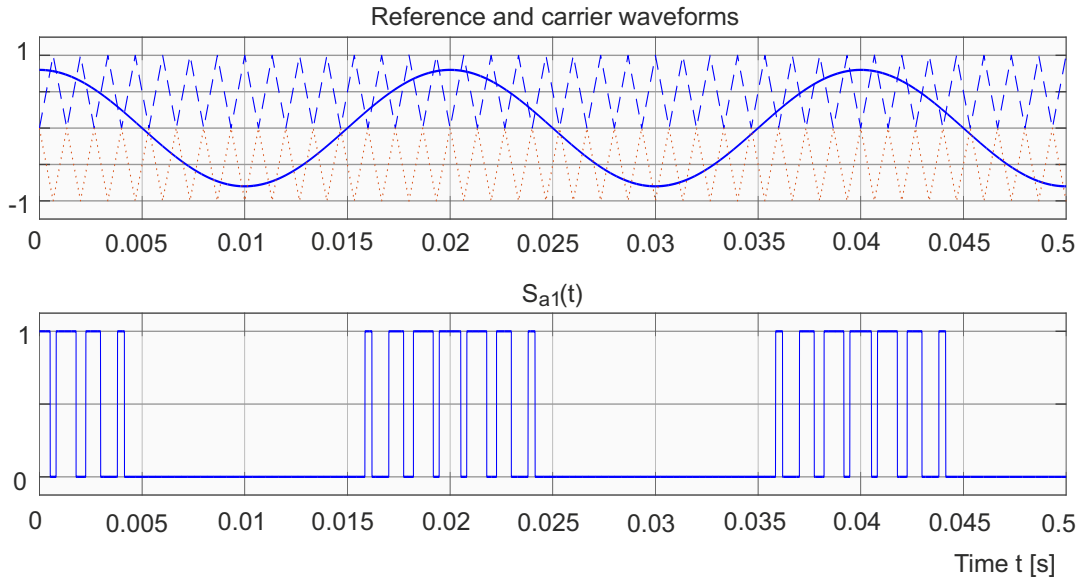
In the phase opposite disposition (POD) modulation the carrier waveforms above or below the zero reference value have the same amplitude $\widehat{U}_c$ $[V]$ and frequency f_c $[Hz]$. However,the carriers are phase shifted with an angle of π $[rad]$. The phase opposite disposition technique has odd symmetry for odd r_f and quarter wave symmetry for even r_f. In phase opposite disposition PWM, the amplitude ratio r_A and frequency ratio r_f are

$$r_A = \frac{\widehat{U}_r}{2\widehat{U}_c}. \tag{4.11}$$

Moreover,

$$r_f = \frac{f_c}{f_r}. \tag{4.12}$$

Fig. 4.9 shows sinusoidal reference waveform and two triangular waveforms, the switching waveforms and the line-to-live voltage in the three-level NPC VSI respectively. Fig. 4.10 illustrates THD_v and line-to-line voltage in three-level NPC VSI.



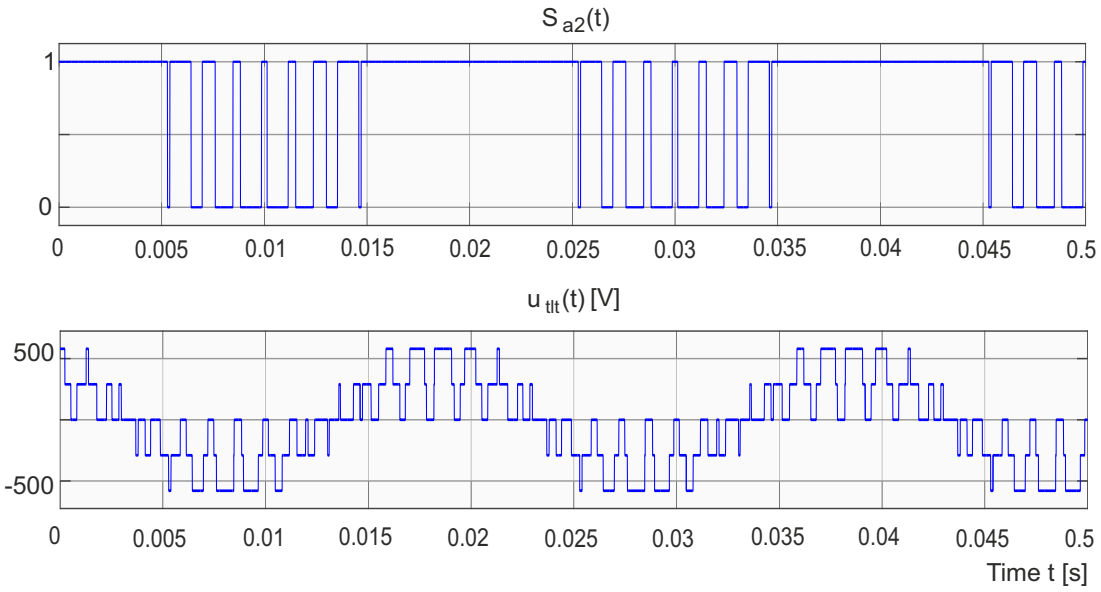


Figure 4.9: Simulated waveforms in the three-level NPC VSI using phase opposite disposition PWM ($f_r = 50$ $[Hz]$, $f_c = 750$ $[Hz]$, $r_A = 0.8$, and $r_f = 15$).

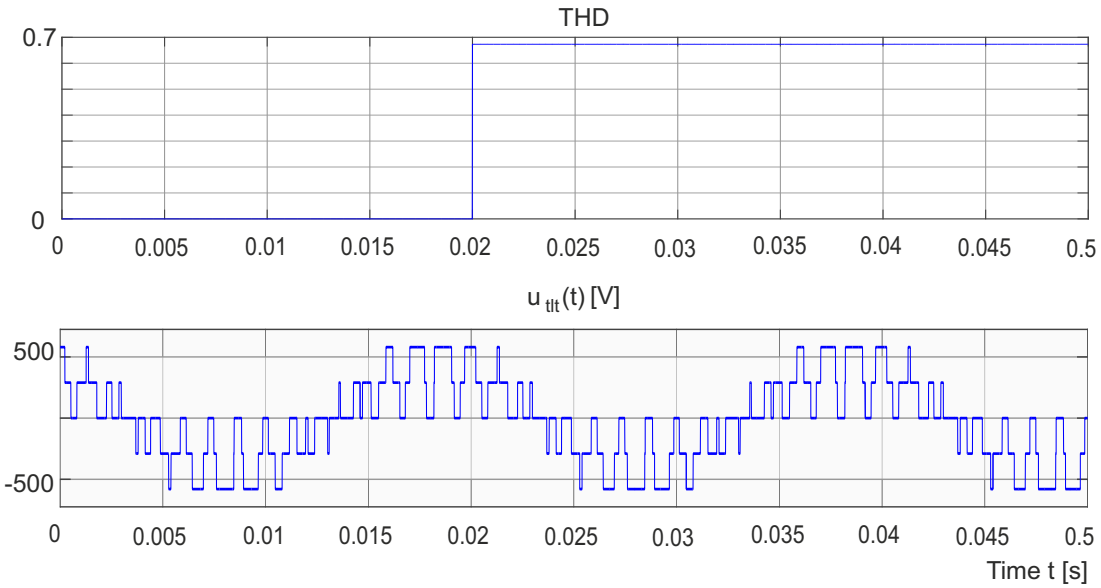


Figure 4.10: Line-to-line voltage total harmonic distortion ($THD_v = 67\%$) and line to line voltage in the three-level NPC VSI using phase opposite disposition PWM ($f_r = 50$ $[Hz]$, $f_c = 750$ $[Hz]$, $r_A = 0.8$, and $r_f = 15$).

4.1.4 Alternative Phase Opposite Disposition PWM

In Alternative phase opposite disposition (APOD) PWM, all triangular carrier waveforms are phase-displaced by π $[rad]$ alternatively. AOPD PWM is just like POD PWM in the three-level NPC VSI, because we have two carrier waveforms. Therefore, all results for POD PWM are valid also for APOD in the three-level NPC VSI.

4.2 Space Vector Modulation

A space vector PWM (SVM) method for a three-level NPC inverter is proposed in this section. As the section (3.2.2) shows, each leg of three-level NPC VSI can be modeled into a three-pole switch. Therefore, each leg has three states resulting a total of 27 possible of switching states. If we assume (3.43), the relationship between switching states and the space vectors can be derived. Therefore, (3.43) means if we have the phase voltage of two phases, we can compute the phase voltage of third phase. Thus, it is possible to apply Clarke-transformation to transform the three phases system to an equivalent two phases system [38].

$$\begin{bmatrix} u_\alpha(t) \\ u_\beta(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} u^a(t) \\ u^b(t) \\ u^c(t) \end{bmatrix}. \tag{4.13}$$

where $u_\alpha(t)$ $[V]$ and $u_\beta(t)$ $[V]$ are the instantaneous voltage vector in the α-β plane.

By inserting (3.47) into (4.13)

$$\begin{bmatrix} u_\alpha(t) \\ u_\beta(t) \end{bmatrix} = \frac{U_{dc}}{9} \begin{bmatrix} 3 & -1 & -1 \\ 0 & \frac{3\sqrt{3}}{2} & -\frac{3\sqrt{3}}{2} \end{bmatrix} \underbrace{\left[\begin{bmatrix} S_a^U(t) \\ S_b^U(t) \\ S_c^U(t) \end{bmatrix} - \begin{bmatrix} S_a^L(t) \\ S_b^L(t) \\ S_c^L(t) \end{bmatrix} \right]}_{[S_a^{U-L}(t)\ S_b^{U-L}(t)\ S_c^{U-L}(t)]^T}. \tag{4.14}$$

A space vector $\overrightarrow{u}(t)$ is expressed in terms of the two-phase voltages in the α-β coordinates such that

$$\overrightarrow{u}(t) = u_\alpha(t) + j u_\beta(t). \tag{4.15}$$

or

$$\overrightarrow{u}(t) = |\overrightarrow{u}(t)| e^{j\theta(t)}. \tag{4.16}$$

where

$$|\overrightarrow{u}(t)| = \sqrt{(u_\alpha(t))^2 + (u_\beta(t))^2}, \theta(t) = \arctan(\frac{u_\beta(t)}{u_\alpha(t)}). \tag{4.17}$$

All twenty seven active vectors can be derived by inserting value of the switching vectors. Tab. 4.1 summarizes the relationship between the space vectors and the switching vectors.

Space Vector $\overrightarrow{u}(t)$	Switching Vector $[S_a^{U-L}(t)\ S_b^{U-L}(t)\ S_c^{U-L}(t)]^T$	$\lvert\overrightarrow{u}(t)\rvert$	$\angle\overrightarrow{u}(t)$
$\overrightarrow{U}_0$	[1 1 1], [0 0 0], [-1 -1 -1]	0	-
$\overrightarrow{U}_1$	[1 0 0], [0 -1 -1]	$\frac{U_{dc}}{3}$	0
$\overrightarrow{U}_2$	[1 1 0], [0 0 -1]	$\frac{U_{dc}}{3}$	$\frac{\pi}{3}$
$\overrightarrow{U}_3$	[0 1 0], [-1 0 -1]	$\frac{U_{dc}}{3}$	$\frac{2\pi}{3}$
$\overrightarrow{U}_4$	[0 1 1], [-1 0 0]	$\frac{U_{dc}}{3}$	π
$\overrightarrow{U}_5$	[0 0 1], [-1 -1 0]	$\frac{U_{dc}}{3}$	$\frac{4\pi}{3}$
$\overrightarrow{U}_6$	[1 0 1], [0 -1 0]	$\frac{U_{dc}}{3}$	$\frac{5\pi}{3}$
$\overrightarrow{U}_7$	[1 0 -1]	$\frac{\sqrt{3}U_{dc}}{3}$	$\frac{\pi}{6}$
$\overrightarrow{U}_8$	[0 1 -1]	$\frac{\sqrt{3}U_{dc}}{3}$	$\frac{\pi}{2}$
$\overrightarrow{U}_9$	[-1 1 0]	$\frac{\sqrt{3}U_{dc}}{3}$	$\frac{5\pi}{6}$
$\overrightarrow{U}_{10}$	[-1 0 1]	$\frac{\sqrt{3}U_{dc}}{3}$	$\frac{7\pi}{6}$
$\overrightarrow{U}_{11}$	[0 -1 1]	$\frac{\sqrt{3}U_{dc}}{3}$	$\frac{3\pi}{2}$
$\overrightarrow{U}_{12}$	[1 -1 0]	$\frac{\sqrt{3}U_{dc}}{3}$	$\frac{11\pi}{6}$
$\overrightarrow{U}_{13}$	[1 -1 -1]	$\frac{2U_{dc}}{3}$	0
$\overrightarrow{U}_{14}$	[1 1 -1]	$\frac{2U_{dc}}{3}$	$\frac{\pi}{3}$
$\overrightarrow{U}_{15}$	[-1 1 -1]	$\frac{2U_{dc}}{3}$	$\frac{2\pi}{3}$
$\overrightarrow{U}_{16}$	[-1 1 1]	$\frac{2U_{dc}}{3}$	π
$\overrightarrow{U}_{17}$	[-1 -1 1]	$\frac{2U_{dc}}{3}$	$\frac{4\pi}{3}$
$\overrightarrow{U}_{18}$	[1 -1 1]	$\frac{2U_{dc}}{3}$	$\frac{5\pi}{3}$

Table 4.1: Switching Vectors and Voltage vectors.

The space vector $\overrightarrow{U}_0$ to $\overrightarrow{U}_{18}$ in Fig. 4.11 are stationary vectors, because they do not move in space. The reference vector $\overrightarrow{u}_{ref}(t)$ rotates in the α-β plane at an angular velocity

$$\omega = \frac{\theta(t)}{t} = 2\pi f_1. \tag{4.18}$$

where f_1 $[Hz]$ is the fundamental frequency of the output voltage of three-level NPC VSI.

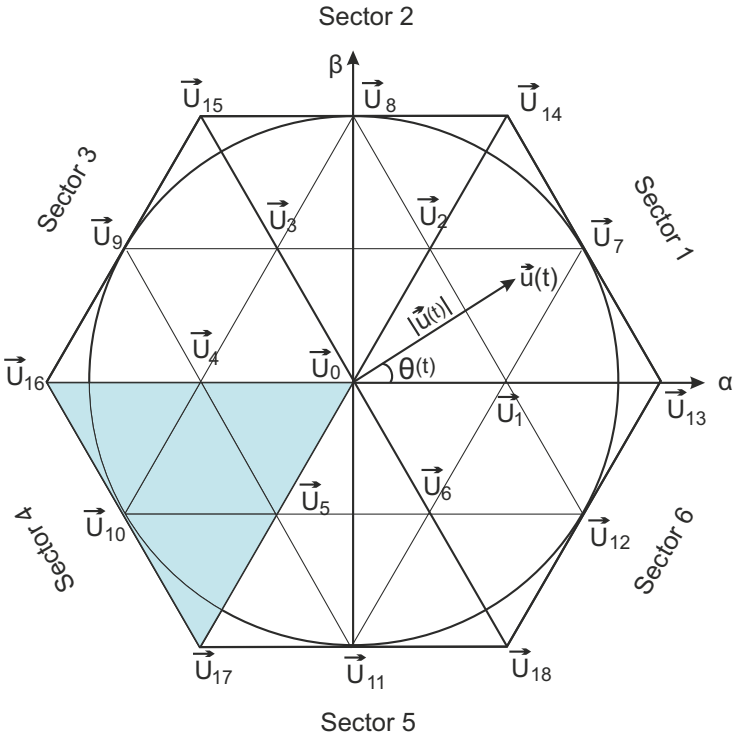


Figure 4.11: Space vector diagram of the three-level NPC inverter.

Space vector PWM for three-level NPC VSI is implemented by considering the following steps [39]

1. Determining the sector.
2. Find the region in the sector.
3. Calculate the switching times (T_a, T_b and T_c).
4. Design the switching sequences.

4.2.1 Determining the Sector

$\angle\overrightarrow{u}(t)$ or $\theta(t)$ $[rad]$ is obtained by (4.17). Then by using $\theta(t)$, the sector where $\overrightarrow{u}(t)$ lies can be obtained. Tab. 4.2 shows the relationship between $\theta(t)$ and the sectors.

$\theta(t)$ $[rad]$	$\overrightarrow{u}(t)$ location
$0 < \theta(t) < \frac{\pi}{3}$	Sector 1
$\frac{\pi}{3} < \theta(t) < \frac{2\pi}{3}$	Sector 2
$\frac{2\pi}{3} < \theta(t) < \pi$	Sector 3
$\pi < \theta(t) < \frac{4\pi}{3}$	Sector 4
$\frac{4\pi}{3} < \theta(t) < \frac{5\pi}{3}$	Sector 5
$\frac{5\pi}{3} < \theta(t) < 2\pi$	Sector 6

Table 4.2: Relationship among location of $\overrightarrow{u}(t)$ and the sectors.

4.2.2 Find the Region in the Sector

If we assume that $\overrightarrow{u}(t)$ is in the sector 1, the relationship among $\overrightarrow{u}(t)$ and regions are (see Fig. 4.12) [40].

$$\overrightarrow{u}_1(t) = \overrightarrow{u}(t)\cos(\theta(t)) - (\frac{\overrightarrow{u}(t)\sin(\theta(t))}{sin(\frac{\pi}{3})})\cos(\frac{\pi}{3}), \tag{4.19}$$

$$\overrightarrow{u}_2(t) = \frac{\overrightarrow{u}(t)\sin(\theta(t))}{sin(\frac{\pi}{3})}. \tag{4.20}$$

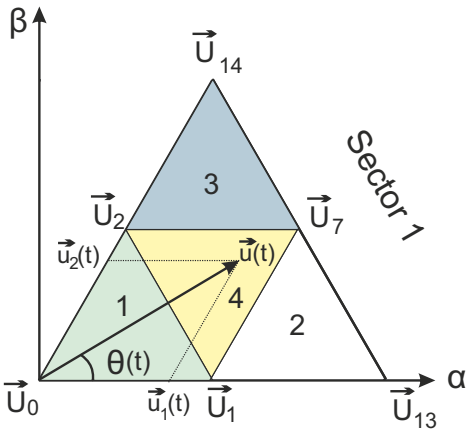


Figure 4.12: Regions of the sector 1.

where $\overrightarrow{u}_1(t)$ and $\overrightarrow{u}_2(t)$ are projections of $\overrightarrow{u}(t)$ on the stationary vectors of $\overrightarrow{U}_{13}$ and $\overrightarrow{U}_{14}$ respectively. Therefore, the relationship among $\overrightarrow{u}(t)$ and the regions are

$$\text{Location of } \overrightarrow{u}(t) = \begin{cases} Region1, & \text{if } (\overrightarrow{u}_1(t) \text{ and } \overrightarrow{u}_2(t) \text{ and } (\overrightarrow{u}_1(t) + \overrightarrow{u}_2(t))) < \frac{U_{dc}}{3} \\ Region2, & \text{if } \overrightarrow{u}_1(t) > \frac{U_{dc}}{3} \\ Region3, & \text{if } \overrightarrow{u}_2(t) > \frac{U_{dc}}{3} \\ Region4, & \text{if } (\overrightarrow{u}_1(t) \text{ and } \overrightarrow{u}_2(t)) < \frac{U_{dc}}{3} \text{ and } (\overrightarrow{u}_1(t) + \overrightarrow{u}_2(t)) > \frac{U_{dc}}{3}. \end{cases}$$

In general, the relationship among the location of $\overrightarrow{u}(t)$ and all regions of each sector are given by

$$\overrightarrow{u}_1(t) = \overrightarrow{u}(t)\cos(\theta(t) - (k-1)\frac{\pi}{3}) - (\frac{\overrightarrow{u}(t)\sin(\theta(t) - (k-1)\frac{\pi}{3})}{sin(\frac{\pi}{3})})\cos(\frac{\pi}{3}), \tag{4.21}$$

$$\overrightarrow{u}_2(t) = \frac{\overrightarrow{u}(t)\sin(\theta(t) - (k-1)\frac{\pi}{3})}{sin(\frac{\pi}{3})}. \tag{4.22}$$

where $k \in \{1, 2, 3, 4, 5, 6\}$ is the sector number.
Fig. 4.13 shows the regions of each sector.

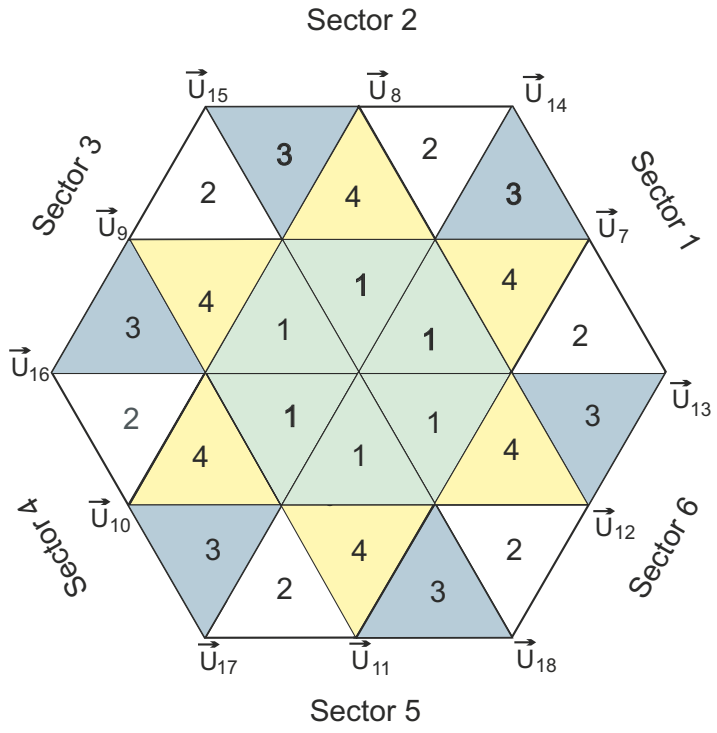


Figure 4.13: Regions of each sector.

4.2.3 Calculate the Switching Times (T_a, T_b and T_c)

$\overrightarrow{u}(t)$ can be made by three adjacent stationary vectors among $\overrightarrow{U}_0$ to $\overrightarrow{U}_{18}$. The switching times calculation are obtained based on volt-second balancing principle [29]. This means the product of $\overrightarrow{u}(t)$ and switching period T_s is equal to the sum of the stationary vectors multiplied by the time interval. If we assume that the switching period T_s is sufficiently small, $\overrightarrow{u}(t)$ can be considered constant during T_s. Under this assumption, $\overrightarrow{u}(t)$ can be approximated by three adjacent stationary vectors (three adjacent stationary vectors are found by the previous steps). For example, if we assume that $\overrightarrow{u}(t)$ is in the region four from sector one (see Fig. 4.12), three adjacent stationary vectors are $\overrightarrow{U}_1$, $\overrightarrow{U}_2$ and $\overrightarrow{U}_7$. The volt-second principle says

$$\overrightarrow{u}(t)T_s = \overrightarrow{U}_1 T_a + \overrightarrow{U}_2 T_b + \overrightarrow{U}_7 T_c, \tag{4.23}$$

$$T_s = T_a + T_b + T_c. \tag{4.24}$$

where T_a $[s]$, T_b $[s]$ and T_c $[s]$ are the switching times for $\overrightarrow{U}_1$, $\overrightarrow{U}_2$ and $\overrightarrow{U}_7$, respectively. If (4.23), (4.16) and Tab. 4.1 are used, relationship among $\overrightarrow{u}(t)$ and the stationary vectors $\overrightarrow{U}_1$, $\overrightarrow{U}_2$ and $\overrightarrow{U}_7$ is

$$|\overrightarrow{u}(t)|e^{j\theta(t)}T_s = \frac{U_{dc}}{3}T_a + \frac{U_{dc}}{3}e^{j\frac{\pi}{3}}T_b + \frac{\sqrt{3}U_{dc}}{3}e^{j\frac{\pi}{6}}T_c. \tag{4.25}$$

If we split (4.25) into the real and imaginary parts

$$Re: 3\frac{|\overrightarrow{u}(t)|}{U_{dc}}\cos(\theta(t))T_s = T_a + \frac{3}{2}T_b + \frac{1}{2}T_c, \tag{4.26}$$

$$Im: 3\frac{|\overrightarrow{u}(t)|}{U_{dc}}\sin(\theta(t))T_s = \frac{3}{2}T_b + \frac{\sqrt{3}}{2}T_c. \tag{4.27}$$

(4.26) and (4.27) together with $T_s = T_a + T_b + T_c$ are three equations for three variables. Therefore, the switching times for the region four from the sector one are

$$T_a = T_s(1 - 2\sqrt{3}\frac{|\overrightarrow{u}(t)|}{U_{dc}}\sin(\theta(t))), \tag{4.28}$$

$$T_b = T_s(2\sqrt{3}\frac{|\overrightarrow{u}(t)|}{U_{dc}}\sin(\frac{\pi}{3} + \theta(t))), \tag{4.29}$$

$$T_c = T_s(1 - 2\sqrt{3}\frac{|\overrightarrow{u}(t)|}{U_{dc}}\sin(\frac{\pi}{3} - \theta(t))), \tag{4.30}$$

If we define x_a, x_b and x_c , we can extend the switching times for all sectors.

$$x_{ak} = \sqrt{3}\frac{|\overrightarrow{u}(t)|}{U_{dc}}\sin(\theta(t) - (k-1)\frac{\pi}{3}), \tag{4.31}$$

$$x_{bk} = \sqrt{3}\frac{|\overrightarrow{u}(t)|}{U_{dc}}\sin(\frac{\pi}{3} + \theta(t) - (k-1)\frac{\pi}{3}), \tag{4.32}$$

$$x_{ck} = \sqrt{3}\frac{|\overrightarrow{u}(t)|}{U_{dc}}\sin(\frac{\pi}{3} - \theta(t) - (k-1)\frac{\pi}{3}). \tag{4.33}$$

where $k \in \{1, 2, 3, 4, 5, 6\}$ is the sector number.
Tab. 4.3 shows the switching times for each sector.

Sector	Region	T_a [s]		T_b [s]		T_c [s]	
k	1	$\overrightarrow{U}_k$	T_s (2 x_{ck})	$\overrightarrow{U}_0$	T_s (1- 2 x_{bk})	$\overrightarrow{U}_{k+1}$	T_s (2 x_{ak})
k	2	$\overrightarrow{U}_k$	T_s (2 - 2 x_{bk})	$\overrightarrow{U}_{6+k}$	T_s (2 x_{ak})	$\overrightarrow{U}_{12+k}$	T_s (2 x_{ck} -1)
k	3	$\overrightarrow{U}_{13+k}$	T_s (2 x_{ak} -1)	$\overrightarrow{U}_{6+k}$	T_s (2 x_{ck})	$\overrightarrow{U}_{k+1}$	T_s (2- 2 x_{bk})
k	4	$\overrightarrow{U}_k$	T_s (1- 2 x_{ak})	$\overrightarrow{U}_{6+k}$	T_s (2 x_{bk} -1)	$\overrightarrow{U}_{k+1}$	T_s (1- 2 x_{ck})

Table 4.3: Switching times for each sector.

where $k \in \{1, 2, 3, 4, 5, 6\}$ is the sector number. Note that for the sector six, $\overrightarrow{U}_7$ and $\overrightarrow{U}_{19}$ are equal to $\overrightarrow{U}_1$ and $\overrightarrow{U}_{13}$ respectively.

4.2.4 Design the Switching Sequences

The next step is to design the switching sequences. In practice, the switching sequences for a $\overrightarrow{u}(t)$ can be designed in many ways, but it should meet the following requirements:
(R_1). The neutral point voltage $u_M(t)$=$U_{C2}(t)$ is defined as the voltage of capacitor C_2 (see Fig. 3.12). In practice, $u_M(t)$ changes with the switching state of the NPC VSI. This means that $u_M(t)$ changes with $\overrightarrow{U}_1$ to $\overrightarrow{U}_6$. If the upper switches ($S_a^U(t)$ and/or $S_b^U(t)$ and/or $S_c^U(t)$) produce the stationary vector $\overrightarrow{U}_1$ to $\overrightarrow{U}_6$, the neutral point voltage $u_M(t)$ increases. On contrary, if the lower switches ($S_a^L(t)$ and/or $S_b^L(t)$ and/or $S_c^L(t)$) produce $\overrightarrow{U}_1$ to $\overrightarrow{U}_6$, the neutral point voltage $u_M(t)$ decreases. Therefore, the effect of switching state on $u_M(t)$ should be minimized [41].
(R_2). Moving from one region or sector to the next one should be done by minimum number of switchings [29].
(R_3). Changing in one switching state to the next should be done by only two switches in the same inverter leg.
(R_4). The line-to-line output voltage waveform should be quarter-wave symmetry to eliminate even-order harmonics (minimum THD).

(R_5). Try to minimize the switching losses of inverter.
Assuming that the fundamental harmonics of the phase voltages $u_1^{abc}(t)$ and currents $i_1^{abc}(t)$ of three-level NPC VSI are [42]

$$u_1^{abc}(t) = \begin{bmatrix} u_1^a(t) \\ u_1^b(t) \\ u_1^c(t) \end{bmatrix} = \widehat{U_1} \begin{bmatrix} \cos(\theta(t)) \\ \cos((\theta(t) - \frac{2\pi}{3}) \\ \cos((\theta(t) - \frac{4\pi}{3}) \end{bmatrix}, \tag{4.34}$$

$$i_1^{abc}(t) = \begin{bmatrix} i_1^a(t) \\ i_1^b(t) \\ i_1^c(t) \end{bmatrix} = \widehat{I_1} \begin{bmatrix} \cos((\theta(t) - \varphi) \\ \cos((\theta(t) - \frac{2\pi}{3} - \varphi) \\ \cos((\theta(t) - \frac{4\pi}{3} - \varphi) \end{bmatrix}. \tag{4.35}$$

where $\widehat{U_1}$ $[V]$ is the amplitude of first harmonic of phase voltage, $\widehat{I_1}$ $[A]$ is the amplitude of first harmonic of phase current and φ $[rad]$ is the load power factor angle.

The space vector expressions are provided by inserting (4.34) into (4.13) (see Fig. 4.14)

$$\overrightarrow{u_1}(t) = |\overrightarrow{u_1}(t)|e^{j\theta(t)}, \tag{4.36}$$

$$\overrightarrow{i_1}(t) = |\overrightarrow{i_1}(t)|e^{j(\theta(t)-\varphi)}. \tag{4.37}$$

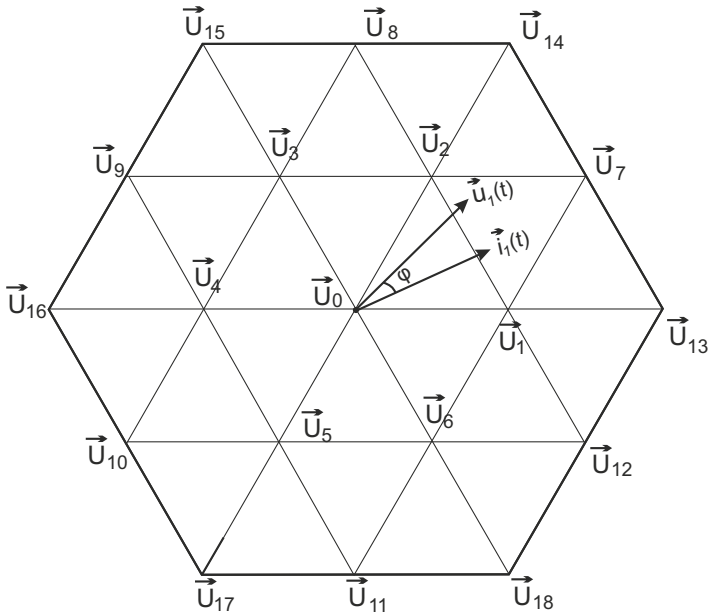


Figure 4.14: Space vector of the first harmonic of phase voltage and current for 3L NPC VSI.

The relationship among the sectors from one to six and first harmonic of phase voltage $u_1^a(t)$ and phase current $i_1^a(t)$ can be obtained by (4.34), (4.35), (4.36) and (4.37). Fig. 4.15 shows this relationship [43].

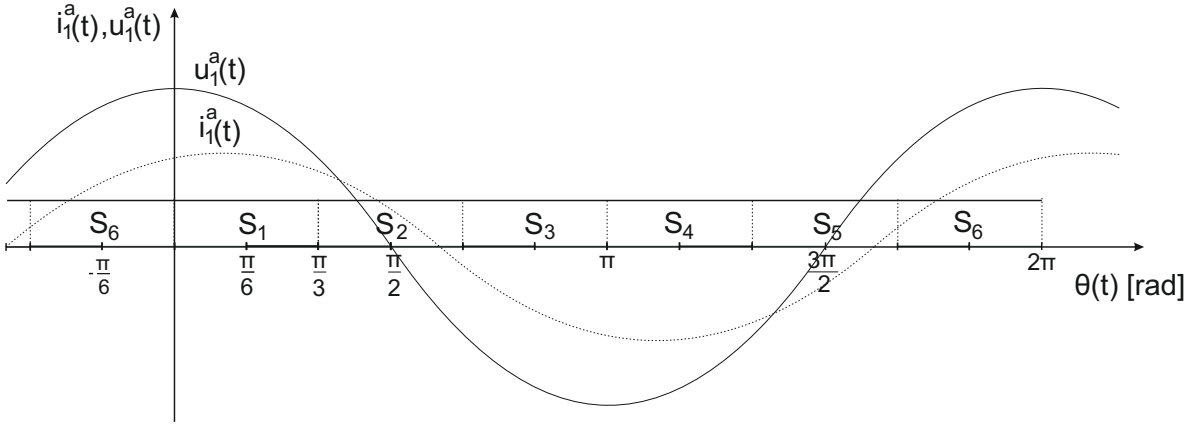


Figure 4.15: Relationship among the sectors and $u_1^a(t)$ and $i_1^a(t)$ for 3L NPC VSI.

As it can be seen from Tab. 4.4, in each sector, the switches in one leg of the three-level NPC VSI remain unchanged. For example, in the sector one, the switches in either leg "a" or leg "c" can be fixed.

Fig. 4.16 and Tab. 4.4 summarize the relationship among the sectors and the switching vector, where $x \in \{-1, 0, 1\}$ and this means the switches can be either on or off.

Sector	$[S_a^{U-L}(t)\ S_b^{U-L}(t)\ S_c^{U-L}(t)]^T$	Turn-on switches
1	$[1\ x\ x]$ or $[x\ x\ -1]$	$S_a^U(t)$ or $S_c^L(t)$
2	$[x\ 1\ x]$ or $[x\ x\ -1]$	$S_b^U(t)$ or $S_c^L(t)$
3	$[x\ 1\ x]$ or $[-1\ x\ x]$	$S_b^U(t)$ or $S_a^L(t)$
4	$[-1\ x\ x]$ or $[x\ x\ 1]$	$S_c^U(t)$ or $S_a^L(t)$
5	$[x\ -1\ x]$ or $[x\ x\ 1]$	$S_c^U(t)$ or $S_b^L(t)$
6	$[1\ x\ x]$ or $[x\ -1\ x]$	$S_a^U(t)$ or $S_b^L(t)$

Table 4.4: Relationship among the sectors and the switching vector.

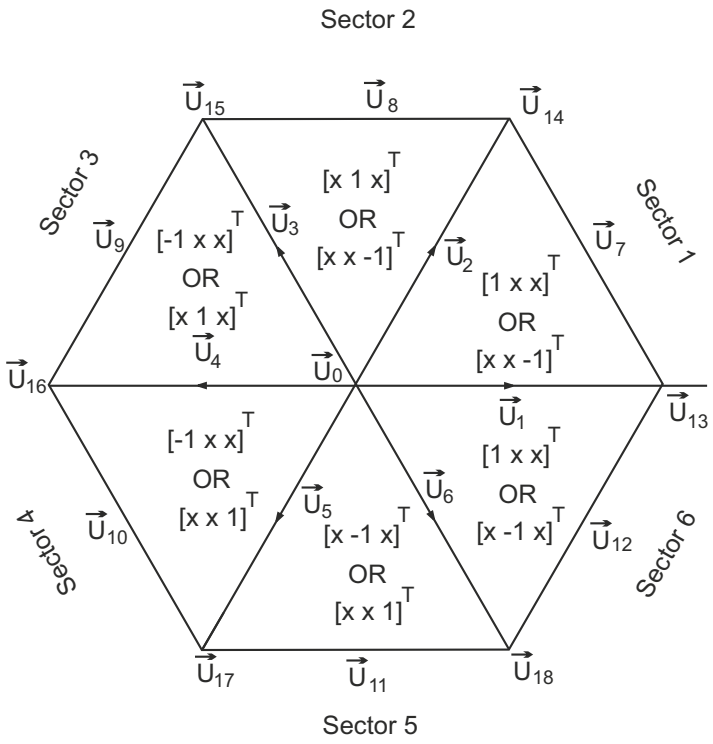


Figure 4.16: Relationship among the sectors and the switching vector.

Therefore, the upper or lower switches of one leg of the inverter can be remained unchanged for maximum two sectors $\theta(t) = \frac{2\pi}{3}$ $[rad]$. For example, the lower switches in leg "c", $S_c^L(t)$, can remain unchanged in the sector one and sector two. Thus, we eliminate switching losses for the leg "c" when the space vector lies in the sector one and two. However, if we want to meet the requirements R_1 and R_4, the switches of one leg do not change for $\frac{\pi}{3}$ $[rad]$. Becuase if the upper switches of one leg are on for $\theta(t)$ $[rad]$, the lower switches of the same leg must be turned on for $\pi+\theta(t)$ $[rad]$. Therefore, the upper and lower switch of each leg are turned on every $\frac{\pi}{3}$ $[rad]$. R_1 is met if the upper switches and lower switches are turned on equally in one switching period. Moreover, R_4 is met if $u_{ltl}^{abc}(\theta(t)) = -u_{ltl}^{abc}(\pi-\theta(t))$. This means the upper switches and lower switches should be alternatively turned on every $\frac{\pi}{3}$ $[rad]$. Therefore, the space vector diagram is divided into six regions equally as shown in Fig. 4.17. The upper switches are turned on in the shaded regions, while the lower switches are turned on in the no shaded regions. As it can be seen from Fig. 4.17, we can define the rotating angle θ_1 $[rad]$ between the axis α and μ. Therefore, the shaded regions and no shaded regions can rotate in the space vector diagram. The rotating angle θ_1 $[rad]$ is given by

$$\theta_1 = \frac{\pi}{6} + \varphi; -\frac{\pi}{2} \leq \varphi \leq \frac{\pi}{2} \rightarrow -\frac{\pi}{3} \leq \theta_1 \leq \frac{2\pi}{3} \tag{4.38}$$

The load power factor angle φ $[rad]$ is used to determine the relationship among the phase currents and the sectors. For example, if $-\frac{\pi}{6} < \varphi < \frac{\pi}{6}$ then the peak of phase current $i_1^a(t)$ lies between the sector six and sector one. Therefore, $S_a^U(t)$ should remain unchanged in the sharing area among these sectors and the area one to reduce the switching power losses. Fig. 4.18 shows the relationship among the phase current $i_1^a(t)$, φ and θ_1 [44].

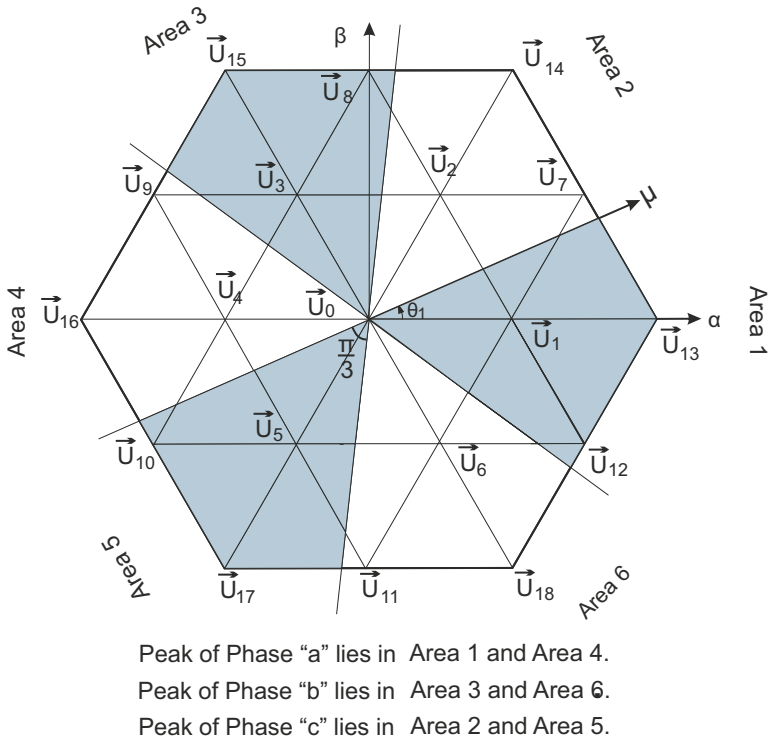


Figure 4.17: Alternative use of two switching sequences.

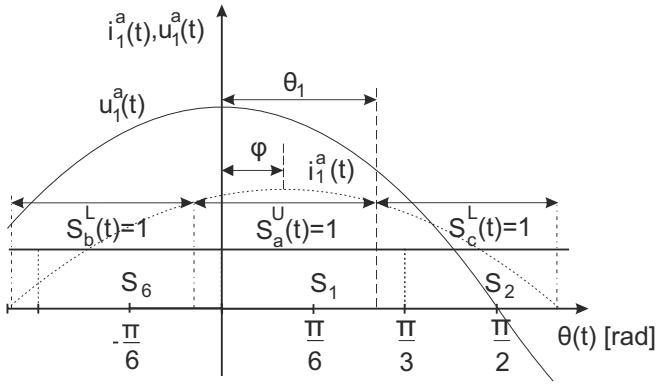


Figure 4.18: Phase current and the rotating angle.

To find out how we reach Fig. 4.17, we assume impedance of load is given by

$$\overrightarrow{z_1}(t) = |\overrightarrow{z_1}(t)|e^{j\varphi(t)}. \tag{4.39}$$

Therefore, the space vector for current is given by

$$\overrightarrow{i_1}(t) = \frac{\overrightarrow{u_1}(t)}{\overrightarrow{z_1}(t)} = \frac{|\overrightarrow{u_1}(t)|e^{j\theta(t)}}{|\overrightarrow{z_1}(t)|e^{j\varphi(t)}} = |\overrightarrow{i_1}(t)|e^{j(\theta(t)-\varphi(t))}. \tag{4.40}$$

It means the the stationary vectors from $\overrightarrow{U}_0$ to $\overrightarrow{U}_{18}$ should be rotated for $-\varphi(t)$ $[rad]$ and divided by $|\overrightarrow{z_1}(t)|$ to find the space vector for current (see Fig. 4.19).

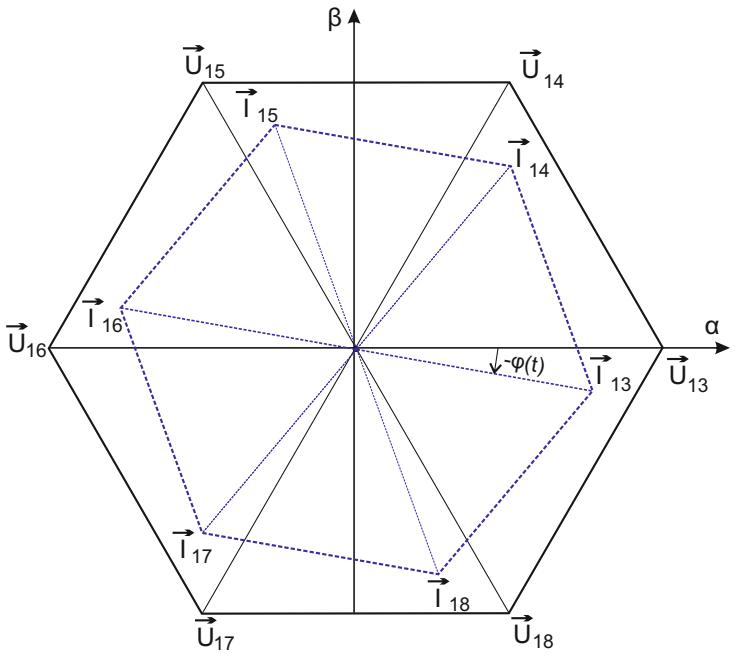


Figure 4.19: Solid lines are space vector of voltage and dashed lines are space vector for current.

And we know that orthogonal stationary reference frame, in which α axis and β axis are perpendicular to each other, but in the same plane as the three-phase reference frame. This means that maximum current $|\overrightarrow{i_1^d}(t)|$ is in phase with α axis (see Fig. 4.20).

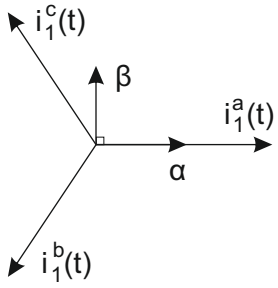


Figure 4.20: Combined vector three-phase reference frame and two-phase reference frame.

Fig. 4.21 is obtained by comibination of Fig. 4.19 and Fig. 4.20

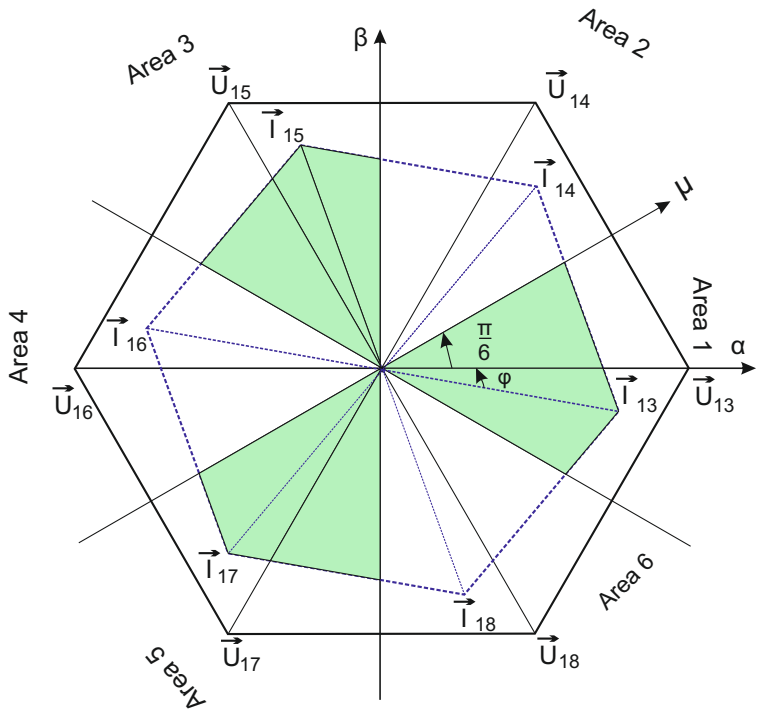


Figure 4.21: How to divide the current space vector to find areas.

Therefore, Fig. 4.17 can be found by multiplying (4.39) in the current space vector. If we consider (4.38), Fig. 4.22 and Tab. 4.4, we can find the relationship among the areas and the sectors. For example, if the load power factor angle φ is between $\frac{\pi}{6}$ $[rad]$ and $\frac{\pi}{2}$ $[rad]$, the peak of $i_1^a(t)$ (Area one) lies between sector one and sector two. Therefore, we try to minimize switching in area one for phase "a" to reduce the switching losses. Thus, if the area one lies in the sector one, the upper switches $S_a^U(t)$ ($[1\ x\ x]^T$) remain unchanged and if the

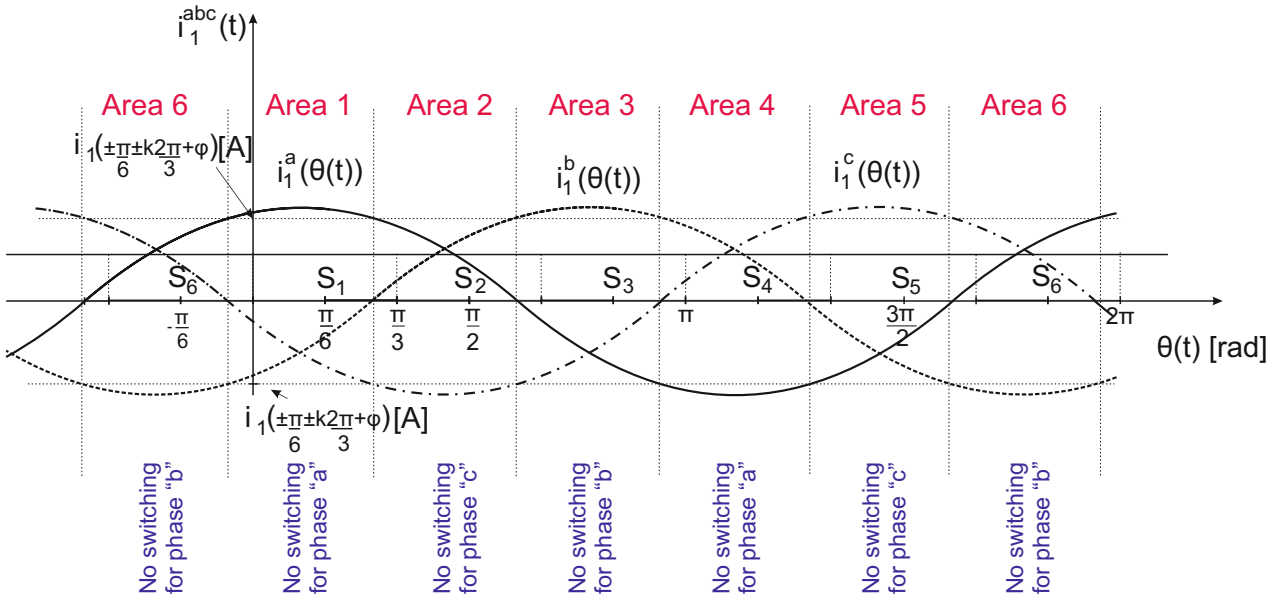
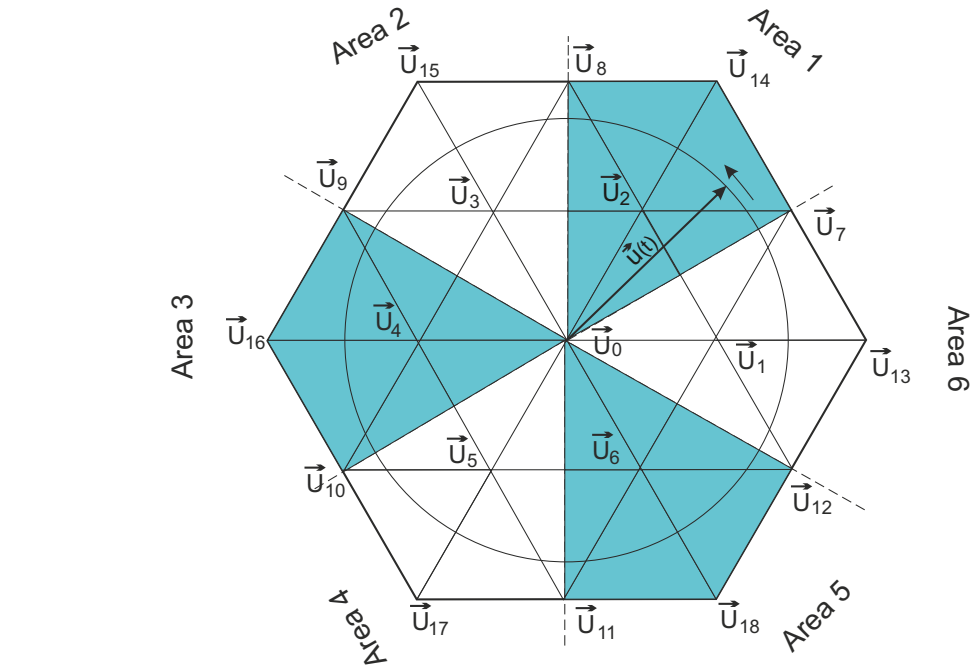


Figure 4.22: Relationship among the phase currents and the sectors ($i_1(\pm\frac{\pi}{6} \pm \frac{2k\pi}{3} + \varphi)$ $[A]$ is the amplitude of phase current in $(\pm\frac{\pi}{6} \pm \frac{2k\pi}{3} + \varphi)$ $[rad]$ where $k \in \{0, 1, 2\}$ is phases a, b and c respectively).

area one lies in the sector two, the inner switches $S_a^M(t)(\ [0\ x\ x]^T)$ remain unchanged for the stationary vectors $\overrightarrow{U}_0$, $\overrightarrow{U}_2$, $\overrightarrow{U}_3$ and $\overrightarrow{U}_8$. Tab. 4.5 summarizes these relationships.
Last step is to design switching sequences. In practice, the switching sequences for a given $\overrightarrow{u}(t)$ is not unique, but it must satisfy the requirements from R_1 to R_5. Fig. 4.23 shows a typical switching sequences for $\varphi = \frac{\pi}{3}$ $[rad]$. As it can be seen from Fig 4.23, the switch changes from one switching state to the next by only two switches in the same phase (R_2). Beside this, if $\overrightarrow{u}(t)$ moves from one sector/region to the next sector/region requires one switching (R_3). In addition to these, we try to minimize the switching when the peak of currents pass through the semiconductor devices (R_5). Moreover, $u_{ltl}^{abc}(\theta(t)) = -u_{ltl}^{abc}(\pi - \theta(t))$ is met, therefore even-harmonics are eliminated (R_4). Finally, every $\frac{\pi}{3}$ $[rad]$, we used the same number of the positive and negative stationary vectors $\overrightarrow{U}_1$ to $\overrightarrow{U}_6$. Thus, the effect of switching states on $u_M(t)$ are minimized (R_1).



Area 1

Sector 1, Rergion 4					
$\vec{U}_7$	$\vec{U}_1$	$\vec{U}_2$	$\vec{U}_2$	$\vec{U}_1$	$\vec{U}_7$
1	1	1	1	1	1
0	0	1	1	0	0
-1	0	0	0	0	-1
$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$

Sector 1, Rergion 3					
$\vec{U}_7$	$\vec{U}_{14}$	$\vec{U}_2$	$\vec{U}_2$	$\vec{U}_{14}$	$\vec{U}_7$
1	1	1	1	1	1
0	1	1	1	1	0
-1	-1	0	0	-1	-1
$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$

Sector 2, Rergion 2					
$\vec{U}_2$	$\vec{U}_8$	$\vec{U}_{14}$	$\vec{U}_{14}$	$\vec{U}_8$	$\vec{U}_2$
0	0	1	1	0	0
0	1	1	1	1	0
-1	-1	-1	-1	-1	-1
$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$

Sector 2, Rergion 4					
$\vec{U}_2$	$\vec{U}_8$	$\vec{U}_3$	$\vec{U}_3$	$\vec{U}_8$	$\vec{U}_2$
0	0	0	0	0	0
0	1	1	1	1	0
-1	-1	0	0	-1	-1
$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$

Area 2

Sector 2, Rergion 4					
$\vec{U}_8$	$\vec{U}_2$	$\vec{U}_3$	$\vec{U}_3$	$\vec{U}_2$	$\vec{U}_8$
0	0	-1	-1	0	0
1	0	0	0	0	1
-1	-1	-1	-1	-1	-1
$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$

Sector 2, Rergion 3					
$\vec{U}_8$	$\vec{U}_{15}$	$\vec{U}_3$	$\vec{U}_3$	$\vec{U}_{15}$	$\vec{U}_8$
0	-1	-1	-1	-1	0
1	1	0	0	1	1
-1	-1	-1	-1	-1	-1
$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$

Sector 3, Rergion 2					
$\vec{U}_3$	$\vec{U}_9$	$\vec{U}_{15}$	$\vec{U}_{15}$	$\vec{U}_9$	$\vec{U}_3$
0	-1	-1	-1	-1	0
1	1	1	1	1	1
0	0	-1	-1	0	0
$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$

Sector 3, Rergion 4					
$\vec{U}_3$	$\vec{U}_9$	$\vec{U}_4$	$\vec{U}_4$	$\vec{U}_9$	$\vec{U}_3$
0	-1	-1	-1	-1	0
1	1	0	0	1	1
0	0	0	0	0	0
$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$

Area 3

Sector 3, Rergion 4					
$\vec{U}_9$	$\vec{U}_3$	$\vec{U}_4$	$\vec{U}_4$	$\vec{U}_3$	$\vec{U}_9$
-1	0	0	0	0	-1
1	1	1	1	1	1
0	0	1	1	0	0
$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$

Sector 3, Rergion 3					
$\vec{U}_9$	$\vec{U}_{16}$	$\vec{U}_4$	$\vec{U}_4$	$\vec{U}_{16}$	$\vec{U}_9$
-1	-1	0	0	-1	-1
1	1	1	1	1	1
0	1	1	1	1	0
$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$

Sector 4, Rergion 2					
$\vec{U}_4$	$\vec{U}_{10}$	$\vec{U}_{16}$	$\vec{U}_{16}$	$\vec{U}_{10}$	$\vec{U}_4$
-1	-1	-1	-1	-1	-1
0	0	1	1	0	0
0	1	1	1	1	0
$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$

Sector 4, Rergion 4					
$\vec{U}_4$	$\vec{U}_{10}$	$\vec{U}_5$	$\vec{U}_5$	$\vec{U}_{10}$	$\vec{U}_4$
-1	-1	0	0	-1	-1
0	0	0	0	0	0
0	1	1	1	1	0
$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$

Figure 4.23: The proposed switching sequences in three-level NPC VSI for $\varphi = \frac{\pi}{3}$ $[rad]$.

$\varphi\ [rad]$	$\frac{-\pi}{2} \leq \varphi \leq \frac{-\pi}{6}$	$-\frac{\pi}{6} \leq \varphi \leq \frac{\pi}{6}$	$\frac{\pi}{6} \leq \varphi \leq \frac{\pi}{2}$
$\theta_1[rad]$	$\frac{-\pi}{3} \leq \theta_1 \leq 0$	$0 \leq \theta_1 \leq \frac{\pi}{3}$	$\frac{\pi}{3} \leq \theta_1 \leq \frac{2\pi}{3}$
Area 1	• Sector 6 [1 x x] • Sector 5 [0 x x] for $\overrightarrow{U}_0$, $\overrightarrow{U}_5$, $\overrightarrow{U}_6$, $\overrightarrow{U}_{11}$	[1 x x]	• Sector 1 [1 x x] • Sector 2 [0 x x] for $\overrightarrow{U}_0$, $\overrightarrow{U}_2$, $\overrightarrow{U}_3$, $\overrightarrow{U}_8$
Area 2	• Sector 1 [x x -1] • Sector 6 [x x 0] for $\overrightarrow{U}_0$, $\overrightarrow{U}_6$, $\overrightarrow{U}_1$, $\overrightarrow{U}_{12}$	[x x -1]	• Sector 2 [x x -1] • Sector 3 [x x 0] for $\overrightarrow{U}_0$, $\overrightarrow{U}_3$, $\overrightarrow{U}_4$, $\overrightarrow{U}_9$
Area 3	• Sector 2 [x 1 x] • Sector 1 [x 0 x] for $\overrightarrow{U}_0$, $\overrightarrow{U}_1$, $\overrightarrow{U}_2$, $\overrightarrow{U}_7$	[x 1 x]	• Sector 3 [x 1 x] • Sector4 [x 0 x] for $\overrightarrow{U}_0$, $\overrightarrow{U}_4$, $\overrightarrow{U}_5$, $\overrightarrow{U}_{10}$
Area 4	• Sector 3 [-1 x x] • Sector 2 [0 x x] for $\overrightarrow{U}_0$, $\overrightarrow{U}_2$, $\overrightarrow{U}_3$, $\overrightarrow{U}_8$	[-1 x x]	• Sector 4 [-1 x x] • Sector 5 [0 x x] for $\overrightarrow{U}_0$, $\overrightarrow{U}_5$, $\overrightarrow{U}_6$, $\overrightarrow{U}_{11}$
Area 5	• Sector 4 [x x 1] • Sector 3 [x x 0] for $\overrightarrow{U}_0$, $\overrightarrow{U}_3$, $\overrightarrow{U}_4$, $\overrightarrow{U}_9$	[x x 1]	• Sector 5 [x x 1] • Sector 6 [x x 0] for $\overrightarrow{U}_0$, $\overrightarrow{U}_6$, $\overrightarrow{U}_1$, $\overrightarrow{U}_{12}$
Area 6	• Sector 5 [x -1 x] • Sector 4 [x 0 x] for $\overrightarrow{U}_0$, $\overrightarrow{U}_4$, $\overrightarrow{U}_5$, $\overrightarrow{U}_{10}$	[x -1 x]	• Sector 6 [x -1 x] • Sector 1 [x 0 x] for $\overrightarrow{U}_0$, $\overrightarrow{U}_1$, $\overrightarrow{U}_2$, $\overrightarrow{U}_7$

Table 4.5: The relationship among the rotating angle θ_1 and the load power factor angle φ and sectors.

Chapter 5

Simulations

This chapter presents the implementation of the power losses of two-level VSI and three-level NPC VSI. The models are built on the corresponding equations in the previous chapters. The parameters of semiconductor devices are taken from the datasheet " 5SNA 1200E330100" and "MTE53N50E/D" to model the VSIs and their power losses. The simulation is done in MATLAB®-Simulink® (2014b) using the solver ode4 (Runge-kutta) with the fundamental sample time $1e-6$ $[s]$. In the following sections, we divide the models into several subsystem and explain each subsystems. Here, we first simulate the power losses in two-level VSI. Afterwards, the losses in three-level NPC VSI are simulated. Finally, we compare the power losses in the two-level VSI to power losses in the three-level NPC VSI.

5.1 Simulation of Power Losses In Two-Level VSI

Fig. 5.1 shows the block diagram of simulation for power losses in two-level VSI. As it can be seen, they are divided into several subsystems. Each subsystem receives the signals as the inputs and generates the outputs for the corresponding subsystems. Some inputs are defined by user. For example, $|U_{ref}|$, φ_{ref} and f_{ref} are the amplitude of reference sinusoidal waveforms, initial phase shift of reference sinusoidal waveforms and the frequency of reference sinusoidal waveforms. Moreover, it is assumed that the DC-link voltage are constant and it is equal to U_{dc}. In addition to these, the switching frequency is given by f_s. Finally, we receive $IGBT/MOSFET$ variable. If it is equal to 1, the switches are composed of IGBTs and diodes, else they are MOSFETs and diodes. The value of parameters are given in Tab. 5.1.

Parameter	$\|U_{ref}\|$ $[V]$	φ_{ref} $[rad]$	f_{ref} $[Hz]$	f_s $[Hz]$	$U_{dc}[V]$
Value	200	0	50	10000	580

Table 5.1: Parameters of reference sinusoidal waveforms.

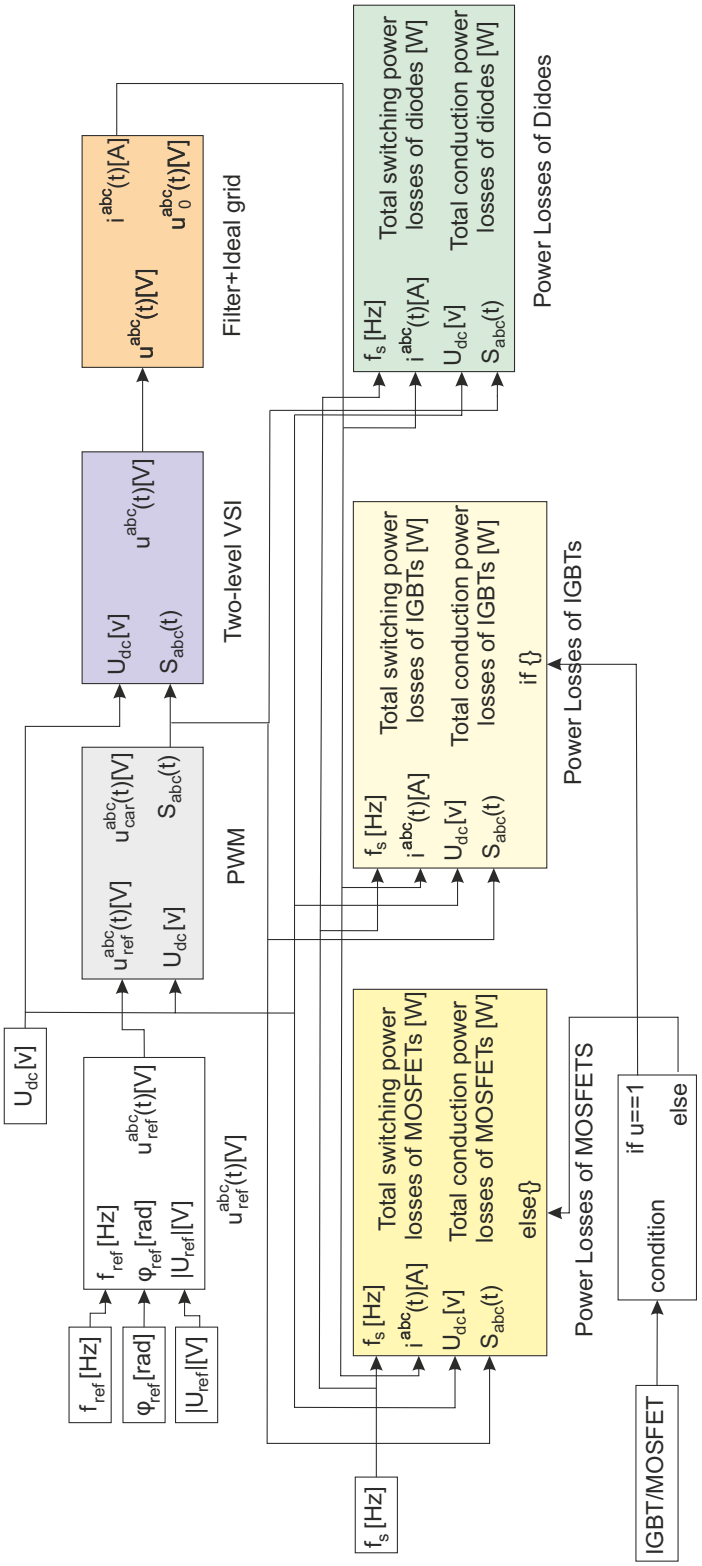


Figure 5.1: Simulation of Power losses in two-level VSI.

Subsystem $u_{ref}^{abc}(t)$ uses (4.1) to generate the three-phase sinusoidal reference waveforms. These waveforms apply in the subsequent subsystem PWM. Fig. 5.2 shows the three-phase sinusoidal reference waveforms model and Fig. 5.3 illustrates the output of this subsystem.

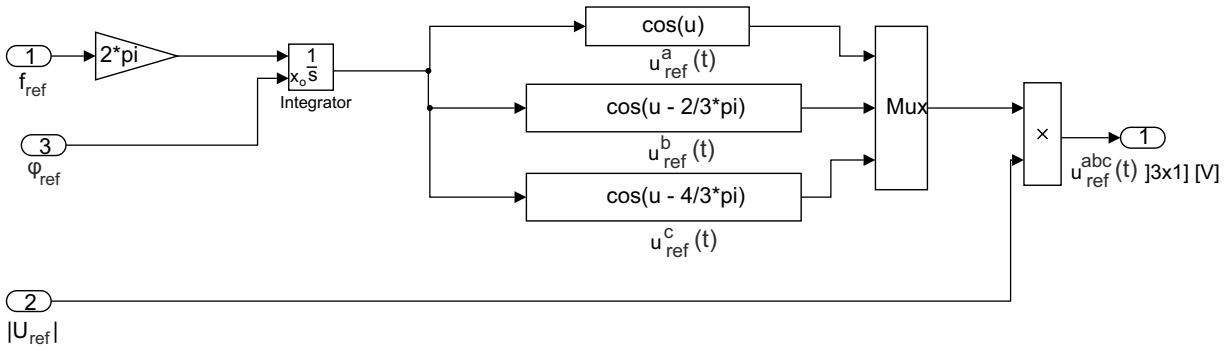


Figure 5.2: Generate three-phase sinusoidal waveforms.

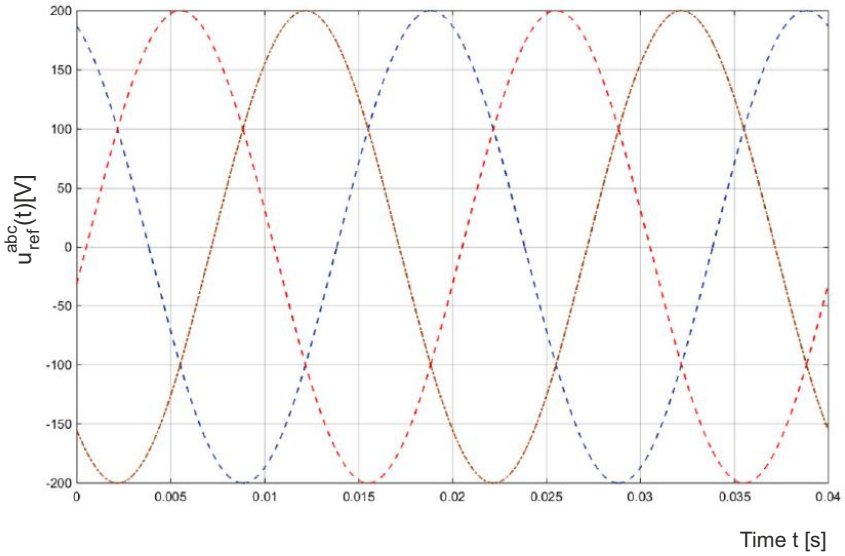


Figure 5.3: The output of subsystem $u_{ref}^{abc}(t)$.

The subsystem PWM receives $u_{ref}^{abc}(t)$ $[V]$ waveforms and U_{dc} $[V]$. $u_{ref}^{abc}(t)$ is normalized and compered to triangular waveform with frequency f_s $[Hz]$ and amplitude $\widehat{U_c} = 1$ $[V]$ to generates $S_{abc}(t)$. Afterwards, the switching function $S_{abc}(t)$ is used in the subsystem

Two – level VSI. Fig. 5.4 shows the model of $S_{abc}(t)$ in Simulink and Fig. 5.5 illustrates the output of the subsystem PWM.

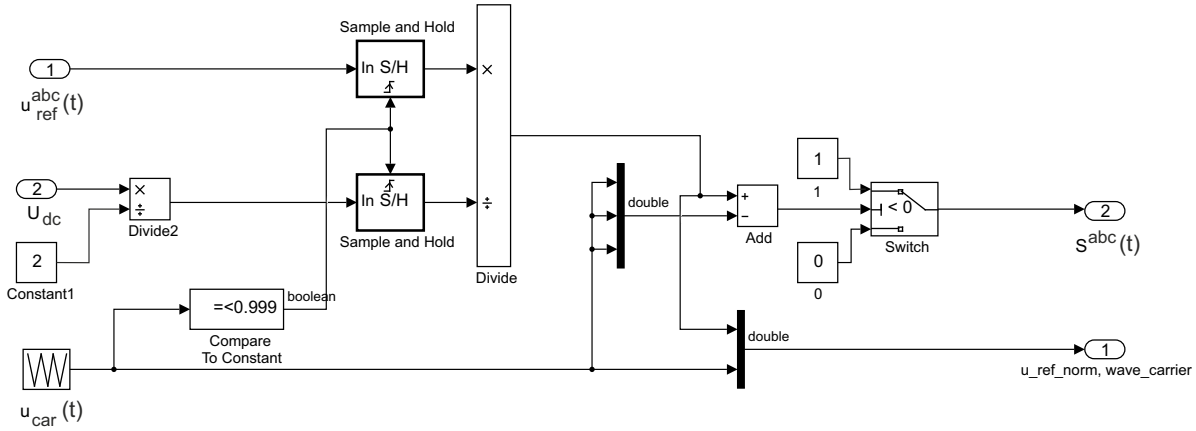


Figure 5.4: Generate $S_{abc}(t)$.

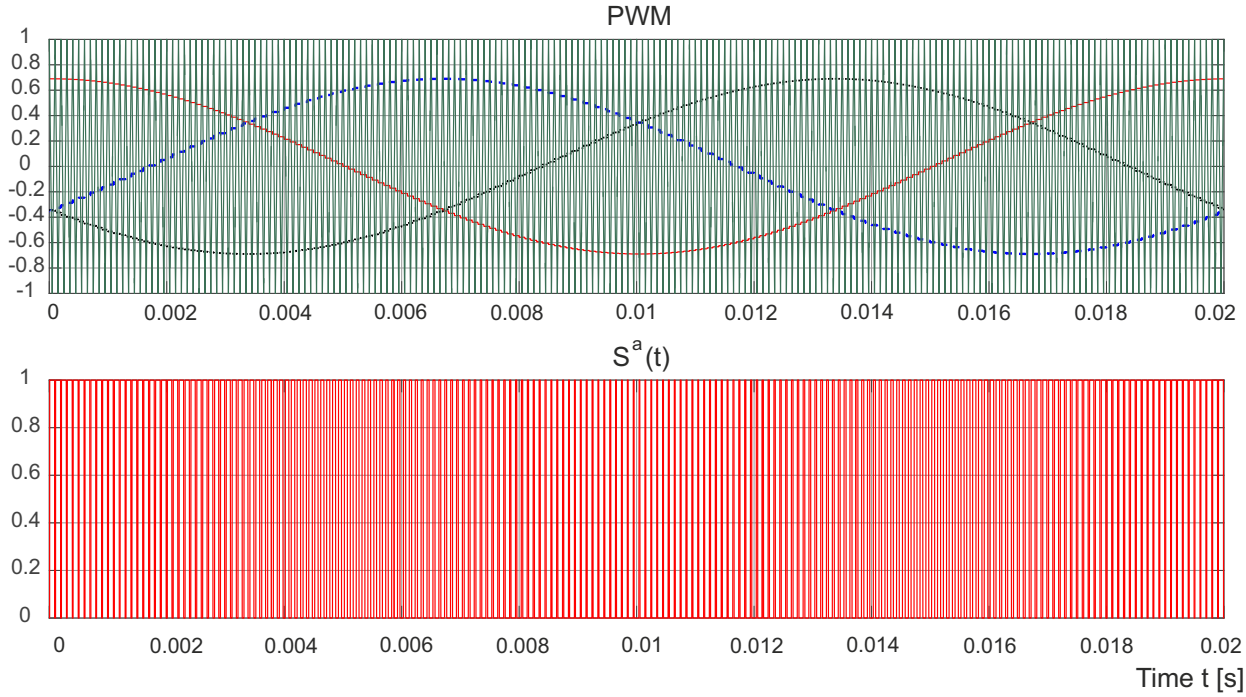


Figure 5.5: The output of subsystem PWM for one period ($f_{ref} = 50\ [Hz]$, $f_s = 10000\ [Hz]$, $r_A = 0.689$, and $r_f = 200$).

(3.11) is used to model the two-level VSI. As it can be seen from Fig. 5.6, $S_{abc}(t)$ and

DC-link voltage are applied in this subsystem to generate the phase voltages $u^{abc}(t)$. Fig. 5.7 shows the output waveform $u^a(t)$.

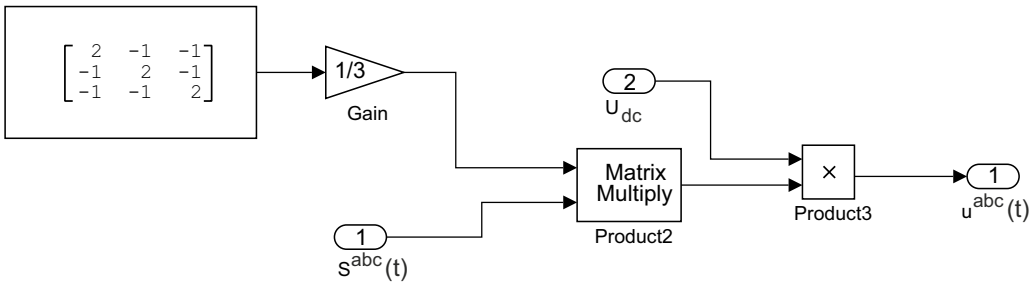


Figure 5.6: Model of two-level VSI.

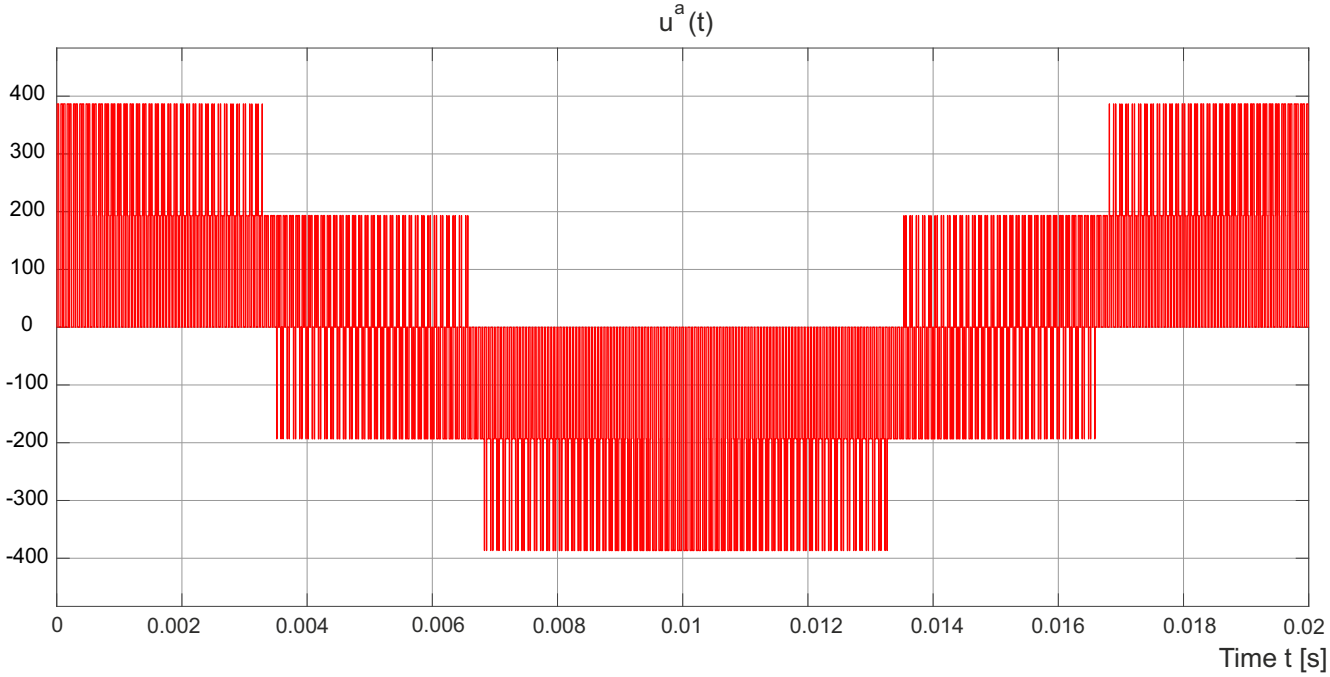


Figure 5.7: The output of one phase of subsystem $Two-level\ VSI$ for one period.

(3.1.2) and (3.1) are used to model the filter and ideal grid. The inputs are $u_{abc}(t)$ from the previous subsystem. The ideal symmetrical three-phase sources are the sinusoidal voltage sources with constant amplitude $|U_0|$ $[V]$, constant frequency f_0 $[Hz]$ and initial phase shift φ_0 $[rad]$. Tab. 5.2 gives $|U_0|$, f_0, φ_0, R_{abc} and L_{abc} used in the simulation.

Parameter	$\|U_0\|$ $[V]$	φ_0 $[rad]$	$f_0[hz]$	R_{abc} $[\Omega]$	L_{abc} $[H]$
value	100	0	50	0.156	18e-3

Table 5.2: The values of the filter and the ideal symmetrical three-phase sources.

Fig. 5.8 and Fig. 5.9 show the model of the filter and the model of ideal symmetrical three-phase sources respectively. Fig. 5.10 illustrates the phase voltage $u^a(t)$, the ideal symmetrical voltage source $u_0^a(t)$ and the phase current $i^a(t)$ respectively. Now, the power losses of the semiconductor devices in two-level VSI can be obtained by using $i^{abc}(t)$ in the subsystems *Power Losses of MOSFETs*, *Power Losses of IGBTs* and *Power Losses of Diodes*.

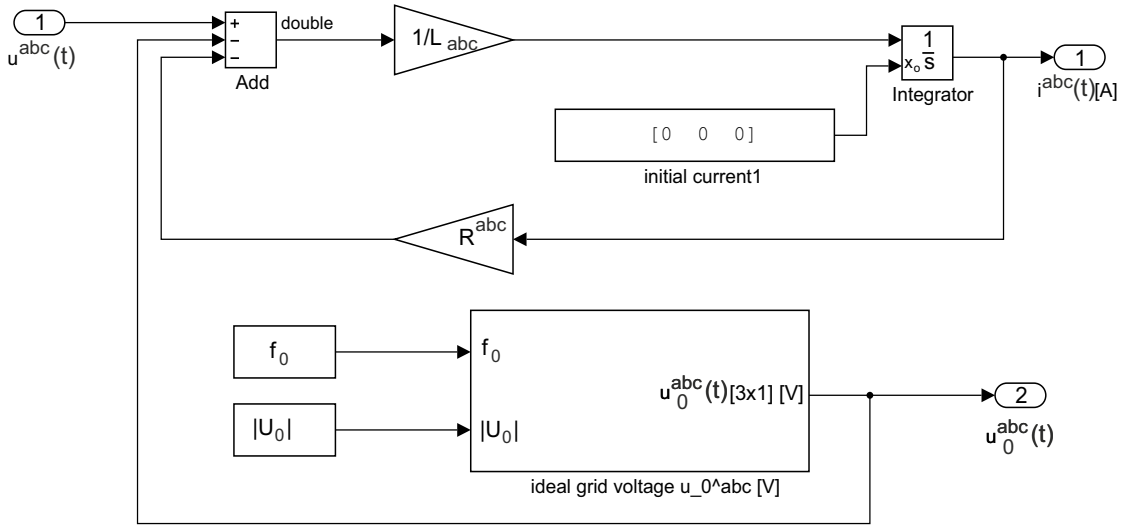


Figure 5.8: Model of the filter and ideal grid.

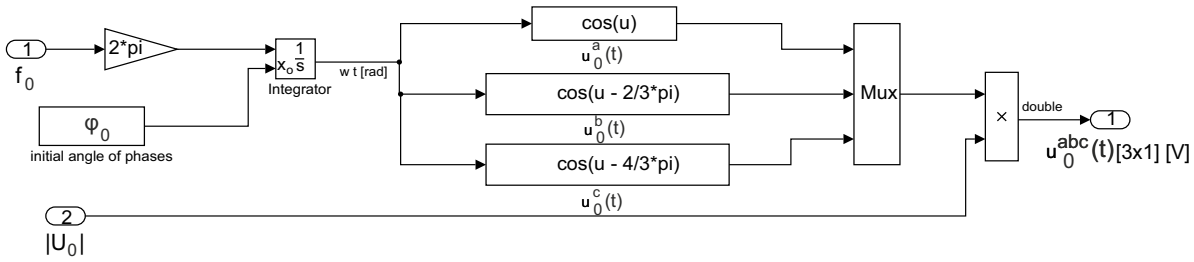


Figure 5.9: Model of the ideal symmetrical three-phase sources.

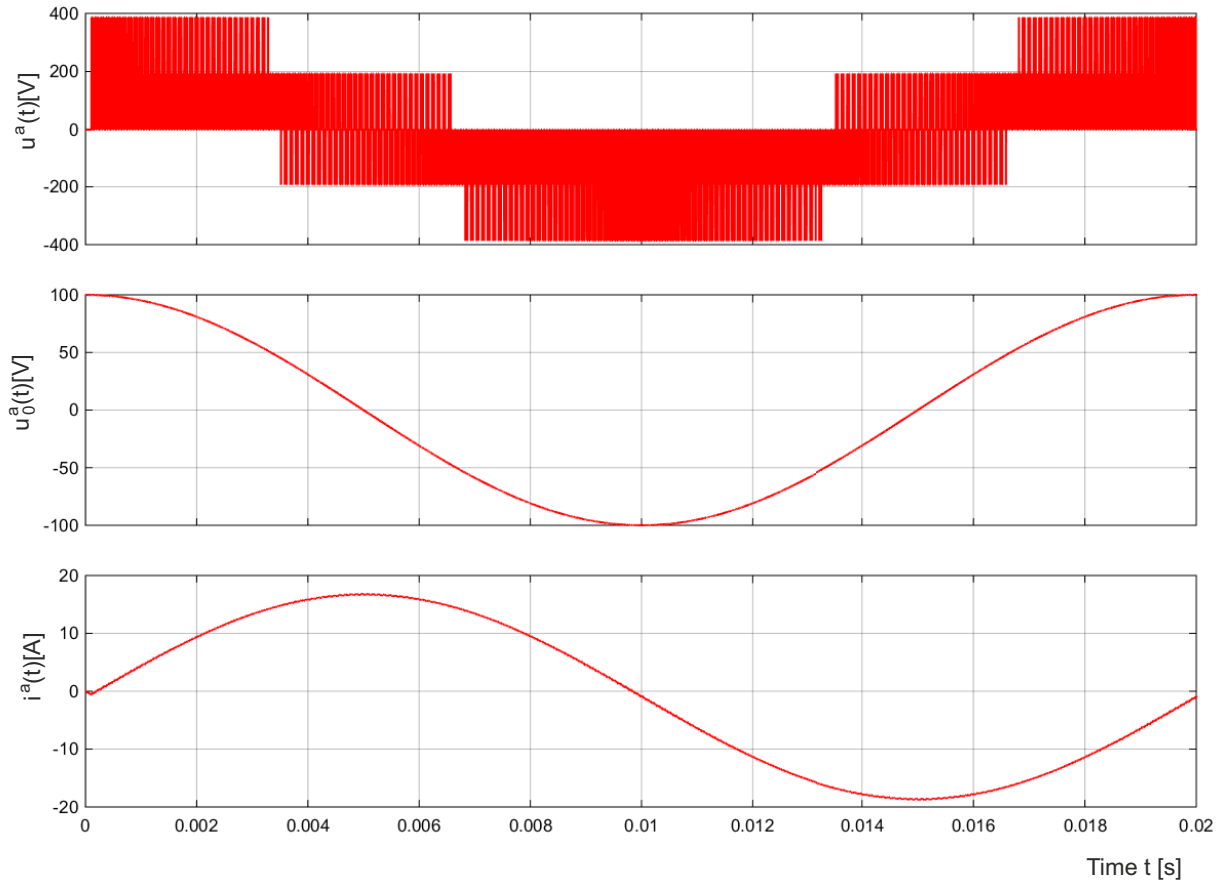


Figure 5.10: The output of one phase of subsystem *Filter + Ideal grid* for one period.

The subsystem *Power Losses of IGBTs* is divided into several subsystems. Fig. 5.11 shows the inside of this subsystem.

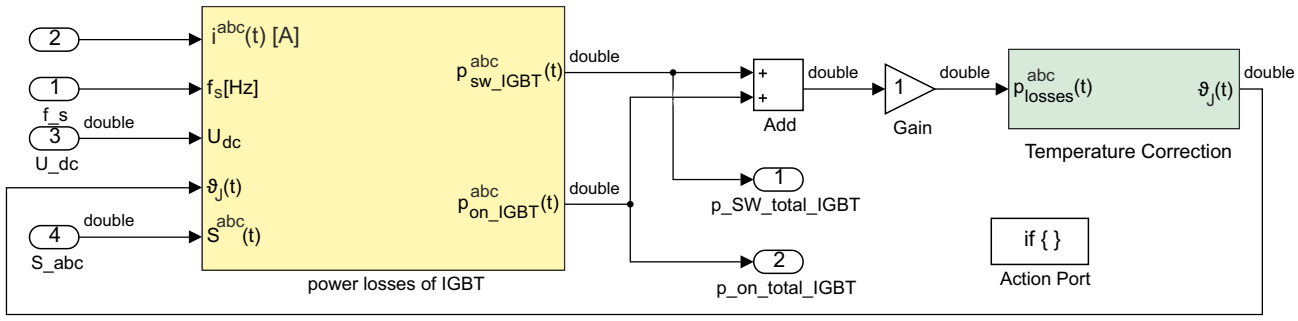


Figure 5.11: Inside the subsystem *Power Losses of IGBTs*

The subsystem *Temperature Correction* receives the summation of the conduction and switching power losses. Afterwards, (A.14) is used to change the junction temperature based on total power losses. Then, the junction temperature $\vartheta(t)$ applies on dynamic resistances, threshold voltages and the switching losses.

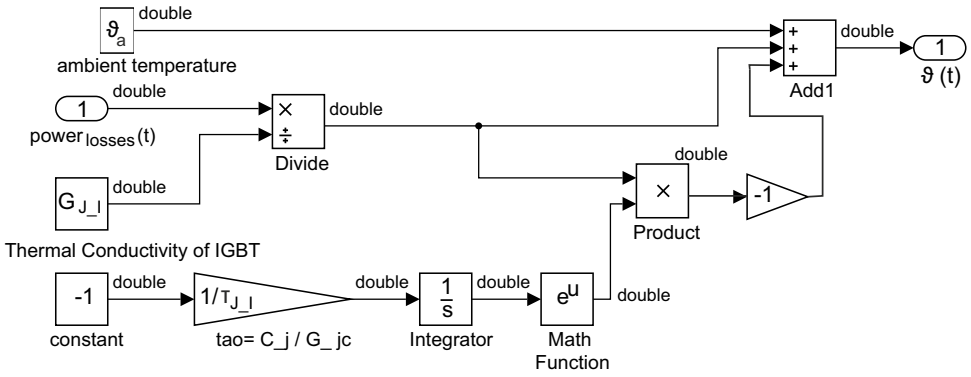


Figure 5.12: Model of junction temperature based on the total power losses.

We can use Fig. 5.12 also for diodes and MOSFETs to change the junction temperature. Note that the thermal conductivity of junction-case G_J and time constant τ_J should be set to the appropriate value for other semiconductor devices. Tab. 5.3 gives the value of parameters that we used here based on the datasheet. Moreover, we assume that the ambient is air and ϑ_a is equal to 40 $[C]$.

Parameter	IGBT G_{J-I} $[\frac{W}{C}]$	MOSFET G_{J-M} $[\frac{W}{C}]$	Diode G_{J-D} $[\frac{W}{C}]$	IGBT τ_{J-I} $[s]$	MOSFET $\tau_{J-M}[s]$	Diode τ_{J-D} $[s]$	$\vartheta_a[C]$	$\vartheta_{ja}(0)$ $[C]$
Value	1/0.0085	1/0.28	1/0.017	0.2	0.2	0.1	40	0

Table 5.3: Thermal parameters based on datasheets $MTE53N50E/D$ and $5SNA1200G450300$.

Inside the *Power Losses of IGBT* block, we have four blocks to compute the power losses the IGBTs in two-level VSI (see Fig. 5.13). The subsystem *Conduction power losses of IGBT* receives the phase currents $i^{abc}(t)$ $[A]$ and the junction temperature $\vartheta_J(t)$ $[C]$. Then, it generates the conduction power losses by using (2.37). The subsystems $Turn-off$ *switching losses of IGBT* and $Turn-on$ *switching losses of IGBT* get the switching frequency f_s $[Hz]$, DC-link voltage U_{dc} $[V]$, the phase currents $i^{abc}(t)$ $[A]$ and the junction temperature $\vartheta_J(t)$ $[C]$. These generate the switching power losses by using (2.44). At the end, the outputs of these three subsystems, phase currents $i^{abc}(t)$ $[A]$ and the switching function $S_{abc}(t)$ are inserted into subsystem *Power losses of IGBT in 2L VSI*. This subsystem generates power losses of IGBTs in two-level VSI by using (3.20) and (3.35).

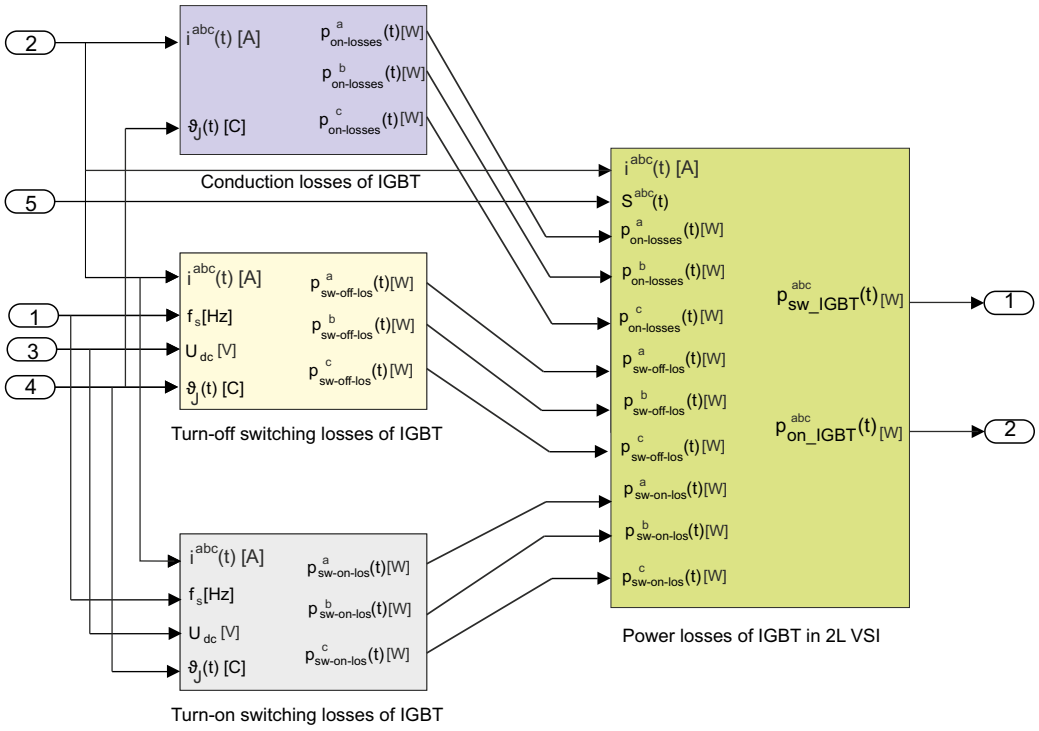


Figure 5.13: Inside the power losses of IGBT block.

Note that the subsystems *Power losses of MOSFETs* and *Power losses of Diodes* have the same subsystems to generate the power losses. Moreover, the rest of parameters that we used to simulate the power losses are given in Tab. 5.4 and Tab. 5.5.

Diode	$R_{d-D}(@25[C])$ $[\Omega]$	$U_{th-D}(@25[C])$ $[V]$	$R_{d-D}(@125[C])$ $[\Omega]$	$U_{th-D}(@125[C])$ $[V]$
Value	0.0009	1.94	0.00126	1.76
Diode	Q_{rr} $[C]$	$I_{f-rated}$ $[A]$	$U_{R-rated}[V]$	-
Value	0.00103	1200	2800	-

Table 5.4: The parameters of diode used in Simulink.

IGBT	$R_{d-I}(@25[C])$ $[\Omega]$	$U_{th-I}(@25[C])$ $[V]$	$R_{d-I}(@125[C])$ $[\Omega]$	$U_{th-I}(@125[C])$ $[V]$
Value	0.00114	1.16	0.00176	1.28
IGBT	$E_{sw-I-on}$ $[J]$	$E_{sw-I-off}$ $[J]$	$I_{C-rated}$ $[A]$	$U_{CE-rated}[V]$
Value	3.08	4.96	1200	2800

Table 5.5: The parameters of IGBT used in Simulink.

Fig. 5.14 to Fig. 5.16 show the results of simulation.

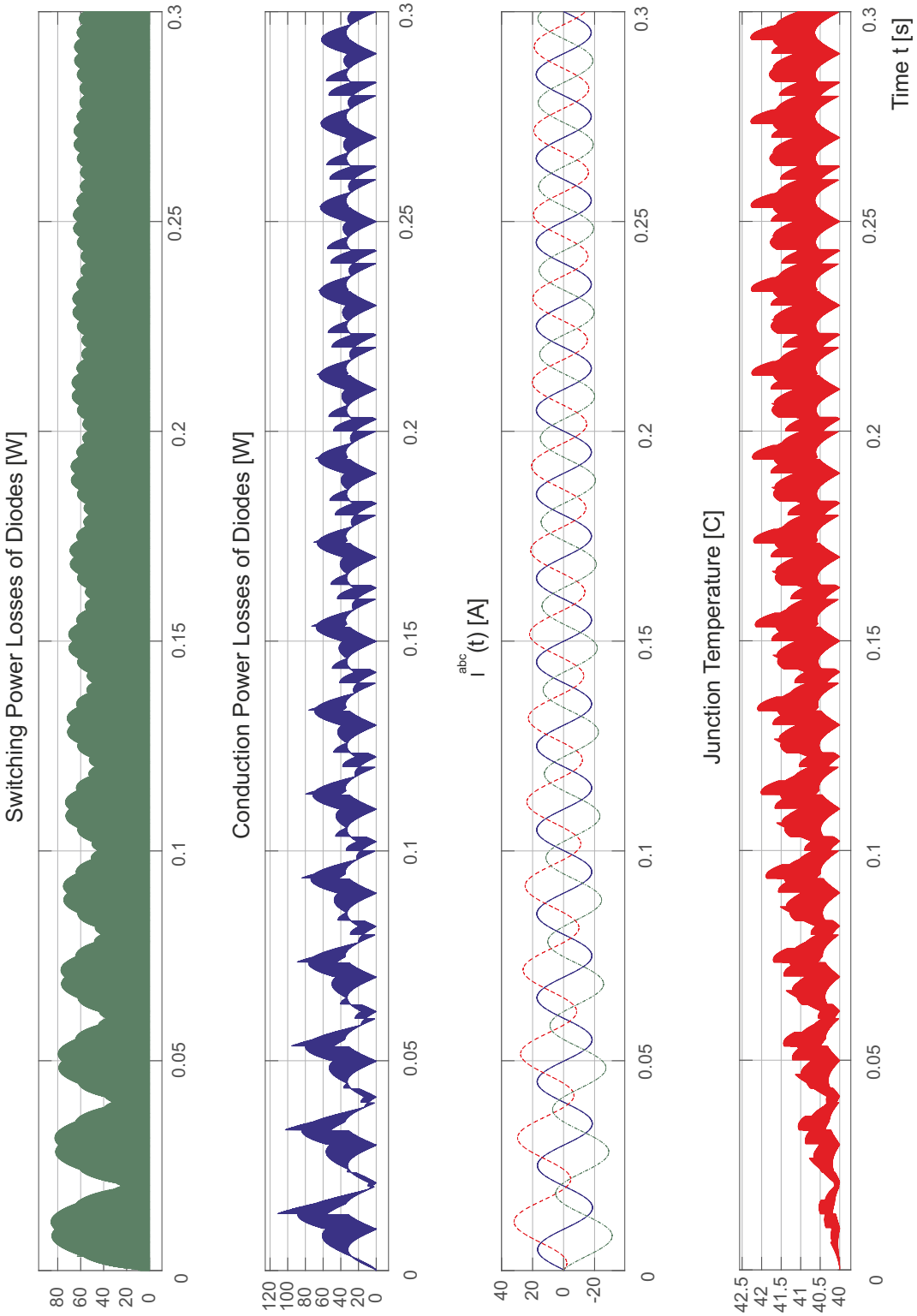


Figure 5.14: Power losses of all diodes in two-level VSI.

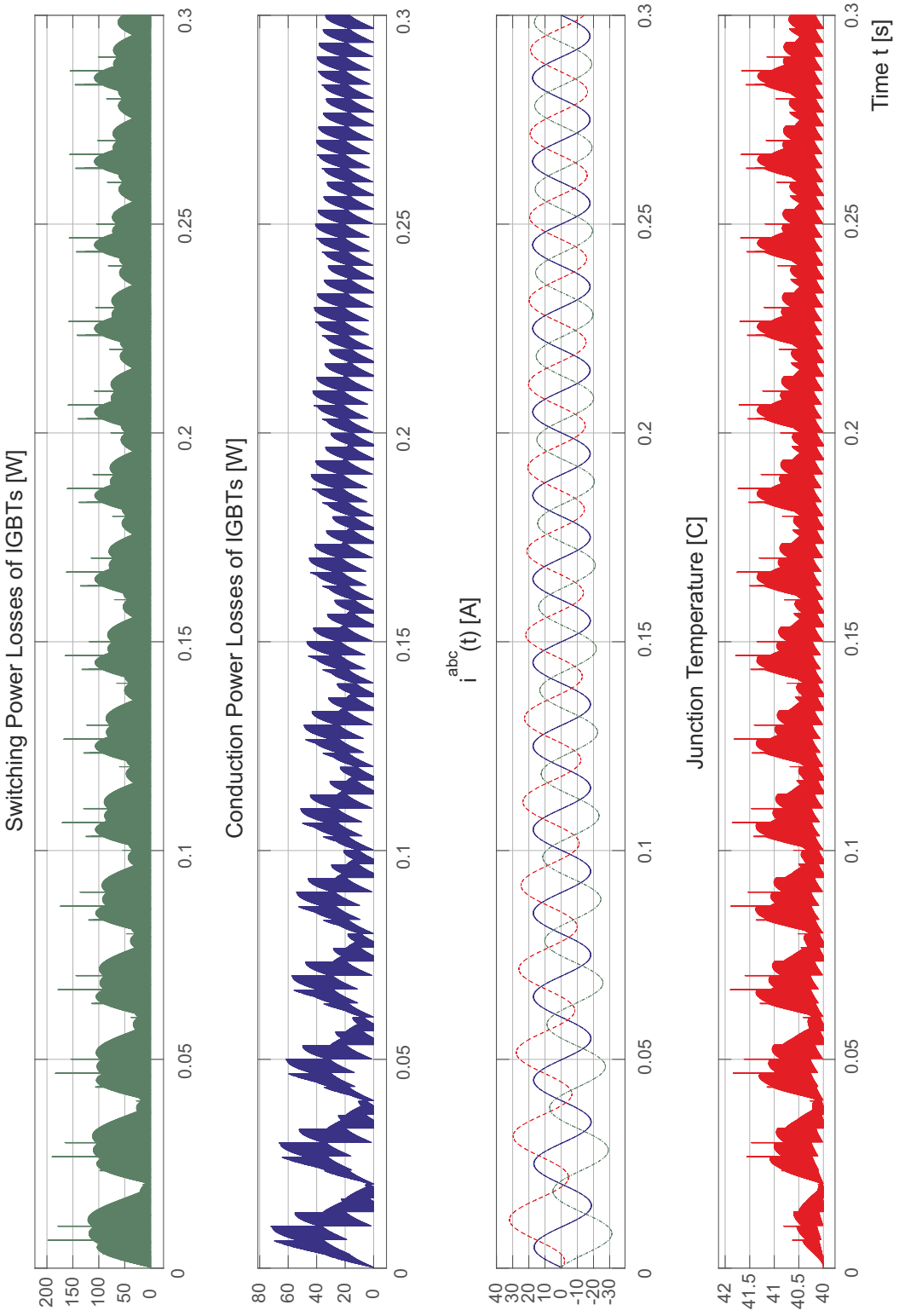


Figure 5.15: Power losses of all IGBTs in two-level VSI.

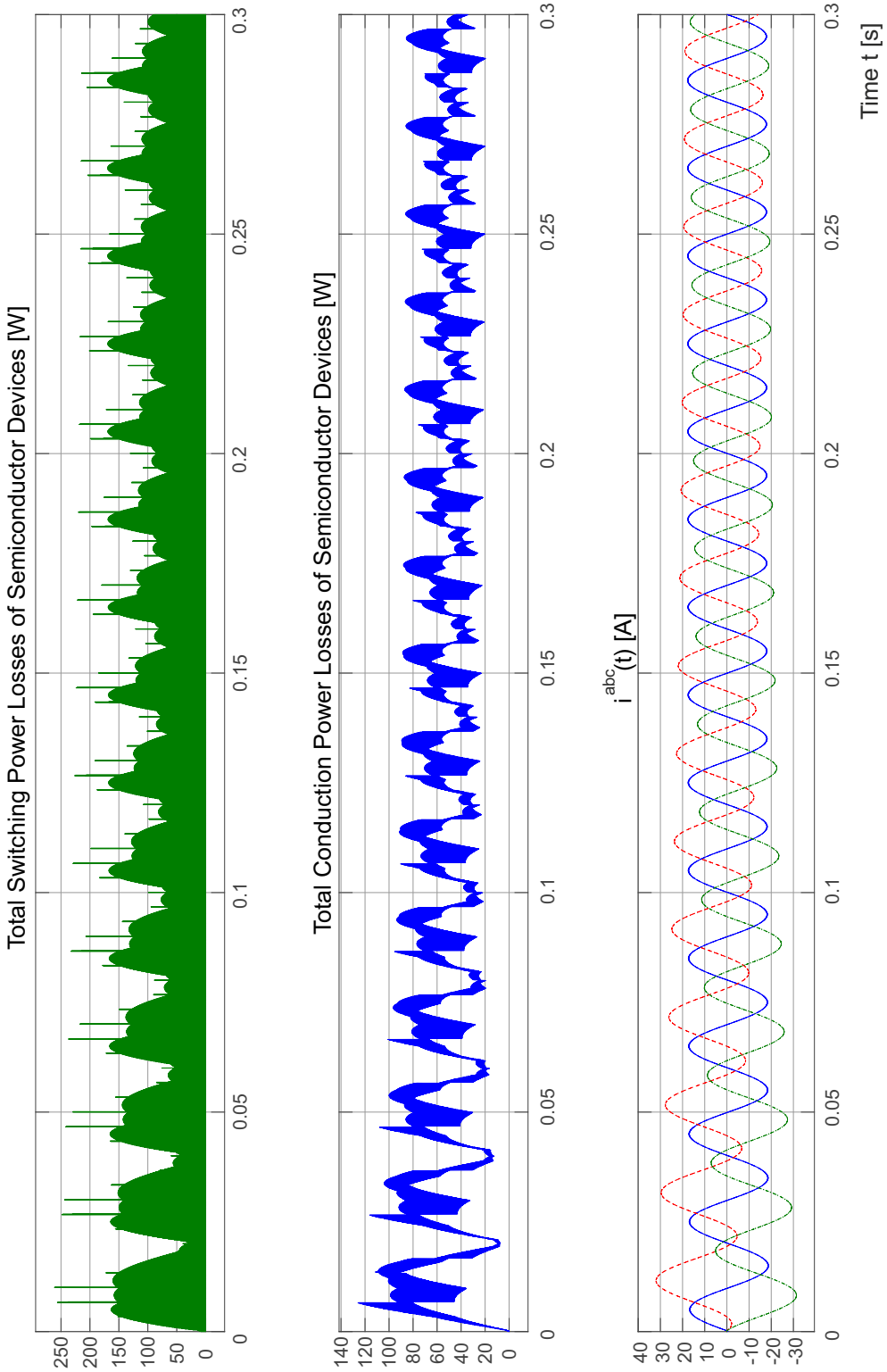


Figure 5.16: Total power losses of semiconductor devices in two-level VSI.

5.2 Simulation of Losses in Three-Level NPC VSI

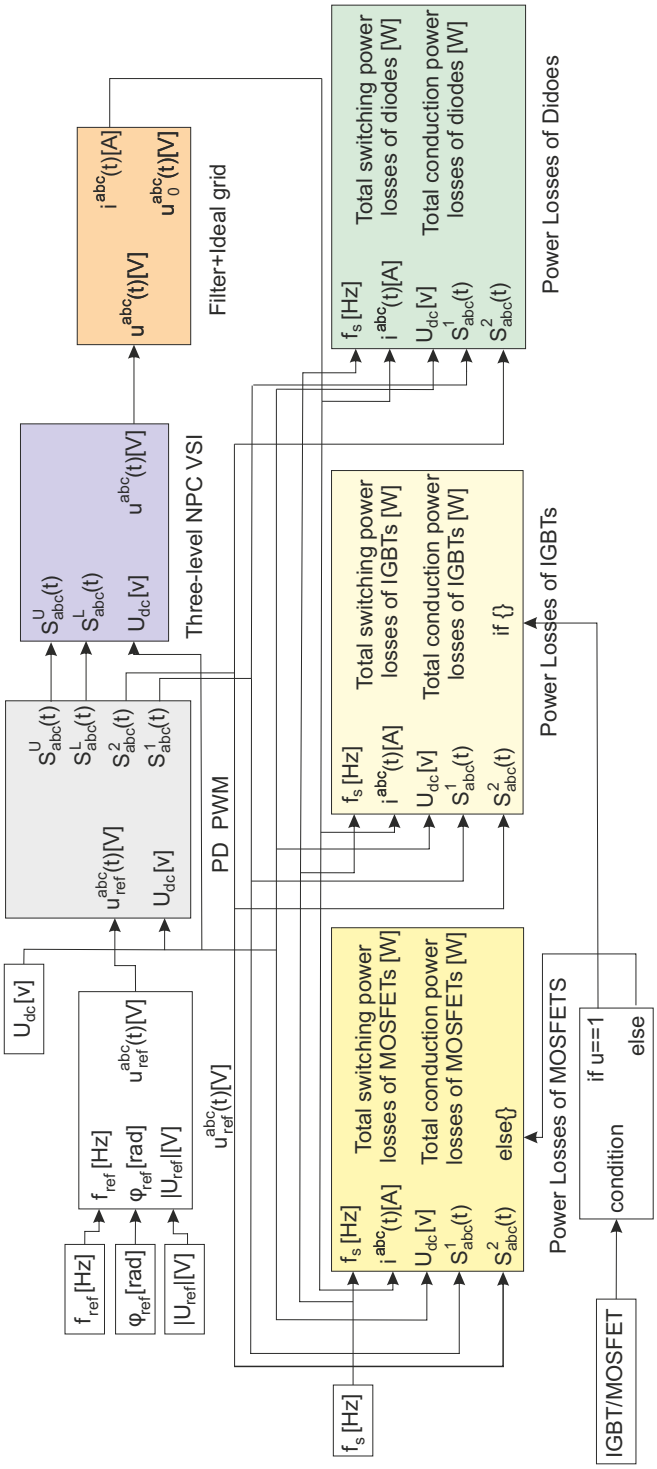


Figure 5.17: Simulation of power losses in three-level NPC VSI.

Fig. 5.17 shows the subsystems for simulation of power losses in three-level NPC VSI. As it can be seen from Fig. 5.17, the reference voltage $u^{abc}_{ref}(t)$ is generated by subsystem $u^{abc}_{ref}(t)$. This subsystem is exactly like the subsystem $u^{abc}_{ref}(t)$ in Fig. 5.2. To generate the switching vectors, we use Phase Disposition PWM (Fig. 5.18 and Fig. 5.19). $u^{abc}_{ref}(t)$ is received by subsystem $PD\ PWM$, then $S^1_{abc}(t)$ and $S^2_{abc}(t)$ are made for calculating power losses in the subsequent subsystems. Moreover, $S^U_{abc}(t)$ and $S^L_{abc}(t)$ are produced to model three-level NPC VSI by (3.47) and (3.48).

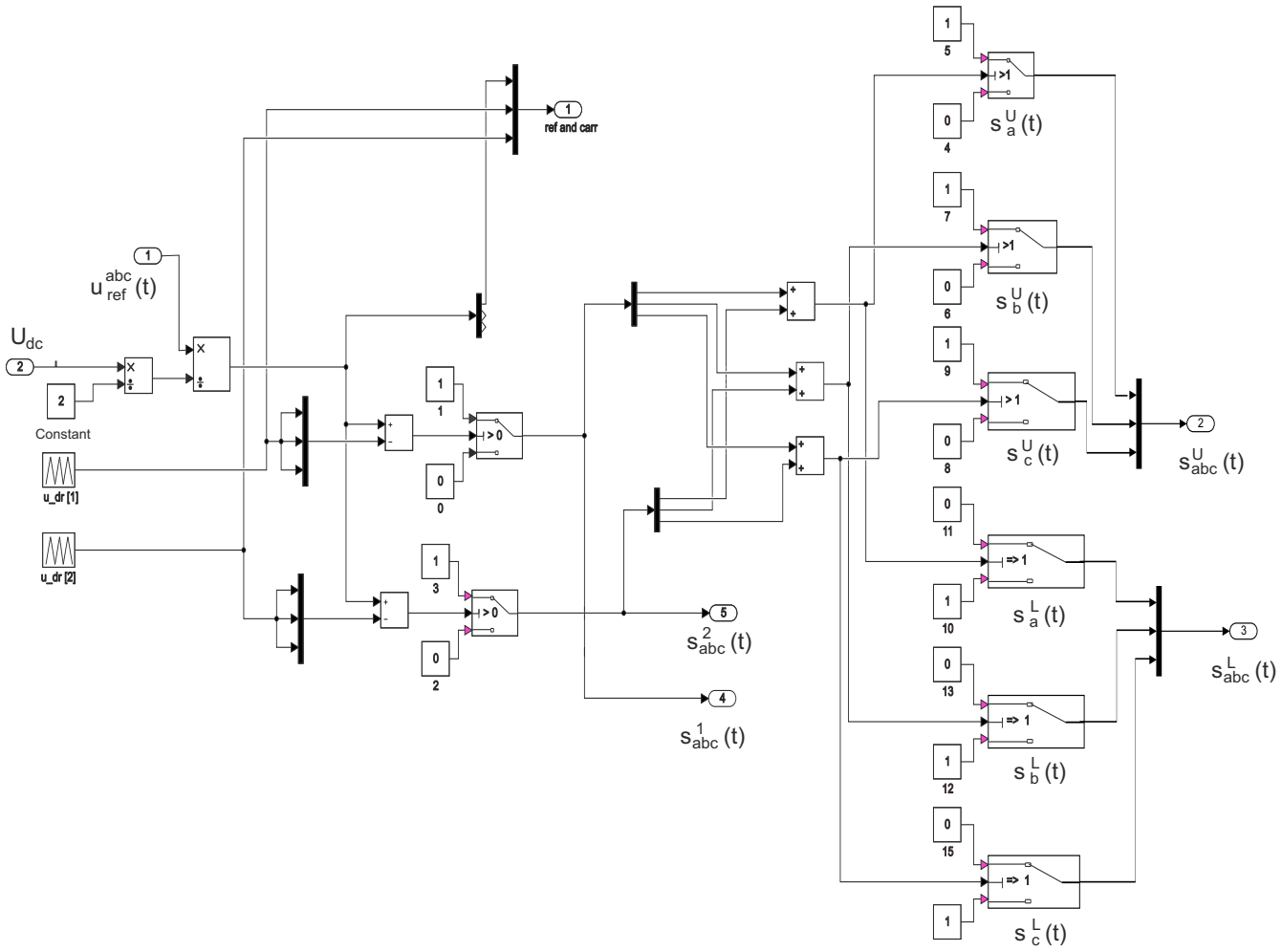


Figure 5.18: Model of PD PWM.

The subsystem $3L\ NPC\ VSI$ receives $S^U_{abc}(t)$ and $S^L_{abc}(t)$ and generates $u^{abc}(t)$ by using (3.47). Fig. 5.20 shows the model of phase voltages for three-level NPC VSI and Fig. 5.21 illustrates the line-to-line voltage $u^{ab}_{ltl}(t)$.

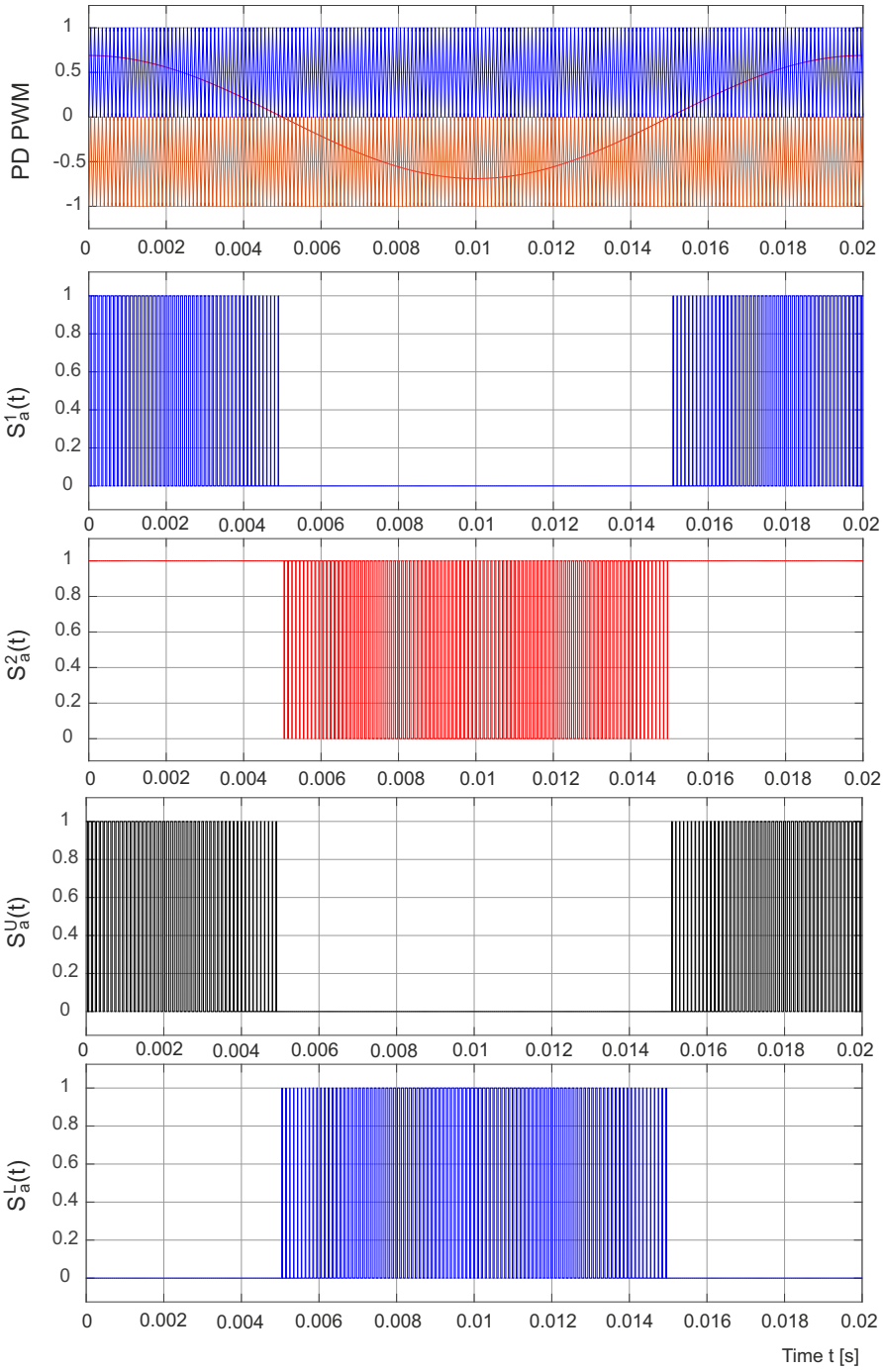


Figure 5.19: PD PWM and the switching vectors $S_a^{1,2}(t)$, $S_a^U(t)$ and $S_a^L(t)$ ($f_{ref} = 50$ $[Hz]$, $f_s = 10000$ $[Hz]$, $r_A = 0.689$, and $r_f = 200$).

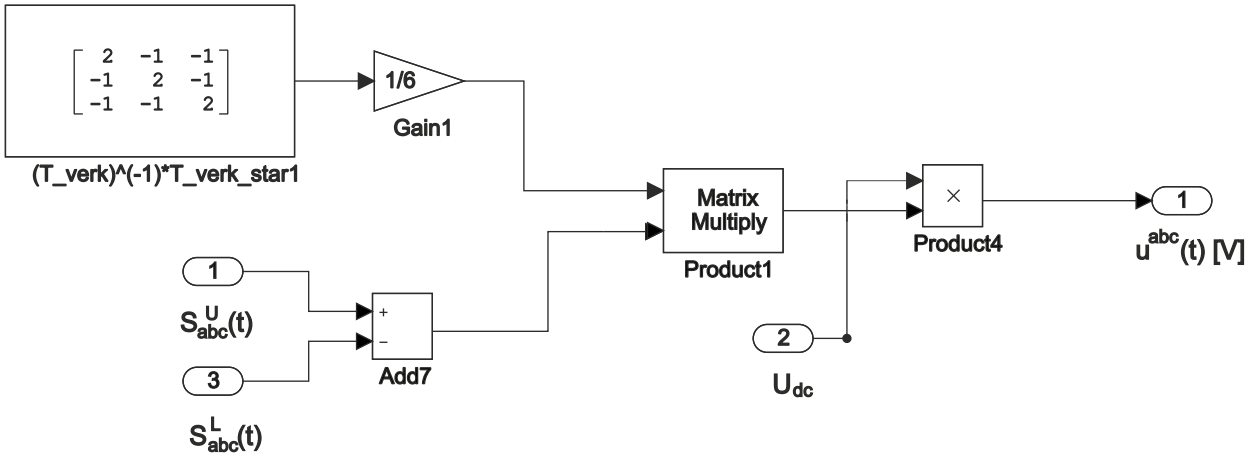


Figure 5.20: Model of phase voltages for three-level NPC VSI.

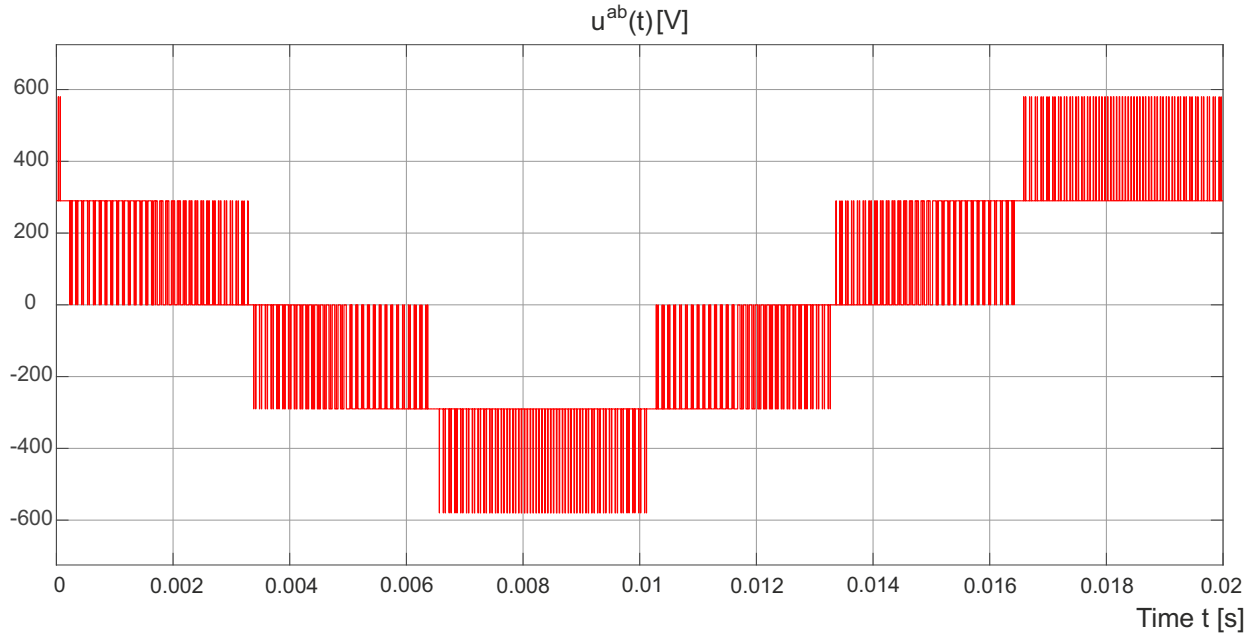


Figure 5.21: Line-to-line voltage $u_{ltl}^{ab}(t)$ in three-level NPC VSI.

The subsystem $Filter + Ideal\ grid$ gets $u^{abc}(t)$ and generates $i^{abc}(t)$. This subsystem uses the models just like the models in Fig. 5.8 and Fig. 5.9. Fig. 5.22 shows the phase voltage $u^a(t)$, the ideal phase source $u_0^a(t)$ and the phase current $i^a(t)$ respectively.

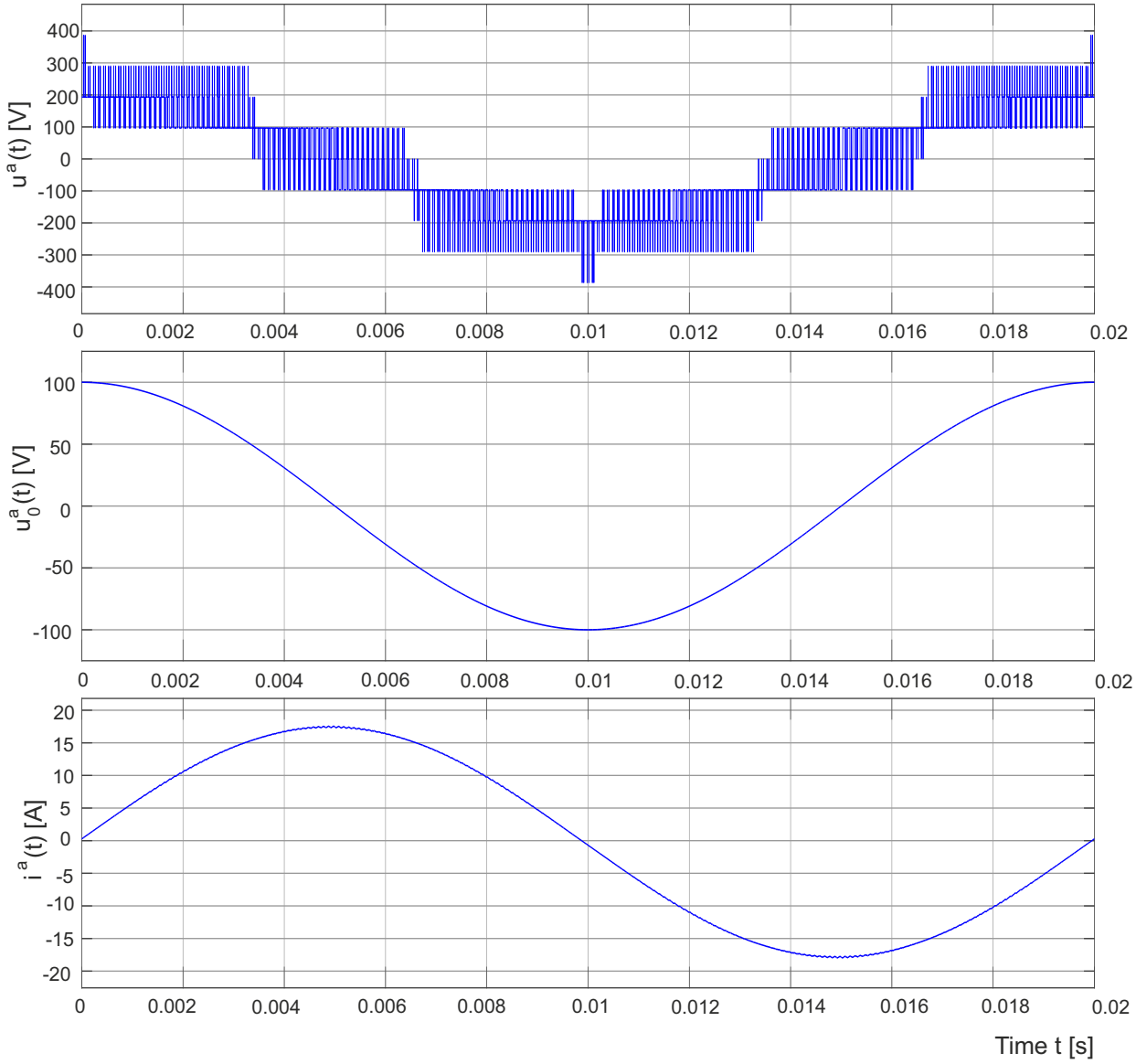


Figure 5.22: Phase voltage $u^a(t)$, the ideal phase source $u_0^a(t)$ and the phase current $i^a(t)$.

Now, we have all the parameters to calculate the power losses of the semiconductor devices. The subsystems for simulation of power losses are very similar to Fig. 5.11 and Fig. 5.13. Note that we use the parameters from Tab. 5.2 to Tab. 5.5 for simulation of the power losses.
Fig. 5.23 to Fig. 5.25 show the results of simulations.

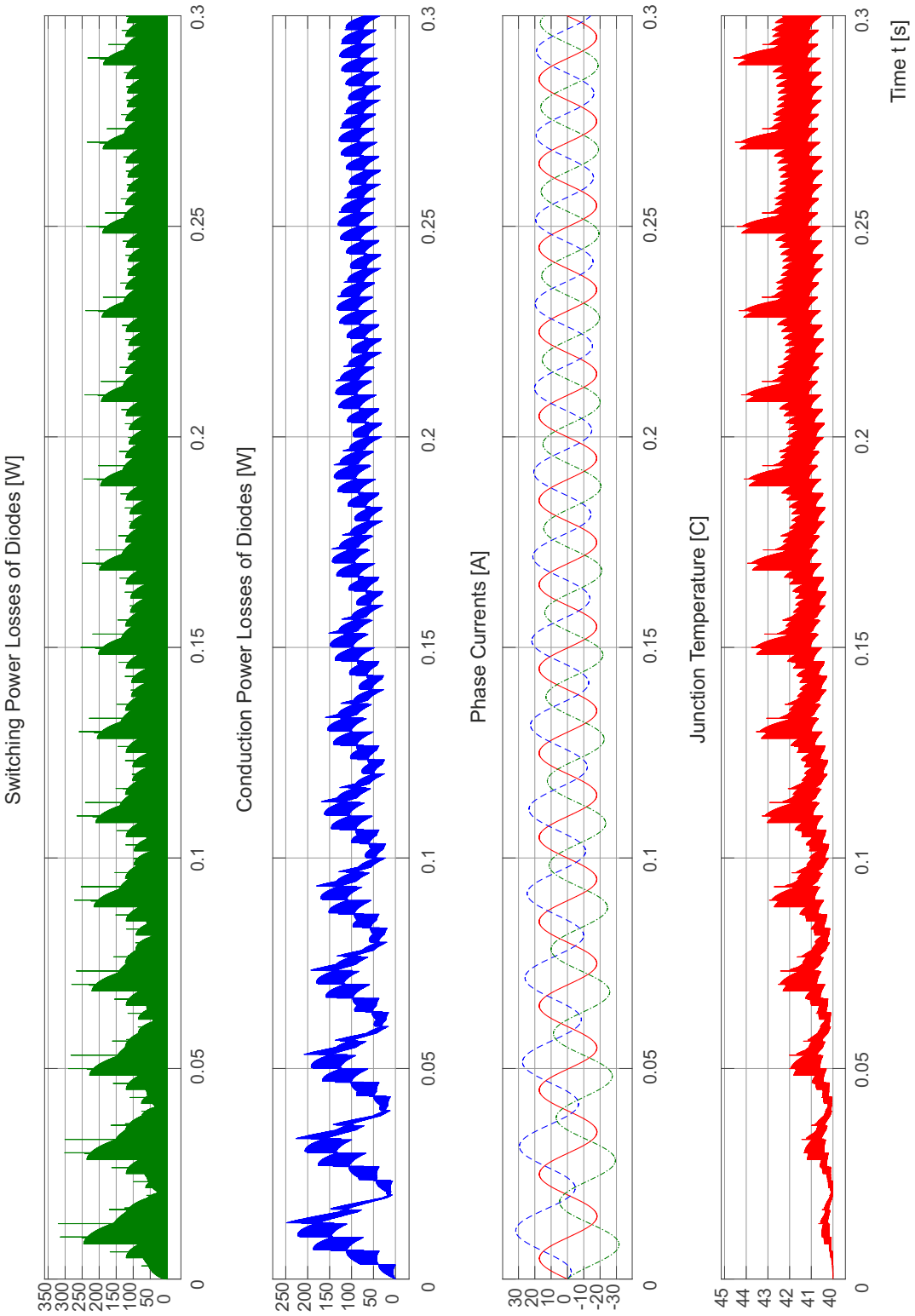


Figure 5.23: Switching and conduction power losses in all diodes, phase currents and junction temperature of diodes in three-level NPC VSI.

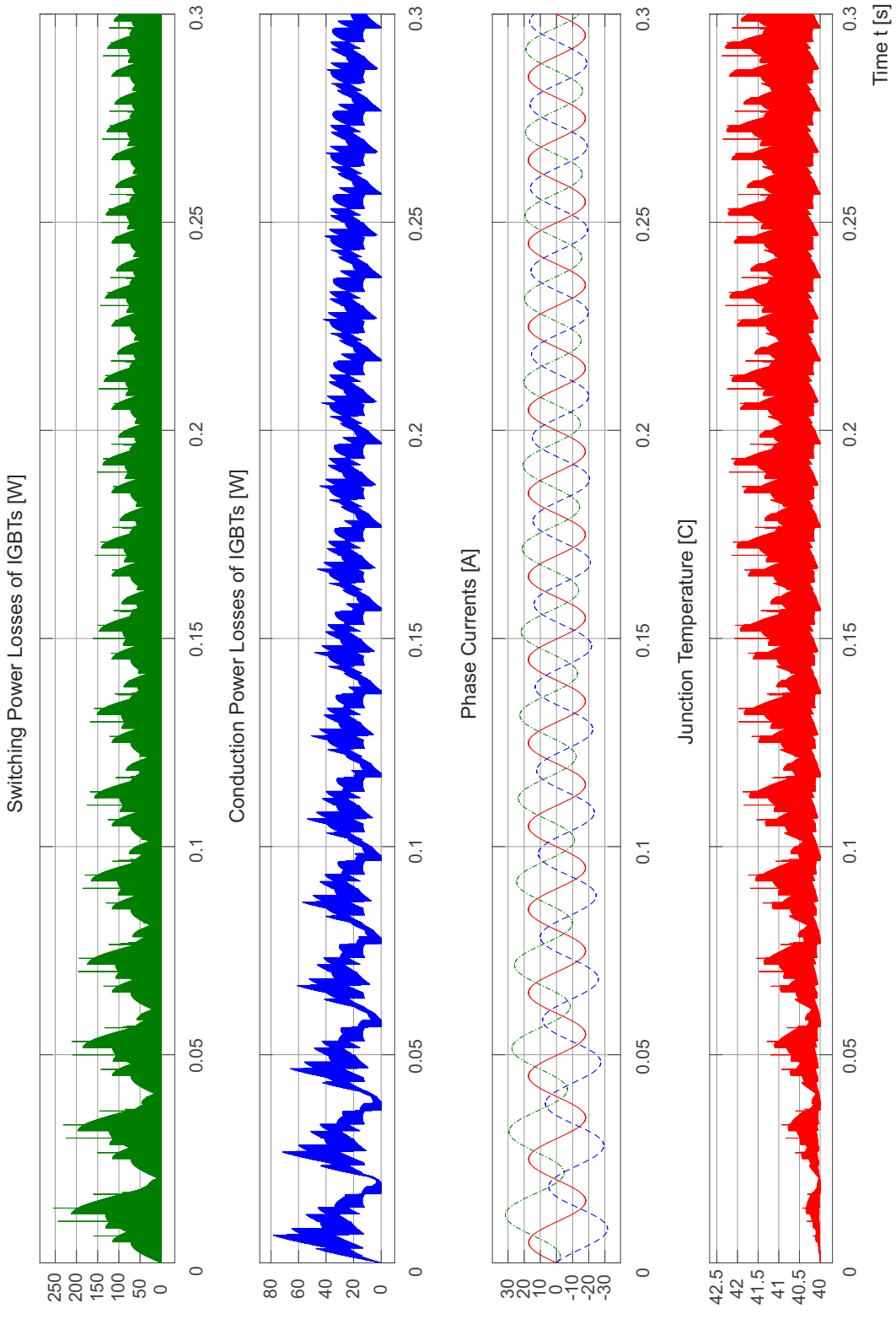


Figure 5.24: Switching and conduction power losses in all IGBTs, phase currents and junction temperature of IGBTs in three-level NPC VSI.

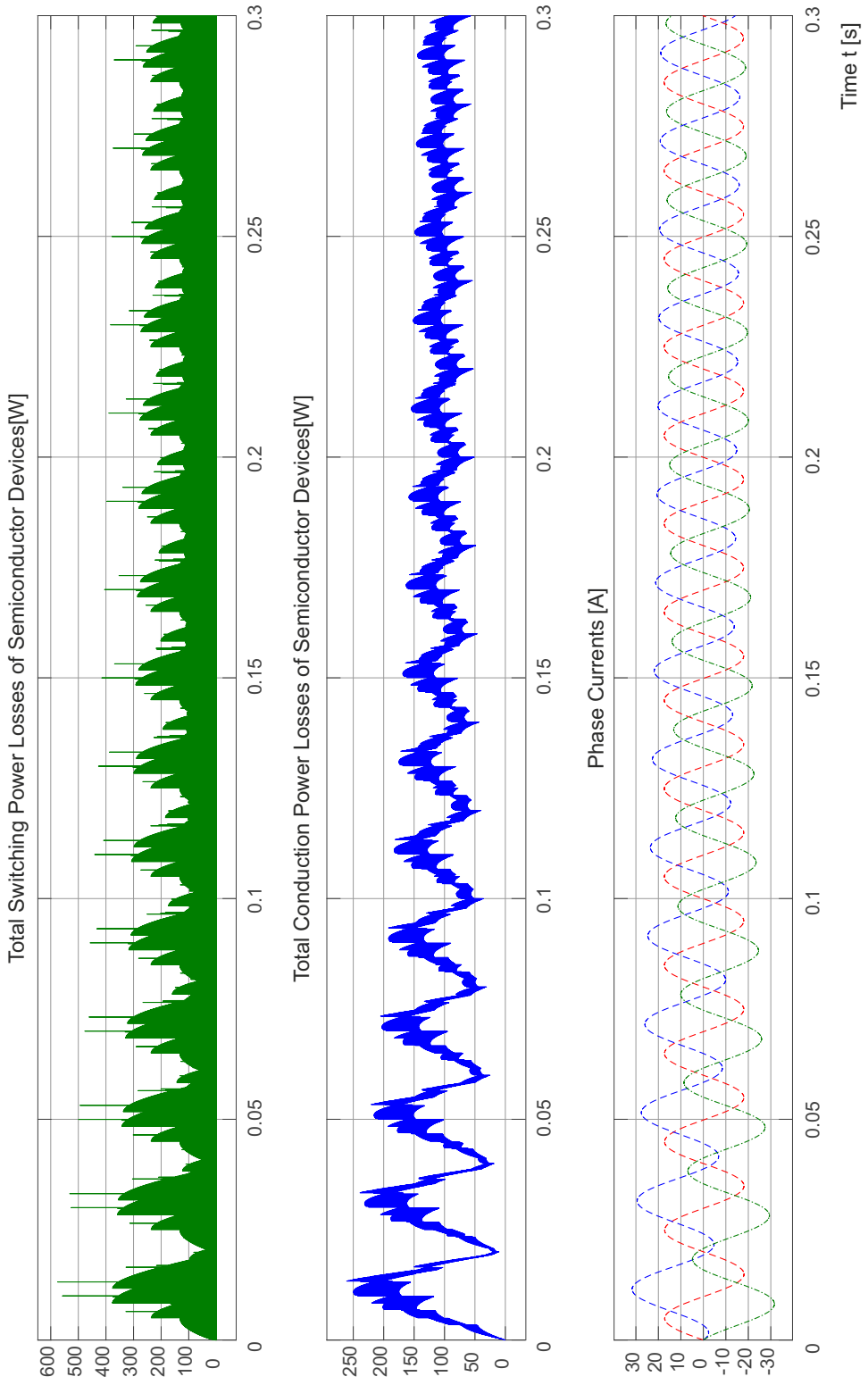


Figure 5.25: Total switching and conduction power losses in all semiconductor devices and phase currents in three-level NPC VSI.

5.3 Power Losses Comparison

In this section, the total power losses of semiconductor devices in two-level VSI are compared with the total power losses of semiconductor devices in three-level NPC VSI. For comparison, the only differences are topology of VSIs and their modulation schemes. This means that we used the same types of semiconductor devices, the same AC side, the same input reference voltages and the same switching frequency. Then, the modulation ratios r_A are changed such that the phase currents have the same amplitudes and frequencies (see Fig. 5.26).

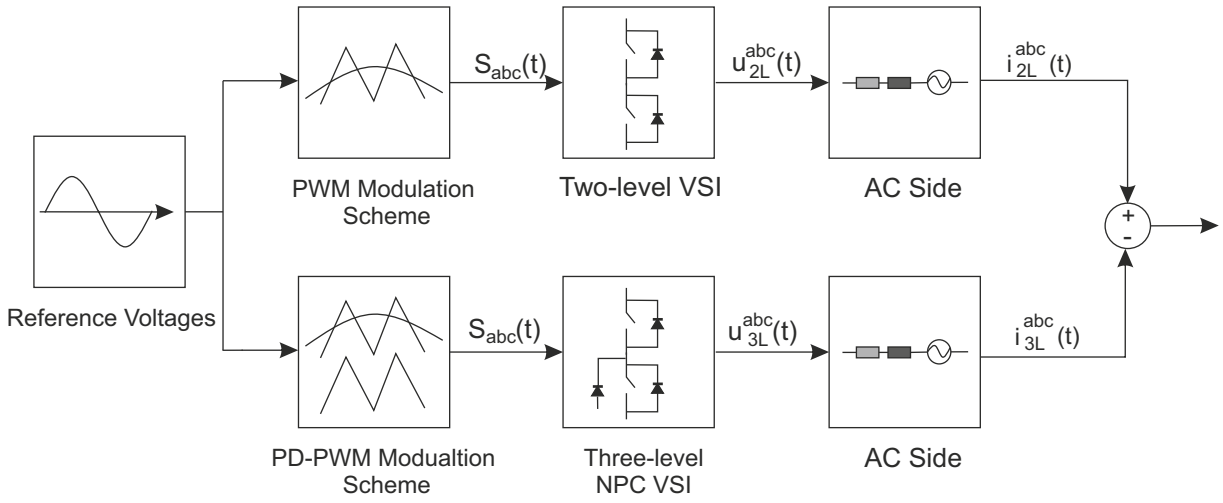


Figure 5.26: Block diagrams of power losses comparison.

Fig. 5.27 shows the total switching power for one period $T_r = 0.02$ $[s]$. Tab. 5.6 gives the values of power losses and output currents.

Parameter	value
Maximum of Switching loss	214.9 [W]
Average of Switching Losses	3.511 [W]
Maximum of Conduction Loss	87.51 [W]
Minimum of Conduction Loss	19.76 [W]
Average of Conduction Losses	52.64 [W]
Peak-to-Peak Phase Current	35.79 [A]

Table 5.6: Values of power losses and output current in Fig. 5.27.

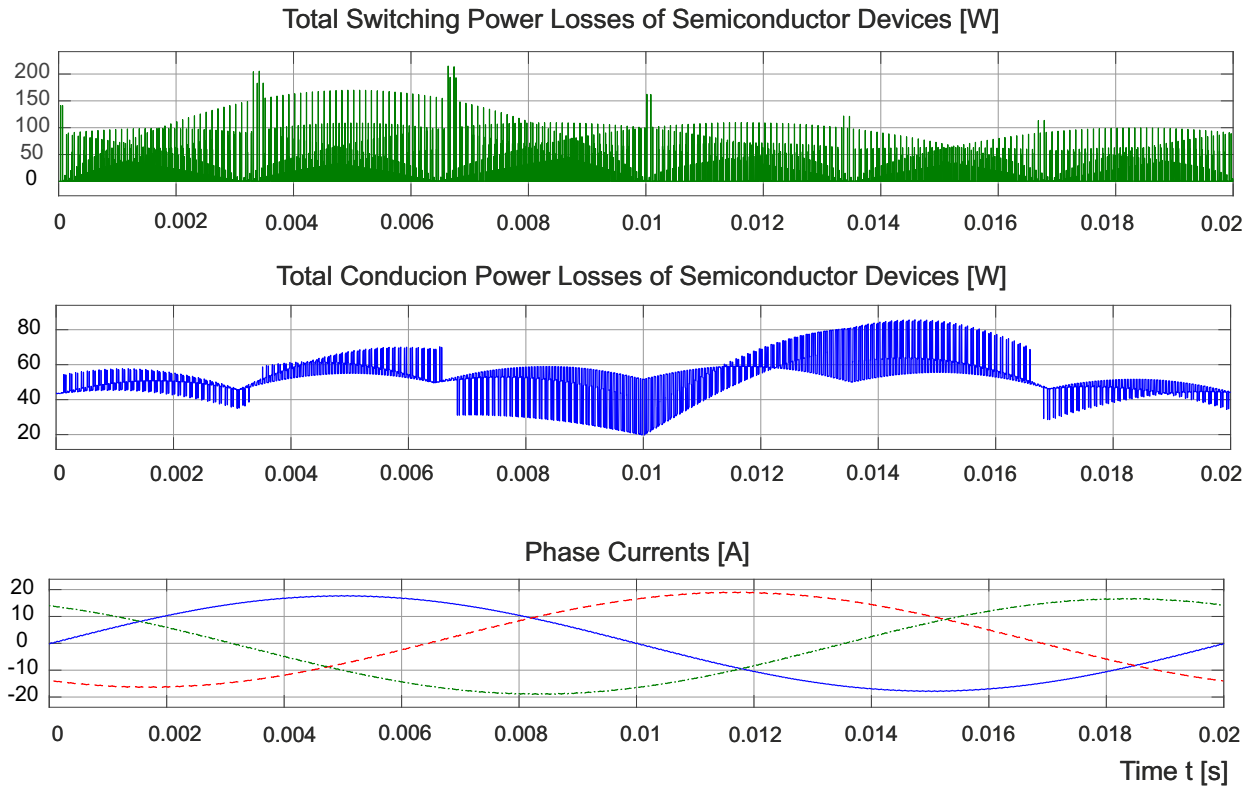


Figure 5.27: Total switching and conduction power losses and phase currents in two-level VSI for one period $T_r = 0.02$ $[s]$.

Fig. 5.28 illustrates the total switching and conduction power losses of three-level NPC VSI. as It can be seen from this figure, the power losses are periodic with the same period of reference voltages. The conduction losses are proportional to output currents. Tab. 5.7 gives the value of power losses for three-level NPC VSI.

Parameter	value
Maximum of Switching loss	370.5 [W]
Average of Switching Losses	4.332 [W]
Maximum of Conduction Loss	144.5 [W]
Minimum of Conduction Loss	57.22 [W]
Average of Conduction Losses	103.9 [W]
Peak-to-Peak Phase Current	35.51 [A]

Table 5.7: Values of power losses and output current in Fig. 5.28.

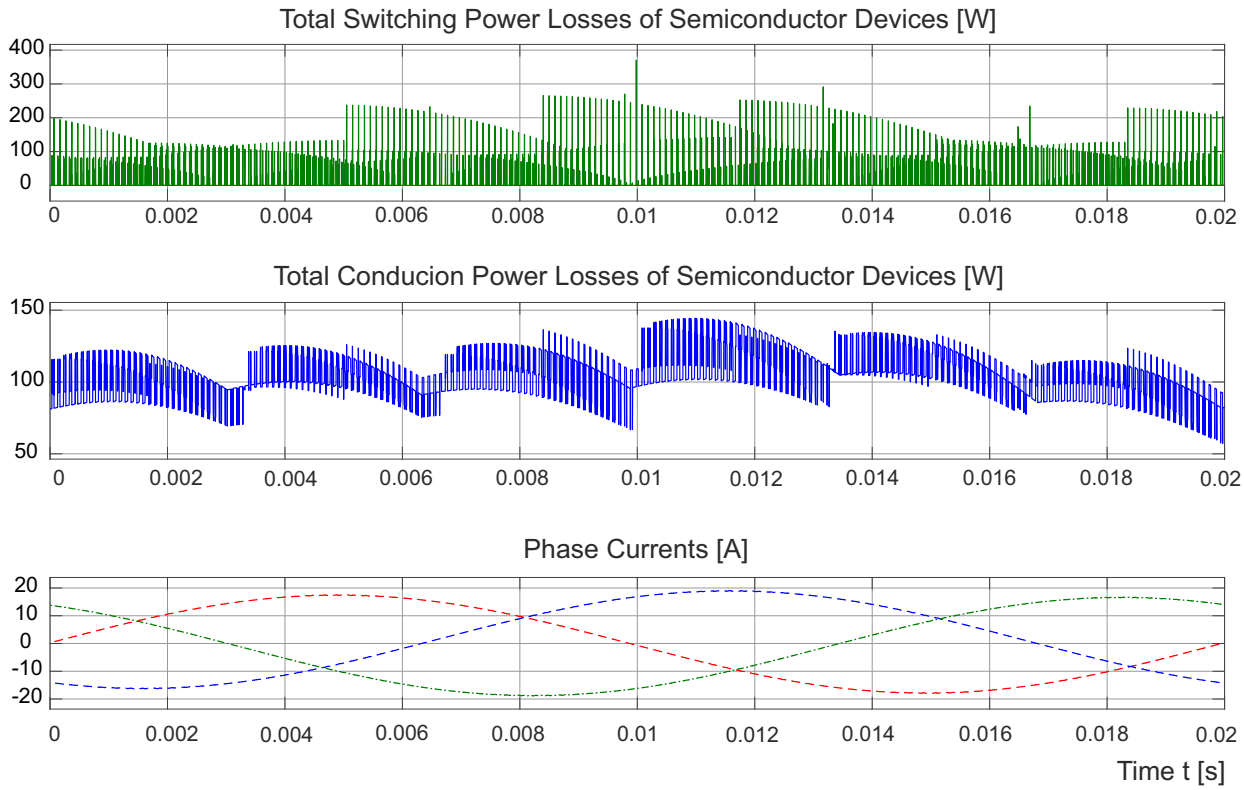


Figure 5.28: Total switching and conduction power losses and phase currents in three-level NPC VSI for one period $T_r = 0.02$ $[s]$.

As shown in Tab. 5.6 and Tab. 5.7, the conduction losses in three-level NPC VSI are doubled the conduction power losses in two-level VSI. we can explain these differences by this fact that the conduction power losses are function of phase currents and the number of semiconductor devices . The phase currents in both VSI are the same, therefore the phase currents do not effect on the conduction losses. However, the number of the semiconductor devices in three-level, that are in the path of phase currents during conduction mode, are twice the number of the semiconductor devices in two-level VSI. Thus, the conduction power losses in three-level NPC VSI are twice the conduction losses in two-level VSI.
The switching losses in the semiconductor devices are the function of the switching frequency, the reverse-bias voltage, gate resistor, number of the semiconductor devices and the junction temperature [45], [27]. The switching frequency, gate resistor and junction temperature are the same for the simulation. The reverse-bias voltage in three-level NPC VSI is half of reverse-bias voltage in two-level VSI. The number of semiconductor devices that are switched in two-level VSI vary from one semiconductor device to two semiconductor devices (see Tab. 3.3) while the number of semiconductor devices that are switched in three-level VSI change from one semiconductor device to three semiconductor devices (see Tab. 3.7). Here the effect of number of semiconductor devices prevail over the reverse-bias voltage. Therefore,

the switching losses in three-level NPC VSI are more than the switching power losses in two-level VSI.

Chapter 6

Conclusion

In this thesis, the complete models of voltage-current for semiconductor devices such as diode, MOSFET and IGBT are presented. Afterwards, two-level VSI and three-level NPC VSI are modeled based on the DC-link voltage and the switching vectors. The advantage of these models is that we can extend these model for any type of multilevel VSIs. All the researches for modeling of power losses in voltage source inverter are based on the average power losses in the inverter, while in this thesis, for the first time the instantaneous power losses are modeled. Therefore, the conduction and switching power losses at any time can be found easily for two-level VSI and three-level VSI.
The next subject in this thesis is modulation schemes. We try to improve SVM to reduce the switching power losses based on the power factor angle between the fundamental voltage and current. The main advantages of this improvement are not only reduce switching losses but also reduce THD and the variation of neutral point voltage in three-level NPC VSI. Based on all models, a comparison of power losses between two-level VSI and three-level VSI have been implemented MATLAB ® - Simulink ® (R2014b).
The simulation results indicate that if the inputs and outputs of two-level VSI and three-level NPC VSI are equal, the conduction power losses in three-level NPC VSI are approximately two times more that the conduction losses in two-level VSI. However, the switching losses in three-level VSI are also more than the switching losses in two-level VSI.

Appendix A

Junction Temperature Analysis of Semiconductor Devices

A.1 Heat Transfer

At present, power semiconductor devices have been broadly used in the power electronic applications. These applications produce losses during both the conduction and the switching modes. These semiconductor power losses are dissipated in the form of heat; therefore, the extraction of relationship between the power dissipation and the junction temperature of semiconductor devices is important. Heat energy is produced into the semiconductor devices due to the power losses. The loss is transferred to the case and then is delivered to the heat-sink and ambient environment . Fig. A.1 shows the simplified structure of a typical power semiconductor device that is mounted on a heat-sink.

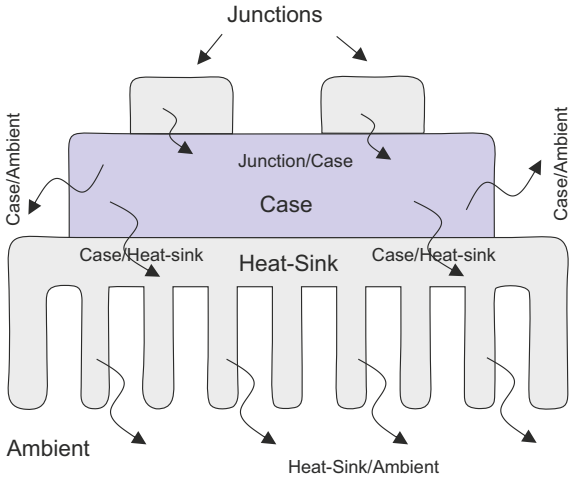


Figure A.1: Module power semiconductor device mounted on a heat-sink.

Heat energy, because of a temperature difference between the semiconductor device and the ambient, can be delivered by a combination of convection, conduction and radiation mechanisms [46]. Since operation is not in a vacuum environment, radiation has a low value compared with convection and conduction. Hence, radiation can be considered negligible [47].

In conduction mechanism, energy transfers from a high temperature object to a low temperature object through material. It forms a thermal path from a high temperature object to a low temperature object. Conduction heat transfer through a homogeneous solid, from Fourier's law, can be given by

$$p_{conduction}(t) = \frac{\lambda}{l} A \left(\vartheta(t_2) - \vartheta(t_1)\right). \tag{A.1}$$

where $p_{conduction}(t)$ $[W]$ is conduction heat transfer , $\vartheta(t_2)$ $[K]$ and $\vartheta(t_1)$ $[K]$ are the temperature of the hotter object and the cooler object respectively, λ $[\frac{W}{mK}]$ is thermal conductivity that is the property of a material to conduct heat, l $[m]$ is material thickness and A $[m^2]$ is heat transfer area .

When the temperature of a fluid flowing over an object differs from that of the surface of object, convection heat transfer occurs by the movement of fluid. Convection heat transfer through a fluid is given by Newton's law, that is

$$p_{convection}(t) = hA \left(\vartheta(t_2) - \vartheta(t_1)\right). \tag{A.2}$$

where $p_{CConvection}(t)$ $[W]$ heat transferred by convection , h $[\frac{W}{m^2K}]$ is the convection heat exchange coefficient , A $[m^2]$ is heat transfer area and $\vartheta(t_2)$ $[K]$ and $\vartheta(t_1)$ $[K]$ are the temperature of the hotter object and the cooler object respectively.
In total, the heat energy is delivered to the cooler object by combination of convection and conduction is given by:

$$p_{convection+conduction}(t) = \left(\vartheta_h(t) - \vartheta_c(t)\right)\left(\frac{\lambda}{l} + h\right)A. \tag{A.3}$$

A.2 Junction Temperature

Principle of conversion of energy can be used to find junction temperature of semiconductor devices based on the power dissipation. This principle says that the dissipation energy during the interval time of dt is equal to the energy stored into the semiconductor device in addition to the energy delivered to the case. Energy can be only delivered from the semiconductor device to the surrounding environment by the conduction heat transfer of junction-case. The energy stored into the switches is given by

$$p_{stored}(t)\, dt = m_J c_J d\vartheta_J(t). \tag{A.4}$$

where $p_{stored}(t)$ $[W]$ is the power stored into junction during the time interval dt, m_J $[Kg]$ is the mass of the semiconductor device, c_J $[\frac{J}{kgK}]$ is the specific heat coefficient of the junction, dt $[s]$ is the time required to heat up the junction and $d\vartheta_J(t)$ $[K]$ is the variation of the junction temperature during dt .

The energy delivered to the case from the junction is given by:

$$p_{delivered}(t)\,dt = \frac{\lambda}{l_J} A_J \left(\vartheta_J(t) - \vartheta_C(t)\right). \tag{A.5}$$

where $p_{delivered}(t)$ $[W]$ is the power stored into junction during the time interval dt , $\vartheta_J(t)$ $[K]$ and $\vartheta_C(t)$ $[K]$ are the temperature of the junction and case respectively, λ $[\frac{W}{mK}]$ is thermal conductivity that is the property of a material to conduct heat, l_J $[m]$ is junction thickness and A_J $[m^2]$ is heat transfer area of junction .

Finally, the principle of conversion of energy says

$$p_{dissipation}(t)\,dt = \frac{\lambda}{l_J} A_J \left(\vartheta_J(t) - \vartheta_C(t)\right) + m_J c_J d\vartheta_J(t). \tag{A.6}$$

(A.6) can be solved by taking three assumptions
(A1). Ambient temperature is constant $(\vartheta_a(t) = \vartheta_a)$.
(A2). The case and the heat-sink are very close to each other $(\vartheta_C(t) = \vartheta_{hs}(t))$.
(A3). The heat-sink thermal's capacity is so high, therefore, $(\vartheta_{hs}(t) = \vartheta_a)$;.
If new variables are defined as

1-Thermal capacitance of junction C_J $[\frac{J}{mK}]$

$$C_J := m_J c_J, \tag{A.7}$$

2-Thermal conduction of junction G_J $[\frac{W}{mK}]$

$$G_J := \frac{\lambda}{l_J} A_J. \tag{A.8}$$

and if the assumptions are applied

$$\left(\vartheta_J(t) - \vartheta_C(t)\right) \equiv \vartheta_{JC}(t) = \vartheta_{Ja}(t), \tag{A.9}$$

and,

$$\frac{d\left(\vartheta_J(t)\right)}{dt} = \frac{d\left(\vartheta_J(t) - \vartheta_a\right)}{dt} \equiv \frac{d\left(\vartheta_{Ja}(t)\right)}{dt}. \tag{A.10}$$

Then (A.6) turns into

$$p_{dissipation}(t) = C_J \frac{d\left(\vartheta_{Ja}(t)\right)}{dt} + G_J \vartheta_{Ja}(t). \tag{A.11}$$

(A.11) is the first order differential equation that has both private answer and homogeneous answer. The complete answer is

$$\vartheta_{Ja}(t) = \left(\vartheta_{Ja}(0) - \frac{p_{dissipation}(t)}{G_J}\right) e^{\frac{-t}{\tau_J}} + \frac{p_{dissipation}(t)}{G_J}. \tag{A.12}$$

where $\vartheta_{Ja}(0)$ $[k]$ is the initial value of the $\vartheta_{Ja}(t)$ and τ_J $[s]$ is the time constant defined by

$$\tau_J := \frac{C_J}{G_J}. \tag{A.13}$$

The relationship between the junction temperature and the power losses therefore is given by

$$\vartheta_J(t) = \left(\vartheta_{Ja}(0) - \frac{p_{dissipation}(t)}{G_J}\right) e^{\frac{-t}{\tau_J}} + \frac{p_{dissipation}(t)}{G_J} + \vartheta_a. \tag{A.14}$$

(A.14) can be used in chapter two to correlate the power losses in the semiconductor devices with the junction temperature.

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