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Applications of Resistor-Transistor Logic in Hybrid Graphene-CMOS Digital Circuits

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Abstract

Graphene is one of the most investigated two-dimensional materials of the last decade. Due to its large carrier mobility and saturation velocity, it has been intensively studied as a potential replacement for Si in electronics. Indeed, the scaling of Si devices is reaching its limits and the search for new materials and architectures is underway. However, there are many obstacles in the application of graphene in electronics. Most importantly, graphene does not have a bandgap and, consequently, graphene field-effect transistors (GFETs) cannot be turned off. This prevents the application of GFETs in digital electronics because GFETs always dissipate static power, in contrast to Si transistors in complementary metal-oxide-semiconductor (CMOS) technology. On the other hand, GFETs have some advantages over Si transistors. One of them is the ambipolar electric field-effect: a GFET can behave either as a n-doped or a p-doped transistor, depending on its biasing. This property allows to simplify the design of logic gates traditionally used in Si transistor technology. Such logic gates can be used together with conventional Si CMOS logic gates to realize hybrid graphene-CMOS circuits which would be more complex if realized only in Si CMOS technology. The aim of this thesis, which was done at the L-NESS Como, is to demonstrate the operation of two hybrid graphene-CMOS circuits. After a brief introduction on graphene and its applications in digital electronics, the main text describes the graphene resistor-transistor logic gates and the fabrication and characterization of the two hybrid circuits. The first circuit is a single-dual edge triggered flip-flop realized with a few components. Depending on the input control bit, it works either as a single or dual edge triggered flip-flop. The second circuit is an astable oscillator that consists only of a Si CMOS latch and a GFET. It can be employed as a voltage controlled oscillator and pulse width modulator. These circuits represent two examples of how the ambipolarity of graphene can be successfully combined with the reliability of Si CMOS to realize very efficient hybrid electronic circuits.

Abstract

Il grafene è uno dei materiali bidimensionali più studiati degli ultimi anni: infatti, grazie alle sue incredibili proprietà elettroniche, tra cui mobilità dei portatori e velocità di saturazione, è stato considerato come un potenziale sostituto al silicio in elettronica. Infatti, la riduzione delle dimensioni dei dispositivi elettronici sta raggiungendo i suoi limiti e la necessità di nuovi materiali diventa sempre più incalzante. Tuttavia, il grafene presenta molti problemi, tra cui l'assenza di un bandgap di energia. Infatti, i transistor in grafene (GFETs) non possono essere spenti e questo rende impossibile un loro utilizzo nell'elettronica digitale, a causa della potenza statica dissipata, che è invece idealmente nulla nei transistor in silicio. Ad ogni modo, l'assenza di un bandgap presenta anche alcuni vantaggi. Uno di questi è la conduzione ambipolare: un GFET può comportarsi alternativamente come un transistor drogato n o p, in base alla tensione di bias. Questa proprietà permette di progettare una nuova porta logica che potrebbe essere usata per realizzare circuiti ibridi grafene-CMOS che presentano nuove funzionalità, le quali necessiterebbero di circuiti molto più complessi se realizzati solo con transistor al silicio. Lo scopo di questa tesi, condotta presso L-NESS Como, è la dimostrazione di due di questi circuiti ibridi. Dopo una breve introduzione sul grafene e le sue applicazioni nell'elettronica digitale, il testo principale descriverà la nuova porta logica in grafene e la fabbricazione e caratterizzazione dei due circuiti ibridi. Il primo circuito è un single-dual edge triggered flip-flop che, in base al valore di un input di controllo, commuta stato su una o su entrambe le transizioni di stato del segnale di clock. Il secondo circuito è un oscillatore astabile realizzato impiegando esclusivamente un GFET e un latch Si CMOS e i cui duty-cycle e frequenza possono essere controllati in tensione. Questi circuiti rappresentano due esempi di come l'ambipolarità del grafene può essere unita con l'affidabilità del silicio per realizzare circuiti ibridi più efficienti.

Chapter 1

Introduction to Graphene

Currently, transistors employed in the realization of processors and memories are realized with semiconductors, in particular silicon. During the years, there has been a continuous attempt to reduce the dimensions of silicon metal-oxide semiconductor field-effect transistors (MOSFET) in order to improve their properties in terms of speed and power consumption. However, a further scaling of the devices is becoming impossible since the physical limits resulting from short-channel effects, parasitisms and fluctuations in doping are becoming more difficult to overcome. Graphene, thanks to its impressive properties has attracted a great deal of attention as a possible substitute for silicon [1][2]. However, as it will be explained in this chapter, there are some problems that seems to preclude the possibility of any application of graphene in digital logic. After a brief introduction on graphene and a description of its properties and peculiarities, the GFET will be presented and compared to silicon field-effect transistors (FET). Then the graphene resistor-transistor logic (GRTL) gate will be introduced, which is the basis of the hybrid circuits described in the following chapters. Finally, the fabrication processes adopted and the electrical characterization of the devices will be briefly described.

1.1 Overview

Graphene is a two-dimensional crystal that consists of carbon atoms arranged in a planar hexagonal lattice and that exhibits supreme properties, such as very high carrier mobility (over 100 000 $cm^2V^{-1}s^{-1}$ [3, 4]), high thermal conductivity (over 3000 W/mK [5]) or the ability to sustain high density of electric current [6]. This wide range of properties is a result of the peculiar band structure of graphene, which can be calculated with a tight binding approach starting from the atomic orbitals of the carbon atoms [7]. The hexagonal structure of graphene can be seen as a Bravais triangular lattice with a basis consisting of two carbon atoms, or, similarly, as the composition of two triangular sublattices, as in Fig. 1.1. If one atom (in light blue, lattice A) is placed in the origin, the other atom of the basis (in yellow, lattice B) will be at $\boldsymbol{u} = a(0, 1)$, where $a = 0.142$ nm is the minimum

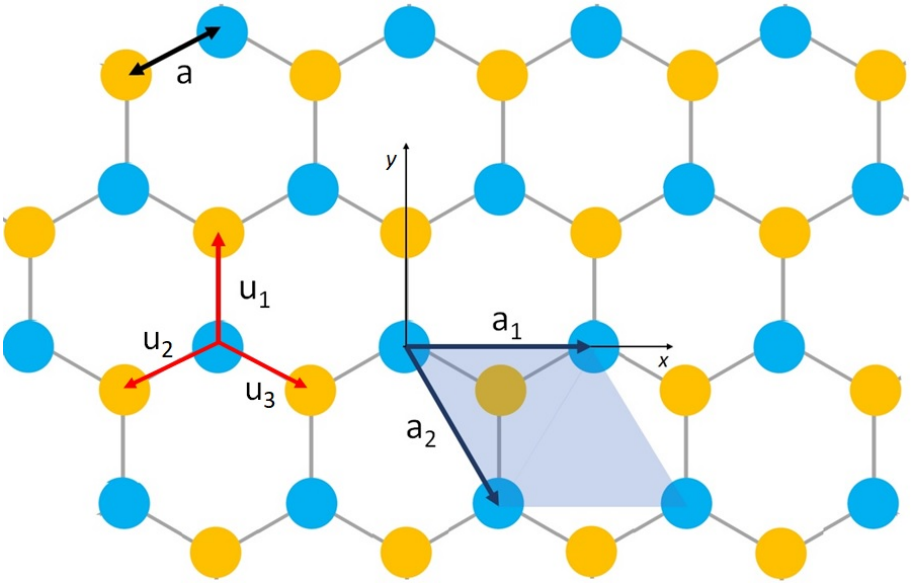


Figure 1.1: Graphene hexagonal lattice: the unit cell in the blue shaded area contains 2 carbon atoms, coming from the two different triangular Bravais lattices, depicted in two different colors. The basis vectors are called $\boldsymbol{a}_1$ and $\boldsymbol{a}_2$, the distance between two neighboring carbon atoms is $a = 0.142$ nm. The closest neighbors of a carbon atom belong to the other sublattice and are separated from the former by the 3 vectors $\boldsymbol{u}_1$, $\boldsymbol{u}_2$ and $\boldsymbol{u}_3$. Adapted from [8].

distance between two carbon atom. One of the possibilities for the choice of the basis vectors is the following:

$$\boldsymbol{a}_1 = a\sqrt{3}\,(1,0) \qquad \boldsymbol{a}_2 = a\sqrt{3}\left(\frac{1}{2}, -\frac{\sqrt{3}}{2}\right) \tag{1.1}$$

The electronic structure of each carbon atom is $1s^2 2s^2 2p^4$. The $1s$ orbital is fully occupied, whereas the $2s$ and $2p$ orbitals show a sp^2 hybridization: the three resulting sp^2 orbitals form three planar σ bonds at low energy, fully occupied, and three σ^* anti-bonds, completely empty, at high energy. These bonds are separated by 120° angles and hence form the graphene honeycomb structure. The pure p_z orbital, on the contrary, is perpendicular to the plane and is occupied by one electron. The valence and conduction bands of graphene are obtained with a tight binding approach starting from these p_z orbitals. Since the honeycomb structure can be built with a triangular lattice with a basis of two carbon atoms. For this reason, the general wave function of the electrons in the valence or conduction band will be a linear combination over all the lattice sites of the p_z orbitals of the

two basis carbon atoms, $|\phi_{\mathrm{A}}(\boldsymbol{r})\rangle$ and $|\phi_{\mathrm{B}}(\boldsymbol{r})\rangle$:

$$\begin{aligned} |\Psi(\boldsymbol{k},\boldsymbol{r})\rangle = &\sum_i \psi_{\mathrm{A}}(\boldsymbol{k}) e^{j\boldsymbol{k}\boldsymbol{r}_{\mathrm{A}i}} |\phi_{\mathrm{A}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{A}i})\rangle \\ &+ \sum_i \psi_{\mathrm{B}}(\boldsymbol{k}) e^{j\boldsymbol{k}\boldsymbol{r}_{\mathrm{B}i}} |\phi_{\mathrm{B}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{B}i})\rangle \end{aligned} \tag{1.2}$$

where the first sum is over lattice A, whose carbon atoms are at $\boldsymbol{r}_{\mathrm{A}i}$, and the second sum is over the lattice B, whose atoms are at $\boldsymbol{r}_{\mathrm{B}i}$. Substituting this formula in the Schrodinger's time-independent equation and multiplying by $\langle\phi_{\mathrm{A}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{A}})|$, it is possible to obtain:

$$\begin{aligned} &\psi_{\mathrm{A}}(\boldsymbol{k}) \sum_i e^{j\boldsymbol{k}\boldsymbol{r}_{\mathrm{A}i}} \langle\phi_{\mathrm{A}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{A}})| H |\phi_{\mathrm{A}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{A}i})\rangle + \\ &+ \psi_{\mathrm{B}}(\boldsymbol{k}) \sum_i e^{j\boldsymbol{k}\boldsymbol{r}_{\mathrm{B}i}} \langle\phi_{\mathrm{A}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{A}})| H |\phi_{\mathrm{B}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{Bi}})\rangle = \\ &= E(\boldsymbol{k})(\psi_{\mathrm{A}}(\boldsymbol{k}) \sum_i e^{j\boldsymbol{k}\boldsymbol{r}_{\mathrm{A}i}} \langle\phi_{\mathrm{A}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{A}})|\phi_{\mathrm{A}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{A}i})\rangle + \\ &+ \psi_{\mathrm{B}}(\boldsymbol{k}) \sum_i e^{j\boldsymbol{k}\boldsymbol{r}_{\mathrm{B}i}} \langle\phi_{\mathrm{A}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{A}})|\phi_{\mathrm{B}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{B}i})\rangle) \end{aligned} \tag{1.3}$$

In the hypothesis that we can neglect the braket between two different sites and we can consider only the matrix elements between closest neighbors, as in a tight binding approach, we get:

$$\psi_{\mathrm{B}}(\boldsymbol{k}) \sum_{i=1}^{3} e^{j\boldsymbol{k}\boldsymbol{r}_{\mathrm{B}i}} \langle\phi_{\mathrm{A}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{A}})| H |\phi_{\mathrm{B}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{B}i})\rangle = E(\boldsymbol{k})\psi_{\mathrm{A}}(\boldsymbol{k}) e^{j\boldsymbol{k}\boldsymbol{r}_{\mathrm{A}}} \tag{1.4}$$

The sum is, as it has been said, over the closest neighbors of the atom with coordinate $\boldsymbol{r}$. As it is possible to see in Fig. 1.1, the closest neighbors of a given atom are the three atoms of the complementary lattice that surround it. The coordinates of these atoms are:

$$\begin{aligned} \boldsymbol{u}_1 &= a\,(0,1) \\ \boldsymbol{u}_2 &= a\left(-\frac{\sqrt{3}}{2}, -\frac{1}{2}\right) \\ \boldsymbol{u}_3 &= a\left(\frac{\sqrt{3}}{2}, -\frac{1}{2}\right) \end{aligned} \tag{1.5}$$

If we define:

$$\begin{aligned} f(\boldsymbol{k}) &= \sum_{i=3}^{3} e^{j\boldsymbol{k}\boldsymbol{u}_i} \\ \gamma &= -\langle\phi_{\mathrm{A}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{A}})| H |\phi_{\mathrm{B}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{B}i})\rangle \end{aligned} \tag{1.6}$$

we get:

$$-\gamma f(\boldsymbol{k})\psi_{\mathrm{B}}(\boldsymbol{k}) = E(\boldsymbol{k})\psi_{\mathrm{A}}(\boldsymbol{k}) \tag{1.7}$$

If the Schrodinger's equation in 1.2 were multiplied by $\langle\psi_{\mathrm{B}}(\boldsymbol{r}-\boldsymbol{r}_{\mathrm{B}})|$, we would get:

$$-\gamma f^{*}(\boldsymbol{k})\psi_{\mathrm{A}}(\boldsymbol{k}) = E(\boldsymbol{k})\psi_{\mathrm{B}}(\boldsymbol{k}) \tag{1.8}$$

The two equations 1.7 and 1.8 can be rearranged in matrix form:

$$\begin{bmatrix} 0 & -\gamma f(\boldsymbol{k}) \\ -\gamma f^{*}(\boldsymbol{k}) & 0 \end{bmatrix} \begin{bmatrix} \psi_{\mathrm{A}}(\boldsymbol{k}) \\ \psi_{\mathrm{B}}(\boldsymbol{k}) \end{bmatrix} = E(\boldsymbol{k}) \begin{bmatrix} \psi_{\mathrm{A}}(\boldsymbol{k}) \\ \psi_{\mathrm{B}}(\boldsymbol{k}) \end{bmatrix} \tag{1.9}$$

which can be written as:

$$H(\boldsymbol{k})\Psi(\boldsymbol{k}) = E(\boldsymbol{k})\Psi(\boldsymbol{k}) \tag{1.10}$$

The solution of this eigenequation, which describes the relation between the energy of the bands and the wavavector $\boldsymbol{k}$, called also dispersion relation, is:

$$E(\boldsymbol{k}) = \pm\gamma|f(\boldsymbol{k})| \tag{1.11}$$

where:

$$|f(\boldsymbol{k})| = \sqrt{3 + 2\cos(\sqrt{3}\mathrm{k_x}) + 4\cos\left(\frac{3}{2}\mathrm{ak_y}\right)\cos\left(\frac{\sqrt{3}}{2}\mathrm{ak_x}\right)} \tag{1.12}$$

The dispersion relation together with the reciprocal lattice and the first Brillouin zone is shown in Fig. 1.2. As it can be seen, the π and π^{*} bands (the valence and conduction bands respectively) touch at the Dirac points. Since every carbon atom contributes with one electron, at 0 K the valence band is completely filled, while the conduction band is empty. Furthermore, the dispersion relation in the neighborhood of these points is linear. In fact, expanding in Taylor series, it is possible to show that:

$$|f(\boldsymbol{k})| = \frac{3}{2}a|\boldsymbol{q}| \tag{1.13}$$

where $\boldsymbol{q} = \boldsymbol{k} - \boldsymbol{K}$. Thus:

$$E(\boldsymbol{k}) = \pm\gamma|f(\boldsymbol{k})| = \pm\gamma\frac{3}{2}a|\boldsymbol{q}| = \pm v_{\mathrm{F}}\hbar q \tag{1.14}$$

where $v_{\mathrm{F}} = \frac{3a\gamma}{2\hbar}$. Finally, considering a degeneracy factor of four, coming from the spin and from the K-K' degeneracy, the density of states (DOS) of graphene around the Dirac points is:

$$DOS(E) = \frac{2}{\pi}q\frac{1}{\hbar v_{\mathrm{F}}} = \frac{2}{\pi}\frac{|E|}{(\hbar v_{\mathrm{F}})^2} \tag{1.15}$$

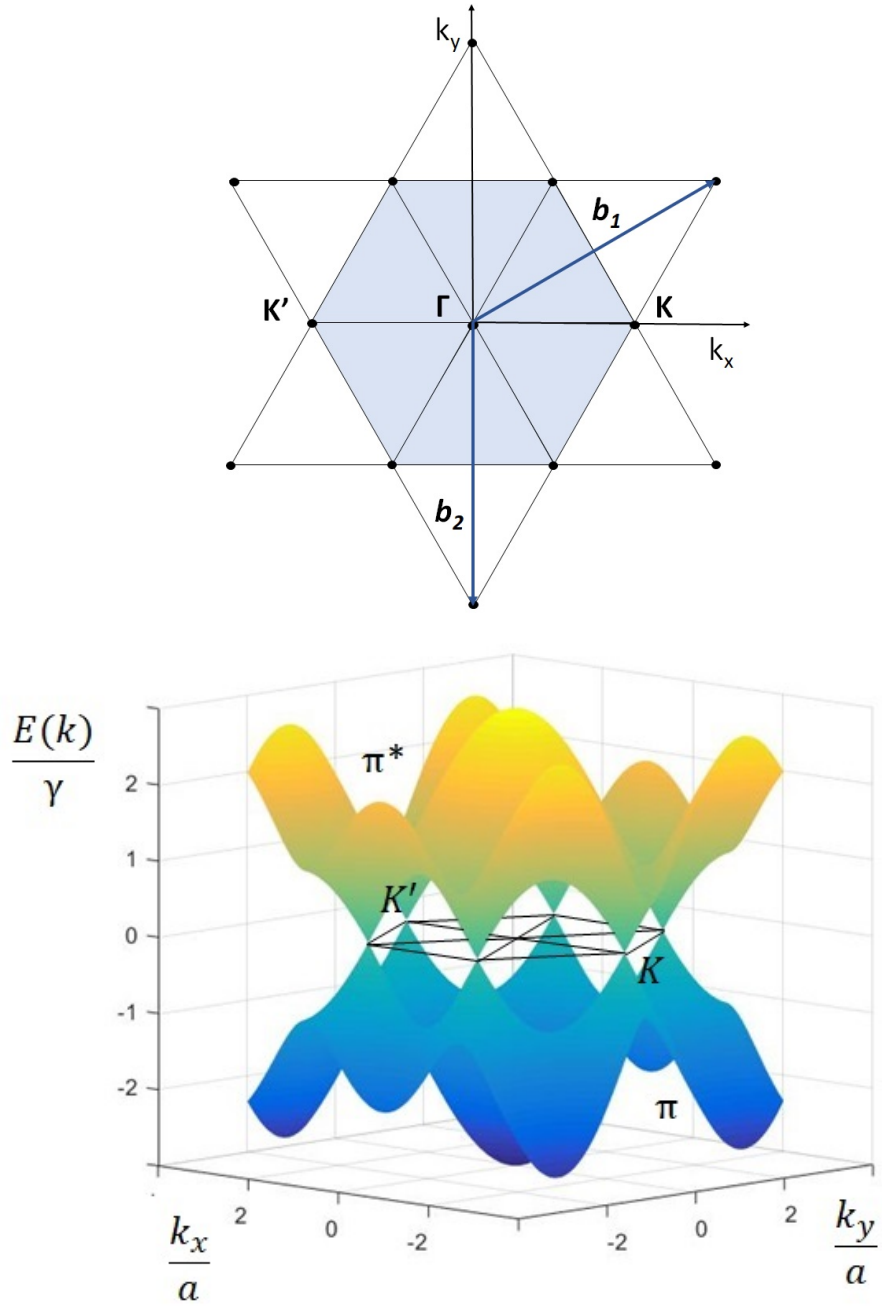


Figure 1.2: Above: Reciprocal lattice and First Brillouin Zone of graphene. The basis vector of the reciprocal lattice are $\boldsymbol{b}_1$ and $\boldsymbol{b}_2$; the First Brillouin Zone is the shaded area. The high symmetry point K and K' are called Dirac points. Below: band structure of graphene: the two bands, π and π^* touch in the high symmetry Dirac points.

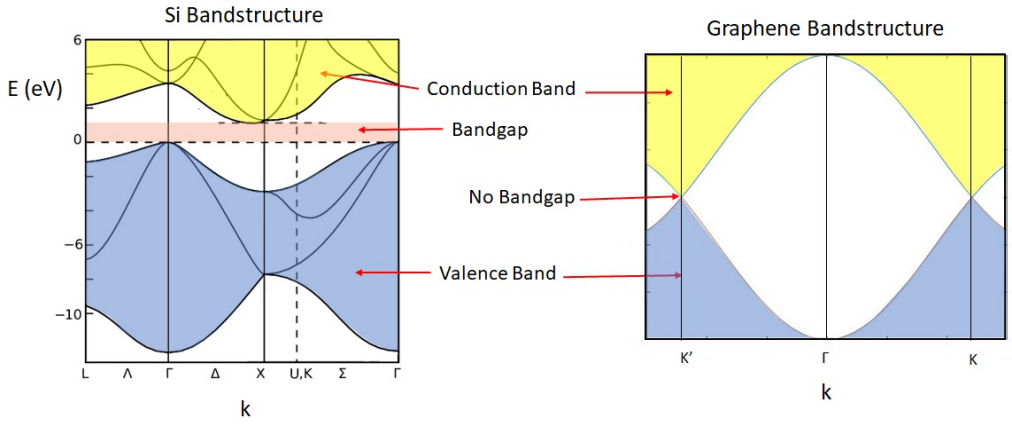


Figure 1.3: Band structure of silicon (left) and graphene (right). The valence band is in blue, while the conduction band is in yellow. While in silicon the conduction band and the valence band are separated by a 1.12 eV bandgap, graphene has no bandgap. Moreover, near the maximum of the valence band and the minimum of the conduction band, the dispersion relation is parabolic in silicon and linear in graphene.

Hence the DOS is zero at the Dirac point, while it linearly depends on the energy both in the valence and in the conduction band. Consequently, graphene can be considered as a zero bandgap semiconductor, or, more correctly, a semimetal. On the contrary, semiconductors as silicon or germanium have a finite bandgap between the conduction and the valence band; moreover, the density of state is parabolic with respect to the energy and not linear, as it can be seen in Fig. 1.3, which shows a comparison between the band structure of silicon and the band structure of graphene.

In the next sections, GFETs and their properties will be presented and compared to silicon devices.

1.2 GFETs

A FET is a device consisting of three terminals: a drain contact, a source contact and a gate contact. Basically, a transistor works as a switch: the gate voltage is used to create a channel between the drain and the source contacts, allowing the flow of a current. In the silicon technology, the three contacts lie on a bulk of doped silicon: the drain and source are directly in contact with the bulk, while the gate is separated by an insulating layer, typically an oxide, as in Fig. 1.4. Applying a voltage V_{GS} between the gate and the source, which is in general connected to the bulk, it is possible to form a conductive channel in the semiconductor near the interface with the oxide. In fact, considering a nMOS device in which the bulk is p-doped (on the right in Fig. 1.4), if the gate contact is at the same potential of

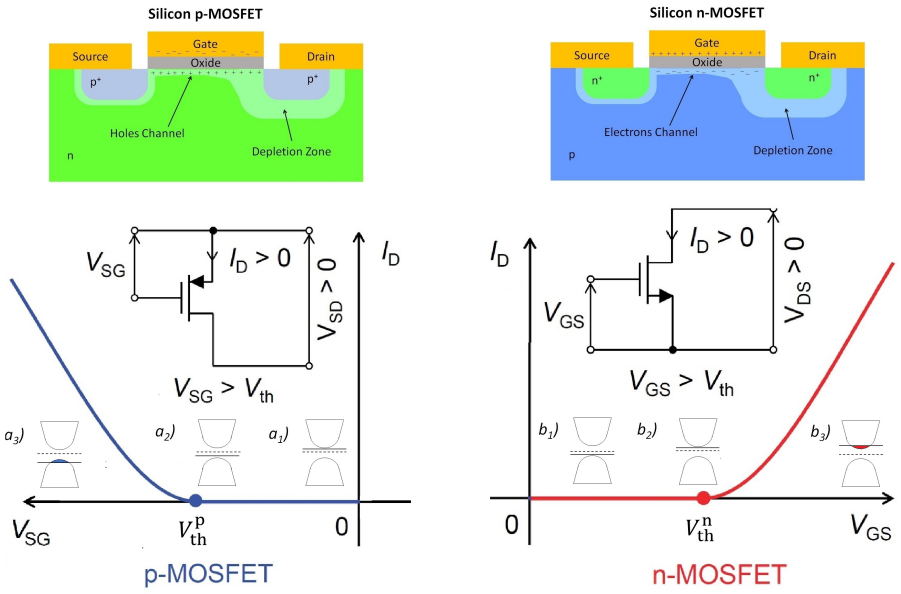


Figure 1.4: Above: structures of silicon MOSFETs, pMOS on the left and nMOS on the right. Below: transfer curves for the two devices with the filling of the bands at different V_{GS}. The filling of the conduction band is in red (electrons), while the emptying of the valence band is in blue (holes); the Fermi level is represented by the black continuous line, while the intrinsic level is the dashed line. Adapted from [8].

the bulk ($V_{GS} = 0$, b_1)), the Fermi level inside the semiconductor is close to the valence band, below the intrinsic level. However, applying a positive voltage to the gate ($V_{GS} > 0$ V), the valence band bends downwards. For small biases, the intrinsic level is still above the Fermi level and there is a depletion zone in the semiconductor near the oxide. For high biases, b_2), in particular for $V_{GS} > V_{th}$, which is called threshold voltage, the bands near the oxide are bent such that the intrinsic level goes below the Fermi level: in this condition, that is called inversion, the semiconductor behaves as a n-doped semiconductor near the oxide and the electric field of the gate attracts electrons to the channel, b_3). Moreover, the higher V_{GS}, the higher the density of charge attracted and hence the higher the conductivity of the channel. As a result, for a fixed V_{DS} (the voltage that sustain the current through the channel between drain and source), the transfer curve of a nMOS is the one on the right in Fig. 1.4. A pMOS works in the opposite way: the bulk is n-doped and it is connected to two highly p-doped zones. In the bulk the Fermi level is close to the conduction band, Fig. 1.4 a_1). A negative voltage on the gate ($V_{SG} > 0$ V), firstly induces a depletion zone until the Fermi level goes below the intrinsic level a_2), and then starts to attract holes as the Fermi level gets closer to the top of the valence band, a_3). In this way, for positive V_{SG}, higher than a certain negative threshold, the channel is conductive. It should be noticed that in this case the carriers are holes. The transfer curve is shown on the left in Fig. 1.4.

A GFET works in a similar way: the only difference is in the channel, which consists of a graphene sheet, usually deposited on a substrate (SiO_2 for example). The two drain and source contacts lie directly above the graphene, while also in this case the gate contact is separated from the channel by an insulating layer (Fig. 1.5). The operation of a GFET can be understood firstly looking at a simpler graphene resistor, obtained transferring a graphene sheet onto a substrate and contacting it with two electrodes. Ideally, the valence band of the graphene would be completely filled, while the conduction band would be completely empty: in this case, the Fermi level would be exactly at the Dirac point and the resistance would be infinite, since no carriers would be available. However, at a temperature different from zero, the thermal agitation promotes some electrons to the conduction band, leading to a situation in which the total number of carriers is different from zero, even though the total charge is zero and the Fermi level is at the Dirac point. Moreover, the presence of a substrate and the atmosphere affect the properties of graphene, introducing what is called ambient doping. In fact, molecules of water from the atmosphere or other ions present between the graphene and the substrate can act as donor or acceptor. In this way, the Fermi level is shifted and enters either the valence or the conduction band. For example, for graphene transferred onto a substrate of SiO_2 the Fermi level is shifted into the valence band (p-type doping) and hence the total number of carrier is different from zero.

Applying a voltage difference between the gate and the substrate, the Fermi level shifts and this shift leads to a change in the density of carriers in the channel

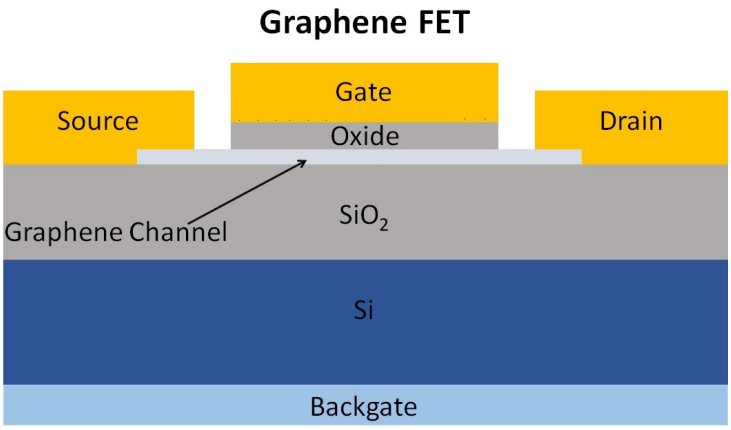


Figure 1.5: Structure of a GFET. Since the device is fabricated on a highly doped silicon chip, it is possible to use it as a dual gate device. The graphene is transferred on the thermal grown SiO_2, while topgate and electrodes (in orange) are evaporated.

itself. The greater the density of carriers, the greater the current that will flow in the graphene channel at a certain voltage difference between drain and source. Considering firstly for simplicity small biases between source and drain, the Fermi level can be considered constant throughout the channel. Moreover, let's consider the substrate and the source at the same potential. In this condition, the total charge present in the channel will be equal to the sum of the charge induced by the impurities and the charges induced by the gate voltage:

$$Q = Q_{\text{imp}} - Q_{\text{G}} = Q_{\text{imp}} - C_{\text{G}} V_{\text{GS}} \tag{1.16}$$

where Q_{G} is related to the V_{GS} via the oxide capacitance C_{G}. The condition of depletion of carriers, which occurs when the Fermi level is at the Dirac point, is reached when the carriers induced by the gate cancel out the carriers present because of the impurities. This V_{GS} is called Dirac voltage V_{Dirac} or threshold voltage V_{th}, as in the silicon FETs.

$$V_{\text{Dirac}} = V_{\text{th}} = \frac{Q_{\text{imp}}}{C_{\text{G}}} \tag{1.17}$$

As it has been said in the previous paragraph, the conductivity of the channel is not zero even at the Dirac voltage, mainly because of the thermal agitation. Moreover, the density of carriers in the graphene channel is not uniform: on the contrary, at the Dirac point, it is characterized by local inhomogeneities, called electron-holes puddles [9]. Hence, even at the Dirac point, the conductivity of the channel will not be zero, but there will be a minimum conductivity.

It is possible to compute the transfer function of the device in the following

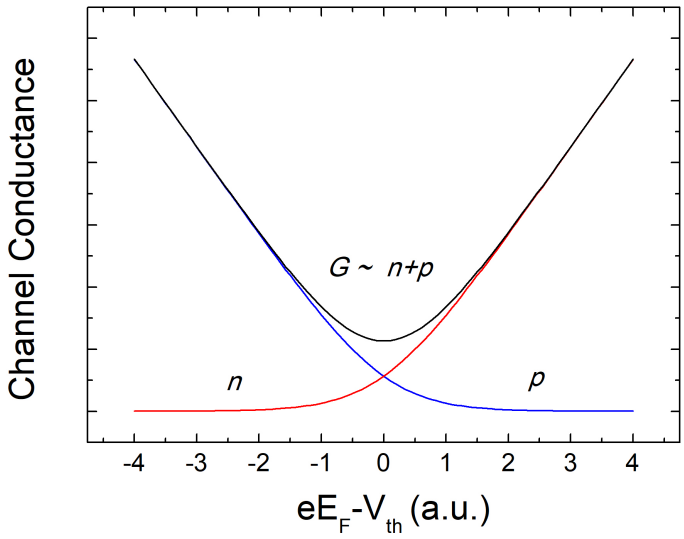


Figure 1.6: Conductance of the graphene channel. The conductance is given by the sum of the carriers. Even if when the Fermi level is at the Dirac point the total charge in the channel is zero, there is a minimum in conductivity given by the thermal carriers.

way:

$$I_{\mathrm{DS}} = GV_{\mathrm{GS}} = \frac{W}{L}\sigma_{\mathrm{ch}}V_{\mathrm{GS}} \tag{1.18}$$

where σ_{ch} is the conductivity of the channel, which can be related to the mobility and to the density of carriers:

$$\sigma_{\mathrm{ch}} = ne\mu_{\mathrm{n}} + pe\mu_{\mathrm{p}} \tag{1.19}$$

The charge density depends on the Fermi-Dirac distribution and on the DOS of graphene:

$$\begin{aligned} n = \int_0^\infty DOS(E) f_{\mathrm{n}}(E)\mathrm{d}E &= \frac{2}{\pi(\hbar v_{\mathrm{F}})^2}\int_0^\infty \frac{E}{1+e^{(E-E_{\mathrm{F}})/k_{\mathrm{B}}T}}\mathrm{d}E \\ &= \frac{2}{\pi}\left(\frac{k_{\mathrm{B}}T}{\hbar v_{\mathrm{F}}}\right)^2 \ln\left(1+e^{\frac{E_F}{k_B T}}\right) \end{aligned} \tag{1.20}$$

$$\begin{aligned} p = \int_{-\infty}^0 DOS(E) f_{\mathrm{p}}(E)\mathrm{d}E &= \frac{2}{\pi(\hbar v_{\mathrm{F}})^2}\int_{-\infty}^0 \frac{-E}{1+e^{-(E-E_{\mathrm{F}})/k_{\mathrm{B}}T}}\mathrm{d}E \\ &= \frac{2}{\pi}\left(\frac{k_{\mathrm{B}}T}{\hbar v_{\mathrm{F}}}\right)^2 \ln\left(1+e^{\frac{-E_{\mathrm{F}}}{k_{\mathrm{B}}T}}\right) \end{aligned} \tag{1.21}$$

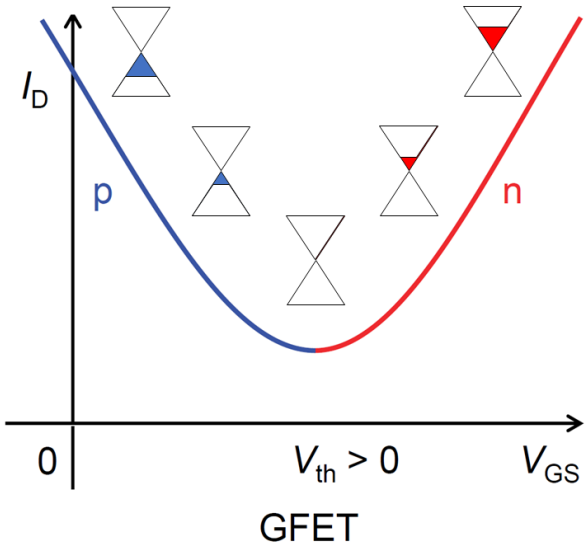


Figure 1.7: Transfer curve of a GFET at low V_{DS}. For $V_{GS} > V_{th}$, the Fermi level is above the Dirac point, in the conduction band and the carriers are electrons (in red); for V_{GS}. For $V_{GS} < V_{th}$, the Fermi level is below the Dirac point, in the valence band and the carriers are holes (in blue). Adapted from [8].

Eventually, the conductance can be expressed as:

$$G = \frac{W}{L}\frac{2e}{\pi}\left(\frac{k_B T}{\hbar v_F}\right)^2 \left(\mu_n \ln\left(1 + e^{\frac{E_F}{k_B T}}\right) + \mu_p \ln\left(1 + e^{-\frac{E_F}{k_B T}}\right)\right) \tag{1.22}$$

The conductivity of the channel (Fig. 1.6) will have a minimum at the Dirac voltage V_{th} and then will increase both for V_{GS} greater than the Dirac voltage and for V_{GS} lower than it, according to the change in the density of carriers resulting from the shift of the bands with respect to the Fermi level, as in Fig. 1.7. For V_{GS} greater than V_{th}, the Fermi level is in the conduction band and hence the carriers are electrons. On the contrary, for V_{GS} lower than V_{th}, the Fermi level is in the valence band and consequently the carriers are holes. This effect is known as ambipolar effect: in fact, in a GFET, the conduction depends on both electrons and holes. In a silicon FET, by contrast, the carriers are always either holes or electrons, depending on the type of doping of the substrate (see Fig. 1.4). In fact, considering the band structure of silicon and the mechanism of formation of the channel described previously, the threshold voltage is given by the minimum gate voltage necessary to have the inversion near the oxide, as it has been explained in the previous section. However, in contrast to graphene transistors, which are ambipolar, the silicon transistors are unipolar. Indeed, while for gate voltages higher than the threshold, the carrier density increases and the channel is more

conductive, for gate voltages below the threshold the channel is depleted and the conductivity decreases ideally to zero.

Since the gate voltage causes a shift in the bands of graphene, a consequence is that graphene cannot be at the same potential of the source contact. Hence, there must be a difference in the Fermi Level between the source contact and the channel. In fact, if a voltage difference between source and gate is applied, the positive charge on the gate side of the oxide must be screened by an equal amount of negative charge on the channel side of the oxide. However, the DOS of graphene is finite, hence it is not able to provide the necessary negative charge to screen the electric field generated by the gate, without a shift in the Fermi Level. Thus, the Fermi Level shifts, moving the potential of the channel somewhere in between the potential of the gate and the potential of the source. The correct description of this situation is thus not a single oxide capacitor, but a series of two capacitors: the first capacitor is related to the voltage difference between the gate and the channel, while the second capacitor is related to the difference between the channel and the source. The latter is called quantum capacitance and is typical of two-dimensional (2D) electron gases with finite DOS. The final result is that both the energy shift in the Fermi Level and the charge densities are lower with respect to the case in which the quantum capacitance was neglected. In particular, the energy shift is eV_{ChS} instead of eV_{GS}. The Dirac voltage will then increase (in absolute value), since a greater voltage difference is required to shift the Fermi Level in graphene in order to compensate the impurity charges. It is possible to demonstrate that, for p doped graphene at $T = 0$ K, the new Dirac voltage is:

$$V_{\mathrm{th}} = \left(\frac{\hbar v_{\mathrm{F}}}{e} \sqrt{\pi p_{\mathrm{imp}}} + \frac{A e p_{\mathrm{imp}}}{C_{\mathrm{G}}} \right) \tag{1.23}$$

The second term is nothing but $Q_{\mathrm{imp}}/C_{\mathrm{G}}$; as it can be seen, the first term is the additional voltage difference necessary to compensate the impurity charges taking into account the quantum capacitance. At the same biases, considering the quantum capacitance, the energy shift is lower, also the induced density of carriers will be lower. Again, at $T = 0$ K, it is possible to show that:

$$n_{\mathrm{e/h}} = n_{\mathrm{G}} - n_{\mathrm{q}} \left(\sqrt{1 + 2\frac{n_{\mathrm{G}}}{n_{\mathrm{q}}}} - 1 \right) \tag{1.24}$$

where

$$n_{\mathrm{q}} = \frac{\pi}{2} \left(\frac{\hbar v_{\mathrm{F}}}{e^2} \frac{C_{\mathrm{G}}}{A} \right)^2 \tag{1.25}$$

As it can be noticed, the total density of charge induced is lower than the density of charge n_{G} that would be induced neglecting the quantum capacitance.

Finally, if the voltage between drain and source is not negligible, the shift of the bands throughout the channel must be considered. In this case, the condition of depletion (Fermi level at the Dirac point) in different points along the channel

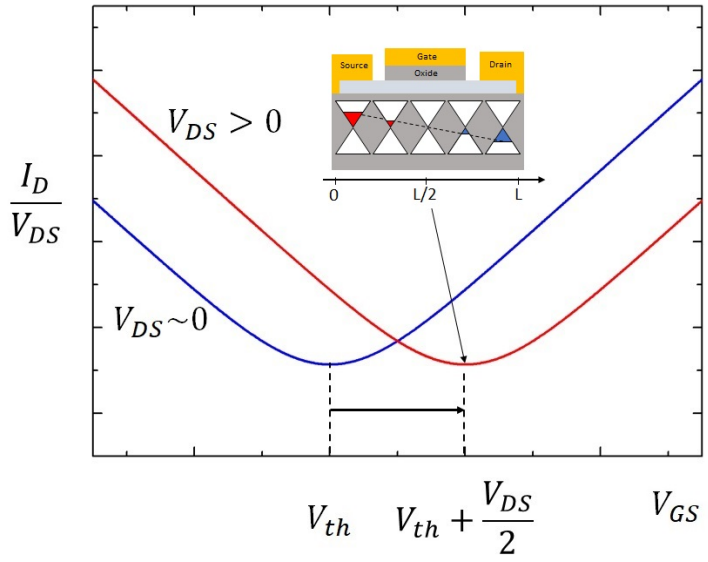


Figure 1.8: Shift in the transfer curve and hence in the minimum conductivity point resulting from a finite V_{DS}. In the insert: Fermi level and bands in a gradual approximation. The minimum in conductivity happens when the middle point of the channel is depleted (*i.e.,* the Fermi level is at the Dirac point): in that point the carriers undergo the ambipolar transition.

is reached at different V_{GS}. In particular, the condition of minimum conductivity happens approximately when the slice of channel in the middle reaches the depletion. Considering a gradual approximation (the potential increases linearly going from the source to the drain), valid in a non ballistic regime, this condition, neglecting the quantum capacitance, happens at:

$$V_{\mathrm{Gch}}(L/2) = V_{\mathrm{th}} \tag{1.26}$$

and hence

$$V_{\mathrm{Dirac}} = V_{\mathrm{Gch}}(L/2) + V_{\mathrm{chS}}(L/2) = V_{\mathrm{th}} + V_{\mathrm{DS}}/2 \tag{1.27}$$

Thus, the Dirac voltage is electrostatically shifted by the drain-source bias, as it can be seen in Fig. 1.8. By contrast, in silicon MOSFET, the threshold voltage depend mainly on the doping of the substrate and it is not shifted by a change in V_{DS} voltage.

Another curve that is usually presented in the study of transistors is the output curve, which is related to the change in the current with respect to a change in the drain-source bias, at a fixed gate voltage. Starting with a GFET with $V_{\mathrm{DS}} = 0$ and a positive V_{GS} above the threshold, the Fermi level is in the conduction band. In this condition, $V_{\mathrm{Gch}}(L) = V_{\mathrm{GS}}$ for every L (Fig. 1.9, 1). As V_{DS} increases, however,

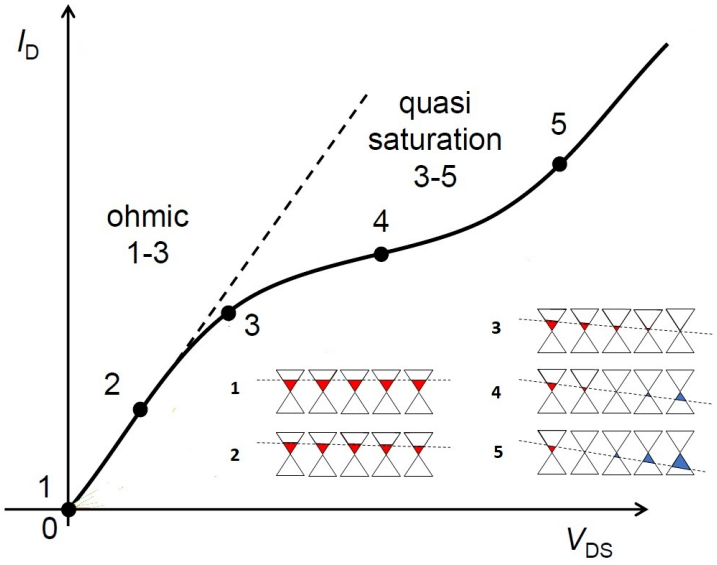


Figure 1.9: GFET Output curve at a fixed V_{GS}. In the insert: bands and Fermi level at different V_{DS}. The quasi saturation region corresponds to 4, when the channel reaches the minimum conductivity condition. However, unlike in silicon MOS, a further increase in V_{DS} is associated with an increase in conductivity.

the Fermi level near the drain starts to move towards the Dirac point: as a consequence, the conductivity of the channel decreases. On the output characteristic this results in a smaller slope of the curve (2 and 3). However, the condition of smallest conductivity is reached, as in the previous case, when the Dirac point is equal to the Fermi level in the middle of the graphene channel. In this condition, the conductivity is at its minimum and the slope of the output curve is the smallest (4). After this point, the conductivity starts increasing again, as well as the slope of the curve (5). The minimum conductivity region is called quasi-saturation, in analogy with the saturation region of silicon MOSFET. However, while in GFET the slope starts to increase after the minimum conductivity point, in silicon FET the slope becomes almost horizontal (neglecting short-channel effects).

GFETs are commonly fabricated on SiO_2(300 nm)/Si substrate, as in Fig. 1.5. Hence, it is possible to use them as double-gate devices. In particular, the top gate, for instance realized in aluminum, is separated from the channel by the thin Al_2O_3 oxide, while the backgate, which consists of the support of the chip and the highly doped silicon layer, is separated from the channel by the thermal SiO_2 oxide, 300 nm thick. The Fermi Level along the graphene channel can then be shifted through a combination of the two gates [10]: in fact, apart from the ambient doping, the charge induced in the graphene channel will be a function of the two voltages V_{TG} and V_{BG}. It can be demonstrated that the position of the Fermi Level satisfies the

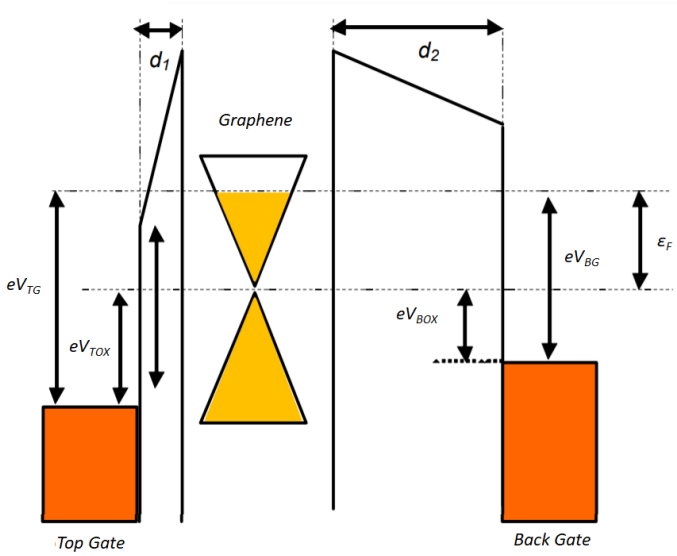


Figure 1.10: Band diagram of the vertical section of a dual gate graphene device. The topgate, on the left, has an oxide with a thickness d_1, while the backgate, on the right, has an oxide with a thickness d_2. Adapted from [10].

following equality:

$$\varepsilon_1\varepsilon_0\frac{eV_{\mathrm{TG}}-E_{\mathrm{F}}}{d_1}+\varepsilon_2\varepsilon_0\frac{eV_{\mathrm{BG}}-E_{\mathrm{F}}}{d_2}=\frac{e^2E_{\mathrm{F}}^2}{\pi(\hbar v_{\mathrm{F}})^2}+C_{\mathrm{it}}E_{\mathrm{F}} \tag{1.28}$$

where C_{it} is the interface traps capacitance, that takes into account the charge impurities. For example, it is possible to use the backgate voltage to control the electrostatic doping induced in the channel and hence shift the Fermi level, changing the topgate voltage at which the GFET presents a minimum in conductivity. For example, considering a GFET with an ambient p-type doping and applying a positive V_{BG}, the electric field will attract electrons, shifting the Fermi level upwards and hence reducing the total doping of the channel. As a result, considering the topgate voltage, the Dirac voltage will be reached at a smaller V_{th}.

1.3 Graphene in Digital Logic

Graphene has a series of properties that would identify it as a possible substitute for silicon in digital logic. First of all, graphene has a very high carrier mobility, as it has been said previously. However, a high mobility is in general not enough: in fact, as the size of the devices are reduced, the electric field in the channel increases. At high fields, the velocity of the carriers tends to saturate. Consequently, also a high saturation velocity becomes an important requirement. Graphene presents

an advantage also in this case, since the carriers can reach saturation velocities of 6×10^7 cm/s on SiO_2 [11], significantly greater than the saturation velocity in silicon, which is around 1×10^7 cm/s. Another problem in the scaling of silicon devices is the short-channel effect. This effect is related to the fact that the length of the channel becomes comparable with the depletion areas near the contacts: this leads to a decrease in the saturation velocity and the dependence of the threshold voltage on the length of the channel. Even in this case, graphene transistors are thought to be more immune to short channel effects and hence could reach smaller channel length [12]. In addition, the band structure of graphene, unlike silicon, is symmetrical, as it can be seen in Fig. 1.3. While holes and electrons have almost the same mobility in graphene devices, they have two different effective masses, and thus mobilities, in silicon. Hence, in silicon CMOS technology, the transistors must be designed in order to take into account this asymmetry. This problem is not present in graphene transistors. Lastly, doping is necessary in silicon devices: however, as the dimensions of the devices decreases, their sizes becomes comparable with the typical dimensions of the dopant atoms. This fact leads to fluctuations in the parameters and properties of transistors and hence could affect the proper operation of integrated circuits. On the other hand, graphene does not need doping and hence could overcome even this problem.

However, in digital electronics, apart from the speed and other fabrication issues, one of the most important properties of a logic transistor is the I_{ON}/I_{OFF} ratio, which is defined as the ratio between the current flowing in the channel in the ON state (when the channel is at its maximum conductivity) and the current in the OFF state (minimum conductivity). A high I_{ON}/I_{OFF} is required to ensure low power dissipation and a high output swing, which is fundamental to have two precise logic levels (high and low). In silicon transistors, ratio of 10^7 can be easily achieved: in fact, in a Si FET, the Fermi level can be shifted in the energy gap, between the conduction and the valence band, when $V_{GS} < V_{th}$. In this condition, there are no states available and the resistance of the device is very high. In a GFET, however, there is no bandgap, since as the Fermi level leaves the conduction band, it continuously enters in the valence band: the channel is never entirely depleted. For this reason, while a Si FET displays very high I_{ON}/I_{OFF} ratio, simple graphene transistors have a I_{ON}/I_{OFF} ratio significantly lower than the minimum ratio required in logic applications, around 10^4 [2]. In principle, opening a bandgap in the graphene sheet could be a way to achieve the required I_{ON}/I_{OFF} ratio. Over the years, many attempts have been made to open a bandgap in graphene: estimations suggest that a bandgap of 400-500 meV would be enough for logic applications [12]. One possibility is to use graphene nanoribbons (GNR): in fact, if the width of the graphene channel is reduced to few nanometers, the confinement of the electrons in the direction perpendicular to the channel on the graphene plane would open a gap in the band structure of graphene. If the GNR are patterned with lithography, however, the resulting rough edges increase the scattering of the carriers, leading to a deterioration in

the properties of graphene, such as the mobility. Nevertheless, it is possible to obtain a bandgap of 200 meV at low temperature with a width of 15 nm [13]. Another approach to obtain GNR is the chemical synthesis: however, even though it would allow to control the smoothness of the edges, it does not allow to control the position of the GNR, resulting in a non-scalable technique. A second way to obtain a bandgap in graphene is the use of bilayer graphene: in fact, applying an electric field perpendicular to the graphene sheet, it is possible to open a tunable bandgap between the valence and the conduction band [14]. However, even though this property is useful in applications of graphene such as photodetectors, the maximum bandgap achieved is too small for applications in digital logic. Even if in future it will be possible to open a sufficiently wide bandgap in graphene, there is an important drawback: in fact, it is a general trend in semiconductors that the bandgap is inversely proportional to the mobility. For example, nanoribbons with a channel width of 20 nm present mobility of the order of 2000 $\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$ at room temperature [15]. Furthermore, it is possible to show that the relation between mobility and bandgap is well described by the following relation [16]:

$$\mu \sim E_{\mathrm{g}}^{-3/2} \tag{1.29}$$

Hence, owing to the necessity of a wide enough bandgap, the advantages of graphene in terms of speed and mobility are lost.

Moreover, there is another obstacle in the use of GFET: the contact resistance, which is the additional resistance arising from the fact that graphene must be connected to a metal in order to realize the drain and source contact. The limited DOS of graphene and the lack of chemical bounds with the metal cause a very high contact resistance. In fact, while in silicon devices the resistance is around $10\ \Omega\cdot\mu\mathrm{m}$, the minimum contact resistance obtained with graphene is around $200\ \Omega\cdot\mu\mathrm{m}$ [17]. Since the total resistance of the device is given by the sum of the contact resistance and the channel resistance and given the fact that the gate voltage affects only the latter, the final $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio that can be achieved is limited by a high value of contact resistance.

In the Si CMOS technology, all the logic gates are obtained with a certain combination (series or parallel) of two components: the nMOS and the pMOS. For example, an inverter, or similarly a NOT gate, is a series of a pMOS and a nMOS with a common gate and a fixed supply voltage V_{DD}. As it can be seen in the insert in Fig. 1.11, when the gate voltage is zero (GND or the negative supply, namely the low logic state), for the nMOS $V_{\mathrm{GS}} < V_{\mathrm{th}}^{\mathrm{n}}$, while for the pMOS $V_{\mathrm{SG}} > V_{\mathrm{th}}^{\mathrm{p}}$: hence, the nMOS is in the OFF state, which is ideally equal to an infinite resistance; the pMOS is in the ON state, with a finite resistance. Hence, the output of the inverter will be close to V_{DD}. On the contrary, when the gate voltage is equal to V_{DD} (the high logic state), the nMOS is ON and the pMOS is OFF: consequently, the output is low, close to zero. More complicated gates are built with different combinations of series an parallel of the two nMOS and pMOS transistors. The fact that in the high state the output is very close to the positive

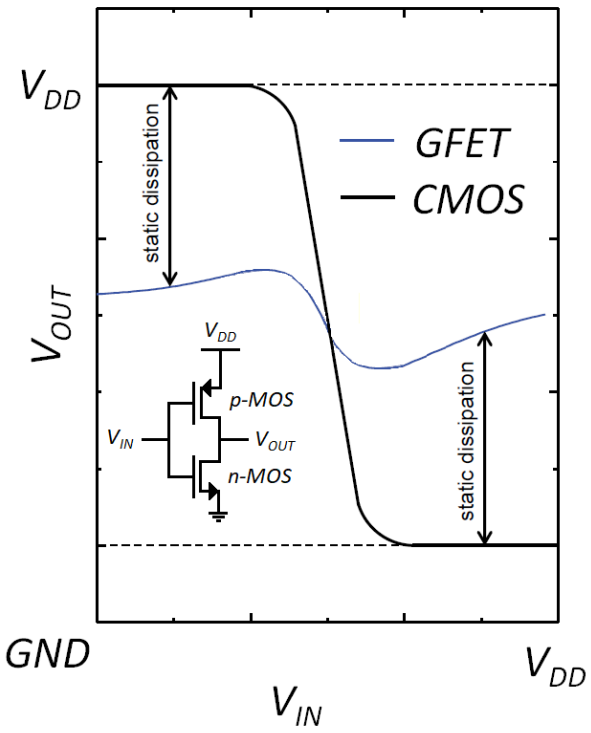


Figure 1.11: Transfer curve of the NOT gate, whose schematic is in the insert. In black the curve of a CMOS NOT gate, characterized by rail-to-rail operation and no dissipation power in static operation. In blue the GFET NOT gate. Adapted from [8].

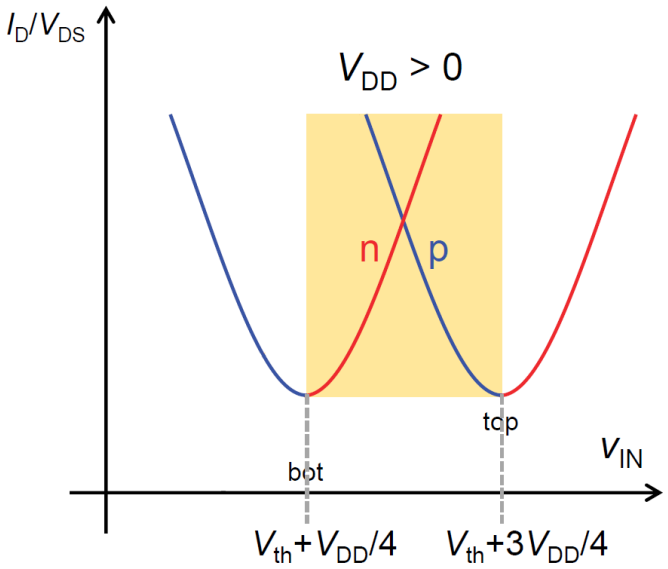


Figure 1.12: Transfer curves of the two GFET used in series to realize a NOT gate. The inverting operation is achieved only in the shaded are, where the GFET above is p-type and the GFET below in n-type. Adapted from [8].

supply and in the same way the low state is close to the negative supply is called rail-to-rail operation. This property is fundamental in the case the output of a logic gate has to drive another gate.

The situation is different with GFETs: in fact, it is possible to obtain an inverter employing a series of two GFETs, without the need of doping. Owing to the ambipolarity of graphene, in fact, there is a window of input voltage such that the GFET above shows a p-type behavior, while the GFET below shows a n-type behavior [18]. In fact, considering at first the hypothesis that the two GFET have the same resistance, the output will be equal to $V_{DD}/2$. Considering now the Dirac voltages of the two GFET and taking into account their dependence on the V_{DS} voltage (see equation 1.27), the Dirac voltage of the GFET below will be shifted by $V_{DD}/4$. Similarly, the Dirac voltage of the GFET above will be shifted by $V_{DD}/4$ above the voltage of the source, which is equal to $V_{DD}/2$. Hence, the situation is the one illustrate in Fig. 1.12: for an input voltage between $[V_{th} + V_{DD}/4, V_{th} + 3V_{DD}/4]$, the device works as an inverter. However, since the two GFET cannot be turned off (*i.e.,* the I_{ON}/I_{OFF} ratio is small), a rail-to-rail operation is not possible and, additionally, the inverter will dissipate static power. The transfer curve of a graphene inverter is shown in Fig. 1.11, together with the transfer curve of a CMOS inverter.

Apart from the small output swing and the power dissipation, the most important obstacle in the realization of more complex gates, such as NAND or NOR

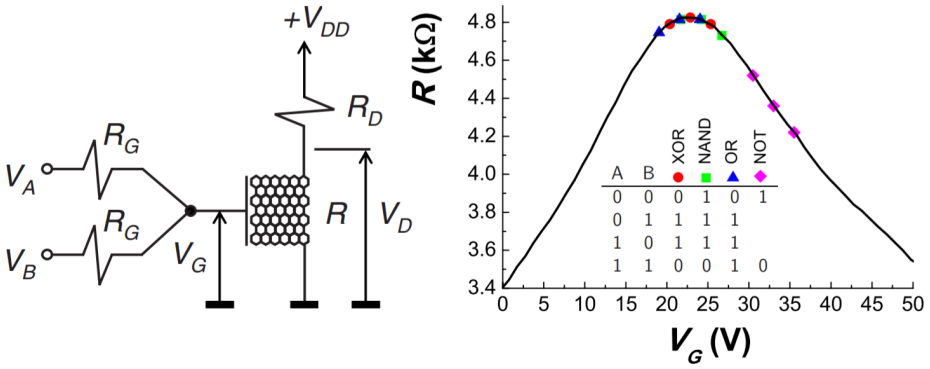


Figure 1.13: Left: two-input logic gate realized with a GFET. The two input V_{A} and V_{B} are chosen in order to select the proper operation of the logic gate required. For the XOR gate, for instance, the high and low levels must be equidistant from the maximum in the resistance (Dirac voltage); in this way, if the inputs have two different values, the gate voltage will be their average mean and hence the resistance of the GFET will be higher and the output of the gate will be higher. The other logic gates work in a similar way. Reproduced from [20].

gates, is the reduced window of operation. In fact, considering for example a NOR gate in the CMOS technology, it is realized with four MOS. The series of two pMOS above and the parallel of two nMOS below ensure that the output is high only if both the input voltages are low. If such a gate is to be realized with GFETs, it is clear that, since the Dirac voltages moves according to the V_{DS} of each GFET, the window of input voltages for which the two GFET above are p-type and the two below are n-type becomes smaller and there are asymmetries among the transistors. An alternate way to improve the splitting between the two Dirac voltages, increasing the window of operation of the device is adding an asymmetry in the fabrication of the GFET that will operate as p-type with respect to the n-type GFET. This can be done with a difference in the gate oxides, for example with a thicker oxide for the p-type GFET: in fact, the smaller the capacitance of the oxide, the greater the voltage necessary to reach the Dirac voltage. Hence the transfer curve of the p-type GFET will be shifted to higher voltages, increasing the window of operation of the device. This technique allowed the fabrication of NAND and NOR gates with an output swing of 30% of the supply voltage [19].

As it can be seen, the direct use of GFET to design and fabricate logic circuits has several drawbacks, stemming for example from the absence of a bandgap and from the uncontrollable shift of the Dirac voltage. However, there are some properties that characterize graphene that are absent in common semiconductor. For example, the absence of a bandgap is also responsible for the ambipolarity effect present in graphene. This peculiarity can be exploited to design unconventional

circuits that show new functionalities or offer in general advantages compared to the circuits that can be obtained with silicon transistors alone. For example, a single graphene transistor was successfully used to obtain four different logic gates, XOR, OR, NOT and NAND [20]. The principle behind this is the exploitation of the minimum in the transfer curve, *i.e.* the Dirac Point, as it can be seen in Fig. 1.13. The same principle has been exploited also to fabricate graphene frequency doublers [21].

Finally, another fact that is important to mention is the compatibility between the fabrication of graphene and silicon devices. In fact, it is possible to realize three-dimensional hybrid circuits in which the first level contains the silicon CMOS devices, while the second level contains the GFETs [22]. In this way, the new properties and peculiarities of graphene, such as the ambipolar effect, can be supported by the reliability and maturity of the silicon CMOS technology, in order to obtain circuits with new functionalities. The circuits described in the next chapters will represent other applications of this idea and are based on a single-graphene logic gate which is presented in the following section.

1.4 GRTL Gates

The ambipolar electric field behavior of GFET can be exploited to develop a new type of electronic component that can be used together with silicon CMOS transistors, to design new circuits with new or improved functionalities. This new component consists, as in the resistor-transistor logic (RTL) family in the series of a fixed resistor and a GFET. In silicon CMOS technology, such components can be used to obtain different logic gates, but the static power dissipation, resulting from the impossibility to turn off the device, has made this logic family disappeared in favour of the CMOS technology. Even though the problem of the too high power dissipation remains, a GRTL gate offers new functionalities, which are the consequences of the unique band structure of graphene. Considering this logic gate, which is shown in Fig. 1.14, the output voltage is equal to the V_{DS} voltage of the GFET, which can be calculated as the divider of the supply voltage between the resistance R_{s} (series resistance) and the resistance of the GFET, R:

$$V_{\mathrm{OUT}} = V_{\mathrm{DS}} = \frac{R}{R_{\mathrm{s}} + R} V_{\mathrm{DD}} \tag{1.30}$$

where $R = R(V_{\mathrm{GS}}) = R(V_{\mathrm{IN}})$, since the resistance of the graphene channel depends on the gate voltage. If we consider a gate voltage starting from zero and increasing up to the supply voltage, if the Dirac voltage is in the same range [0, $\mathrm{V_{DD}}$], the resistance R will at first increase until V_{GS} reaches the Dirac voltage, and then will decrease. As a consequence, $V_{\mathrm{DS}} = V_{\mathrm{OUT}}$ will at first increase and then decrease. From a logic point of view, as it is shown on the right of Fig. 1.14, for a voltage input which is either high or low, the output of the gate will be low; for an input whose value is between 0 and V_{DD}, the output will be high.

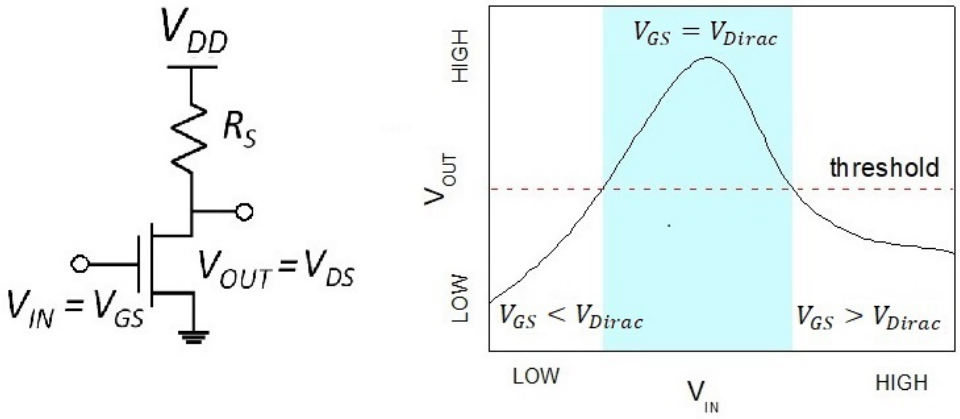


Figure 1.14: Output curve and structure of the GRTL gate proposed. For V_{IN} close to the Dirac Voltage, the resistance R is at its maximum value. Hence, V_{OUT}, obtained as the divider between R_{s} and R, will be at his maximum. For V_{IN} above or below the Dirac voltage, on the contrary, the resistance of the GFET is low and therefore V_{OUT} is at its minimum level.

The swing on the output of the logic gate depends on the ratio between the resistance of the GFET at the Dirac voltage, R^{HIGH}, and the value of the resistance at the two extreme voltages (0 and V_{DD}), R^{LOW}. In fact:

$$\begin{aligned}\Delta V_{\mathrm{DS}} = \Delta V_{\mathrm{OUT}} &= V_{\mathrm{DS}}^{\mathrm{HIGH}} - V_{\mathrm{DS}}^{\mathrm{LOW}} \\ &= \left(\frac{R^{\mathrm{HIGH}}}{R^{\mathrm{HIGH}} + R_{\mathrm{s}}} - \frac{R^{\mathrm{LOW}}}{R^{\mathrm{LOW}} + R_{\mathrm{s}}} \right) V_{\mathrm{DD}}\end{aligned} \tag{1.31}$$

Deriving this function with respect to R_{s}, the series resistance, it is possible to show that the maximum swing is obtained if the following condition is met:

$$R_{\mathrm{s}} = \sqrt{R^{\mathrm{LOW}} R^{\mathrm{HIGH}}} \tag{1.32}$$

In this optimal case, the swing on the drain becomes:

$$\Delta V_{\mathrm{DS}} = \Delta V_{\mathrm{OUT}} = \frac{1 - \sqrt{x}}{1 + \sqrt{x}} V_{\mathrm{DD}} \tag{1.33}$$

where $x = R^{\mathrm{LOW}}/R^{\mathrm{HIGH}}$. Hence, the swing, in the optimal condition, depends only on the ratio of the two resistances. For example, a ratio of 2/3 leads to a swing of 10% of the supply V_{DD}. In any other non-optimal condition, the swing will be certainly lower. The power, on the contrary, depends on the absolute value of the resistances: the smaller those values, the higher the power dissipation.

In general, it is not possible to work in the optimal conditions. In fact, in hybrid circuits the GRTL gate must satisfy some requirements, concerning the

voltage levels of the outputs for example. For this reason, the series resistance R_s can be tuned in order to shift the output upwards or downwards. If it is necessary, also the supply of the GRTL gate could be changed with respect to the supply of the rest of the silicon CMOS circuit. Anyway, this could be a problem in a more complex circuit, since it would require two different supply lines.

Before introducing the two circuits in which the GRTL gate is used, the fabrication processes and the electrical characterization of the GFETs will be briefly described.

1.5 Fabrication

The graphene transistors used in the measurements were fabricated on a SiO_2 300 nm substrate, thermally grown on a silicon chip. Although, even if the SiO_2 is compatible with the processes of fabrication of standard silicon integrated circuits, it is not an optimal substrate for graphene. In fact, the high rugosity and the presence of dangling bonds acting as charge traps deteriorate the properties of graphene. For these reasons, other substrates have been studied. One of them is the hexagonal boron nitride (hBN), which is an insulating material with a honeycomb structure similar to the graphene structure. The lattice parameter close to the one of graphene (only 1.7 % difference), the very low rugosity and the absence of charge traps allow to obtain graphene of better quality [23].

Another important fact that affects the quality of graphene is how the graphene itself is obtained. Even if the mechanical exfoliation allows to get graphene of pure quality and with optimal properties [1], it is not possible to use this technique on large scale, since it is not possible to control the position and the size of the flakes produced. Hence, it has been necessary to develop other techniques: for example, it is possible to grow graphene on copper [24] with chemical vapor deposition (CVD) and then transfer it on the SiO_2 substrate. Once transferred, it is possible to use Si-CMOS compatible methods (e-beam lithography, evaporation, plasma etching) in order to shape the channel and deposite the electrodes and the gate contact. In this section all the steps of fabrication will be presented. Apart from the CVD, all the other processes have been performed at the L-NESS laboratories.

1.5.1 Preparation of Substrate and hBN Exfoliation

The SiO_2(300 nm)/Si substrate is first cleaned in a Reactive Ion Etching (RIE) with oxygen plasma (with a flux of 250 ml/sec) for 2 minutes at 350 W. This process removes residuals and activate the SiO_2 surface, creating dangling bonds that will facilitate the adhesion of the hBN flakes. The hBN crystals are then exfoliated with scotch-tape technique employing dicing tape, in order to reduce the thickness of the flakes. The tape is then placed over the substrate and gently pressed in a uniform way. The chip is heated at 85° C for 10 minutes: in this way, the bonds between the tape and the hBN flake are weakened and the hBN remains

Figure 1.15: Optical image of the chip with exfoliated hBN flakes. The flakes obtained are different in dimensions and thickness.

bound to the SiO_2 surface. Subsequently, the tape is removed: experimentally, it has been observed that the hBN flakes are more easily left on the chip if the angle at which the tape is removed is 180° C. Finally, the chip is cleaned in acetone for few minutes in order to remove the tape residuals.

The surface of the chip can be observed with a optical microscope in order to identify the hBN flakes, as in Fig. 1.15. In fact, hBN flakes are visible due to the difference between the reflectivity of the substrate and the reflectivity of the area where hBN is present. The contrast, which is the normalized difference in reflectivity, depends in general on the dielectric constants of the materials, on their thickness and on the wavelength of the incident light. In the case of hBN, the bilayer and monolayer are very hard to be spotted: in fact their contrast is very low, around 1.5% [25]. However, since the hBN must be used as a substrate for graphene, it is necessary to find multilayers in order to suppress the influence of the SiO_2 substrate. Furthermore, the color of the flakes appears dark blue for thin multilayers and, as the number of layers increases, it becomes firstly light blue, then green, yellow and finally red, for the very thick flakes. A too thick hBN flake would stretch and possibly break graphene, hence these flakes should be avoided. Usually, light blue or blue flakes are preferred.

1.5.2 Graphene Transfer

The graphene used had been grown with CVD on Copper by the Nanocarbon Group (DTU, Nanotech). The Graphene/Cu film is firstly spincoated with poly (methyl methacrylate) (PMMA) and anisole (996 K, 2%) for 60 seconds at 1000 rpm and then heated at 100° C for half an hour. In order to etch the copper layer,

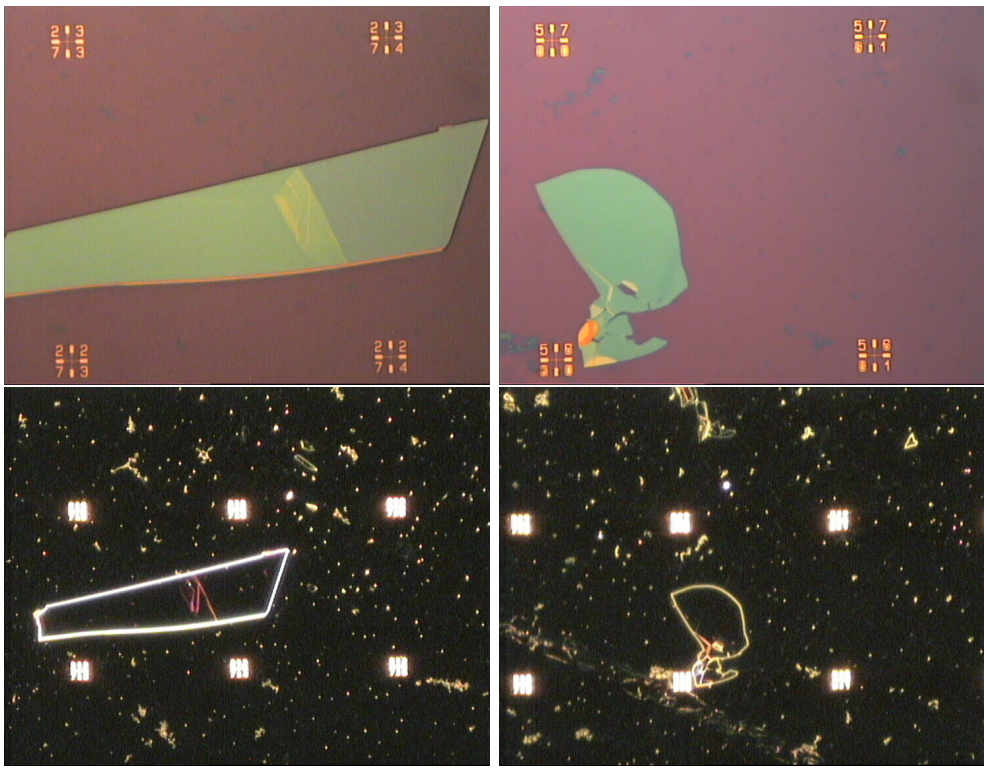


Figure 1.16: Above: optical image of two hBN flakes with a uniform coverage of graphene, in bright field. Below: same images in dark field. The two area with hBN flake are clean enough to be chosen to fabricate the devices.

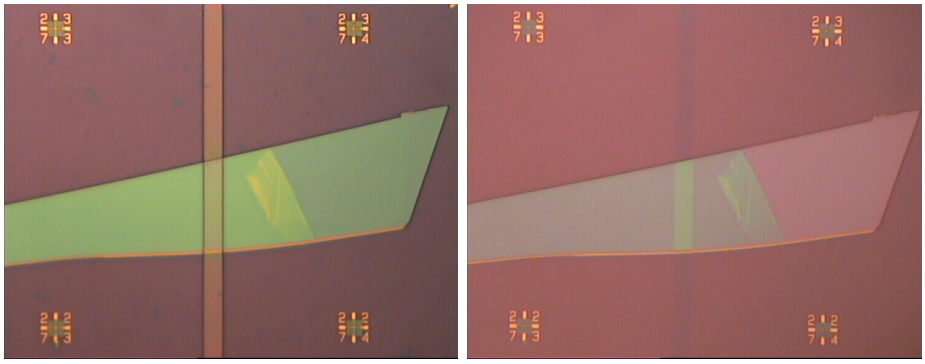


Figure 1.17: Channel definition. On the left, the PMMA that covers the channel is visible. The graphene transferred is still present everywhere. On the right, the graphene that surrounds the channel is removed with RIE and the PMMA is removed with acetone. The results consists in a 5 μm wide channel on a hBN flake.

the PMMA/Graphene/Cu film is placed in a solution 7:1:0.3 H_2O:HCl:H_2O_2 until the copper is completely etched. The PMMA/Graphene film is then fished with a glass slide and put in water for three times, in order to clean it from other contaminants. Finally, the chip with hBN flakes is used to fish the PMMA/Graphene film and is placed in an oblique position for a day, until it dries. Eventually, the chip is heated with temperature ramps from 50° C to 110° C with a change of 20° C every 15 minutes. At last, the chip is put in acetone to remove the PMMA layer. The result is shown in Fig. 1.16. The chip is observed with optical microscope in bright field and dark field in order to find the hBN flakes with transferred graphene with a good quality to fabricate the device. In particular, the bright field is used to identify the flakes and any possible scratch in the graphene sheet. The dark field provides information about defects or residuals: in fact, those impurities are centers of scattering for the light and they appear bright. A good area to fabricate a device should be free of scratches and impurities, as the two example in Fig. 1.16.

1.5.3 Channel Definition

The channel is patterned by removing the surrounding graphene with RIE. Firstly, it is necessary to cover the channel with a mask. Hence the chip is spincoated with three layers of PMMA (950 K, 6500 rpm) and baked (160° C for 5 minutes), so that the solvent evaporates. The PMMA is a positive resist: if it is exposed to an electron beam, the polymeric chains of PMMA are broken and they can be removed with a development in a solution 1:3 4-methyl-2-pentanone:isopropanol. For this purpose, the chip is exposed with a Scanning Electron Microscope (SEM) used as a Electron Beam Lithography (EBL) system. In particular, a square with side of 1000 μm around the hBN flake is exposed, with the exception of the channel, which is 80 μm long and 5 μm wide. After the development, the result is the one

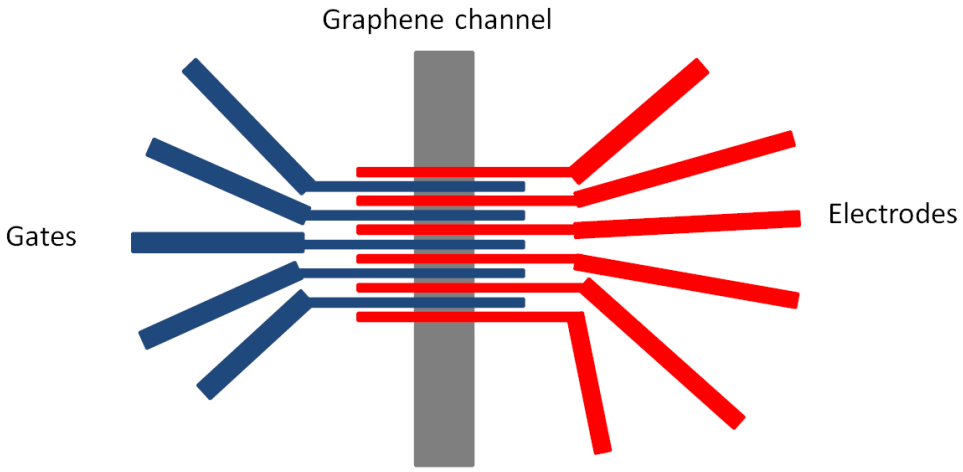


Figure 1.18: Design used to realize the devices. The gates are in blue, while the electrodes are in red. With the same design it is possible to realize inverters, using a common electrodes, without the need of external connections.

in Fig. 1.17, on the left.

Once the mask of the channel is developed, the graphene around the channel, now exposed, must be removed. This is done in a RIE with an O_2 plasma, with a 250 ml/minute flux at 100 W. The chip is then put in acetone to remove the PMMA mask. The result is on the right in Fig. 1.17. As it can be seen, the oxygen plasma removes the graphene around the channel and some layer of hBN, which appears more transparent.

1.5.4 Contacts Deposition

The final step is the deposition of the electrodes (that will be used as drain and source contacts) and the gates. The design used, illustrated in Fig. 1.18, consists of a structure of five devices, with common electrodes (in red) and local topgate (in blue). Firstly, gates are fabricated. The chip is spincoated with two layers of PMMA and exposed with EBL. After the development, analogous to the same step in the channel definition, the chip appears as in Fig. 1.19. Once the PMMA has been patterned with the design of the gate, the chip is placed in an evaporator in order to deposit 100 nm of Aluminum. Then the chip is cleaned in acetone, which removes the PMMA and hence leave the Aluminum gates as in Fig. 1.19. The two layers of PMMA previously spincoated have two different densities. In particular, the PMMA of the first layer is less dense and hence it will be more exposed than the second layer. In this way, while the dimensions of the gates depend on the pattern of the second layer, since the first layer has greater holes, the acetone will

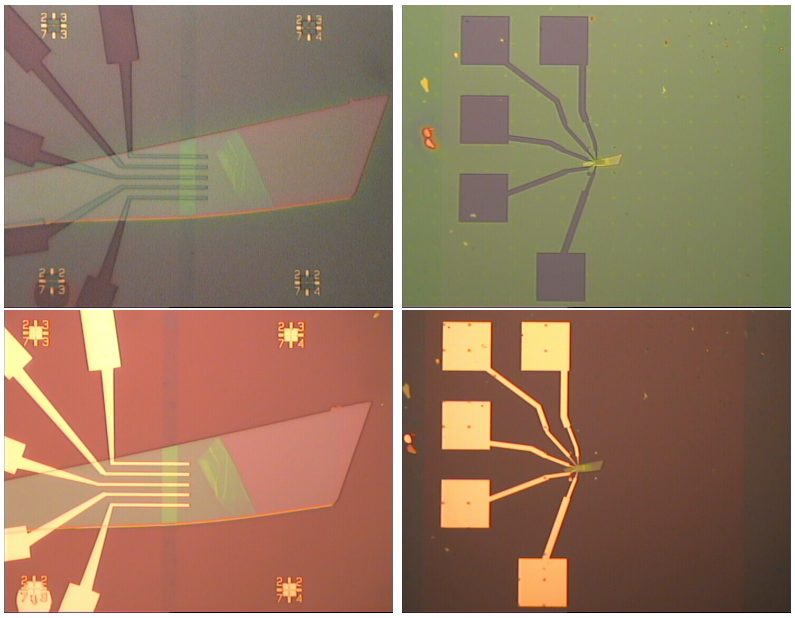


Figure 1.19: Optical images of the gate deposition. The images on the left are at a 100x zoom, while the images on the right at a 10x zoom. Above, it is possible to see the PMMA mask after the development. Below, the gates after lift-off following the deposition of 100 nm of Aluminum. The pads visible in the 10x images are used to contact and measure the devices with external probes.

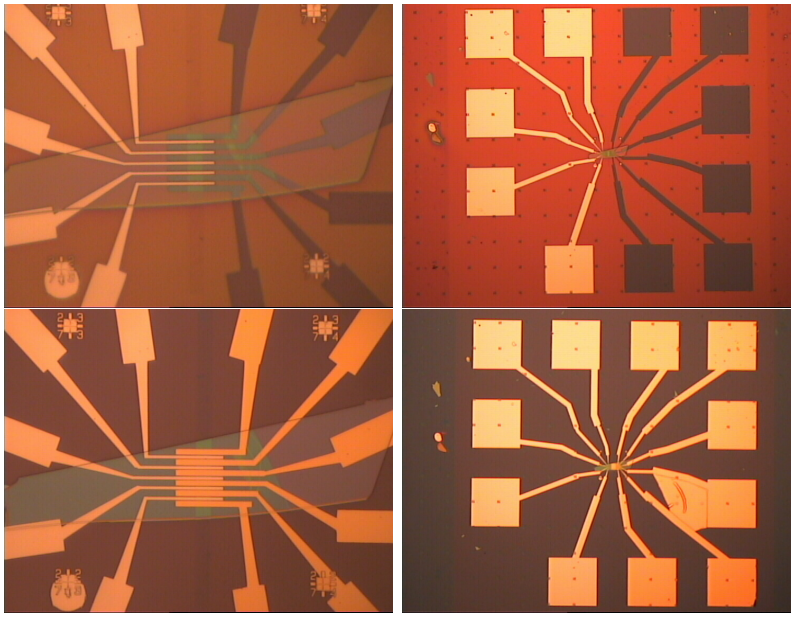


Figure 1.20: Optical images of the electrodes deposition. The images on the left are at a 100x zoom, while the images on the right at a 10x zoom. Above, it is possible to see the PMMA mask after the development. Below, the electrodes after lift-off following the deposition of 100 nm of Gold.

be able to penetrate and to facilitate the lift-off. Moreover, since the Aluminum oxides in air, a thin layer of oxide will be formed at the interface with graphene. The electrodes, in gold, are deposited with the same procedure. The chip after the development and after the evaporation is shown in Fig. 1.20. Ten structures have been fabricated with this method, on the same chip. The electrodes are all 2 μm wide, while the space between two consecutive electrodes is 1.2 μm. Different values (600, 700, 800, 900 and 1000 nm) have been used as gate width.

1.6 Characterization and Problems

In order to set the parameters to use the GFETs in a GRTL gate, the device fabricated have been firstly characterized. In particular, it is necessary to measure the resistance at the Dirac voltage (*i.e.,* the voltage at which the conductivity of the channel is the minimum), in order to choose a correct range for the series resistance R_s of the GRTL gate, and the Dirac voltage itself, in order to find the input voltage at which the GRTL gate's output presents a maximum. In this first part of this section, the relation between the resistance of the GFETs, the Dirac voltage and V_{DS} will be described. Later, the problems of the measurements regarding hysteresis and contact resistance will be discussed.

The transfer curve of the GFET have been measured at different V_{DS}, in the

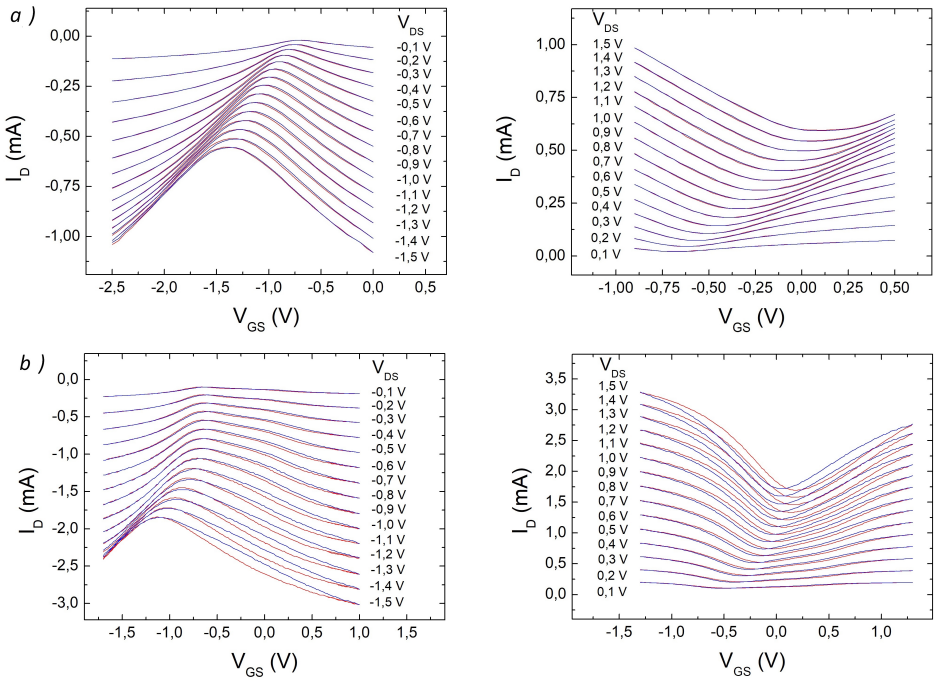


Figure 1.21: Series of transfer curves of two different GFETs (a and b): on the left, V_{DS} changes from -0.1 V to -1.5 V and the gate voltage range is $[-2.5\ \mathrm{V}, 0\ \mathrm{V}]$ (a) and $[-1.7\ \mathrm{V}, 1.0\ \mathrm{V}]$ (b). On the right, V_{DS} changes from 0.1 V to 1.5 V and the gate voltage range is $[-0.9\ \mathrm{V}, 0.5\ \mathrm{V}]$ (a) and $[-1.3\ \mathrm{V}, 1.3\ \mathrm{V}]$ (b). The blue (red) transfer curves are related to the upsweep (downsweep) measurement. As it can be seen, the hysteresis in the GFET a is negligible, while it is stronger in the GFET b, especially at positive V_{DS} (b2).

range $[-1.5\ \mathrm{V}, 1.5\ \mathrm{V}]$ with a step of 100 mV. In particular, two measurements have been performed: firstly each transfer curve has been measured at positive bias $[0\ \mathrm{V}, 1.5\ \mathrm{V}]$ and then at negative bias $[-1.5\ \mathrm{V}, 0\ \mathrm{V}]$ with a V_{GS} whose range contained the Dirac voltage V_{Dirac} at all the different biases. Each measurement has been performed with a Keithely 2611A, firstly setting the V_{DS} and then sweeping the V_{GS}. In particular, in every measurement V_{GS} starts from zero, increases to the highest value in the range selected, decreases to the lowest value and eventually repeats the sweep. In this way it is possible to have two type of transfer curve: the first correspond to an upsweep of the V_{GS}, while the second to a downsweep. As it will be explained in the next section, the two curves can be different owing to hysteresis present in the devices.

Two examples of the transfer measurements are given in Fig. 1.21, for positive and negative V_{DS}. As it can be seen, the minimum in the conductivity shifts according to V_{DS} (see equation 1.27). As V_{DS} tends to zero, the Dirac voltage

tends to a negative value: -650 mV for the GFT a) and -500 mV for the GFET b). Also the other GFETs measured displayed this behavior, hence, it can be concluded that for the sample fabricated with CVD graphene and hBN substrate and Al gate, the ambient doping is n-type. The impurities act as donors, shifting the Fermi level in the conduction band. A negative topgate voltage is thus necessary to bring the Fermi level back to the Dirac point.

The shift in the Dirac voltage with respect to V_{DS} is shown in Fig. 1.22. On the whole, the general trend can be described by:

$$V_{\mathrm{Dirac}} = V_{\mathrm{amb}} + kV_{\mathrm{DS}} \tag{1.34}$$

where V_{amb} is close to -500 mV and k is around 0.5. This is in accordance with the equation 1.27. This is true especially in the first case. In the other cases, there are deviations from the ideal behavior. Probably these are due to charging effects or to the hysteresis. Nevertheless, the general trend is respected in almost all the devices measured. The only relevant deviations appear at very high V_{DS} (more than 2.0 V, in absolute value).

The relation V_{Dirac} (V_{DS}) can be used to define the supply and the voltage range of the GRTL gate and the other CMOS gates. In order to use the GFET in the GRTL gate, the Dirac voltage must be in a window around the middle of the range of the gate voltage. In general, the range of this window depends on the specific application and on the quality of the GFET (concerning for example ON/OFF ratio and asymmetry in the transfer curve). For simplicity we can consider a window of 25% of the total gate voltage range. Since the GRTL gate will be connected to other CMOS components, the range of the gate voltage will be equal to the supply range of those components. Moreover, to avoid multiple supplies, we consider the supply of the GRTL gate equal to the supply of the other CMOS components. Additionally, in order to avoid double supply biases, it has been chosen to work with a single supply, meaning that the range of the supply can be indicated as $[0\ \mathrm{V}, \mathrm{V_{DD}}]$, where V_{DD} is either a positive or a negative voltage. Hence:

$$\frac{3V_{\mathrm{DD}}}{8} < V_{\mathrm{Dirac}} < \frac{5V_{\mathrm{DD}}}{8} \tag{1.35}$$

Assuming for simplicity $R_{\mathrm{Dirac}} \sim R_{\mathrm{s}}$, the output of the GRTL gate, equal to V_{DS}, will then be half of the range of supply. Finally, the condition that must be met to ensure the proper operation of the GRTL gate is:

$$\frac{3V_{\mathrm{DS}}}{4} < V_{\mathrm{Dirac}} < \frac{5V_{\mathrm{DS}}}{4} \tag{1.36}$$

As it is possible to observe in Fig. 1.22, given the n-type doping of the GFETs on hBN, only a negative supply allows to ensure a proper operation of the GRTL gate. For example, a supply voltage V_{DD} lower than -2.0 V ($V_{\mathrm{DS}} < -1.0$ V) usually ensures that the Dirac voltage is at the center of the gate range. If, for any reason, it is necessary to have more precision in the position of the Dirac voltage or if

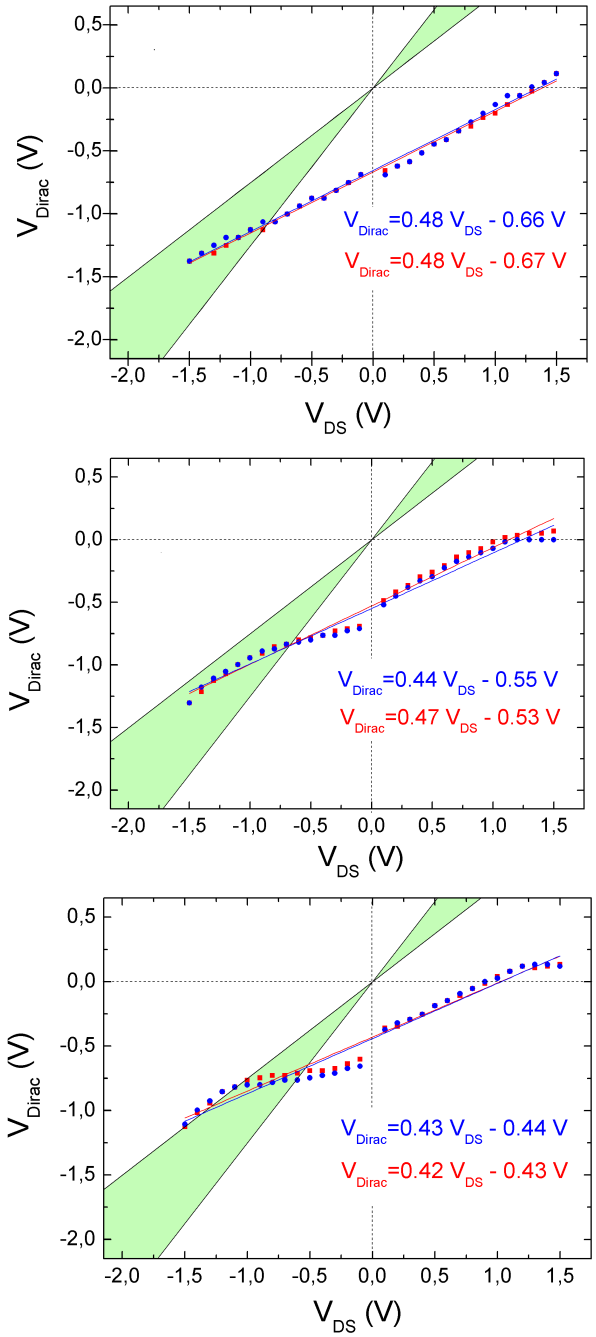


Figure 1.22: Three example of the shift of the Dirac voltage at different V_{DS}. In blue (red) the Dirac voltages related to the upsweep (downsweep) of V_{GS}. The three sets of data have been fitted with a linear curve, in order to find the ambient doping and study the accordance with the equation 1.27. Moreover, the green shaded area corresponds to the window of voltage that ensures a proper operation of the GRTL gate.

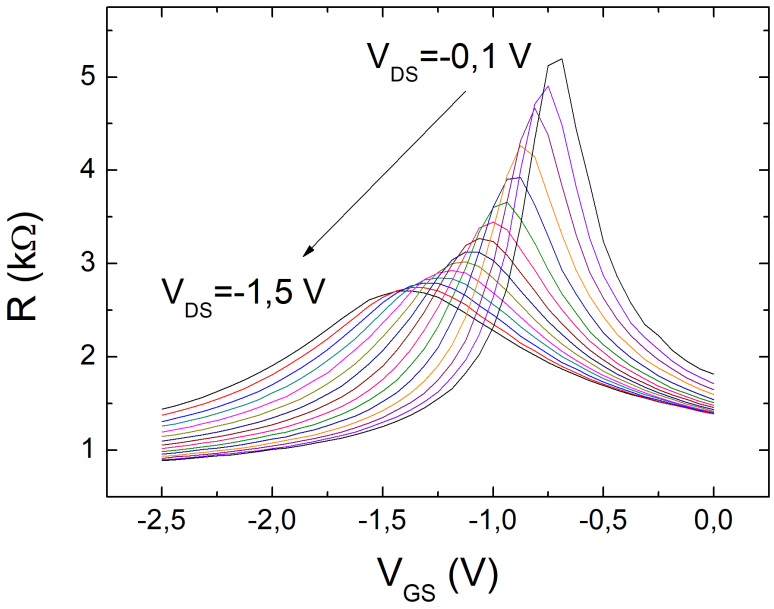


Figure 1.23: Total resistance of the GFET as a function of V_{GS} at different V_{DS}, from -0.1 V to -1.5 V. The maximum resistance decreases, together with the ratio between the maximum and the minimum resistance.

the experimental V_{Dirac} is out of the allowed voltage window, it is still possible to employ two different supply voltages: one for the GRTL gate, that will determine the V_{DS} and one for the other CMOS components, that will determine the V_{GS} range. The drawback is a more complicated supply system.

The second parameter that has been studied is the resistance of the GFET, especially the total resistance at the Dirac voltage. From the transfer curves it is possible to extract the value of the resistance of the GFET (channel plus all the parasitisms) at different V_{GS} and V_{DS}. An example of the dependence of the resistance on these two parameters is shown in Fig. 1.23. The curves have been extracted from the measured transfer curves (only related to the V_{GS} downsweep). As it can be seen, V_{DS} affects both the value of the peak resistance and the ratio between the maximum and minimum resistance. The maximum resistance is shown in Fig. 1.24 for three different devices. As it can be seen, the resistance at the Dirac voltage has a maximum at $V_{DS} = 0$ V. In fact, if the voltage different between drain and source is small, then the Fermi level will be approximately constant along the whole channel and, at V_{Dirac}, the channel is all depleted (a, in the insert in Fig. 1.24). On the contrary, if $V_{DS} > 0$, the condition of depletion is reached at different voltages along the channel. The total resistance, a part from the parasitisms, can be calculated as the sum of many resistance in series:

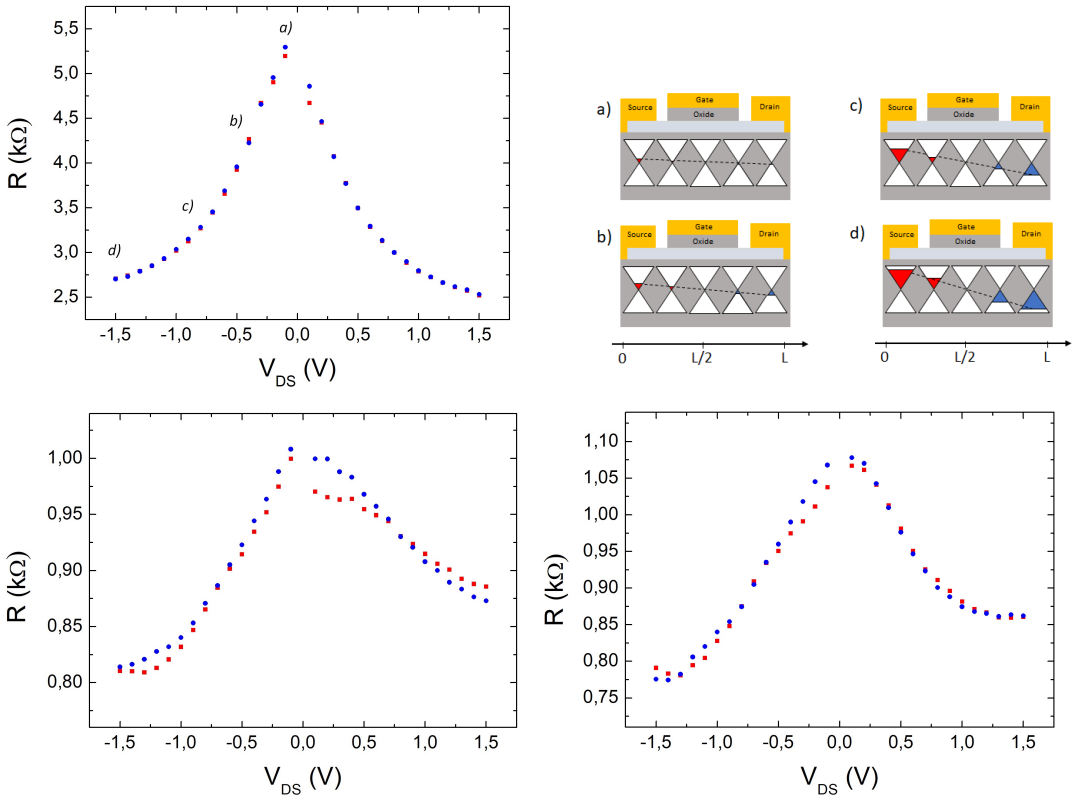


Figure 1.24: Three examples of the dependence of the maximum resistance as a function of V_{DS}. The maximum is found at $V_{\mathrm{DS}} \sim 0$, when the channel is fully depleted (a). As V_{DS} increases in absolute value (from b to d), the Fermi level near the drain and source is shifted in the conduction (or valence band), hence reducing the total resistance of the device.

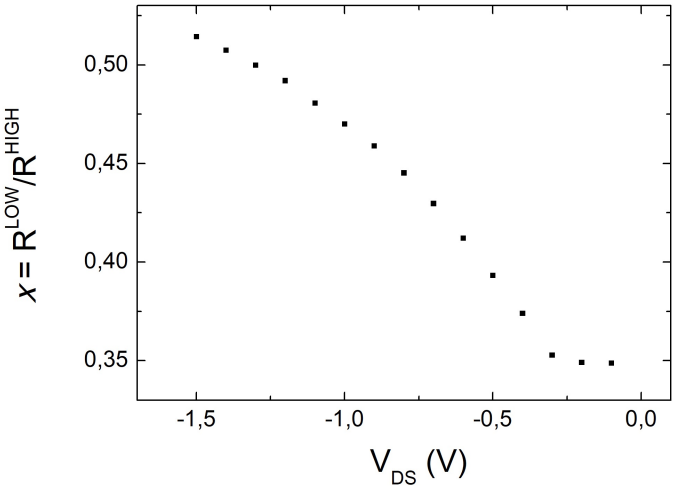


Figure 1.25: Ratio between minimum and maximum resistances as a function of V_{DS}.

if $V_{\mathrm{DS}} = 0$ V, all the resistances in series will have a high value, since the Fermi level is approximately at the Dirac point and the density of carriers is low. If V_{DS} is bigger, even at $V_{\mathrm{GS}} = V_{\mathrm{Dirac}}$, near the drain and source contacts, the Fermi level will not be at the Dirac point and the local resistance will be lower. As a result, the total resistance of the channel will be lower (b, c, d). Since the voltage difference between drain and source voltage affects the peak resistance of the GFET, it has a direct consequence on the ratio $R^{\mathrm{LOW}}/R^{\mathrm{HIGH}}$ and hence on the swing of the output of the GRTL gate. The ratio between minimum and maximum resistance, called x in 1.4, for the GFET in Fig. 1.23 is in Fig. 1.25. The swing of the output of the GRTL gate is directly related to the ratio x: the higher the ratio, the smaller the swing.

As it can be seen, the relative swing of the output gets smaller as the bias in increased. For example, at $V_{\mathrm{DS}} = -1.5$ V, that would correspond approximately to $V_{\mathrm{DD}} = -3.0$ V, the relative swing of the output would be less than 17%. As a consequence, the supply of the GRTL gate must be not too high, in order to have two clear digital levels high and low.

Finally, there are two ways to bias the RGT logic gate. In fact, with a sweep of the input voltage, it is possible to obtain either a positive or negative pulse on the output voltage. As it is shown in Fig. 1.14, the GRTL gate has two bias: V_{DD} and ground. There are two ways to apply a negative bias to the gate: firstly, the ground could be at 0 V and V_{DD} at -2.0 V. This can be called *negative pulse configuration*, since the result of a sweep of the input voltage would be a negative pulse, as in Fig. 1.26. In the other configuration, *positive pulse configuration*, the ground is the negative supply, -2.0 V, while $V_{\mathrm{DD}} = 0$ V. In this way, the pulse is positive, as in Fig. 1.26.

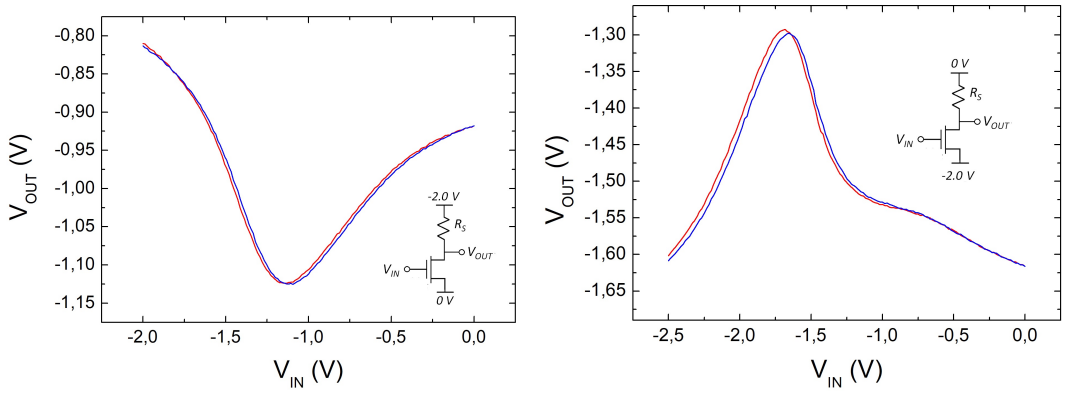


Figure 1.26: Two different supply configuration of the GRTL gate. On the left, negative pulse configuration, related to a negative pulse on the output. On the right, the positive pulse configuration, in which the pulse in positive. In blue the transfer related to un upsweep of the gate voltage, and in red the downsweep.

1.6.1 Hysteresis

Graphene is a two-dimensional material with a very low density of states at the Dirac point. As a consequence, it is extremely sensible to the surroundings, for example to adsorbed particles. One consequence is the hysteresis that affects the electronic properties of graphene. For example, the gate voltage corresponding to the charge neutrality point depends on the gate sweeping rate and range. Various explanations have been proposed to justify this behavior. Probably, it is mostly caused by the charge injection into the trap sites (for example of the Al_2O_3 oxide) or interface states [27] and by the charge transfer from the adsorbed molecules (for example of water). The charge traps are occupied by holes or electrons. Hence the electric field of the gate is screened, causing a shift in the charge neutrality point. If the gate is at a negative value and starts increasing, holes will be trapped in the oxide and the Dirac point in the channel will be reached at more negative bias. Hence, the minimum in the conductivity is shifted to the left. On the other hand, as the gate voltage becomes positive, electrons will be attracted and trapped in the oxide. As a consequence, the Dirac voltage will be reached at higher biases and the minimum conductivity point will be shifted towards positive values (Fig. 1.27). Since the trapping mechanism has a time scale of few seconds, the rate at which the transfer curve of the GFET is measured affects the strength of hysteresis. Ideally, for a very high gate sweeping rate, hysteresis coming from charge trapping should be suppressed. Moreover, also the range of sweeping can increase the hysteresis effect. The higher the voltage, the higher the electric field and the greater the density of charge that are trapped. As a consequence, the shift of the minimum in conductivity is more accentuated. Since the presence of the oxide seems to be an important factor that causes the hysteresis, in principle it

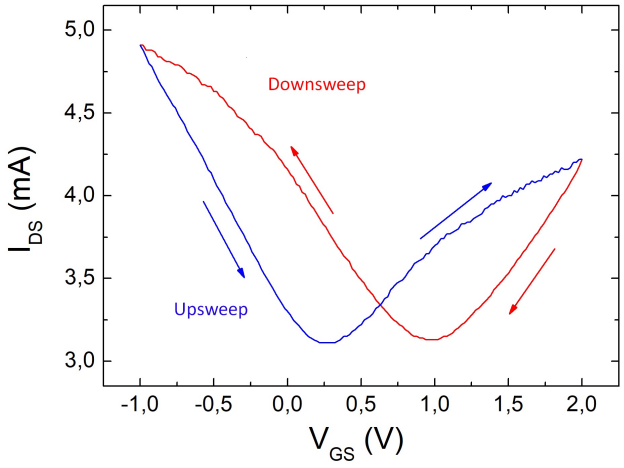


Figure 1.27: Hysteresis present in GFET devices. The transfer curve, with $V_{\mathrm{DS}} = 2.5$ V, is different if the gate voltage is increasing or decreasing. In particular, for negative (positive) gate voltage, holes (electrons) injected in the charge traps of the oxide screen the topgate electric field, causing a shift of the minimum in conductivity to the left (right).

would be possible to reduce its effect employing non oxide dielectrics, such as hBN. However, the fabrication becomes considerably difficult, since it would require the realization of hBN/Graphene hBN stacks. In certain condition the hysteresis could be opposite: the Dirac voltage may be shifted in the other direction and hence be lower for the downsweep. This could be related to capacitive gating. In fact, if a charge is induced in the channel via an electric field, the surrounding charges could polarize, enhancing the electric field itself, hence attracting even more charges. For example, during a downsweep, starting from a high voltage, electrons are present in the channel. Due to capacitive gating, more electrons will be attracted and hence the charge neutrality point will be found at a lower bias. This means that the Dirac voltage associated to the downsweep will be shifted to the left, on the contrary to what happend with the hysteresis caused by charge injection.

1.6.2 Backgate and Contact Resistance

Due to the substrate used in the fabrication, the devices can be used as dual gate GFET, since, besides the aluminum topgate, the highly doped silicon substrate can work as a backgate. However, there is an important difference between the two gates, apart from the different thickness and material of the oxide. In fact, while the top gate is local and in contact only with the graphene channel, the backgate is global: hence, applying a voltage difference between the channel and the backgate,

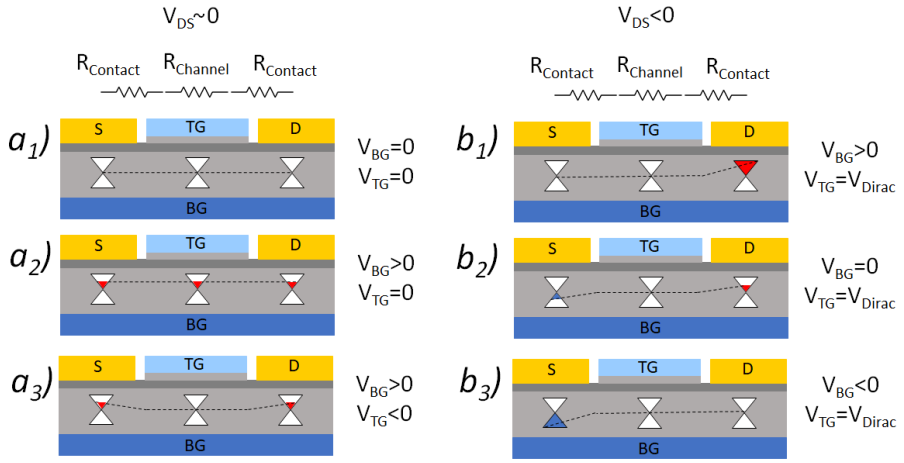


Figure 1.28: Effect of the backgate (BG) and topgate (TG) on the Fermi level in the channel and under the electrodes at negligible V_{DS} (a) and finite V_{DS} (b). The backgate voltage shifts the Fermi level everywhere, while the action of the topgate is limited to the graphene in the channel under the topgate oxide.

the electric field will affect not only the channel, but also the graphene under the electrodes. This fact has an important effect, which consists in the change of the contact resistance. In general, the total resistance of the GFET is given by the sum of the channel resistance and all the parasitic resistances, such as the contact resistance, which is the resistance coming from the metal-graphene junction and the finite density of states of graphene. The topgate can change the resistance of the channel, shifting the Fermi level and hence varying the density of carriers via its electric field. The contact resistance, on the other hand, is fixed with respect to the topgate and its effect regards the reduction in the speed of the device and the decrease of the I_{ON}/I_{OFF} ratio. However, the backgate voltage, which is global, can shift the Fermi Level of the graphene under the electrodes, changing the contact resistance and hence the total resistance of the device. As a result, if the backgate voltage is used to shift the Dirac voltage for any purpose, the change in the resistance must be taken into account. Assuming no doping induced neither in the channel nor in the graphene under the electrodes and a negligible V_{DS}, if both the topgate and the backgate are a zero voltage (Fig. 1.28, a_1), the Fermi level will be at the Dirac point both along the channel and under the electrodes. This is the condition of highest resistance, since the the graphene is almost depleted everywhere. Applying a certain backgate voltage, the electric field will shift the Fermi level both in the channel and under the electrodes (a_2). If now the topgate is used to bring the Fermi level back to the Dirac point (a_3), only in the channel, the total resistance will now be lower than before, since the contact resistance is lower, owing to the fact that, under the electrodes, the Fermi level is not at the Dirac point [26].

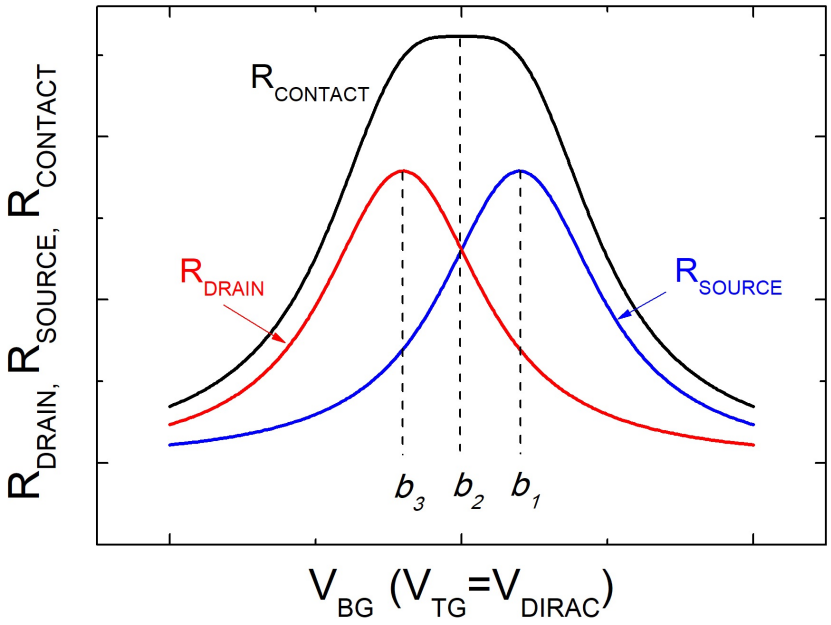


Figure 1.29: Contact resistance as a function of the backgate voltage (V_{BG}), when the topgate voltage V_{TG} is such that the Fermi level in the channel is at the Dirac point (minimum conductivity). The drain contact resistance, in red, has a maximum at b_3, when the Fermi level is at the Dirac point under the drain contact. The source contact resistance, for the same reason, has a maximum at b_1. The sum of the two, R_{CONTACT} will have two peaks, or, as here, a broad peak, in black.

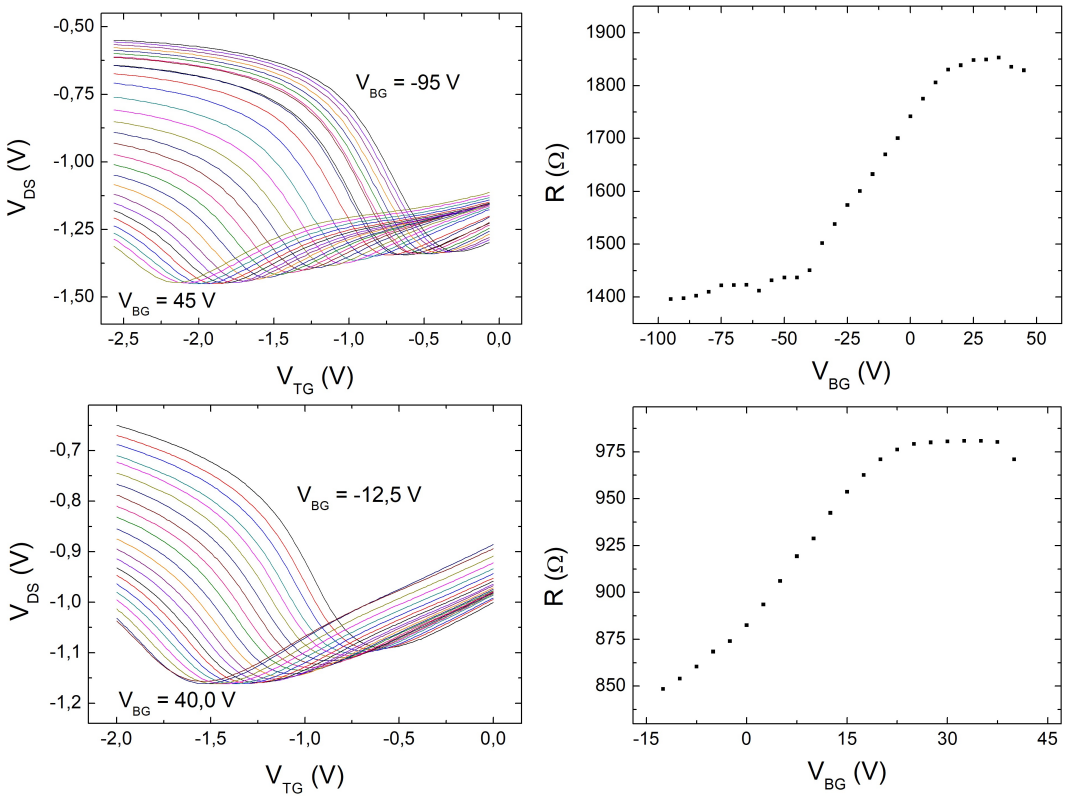


Figure 1.30: On the left: shift of the transfer curves of two GRTL gates as a function of the backgate voltage. The two GFETs employed had a peak resistance of 1600 Ω (the one above) and 850 Ω (the one below). The series resistances are respectively 700 Ω and 708 Ω, while the supply of the GRTL gate is -2.0 V.

With a finite V_{DS}, for example lower than zero as in Fig. 1.28 b), the depletion under the two electrodes (source and drain) is reached at two different V_{BG}. For example, the resistance at the drain contact in b_1 will be lower than the source contact resistance, which is, on the contrary, at its maximum value. Eventually, the total contact resistance, which is the sum of the two contact resistances (drain and source) will present two peaks, or, if the two peaks are close, a unique broad peak, as it can be seen in Fig. 1.29. Given the dependence of the contact resistance on the backgate, as a result, the total resistance of the GFET at the Dirac voltage changes and the transfer curve of the device will be shifted upwards or downwards. For example, as it can be seen in Fig. 1.30, apart from the shift to the left associated to the electrical doping of the backgate, the transfer curve, as the backgate voltage increases, moves downwards. This in caused by the increase in the resistance of the two junctions graphene-electrode. The change in the resistance with respect to the backgate voltage is shown in Fig. 1.30 too: this change is coherent with the theoretical explanation given above.

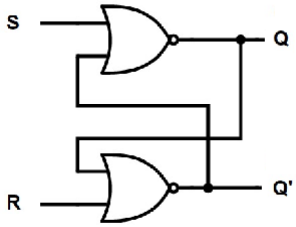
The change in the resistance could be a problem in the case in which it is necessary to have a fixed value for the output voltage at the Dirac voltage. In this case, it would be necessary to change the fabrication process, realizing a local backgate that do not affect the graphene under the electrodes.

Chapter 2

Single-Dual Edge Triggered Flip-Flop

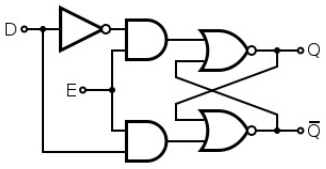
2.1 Introduction to Flip-Flops

Flip-flops are the building blocks or a variety of electronic digital circuits: for example, they can be used to store a bit of information in the registers of a processor. Together with latches, they consist in bistable circuits that can switch between two different stable states depending on the values of their inputs [28]. In particular, flip-flops change state only as a response to the edges of a signal called clock. Instead, a latch is a bistable circuit that does not have a clock input and changes state according only to its data input. There are several types of latches and flip-flops and the simplest member of this family of memory elements is the SR Latch, whose name comes from its two inputs, which are the Set and the Reset inputs. This latch, whose schematic and truth table are shown in Fig. 2.1, consists of two NOR gates; the output of each of these gates constitutes one of the inputs of the other one. If both the inputs S and R are 0, the latch holds its present state, whatever it is 1 or 0. If $S = 1$ and $R = 0$, the output Q becomes 1 if previously it was 0 and holds its state if it was already 1. On the contrary, if $S = 0$ and



S	R	Q
0	0	Hold state
1	0	1
0	1	0
1	1	Not allowed

Figure 2.1: Left: schematics of the SR Latch. Right: truth table of the SR Latch.



D	E	Q
0	0	Hold state
1	0	Hold state
0	1	0
1	1	1

Figure 2.2: Left: schematics of the D Latch. Right: truth table of the D Latch

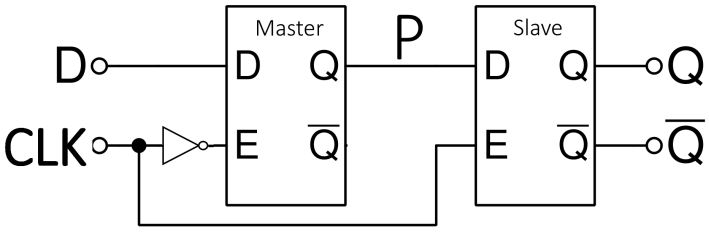
$R = 1$, the output $Q = 0$. If both the input $S = R = 1$, both Q and $\overline{Q}$ are 1. This condition, that can lead to an uncontrollable oscillation, goes against the logic of a latch, in which Q and $\overline{Q}$ must be opposite, and therefore must be avoided. The characteristic equation of the SR latch, which gives the output of the latch as a function of its input and its previous state, can be demonstrated to be:

$$Q^+ = S + \overline{R}Q \qquad (SR = 0) \tag{2.1}$$

which means that the output of the latch Q^+ is 1 only in due conditions: if $S = 1$ or if $R = 0$ and the previous state Q was 1, provided that S and R are not 1 at the same time. One way to avoid this condition is to use a gated latch as the one in Fig. 2.2, which is called gated D latch. A gated latch has an additional input E, called gate or enable, which doesn't allow the latch to change if E=0. A D latch, moreover, has a D input which is connected to S and to $\overline{R}$. In this way, whatever the value of D, it is not possible to be in the condition $R = S = 1$. The characteristic equation of the D latch is the following:

$$Q^+ = \overline{E}Q + ED \tag{2.2}$$

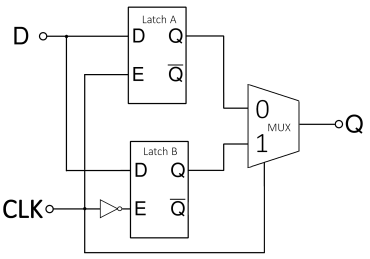
The output of the latch Q^+ becomes equal to the input D after a propagation delay, whenever the enable input is activated. In particular, the propagation delay depends on the critical path from the D to Q: in a D latch, consequently, in the worst case, the propagation delay is given by the series of a NOT gate, an AND gate and a NOR gate. Finally, the D latch is also called transparent latch, since the output depends continuously on the input, if the enable input is 1. In a clocked system, it is necessary that memory devices, such as latches and flip-flops, are synchronized to an edge of the clock signal, which means that their output can change only during either the 1 to 0 or the 0 to 1 transition of the clock signal. A circuit like this is called edge triggered flip-flop and one example is the edge triggered D flip-flop, which can be constructed from two D latches and a NOT gate, as in Fig. 2.3. When the clock is 0, the first latch, called master, is transparent and D is written and held at the output, P. The second latch, the slave, is disabled, since its enable input is 0. As the clock has a rising-edge, the



Clock	Q
0-1	Hold state
⌝⌞	Hold state
⌟⌜	D

Figure 2.3: Above: schematics of D flip-flop. The two boxes are the common symbol used to indicate a D latch. In a D flip-flop, the output of the first (master) latch is the input of the second (slave). The clock is connected to the master latch via a NOT gate and directly to the slave latch. Below: truth table of the D flip-flop.

master latch is disabled, while the slave, now enabled, writes its input P on the output Q, which represents also the output of the flip-flop. Therefore, the data input are written on the output at every rising edge of the clock. During the falling edge, the slave latch is disabled and the master latch is enabled: hence, even if P changes, it will not be written on the output of the flip-flop until the next rising edge. In this circuit the propagation delay is defined as the delay between the active edge (in this particular case, the rising edge) and the change in the output. Moreover, other important timing parameters are the setup time and the hold time: the former is related to the time in which the D input must be stable before the active edge, while the former is related to the time in which D must be held constant after the active edge, in order to have a proper behavior of the flip-flop. In a flip-flop such as the one described above, which is called single edge triggered flip-flop (SETFF), the data throughput depends on the frequency of the clock: hence, in order to increase the former, it is necessary to increase the latter. However, high frequency clocks have a series of drawbacks in terms of stability, uncertainty and power consumption. For this reason, double edge triggered flip-flops (DETFF), which are storage elements that changes state at every edge of the clock, have been proposed and studied [29]. With these devices, it is possible to obtain the same data throughput employing a clock with half the frequency of the clock that would be used in a standard SETFF. However, DETFFs have some disadvantages too, for example the design complexity. An example of a DETFF is the Latch-Multiplexer DETFF, shown in Fig. 2.4. In this circuit, the latch A is transparent



Clock	QA	QB	Q
0	D^-	D	QA - hold
1	D	D^-	QB - hold
⌞	D	D	QA - D
⌟	D	D	QB - D

Figure 2.4: Schematics and truth table of the Latch-Multiplexer DETFF. Input data D are written at every edge of the clock.

on the positive semi-period of the clock, while the latch B is transparent on the negative semi-period. However, the clock signal is used to select the channel of the multiplexer (MUX) which is connected to the actual non-transparent latch. In this way, data can pass through the latches and the MUX only at both the edges of the clock, while the output is held during the two semi-periods.

In the following sections, new circuits employing the GRTL gate that can act as SETFF, DETFF or both (SDETFF) will be presented.

2.2 Graphene-CMOS DETFF

The easiest circuit that can be designed with the GRTL gate is a DETFF that consists only of the component itself and a D latch. The circuit is shown in Fig. 2.5. The input of the GRTL gate is connected to the clock signal, while the output is connected to the enable input of the latch. The GRTL gate is in the positive pulse configuration. In this way, if the clock is in the high 1 or low 0 state the latch is not enabled and it holds its state. On the contrary, during both the edges of the clock, there is a pulse at the enable input, the latch is transparent and data D are written on the output Q. In this case, consequently, the GRTL gate behaves as a pulse generator and the circuit becomes a DETFF. This circuit is significantly simpler compared to the Latch-Mux DETFF. The critical path between data D and output Q is reduced from the series of a latch and a MUX [29] to only a single latch. The propagation delay from the edge of the clock to the change in the output decreases from the sum of the delays in the series of NOT gate, latch and MUX to the sum of delays of the GRTL gate and latch.

The experimental demonstration of this circuit was done employing a GFET, which was fabricated as described in the section 1.5 and whose transfer curve is shown in Fig. 2.6. The GFET was connected to the other discrete elements of the circuit on a testboard via BNC cables and testboard wires. The latch used was a Toshiba 74HCC375AP. The clock and data signal were generated with a Tektronix AFG3022B dual channel arbitrary function generator, while the waveforms were measured with a Agilent Technology Infinium DS09064 Digital Storage. The

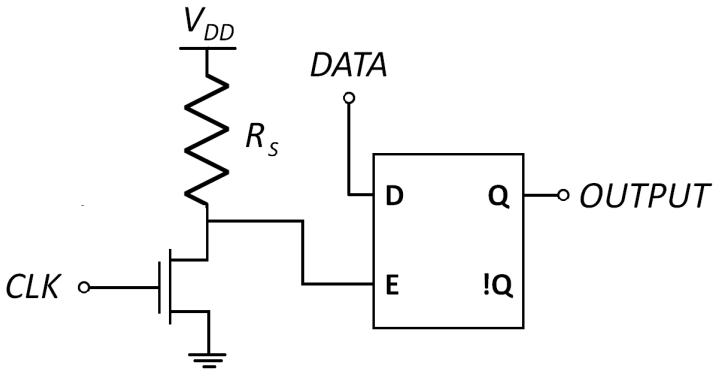


Figure 2.5: Schematics of the proposed graphene-CMOS DETFF. The output of the GRTL gate is connected to the enable input of the latch: in this way, the latch is enabled at every edge of the clock.

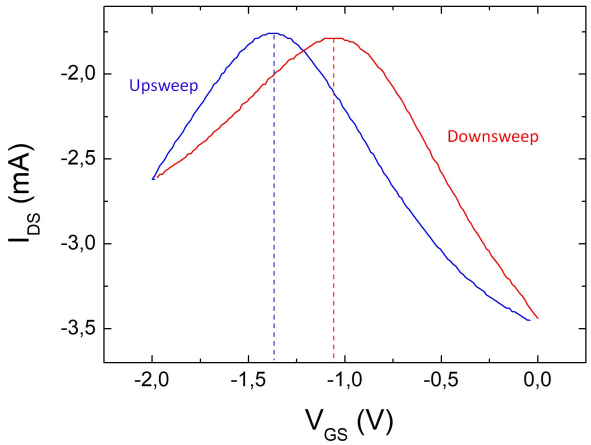


Figure 2.6: Transfer curve of the GFET employed in the DETFF circuit. As it can be seen, the hysteresis is significantly strong. The transfer curve has been measured with $V_{\mathrm{DS}} = -1.5$ V. In these conditions, the Dirac voltage for the upsweep (downsweep) is around -1.37 V (-1.06 V) and the maximum resistance is 850 Ω (840 Ω).

supplies of the GRTL gate and of the latch were generated separately with two Keithley 2611A. As it is explained in 1.4, the supplies must be negative: in particular, the supply of the GRTL gate is [-2.0 V, 0 V] (positive pulse configuration), while the negative and positive supplies of the latch are respectively -2.5 V and 0 V. Since the swing on the output of the GRTL gate in the worst condition was found to be approximately 100 mV, the series resistance R_s had to be tuned in order to have a proper operation of the device. In fact, when the clock is either in the positive or negative semi-period, the output of the GRTL gate must be below the threshold of the latch; by contrast, at the two edges of the clock the same output must be above the threshold. Given the threshold of the latch around -1.29 V and resistance at the Dirac voltage measured as in Fig. 2.6, a proper operation can be obtained with $R_s = 1260\ \Omega$. It should be noticed that there may be differences between the values of the resistances at the Dirac voltage between the measurement carried out with the Keithley 2611A and the values during the operation in the flip-flop circuit. In fact, the V_{DS} will not be fixed and equal to -1.5 V as in the transfer curve measurement, hence the Dirac point and the peak resistance could slightly change. Moreover, the frequency of sweeping of the gate is higher and hence hysteresis could affect the electronic properties of the GFET during operation.

Fig. 2.7 shows the measured waveforms related to the DETFF. The clock signal (in black) has a frequency of 1 MHz and a shift of -30°, with trailing and leading edges of 200 ns. Given the limited bandwidth of the system, mainly resulting from the poor connections and the discrete components, shorter trailing and leading edges would have suppressed the pulses. The data signal (in red) has a frequency of 333 KHz, with no delay. The enable signal (or output of the GRTL gate, in green) presents a pulse above the threshold (red horizontal line) at every edge of the clock: during these windows of time, the latch is enabled and the output changes according to the data signal. In particular the light blue areas correspond to a rising edge of the clock, while the orange area is related to the falling edge. The pulses associated to rising and falling edges are clearly different: this is due to the hysteresis of the device (1.6.1). Moreover, ideally, the pulse of the enable signal should happen when the clock is at -1.25 V, which is the middle level of the supply range of the latch. However, the peak in the resistance of the GFET is not in the center of the range of the gate voltages (-2.5 V, 0 V), but it is shifted towards -2.5 V. Adding the propagation delay of the GRTL gate, the result is that the peak of the pulse associated with a rising (falling) edge is 21 ns (78 ns) after the instant at which the clock is at -1.25 V. However, the enable signal goes above the threshold before reaching the peak: hence it is possible to define the propagation delay of the GRTL gate as the time between the instant at which the clock is at -1.25 V and the instant at which the enable hits the threshold from below.

$$t_{delay} = t_{th} - t_{clk} \quad V_{ENABLE}(t_{th}) = V_{th} \quad V_{CLK}(t_{clk}) = -1.25\ \text{V} \tag{2.3}$$

For the rising (falling) edge this propagation delay is -46 ns (41 ns). It has to be

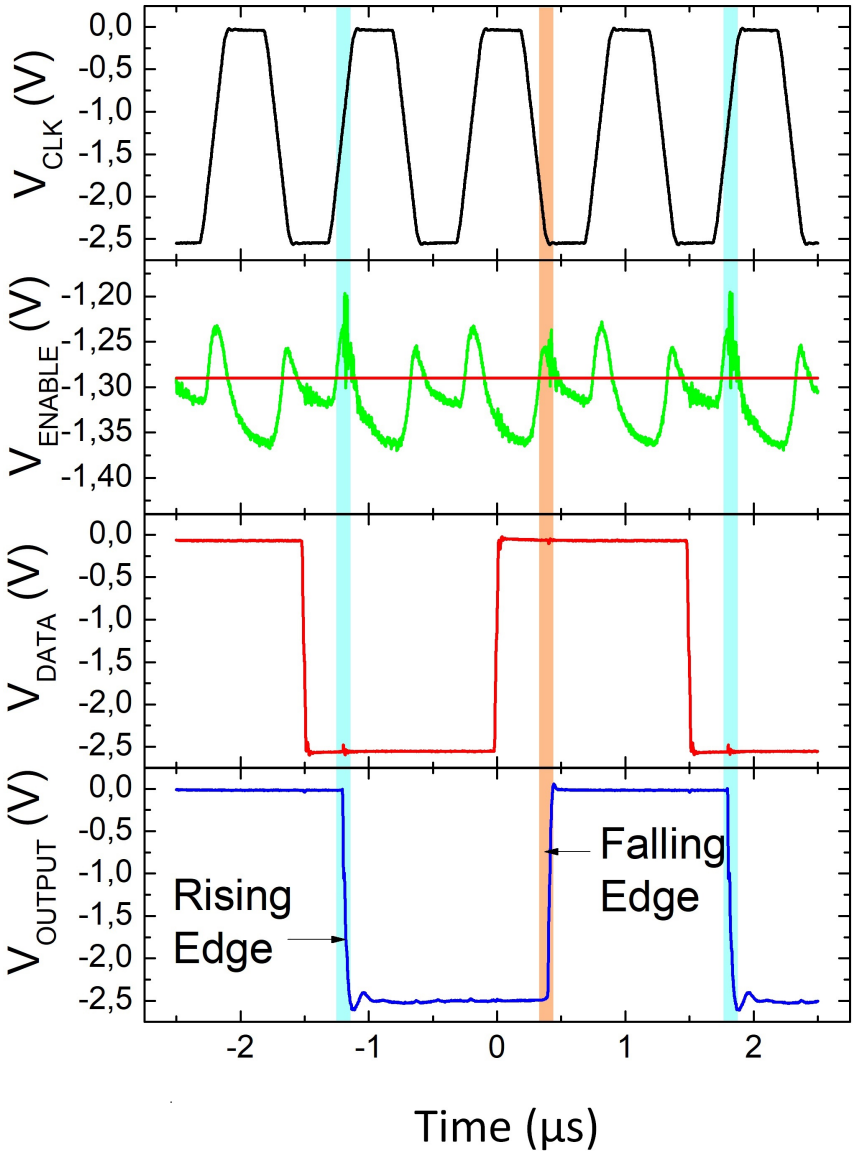


Figure 2.7: Digital waveforms related to the circuit in 2.5. The clock signal (in black) has a frequency of 1 MHz; the output of the GRTL gate (in green) presents a pulse at every edge of the clock. The pulses enable the latch and the output (in blue) can change according ot the data input (in red).

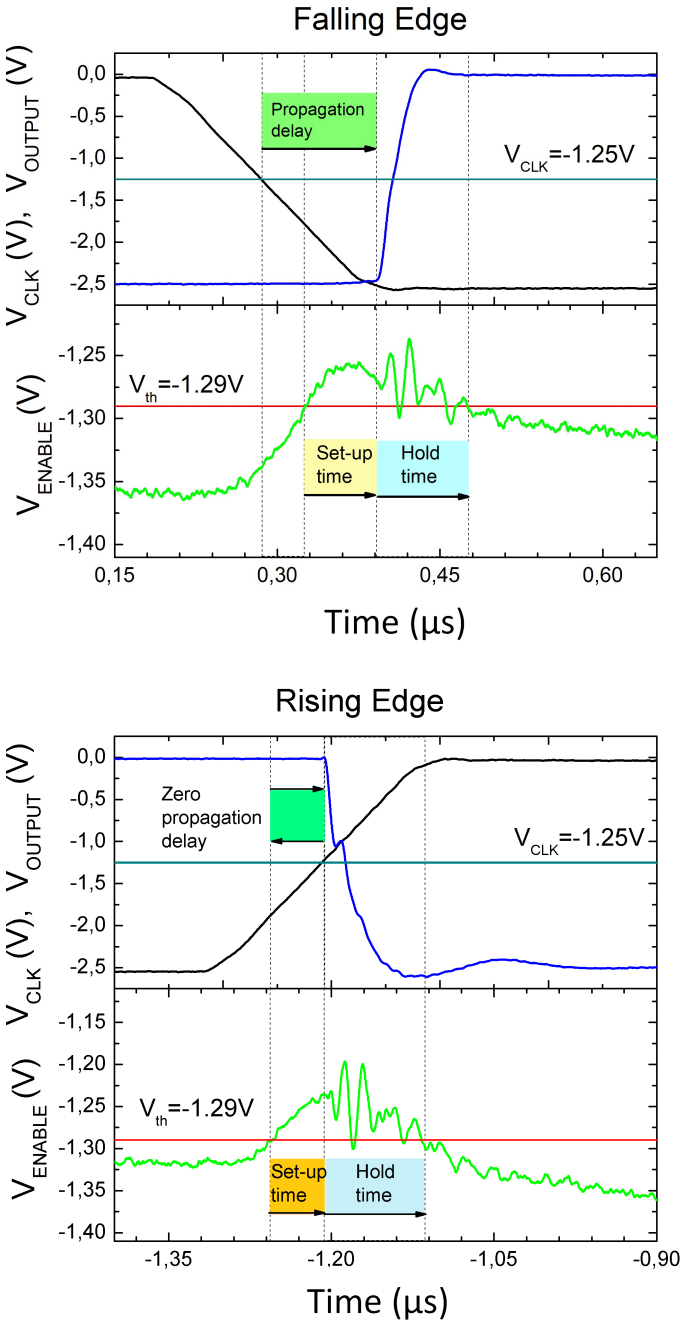


Figure 2.8: Important time parameters of the DETFF: propagation time, set-up time and hold time.

noticed that the propagation delay related to the rising edge is negative: in fact, due to the fact that the Dirac voltage is closer to -2.5 V than to 0 V, the enable signal goes above the threshold before the instant at which the clock is at -1.25 V. Moreover, this delay is strongly dependent on the duration of the trailing and leading edges and hence can be significantly reduced in a integrated circuit.

The output of the latch does not change immediately after the enable is above the threshold, but with a certain delay. This delay depends on the propagation delay of the latch itself and on the voltage of the enable signal: in fact, the enable signal is only slightly above the threshold. In general, the higher the enable signal in the high state (ideally it should be 0), the smaller the delay. For the rising edge, the pulse is higher and the delay is around 46 ns; for the falling edge, the pulse is smaller and the delay is around 66 ns. Summing all the delays, the total propagation delay of the DETFF is around 107 ns for the falling edge and 0 ns for the rising edge.

The data signal must be stable for a certain period of time before the edges of the clock, to ensure a proper operation of the device. This period is called set-up time. In the proposed device, the data signal must be stable starting at least from the moment at which the pulse of the enable signal hits the threshold and depends only on the latch. The total set-up time of the DETFF is hence the same of the one of the latch itself. Another parameter to characterize the DETFF is the hold-time, which is the interval of time after edge in which the data input must be held to ensure proper operation of the device. Again, in this case we can define it as the interval between the moment in which the clock is at -1.25 V and the instant at which the enable signal decreases and hits the threshold from above. For this period, in fact, the latch is transparent and a change in the data input would propagate to the output. For the rising (falling) edge, the measured hold time is 92 ns (190 ns).

2.3 Graphene-CMOS SETFF

In some applications, it is necessary to have a flip-flop that changes state only on one edge. It is still possible to obtain a SETFF with the same circuit employed for the DETFF with the addition of an AND gate. As it can be seen in the circuit shown in Fig. 2.9, the inputs of the AND gate are the output of the GRTL gate and the clock signal, delayed with a delay stage.

Given the truth table of an AND gate, the output is high only if all the inputs are high: in this case, there will be a pulse at the output of the AND gate only at the falling edge of the clock. In fact, the input related to the GRTL gate will be high at every edge of the clock, but the input related to the delayed clock will be high only after a falling edge and not after a rising edge. Hence, the circuit works as a SETFF. It has to be noticed that this circuits employs only one latch, an AND gate and the GRTL gate: the other common SETFF circuit needs two latches and a NOT gate. The critical path from data to output consists only in

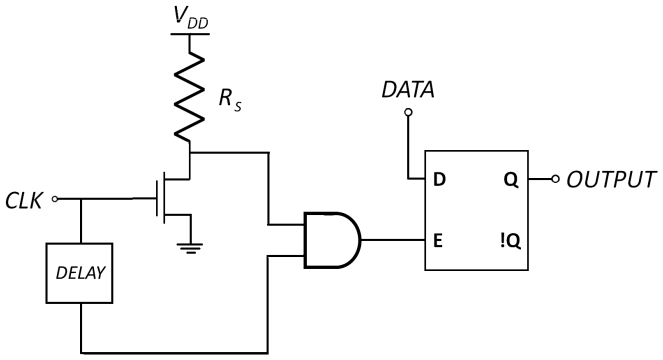


Figure 2.9: Schematics of the proposed graphene-CMOS SETFF: the additional AND gate is used to select only a series of pulses at the output of the GRTL gate.

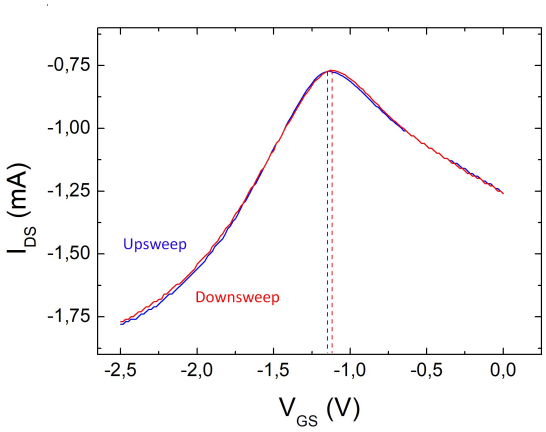


Figure 2.10: Transfer curve of the GFET used in the SETFF circuit at $V_{\mathrm{DS}} = -1.25$ V. Compared to the GFET of Fig. 2.6, the hysteresis is less important, almost negligible. In fact the Dirac voltage for downsweep and upsweep are -1.14 V and -1.16 V respectively. The resistances at the Dirac voltage are both around 1620 Ω. At the two extremes ($V_{\mathrm{GS}} = -2.5$ V or 0 V), the resistances are 705 Ω and 1000 Ω.

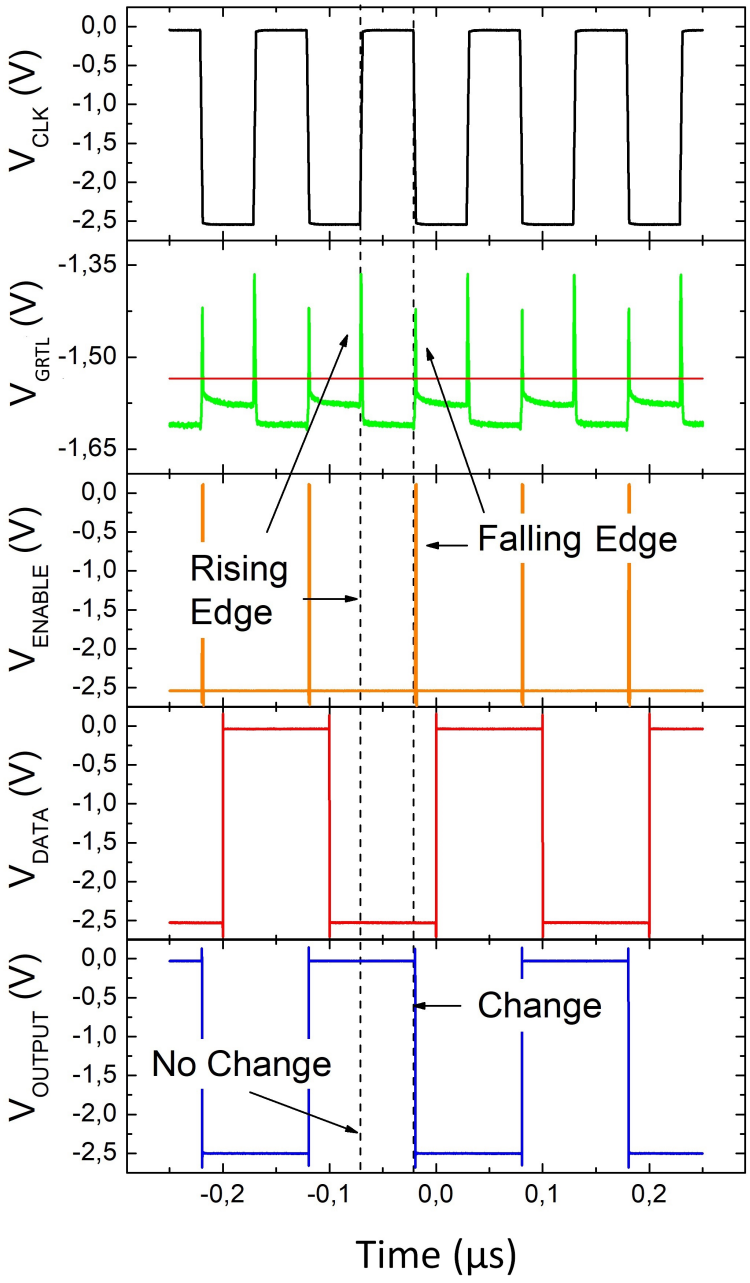


Figure 2.11: Digital waveforms of the SETFF: the output of the GRTL gate (in green) has a pulse at every edge of the clock (in black), but only the pulses associated to a falling edge generate a pulse at the output of the AND gate (orange). Hence, the output of the latch (in blue) changes only at the falling edge of the clock, following the data input (in red).

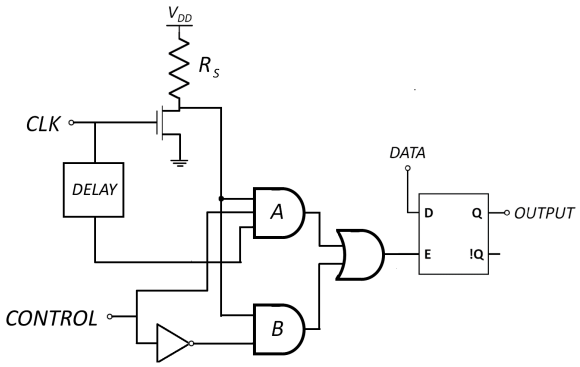


Figure 2.12: Schematics of the SDETFF: the control bit is used to select the operation as a SETFF or as a DETFF.

the latch, while the propagation delay is the sum of the delays introduced by the GRTL gate, the AND gate and the latch itself. The transfer curve of GFET used in the experimental demonstration is shown in Fig. 2.10. The other components are the same as in the previous section about the DETFF, with the addition of the TI CD74HC21E AND gate, which has a threshold $V_{\mathrm{th}} = -1.535$ V with a supply [-2.5 V, 0 V]. For this reason, given the resistance of the GFET at the Dirac voltage (1620 Ω) and the resistances at the two extremes (lower than 1000 Ω), the series resistance of the GFET must be equal to $R_{\mathrm{s}} = 2900$ Ω in order to have a swing of the GRTL gate output that crosses the threshold. The delay stage was realized with an RC circuit ($R = 4700$ Ω and $C = 1$ nF). An example of operation is shown in Fig. 2.11. The frequency of the clock (in black) is 10 kHz, with trailing and leading edges of 2.5 μs. The data signal (in red) has a frequency of 5 kHz and a 50° delay with respect to the clock. The orange signal is the output of the AND gate, connected to the enable input of the latch: for every pulse of the GRTL gate output (green) associated with a negative edge, there is a pulse that activate the latch and the output (in blue) changes according to the data input. On the other hand, there is no change for a rising edge.

2.4 SDETFF with Control bit

The two functionalities presented in the previous sections can be joint in a unique circuit that can work either as a DETFF or as a SETFF, depending on the value of an additional input, called control bit. As it can be observed in Fig. 2.12, the circuit has now two AND gates. The one above (A) has three inputs: the output of the GRTL gate, the delayed clock and the control input. If the latter is high and the clock is at the falling edge, the output of the AND gate will be high. By contrast, the AND gate (B) below has only two inputs: the output of the GRTL gate and the opposite of the control input (via the NOT gate). In this

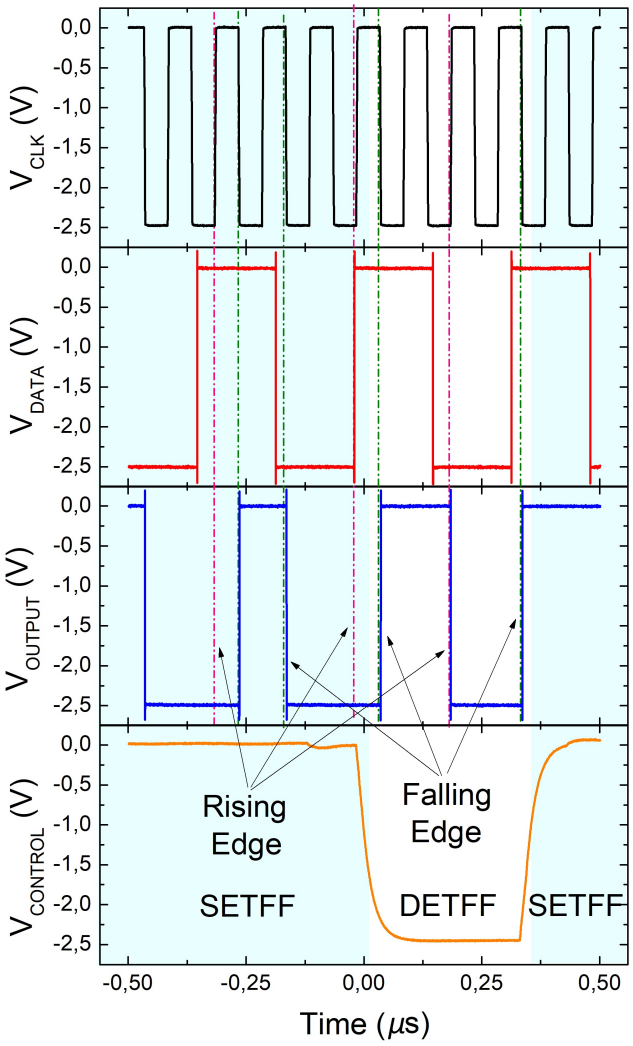


Figure 2.13: Digital waveforms of the SDETFF in 2.12. When the control bit (in orange) is high, the circuit is a SETFF and data (red) are written to the output (blue) only on the falling edge (green vertical lines) of the clock (black). When the control bit is low, the circuit works as a DETFF and the output changes at every edge (green and pink vertical lines).

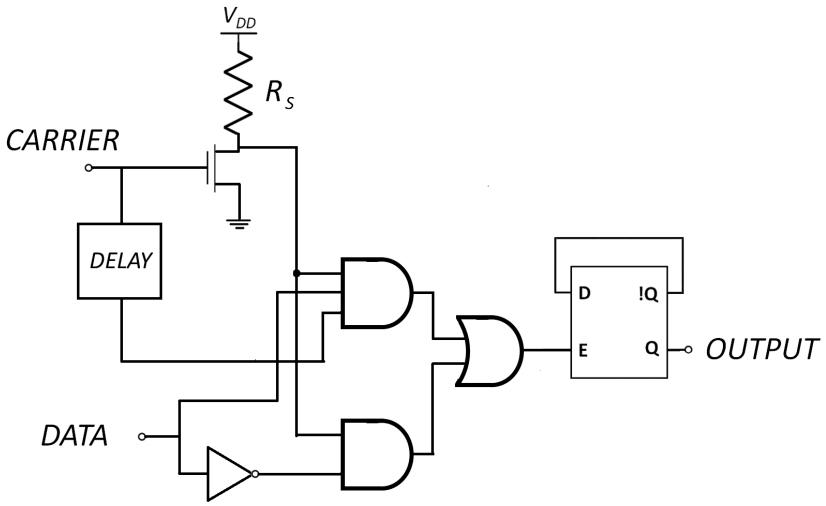


Figure 2.14: Schematics of the circuit used as a frequency modulator. The data input corresponds to the control input of the SDETFF, while the carrier is the clock input. The complementary output of the latch is feedback to the input of the latch itself.

way, the output of the AND gate below will be high on every edge of the clock, only if the control input is low. An OR gate is used to connect the outputs of the two AND gates to the enable input of the latch. In conclusion, if the control input is high, the circuit behaves as a SETFF; if the control input is low, it works as a DETFF. The total number of gates employed is only eight, less than in a D master-slave flip-flop. In the experimental demonstration the same GFET and R_s as in 2.3 were used. The additional gates (NOT and OR) were realized with TI AND gates CD74HC21E and NOR gates CD74HC4002EE4. The results are shown in Fig. 2.13: the control bit consists in a negative pulse generated with a Keithley 2611A.

2.5 Application: Binary Frequency-Shift Keying

Digital bandpass modulation is the process in which the properties, such as amplitude, phase or frequency, of a sinusoidal or square waveform called carrier are modified in order to allow the transmission of information. In particular, depending on the data that has to be transmitted (*i.e.,* a one or a zero), the properties of the carrier, for example the frequency, changes. This particular example is called frequency modulation and the technique used to transmit information via the modulation of frequency is known as frequency-shift keying [30]. In general, a system could be able to transmit multiple discrete levels, but in a digital system the levels are only two. In this case we thus talk about binary frequency-shift keying (BFSK): the carrier can have two different frequencies and each of them

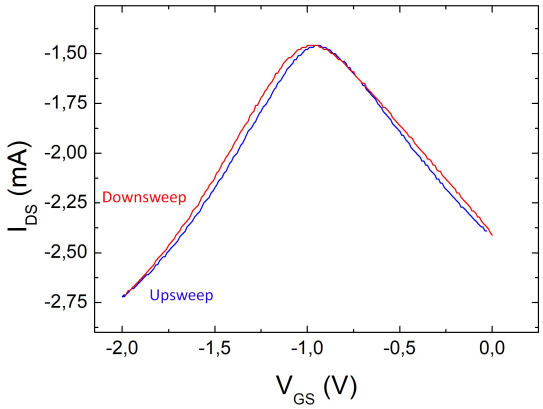


Figure 2.15: Transfer curve of the GFET used in the BFSK circuit, at $V_{\mathrm{DS}} = -1.5$ V . The Dirac voltage is around -0.95 V and the peak resistance is 1030 Ω.

is associated either to a one or to a zero. The SDETFF circuit proposed in this chapter can be used to obtain a frequency modulator of this kind, employing the circuit in Fig. 2.14. In this circuit, the complementary output of the latch is feedback to the input of the latch itself. In this way, whenever the enable input is high, the latch changes state. If the control input is high, the latch is enabled only at the negative edge of the clock: hence, the latch will change state only one every other edge of the clock. The frequency of the output, consequently, will be half of the frequency of the clock. On the contrary, if the contol input is low, the latch changes state at every edge of the clock and the output of the latch will be a square wave with the same frequency of the clock. Hence, it is possible to change the frequency of the carrier depending on the value of the control bit, which can then be considered as a data input.

An example of the operation of this circuit is given in Fig. 2.16. The transfer curve of the GFET employed is shown in Fig. 2.15. The peak resistance at the Dirac voltage is 1030 Ω. The series resistance is $R_{\mathrm{s}} = 1100$ Ω. The experimental setup is the same as in the previous sections, with a difference in the supply of the components. In fact, also the supply of the GRTL gate is [-2.5 V, 0 V] and hence only one bias line is necessary. For the measurement, the clock signal (the carrier) has a frequency of 100 kHz, with trailing and leading edges of 1 μs. The data signal (connected to the control input), has a frequency of 5 kHz. The delay stage for the clock is again a RC circuit ($R = 2200$ Ω, $C = 1$ nF). All the logic gates and the latch are the same as in 2.4. Moreover, a delay stage is needed on the complementary Q - D feedback, in order to avoid multiple switching of the latch. In fact, during the pulses at the enable input, the latch is enabled and it would continuously changing state, limited only by its propagation delay. Hence, in order to have only one change of the state during the pulse, an RC circuit is

used to slow down the change at the data input. In particular, $R_{\mathrm{FB}} = 6200\ \Omega$ and $C_{\mathrm{FB}} = 1$ nF. Clearly, those values should be changed according to the frequency of the carrier.

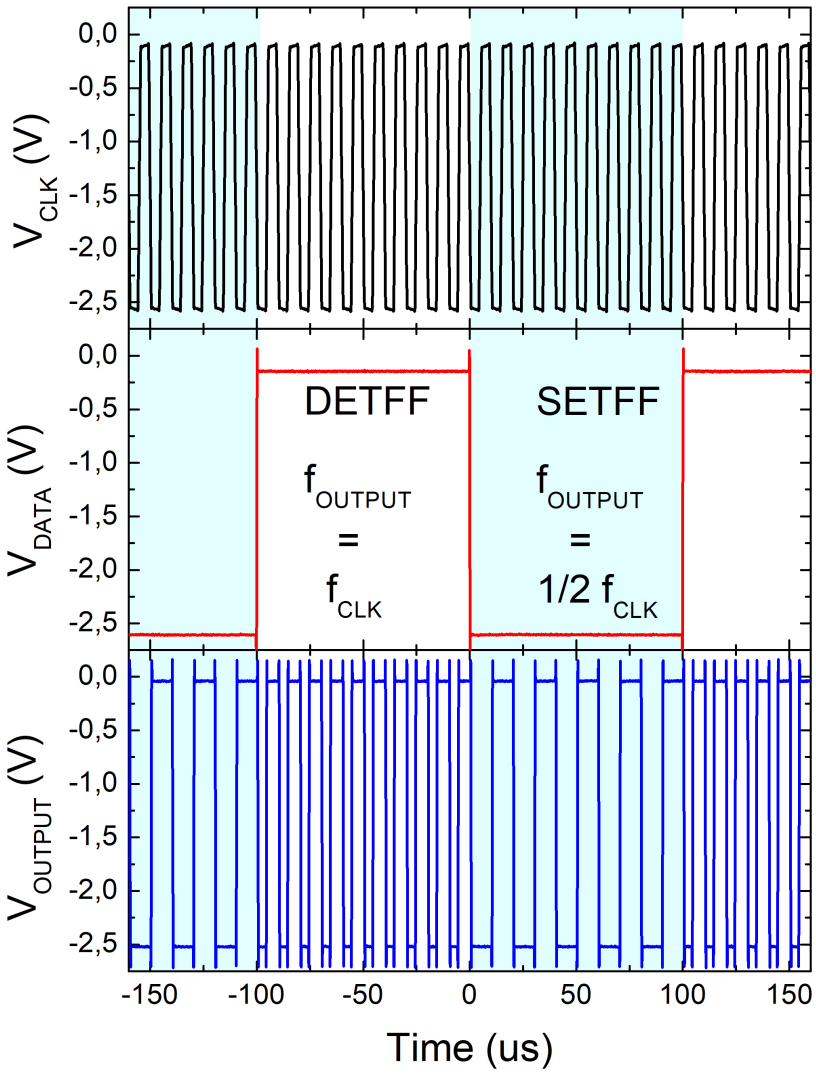


Figure 2.16: Digital waveforms of the circuit used in a binary frequency-shift keying scheme: the clock (in black) is the original carrier signal, which is modulated by the data signal (in red). The final carrier signal (in blue) has a frequency which is equal to the clock if the data input is one and is only half of that frequency if the data input is zero.

The flip-flop circuits proposed have many advantages with respect to the circuits that employ only Si CMOS components. Firstly, all the circuits employ very few components. For example, the hybrid graphene-CMOS DETFF employs only a latch (4 logic gates) and a GFET; by contrast, the most common Si CMOS SETFF requires ten logic gates and the Si CMOS DETFF circuits are even more complicated. Given this reduction in complexity and in number of components used, the hybrid graphene-CMOS circuits proposed could be useful to reduce the size of the integrated circuits containing huge number of flip-flops, as well as to reduce the propagation delays, hence increasing the speed of the whole circuit. Additionally, in Si CMOS, the SETFF and DETFF circuits are completely different and cannot be combined without increasing the complexity of the circuit. On the contrary, the hybrid SETFF and DETFF are based on the same idea, hence they can easily combined in order to obtain the SDETFF: this new circuit offers new functionalities that could be useful for example in the registers of a processor, such as the arbitrary switching between two different frequency of data processing.

However, the presence of GFETs has also an important drawback: the power dissipation. Even if it would be possible to open a bandgap, the operation of the RTL and the fact that the Dirac voltage must be in the middle of the supply window does not allow to reduce the dissipated power. However, there is only one GFET in all the circuits proposed and, moreover, in a hypothetical integrated circuit, the GFET should be fabricated on a second layer above the Si layer and only one GFET could works as a pulse generator for every flip-flop in the circuit. Hence the power dissipation could be not as important as in a common integrated circuit.

Chapter 3

Graphene-CMOS Dirac Oscillator

3.1 Introduction to Relaxation Oscillators

An oscillator is a circuit that is able to generate and sustain a periodic signal. There exist different types of oscillator, depending on the nature of the circuit and on the waveform of the periodic signal. The term oscillator commonly refers to a generator of a sinusoidal waveform: for example, a circuit realized with an operational amplifier with a positive feedback greater than 1 could sustain such an oscillation. The circuits able to generate square waveforms, on the other hand, are called astable multivibrator or relaxation oscillator [31][32]. In these circuits, there is an active device which presents two states and the oscillation is given by the continuous switching between these two states. An example of this kind of circuit is the Schmitt trigger oscillator, whose schematic is shown in Fig. 3.1. In this case, the active device is a Schmitt trigger inverter, which works as a comparator with hysteresis. In fact, there are two thresholds: if the voltage input is greater that an upper threshold, the output of the inverter will be low (close to the negative supply of the inverter). On the contrary, if the input voltage is smaller than a

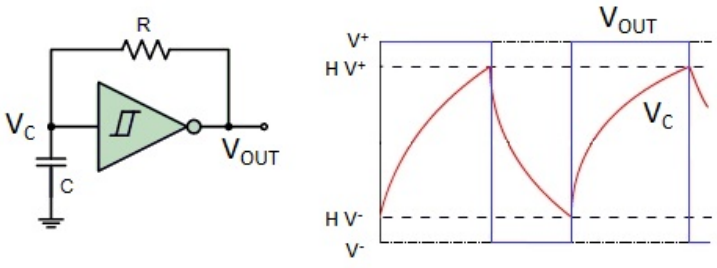


Figure 3.1: Right: schematics of the Schmitt trigger oscillator. Left: waveforms associated to the oscillator: when the output is in the high (low) state, the voltage on the capacitor increases (decreases) until it reaches the upper (lower) threshold of the inverter, causing a change in the state

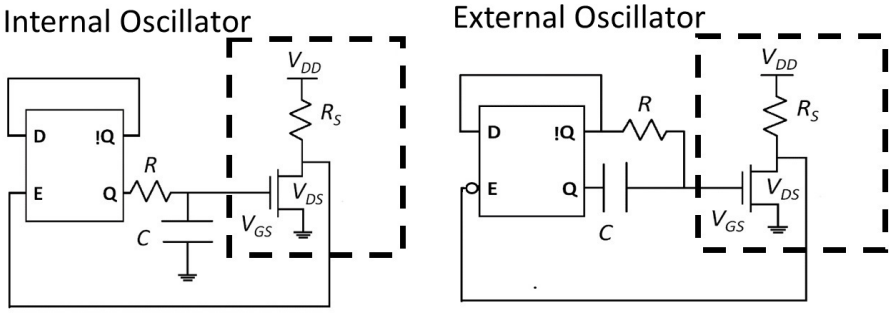


Figure 3.2: Schematics for the Internal Dirac Oscillator (on the left) and External Dirac Oscillator (on the right). The GRTL gate is highlighted in the dashed box and is biased in the negative pulse configuration.

lower threshold, the output will be high (close to the positive supply). When the output changes from V^- to V^+, the voltage on the capacitor starts increasing with a time constant $\tau = RC$ until it reaches the threshold HV^+; the output of the inverter changes and consequently the capacitor starts decreasing, until the lower threshold, leading to the oscillation. In particular, the frequency of oscillation depends on the two thresholds and on the time constant of the RC circuit. In the following sections, a new oscillator circuit, employing the GRTL gate discussed in the previous chapters, will be presented.

3.2 Principles of Internal Dirac Oscillator and External Dirac Oscillator

The ambipolar electric field effect of graphene allows to design two circuits able to sustain stable oscillations and work as relaxation oscillators. The two circuits are shown in Fig. 3.2. In the Internal Dirac Oscillator (IDO), on the left, the CMOS latch (see Section 2.1 for a description of this component) has a positive feedback from the complementary output to the data input. In this way, whenever the latch is enabled (*i.e.,* E is above the threshold), the latch changes state. The output is connected to an RC circuit: if the state of the latch changes for example from low to high, the node that corresponds to the GFET gate voltage stars increasing, with a time constant $\tau = RC$. The GRTL gate is designed to assure that the Dirac voltage of the GFET is reached within the range of the V_{GS}, which corresponds to the supply range of the latch. Moreover, the GRTL gate is in the negative pulse configuration. As it can be seen in Fig. 3.3, in the red area, when the oscillation is about to start, the gate voltage is below the point B and the drain voltage (*i.e.,* the output voltage of the GRTL gate) is above the threshold of the latch (assumed to be around -1.0 V). Hence the latch is enabled. The state of the latch changes and the gate voltage starts increasing, becoming greater than the voltage

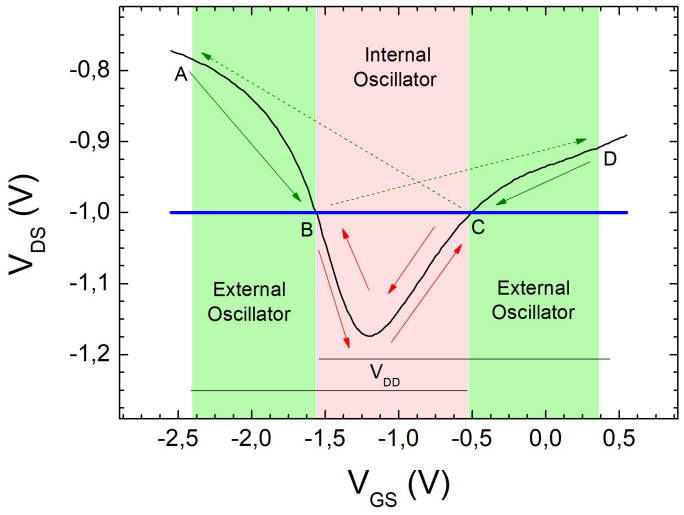


Figure 3.3: Above: GFET transfer curve. The peak resistance, at $V_{\mathrm{DS}} = -1.25$ V is $R = 1620\ \Omega$. Below: GRTL gate transfer curve in the negative pulse configuration. In the red area: principle of operation of the Internal Dirac Oscillator, between B and C, around the Dirac voltage. In the green area: principles of operation of the External Dirac Oscillator. The biases for the digital components, as well as for the GRTL gate, are $[-2.0\ \mathrm{V}, 0\ \mathrm{V}]$.

at B. The drain voltage is now below the threshold and the latch holds its state, until the gate voltage reaches the point C. At this point, since the drain voltage has reached the threshold, the latch changes states and the gate voltage starts to decrease, until it reaches the point B again: the latch's state changes, leading to the oscillation between the point B and C, with the gate voltage constrained in the red area. An example of the oscillator described is in Fig. 3.4.

The circuit (as well as the circuits described later on) is realized with discrete components (latch, Toshiba 74HCC375AP) and a GFET fabricated on chip (see section 1.5), connected on a testboard via BNC cables and wires. The waveforms are measured with a Agilent Technology Infinium DS09064 Digital Storage and the supplies of the GRTL gate and of the latch were generated separately with two Keithley 2611A and are both equal to -2.0 V. The series resistance R_{s} is tuned in order to place the Dirac voltage as close as possible to -1.0 V and at the same time ensure that the GRTL gate output voltage at the Dirac voltage is below the threshold of the latch, which is equal to -1.08 V. The resistance and the capacitance of the RC circuit are obtained respectively with a 10 kΩ potentiometer and a 1 nF capacitor. The potentiometer can be used to tune the frequency of the oscillator. In fact, as it will be demonstrated in the following sections, the frequency of oscillation is directly proportional to the time constant τ of the RC circuit. From the Fig. 3.4 few things can be also noticed. First of all, in the oscillator above,

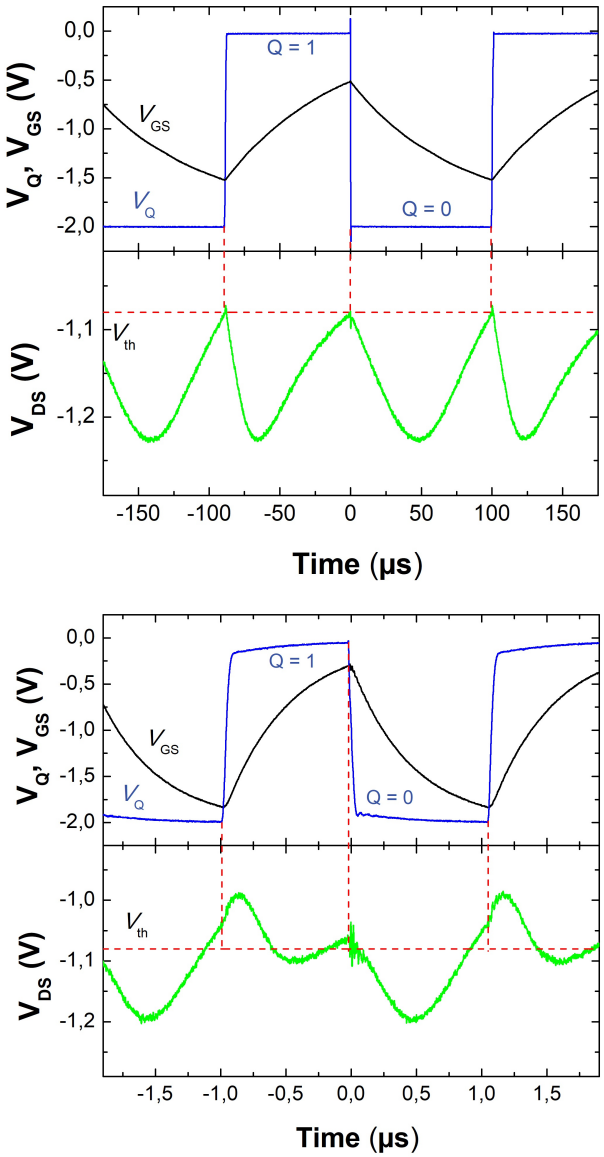


Figure 3.4: Waveforms related to the IDO. In green the drain-source voltage: when it reaches the threshold of the latch (measured around -1.08 V), it triggers a change in the output Q, in blue. The voltage on the capacitor (*i.e.,* the gate source voltage, in black) starts to change accordingly, with a time constant $\tau = RC$, leading to a negative pulse in the GRTL gate output. During the pulse the latch is not enabled and holds its state. After the pulse, V_{DS} hits the threshold again, causing another change in the state. In the first example, above, the frequency is 5.3 kHz with a duty cycle of 0.47, whereas in the second example, below, the frequency is 500 kHz with a 0.5 duty cycle. The series resistance of the GRTL is $R_{\mathrm{s}} = 1260\ \Omega$, $C = 1$ nF.

it is clear that there is a difference between the V_{DS} pulse associated with the charging of the capacitor with respect to the pulses associated to the discharging of the capacitor. This difference is likely to be caused by the hysteresis present in the devices. Secondly, in the plot below, the limits of the latch are visible: in fact, to have a proper operation of the latch, the minimum width of an enable pulse at 2.0 V supply is around 75 ns. However, the enable signal goes only slightly above the threshold, so the effective minimum pulse width is likely to be bigger. In fact, the latch changes state approximately after 150 ns in the low-high transition and after 170 ns in the high-low transition. Finally, in order to have a proper operation of the oscillator, it is necessary to add a delay stage between $\overline{Q}$ and D. In fact, without such a delay, the latch would continuously change state when enabled, leading to a not stable condition. Hence, it is necessary to delay the complementary output signal during the time window in which the latch is enabled. This time window depends on the propagation delay of the GRTL gate and on the delay of the latch. In the measured oscillator, the delay stage was realized with an RC circuit ($R_{\mathrm{FB}} \sim 10$ kΩ, $C_{\mathrm{FB}} = 1$ nF).

The unique transfer curve of the GRTL gate can be used to design also an alternative oscillator, the External Dirac Oscillator (EDO), which exploit the external part of the transfer curve, rather than the central part around the Dirac voltage. As it can be seen in Fig. 3.2, on the right, the differences between the two circuits are the position of the resistor R and capacitor C at the output of the latch and the presence of a NOT gate at the enable input. In this circuit, the latch changes state every time the V_{DS} signal goes below the threshold of the NOT gate. This happens between the point B and C (Fig. 3.3). Since the voltage across the capacitor is continuous, the gate voltage V_{GS} is discontinuous for every change in the latch state. In particular, when the latch changes state and Q switches from high to low, V_{GS} will decrease by V_{DD}, which is the supply of the latch. At this instant, V_{GS} is in the point A and will increase towards its asymptotic value, which is equal to the voltage of $!Q$, 0 V in this case. In the meantime, as V_{GS} increases, V_{DS} decreases (since the gate voltage is below the Dirac voltage), until it reaches the threshold of the NOT gate (point B). At this point, the latch changes state, V_{GS} has a discontinuity with a jump of V_{DD} to the point D. Now the asymptotic value is -2.0 V, hence the capacitor starts discharging and V_{GS} decreases until it reaches the point C. At this point, V_{DS} is below the NOT gate threshold and the latch changes state again. An example of this oscillation is in Fig. 3.5. The measurements have been carried out with the same set-up of the previous example regarding the IDO. Additionally, an OR gate (Texas Instruments CD74HC4002EE4) has been used as the NOT gate in order to invert the enable signal. The same observations concerning the limits of the circuit are valid also for this oscillator. In the fastest oscillator, it can be noticed that, even if the drain goes below the threshold, the latch is too slow and changes state only after some time. The time length is now greater however, around 400 ns. This increase is due to the presence of the NOR gate, which has a propagation time of 150 ns according

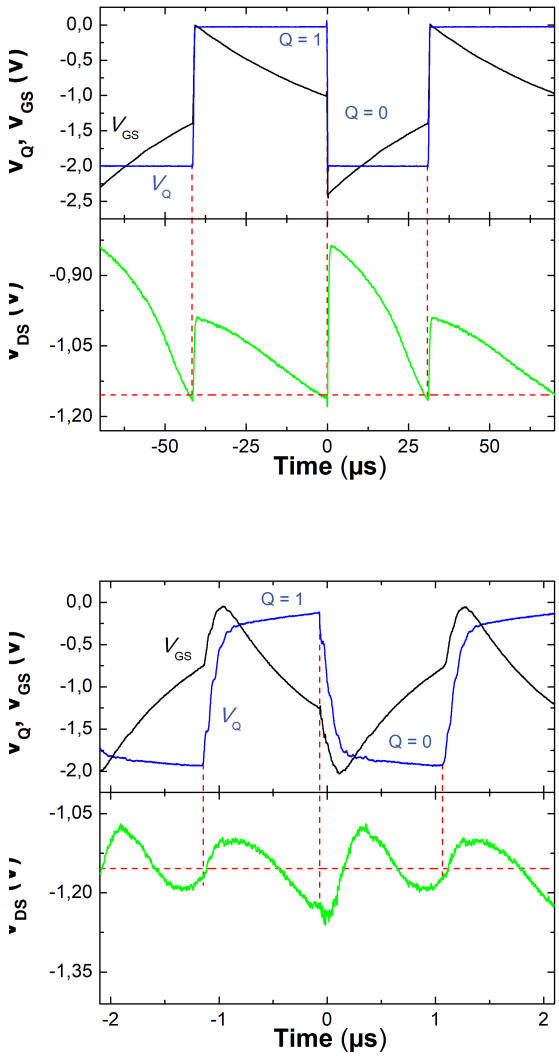


Figure 3.5: Waveforms related to the EDO. In green V_{DS}: when it goes below the threshold of the NOT gate, it triggers a change in the state Q, in blue. V_{GS} changes discontinuously and then tends to its asymptotic value, while V_{DS} decreases, until it goes again below the threshold (measured at -1.154 V). The frequency, as in the IDO, is tuned varying the value of the resistance of the RC circuit with a potentiometer. In the first example, above, the frequency is 4 KHz with a duty cycle of 0.57, whereas in the second example, below, the frequency is 500 KHz with a duty cycle of 0.5. The sudden change in V_{GS}, which should be about V_{DD}, is partially suppressed by the bandwidth of the circuit itself. The series resistance of the GRTL gate is $R_{\mathrm{s}} = 1260\ \Omega$, $C = 1$ nF.

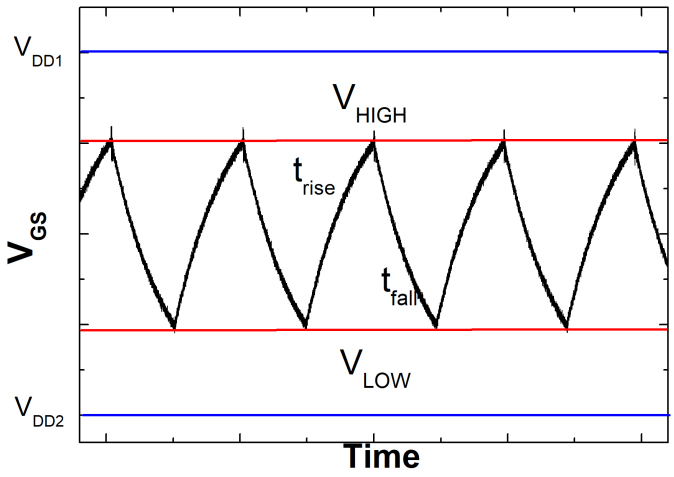


Figure 3.6: Example of the waveform corresponding to the gate voltage. The signal oscillates between $V_{\rm LOW}$ and $V_{\rm HIGH}$. During the rise, the asymptotical value of the exponential function is the upper voltage supply $V_{\rm DD1}$ (in the oscillator obtained $V_{\rm DD1} = V_{\rm DD} = 0.0$ V), while during the fall the asymptotical value is the lower voltage supply $V_{\rm DD2}$ (in the measurements, $V_{\rm DD2} = -2.0$ V). The total period is given by the sum of the two exponential tails, $t_{\rm rise}$ and $t_{\rm fall}$.

to the datasheet, that must be added to the minimum pulse width, in order to get the transition. In this way, sometimes the Dirac voint is reached and passed, as after the high to low transition. Eventually, in an even faster oscillator, if the time in which $V_{\rm DS}$ is below the threshold is too short, the oscillation will be suppressed.

3.3 Voltage Controlled Frequency Tuning

Considering the IDO, with the gate voltage varying from a level $V_{\rm LOW}$ to a level $V_{\rm HIGH}$, as in Fig. 3.6, the period of the signal can be found summing $t_{\rm rise}$ and $t_{\rm fall}$:

$$T = t_{\rm rise} + t_{\rm fall} = \tau \ln \left(\frac{V_{\rm DD1} - V_{\rm LOW}}{V_{\rm DD2} - V_{\rm LOW}} \frac{V_{\rm DD2} - V_{\rm HIGH}}{V_{\rm DD1} - V_{\rm HIGH}} \right) \tag{3.1}$$

The two values $V_{\rm LOW}$ and $V_{\rm HIGH}$ correspond to the gate voltages at which the drain voltage hits the threshod of the latch, causing a change in its state. In the hypothesis that the gate oscillates around $\frac{V_{\rm DD1}+V_{\rm DD2}}{2}$, with an amplitude ΔV, the

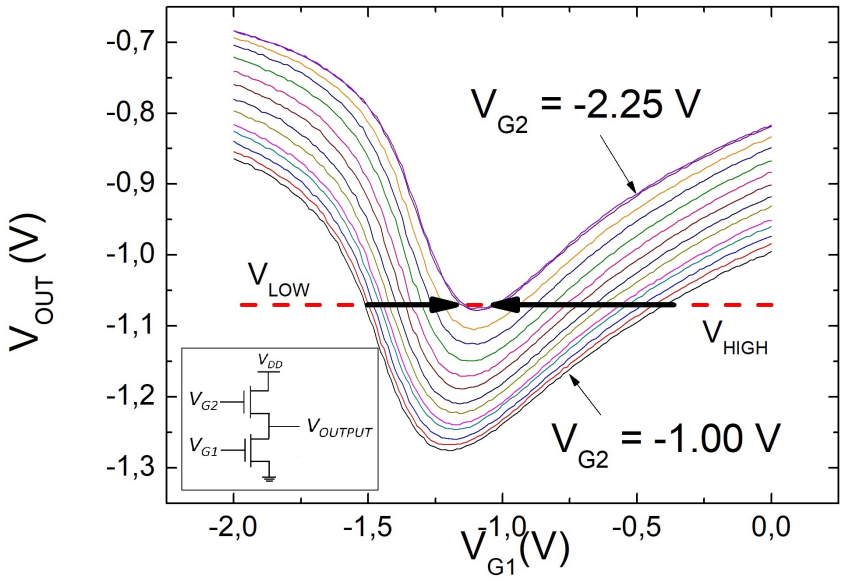


Figure 3.7: Shifting of the output curve of the GRTL gate due to the change in the resistance of the upper GFET, tuned by its gate voltage (V_{G2}). The values at which the output voltage hits the threshold (red dashed line, around -1.08 V) move to the center and ΔV decreases as V_{G2} goes from -1.00 V to -2.25 V.

frequency is therefore equal to:

$$f = \left(2\tau \ln \frac{1+x}{1-x}\right)^{-1} \tag{3.2}$$

where $x = \frac{\Delta V}{V_{DD1} - V_{DD2}}$.

From the equation 3.2 it can be noticed that it is simply necessary to vary the ratio x in order to vary the frequency of the oscillator. Considering the transfer curve, it can be seen that the value ΔV is directly related to the output voltage of the GRTL gate at the Dirac voltage (*i.e.,* the mininum of the signal): the lower output voltage at the Dirac voltage, the higher ΔV, the smaller the frequency. Since the output voltage of the GRTL gate is simply the voltage divider between the series resistance R_s and the resistance of the GFET, a change in the former will change the output voltage at the Dirac voltage. For example, if R_s is increased, the output voltage at the Dirac voltage decreases. Hence, since all the transfer curve is shifted downwards, V_{LOW} and V_{HIGH} approach the two extreme levels (-2.0 V and 0.0 V respectively) and the ΔV increases, leading to a decrease in the frequency. A way to obtain this shift in the transfer curve is to employ a second GFET (or any transistor) instead of a fixed resistor. In this way, with the gate voltage of the GFET above (V_{G2}), it is possible to shift the output voltage and modify the frequency.

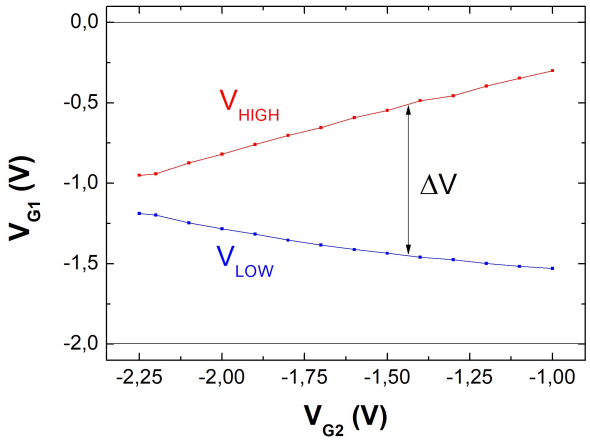


Figure 3.8: Change in the two values of V_{G1} at which the output voltage hits the threshold of the latch. The two limits change approximately linearly with respect to V_{G2}. However, owing to the asymmetry of the transfer curve of the GRTL gate, the slope of V_{HIGH} is slightly greater.

The Fig. 3.7 shows the shift of the transfer curve as V_{G2} varies in a window [-2.20 V, -1.00 V] with a step of 0.1 V. Additionally, the measurement corresponding to $V_{G2} = -2.25$ V has been taken; a greater value of V_{G2} destroys the oscillation, since the output voltage at the Dirac voltage reaches the same level of the threshold. The supply V_{DD} of the GRTL is -2.0 V and the measurement has been carried out with a Keithley 2611A. The two GFET used belonged to the same structure, as described in 1.5. The behavior of V_{LOW} and V_{HIGH} as a function of V_{G2} is shown in Fig. 3.8. As it can be seen, due to the asymmetry in the transfer curve (the change in V_{HIGH} is greater than the change in V_{LOW}, since the left part of the transfer curve is steeper), the equation 3.2 cannot be apply.

Fig. 3.9 shows the frequency of oscillation obtained as a function of V_{G2}. The measurements have been done sequentially with a Agilent Technology Infinium DS09064 Digital Storage. As it can be seen, the relation between f and V_{G2} is nearly equal to the reciprocal of a logarithm: in fact, the frequency V_{HIGH} and V_{LOW} (and hence ΔV) change linearly with respect to V_{G2}, and thus the same relation that exists between f and ΔV, also exists between f and V_{G2}. In particular, it is interesting to notice that the change in the frequency is greater if ΔV is small (it diverges for $\Delta V = 0$ V, in fact). Hence, it is possible to obtain a significant frequency tuning even if ΔV remains contained with respect to $V_{DD1} - V_{DD2}$. This fact has several advantages. Firstly, since the slope of the transfer curve decreases away from the Dirac voltage, the instant at which the output of the GRTL gate hits the threshold becomes more sensible to the noise. The result is a decrease in the short-time stability of the oscillation, which means that the frequency is not fixed and oscillates. Secondly, in general, the transfer curve is more symmetric

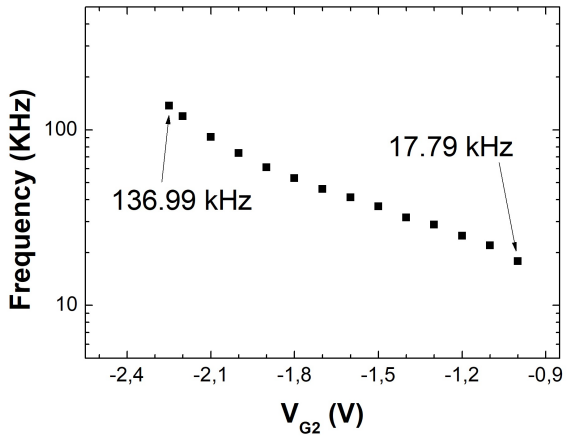


Figure 3.9: Frequency tuning of the IDO. V_{G2} is varied from -2.25 V to -1.00 V and the frequency changes by a factor of almost 8, from 136.99 kHz to 17.79 kHz.

near the Dirac voltage: hence, if ΔV is small enough, the resulting waveform will have a duty cycle close to 0.5. Finally, the hysteresis is accentuated if the gate voltage swing is big, which means if ΔV is big.

Fig. 3.10 shows four examples of the oscillations obtained. As it can be noticed, considering V_{G2}=-1.00 V, the output voltage of the GRTL gate at the Dirac voltage is around -1.35 V and the swing on the gate is $\Delta V = 1.59$ V. The frequency is 17.79 kHz and the duty cycle is 0.64. Such a high value is caused by the asymmetry in the transfer curve and by the fact that the Dirac voltage is not exactly -1.0 V, which is the average value of the two supplies. This can be seen observing the V_{DS} and the V_{GS} signals: in fact, on the whole the gate voltage is shifted upwords and oscillates around -0.91 V. Hence, the time taken during the rise increases exponentially and is greater than the time taken during the fall. This eventually results in a duty cycle different from 0.5.

If V_{G2} is increased, the output voltage at the Dirac voltage is shifted up: for example, in Fig. 3.10 it changes from -1.35 V, to -1.25 V at $V_{G2} = -1.60$ V, -1.18 V at $V_{G2} = -1.90$ V and -1.11 V at $V_{G2} = -2.20$ V; ΔV decreases accordingly, respectively from 1.59 V, to 1.02 V, 0.73 V and finally 0.39 V, leading to an increase in frequency, up to 119.05 kHz. In the last three examples, since the gate voltage does not get too close to the two extremes, the waveforms have a duty cycle close to 0.5: in particular, 0.52 at $V_{G2} = -1.60$ V, 0.49 at $V_{G2} = -1.90$ V and 0.48 at $V_{G2} = -2.20$ V. Finally, the frequency change only due to the change in the ΔV, since the time constant τ remains constant. Its measured value is around 10.7 μs, coherent with the values for the resistance $R = 10$ kΩ and $C = 1$ nF.

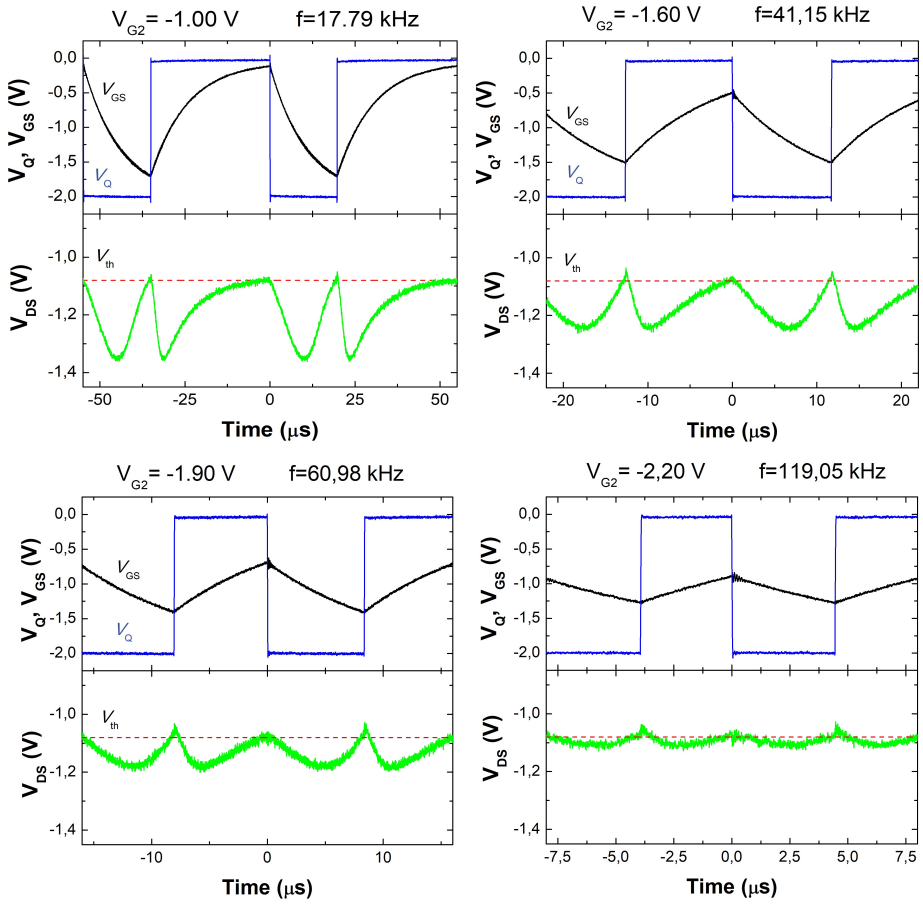


Figure 3.10: Waveforms related to the oscillator at four different V_{G2} (-1.0 V, -1.6 V, -1.9 V and -2.2 V). Due to the change in the resistance of the upper GFET, the drain voltage (or output of the GRTL gate, in green)) is shifted up: since the threshold is fixed, the swing on the drain decreases together with the range of oscillation of the gate (in black). This leads to an increase in the frequency of oscillation, which goes from 17.8 kHz to 119.0 kHz in the four examples.

3.4 Pulse Width Modulation - Duty Cycle Tuning

The Pulse Width Modulation (PWM) consists in a technique in which the duty cycle of a square wave in varied. The duty cycle of a square wave is defined ad the fraction of the period in which the waveform is in the high state, over the total period of the square wave [31]. Since in the Graphene-CMOS Dirac Oscillator the voltage oscillates between two levels (V_{HIGH} and V_{LOW}, see Fig. 3.6) with an exponential decay with a fixed time constant τ, it is possible to calculate the duty cycle of the oscillator's signal directly from the two levels V_{HIGH} and V_{LOW}:

$$D_{\%} = \frac{T_{\mathrm{HIGH}}}{T_{\mathrm{TOTAL}}} = \frac{\ln\left(\frac{V_{\mathrm{DD}}-V_{\mathrm{LOW}}}{V_{\mathrm{DD}}-V_{\mathrm{HIGH}}}\right)}{\ln\left(\frac{V_{\mathrm{DD}}-V_{\mathrm{LOW}}}{V_{\mathrm{LOW}}}\frac{V_{\mathrm{HIGH}}}{V_{\mathrm{DD}}-V_{\mathrm{HIGH}}}\right)} \tag{3.3}$$

In fact, if V_{Q} is in the high state, the voltage on the capacitor (*i.e.,* V_{GS}) will start from V_{LOW} and will tend exponentially to its asymptotic value, 0 V, until it will reach V_{HIGH}. Similarly, when V_{Q} is in the low state, V_{GS} will start from V_{HIGH} and will tend to -2.5 V. If the two levels are not equally distant from their asymptotic values, the time taken in the two exponential tails is different and this results in a duty cycle different from 0.5.

3.4.1 Princicples of Modulation

As it has been said, the two levels V_{HIGH} and V_{LOW} are the two gate voltages for which the drain signal hits the threshold of the latch. If the transfer curve of the GRTL gate is shifted via the backgate (see 1.6.2 and Fig. 3.11), also the two levels will change, following the change in the charge neutrality point. These two levels, whose behavior with respect to V_{BG} is shown in Fig. 3.12 will be fixed, provided that the backgate voltage is fixed and the threshold level of the latch does not change during the operation. As a result, it is possible to control the range of oscillation of the gate voltage, acting on the backgate voltage and hence changing the duty cycle of the oscillation. However, there is a drawback in this pulse width modulation mechanism: in fact, since the time taken during each exponential tail changes, the frequency of the oscillation will also vary. In some applications, for example in telecommunications, in which the widths of the pulses correspond to a precise value that must be transmitted, this fact can be detrimental: in fact, a change in the frequency of the carrier would lead to errors in the decoding of the signal. Nervertheless, in applications such as digital to analog conversion, such problems do not exist. For example, a digital signal can be converted into an analogic signal using the pulse width modulation technique and a low pass filter (such as an RC circuit): in fact, the output voltage of the filter will be proportional to the duty cycle of the square waveform at the input of the filter. If the duty cycle is varied accordingly to the digital signal, it is possible to obtain a precise

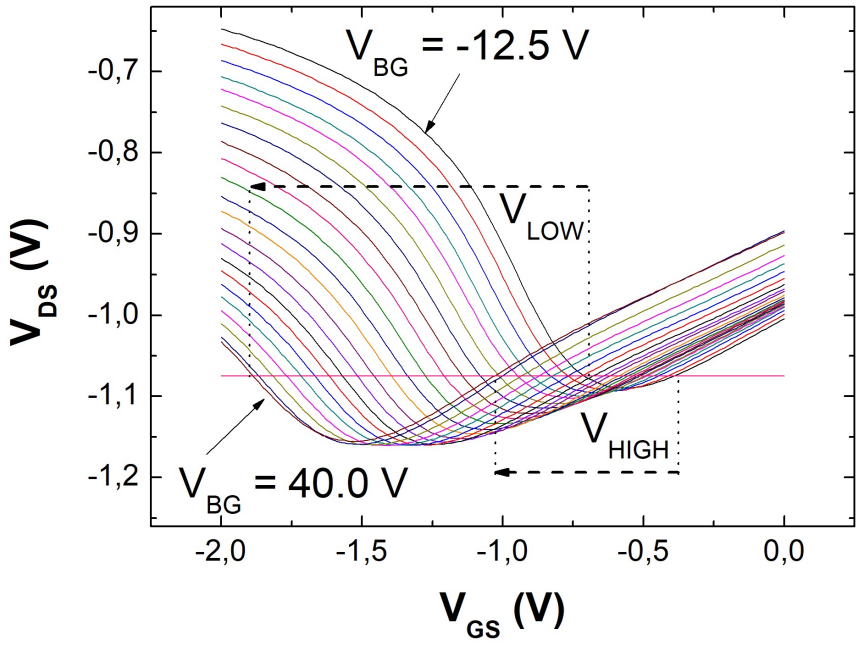


Figure 3.11: Series of transfer curves of the GRTL gate at different backgate voltages. The supply of the GRTL gate component is -2.0 V, the series resistance R_s=708 Ω and the top gate range is [-2.0 V, 0 V]. The output curve is shifted towards 0 V, the upper limit of the range, for backgate negative, up to -12.5 V. As V_{BG} increases, the curve is shifted to the left (towards -2.0 V, the lower limit of the range). At the same time, the curves are moved down and this is due to the increasing of the contact resistance (see 1.6.2).

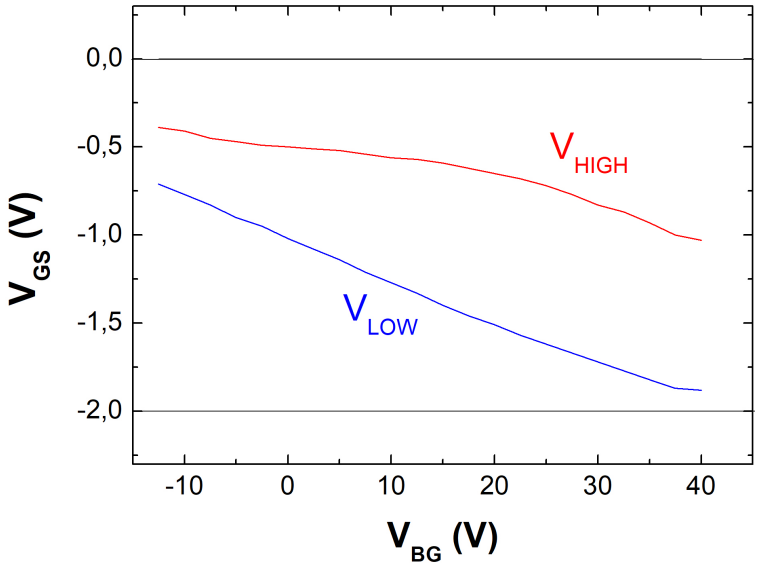


Figure 3.12: V_{HIGH} and V_{LOW}, the two levels at which the output of the GRTL gate hits the threahsold of the latch, as a function of the backgate voltage V_{BG}. The two values start close to the upper extreme, 0 V and then decrease towards the lower extreme, -2.0 V, as the backgate voltage increases from -12.5 V to 40 V.

voltage value. In this application, the frequency of the waveform is not important, as long as it is significanlty higher than the pole of the low pass filter.

Examples of the pulse width modulation are given in Fig. 3.13. The waveforms were measured with an Agilent Technology Infinium DS09064 Digital Storage oscilloscope; the series resistance of the GRTL gate was $R_s = 708\ \Omega$, while the resistor and capacitor of the RC circuit were respectively $R = 17.78\ \text{k}\Omega$ and $C = 0.5$ pF. To avoid instability, a RC circuit was added on the $\overline{Q}D$ feedback ($R_{FB} = 5.76\ \text{k}\Omega$ and $C_{FB} = 1$ pF). The first example is related to a backgate voltage of +40 V: the output curve is shifted towards -2.0 V and the gate oscillates approximately in the range [-0.43 V, -1.99 V]. The resulting duty cycle is 0.20. In the second one ($V_{BG} = 17.5$ V) V_{GS} changes in the range [-0.30, -1.69] and the duty cycle is 0.51. The last one on the right has a backgate voltage of -12.5 V: the range of the V_{GS} is [-0.15, -1.00] and the final duty cycle is 0.78. Since the backgate changes also the resistance of the GRTL gate, there is a side effect consisting in an additional change in the frequency of the oscillation. At positive backgate voltages (+40 V) the resistance of the GFET is higher and the minimum V_{DS} is lower and this cause an increase in the width of the range of oscillation of the gate, leading to an increase in the frequency. Moreover, the voltage on the capacitor (V_{GS}) is very close to its asymptotical value and this contributes to increase the period. On the contrary, the resistance of the GFET is lower for negative backgate voltages and hence the resulting frequency is higher. In particular, the frequency of the oscillation related to V_{BG}=-12.5 V, 17.5 V and 40.0 V are respectively $f = 59\ \text{k}\Omega$, 48 kΩ and 24 kΩ. As it can be seen the frequency change is significant and cannot be neglected. The overall relation between the duty cycle and the backgate voltage is shown in Fig. 3.14.

The Dirac Oscillator used as PWM can be improved with a slightly more complicated fabrication. In fact, the GFET used in the measurements had a global backgate on the back of the chip. However, in principle it is possible to pattern a backgate on the SiO_2 substrate, before the hBN exfoliation and the graphene transfer. In this way, it is possible to obtain a dual gate device in which both the gates are local and act only on the channel and not on the graphene under the contacts. Therefore, the resistance at the Dirac voltage will be independent of the backgate voltage and hence it is possible to limit the change in frequency, at least for waveforms with a duty cycle not too close to 1 or 0. In fact, in those cases, since the gate voltage goes close to its asymptotic value, the frequency will decrease regardless of the Dirac Point resistance. Another advantage of the new design would be the possibility to employ small values for the backgate: in fact, reducing the thickness of the gate oxide, the voltage necessary to shift the transfer curve would decrease.

In the case of the Dirac Oscillator, the proposed circuit does not present any advantage over Si oscillators in term of number of components employed. However, it is a flexible circuit, since the oscillation of the circuit can be tuned both in

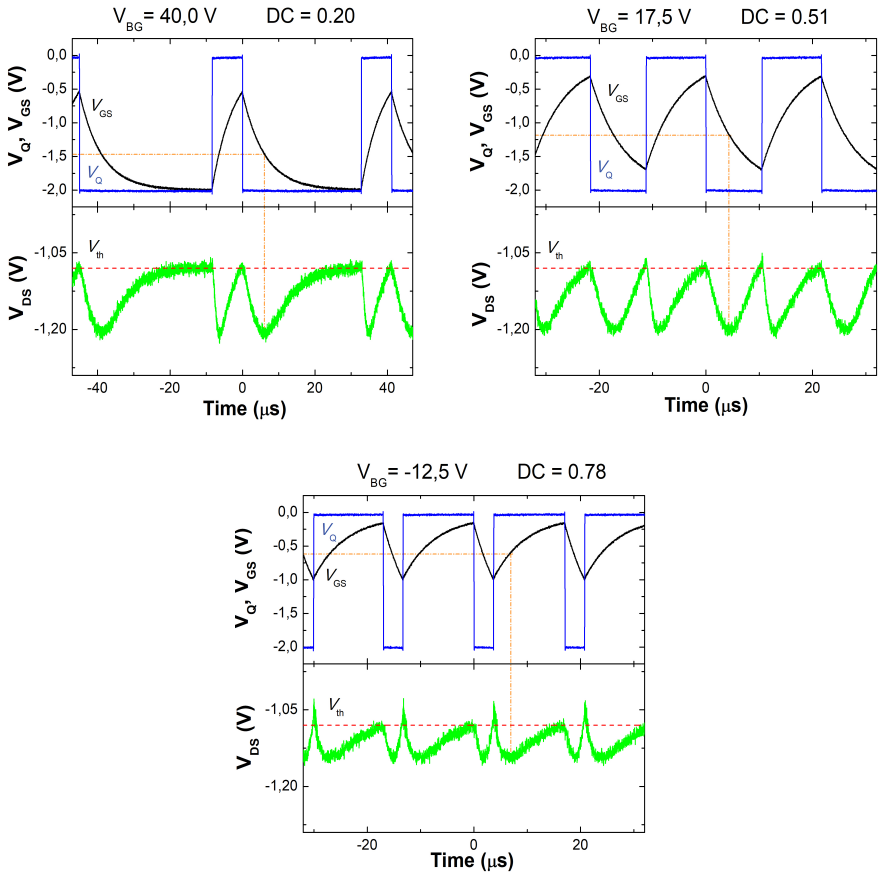


Figure 3.13: Waveforms related to the oscillator used as a PWM at three different V_{BG} (40 V, 17.5 V and -12.5 V). The backgate is used to shift the charge neutrality point across the range [-2.0 V, 0 V]. In this way, the gate is forced to oscillate around a different position. The two exponential signals have a different duration, since one of them is closer to its asymptotic value than the other. This cause a difference in the time in which the output Q is in the high state with respect to the time during which Q is in the low state, resulting in a duty cycle different from 0.5 and depending on the backgate voltage.

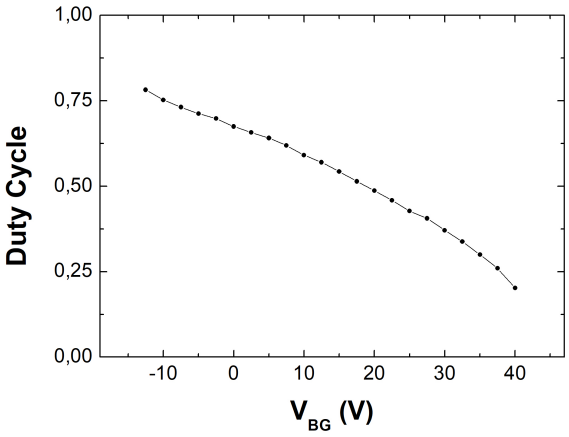


Figure 3.14: PWM of the IDO via backgate voltage. The duty cycle changes from 0.78 at $V_{\mathrm{BG}} = -12.5$ V to 0.20 at $V_{\mathrm{BG}} = 40.0$ V.

frequency (VCO) and in duty cycle (PWM) and these functionalities are achieved with a relatively simple circuit. Moreover, on the whole, the power dissipation issue here is not pressing, since the number of oscillator in an integrated circuit is small and, moreover, every oscillator circuit, by nature, is based on an oscillating current or voltage and hence will dissipate power.

Chapter 4

Conclusions

Graphene, even though characterized by remarkable electronic properties, seems to be unlikely to replace silicon in digital logic. In fact, the absence of a finite bandgap and the problems arising from the shift in the Dirac voltage lead to complexities in the design of logic gates, high power dissipation and low I_{ON}/I_{OFF} ratio. However, graphene could be used together with silicon in hybrid devices that exploit the reliability of silicon and the new properties of graphene, such as the ambipolar electric field-effect. For example, the GRTL gate has a transfer function completely different from the Si RTL gates and hence can be used to add functionalities or to reduce the complexity of actual Si-only circuits. The aim of this thesis was to demonstrate two examples of the idea: in fact, the GRTL gate was succesfully used to design a SDETFF and a Dirac Oscillator.

These circuits are characterized by two main characteristics: the reduced number of components and the flexibility. First of all, even if there exist oscillators that employ fewer components, both the circuits are very simple and employ a very small number of components. In particular, the SDETFF has less gates than a common SETFF; the hybrid graphene-CMOS DETFF employs only a latch and the circuit is considerably simpler than the Latch-MUX Si-only DETFF. This fact could simplify and reduce the area occupied by integrated circuits containing flip-flops. Secondly, both circuits are flexible: the Dirac Oscillator has two voltage input that can change the frequency and the duty cycle of the oscillatior (VCO and PWM). The SDETFF has a control input to set the operation either as a SETFF or as a DETFF.

However, there are also several drawbacks of the use of graphene. First of all, GFETs cannot be turned off and hence they dissipate power in every state. This consititutes clearly a problem, at least in the SDETFF circuit that could have a high degree of integration. Moreover, the zero bandgap leads also to a small I_{ON}/I_{OFF} ratio. Hence, the output swing of the GRTL gate may be very small: however this is a tangential problem. In fact, the GRTL gate is used to drive other Si CMOS components that can tolerate a small input swing without affecting their rail-to-rail output operation. Furthermore, since there is a great

variability in the electronic properties of the GFETs fabricated (position of the Dirac voltage, resistance etc.) every GRTL gate must be tuned in order to ensure a proper operation of the circuits. A way to solve both the problems, namely the small output swing and the variability of the GFET, could be to use GNR or bilayer graphene: in fact, with a finite bandgap, the change in the resistance of the channel would be higher and then the swing of the GRTL gate would increase. Given this increase, the variabiity of the electronic properties of graphene would not prevent the operation of the GRTL gate, since the latter would be more robust with respect to changes in the position of the Dirac voltage or in the resistance of the devices.

Finally, other issues are related to the fabrication process. Firstly, in order to use the Dirac Oscillator as a VCO, it is necessary to use dual gate devices with two local gates. This fact would reduce the backgate voltage range and would avoid the problem of the change in the contact resistance. Moreover, the experimental demonstration of the two circuits was carried out employing discrete components. A proper demonstration should be done with an integrated circuit: hybrid graphene-CMOS circuits have been already fabriacated, hence this should not be a problem. Nevertheless, in an integrated circuit, the SDETFF and the Dirac Oscillator could be characterized more precisely, for example concerning the set-up and hold time, or the short term and long term stability of the oscillation.

In conclusion, GRTL gates and hybrid graphene-CMOS circuits seem to be quite promising, since they succesfully combine the strenght of Si with the new functionalities of graphene. Moreover, there is room for further improvements regarding the fabrication of integrated circuits and new circuits or logic components that could be designed employing the GRTL gate.

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