POLITECNICO DI MILANO

School of Industrial and Information Engineering

Master of Science in Electronics Engineering

DEVELOPMENT AND QUALIFICATION OF READOUT ELECTRONICS AND DATA ACQUISITION FOR THE SIDDHARTA EXPERIMENT

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Abstract

This thesis work is part of the Siddharta project, a nuclear physics experiment that aims to increase today's knowledge about the strong nuclear force inside atoms. To achieve that, is important to measure correctly the shift ε and the amplitude Γ of the Kα emission line of exotic atoms, as the Kaonic Hydrogen. A Kaonic atom is an atom where a Kaon has replaced on electron in the orbitals. The shift and width to be measured derive from the contribution of the nuclear force in addition to the electromagnetic one. In order to perform these spectroscopic measurements correctly, it is necessary to develop sensors and readout electronics that provide adequate energy resolution with respect to the specifications required by the experiment. The first installation of the experiment has provided useful data since it was the first-ever measurement of the Kaonic Hydrogen X-rays, but still had some limitations due to the limited number of detectors and the signal-to-background ratio of the apparatus. So it was necessary an upgrade. Therefore, both the detectors and readout electronics have been increased in number and solid angle to match statistics requirements. In the new apparatus, all detectors must be thoroughly tested and characterized before they can be assembled and used for the purpose of the experiment. In the new experiment there will be 48 arrays with 8 SDDs detectors each, for a grand total of 384 SDD cells, this is the first experiment ever with such an high number of X-ray spectroscopy SDDs.
This thesis is composed of 4 chapters; the first one introduces the SIDDHARTA project, and the physical principles that lies beneath the experiment. The second chapter discusses about SFERA, an ASIC developed in Politecnico laboratory for a fast multi-channel readout of radiation detectors. Finally, modifications and improvements of the new release (SFERA III) are presented. The third chapter describes the characterization of some SDD arrays that are needed for the final SIDDHARTA experiment. First, the mechanical characteristics of the detectors are presented, then the testing setup is shown. Afterwards, the results of these tests are presented. The last chapter describes the development of a DAQ system operating according to a Sparse Readout scheme, a type of acquisition of x rays useful for the sparsification of the events. Finally, an

intensive analysis about the crosstalk and a study regarding the timing signals will be presented.

Abstract (Italian)

Questo lavoro di tesi di inserisce nell'ambito del progetto Siddharta, un esperimento di fisica nucleare che si propone di accrescere le conoscenze odierne riguardo la forza nucleare forte. Per farlo è importante misurare correttamente lo spostamento ε e l'ampiezza Γ della linea di emissione Kα degli atomi esotici, come l'Idrogeno Kaonico. Un atomo kaonico è un atomo dove un kaone ha rimpiazzato un elettrone negli orbitali. Lo spostamento e l'ampiezza sono stati misurati tenendo conto oltre del contributo della forza nucleare forte, anche di quella elettromagnetica. Per effettuare correttamente tali misure spettroscopiche è necessario sviluppare sensori, ed una elettronica di lettura, in grado di provvedere un'adeguata risoluzione energetica, considerando le specifiche richieste dall'esperimento. La prima installazione dell'esperimento ha fornito dati molto utili, visto che è stata la prima misura in assoluto dei raggi X emessi dall'Idrogeno Kaonico, questa però aveva dei limiti in risoluzione, soprattutto dovuti al rumore degli strumenti. Quindi è stato necessario effetturare un upgrade. Dunque, sia i rilevatori che l'elettronica di lettura sono stati migliorati per soddisfare le specifiche richieste. Nella nuova strumentazione, tutti i rivelatori devono essere accuratamente testati e caratterizzati prima di poter essere montati ed utilizzati ai fini dell'esperimento. Nel nuovo esperimento saranno presenti 48 matrici con 8 rilevatori SDD per ogni matrice, quindi un totale di 384 SDD, questo esperimento è il primo che sfrutta un così alto numero di celle SDD per spettroscopia a raggi X.
Questa tesi è composta da 4 capitoli; il primo introduce il progetto SIDDHARTA e i principi fisici che si trovano dietro l'esperimento. Il secondo capitolo riguarda SFERA, un ASIC sviluppato nel laboratorio del Politecnico per una lettura multicanale veloce di rilevatori di radiazione. Infine verranno presentate le modifiche e migliorie apportate per la nuova versione (SFERA III). Il terzo capitolo mostra la caratteristazione di moduli SDD, necessari per l'esperimento finale di SIDDHARTA. Prima verranno presentate le caratteristiche meccaniche dei detectors, in seguito viene mostrato il setup utile per effettuare il testing. Successivamente, verranno presentati i risultati dei questi tests. L'ultimo capitolo mostra lo sviluppo del DAQ, usando la modalità di lettura Sparse,

cioè un tipo di acquisizione di raggi x utile per la sparsificazione di eventi. Infine verrà presentato un'intensiva analisi del crosstalk e uno studio relativo a segnali di temporizzazione.

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Chapter 1

SIDDHARTA project

This chapter describes the SIDDHARTA (Silicon Drift Detector for Hadronic Atom Research by Timing Applications) experiment; It is a research experiment in the field of nuclear physics which aims to study strong nuclear interactions by measuring the shift of energy levels in exotic Kaonic atoms.

1.1 Introduction to the experiment

My thesis experience is included in the project SIDDHARTA (Silicon Drift Detectors for Hadronic Atoms Research by Timing Applications), an experiment founded by the European Union and the National Institute of Nuclear Physics (INFN), which is carried out within an international collaboration of 8 institutes from 6 countries (Austria, Canada, Italy, Germany, Japan and Romania). The main objective to be pursued is to study the strong nuclear force, the force that holds united protons and neutrons within the nucleus of each atom. The first goal is therefore to unify the four elemental forces (electromagnetic, strong nuclear, weak nuclear and gravitational) in a single theory, to explain why the particles have a mass and to understand even more the structure of the atom. In reality, the weak nuclear and electromagnetic forces have already been unified in the so-called Electroweak theory. So physicists want to find a theory that explains the operation of the atom by grouping, in addition to the weak electromagnetic and nuclear force, already unified in the current theory, also the strong nuclear force. A theory of this kind should have as a limiting condition the results provided by the standard model, the latter would be only a low energy approximation of a more general theory. SIDDHARTA, investigating the strong nuclear force and its interactions with matter, could lead to a deeper understanding of nuclear phenomena overcoming this approximation of low energies. There is also a problem related to the mass of the particles. Considering the standard model of the atoms, this states: protons, neutrons and electrons as elementary particles, they are considered indivisible and without dimension. Today it is known that is not the case: protons and neutrons are composed by smaller particles, quarks, in particular we know that a proton is made up of three quarks, 2 up and 1 down, instead the neutron is made up of 1 up and 2 down, whose mass is known to us, but we do not know yet why the mass of the proton is greater than the sum of the mass of these three quarks. The most reliable hypotheses refers to the continuous creation and destruction of quark pairs "inside" the proton, which would then increase the equivalent mass observed "from the outside".

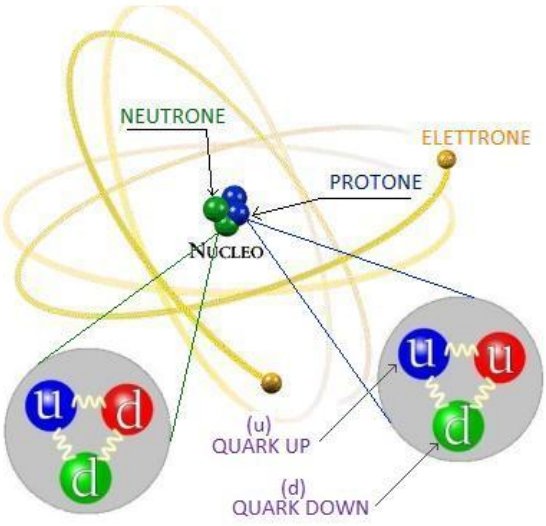

Figure 1.1 *Composition of the atom. Proton is made by three quarks, 2 up and 1 down, but the total mass is greater than the sum ofthe mass of this 3 subatomic particles*

So the Siddhartha project is focused on the study of the particles that are part of the hadron family, which unlike leptons (which do not contain quarks), are subject to strong nuclear force. The hadrons are subdivided into baryons (3 quarks), exotic baryons (5 quarks) and mesons (quark and antiquark pairs). The study of the project focuses on the meson, which typically decays into a pair of kaons, one negatively and one positively charged.

1.2 The physics of kaonic atoms

The experiment will take place in the INFN national laboratories in Frascati, more precisely in the DAFNE particle accelerator, where the kaons are produced by annihilation between matter and antimatter. The peculiarity of these Kaons is to have a very high mass: about 1000 times higher than the electron, comparable to the mass of a proton. For this experiment, of considerable importance are the K^-, infact when a negatively charged kaon goes to an atomic target (as ad example hydrogen or deuterium) and loses all or part of its kinetic energy through the ionization and excitement of atoms of a medium, with a certain probability it can be caught in an orbit excited by the target atom. When this happens, and the kaon in question replace the electron orbital, we attend the formation of an kaonic hydrogen atom.

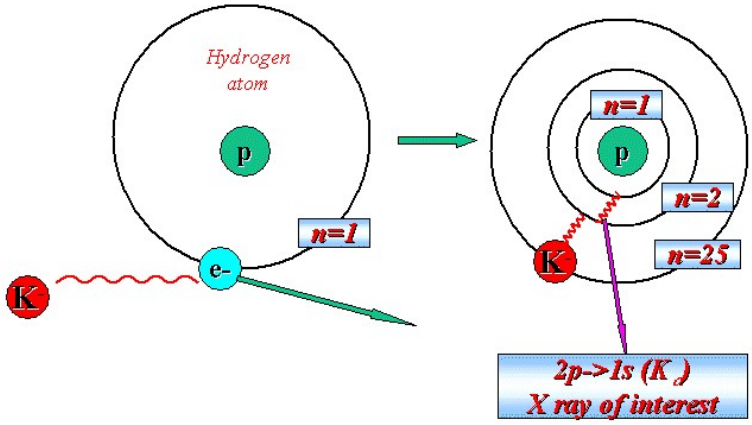

Figure 1.2 *Process of transformation of simple Hydrogen into Kaonic Hydrogen*

Before the kaons come into contact with the target they must lose part of their kinetic energy. In the process of formation of kaonic atoms the density of the target plays a fundamental role, if the gas density is too low, few kaons will be captured in the excited orbit of the atom, on the contrary if the density is too high, even if many kaons will be captured, few will reach the transition 2p $\rightarrow$ 1s of fundamental interest in the experiment (due to the presence of strong interaction). In SIDDHARTA the optimal density, that is been calculated taking into account such effects, turns out to be of $2 - 3g/l$. As already said the substitution of the kaon in the atom instead of the electron it involves in a change of eigenvalues energy systems, and therefore of the main quantum number n. At equal distance from the nucleus, at value n = 1 present in the system electron-proton, corresponds to the been excited with n = 25 of the antikaon-proton system. Radiative transitions carried out by the kaon on its way to the lower energy state, are all related to electromagnetic interactions, except those on 1s, where they also intervene strong interactions. The strong interactions produce both a shift ε in the position of the line (relative to the transition 2p $\rightarrow$ 1s) with respect to its position calculated considering a purely electromagnetic interaction, and an enlargement of the width Γ relating to level 1s.

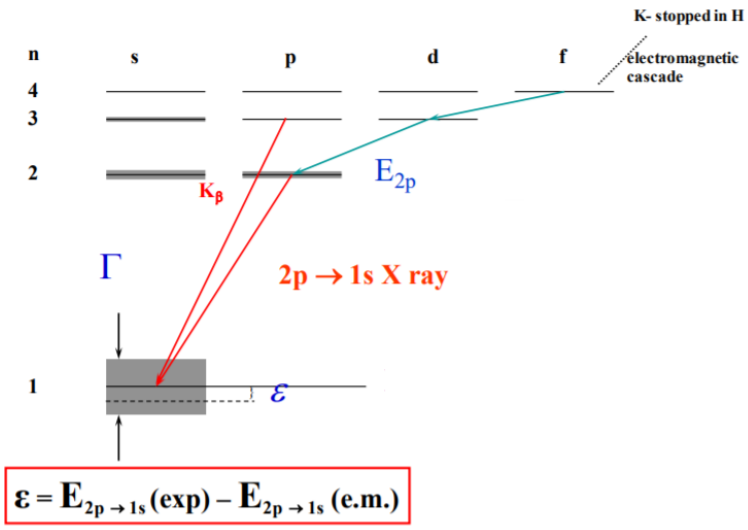

Figure 1.3 *Transitions related to kaonic hydrogen*

According to what reported above, we can therefore go back to the strong interaction going to measure the shift ε

$$\varepsilon = |E_{2p-1s}^{measured}| - |E_{2p-1s}^{e.m.}| \tag{1.1}$$

Where $E_{2p-1s}^{e.m.}$ measures the shift ε of the Kα line (2p- 1s transition), and $E_{2p-1s}^{e.m.}$ is the one calculated from a purely electromagnetic interaction. The resulting value is $E_{2p-1s}^{e.m.}$ equal to 6480 eV with an uncertainty of ± 1 eV due to the inaccuracy on the knowledge of the mass of the kaon. As for the enlargement Γ , it is due to the low average life time of the kaonic atom (of the order of 10^{-8} seconds), in which the kaon is captured by the nucleus when it is on the essential state. This behavior is reflected in a broadening of the emission line, according to the Heisenberg uncertainty principle

$$\Delta T \cdot \Delta E \geq \frac{1}{2}\hbar \tag{1.2}$$

Experiments have been performed in the DAFNE accelerator on kaonic hydrogen and one of the most significant energy spectra is shown in 1.4. The shift that is also taking into account the strong force with respect to the vertical dotted line indicating the peak value predicted by electromagnetic theory.

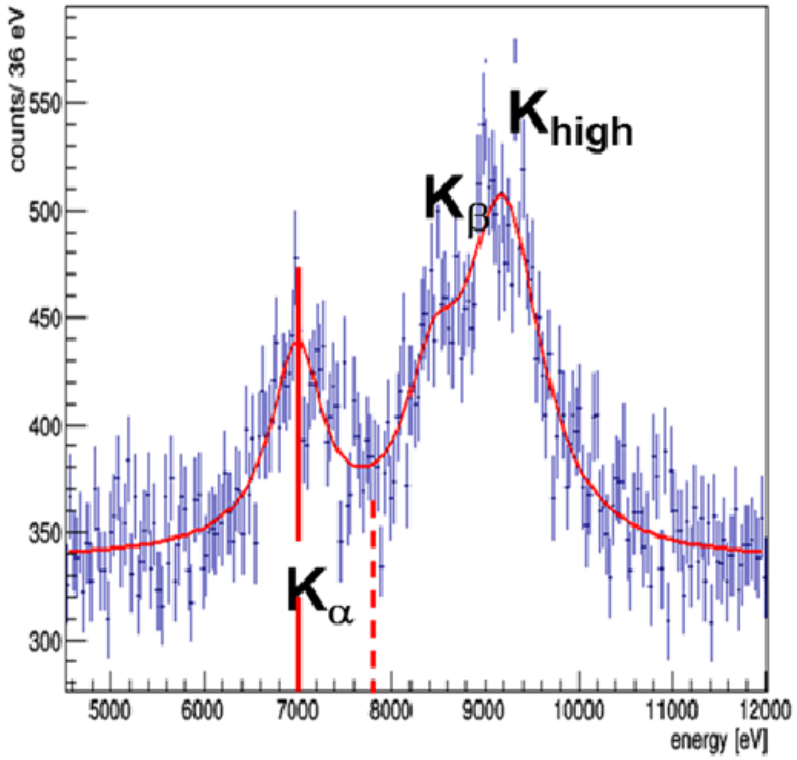

Figure 1.4 *Background subtracted X-ray energy spectrum of kaonic hydrogen*

The measurements already obtained are encouraging, in fact we can note the shift to the left of the Kα line, but the measure is very noisy because of the strong background; the figure already shows the data obtained by subtracting from the spectrum obtained the background measured separately, without the signal. With this processing, even if it was possible to identify the different emission lines, the quantitative measure is however affected by a great uncertainty because even if, it is the relationship between desired events and background has improved a lot, due to the very low rate of events, the signal remains however comparable with the statistical fluctuations of the background. So there is an uncertainty of 70eV in the determination of the shift, and 100eV for the width. With the new SIDDHARTA experiment we want to overcome this limit. In all this the task of electronics is "simply" to detect a line of Kα emission around 6.46KeV, with extreme precision; at the same time you want also measure its width.

Esotic Atom	Kα position	ε shift	FWHM Γ
Hydrogen:	6.46KeV	$\approx$ 300eV	$\approx$ 450eV
Elium:	7.81KeV	$\approx$ 500eV	$\approx$ 800eV

Table 1.1 *Expected values that electronic has to acquire with good resolutions*

Given the nature of the experiment, however, the main requirement that electronics must satisfy is the stability in the position of the Kα peak, due to the long time of acquisition necessary to accumulate a significant event statistic. In fact it was demanded a stability of the order of a few eVs in the measure of the peaks of interest, therefore with a relative stability of about 1‰. In this experiment, accuracy is limited by the particularly high background compared to the average rate of useful events. This is because the events that we want to study are particularly rare and little probable: a rate of one useful event is expected every 300 seconds. While there are remarkable background phenomena that generate high energy photons up to about 400KeV inside the target and which are therefore equally collected by SDD detectors. This causes signs of very high loads, which can disturb and compromise the measurements of useful signals, due to a variation in the state of polarization, or generate long recovery times which effectively lead the system unusable for hundreds of µs. Photons so energetic in fact, deposit a lot of charge on the SDD which must then be disposed of. Mainly two causes of background are identified: the synchronous background, that is generated by the same kaons that entered in the target containing the hydrogen, and that interact with the nuclei of the materials that make up the setup, or later to a further decay in other relativistic particles give rise to phenomena radiative. The second contribution is instead asynchronous, that is due to external causes, in particular to the electromagnetic irradiation of the machine generating the beam or to particles lost from the main beam, due to ions of residual gas in the accelerator. The latter is the predominant contribution, precisely because of an asynchronous nature, with logic of timing we will try to eliminate it. With these measurements we want to reject all those events that are not synchronous with the signal, so that are not directly generated by the Kaones entering the targets. In order to reduce the asynchronous background component, it was used the system showed in Figure 1.5, done with two scintillators, one hit by the negative kaons and the other hit by the positive kaons, creating a windows of the duration of 1 μs, where the detector provides signals due to useful events. Detectors such as SDDs that, in addition to being extremely efficient and offering high resolution, ensure adequate high response speeds (in the order of a few hundred ns, limited by the maximum drift time of the charge in the device), lend themselves well to these coincidence measures.

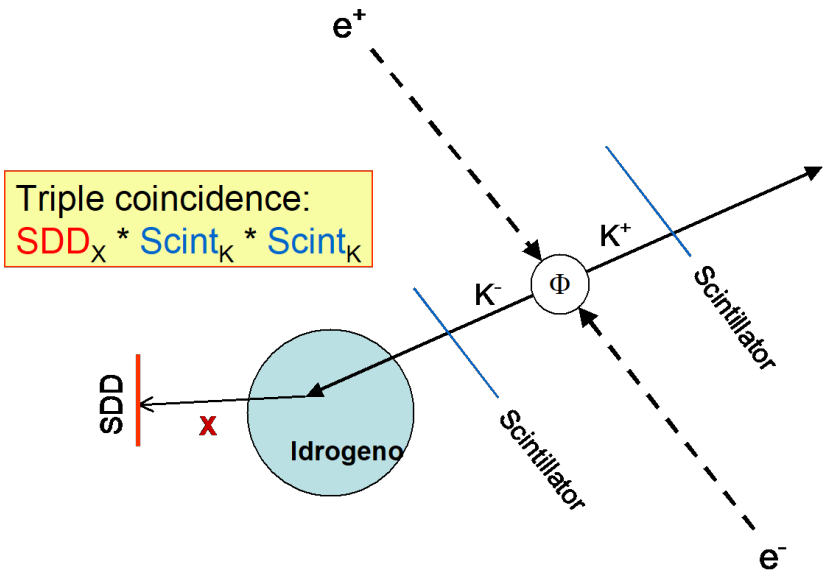

Figure 1.5 *Coincidence measures for the rejection of asynchronous background.*

So, the SDDs with their response (1μs) allow SIDDHARTA to carry out a measurement with fast signal trigger mechanism, which is impossible in DEAR using CCD, detectors in comparison much more "slow" in the measure. Use of a trigger system relatively fast ($\approx\mu$s) on SDD detectors for X spectroscopy measurements in SIDDHARTA an improvement with the previous appartus using CCDs. In conclusion, the electronics must provide, in addition to the classic analog signal on the photon energy, also a digital signal in real time, which identifies the instant of arrival of the photon: for this signal a good temporal precision with a value less than the μs.

1.3 First experimental setup of Siddharta

The experimental setup, in the first SIDDHARTA experiment was based on a detector module componsed by six SDD modules with a square active area as shown in the Figure 1.6. The system was composed of 198 SDD drift chambers of $1cm^2$ each, for a total of almost $200cm^2$ of sensitive area. Due to different type of faillures, about 140cm2 were finally operational during the experiment. The system is made with all the same modules arranged around a target cylindrical containing gaseous hydrogen; each module consists of 6 SDDs arranged on two 3cm x 1cm chips, the module then includes the polarization electronics for the detectors and the front-end CHIP for reading the signals, which in this way results very close to the SDDs. In total, 33 modules was used.

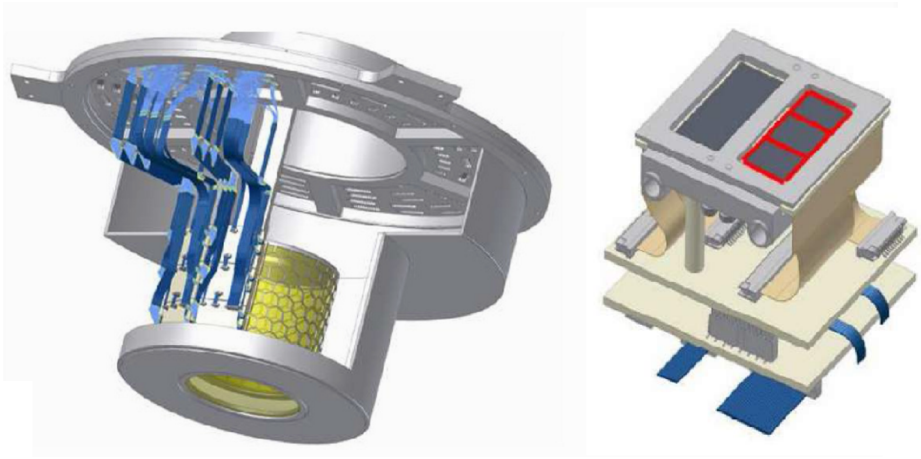

Figure 1.6 *Setup of the machine that will perform the experiment. On the left, the whole machine is shown. On the right, the single module is presented*

From Figure 1.6, it can be noted that the SDD detection assembly was not characterized by high efficiency, due to the relevant dead area between the SDD arrays. This aspect will be addressed in the new SDD apparatus. To handle events from all these channels the CHIP must also integrate a part of digital logic to manage communication with the acquisition system; the latter provided the analog-digital conversion of the signal and its storage. Finally, at the end of the acquisition, the DAQ had to deal with it to make the coincidence with the signals coming from the kaonic triggers to reject the asynchronous background and select only the events of interest.

1.4 Spectroscopy and energy resolution

The term spectroscopy refers to the analysis of the energy distribution of the photons of any radiation: a spectroscopy system must therefore discretize every single photon incident on a given detector, measure the energy and then accumulate the number of photons at different energies. The progress achieved in recent years in X-ray spectroscopy is responsible of the remarkable development of semiconductor detectors, able to transform X photons into charge signals that can be acquired electronically. Among the most important in terms of resolution and response time are undoubtedly the detectors a semiconductor derivation, whose concept was introduced by E. Gatti and P. Rehak in 1983. To get a better understanding of their functioning we see some of the most important features of semiconductor detectors, after which we will move to the SDD detectors themselves. Semiconductor detectors have a high density: great loss of energy over small distances and the diffusion is less than a gas detector, which translates into

better performance in terms of spatial resolution (<10μm). Moreover they have low ionization energy (a few eVs to generate an e-h pair) compared to gas detectors (20-40 eV for one e-ion pair) or scintillators (400-1000eV for the creation of a photoelectron). To better understand the reasons why the structure of the silicon detectors translates into high spectroscopic performances, it is advisable to study the contributions to energy resolution in a generic detection system (formed by the detector and associated electronics for signal processing). There are several factors that combine in determining the width of a row of the spectrum, three in particular:

- Statistical fluctuations in the number of charge carriers created by the passage of ionizing radiation
- The electronic noise associated with the detector and the electronics used in the signal processing
- Problems in the operation of the detector (for example incomplete collection of charge) or electronic drift

The first contribution determines the so-called intrinsic resolution of the detector and produces a width at half height (Full Width Half Maximum) that can be expressed in following way:

$$FWHM_{stat} = 2.35\sqrt{\varepsilon FE} \tag{1.3}$$

where E is the energy released in the detector, ε the energy needed to create a pair (3.7eV in silicon) and F is the Fano factor (about 0.11), which takes into account the deviations of the Poisson statistics in the fluctuations in the number of charge carriers. The second important contribution, related to noise in the detector and electronics associated, is typically expressed in terms of equivalent charge of noise (ENC); when the ENC is expressed in terms of the number of equivalent electrons, the noise contribution at the width of the line takes the form:

$$FWHM_{noise} = 2.35\varepsilon ENC \tag{1.4}$$

The third factor that intervenes to determine the energy resolution is linked to any system malfunctions; for example all those factors that lead to an inefficient collection of charge in the detectors. It results in a global resolution:

$$FWHM_{tot} = 2.35\varepsilon\sqrt{(ENC)^2 + FE/\varepsilon} \tag{1.5}$$

1.5 Electronic acquisition chain for X-ray spectroscopy

The general scheme of an instrumentation for spectrographic measurements is shown in Figure 1.7. The detector (for us an SDD) has the task of converting the photon energy accident in an electrical signal, generating a proportional charge to the energy released in the detector; the charge, as described below, is collected from the electric field inside the silicon and accumulated on the detector's anode; the latter is schematized with a Dirac delta current, that represent an area equal to the charge generated, and with a capacity in parallel, equal to the sum of the capacities related to the node of anode. The delta is subsequently integrated and amplified by the preamplifier, obtaining a voltage signal: ideally a step; in reality, given the impossibility of make an ideal integrator, the preamp is best approximated as one single pole system: the voltage signal obtained is therefore an exponential descending. This stage must respond to important characteristics: how to introduce a noise contribution comparable to the intrinsic one of the detector in order not to worsen the quality of the signal; at the same time it must provide a large amplification for break down the noise contribution of the later stages. Moreover between the preamplifier and the shaper is necessary introduce a passive network, called the pole-zero compensation network, with the task of introduce a zero in the transfer at the same frequency of the preamplifier pole; in fact, the shaper needs a Dirac delta signal at its entrance. For this, another important feature of the preamp is to have a good time of climb, to generate a delta as ideal as possible. The subsequent stages used for the "forming" of the signal, by means of a shaper whose form is chosen to minimize the noise contribution. The signal is first sampled in its maximum valueusing a circuit that maintain the value of the peak (Peak-Stretcher) and converted into digital format by an analog digital converter (ADC), at this point we proceed to counting the events, belonging to each measurement channel (corresponding to a given photon energy) using the Multi Channel Analyzer (MCA), and finally the data are collected by PC for processing later. [2]

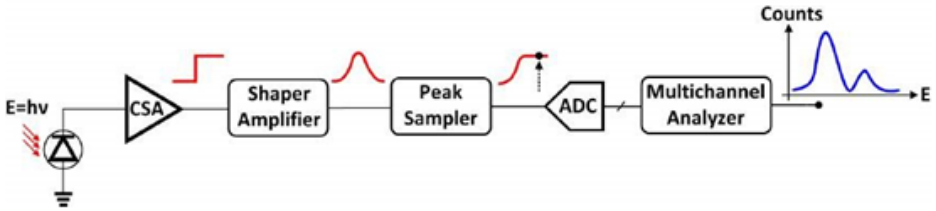

Figure 1.7 *Detector signal-processing electronics*

1.5.1 NOISE contribution

In a spectroscopy system it is important to evaluate correclty the causes of noise, because an high noise directly translates in a loss of resolution in the final measure; this fact is evident when we want to measure a single emission line, with narrow distribution at a defined energy, which is the goal of SIDDHARTA. Due to noise, the measured spectrum is not a single line but is distributed; generally the system resolution is characterized by the value of the Full Widh at Half Maximum (FWHM) of that distribution. It is then important to identify the main noise sources when designing a front-end electronic: in the optimal condition the preamplifier has to introduce less noise than the intrisic one, due to the statistical generation of charge inside the silicon, which represents the ultimate limit. Moreover, since different contribution has different frequency transfer, there is an optimal way to filter the signal which maximize the signal to noise ratio. Then it is important to understand from where each noise contribution comes, with the purpose to get the best possible performances.

1.5.1.1 ENC (Equivalent Noise Charge)

As mentioned above, the noise performance are referred in terms of ENC, related both to the detector and to the front-end electronics. The ENC is usually expressed as number of equivalent electrons by dividing its value (in Coulomb) by the fundamental electric charge (q = $1.6 \cdot 10^{-19} C$).

- **Intrinsic noise**
  This noise arise from the same phenomenum of energy conversion from photon to charge; it is an intrinsic contribution which value is not reducible: it is due to the statistical process of generation of electron-hole pairs, after the absorption of the photon energy. For an energy E of the incident photon the average number of produced pairs is:
  $$\bar{N} = \frac{E}{\varepsilon} \tag{1.6}$$
  where ε is the needed mean energy to create a eletron-hole pair (conversion factor): its value depends on the material which the detector is made by and, in the case of silicon, is equal to 3.6 $\frac{eV}{pair}$. This phenomenum of generation doesn't necessarily follow the poisson's statistic: indeed the creation of an electron-hole pair is not completely indipendent from the creation of other pairs, because it implies a reduction of the available energy.

- **Electronic noise**

Let's now consider the electronic noise. The electrical model of the analog acquisition chain is shown in Figure 1.8. in particular we have to analyze the noise of the first stage that, being at the input, has the greater contribution. Indeed it is known that, by moving back at the input the noise of the stages following an high gain stage, the noise is divided by the square of the gain of that stage, and becomes then negligible. In the Figure 1.8 we can see that the detector is modeled as the parallel of a generator delivering delta-like current pulses that carry the charge Q, and its depletion capacitance C_D. For what concerns the preamplifier, C_F and C_G represent respectively its feedback and input capacitance thus the output step amplitude is equal to $Q = C_F$ while the shaping filter is represented with its transfer function T(s).

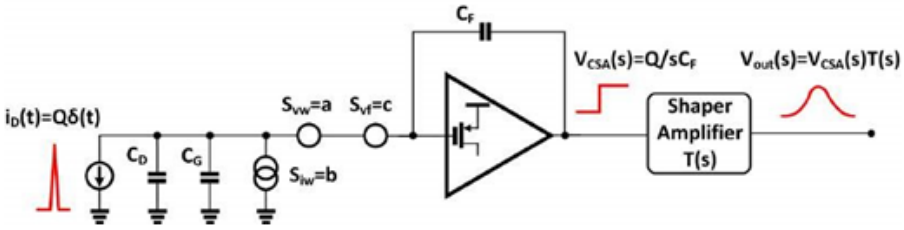

Figure 1.8 *Signal processing chain with equivalent noise generators*

The SNR of the measurement is defined as the ratio between the signal peak amplitude and the voltage noise root mean square, both referred to the same point of the acquisition chain (output of the shaper):

$$SNR = \frac{Q \cdot max[v_{out,\delta}(t)]}{\sqrt{\overline{v_{noise}}^2}} \tag{1.7}$$

where $v_{out,\delta}$(t) is the peak amplitude of the shaper output pulse when the charge delivered by the detector is considered to be unitary. It follows that:

$$ENC = \frac{\sqrt{\overline{v_{noise}}^2}}{max[v_{out,\delta}(t)]} \tag{1.8}$$

All noise sources of the system can be modeled by the three input-referred equivalent noise generators of Fig. 1.8. The white voltage noise, also known as series noise, is typically dominated by the preamplifier input transistor thermal noise:

$$S_{v\omega} = \alpha \frac{2kT}{C_G \omega_T} = a \tag{1.9}$$

where ω_T and α are respectively the cut-off angular frequency and a process-dependent constant whose value is about 2/3 for silicon FET. The white current noise, or parallel noise, instead is due to the shot noise associated with the leakage current of both the detector (I_D) and the preamplifier input transistor gate (I_G) and also to the current noise of any resistance connected to the gate of the latter (I_R). Therefore the expression of the white noise current is:

$$S_{iw} = q(I_D + I_G + I_R) = qI_{TOT} = b \tag{1.10}$$

Finally, the flicker noise is related to the charge trapping phenomena. The expression is:

$$S_{vf}(\omega) = \alpha \frac{2kT}{C_G} \frac{\omega_c}{\omega_T} \frac{1}{|\omega|} = \frac{c}{\omega} \tag{1.11}$$

where A_f and ω_C are the 1/f process parameter and the frequency at which flicker and white voltage noise power spectral densities are equal. According to the model developed and to Eq. 1.8, the ENC of the system can be expressed as :

$$ENC^2 = (C_G + C_D)^2 a \frac{1}{\tau} A_1 + (C_G + C_D)^2 c A_2 + b\tau A_3 \tag{1.12}$$

where:

- A_1, A_2 and A_3 are the so-called shaping factors, coefficients that depend only on the filter output-pulse shape.
- τ is the characteristic time of the front-end, also referred as shaping time.
- C_D is the detector capacitance.

If in equation 1.12 we substitute the expression of the noise contributions (equations 1.9, 1.10 and 1.11) we obtain:

$$ENC^2 = A_1 C_D (\sqrt{\frac{C_D}{C_G}} + \sqrt{\frac{C_G}{C_D}})^2 \alpha \frac{2KT}{\omega_T} \frac{1}{\tau} + A_2 C_D (\sqrt{\frac{C_D}{C_G}} + \sqrt{\frac{C_G}{C_D}})^2 \alpha \frac{2KT}{\omega_T} \omega_c + A_3 q I_L \tau \tag{1.13}$$

As evident from the expression above, the three terms respectively represent the series, parallel and flicker noise contributions of the ENC of the system. In Figure 1.9 we can see the trend with the shaping time of the filter, highlighting the single contributions dependence from it.

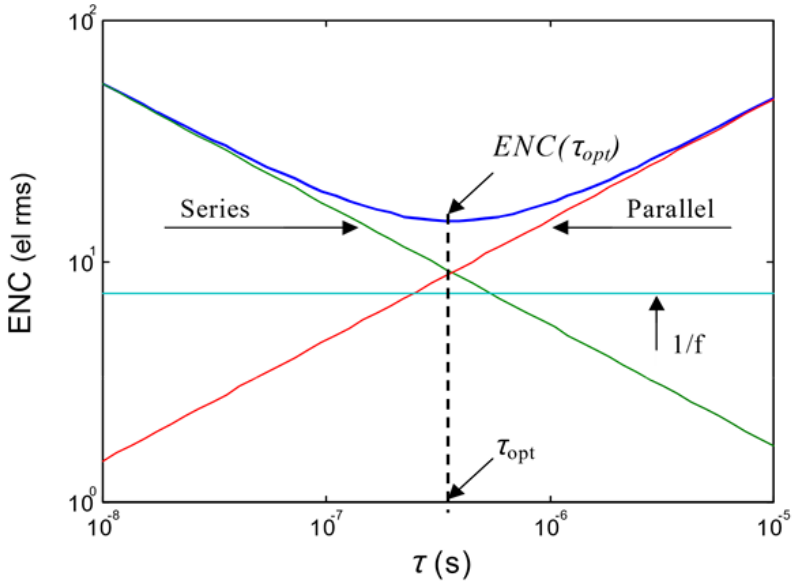

Figure 1.9 *ENC as a function of the shaping time.*

For low τ dominates the contribution of the noise series, while for long times the series noise becomes negligible (we can think that it is mediated over time), but the parallel noise due to leakage currents becomes dominant. Anyhow, as shown in the graph, there is an excellent shaping time. This time must be evaluated from time to time depending on the characteristics of the system: capacity of anode and gate, transconductance of the JFET, leakage currents, etc .... To calculate the optimal τ it is sufficient to equal the series and parallel components, obtaining:

$$\tau_{opt} = \sqrt{\frac{C_D}{I_L \cdot \omega_T}} \tag{1.14}$$

Because of its dependence on the characteristics of the components, the τ_{opt} and all the minimum ENC depend on the operating temperature of the detector: in fact, by cooling, there is a noticeable reduction in parallel noise therefore a notable improvement of ENC, besides the optimal τ tends to move towards longer times. It should be noted that ENC depends somehow on C_D for the first two contributions; anyway a reduction of that value brings an improvement on noise performances. Moreover, both the series contribution and the 1/f value are multiplied by the M factor:

$$M = (\sqrt{\frac{C_D}{C_G}} + \sqrt{\frac{C_G}{C_D}})^2 \tag{1.15}$$

that is minimized when the matching condition C_D=C_G is achieved [3].

1.6 SDD (Silicon Drift Detector)

In the field of high performance detection technologies, the SDD detectors (Silicon Drift Detectors), introduced by E. Gatti e P. Rehak in 1983, play an important role [4–7, 12]. These detectors are characterized by a very low capacity of junction to the anode electrode that collects the charge; this feature allows to have better noise performance and get a very short duration signal that therefore make it very versatile for high rate count applications. These unique aspects make this detector the best candidate for spectroscopy measurements for high resolution X-rays and, then, for SIDDHARTA experiment.

1.6.0.1 Working principle

The working principle of SDD can be understood starting from the sideward depletion concept showed in Fig 1.10. Compared to a conventional PIN-junction detector (Fig.1.10a), where n+ and p+ ohmic contacts cover the full area of opposite wafer sides, thus leading to an area-dependent anode capacitance which makes the PIN diode not suitable for low-noise applications, the SDD bulk depletion is achieved by positively biasing a small n+ contact with respect to p+ electrodes placed on both sides of the wafer (Fig.1.10b). Applying a high enough n+ (anode) voltage ensures that the two space-charge regions merge together (Fig.1.10c), leaving just a small undepleted bulk region only in proximity to the anode electrode. Compared to the conventional PIN diode, the sideward depletion of the bulk guarantees a lower biasing voltage for the same detector thickness. From Fig.1.5 it can also be observed that the electric potential energy along the orthogonal dimension to the wafer surface has a parabolic shape with a minimum located at half the thickness of the bulk, which is where photo-generated electrons are attracted. In this way the complete emptying of the area is achieved by applying a bias voltage of about four times lower in comparison to that necessary for a common diode of the same thickness: about 100V per a thickness of 350μm. With this mechanism the diagram of potential energy (for electrons) perpendicular to the surface of the wafer has a parabolic pattern, with the minimum placed in the center of the wafer itself.

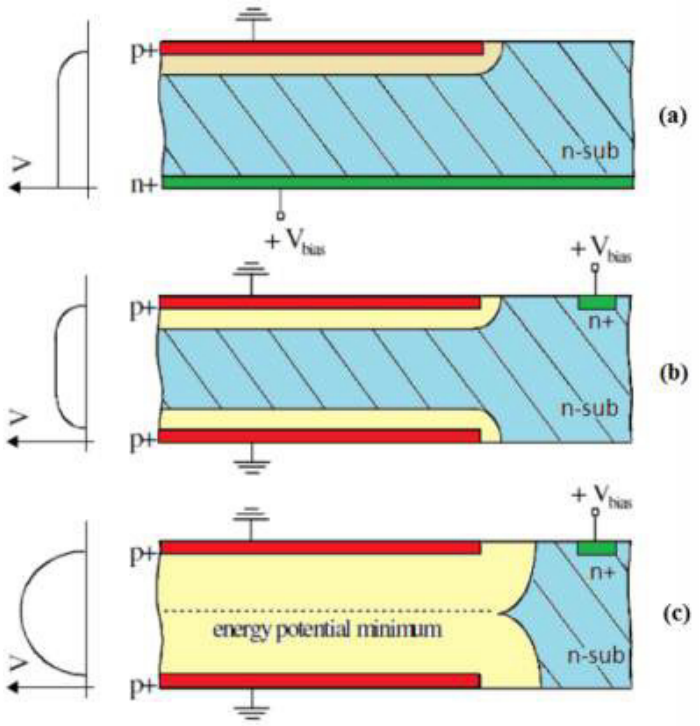

Figure 1.10 *(a) Structure of a traditional PN detector, (b) Non-polarized SDD detector, (c) Polarized SDD detector.*

The SDD is derived from this principle of sideward depletion by adding an electrical field parallel to the surface of the wafer to promote the electrons drift towards the anode electrode. This task is accomplished by the structure shown in Fig.1.11, where the single p+ implants of Fig.1.10b-c are replaced by two arrays of p+ electrodes on both sides of the wafer. The direction of the voltage gradient is such that the n+ readout anode is the point of minimum potential energy for electrons and therefore collecting all signal electrons generated in the depleted volume.

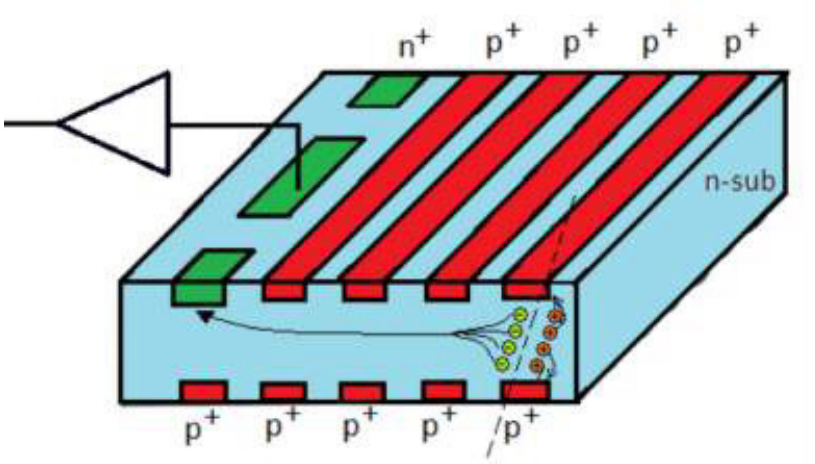

Figure 1.11 *(a) Structure of a traditional PN detector, (b) Non-polarized SDD detector, (c) Polarized SDD detector.*

The electric potential energy in the drift region is shown in the diagram of Fig.1.12a. Charge carriers generated by the ionizing radiation experience difference paths: the electrons move toward the anode region of the SDD along the potential channel while the holes are quickly collected by the nearest p+ electrodes under the push of the depletion field. In order to promote electrons charge collection, the bottom of the potential channel, as visible from Fig.1.12b, bends toward the anode electrode by suitably biasing the p+ implants on the opposite side. The output pulse induced at the anode by the electrons cloud is generated only when the carriers are close to it due to the electrostatic shield effect of the p+ electrodes. Measuring the drift time of the electrons could be useful to estimate the interaction coordinates while the collected charge provides information about the energy released by the ionizing event. The main advantage of a Silicon Drift Detector compared to the conventional PIN diode is the low collecting-electrode capacitance for the same device area and thickness, which is in the order of 100 fF and it is furthermore independent from the detector active area, allowing to reduce both the electronic noise, thus improving spectroscopic performance, and the signal processing shaping-time

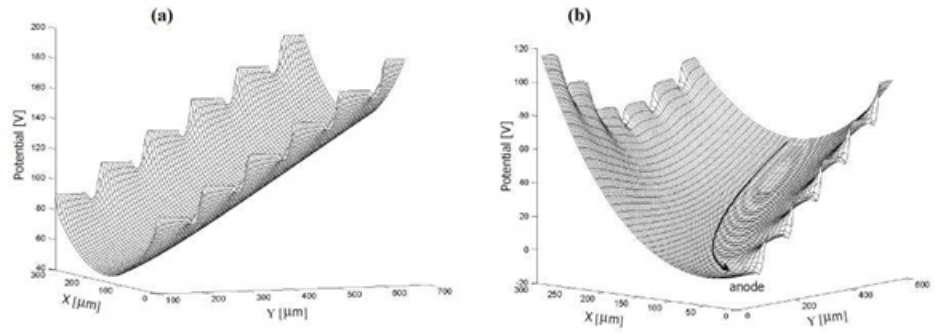

Figure 1.12 *Electric energy potential diagrams in the drift region of the SDD (a) and in proximity to the anode electrode (b).*

In the Figure 1.13 instead we can see the actual structure of a SDD for X-ray spectroscopy. One side is a unique p+ (BACK) contact in order to have a uniform entrance window. On the other side, cylindrical contacts (RING) are located to shape the potential. The small n+ anode is located in the center of the device. In order to take advantage of the good energy resolution of these detectors, parasitic capacitances of the connection cables and of the external amplifier must be very small. The best solution is to integrate the first stage (first-FET), directly into the chip, in this way the capacities of the connections between detector and external amplifier are replaced by a short strip of metal directly on the chip. In Figure 1.13 we can see that the amplifier is realized with an n-channel JFET, designed to work in the high resistivity region (fully depleted) of the detector. The JFET transistor, usually in the center of the drift chamber is surrounded by the anode and by the p+ implants. The choice of preamplifying SDD signals by means of integrated JFETs relies, how said before, on the fact that the stray capacitances associated to the detector collection electrode are minimized thanks to the short metal strip connection between the anode and the JFET gate. By an accurate design of the detector layout the capacitance matching condition ($C_D = C_G$) can also be ensured, thus further improving noise performance. The JFET transistor can be effectively considered as part of the preamplifier and therefore it is correlated to the front-end electronic design. The transistor is separated from the anode by a potential barrier generated by a guard ring (IGR). The gate of the JFET is connected to the anode; the source and the drain are available externally for the readout.

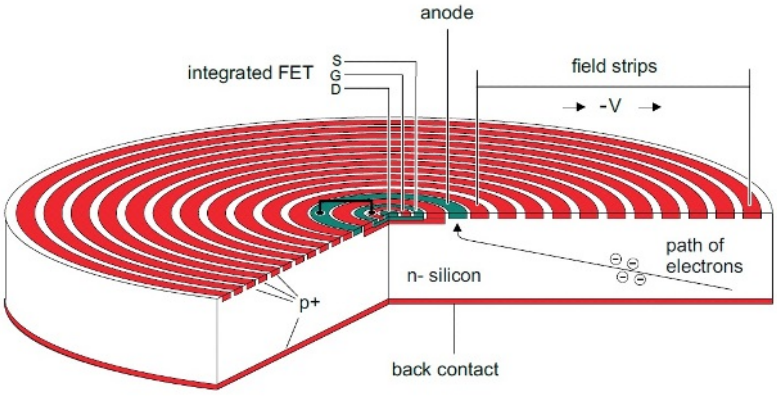

Figure 1.13 *SDD for X-ray spectroscopy: schematic structure with the p+ back contact*

Integrating the JFET leads to a total capacitance, in addition to that of the SDD anode, below 20 fF, one order of magnitude lower than the one added by an external JFET or a CMOS preamplifier. Nonetheless the integration of the JFET involves some drawbacks, such as the need of using a sophisticated technology compatible for both SDD and JFET and poor noise performance because of the higher contribution of flicker noise. An evolution of the integrated-JFET SDD topology described above is the so called droplet-SDD (or SD^3) shown in Fig.1.14, in which the anode of the transistor is placed at the margin of the detector to achieve smaller dimensions thus further reducing the total anode capacitance down to 120 fF, approximately 80 fF lower than the circular topology. Apart from the energy resolution improvement, droplet-SDDs resolve the problem of charge photo-generation below the JFET region due to the incident radiation and leading to low peak-to-background ratios. The detector JFET region is indeed not an active area and it can be therefore shielded from incident photons.

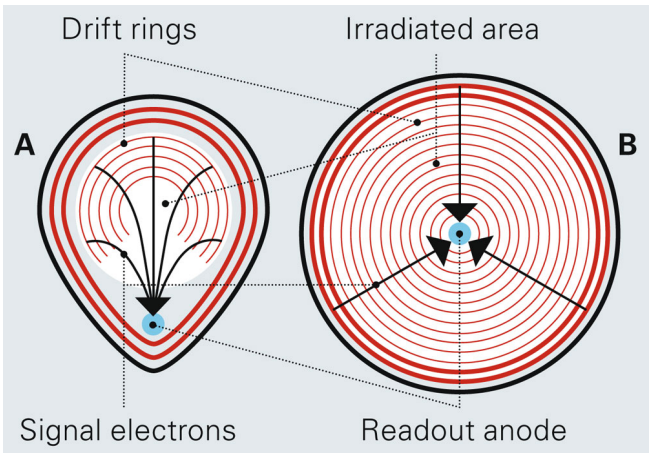

Figure 1.14 *Droplet (A) and circular SDD (B) with integrated JFET*

The transistor operates in source-follower configuration, with an external current generator connected to the source and to the gate connected directly to the anode electrode. In figures 1.15 it is shown the design of the SDD that SIDDHARTA employs for its first realization.

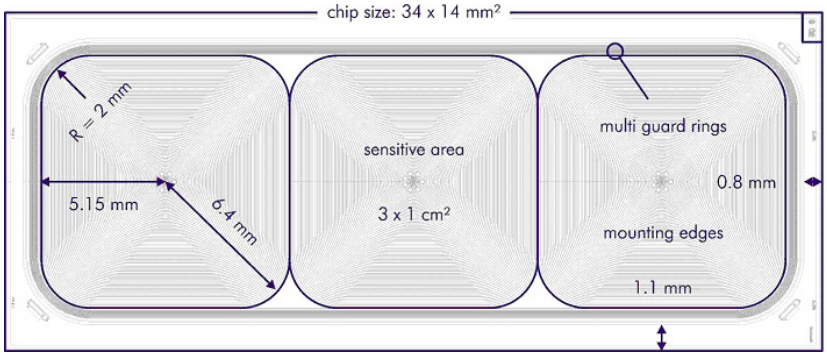

Figure 1.15 *Structure of the SDD used in the first experiment*

every chip integrates 3 SDD of 1cm of side, the thickness of the silicon wafer is 450µm and are 74 rings were created to create the potential gradient. SDDs need various voltages to be polarized correctly:

- BACK and last RING polarized at very negative voltage about -120V for completely empty the active area
- RING 1 polarized to a voltage of about -15V
- IGR polarized at about -20V to electrically separate the JFET channel from the detector substrate

The very low contribution of the noise series (due to the low capacity of the anode and to the integration on the transistor chip) and the low value of the leakage current maintain the overall noise at low levels even at room temperature for the detectors of SDD with a surface of 5mm^2, allowing to obtain acceptable values for the energy resolution. As a consequence, the resolution values typical of traditional detectors (cooled with liquid nitrogen) are reached with an SDD at lower temperatures (between -10 ° C and -20 ° C), obtainable with a simple thermoelectric cooling using a Peltier element. In the SIDDHARTA experiment, given the very large surface of the detectors used (1cm^2), to limit the thermal noise they will be cooled to low temperatures (around -100 ° C). However, the particular structure of the SDDs guarantees a great versatility of use in a lot of different fields. An important element on which to focus our attention and which characterizes the detector is related to the timing of signal formation: commonly

for an SDD ranging from 250 ns at 1µs, thus making count rates even higher than this Hz. The ability to perform measurements with trigger mechanism in SIDDHARTA is linked to this peculiarity of the SDD. In the first version of SIDDHARTA, it was decided to utilize an integrated JFET directly in the SDD detector. In the new version instead, also thanks to the innovation introduced with CUBE (a preamplifier developed at Politecnico di Milano - explained in the next paragraph), it was possible to place the preamplifier outside the SDD detector, without a worsening in the performances, leaving the SDD much more uniform.
The new experiment is planned for 2018-2019, both in the DAFNE collider (in Frascati) and in JPARC (Japan Proton Accelerator Resarch Complex) collider (in Tsukuba, near Tokyo). This new experiment will employ detection rings formed by 8 SDD, distributed in 2 rows and four columns, as shown in Figure 1.16.

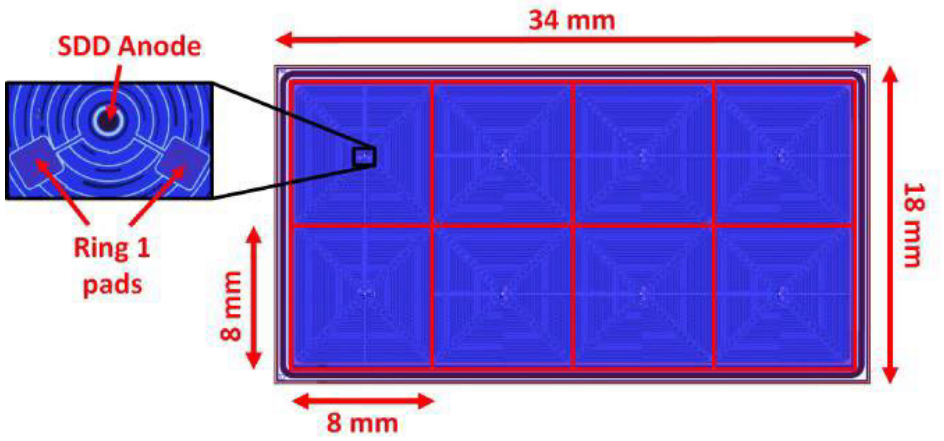

Figure 1.16 *SIDDHARTA 2 detector module*

The eight square shaped SDD units are made by Fondazione Bruno Kessler (Trento, Italy). Moreover, is possibile to notice that the central zone of the cell is reserved for the anode and the ring 1 pad, without any presence of preamplifiers. On the cercamic have been inserted holes of 2.4 mm diameter to allow the bonding for ring 1 biasing and to connect the anode to the CUBE preamplifier input., that will be described in the next paragraph.

1.7 Cube Preamplifier

The need of better spectroscopic performance has inspired, along the years, to look for alternative solutions to JFET . Given the quick growth that the microelectronics

market has encountered in the last decade, many efforts have therefore been oriented to explore the feasibility of CMOS implementations as external charge preamplifiers, leading to the development of monolithic CMOS integrated circuits showing superior performance, both in terms of noise and bandwidth, than the JFET-based counterparts. Considering that the general trend, in most applications, is to increase the count rate in order both to reduce the measurement time and to increase the accuracy thanks to the higher statistics, so the system noise performances at short processing times are of primary concern. The proposed circuit, developed at the Politecnico di Milano, is a CMOS CSA named CUBE, intended to be wire-bonded to the SDD anode, as shown in the block diagram of Figure 1.17:

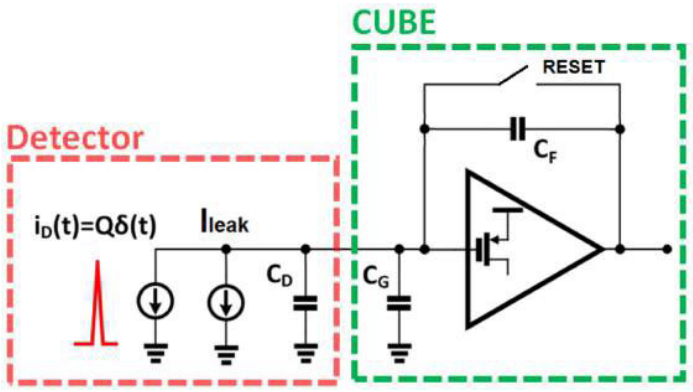

Figure 1.17 *SDD readout by the CUBE charge preamplifier*

The higher anode capacitance due to the wire-bond connection parasitic capacitance is compensated by the high transconductance of CUBE input p-MOS compared to JFET preamplifiers. This basically relies on the CMOS process scaling, oriented to a reduction of transistors dimensions, thus of their gate capacitance for the same transconductance value. A well-engineered anode-to-preamplifier connection is anyway required to minimize the overall capacitance, reason for which CUBE is typically mounted in close proximity to the SDD anode and therefore it is cooled down to the detector operating temperature, leading then to compact detection modules, an example of which is presented in Fig 1.18

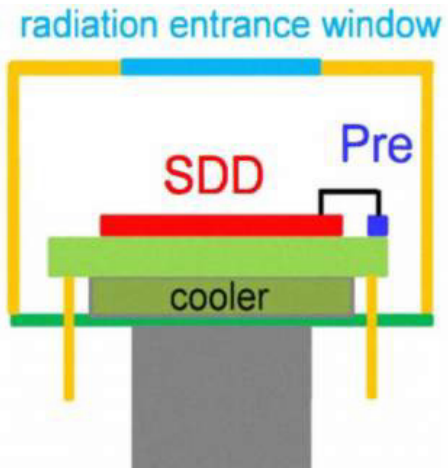

Figure 1.18 *Example of detection module made of a SDD and CUBE charge preamplifier*

The signal at the input of CUBE is made by a constant current (detector leakage current) and by the signal of interest, a series of current spike (approximabe by current δ function). The preamplifier integrates those currents, showing at its output the waveform in Figure 1.19 (V_{OUT} is the output, V_{rd} is the reset signal for the CUBE preamplifiers). The ramp is made by the integration of the leakage current, the steps are the effect of the integration of short duration spikes, which amplitude is proportional to the energy value of the absrorbed event.

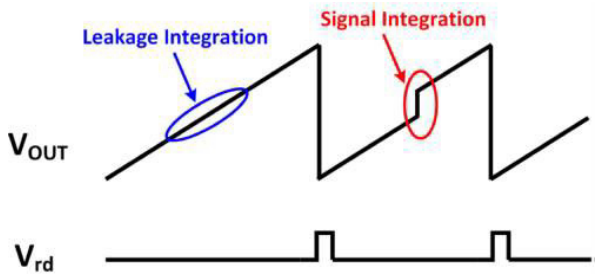

Figure 1.19 *Output voltages of CUBE preamplifier*

CUBE is equipped with a digital reset that allows to discharge the feedback capacitor (C_F), setting V_{OUT} to zero, and allowing a continuous acquisition of event without saturating the preamplifier [8]. The choice of the type of preamplifier is determined not only by considerations of noise, but above all from stability. For SIDDHARTA, due to the low rate of events desired, one data acquisition and accumulation phase has an expected duration of approximately 6 months; it becomes then a circuit that keeps its characteristics stable in this way is essential prolonged within 1‰. By stability of a system, we mean that property of the circuit to always supply it same mean level

of output signal, with the same amplitude of the input quantity. The term "medium" indicates that in any case there will be a dispersion of the signal of output due to noise. Therefore, to check stability, we consider a large number of events. For a spectroscopy system, gain stability becomes relevant when the period of statistical fluctuations becomes comparable with the duration of the phase of data acquisition. Therefore stability becomes fundamental in an experiment like SIDDHARTA, where the acquisition phase will last for a few months without interruption.

Chapter 2

SFERA ASIC

In this chapter the SFERA ASIC is presented and its features explained. Finally the modifications and the improvements of the new release are introduced.

2.1 Introduction to the ASIC

In this chapter we present SFERA (SDDs Front-End Readout Asic), a low-noise fully-programmable 16 channel readout ASIC designed for both X- and γ -ray spectroscopy and imaging applications. The design has been guided by the use of Silicon Drift Detectors (SDDs) and CUBE charge sensitive amplifiers (CSAs). The idea of developing a general purpose readout front-end which is able, in principle, to meet a wide range of specifications for both X and γ-ray spectroscopy applications has been investigated and subsequently implemented in the design of SFERA. It has originally been thought as an upgrade of the SIDDHARTA-1 readout electronics. The chip is designed to process signals coming from solid-state detectors and CMOS preamplifiers. Three data multiplexing strategies are implemented: the so-called polling X, intended for high-rate X-ray applications, the polling γ , for scintillation light detection and the sparse, for signals derandomization.

2.2 ASIC requirements

SFERA requirements such as gains and peaking times have been outlined from system level considerations with both reference to the SDDs technology and energy resolutions achievable when coupling the detectors to CUBE preamplifiers. The analog shaping amplifier order and topology are a trade-off between noise performance, pile-up probability, ballistic deficit immunity, power consumption and circuit complexity while three data multiplexing strategies have been adopted to fulfil different applications.

2.2.1 Choice of the filter (Shaping Amplifier)

The filter chosen for the SFERA analog readout channels is the semi-Gaussian. The order depends on the trade-off between three parameters: Balistic Deficit (BD), high throughput capability and energy resolution. Figure 2.1 shows the response of the four different filters with the same width of the pulse at 1%. of the peak. For shaping time showed in tab.2.1 it is considered the time between the 1% pulse amplitude and the peak.

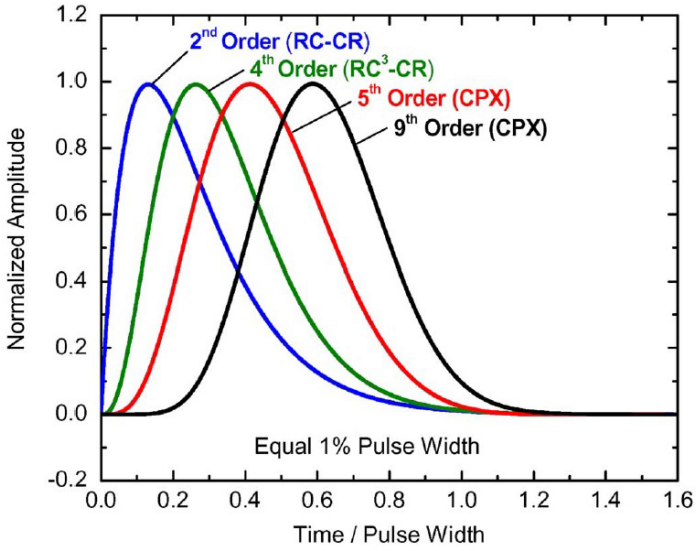

Figure 2.1 *Comparison between four filters with 1% of pulse width [1]*

We can see that the 2nd order CR-RC presents for instance a short rising time compared to the 9th order, despite its worse symmetry around the peak. As already stated to choose the proper filter it was necessary to introduce some constraints:

- **High throughtput:** Capability refers to the pile-up probability which, given a certain input photons rate, decreases with the width of the filter output shaped-pulses. The 9th order potentially offers the best performance thanks both to its higher pulse symmetry and lower width. A more quantitative analysis of the pile up is address in [9–11]

- **Ballistic Deficit:** The ballistic deficit is a phenomenon which affects both X and γ-ray detection systems. The Figure 2.2 shows the Ballistic Deficit. This effect depends on the finite drift time of the photo-generated charge travelling towards the SDD anode electrode. The electrons cloud (Amplitude vs Drift Time) is spread in time, with a distribution that for simplicity is considered to be uniform. This is exactly what happens when incident photons are detected far from the SDD anode. The more distant an event is detected, the longer the drift time is. The spectrum energy peak measured in electrons has the following expression :

$$E_{peak} = N_e \frac{max[y(t)]}{max[h(t)]} \tag{2.1}$$

where N_e is the number of generated charge carriers, y(t) is the real filter response with SDDs, and h(t) is the filter pulse response.

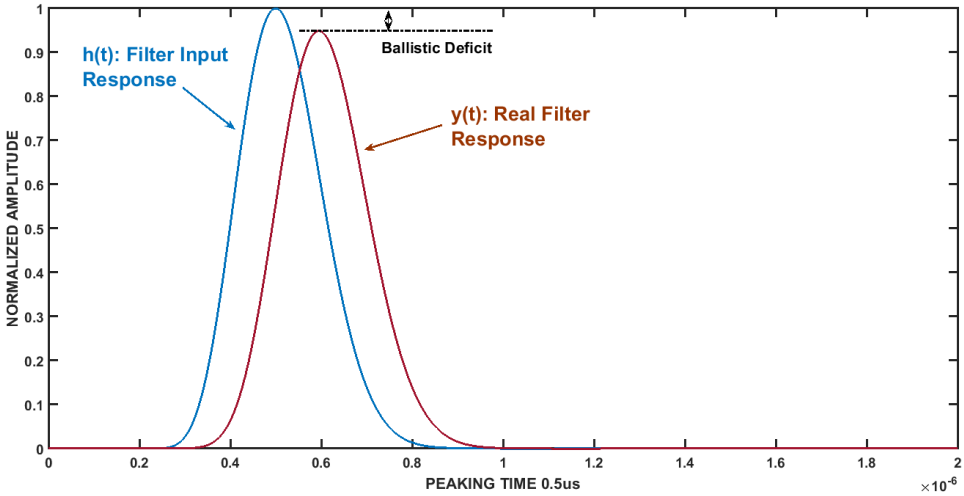

Figure 2.2 *Filter output signals in case of ideal delta-like input h(t) and real input signal from SDDs y(t).*

So if we want to quote the Ballistic Deficit:

$$BD = \frac{max[h(t)] - max[y(t)]}{max[h(t)]} = 1 - \frac{max[y(t)]}{max[h(t)]} \tag{2.2}$$

In the Figure 2.3 instead we can see an example of anode current waveforms for charge carriers generated at different distances from the electrode, thus for different drift times t_{drift}.

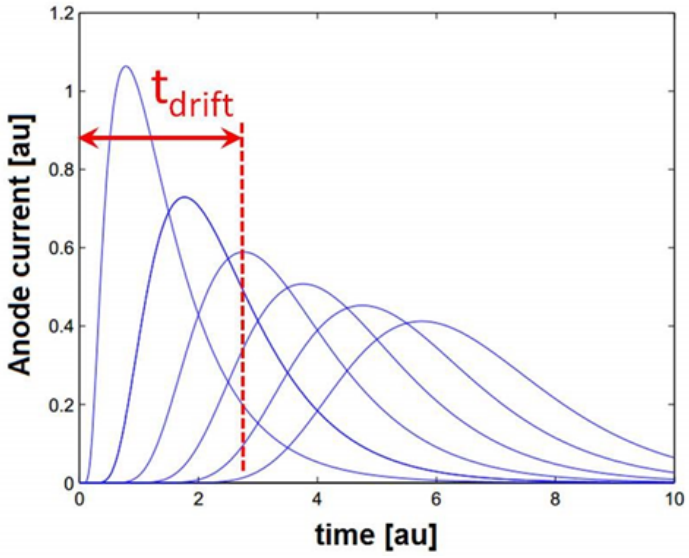

Figure 2.3 *Anode current waveforms for different drift time.*

What is important to note is that the Ballistic Deficit and the system noise performance follow same trends with the filter peaking time. If the latter is increased, the ballistic deficit gets lower. With all these considerations, definitely, analyzing the Figure 2.4 it was chosen for SFERA a shaper with semigaussian filter with complex conjugate poles of the 9th order. This filter ensures high pile-up immunity, great performances for the ballistic deficit, and excellent results regarding the energetic resolution.

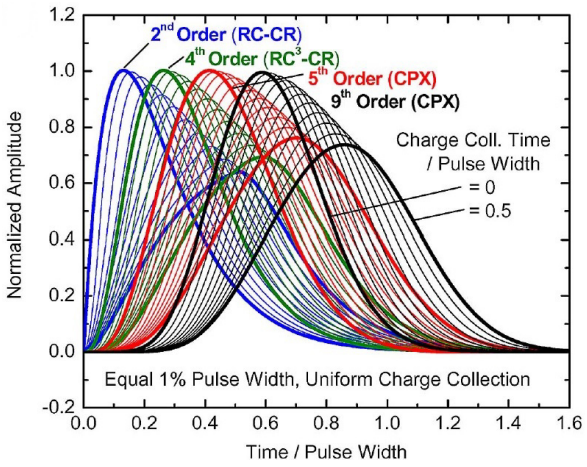

Figure 2.4 *Ballistic deficit effect on the four shapers output pulses, for different collection times [1]*

2.2.2 Peaking Times

The choice of the peaking times (t_P) to be implemented relies on preliminary considerations about the state-of-the-art spectroscopic performance achievable with SDDs coupled to CUBE preamplifier. Using an evaluation system with a square SDD with 64 mm^2 of active area, cooled down to 240 °K, it has been obtained better results with shaping time of 1.5 μs and 2 μs due to the fact that we obltain the optimum value of the system ENC. Moreover shaping times of 0.5 μs and 1 μs have been added, to reduce the pile-up probability for high rate x-ray spectroscopy, this comes at the cost of lowering the energy resolution. Instead for γ ray applications with wide area monolithic scintillators, also the 4 μs and 6 μs shaping times were implemented. In conclusion, six different peaking times has been outlined, namely 0.5 μs, 1 μs, 2 μs, 3 μs, 4 μs and 6 μs. An additional peaking time of 200 ns has been chosen for the fast shaper. We can summarize everything in the following table:

T_P [μs]	Application
0.2	fast shaper
0.5	high throughput
1	high throughput
2	high energy resolution
3	high energy resolution
4	scintillator light (γ rays)
6	scintillator light (γ rays)

Table 2.1 *Analog processing-chain peaking and shaping times implemented in SFERA.*

2.2.3 Filter Gains

Depending on the target use of the chip, the analog acquisition chain CUBE-SFERA must be able to handle different input energy (E_{in}) and dynamic ranges (DR). It is therefore convenient, that the shaping amplifier implements a different peak gain for each of them, such that input and output DR are matched. The first energy range that has to be detected is the 10 keV, used to characterize the system with a standard ^{ff}Fe x-ray source, or for low energy systems (soft x-rays). Second energy range is specific for the SIDDHARTA experiment: the energy associated to the kaonic hydrogen (for the deuterium isotope) is 16 keV. Another range is the one of 36 keV, this is useful because for SIDDHARTA (along parallel projects) it may happen that thicker SDD detectors (400 μm) will be used, these detector will be able to stop more energetic particles, therefore an higher energy range is needed. Two further gains have been implemented with the purpose of detecting X-rays with very thick detectors and scintillation light in γ-ray applications. These two energies are measured in photo-electrons generated from scintillation light detection and are 50 keV (13800 photo-electrons) and 20000 photo-electrons. These dynamic ranges have to be fitted with the SFERA's electronics. In order to do it the maximum CUBE voltage and the energy involved must be considered in the equation:

$$\Delta V_{out,CUBE-max} = \frac{Q_{max}}{C_F} \tag{2.3}$$

Where Q_{max} represents the charge generated in the SDD bulk by the signal at the upper edge of each considering the dynamic range, while C_F is the 25 fF CUBE feedback capacitance and $\Delta V_{out,CUBE-max}$ the maximum output voltage variation of the CUBE preamplifier. Table 2.2 summarizes the input energy dynamic ranges that have been outlined for the design of SFERA, with the corresponding total gain and application:

E_{in}	Gain	Application
10 keV	230 $\frac{mV}{keV}$	system characterization and soft x-rays
16 keV	144 $\frac{mV}{keV}$	SIDDHARTA
36 keV	64 $\frac{mV}{keV}$	SIDDHARTA with thick SDDs
50 keV	46 $\frac{mV}{keV}$	x-rays with thick detectors
20000 e^-	115 $\frac{\mu V}{e^-}$	γ rays measurements

Table 2.2 *Summary of gains implemented in SFERA.*

2.3 SFERA Design

The SFERA ASIC is a 16-channel IC suitable for both X and γ-ray spectroscopy and imaging applications. The purpouse of this ASIC is to filter and properly shape the pulses that are feed at its imput by the detector-preamplifier pair (SDD and CUBE for the SIDDHARTA experiment) The general architecture of the overall pulse processing chain is shown in the block diagram of Figure 2.5.

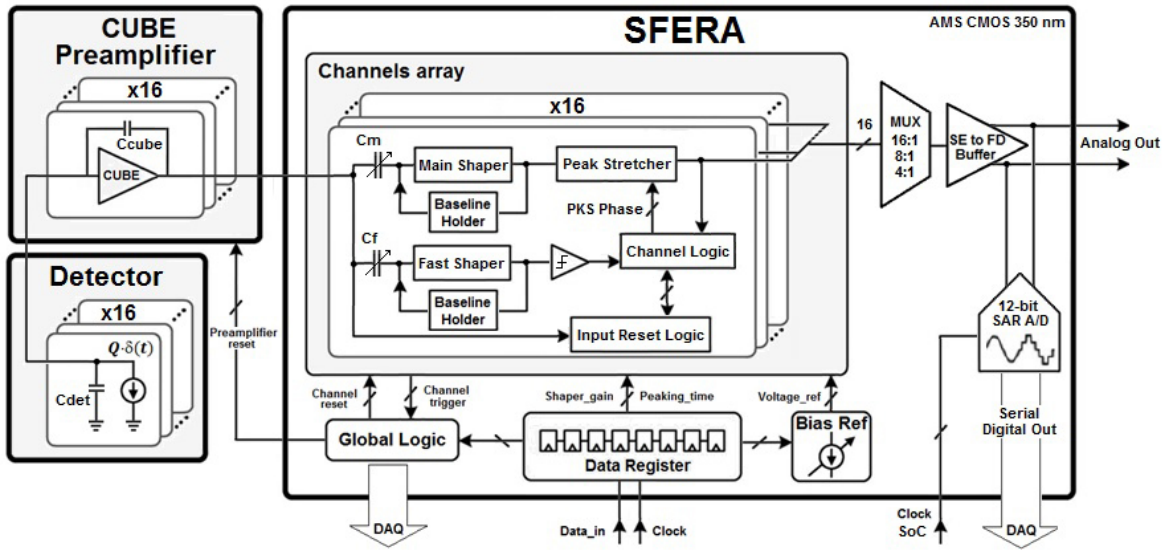

Figure 2.5 *SFERA simplified block diagram*

The analog section of the chip comprises a bank of 16 readout channels each of which integrates the main shaping amplifier and an additional 9th order semi-Gaussian SA with the same peak-gains but fixed 200 ns peaking time (the fast shaper), designed to accomplish pileup rejection (PUR) purposes. Both main and fast SA output baseline

voltages are stabilized by baseline-holder (BLH) circuits. The main shaper is then followed by a three-phase peak-stretcher (PKS) and by some digital logic (the channel logic) dedicated to the PKS phases synchronization and to properly discard piled-up events. A digital logic section common to all channels (the global logic) is instead responsible for driving the output multiplexer (MUX) in all the different operational modes and furthermore for storing in a 256-bit internal data register (SRAM), by means of an SPI communication control interface, for example to select gain and peaking time, tune internal comparators thresholds, define the duration of time-coincidence windows and to program voltage and current-references. Beyond that, the global logic handles all the I/O signals that enter and exit sfera, providing a communication interface with the external DAQ system with LVDS electronic (TRX). Part of the global logic (reset logic) is dedicated to generate the reset signals to CUBE (taking this duty from the external DAQ), using threesholds on the signal at the output of the preamplifier. Moreover the the reset logic has the duty to disable the BLH and PKS in each channel during the reset of the CUBE, this to avoid any casual spurious signals that may possibly be acquired and appear in the spectrum. SFERA integrates two single-ended to fully-differential analog output buffers in order to let the MUX be operated also in 8:2 and 4:2 mode, particularly suitable for instance in high throughput applications. Three additional single-ended buffers offer the possibility to monitor the main and fast shaper output and also the ASIC input voltage of a single channel, selectable by an SRAM bit. Current and voltage references are on-chip generated by means of dedicated trimming DACs properly programmed by static bits in the SRAM in order to minimize the amount of external electronic components.

2.3.1 Shaping Amplifier

The topology that has been chosen for SFERA shaping amplifiers is the semi-Gaussian [13]. The design relies on a trade-off between ballistic deficit (BD), high-throughput capability and energy resolution, which all influence the ENC of the system. For this reason the order of the filter has been chosen to be the 9th by cascading a real stage (RE), that introduces the real pole of the transfer function, and four biquadratic (BIQ) cells, responsible for one complex-conjugate poles pair each. The shaper block diagram is illustrated in Fig. 2.6

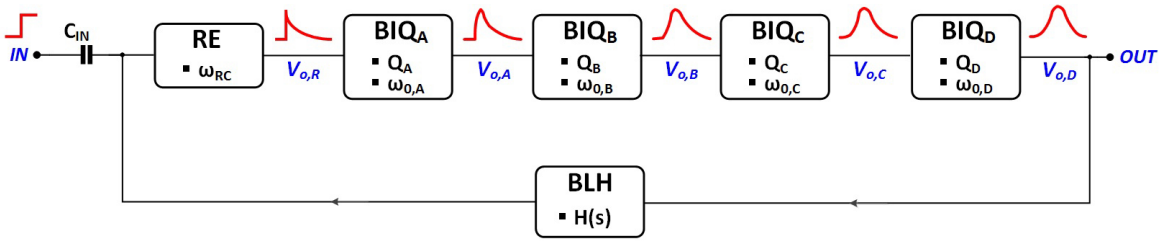

Figure 2.6 *Block diagram of the unipolar 9th order semigaussian filter*

The real stage, shown in Figure 2.7 is realized as a single-pole trans-impedance active filter with an input AC coupling capacitor (C_{IN}) to cut-off the cube output ramp due to the detector leakage integration. So C_{IN} introduces a zero at DC which compensates the pole at DC given by CUBE feedback capacitance (C_{CUBE}).

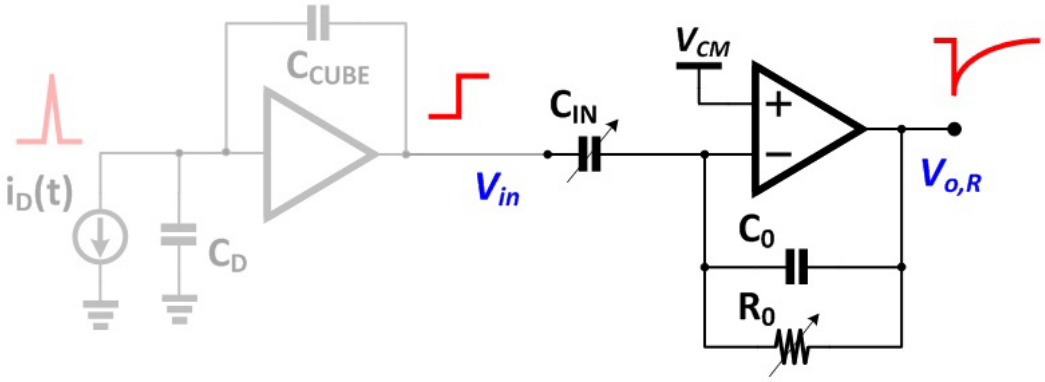

Figure 2.7 *Real stage of SFERA shaping amplifierr*

The real stage input-output voltage transfer function ($T_{RE}(s)$) and the frequency response from the input of the detector to real filter output ($T_1(s)$) are respectively:

$$T_{RE}(s) = \frac{v_{o,R}(s)}{v_{in}(s)} = -\frac{sR_0C_{IN}}{1+sR_0C_0} \tag{2.4}$$

$$T_1(s) = \frac{v_{o,R}(s)}{i_D(s)} = -\frac{C_{IN}}{C_{CUBE}}\frac{R_0}{1+sR_0C_0} \tag{2.5}$$

Having C_0 influence also on the filter frequency response, a constant value of 700 fF has been chosen for it. So the real pole frequency and the shaping amplifier peak-gain are selected by tuning respectively R_0 and C_{IN}, exploited by means of static selection switches, using the structure in Figure 2.8.

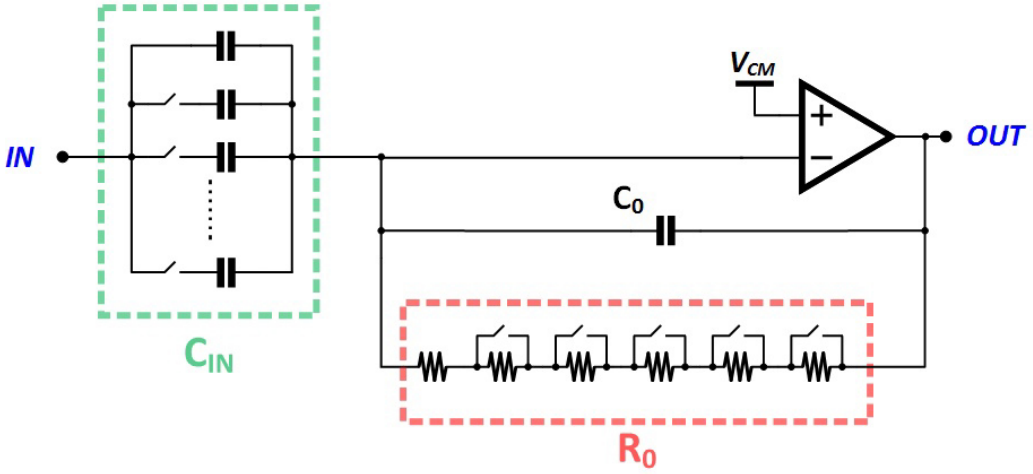

Figure 2.8 *Circuit implementation of the programmable real stage*

To implement each of the complex conjugate poles the chosen topology has been the multiple-feedback cell (MFB, or Rauch cell), showed in Figure 2.9 which is a bi-quadratic cell preferred to Sallen-Key for its insensibility to mismatches and the finite DC impedance allowing current to flow through the DC path represented by resistors R_3 and R_2. This is particularly useful to achieve an unbalanced biasing of the MFBs output voltage baselines along the chain, so as to extend as much as possible the stages output voltage shift and allowing eventually to design the real stage with a higher peak-gain. Amplifying as much as possible the signals at the level of the very first stages of the analog filter is indeed beneficial for minimizing their noise contribution.

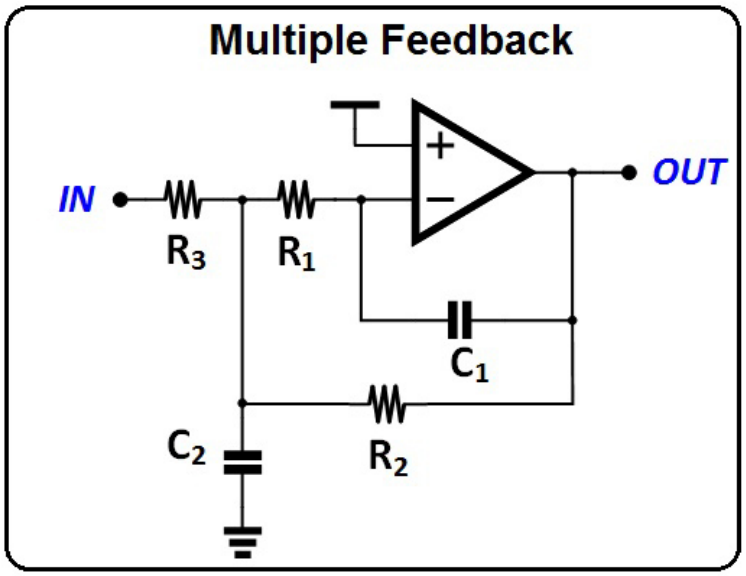

Figure 2.9 *Multiple-feedback, or Rauch cell*

The transfer function may be expressed as:

$$T_{BIQ}(s) = \frac{K\omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \tag{2.6}$$

With:

- $K = -\frac{R_2}{R_3}$ DC gain of the stage
- $\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}}$ cut-off frequency of the filter
- $Q = \frac{1}{\sqrt{\frac{C_1}{C_2}\left(\frac{R_1+R_2}{\sqrt{R_1 R_2}} + \frac{\sqrt{R_1 R_2}}{R_3}\right)}}$ quality factor of the filter

The circuit implementation of both main and fast shaping amplifiers is shown in Figure 2.10. where we can see that the output voltages are sensed by comparators whose task is to generate the trigger signals TR_{MAIN} and TR_{FAST} needed by the the output logic. An additional comparator is placed at the output of the real poles filter to detect photon energies out of the selected input dynamic range. Such photons cause in fact the real stage voltage-shift to be higher than expected hus it can generate a useful trigger TR_{HT}) by properly setting the comparator threshold.

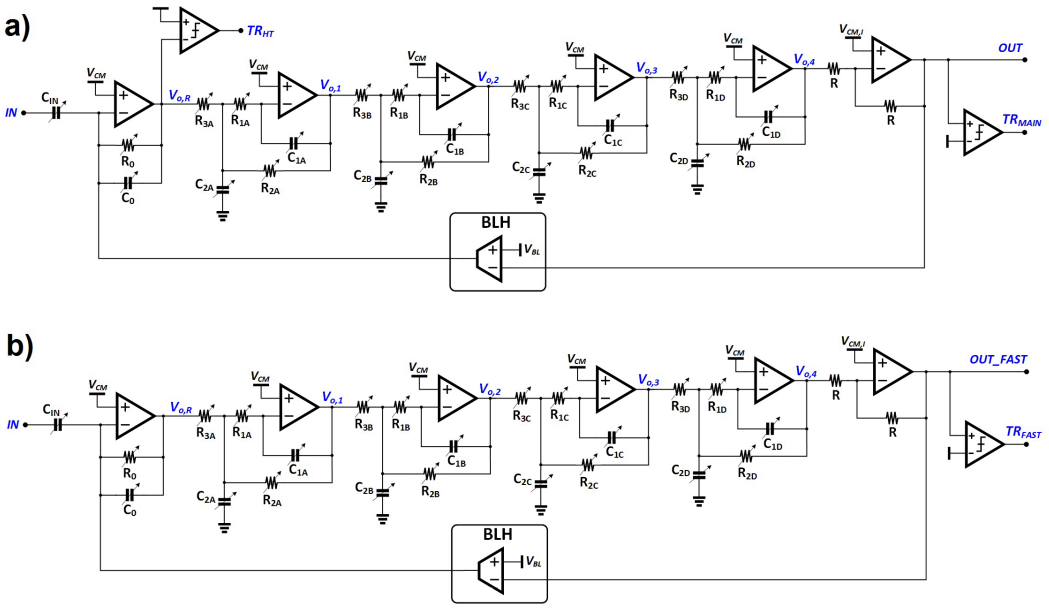

Figure 2.10 *Main (a) Fast shaper (b) (circuit implementation)*

In the Fig.2.10 we can also notice the baseline-holder (BLH), that has the task to stabilize the shaping amplifier DC output voltage baseline to a constant value, set

to 500 mV. Process, voltage and temperature variations are mitigated by its negative feedback operation. Moreover the BLH also avoid the output baseline to shift in case of high input photons rates.

2.3.2 Peak detector and Pile-up rejection circuit topology

Once an event has been correctly processed and shaped by the filter the peak of this output must be sampled and multiplexed to the output, leaving the DAQ the task of building the spectra. When the input rate is too high, however, the superposition of two signals could lead to a corruption of the acquisition (pile-up phenomena) and therefore degrading the spectroscopic performance of the front-end. Higher the event count-rate the more likely to occur pile-up, especially when dealing with high-rate X-ray spectroscopy applications, for which, therefore, an efficient joint peak detection and pile-up rejection strategy has to be implemented. To overcome this problem, a dedicated logic has been implemented, to detect the peaks of each shaped input and discard events if too close to each other. An effective solution, adopted for SFERA comprises a 3-phase PKS driven by the PUR logic control-signals. The main idea is starting an inspection window, and whenever an event is detected, making use of the TR_{FAST} signal of the fast shaper or the TR_{MAIN}. If no other photons are detected during such inspection window, the original event is then properly acquired. In case, instead, one or more additional photons hit the detector during this time window the PKS promptly discards the piled-up shaping amplifier output pulse, by not stretching its peak, and becomes ready again to track a next pulse. The strategy proposed is intended to allow the acquisition of also partly overlapped pulses with uncorrupted peak amplitudes. The 3-phase PKS architecture that has been adopted for the design of SFERA includes the read (RD), write (WR) and track (TRK) phase. The final circuit implementation is shown in the schematic diagram of Fig.2.11

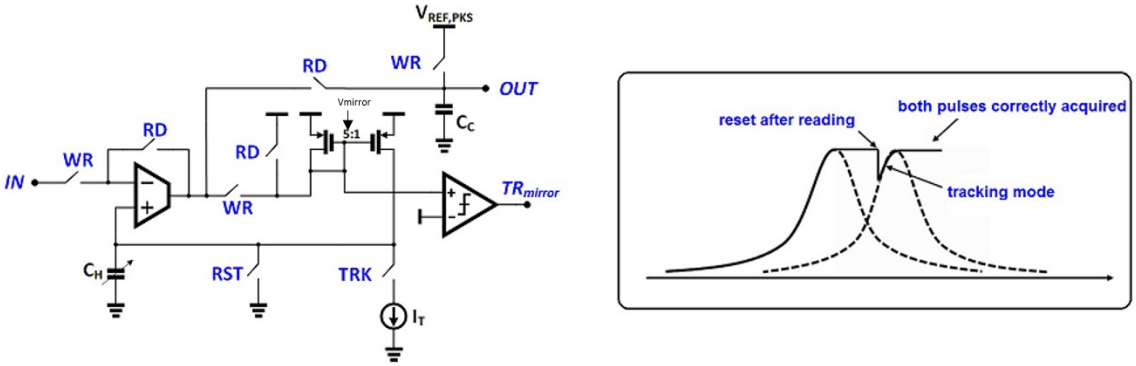

Figure 2.11 *3-phase PKS circuit implementation with control signals names (left) and working principle (right).*

In the Figure 2.12 there is the working block diagram of the signal presented above.

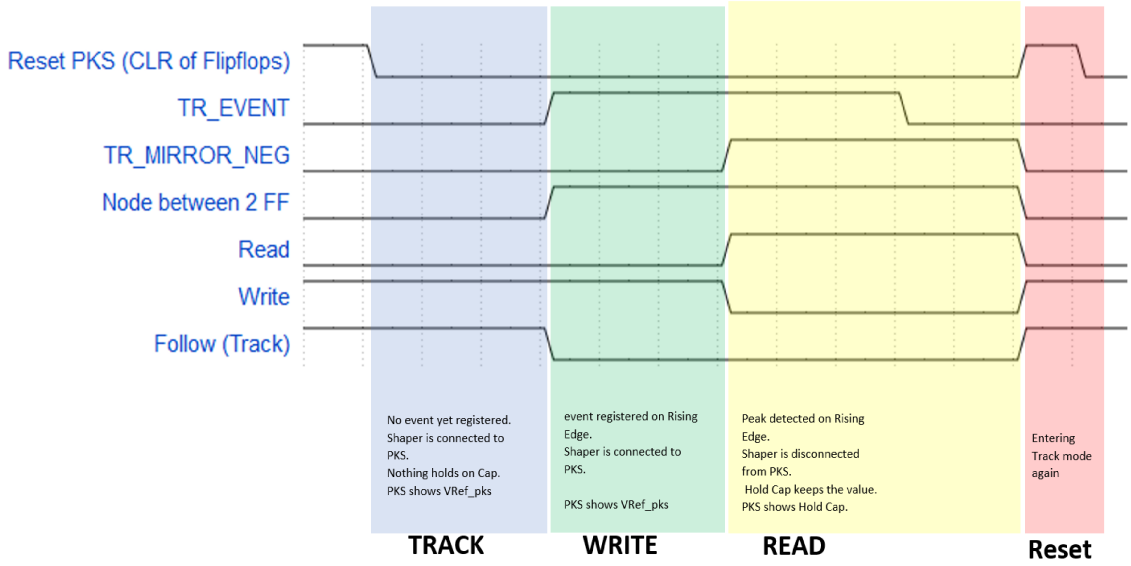

Figure 2.12 *Peak stretcher control signals.*

A description of the 3-phase PKS operation and digital control signals is instead presented in Fig.2.13

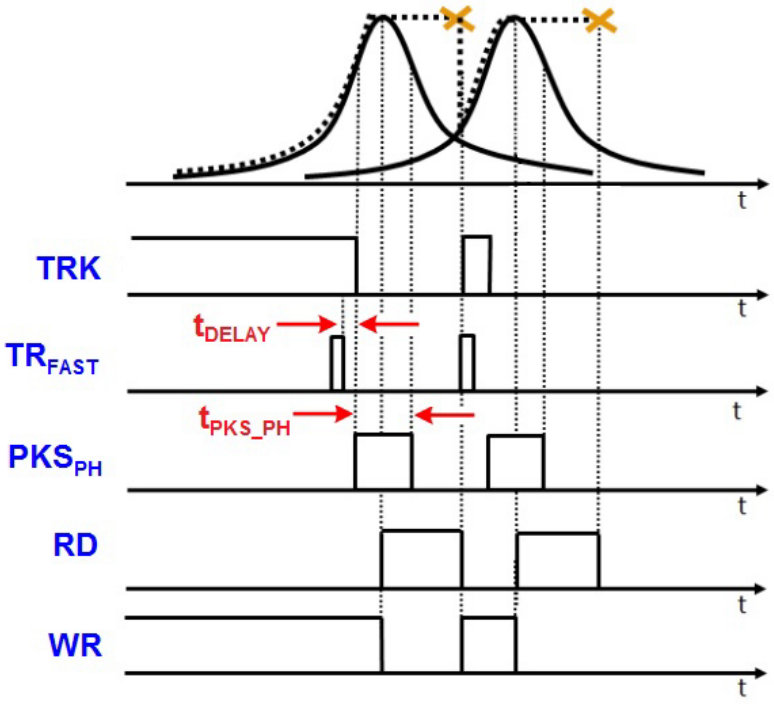

Figure 2.13 *3-phase PKS circuit implementation with control signals names (left) and working principle (right).*

WR and RD signals are in antiphase. During the tracking phase both the TRK and WR switches are closed, allowing the system to follow the input, being in a buffer configuration. A dedicated digital logic triggered by the falling edge of TR_{FAST} starts the time coincidence window after t_{DELAY}. If during this interval no other event occurs then the peak can be correctly sampled, otherwise peak is discarded (pile-up has occurred). T_{DELAY} and the next signal PKS (both user programmable) are chosen in such a way to obtain that the PKS_{PH} is centred around the peak and proportional to the shaping time. This means that in the middle of the PKS_{PH} interval, when the Read phase starts (RD switches closes, WR and TRK switches open), the peak and not side values of the filter output are read. This is the value that is stretched, sampled and multiplexed to the output, and at the end of this phase the PKS must be reset and brought to the Tracking phase, where C_H is discharged trough the current generator I_T. The digital logic responsible for the proper synchronization of PKS phases (TRK, WR and RD signals generation) operates jointly to the PUR logic, which basically prevents the PKS to switch from write to read by inhibiting the PKS signal generation in case of pile-up. The PUR section is designed to discard two events if they're too close in time. Before explaining its working principle it is necessary to define with which criterium it is identified the time interval for the discard, considering:

- rise time at 1% (t_R): interval between the 1% of the pulse amplitude and its peak
- fall time at 1% (t_R): interval between the peak of the pulse and the 1% of its amplitude

Considering the worst case 500 ns of peaking time, t_R has a value of 400 ns and t_F is more or less the same.

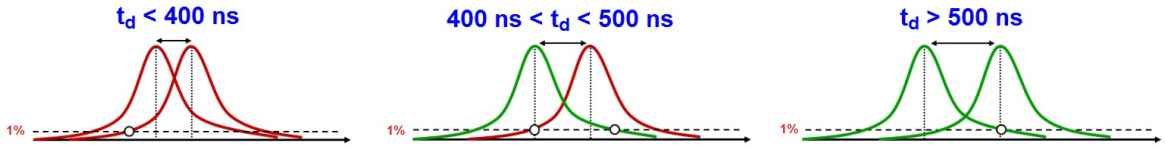

Figure 2.14 *PUR cases: in the first case both events are discarded, for the middle case the first event is acquired, the second is discarded, for the last case both events are acquired.*

As it is possible to see in Figure 2.14, if the second pulse is delayed for more than t_R from the first one, then the rising edge of the second pulse doesn't corrupt the first one (the peak of the first has happened before the 1% of the second pulse). In the second condition, PUR processes correctly the first pulse, but it cannot acquire properly the second one: if the delay is lower than t_F, the falling tail of the first peak will corrupt the second information. If the delay is lower than the shaping time, then both pulses will have their information corrupted and will be both discarded. The PUR circuit that implement what it has been discussed is shown in Figure 2.15

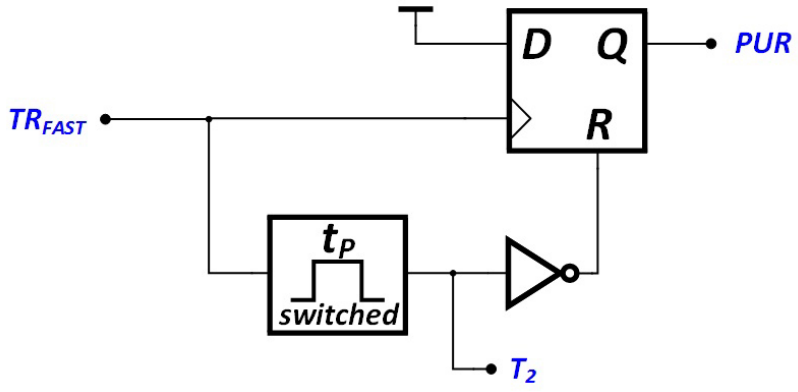

Figure 2.15 *PUR circuit.*

The input signal TR_{FAST} (generated by the fast shaper) starts the inspection window called T_2, thanks to the switched-mode monostable block; if during this time interval no other events are detected, then no PUR signal is generated at the output and the PKS can go to the Reading phase.

2.3.3 Multiplexer and Output Buffers

The analog values that come from the PKS are fed into an analog multiplexer (MUX) and subsequently buffered by two single-ended to fully-differential (SE-to-FD) output buffers, as shown in Figure 2.16.

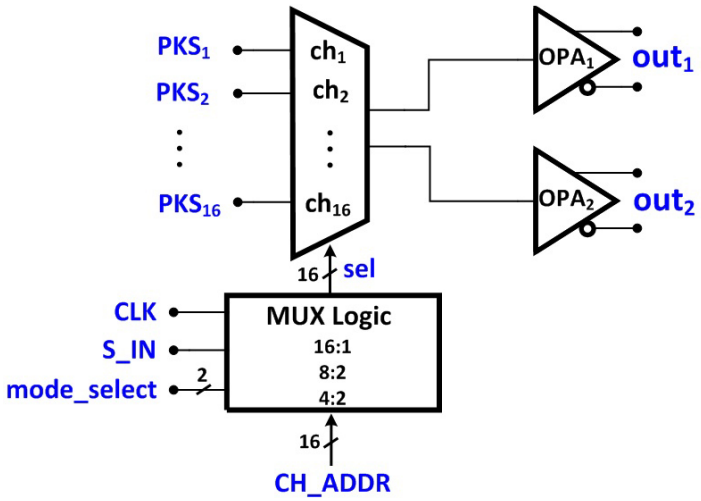

Figure 2.16 *MUX block diagram and single-ended to fully-differential output buffers.*

The multiplexer is organized in four banks of four switches each such that, the output data can be multiplexed in a 16:1 as well as 8:2, 8:1, 4:2 and 4:1 configuration, depending on the target application, and according to the static programming bits of the SRAM (mode_select). In the polling operational mode (both Polling X and γ) the MUX line selection-signal (sel) is incremented by 1 on each rising edge of the clock signal provided by the external DAQ system (CLK) in this way at the output is presented a continuous sequence of signals. A different readout protocol (the Sparse mode) requires instead only some specific channels, selected by dedicated address lines (CH_ADDR) also here the switch happens at the rising edge of the CLK signal, at the output is given only the sequence of selected channels. For the SIDDHARTA it is foreseen an input count rate of 1 Mcps, therefore the operative frequency of the MUX was set to 10 MHz; operating in 4:2 or 4:1 mode this means that each channel is read at 2.5MHz, sufficient for the above specifications. For what concerns the two output buffers their architecture is shown in Figure 2.17.

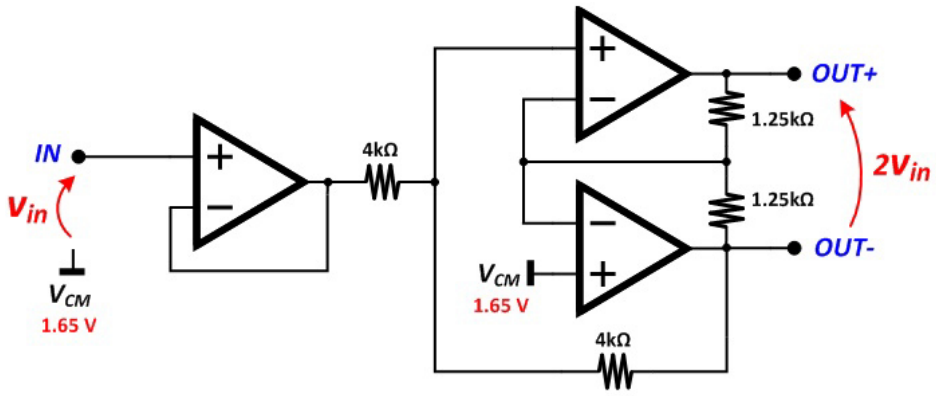

Figure 2.17 *Architecture of the output buffers, from Single Ended signal to Fully Differential (SE to FD).*

These components amplify the single ended signal by a factor two and converts it to fully differential; the signal will then be more robust against the common mode noise and disturbances that affects the analog outputs. Moreover they can drive a 50Ω coaxial line. All the different requirement for the output buffers are resumed in the next table.

DC gain	2
Input dynamic range	75 mV - 3.23 V
BandWidth	109 MHz
Power dissipation	57 mW
Slew rate +	230 $\frac{V}{\mu s}$
Slew rate -	239 $\frac{V}{\mu s}$
V_{OFFSET}	6.4 mV_{rms}
White noise at input ($S_{Vw\|in}$)	$29^2 \left(\frac{nV}{\sqrt{Hz}}\right)^2$
1/f noise at input ($S_{Vf\|in}$ @ 1Hz)	$7.2^2 \left(\frac{\mu V}{\sqrt{Hz}}\right)^2$

Table 2.3 *Amplifier specifications for the output buffers.*

Along these two, there are present other three single ended buffers, this to allow the

monitoring of the analog outputs of: main shaper, fast shaper and the output of the CUBE preamplifier of a selectable channel. In the next paragraphs, we will briefly analyze the three acquisition methods used in SFERA.

2.3.4 Polling X

In the polling-X multiplexing strategy, particularly suitable for high-throughput X-ray applications, the MUX operates a fast sequential readout of the PKS outputs, asynchronously and uncorrelated with peak detection and pile-up rejection operations taking place upstream. In the Figure 2.18 we have a summary of all the timing signals used in this acquisition modality.

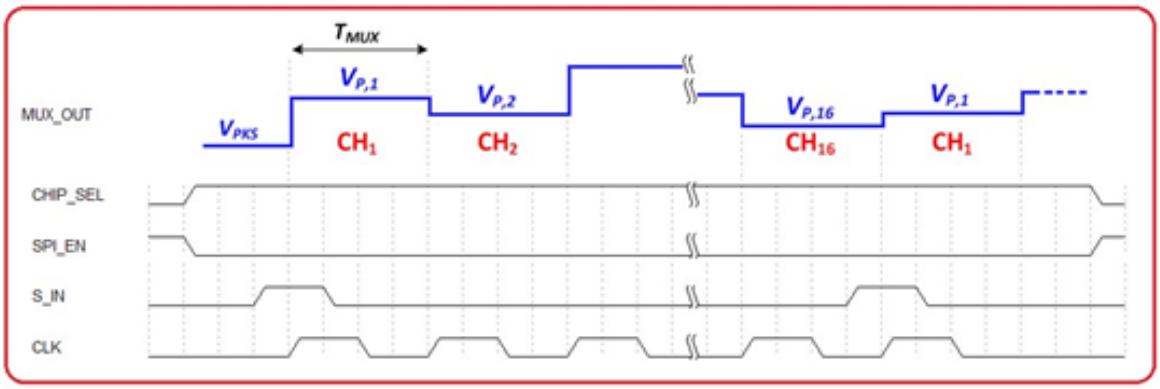

Figure 2.18 *Polling-X readout control signals.*

The polling-X SFERA MUX digital logic comprises a shift register (SR) in which a logic 1 is right-shifted on each rising edge of a clock signal (CLK) provided by the acquisition. The S_IN signal, also generated by the external DAQ, is provided to the MUX shift-register input after a number of clock pulses equal to the number of channels being multiplexed and is sampled on the CLK rising edge, so has to load a new logic 1 in such SR, thus giving rise to a new readout sequence.

2.3.5 Polling γ

The polling-γ multiplexing protocol is intended for the use of SFERA in γ-ray spectroscopy and imaging applications, where several detection modules, made of solid-state detectors coupled to monolithic crystal scintillators, need to be readout by multiple ASICs. This operational mode also exploits a sequential readout of all the ASIC 16 channels, that this time is instead synchronous to the event detection. When a γ-ray

photon is absorbed by the crystal, the visible light emitted is spread with a certain distribution over the detection units, thus all the electronic readout channels have to be processed to properly reconstruct the γ-ray photon energy. The first SA among all the channels of all the ICs employed in the system detects a valid event, which means its output overcomes a voltage threshold typically set slightly above the 500 mV baseline in order to record small amplitude signals as well, will generate a TR_OUT_LT pulse. A summary of the waveforms digital patterns involved in the polling-γ 16:1 multiplexing protocol is shown in Figure 2.19

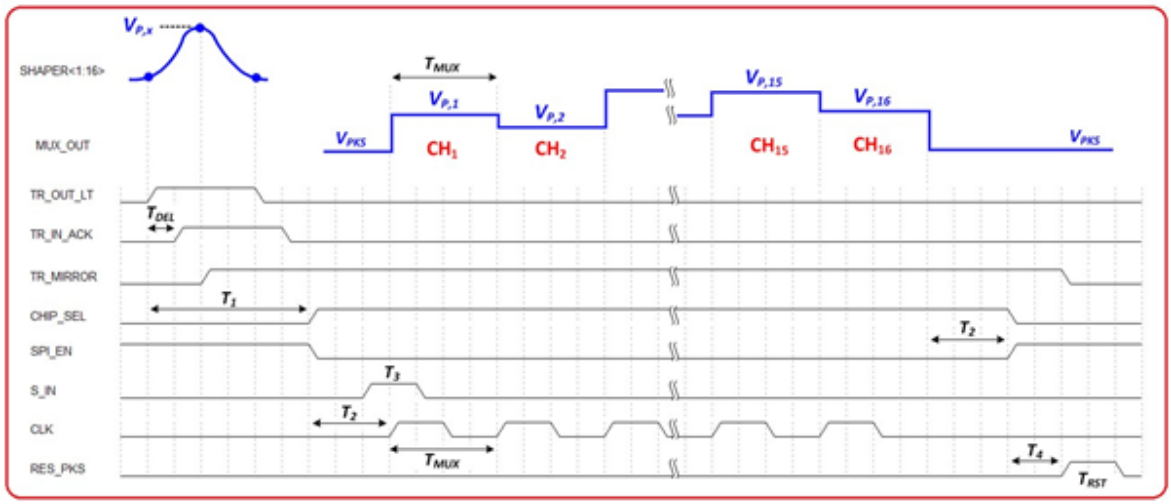

Figure 2.19 *Polling-γ readout control signals*

The DAQ has th role to communicate a signal called TR_IN_ACK, time-shifted by T_{DEL} from TR_OUT_LT, to the IC that has to be readout. At first, the peak-stretchers are now allowed to switch from write to read, thus after the semi-Gaussian pulse rising time they will have reasonably held the SA peak-amplitudes, giving rise to the TR_MIRROR signal (the logic OR of the single channels TR_MIRROR), which remains to 1 until a reset pulse RES_PKS is provided at the end of the acquisition. S_IN and CLK signals accomplish the same operation as for the polling-X multiplexing, with the only difference that a single train of clock pulses (16, 8 or 4 depending on the MUX mode) is provided for each detected event.

2.3.6 Sparse Readout

The sparse readout mode has been implemented to accomplish the requirements of the SIDDHARTA project, in which only those channels detecting an event need to be output multiplexed. In this operational mode, once a photon hits the detector, the

arrival timestamp is communicated to the data acquisition system by the TR_OUT_LT. On the rising edge of the TR_OUT_LT trigger, the instantaneous values of all the 16 LT signals are clocked in the first free position of a 16-bit first-in-first-out (FIFO) memory, thus storing the one-hot-encoded address of the channel that generated such TR_OUT_LT. The use of a FIFO multi-bit register accomplishes a dual purpose: implementing the sparsification of events by simultaneously providing the channel address both to the external DAQ and to the analog MUX (using it as selection line), thus ensuring the synchronism with the associated analog output value. The second function is managing high-rate event bursts. In case of close-intime photon detections on different channels, as shown for instance in the timing diagram of Figure 2.20, each PKS holds an analog peak while the addresses are sequentially stored in the FIFO and shifted-out at a lower speed, allowing the DAQ to properly digitize the related MUX outputs one after the other. The latter operation occurs indeed at a specific request from the DAQ by means of the TR_IN_ACK signal, which triggers a right-bit shift of the elements.

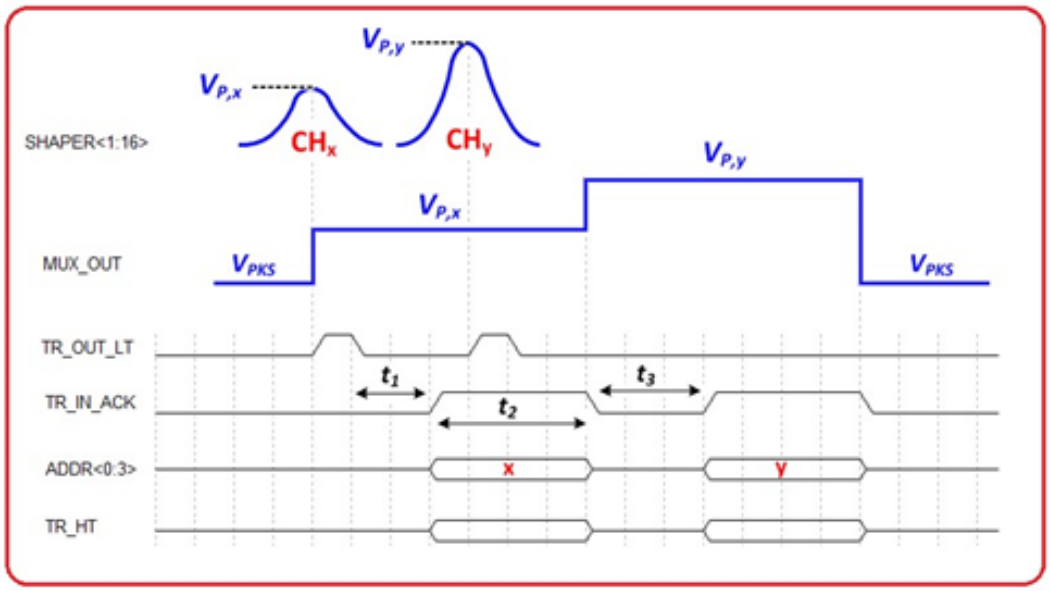

Figure 2.20 *Sparse readout control signals*

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2.4 Modification on SFERA II

2.4.1 LT width

the last ASIC prototype, the LT duration is programmable from 24ns to 267ns. In our modifications it was possibile to obtain an LT with a width of 14.8ns without damaging the correct functioning of the ASIC. It has also been studied the possibility to go lower than 14.8 ns, but some physical limits in the used technology has been encountered. For instance as shown in the Figure 2.21 the FIFO block is composed of 16 blocks, so for the input data, itakes around 10ns to pass all the cells and reaches to the last FIFO block. This 10ns of delay can be increased to 14ns of delay based upon process and mismatch studies which we have made and so, accordingly it was not possibile to generate LT signals that would have a width below this physical limitation.

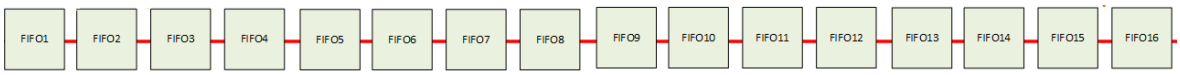

Figure 2.21 *Blocks of FIFO_16*

When an event happens, and so an LT is generated, it is necessary to read the amplitude of the PKS, and then reset it. Therefore, is important to introduce other important signals called TRASP, and ACK_INT, in particular the FIFO16_TRASP control signals are controlled by LT and ACK_INT. The TRASP_16 signal is useful to make all the 16 blocks trasparent, so that the signal can pass all the blocks. Each LT signals change the status of one TRASP (we have 16 TRASP because we have 16 cells). Each ACK_INT will generate one shift of the data to right by managing TRASP signals accordingly. The ACK_INT pulse width is controlled by a monostable that is programmable by changing Vbias like LT signal. In the Figure below 2.22, the strategy of the FIFO16 is summarized.

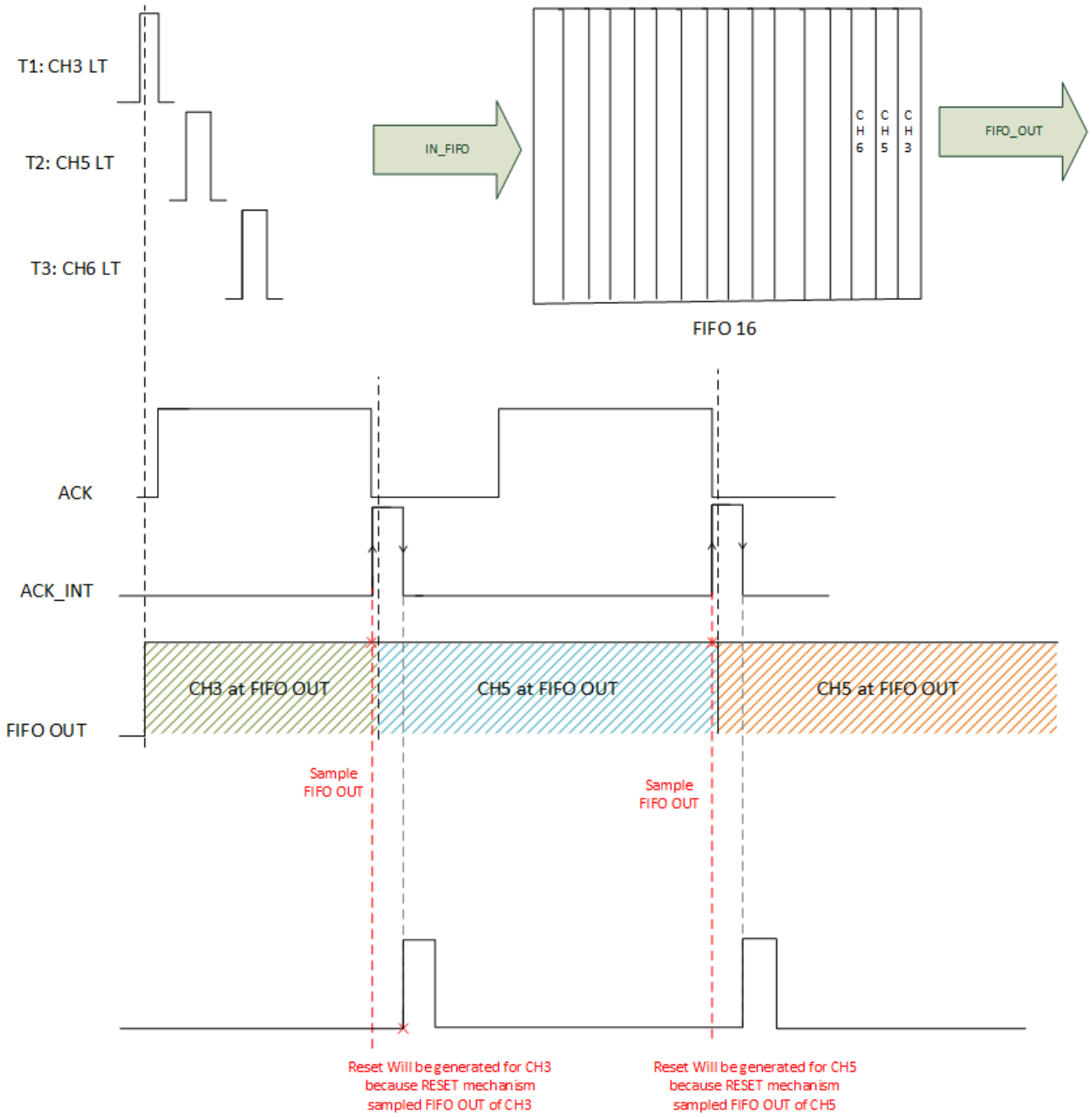

Figure 2.22 *Strategy of FIFO_16*

As shown in the Figure above, 3 events provide 3 different LTs with a different timing: T1, T2, T3.

- During T1, related to CH3, TRASP 15 (the TRASP signal associated to the block 15) is on, therefore all the blocks except the last one will be trasparent and the

signal associated to CH3 will be transferred to the last block and latched to the output.

- During T2, related to CH5, TRASP 14 (the TRASP signal associated to the block 14) is on, therefore all the blocks except the last two will be trasparent and the signal associated to CH5 will be transferred to the one before last and will be latched.
- During T3, related to CH5, TRASP 13 (the TRASP signal associated to the block 14) is on, therefore all the blocks except the last three will be trasparent and the signal associated to CH6 will be transferred to the third from last and will be latched.

2.4.2 Inhibit strategy

In Sfera II, the comparator for identifying the saturated events (HT comparator) was placed at the end of first stage of shaper (Real Cell), as shown in Figure 2.23.

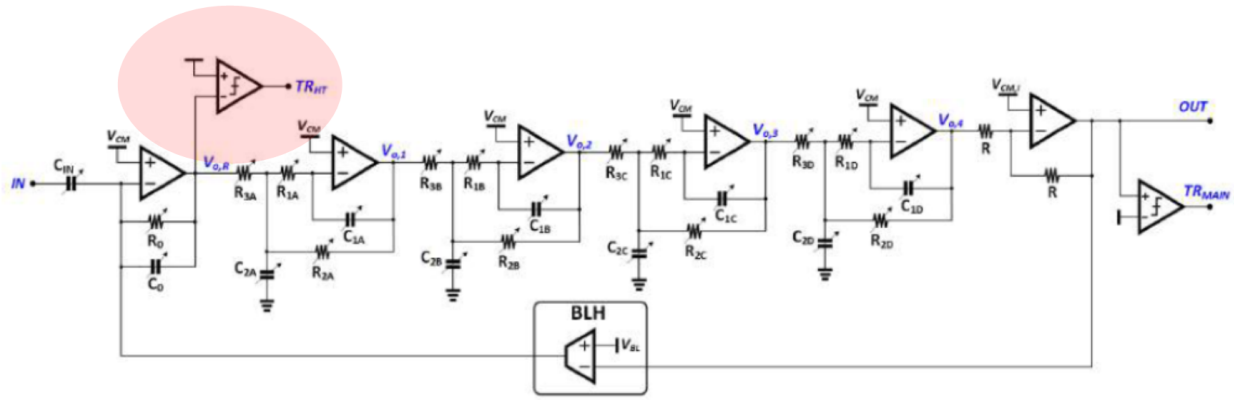

Figure 2.23 *Sfera II HT Comparator*

The first modification in Sfera III, is to place it at the end of shaper as shown in Figure 2.24. The reason to realize this modification is to make the shaper less sensitive to the ballistic deficit.

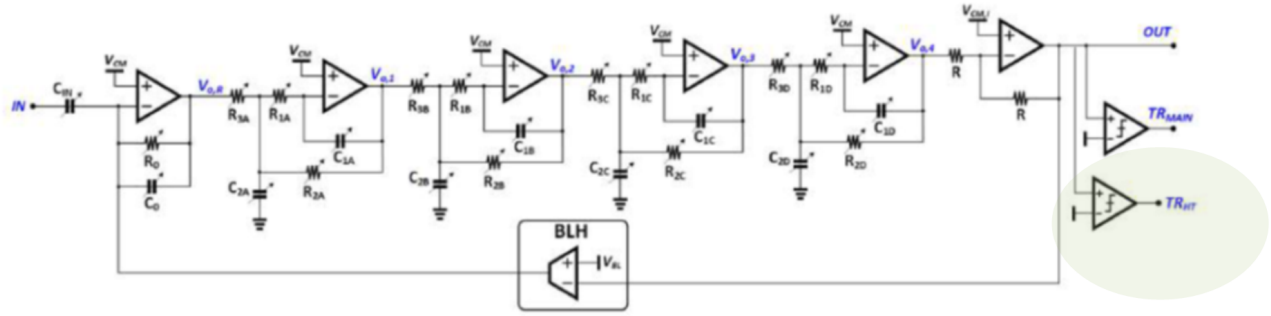

Figure 2.24 *Sfera III HT Comparator*

Regarding the inhibit three modalities are taken into consideration:

- **Global HT inhibit**: present also in SFERA II, that is, when a saturating event happens and triggers HT comparator, all 16 channels will be inhibited for a certain amount of time.
- **Local HT inhibit**: when a saturating event happens and triggers HT comparator, only that channel will be inhibited.
- **No HT inhibit**: when a saturating event happens, the system behaves with it like a normal signal and nothing will be inhibited.

2.4.2.1 Global HT Inhibit

When an HT happens in one channel, LT will be generated. Regarding the HT to be more precise we generate a signal called HT_INT that stays high for a time set by a monostable. This HT_INT triggers three important signals: TO_DEV (Switch Inhibit), TO_BLH (BLH inhibit), TO_PKS (PKS inhibit)

- TO_DEV signal is useful to inhibit the input switch as we can see in Figure 2.25. Its duration is programmable independently, and can go from 1.4us to 27.7us. It can be greater or smaller than TO_BLH, but is always smaller than TO_PKS.

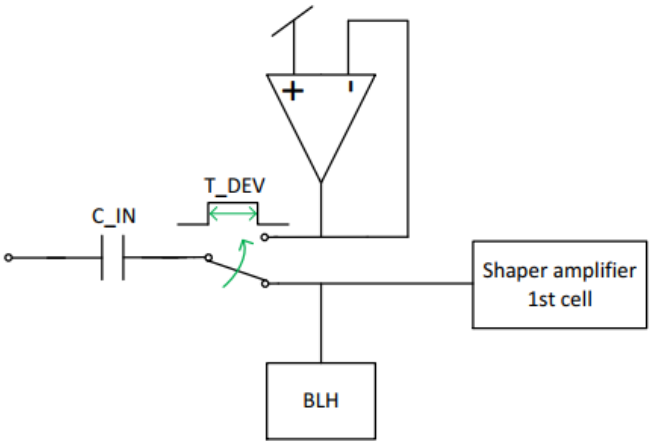

Figure 2.25 *TO_DEV signal*

- TO_BLH signal is useful to inhibit the baseline holder. Its duration is programmable independently, and can go from 720ns to 124.3us. It can be greater or smaller than TO_DEV, but is almost always smaller than TO_PKS.
- TO_PKS signal is useful to inhibit the peak stretcher. Its duration is programmable independently, and can go from 2.2us to 124.2us. It is almost always greater than TO_DEV and TO_BLH.

When an HT event happens in one channel, the output of the multiplexer shows REF_PKS at the output. In SFERA II is present a bug related to the width of the TO_PKS. Considering the case that in the same channel are present a saturated event and a good event, if the TO_PKS signal finishes before the second event, one extra LT is introduced, that should be correspondent to the good event, but is not possible to read its amplitude correctly, not only for that event, but also for the other events that arrive in that channel, as shown in the simulation in Figure 2.26.

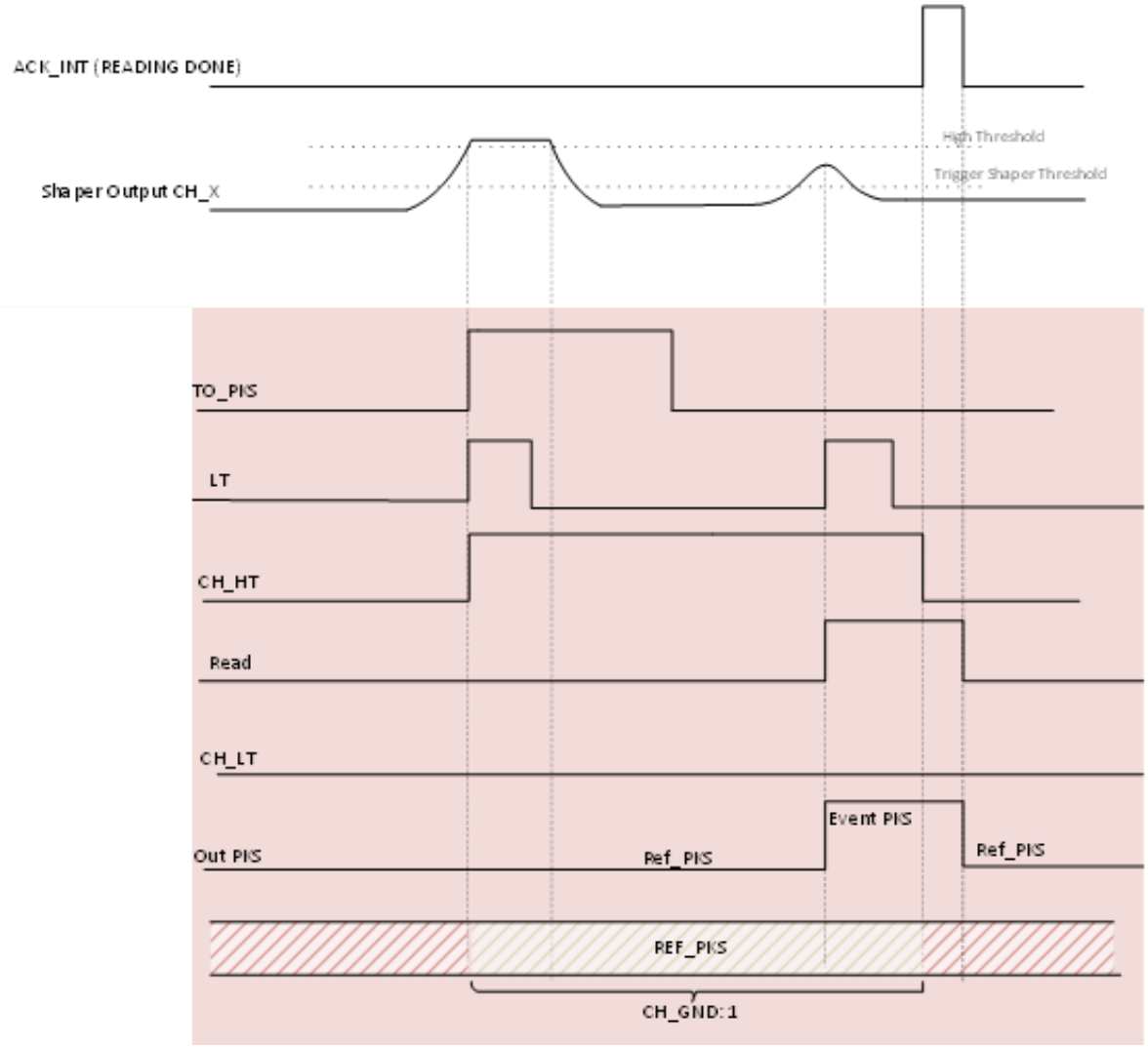

Figure 2.26 *Sfera II Bug*

To prevent this bug to happen, it is necessary to prevent PKS to go to the READ mode and consequently preventing LT from generation. The proposal is to add a simple Flip Flop, latching TR_REAL and as a result, increasing the reset of PKS duration. In this way until the CLR signal of FlipFlop is generated (on the falling edge of TR_REAL), the PKS is not able to go to the Read mode and so it doesn't produce any spurious LT signal, until the channel reading is complete. With this strategy is important to face also another condition: if in one channel is present an HT event, and in another channel there is a good event, if the TO_PKS finishes after the generation of the good event, as shown in Figure 2.27 that event is lost.

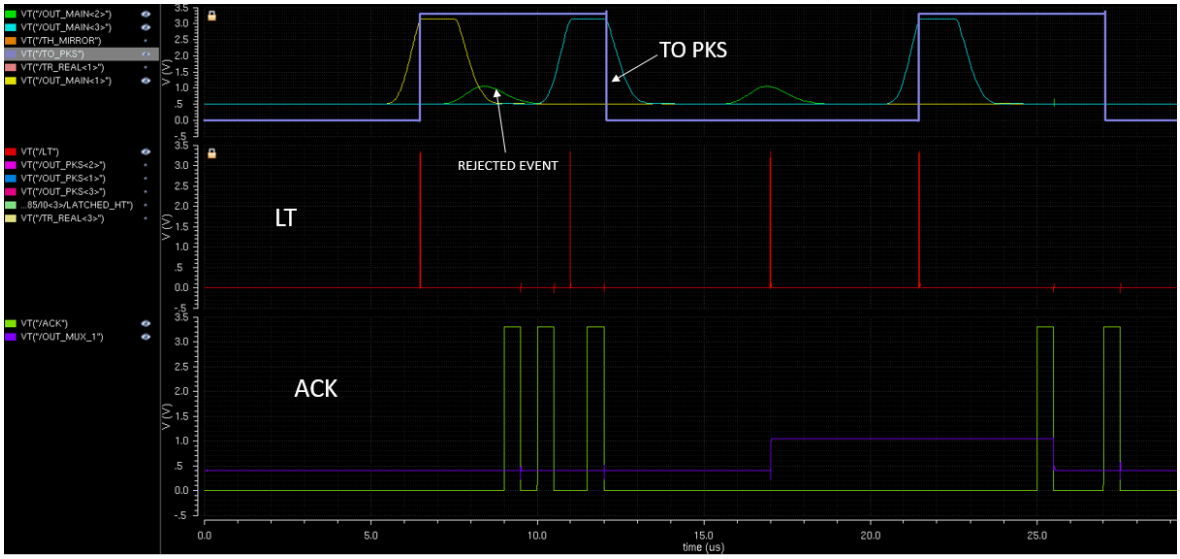

Figure 2.27 *Working principle of Global Inhibit*

In order solve this issue of losing good events on another channel, we need to introduce Local inhibit option.

2.4.2.2 Local HT inhibit

In this new inhibit strategy, the idea is to only inhibit one channel, when an HT trigger happens the TO_PKS signal or any other GLOBAL inhibition signals for other channels are not produced. In Sfera II when a high threshold event happens in one channel, CH_HT will be generated and due to the presence of the OR of CH_HT of all 16 channels the inhibiting signals will be generated. In Sfera III, instead at first step the generation of CH_HT_16 is prevented with a control bit (254) that enable or disable the global inhibit, allowing us to use the local inhibit strategy. it has also been implemented the Local inhibit in each channel by simply adding the Flip Flop locally to the reset mechanism of PKS. So, if CH_HT in one channel happens, the PKS of that channel stays inhibited until its reading has been done (by generation of CLR signal of the Flip Flop). At the meantime, other channels can normally continue their functionality. Regarding simulation shown in Figure 2.28, is important to notice that, using the same signals present in 2.27, is present also the LT referred to the good event, due to the fact that now the TO_PKS signal, used in the global inhibit, is not generated.

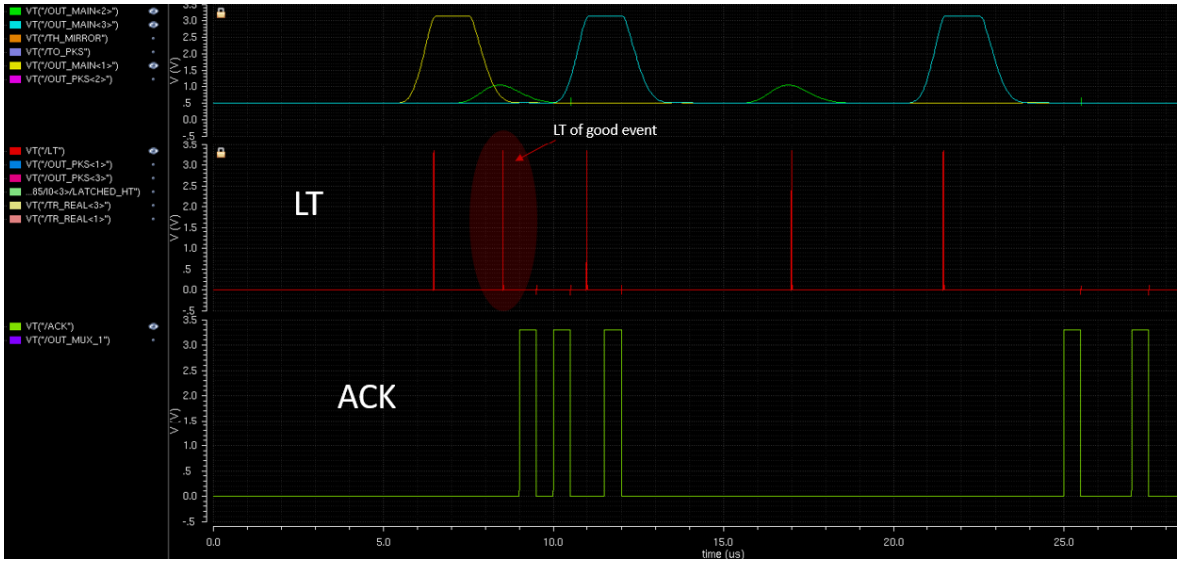

Figure 2.28 *Working principle of Local Inhibit*

2.4.2.3 NO inhibit

It has also been implemented the case of NO INHIBIT and so, no HT generation. The SPI control bit is 251 and it should be always 1, to have the inhibit signal. In this case, how said before, the system behaves like a normal signal and nothing will be inhibited. All the events (saturated and good) are considered as good events, and so also the output of the multiplexer shows us a very high value for the saturated events, instead of REF_PKS as shown in Figure 2.29

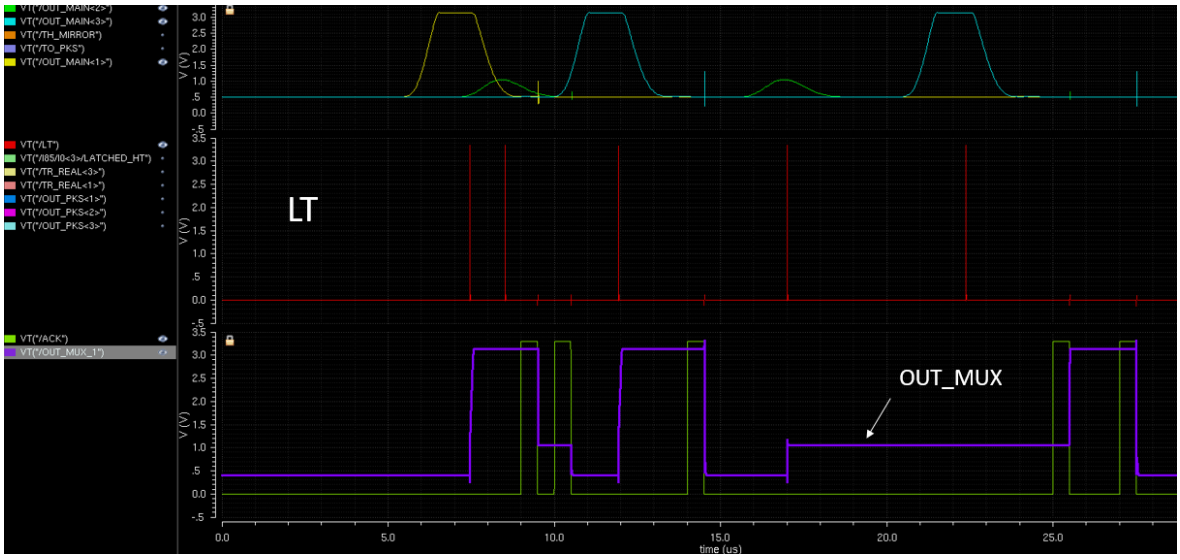

Figure 2.29 *Working principle of NO Inhibit*

2.4.3 Peak Stretcher throubleshooting

Analizing the circuit of PKS in Figure 2.11 in SFERA II focusing on Vmirrorit was discovered a weird behaviour of the current mirror.

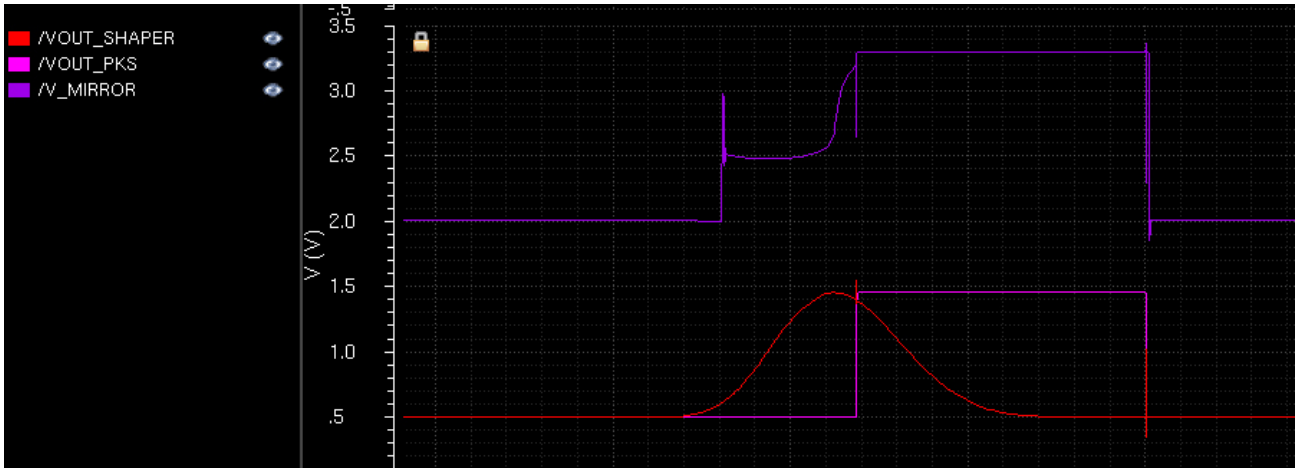

Figure 2.30 *Overshoot of the PKS present in SFERA II*

In Figure 2.30 it is possible to notice the weird shape of the voltage of the gate of the current mirror transistors. This earlier peak is synchronous with the LT trigger and may overcome the threeshold of the comparator that generates the LT. If that would be the case it may happen to have anticipated trigger timings whenever the anticipated peak is too high. This problem arise in SFERA II, this is why we made another release of the SFERA chip where this problem is solved. To solve that problem, we have to analyze the Gloop of the PKS circuit, during the transition of the write phase, when we have:

- WR switches CLOSE
- RD switches OPEN
- TRK switches OPEN

$$Gloop = GM_{ota} \cdot \frac{1}{sCh} \cdot \frac{1}{K} \tag{2.7}$$

Where Ch is the hold capacitor of PKS, K is the mirroring factor, and GM_{ota} is the transconductance of the OTA. To solve this problem is necessary to make the circuit more stable, and so the Gloop must be reduced. So to increase the stability is possible either increase Ch, increase k, or reduce GM_{ota}. This modification was made

by increasing k. In the following Figure 2.31 is possible to see the simulation result after the modification

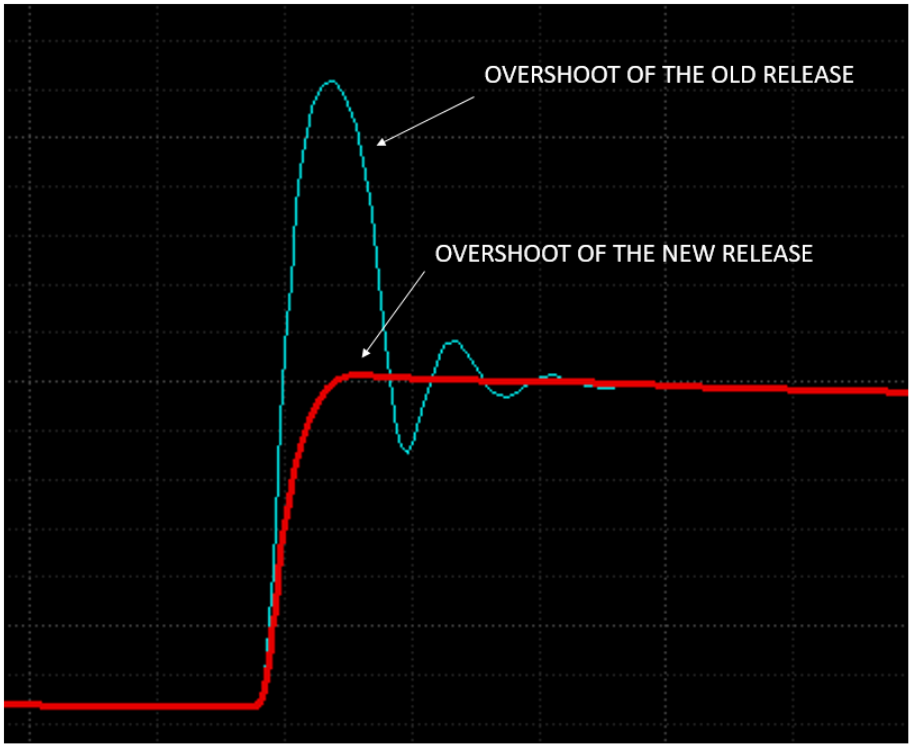

Figure 2.31 *Overshoot in Vmirror solved*

2.4.4 KILL Bug

In Sfera II, there was a bug in the comparators. This problem is that, when the kill (KILL=0), is enabled there is a short circuit between the VDD and V_REF_P. The latter should be instead always equal to 2.443 V. In this new version, it was introduced a nmos in such a way that, when the KILL=0, the pmos is close, but the nmos is open, so the short between the V_REF_P and VDD is avoided as shown in Figure 2.32.

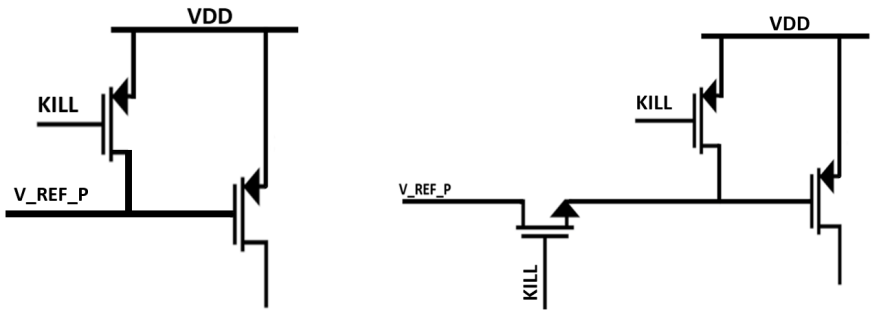

Figure 2.32 *SFERA II Kill Bug (left), SFERA III Kill Bug solved (right)*

In the Figure 2.33 is possible to see that, killing the Ch3, despite there are 2 inputs with different amplitude, the ouput of the PKS shows us the REF_PKS, so the channel was killed correctly.

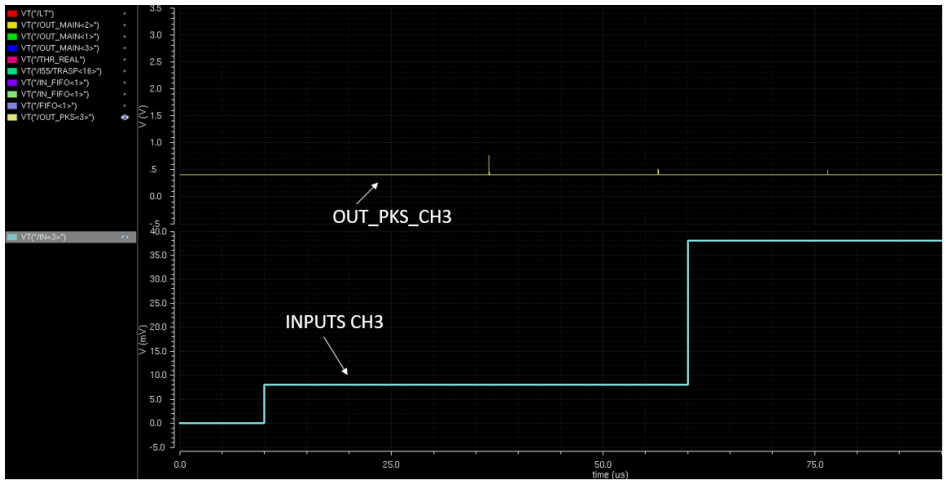

Figure 2.33 *KILL bug solved*

Chapter 3

Setup and Detector Characterization

This chapter focuses on the characterization of the SDD arrays that are needed for the final SIDDHARTA experiment. First the mechanical characteristics of the detector modules is described, then the testing setup is shown. Afterwards the results of tests on detectors are presented.

The final experiment will require 384 SDDs, arranged in arrays with 8 SDDs each, so 48 arrays are needed and these detectors have to be characterized. The characterization process aims to qualify that the detectors are properly functioning and that they fullfill the requirements for the experiment. This qualification is made by 3 set of measurements:

- detectors leakage currents at room temperature
- detectors leakage currents at -30 °C (253 °K)
- spectroscopy with Fe55 source at -30 °C (253 °K)

After the characterization process the array is then packed in a shipment box and remains sealed until the experiment installation.

3.1 SDD structure

A single array is made by many parts: the silicon layer, which comprehends 8 identical Silicon Drift Detectors, a ceramic holder which is responsible for the various electrical connections and that provides a footing surface for the silicon and the CUBE preamplifiers, then an alluminium support which connects the ceramic either to the test setup or to the cylinder of the final experiment.

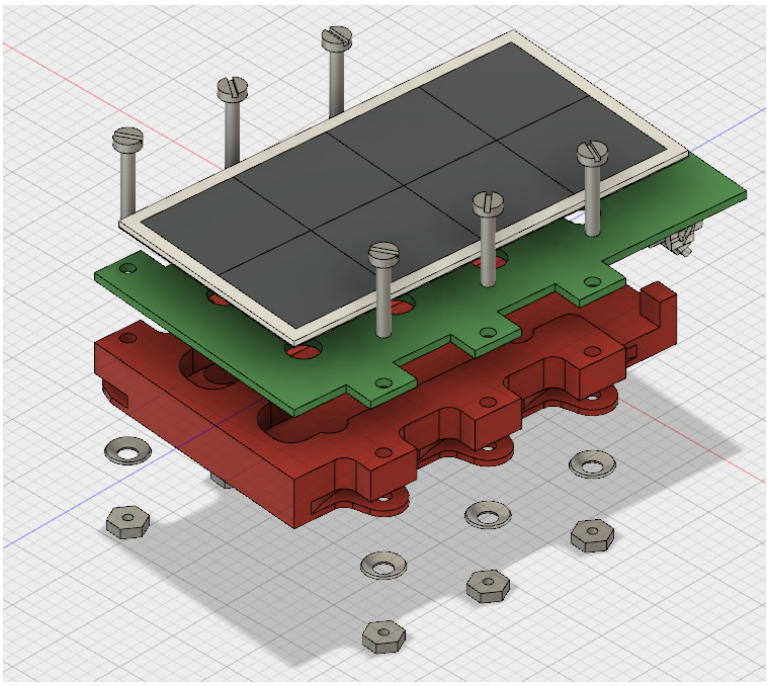

Figure 3.1 *Detector components. The top part is the silicon with 8 SDD cells , the green part is the ceramic and the brown is the alluminium piece. Ceramic and alluminium are connected togheter with 6 titanium screws*

The silicon layer is a matrix of 8 SDDs displaced in two rows by four columns. Each cell has its anode pad in the center and two pads for first ring voltage close to the anode. Ground and last ring pads are available all around the array on the anode side. The opposite side is the so called back, this is the entrance window for the radiation. The ceramic is glued to the silicon via kapton^{TM} film : a bihadesive material which acts as electrical insulator, and remains stable across a wide range of temperatures (4 - 673 °K), moreover it has a good thermal conductivity, which enables easy cooling of the detector. The ceramic has, besides all the various tracks for the different supplies, 8 holes to access the anode side of the silicon, as we can see in Figure 3.2.

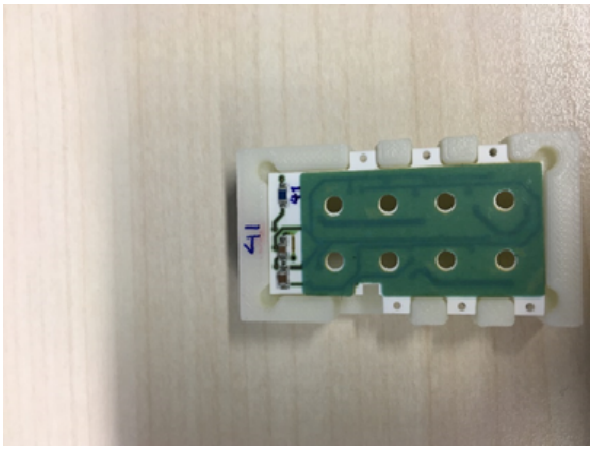

Figure 3.2 *Detector with the bihadesive attached*

Then the detectors are stored and transported in some specific boxes called Gel-Pak Vacuum Release (VR). The vacuum release trays consist of a thin, flexible Gel membrane, which is placed over a mesh material. The Gel holds the device securely in place until it is released "on demand" by applying vacuum to the underside of the tray. The device orientation does not change even during release. Applying a vacuum under the tray causes the Gel membrane to conform to the shape of the mesh, which significantly reduces the surface contact area between the Gel and the device. This temporarily minimizes the Gel holding force for easy device removal. Devices can be removed with a vacuum pick-up tool once the tray is in the release mode. The hold/release mechanism is reversible and the tray returns to its original holding mode when the vacuum is removed. All the setup is shown in Figure 3.3

Figure 3.3 *Cross-Sectional view illustrating vacuum release technology (left), vacuum pump (right)*

Now we have to remove the top side from the tape of ceramic, and then place the ceramic on the detector so that they attach, as shown in Figure 3.4.

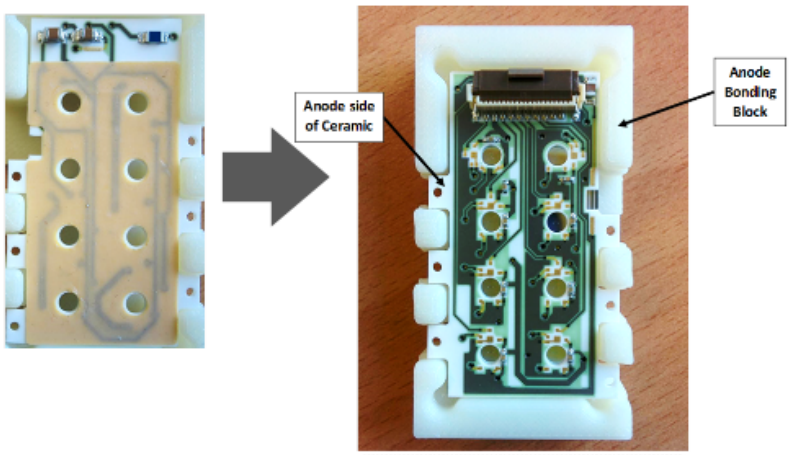

Figure 3.4 *Ceramic onto the SDD array present in the anode bonding block*

When the bonding is done, you should check it by the microscope to make sure it is done correctly. After back bonding has been also done, now the detector is ready to be attached to the aluminium block. The latter is linked to the ceramic with six titanium bolts, this component is made to allow a mechanical adaptation between the ceramic and the outer structure and acts as a more reliable base to manipulate the detector unit, showed in Figure 3.5

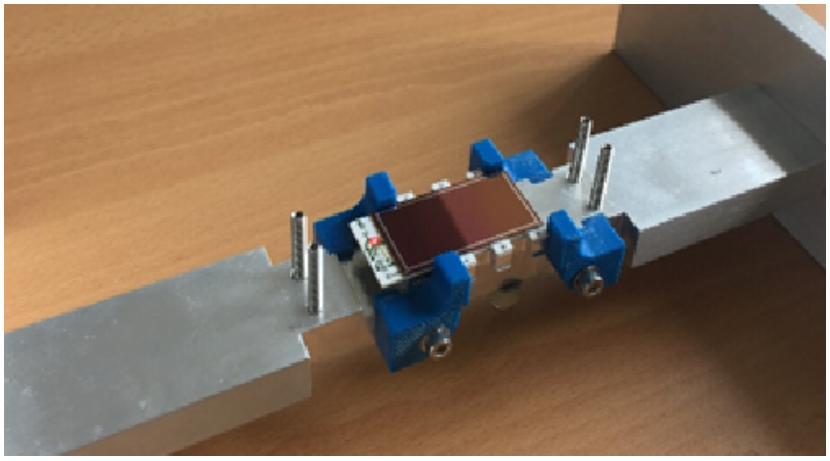

Figure 3.5 *strategy to attach the alluminium block*

In Figure 3.6 we summarize all the important steps.

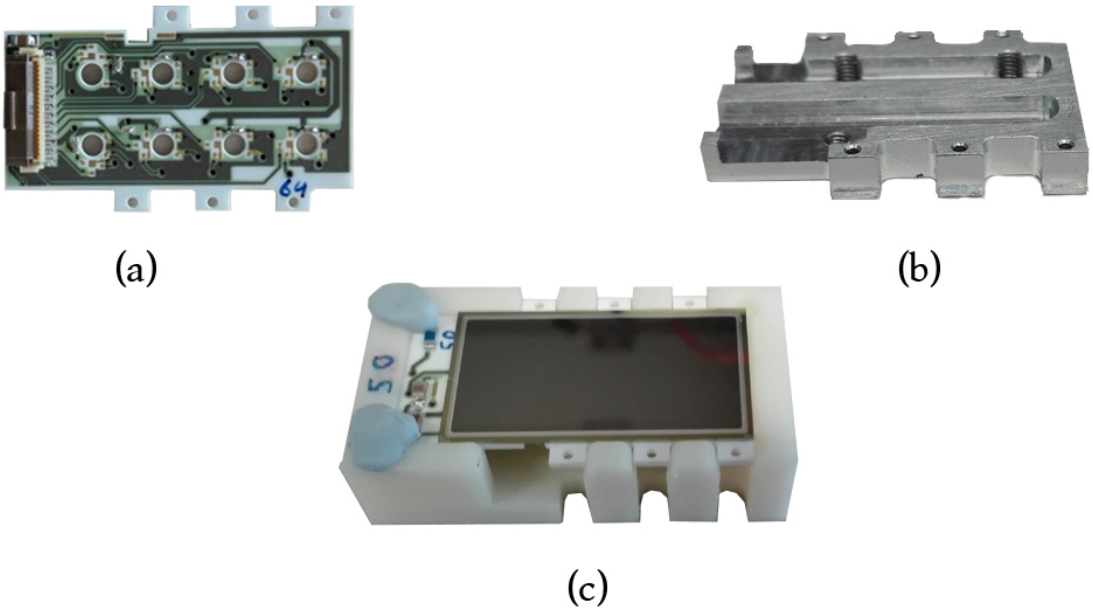

Figure 3.6 *Detector components:* ***(a)*** *ceramic which wires all the SDD and cube's pad to the cable's connector (on the left);* ***(b)*** *alluminium holder, this component holds the ceramic and makes a better base to manipulate the array;* ***(c)*** *back side of the SDD.*

Finally we have the detector assembled and ready for the characterization test.

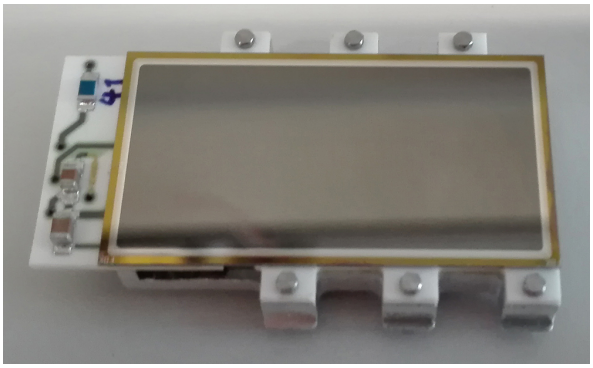

Figure 3.7 *Detector assembled*

3.2 Experimental setup

This setup needs to provide a proper environment for a correct measurements of the quality for the detector units. The experimental set-up developed to characterize SFERA and the detectors, can be split into two main sections, the first made of detectors and front-end electronics and the second one comprising the data acquisition system based on National InstrumentsTM (NI) hardware, as pictured by the block diagram of Fig.4.1. with an ADC board and a FPGA module that: acquires the data from the front-end and provides the control signals for the chip.

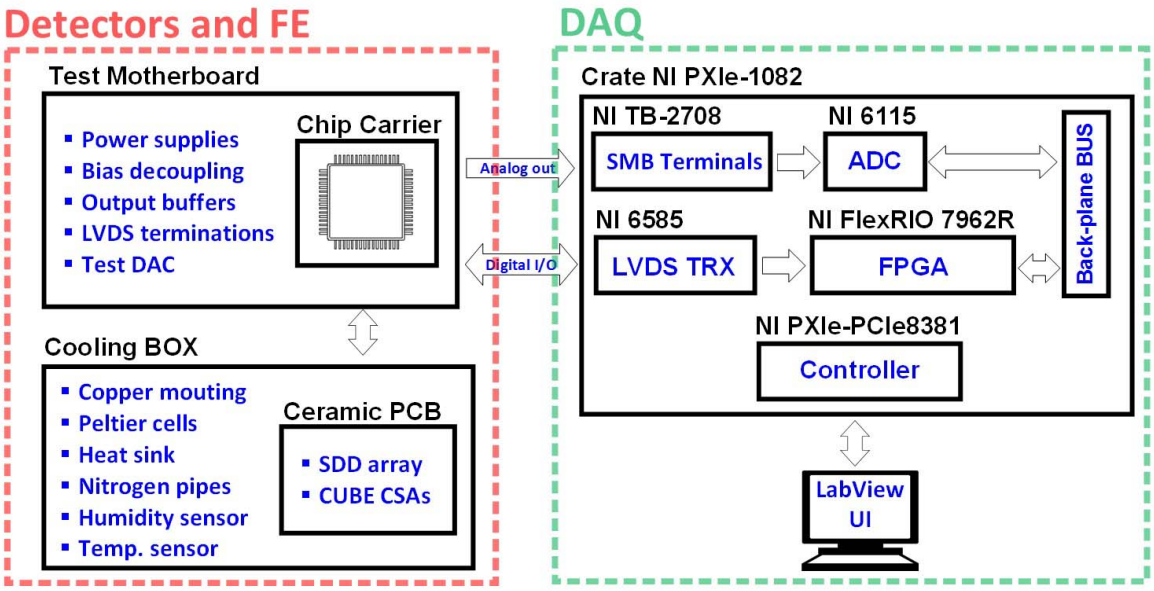

Figure 3.8 *Block diagram of the complete acquisition system comprising detectors, front-end and back-end electronics.*

3.2.1 Cooling box

The experimental characterization has been carried out cooling the silicon drift detectors with a Peltier-based custom set-up (referred to as the cooling box) whose general architecture is shown in Figure 3.9.

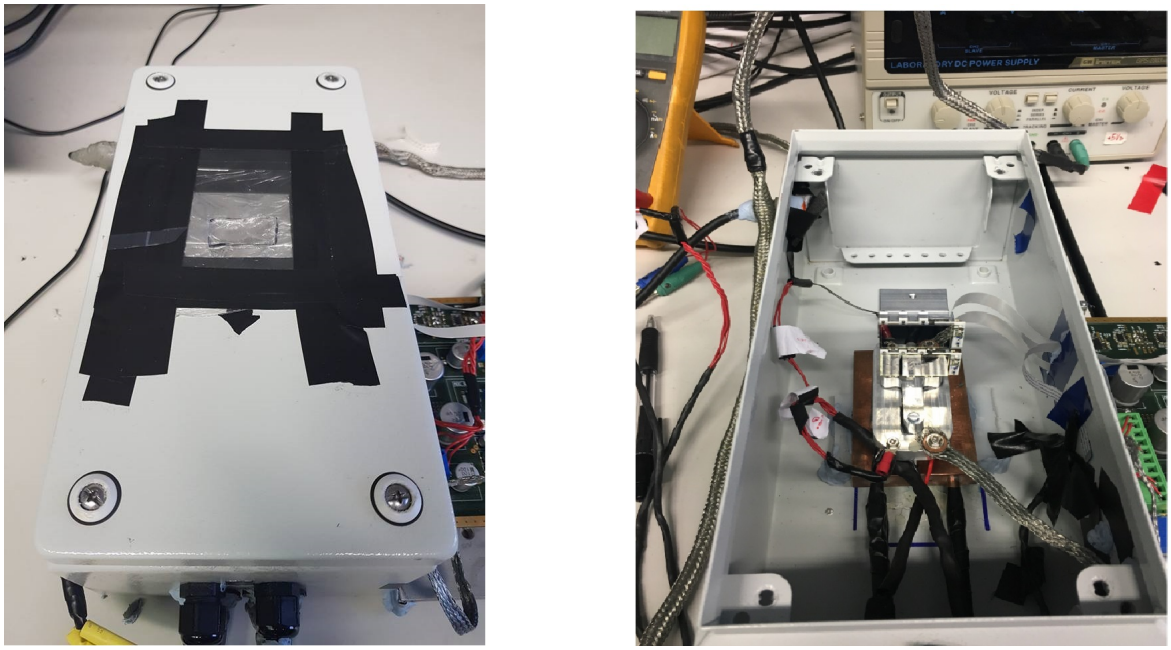

Figure 3.9 *Box used for the characterization test (left). Inner part of the box where we mount the detectors (right)*

This box keeps the main structure that holds the detectors, a stacked tower composed by: a copper thermostat which is kept at 10 °C by water cooling, a peltier module which allows the cooling to -30°C, an aluminium block that holds two pt100 thermoresistors for temperature monitoring and keeps the detectors in the correct position to receive the radiation from the calibrating source. The box presents various cables and connectors. On the front panel there are: the tubes for water cooling, the cables for the two pt100, the supply for the peltier module and the cables for a humidity sensor. On the side panels there are the flat cables that links the detectors to the readout electronic and the tube for nitrogen pumping. CUBE CSAs are placed in close proximity to the detectors to minimize the bond-wire length thus the anode stray capacitance. The ceramic PCB carrier also ensures good thermal conductivity (180 W/(m°K)) with the copper frame below on which it is stuck. The latter is placed on the top of a Peltier-stage that allows to cool the SDDs down to -40 °C to reduce the leakage current ENC contribution, provided a proper heat dissipation by the copper cold plate below (water heat sink).

3.2.2 Peltier

The Peltier has two sides, and when a DC electric current flows through the device, it transfer heat from one side to the other, so that one side gets cooler while the other gets hotter, as shown in Figure 3.10. The "hot" side is attached to a heat sink so that it remains at a fixed temperature, while the cool side goes below fixed temperature.

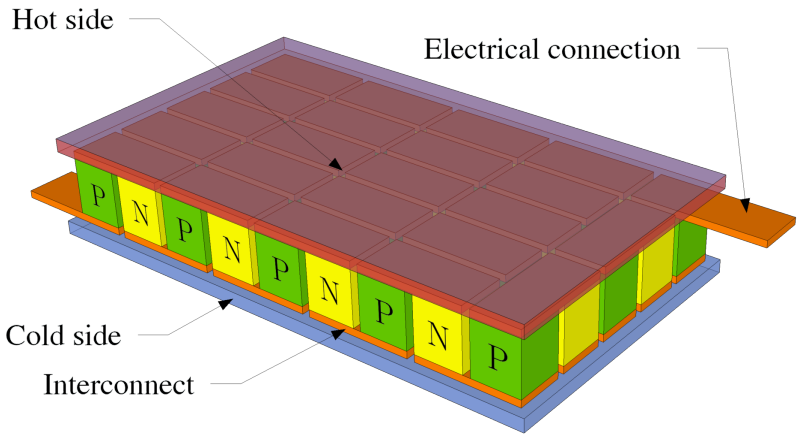

Figure 3.10 *Peltier Structure*

In order to decrease the temperature of SDD by means of Peltier in our setup, we increase the current little by little so that it increases the difference between two plates of Peltier.

3.2.3 Front-end electronics

The front-end electronics basically comprises two custom evaluation boards of standard FR4 material, depicted in Figure 3.11. A first one, namely the motherboard, incorporates output buffers for SFERA analog multiplexed. It takes care of holding the connectors for the external world: power supply lines, cables for NI FPGA and ADC, many lemo connectors to check different chip outputs on the oscilloscope. This board also has different trimmers to fine regulate R1, RN and back voltage to obtain the optimal biasing for the detectrs. Regarding the chip carrier showed in Figure 3.11 (right), is mounted on the top of the main board through two 32-pin connectors that provides all the supplies and the control signals to both the chip and the detectors. We can see the presence of two connectors for the flat cables (one for each detector) and a lemo connector to pulse a single channel to test the chip. There are also 16 switches that control the signal of each SDD channel, they are useful to monitor channel by channel during the characterization procedure.

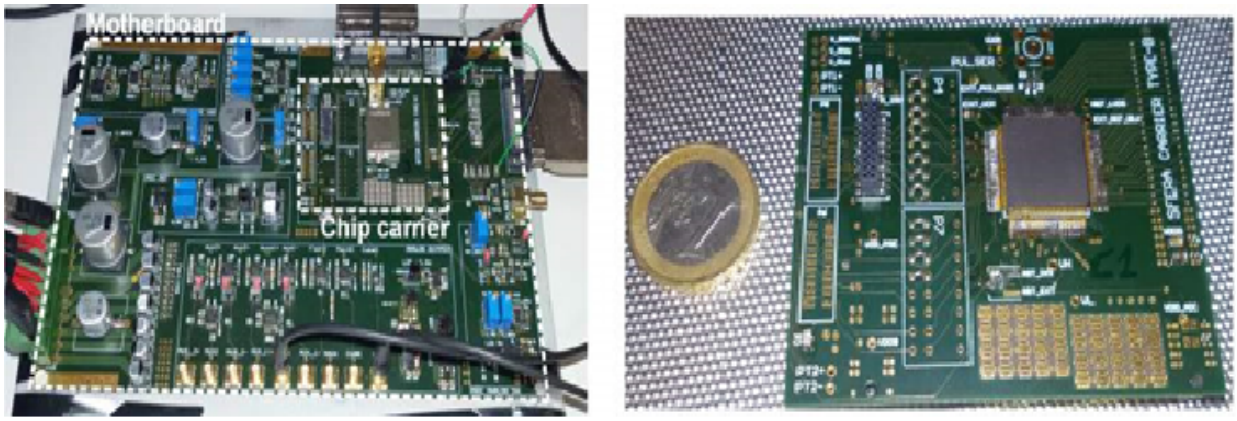

Figure 3.11 *MainBoard (left), SFERA carrier (right).*

3.2.4 NI crate and PC

The data acquisition system is based on commercial NI-PXIe 1082 showed in Figure 3.12 equipped with the ADC module and the FPGA module. ADC module (NI-6115), provides for each of its 4 channels a 12 bit SAR with 10Mspls rate. This ADC has been chosen because for its excellent thermal stability. This module reads the data from the output of the MUX of SFERA, samples it and stores in an internal memory, which then will be read from the PC. The other component is the FPGA module (NI FlexRIO 7962R). This part is responsible to give the correct signals to SFERA during the testing phase. The last part of the test setup chain is the PC. With the NI software LabVIEW it is possible to commands the FPGA which sends control signals to the chip. Different acquisition protocols are available for this ASIC and for each of them a proper LabVIEW program has to be developed. Depending on which protocol the measurements need to be done the chip has to be correcly programmed, then the PC software has to deliver to the FPGA the correct sequence of inputs for a proper data acquisition. The data are saved in txt files, ready to be processed with MATLAB.

Figure 3.12 *National Instrument PXIe-1082. This box is equipped with an FPGA (middle connector) and an ADC (rigthmost connector) module. The left connector is the link with the PC.*

3.3 Characterization of SDD

As described in paragraph 3.1, the qualification of the detectors is made by many steps that are well defined in Figure 3.13. The first part concerns the assembly of the detector: the silicon chip sent by FBK is glued on the ceramic through the Kapton adhesive. Then CUBEs are soldered on the ceramic and all the connection between detector, ceramic and preamplifier are done. After this step an optical inspection is done on every array to check for errors or defects concerning the mounting. If an error regarding bonding or CUBE is encountered it is possible to fix it by mounting other CUBEs or doing another connection. The detector is then mounted on the alluminium. It is possible then to proceed with the eletrical tests and the x-ray spectroscopy.

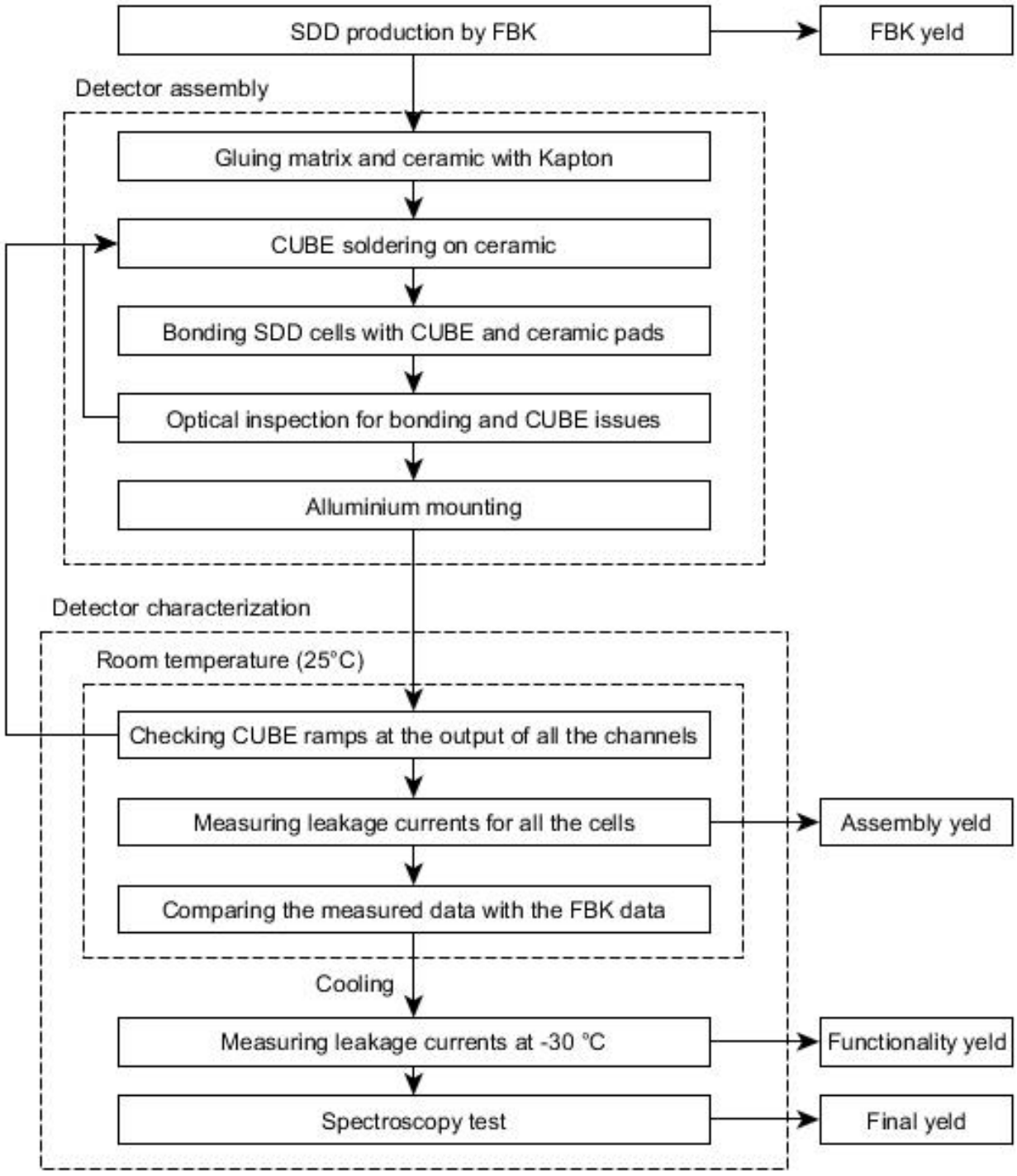

Figure 3.13 *Characterization diagram.*

3.3.1 Measurements at Room Temperature

When the alluminium is mounted, the detectors must be tested, at the beginning at room temperature (25°C). The leakage current is associated to the thermal electron-hole generation, this effect creates carriers also in a depleted region and, since those carriers experience an electrical field, they will be pushed to either, one of the rings (holes) or the anode pad (electrons). Those carriers contribute to a current which, due to its statistical fluctuation, superimposes a noise contribution on the signal of interest. This current depends on few parameters like: the area of the device (usually the thermal generation is computed as a density since depends on the concentration of atoms) and the temperature. Moreover, since the carrier are accumulated on the preamplifier capacitor, the final noise value will depend on the shaping time (greater shaping time leads to greater leakage current noise), for this fact a low value for the leakage current is needed. At the beginning the test is done without any source and by having the box that blocks the entry of light, in such a way that the detector doesn't pick up any photons, corrupting the measurements. In this way the only signal integrated on the preamplifier is due to the detector leakage current. To do that measure, the output of the cube voltage signal is monitored, by using an oscilloscope. SFERA can provide the output of a single channel, so to obtain the data for all the sixteen channels, SFERA has to be programmed once for each channel, using the SPI control interface. Once the chip is programmed, we can monitor on the oscilloscope the output of the CUBE. The result is a sawtooth waveform. The ramps showed in Figure 3.14 are due to the fact that the anode provides a constant current that is integrated on the feedback capacitor.

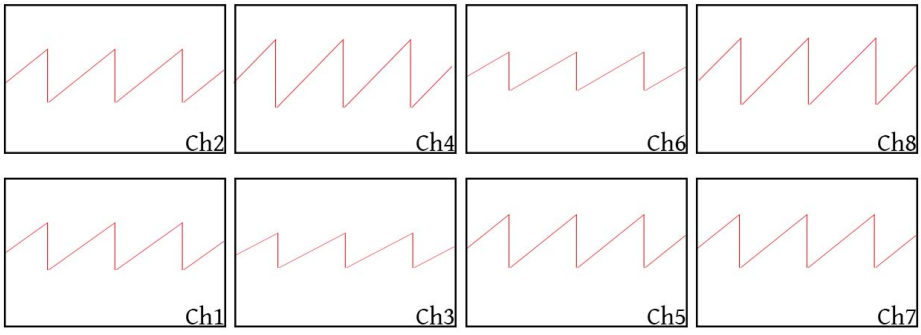

Figure 3.14 *Ramps for each channel of the detector under test. We can notice that the Channel 4 and Channel 8 show high leakage, instead in Channel 3 and Channel 6 there is low leakage*

The ramps keep on repeating, because when a CUBE saturates a digital signal is generated by a comparator, then SFERA reacts by providing a global reset to all the

cubes, this reset makes all the ramps starting over and over again in a periodic way. To evaluate the leakage current the measure is simply done by computing the derivative of the ramp. Therefore, looking to the slope and considering the fundamental relation:

$$q = C \cdot V \tag{3.1}$$

It is possible to differentiate both terms in time, and since the capacitor (C) is constant in time the result is:

$$\frac{\delta q}{\delta t} = I_{leakage} = C \cdot \frac{\delta V}{\delta t} \tag{3.2}$$

Analyzing the equation 3.2, the term $\frac{\delta V}{\delta t}$ corresponds to the slope of the ramp shown at the output of the CUBE. These measurements are necessary for a first quality evaluation of the detector. So, looking to the leakage current is possible to get informations about the status of the detector. If the values reported are too high, it is possible that some channels are damaged and then need further analysis. All the values are then reported in a file which keeps track of all the information regarding a specific array, from the silicon producer (FBK) to the final characterization evaluations.

3.3.2 Measurements at -30°C

After the measurements at room temperature, the next steps are done with detectors colled down to -30°C. To cool the detectors, two components must be used: a water chiller and a peltier module showed in Figure 3.15.

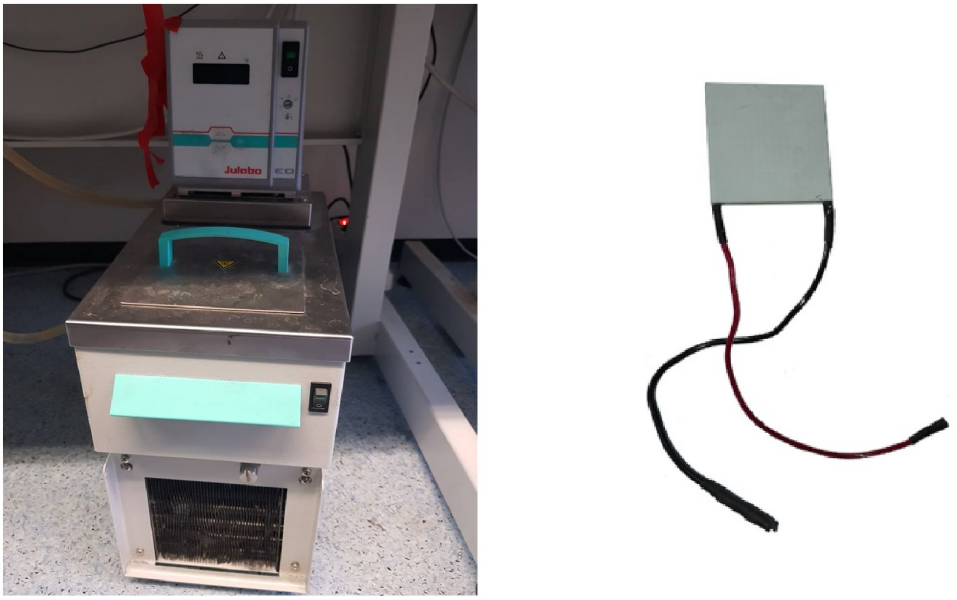

Figure 3.15 *Water chiller (left) and peltier module (right)*

It is also important to take care of the humidity inside the setup. When sealing the box there's still present the atmospheric humidity. This fact could create issues for the detector: when reducing the temperature, the water particles suspended in the box will condensate on any cold surface they encounter, even the exposed SDD back side. This process could damage certain area of the detector. Furthermore, since the water is conductive, it could create short circuits between parts of the detector. Therefore, we have to avoid all these problems. To do that is needed to reduce the humidity, this is done by pumping nitrogen, using appropriate valves, showed in Figure 3.16, inside the box.

Figure 3.16 *Nitrogen Valves*

An external nitrogen tank is available. During the measurements the flow is kept at a minimum flux to compensate the gas leakages. The humidity inside the box is measured with a capacitive sensor: the Honeywell HIH-4000-003. This sensor is supplied with 5 volts and presents an output voltage which depends on the relative humidity (RH) with the following relation:

$$V_{out} = V_{supply} \cdot 0.0062(RH) + 0.16 \tag{3.3}$$

When the humidity reaches the correct value (20%) the box is ready for cooling. When the multimeter shows a number around 1.1 V, the humidity is fine. (The recommended value in our setup is around 1V). If the humidity is too low or too high adjust the nitrogen flow. The general concept here is to not waste nitrogen and neither have high humidity in the setup. When Humidity is ok, the nitrogen pressure can be reduced to conserve nitrogen and the water circulation can be started. Both the chiller and the Peliter supply are turned on and the detectors starts to drop in temperature. Temperature is monitored by 2 pt100 thermistors screwed on the alluminium block, moreover on each detector module is present a pt100 component which can be probed on the carrier board. Once the setup is cold enough, there must always be a small amount of nitrogen flowing into the setup even if the humidity goes to low. Make sure that the nitrogen pressure from the main does not drop to zero. When the temperature reaches -30 °C it is possible to compute again the leakage current. There is an empirical

law for the leakage current. It decreases by two order of magnitude when cooling from room temperature to the test temperature. The measurements at -30 °C is done in the same way as the one done at room temperature: by programming the chip to show a desired channel, then measuring the ramp slopes on the oscilloscope and repeating this process for all the channels. For warming, we put reasonably high nitrogen flux into the setup and stop the flow only when the setup temperature is above 15 °C.

3.3.3 Measurements with ^{55}Fe at -30 °C

The last measurements are the x-ray spectroscopy characterization. These measurements analyze at the same time the sixteen channels, focusing on the spectroscopy resolution. For this purpose, 55-Fe calibration source is used: the latter provides radiation at two fixed wavelength (Kα line at 5895 eV and Kβ at 6492 eV). The aim of the spectroscopy is then to evaluate the FWHM of the main peak (Kα) from the source so, is possible to obtain the value of the noise of the system. The spectroscopy is done with an acquisition modality called SWEEP, in order to save a file for each shaping time automatically, in this way the post-processing can be done easily, to have access to various shaping time obtaining the best setting for each couple of detectors. When the acquisition for each shaping is finished, the measurement is done and the radioactive source is removed. Finally, all the data are saved in an excel file reporting the different analyses done on the detector. Each file is then provided when the different arrays are shipped for the final experiment, to always have a reference document for the specific sensor. After this last step the setup must be heated up gradually, so the nitrogen valves are closed and the setup is ready for a new measurement hosting two new detector units.

3.4 Unexpected results

During the characterization process few times some unexpected results arised from the test. The main and quickest parameter that would give a feedback about the functionality of the cells of the detectors, is the output of the CUBE preamplifier. When the detector works properly, a sawtooth waveform is expected when monitoring the preamplifier output with the oscilloscope. When a cell is not properly working, most of times it is known by the CUBE's ramps. Figure 3.17 shows the standard ramps and the problematic ones.

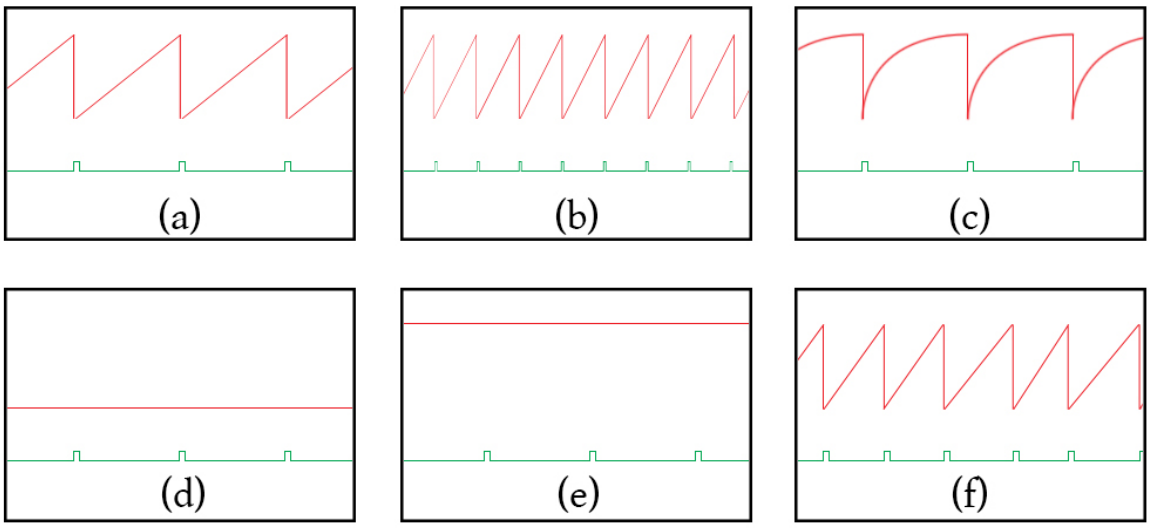

Figure 3.17 *Possible oscilloscope results. For each case the red line is the preamplifier output and the green line the reset signal for the CUBE.* ***(a)*** *standard ramps* ***(b)*** *high leakage ramps* ***(c)*** *curved ramps* ***(d)*** *preamplifier fixed to ground* ***(e)*** *preamplifier fixed to supply* ***(f)*** *jittering ramps*

All the different behaviours (and the action taken after seeing them) are described below:

- **standard ramps:** those are seen when a SDD and corresponding CUBE are working correctly. Since everything is properly working, the characterization continues normally.
- **steep ramps:** those show a channel with high leakage current, this may lead to a worsening in resolution performances, but doesn't imply a damage or a not working cell. So during the test this channel will be monitored with more attention, trying to understand if that channel affects the performance of the others.
- **curved ramps:** those highlight an problem related to the CUBE. If it is possible another preamplifier has to be mounted above the existing one and bound again with the SDD. This procedure could damage the nearby cells, so it's not always executable.
- **constant voltage:** it is possible that either ground or CUBE supply voltage were seen on the oscilloscope, in this case the problem could again be the preamplifier, it must be pursued the same procedure as the one with curved ramps.

- **jittering:** this happened only a couple of times, here the ramps vary their slope quite frequently (the slope is a bit different for each ramp), test proceed as normal with higher focus on this channel, it may not work.

Another surprising effect that happened during the characterization measurement was a malfunction of a line of SDD cells for five detectors. During the testing it was noticed that for channels 2-4-6-8 the CUBE didn't gave any ramp. Due to this peculiar symmetry and to the fact that such an high number of cell was damaged, further inspection was done on those detectors.

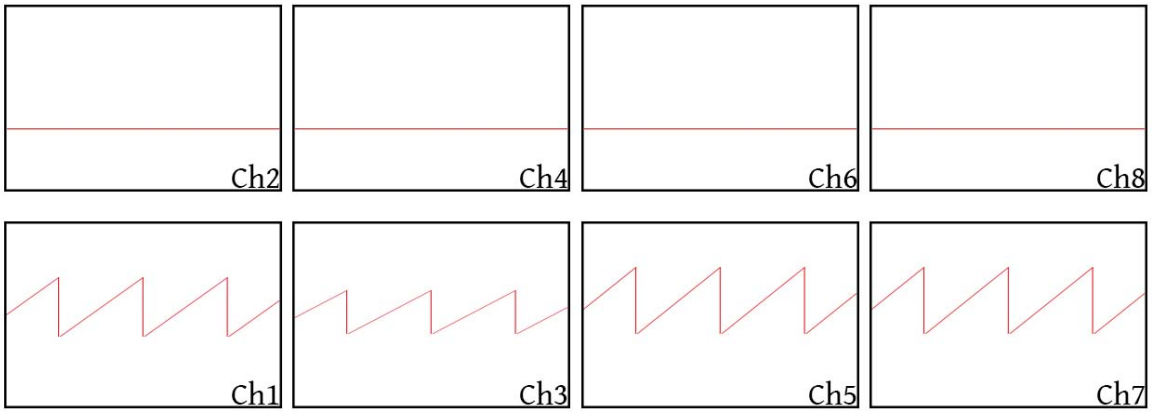

Figure 3.18 *Peculiar behaviour for some detectors: one line is not active for the leakage test.*

The cause for any problem can be many, the main components that make an array are: SDD cells, CUBE preamplifiers, ceramic and a damage can be on any of these components. For instance, Figure 3.19 highlights a type of bonding issue.

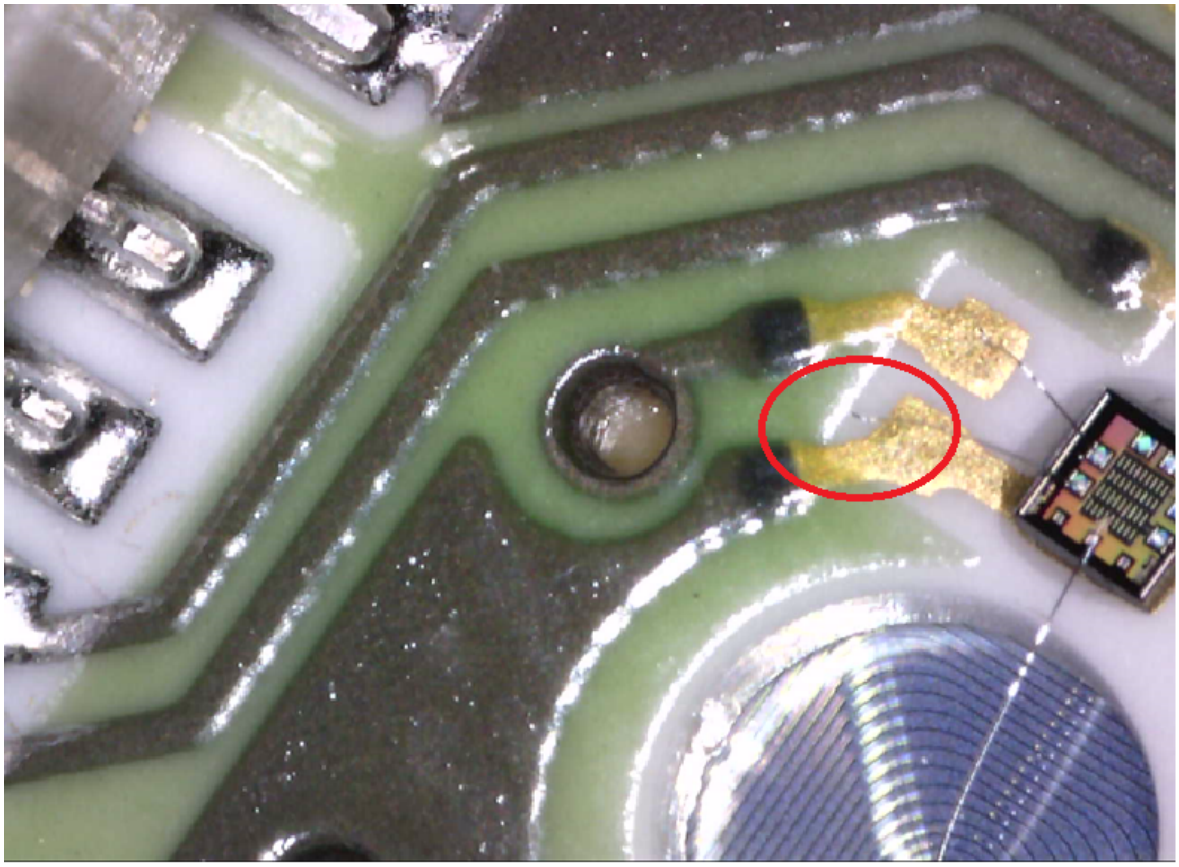

Figure 3.19 *Bonding not connected to Ground PAD*

Chapter 4

DAQ implementation and Crosstalk analysis

In this chapter, first the development of the DAQ is presented. Then an extensive study regarding the crosstalk is shown. Finally results and conclusion will be shown.

4.1 DAQ code

4.1.1 SPI control interface

A the beginning, the ASIC must be programmed with all the settings mentioned in chapter 2 (multiplexing modes, protocols, comparator thresholds, voltage, current references, filter gains and peaking times, etc..), that are stored in an internal memory whose block diagram is presented in Figure 4.1, and are properly programmed by means of a custom serial-protocol-interface (SPI) communication. This digital logic block comprises three main sections:

- the input shift-register, made of 256 master-slave flip-flops in series, in which the binary word is clocked during the chip programming phase by means of the external signals S_IN and CLK.
- a read-only-memory (ROM), which stores a default set of bits.
- a random-access-memory (RAM), on which both the incoming binary word from the SPI shift-register and the default ROM setting can be loaded.

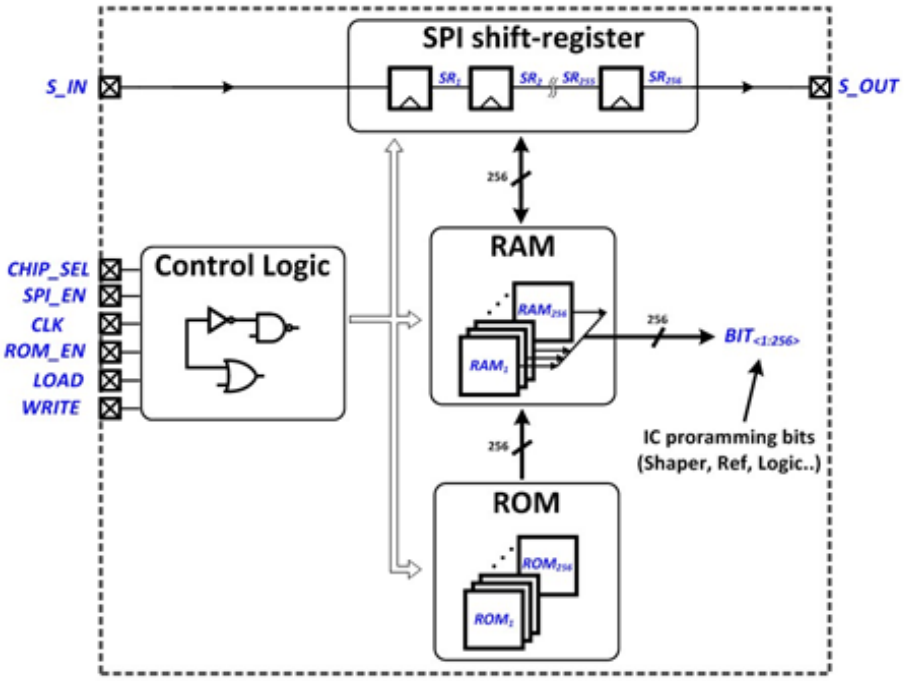

Figure 4.1 *Internal memory block diagram*

So, before starting each type of acquisition the SPI_data_generation VI, shown in Figure 4.2, must be run, where is possible, easily change the modality of acquisition, gain of the filter, peaking time, acquisition protocol, reset logic and related settings, monitored channel, thresholds for the various comparators that gives digital trigger for timing purposes and other finer settings like the tail current for the peak stretchers. according to our purpose.

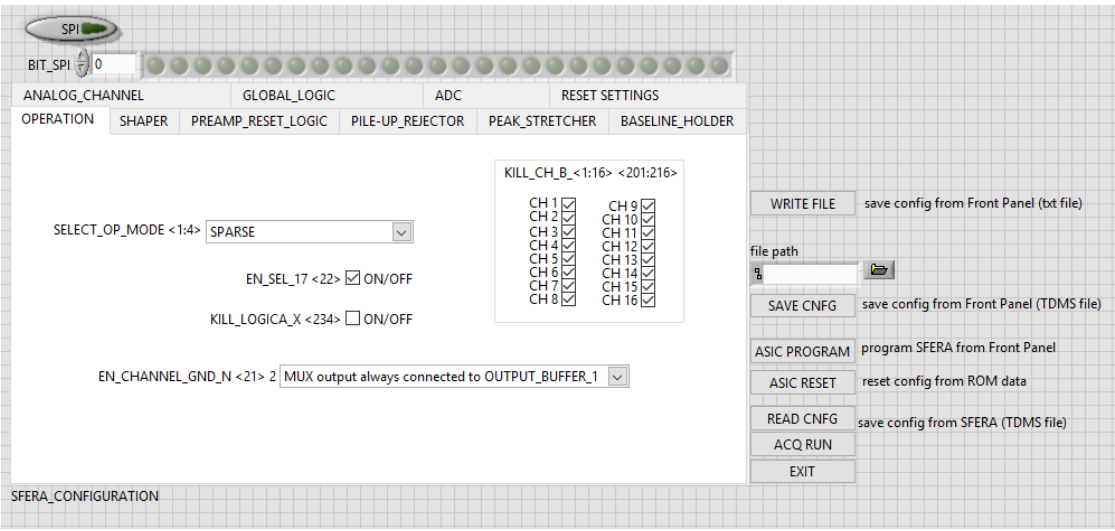

Figure 4.2 *SPI interface*

4.1.2 SPARSE implementation

After the chip has been programmed, another software is needed for the acquisition. SFERA as mentioned in chapter 2 is able to acquire in three different modalities: Polling X, Polling γ and Sparse. During my thesis, I developed the Sparse readout protocol which is the one implemented in the final experiment in Frascati. In this way it was possible to study in detail SFERA behavior in this modality, with relevant results towards its use in the experiment. A dedicated digital logic, shown in Figure 4.3, manages the data transfer to the downstream DAQ system, synchronously providing it both the "firing channels" addresses and related stretched pulse-peaks in the same time order the events are detected. In this operational mode, once a photon hits the detector, the arrival timestamp is communicated to the data acquisition system by the TR_OUT_LT signal, which is the logic OR of all the triggers coming from the channel peak-stretchers indicated with LT $< 1 : 16 >$ in Figure 4.3. On the rising edge of the TR_OUT_LT trigger, the instantaneous values of all the 16 LT signals are clocked in the first free position of a 16-bit first-in-first-out (FIFO) memory. Prior to their transfer

to the data acquisition system, the one-hot-encoded addresses are converted into a 4-bit binary format (ADDR $< 0 : 3 >$). We can see also a TR_HT trigger, which is the logic OR of the single channels TR_HT signals indicated with HT $< 1 : 16 >$

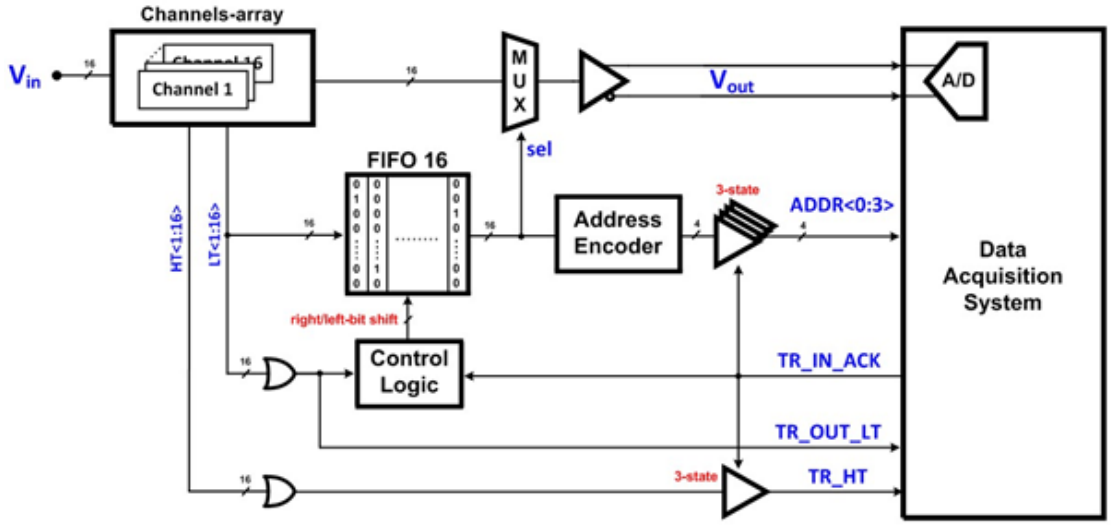

Figure 4.3 *Sparse digital logic block diagram and interface with the DAQ*

Figure 4.4 presents the main signals involved in the sparse operational mode. As soon as a CUBE output signal is given on a readout channel, the output shaped-pulse triggers the TR_OUT_LT signal, that in this case is the output of the comparator sensing the PKS current mirror. In response, the DAQ provides the TR_IN_ACK signal which enables the output multiplexer on such readout channel.

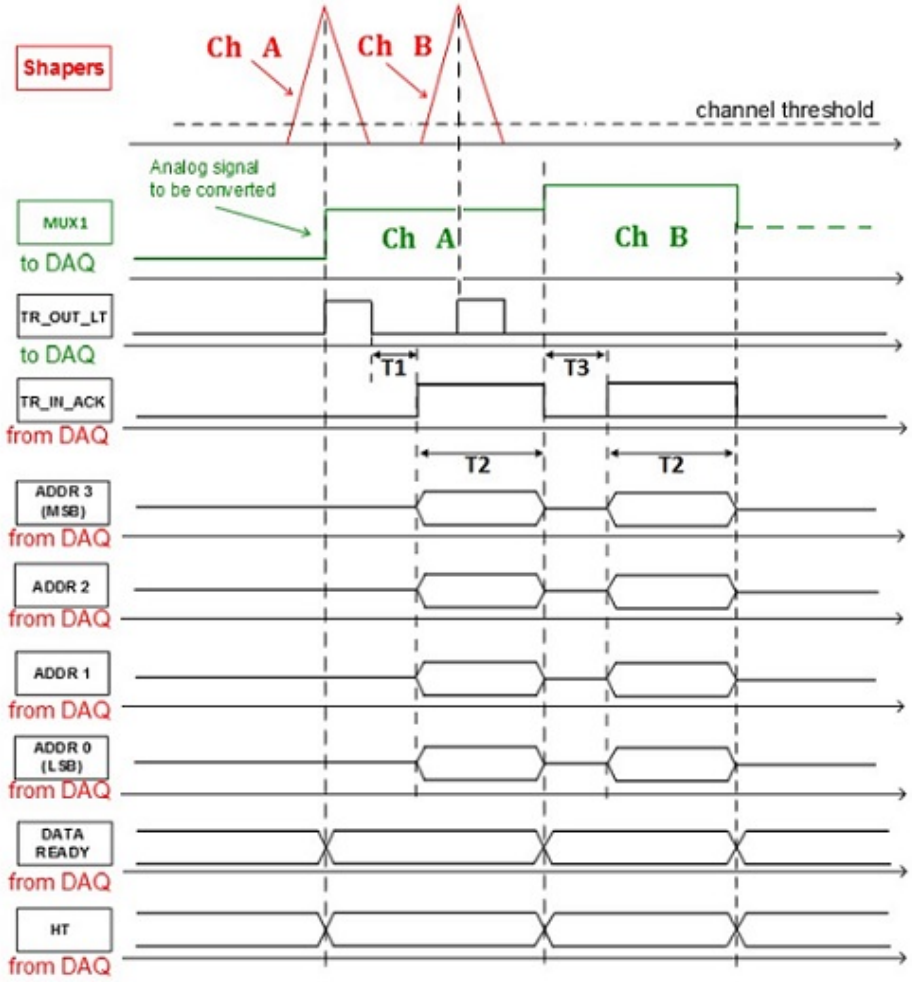

Figure 4.4 *Main signals involved in Sparse Readout*

Referring to Figure 4.4, it is of utmost importance that in Sparse Modality all the timing constraints are met:

- T1 is the distance between the first LT and the rising edge of the TR_IN_ACK related to that LT.
- T2 is the width of the TR_IN_ACK pulse.
- T3 is the distance between two TR_IN_ACK.

How said before, the data that comes from the output of the multiplexer is read on the falling edge of the TR_IN_ACK. As showed in Figure 4.4 the value of the address is available only when TR_IN_ACK is high. In my acquisition system two LabVIEW VI were used: one related to the HOST and the other one related to the FPGA, that

has to provide all the useful signals. These two VI must be connected to each other. To summarize the Sparse readout acquisition strategy, at the beginning we wait the generation of a new event, then a specific channel detects that event, and so is necessary to provide with the timing strategy already described a correct TR_IN_ACK signal. At the same time, the address of the channel that receives that event, must be provided. When the TR_IN_ACK of that event is finished we are able to read that specific channel. If the energy exceeds a certain threshold (20 / 40Kev), the HT signal is placed at a high level, and the channel that receives the HT is inhibited using the strategy described in the section 2.4.2.2 . Data remains stable until the acknowledgment pulse arrives (ACK), if there is an event waiting, the address and HT outputs are immediately updated for the second event and its response must be done with a new ACK pulse. In the FPGA program, was used a structure that can be summarizes in the block diagram showed in Figure 4.5.

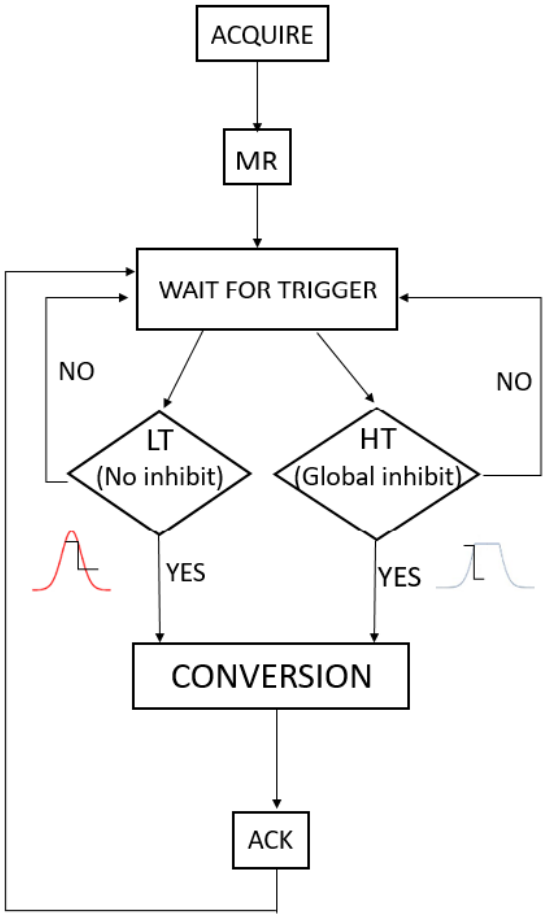

Figure 4.5 *Sparse steps during acquisition*

Once the ASIC is programmed, the acquisition must be run, pressing ACQUIRE. It is important to give a Master Reset to the chip in such a way all the Fip Flops return to their correct initial values. Therefore, now we have to wait for the generation of the event. The FPGA, when receives a good event (LT), goes in the conversion mode generating the TR_IN_ACK with a timing described above. So far, it was considered only the presence of a good event and so LT, however in most cases there is the presence of high energy events. In this case the chip provides us an HT signal (saturated event). Therefore, as already described in chapter 2, SFERA provides us the inhibit, rejecting that event. The FPGA also for HT, goes in conversion mode, generating so the TR_IN_ACK. To manage correctly all these signals, it was introduced a counter of LT, that goes up when it receives an LT, and goes down on the falling edge of the ACK.
At the end is important to save all the values of the PKS, sampled by the ADC. To do that two opportunity are considered:

- **Save each event**: in this case all the events are saved, no matter if there is an LT or HT event.
- **Save a particular event**: in this way, is possible to set a condition of saving the event, for instance there is the opportunity to save only the good events (LT) or save only the satured events (HT)

At the end a txt file will be generated, with the values of the TR_IN_ACK, HT, Drift Time, Address of the channel that receives the event and Ch_Data that comes from the ADC. The latter is drived by a clock, generated by the user using the interface of acquisition. The clock used for ADC, is created only when TR_IN_ACK is high, in this way each time the correct value is sampled, as shown in Figure 4.6.

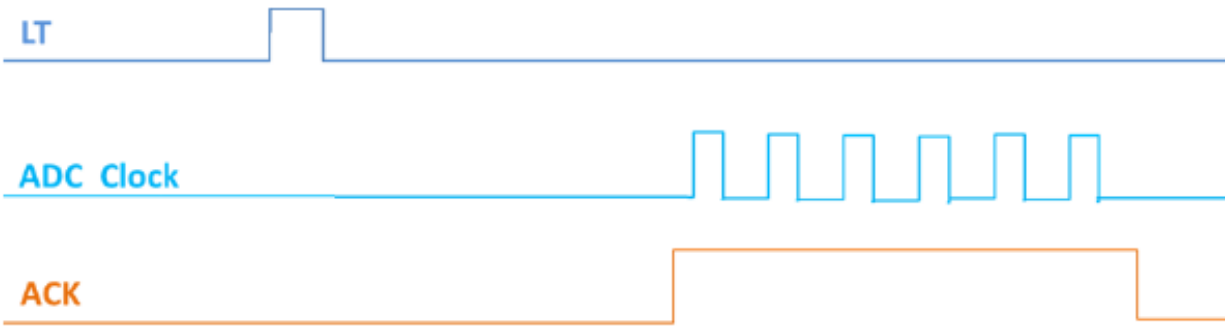

Figure 4.6 *behaviour of ADC clock*

4.1.3 Pulser Measurements

To analyze the crosstalk effect, was simulated the generation of an event using the pulser. The latter is useful to give to SFERA as input a pulse with a high energy up to 1.25MeV (3V) to simulate the generation of a MIP (Minimum ionizing particles). In this situation four cases have been analyzed:

- Inputs floating
- Inputs grounded
- Inputs connected to the 1kOhm impedance (Output impedance extimated for the preamplifier)
- Inputs connected to the CUBE(Preamplifier)

Figure 4.7 shows the results obtained on the oscilloscope, when a high energy event is sent on Channel 1, with all the other inputs floating.

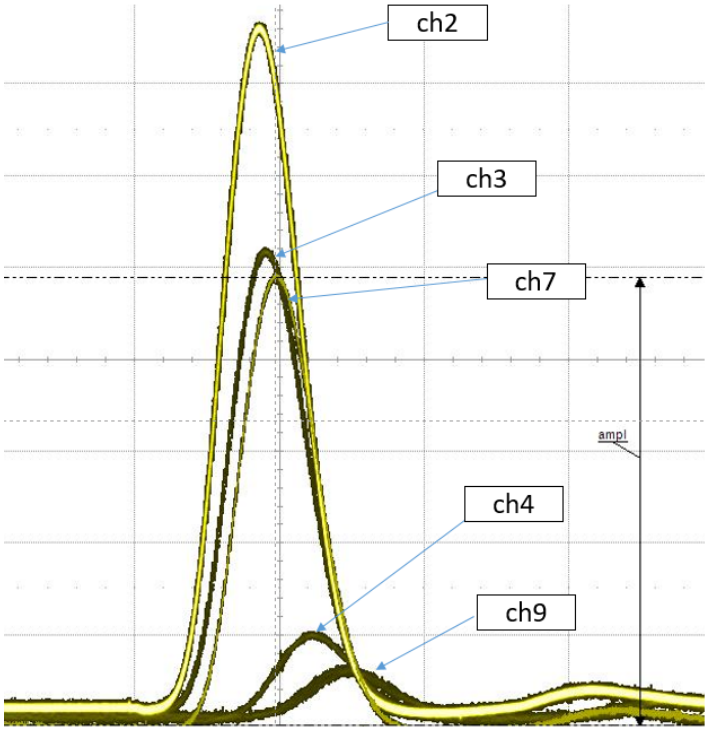

Figure 4.7 *Crosstalk in all the channels pulsing Ch1 with an high energy event (1.25Mev). Inputs FLOATING*

So when the inputs are floating, there is a very high crosstalk effect between the channels, expecially on Channel 2, that is the closest to the channel where the pulse

has been sent. This behaviour can be explained considering the capacitive coupling between the channels that are close to each other.
On the other hand, pulsing Channel 1 with an amplitude of 1.25MeV(3V) energy, connecting all the inputs to ground, no crosstalk is observed (as shown in Figure 4.8) on other channels. Is present only Baseline without any crosstalk.

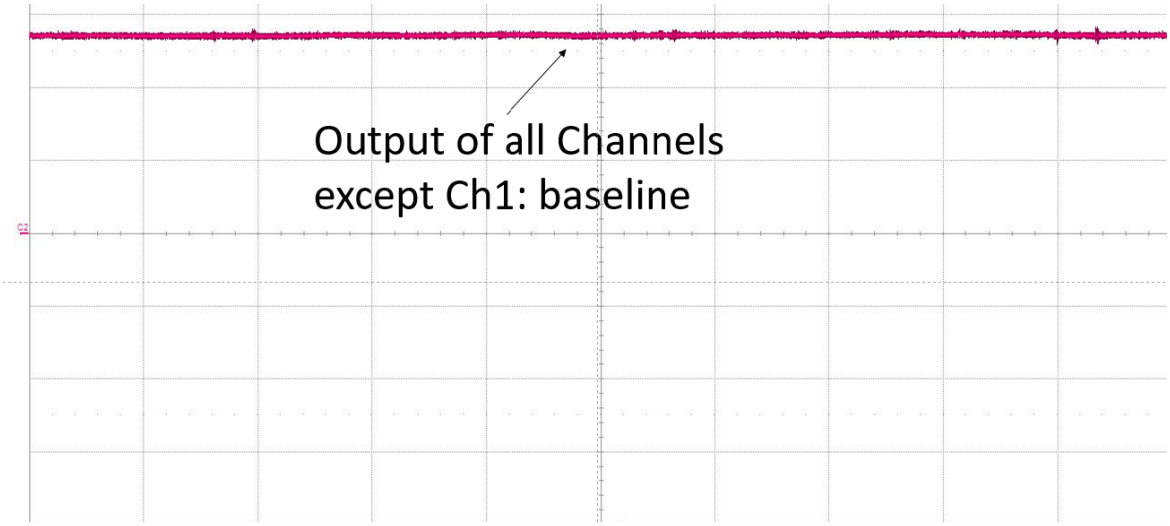

Figure 4.8 *Crosstalk in all the channels pulsing Ch1 with an high energy event (1.25Mev). Inputs GROUNDED*

By doing a more in-depth study, it was noted that, if we provide on Channel 1 a pulse with an amplitude of 1.3Mev(3.2V), as shown in Figure 4.9, with all the other inputs to ground it is possible to notice a crosstalk effect, that is more evident on Channel 2 (the closest to the one where we are sending the pulse). This crosstalk effect is due to the internal reset of the cube. In fact using a pulse with an amplitude of 3.2V, the threshold used for the internal reset is overcomed. The latter is responsible of the behaviour shown in Figure 4.9

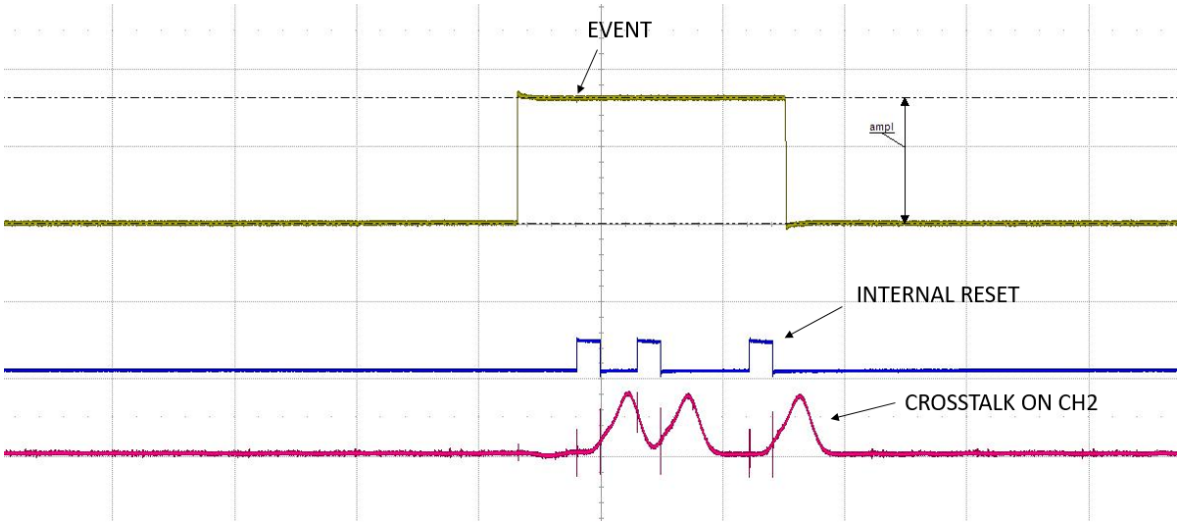

Figure 4.9 *Crosstalk in all the channels pulsing Ch1 with a high energy event (1.3Mev). Inputs GROUNDED*

The third study was the measurements with inputs connected to the 1kOhm impedance (Output impedance of the preamplifier). In this way we replace the impedence of the CUBE premaplifier using a simple resistance,in such a way that we avoid that the cables can create a kind of crosstalk. Figure 4.10 shows that the result of this measurements was the same of the measurements with all the inputs grounded.

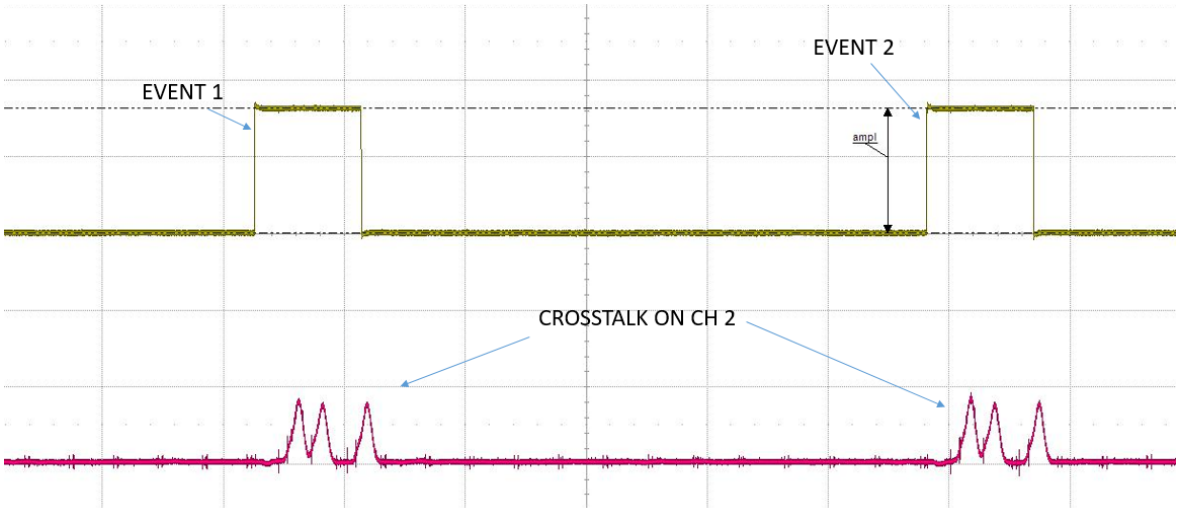

Figure 4.10 *Crosstalk on Channel 2, pulsing Ch1 with a high energy event (1.25Mev). Inputs connected to 1kOhm impedence*

The last study regarding the crosstalk, was the measurements connecting the inputs to a real detector, in this way, the inputs see the real impedence of cube. In particular

the pulser has been connected to the Channel 9, and the Detector to Ch 1:8. The result is summarized in Figure 4.11.

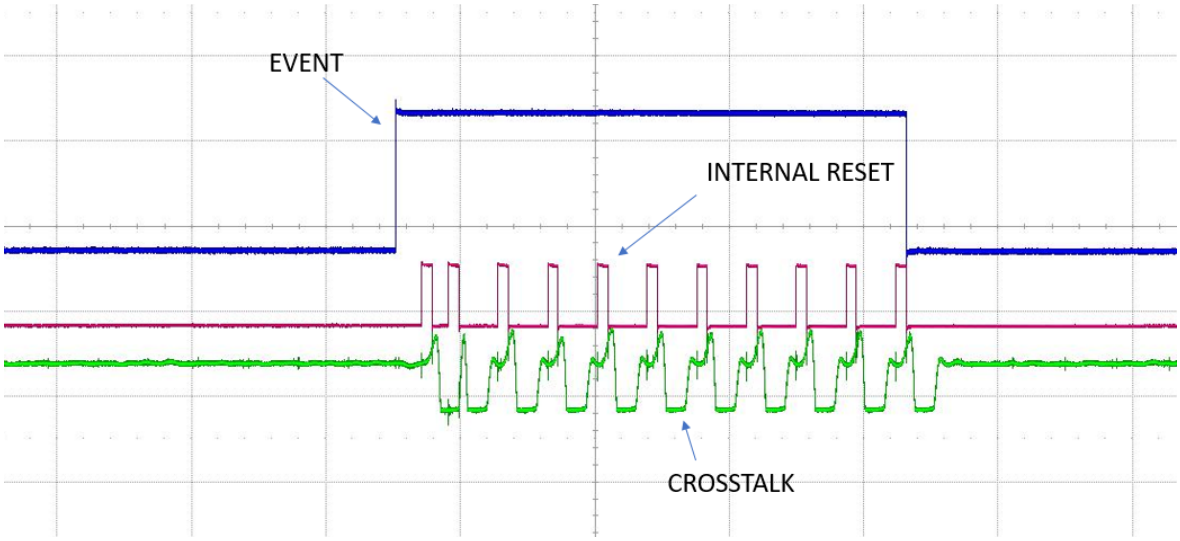

Figure 4.11 *Crosstalk in all the channels pulsing Ch9 with an high energy event (1.3Mev). Inputs 1:8 connected to Cube*

The Figure 4.11 shows that it was obtained more or less the same behaviour of the previous measurments (when all the inputs were grounded). Therefore, this confirms that the internal reset is responsible of that strange behaviour.

4.2 Drift Time

Another aspect that has been studied is the timing application. In particular it has been analized the Drift Time, as shown in Figure 4.12, it is the distance between the generation of the event and the generation of the LT related to that event.

Figure 4.12 *DAQ timing sequence for a single event*

This aspect was very important for the final experiment, in fact the timing is crucial due to the high background, in fact to reject the asynchronous background events, is important to analyze the events detected within a time window generated by a kaon trigger.

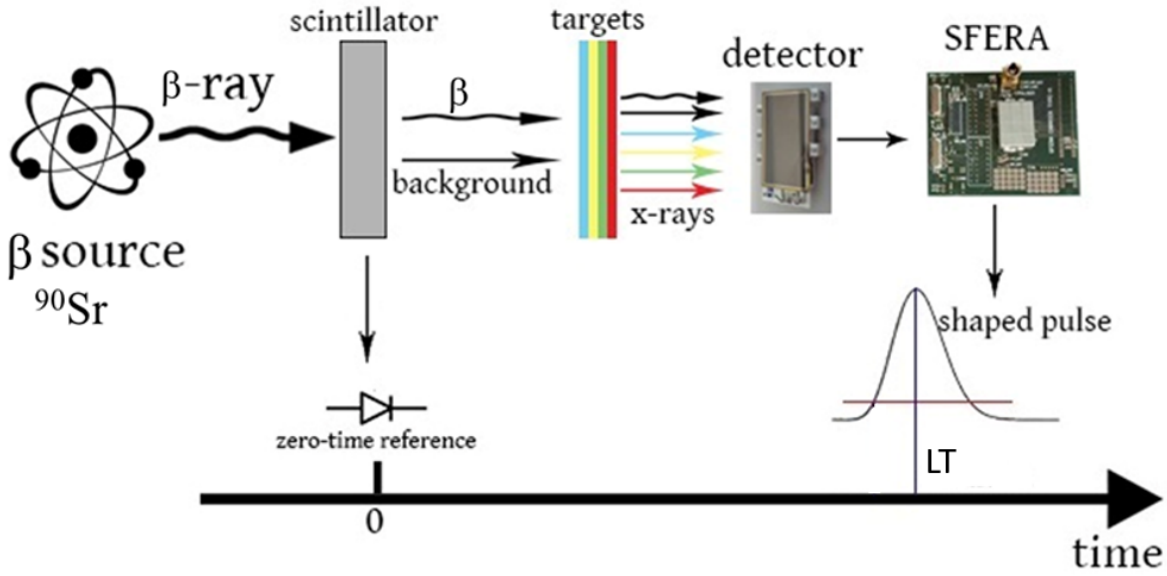

Figure 4.13 *Timing mechanism*

To compute the Drift Time with the DAQ, it was used a counter that is enable with a signal called TR_EVENT_LATCHED. The latter is created using as trigger the generation of the event, and as CLR the rising edge of the TR_OUT_LT. In this way the value of the counter is the Drift Time (the value of the counter is read on the falling edge of the ACK). With the DAQ it is also possible to plot the Drift Time vs the Amplitude.

4.3 Conclusions

During my thesis and so my experience in laboratory, numerous experimental and analytical issues have been studied. A new version of Chip has been developed with a focus on ameliorating its timing applications. Some analogue blocks like the Peak-stretcher and some digital blocks have been modified respectively. Moreover, the standard characterization of detectors and SDD units were studied, that allow us to highlight the effectiveness of the procedure and the quality of the different instruments

that the experiment will exploit. Some of those analyses just uncovered unreparable defects in the cells, while others addressed some issues that may be repaired with accurate procedures. Then, I was focused on the development of the DAQ related to the Sparse Readout acquisition, improving so the sparsification of the events. Moreover, the crosstalk study was of particular interest for the final experiment, to avoid to corrupt the valid signal, making the measurements too unrealiable, obtaing so false positive in the analysis. Furthermore, the latter study was important to try to understand the problem related to the drift time. To analyze that problem of higher drift time, inside the DAQ a way to compute correctly the timing was developed, to understand if a MIP (Minimum Ionizing Particle), can be the cause of that problem. In our analysis since all the events with multiplicity greater than or equal to 2 have been removed, it was discovered that the crosstalk is not the main reason of the problem related to the drift time, so further analyses must be done. After those analyses it was found that an improvement in the chip may be the solution. Finally, considering all the modifications made for the new release of the SFERA chip, one should expect better performance in terms of timing resolution and validity of acquired data. From the detector unit to the data storage system the chain has been analyzed and tested, there are still few detector units to be analyzed, so the characterization of the SDD modules is on-going.

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