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Department of Electronics, Information and Bioengineering
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Electronics boosts Photonics:

detector and electronic design for non-invasive monitoring and control of Silicon Photonic systems

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Emanuele Guglielmi – Electronics boosts Photonics: detector and electronic design for non-invasive monitoring and control of Silicon Photonic systems

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"Don't keep forever on the public road, going only where others have gone. Leave the beaten track occasionally and dive into the woods. You will be certain to find something you have never seen before."

— Alexander Graham Bell

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"If there is something I'm sure about, I will never do research... It's boring!" – It's funny how you often end up where you least expected. I was wrong. Four years in an awesome team proved me wrong. And now at the end of a fantastic journey, there are many people that I need to thank.

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> "**Don't keep forever on the public road, going only where others have gone.** Leave the beaten track occasionally and dive into the woods. You will be certain to find something you have never seen before. Of course it will be a little thing, but do not ignore it. Follow it up, explore around it; one discovery will lead to another, and before you know it you will have something worth thinking about to occupy your mind. All really big discoveries are the result of thought."
>
> — Alexander Graham Bell

ABSTRACT

Electronics is an essential tool that can unlock the true potential of modern Silicon Photonic technologies, overcoming their limitations. My thesis contributes to the field of electronic-photonic integration, studying and improving the innovative CLIPP detector and developing the electronics to use it in novel scientific applications.

Silicon Photonic technologies can achieve outstanding datarates, low losses, and power consumption, but require the closed-loop control of the optical devices, to compensate for their extreme sensitivity to fabrication tolerances and temperature fluctuations. The large-scale implementation of feedback control systems is halted by the inadequate state-of-the-art photo-detectors, that introduce losses to monitor the working point of the photonic circuits.

The CLIPP, ContactLess Integrated Photonic Probe, is an innovative detector developed at Politecnico di Milano that overcomes these limitations by enabling non-invasive light monitoring in silicon photonic circuits, through an impedance measurement of the waveguide.

My thesis explores the disruptive applications in Silicon Photonics that an innovative device like the CLIPP has unlocked. The work has mastered the electronic detection of the signal coming from the CLIPP, designing specific circuit implementations, in both standard discrete electronics and integrated CMOS technology. In particular, a new pseudo-resistor topology has been designed and tested to bias low-noise Trans-Impedance Amplifiers with capacitive feedback, achieving high linearity, wide bandwidth, three decades of resistance tuning range and dynamic compensation of the output offset.

In order to improve the tiny signals available when measuring

very low optical powers, this thesis has also addressed the sensor itself by demonstrating that more efficient designs can be achieved by exploiting the deep implantations at the same level of the waveguide, offered by active Silicon Photonics technologies. The new design achieved the best sensitivity ever measured with CLIPPs, while giving an insight into new aspects of the device to be studied in the future.

The effectiveness of CLIPP-assisted circuit control was exploited for light path tracking, reconfiguration, and thermal crosstalk compensation on a switch fabric router, and for light mode unscrambling on a novel topology for Mode-Division Multiplexing, that requires non-invasive monitoring to avoid disrupting the orthogonality of the spatial modes. The results would not have been possible without advanced control strategies implemented on a reconfigurable FPGA-based electronic platform specifically conceived for Silicon Photonic applications.

CONTENTS

CHAPTER

ONE

INTRODUCTION

1.1 | Silicon Photonics

Silicon Photonics is a fabrication technology that allows the realization of optical circuits on a silicon substrate using the modern manufacturing processes of the CMOS industry, and has become, in recent years, one of the most promising photonic platforms. The merit of this success can be attributed both to the excellent optical properties of silicon and to its compatibility with the CMOS industry, allowing the use of the same facilities for the production of optical devices [1].

The Silicon On Insulator (SOI) technology, in particular, offers an excellent support for the realization of these devices. Thanks to the great difference between the refractive index of silicon ($n = 3.45$) and silicon oxide ($n = 1.45$), it is possible to fabricate low-loss rectangular waveguides and devices in Si/SiO_2 with very good optical confinement characteristics and dimensions of a few hundred nanometers [2, 3]. For the same reason, Silicon Photonics allows small turn radius and, as a result, a very high miniaturization of the optical components, achieving densities of thousands of devices in less than $1\,mm^2$ [4–6]. Furthermore, silicon is transparent at wavelengths between 1100 nm and 7000 nm, widely including the IR transmission band 1300 nm to 1550 nm typically used in the field of optical telecommunications.

The ultimate goal of Silicon Photonics is the creation of high-performance integrated systems including both optical and electronic

components. Monolithic integration is the first possible approach to reach this goal, realizing Electronic-Photonic Integrated Circuits (EPIC) on the same chip using a single fabrication process [7, 8]. The topic is discussed on several paper by the scientific community: assessing the current status of the technology and the next required steps [9], discussing progress on the integration platform [10], or presenting working prototypes of monolithically integrated circuits [8, 11].

Hybrid integration is another possible approach to achieve high-performance electronic-photonic systems. The electronic and photonic chip are fabricated through different processes, allowing the optimization of each one separately, and are electrically connected though wire-bondings [12] or flip-chip [13].

1.2 | The need of control electronics

The optical properties of Silicon Photonics also involve two important disadvantages that have restrained the widespread development of the technology.

The optical devices are extremely sensitive to fabrication tolerances, as a consequence of the same high index contrast between Si/SiO_2 [14] that allows dense integration of components. For example, changing the waveguide width by only 1 nm can shift the spectral response of an interferometric device by about 100 GHz. For devices that rely on physical and geometrical parameters to provide a certain resonance, such as high-quality-factor Micro-Ring Resonators (MRR), this sensitivity is a challenging issue [15–17].

Another critical limitation of Silicon Photonics is represented by the devices vulnerability to thermal fluctuations, due to the high thermo-optic coefficient of silicon ($1.86 \times 10^{-4}\,\mathrm{K}^{-1}$ at 300 K [18]). While the sensitivity to temperature variations can be exploited by thermo-optic actuators to tune the working point of the devices, it also makes the devices susceptible to thermal drift and crosstalk, and imposes the chips to be temperature controlled. For example, a deviation of $\Delta T = 1\,\mathrm{K}$ can shift the resonance frequency of a Micro-Ring Resonator by ≈ 10 GHz [19, 20]. This susceptibility is not compatible with the typical temperature ranges of datacenter environments, without a proper cooling solution.

Sensitivity to fabrication tolerances and temperature cause the

characteristics of a fabricated photonic chip to hardly match the simulated performance, requiring an additional calibration to recover the designed functionalities [21]. Furthermore, the possibility to actively control the Photonic Integrated Circuit (PIC) is a key requirement in many applications for several reasons:

(i) Compensation of fabrication tolerances and technological non-uniformities;

(ii) Locking or stabilization of the circuit in a well-defined state independently of the temperature, electrical fluctuations, drifts, stress, and aging;

(iii) Reconfigurability of the circuit to provide the required functionality: such as in routers, cross connects, tuneable bandwidth filters, and reconfigurable add-drop multiplexers;

(iv) Adaptive circuits that modify their behavior depending on the state of the system such as signal polarization state, signal-to-noise ratio, crosstalk, eye aperture, and Bit-Error-Rate (BER).

To satisfy these requirements, the use of look-up tables of the actuators control variables is not a reliable solution, due to functional drifts and aging of the components. All these aspects become even more critical when dealing with wavelength selective devices, such as Micro-Ring Resonators, high bit-rate signals operating in coherent domain, and dense Wavelength Division Multiplexing (WDM) systems. Therefore, the closed-loop control of the optical devices has become a necessity, to compensate for their extreme sensitivity to fabrication tolerances and temperature fluctuations [22].

Electronics is a key technology to satisfy these requirements, in the form of multichannel control platforms to reliably monitor, set, hold and steer the desired working point of complex photonic systems. The control systems are realized through the implementation of multiple feedback loops. The light in the circuit is monitored by several detectors placed in strategic positions, obtaining information on the working point of the optical devices. Then, dedicated actuators are used to correct and stabilize the system operation through closed-loop control algorithms [13, 23–28].

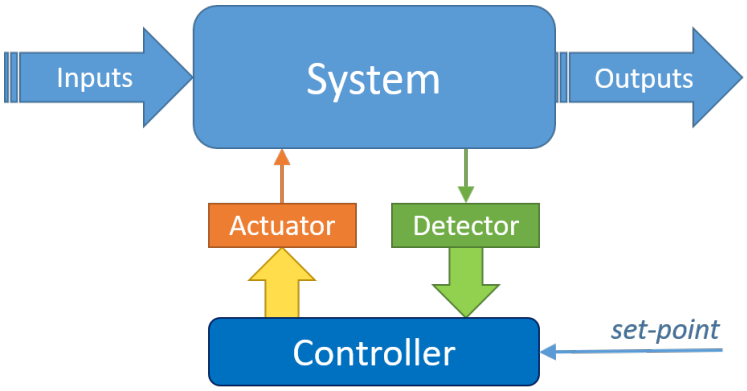


Figure 1.1 – *The control paradigm. A given system with inputs and outputs is controlled by an external controller entity, that monitors the state of the system with a detector and affects it with an actuator.*

1.3 | State of the Art of on-chip Light Detectors

The archetype of the closed-loop control scheme of a system, represented in Figure 1.1, is composed by a three essential elements:

(i) The detector, or sensing element, to extract information about the state of a system, ideally without perturbing the system itself;

(ii) The controller, able to interpret the information from the sensing element and determine the best course of action to intervene on the system, through the execution of a control algorithm or logic;

(iii) The actuator, driven by the controller to modify the state of the system towards the desired working point.

Electronics can offer robust, powerful and configurable controllers in the form of Field-Programmable Gate Arrays (FPGA) with excellent parallel computation performances for multichannel applications, easy-to-use microprocessors offering good all-round performance, and custom mixed-signal electronics for ultra-optimized applications.

At the same time, Silicon Photonic technologies provide state-of-the-art actuators based on thermo-optic effect to realize pure phase shifters. When fast tuning and low power consumption are required,

actuators based on carrier injection/depletion effects can reach modulation speeds up to 80 Gb/s [29] at a cost of only 0.8 fJ/bit [30].

Instead, the development of minimally-invasive waveguide power monitors for the estimation of the working point of a PIC is still one of the key challenges for integrated optical technologies [1, 31–33]. The main reason is that state-of-the-art integrated photo-detectors require the absorption of a certain amount of light, wasting usable signal and affecting the circuit functionality [34]. In this section, I review the state of the art of on-chip light detectors, discussing two main approaches: monolithic and heterogeneous integration.

1.3.1 | Monolithic Integration

The first approach relies on the integration of the detectors directly on the same chip, by using a single unified fabrication process. The detectors proposed by the scientific community in this category exploit two different techniques.

Waveguide photo-detectors

The silicon waveguide itself can be used as a detector, exploiting different photon absorption phenomena to generate an electrical signal. The realization of these detectors is challenging due to the bandgap properties of the material. Silicon has an indirect bandgap of 1.12 eV, higher than the energy of the photons from 0.8 eV to 0.95 eV in the typical wavelength range from 1300 nm to 1550 nm of optical telecommunications. However, the absorption of photons with a lower energy than the silicon bandgap is possible due to sub-bandgap absorption phenomena: Defect-State Absorption (DSA), Two-Photon Absorption (TPA) and Surface-State Absorption (SSA). Waveguide integrated detectors found in the literature usually exploit or promote these mechanisms to generate an electrical signal.

Defect mediated photo-detectors use inert ions implantation to create mid-gap states that increase the absorption at wavelegths from 1270 nm to 1740 nm [35], including the typical telecommunication bands. High speed implementations have been presented in the literature, achieving a bandwidth up to 20 GHz [35]. In this case, Si^+ ion implantation increased the optical absorption from the regular 2-3 dB/cm to 100-200 dB/cm. The integration has also been demonstrated in rib waveguides, with the fabrication of two

contacts (p^+ and n^+) allowing access to the waveguide bulk [36]. Here, proton implantation is used to boost the optical absorption in the core of the waveguide, achieving a responsivity of 3 mA/W in a wavelength range from 1530 nm to 1610 nm. Other works have reported good performance with B^+ [37] and He^+ [38] ion implantations. The main advantage of this approach is that annealing at high temperatures > 400 °C can effectively remove the ions and the additional losses [39], allowing the integration of multiple detectors for the device testing at wafer scale to be eventually removed before packaging.

Two-Photon Absorption detectors exploit a second-order nonlinear phenomenon where two photons of identical or different frequencies are absorbed together to excite an atom to a higher energy state. Since it is proportional to the square of the optical intensity, it is generally a weaker contribution than first-order phenomena, but can dominate in presence of intense optical fields. Resonant cavities can be employed to enhance the generated photocurrents by over 5 orders of magnitude, as demonstrated in a sub-Gb/s telecom detector [40]. TPA has also been successfully exploited for pulse autocorrelation measurements at 1500 nm [41].

Finally, Surface-State Absorption is a sub-bandgap phenomenon allowing free carrier generation, due to defects present at the edge of the silicon crystal or at the Si/SiO_2 interface between the waveguide core and cladding, even in an ideal roughness-free interface [42]. These defects create mid-gap energy states that support the absorption of photons and the generation of electron-hole free carrier pairs. The phenomenon can be enhanced by exploiting the energy build-up of resonant cavities, as it has been demonstrated with a p-i-n diode embedded in a silicon Micro-Ring Resonator [43]. Additionally, the waveguide geometry can be modified in a small section to increase the interaction of the optical mode with the edge of the waveguide, obtaining losses of 5 dB/cm and a responsivity of 36 mA/W [44].

Germanium photo-detectors

Germanium is a good candidate as an absorbing material to be used in Silicon Photonic PICs [5], because it can be introduced in a CMOS fabrication process relatively easy, since Si/Ge contacts are already used in CMOS electronics. Additionally, bulk germanium absorbs the 1300 nm telecommunication window, and most of the C and L

bands.

Area grown by chemical vapor deposition is one of the most common ways to integrate germanium and silicon [45]. However, there is a 4% lattice mismatch that causes the formation of threading defects [46]. These produce mid-gap generation-recombination centers, which increase the dark current of the detector relative to a bulk Ge diode [47, 48]. Additionally, they affect the planarity of the wafer hindering the CMOS compatibility of the process. The introduction of graded *SiGe* buffer layers can be used to smooth the transition, however, this comes at the cost of a more complicated deposition process.

Germanium epitaxially grown on silicon has better absorption properties to bulk germanium in the C and L transmission bands. The improved detection is due to a mechanical strain between the two materials, due to the different thermal expansion coefficients of silicon and germanium [49]. This effect decreases the direct bandgap energy to $\approx 0.782\,\text{eV}$ or lower [5].

Several papers in the literature present germanium photo-detectors monolithically integrated on silicon [50–56], some obtaining remarkable performance in terms of responsivity, efficiency, current noise [54, 55] and bandwidth [52].

1.3.2 | Heterogeneous Integration

The second approach to integrate detectors in Silicon Photonic is called Heterogeneous Integration, and relies on the realization of the photo-detectors through a completely separate fabrication process. The photonic circuit and the detectors follow different processes until they are interfaced together. This approach allows freedom in the development of the photo-detectors, using Germanium or III-V photodiodes, obtaining exceptional results in terms of responsivity, bandwidth and dynamic range [57].

The critical aspects of heterogeneous integration are the mechanical assembly of the devices and the coupling scheme used to redirect the light into the photo-detectors. In the literature, several coupling methods have been proposed, including gradually pushing the optical field into the detector through evanescent coupling [58] or adiabatic taper [59, 60], vertical redirection of the light through gratings [61, 62] or 45° polished facet [63], direct butt-coupling of

the detectors at the end of the waveguide [64].

1.4 | The CLIPP

Most the techniques presented in the previous section require the use of on-chip or external photo-detectors to partially tap (or completely redirect) the light traveling in the optical circuit. In other cases, like in waveguide detectors, the propagation losses are increased on purpose through ions implantation or engineering of the waveguide shape, to increase the responsivity of the devices. Though effective on single devices, these approaches are not suitable to large-scale integration circuits, where tapping or attenuating light in several points would result in a large and impractical optical power waste.

Local feedback control, assisted by transparent optical detectors, is envisioned as an enabling technology for the realization of complex and arbitrarily reconfigurable systems on a chip. In this panorama, the CLIPP, a detector developed at Politecnico di Milano, offers promising results to overcome the mentioned issues.

The CLIPP (ContactLess Integrated Photonic Probe) is a device that allows non-invasive light monitoring in silicon photonic circuits, through an impedance measurement [65]. The light travelling through integrated waveguides induces a variation in the conductivity of the core, due to the Surface-State Absorption phenomenon. Differently from any other detector in the literature, the core is accessed capacitively with two electrodes, that are placed distant enough from the waveguide to avoid any perturbation in the light electric field. The changes in conductivity can be detected with a low-noise electronic readout circuit and used to steer the bias point of the optical devices towards the optimal functioning regime [66]. Single CLIPPs have been used to assist in the fiber-to-waveguide alignment process [67, 68] and to achieve wavelength locking of silicon Micro-Ring Resonators [69]. Multiple CLIPPs can monitor the working point of several optical devices without perturbing the system, allowing the implementation of simultaneous feedback loops to control the global behavior of photonic circuits [70].

A vibrant research ecosystem has born around this promising and effective device: studying the technological optimization of the detector itself, the development of a dedicated control electronics, and the design of specific photonic circuits that take advantage of

the CLIPP unique features.

My thesis is part of this context and contributes to the research with the study and the definition of the device design guidelines, the development of an improved CLIPP architecture, and the enhancement of the low-noise readout front-end. Additionally, electronic platforms specifically developed have been used to successfully control both well-known router topologies and a novel photonic circuit for Mode Division Multiplexing.

Part I

The Detector

CHAPTER

TWO

CLIPP DESIGN RULES

In this chapter, I introduce the basic concepts of the CLIPP detector, providing the relations between the electrical and geometric parameters of the device. In particular, I discuss the optimization of the CLIPP design, through an in-depth analysis of its equivalent electrical circuit, systematic electrical simulations and experimental data. This includes the CLIPP miniaturization, the layout on the photonic chip and the off-chip electrical interconnections to target dense photonic circuits.

The results of this work have been published in the paper

M. Carminati, A. Annoni, F. Morichetti, **E. Guglielmi**, G. Ferrari, D. O. De Aguiar, A. Melloni, and M. Sampietro. "Design Guidelines for Contactless Integrated Photonic Probes in Dense Photonic Circuits". In: *Journal of Lightwave Technology* (2017). ISSN: 07338724. DOI: 10.1109/JLT.2017.2710268

and are here presented with some additional findings and results.

2.1 Working principle

Figure 2.1 shows the schematic of a CLIPP integrated with a channel Si waveguide buried in a silica cladding. The CLIPP consists of two electrodes placed on top of the upper cladding, thus separated from the Si waveguide core by an electrically insulating layer. The thickness of the optically-transparent insulating layer is chosen in order to make the loss induced by the electrodes on the guided light negligible. This concept will be discussed in detail in Section 2.2.1.

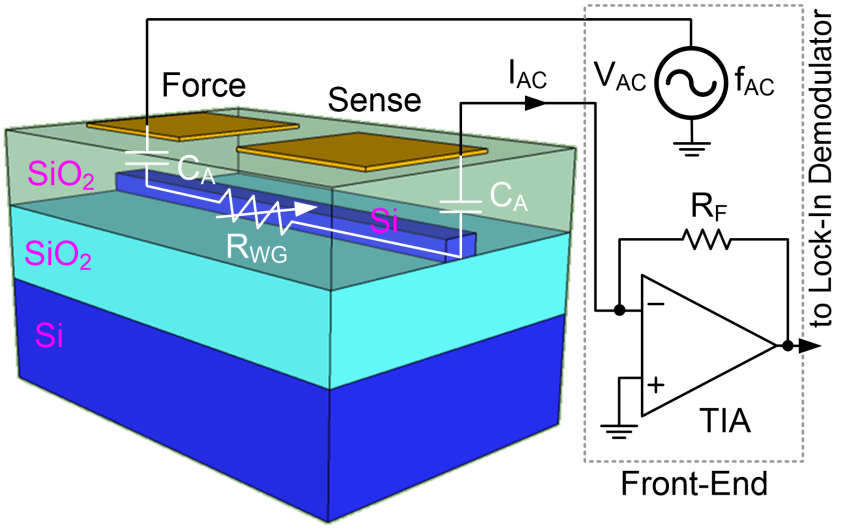
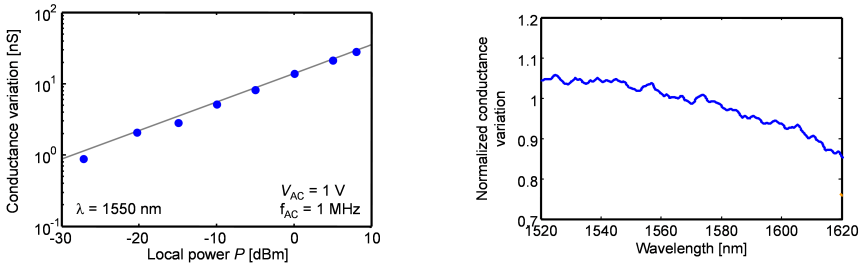


Figure 2.1 – *3D representation of a CLIPP applied on a Si core channel waveguide and connection to external electronics.*



(a) **(b)**

Figure 2.2 – *(a) Waveguide conductance variation as a function of the local optical power in the waveguide. Experimental data reproduced from [72]. (b) Normalized CLIPP response as a function of the light wavelength over a range of* 100 nm *around* 1570 nm.

The CLIPP monitors the light intensity in the waveguide by measuring the light-induced change of the electrical conductance of the waveguide associated with SSA at the surface of the Si core [42, 44]. Because the insulating layer prevents a direct DC access to the conductance of the waveguide, AC electrical probing is necessary. To this aim, an alternated voltage V_{AC} at frequency f_{AC} is applied at one electrode (called *"Force"*) of the CLIPP, and the current I_{AC} from the other electrode (called *"Sense"*) is collected by a Trans-Impedance Amplifier (TIA), feeding a Lock-In Amplifier for the measurement of the complex impedance between the two metallic electrodes. As it will be detailed later, this impedance is related to the waveguide conductance, allowing the detection of the local optical power in the waveguide. To give an example of the CLIPP responsivity, Figure 2.2a shows the measured light-induced change of the waveguide conductance vs the optical power in a Si channel waveguide buried in a silica cladding and operating at a wavelength of 1550 nm. A sensitivity down to −30 dBm, over dynamic range of 40 dB is demonstrated [66]. In this device, the width of the Si core is $w = 480$ nm, and the size of the CLIPP electrodes is 20 µm × 200 µm separated by 100 µm. Previous works have proved the functionality of the CLIPP in single mode and multimode waveguides [65], both for TE and TM polarization [66]. Figure 2.2b also shows that the CLIPP exhibits a small sensitivity to wavelength, behaving as a broadband light monitor. Over a span of 100 nm around 1570 nm, an efficiency variation of ±10% is observed, that has to be attributed to a reduction of the SSA photo-generation for increasing wavelength, in agreement with decreasing photon energy. A summary of the CLIPP performances extracted from previous contributions is in Table 2.1.

Table 2.1 – *Summary of the CLIPP performance and geometry from previous contributions.*

Performances of the CLIPP in Si Waveguides		
Feature	Parameter	Value
Electrode size	L	100 µm
Electrode distance	D	80 µm to 100 µm
Minimum sensitivity	P_{min}	−38 dBm
Dynamic range	$\frac{P_{max}}{\Delta P_{min}}$	40 dB
Perturbation	$\frac{\Delta n}{n}$	0.5 ppm
Probing voltage range	V_{AC}	0.1 V to 10 V
Maximum speed	BW	40 kHz
Operating wavelength	λ	1.3 µm to 1.6 µm

2.2 | Equivalent electrical model

The equivalent electrical model of the CLIPP is discussed in detail in this section, in order to identify the different paths that induce a current through the device. Understanding the parameters that affect the current through the waveguide (modified by the local optical power) with respect to the current through all other electrical elements (not modified by the optical power) is crucial for the optimization of the device geometry.

Figure 2.3 shows the main design parameters of a CLIPP integrated on a Si waveguide buried in a SiO_2 cladding. The upper and lower cladding have thickness t_{CLA} and t_{BOX}, respectively, and are considered for simplicity of the same material with relative dielectric constant ϵ_{ox}. The two eletrodes of the CLIPP (assumed of the same size) have a rectangular shape, with a width W and a length L, and are separated by a distance D.

The electrical model of the structure includes the following elements:

- Access capacitance C_A from the electrodes to the waveguide;
- Resistance R_{WG} of the silicon waveguide;
- Capacitance C_B between each electrode and the silicon substrate;
- Capacitance C_{SUB} between the waveguide and the substrate;

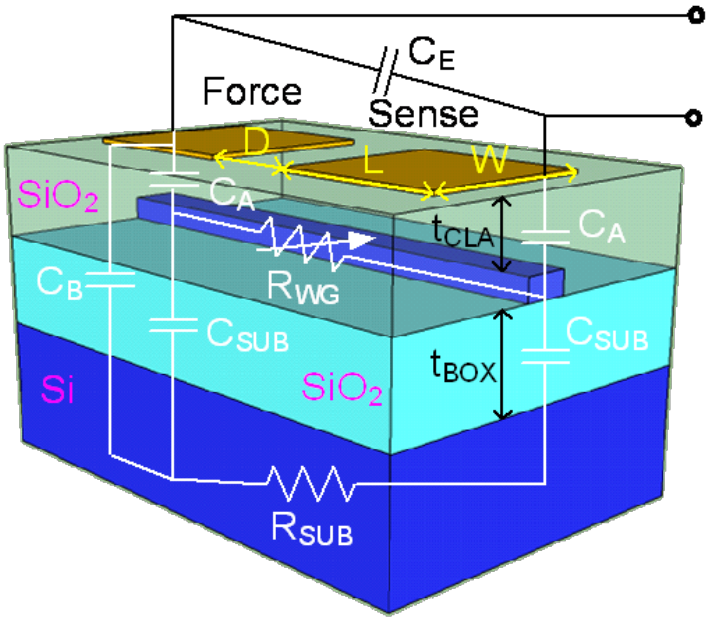


Figure 2.3 – *Linear optical waveguide with CLIPP electrodes over the cladding highlighting the equivalent electrical model of the probe. A main sensing path from the Force electrode to the Sense electrode through the waveguide is identified ($C_A - R_{WG} - C_A$) in parallel to a substrate contribution ($C_B - C_{SUB} - R_{SUB}$). The stray capacitance (C_E) between the electrodes and the wires connecting the probe to the front-end electronics is also highlighted.*

- Resistance R_{SUB} of the silicon substrate;
- Parassitic capacitance C_E between the CLIPP electrodes (including external bondings and connections).

In the following subsections, the relations between the elements of the electrical model and the design parameters of the CLIPP are extensively discussed.

2.2.1 | Waveguide resistance and access capacitance

The resistance R_{WG} of the Si core in the waveguide section of width w and thickness h between the electrodes is given by

$$R_{WG} \approx \frac{D}{\sigma w h} \tag{2.1}$$

where σ is the Si electrical conductivity that changes with the number of carriers photo-generated by the optical signal in the waveguide.

The access capacitance C_A is the capacitance of the dielectric slab between the top metal electrode of width W and the waveguide of width $w \ll W$. Because the electrode is much larger than the waveguide, the effective width can estimated as $(w + 2t_{CLA})$ and used in the parallel plate expression, where the correction factor $2t_{CLA}$ accounts for the isotropic expansion of the electric fringing field [73], thus giving:

$$C_A \approx \epsilon_0 \epsilon_{ox} \frac{L\,(w + 2t_{CLA})}{t_{CLA}} \tag{2.2}$$

Assuming a Si core of width $w = 480\,\text{nm}$ and height $h = 220\,\text{nm}$ (a common choice for single-mode Si waveguide) with an upper cladding thickness $t_{CLA} = 700\,\text{nm}$, and a Si doping level of about $10^{15}\,\text{cm}^{-3}$, the capacitance per unit length amounts to $\sim 90\,\text{aF}/\mu\text{m}$ ($\epsilon_{ox} = 3.9$) and the resistance per unit length results $\sim 1.3\,\text{M}\Omega/\mu\text{m}$. For an electrode of $L = 100\,\mu\text{m}$, C_A results $\sim 9\,\text{fF}$, linearly increasing with L at the expenses of a larger area occupation of the electrode. For a distance between electrodes of 100 µm the waveguide resistance R_{WG} results equal to 130 MΩ.

From the standpoint of the AC measurement of R_{WG}, the voltage drop across C_A should be minimized by imposing its impedance, given by $1/(2\pi f_{AC} C_A)$, much smaller than R_{WG}. Consequently, a

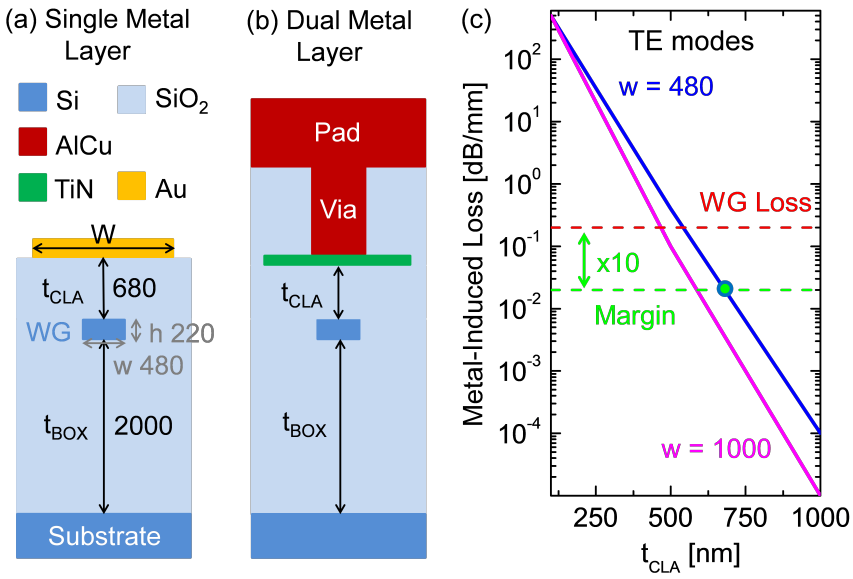


Figure 2.4 – *Scale drawing (dimensions in* nm*) of two vertical cross-sections of SOI technological platforms with one (a) and two (b) metal layers, where the CLIPP is implemented with a cladding thickness t_{CLA} of about* 700 nm *to keep negligible the metal induced loss (c) due to the CLIPP interaction with the optical field.*

high value of C_A would be beneficial in lowering the probing frequency f_{AC} required to short this capacitance. On the other hand, the reduction of t_{CLA} causes an increase of the waveguide loss due to the light interaction with the metal electrode, as shown in the simulations reported in Figure 2.4c. For a single mode waveguide ($w = 480\,\text{nm}$) the fundamental TE mode experiences a lower loss with respect to the TM mode, due to the higher confinement of the field in the Si core. Analogously, for multimode waveguides ($w = 1\,\mu\text{m}$), the higher confinement of the fundamental mode results in a slightly lower loss compared to single mode waveguides. Targeting a metal induced loss 10 times lower than the intrinsic propagation loss (0.2 dB/mm, as indicated in the figure, is a common value for typical Si waveguides), a value of t_{CLA} around 700 nm is obtained for the effect of the CLIPP to be completely negligible independently of its size.

2.2.2 | Electrical parasitic components

An alternative path for the current I_{AC} is provided through the conductive Si substrate with resistance R_{SUB} coupled by C_B. This is in addition to the main path through C_A and R_{WG} that allows to sense the resistance variation ΔR_{WG} as a consequence of local optical power variations. The current through this alternative path should be minimized by maximizing its impedance. The capacitance C_B between the top metal electrodes (dimensions W and L) and the substrate (supposed of larger area) is, similarly to (2.2), well described by

$$C_B \approx \epsilon_0 \epsilon_{ox} \frac{L\,(W + (t_{CLA} + t_{box}))}{(t_{CLA} + t_{box})} \tag{2.3}$$

where $t_{CLA} + t_{box}$ is the overall thickness of the dielectric slab. To obtain a small C_B the width W of the CLIPP electrode should be small, while the length L is constrained by the choice of a sufficiently large C_A. Assuming $t_{box} = 2000\,\text{nm}$, an electrode size of $W = 5\,\mu\text{m}$ and $L = 100\,\mu\text{m}$, C_B results in about 13 fF. Note that a photonic platform with a bigger t_{box} is beneficial to provide smaller values of C_B.

The two CLIPP electrodes are also connected by a direct stray coupling, indicated as C_E in Figure 2.3, due to the capacitance between the two metal electrodes and their routing to the bonding pads on the chip. The coupling between the corresponding bonding

wires and eventually between the cables of the external connection also contribute to C_E. The capacitance C_E is driven by the same voltage signal V_{AC} of the R_{WG} path and produces a current that is not modulated by the optical power but is read by the same TIA. High value C_E would therefore degrade the CLIPP performance, eventually saturating the TIA itself. Furthermore, it is difficult to estimate the value of C_E since it depends on many different contributions, coming from both the on-chip connection design and the off-chip PCB design. The uncertain value of the C_E forces the TIA to be designed around the worst case estimation of its value. In particular, a high value of C_E has to be contained by limiting the gain of the TIA. If the feedback element of the TIA is implemented with a capacitor C_F to optimize the noise, the worst case of the C_E sets a lower limit to C_F to avoid saturation of the output of the amplifier. The current signal through C_E is, therefore, a direct competitor to R_{WG} and should be minimized. As the main contribution is generally due to the layout of the CLIPP in the photonic chip, some design guidelines will be explained in Section 2.4. Despite its value, it is important to note that the current through C_E is in quadrature (up to 90° phase shifted) with respect to the signal current in R_{WG}. Thanks to this property, a Lock-In demodulator scheme is ideal to dump the contribution of the C_E as much as possible while selecting the signal in phase to R_{WG}.

2.2.3 | The role of the substrate electrical connection

The Si substrate provides a resistive path, R_{SUB}, in parallel to the waveguide resistance R_{WG}. The lower the substrate resistivity, the higher is the parasitic current that ultimately mixes with the current flowing through R_{WG}, especially at higher frequency where the admittance of C_B decreases. Low resistivity substrate therefore may lead to a reduction of the measurement sensitivity. This parallel effect on the overall current between the two CLIPP metal electrodes is shown in the Figure 2.5. The dashed line corresponds to the ideal case in which only the $C_A - R_{WG} - C_A$ path for the signal current is considered (no substrate). Their values are calculated as lumped parameters given by (2.1) and (2.2), showing that the R_{WG} plateau at the expected value of about $R_{WG} = 130\,\mathrm{M\Omega}$ is correctly reached at frequencies above 1 MHz ($L = 200\,\mu\mathrm{m}$, $D = 100\,\mu\mathrm{m}$). This

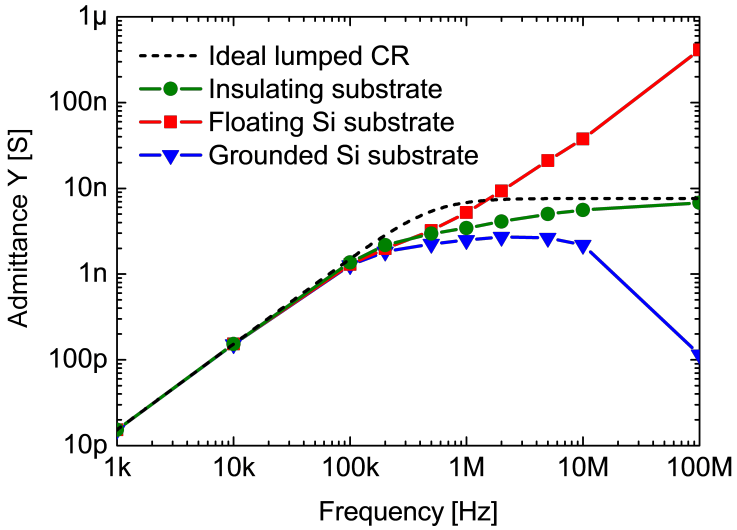


Figure 2.5 – *FEM simulations of the CLIPP structure as in Figure 2.3 ($L = 200\,\mu m$, $D = 100\,\mu m$, $W = 20\,\mu m$, $C_A = 18\,fF$, $R_{WG} = 131\,M\Omega$, $C_E = 0$, $t_{BOX} = 2\,\mu m$) with different electrical connections of the conductive silicon substrate, either floating or grounded. The graph shows the admittance between the two CLIPP electrodes as a function of frequency.*

ideal situation is compared in Figure 2.5 with the numerical results obtained by COMSOL (Finite Element Method, FEM) simulations of the full device as in Figure 2.3. The circles represent the simulated case in which the resistivity is made very high (insulating substrate) showing a very good matching with the lumped prediction.

The possibility to address the waveguide resistance (the plateau in the figure) in order to be sensitive to optical power variations is also verified by connecting the substrate to ground (triangles). In this case, indeed, the current signal collected by the sensing CLIPP electrode is still due to the $C_A - R_{WG} - C_A$ path thanks to the fact that the current through the substrate is driven away by the ground short circuit. Only at very high frequencies the curve tends to decrease as a result of the current loss toward the substrate due to the distributed C_{SUB} capacitance along R_{WG}. In this situation the voltage divider given by C_A and C_{SUB} reduces the voltage across R_{WG} and correspondingly decreases the plateau of the admittance spectrum.

Figure 2.5 also shows the detrimental effect of leaving the substrate floating (squares). In this case the device becomes a two

electrodes device and consequently both currents through R_{WG} and through R_{SUB} are collected by the sensing electrode (TIA) and measured. The plateau might disappear (in fact it moves to higher frequencies the higher is the substrate doping) and the dynamic range of the TIA must be designed for a total current higher than that of R_{WG} alone.

The best CLIPP sensitivity is achieved with the use of a high resistivity wafer and a favorable ratio between the oxide thicknesses ($t_{box} > t_{CLA}$), to have the overall admittance of the $C_A - R_{WG} - C_A$ path much lower than the $C_B - R_{SUB} - C_B$ path. In addition, it is important to have a solid grounding of the chip substrate. The use of suspended waveguides of micro-machined Si chips, where the bulk is etched away [74], goes favorably in the direction of a more sensitive CLIPP.

The COMSOL simulation of Figure 2.5 also indicates that the capacitance C_{SUB}, which is distributed along R_{WG} toward the substrate, has a minor effect on the admittance spectrum in the frequency range of interest as long as the width W of the CLIPP electrode is larger than the waveguide width w, as it normally is.

2.3 | Optimal readout frequency

Understanding the interplay between the electrodes dimensions (W, L) and distance (D) and the most suitable probing frequency f_{AC}, is crucial to optimize the sensitivity of the measurement. The reference frequency f_{low}, corresponding to the pole of the admittance of the $C_A - R_{WG} - C_A$ path when the substrate effect is negligible, is the lower bound of the sensing plateau as discussed in Figure 2.5:

$$f_{low} = \frac{1}{2\pi R_{WG} \frac{C_A}{2}} \approx \frac{1}{DL} \tag{2.4}$$

In order to measure the resistance $R_{WG} = \frac{1}{G_{WG}}$ without the attenuation caused by the voltage drop across C_A (i.e. well in the resistive plateau), the CLIPP operating frequency f_{AC} should be higher than f_{low}. Note that a reduction in size of the CLIPP, i.e. D and L, implies increasing f_{AC}. Assuming the coupling to the waveguide and its resistance only proportional to the length of the electrode L and the distance between the electrodes D respectively, given a certain total

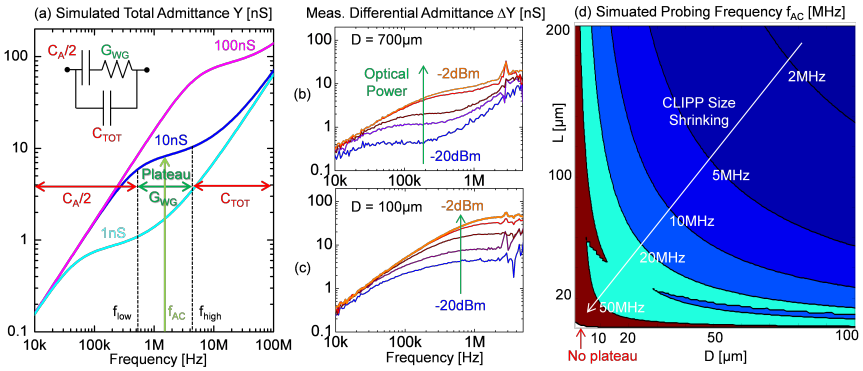


Figure 2.6 – *(a) Simulated CLIPP admittance spectra Y approximated with the lumped model in the inset (with* $G_{WG} = 1\,\text{nS}$, $10\,\text{nS}$ *and* $100\,\text{nS}$, $C_A = 18\,\text{fF}$, $C_{TOT} = 1\,\text{fF}$*), showing the shift of the plateau as* G_{WG} *varies. (b) (c) Shift of the plateau in the measured differential admittance spectra for two values of D (*700 *vs* $100\,\mu\text{m}$, $L = 200\,\mu\text{m}$, *grounded substrate) for increasing local optical power (*$-20\,\text{dBm}$, $-15\,\text{dBm}$, $-10\,\text{dBm}$, $-5\,\text{dBm}$ *and* $-2\,\text{dBm}$*). (d) Simulation of the interplay between the CLIPP footprint (L, D) and the corresponding probing frequency* f_{AC}*. CLIPP miniaturization results in higher* f_{AC}*; at* $50\,\text{MHz}$ *the minimum CLIPP length is* $50\,\mu\text{m}$ *(*$L = 20\,\mu\text{m}$, $D = 10\,\mu\text{m}$*).*

CLIPP length (L_{TOT}), the lowest operating frequency is obtained with $L = \frac{L_{TOT}}{4}$ and $D = \frac{L_{TOT}}{2}$. Figure 2.6a reports the admittance spectra simulated using the simplified electrical model shown in the inset, where C_{TOT} is the total capacitance in parallel to the main sensing path $C_A - R_{WG} - C_A$. In the common situation of $R_{SUB} \ll R_{WG}$, C_{TOT} is given by C_B (CLIPP device) in parallel to C_E (external connection). The simulations are reported for three values of conductivity of the waveguide, emulating different local optical power, and show the existence of a range of frequencies where the admittance is sensitive to R_{WG}. Figures 2.6b and 2.6c report the differential admittance spectra ΔY obtained subtracting the spectrum recorded in absence of light from the spectrum measured as a function of local optical power (from $-20\,\text{dBm}$ to $-2\,\text{dBm}$) for two values of D (100 and $700\,\mu\text{m}$). A differential measurement is preferred to reduce the admittance term given by C_{TOT}, ideally independent of the optical power. The figures show i) how the admittance increases with light intensity, ii) how the plateau shifts to higher frequency for increasingly smaller CLIPPs (shorter D) in accordance to (2.4) and iii) how the plateau

shifts to higher frequency also when increasing the optical power, i.e. the conductivity of the waveguide increases and the resistance R_{WG} decreases. Thanks to the sub-linear relation between conductivity and optical power [65], a span of about two orders of magnitude of optical power corresponds to only one decade of variation of the value of G_{WG} and, correspondingly of f_{low} (since C_A is fixed), thus allowing operation at a fixed frequency f_{AC}, as exemplified by the arrows in Figure 2.6b and 2.6c. In case extremely large dynamic ranges ($>$ 30 dB) should be monitored, an adaptive algorithm for tracking the conductance by adjusting f_{AC} would represent a feasible and robust solution.

Since f_{low} is inversely proportional to the product $D \cdot L$, a size reduction of the CLIPP (as might be the case when fitting the CLIPP into small ring resonators) corresponds to an increase of f_{low} and consequently of the operating frequency f_{AC}. As visible in Figure 2.6(a-b), an increase of f_{AC} collides with f_{high}, the upper bound of the plateau due to C_{TOT}: $f_{high} \sim \frac{1}{(2\pi \cdot R_{WG} \cdot C_{TOT})}$. The contour plot of Figure 2.6d shows the value of the optimal f_{AC} as a function of L and D. In this numerical simulation, C_{TOT} includes C_B and the direct coupling capacitance between the two coplanar electrodes through air and silicon, estimated with conformal mapping expressions [75]. In this map, if the plateau extends for more than a decade, f_{AC} is set as $10 \cdot f_{low}$. If the plateau is narrower, f_{AC} is the mean between f_{high} and f_{low}. Finally, if $f_{high} \leq f_{low}$, the plateau vanishes. This plot can be useful in sizing the optimal CLIPP dimension. Although in its prototypal implementation the CLIPP operation was initially demonstrated with conservative values ($L = 2D = 200\,\mu m$), a significant reduction of this size can be achieved. In fact, setting $L = 2D = 20\,\mu m$ ($L_{TOT} = 50\,\mu m$, compatible with the size of most photonic devices) would require f_{AC} around 50 MHz.

Going high in measurement frequency requires a careful pace. In order to extend f_{AC} to such high frequencies, the substrate capacitances C_B and C_{SUB} should be minimized by maximizing t_{BOX} or by choosing a high-resistivity substrate. From an instrumentation point of view, operating above 50 MHz requires a careful electronic design because the impact on the phase delays of the connection cables is no longer negligible. Furthermore, it requires a TIA and a Lock-In amplifier with larger bandwidth.

2.4 | Layout Guidelines

2.4.1 | Inter-electrode capacitance of the bonding wires

The spurious capacitance C_E between the two electrodes of the CLIPP, introduced in Section 2.2.2, activates a parasitic current in parallel to the signal in R_{WG} which is not modulated by the optical power, thus affecting the measurement. To minimize its value, the *Force* and *Sense* connections to the corresponding electronic inputs should be as distant as possible, one with respect to the other. If the CLIPP pads are locally placed, as in Figure 2.7a, bonding wires may be the major source of C_E. Consider that two bonding wires running parallel for 1 cm at a distance of 200 µm would contribute for about 100 fF, giving a high spurious current contribution at the typical working frequencies of 1 MHz. Therefore, it is a good practice to plan the bonding wires of the *Force* and of the *Sense* electrodes in opposite directions, as sketched in Figure 2.7a.

2.4.2 | Routing and minimization of the interconnections

In optically dense chips [76, 77] where several CLIPP devices are integrated, the bonding pads will likely be aligned along the PIC border. In this case, in addition to the bondings, also the routing from the electrodes to the bonding pads becomes important. First, it would be convenient to connect the V_{AC} *Force* electrodes of all the CLIPP to a single shared *Force* pad, thus saving space on the PIC and reducing the number of external bonding wires. Figure 2.7b shows the advantages in terms of area occupation and of bonding connections that a common V_{AC} can bring. Figure 2.7c highlights how a single *Force* line helps in keeping C_E to a minimum: the V_{AC} signal can be routed to the CLIPPs from a side pad of the PIC, placed well apart from the signal lines and from the pads (lined in the north border of the PIC).

The layout of the *Sense* lines on the PIC is more relaxed, affecting cross-talk between channels and noise very marginally. In fact the coupling capacitance between channels is indeed small for strips routed in parallel at a distance > 50 µm, indicating that there is a great freedom in the layout to cope with even very dense optical architectures. Also the width of the *Sense* lines is not critical: it would translate into a capacitance to ground that adds to the TIA

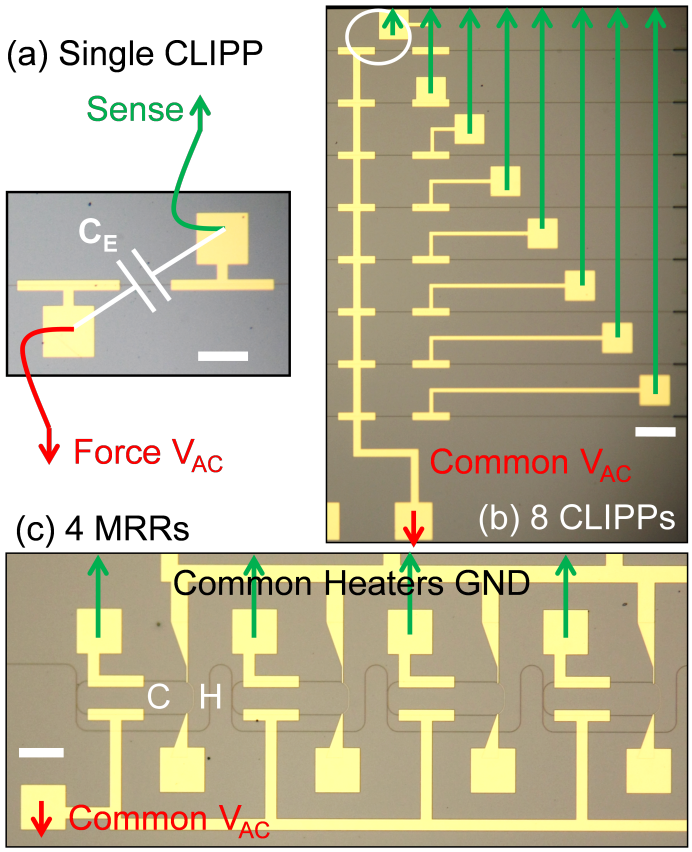


Figure 2.7 – *Guidelines for optimal layout (a) opposite V_{AC} Force and Sense bonding wires (red and green lines, respectively) to minimize C_E, (b) sharing of V_{AC} pads for 8 parallel CLIPPs, (c) common V_{AC} and common heater grounds (H) in 4 cascaded MRRs. The scale bar is 100 µm in all the photos.*

input, eventually increasing the TIA noise. As long as the width of these strips is within 5 µm, their contribution to the total input capacitance at the TIA (typically of few pF) is indeed negligible.

2.4.3 | Dummy metal tiles

When dealing with the PIC layout, care should be dedicated to the dummy metal tiles that foundries add to balance the metal fill factor for the etching process. These metal tiles, despite being usually floating, offer a bridge between the electrodes, increasing C_E, and from the *Sense* electrode towards the grounded substrate (C_B), usually increasing the input noise of the amplifier.

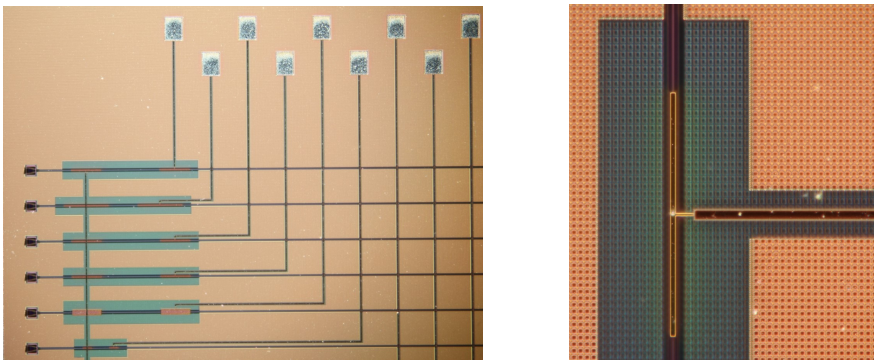
A non-filling area around the CLIPP is important to avoid dummy metal tiles near the electrodes and especially in between, that would increase C_E favoring the direct coupling between the electrodes. The presence of metal tiles should also be considered when designing the *Force* and *Sense* traces, as metal tiles effectively reduce the equivalent distance between them.

The dummy metal tiles can also aid the coupling C_B towards the substrate: being close to the *Force* and *Sense* traces they are capacitively coupled to them and aid the connection with the substrate. A small no-fill area around both *Force* and *Sense* traces can be beneficial to reduce their indirect coupling to the substrate through the dummy tiles. Additionally, the *Force* and *Sense* traces themselves can be designed thin, because they do not carry large currents, to reduce their direct C_B to the substrate.

Figure 2.8 shows an example of optimal routing of multiple CLIPP with the *Force* connection shared. A large no-fill zone was designed around the CLIPP removing the tiles closer than ~ 30 µm, and two smaller margins were introduced on either side of the *Force* (~ 8 µm) and *Sense* (~ 3 µm) connection.

2.4.4 | Heater-CLIPP electrode sharing topologies

In addition to CLIPP, also heaters may share common electrodes when layout simplicity is a concern. Figure 2.7c shows an example in a cascade of 4 MRRs, reducing the required bonding pads from 16 to 10. When space is an issue, as in small size MRR or in Mach-Zehnder interferometer (MZI) [78], one of the electrodes already available to access the heater can be used also to access the CLIPP by profiting



(a) (b)

Figure 2.8 – *Photo of an optimized layout with multiple CLIPPs with no-fill areas around the devices and on the sides of the electrical connections.*

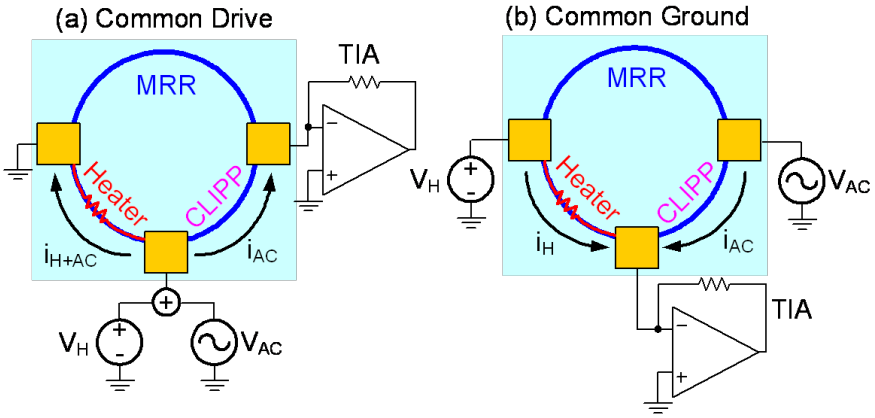


Figure 2.9 – *Comparison between two possible electrode-sharing topologies between the heater and the CLIPP: (a) common driving electrode vs. (b) common ground electrode.*

from the two signals being spectrally decoupled. As illustrated in Figure 2.9, this solution can be implemented in two ways.

In the common drive topology (Figure 2.9a) the sum of the V_{AC} signal for the CLIPP excitation and the V_H signal for the heater is applied to the middle pad, while the companion pads are separately grounded. The advantage of this scheme is that the TIA does not need any modification and can be optimized to amplify the CLIPP signal. The disadvantage is that the V_{AC} excitation is applied also across the heater: if the frequency f_{AC} falls within the response bandwidth of the heater (that can reach the MHz range), an undesired modulation can be induced.

In the common ground topology (Figure 2.9b) the common middle pad is connected to the virtual ground of the TIA and the other pads are used to drive separately the CLIPP and the heater. The price of this solution is a more complex TIA that, in addition to the AC current signal (in the nA range) from the CLIPP, must also handle the large (typically in the mA range) DC current of the heater.

Note that in both configurations the noise of the V_H generator is injected also in the CLIPP path, thus requiring a well filtered V_H generator in order to minimize the noise at f_{AC}. Furthermore, in the common ground configuration the thermal noise of the heater resistor ($\frac{4kT}{R_{heater}}$) is an additional noisy current source to be considered in the design of the TIA. Consequently, if the f_{AC} signal is not excessively perturbing the heater, the common drive configuration is preferable. The common drive solution also allows to share a wide common ground track for the heaters.

As a last consideration, the minimum distance between the heater and the CLIPP is dictated by the thermal cross-talk. Thermal simulations are required to evaluate the amount and the speed of thermal gradients in the waveguide under the CLIPP during the operation of the heater in the case of highly packed devices [79, 80]. However, given a thermal sensitivity of $\sim 1\,\mathrm{nS}/^{\circ}\mathrm{C}$ for the conductance of Si waveguides [65], a few tens of µm of separation are typically enough to make negligible the effect of heaters dissipating tens of mW.

CHAPTER

THREE

EMBRACING CLIPP

I present the design of an new CLIPP architecture, called *Embracing CLIPP*, that exploits the possibilities offered by *active* Silicon Photonic fabrication processes. The improved device has been designed, fabricated and characterized within the context of the European Project ICT-STREAMS. A discussion of the measurement results concludes the chapter, along with some suggestions for additional improvements and future experiments.

3.1 Introduction

The previous chapter analyzed in detail the different aspects that lead to an optimized CLIPP design, from the basic parameters and parasitic components to the layout guidelines for dense optical chips. However, the structure of the device has never been altered from the two simple flat metal electrodes that was presented in the first paper on the CLIPP [65]. Such a simple structure has many advantages, because it is compatible with the standard CMOS processes of the electronic industry and can be implemented without any issue on virtually any photonic process.

Simple photonic manufacturing processes usually have one or two metal layer, with the lower one being a higher resistive material dedicated to the fabrication of thermo-optical actuators. Tungsten heaters have been successfully integrated with CMOS compatible back-end fabrication processes [81]. Figure 3.1 shows a typical stack of a Silicon Photonic process with two metal layers. The CLIPP elec-

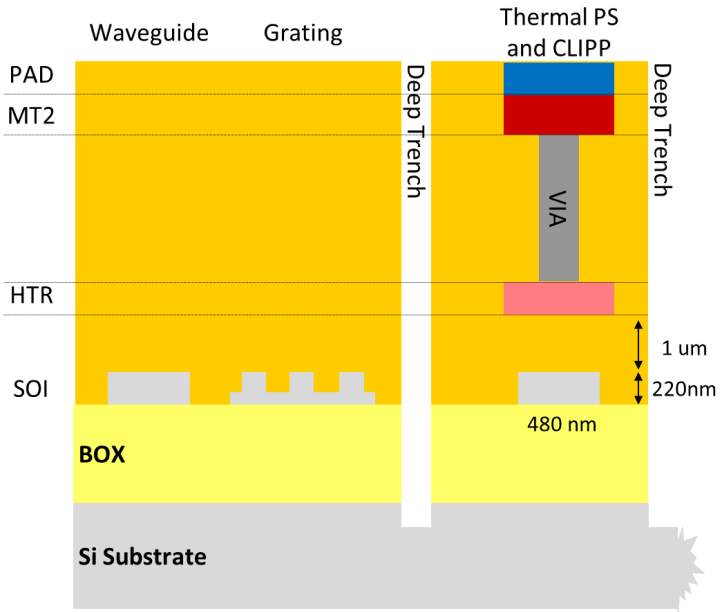


Figure 3.1 – *Typical stack of a simple SOI photonic technology. The first metal layer (HTR) is dedicated to thermo-optical actuators but can also be used to fabricate the CLIPP electrodes, to exploit the smaller distance from the waveguide. MT2 is the second layer of metal and should be used for routing the signals.*

trodes should be fabricated with the lowest Metal layer to improve the capacitive coupling to the waveguide, increasing C_A and lowering the optimal readout frequency f_{AC} of the device (as explained in Section 2.2.1). Improving the coupling to the waveguide by using the lowest metal layer available is worth even if the material has a high sheet resistance. If the electrode of the CLIPP is designed with a very thin width (W), the resistance along the electrode might become important and the CLIPP design might require a more complicated electrical model. To avoid this, it is sufficient to use more vias to connect multiple points of the electrode to the low-resistance routing layer above.

Metals are not the only material that can be used to manufacture the electrodes of the CLIPP: in principle, any conductive material can be used thanks to the simple working principle of the device. Silicon Photonic *active* processes (Figure 3.2) include many additional fabrication steps to offer a wider variety of optical devices, such as germanium photo-detectors and ring modulators with integrated carrier-depletion effect actuators for Gb/s modulation. In particular, heavily doped n++ and p++ silicon implantations at the same height of the waveguide are available in IMEC technology [82] and, being very conductive with a sheet resistance of about 50 Ω/□, can be used as CLIPP electrodes.

3.2 | Design

The idea is to exploit the heavily doped n++ silicon implantations as an extension of the standard flat electrodes of the CLIPP. While the top electrode is 2 µm distant from the waveguide, the implantations can be placed much closer, down to a minimum distance of 300 nm. By connecting the implantations to the top metal electrode, it is possible to create an enclosing electrode, thus enhancing the capacitive coupling with the waveguide. Due to the peculiar design of its electrodes, this variant of the original CLIPP structure has been called *Embracing CLIPP*.

The increased C_A obtained with the embracing electrodes allows a reduction of the optimal working frequency f_{AC}, as explained in the Section 2.3. This improvement is beneficial to achieve a higher Signal-to-Noise Ratio (SNR), because the TIA of the readout electronics shows a lower current noise at lower frequencies. Another possibility

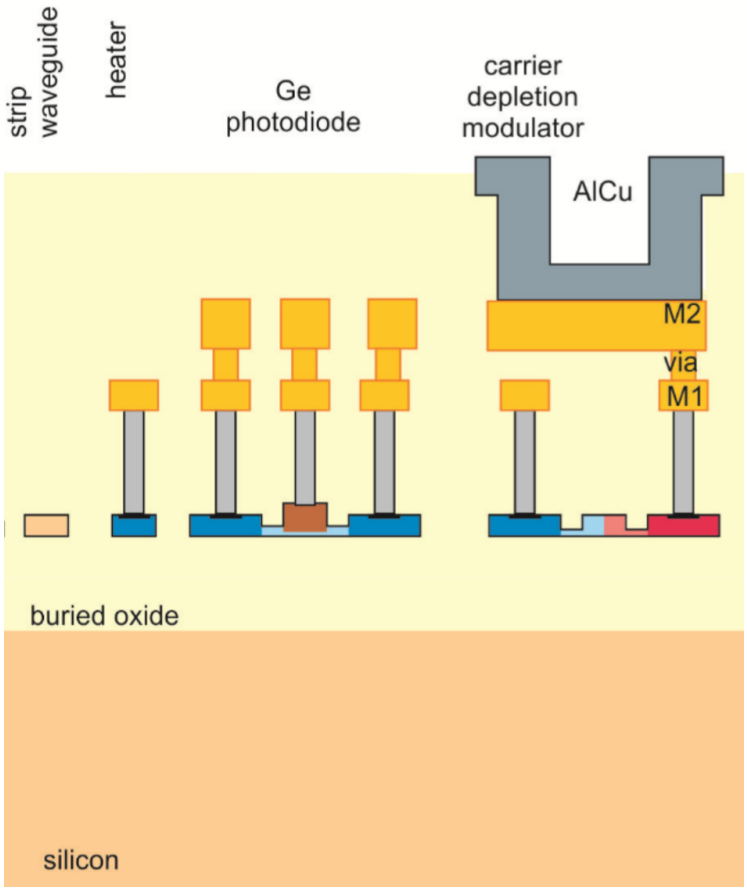
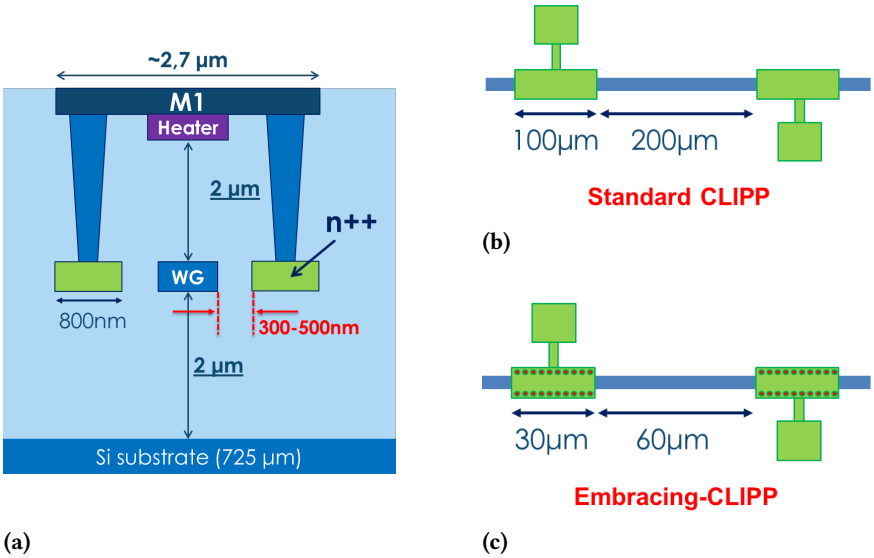


Figure 3.2 – *Typical stack of an* active *Silicon Photonic fabrication process. They usually feature one or more metal layers for routing (M1 and M2), the possibility to integrate Ge photodiodes (Section 1.3.1) and carrier depletion modulators. Both of these components require deep implantations (n++ or p++) at the same level of the waveguide that can be exploited as CLIPP electrodes.*



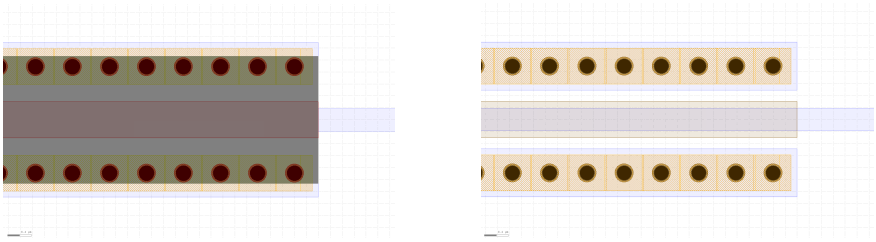
(a) (b) (c)

Figure 3.3 – *Embracing CLIPP. (a) Cross-section view of the Embracing electrode. (b) (c) compare the top view of the Standard CLIPP and Embracing CLIPP respectively.*

is, instead, to keep the same optimal frequency by reducing the total length of the CLIPP accordingly, allowing the device to fit in smaller optical components.

Figure 3.3a shows the cross-section view of the Embracing CLIPP electrodes, where two n++ implantations are placed on either side of the waveguide for the whole length of the electrode. The implantations are connected directly to the metal layer M1 with a comb of vias, to create a a C shape that encloses the waveguide. Figure 3.4 shows the comb of vias from the layout file *.gds*: in principle, a single elongated via could have been used but employing standard components offered by the manufacturing facility ensures consistent and reliable fabrication results.

The implantations are fabricated in the same technological step of the silicon waveguides and are heavily doped, n-type or p-type, later in the process. As such, they could be designed very close to the waveguide, down to 100 nm to 150 nm like the couplers of common ring resonators and multiplexers. The objective, however, is to design a variant of the CLIPP that is still completely non-invasive and it is better more conservative distance > 300 nm. However, since the



(a) (b)

Figure 3.4 – *Detail of the layout* .gds *file of the Embracing electrode: (a) and (b) show the layout with the metal layer M1 visible (in semitransparent black) and hidden, respectively.*

electrodes approach the waveguide from the side, it is safer to design the implantation closer than what was shown in Figure 2.4. This is because the fringing field is more contained horizontally rather than vertically due to the rectangular shape of the waveguide.

The width of the implantation has to be designed as thin as possible to reduce the coupling C_B of each electrode towards the substrate. Unfortunately, the minimum width is limited by the presence of the vias that occupy a square of 600×600 nm and require a margin of 100 nm. The minimum width with IMEC technology is, therefore, 800 nm.

3.3 | Fabrication

The IMEC fabrication run within the context of the European project ICT-STREAMS, offered the possibility to allocate some space for test structures of the CLIPP. The structures included in the IMEC run featured two different CLIPP architectures, each implemented multiple times varying their main parameters:

- The traditional CLIPP structure has been integrated to study the performance of the sensor in IMEC technology. It was important to verify the CLIPP working principle on the IMEC technological platform, different from the ones tested in the past for the supported wavelength of the optical signal (1300 nm instead of 1500 nm) and other technological parameters. These CLIPP differ from the overall length (400 nm and 120 nm), the ratio between the length of the electrodes and their spacing

(1/6, 1/2, 3/2, 7/2), the width of the electrodes (1 µm, 2 µm, 5 µm and 20 µm), to study the impact of these parameters on the performance of the sensor.

- The Embracing CLIPPs have been designed in two lengths (400 nm and 120 nm) with three different gaps between the implants and the waveguide (500 nm, 400 nm and 300 nm).

The layout of the test site, shown in Figure 3.5, is composed by multiple straight waveguides accessible by grating couplers with two or three CLIPPs each. The design shows how the experience from previous realization has matured, following all the layout guidelines discussed in Chapter 2. The Force lines are shared among groups of CLIPPs, while the Sense traces are kept as far as possible and immediately travel away from the nearest *Force* path. The pads are positioned to keep the bondings as far away as possible from the Forcing signal that is routed to the opposite side of the chip. Additionally, the CLIPPs have a large no-fill zone that removes the tiles closer than ~ 30 µm, while the Force and Sense connections have two smaller margins of 8 µm and 3 µm respectively. The design optimization was extremely successful in reducing the parasitic capacitance C_E, that was measured from 1 fF to 5 fF for every CLIPP of the array, compared to the hundreds of fF from previous designs.

3.4 | Experimental results

3.4.1 | Testing Procedure

The testing procedure of the CLIPPs, here explained, is a complete series of characterization measurements aimed at assessing the behavior of the device in response to optical power. In particular, the evaluation analyzes the impedance spectrum of the CLIPP and how it is modified by the presence of light in the waveguide. From the spectrum plots it is possible to identify the presence of a *plateau*, the best readout frequency and the sensitivity range of the device.

Each CLIPP is tested with the following procedure:

a) A *Force* signal of given amplitude and variable frequency is applied to one of the electrodes of the CLIPP, while the other one is connected to the virtual ground of the preamplifier stage of a Lock-in Amplifier. The forcing signal amplitude is chosen as the

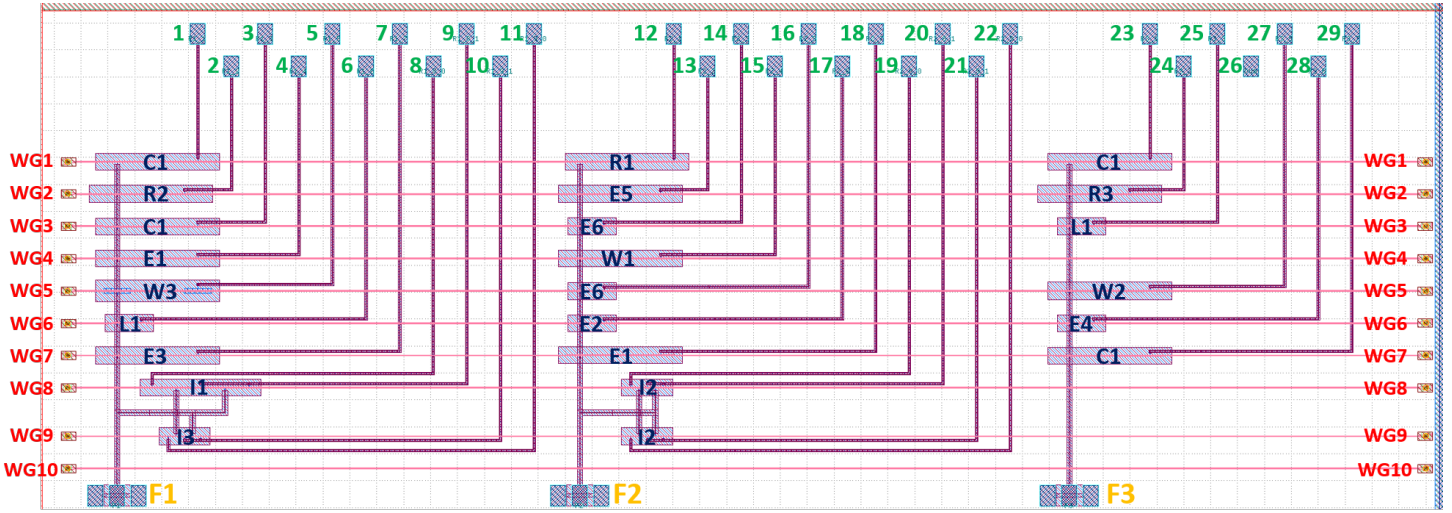


Figure 3.5 – *Layout of the CLIPP test sites. Three columns of CLIPPs with different characteristics and features to be tested and compared. CLIPPs marked as "C1" and "L1" are the traditional CLIPP structure with L : 2D ratio and overall length of* 400 nm *and* 120 nm*, respectively. The R1, R2, R3 series are CLIPPs with different L : D ratios (*1 : 6, 3 : 2, 7 : 2*). W1, W2 and W3 are traditional CLIPPs with different electrode widths (*1 µm, 5 µm *and* 20 µm*). E1, E2, E3, E4, E5 and E6 are Embracing CLIPPs of two lengths (*400 nm *and* 120 nm*) with three different gaps between the implants and the waveguide (*500 nm, 400 nm *and* 300 nm*). I1, I2 and I3 are a Interdigitated CLIPPs, smaller CLIPPs put in parallel with common Force and Sense electrodes.*

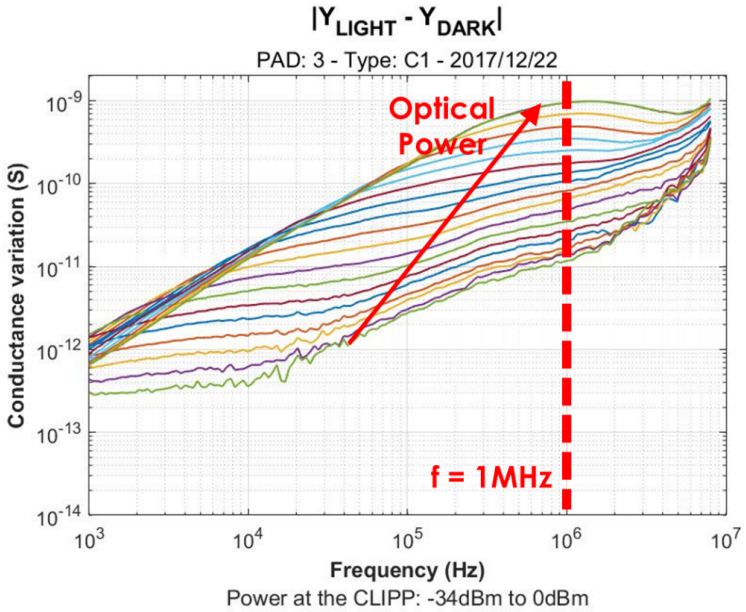


Figure 3.6 – *Conductance variation spectra, calculated as* $|Y_{LIGHT} - Y_{DARK}|$*, at increasing optical power in the waveguide of a Standard CLIPP of total length* 400 µm *(*$L = 100\,\mu m$*,* $D = 200\,\mu m$*,* $W = 2\,\mu m$*). The plot highlights the best readout frequency to maximize the output signal.*

maximum possible value without saturating the output of the amplifier. This ensures the best results in terms of sensitivity.

b) A frequency sweep of the *Force* signal (usually between 100 kHz and few MHz) is performed and the output of the Lock-in demodulator is acquired, effectively measuring the admittance spectrum of the CLIPP. This first measurement is done without any light power in the waveguide and represents the reference *"Dark Spectrum"* of the CLIPP.

c) The admittance spectrum measurement is repeated multiple times with different light power intensities.

d) The reference *"Dark Spectrum"* is subtracted from each measurement performed in light condition and the result is the detected conductance variation as a function of light power and *Force* signal frequency. The subtraction between the two spectrums can be performed in few different ways: either the two

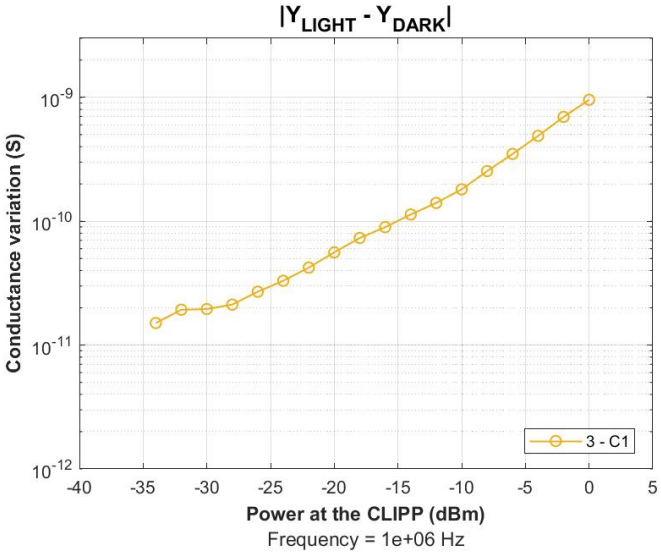


Figure 3.7 – *Conductance variation* (S) *vs Optical Power* (dBm) *of a Standard CLIPP of total length* 400 µm ($L = 100\,\mu m$, $D = 200\,\mu m$, $W = 2\,\mu m$).

complex number are subtracted and the absolute value of the result is analyzed ($|Y_{LIGHT} - Y_{DARK}|$), or only the real parts are subtracted ($Re\,(Y_{LIGHT}) - Re\,(Y_{DARK})$). This ultimately depends on how the acquisition is done by the system that follows the electronic front-end. In general, the absolute value of the difference of the complex numbers gives the best results, as it gathers the effects of the light on both components of the impedance. However, it requires more resources to acquire both in-phase and quadrature signals from the Lock-in demodulation. The plot in Figure 3.6, referred to a Standard CLIPP of total length 400 µm ($L = 100\,\mu m$, $D = 200\,\mu m$, $W = 2\,\mu m$), shows a typical impedance spectrum of a CLIPP as a function of the optical power and it is useful to select the best working frequency to maximize the detected signal.

e) Finally, the conductance variation at the optimal *Force* frequency can be extracted from the previous measurement and represented in a "Conductance variation (S)" vs "Optical Power (dBm)" plot (Figure 3.7), also called "Sensitivity Curve". This graph is useful to compare the performance of different CLIPPs in terms of sensitivity.

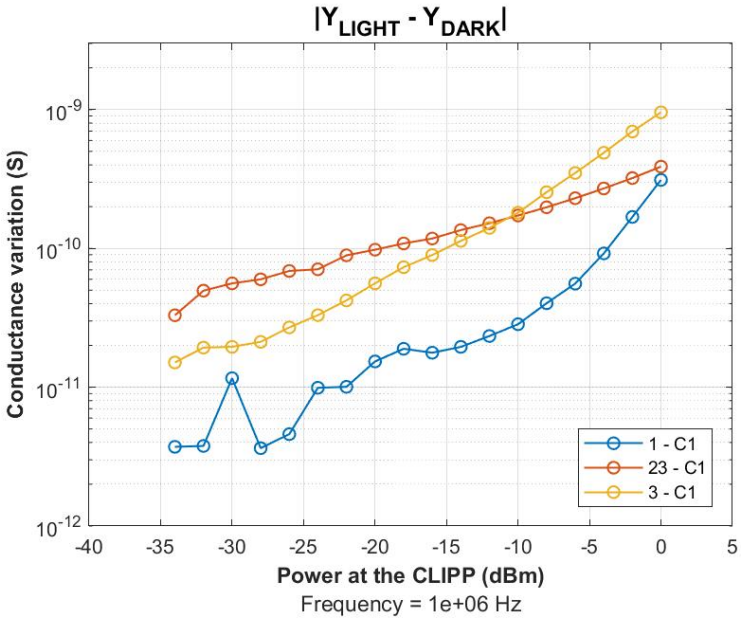


Figure 3.8 – *Sensitiviy curves of three different Standard CLIPP ($L_{TOT} = 400\,\mu m$, $L = 100\,\mu m$, $D = 200\,\mu m$, $W = 2\,\mu m$). The CLIPPs marked as "1-C1" and "23-C1" are on the same straight waveguide of the test site (Figure 3.5).*

3.4.2 | Measurement Results

Both the Traditional CLIPP and the Embracing CLIPP have been tested with the explained procedure and proved to work very well, with conductance variations from 10 pS to 1 nS with an optical power from −35 dBm to 0 dBm. However, three Standard CLIPPs ($L_{TOT} = 400\,\mu m$, $L = 100\,\mu m$, $D = 200\,\mu m$, $W = 2\,\mu m$) that have been tested show very different sensitivity curves (Figure 3.8), with discrepancies as high as one order of magnitude, despite being nominally identical from a geometrical point of view. They differ both in sensitivity (blue and yellow curves) and in exponent of the sub-linearity, that is the slope of the curve (orange, see Appendix A). A similar variability is measured when comparing different CLIPP structures and, therefore, it is difficult to distinguish the impact of the geometrical parameters on the sensor performance.

Since the sensitivity of the CLIPP is highly related to the absorption losses of the waveguide, the fiber-to-fiber insertion loss

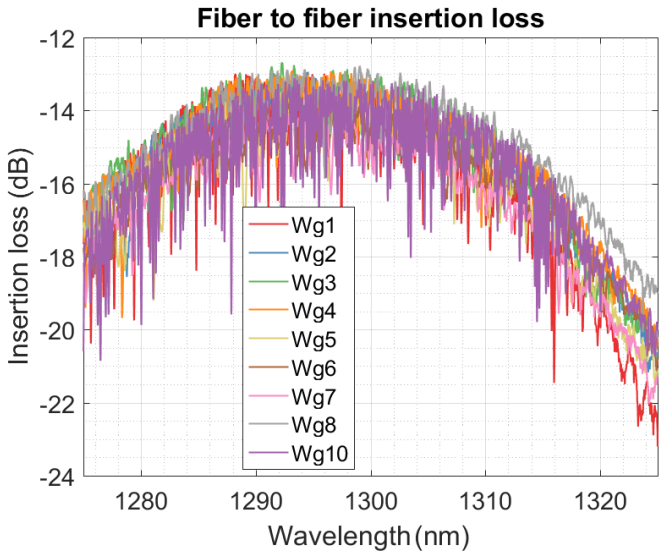


Figure 3.9 – *Fiber to fiber insertion loss spectrums of the straight waveguides of the CLIPP Test Chip.*

spectrums of the straight waveguides of the CLIPP Test Chip has been analyzed. The spectrums are very "noisy" and exhibit a high variability among the waveguides, as shown in Figure 3.9. This variability is not explained by the presence on some of the waveguides of the Embracing CLIPPs, that could in principle increase the insertion loss due to the n++ implantations close to the waveguide: the waveguide with 2 Embracing CLIPPs (WG6) has lower losses that one with none (WG1), and the reference waveguide (WG10) with no CLIPPs has higher losses than most of the others. It is also worth noting that the Standard CLIPPs on pads 1 and 23 ("1-C1" and "23-C1" in Figure 3.8) are on the same waveguide, showing that the phenomenon cannot be explained only by the variability among the waveguides. Furthermore, the CLIPP "23-C1" shows a higher sensitivity to the optical power, but it is located further away from the input grating compared to the CLIPP "1-C1", excluding the extra propagation losses as a possible explanation.

The noisy spectrums are a symptom of high backscattering losses, typical of the O-band in the order of 3 dB/cm to 3.5 dB/cm, probably due to sidewall roughness. Backscattering is not directly the phenomenon that generates a signal for the CLIPP, as the photon needs

to be absorbed and to generate an electron-hole pair to affect the conductivity of the waveguide. However, the edge roughness can increase the absorption losses through defect-mediated absorption and can be in principle different along the waveguide, leading to some variability among nominally identical CLIPPs.

Safer conclusions on these delicate technological aspects of the fabrication process might be reached in the future by measuring a higher number of CLIPPs, to build a statistical model of the device. To this aim, it is extremely important to automate every part of the testing procedure to obtain repeatable and comparable results even in the span of multiple days. In particular, a programmable optical attenuator, not available at the time of the experiments, could speed up the procedure of sweeping the light power intensity (see 3.4.1, step c) currently done manually.

Despite high process variation of the IMEC technology, confirmed by the optical characterization of the waveguides, the new and improved Embracing CLIPP showed exceptional performance. The Embracing CLIPP E5 ($L_{TOT} = 400\,\mu m$, $L = 100\,\mu m$, $D = 200\,\mu m$, $W \approx 2.7\,\mu m$), with n++ implantations at 400 nm from the waveguide, achieved the record of the lowest detectable power measured so far with a CLIPP, -55 dBm. Figure 3.10 shows the sensitivity curves, comparing the different instances of the traditional CLIPP (yellow, orange and blue) and two Embracing CLIPPs (purple and green).

3.4.3 | Light in the substrate

The superior sensitivity of the Embracing CLIPPs is partially unexpected. As explained in the Section 2.3, the increased C_A obtained with the embracing electrodes should only reduce the optimal working frequency f_{AC}. This improvement is beneficial to achieve a higher Signal-to-Noise Ratio (SNR), because the TIA of the readout electronics shows a lower current noise at lower frequencies. However, when comparing the Standard and Embracing CLIPPs of the same size, they should show the same signal variations since they access a piece of waveguide of the same length.

The characterization of the CLIPP matrix was performed with a multichannel eletronic plaform that allows to monitor multiple CLIPP signals simultaneously. During the tests, it became apparent that there was some sort of interaction between the CLIPPs. By

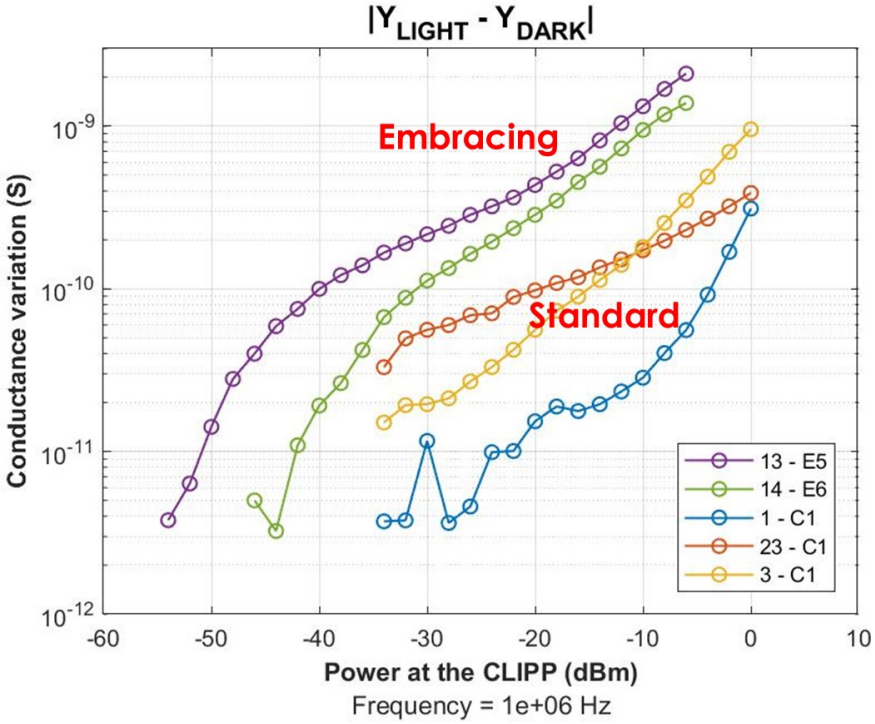


Figure 3.10 – *Comparison between the sensitivity plots of the Standard CLIPPs and Embracing CLIPP. CLIPPs marked as C1 are stardard designs with* $L_{TOT} = 400\,\mu m$, $L = 100\,\mu m$, $D = 200\,\mu m$, $W = 2\,\mu m$. *The Embracing CLIPP E5 and E6 both have implantations at a distance from the waveguide of* 400 nm *but differ for the overall length: E5 has* $L_{TOT} = 400\,\mu m$, $L = 100\,\mu m$, $D = 200\,\mu m$, $W \approx 2.7\,\mu m$, *while E6 has* $L_{TOT} = 120\,\mu m$, $L = 30\,\mu m$, $D = 60\,\mu m$, $W \approx 2.7\,\mu m$

monitoring the CLIPP signals in time and increasing the optical power emitted by the laser, an impedance variation was shown not only by the CLIPPs along the waveguide under test. Some CLIPPs on different non-illuminated waveguides shown a signal variation proportional to the light as well.

The phenomenon might be caused by the silicon substrate and in particular by the huge interface between substrate and silicon oxide where the optical devices are fabricated. When the optical signal is injected in the photonic chip, either through butt-coupling or by means of a grating coupler, the majority of the light actually fails to couple to the waveguide and scatters into the substrate instead. When this happens it is possible that the conductivity of the substrate itself is altered by the same phonomenon of Surface State Absorption (SSA), due to the interface between silicon and silicon oxide of the substrate. Since the CLIPPs are tested by modifying the power emitted by the laser, before the light is injected into the chip, the increased signal proportional to the light might be caused by the conductance variation of the substrate itself. The Embracing CLIPPs have a higher C_B due to the fact that the implantations are 800 nm wide and are closer to the substrate, therefore, they access it better than the standard CLIPPs. However, the additional current signal through the substrate should not reach the TIA if the substrate is grounded, like it was in every experiment with the IMEC chips. A possible explanation is that the grounding is not effective enough to make the impedance path through the substrate negligible, probably due to its 700 µm thickness. An insulating substrate, again, would be ideal to eliminate the problem. Alternatively, a new and more complex electrical model should be studied to optimize an updated design of the Embracing CLIPP.

3.5 | Future improvements

The high process variation of the IMEC technology, confirmed by the optical characterization of the waveguides, causes the sensitivity curve of nominally identical CLIPPs to be different. On one hand, this variability corroborates the superior structure of the Embracing CLIPP, achieving better results despite the process variation. On the other hand, unfortunately, it impeded a detailed comparison of similar CLIPPs as a function of small variations of their key parameters

(electrode length, spacing, width...).

The phenomenon of the light in the substrate needs to be properly investigated in more detail, possibly on a chip that has more consistent optical performance:

- The signal read by Embracing and Standard CLIPPs should be compared in two different scenarios of optical power sweep. One by sweeping the power emitted by the laser itself, the second by modifying the power that reaches the CLIPP with an on-chip device: a Mach-Zehnder Interferometer or an Add-and-Drop Multiplexer based on a ring resonator. In the second case the light in the substrate should be constant.
- The technique of Pilot Tones explained in Chapter 6 can be used to reject the additional signal from the substrate, provided that the modulation is performed on-chip.
- Since the grounding of the substrate seems ineffective to minimize its impedance path, a new electrical model should be designed and studied to model the effect, like the one shown in Figure 3.11. The resistances R_G towards ground model the resistance of the substrate from the oxide interface to the ground connection on the bottom of the chip. Additionally, both R_G and R_{sub} could be made dependent on the optical power in the substrate. COMSOL and Matlab simulations can be an useful tool to validate the new model and to compare it to the experimental measurements. If the model proves effective in describing the behavior of the CLIPP, a new optimization of the device structure is possible to improve the CLIPP sensitivity and reduce the parasitic effects.

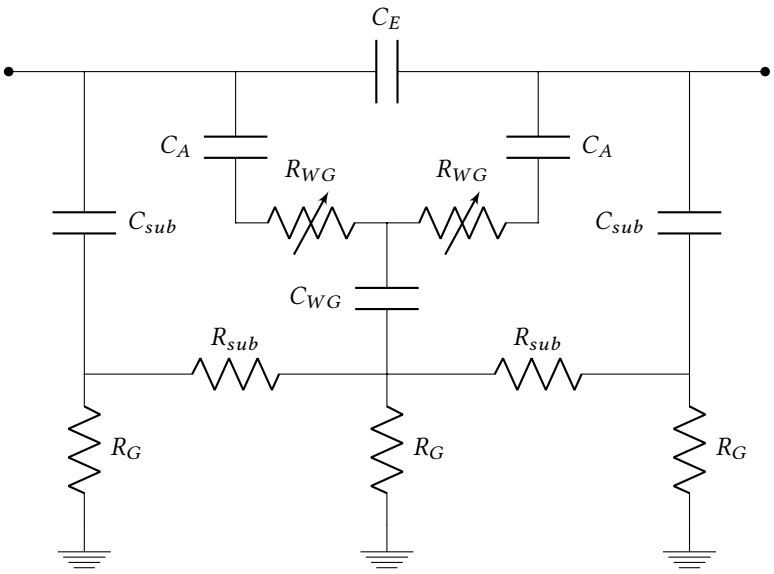


Figure 3.11 – *Proposition for a new equivalent electrical model of the CLIPP detector. The resistances R_G model the thickness of the silicon substrate, that is usually grounded only at the bottom. Both R_{sub} and R_G could be made dependent on the optical power present in the substrate and taken into account as a spurious contribution. C_{WG} is added to evaluate the behavior of the waveguide as a transmission line, with a T-shape equivalent model.*

Part II

The Electronics

CHAPTER

FOUR

ELECTRONICS FOR CLIPP-MONITORED PHOTONIC SYSTEMS

4.1 Key aspects of the CLIPP readout design

4.1.1 Lock-In Technique

The information that needs to be extracted from the CLIPP is the real part of its impedance, measured at a frequency f_{AC} higher than the pole given by the access capacitance C_A and the resistance R_{WG} of the waveguide (as shown in Section 2.3). The readout scheme has to be selective both in frequency and in phase: the Lock-In technique (Figure 4.1) qualifies as the best approach for the job, as already anticipated in Section 2.1.

The measurement is performed by applying a sinusoidal *"Force"* signal $V_E = V_e \cos(2\pi f_{AC} t)$ to one of the electrodes of the CLIPP. The other electrode is connected to the virtual ground of a Trans-Impedence Amplifier (TIA) and kept fixed in voltage by the feedback loop. The configuration converts the current flowing through the different impedance paths of the device into a voltage signal. The amplification is set by the components in the feedback path of the amplifier, being, in general, a resistance R_F or a capacitor C_F. By stimulating the device above f_{min} (Section 2.3), the access capacitances C_A are effectively short circuited, and a current flows through the waveguide, proportional to its impedance. At the same time, two other unwanted contributions flow to the virtual ground of the TIA: the current through the parasitic capacitance C_E and the one

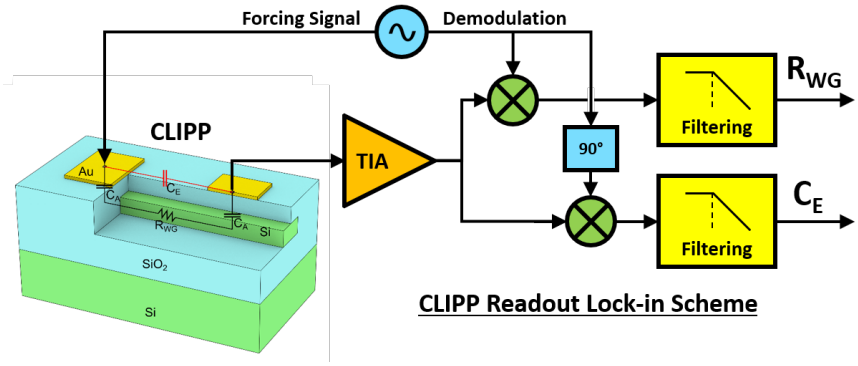


Figure 4.1 – *Readout scheme of the CLIPP detector based on a Lock-In demodulation, both in phase and in quadrature, to extract the real and imaginary part of the impedance.*

through the substrate $C_B - R_{sub} - C_B$. However, the major parasitic component, the one due to the capacitance C_E is 90° phase-shifted to with respect to the wanted signal and can be filtered out thanks to the Lock-In technique.

The voltage signal at the output of the amplifier is demodulated both in phase and in quadrature by two mixers, driven at the same frequency f_{AC} of the *Force* signal. In this way, the amplitude of the sinusoidal signal is extracted moving to base-band the information on the impedance. The parallel demodulation in phase and in quadrature allows the extraction of both the value of the real and imaginary part of the impedance. After the mixers, two Low-Pass-Filters (LPF) eliminate the residual oscillations due to the stimulation frequency f_{AC} and its harmonics, providing two stable and slowly varying voltage signals that represent the quantities of interest.

The Lock-In technique, in addition, minimizes the effects due to the amplifier offset and flicker noise, because these two factors are at low-frequency and interact with the wanted signal when it is still modulated. As a result, they are ideally eliminated by the mixer and the following filtering stage.

Finally, a proper design of the bandwidth of the two Low-Pass-Filters (LPF) limits the integrated bandwidth of the white noise at the output, enabling the detection of extremely small variations of the waveguide conductance, down to the pS scale.

4.1.2 | Noise optimization

The design of the TIA is very critical because it has to introduce the lowest possible noise to boost the sensitivity of the system. At the same time, it needs to ensure a wide enough bandwidth to operate CLIPPs that require different *Force* frequencies depending on their geometry.

The simplest structure of the TIA, based on a single feedback resistor, is not suitable to satisfy these requirements. A feedback resistor R_F determines both the equivalent input current noise ($4kT/R_F$) and the bandwidth of the system due to its parasitic parallel capacitance ($BW \approx \frac{1}{2\pi C_F R_F}$).

A more advanced circuit topology for current amplifiers, based on a feedback capacitor C_F, can be used to relax the speed-vs-resolution trade-off affecting the basic TIA configuration with resistive feedback. Due to the prominently capacitive nature of the CLIPP equivalent impedance, a TIA with capacitive feedback can achieve a frequency independent gain ($G \approx \frac{C_E}{C_F}$) and wide bandwidth ($> 10\,\text{MHz}$). At the same time, the capacitance C_F, being a noiseless component, improves the resolution of the measurement. The disadvantage of a capacitive feedback is that it requires a DC handling network, to deal with DC leakage currents that would saturate the amplifier and to properly bias the stage in DC.

The way the electrodes of the CLIPP are connected to the electronics is also crucial in terms of achievable sensitivity. In order to minimize the noise, the total capacitance of the connection of the CLIPP to the TIA input must be minimized. Coaxial cables should be avoided in the most sensitive applications due to the high capacitance per unit length (6.5 pF/cm to 10 pF/cm). When a permanent connection is acceptable, bonding wires arranged as described in Section 2.4 should be preferred to the use of macroscopic spring contacts or microprobes. In order not to jeopardize the benefit of the low-capacitance bonding wires, the length of the connection from the bonding to the TIA input, typically consisting in a copper trace on a PCB, should be carefully minimized. To this purpose, the TIA (either an off-the-shelf component [11] or a dedicated ASIC [23]) can be soldered on a small PCB holder hosting at close distance both the photonic chip and the front-end components of the readout chain [10], as will be described in Section 4.2.

Finally, the noise of the Low-Pass-Filter (LPF) should be considered and compared to the output noise of the TIA, to avoid detrimental effects due to a careless design. When the filter is implemented with a simple $R-C$ network, the noise contribution is $\frac{kT}{C}$ and the capacitance should be sized to keep the noise negligible. This is generally easy when the system is realized on a board with discrete components, where C can be made as large as needed. However, the integration of the readout electronic in an ASIC can be challenging due to the large area occupation of integrated capacitors.

4.1.3 | Leakage currents

The TIA with a capacitive feedback grants a higher sensitivity at the cost of a more complex handling of the DC currents at the input node of the system.

When working with a discrete components front-end, the problem is easily fixed with a single high-value resistance R_F connected in feedback, in parallel to the feedback capacitance C_F. The value should be chosen high enough to keep its noise contribution negligible, from 100 MΩ to 1 GΩ, while keeping contained the resulting offset at the output of the amplifier ($R_F \cdot I_{leak}$).

However, when the front-end is integrated, high-value resistances are difficult to design because they occupy a large area, due to the limited sheet resistance of integrated resistors. Furthermore, they do not support frequencies higher than few tens of kHz, as they bring along large parasitic capacitances associated with the area occupation.

The problem is even more complex in an ASIC because there are multiple sources that can cause a leakage current. The amplifier itself, the protection diodes of the input pads, and other parasitic photodiodes can contribute to DC current at the input of the TIA, that needs to be handled properly.

Parasitic photodiodes can be particularly insidious because they make the offset at the output of the amplifier sensitive to the environmental light. They are unwanted p-n junctions that typically form between doped implantations (as Sources and Drains of MOSFETs) an the substrate.

The front-end ASIC and the photonic chip should be bonded directly chip-to-chip to minimize the parasitic capacitances related to

the connection. However, this hinders the isolation and the shielding of the ASIC from the environment.

The DC offset at the output of the TIA does not affect, ideally, the proper acquisition with the Lock-In demodulation scheme. Any continuous signal is simply up-converted by the mixer to the frequency f_{AC} and then filtered by the subsequent Low-Pass Filters. However, when the filtering is performed in an ASIC, it is difficult to implement narrow and steep filters and the residual modulation can saturate the following stages.

An innovative circuital solution will be described in the following Chapter 5, featuring a tunable pseudoresistor topology to synthesize a linear high-value resistance.

4.1.4 | CLIPP resolution vs response time

The response time of the CLIPP is set by the Lock-In demodulation bandwidth BW and is governed by the speed-resolution trade-off inherent to all noise-limited measuring systems. By enlarging the bandwidth, a faster response is achieved but more noise components are integrated, thus resulting in a worse resolution.

In order to experimentally explore the speed detection limits, the optical power on a straight waveguide is chopper modulated at increasing frequency (up to 10 kHz) and tracked with the CLIPP signal ($V_{AC} = 2\,\mathrm{V}$, $f_{AC} = 2\,\mathrm{MHz}$) filtered at correspondingly larger BW from 1 kHz to 40 kHz. Figure 4.2 reports the measured minimum detectable signal variation (calculated as 6 times the rms value of the measured noise) as a function of BW.

The experiments confirm that the noise decreases as $\sqrt{BW}$ as the BW is decreased (dotted line) and that a optical signal of 30 µW can be detected with a speed of 1 kHz. For very narrow bandwidths (the point at 1 Hz in the figure) other noise sources, in addition to the TIA, come into play, such as the intrinsic limitation of the lock-in detector, setting a lower limit of resolution to around 220 pS in our system. Note that the resolution linearly depends on V_{AC}, which can be increased from the used value of 2 V up to tens of volts if even better resolution than the one in Figure 4.2 is desired.

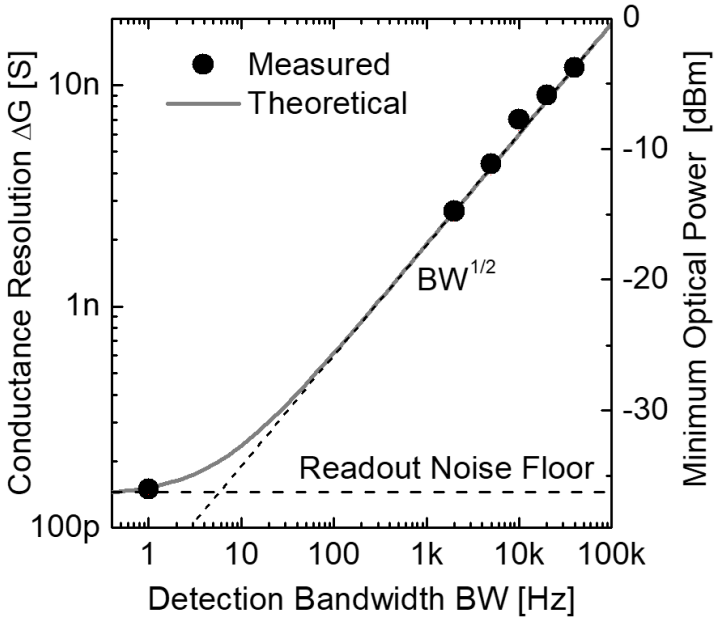


Figure 4.2 – *Diagram showing the bandwidth BW vs. resolution trade-off for a CLIPP of standard size ($L = 2D = 200\,\mu\text{m}$, $V_{AC} = 2\,\text{V}$, $f_{AC} = 2\,\text{MHz}$). Circles are the experimental points, while the dotted line is the theoretical expectation according to the TIA noise. At high bandwidth the curve increases as $\sim \sqrt{BW}$.*

4.2 | Electronic Control Platforms

The sensor readout alone is not sufficient and the system needs several additional parts to be able to control a complex photonic circuit with multiple optical devices and CLIPPs.

The system needs a brain, in the form of a microcontroller or an FPGA, to interpret the signals read from the CLIPP detectors and to act accordingly. A microcontroller is cheaper and easier to program, however, an FPGA offers superior performance when dealing with extremely parallelized and multichannel workloads.

ADCs and DACs are required to convert the signals to and from the digital domain. While in digital form, the signals can be processed by additional logic, digital filters and mixers to implement control algorithms. The data can be also sent to a Personal Computer, where a software interface monitors the signals and controls the different functions of the system.

Signal conditioning chains are required to adapt the signals coming from the analog front-end, before they can be converted by the ADCs. These usually include some additional amplifier stages and Anti-Alias filters.

Finally, the system should include the drivers to control the optical actuators and complete the feedback loops. In this section, the *Force* signal to stimulate the CLIPP detector should also be generated, in parallel to the demodulation sinusoid or square-wave for the Lock-In mixers.

4.2.1 | Discrete components boards

The easiest way to develop such complicated control systems is to design Printed Circuit Boards (PCB) with discrete components. However, the complete implementation of the functions described in the previous section usually occupy a large area, especially in multichannel applications.

For this reason, it is best to separate the electronics in two distinct boards. A small support PCB, that could be called *"Photonic Board"*, can host the photonic circuit and the first stages of the acquisition chain. The rest of the electronics can be placed on a separate board, a *"Motherboard"*, connected via flexible cables and containing the main processing unit. With this organization the *Photonic Board* can

be very compact and shaped to adapt to the optical bench or to fit in small CFP2 optical modules (Figure 4.3).

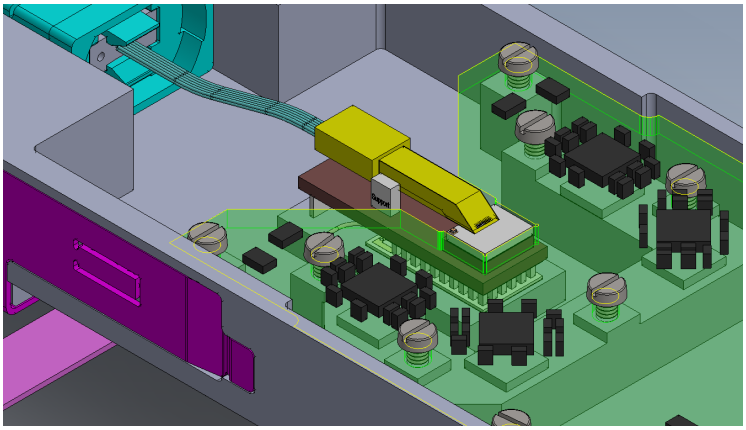
4.2.2 | Hybrid platforms

The CLIPP readout electronics, including the Lock-In demodulator, can be implemented in standard CMOS technology, as already demonstrated with a low-noise ASIC custom-designed to read 32 CLIPPs [83]. The major advantage of an integrated implementation of the readout circuit is the parallelization of several channels in a miniaturized space. This choice becomes mandatory when several tens of CLIPPs need to be simultaneously probed. Another advantage is the possibility to use small values for the capacitor components in the readout electronics, especially for the feedback element C_F. In discrete component electronics, the lowest values available on the market are 500 fF from small footprint Surface Mount Technology (SMT) components (0402). Lower values down to 100 fF are also offered by select manufacturers but have tolerances of over $50 - 100\%$. Integrated CMOS technologies allow smaller and more reliable values of C_F, down to 10 fF thanks to a specific capacitance of $1\,\mathrm{fF}/\mu\mathrm{m}^2$, achieving a higher gain ($|G| \approx 1/(2\pi f_{AC} C_F R_{WG})$) for the R_{WG} signal at the same optimal frequency f_{AC} that is set by the geometrical parameters of the CLIPP. However, a lower C_F poses some challenges on the electronic design with the bandwidth and the stability of the TIA and also requires a proportionally low C_E to avoid the saturation of the stage.

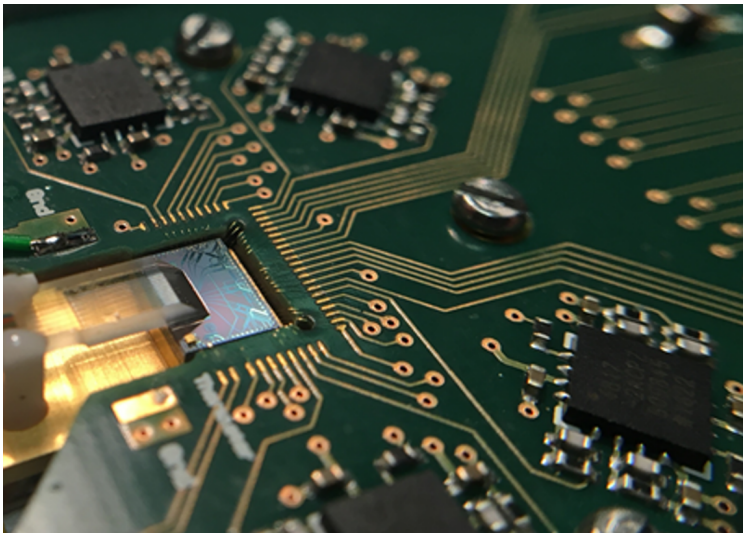
The CLIPP technology is suitable for the monolithic integration of both photonics and electronics on the same silicon chip (Electronic-Photonic Integrated Circuits, EPIC). This scenario would be optimal from the point of view of the minimization of C_E and therefore for the highest possible sensitivity. Analogously, the hybrid solution of bonding a standard CMOS chip on top of a larger photonic chip, such as in the case of copper pillars technology [84], would be suited for the readout of several CLIPPs.

However, the monolithic integration is still being actively developed [10] and the flip-chip bonding based on the copper pillars technology poses some challenges in terms of the mechanical assembly and thermal dissipation of the system.

For these reasons, the most accessible way to profit from the



(a)



(b)

Figure 4.3 – *A compact photonic board contained in a small CFP2 optical module. (a) shows the 3D model of the module, including the photonic chip, the optical connection of the fibers through an interposer, and compact TIAs made with small footprint discrete components. (b) shows a detail of the assembled module, where the photonic chip is bonded to the PCB.*

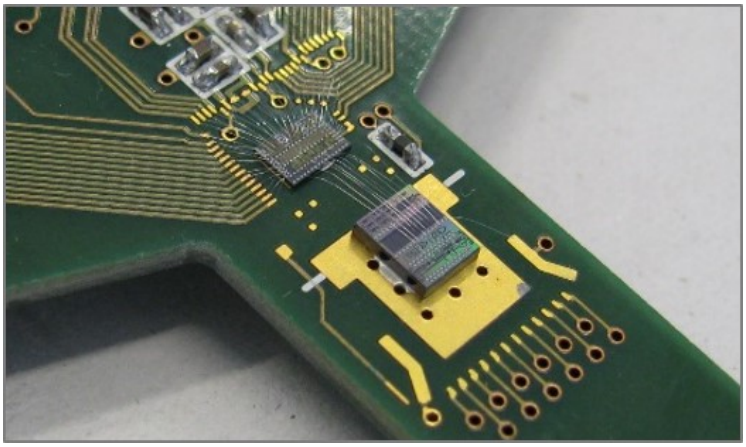


Figure 4.4 – *Hybrid integration of Electronics and Photonics on the same PCB, a Photonic board, through direct chip-to-chip wire bonding.*

multichannel capabilities of an Integrated Circuit is to connect the ASIC and the photonic circuit with chip-to-chip wire bondings on a support PCB, as shown in Figure 4.4.

Figure 4.5 shows an example of Photonic Board where the board has been shaped to fit in an optical setup with manual alignment of the optical beams. The compactness of the board itself is made possible by the use of an ASIC that includes several channels in parallel of the Lock-In Amplifier scheme. Finally, the board is connected through flexible cables (a white flat-cable is visible in the photo) to a separate motherboard, as shown in Figure 4.6.

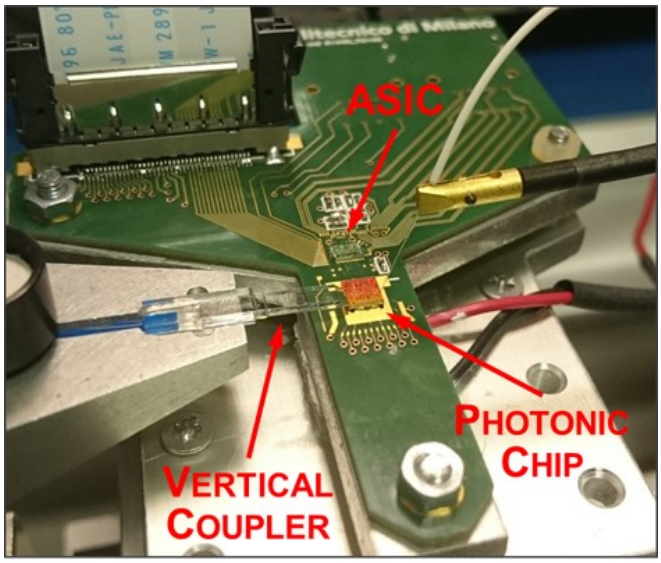


Figure 4.5 – *Photonic Board featuring hybrid integration shaped to fit the experimental bench for easy vertical optical coupling with a glass interposer and fibers.*

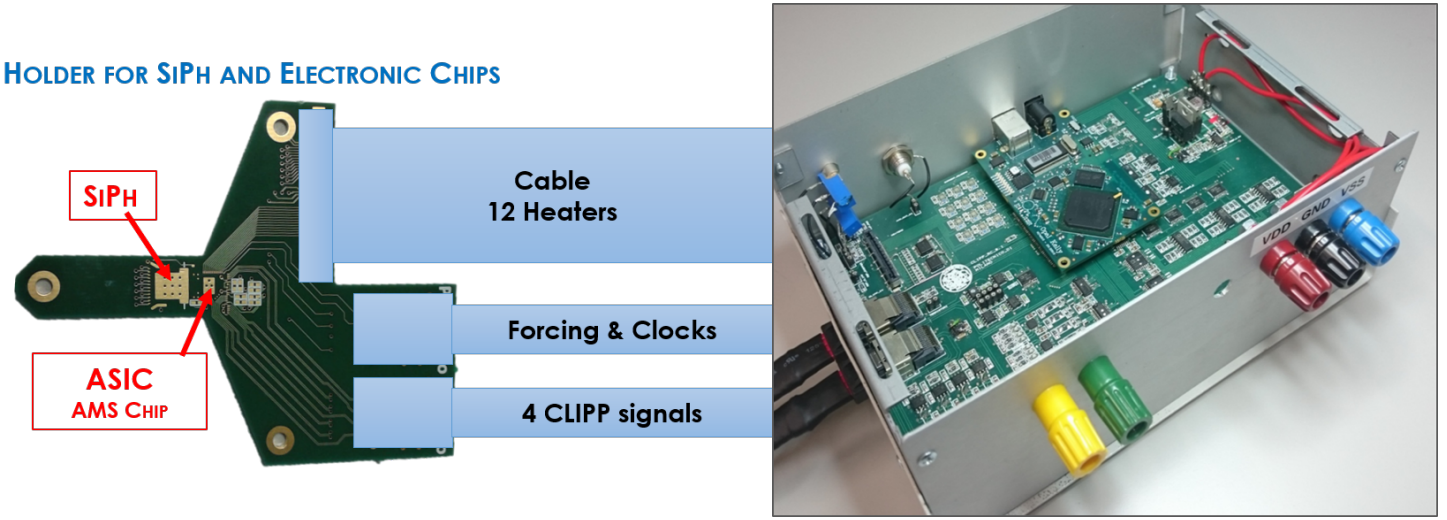


Figure 4.6 – *Connection of the Photonic board, where the low-noise analog front-end is hosted, to the main control motherboard, including the FPGA controller, acquisition chains for the conversion to the digital domain, thermal-actuator drivers, and generation of the CLIPP Force signal.*

CHAPTER

FIVE

CMOS PSEUDO-RESISTORS

5.1 | Introduction

The most important element of the readout chain for the CLIPP sensors is the first preamplifier stage, a Trans-Impedance Amplifier (TIA) that needs to convert the tiny current signal in a useful voltage signal. The TIA has to be optimized for extremely low-noise to achieve the best possible sensitivity, while maintaining a suitable bandwidth for the Lock-In technique to be used. To this aim, the TIA is designed with capacitive feedback to remove the noise component of a feedback resistor. However, the capacitive feedback requires a DC handling network to deal with DC leakage current that would saturate the OpAmp and to properly bias the stage in DC (Figure 5.1).

High value resistors are known to be difficult to be designed in standard integrated technology. This is because the minimum doping level that is available in the process workflow, below which process reproducibility may be affected, gives typical values of sheet resistance in a range from few $\Omega/\square$ to few $k\Omega/\square$. High-value resistors would, therefore, be reached only by designing long resistors, with multiple folding to keep the layout compact. In addition to size and related cost, long resistors made of hundreds of squares bring along large parasitic capacitances that degrade the frequency response of the device and impose a transmission line approach to its analysis.

In this chapter, I present an innovative tunable and highly linear pseudo-resistor based on active transistors, that has been designed,

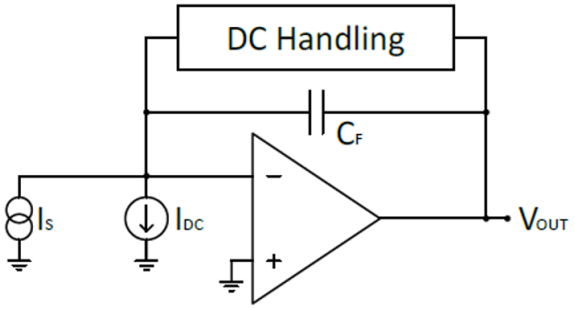


Figure 5.1 – *Schematic of a TIA with capacitive feedback, biased by a "DC Handling" network.*

fabricated and tested in AMS CMOS 0.35 µm technology. The first part of the chapter contains a didactic review of the possible pseudo-resistor architectures that can be created with few transistors, discussing advantages and disadvantages of each configuration. Follows the presentation of our implementation, including the realization of the floating voltage generators required to tune the resistance of the device.

5.2 | Single-cell Pseudo-resistors

5.2.1 | Non-tunable

The simplest way to implement a high-value pseudo-resistor is by using a single MOSFET transistor connected in trans-diode configuration, like the pMOSFET shown in Figure 5.2 [85–87]. To use this pseudo-resistor with relatively large bipolar signals, it is necessary to short-circuit the well and source terminals: the resulting device behaves as a MOSFET for $V_{AB} = V_A - V_B < 0$ and as a diode (formed between the p-type drain and n-type well) for $V_{AB} > 0$.

When operating around $V_{AB} = V_A - V_B = 0\,\mathrm{V}$ bias, the parasitic diode is off and the MOSFET operates in weak-inversion region. The small signal equivalent resistance can reach very high-values, up to the TΩ range, and can be evaluated by using the following sub-threshold equations:

$$I_{SD} = I_{SD0} \exp\left(\frac{V_{SG}}{nV_{TH}}\right)\left[1 - \exp\left(-\frac{V_{SD}}{V_{TH}}\right)\right] \tag{5.1}$$

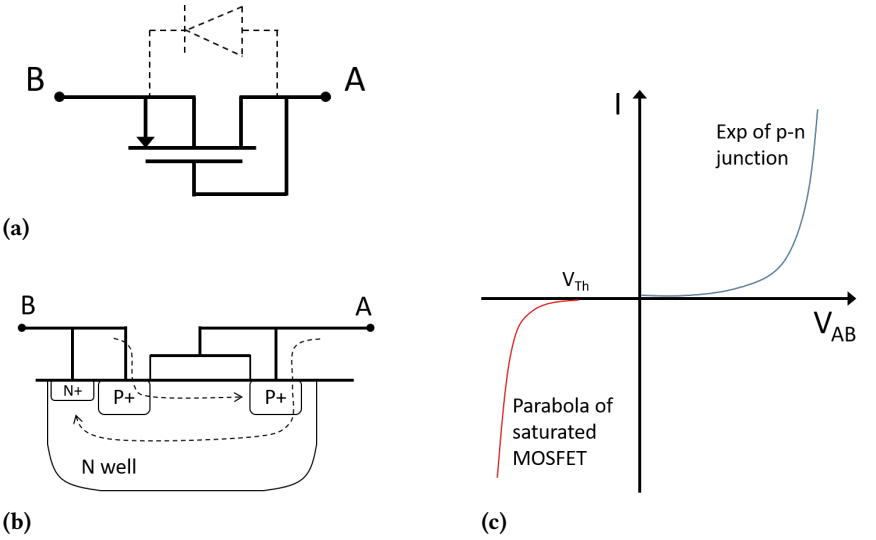


Figure 5.2 – *Single cell non-tunable pseudoresistor: (a) Schematic (b) Layout and (c) Characteristic curve*

$$r_{eq} = \left(\frac{\partial I_{SD}}{\partial V_{SD}}\bigg|_{V_{SG}=V_{SD}=0} \right)^{-1} = \frac{V_{TH}}{I_{D0}} \tag{5.2}$$

with

$$I_{D0} = 2n\mu C_{OX} \left(\frac{W}{L} \right) V_{TH}^2 \exp\left(-\frac{|V_T|}{nV_{TH}} \right) \tag{5.3}$$

where n is the sub-threshold slope, C_{OX} is the gate oxide capacitance per unit area, μ is the mobility, $V_{TH} = \frac{kT}{q}$ is the thermal voltage, $\left(\frac{W}{L}\right)$ is the aspect ratio of the transistor and V_T is the threshold voltage of the transistor.

This pseudo-resistor, being made by a single transistor, is very compact, but has an inherently asymmetric characteristic curve and shows a linear behavior only for very small signals. The resistance cannot be regulated during operation, as it is set by the technological parameters and by the dimensions chosen in the design phase, and the exact value is hardly controllable due to its sensitivity to process variations.

No conceptual difference would be present in using a nMOSFET, provided that it is enclosed in its own floating p-well and has the same connections (source-well shorted, gate-drain shorted). Being the goal to reach high resistance values, pMOSFETs are usually the

chosen option. It is worth mentioning that it is also possible to connect the well to the drain-gate contact, instead of the source. However, this effectively swaps the orientation of the parasitic diode and means that both diode and MOSFET turn on when $V_{AB} < 0$ and are simultaneously off when $V_{AB} > 0$. Furthermore, the MOSFET in this configuration is subject to the *body effect* phenomenon that lowers its threshold voltage, increasing the transistor conductivity. As a consequence, the resulting structure is even more nonlinear than the standard transdiode and is hardly useful.

5.2.2 | Fixed Gate

Lower equivalent resistances, in the MΩ and GΩ range, can be obtained by disconnecting the gate terminal of the transistor from the drain and connecting it to a fixed potential, as shown in Figure 5.3 [86–89]. In this configuration the channel resistance can be lowered and set to the required value. It is also possible to handle the high variability of the equivalent resistance of the pseudo-resistor by making the gate control voltage externally tunable during operation.

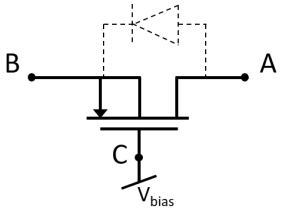


Figure 5.3 – *Fixed Gate pseudo-resistor*

The Fixed Gate pseudo-resistor is still highly asymmetric (a symmetric version has been proposed in [87, 90]) and has the added disadvantage of being a *tripole*, whose behavior depends not only on the drain-source potential difference V_{DS}, but also on gate-drain (V_{GD}) and gate-source voltages (V_{GS}). This means that the *common-mode* voltage of drain and source can greatly affect the resistance of the device and makes this structure more difficult to use where a simple high-resistance element is needed.

5.2.3 | Tunable

The resistance of the pseudo-resistor can be modified by imposing a voltage difference between the channel and the gate, thus affecting the conductivity of the channel. To this aim, a *floating voltage generator* can be placed either between gate and drain or between gate and source-well. A floating voltage generator keeps the de-

vice conceptually a bipole and ideally allows to tune the resistance independently from the absolute voltage of source and drain. The behavior of the tunable structure in its two variants is better understood by considering the MOSFET and the well diode separately.

The orientation of the well diode is decided by shorting the well contact to one of the two terminals (source or drain) of the transistor. For example, like in Figure 5.4a, the connection between the well and Node B creates a p-n junction (Figure 5.4c) with Anode and Cathode at Node A and Node B, respectively. Given this orientation, an exponential current flows in the diode when $V_{AB} > 0.7\,\mathrm{V}$, while it is limited to the leakage current I_B when $V_{AB} < 0$. This behavior is not affected by the additional floating voltage generator, that only affects the gate potential with respect to the transistor channel.

The behavior of the transistor, instead, is greatly affected by the floating voltage generator, as it determines the working region of the transistor among weak, moderate and strong inversion. The first variant has the voltage source placed between the gate and Node A (Figure 5.4a and 5.4c). Note that the symbol does not explicitly mark the source of the transistor, because source and drain can swap depending on the polarity of the applied differential voltage. When $V_{AB} > 0$, the current flows from A to B and the source of the transistor is at node A. The pMOSFET works in the chosen inversion region, with a set V_{SG}, starting a from Ohmic regime for small voltage differences and showing a saturating behavior when the voltage difference increases over a certain threshold: $V_{AB} > V_G$ for strong inversion, $V_{AB} > 4V_{th} \approx 100\,\mathrm{mV}$ for sub-threshold regime. If $V_{AB} < 0$, the current flows in the opposite direction (from B to A) and the source of the transistor is at node B. In this case, the gate-source voltage difference is no longer set by the voltage generator and current increases quadratically with the voltage V_{AB}. It is worth noting that the MOSFET reaches strong inversion for high V_{AB} even if it is initially biased in sub-threshold regime by the floating generator.

The second variant, represented in Figure 5.4b and 5.4d, has the floating voltage source between the gate and Node B [87–89]. The behavior of the MOSFET in this case is completely symmetrical to the one just explained.

The mayor difference between the two structures is how the current contribution of the diode and the transistor sum up. When the diode turns on, it dominates the quadratic or saturating behavior

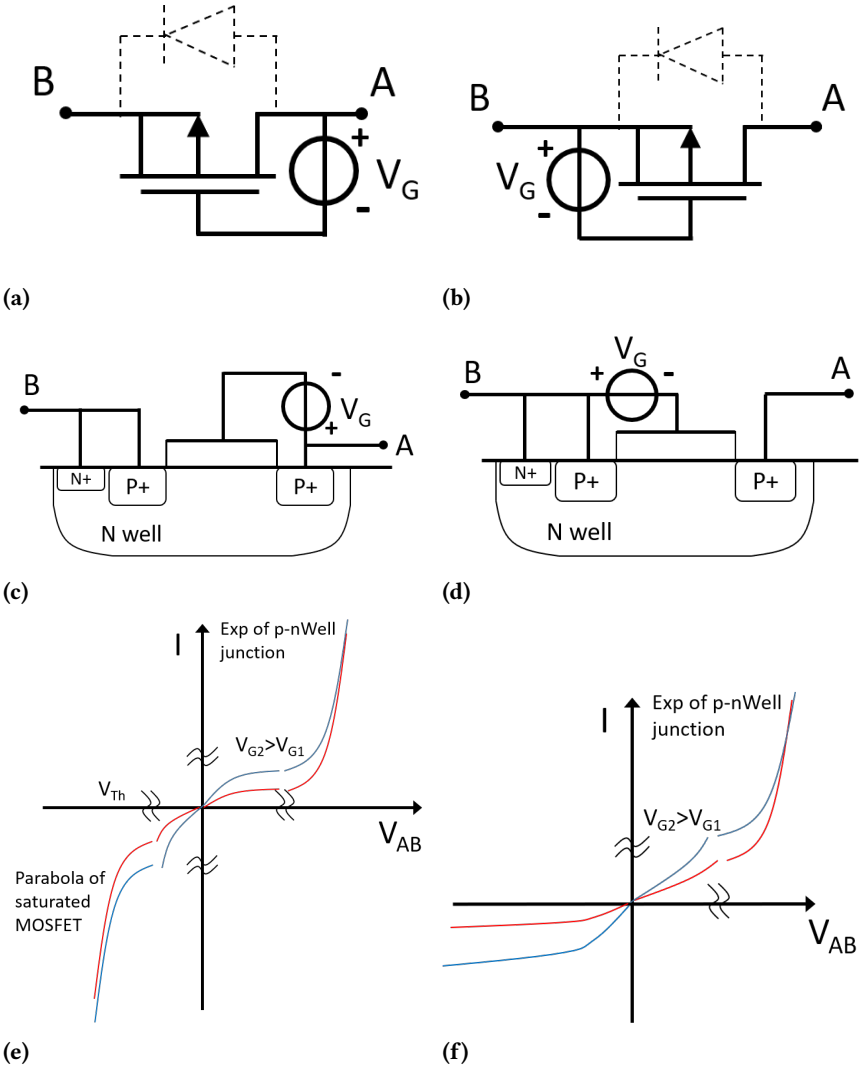


Figure 5.4 – *Two variations of the Tunable pseudo-resistor cells with the floating voltage source placed at either side of the transistor. The left column (a), (c) and (e) show Schematic, Layout and Characteristic curve of the variant with the generator connected to Node A. The right column (b), (d) and (f) have the generator connected to Node B.*

of the MOSFET and, depending on how the two are connected, the overall characteristic curve changes. Figure 5.4e and 5.4f show the resulting characteristic curves of the two pseudo-resistor variants. In Figure 5.4e, the diode dominates the saturating behavior of the transistor when $V_{AB} > 0.7\,\mathrm{V}$, considerably changing the overall response of the device. In Figure 5.4f, the diode still dominates when $V_{AB} > 0.7\,\mathrm{V}$ but the transistor current already has a quadratic growth and the concavity of the curve is not affected. When $V_{AB} < 0\,\mathrm{V}$, the MOSFET defines the behavior of the device since the diode is off and its leakage current is negligible.

The floating voltage generator is crucial to allow the tunability of the resistance of the pseudo-resistor and only affects the MOSFET behavior by changing its channel conductivity. The effects of a larger bias V_G of the generator are shown in blue (compared to the red curve) in Figure 5.4f and 5.4e. While the impact on the saturation current of the MOSFET is evident, it also reflects in a variation of the resistance of the pseudo-resistor for small symmetrical oscillation of V_{AB} around $V_{AB} = 0\,\mathrm{V}$.

Both structures presented in this section are still very asymmetric [88]. The variant of Figure 5.4b, in particular, has really different behaviors for two opposite polarities of the differential voltage: saturating on one side and exponential on the other. Furthermore, the MOSFET is affected by the *body effect* when it turns on, for $V_{AB} > 0$, due to the well not being connected to the terminal that acts as a source. To really profit of the unbeatable compactness and design flexibility of these simple MOSFET-based devices, the architecture should be elaborated further.

5.3 | Symmetric Pseudo-resistors

A symmetric pseudo-resistor structure has several benefits. First, it has the same response for both positive and negative currents, a desirable behavior for resistive bipoles. Second, the symmetric characteristic curve suppresses the generation of even-order harmonics, when stimulated by a sinusoidal signal around the $V_{AB} = 0\,\mathrm{V}$ bias. This also avoids the flow of a spurious continuous current that is a component of the even-order harmonics.

The elementary building blocks presented in the previous Section 5.2 can be mirrored in series or in parallel, to recover symmetry.

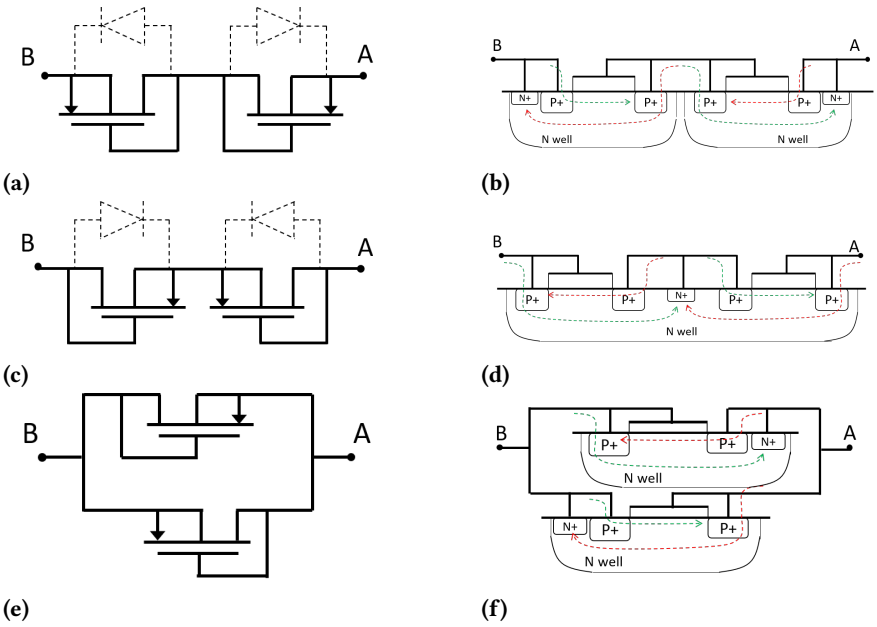


Figure 5.5 – *Symmetric pseudo-resistors based on non-tunable cells, with the schematic on the left column and the corresponding layout on the right column.*

When they are connected in series, the current is set by the least conductive element. Instead, when they are connected in parallel, the current is the sum of each element in the structure.

In the following, the possible combinations of non-tunable and tunable cells are shown and discussed, highlighting the major advantages and drawbacks in terms of layout, dynamic range, linearity and frequency behavior.

5.3.1 | Non-tunable

Figure 5.5 shows three different alternatives to build a symmetric structure with the non-tunable pseudo-resistor cell of Figure 5.2:

(a-b) The series of two elementary cells connected gate-to-gate [86, 87, 89], where the two wells are independent and operate at different voltages, one at the potential of Node A and the other at the potential of Node B. Since the differential voltage applied to the structure splits between the two cells, the dynamic range is roughly doubled. Furthermore, the frequency behavior of

this pseudo-resistor is only minorly impaired because the large parasitic capacitances of the two wells toward the substrate are voltage driven directly by the A and B nodes.

(c-d) The series connection of two elementary cells mounted well-to-well [86, 87]. In this case, the n-type wells can be shared between the two MOSFETs, leading to a more compact layout. As a drawback, the potential at the internal node also modulates the voltage of the well. Consequently, the capacitive coupling to the substrate introduces a pole that affects the frequency behavior of the device. Due to the high resistance of the pseudo-resistor cells in the structure, the pole is likely to limit the use of this structure to very low-frequency applications. The dynamic range is still increased like in the previous structure.

(e-f) Two mirrored cells connected in parallel. Differently from the previous two cases, this realization does not improve the dynamic range and still requires two separate wells, but has the advantage of a higher bandwidth thanks to the absence of internal nodes.

5.3.2 | Tunable

The tunable pseudo-resistor cells also benefit from the series and parallel implementations, but there are six combinations due to the two possible connections of the floating voltage generator.

The advantages and disadvantages of the different architectures will be discussed in the following paragraphs, focusing on the sub-linear or super-linear behavior of each configuration. This is particularly interesting for the series configurations, as the composite device retains the I-V curve of the cell with the *lowest current*. Choosing the best type of non-linearity might be essential depending on the specific application. When the pseudo-resistor is used as a feedback element of a Trans-Impedance Amplifier, the non-linearity reflects on the offset that a signal would induce when applied over a bias different from $V_{AB} = 0\,\mathrm{V}$, as highlighted in the following paragraphs.

Sub-linear Series Structures

The two possible series configurations using the single tunable cell from Figure 5.4b are shown in Figure 5.6. Being V_{SG} fixed, the overall

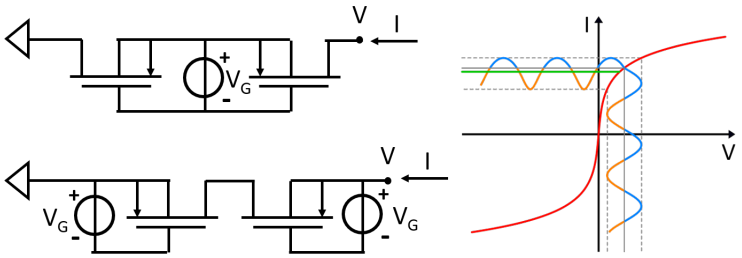


Figure 5.6 – *Possible series combinations of the elementary pseudo-resistor tunable cells, exhibiting a sub-linear behavior.*

current flowing in the Pseudo-Resistor tends to the saturation current I_{DSS} of the MOSFET with that V_{SG}. Since the current is always limited in value by one of the two transistors, the composite structure globally shows a symmetric and sub-linear behavior.

The resistance of the device when biased at $V = 0\,\text{V}$ is very linear, thanks to the symmetric structure, and its value can be tuned by setting V_{SG}. Instead, when a constant bias current I_{DC} is flowing in the device (Figure 5.6, right), the working point changes and enters the non-symmetric sub-linear region. Here, a sinusoidal voltage signal superimposed to the I_{DC} bias produces different amplitudes on each half-wave, leading to an average current different from I_{DC}, in this case lower than the one flowing without the signal.

This behavior should not be neglected if the pseudo-resistor is the feedback element of a Trans-Impedance Amplifier (TIA), with an input current I_{DC} being an intended bias or a leakage current. When a signal is applied, the average current drawn by the feedback would be reduced due to the sub-linear behavior. However, the feedback of the TIA reacts by further *increasing* its DC output voltage, to keep the original value of DC current. This offset can impair the following stages of the circuit because it depends on the signal amplitude and the initial working point.

Nevertheless, the pseudo-resistor as in Figure 5.6 can be advantageously used in the applications that require a device that automatically limits its own current when the applied voltage tends to increase, thanks to its sub-linear behavior.

Between the two architectures of Figure 5.6, the one on the top-left has the advantage of requiring a single floating voltage generator.

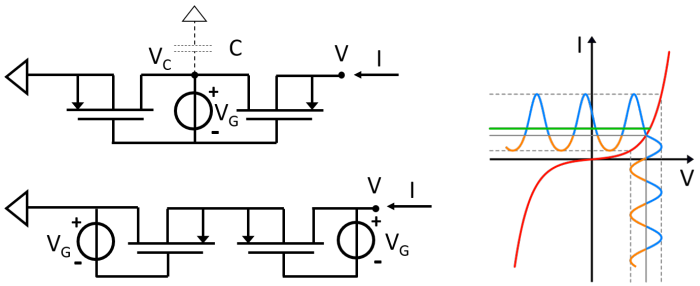


Figure 5.7 – *Possible series combinations of the elementary pseudo-resistor tunable cells, exhibiting a super-linear behavior.*

Additionally, the two transistors can share the same n-well at the expense of the frequency response, sharing very similar considerations to the non-tunable structures.

Conversely, the structure on the bottom-left of Figure 5.6 has the disadvantage of requiring two matched generators. However, these are easier to design because they are referenced to the external pins, in this case ground and V. Additionally, their parasitic capacitances do not load the internal nodes of the pseudo-resistor, leading to a wider frequency response.

Super-linear Series Structures

The two possible series configurations using the single tunable cell from Figure 5.4a are shown in Figure 5.7 [91–93]. The I-V characteristic curve (on the right) shows a symmetrical and super-linear (meaning *more-than-linear*) behavior. When the device is biased by a constant current I_{DC} in a working point away from $V = 0\,\mathrm{V}$, applying a sinusoidal voltage results in an asymmetric current signal, with an average value higher than I_{DC}.

Recalling the example from the previous section, the behavior of a TIA with this pseudo-resistor in the feedback loop and an input current I_{DC} is different from before. The circuit would react to a sinusoidal signal by *reducing* the DC output voltage, to recover to the correct current value I_{DC}. This effect is extremely beneficial when I_{DC} is a parasitic leakage current, because the device reduces any output offset. The reduction increases with the amplitude of the signal and restores the full output dynamic range of the amplifier.

The architectures of Figure 5.7 are identical to the ones shown

in Section 5.3.1, but the short circuit connection from the gate has been replaced by a voltage generator. Therefore, they share very similar considerations to their corresponding non-tunable structure regarding layout, dynamic range and frequency response. Both variants load their internal node with a parasitic capacitance and are not suitable for high-frequency: the one on the top has the generator (with its parasitic capacitance) connected to the internal node, the one on the bottom has the well at the internal node. Nevertheless, the variant on the top is particularly indicated for low-frequency operation up to 100 kHz, as it is very simple and requires only a single voltage generator [91–93].

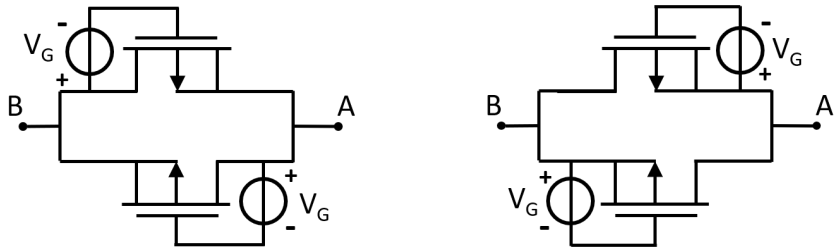
Linearity behavior of Parallel Structures

The structures of the previous sections, made with a series of non-symmetric resistive cells, will have the voltage at the internal point (V_C in Figure 5.7) moving in a non-linear and non-symmetric way. This aspect, giving no effects at low-frequency, becomes important at high-frequency due to the presence of the parasitic capacitance C to ground at the same internal node.

The current absorbed by this capacitance alters the balance of currents between the transistors and modifies their working points, thus affecting the output offset of the full pseudo-resistor. When placed in the feedback path of a TIA, the series topologies shown so far cause, in general, an increase of the output voltage offset as the frequency increases, whatever the type of non-linearity. This effect competes with the dynamic reduction of the offset of the super-linear structure (Figure 5.7) and quickly becomes dominant as the frequency increases.

The parallel structures shown in Figure 5.8 support higher frequencies due to the absence of internal nodes. Since every element (MOSFETs and diodes) is in parallel with each other, the I-V curve is the result of the sum of each current contribution. Both 5.8a and 5.8b have the two well diodes in parallel with opposite orientation. Therefore, their exponential behavior becomes dominant when the differential voltage V_{AB} is enough to turn on the diodes: $|V_{AB}| > 0.7\,\text{V}$. In these regions, or for very large voltage signals, both pseudo-resistors exhibit a super-linear behavior.

The difference between the two structures is the type of linearity behavior shown when the diodes are not dominant: $|V_{AB}| \ll 0.7\,\text{V}$.



(a) (b)

Figure 5.8 – *Possible parallel combinations of the elementary pseudo-resistor tunable cells.*

The pseudo-resistor from Figure 5.8a has a super-linear behavior, while the one of Figure 5.8b shows a sub-linear behavior.

Given the benefits of the super-linearity when used as the feedback element of a TIA, and the exceptional characteristics in terms of tunability, symmetry, and frequency behavior, the parallel pseudo-resistor of Figure 5.8a deserves a dedicated analysis (Section 5.5).

5.4 | Floating voltage generator architectures

The floating voltage generator can be implemented with to two different circuit topologies: a source-follower stage used as a voltage shifter, or a MOSFET transistor in trans-diode configuration, biased with a fixed current. Variations of these basic topologies are found in the literature [88, 91–95]. In the following sections, we analyze the most relevant configurations.

5.4.1 | Source-Follower

The simplest topology is the source-follower stage of Figure 5.9(a), presented in [91, 93] to bias a tunable gate-to-gate pseudo-resistor. In essence, the stage is voltage shifter, where the gate of M1 is used as an input to read with high-impedance the potential of a node, and the output is taken on the source of M1. The differential voltage V_{GS1} between gate and source is fixed and can be tuned by changing the bias current of the stage.

The source-follower transistor needs to be of the opposite type of the pseudo-resistor MOSFET. For example, if the pseudo-resistor

Figure 5.9 – *Topologies to implement a floating voltage generator: (a) Source-Follower (b) Improved Source-Follower (c) Buffered-Input Trans-diode (d) Hanging Trans-diode.*

is designed with a pMOSFET, its gate has to be driven at a lower voltage compared to its source/drain node. Thus, an nMOSFET source-follower must be used, because the required voltage shift is negative. If the pseudo-resistor is a nMOSFET, a pMOSFET source-follower must be used.

Although very simple to integrate, this basic structure has two important disadvantages:

i) The CMOS technology must offer both p-wells and n-wells. The body effect in the follower (transistor M_n) must be avoided, because it would make V_{GS} dependent on the absolute potential of the reference voltage. Therefore, both the pseudo-resistor and the source-follower need an isolated body-source connection, and both types of wells are required.

ii) The value of the resistance is highly affected by the technological process variation. Given a fixed bias current, V_{GS} depends on the process and temperature variations of the threshold voltage of the nMOSFET transistor. At the same time, the resistivity of the pseudo-resistor depends on the threshold voltage variations of the pMOSFET transistors. The two effects combine and lead to a very large variability in the resistance of the device.

5.4.2 | Improved Source-Follower

An improved topology of the source-follower, that solves the sensitivity to the threshold voltages variations, has been proposed in [92]. A pseudo current mirror is used to bias the source-follower stage, as shown in Figure 5.9(b) for a n-type follower. Since M_n and M_{Bn} share the same current I_{BIAS}, the dependence of V_{BIAS} on the nMOSFET threshold process variations is cancelled. At the same time, changes in the threshold voltage of the transistor M_{Bp} and the pseudo-resistor pMOSFET perfectly compensate each other. Therefore, the equivalent resistance of the device, tuned with the current I_0, is independent on the process-variations of the threshold voltages [92]. If I_0 is generated by a PTAT current generator the pseudo-resistor bias is also independent on the temperature fluctuations [94].

However, the Improved Source Follower still requires both type of wells to avoid the body effect (through isolated body-source connections), which would otherwise ruin the matching between the pairs of transistors.

5.4.3 | Buffered-input Trans-diode

A trans-diode configuration topology, as proposed in [93], can be exploited to use just one type of transistor for both the bias circuit and the pseudo-resistor. As shown in Figure 5.9(c), the input voltage is read at high-impedance by an OpAmp and is replicated on the source terminal of a pMOSFET M_p by a voltage buffer configuration (OpAmp + M_b). The transistor M_p is connected as a trans-diode and biased with a fixed current. The output voltage is taken on the gate-drain terminal of the M_p transistor.

The voltage shift is still given by the V_{GS} of a transistor and can be tuned by changing the bias current of the stage, like in the previous configurations. Differently from before, the shifting transistor is of the same type of the pseudo-resistor, thus the process variations of the threshold voltage are cancelled.

The main disadvantage of this structure is that it requires an additional operational amplifier to operate. This is not a problem for low-frequency operation, where the design of the amplifier can be kept relatively simple and low power. However, in applications where the signals applied to the pseudo-resistor are at frequencies higher than a few kHz, the topological complexity and the power consumption of the operational amplifier could become relevant.

5.4.4 | Hanging Trans-diode

A simplified version of the Buffered-Input Trans-diode, where the input buffer is removed, has been used to bias a cross-coupled pseudo-resistor [95] and allows high frequency operation without the power consumption of a high-speed OpAmp. As shown in Figure 5.9(d), the source of the trans-diode is directly connected to the input node, and the output voltage is take at the gate-drain contact. This configuration retains the advantages of the previous one: only one type of well is required, and it is not sensitive to threshold process variations.

However, the input voltage is now read with a resistive impedance, and the bias current is directly injected into the input node [95]. The injection of current dramatically increases the transconductance of the pseudo-resistor, increasing its noise spectral density [88]. Therefore, the use of this configuration should be evaluated carefully depending on the pseudo-resistor and the specific application.

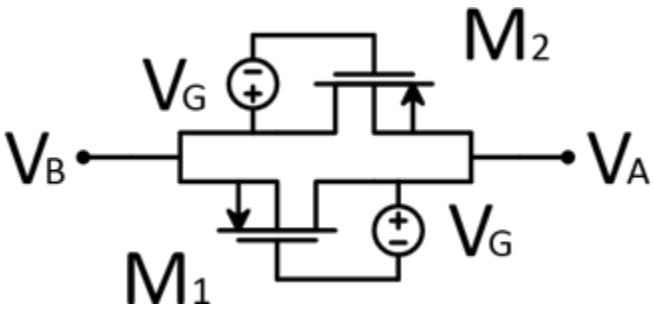


Figure 5.10 – *Schematic of the symmetric and tunable pseudo-resistor topology, based on the parallel composition of elementary tunable cells.*

5.5 | High-linearity Tunable Pseudo-resistor

The symmetric and tunable pseudo-resistor topology shown in Figure 5.10 has been selected among the other possibilities for its exceptional characteristics: i) high-linearity at the bias $V_{AB} = 0$ ii) symmetric behavior, iii) tunability range of its resistance value, iv) dynamic offset reduction thanks to the super-linear I-V curve, v) wide frequency range due to the absence of internal nodes.

The following paragraphs compute with detailed mathematical expressions the equivalent resistance of the pseudo-resistor, to guide the design of the transistor. Methods to extend the linear range around $V_{AB} = 0$ are also discussed.

5.5.1 | Equivalent resistance

The equivalent resistance depends on the current contribution of each MOSFET, in particular around $V_{AB} = 0$. The two transistor have opposite behavior due to their mirrored connections: when V_{AB} increases, the driving voltage of the transistor M_2 grows accordingly ($V_{GS} = V_{AB} + V_G$) and leading to a higher current. At the same time, M_1 reduces its current correspondingly. In the practical case of transistors operating in the sub-threshold regime, the current can be approximated by:

$$I_D = I_{D0} \exp\left(\frac{V_{GS}}{nV_{th}}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_{TH}}\right)\right] \tag{5.4}$$

where

$$I_{D0} = 2n\mu C_{OX}\left(\frac{W}{L}\right)V_{TH}^2 \exp\left(-\frac{V_T}{nV_{th}}\right) \tag{5.5}$$

The small signal resistance of each cell can, therefore, be obtained from (5.4) as:

$$\left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{DS}=0} = \frac{I_{D0}}{V_{TH}} \exp\left(\frac{V_{GS}}{nV_{TH}}\right) \tag{5.6}$$

leading to the resistance of the pseudo-resistor as the parallel of the two transistors:

$$R_{pseudo} = \frac{1}{2}\frac{1}{\left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{DS}=0}} = \frac{V_{TH}}{2I_{D0}} \exp\left(-\frac{V_{GS}}{nV_{TH}}\right) \tag{5.7}$$

The exact value of resistance of the final pseudo-resistor depends on the technology and can be adapted to the application by properly sizing the transistors. The matching of the transistor pairs is extremely important to keep the symmetry of the device and a proper layout should be designed to minimize mismatches.

It is worth mentioning that the parasitic capacitances of the device may eventually modify the value of its equivalent impedance, changing the effective resistance depending on the working frequency. However, they cannot produce any asymmetry in the behavior of the device nor induce a modification in the working point of the transistors.

The tunability with V_G and the symmetry of operation of this pseudo-resistor can be appreciated in Figure 5.11, showing a circuital simulation of the device.

5.5.2 | Linearity over an extended range

The linearity of the pseudo-resistor can be extended over the few tens of mV shown in Figure 5.11 by adding more cells in series (Figure 5.12a) [89]. Figure 5.12b shows how three stages already extend the dynamic range of the linear response to hundreds of mV.

A better option for high linearity applications is shown in Figure 5.13. It uses only one pseudo-resistor and a resistive voltage divider to provide an equivalent resistance R_{eq} given by:

$$R_{eq} = R_{pseudo}\left(1 + \frac{R_1}{R_2}\right) \tag{5.8}$$

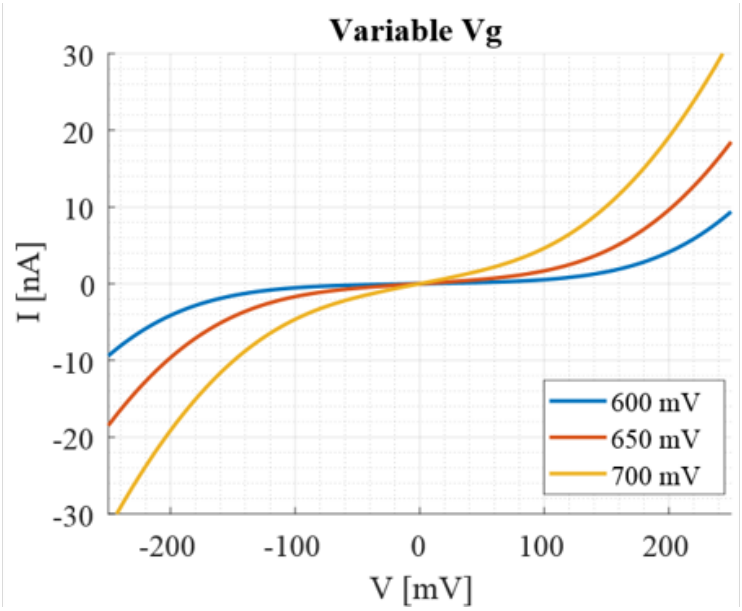


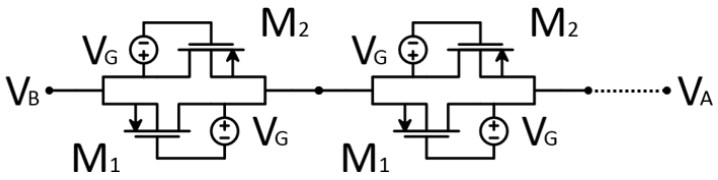
Figure 5.11 – *Simulated I-V curve of the pseudo-resistor cell for three different values of the generator voltage V_G.*

By using two simple resistors of small value we obtain a resistor equivalent to $\left(1+\frac{R_1}{R_2}\right)$ number of stages in series, with an enormous advantage in term of occupied area (minimum number of transistors, minimum number of voltage sources). This structure, by reducing the effective voltage applied across the pseudo-resistor, increases linearity by the same factor $\left(1+\frac{R_1}{R_2}\right)$ providing easily a wide range of operation.

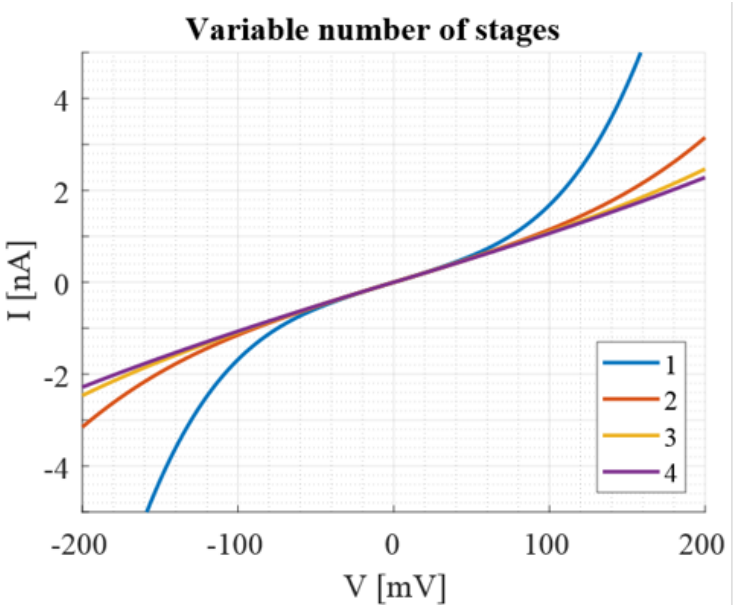
However, only the equivalent differential resistance between Node A and Bode B is increased, the single ended resistance from A to ground is considerably reduced to (R_1+R_2). Therefore, this technique is only useful in the feedback path of a TIA. For other applications where a floating bipole is required, the best method to extend the linear range is adding more cells in series.

5.5.3 | Improved Hanging Trans-diode

We propose an improved version of the Hanging Trans-diode that has been used to bias the pseudo-resistor presented in Section 5.5.



(a)



(b)

Figure 5.12 – *Extension of the linear range of the device by cascading multiple pseudo-resistor cells in series. (a) Series composition of the cells (b) Simulated I-V curves as a function of the number of cells.*

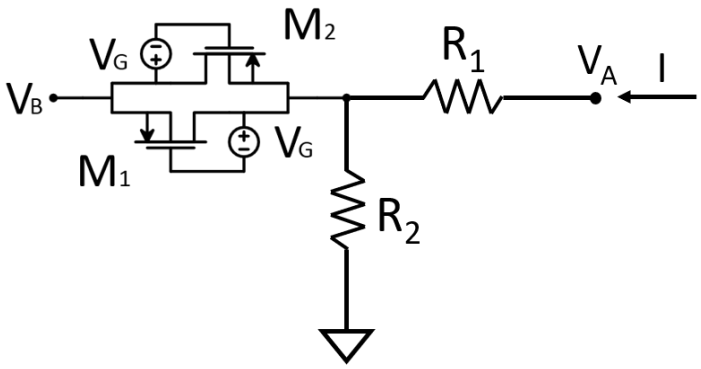


Figure 5.13 – *Method to extend the linear range of the pseudo-resistor, by means of a resistive voltage divider.*

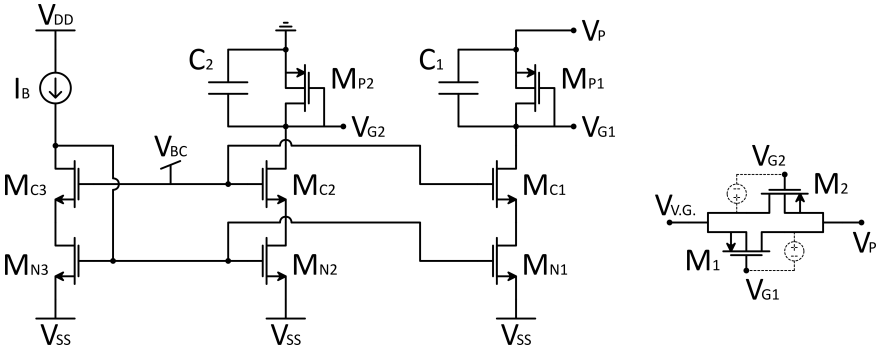


Figure 5.14 – *Improved topology for the implementation of two matched floating voltage generators, to bias the pseudo-resistor (on the right).*

The complete schematic of two matched floating voltage generators is shown in Figure 5.14, detailing the connections to the pseudo-resistor.

Two identical pMOSFET trans-diodes, each in its own n well, are used to bias our p-type pseudo-resistor, allowing only one type of well to be used. The bias currents are provided by two matched branches ($M_{N1} - M_{C1}$ and $M_{N2} - M_{C2}$) of a cascode current mirror from a single branch ($M_{N3} - M_{C3}$) with current I_B. The cascode structure minimizes the introduction of parasitic capacitances (towards ground) at the pseudo-resistor nodes, allowing for a better frequency behavior. Additionally, two capacitors C_1 and C_2 have been added in parallel to the trans-diodes to stabilize the generated voltage at high-frequency.

The tunable pseudo-resistor presented in the previous sections, complete with floating voltage generators, was used to bias a capacitive feedback Trans-Impedance Amplifier, as shown in Figure 5.1. In this specific application, the voltage buffers can be omitted for both the trans-diodes because:

i) M_{P1} injects its current in a low-impedance node, the output of the OpAmp, and its effect is negligible.

ii) M_{P2} would inject its current into the virtual ground of the operational amplifier, critically impairing the correct operation of the circuit. However, being the voltage of the virtual ground fixed by the circuit topology, the voltage shifter can be referenced to a fixed ground reference instead of the virtual ground, avoiding the current injection.

Having defined the bias circuit, it is possible to further elaborate the expression of the equivalent resistance of the device. Applying the sub-threshold equation (5.1) to the bias transistor $M_{P1,P2}$ and considering $V_{DS} \gg V_{th}$, the expression for V_{SG} becomes:

$$V_{SG} = nV_{TH} \ln\left(\frac{I_B}{I_{D0,B}}\right) \tag{5.9}$$

with

$$I_{D0,B} = 2n\mu C_{OX}\left(\frac{W_B}{L_B}\right) V_{TH}^2 \exp\left(-\frac{|V_T|}{nV_{TH}}\right) \tag{5.10}$$

Replacing the (5.9) in the (5.7), with the hypothesis of using all transistors with the same length L:

$$R_{pseudo} = \frac{V_{TH}}{2I_B} \cdot \frac{I_{D0,B}}{I_{D0}} = \frac{V_{TH}}{2I_B} \cdot \frac{W_B}{W} \tag{5.11}$$

and, from (5.8):

$$R_{eq} = \frac{V_{TH}}{2I_B} \cdot \frac{W_B}{W}\left(1 + \frac{R_1}{R_2}\right) \tag{5.12}$$

This expression directly links the equivalent resistance of the pseudo-resistor to the geometrical dimensions of the transistors, the multiplication factor, and the bias current, that can be externally changed to fine-tune the resistivity of the device.

5.5.4 | Measurement results

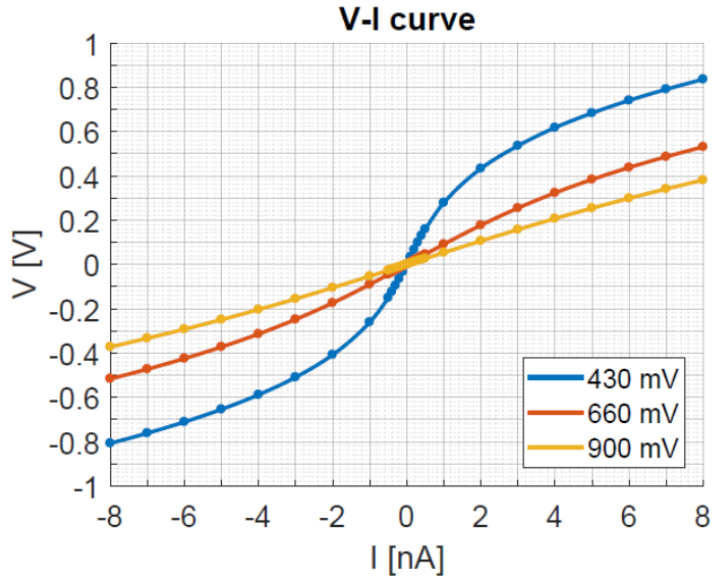
The proposed pseudo-resistor, complete with the floating voltage generators, has been designed, fabricated and tested in AMS CMOS 0.35 µm technology as the feedback element for a high-bandwidth low-noise Trans-Impedance Amplifier for the CLIPP readout. The device has been characterized with several tests by measuring its V-I curve, evaluating the equivalent resistance, and verifying the dynamic output offset reduction.

The characteristic curve of the device, due to its connection in the feedback path of the TIA, has been measured by setting the DC input current I and by measuring its output voltage V_{out}. The obtained curve is therefore a V-I curve and is shown in Figure 5.15a for different values of the *external control* voltage V_C, proving the exceptionally symmetric behavior of the pseudo-resistor. The external bias allows a convenient tuning of the bias current I_B of the floating voltage generators. The link between V_C and I_B depends on an integrated resistance of 50 kΩ and a cascade current mirror reducers (of factors $\frac{1}{9}$, $\frac{1}{9}$, $\frac{1}{3}$, $\frac{1}{10}$):

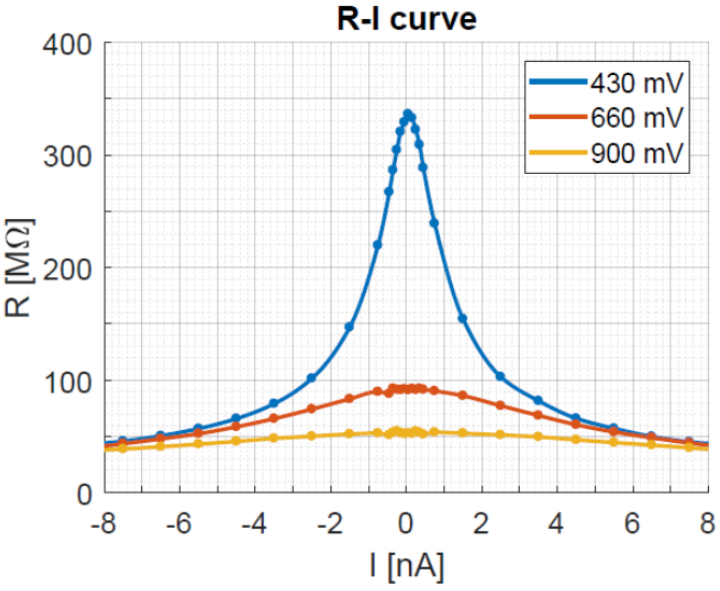
$$I_B = \frac{V_C}{50\,\text{k}\Omega} \cdot \frac{1}{2430} \tag{5.13}$$

The synthesized small-signal resistance depends both on the DC input current and the control voltage V_C and can be extracted as the slope of plot of Figure 5.15a, and is shown in Figure 5.15b. The resistances at different bias voltages converge for currents $I > 8$ nA because the well diodes contribution contributions become relevant and are not affected by the bias V_G.

Figure 5.16a shows the effect of the dynamic output offset reduction. A current of −1 nA has been injected into the TIA to simulate a leakage current for three different values of the control voltage. At the same time, an additional sinusoidal voltage signal in the range of 0 mV to 600 mV has been applied to the TIA through a 1 pF capacitance, leading to an oscillation of the output voltage in the range of 0 V to 1.2 V (the TIA has a 500 fF feedback capacitance). The plot clearly shows the reduction of the output offset due to the simulated leakage current, thanks to the super-linearity behavior of the pseudo-resistor.

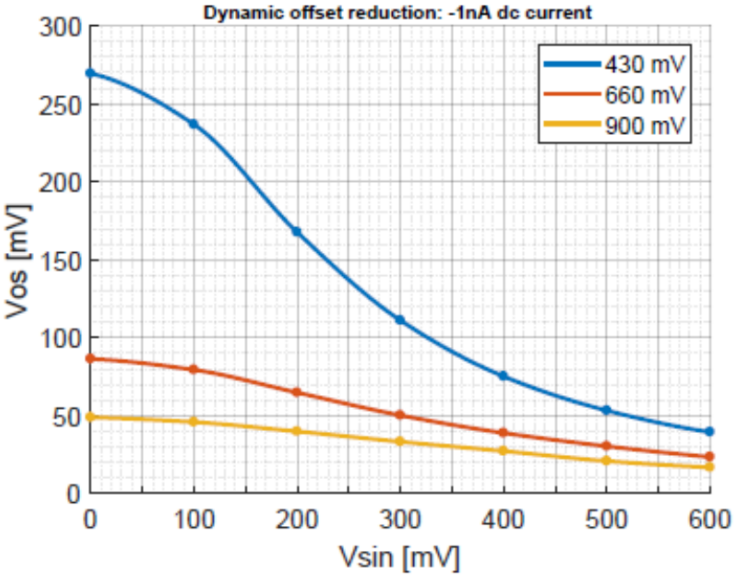


(a)

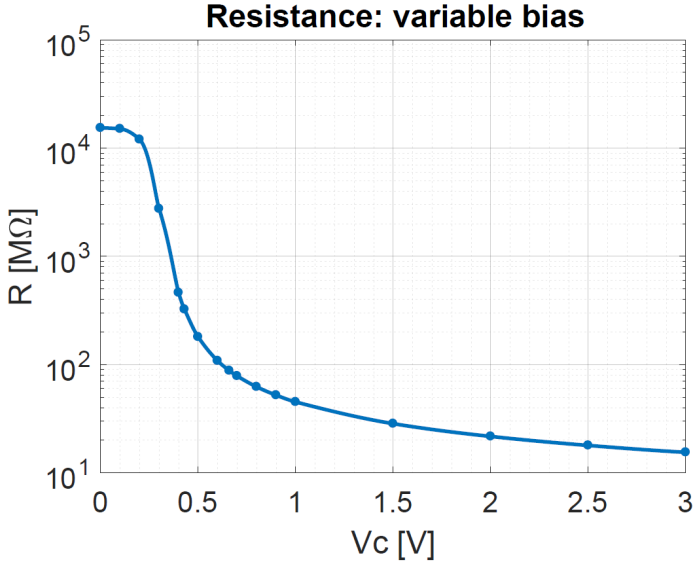


(b)

Figure 5.15 – *(a) Measured V-I curves of the pseudo-resistor for three different values of the control voltage V_C. (b) R-I curves of the pseudo-resistor for three different values of the control voltage V_C. Calculated by extracting the derivative of the V-I curves.*



(a)



(b)

Figure 5.16 – *(a) Measured dynamic offset reduction as a function of the input signal amplitude, in presence of a constant current of* -1 nA*, for three different values of the control voltage* V_C*. (b) Indirectly measured resistance of the pseudo-resistor as a function of the control voltage* V_G*.*

Finally, the tunability range of the resistance has been evaluated through an indirect measure from the transfer function of the TIA. In particular, knowing the value of the feedback capacitance of the TIA, it is possible to compute the equivalent resistance of the pseudo-resistor from the low-frequency pole of the transfer function. Figure 5.16b shows the resistance for values of V_C from 0 V to 3 V. The device is capable of synthesizing a tunable resistance from 20 MΩ to 20 GΩ.

Part III

The Applications

CHAPTER

SIX

ADVANCED CONTROL TECHNIQUES WITH CLIPP

This chapter discusses the pilot tones and dithering techniques, two essential ways to use the CLIPP detector for the implementation of tuning and control algorithm of optical devices. Pilot Tones allow the identification of specific optical signals when multiple of them are concurrently present in the same waveguide. Instead, the dithering technique allows the extraction of the transfer function derivative of an optical device, directly from the physical system, to be used in optimization algorithms.

6.1 | Pilot Tones

Pilot Tones are a technique to discriminate specific optical signals regardless of the presence of other concurrent channels in the same waveguide. This is particularly useful in Wavelength Division Multiplexing (WDM) systems, that use multiple carrier wavelengths at the same time to expand the capacity of the network. Optical circuits can also exploit WDG to process multiple signals at once or to separate them on-chip.

Pilot Tones can be used to label specific signals by introducing a small modulation of their optical intensity. The tone can be a small percentage of the signal amplitude to avoid disruption of the optical transmission, and can be at a frequency of few kHz, not interfering with the GHz digital modulation of telecommunication systems.

For example, the total power of two optical signals travelling in the same waveguide at the wavelengths λ_1 and λ_2 can be expressed as:

$$P_{TOT} = \left(P_{\lambda_1} + \widetilde{P}_{\lambda_1} \cdot \cos\left(2\pi f_{tone} \cdot t\right)\right) + P_{\lambda_2} \tag{6.1}$$

where λ_1 and λ_2 are two different wavelengths and f_{tone} is the frequency of the pilot tone, only applied to λ_1.

When read with a CLIPP detector, the pilot tone combines with the Lock-In *Force* modulation of the CLIPP and shifts in frequency:

$$\begin{aligned} I_{CLIPP} = &\left(I_{dark} + I_{\lambda_1} + I_{\lambda_2}\right) \cos\left(2\pi\omega_{AC} \cdot t\right) + \\ &+ \frac{\widetilde{I}_{\lambda_1}}{2} \cos\left(2\pi\left(f_{AC} + f_{tone}\right) \cdot t\right) + \\ &+ \frac{\widetilde{I}_{\lambda_1}}{2} \cos\left(2\pi\left(f_{AC} - f_{tone}\right) \cdot t\right) \end{aligned} \tag{6.2}$$

where I_{dark} is the base current of the waveguide resistance in dark condition, I_{λ_1} and I_{λ_2} are the contributions from the two signals, and $\widetilde{I}_{\lambda_1}$ the modulated current due to the pilot tone.

To identify the channel λ_1, the CLIPP electric signal has to be demodulated twice: first at the driving frequency f_{AC} of the CLIPP, then at the modulation tone f_{tone}. The implementation of the readout usually features two cascaded Lock-In Amplifiers, each with its own filtering. The first filter must be designed with a bandwidth wide enough to let the pilot tone pass after the first demodulation. The second one, instead, can be as narrow as needed to obtain a sufficient SNR, with the usual trade-off between sensitivity and time response.

The Pilot Tones technique has an additional advantage: since the double demodulation only selects the signal $\widetilde{I}_{\lambda_1}$, induced by the pilot tone, every other component of the CLIPP current is filtered out. In particular, both the contribution due to the dark resistance of the CLIPP I_{dark} and the current I_{λ_2} are filtered by the readout. This means that the measurement system ignores any fluctuations of the resistance of the CLIPP due to the thermal gradients caused by the actuators, or by concurrent optical channels of the system. This huge advantage for the implementation of control loops comes at the cost of a smaller signal, only a percentage of the total current of the CLIPP, and a more complex readout scheme.

In a previous work, my group has demonstrated that the CLIPP can indeed discriminate optical signals of different wavelengths

propagating through the same waveguide if these are labelled with an intensity modulation amplitude of few percent at a frequency in the kHz range [66]. Furthermore, CLIPP assisted signal identification is possible without affecting the quality of the optical signal [96].

Our recent work, presented in Chapter 7, demonstrated that the labelling operation can be performed directly on-chip, allowing to manage the channel identification locally, without imposing any constraint on the transmission system used to generate the input channels [27].

Chapter 8 will present another application where the pilot tone technique has been used even to distinguish signals of the *same wavelength*, to unscramble hard-mixed modes in a Mode Division Multiplexing photonic circuit [97].

6.2 | Dithering

Dithering is a technique to extract the derivative of the transfer function of an optical device directly from the physical system and can be used to implement optimization control algorithms. In particular, the information can be useful in a feedback loop to tune and lock the working point of a device in a maximum/minimum of the transmission or in a point with the highest slope.

Integrated optical components are usually designed with an actuator, like a thermo-optical actuator, that is able to shift the optical transfer function at a different wavelength. The dithering technique is based on the addition of a small modulation signal, superimposed to the control voltage of an actuator of the optical device.

The dithering signal induces an additional modulation to the phase shift introduced by the actuator, producing an oscillation of the working point of the device and leading to an amplitude modulation of the output optical power. If the applied signal sufficiently small, the amplitude of the optical modulation is directly proportional to the slope of the transfer function at the working point.

Figure 6.1 represents the working principle of the dithering technique, showing how a sinusoid is obtained with the amplitude tied to the slope of the curve. Note that the entire transfer function is oscillating left and right, while the laser wavelength is fixed. If the working point were in a minimum/maximum of the transmission, the dithering would not generate any signal (or only a signal at

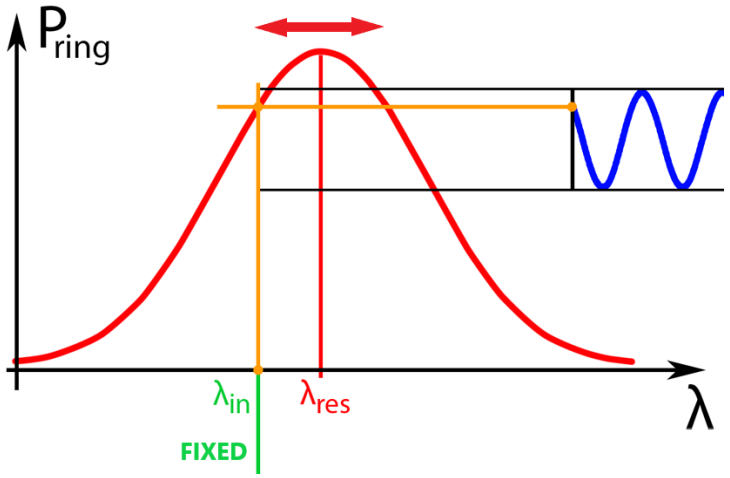


Figure 6.1 – *Working principle of the dithering technique. The entire transfer function oscillates around the bias point, leading to an amplitude modulation of the optical power.*

double the frequency).

In formulas, the dithering technique can be expressed as:

$$V_{ACT} = V_{BIAS} + v_{dith} \cdot \sin\left(f_{dith} \cdot t\right)$$

$$P_{OUT} \approx P_{OUT}\left(V_{BIAS}\right) + P_{dith} \sin\left(f_{dith} \cdot t\right) \tag{6.3}$$

with

$$P_{dith} = v_{dith} \cdot \left.\frac{\partial P_{OUT}}{\partial V_{ACT}}\right|_{V_{ACT}=V_{BIAS}} \tag{6.4}$$

where V_{ACT} is the driving voltage of the actuator, V_{BIAS} the initial bias voltage, v_{dith} and f_{dith} the amplitude and the frequency of the dithering signal, respectively.

It is important to note that the amplitude of the output modulation P_{dith} is proportional to the dithering signal amplitude v_{dith}. However, a large signal may disturb the operation of the optical device depending on the application. Furthermore, if the dithering oscillation is too wide, the output signal becomes corrupted by other components related to the concavity and the shape of the transfer function. Therefore, the amplitude of the dithering signal must be chosen carefully, evaluating the trade-off between a clean signal extraction and the perturbation of the optical system.

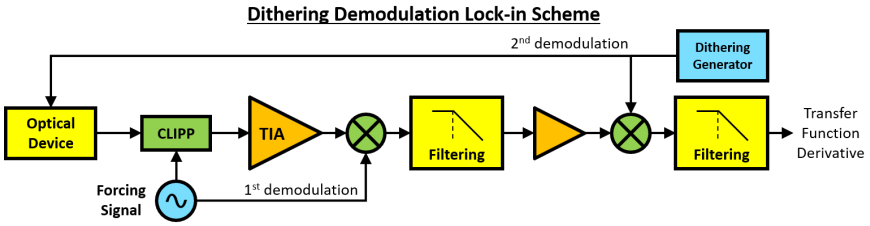


Figure 6.2 – *Complete readout scheme for the dithering technique when using a CLIPP detector.*

By demodulating the optical power, read by a detector like a CLIPP or a photodiode, at the dithering signal frequency, the derivative of the transfer function is extracted directly from the physical system. The signal also preserves the information on the sign of the derivative because if the curve has a negative slope the phase of the optical power modulation is opposite to the original dithering signal. Figure 6.2 shows the readout scheme for a CLIPP detector with the addition of the dithering demodulation.

Considering a CLIPP as the chosen detector to read the optical power, it is possible to express the dithering signal as:

$$G_{WG} \approx G_{WG,Dark} + \Delta G_{WG}(V_{BIAS}) + \Delta G_{WG,dith} \cdot \sin\left(f_{dith} \cdot t\right) \quad (6.5)$$

where

$$\Delta G_{WG,dith} = v_{dith} \cdot \left.\frac{\partial \Delta G_{WG}}{\partial V_{ACT}}\right|_{V_{ACT}=V_{BIAS}} \quad (6.6)$$

The technique shares the same advantage of the pilot tones, being insensitive to the thermal drift of the waveguide resistance (the dark condition), and can be used both with sinusoidal and square-wave dithering signals applied to the actuators, the latter being generally easier to synthesize and demodulate.

6.2.1 | Controlling a Ring Modulator

Figure 6.3 shows a typical transfer function of an All-Pass Ring Modulator. The response is flat and equal to 1 for most of the wavelengths, letting all the light pass. When the optical wavelength is in resonance with the Ring Modulator, the light is captured and dissipated by the device, causing a dip in the transfer function.

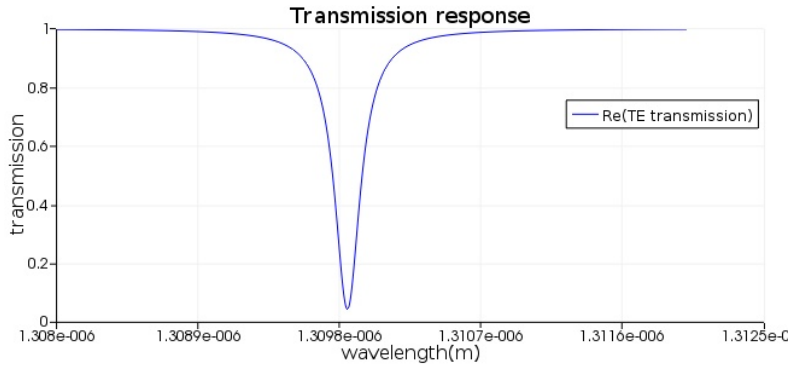


Figure 6.3 – *Typical transfer function of an All-Pass Ring Modulator [98].*

These kind of devices are typically tunable though one or multiple actuators and modern realization of Ring Modulators usually have two: a fast integrated p-n junction to modulate the optical signal at GHz frequencies, and thermo-optical actuator to control the bias point of the device.

Within the context of the European Project ICT-STREAMS, IMEC fabricated several Ring Modulators capable of operating at frequencies up to 50 GHz. Figure 6.4 shows the derivative of the transfer function of one of these modulators, extracted with the dithering technique. The measurement has been repeated for different amplitudes of the dithering sinusoid, showing that a usable signal can be extracted even with extremely small sinusoids, down to 1 mV. Additionally, the plot shows a proportional growth of the signal until 20 mV of dithering sinusoid, while the derivative extracted with 50 mV is becoming distorted by the higher order components of the transfer function.

The next plots show how the derivative can be used to implement a feedback loop to stabilize the working point of the Ring Modulator in a particular point of the transfer function. The experiment has been repeated for two target points: the resonance condition (Figure 6.5), where the modulator captures the incoming wavelength and shows minimum transmission, and the maximum slope point (Figure 6.6), a good bias point to introduce a digital modulation of the light with the fast actuator of the ring. Both figures show in the top plot the average optical power acquired by a CLIPP and a photodetector, and the derivative extracted at the same time with

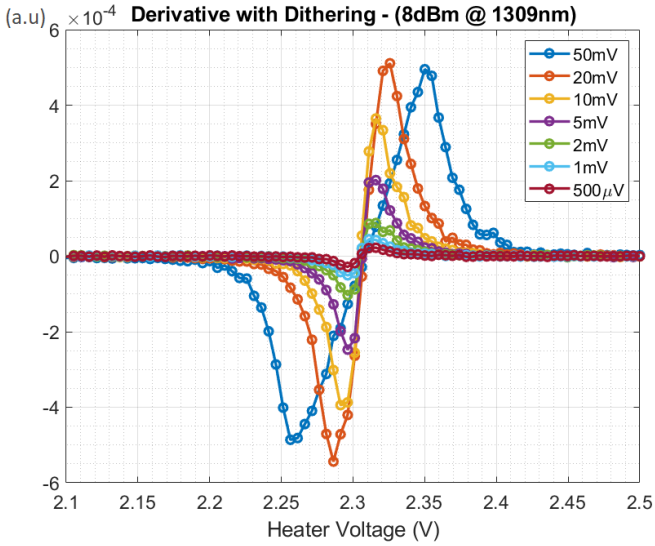


Figure 6.4 – *Derivative of the transfer function of a Ring Modulator, extracted with the dithering technique through a CLIPP detector.*

the additional demodulation of the dithering. The X axis counts the iterations of the control algorithm, a simple *"bang-bang"* controller chasing the target point.

At the 50th iteration, the bias point of the ring is affected by an external disturb, in the form of a nearby thermal actuator switching from OFF to a high power condition. The two plots show how the system recovers the desired bias point condition in few tens of iterations, proving the effectiveness of the technique even with very simple control schemes.

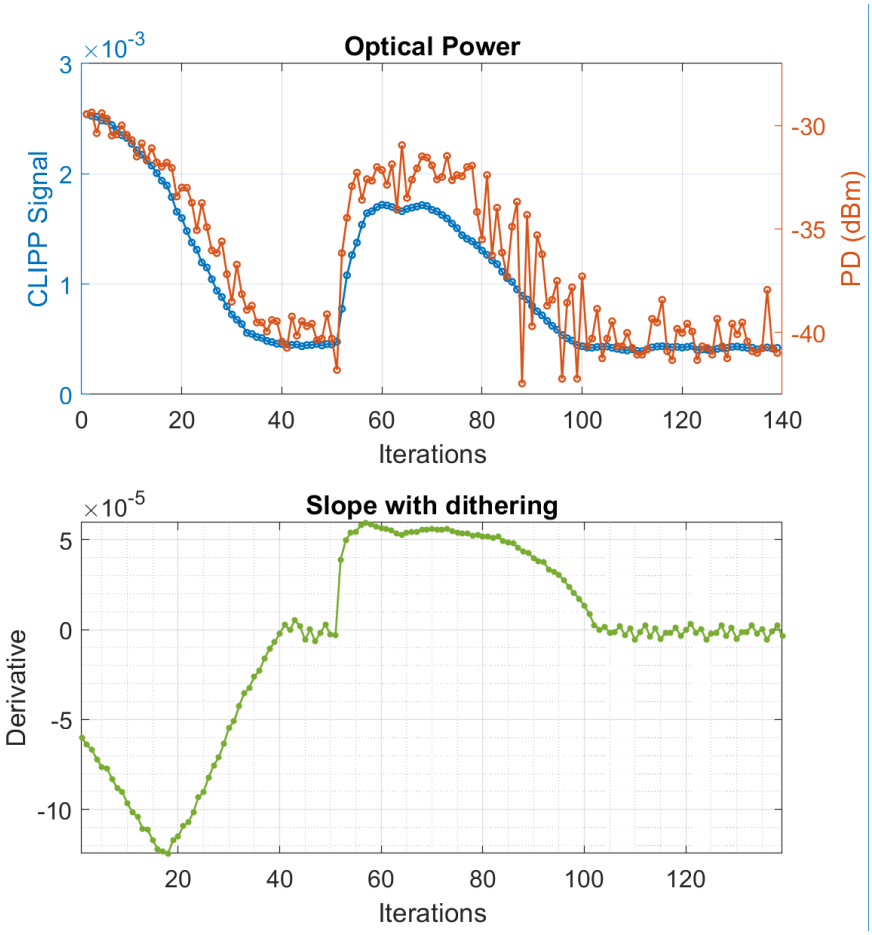


Figure 6.5 – *Locking of the minimum transmission point of the Ring-Modulator by exploiting the derivative signal extracted through the dithering technique. The top plot show the average optical power acquired by a CLIPP and a photodetector. The plot on the bottom shows the derivative. After an initial transient that tunes the ring to the resonant condition (corresponding to the minimum of the transmission and the derivative), an abrupt disturb is introduced at iteration 50. The system recovers the desired bias point in under 50 iterations.*

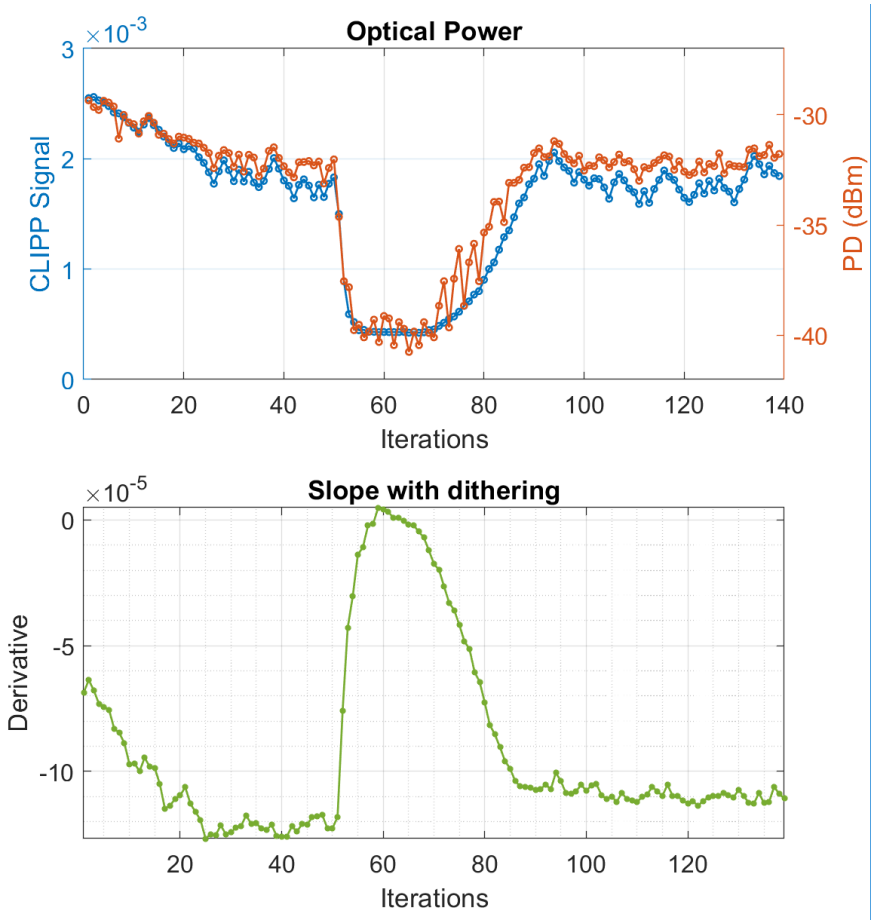


Figure 6.6 – *Locking of the maximum slope point (negative in sign) of the Ring-Modulator by exploiting the derivative signal extracted through the dithering technique. The top plot show the average optical power acquired by a CLIPP and a photodetector. The plot on the bottom shows the derivative. After an initial transient that tunes the ring to the maximum slope condition (corresponding to the most negative value of the derivative), an abrupt disturb is introduced at iteration 50. The system recovers the desired bias point in under 40 iterations.*

CHAPTER

SEVEN

AUTOMATED ROUTING AND CONTROL OF SILICON SWITCH FABRICS

This chapter shows the disrupting possibilities that the CLIPP detector unlocks, allowing the stabilization, tracking and reconfiguration of the working point of an entire photonic circuit. The work focuses on a classical and very well known 8×8 switch fabric, made by 2×2 switches based on silicon Mach-Zehnder interferometers (MZI), monitored by 24 CLIPP detectors in total. Although such router is very popular for its geometrical simplicity, its control and stability in real operative conditions with simultaneous multi-wavelength signals pose several challenges.

The array of CLIPPs, simultaneously interrogated by an integrated CMOS ASIC [83], allows to track the optical power in each path, enabling real-time monitoring of the status of the router, its automated reconfiguration, and compensation of the thermal crosstalk among the switching elements.

The results of this work were published in the paper:

A. Annoni, **E. Guglielmi**, M. Carminati, S. Grillanda, P. Ciccarella, G. Ferrari, M. Sorel, M. J. Strain, M. Sampietro, A. Melloni, and F. Morichetti. "Automated routing and control of silicon photonic switch fabrics". In: *IEEE Journal on Selected Topics in Quantum Electronics* 22.6 (Nov. 2016), pp. 169–176. ISSN: 1077260X. DOI: 10.1109/JSTQE.2016.2551943. URL: http://ieeexplore.ieee.org/document/7450148/

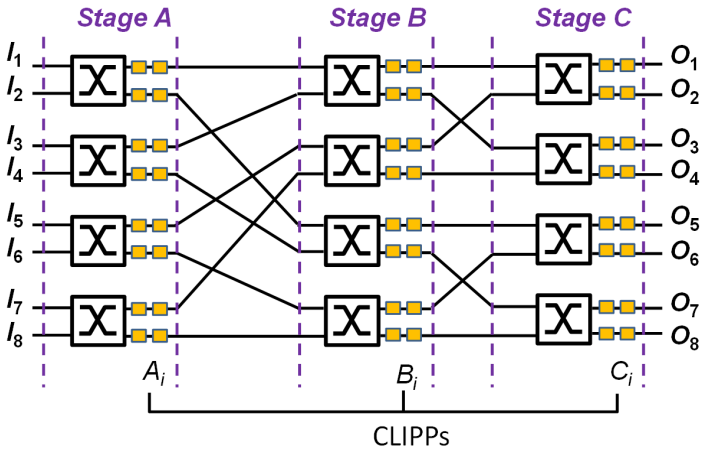


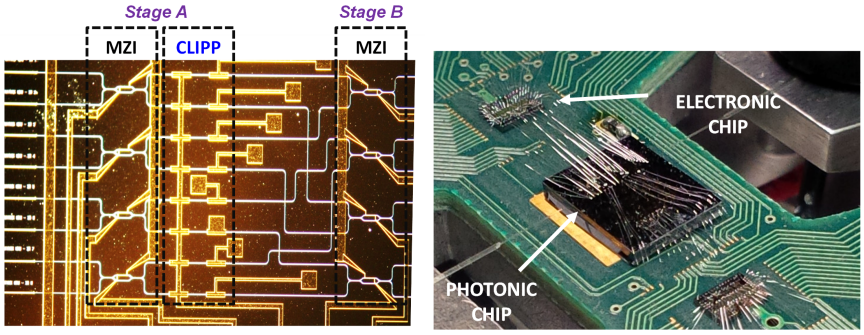
Figure 7.1 – *Scheme of the switch fabric, twelve 2×2 switches are arranged in three stages and interconnected. Each switching element is monitored with two CLIPP at its outputs.*

7.1 | Photonic Circuit Architecture

The photonic circuit employed to demonstrate control and reconfiguration through on-chip light-path tracking is schematically shown in Figure 7.1. It consists of an 8×8 switch fabric, composed by twelve 2×2 switches realized through thermally-actuated balanced MZIs and arranged in 3 switching stages (A, B, and C). The topology is organized as a *Benes network*, but the proposed approach can be generalized to different switch fabric architectures, to larger port counts and, more generally, to any routing/switching photonic integrated circuit. A CLIPP detector is integrated at both output ports of each MZI switch, thus resulting in 24 CLIPPs in total, allowing to monitor the optical power in each waveguide.

The silicon channel waveguides employed in the circuit are fabricated by e-beam lithography on a standard 220 nm SOI platform. The waveguide core is 480 nm wide and is buried underneath a 1 µm thick SiO_2 top cladding, that is grown by plasma enhanced chemical vapor deposition (PECVD) [2]. The waveguide propagation loss is 2.5 dB/cm at a wavelength of 1550 nm.

Thermal actuators for the MZI switching are realized through 50 µm long and 900 nm wide Ni/Cr stripes deposited above the SiO_2



(a) (b)

Figure 7.2 – *(a) Top view photograph of a portion of the switch fabric matrix; stages A and B and the first series of CLIPPs are visible. (b) Photo of the Silicon Photonic chip and the two CMOS ASIC mounted onto a PCB, wire bonding allows electrical connections between the chips and the PCB.*

cladding. Electrical power consumption required to induce a π phase-shift is about 10 mW. The total footprint of the circuit is 1.5 mm × 5.5 mm, including input/out inverse tapers, metallic buses and contact pads. Figure 7.2a shows a top view photograph of a portion of the fabricated circuit, where the two MZI switching stages A and B are visible in the leftmost and rightmost part of the picture, respectively. Between the two MZI stages, the first arrangement of 8 CLIPPs is visible.

The CLIPPs electrodes have a size of 20 µm × 100 µm and are mutually spaced by 100 µm. Both the CLIPPs' electrodes and the metal connections of the heaters are realized with the same gold layer. Thermal actuator and CLIPP buses are terminated on 100 µm×100 µm contact pads, that allows the wire-bonding of the photonic chip to the external electronic circuit. As shown in Figure 7.2a, a common metal bus delivers the *Force* signal simultaneously to all the CLIPPs of each stage, reducing the number of required interconnections.

Simultaneous monitoring of several CLIPPs is performed through a 32-channel ASIC realized in standard CMOS technology and designed to perform low-noise CLIPP signal detection. Details on the design, technology and characterization of the ASIC can be found in [83]. Figure 7.2b shows how the SiP chip and the ASIC are assembled onto the same Printed Circuit Board (PCB). Since the wiring is very critical from the signal-integrity point-of-view, the CLIPPs are

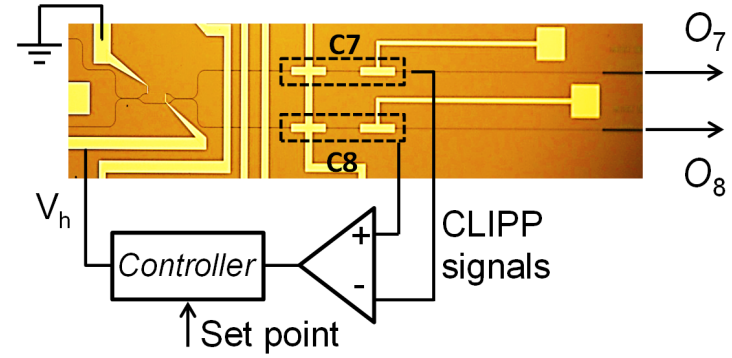
directly bonded to the ASIC in order to reduce parasitics, while the heaters are connected to the PCB. This is an example of an hybrid platform, as explained in Section 4.2: the readout front-end is integrated into the ASIC and then connected to a separate board that allows the acquisition of the signals, their conversion to the digital domain, the management of the heaters driving voltages, and the implementation of multiple feedback loops [99].

The CLIPP detectors integrated in this photonic chip contributed to the study and formalization of design rules discussed in Chapter 2 and published in [71]. For example, the particular design with wide electrodes and 1 : 1 ratio between electrode length and spacing, visible in Figure 7.2a (and later in Figure 7.3a) can be recognized in Figure 2.7 from Chapter 2. The design led to an optimal operating frequency f_{AC} in the 100 kHz to 1 MHz range. However, the *Force* signal amplitude was limited to few V by the value of the parasitic C_E, not carefully minimized and in the range of 500 fF to 1 pF. Despite being one of the first design iterations, thus not following all of the design rules explained in Chapter 2, the CLIPPs achieved a good sensitivity (down to −30 dBm) and a large dynamical range (40 dB), without perturbing th optical field thanks to the 1 µm thick SiO_2 top cladding.

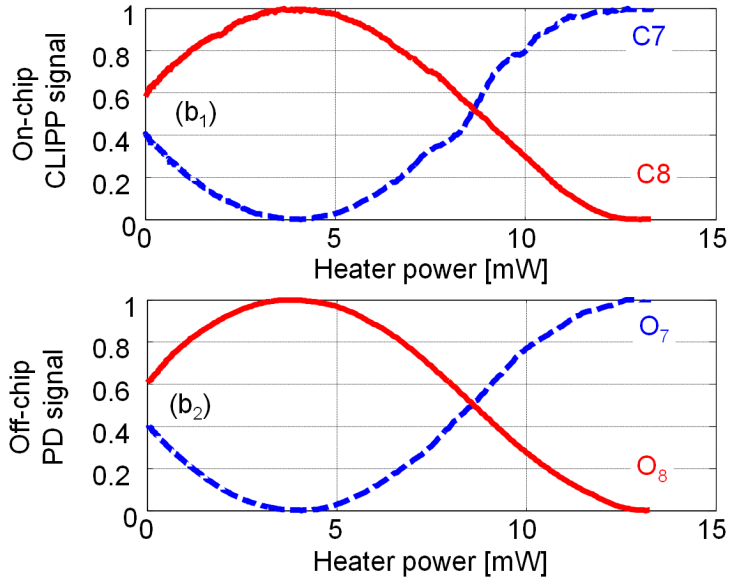
7.2 | Feedback control of MZI switches

To assess the CLIPP effectiveness to monitor and feedback control the switching state of a silicon MZI, only one of the MZIs of stage C is initially considered. Figure 7.3a shows a top-view photograph of the considered MZI (bottom-most switch of stage C). Here, the optical power at the output ports of the MZI can be directly measured both by using external photo-detectors (PDs) and by means of the integrated CLIPPs, thus providing a direct comparison between the two types of detectors. Figure 7.3($b_1 - b_2$) show, respectively, the normalized light intensity measured in the output waveguides by CLIPPs C_7 and C_8, and the normalized optical output power O_7 and O_8 that are simultaneously measured by external PDs for increasing voltage V_h applied to the thermal actuator. The normalization also includes the non-linearity of the CLIPP (see Appendix A), estimated with an exponent $\alpha \approx 0.7 - 0.8$.

The good agreement demonstrates that CLIPPs can provide the



(a)



(b)

Figure 7.3 – *CLIPP assisted feedback-control of a MZI switch. (a) Top-view photograph of a MZI of the switch fabric (stage C). The MZI status is monitored by two CLIPPs placed on the output waveguides; the monitoring signals are used by an external controller to steer the working point of the Mach-Zehnder by acting on the thermo-optical actuator. (b) Comparison between (b_1) the electrical signal provided by CLIPPs C_7 (dashed blue) and C_8 (solid red) at the output of the MZI and (b_2) the optical signal simultaneously measured with an external PD at output ports O_7 (dashed blue) and O_8 (solid red) versus the electrical power dissipated in the thermal actuator.*

same information as conventional PDs on the bias point of an integrated MZI. In this measurement, the wavelength of the laser source is about 1550 nm; at maximum transmission (that is the MZI in ON state), the light intensity in the MZI output waveguide is about −5 dBm.

As shown in Figure 7.3a, the CLIPP signals are sent to an external controller, which modifies the MZI working point by acting on the thermal actuator on one of the two arms of the MZI. In principle, for the routing applications described in this work where the MZI operates "digitally" as an ON (OFF) switch, the control algorithm (with a single degree of freedom represented by V_h) only requires a single CLIPP at one of the two output ports, to maximize (minimize) the optical power in the two states. The integration of a CLIPP at both ports, not only can be exploited to increase the control robustness, but also enables to lock the MZI to any intermediate bias condition (such as, for instance, a balanced 50%-50% state), independently of optical power fluctuations at the input port.

Real-time closed-loop control is implemented in a programmable digital controller (a 32-bit floating-point RISC processor running at 64 MHz) that directly drives the actuator voltage V_h by means of a 16-bit DAC with a 10 V swing and acquires the lock-in demodulated CLIPP signals, which are conditioned by the ASIC.

The control algorithm is a simple max/min chaser that can be used to initially tune the MZI to the desired operating point and, if kept active, to compensate for drifts and perturbations by continuously updating V_h. The algorithm periodically monitors the CLIPP power level and modifies the actuator driving voltage in steps that are constant in power (ΔV_h^2), in order to uniformly explore the MZI thermal response curve. By comparing the current power level with the previous reading acquired at a different V_h, it is possible to determine if the last control voltage adjustment was done in the correct direction. For example, when the minimum is targeted, if a decreasing signal is detected and V_h was increased at the previous step, then the next adjustment is done in the same direction.

Figure 7.4 shows the time-dependent normalized optical power measured with a conventional photodiode at the output port O_7, during the CLIPP-assisted switching of the MZI. At the starting point, the heater is switched OFF ($V_h = 0$ V) and the output power is about 4 dB below the maximum (see Figure 7.3b). At time $T = 100$ ms, the

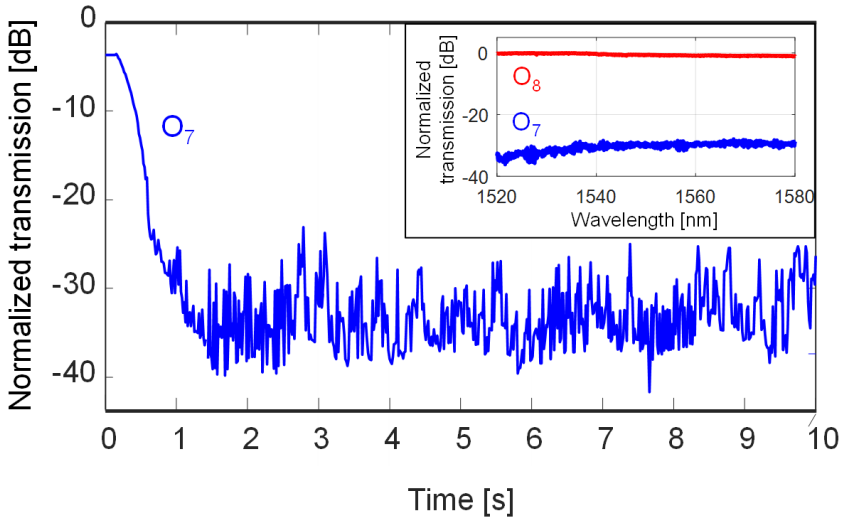


Figure 7.4 – *Measured normalized intensity at the output port O7 during the switch* OFF *of the MZI; the inset shows the steady state normalized spectrum at the output ports O7 (blue,* OFF *state) and O8 (red,* ON *state).*

tuning algorithm is switched ON to bring the output port O_7 to the OFF state. The optical power level drops by more than 20 dB in about 450 ms and reaches a normalized transmission of less than −30 dB in less than 1 s. Once the minimum transmission is reached, the controller holds the MZI in this state.

The closed-loop MZI switching speed is limited by the time response of the CLIPP (set to 8.3 ms by the 120 Hz lock-in filter BW) and by the decision rate of the algorithm (4.4 ms, 225 Sa/s). As detailed in Section 4.1.4 and in [66], the CLIPP time response can be reduced by increasing the CLIPP driving voltage or the CLIPP size. The residual fluctuations at the MZI output, visible in Figure 7.4, are due to the locking algorithm that keeps on evaluating the actual operating point. In order to increase the resolution, and thus to reduce the value of V_h^2 that produces the residual ripple, the signal can be acquired at a higher sample rate (1.8 kSa/s from 225 Sa/s) and additionally processed with a 256-sample wide moving average filter which increases the decision rate of the algorithm to 200 ms. With these settings, an optimal value of the adjustable ΔV_h^2 has been empirically identified at 20 mV^2, as a trade-off between speed, accuracy and residual fluctuations.

7.3 | Light-path tracking and circuit reconfiguration

This section discusses the procedure to perform CLIPP-assisted light-path tracking and closed-loop reconfiguration of the 8×8 switching fabric of Figure 7.1. For simplicity, a single optical signal is injected into an input port and routed in the circuit; however, as shown in Section 7.4, circuit reconfiguration can be performed even when several optical signals are simultaneously coupled to the input ports of the circuit.

A CLIPP-assisted feedback control scheme similar to the one discussed in Section 7.2 is applied to configure the circuit, exploiting both CLIPPs of all the MZIs involved in the routing operations. In this way, each switching element is monitored individually, regardless of the state of the other switches, and can be controlled by means of a simple local feedback loop with a single degree of freedom (e.g. actuator driving voltage). In addition, this method requires neither previous calibrations nor lookup tables, and it is also robust against power fluctuations of the input signals and mutual thermal cross-talk effect, as will be discussed in Section 7.5.

As a first example, Figure 7.5a shows light routing from input I_8 to output O_8. The configuration procedure is sequential, although simultaneous adjustment of different stages can be implemented with more advanced algorithms. At the beginning of the tuning operations all the heaters of the circuit are switched OFF and hence all the MZIs have random biasing points due fabrication tolerances. Figure 7.5($b_1 - b_2$) show the time-dependent electric signals of the CLIPPs during the circuit reconfiguration. These signals provide real-time information of the path of the light across the photonic chip. Figure 7.5(b_3) shows the optical signal that is simultaneously acquired by external PDs coupled at output ports O_6, O_7 and O_8.

As a first step (Tuning A), stage A is tuned to maximize the optical power in the lower output waveguide; this condition is reached when the difference between the signals provided by CLIPP A_8 (black dashed line) and CLIPP A_7 (blue dotted line) of Figure 7.5(b_1) is maximum. Once stage A is tuned, its state is continuously monitored and feedback locked, while the following stages of the circuit are sequentially tuned. In the second step (Tuning B), all the power is routed in the lower output waveguide of stage B, by maximizing the difference between the signals from CLIPPs B_8 (purple dash-

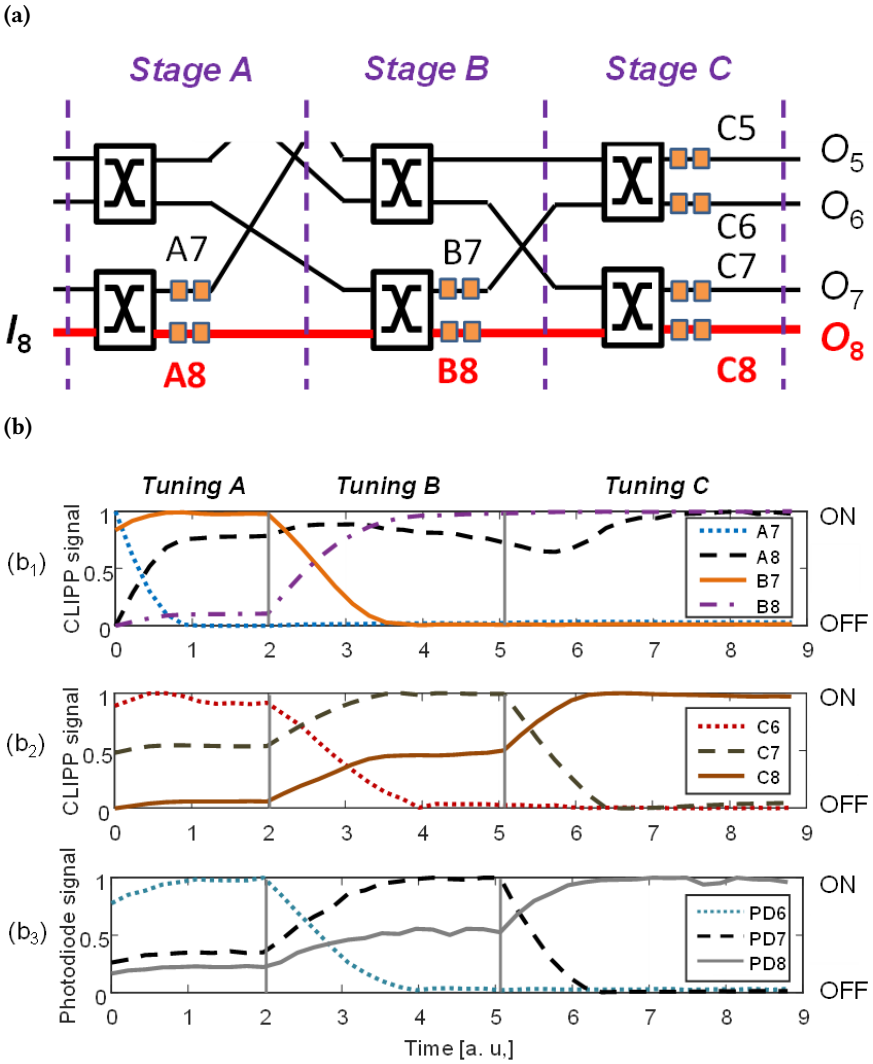


Figure 7.5 – *CLIPP-assisted light-path tracking and circuit reconfiguration. (a) An optical channel from input I_8 is routed toward the output O_8. (b) The stages of the switch fabric are tuned sequentially by exploiting the information provided by the CLIPPs placed throughout the circuit; (b_1) during the tuning of the stage A, the signal from CLIPP A_8 increases while A_7 decreases. B_7 and B_8 both increases since more power is routed to the fourth MZI of stage B; then the second stage is tuned in order to maximize signal from B_8. (b_3) Signals simultaneously measured by external PDs coupled to the output waveguides during the tuning procedure.*

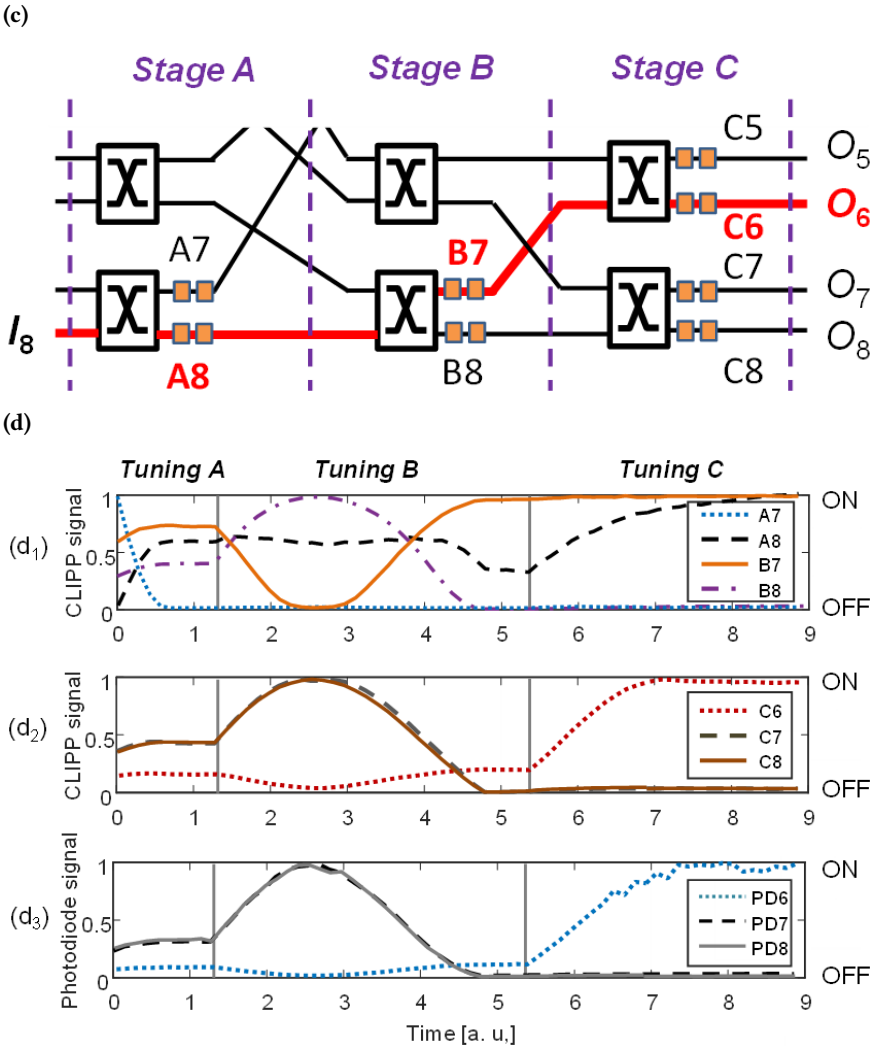


Figure 7.5 – *(c) and (d) show routing, light-path tracking and optical intensity at the output ports when input I_8 is routed toward output O_6.*

dotted line) and B_7 (orange solid line). Likewise, the third stage C is configured by looking at the signal provided by CLIPPs C_7 (grey dashed line) and C_8 (brown solid line) of Figure 7.5(b_2).

PD signals of Figure 7.5(c) confirm the effectiveness of the CLIPP-assisted reconfiguration procedure. At the end of the tuning operations, the intensity at output ports O_6 (cyan dotted line) and O_7 (black solid line) is minimized, while all the power is transferred to port O_8 (grey solid line). It is worthwhile to note that, even though some information on the current state of the circuit could be inferred from the output PD signals, CLIPP-assisted on-chip local monitoring provides direct information on the status of every single element of the entire architecture. For instance, during the tuning of the stage A, the three PD output O_6, O_7 and O_8 all increase since the MZI is redirecting the light to the lowest four ports of the switch fabric. Therefore, to optimize the working point of this MZI, all the eight output ports ($O_1 - O_8$) should be simultaneously monitored; in contrast, by exploiting on-chip monitoring only two CLIPPs (A_7 and A_8) need to be used. Similar considerations apply to any switching element whose output ports are not directly connected to external PDs.

In a second example, Figure 7.5(c)-(d) show the reconfiguration procedure to route signal I_8 to output ports O_6. Note that the optical signal at each stage is continuously monitored on-chip even after achieving the optimum tuning conditions, in order to assure robust locking of the MZI state against thermal crosstalk effects between adjacent actuated devices.

7.4 | On-chip Labelling and Discrimination

When multiple optical signals are simultaneously injected at different input ports of the switch fabric, CLIPP detectors can be used to identify channels coming from specific input ports regardless of the presence of other concurrent channels injected at the other input ports. However, in these conditions, both input ports of each MZI switch are fed with an optical signal, so that it is not possible to infer the MZI switching state by simply monitoring the light intensity of the two outputs.

The Pilot Tones technique, described in detail in Section 6.1, can be effectively used to label the different signal and make the CLIPP

discriminate each input. In this way, the reconfiguration of the entire circuit can be performed as in the single-input case described in the previous section.

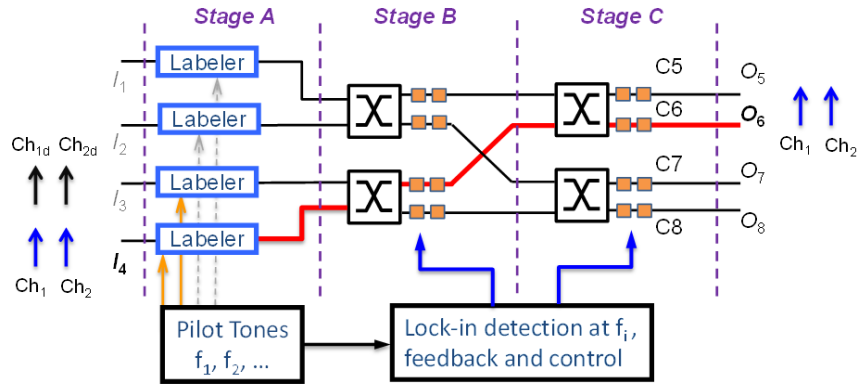
This work demonstrates that the labelling operations can be performed directly on-chip, allowing the channel identification procedure to be managed locally, without any constraint on the transmission system used to generate the input channels. As shown in Figure 7.6a, the four MZIs of stage A are employed as slow thermal modulators to label channels coming from port I_i with different tones f_i ($k = 1, 2, 3, 4$). The subsequent MZI switches are used to route the labelled signals through the 4×4 switch matrix identified by stages B and C. For clarity, in this section the same input port numbering as in Figure 7.1 is maintained, even though only even input ports are used.

To demonstrate lightpath tracking and broadband routing of concurrent signals, two channel pairs are simultaneously injected at two input ports of the switch fabric. Two signals Ch_1 and Ch_2, with carrier wavelength $\lambda_{Ch_1} = 1558.2\,\text{nm}$ and $\lambda_{Ch_2} = 1545.8\,\text{nm}$, and 10 Gbit/s ON-OFF keying (OOK) modulation are injected at input port I_8. At input port I_6, concurrent channels Ch_{1d} and Ch_{2d} are injected, that are obtained by delaying and decorrelating Ch_1 and Ch_2 though a fiber span of a few km.

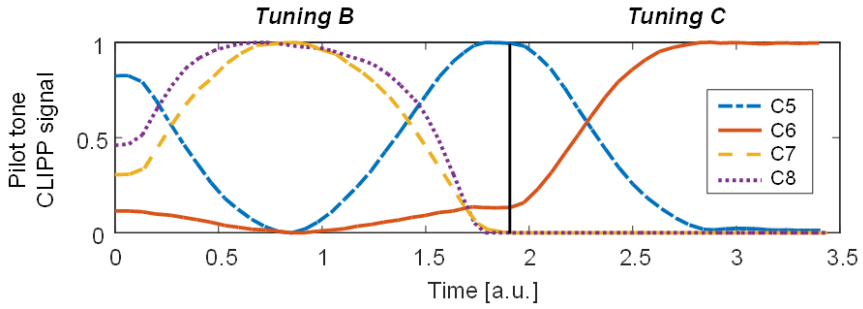
The pilot tones applied by on-chip labeler have a frequency $f_4 = 7\,\text{kHz}$ for Ch_1 and Ch_2, and $f_3 = 10\,\text{kHz}$ for Ch_{1d} and Ch_{2d}. The MZI labelers are biased in the linear working point (3 dB attenuation) of their characteristic and introduce a peak-to-peak intensity modulation of about 5%.

As an example, the routing of both channels $Ch_1 - Ch_2$ from input port I_8 to output port O_6 is considered. Figure 7.6b shows the time-dependent signal provided by the four CLIPPs of stage C ($C_1 - C_4$) after demodulation at frequency f_4 of the channels to be monitored and routed. First, the MZI of stage B is tuned to a switching state where the signals provided by C_7 and C_8 are minimized. Noteworthy, the presence of concurrent channels Ch_{1d} and Ch_{2d}, that are routed towards C_7 and C_8, does not introduce significant crosstalk in the CLIPP signal.

Mismatch in the demodulation frequency from the intended modulation tone produces a very low crosstalk signal, evaluated to be lower than $-50\,\text{dB}$ and mainly due to the noise level of the electronic



(a)



(b)

Figure 7.6 – *CLIPP-assisted lightpath tracking of concurrent signals discriminated by using on-chip labelling through pilot tones. (a) MZI of stage A are used as channel labeller adding a weak modulation tones at each input port. Two channels pairs are simultaneously injected at input ports I_6 (Ch_{1d}, Ch_{2d}) and I_8 (Ch_1, Ch_2) and labelled with tones $f_3 = 10\,\text{kHz}$ and $f_4 = 7\,\text{kHz}$, respectively. (b) By demodulating the CLIPP signal at frequency f_4, channel pair $Ch_1 - Ch_2$ can be can be monitored and routed through the switch fabric regardless of the presence of channel pair $Ch_{1d} - Ch_{2d}$.*

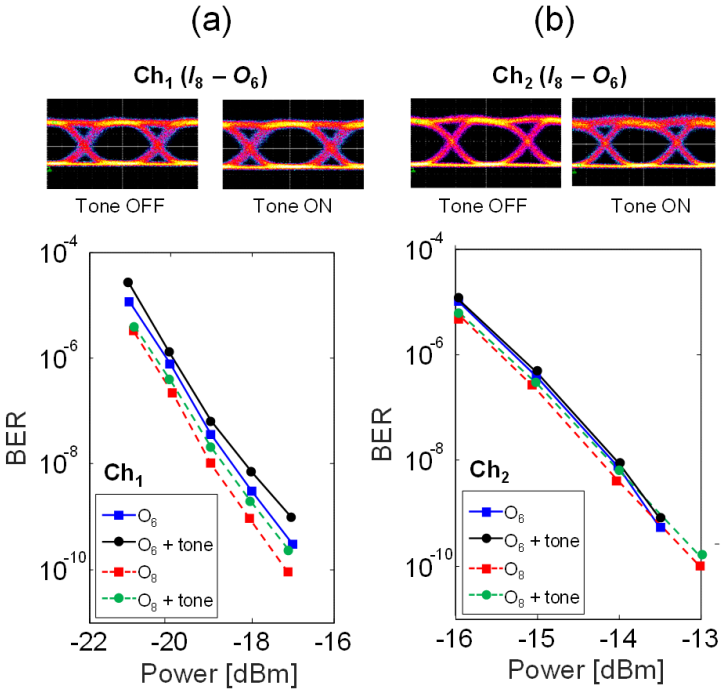


Figure 7.7 – *Impact of the CLIPP-assisted light-path tracking and routing on the quality of concurrent channels discriminated by using on-chip labelling. (a) Top panel: eye diagrams of Ch_1 transmitted though the path $I_8 - O_6$ with the pilot tone switched* OFF *(left) and* ON *(right). Bottom panel: BER curves measured along the paths $I_8 - O_6$ (solid lines) and $I_8 - O_8$ (dashed lines) with pilot tone switched* OFF *(squares) and* ON *(circles). (b) Eye-diagrams and BER curves of Ch_2 in the same cases considered in (a). No appreciable penalty is observed for both channels.*

front-end. Therefore, this perturbation is 20 dB lower than the signal provided by a frequency matched CLIPP at the OFF-state port of a MZI with 30 dB optical extinction. This result is confirmed by the CLIPP signals measured after the tuning of stage C. In fact, the signal measured by C_5 (dominated by the optical crosstalk of frequency matched channels $Ch_1 - Ch_2$ at port O_5) is even more pronounced than the signal provided by C_7 and C_8 (dominated by the frequency mismatched channels $Ch_{1d} - Ch_{2d}$).

The impact of on-chip channel labelling, discrimination and routing on the quality of the optical signals has been evaluated: Figure 7.7 shows the eye diagrams and bit-error rate measured on channels Ch_1

(a) and Ch_2 (b). The two channels are demultiplexed off-chip with a commercial free space tunable filter with a bandwidth of 0.3 nm. Eye diagrams show that neither distortion nor eye opening reduction are observed when the MZI labelers are switched ON, in agreement with results obtained in the case of pilot tones applied through off-chip modulators [96]. This is confirmed by Bit Error Rate (BER) curves, performed for both channels routed along paths $I_8 - O_6$ and $I_8 - O_8$. For each path configuration, the labelled channels are routed by using pilot tones, then the BER is compared with the tones ON and after switching them OFF. As shown in the curves, no significant power penalties associated to the use of modulation tones was observed.

7.5 | Active Compensation of Thermal Crosstalk

When tuning switch fabrics, the general approach is to create, during calibration tests, a look-up table that correlates the switching state of each element with the control signal required to tune it to the optimal working point [100]. This approach lacks of both flexibility and robustness since it cannot compensate dynamical temperature gradients, thermal crosstalk between elements, and ageing effects of the overall system. This section shows the effectiveness of the proposed feedback control tuning strategy to counteract mutual thermal crosstalk among the switching elements of the circuit.

The case sketched in Figure 7.8(a) is considered, where an optical signal coming from the stage A is routed by stages B and C to output port O_8. The focus is on the performance of the bottom-most MZI switch of stage B, while several reconfiguration events occur in the switch fabric. The optical crosstalk, evaluated as the optical power reaching the output port O_6, is monitored while three surrounding MZIs (highlighted in green in the figure) randomly switch their state from ON to OFF condition. Since switching power of each MZI is about 10 mW (see Section 7.1), this results in a total power ranging from 0 mW to 30 mW, with a variable combination of heat source position.

Figure 7.8(b) shows the time-dependent crosstalk at output port O_6 when the active thermal compensation of the MZI is OFF (green curve) and ON (blue curve). In this experiment the temperature of the entire silicon chip is stabilized with a thermo-electric cooler (TEC) inserted below the PCB. In the initial condition, the three surround-

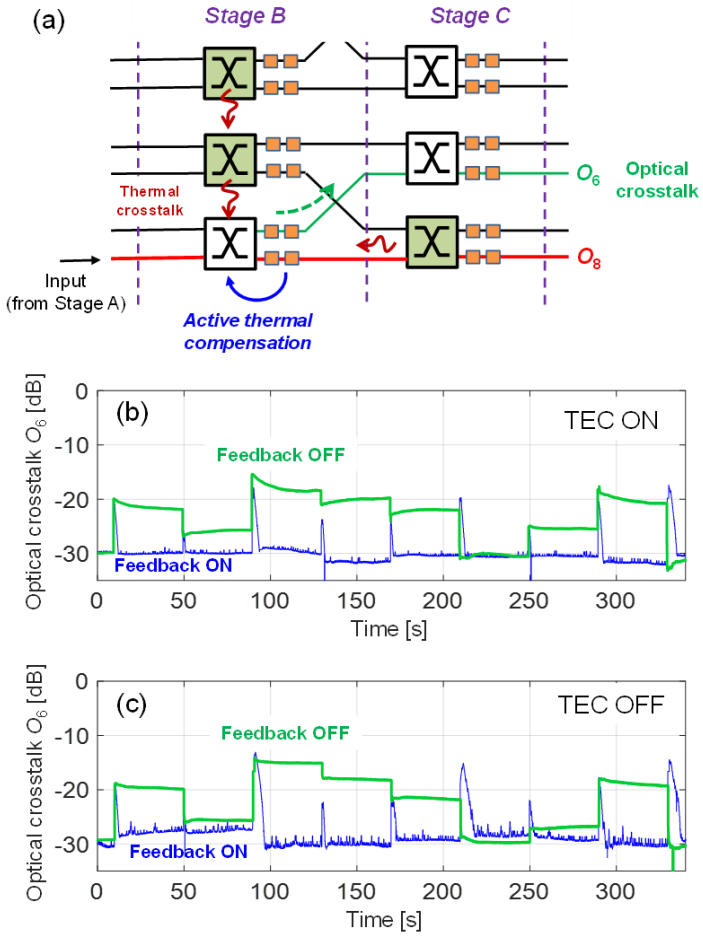


Figure 7.8 – *CLIPP-assisted compensation of mutual crosstalk effects induced by the switching elements of the circuit. The control algorithm implements the additional moving average filter described in Section 7.2 to reduce residual fluctuations. (a) Schematic of the considered experiment: when the state of three surrounding MZI switches (highlighted in green) changes, thermal crosstalk modifies the switching state of the bottom-most MZI of stage B (biased to route the light to output O_8), thus inducing optical crosstalk at other output ports (for instance O_6). Panels (b) and (c) show the measured optical crosstalk at port O_6 during several random switching events of the three surrounding MZIs, when active thermal compensation is OFF (green curve) and ON (blue curve), when the silicon chip is cooled (b) and uncooled (c). In both cases, after every circuit reconfiguration, feedback control recover the original crosstalk level (−30 dB), whereas a steady-state crosstalk as high as −15 dB is measured in open loop operation.*

ing MZIs are all switched OFF and a crosstalk signal of about −30 dB is measured. Then, the switching state of the three MZIs is randomly switched every 40 s. Without feedback control, the voltage on the MZI heater is kept constant. The crosstalk signal sharply increases after each circuit reconfiguration and, after some thermalization due to the TEC action, a residual steady-state optical crosstalk as high as −15 dB is observed. The blue curve demonstrates the effectiveness of active thermal compensation locally performed at the MZI site by using the CLIPP-assisted feedback control. An original optical crosstalk as low as −30 dB is rapidly recovered after the occurrence of every circuit reconfiguration. Noteworthy, Figure 7.8(c) shows that the benefits of CLIPP-assisted control remain also if the TEC underneath the sample is switched OFF. This result suggests the possibility to exploit the proposed approach for the reconfiguration and control of *uncooled* silicon photonic circuits.

7.6 | Conclusions

This work shows a new, original and deep insight on a very well known architecture for on-chip optical signal routing, an 8×8 Silicon Photonic switch fabric based on Mach-Zehnder interferometers. The main novelty is the use of CLIPPs as a effective, non-invasive optical power monitor after each switching stage of the routing matrix, enabling on-chip real-time monitoring of the working state of the router.

The use of the CLIPPs in local feedback control loops allowed the sequential tuning of the individual photonic elements to establish a routing path, also exhibiting great robustness towards thermal crosstalk. The switching state of each MZI can be locally monitored and the feedback operates in real time regardless of the switching state of the other MZIs of the circuit, even without an external temperature stabilizer. In addition, neither previous calibration of the working points nor lookup tables are required.

The routing of several 10 Gbit/s WDM signals simultaneously present at the input ports can be achieved by simply labeling the different channels with suitable pilot tones, thanks to the selectivity of the CLIPP readout algorithm to the different tones. Moreover, the technique is inherently insensible to channels power fluctuations, as explained in Section 6.1.

The CLIPP-assisted automated routing and control is scalable to switch fabrics with higher port counts, different network-on-chip topologies as well as generic photonic integrated architectures.

CHAPTER

EIGHT

UNSCRAMBLING LIGHT

Electronics and CLIPP detectors are the key elements to operate complex photonic circuits, improving their reliability and simplifying multi degrees-of-freedom optimizations into textbook manageable problems. In the following sections, I present a complete electronic-photonic system capable of automatically unscramble optical beams that have been arbitrarily mixed in a multi-mode waveguide.

The concept of the optical device was first proposed in 2013 by David A. B. Miller from Stanford University [101–105]. The Photonic Devices Group of Politecnico di Milano, lead by Prof. Andrea Melloni, implemented Miller's idea in a Mode Division Multiplexing (MDM) photonic integrated circuit, that can undo the scattering and mixing between the spatial modes through a mesh of silicon photonics tuneable beam splitters. The photonic chip is operated by a mixed-signal electronic platform, that allows the closed-loop control of up to 16 independent integrated photonic devices, monitoring their working point with CLIPP detectors and exploiting the pilot tones technique to distinguish the different signals.

The results of this work have been published in the prestigious journal *Light: Science and Applications* of the Nature Publishing Group, in the paper:

A. Annoni, **E. Guglielmi**, M. Carminati, G. Ferrari, M. Sampietro, D. A. B. Miller, A. Melloni, and F. Morichetti. "Unscrambling light - Automatically undoing strong mixing between modes". In: *Light: Science and Applications* 6.12 (Dec. 2017), e17110. ISSN: 2047-7538. DOI: 10.1038/lsa.2017.110. URL: http://www.nature.com/doifinder/10.1038/lsa.2017.110

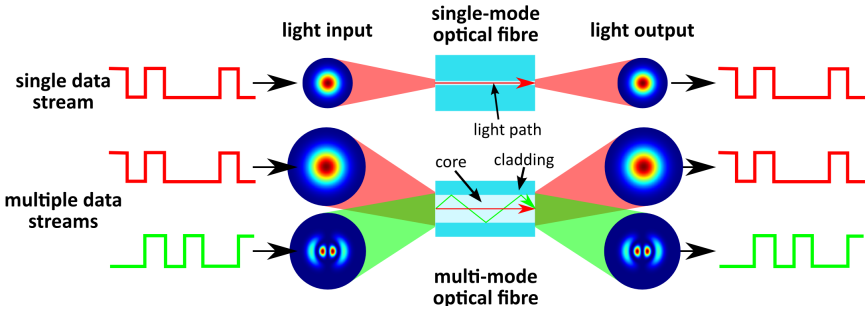


Figure 8.1 – *Working principle of Mode Division Multiplexing. On the top, a single-mode optical fiber is only able to transmit a single data stream at a certain wavelength. On the bottom, a multi-mode optical fiber exploits different spatial propagation modes to transmit multiple datastreams.*

8.1 | Mode Division Multiplexing

In the field of electronics and telecommunication, *multiplexing* is a technique that combines different signals together to create a new one that contains the information of all its components. The advantage is that the capacity of the transmission medium can be expanded, while keeping a single transmission link. The opposite procedure, called *demultiplexing*, separates the signal back in to its original components.

The multiplexing principle can also be applied to the optical telecommunications, where different data streams are transmitted at the same time in a single waveguide or fiber optic. Wavelength Division Multiplexing (WDM) is one of the most common techniques and exploits multiple wavelength carriers to avoid the interaction of the different signals.

Mode Division Multiplexing is an emerging technology that scales the capacity of a single wavelength carrier by using different propagation modes, that are the spatial configurations of the electric field propagating in a waveguide. The technique exploits the non-interaction of signals transmitted with *orthogonal* propagation modes, even if at the same carrier wavelength. Figure 8.1 shows a visual representation of the technique.

However, the propagation of light beams through scattering [106, 107] or multi-mode systems [108, 109] may affect the spatial coherence of the light. Although information is not lost, its recovery

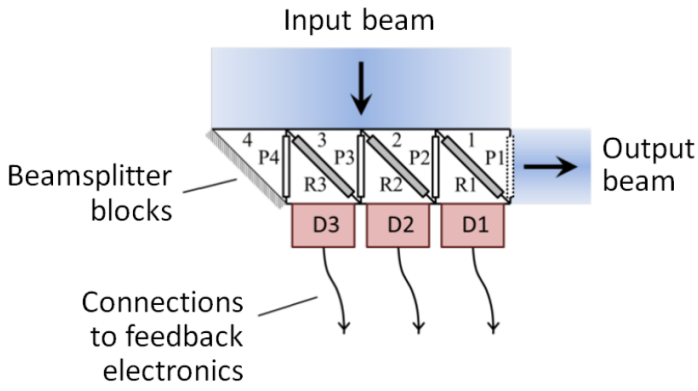


Figure 8.2 – *Schematic representation of a single channel light unscrambler. The light from a single beam is split into 4 different inputs and then recombined at the output by a system of tunable phase shifters and controllable reflectors. [102, 103]*

requires a coherent interferometric reconstruction of the original signals, which have been scrambled into the modes of the scattering system. These approaches require complex digital circuits with fast Analog-to-Digital Converters and high-performance Multiple-Input-Multiple-Output (MIMO) processors [110, 111], with speed and capacity limits, and high power consumption.

In the following section, an integrated optical circuit is presented to automatically unscramble the signals mixed by the non-idealities of the multi-mode link. The separation is performed directly in the optical domain thanks to an automatic electronic control of the device, exploiting the CLIPP as a non-invasive detector.

8.2 | Integrated Optical Modes Unscrambler

8.2.1 | Working Principle

The architecture of the device has been proposed in 2013 by Davis A. B. Miller [101], from Stanford University, that shows a conceptual design based on beam-splitters, tunable phase shifters and controllable reflectors. The complete and detailed description of the working principle of the device can be found in his paper, but follows a brief explanation of the tuning procedure to separate the mixed signals.

Figure 8.2 shows a schematic representation of the device from his paper: the light containing just 1 signal comes from the top and is split between 4 inputs, numbered from 1 to 4. P1-P2-P3-P4 are independently controllable phase shifters, R1-R2-R3 are tunable reflectors, and D1-D2-D3 transparent light detectors. The objective is to tune the elements of the system to collect all the light at the output beam. Normally it would be a 7 degrees of freedom optimization, but with this particular architecture the process is simpler and sequential.

First, the phase shifter P4 is tuned to minimize the power read by the detector D3 (after the reflection on R3). This optimization align two light beams in counter-phase: one from Input 4 shifted by P4 and reflected by R3, the other from Input 3 transmitted through R3. Second, the reflector R3 is tuned to minimize the power at the same detector D3. This operation regulates the amplitude of the same two light beans to be equal. Being tuned to be in counter-phase from the previous step, the two light beams completely cancel each towards the detector D3 and instead propagate to the next stage on the right.

The same two step optimization can be repeated again in the next stage: tuning P3 and R2 sequentially to cancel any light reaching D2, through destructive interference. When every stage is tuned, all the light coming from the 4 inputs is collected at the output.

The structure can be upscaled like in Figure 8.3 to handle 4 different input signals mixed together, and reconstruct them at the 4 outputs of the device. The tuning procedure is still sequential. First, the elements in the top row are tuned as already explained to collect *one* of the signals at the first output. Then, the procedure is repeated sequentially in the following rows of elements, reconstructing the other signals at a separate output.

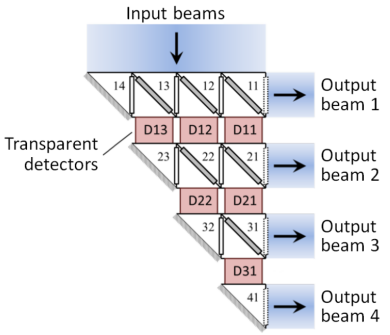


Figure 8.3 – *Upscaled 4 channel version of the light mode unscrambler. The light, split among the inputs, contains 4 different signals that are unscrambled and reconstructed at the 4 outputs. [102, 103]*

The orthogonality of the optical signals ensures that when one of them is completely collected at the first output, the others are entirely transmitted to the following row and none of their power is reaching

the same output.

However, in order for this extended optimization strategy to work, the detectors need to have two essential characteristics:

(i) The detector readout technique needs to be able to distinguish the each one of the 4 original signals. For example, when the optimization of the first row of elements is performed, the algorithm has to minimize the power of the signal to be collected at the first output. It is not enough to minimize the total power of the 4 signals combined.

(ii) The detectors need to be transparent and non-invasive, to allow the transmission of the remaining components to the following rows without any alteration.

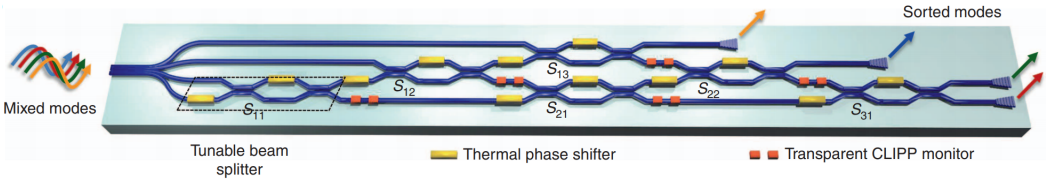
The CLIPP detector fulfills both of these requirement, for the on-chip realization of the device, being completely transparent and non invasive and allowing the identification of each signals with the Pilot Tones technique.

8.2.2 | Chip Design

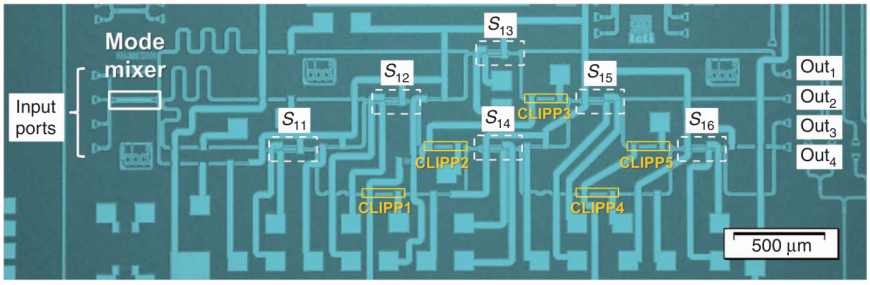
The photonic integrated circuit implementing Miller's idea has been designed using a mesh of Mach-Zehnder Interferometers (MZI) as the controllable reflectors, and thermo-optic actuators as tunable phase-shifters.

The architecture, shown in Figure 8.4, features 4 separate input channels unscrambled by 6 MZI arranged in a triangular matrix, similarly to what shown in Figure 8.3. Four orthogonal signals (Ch.A - Ch.D) are injected into the chip at the same time through a glass interposer. They are scrambled together by a short connection made with a multi-mode fiber, thus emulating a fiber optic with low dispersion that would be used in a real MDM transmission system. The link is then coupled to 4 single-mode waveguides splitting the light among the inputs. At this point, each waveguide has a portion of the optical power of each one of the input signals, at least 20%.

The particular arrangement of the MZI allows the reconstruction of the 4 input signal at any of the 4 output. The use of CLIPP detectors is essential to avoid any impact on the orthogonality of the optical modes: different losses along the paths of the mesh would make the reconstruction operation impossible by irreversibly mixing



(a)



(b)

Figure 8.4 – *(a) Implementation of the 4 channel mode unscrambler with 6 MZI arranged in a triangular matrix. (b) Photo for the fabricated chip.*

the signals. For this reason, tapping light out of the system through standard directional couplers is not an option. Without any information on the state of each MZI, the problem of unscrambling is a 4 output, 12 degrees of freedom non sequential optimization. The use of the CLIPP, instead, allows a considerable reduction of the complexity, dropping the problem to a series of 1 output, 2 degrees of freedom optimizations.

In theory, the structure should allow sequential 1 degrees of freedom optimizations. However, due to the high thermal crosstalk between the actuators before and inside the MZI, tuning the second element could affect the bias of the first one. Therefore, it is best to tune both heaters simultaneously, or to alternate between the two until a global optimum is reached.

8.3 | Electronic platform for tuning and locking

A mixed-signal electronic system allowing closed-loop control of 16 independent integrated photonic devices equipped with CLIPP transparent optical probes (−35 dBm sensitivity, 50 kHz speed) has been designed to control the mode unscrambler and is shown in

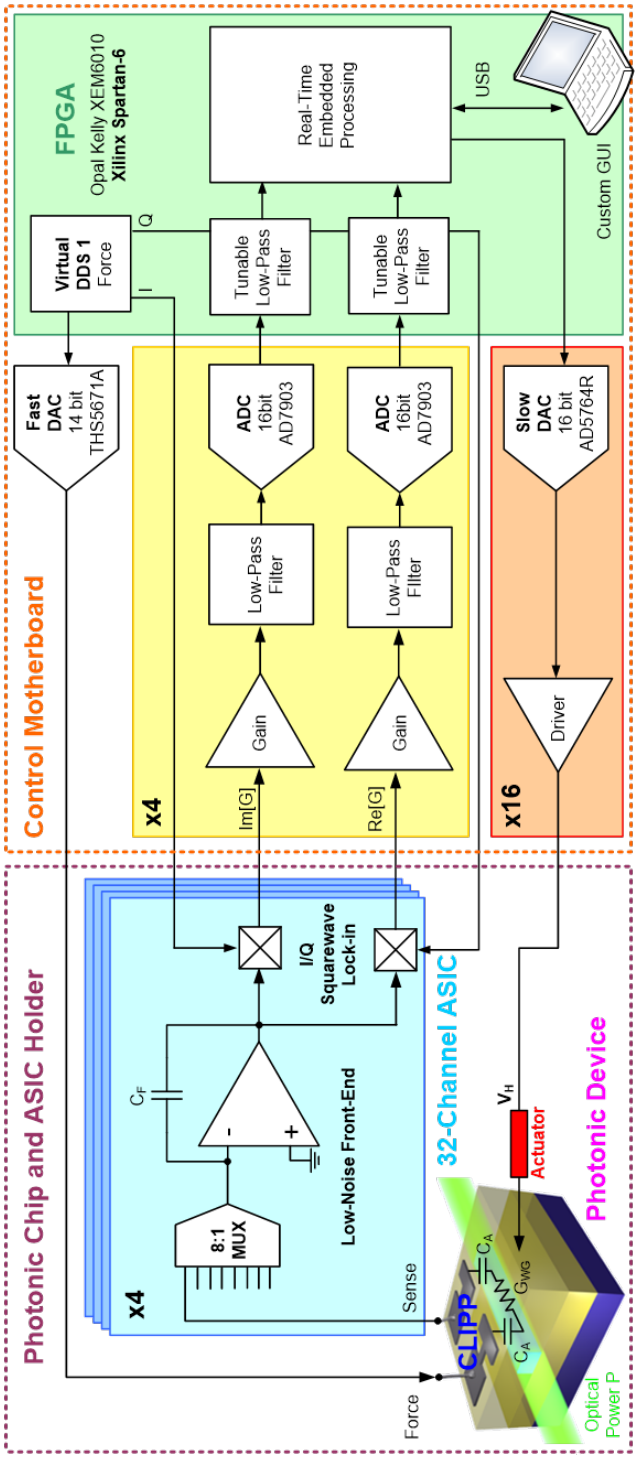


Figure 8.5 – *Control platform architecture including 32 input channels (4 chains with 8:1 input multiplexers) and 16 output parallel signals driving actuators (V_H).*

Figure 8.5 [112].

The simultaneous readout of all the CLIPPs integrated in the photonic circuit was made possible by a custom-designed multi-channel CMOS ASIC realized in a 0.35 µm AMS CMOS process, bridged to the silicon photonic chip and mounted on the same printed circuit board [66, 83]. The ASIC contains a low-noise front-end amplifier (100 fA/$\sqrt{\text{Hz}}$ noise, 100 dB dynamic range) followed by a fully integrated Lock-In system for the extraction of the in-phase and quadrature components of the light-dependent waveguide impedance [65]. The ASIC has four parallel readout channels, with each channel featuring an 8× input multiplexer to address up to a total of 32 CLIPPs. It is interfaced via conditioning chains to multiple ADCs and DACs driven by a Xilinx Spartan-6 FPGA (Field Programmable Gate Array) for real-time processing, including the generation and demodulation of multiple pilot tones for channel labeling and dithering-based feedbacks.

When the input modes A, B, C and D are simultaneously coupled into the chip, the CLIPP detectors can identify the power associated with each mode, regardless of the presence of other concurrent modes injected at other input ports and scrambled by the mode mixer. To enable mode discrimination, each mode is labelled with a weak pilot tone before being coupled to the silicon chip. As mentioned in Section 6.1, previous studies have demonstrated that the labelling operation can be performed without affecting the quality of the signals [27, 96].

Sinusoidal tones with 5% peak-to-peak relative intensity are generated through external MZI lithium niobate modulators biased at the linear working point (3 dB attenuation). The tone frequency $f_q = \{4\,\text{kHz}, 7\,\text{kHz}, 10\,\text{kHz}, 11\,\text{kHz}\}$ of the q-th mode ($q = A, B, C, D$) was suitably chosen to avoid mutual overlap of the harmonics that can be generated by the non-perfectly linear response of the modulators. Different tone waves (for example, square-waves) as well as different biasing points of the modulator could also be used to reduce the loss associated with tone generation, but such tones would require a more careful selection of the tone frequencies in order to avoid mutual overlaps.

To identify the q-th mode, the CLIPPs are demodulated twice, first at the readout frequency f_{AC} around which the CLIPP sensitivity to optical power variations is maximized ($\sim$ 100 kHz in the

reported experiments), and then at the frequency f_q of the mode to be monitored. The second demodulation produces a very low crosstalk signal (lower than −50 dB) at a frequency different from f_q, which is mainly due to the noise level of the electronic front-end [27, 83].

The four output signals from the ASIC are acquired and conditioned by the FPGA-based electronic platform. The second demodulation at the frequencies f_q is performed digitally, and the results are processed by tuneable Infinite Impulse Response (IIR) filters (down to 4 Hz bandwidth) to identify the power level of each mode. The FPGA drives the 12 heaters of the silicon photonic chip to tune and lock the 6 MZIs to the desired working points.

Figure 8.6 shows how the digital demodulation and filtering is implemented in the FPGA of the controller board. An internal Direct Digital Synthesizer (DDS) is used to create a sinusoid at a tunable frequency, fed to a generation logic that sums the bias for the external modulators and sends the data to a Digital-to-Analog Converter (DAC). At the same time, the sinusoid is sent to the acquisition logic and used in a digital multiplier to perform the demodulation. Thanks to the parallel processing power of the FPGA, it is simple to perform both the demodulation and the simple CLIPP readout, obtaining the information on the average power and the pilot tone at the same time.

8.4 | Experimental measurements

The tuning process of the mesh is performed through the sequential control of the MZI, because each element affects the following ones. As shown in Figure 8.7, the first MZI to be optimized is the one marked as S1, followed by the MZI S2 and S3. By using the pilot tone technique, the power of a chosen mode is minimized at bottom output of each MZI, thus reconstructing the signal at the Out_1. Any of the 4 initial signals can be collected at Out_1 while the other channels are entirely diverted to the MZI S4 and S5, thanks to the orthogonality between the propagation modes. The stages S4 and S5 are tuned next, recollecting one of the three remaining signals to Out_2. Finally, the stage S6 separates the last two signals at Out_3 and Out_4.

The CLIPP detector offers the possibility to monitor the configuration of each MZI as a function of the phase shift introduced by

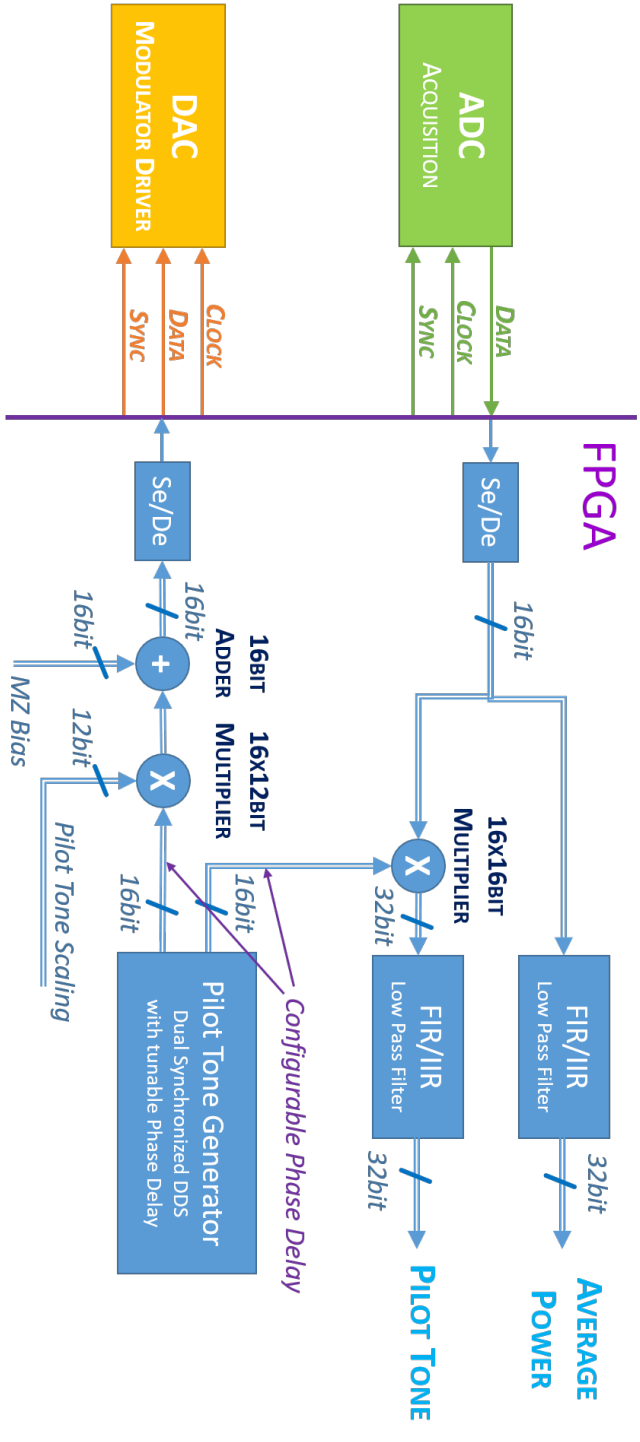


Figure 8.6 – *Firmware implementation of the Pilot Tones demodulation scheme.*

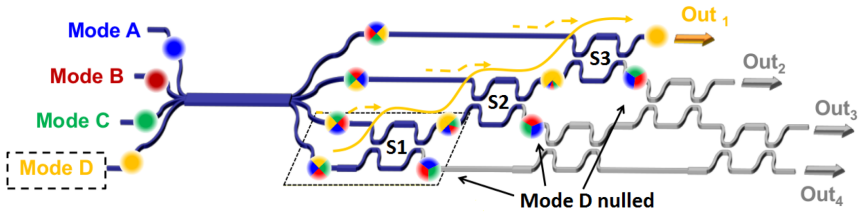
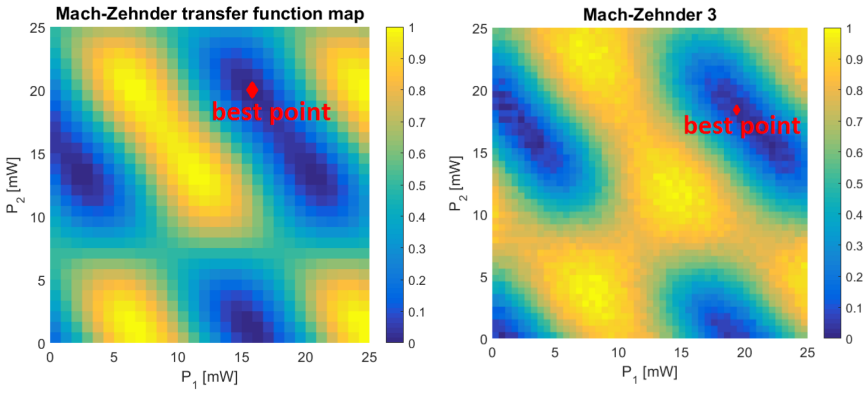


Figure 8.7 – *Tuning of the first MZI row of the mesh, by minimizing Mode D on the bottom output of each stage, thus collecting it at* Out_1*. Colors are used to represent the mixes of the different modes as they travel through the mesh.*



(a) **(b)**

Figure 8.8 – *Complete maps of the signal of the CLIPP as a function of the power dissipated* (mW) *by each thermal actuator. (a)* 30×30 *map of the stage S1. (b)* 50×50 *map of the stage S3.*

its two thermal actuators. By sweeping the control voltage of both actuators, a complete 2D map of the signal read by the CLIPP is obtained.

In the first case, only one channel is injected into both inputs of the first stage S1. In the map, shown in Figure 8.8a, it is possible to identify the best bias point of the stage, being where the average optical power read by the CLIPP is minimized. The map, containing 30×30 points, was obtained by sweeping each actuators to induce a maximum shift of about 2π, with 30 steps linear in power. The resolution of the map can be chosen through the software settings of the electronic board, affecting the total time required for the scan.

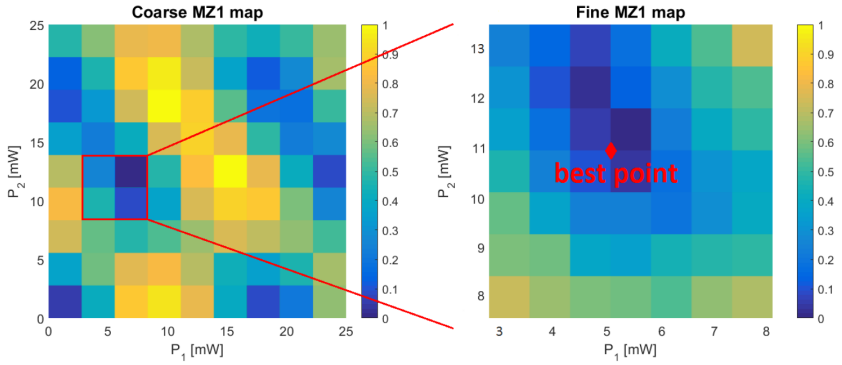


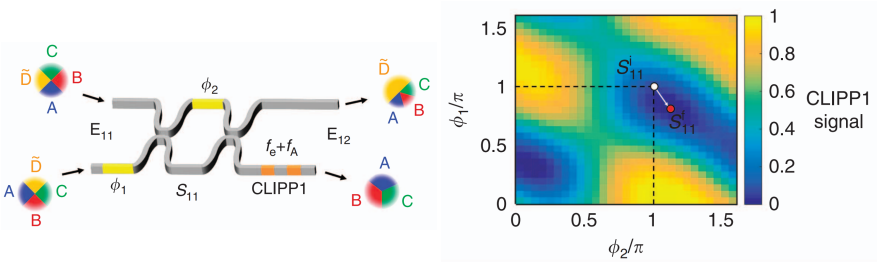
Figure 8.9 – *Double coarse-fine scan of the MZI, to reduce the number of measurement points and speed up the algorithm. The first coarse scan is a map of* 9×9 *points, while the fine scan is made by* 7×7 *measurements and limited around the best point found in the coarse map.*

Figure 8.8b shows a finer map of a different MZI with 50×50 points.

Different strategies can be tested to increase the speed of the algorithm to find the best bias point of each stage (this Master's thesis work [113] compares different interesting algorithms, like transfer function interpolation and genetic algorithms). Figure 8.9 shows the results of a double coarse-fine scan strategy, where an initial coarse map of 9×9 points is measured to find the general area of the local minimum, followed by another 7×7 scan in a limited area around the best point of the previous scan. With this approach, the optimum bias point can be found almost 20 times faster, thanks to the limited number of measurements required: only $9 \cdot 9 + 7 \cdot 7 = 130$ compared to the 2500 points of a full 50×50 scan.

The final application requires the mesh to be able to unscramble 4 signals present at the same time in each MZI. Figure 8.10a graphically represents the optimization problem of the stage S1, where 4 concurrent modes enter from both inputs and Mode D has to be minimized at the bottom output port. As already mentioned, the pilot tone technique is essential to discriminate each signal and the MZI maps (Figure 8.10b) are powerful tool to optimize the bias of each stage, provided that the CLIPP signal is demodulated twice to select the pilot tone.

The effectiveness of the mode identification performed by the



(a) (b)

Figure 8.10 – *Tuning of the stage S1 with 4 concurrent modes present at the inputs. (a) Schematic representation of the optimization problem. (b) MZI map identifying the best bias point.*

CLIPP and its use for the monitoring of the tuneable beam splitters of the mesh is shown in Figure 8.11. The three maps show the signal provided by $CLIPP_1$ when the beam splitter S_{11} is tuned by changing the phases ϕ_1 and ϕ_2 in three different cases:

(a) Only one mode (Channel D) is injected at the inputs of the mesh.

(b) Two modes (Channels B and D) injected into the mesh. The presence of concurrent channels strongly modifies the map, hindering the biasing of the MZI at the proper working point for mode D reconstruction.

(c) Two modes (Channels B and D) injected into the mesh, with Channel D labelled through a pilot tone. The CLIPP is read with a double demodulation to distinguish the Channel D, enabling monitoring and control of the state of the MZI with no side effects associated with the presence of the concurrent channels.

In the experiments, the system was set to perform the CLIPP readout in 50 ms, allowing an automatic 2D scan of each MZI (30×30 pixel map, as in Figure 8.8a) in $\sim$ 45 s and the automated full reconfiguration of the mesh (starting from unbiased MZIs) with an optimized coarse-fine tuning algorithm in $\sim$ 15 s. Once the mesh is configured, tracking of time-varying mixed modes can be performed on a time scale of a few hundred milliseconds, to compensate for drifts of the optical elements and of the mode scrambling.

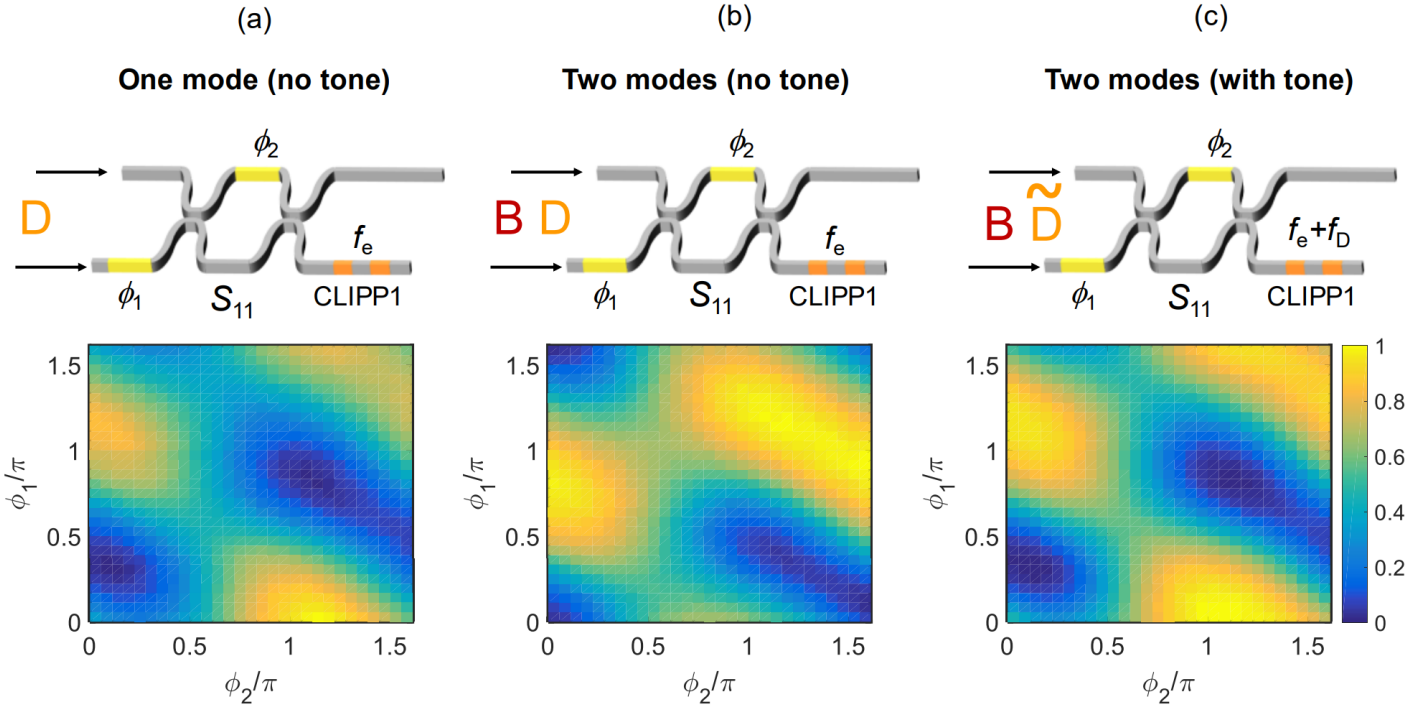


Figure 8.11 – *CLIPP-assisted monitoring of the tuneable beam splitters of the mesh by using mode labelling. Maps show the signal measured by CLIPP$_1$ during the tuning operation of the beam splitter S_{11} as a function of ϕ_1 and ϕ_2, when: (a) only mode D is injected in the mesh, concurrent modes are off and no tone is applied; (b) concurrent mode B is switched on, no tone is applied and the CLIPP is read at frequency f_e; (c) concurrent mode B is switched on, a tone at frequency f_D is applied on mode D and the CLIPP is read at frequency $f_e + f_D$.*

By following the design rules and electronic readout optimization strategies discussed in Section 4.1.4 and Appendix B [71, 83], the CLIPP readout time can be reduced by two orders of magnitude, while maintaining a sensitivity better than −20 dBm, thus enabling the tracking of mode mixing variations occurring within a millisecond range.

CHAPTER

NINE

CONCLUSIONS AND FUTURE WORK

9.1 | Conclusions

CLIPP-assisted control Electronics can boost modern Silicon Photonic technologies, by overcoming their intrinsic limitations. This thesis contributes to three aspects the research: the optimization of the Detector itself, the improvement of the Electronics to read it, and the development of novel Applications.

The knowledge of the CLIPP detector has been deepened through experimental measurements, modeling and simulations. In particular, the key components of the electrical model of the device have been identified and linked to the geometrical parameters of the detector. The photonic circuit substrate plays an important role in the operation of the device: it has been shown how an insulating substrate, or even its complete removal, goes favorably in the direction of a more sensitive CLIPP. The CLIPP miniaturization is tied to the optimal readout frequency f_{AC}, that is defined by the geometrical parameters and should be minimized with a $1:2$ ratio between the length of the electrodes and their distance. Simulations show that CLIPPs smaller than 50 µm pose a challenge to the electronic design, implying $f_{AC} > 50\,\text{MHz}$.

The theoretical analysis concludes with practical layout guidelines for the integration of the CLIPP detector in dense photonic circuits. Particular attention should be devoted to the minimization of C_E, direct coupling between the electrodes and main parasitic capacitance of the detector. *Force* and *Sense* paths should be kept as far as

possible, with clever routing from the electrodes to the pads, distant bonding wires and PCB traces, until the corresponding electronics. In optically dense chips where several CLIPP devices are integrated, the metal interconnections can be minimized by sharing the *Force* pad among the CLIPPs. Furthermore, electrode sharing topologies between CLIPPs and thermal actuators may be employed to reduce the number of pads. Finally, no-fill zones should be included in the design around the CLIPP detectors ($\sim 30\,\mu m$) and the Force ($\sim 8\,\mu m$) and Sense ($\sim 3\,\mu m$) connections, to avoid the introduction of dummy metal tiles from the manufacturer in critical locations of the design, that would increase C_E. CLIPP following these design guidelines have been fabricated within the context of the ICT-STREAMS project, obtaining C_E as low as 1 fF and never exceeding 5 fF, an exceptional result compared to previous fabrications where the C_E was hundreds of fF, sometimes reaching 1 pF.

A new CLIPP architecture, called Embracing CLIPP, exploits deep n++ implantations at the same level of the waveguide, available in Active Silicon Photonic technologies, to enhance the capacitive coupling with the waveguide. The device has been fabricated with IMEC technology and shows exceptional performance despite the high process variation. The Embracing CLIPP ($L_{TOT} = 400\,\mu m$, $L = 100\,\mu m$, $D = 200\,\mu m$, $W \approx 2.7\,\mu m$), with n++ implantations at 400 nm from the waveguide, achieved the record of the lowest detectable power measured so far with a CLIPP, −55 dBm. At the same time, the non-invasive nature of the device is still unaltered.

The Electronics to read the CLIPP is based on a Lock-In Demodulation scheme to sense the resistive waveguide despite the capacitive nature of the detector. The key aspects of the readout circuit have been discussed, highlighting the importance of using a TIA with capacitive feedback and minimizing the noise contributions of the input capacitance and the Lock-In filter. Input leakage currents needs to be handled with robust bias networks to avoid the saturation of the amplifier. Additionally, the choice of the filter bandwidth implies a response time vs. sensitivity tradeoff, verified through experimental measurements down to a resolution of 220 pS for very narrow filtering (1 Hz).

The integration of the control electronic in an ASIC is essential for multichannel applications where a photonic circuit is monitored by tens of CLIPP detectors. However, the n-type and p-type implan-

tations of the CMOS technology can create parasitic photodiodes that aggravate the problem of leakage currents and make the system sensitive to the environmental light. Pseudo-resistors made by active CMOS transistors are a compact integrated solution to bias TIA with capacitive feedback and to handle the leakage currents. After a comprehensive analysis of the state of the art, a new pseudo-resistor structure has been designed, realized and tested in AMS CMOS 0.35 µm technology. The device is tunable through floating voltage generators, carefully designed to avoid the introduction of parasitic capacitances that would impair the frequency performance of the pseudo-resistor. The device is capable of synthesizing a tunable resistance from 20 MΩ to 20 GΩ. Large signal non-linearities have been designed to achieve a dynamic reduction of the output offset when the AC signal is applied. For example, in presence of a 1 nA parasitic current, and a 500 mV sinusoidal signal, the output offset is reduced from 260 mV to less than 50 mV when the pseudo-resistor is set to 260 MΩ (bias of 430 mV). Furthermore, it is highly symmetrical to handle sinusoidal signals up to 10 MHz.

The CLIPP is a formidable tool to monitor the state of a photonic circuit and use the information to implement closed-loop control algorithms. The Pilot Tones and Dithering techniques offer the possibility to monitor specific signals or to extract the derivative of the optical components transfer function. Furthermore, they make the measurement insensitive to the parasitic effects and drifts, improving the robustness of advanced control algorithms and potentially overcoming the effect of the light in the substrate.

CLIPPs have been used to control a very well-known 8×8 router architecture, showing light path tracking and automatic reconfiguration. Each switching element can be tuned sequentially in less than 500 ms with very simple min/max chaser algorithms. Routing of multiple WDM signals through the matrix has been demonstrated with the pilot tones technique, that allows to track each signal independently with more than 50 dB of isolation. Thermal crosstalk effects between the switching elements have been counteracted with local feedback loops, achieving a stable optical crosstalk level of −30 dB in both cooled and uncooled cases.

CLIPPs have also been applied to a Mode-Division Demultiplexer photonic integrated circuit, a novel application that requires non-invasive monitoring to avoid disruption of the orthogonality of the

spatial modes. The employment of CLIPPs in strategic points of the circuit allows to reduce the tuning complexity from a 12 degrees of freedom global optimization on 4 outputs, down to simpler 2 degrees of freedom sequential optimizations on single outputs. Tuning of the chip has been achieved with a flexible FPGA-based multichannel platform allowing simultaneous monitoring and control of multiple CLIPPs and actuators of the circuit. The system can perform a fine 2D scan of each MZI element (30×30 pixel map) in $\sim$ 45 s. The 2D scans with the Pilot Tones active proved the effectiveness of the mode identification, even if the signals are at the same wavelength. The automated full reconfiguration of the mesh (starting from unbiased MZIs) with an optimized coarse-fine tuning algorithm has been achieved in $\sim$ 15 s. By optimizing the design of the CLIPP, the readout time can be reduced by two orders of magnitude, while maintaining a sensitivity better than -20 dBm, thus enabling the tracking of mode mixing variations occurring within a millisecond range.

9.2 | Future Work

My dissertation has shown the potential of the CLIPP detector and the new possibilities it unlocks in both well-known and innovative photonic circuits. The research should not stop, as there are still some steps left before this disruptive non-invasive detector can *invade* every photonic system to come.

The experimental measurements gave an additional insight on the role of the substrate, that is flooded with light when fibers are coupled to the photonic chip through gratings or butt-coupling. Its contribution is dependent on the optical power injected into the chip and can be detected by other CLIPPs in the circuit. Although Pilot Tones and dithering techniques can effectively ignore the crosstalk thanks to their signal selectivity (provided that the modulations are performed on-chip), the phenomenon needs to be investigated further. The elimination of the substrate entirely could solve the problem and would improve the sensitivity of the CLIPP at the same time. Thinning the substrate is also a viable alternative, because it would make the grounding of the chip more effective, isolating the different detectors by sweeping away the carriers that are generated in the substrate.

The time response of the control system is currently limited by the readout of the CLIPP, that is designed for maximum resolution. New systems should target a faster reaction time, possibly reaching the ms range, to compensate abrupt changes of the working point. To work around the speed-resolution trade-off, the electronics could provide two parallel readout chains: one high-speed to be used for prompt compensation of abrupt events, and the other high-resolution for the precise tuning of the working point. Additionally, the sensitivity of the CLIPP could be increased with a further optimization of the design.

Power dissipation of the system is the next challenging aspect to be improved: the main consumption is currently due to the FPGA platform, in particular the thermal actuator drivers and the acquisition chains to convert the signal to the digital domain. However, the digital control is not the only option: low-power analog feedback loops can be designed and integrated directly into the ASIC, providing a tailored control system for specific optical components. With this approach, the power consumption could be greatly reduced and be comparable to the power dissipation of the thermal actuators.

Integrating the complete control system in the ASIC is an important milestone for the development of compact CLIPP-assisted photonic systems. The electronic and photonic chip could be assembled together, profiting from the knowledge of the scientific community on Systems-on-a-Chip (SoC) and on the fabrication of extremely complex MEMS. The European Project ICT-STREAMS is already working in this direction, pushing the research effort towards new, power efficient, Tb/s, optical on-board interconnection paradigms.

Finally, the new exciting frontier of innovation in the field is the monolithic integration of photonics and electronics on a single Electronic-Photonic Integrated Circuit. If EPICs live up to their name, Electronics would not only boost Photonics: the two technologies would blend together, offering the best of both worlds.

LIST OF PUBLICATIONS

A list of the publications and original contributions that are fruit of this thesis is here provided.

Journal papers

A. Annoni, **E. Guglielmi**, M. Carminati, G. Ferrari, M. Sampietro, D. A. B. Miller, A. Melloni, and F. Morichetti. "Unscrambling light - Automatically undoing strong mixing between modes". In: *Light: Science and Applications* 6.12 (Dec. 2017), e17110. ISSN: 2047-7538. DOI: 10.1038/lsa.2017.110. URL: http://www.nature.com/doifinder/10.1038/lsa.2017.110

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Appendices

APPENDIX

ONE

NON-LINEARITY OF THE CLIPP

The electrical response in terms of conductance variation ΔG_{WG} of the CLIPP to an optical power P_{opt} is sub-linear. This aspect was never mentioned in the previous sections but has an important effect when using the pilot tones or the dithering technique. First, let us evaluate the non-linearity on an optical power variation, expressed as:

$$P_{opt} = P_0 + \Delta P$$

where P_0 is the initial optical power and ΔP represents a generic variation.

The waveguide conductance G_{WG} can, in turn, be expressed as a function of the optical power:

$$G_{WG} = G_{dark} + k \left(P_{opt}\right)^{\alpha}$$

where G_{dark} is the conductivity of the waveguide in the absence of light, k is the sensitivity coefficient of the CLIPP, and α is the non-linearity exponent of the CLIPP conductance response. During the years, non-linearity exponents $0.5 < \alpha < 1$ have been measured in different CLIPP realizations in various technologies.

By substituting the expression of the optical power:

$$G_{WG} = G_{dark} + k \cdot P_0^{\alpha} \cdot \left[1 + \frac{\Delta P}{P_0}\right]^{\alpha}$$

Applying the approximation $(1 + x)^{\alpha} \sim 1 + \alpha x$:

$$G_{WG} \approx G_{dark} + k \cdot P_0^{\alpha} \cdot \left[1 + \alpha \frac{\Delta P}{P_0}\right]$$

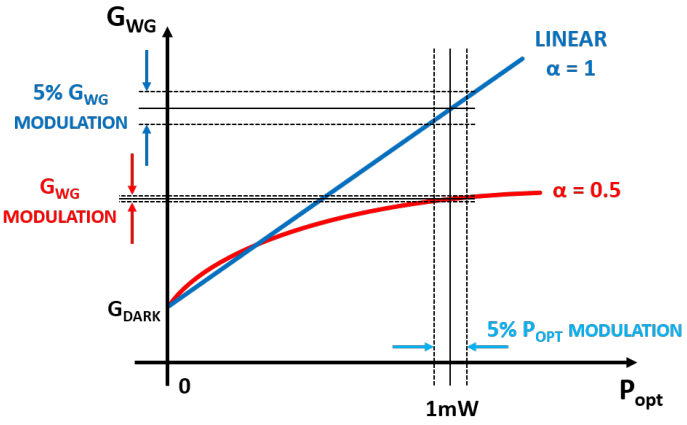

Figure A.1 – *Visual representation of the effect of the non-linearity of the CLIPP response on a pilot tone modulation. An optical modulation of 5% of the average power would lead to a 5% conductance modulation if the response were linear. Instead, if $\alpha = 0.5$, the conductance modulation is considerably reduced at higher average optical power.*

Therefore, the conductance variation ΔG_{WG} due to the optical power variation can be approximated as:

$$\Delta G_{WG} \approx k \cdot P_0^{\alpha} \cdot \alpha \frac{\Delta P}{P_0}$$

This means that the same optical step ΔP might cause different conductance signals depending on the average power P_0 in the waveguide. For example, if $\alpha = 0.5$, $\Delta G_{WG} \approx k \cdot \frac{1}{2} \frac{\Delta P}{\sqrt{P_0}}$. The same power step ΔP causes an electrical signal 10 times lower if the average power is increased by 20 dB (a factor 100). Instead, if $\alpha = 1$ the CLIPP response is linear and ΔG_{WG} is not dependent on the average power P_0.

A similar analysis can be performed when considering an optical modulation due to a pilot tone or dithering. In these cases, the optical power in the waveguide can be expressed as:

$$P_{opt} = P_0 + A \sin\left(2\pi f_{tone} \cdot t\right)$$

where P_0 is the non-modulated optical power, A is the amplitude of the optical modulation, and f_{tone} is the frequency of the pilot tone or dithering sinusoid. The ratio $\frac{A}{P_0}$ is defined as *modulation depth*.

By substituting the expression of the optical power and applying the same approximations:

$$G_{WG} = G_{dark} + k \cdot P_0^{\alpha} \cdot \left[1 + \frac{A}{P_0} \sin\left(2\pi f_{tone} \cdot t\right)\right]^{\alpha} \approx$$
$$\approx G_{dark} + k \cdot P_0^{\alpha} \cdot \left[1 + \alpha \frac{A}{P_0} \sin\left(2\pi f_{tone} \cdot t\right)\right]$$

Therefore, the conductance variation ΔG_{WG} due to the modulated tone can be approximated as:

$$\Delta G_{WG}|_{tone} \approx k \cdot P_0^{\alpha} \cdot \alpha \frac{A}{P_0}$$

Showing the same dependence on the average optical power. A qualitative visual representation of the phenomenon is shown in Figure A.1.

APPENDIX

TWO

CLIPP SPEED ANALYSIS

The analog front-end has an equivalent input noise that can be filtered with wide or narrow bandwidth depending on the desired Signal-to-Noise Ratio (SNR) needed by the application. A theoretical analysis has been performed to quantify what is the minimum time constant of the Lock-In filter (highlighted in the scheme of Figure B.1) necessary to read the signal coming from the CLIPP, as a function of the expected optical power in the waveguide.

Since it is the time constant of the filter of the readout chain, this is an evaluation of the time required for a single measurement of the sensor and it is dependent on the CLIPP structure, the *Force* signal amplitude and the wanted SNR. If a higher time constant is chosen, compared to the minimum suggested by the results, a higher SNR is obtained. In equations:

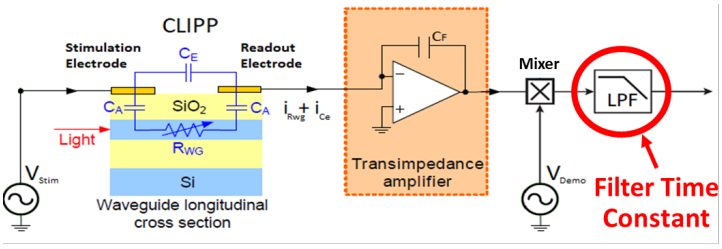

Figure B.1 – *Schematics of the front-end circuit that reads the CLIPP. Highlighted is the filter time constant that sets the speed of the measurement and the achievable resolution.*

$$SNR = \frac{V_{AC} \cdot \Delta G_{WG}}{S_I \sqrt{\frac{1}{4T_C}}}$$

The analysis has been conducted using the numerical results of the experimental measurements of the CLIPPs, presented in Chapter 3, in particular the "Conductance variation (S)" vs "Optical Power (dBm)" plot at $f_{AC} = 1\,\text{MHz}$. Additionally, the equivalent input current noise of the TIA used for this analysis is $S_I = 240\,\text{fA}/\sqrt{\text{Hz}}$, noise of the CLIPP readout ASIC [83] evaluated at 1 MHz.

It is very important to note that the minimum time constant of the filter needed for a specific application does not only depend on the aforementioned sensor conditions (such as the power in the waveguide, CLIPP structure, *Force* signal amplitude, wanted SNR), but also on the specific use of the signal in the application. To clarify this concept, the following sections will evaluate three different common use cases of CLIPP detector.

B.1 | Detecting a given optical power

This scenario evaluates the filtering required to detect a given optical power with a desired SNR, using as a reference the condition with no optical power in the waveguide (in the following simply called *dark condition*).

The useful signal is the whole signal variation caused by the light at the output of the Lock-In Amplifier compared to the *dark condition*. The results of the analysis, assuming a *Force* signal amplitude of 10 V and a minimum target SNR of 3, are shown in Figure B.2 for each measured CLIPP. Some results from other CLIPPs fabricated with the technology from IME are also included for comparison. These CLIPPs from IME have been tested at 1500 nm, so a smaller signal and consequently a higher time constant is expected due to the lower energy of the photons.

As the optical power decreases, the useful signal becomes smaller and smaller and requires a narrower filter, that is a higher time constant, to be distinguishable from the noise of the electronic front-end. The CLIPPs with higher sensitivity, such as the Embracing CLIPPs E5 ($L_{TOT} = 400\,\mu\text{m}$, $L = 100\,\mu\text{m}$, $D = 200\,\mu\text{m}$, $W \approx 2.7\,\mu\text{m}$, $d_{impl} = 400\,\text{nm}$) and E6 ($L_{TOT} = 120\,\mu\text{m}$, $L = 30\,\mu\text{m}$, $D = 60\,\mu\text{m}$,

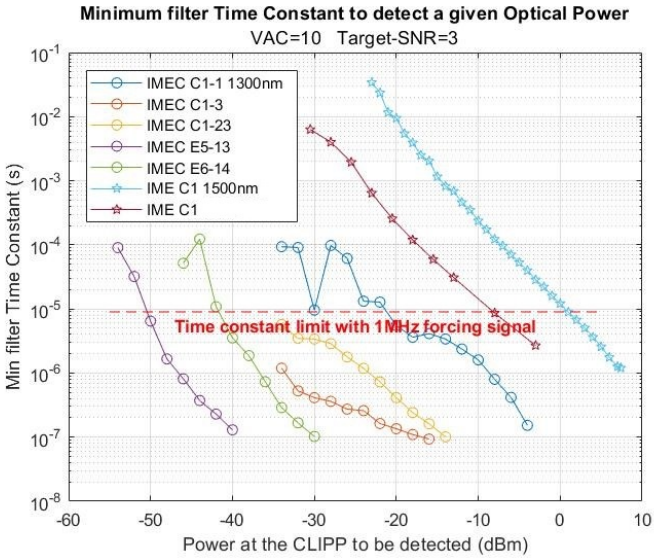

Figure B.2 – *Improvement of performance of the CLIPP detection (in terms of reducing the Lock-in time constant, i.e. of faster response) as the optical power in the waveguide increases.*

$W \approx 2.7\,\mu m$, $d_{impl} = 400\,nm$), require less filtering to detect the same optical power.

Since the readout architecture is a Lock-In Amplifier, the use of a filtering bandwidth so wide that reaches the frequency of the *Force* signal negatively impacts the performance. Therefore, a time constant limit has been highlighted in the graph: time constants lower than the limit are not reasonable for the application.

As a final note, the analysis showed a quadratic dependence on the *Force* signal amplitude and on the target SNR:

$$T_C \propto \frac{(SNR)^2}{(V_{AC})^2}$$

This confirms the importance of choosing the *Force* signal amplitude as high as possible and justifies the effort to reduce the entity of the C_E signal, main cause of the preamplifier saturation. Furthermore, it shows that if the application allows for a smaller SNR, the speed of the readout can be increased accordingly.

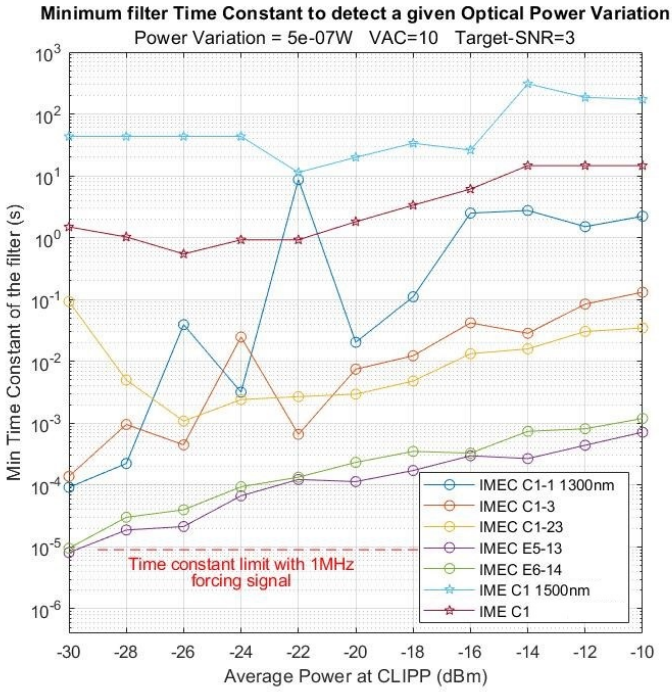

Figure B.3 – *Minimum lock-in time constant to detect a given Optical Power Variation as a function of the optical power in the waveguide. Curves refer to different CLIPP geometry from different foundries.*

B.2 | Detecting an optical power variation

This scenario evaluates the filtering required to detect a given optical power variation starting from a condition with a given average power already present in the waveguide. It is conceptually different from the previous case because the useful signal is related to slope of the "Conductance variation (S)" vs "Optical Power (dBm)" plot, instead of the absolute value, at a given optical power.

Figure B.3 shows the minimum time constant to detect an optical power variation of 0.5 µW in the same conditions of the previous section (*Force* amplitude of 10 V, target SNR of 3). Compared to the previous scenario, the useful signal is much smaller and it is reflected by values of the time constant obtained with the analysis.

Due to the sub-linearity of the CLIPP sensor, explained in Appendix A, as the average power increases the useful signal generated

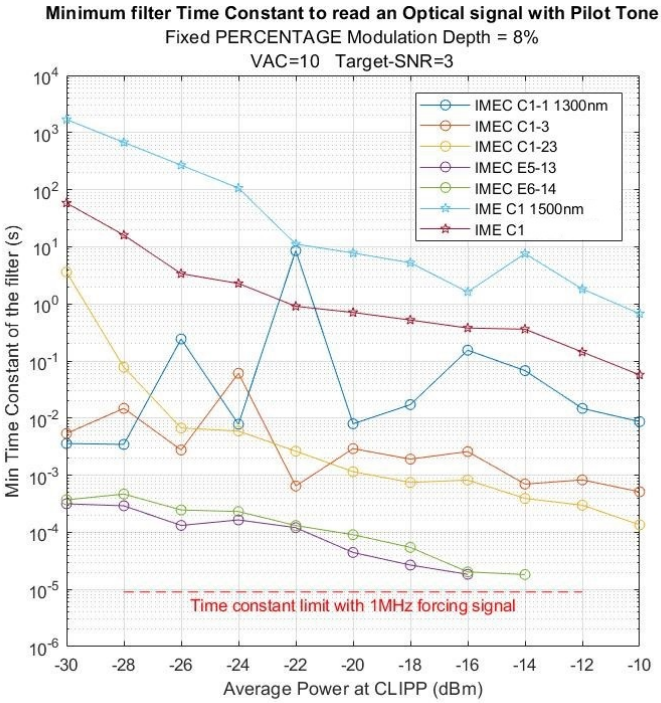

Figure B.4 – *Minimum lock-in time constant to read an optical signal with pilot tones as a function of the average optical power in the waveguide.*

by the optical power variation becomes smaller and the required time constant is higher. Therefore, if the application requires to monitor small variations of the optical power in the waveguide, working at a lower average power leads to a higher SNR. If the CLIPP were a perfectly linear sensor, the plot would be flat.

B.3 | Detecting an optical signal labeled with a Pilot Tone

The final scenario is detecting an optical signal in the waveguide by recognizing the pilot tone that modulates its intensity at a very low frequency. The useful signal is the variation caused by the small pilot tone and is conceptually similar to the previous case of the fixed optical power variation. The pilot tone is, however, a fixed percentage of the average power of the carrier signal and increases linearly with it.

The plot in Figure B.4 shows the minimum optical power to detect a pilot tone that is 8% of the average power in the waveguide, in the same conditions of the previous scenarios (*Force* amplitude of 10 V, target SNR of 3).

The results show that, despite the sub-linearity of the CLIPP sensor that makes it more sensitive at low average power, the pilot tone detection requires less filtering at high optical power. This is because the linear growth of the pilot tone as a fixed percentage of the average power is dominant with respect to the penalty due to the sub-linearity of the CLIPP. On the other hand, this is true only if the increase in average optical power is related to the same optical signal that is labelled with a pilot tone. If another signal is added in the same waveguide, the average optical power increases without a proportional effect on the pilot tone. Due to the sub-linearity of the CLIPP the electrical signal of the pilot tone is reduced, and a narrower filtering is required to achieve the same SNR.

However, it is important to remember that the detection of a pilot tone requires a double demodulation scheme and an additional filter is placed after the second demodulation. The role of the filter is to eliminate ripples at the output of the second mixer and generally has a bandwidth narrower than the pilot tone frequency itself. For example, if the pilot tone is at 1 kHz, a bandwidth < 100 Hz is advisable to filter the ripples. Therefore, this requirement is likely to be more stringent than the one on the SNR. On the other hand, the pilot tone frequency can be selected by matching both requirements, thus maximizing the responsiveness of the system in a given application.

LIST OF FIGURES

LIST OF TABLES

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