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Low voltage printed organic electronics

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"Oracle, how can I live forever?"
"Be difficult to forget."
"How?
Should I create art?
Should I be famous?
Or powerful?"
"You should be kind."
– @theoatmeal

Abstract

During the last decades, electronics has faced great technological improvements, leading to disruptive changes in everyday applications that have affected every aspect of human life. One of the most recent advances deals with organic semiconductors and their integration into thin-film electronic devices, toward the development of an alternative to conventional silicon electronics. Differently from their inorganic counterparts, organic transistors and circuits are characterized by peculiar features such as great mechanical stability, lightness, transparency, flexibility and, in some cases, even ultraflexibility and conformability. Additionally, their ease of processing and the possibility to fabricate them by means of solution-based and large-area compatible printing techniques make them the ideal candidate for the realization of low-cost and widespread electronic circuitry to be integrated into everyday life products, mainly in the fields of health-care, automation and security.
In the path toward the development of mass-produced organic electronic devices, one of the main limitation to be overcome is their high operating voltage, which hinders their integration with thin film batteries and other flexible energy harvesting devices. Within this framework, in the first part of this thesis a low-voltage and low-leakage dielectric bilayer has been optimized and integrated into all-organic, flexible and transparent organic field effect transistors (OFETs), which show low-voltage operation, high yield of fabrication and superior mechanical performances, with great stability up to 1000 bending cycles for an applied strain higher than 1%. The realization of n- and p-type OFETs operating at low voltage, and by means of compatible manufacturing techniques, paved the way toward the realization of complementary organic circuits, and culminated with the realization of the first printed, transparent and all-polymeric ring oscillators and D-Flip-Flops operating at voltages as low as 2 V.
Afterwards, focusing on the improvement of the mechanical characteristics of these devices, a strategy toward the realization of ultraflexible and conformable circuits, able to conform and adapt to irregular

shapes and surfaces, has been implemented. An ultrathin parylene film has been used as substrate, and devices have been encapsulated with an equally thin parylene layer, allowing of the realization of transistors and complementary inverters able to withstand harsh mechanical stresses such as rolling and crumpling with no significant losses in their performances, and leading to the first demonstration of printed, all-organic, transparent and ultraflexible OFETs and inverters operating at low voltage.
Lastly, the possibility to move from organic and recyclable devices to biodegradable ones has been considered, with the employment of biodegradable plastics as an alternative to commodity polymers, in order to minimize the environmental impact of the organic electronics. In particular, the substrate constitutes the greatest portion of the volume of the final device, and the employment of degradable substrate materials strongly limits the amount of waste produced. For this reason, biodegradable and compostable Mater-Bi films, onto which non-degradable organic devices have been integrated, act as substrate for the organic transistors presented in the last part of the thesis. In this way, *n*-type printed and ultraflexible OFETs have been realized, and their effect on the degradation behaviour has been assessed.
All the results presented in this work demonstrate how organic electronic devices are a viable alternative for the development and widespread integration of augmented functionalities into consumer products with limited additional costs.

Acknowledgments

"It is good to have an end to journey toward,
but it is the journey that matters in the end."
– Ursula K. Le Guin

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Contents

1

Introduction

"If knowledge can create problems, it is not through ignorance that we can solve them."
– Isaac Asimov

Two of the most significant advances that characterized the twentieth century, and that currently are present in every aspect of our lives, are the development and diffusion of synthetic polymers and the evolution of electronics.
The first started with the discovery of polyethylene in 1939,[1] followed by the discovery of isotactic polypropylene by Natta in 1954,[2] and has seen a steady increase during the last decades, covering needs in a wide variety of fields such as packaging, automotive, electrical and electronics, building and construction, agriculture, household and leisure, and many others. In 2017, the estimated plastic production has reached 348 million tons, with an ever increasing trend with respect to the previous years.[3] The most used commodity polymers are polyethylene (PE), polypropylene (PP), polystyrene (PS), polyethylene terephtalate (PET), polyvinyl chloride (PVC) and polyurethane (PUR).[3] Plastic materials show mechanical properties that cover a wide spectrum, from stiff and tough to ductile and flexible, interesting chemical features, and

can be manufactured with a variety of techniques, such as blow moulding, blow filming, injection moulding, extrusion and solution casting, with high production rates and low costs.
The electronic age, on the other hand, started with silicon, from the invention of the transistor in 1947,[4] to the development of integrated circuits and the always evolving tools for microfabrication, which have lead to the nowadays widespread use of this material for a variety of applications, ranging from the above mentioned integrated circuits and microsystems, to displays, solar cells and optoelectronic applications. Silicon plays this crucial role in electronics thanks to a combination of factors. In fact, this material is abundant and relatively cheap, it has superior semiconducting properties, with resistivity values in the range 0.001 to 10 000 Ω cm, and interesting mechanical features when in bulk, but becomes brittle when in crystalline form. Additionally, it forms stable and reproducible interfaces with its oxide, SiO_2, which plays a crucial role both in the development of electronic devices and during their fabrication, thanks to their different etching selectivity. Unfortunately, the manufacturing of silicon electronics is a complex and pretty expensive procedure, both economically and environmentally, since it involves plenty of steps, hazardous chemicals and high temperature annealing steps.
Most of the known plastic materials, and all the commodity plastics mentioned above, act as dielectrics. In 1954, organic conducting materials have been synthesised for the first time,[5] and the interest for these applications boosted in 1977, with the work of MacDiarmid, Shirakawa and Heeger on highly conductive polyacetylene,[6] for which they won the Nobel prize in 2000.[7] The possibility to have conducting and semiconducting polymeric materials lead to the realization of organic electronic devices, with the first organic field effect transistor in 1987,[8] the first light-emitting diode in 1990,[9] and the development of organic solar cells.,[10] with the employment of plastics in the electronic industry not only for packaging and adhesive applications, but also with active roles.
The main advantages of carbon-based devices compared to standard silicon ones are related to their mechanical properties, being flexible and ductile, and in some cases even stretchable and conformable, as opposite to the brittle crystalline silicon, their lightness, biocompatibility and optical transparency, but also to their fabrication techniques, which are solution-based methods that allow for an efficient use of raw materials, limit the required thermal budget and are easily customized thanks to their digital nature, leading to low-cost, large-area compatible and highly efficient production, with improved environmental friendli-

ness compared to the processing required for the realization of silicon devices. The main fabrication techniques, mostly inherited from the graphical arts, are presented in Figure 1.1. These techniques can be divided into two main groups, coating methods, generally used for full-layer depositions, and printing processes, which allow for the patterning of the deposited ink.
In gravure printing, the main player is surface tension transfer of ink from the cavities in the gravure cylinder to the substrate, with the cavities being continuously filled in an ink bath, possibly combined with a chambered doctor blade system, and with a good contact between cylinder and substrate ensured by an impression cylinder. The final patterning of the ink is given directly by the pattern which is present on the gravure cylinder, and it allows to reach high printing speeds, up to $15\,\mathrm{ms}^{-1}$. In flexographic printing, on the contrary, the ink is transferred via direct contact between the substrate and a printing plate cylinder onto which the desired pattern stands out, in a stamp-like fashion. This cylinder is continuously inked by an anilox cylinder, which is in contact with a fountain roller, in turn partially immersed in an ink bath.
In screen printing, the final pattern is defined by a mesh, which presents open areas in correspondence of the desired design. The ink is forced through the open areas, and onto the substrate, by a squeegee. As shown in Figure 1.1, there are two main kinds of screen printing. In flat bed screen printing, the screen is lowered on the substrate, the the squeegee is swiped on the screen and finally the screen is removed, leading to a stepwise process. In order to achieve a continuous process, rotary screen printing should be considered, where the same working principle of flat bed screen printing is employed, but the screen is folded onto a tube and both the ink and the squeegee are placed inside the tube itself, allowing for a continuous deposition during the simultaneous rotation of the tube and the substrate, reaching speeds as high as $100\,\mathrm{mmin}^{-1}$. The last printing technique shown in Figure 1.1 is ink-jet printing, but it will not be presented here since it will be extensively considered as the main fabrication technique employed for this work.
For what concerns coating methods, on the other hand, they can be defined as a one-dimensional application of an ink stripe, with patterning capabilities only in the width direction. In knife coating, a knife is placed close to the substrate, and an ink source is right next to the knife itself. As the substrate moves, the knife allows only a limited amount of ink to pass, corresponding to the gap between the knife and the substrate, and this allows to directly control the wet layer thickness, and so the final thickness of the film. Slot-die coating has a similar

working principle, but the ink is supplied through a coating head, close but not in contact with the substrate. The continuous ink flow leads to the formation of a standing meniscus, which allows for a continuous coating with an even thickness. For both these coating processes, speed values range from 0.1 up to 200 mmin^{-1}.
Spray coating, the last technique reported in Figure 1.1, is not a printing technique, but shows some similarities to ink-jet printing. In this technique, a continuous spray of ink is created in the nozzle, usually by means of pneumatic-based systems that make use of air or gas in order to atomize the ink. The droplets then spread on the substrate, and the spreading is enhanced by the kinetic energy of the droplets themselves. In spray coating, patterning is possible if shadow masks are used, but there might be some contaminations given by the ink mist, and the allowed edge resolution is pretty low.
Thanks to all the factors listed here, and despite their reduced electrical and electronic performances when compared to silicon electronics, organic electronic devices can play a significant role, both replacing standard devices and expanding the realm of electronic applications, having a clear path toward a cost-effective industrial scaling, and thus a mass production of organic electronic devices.
Plastic electronic devices can be used for a wide variety of applications such as flexible and rollable displays, RFIDs (radio-frequency identification tags), wearable systems, intelligent packaging and textiles, interactive surfaces, disposable diagnostic devices and sensors, to be employed in the fields of security, diagnostics, automation, health-care and many other.[12] In this thesis, focus will be on Organic Field Effect Transistors (OFETs), which form the building block for the development of the next generation of thin film electronics.[13] The electrical performances of OFETs have seen a dramatic increase in the last years, reaching mobilities up to 10 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$, which are comparable with and sometime higher than those of amorphous silicon.[13] Aiming at the fabrication of robust electronic circuitry, complementary devices need to be developed. Up to now, most of the devices presented in literature rely on unipolar circuits,[14] with only few examples of complementary and reliable ring oscillators and D-Flip-Flops.[15]
An additional limit hindering the success of organic electronic circuitry is related to their operating voltage. These devices need to be portable, to allow for an easy integration into consumer products, and as such should be powered by energy harvesting devices, such as plastic solar cells and/or thin film batteries. The maximum operating voltage and power consumption allowed are low, limited to few volts. Most of the devices presented in literature, on the other hand, have operating volt-

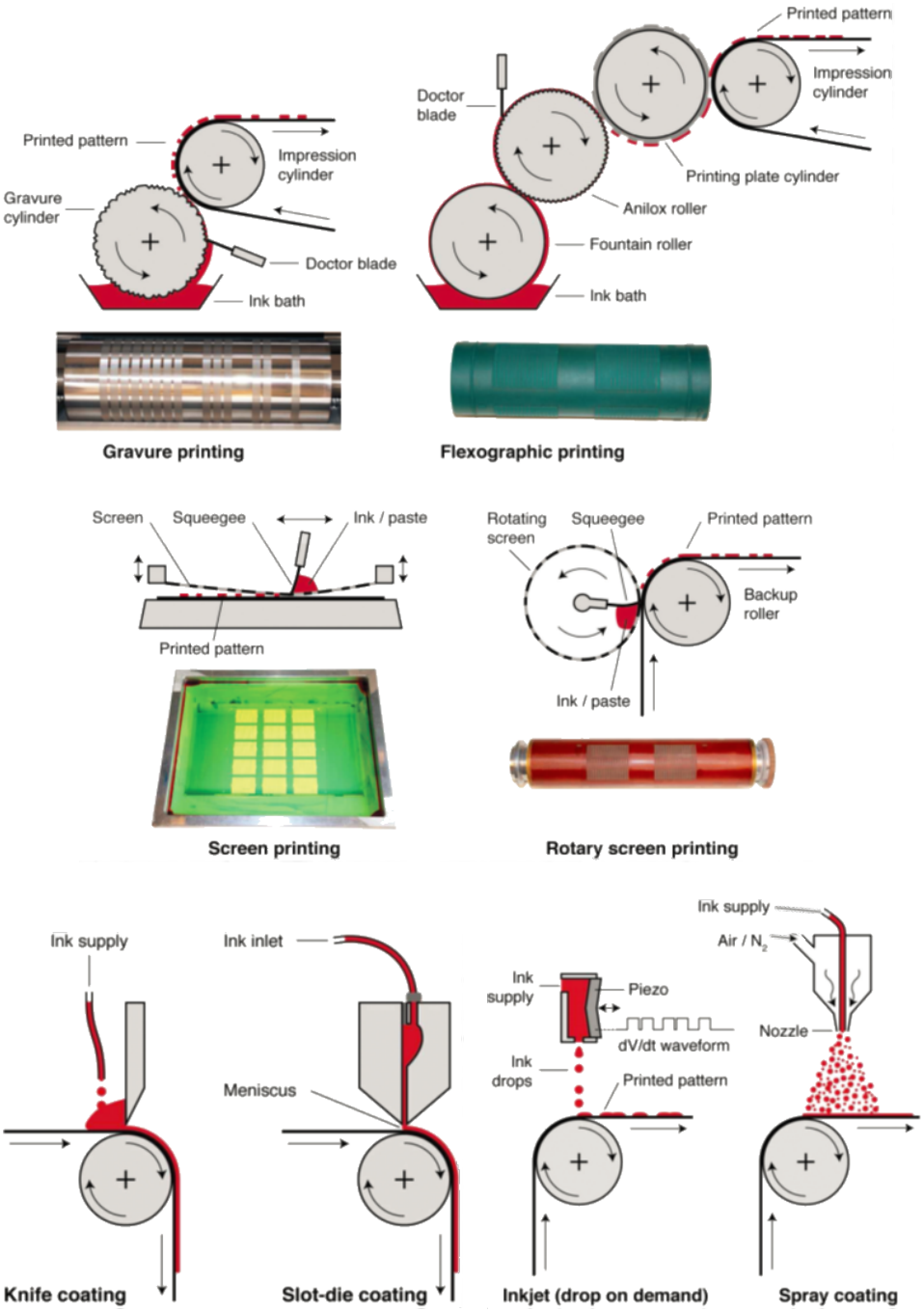

Figure 1.1: Schematic of solution-based fabrication techniques used for the realization of organic electronic devices. Gravure printing, flexographic printing, screen printing, rotary screen printing, knife coating, slot-die coating, ink-jet printing, spray printing. Adapted from[11]

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ages in the order of tens of volts, which strongly limit their portability and diffusion on the market. A reduction of this parameter is thus a key enabler toward the diffusion of organic electronic devices in the consumer market. During the first part of this work, this issue has been tackled. The strategies toward the development of low-voltage devices will be presented in Chapter 4, where the implementation of a high-capacity dielectric and its integration in flexible OFETs and complementary integrated circuits will be presented.[16]
Flexible electronic devices play a crucial role in the transition from rigid silicon-based electronics to applications with more appealing mechanical features. In recent years, the field expanded even further with the realization of devices with ever increasing mechanical characteristics, such as ultraflexibility and conformability, and the creation of the so called epidermal or imperceptible electronics. Here, devices have a thickness lower than 10 µm and improved lightness and form factor, and are thus capable of adhering to irregular surfaces. The realization of ultraflexible and biocompatible devices is of great interest for the healthcare industry, with the possibility of developing conformable devices for a wide variety of applications. Different strategies to achieve high mechanical capabilities will be presented in Chapter 5, together with the realization of ultraflexible, all-organic and transparent OFETs and complementary circuits.
As it was mentioned above, the annual plastic consumption is in the order of hundreds of million tons, and only a limited percentage of this volume is properly disposed of and recycled. Now that organic electronics is approaching its commercial phase, problems and challenges not yet considered need to be addressed, and one of them deals with the disposal of broken and old devices. In order to tackle this issue, biodegradable electronics has been proposed, with the employment of biodegradable materials for the realization of environmentally friendly and disposable electronic devices. In this way, not only the amount of e-waste and plastic waste generated is reduced, but there is also the possibility to widen even further the field of organic electronics, with the realization of medical applications, environmental sensors, conformal components for recreational and leisure purposes, food packaging, use-and-throw-away devices and security applications.[17] In the first step toward the realization of not only recyclable but also degradable and compostable electronic devices, in Chapter 6 the realization of printed OFETs on a Mater-Bi substrate is presented.

2

Background knowledge

"'If I have seen further, it is by standing on the shoulders of giants."
– Bernard of Chartres

In this chapter, the electrical properties of organic semiconductors will be discussed, with a focus on charge transport and charge injection. In the second part of the chapter, the structure of an Organic Field Effect Transistor (OFET) will be presented, together with its working principle and the parameters used to evaluate the quality of a device.

2.1 Electrical properties of organic semiconductors

Organic materials, as well as all the other classes of materials, can be divided into three main classes, namely insulators, semiconductors and conductors, depending on their ability to conduct an electrical current, represented by the electrical conductivity σ, or its reciprocal, the resistivity ρ. In order to present the main differences between the three categories mentioned above, it is useful to consider the electronic band structure. In this model, energy bands for a specific material are obtained solving the Schrödinger equation, and each electron occupies a discrete energy level,which corresponds to one of the eigenvalues. When atoms combine to form molecules, molecular orbitals are formed, and the distribution of energy levels inside them is usually calculated by means of the Linear Combination of Atomic Orbitals (LCAO) method. If the number of atoms is high enough, the distance between the discrete levels becomes so small that they can be considered as a continuum, leading to the formation of bands.
The levels occupancy follows a Fermi-Dirac distribution function, with the lowest levels always filled, and the highest ones always empty. In this context, the Fermi level for temperatures higher than 0 K is defined as the state where there is a 50% probability of occupation, so that also states above it can seldom be occupied by electrons, while at 0 K, the occupation probability is exactly 1 below the Fermi level and 0 above it. The position of the Fermi level is what allows to distinguish between the three classes mentioned at the beginning of the paragraph:

Conductors The Fermi level lies inside the band, so electrons always have an available higher energy level, and upon the application of a voltage, they are able to move and generate an electric current

Semiconductors In this case, the Fermi level lies in a forbidden state inside the gap between the valence band, which lies below the gap, and the conduction band, above it. Semiconductors are characterized by a relatively small gap, so some electrons are able to hop from valence to conduction band when a voltage is applied.

Insulators Insulators show a structure similar to that presented for semiconductors, but with a much larger gap between the bands. The probability for electrons to jump to the conduction band is much smaller, unless a very high voltage is applied, reaching the so called breakdown.

For what concerns inorganic semiconductors, the most known and used is silicon, which presents a band gap of 1.1 eV. Silicon is an intrinsic

semiconductor, while extrinsic semiconductivity can be achieved by means of doping, a process during which impurities, atoms with one valence electron more (n-doping) or less (p-doping) than silicon, are added to the pristine material, creating a spare energy level inside the gap. An increasing amount of dopant leads to the formation of a multitude of states, up until the formation of an actual band inside the gap, closer to the conduction or the valence band depending on the kind of doping, shifting the Fermi level and thus lowering the energy barrier for the conduction of electrons or holes.
Organic semiconductors, on the other hand, are a very interesting class of materials, characterized by peculiar electrical and mechanical features; they combine, in fact, the electrical characteristics of semiconducting molecules with the mechanical properties of plastics. These materials are composed mainly of carbon and hydrogen atoms, together with few heteroatoms such as oxygen, nitrogen and sulphur. They emit and absorb light in the visible region, and show a conductivity compatible with the classical application of semiconducting materials.

2.1.1 Atomic carbon structure

In order to describe charge transport inside these materials, it is useful to first consider the structure of carbon. Atomic carbon has 6 electrons, two in the $1s$ orbital, two in the $2s$ and the remaining two in two of the three $2p$ orbitals. When other atoms bind with carbon, hybrid orbitals are formed as linear combination of the $2s$ and $2p$ orbitals, with the binding energy compensating for the energy difference between the orbitals involved. If all four orbitals combine, 4 hybrid sp^3 orbitals will be formed and, being equivalent, they will be spatially arranged as a tetrahedra. If only two $2p$ orbitals form hybrid with the $2s$ one, three sp^2 orbitals will be formed, distributed in-plane with 120° angles between them. Finally, if the hybridization involves only one $2p$ and the $2s$ orbital, two sp hybrid orbitals will form, with a 180° angle.[18] The shape and orientation of the hybrid orbitals formed by carbon atoms are shown in Figure 2.1.
When hybridized carbon atoms form chemical bonds with other atoms, such as other carbon atoms or hydrogen, two different kinds of orbitals can be formed. When hybridized orbitals interact with other orbitals, such as a $1s$ from a hydrogen atom, they form end-to-end bonds, called σ bonds, which lead to the formation of σ molecular orbitals. Oh the other hand, when p orbitals interact, there is the overlap between the lobes of the orbitals, forming the so-called π bond and π molecular orbitals.[18] σ bonds are always stronger than π bonds, since they arise from a larger overlap between atomic orbitals. Bonding orbitals always

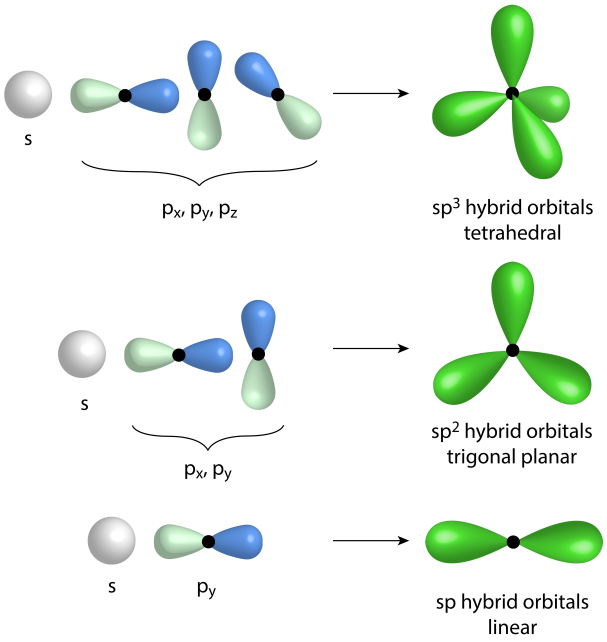


Figure 2.1: Carbon atom hybrid orbitals, from top to bottom hybridization sp^3, sp^2 and sp.

have a lower energy compared to the originating atomic orbitals, while anti-bonding ones have a higher energy. In Figure 2.2, three simple carbon-based molecules and their molecular orbitals are shown.
Organic semiconductors are characterized by an extended π conjugation, thanks to the presence of carbon atoms with sp and sp^2 hybridization. The σ orbitals allow the formation of a molecular backbone characterized by strong covalent bonds, while π orbitals interact and give rise to a delocalized electron cloud over the whole molecule. The latter forms the frontier orbital of these molecules, and thus defines their optoelectronic properties; the Highest Occupied Molecular Orbital (HOMO) is a π orbital, while the Lowest Unoccupied Molecular Orbital (LUMO) is a π^* orbital. The energy gap between HOMO and LUMO is proportional to the number of alternating π bonds, and an increasing conjugation length leads to a reduction of the gap, and thus to a semiconducting behaviour. The absorption of light is related to the distance between HOMO and LUMO, with π orbitals giving rise to a smaller splitting between frontier levels and thus optical transitions at lower frequencies, while the injection of charges, electrons or holes, depends on the relative position of the electrode work function with respect to the HOMO or LUMO of the molecule.

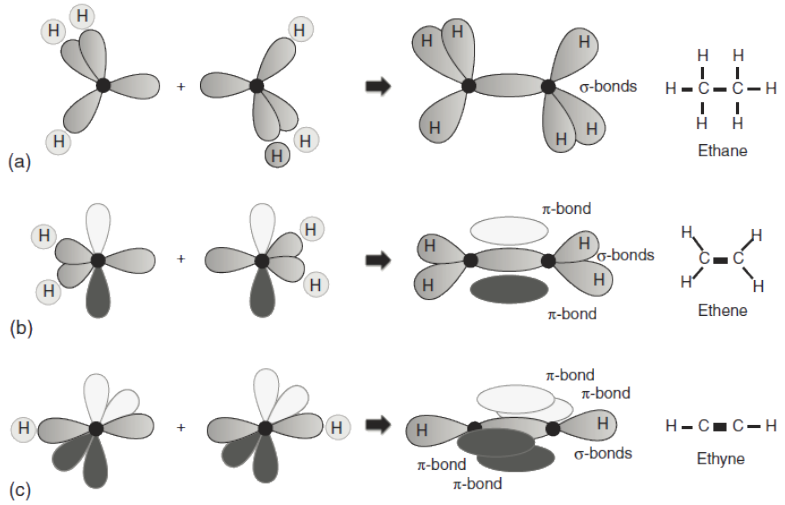


Figure 2.2: Three carbon-based molecules and their molecular orbitals. (a) Ethane, with only sp^3 carbon hybridization and four σ bonds, (b) ethene, with sp^2 hybridization, two σ and one π bond, and (c) ethyne, with sp hybridization, one σ and two π bonds. Adapted from[19]

The HOMO energy level of organic semiconductors plays a crucial role for the stability of these materials in ambient conditions, which in turn impacts the lifetime of the devices and their ON-OFF ratio. In particular, the HOMO level needs to be lower than 4.9 eV from the vacuum energy level, or otherwise a reaction with oxygen takes place in presence of water, leading to the loss of an electron.
The delocalization of π electrons is not extended over the whole system but limited within a molecule, so transport is mostly related to hopping phenomena between molecules. The mobilities that can thus be achieved are lower than those of inorganic systems; nonetheless, polymeric devices with mobilities up to $1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for n-type OFETs[20] and up to tens of $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for p-type transistors have been reported in literature.[21] An analysis of the results published in literature in the last 30 years has been published recently,[22] and it shows how the majority of the reported mobility values higher than $1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ are actually obtained from devices presenting some non-idealities, but nonetheless significant progresses have been made, and mobility values steadily continue to rise.
Most of the high performing organic semiconductors present three different phase upon heating, a crystalline one, a melt phase and an amorphous one. For some polymers, also a liquid crystalline phase is present, between the crystalline and the isotropic melt ones. If the organic semiconductor is annealed in this temperature range, highly

crystalline and ordered films are produced, reaching a favourable configuration for high mobilities. This behaviour is strongly present in aromatic planar extended polymers, and can be achieved via molecular design by increasing the stiffness of the backbone, which in turn reduces the disorder of the melt.[23]
The mobility of the semiconductors is also dependent on their molecular weight, with a direct proportionality between the two up until a plateau is reached, for molecular weight values around 20 kDa. This is mostly given by the fact that higher molecular weights lead to more interlinked and better defined crystalline domains, while low molecular weights give rise to sharply defined grain boundaries and thus lower mobilities. Too high molecular weights, on the other hand, lead to a huge increase in viscosity, hindering the crystalline structure and reducing the mobility.
The presence of localized wave functions leads not only to a hopping transport regime, but also to limited molecular interactions, mostly weak $\pi - \pi$ or van der Waals overlap. For this reason, these materials have an intrinsic high flexibility and can easily be processed by means of solution techniques or vacuum evaporation, being soluble and/or vaporizable at low temperatures. There is thus a trade-off to be reached between mobility and processability.[24]
Organic semiconductors usually contain high amounts of impurities, mostly due to additives and reaction products from synthesis or due to intrinsic purification limits. Despite all this, organic semiconductors still show decent mobility values like the ones reported above, and the explanation for this can be found once again in the localization of the wavefunctions in disordered systems. In fact, during an hopping event, an impurity located far enough is not influential, while it would strongly impact the mobility of a single crystal device at low temperature.[24]

2.1.2 Charge transport

The operation of OFETs and other organic electronic devices relies on the movement of charges inside the semiconductor material. For this reason, it is necessary to consider how charges are generated inside these systems and how they are able to move from one molecule to another.
Adding an electron to a neutral molecule is called *reduction*, and leads to the formation of a radical anion, while the removal of an electron, or creation of an hole, is an *oxidation* and generates a radical cation. In both cases, the energy of the radical species is different from that of the neutral molecule and depends on the geometric relaxation energy, defined as the energy needed to change the molecular geometry

from the neutral to the charged equilibrium position. When a charge moves from one molecule to another, the overall reorganization energy needs to take into account also the relaxation energy related to the removal of a charge from the first molecule. Considering a solid state scenario, which is the most common one when focusing on organic semiconductors applications, moving charges in the system will lead to a reorganization of neighbouring molecules; in this way, not only the geometry of the charged molecule itself, but also the distance between adjacent molecules will change, giving rise to a lattice distortion. The combination of the charge and the related lattice distortion is called a *polaron*.[19,25]
Energetically, the polaron modifies the energetic structure of the molecule, being related to a new state in the HOMO-LUMO gap. If many polarons are present, these isolated states will interact and form polaronic bands, related to a semi-metallic behaviour.
The mobility of these systems depends on how easily the charges are able to move between molecules, since the transport, as it was mentioned above, can be described as an hopping process. Since these materials form non-ordered structures, the electronic state density has some dispersions, and this generates an additional energetic barrier.[13]
There are two main barriers, the first to be overcome by quantum tunnelling and the second via phonon vibrations; the process is called hopping, a thermally activated tunnelling, which takes place with probability $P_{hopping}$ equal to

$$P_{hopping} \propto exp\left\{\frac{-\Delta E}{kT}\right\} exp\{-\alpha x\} \tag{2.1}$$

The energy difference ΔE and the distance x determine the most probable transitions. When considering the role of temperature, it might be noticed that high temperatures can interfere with molecule's vibrational methods, increasing photon activity and hopping events, and thus increasing the mobility, contrary to what would happen in systems such as crystalline silicon, where increasing temperatures reduce the phonon-electron scattering and thus the mobility.
Additionally, the molecular structure plays a role in determining the mobility of the system; specifically, the synthesis and deposition of organic semiconductor films with a supra-molecular, long-range order might lead to a more coherent transport and thus to a higher mobility.[26]

2.1.3 Charge injection

Charged species in organic semiconductors are usually generated via charge injection from an electrode. The cathode is the electrode inject-

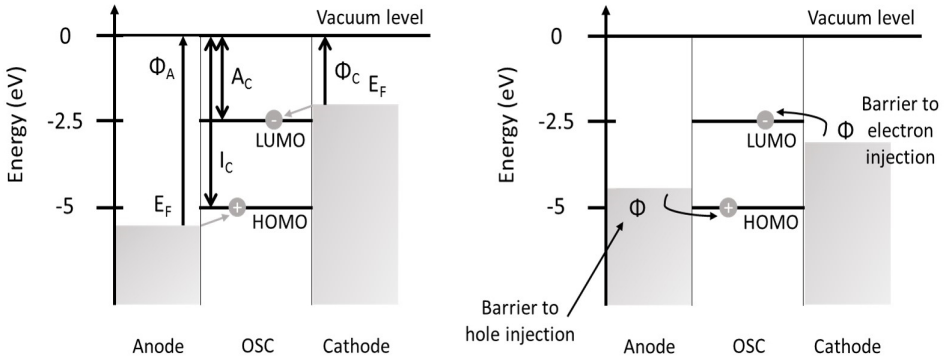


Figure 2.3: (a) Ideal charge injection scenario, with a semiconductor sandwiched between two metals. An electron can move from the Fermi level of the cathode to the LUMO, and a hole can be injected by transferring an electron from the HOMO to the anode. (b) injection process in a realistic environment, with injection barriers to be overcome.

ing electrons, which adds an electron to the system, while the anode injects holes, which correspond to the removal of electrons.
In an ideal situation, the cathode work function is equal or higher than the molecule's electron affinity, but this is hardly the case. In a more realistic scenario, electron affinities are around 2.5 eV, and there are basically no metals, semi-metals or heavily doped semiconductors showing work functions at lower energies. For this reason, when an organic semiconductor is put in contact with a metal, there is the formation of potential difference across the interface, which is called built-in potential V_{bi}.[19]
In a first approximation, this energy barrier is related to the difference between the metal work function and the HOMO/LUMO level of the semiconductor. Charges are transferred to the semiconductor, and they can be stored both as space charge, with the contact potential dropping in the semiconductor space charge area, or as surface sheet charge, with the potential drop generating a surface dipole at the metal-semiconductor interface, or as a combination of these two. More in details, the energetic barrier depends on the materials and the physical phenomena involved:

Physiosorption This usually takes place when active materials are processed onto metals, with the organic semiconductor not hybridizing with the metal but being physiosorbed on its surface. In this configuration, the metal electrons tail is pushed back closer to the metal surface by the π-electrons cloud, and this leads to a modification of the surface dipole and a decrease of the work function. In this regime, if the Fermi level of the metal is aligned

with or close to that of the isolated semiconductor, a common Fermi level is established between the two systems, with no significant charge transfer and potential drop. On the other hand, when the metal Fermi level approaches the LUMO level, a significant charge transfer from the metal to the LUMO takes place, and the charge stored in the semiconductor leads to a bending of the energy levels; if the Fermi level approaches the HOMO level, the same happens, with charges being transferred from the HOMO level to the metal. The charge carrier concentration at the interface depends on the relative position of the metal Fermi level with respect to the HOMO or LUMO level, with larger concentrations when E_F is closer to the frontier orbitals.

Weak chemisorption This case applies to very clean interfaces prepared in high vacuum, where intimate contact is created between the organic semiconductor and the metal, leading to a metal-hybridization of the molecular orbitals, and the creation of a continuum distribution of states in the energy gap, with a non-negligible density. This states distribution is called Induced Density of Interfacial States (IDIS) and is filled up to the Charge Neutrality Level (CNL), with the charge transfer being driven by the relative position of the CNL and the metal Fermi energy.

Strong chemisorption This last case applies to strongest interaction strength, typical of metal/organic covalent bonds. Here, chemical bonds are formed, with a partial charge transfer and the development of an interfacial dipole.

In summary, the alignment between the energy levels of the metal and the organic semiconductor depends on a variety of factors, so the sole knowledge of the metal E_F and the HOMO/LUMO levels of the semiconductor is not enough, and all the interactions need to be taken into account.
When considering injection in organic semiconductors, it needs to be taken into account that (a) transport in disordered medium is governed by hopping, a thermally-activated tunneling ,(b) the application of an external voltage on the image charge potential leads to a maximum for the electron energy, (c) and the LUMO level is an average quantity over a statistical distribution. If a metal electron has energy higher or equal to that of semiconductor's unoccupied states, injection can occur. After injection, due to the peculiarity of the hopping process, the electron quickly loses its energy, so hops to only the first few layers are to be considered. This excess electron might then drift back to the

metal, or diffuse in the semiconductor bulk. At the thermal equilibrium, backflow and injection cancel out, while the energy maximum shifts closer to the interface if an external voltage is applied, and so injection overcomes the backflow.
The injected current is equal to $J = e\mu E N_0 exp(-\Phi_B/kT+\beta_s E^{0.5})\Psi(E)$, with μ representing the carrier mobility, E the electric field, N_0 the total site density, β_s the Schottky effect, and $\Psi(E)$ a correction factor.[27] The injection current has an Arrhenius-like dependence on the nominal energetic barrier Φ_B, and a direct one on mobility. The LUMO level, as mentioned above, is to be considered as a statistical distribution, so the barrier Φ_B is an average barrier, with some semiconductor tail states below the metal Fermi energy even when it lies below the average LUMO level. Lastly, considering the role of disorder, it might seem at a first glance that more disordered systems are advantageous, since they lower the barrier thanks to more populated interface tail states, but disorder affects significantly also the mobility, reducing it as well, and the final balance of these two effects is not easily predicted.

2.2 Organic Field Effect Transistor (OFET)

The first demonstration of the field effect principle has been given in 1930 by Lilienfeld,[28] while the first transistor was presented in 1947.[4] In 1960 Kahng and Atalla showed the first field-effect-based MOS (metal oxide semiconductor) transistor, laying the basis for the development of microelectronics.[29]
For what concerns the organic side, in 1987 the first Organic Field Effect Transistor (OFET) was realized by Tsumura[30] using a polythiophene molecule as semiconductor. These devices have been extensively studied in the last decades, not only as a useful tool for the characterization of the electrical performances of organic semiconductors, but they have also been employed as building block for the realization of complex digital circuits, characterized by peculiar optical and mechanical features.
In this section, the structure of an OFET will be presented, together with the working principle of this device and the main parameters used to characterize its performances.

2.2.1 Device structure

OFETs are thin film transistors, three-electrode devices in which one electrode, the *gate* electrode, is used to modulate the current flowing between the other two electrodes, namely *source* and *drain*. These devices can be described as capacitors, where the conductive plates are represented by the above mentioned electrodes, while the layer between them is composed of a semiconductor and a dielectric film.
The region between source and drain electrodes is called *channel*, and it is defined by two main geometrical parameters, channel length L and channel width W, shown in Figure 2.4.
There are four main topological structures that can be realized, depending on the relative position of gate and source/drain electrodes. There are top gate and bottom gate devices, top contact and bottom contact ones; all the four possible combinations are shown in Figure 2.5. These configurations can be divided in two classes, coplanar and staggered; the first comprises those devices in which the gate dielectric and the source/drain electrodes are on the same side of the semiconductor film, shown in Figure 2.5a and 2.5b, while the latter refers to the devices where the semiconductor films stays between the dielectric and the source/drain electrodes' plane, represented in Figure 2.5c and 2.5d. Different structures affect both device performances and manufacturing feasibility. Bottom-gate configuration is often used for research purposes, mostly because of the commercial availability of doped Si

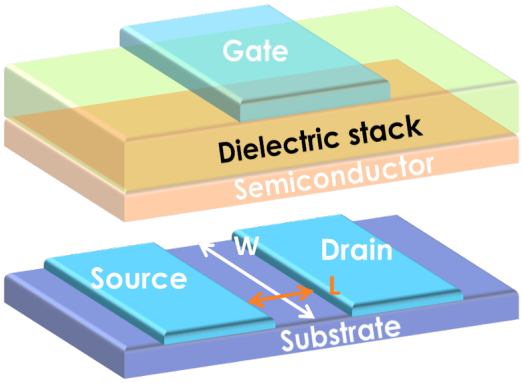
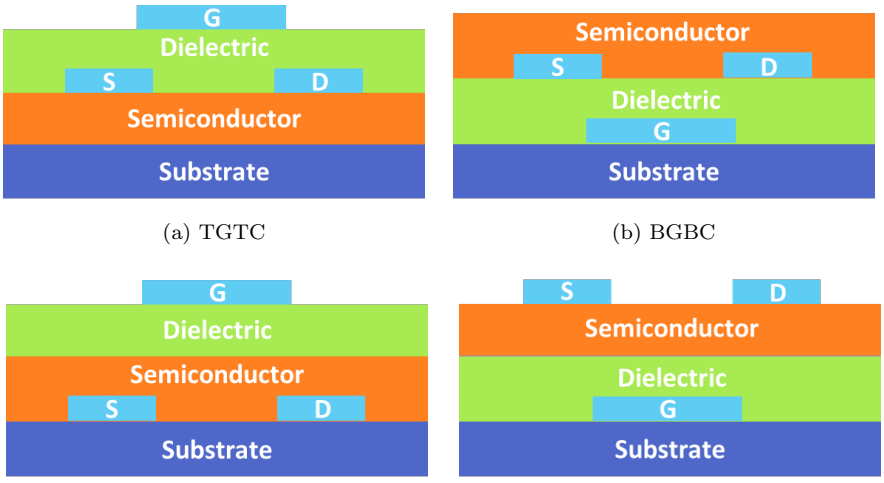


Figure 2.4: Structure of an Organic Field Effect Transistor and geometrical parameters of the channel region.



(a) TGTC

(b) BGBC

(c) TGBC

(d) BGTC

Figure 2.5: Four configurations of OFET. The blue rectangle, at the bottom in all the configuration, is the substrate, the orange layer represents the semiconducting film, light green is the dielectric layer, and light blue rectangles represent the electrodes.

substrates covered with thermally grown SiO_2, acting as bottom gate electrode and dielectric. In this kind of devices, the surface quality of the dielectric layer is very high, and it thus allows for an easy deposition of all kinds of semiconductors, also those with a higher sensitivity to the surface roughness. On the other hand, this configuration shows two main drawbacks, a rigid substrate and a common gate for all devices on the same substrate, which hinders the development of IC circuitry. The top-gate configuration clearly makes it easier to develop complex integrated circuitry. Additionally, since the dielectric layer is deposited on top of the semiconducting one, it acts as a passivation layer, and increases the device stability. However, in this configuration the dielectric/semiconductor interface is not as ideal as in the bottom-gate configuration, because of the high roughness of the semiconducting film; as such, there are scattering events and the mobility of the devices is reduced. Additionally, the deposition of a dielectric layer on top of the already deposited semiconductor might be harmful for the latter, mostly if solution-based techniques are considered.
On the contacts side, bottom-contact architectures lead to a non-ideal morphology of the semiconductor film in the regions close to the contacts themselves, degrading thus charge injection and the overall transport properties. Yet, in this configuration source and drain contacts can be fabricated with high resolution and with a variety of manufacturing techniques. On the other hand, top-gate configurations, despite being safer for what concerns the semiconductor film quality, can be realized only with a limited number of techniques, characterized by high costs and, most importantly, low resolution.
Staggered top-gate configuration grants optimal charge injection,[31] since there is an overlap between source/drain electrodes and the gate, which leads to a reduced contact resistance;[32] additionally, in this configuration there is a control over the interfaces between the dielectric and semiconductor layer,[27,33] and the dielectric layer and gate electrode act as a partial self-encapsulation,[34] improving the environmental stability of these devices. In this work, top-gate bottom-contact structure has been used for all the devices.

2.2.2 Working principle

Organic transistors, differently from their inorganic counterpart, work in *accumulation* mode. Undoped organic semiconductors, in fact, do not show a prevailing density of charge carriers, and there is thus the need to inject them from the electrodes.
The working principle of this device is shown in Figure 2.6. A voltage V_G is applied at the gate electrode and it generates an electric field

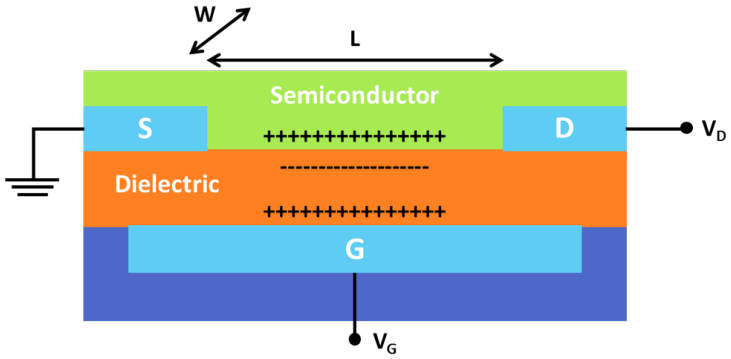


Figure 2.6: Working principle of an OFET.

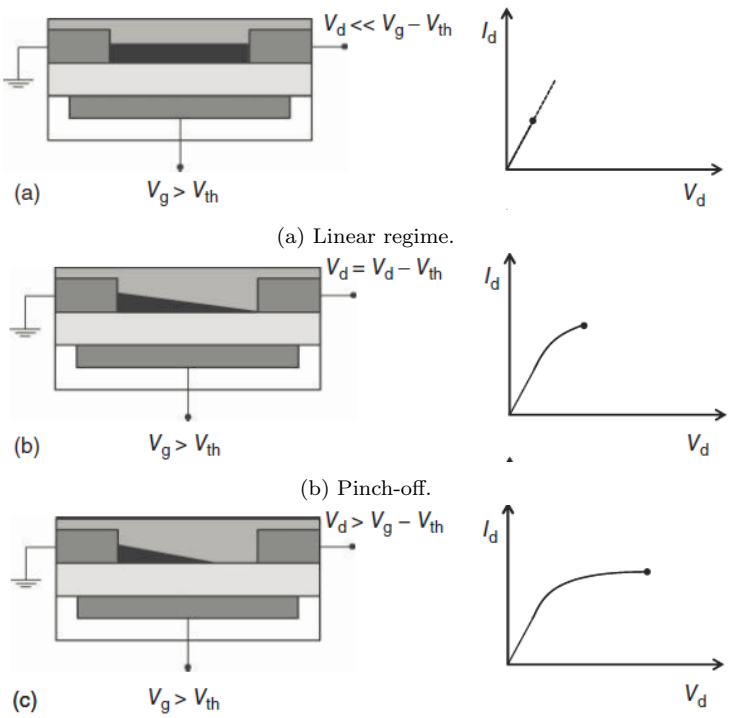
across the dielectric layer and the subsequent accumulation of charges in a narrow region of the semiconductor film close to the interface with the dielectric; if, for example, a negative voltage is applied, the electric field in the dielectric leads to the accumulation of positive charges in the semiconductor.
If the source and drain electrodes are ideal and there is no voltage applied between them, the injected charges are proportional to the dielectric capacitance C_{diel} and the applied gate voltage V_G. In a real device, the semiconductor layer has some trap states, so the first accumulated charges will fill up these traps and, in order to form an accumulation layer, the applied voltage needs to be higher than a threshold voltage V_{th}. The amount of mobile charges per unit area is given by

$$Q_{mob} = C_{diel}(V_G - V_{th}) \tag{2.2}$$

Once an accumulation layer is formed, there can be a flow of current between source and drain electrodes, depending on the voltage applied between them. Under this condition, a gradient of charge carriers is formed in the channel, with a potential $V(x)$ that varies from 0, at the source electrode, to V_D, at the drain electrode. The density of charges can be thus re-written as

$$Q_{mob} = C_{diel}(V_G - V_{th} - V(x)) \tag{2.3}$$

The mutual relationship between the applied drain voltage and the difference $V_G - V_{th}$ allows to define the two main working regimes of an OFET.
If $V_D << V_G - V_{th}$, the current in the channel obeys to the Ohm's law, increasing linearly with V_D, and the transistor is in the *linear* regime, as shown in Figure 2.7a.
When $V_D = V_G - V_{th}$, the concentration of charge carriers at the drain



(a) Linear regime.

(b) Pinch-off.

(c) Saturation regime.

Figure 2.7: Operating regimes of an OEFT. Adapted from[19]

electrode is zero, and the transistor is *pinched-off*.
If the drain voltage increases further, with $V_D > V_G - V_{th}$, the pinch-off point moves toward the source electrode, as shown in Figure 2.7c, and the transistor operates in *saturation* regime. In this case the charges are pulled across the depletion zone by an electric field that is formed between the pinch-off point and the electrode, and the current still flows in the channel. This current is controlled by the potential drop between the source electrode and the pinch-off, which is constant at $V_G - V_{th}$, so I_D does not increase with a further increase in V_D once the saturation regime is reached.[35]
In order to analytically describe the current-voltage characteristic of an OFET in the different regimes, the *gradual channel approximation* is needed. Under this assumption, the electric field is considered to be perpendicular to the transistor plane, and this is satisfied if the channel length L is 10 times larger than the dielectric thickness. The drain current thus follows the Ohm's law

$$I_D = WQ_{mob}\mu F \tag{2.4}$$

where W is the channel width, Q_{mob} is the charge density defined above,

μ is the mobility of the organic semiconductor, and F is the source-drain electric field.
Substituting Equation 2.3 in Equation 2.4, and writing the electric field as dV/dx, the following is obtained

$$I_D \int_0^L dx = WC_{diel}\mu \int_0^{V_D} (V_G - V_{th} - V(x))dV \tag{2.5}$$

which yields to

$$I_D = \frac{W}{L}\mu C_{diel}\left[(V_G - V_{th})\, V_D - \frac{1}{2}V_D^2\right] \tag{2.6}$$

If $V_D << V_G$, so considering the linear regime, the current expression can be re-written as

$$I_{D,lin} = \frac{W}{L}\mu_{lin} C_{diel}\,(V_G - V_{th})\, V_D \tag{2.7}$$

from which the expression for the linear charge mobility can be extracted

$$\mu_{lin} = \frac{\partial I_{D,lin}}{\partial V_G}\frac{L}{WC_{diel}V_D} \tag{2.8}$$

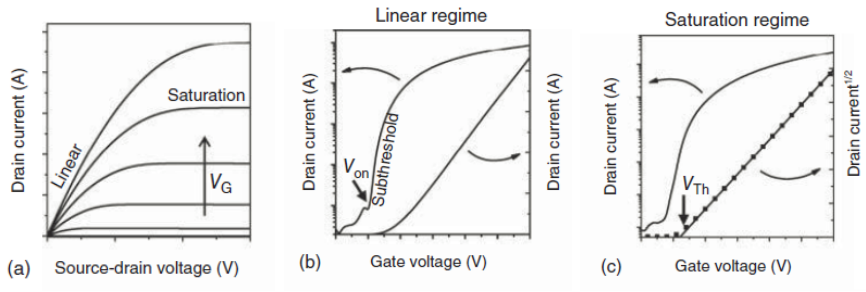
In saturation regime, on the other hand, the drain voltage in Equation 2.6 can be replaced with the pinch-off voltage, and the following is obtained

$$I_{D,sat} = \frac{W}{2L}\mu_{sat} C_{diel}\,(V_G - V_{th})^2 \tag{2.9}$$

From Equation 2.9, the expression for charge carriers mobility in saturation is derived

$$\mu_{sat} = \frac{\partial I_{D,sat}}{\partial V_G}\frac{L}{WC_{diel}(V_G - V_{th})} \tag{2.10}$$

The characteristics of an OFET can be presented in different ways.
If the drain current is plotted as a function of the drain voltage, for constant values of gate voltage applied, the *output* curves are obtained, presented in Figure 2.8a; in these plots, the linear and saturation regimes can be easily distinguished. The *transfer* characteristics, on the other hand, are obtained plotting the drain current as a function of the gate voltage, for constant drain voltages applied; in this case usually two curves are presented, one in linear and one in saturation regime, as shown in Figure 2.8b and 2.8c.



(a) Output curve (b) Transfer curve, linear (c) Transfer curve, saturation

Figure 2.8: Characteristics of an OFET. Adapted from[19]

2.2.3 Main parameters

In order to evaluate the performance of an OFET, different parameters should be taken into account, and they will be presented in this section.

Mobility In OFETs, a higher semiconductor mobility leads to a higher output current, better on/off ratio and switching speed. In Section 2.2.2, the expression for the mobility of charge carriers in organic semiconductors, derived from the characteristics of an OFET, has been defined. The actual value of mobility of the active semiconductor depends on a variety of parameters, such as interaction with the dielectric, charge trapping at the interfaces, charge injection;[27,36,37] as such, not only the material itself but all these factors need to be taken into account.

Reliability factor The equation for the extraction of the charge carrier mobility from the transfer characteristics mentioned above are derived according to the gradual channel approximation, for which the gate electric field orthogonal to the channel is much larger than the longitudinal one, and the mobility is independent from the carrier density. In this case, the extracted mobility values are influenced not only by the material properties, but also by extrinsic factors, such as grain boundaries, inhomogeneities, impurities and carrier trapping, and thus they need to be used carefully. In order to estimate the reliability of these parameters, a reliability factor r has been proposed.[38] It is defined as the ratio of the maximum channel conductivity measured experimentally with respect to the maximum conductivity in an equivalent ideal device, and has been calculated as follows

$$r_{lin} = \left(\frac{|I_{SD}|^{max} - |I_{SD}|^{0}}{|V_G|^{max}}\right) \Bigg/ \left(\frac{|V_{SD}|WC_{diel}}{L}\mu_{lin}\right)_{measured} = \left(\frac{|I_{SD}|^{max} - |I_{SD}|^{0}}{V_G^{max}}\right) \Bigg/ \left(\left|\frac{\partial I_{SD}}{\partial V_G}\right|\right)_{measured} \tag{2.11}$$

$$r_{sat} = \left(\frac{\sqrt{|I_{SD}|^{max}} - \sqrt{|I_{SD}^{0}|}}{|V_G|^{max}}\right)^2 \Bigg/ \left(\frac{WC_{diel}}{2L}\mu_{sat}\right)_{measured} = \left(\frac{\sqrt{|I_{SD}|^{max}} - \sqrt{|I_{SD}^{0}|}}{|V_G|^{max}}\right)^2 \Bigg/ \left(\frac{\partial\sqrt{|I_{SD}|}}{\partial V_G}\right)^2_{measured} \tag{2.12}$$

Once the reliability factor has been calculated, it is possible to determine the effective value of mobility, $\mu_{eff} = r * \mu_{measured}$.

Threshold voltage When dealing with organic devices operating in accumulation regime, this parameter loses its classical meaning. As seen in Section 2.2.2, the threshold voltage can be described as the minimum gate voltage that needs to be applied in order to have an accumulation of charges in the semiconductor layer. For high performance OFETs, and in order to grant a low voltage operation, this value needs to be as low as possible. The threshold voltage depends on a wide variety of factors, such as the thickness of the semiconducting layer, the quality of the substrate surface, the work function of the electrodes, the polarizability of the gate dielectric, the exposure to light and the bias stress.[39]

Contact resistance One of the critical aspects in the OFET performances is related with charge injection. In these devices, there is direct contact between the metal electrodes and the organic semiconductor, which leads to the formation of an energy barrier that hinders the flow of charges from one material to the other. This barrier can not easily be modified, and also the assessment of its value is compex, because of the two-dimensional nature of the electrode-semiconductor interface and the electrostatic modifications given by the gate electrode. All these factors are usually summed up into one single factor, called *contact resistance*. This is another critical parameter for the development of highly performing devices, and it needs to be as low as possible. In order

to decrease it, a proper alignment between the electrodes work function and the frontier orbital of the semiconductor needs to be obtained; this can be done, for example, by altering the electrodes' work function through the application of Self-Assembling Monolayers (SAMs). Additionally, staggered structures are to be preferred, since they have larger injection areas compared to planar devices.

On/off ratio This parameter is defined as the ratio between the drain currents in the "on" and "off" states, and it is desirable to have a ratio as high as possible. High on-currents drive the load faster, and can be achieved with higher semiconductor mobilities, while lower off-currents limit the static power consumption and leakage currents, and are obtained through proper material purification, optimization of the films' quality and suppression of defects and parasitics.[34]

Subthreshold swing The subthreshold region is defined for V_G lower than the threshold voltage. The subthreshold swing SS is measured at the maximum slope of $log(I_D)$ with respect to V_G,[40] as follows

$$SS = \frac{dV_G}{d(logI_D)} = \frac{kT}{q} ln10 \left(\frac{C_{diel} + C_D + CSS}{C_{diel}} \right) \tag{2.13}$$

where k is the Boltzmann constant, T the absolute temperature, q the charge of an electron, C_D the depletion capacitance per unit area and C_{SS} the surface state capacitance.
This parameter describes how fast the channel is switched on and off, and how wide is the gate voltage interval needed to turn on and off the device, so it needs to be minimized in order to have fast and low-voltage performances.

Hysteresis This parameter is defined as a shift in the threshold voltage between the forward and backward sweeps in a transfer characteristic; it is not directly related to the device itself, but more to its quality and stability. There are some parameters that might influence the presence of hysteresis in an OFET, namely migration of dopant molecules, slow dielectric relaxation, charge storage in the dielectric layer, and charge trapping in the semiconductor, caused by the presence of defects and impurities. Clearly, a small hysteresis is required, since large shifts in threshold voltage might lead to misoperations in logic circuits.[34]

Uniformity and stability Most large-scale applications require uniform performances for all the involved devices, so a high uniformity of the OFETs parameters is needed. This is not trivial for printed devices, where there might be variations in film thickness and microstructure; these defects need to be minimized, and this can be done, for example through thermal annealing steps, which relax mechanically the film, remove residual solvent and moisture, and stabilize the interface.

Additionally, devices should be stable, both in terms of long-term stability and under an applied bias. The first can be improved by means of passivation and encapsulation, while the latter is usually characterized by means of bias stress. A continuous application of gate bias might lead to an increased hysteresis, degradation of SS and/or a shift in the threshold voltage; a pure and ordered semiconductor film might help in mitigating this effect.

3

Experimental methods

"I've never seen the Icarus story as a lesson about the limitations of humans. I see it as a lesson about the limitations of wax as an adhesive."
– Randall Monroe

In this chapter, the materials and the fabrication techniques employed for the manufacturing of the devices realized during this thesis will be presented.

3.1 Materials

In this section, all the materials used for the fabrication of OFETs and circuits will be introduced. All the devices are fully organic, and carbon-based materials have been used as conductors, semiconductors and dielectrics.

3.1.1 PEDOT:PSS

$poly(3,4-ethylenedioxythiophene) : poly(styrene-sulfonate)$ (PEDOT:PSS) is a conductive polymer compound, obtained from a mixture of $poly(3,4-ethylenedioxythiophene)$ (PEDOT) and $poly(styrene-sulfonate)$ (PSS). PEDOT is a highly conductive but insoluble polymer, which can be made soluble in aqueous dispersion by synthesis in the presence of PSS, which forms a polyanionic matrix in which the PEDOT chains are incorporated. The chemical structure of these two polymers are shown in Figure 3.1.

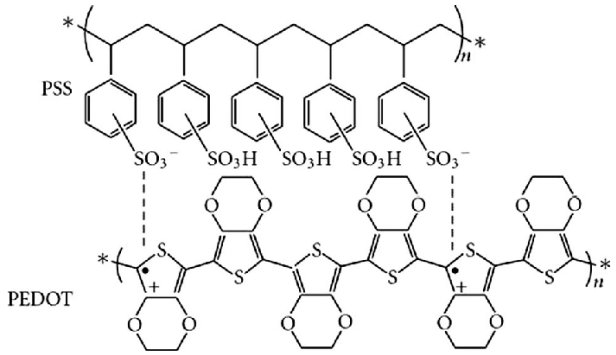


Figure 3.1: Chemical structure of PEDOT:PSS.

PEDOT:PSS films by themselves are highly hygroscopic and show relatively low values of mobility. Additives such as sorbitol, glycerol, DMSO and isopropanol, lead to an increased conductivity, which can reach values as high as 1000 Scm^{-1}.[41] This effect is mostly related with a reorganization and stabilization of the structure of the film, which becomes more homogeneous in presence of additives. Mobility values can be further enhanced through an annealing step.[42] In this work, a commercial formuation of PEDOT:PSS has been used, *Heraeus Clevios P Jet* 700.

3.1.2 PEI

Polyethyleneimine (PEI) is a polymer composed of two repeating units, an amine and an aliphatic spacer. There are two varieties of PEI,

linear and branched, as shown in Figure 3.2; in this work, branched PEI has been used, purchased from *SigmaAldrich* and with a $M_W = 10000$.

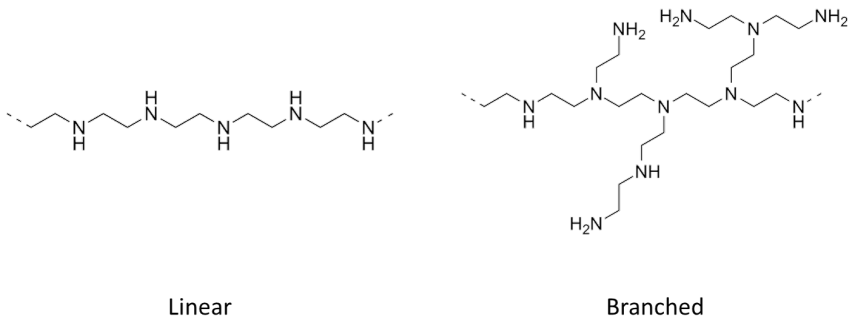


Figure 3.2: Chemical structure of PEI.

The role of PEI, and its contribution to the improvement of transistors' performances, will be discussed in Section 4.3.

3.1.3 P(NDI2OD-T2)

P(NDI2OD-T2), also known as *ActivInk N*2200, is an organic semiconductor produced by *Flexterra*, formerly *Polyera*, whose chemical structure is shown in Figure 3.3. It is an electron-transporting polymer, which shows high solubility and printability, together with outstanding electrical performances.[43]

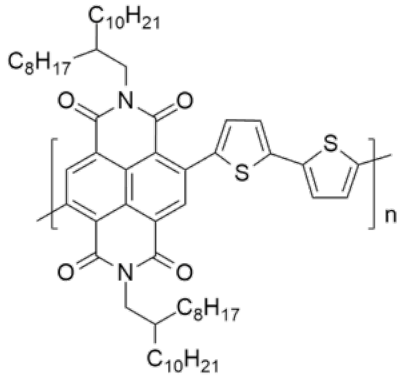


Figure 3.3: Chemical structure of P(NDI2OD-T2).

This material is highly soluble in conventional organic solvents and presents no thermal transitions up to 300 °C, its LUMO and HOMO levels are around −4.0 eV and −5.6 eV respectively,[43] and field-effect mobilities up to 6.4 $cm^2V^{-1}s^{-1}$ have been shown.[20]
Electron injection from high W_F materials is not favourable, so a strategy to decrease the work function of the contacts has been developed,

and will be presented in Section 4.3.
For the devices presented in this work, P(NDI2OD-T2) has been dissolved in mesitylene, with a concentration of 5 $mgml^{-1}$; this solution allows to combine proper printability of the ink with the formation of pre-aggregates in solution, key element for achieving high mobility values.[20]

3.1.4 DPP-based organic semiconductors

In this thesis different organic semiconductors have been used for the fabrication of *p*-type OFETs. These materials have a common backbone, the electron-accepting diketopyrrolopyrrole (DPP) moiety, which has attracted great interest for the fabrication of high-performance donor-acceptor polymers.
For the work presented in Chapter 4, $29-(diketopyrrolopyrrole-thiophene-vinylenethiophene)$ (29-DPP-TVT) has been used. This material has been synthesized according to[44] and its chemical structure is shown in Figure 3.4. It has LUMO and HOMO levels around −3.97 eV and −5.25 eV respectively, which allow for a good injection from high work function polymers and metals. The maximum field-effect mobility reported in literature is equal to 5.76 $cm^2V^{-1}s^{-1}$.

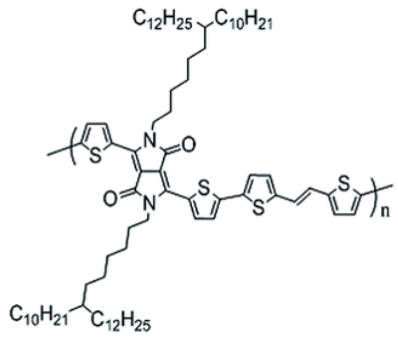


Figure 3.4: Chemical structure of 29-DPP-TVT.

In the second part of this work, another DPP derivative has been used, $diketo-pyrrole-pyrrole-thieno[2-3,b]thiophene$ (DPPT-TT); this material has been purchased from $1-Material$. Its HOMO and LUMO levels are close to those of 29-DPP-TVT, equal to −5.33 eV and −4.07 eV respectively.[45]
Both these materials have been dissolved in 1,2-dichlorobenzene (o-DCB), with concentrations varying between 2.5 and 5 $mgml^{-1}$.

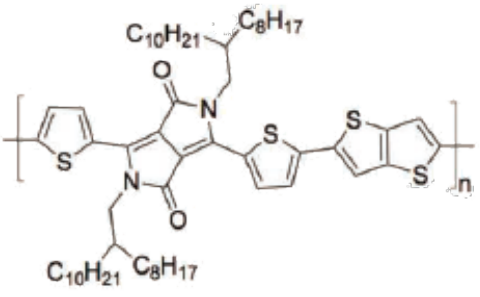


Figure 3.5: Chemical structure of DPPT-TT.

3.1.5 PS

Polystyrene (PS) is an aromatic polymer and one of the most widely used plastic, with applications such as packaging, containers and bottles. In organic electronics, it founds applications both as dielectric material and as blending component, to be used in combination with semiconducting materials; for what concerns the results presented in this thesis, it has only been used in semiconducting blends and not as a dielectric.

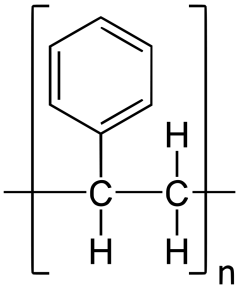


Figure 3.6: Chemical structure of PS.

The PS used in this work, purchased from *SigmaAldrich*, has a molecular weight of $M_W =$. Since it has been used only for blending purposes with the DPP-based semiconductors, the same solvent has been used, namely 1,2-dichlorobenzene (o-DCB), and the same concentration has been considered for both materials, in order to simplify the evaluation of the relative concentrations in the final solution.

3.1.6 PMMA

$Poly(methyl - methacrylate)$ (PMMA) is a trasparent thermoplastic polymer, commonly used for a wide variety of applications. In organic electronics, it is used as a solution processable dielectric, with a relative

dielectric constant $\epsilon_r = 3.6$.

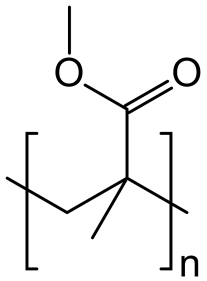


Figure 3.7: Chemical structure of PMMA.

For the devices presented in this work, PMMA has been purchased from *SigmaAldrich* and has a molecular weigth $M_W = 120000$. The solvent of choice is n-butyl acetate.

3.1.7 Parylene

Parylene is the trade name for $poly(p-xylylene)$, a family of dielectric polymers usually deposited by chemical vapour deposition. There are different kinds of parylene, showing different substituents on both the benzene ring and the alkyl groups. The most popular version, and the one used in this work, is parylene C, also known as $poly(chloro-p-xylylene)$, whose structure is shown in Figure 3.8.

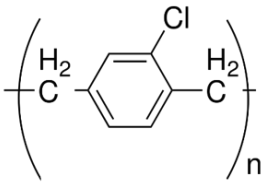


Figure 3.8: Chemical structure of parylene C.

This material is a low-k, semi-crystalline, thermoplastic polymer, deposited by a solvent-free technique. This allows to deposit conformal and pinhole-free films, which are thus very interesting as moisture and dielectric barrier.
In this work, parylene has been employed both as substrate and encapsulation layer, exploiting its properties as barrier against the environment, and as dielectric layer. The latter has been considered for all the devices presented in this work, while for what concerns the barrier role, it will be presented in Chapter 5.

3.2 Methods

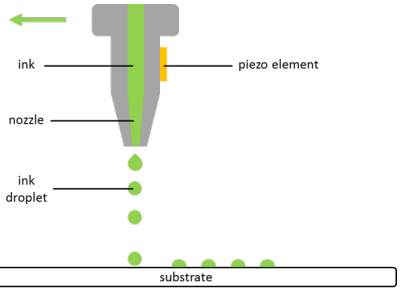
In this section, the manufacturing technique considered in this work will be presented. All processes have been performed in a grey room, with controlled temperature and humidity.

3.2.1 Ink-jet printing

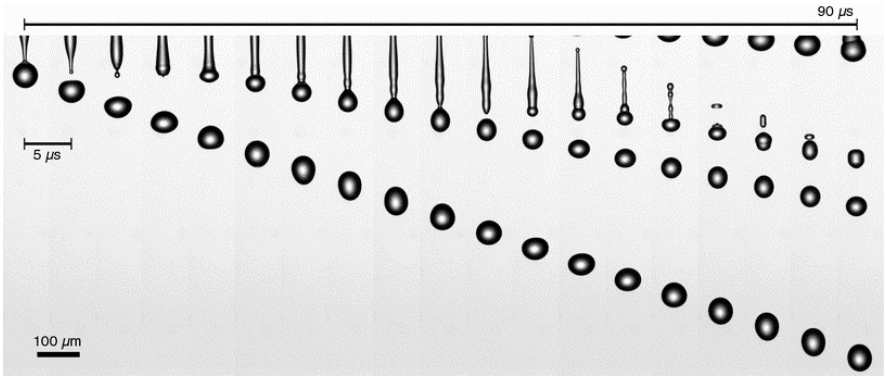
The main manufacturing technique used for the devices presented in this thesis is ink-jet printing.
Ink-jet printing is a digital manufacturing technique, which allows to create custom pattern without employing masks or other expensive templates. It is used for many applications, ranging from electronics to tissue engineering, thanks to the possibility of precisely depositing picoliters of solution in the desired fashion, with a very low wastage of ink. It is a non-contact additive technique, compatible with a variety of substrates, such as delicate and fragile ones, but also flexible films. It is possible to ink-jet print a wide range of materials, by appropriately tuning the viscosity of the ink, which should lay in the range between 1 and 50 mPa. Lastly, it is a roll-to-roll and easily scalable technique, compatible with large-area fabrication.[46,47]
There are two kinds of printers, continuous and drop-on-demand (DoD). In the first case, a stream of droplets is continuously ejected from the nozzle, and the fluid is then either directed on the substrate or recirculated. DoD printers, on the other hand, make use of a print head from which a droplet is ejected only when needed. This approach is very useful for the deposition of functional inks, since it has high flexibility and allows for the deposition of high-resolution patterns, but has one main drawback related to the ease of clogging of the nozzle. There are different actuation methods that have been reported for DoD ink-jet printing, namely piezoelectric actuation, acoustic actuation, electrohydrodynamic-jet printing and thermal ink-jet printing. Electrohydrodynamic is the one giving the smallest drop size, and so the best resolution, but the only actuation method which has been scaled to multi-nozzle systems, and thus applied to industrial scale manufacturing, is the piezoelectric one.[47]
For the devices fabricated in this work, a *Fujifilm Dimatix DMP 2831* has been used. This is a drop-on-demand printer with piezoelectric actuation. In these systems, the ejection of the droplet is given by the pressure waves generated by the variation in volume of the cavity of the printhead, in turn given by the application of a voltage to the piezoelectric actuator. The cycle that leads to the formation and ejection of a droplet can be divided into four main steps, reported in Figure 3.10.

During the idle phase, before the pulse starts, the piezoelectric element is kept in a slightly deflected position. When the pulse starts, the signal applied to the piezoelectric element leads to its relaxation and the subsequent expansion of the cavity, with a negative pressure wave expanding both toward the supply end and the nozzle. At the supply side, the pressure wave is reflected, generating a positive compression wave which pulls the ink inside the chamber. In the following phase, the piezoelectric element is bent inward, compressing the ink in the cavity, and generating a positive pressure wave that, properly timed with the reflected wave of the previous phase, can generate a reinforced wave. In this way, when the pressure wave reaches the nozzle orifice, the ink is ejected, and the acoustic energy is converted in kinetic energy. After the droplet ejection, the last step takes place, needed in order to remove the residual acoustic waves propagating in the chamber. Here the signal applied to the piezoelectric actuator is brought back to its original value, with a final expansion of the cavity, and in this way the ejection of satellites droplets is avoided.
In order to overcome the deceleration given by the ambient atmosphere, the droplet initial velocity needs to be very high, otherwise it would deviate from its intended trajectory. The volume of the droplet and its velocity are directly proportional to the amplitude of the driving voltage, while a more complex relationship is given by the variations in pulse width and frequency. The cartridges employed in this work are 10 *pl* ones, which allow for the deposition of lines with a width in the order of tens of µm.[48]
In this work, ink-jet printing has been used for the fabrication of all the layers except for the dielectric one, namely PEDOT:PSS conductive electrodes, the injection layer and all the semiconductive pads.

(a) Fujifilm Dimatix DMP-2831.



(b) Ink-jet printing process.



(c) Drop-on-demand printer jet.

Figure 3.9: (a) Photo of the Fujifilm Dimatix DMP-2831 printer. (b) Schematic representation of the ink-jet printing process. (c) Stroboscopic sequence of a drop-on-demand-printed jet that breaks up into droplets, adapted from.[49]

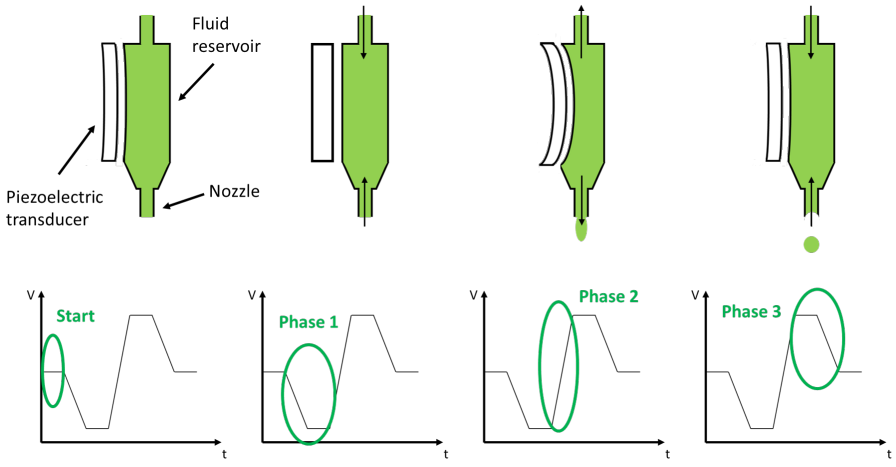
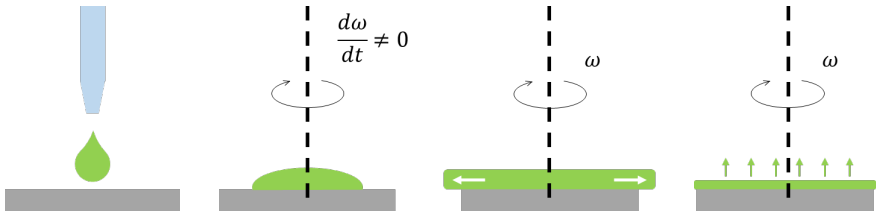


Figure 3.10: Four main steps of the droplet formation by means of piezoelectric actuation.

3.2.2 Spin-coating

Spin coating is a manufacturing technique used to deposit uniform thin films onto flat substrates. A certain amount of ink is deposited on the substrate, which is then rotated at high speed; this technique relies on the use of centrifugal forces in order to spread the solution uniformly over the substrate. The thickness and quality of the so-obtained films depend on a variety of parameters, e.g. rotation speed, rotation acceleration, processing time, viscosity of the solution.[50]
This technique has become very popular thanks to its simplicity, but some drawbacks are present, namely the fact that some of the material is wasted, the limitations on the maximum device size, and the difficult inclusion of this fabrication step into a roll-to-roll processing. Possible alternatives to spin coating, which has not been considered in this work but would need to be explored in case of an industrially scaled manufacturing of these electronic devices, include bar coating, knife coating, doctor blade, slot die, multilayer slot and slide coating.[51]



(a) Deposition of the solution. (b) Acceleration. (c) Spreading of the solution. (d) Solvent evaporation.

Figure 3.11: Different stages of the spin coating process.

For what concerns this work, spin coating has been used for the deposition of ultra-thin layers of PMMA.

3.2.3 Chemical Vapour deposition (CVD)

Chemical vapour deposition (CVD) is a manufacturing technique used for the deposition of conformal and high-quality thin films. It is a vacuum and solvent-free technique, in which the precursors are deposited on the substrate, where they react and form the desired coating.
In this work, this technique has been used for the fabrication of parylene films. The precursor in this case is a dimer, which is first vaporized at a temperature in the range 120 to 150°C, then undergoes pyrolysis inside a furnace at 690 °C, and lastly enters the deposition chamber in the form of highly reactive monomer, which deposits on all the surfaces and polymerizes at room temperature, as shown in Figure 3.12.[52] The deposition chamber is connected with the cold trap, a metallic finger

kept at about −90 °C, where all the byproduct of the polymerization is collected. The deposition is carried out in low-vacuum conditions, with a pressure inside the deposition chamber of about 0.05 Torr.

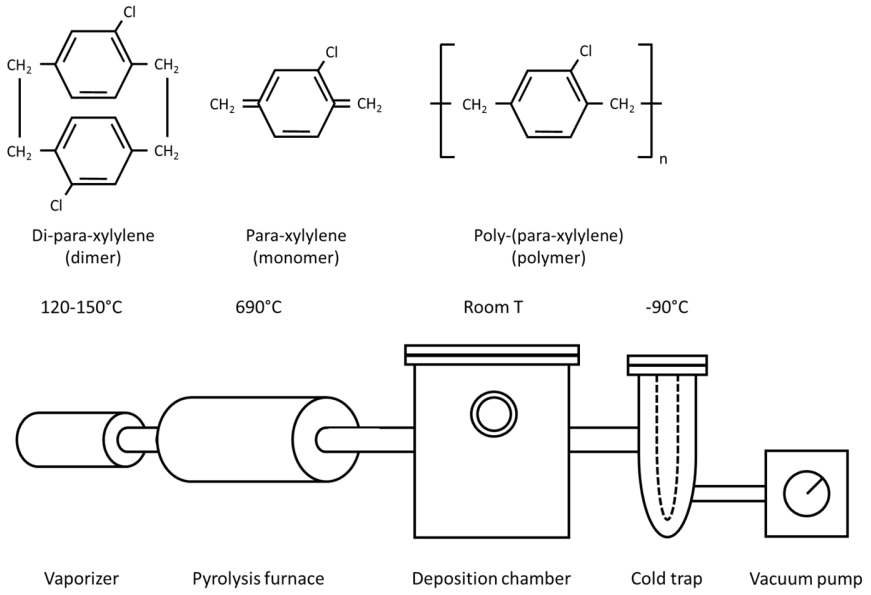


Figure 3.12: Deposition steps for parylene films via chemical vapour deposition. The raw dimer is vaporized in the vaporizer, then undergoes pyrolysis into the furnace, and finally is deposited in the deposition chamber.

4

Low-voltage complementary transistors and circuits on flexible substrates

"Never let the fear of failure keep you from failing."
– @TheTweetOfGod

In this chapter, the fabrication and characterization of all-organic complementary organic transistors and circuits, operating at low-voltage, is presented. The first part of this work is devoted to the optimization and integration of a dielectric layer that allows for a low-voltage operation of the electronic devices. In the second part of the chapter, the fabrication of complementary organic transistors is presented, together with their electrical and mechanical characterization. Lastly, the realization and characterization of complementary organic circuits is reported, namely inverters, ring oscillators, D-Latch and D-Flip-Flop. The work presented in this chapter represents the first demonstration of printed, all-polymeric, transparent, and flexible complementary transistors and circuits operating at low voltage.

4.1 Introduction

In the last decades, there has been great interest in the field of flexible microelectronics, given mainly by the possibility of integrating low-cost and light-weight electronic devices into consumer products. Working in this direction, one of the best candidates is represented by organic electronics, where transistors and circuits based on printed semiconductors can be fabricated by means of low-temperature printing techniques onto a wide variety of substrates, including flexible plastic ones. For this reason, these devices are one of the best candidates to meet the cost requirements needed for flexible electronics to hit the consumer market.[53]

Many examples of organic electronic devices can be found in literature, with reports of OLEDs,[54–57] organic solar cells,,[58–62] organic memory devices,[63–69] and organic transistors and circuits.[70–78] Focusing on Organic Field Effect Transistors (OFETs), they are the main building block for a variety of electronic application such as circuits,[15,79] memory devices,[80] displays,[81] sensors,[82–84] photodetectors,[85–88] amplifiers,[89,90] and oscillators.[91] Many works have been reported in literature, with a wide variety of processing techniques and materials employed to fabricate high-performance OFETs. These devices can be classified in many different ways, following the most different criteria; a whole classification of the OFETs presented in literature is however beyond the scope of this work. For what concerns this thesis, focus will be on ink-jet printed and all-organic OFETs. The first all-polymeric printed organic transistor has been presented by Garnier *et al.*[92] Many works have followed, with continuously improving performances, but some constraints are still present.

One of the limitations hindering the diffusion of flexible organic devices is related with the operating voltage of these devices. In order to have a successful integration into everyday products, organic circuits need to be portable, and this means that their powering units should be small and portable too. Thin film batteries and/or plastic solar cells are the best candidates to fullfill these requirements, but they are capable of sustaining only an operating voltage of few volts and small power consumption.

In the first part of this chapter, the main strategies for the development of OFETs operating at low voltages are introduced, and the successful implementation of one of them is shown, with the realization of organic transistors operating in the sub-$10V$ regime. In the second part, the integration of these transistors into more complex organic circuitry will be presented.[16]

4.2 Dielectric layer optimization

Different strategies can be employed toward the development of efficient low voltage devices, working on various transistors parameters; the one we chose for this work, in particular, acts on the capacitance of the dielectric layer. In order to reduce the operating voltage of an OFET, the dielectric capacitance needs to be as high as possible, and it should guarantee proper charge accumulation and transport for both electrons and holes at the same time.
The capacitance of a dielectric layer C_{diel} can be described as

$$C_{diel} = \frac{\epsilon_0 \epsilon_r S}{t} \tag{4.1}$$

where ϵ_0 is the vacuum permittivity, ϵ_r is the relative permittivity of the dielectric material, S is the area involved and t is the thickness of the dielectric layer. In order to increase the dielectric capacitance, we can either increase the dielectric constant of the material or decrease its thickness. For what concerns the first, the integration of high-k materials in OFETs is not straightforward, since they induce energetic disorder at the interface with the semiconductor, and can thus disrupt charge transport processes inside the semiconducting layer.[93,94] In order to overcome this issue, multilayer structures have been proposed, with a combination of low-k and high-k materials;[95,96] in this way, proper low voltage operation can be achieved, but high-k materials undergo dielectric relaxation at low frequency,[97,98] thus limiting the maximum operating frequency of the so-obtained OFETs. This limitation becomes even more evident when considering electrolyte-gated devices,[99] even solid-state ones,[100] in which huge capacitances are achieved thanks to the employment of electrolytes as gate dielectrics, characterized by huge amounts of ions, which unfortunately are very slow-moving.
In order to avoid these limitations, downscaling of the thickness of a low-k dielectric layer seems the obvious choice; however, thickness reduction in solution-processed dielectrics commonly used in OFETs leads to high leakage currents and breakdown of the transistors. One material that might help overcoming this issue is *poly(chloro-p-xylylene)-C*, also known as parylene C, a semicrystalline, low-k, thermoplastic polymer; the deposition technique of choice for parylene is Chemical Vapour Deposition (CVD), which is industrially scalable and compatible with large-area substrates.[52]
Parylene shows some appealing features, such as low disorder at the dielectric-semiconductor interface,[101] flexibility and chemical inertness, and it is able to form conformal, pinhole-free films even with reduced

thicknesses.[101,102] For these reasons, parylene has been investigated as dielectric material for OFETs, with most of the works dealing with bottom-gated structures,[103–111] where the dielectric is deposited directly onto the substrate and not on the semiconductor's surface. Top-contact staggered configurations, on the other hand, are to be preferred, for the reasons mentioned in Section 2.2.1. Only one single example of staggered devices with parylene as dielectric has been reported in literature,[112] and it showed devices with opaque metallic contacts and operating voltages around 30 V, thus far away from the low voltage regime.
In this work, a thin parylene film has been exploited for the realization of a high capacitance dielectric layer. Parylene has been integrated into a bilayer configuration, together with an ultra-thin solution-processed PMMA layer. In this way, the excellent dielectric properties of parylene have been combined with the optimal interface that PMMA forms with many organic semiconductors.[113] The presence of PMMA leads also to better injection performances and allows to reach higher currents, mostly in the linear regime, as shown in Figure 4.1; the degradation in performances given by a direct interface between parylene and the semiconductors is mostly due to the presence of chlorine atoms in the first, which alter the charge transport properties of P(NDI2OD-T2).[112]

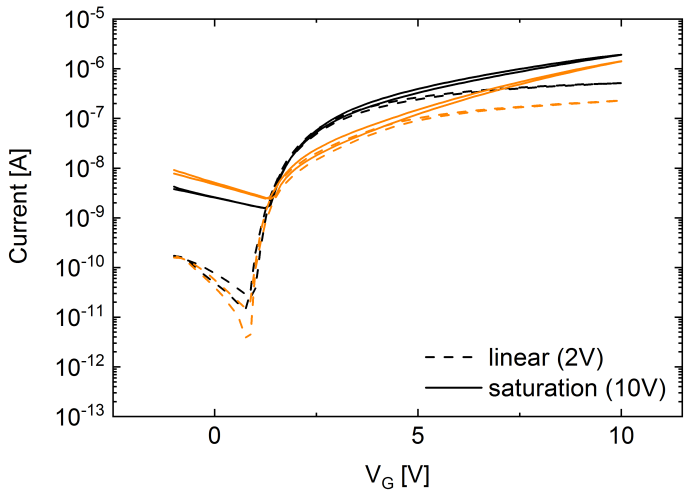
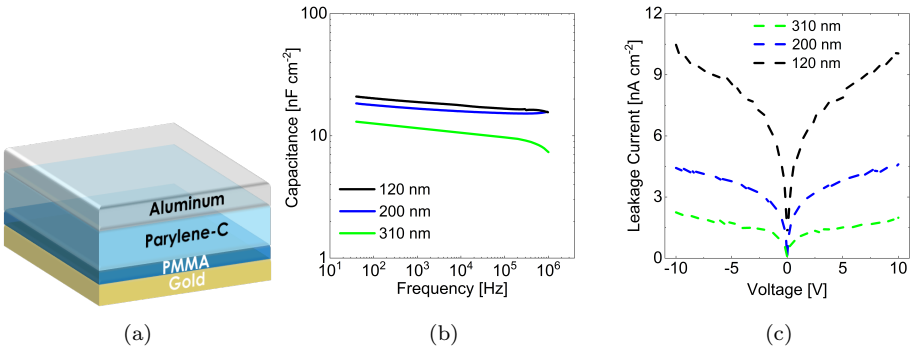


Figure 4.1: Transfer curves for *n*-type OFETs, with (black) and without (orange) the PMMA interlayer.

As a first step, the dielectric performances of the above mentioned bilayer have been investigated. While the PMMA layer is 20 nm thick, the thickness of the parylene layer has been varied in order to find

the optimal one, and three different capacitors have been examined, with parylene layers' thickness equal to 120, 200 and 310 nm. The capacitance as a function of frequency has been measured and is shown in Figure 4.2b; for this characterization, a MIM (metal-insulator-metal) structure, with the dielectric layer sandwiched between two metallic electrodes, has been employed, as shown in Figure 4.2a. The areal capacitance at 1 kHz for the 310 nm device is equal to 11.54 $nFcm^{-2}$, while it increases to 16.69 and 19.00 $nFcm^{-2}$ for the 200 and 120 nm capacitors respectively.
The average leakage currents at 10 V have also been characterized, and the average values are 10, 4.6 and 2.2 $nAcm^{-2}$ for the 120, 200 and 310 nm devices respectively (4.2c). A parylene thickness lower than 120 nm clearly leads to higher capacitances, but the leakage currents increase too, leading to a too high number of defective capacitors. As a result of this characterization, the dielectric layer employed for the fabrication of the transistors and circuits presented in this chapter is composed of a 20 nm thick PMMA layer and a parylene film with a thickness of about 100 nm, ensuring a good compromise between low operating voltage and reduced leakage currents, uniform perfomances and high yield.



(a) (b) (c)

Figure 4.2: (a) Schematic of the MIM structure. (b) Capacitance as a function of frequency and (c) leakage current density of the capacitors. The values shown here have been obtained as an average over three identical devices.

4.3 Injection layer optimization

After the successful fabrication of a dielectric layer with high capacitance and relatively low leakage current, and before being able to fabricate complementary OFETs with high performances, an interlayer for the *n*-type devices has been formulated and optimized. This need arises from the misalignment between the electrodes' work function and the LUMO level of the semiconductor; in fact, the source and drain electrodes of the *n*-type OFETs need to show a low work function, in order to properly align with the LUMO of the semiconductor and so easily inject electrons.
This requirement is readily satisfied by low work function metals, such as calcium and magnesium or alkali-coated metals, but they are usually highly reactive elements that quickly oxidize if oxygen is present, so they are not compatible with the fabrication techniques usually employed in organic electronics. Other approaches have been exploited and presented in literature, and they rely on the use of ultra-thin layers of low WF conducting or semiconducting materials deposited on top of the electrode, such as ZnO or In_2O_3, acting as mediator during the charge injection from the electrode to the semiconductor,[114,115] or the use of chemisorbed self-assembled monolayers (SAMs) of dipolar molecules,[116] or the coating with chemi/physically adsorbed layers of materials creating strong molecular dipoles able to shift the vacuum level and so the work function of the electrode.[117] All these approaches are case-specific, relying on a specific combination of electrode and interlayer. A universal approach, on the other hand, has been proposed by Zhou *et al.*,[118] with the employment of an ultra-thin layer of a polymer presenting aliphatic amine groups which is physisorbed on the electrode surface. This layer, differently from the physisorbed ones mentioned above, is not acting as charge-injection layer but as surface modifier. It is, in fact, a large band-gap insulator with an intrinsic dipole moment given by the neutral amine groups, and its interaction with the electrode surface has a charge-transfer character; the combined effect of this kind of interaction and of the dipole moment leads to a work function shift with a variety of conductors.
In this work, *polyethyleneimine* (PEI) has been considered for the injection layer, since it presents a high quantity of primary, secondary and tertiary amines, and because it can easily withstand the thermal treatments that characterize the fabrication of the devices presented in this thesis.
The injection layer solution has been optimized, properly tailoring the components, their relative ratio and the concentration of PEI in the

final solution. The best performing injection layer is composed of ethylene glycol (20% vol), a solution of ZnO nanoparticles in isopropanol (30% vol, the nanoparticles concentration is 2.5% *wt*) and PEI dissolved in water (50% vol). The concentration of PEI in water is 0.2% *wt*, so its concentration in the injection layer solution is close to 0.1% *wt*. This hole-blocking/electron-injecting solution can be deposited by means of ink-jet printing and has been used for all the *n*-type devices presented in this work. The role of the PEI interlayer on the performances of *n*-type transistors is shown in Figure 4.3. Its presence improves the turn-on of the device in saturation regime, but it has a more marked effect in linear regime, where it strongly improves the subthreshold swing and allows to reach mobility values up to one order of magnitude higher than those without interlayer.

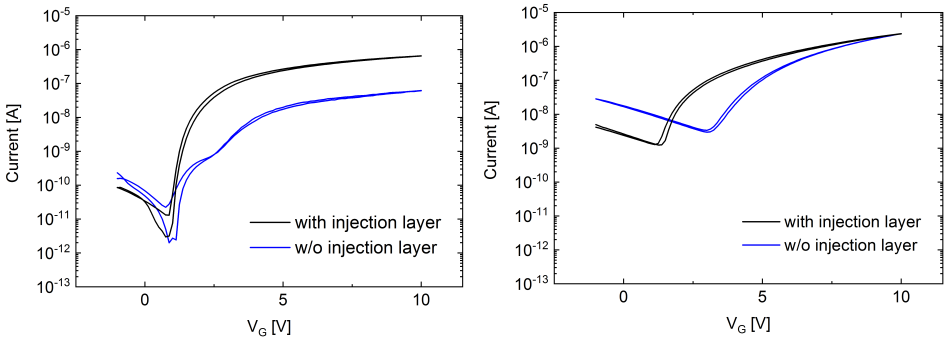


Figure 4.3: Transfer characteristics, in (a) linear and (b) saturation regime, for an *n*-type OFET. These devices have been fabricated at the same time on the same substrate, the only difference between them being the presence or not of the PEI injection layer.

4.4 OFETs fabrication and electrical characterization

All the OFETs presented in this work, both in this chapter and the following, employ a bottom-contact top-gate structure (Figure 4.4a), and have been fabricated by means of additive, cost-effective and industrially scalable processes; ink-jet printing is the technique of choice, and has been used for all the layers except for the dielectric one.
First, PEDOT:PSS source and drain contacts have been ink-jet printed onto the substrate (Figure 4.4b). The channel length L is equal to 60 µm on average, being the smallest distance between two printed PEDOT:PSS lines that can be reproducibly and reliably deposited by the ink-jet printing system employed in this thesis, while the channel width W is equal to 1000 µm, granting a high enough drain current flow in the device, without being too wide and thus leading to an excessive surface occupation. Small metallic pads have been printed on the electrodes involved in the electrical characterization, using a silver nanoparticles-based ink; these pads are only needed in order to facilitate the electrical tests, and the devices can properly operate also without them in a fully transparent configuration. The contacts of n-type devices have been functionalized with the PEI-based injection layer presented in Section 4.3 (Figure 4.4c), which has been deposited by ink-jet printing, as well as the semiconducting layer. For the devices presented in this chapter, P(NDI2OD-T2) is the semiconductor of choice for the n-type OFETs, while 29-DPP-TVT has been used in p-type ones (Figure 4.4d and Figure 4.4e). The PMMA layer has been spin-coated on the devices after the deposition of the semiconducting layers, and parylene has been subsequently deposited by means of CVD. As a last step, PEDOT:PSS gate electrodes have been ink-jet printed (Figure 4.4f).
The process presented here allows to fabricate OFETs and inverters, while there is the need of additional steps for realizing ring oscillators, D-Latches and D-Flip-Flops. In particular, all of them require the creation of interconnections between the source/drain layer and the gate electrodes, and this is achieved by drilling via-holes with a laser before printing the gate electrodes. D-Latches and D-Flip-Flops also need a further layer of interconnections; for this reason, a thick insulating layer of PMMA (around 400 nm thick) has been deposited after the gate printing, via-holes have been chemically drilled in this layer using *chlorobenzene* as solvent, and finally the PEDOT:PSS interconnections have been ink-jet printed.

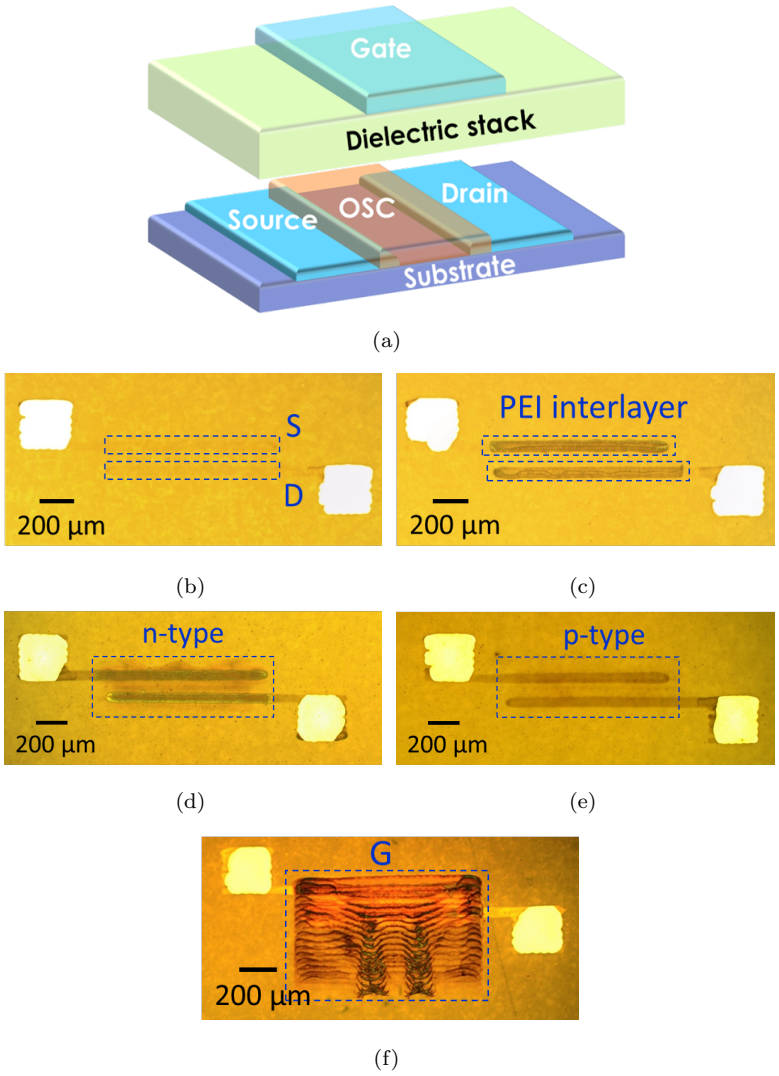
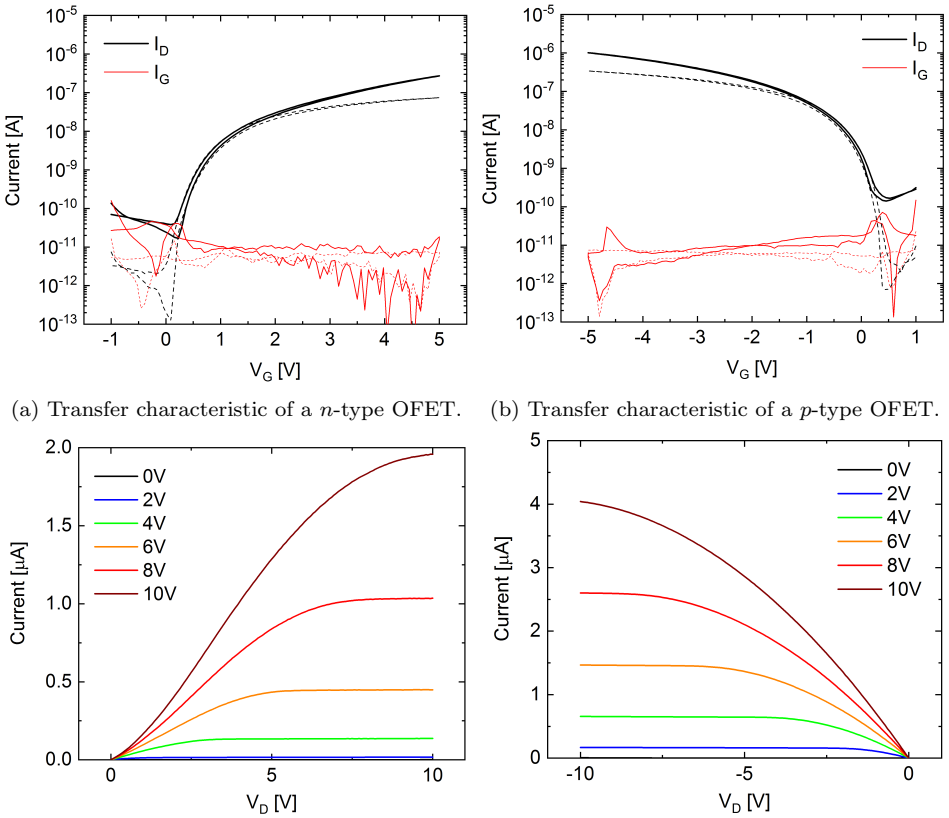


Figure 4.4: (a) Schematic of the structure of the printed top-gate bottom-contact OFET. Optical micrographs of the fabrication steps: (b) PEDOT:PSS source and drain electrodes, (c) electrodes of the *n*-type devices with the PEI interlayer, (d) and (e) printed semiconductor pads, P(NDI2OD-T2) and 29-DPP-TVT for *n*- and *p*-type respectively, and (f) printed PEDOT:PSS gate.

OFETs have been electrically characterized, and the results are shown in Figure 4.5. First, the transfer curves for *n*- and *p*-type devices are presented in Figure 4.5a and 4.5b, and they show proper current modulation for voltages as low as 1 V. Output curves (Figure 4.5c and 4.5d) show an ideal behaviour for what concerns *p*-type OFETs, while *n*-type devices show an S-shaped curve, mostly related to contact effects, which does not hinder low voltage behaviour nonetheless.
The uniformity of the performances of these devices have been tested,



(a) Transfer characteristic of a n-type OFET.

(b) Transfer characteristic of a p-type OFET.

(c) Output characteristic of a n-type OFET.

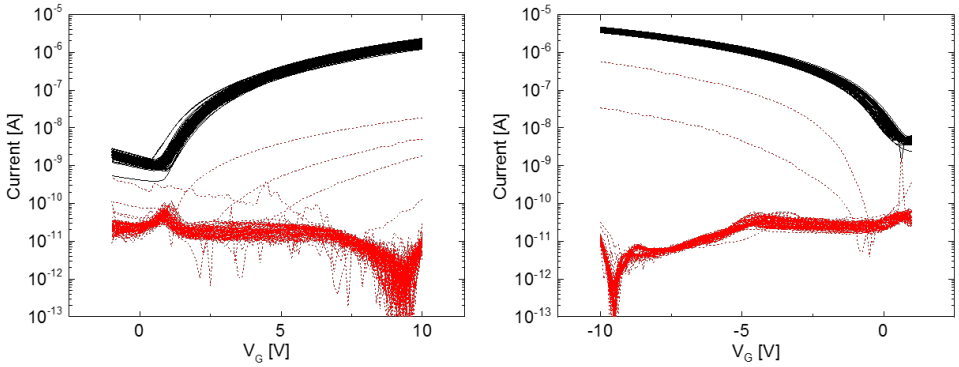
(d) Output characteristic of a p-type OFET.

Figure 4.5: Electrical characteristics of printed n- and p-type OFETs.

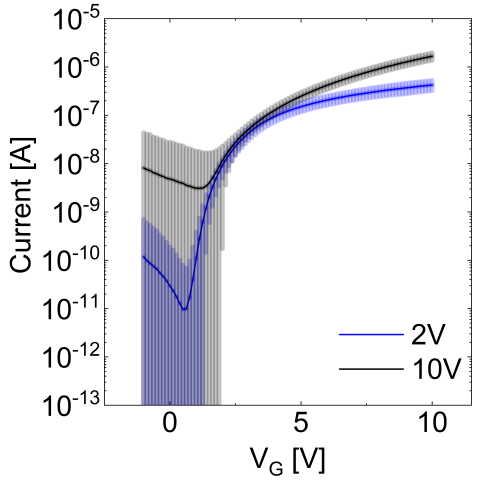
and 100 transistors for each type have been electrically characterized. The raw data are shown in Figure 4.6a, while the average transfer curves, for n- and p-type devices, are shown in Figure 4.6b and 4.6c, for applied source-drain voltages V_{DS} equal to 2 V in linear regime and 10 V in saturation. As it can be seen from the standard deviations in these last two plots, the performances of the OFETs are pretty uniform.

The average maximum current, extracted from the 10 V curves, is equal to 1.67 ± 0.29µA for n-type OFETs and 4.02 ± 0.28µA for the p-type ones. The difference between these two values can be explained considering the combined effects of the field effect mobilities of the two semiconductors and their threshold voltages.

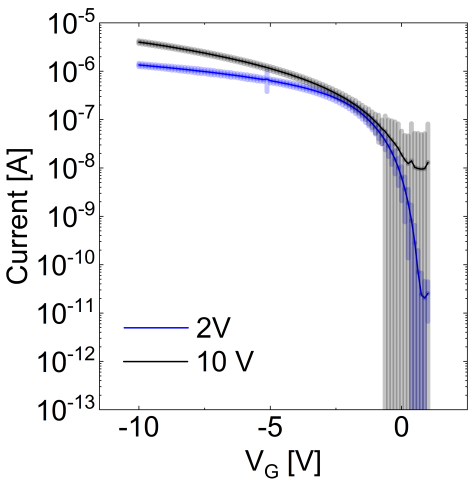
The average field effect mobilities for these devices have been extracted, according to Equations 2.8 and 2.10 presented in Section 2.2.2, and the resulting values, all in $cm^2V^{-1}s^{-1}$, are shown in Table 4.1, while the average mobility curves are shown in Figure 4.7.



(a) Raw data of the transfer curves for the 100 transistors arrays, p-type (left) and n-type (right).



(b) Average transfer curve and standard deviation for n-type OFETs.



(c) Average transfer curve and standard deviation for p-type OFETs.

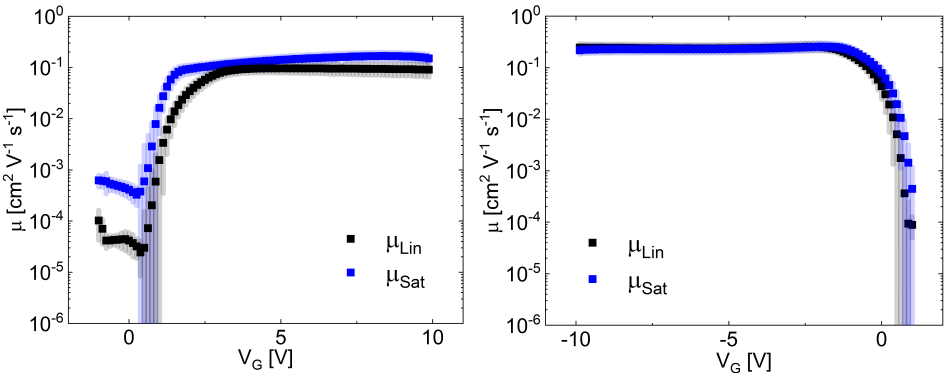
Figure 4.6: Raw transfer curves for the two 100-transistors array (a) and average transfer curves, with standard deviation, for (b) n- and (c) p-type OFETs. The average curves are shown for both linear and saturation regimes, while raw data refer only to the saturation one, with an applied drain voltage equal to ± 10 V.

The reliability factors, presented in Section 2.2.3, have been calculated, and the mobility values have been corrected accordingly. The r factors for n-type devices are equal to 0.81 and 0.73, for linear and saturation regimes respectively, while for p-type OFETs they are equal to 0.96 and 0.95. The latter thus show almost ideal performances, and the difference between measured and effective mobilities is negligible, while the first have slightly less ideal characteristics, yet with effective mobilities not so far from the measured ones. The effective mobilities, calculated as $\mu_{eff} = r * \mu_{measured}$ and all in $\mathrm{cm^2V^{-1}s^{-1}}$ units, are presented in Table 4.2.

The electrical characterization of these devices has been completed

Table 4.1: Average mobility values for p- and n-type OFETs, in linear (±2 V) and saturation regimes (±10 V).

	Linear regime ($V_{DS} = \pm 2V$)	Saturation regime ($V_{DS} = \pm 10V$)
p-type OFETs	0.24	0.25
n-type OFETs	0.09	0.14



(a) Average linear and saturation mobility curves as a function of the gate voltage for n-type OFETs.

(b) Average linear and saturation mobility curves as a function of the gate voltage for p-type OFETs.

Figure 4.7: Mobility curves, in linear and saturation regimes, as a function of the gate voltage, for (a) n- and (b) p-type transistors.

with the evaluation of few other parameters presented in Section 2.2.3, namely threshold voltage, turn-on voltage, subthreshold swing and on-off ratio. All the average values, for n- and p-type devices, are shown in Table 4.3.

For what concerns the yield of this manufacturing process, only two devices over the 200 considered were found to be not working, leading to a yield equal to 99%. The two not working devices have been inspected under the microscope, and in both cases some particulate has been

Table 4.2: Average effective mobility values for p- and n-type OFETs, in linear (±2 V) and saturation regimes (±10 V), obtained from the mobilities in Table 4.1 corrected for the r factor.

	Linear regime ($V_{DS} = \pm 2V$)	Saturation regime ($V_{DS} = \pm 10V$)
p-type OFETs	0.23	0.24
n-type OFETs	0.07	0.10

Table 4.3: Average threshold voltage, turn-on voltage, subthreshold swing and on-off ratio for n- and p-type OFETs.

	n-type OFETs	p-type OFETs
Threshold voltage [V]	1.35 ± 0.41	0.49 ± 0.21
Turn-on voltage [V]	1.00 ± 0.22	0.68 ± 0.30
Subthreshold swing [mVdec^{-1}]	126 ± 25	148 ± 23
On-off ratio	$7 * 10^6$	$5 * 10^5$

found in the active region (Figure 4.8); it is thus possible to claim that this fabrication method, carried out in more controlled environment, such as a cleanroom, can give a 100% yield.

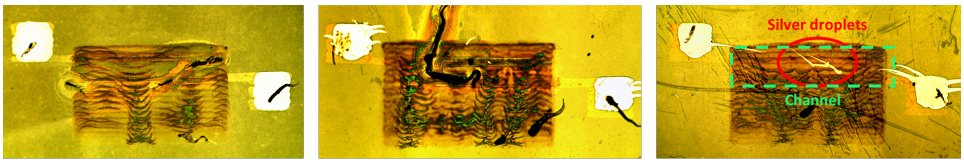


Figure 4.8: Optical micrograph of some defective transistors. The two pictures on the left refer to non-working OFETs; in both cases, the cause of failure can be found in the presence of dust particles in the channel. The image on the right, on the other hand, represents an OFET with non-ideal leakage current; the cause of this non-ideality is to be found in the presence of silver droplets in the channel.

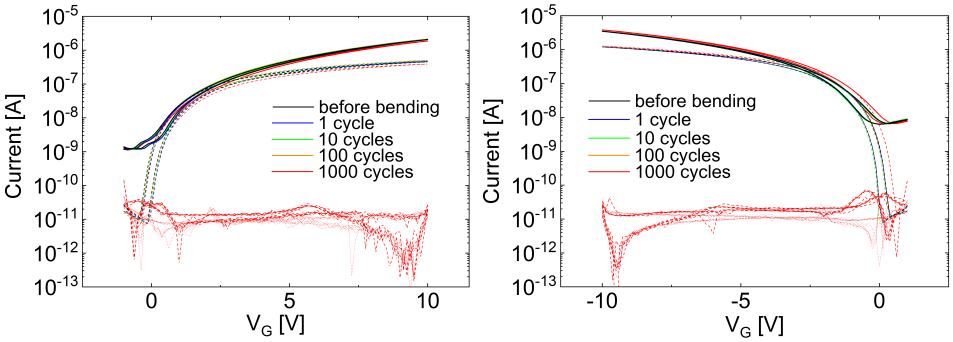
Lastly, considering the leakage current, it can be seen that the vast majority of the analysed OFETs shows flat gate currents, with average values below 100 pA. Figure 4.6a shows how more than 90% of the devices are in this regime, while only few OFETs for each polarity have a leakage current that increases with the applied gate voltage, yet maintaining proper operation and mobility values close to the low-leakage ones. A further analysis of these devices has highlighted the possible cause of the non-ideal leakage current, which is related with the accidental presence of small silver droplets. Considering that silver pads are only needed for the characterization of transistors and circuits in the development phase, and not for their actual operation, it can be seen how the main cause of non-ideal leakage would be eliminated considering the fully-transparent configuration.

4.5 OFETs mechanical characterization

The transistors presented in the previous section have been mechanically characterized in order to test their flexibility. Bending tests have been performed, with different bending radii and with an increasing amount of bends. The electrical measurements have been carried out after each test, with the device in flat position, and not during the mechanical tests; this is mostly due to the set up employed for the electrical characterization, which does not allow to perform measurements during the tests.
The strain applied to the devices has been calculated according to

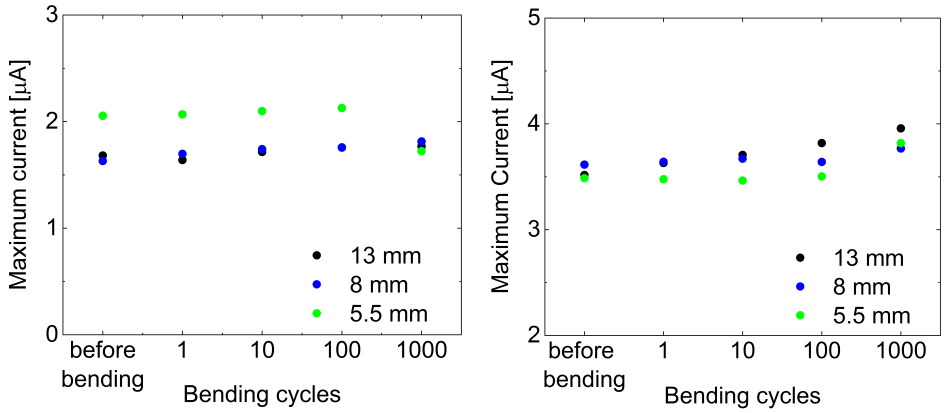
$$strain = \frac{t_{substrate}}{2r_{bending}} \tag{4.2}$$

where $r_{bending}$ is the applied bending radius and $t_{substrate}$ is the thickness of the substrate; the thickness of the device itself is orders of magnitude lower than that of the substrate, so it can be neglected and only the nominal substrate thickness is used in this calculation.
The three bending radii considered for this test are equal to 5.5, 8 and 13 mm, which correspond to applied strains equal to about 1.1%, 0.8% and 0.5% respectively.
For each bending radius, the device transfer curve has been measured before the test and after 1, 10, 100 and 1000 bending cycles. The results, comprising transfer curves, maximum current, mobility values in linear and saturation regimes and the onset voltage, after each step are shown in Figure 4.9. The *p*-type devices show a slight increase in current and mobility, with almost unchanged onset voltage and overall no relevant variation in the performances after up to 1000 bending cycles for all the applied strains. *n*-type OFETs, on the other hand, present no significant variation for all the parameters with strains lower than 1%; considering the highest applied strain, 1.1%, current and mobility values are constant up to 100 bending cycles, with a loss in performances only after 1000 cycles.



(a) Transfer curves for n-type OFETs after up to 1000 bending cycles.

(b) Transfer curves for p-type OFETs after up to 1000 bending cycles.



(c) Maximum drain current measured for n-type OFETs after up to 1000 bending cycles.

(d) Maximum drain current measured for p-type OFETs after up to 1000 bending cycles.

Figure 4.9: Bending tests results. (a), (b) Transfer curves and (c), (d) maximum drain current measured for n- and p-type OFETs before the test and after 1, 10, 100 and 1000 bendings. The maximum current values are presented for all the three bending radii considered; the 13 mm radius gives a strain of about 0.5%, the 8 mm gives about 0.8% while the maximum strain, equal to 1.1%, is given by the 5.5 mm radius. The transfer curve shown refers to the worst case scenario, with an applied strain of 1.1%.

4.6 Complementary circuits

During the development of logic gates, unipolar or complementary configurations can be considered. The first one relies on devices of one single polarity, usually p-type transistors when dealing with organic electronics, while the latter requires the co-existence of p- and n-type OFETs. Complementary circuitry has more strict requirements, including the need to have the two kinds of transistors with matching currents and low threshold voltages, and more complex fabrication procedures, but they allow for the fabrication of more stable circuits with reduced power consumption.[53]

In the previous section, p- and n-type OFETs, manufactured with the

same techniques and on the same substrate, using identical electrodes and dielectric layer, have been presented. The integration of these two devices into complementary logic circuits is the next obvious step toward the development of organic circuits.
In this section, the fabrication and characterization of some complementary devices is presented, starting from the simplest one, the logic inverter, and increasing the level of complexity up to D-Flip-Flop, which is the most complex circuit developed in the framework of this thesis.

4.6.1 Inverter

The simplest integrated circuit developed during this thesis is the logic inverter or NOT gate, a device composed of two OFETs, one for each polarity, which implements the logical negation. In this device, the two transistors share the drain contact and have the same electrode, as shown in Figure 4.10.

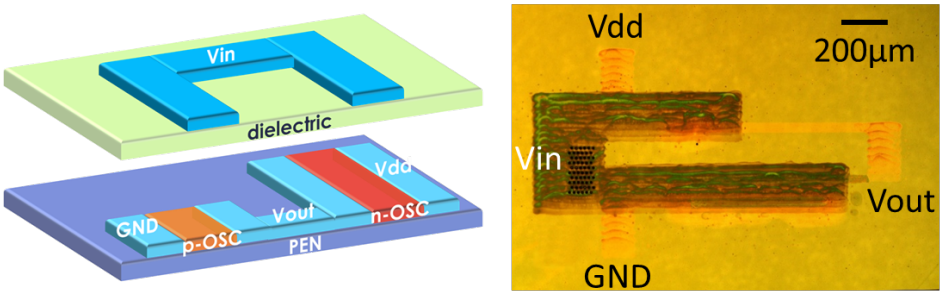
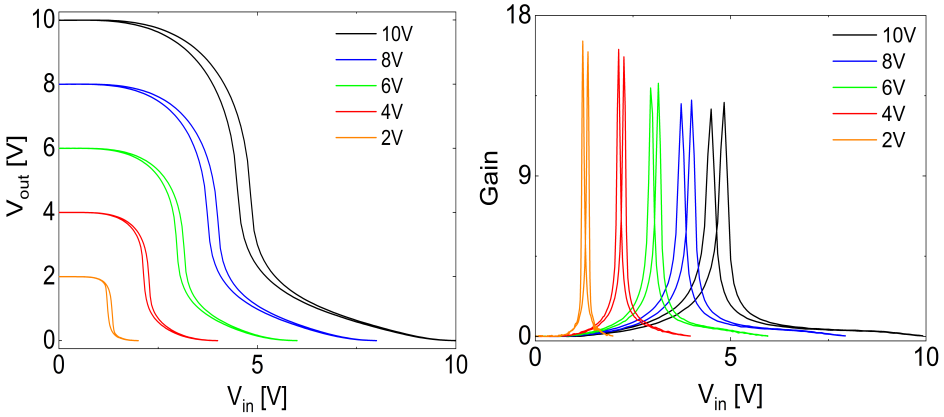


Figure 4.10: Schematic representation (left) and optical micrograph (right) of a printed complementary inverter.

The operation of this device can be explained as follows: when the supply voltage V_{in} is high, the p-type transistor is off, while the n-type is on, so there is a direct path between the ground node and the output electrode, and V_{out} is steadily equal to 0. When V_{in} is low, on the other hand, the p-type OFET is on and the n-type one is off, so the direct path is formed between the electrode where the supply voltage is applied and the output node, so the output voltage is high.[119]
For each applied voltage, the current flowing in the two transistors is equal and the corresponding output voltage value can be found by intersecting the output curves of the n- and p-type transistors. The switching threshold of an inverter is defined as the point where $V_{in} = V_{out}$, and corresponds to a situation where both transistors are in saturation; in order to have a balanced inverter, and an inverting threshold close

to the half of the applied supply voltage ($V_{inv} = V_D/2$), the currents flowing through n- and p-type transistors in saturation regime need to be almost identical.
As it has been shown in the previous section, the performances of the transistors presented in this work are not perfectly balanced, and the p-type OFETs show current values slightly higher than those of the n-type ones. In order to balance the complementary devices and achieve identical current outputs for the two transistors when equal voltages are applied, the channel width of p-type transistors (W_p) has been reduced, compared to that of n-type ones (W_n), to roughly a third. The fabricated devices have $W_p = 300\,\mu m$ and $W_n = 1000\,\mu m$, while the channel length is the same for both kind of devices, $L_p = L_n = 60\,\mu m$. Thanks to this tailoring of the channel geometry, the differences in charge carrier mobilities have been overcome and current levels have been matched.
In order to obtain the static characteristic of an inverter, Voltage-Transfer Characteristic (VTC) have been measured, sweeping the input voltage from a 0 logic state to a 1 logic state;[119] for this characterization, supply voltages (V_D) ranging from 2 to 10 V have been used. The VTC presented in Figure 4.11a are obtained as an average over 5 different printed transistors.



(a) Voltage transfer curves.

(b) Gain curves.

Figure 4.11: Static characterization of printed complementary inverter, with (a) voltage transfer curves and (b) gain curves.

The inverting threshold, mentioned above, has been evaluated finding as the intercept of the VTC with the bisector of the axis. An average inverting threshold of 4.9 V has been obtained for a supply voltage of 10 V, with a standard deviation of 0.05 V. The inverters are still properly functioning with only 2 V applied, and they present a threshold

voltage of 1.19 ± 0.07V.
In Figure 4.11b, the average gain values for the inverters are shown. The gain of an inverter is calculated as the derivative of the VTC, and the maximum value is extracted. The average gain for the devices fabricated in this work is 14, with maximum gain equal to 17, obtained for an applied input voltage of 2 V.
Lastly, noise margins (NM) for these devices have been calculated according to the maximum equal criteria.[120] This parameter gives an useful estimate of the noise immunity of an inverter; for the printed devices presented in this thesis, NM values for all the supply voltages are comprised between 50% and 60% of $V_D/2$, and the best performances have once again been obtained for supply voltage equal to 2 V, which gives an average NM of 0.62.
All the above mentioned figures of merit are close to ideality, and thus these simple electronic devices can be used for further developing printed complementary logic circuits operating at low voltage.[119]

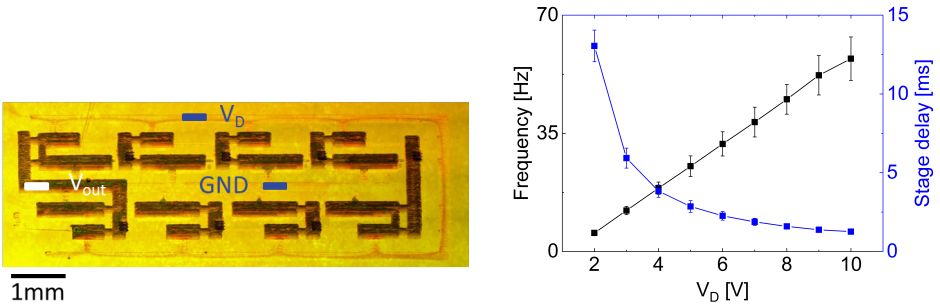
4.6.2 Ring oscillator

The second complementary circuit presented in this thesis is the ring oscillator, which has been used to dynamically characterize the inverters. A ring oscillator (RO) can be described as a chain containing an odd number of inverters, where the output of the preceding inverter acts as the input of the successive one. This device, being composed of an odd number of components, has no stable operation point and oscillates with a frequency of oscillation f_{RO} that depends directly on the time needed by the signal for propagating through the circuit, and is equal to

$$f_{RO} = \frac{1}{2 * N * SD} \tag{4.3}$$

where N is the number of stages and SD is the stage delay. The optical micrograph of a printed 7-stage ring oscillator is shown in Figure 4.12a, while in Figure 4.13 the characteristic oscillating behaviour of these devices is shown, for three different supply voltages. The characterization of the ring oscillators has been performed with increasing supply voltages, from 2 up to 10 V, and the average oscillating frequency and stage delay are presented in Figure 4.12b; these values have been obtained as an average over three different samples.
The oscillating frequency for the RO fabricated in this work is around 6 Hz for a supply voltage of 2 V, and increases up to 57 Hz at 10 V, which leads to average stage delay values equal to 13.1 ms and 1.3 ms with supply voltages of 2 and 10 V respectively. The best performing

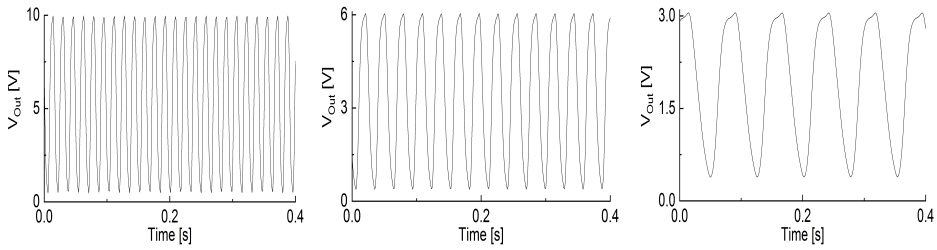
RO has an oscillating frequency equal to 62.5 Hz at 10 V, corresponding to the minimum stage delay recorded for these devices, equal to 1.14 ms.
This is, at the best of our knowledge, the first demonstration of a printed, transparent, all-polymeric ring oscillator operating at low-voltage.[15,121–124]



(a) Optical micrograph of a printed complementary 7-stage ring oscillator.

(b) Average oscillating frequency and stage delay for 3 different devices.

Figure 4.12: (a) Optical micrograph and (b) average oscillation frequency and stage delay as a function of the supply voltage.



(a) $V_D = 10$ V.

(b) $V_D = 6$ V.

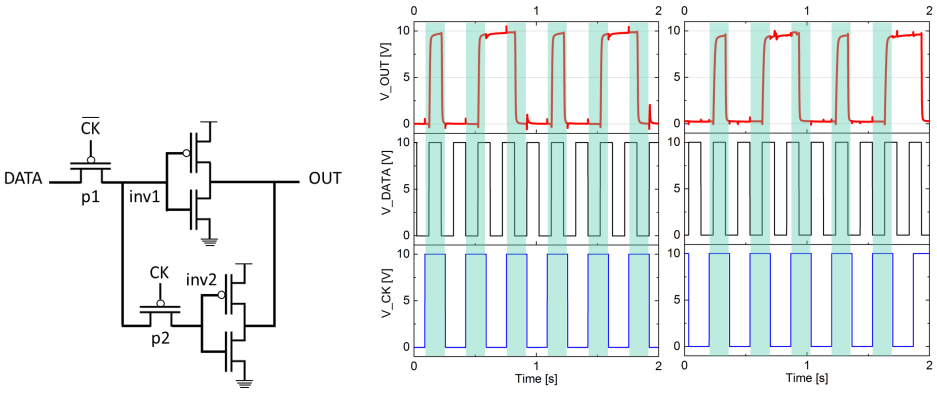
(c) $V_D = 3$ V

Figure 4.13: Oscillating behaviour for different applied voltages of a 7-stage ring oscillator.

4.6.3 D-Latch

Moving further with the fabrication of more complex complementary circuits, a printed D-Latch operating at low voltage has been realized. This device is the basic building block of memory elements, and it is able to store 1 bit of information. In order to implement this device, two main components are needed, the inverter, whose characterization and development have already been addressed in Section 4.6.1, and the transmission gate, a logic port acting as a switch. In standard design, the transmission gate is composed of two transistors with opposite polarity, which share drain and source contacts and have opposite gate

polarity. In this work, a single p-type transistor has been used as transmission gate, aiming at a reduction of the number of transistors per circuit, and because of the lack of gain in adopting a complementary configuration.
A D-Latch contains two inverters and two transmission gates, as shown in Figure 4.14a, and can thus be realized with only 6 transistors. The operation of this device takes place in two main phases, *transparency* and *hold*. During the transparency phase, the clock (CK) is high and the input signal goes through the circuit and reaches the output unaltered. During the hold phase, on the other hand, the clock is low and the device holds a constant output signal, equal to the one received as input at the clock falling edge. More in details, when CK is high (*transparency* phase) and $\overline{CK}$ is low, the transmission gate $TG1$ acts as short circuit and $TG2$ acts as open circuit; in this configuration, the input signal $DATA$ is inverted by both $INV1$ and $INV2$, and thus is transmitted to the output node delayed but unaltered. On the other hand, in the *hold* phase, CK is low and $\overline{CK}$ high, so $TG1$ is an open circuit and $TG2$ a short, and they form a loop; in this case the output corresponds to the input of $INV1$, which is not sensitive to any $DATA$ change in this phase.
In Figure 4.14b, the operation of two D-Latches is shown, for an applied supply voltage of 10 V, and with data and clock frequency equal to 5 and 3 Hz respectively.



(a) Schematic of the printed D-Latch.

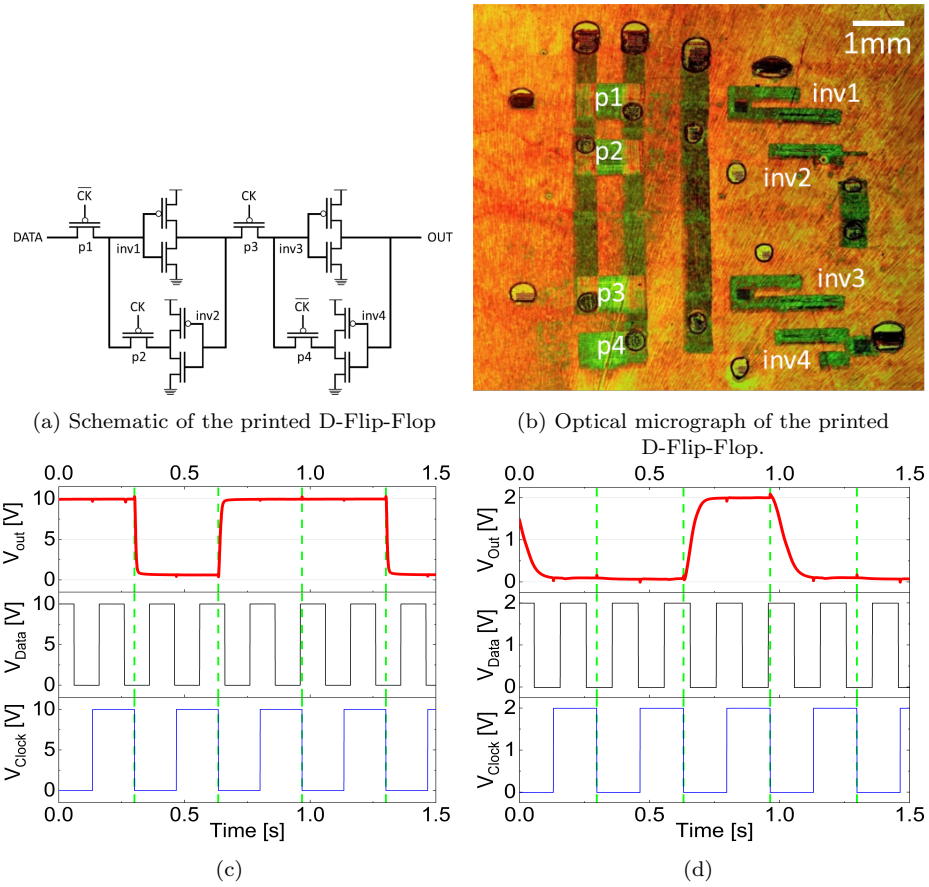
(b) Proper operation of the printed D-Latches.

Figure 4.14: (a) Schematic representation and (b) proper operation of printed D-Latches.

4.6.4 D-Flip-Flop

The last device presented in this chapter is the D-Flip-Flop (DFF), a basic electronic circuit used to store information.[79,125–127] A clocked

system has been designed, such that it ignores the input all the time except for the transition of a clock signal, where it either changes or retains the output signal, based on the input value at that moment. A Master-Slave configuration has been used, in which two D-Latches are connected in series and receive opposite clock signals, so they have opposite transparency phases.[119] In this work, falling-edge triggered devices have been realized, which means that the output value changes only when the clock switches from high to low. In that moment, in fact, the first latch $DL1$ goes from transparency to hold, it samples the input data and stores it in the feedback loop; the second latch $DL2$, on the other hand, goes from hold to transparency phase, and thus makes it possible for the input signal to reach the output node.
The schematic and microscope image of a printed D-Latch are shown in Figure 4.15a and Figure 4.15b; as it can be seen, using a pass-transistor logic, and with the single-transistor transmission gate presented in the previous section, a DFF can be realized using only 12 transistors. The proper operation of these devices is shown in Figure 4.15c and Figure 4.15d, for applied supply voltages of 10 and 2 V.
As a last characterization of these devices, their transparency has been taken into account. The transmittance of the printed circuits has been evaluated using UV-vis spectroscopy in the visible range, and values higher than 90% has been obtained for a printed DFF, as shown in Figure 4.16b. The contribution of the substrate alone has also been measured, and the normalized transmittance for the DFF only amounts to more than 95%.
This is not the first demonstration of a low-voltage DFF that can be found in literature,[128–130] but it represents, to the best of our knowledge, the first low-voltage, all-polymeric, printed, transparent DFF.[16]
The shelf life of these devices, non-encapsulated and stored in an inter nitrogen atmosphere, has been assessed after 4 months; the DFF is still properly operating, thanks to the unaltered characteristics of both transistors and inverters, as shown in Figure 4.17 and 4.18.



(a) Schematic of the printed D-Flip-Flop

(b) Optical micrograph of the printed D-Flip-Flop.

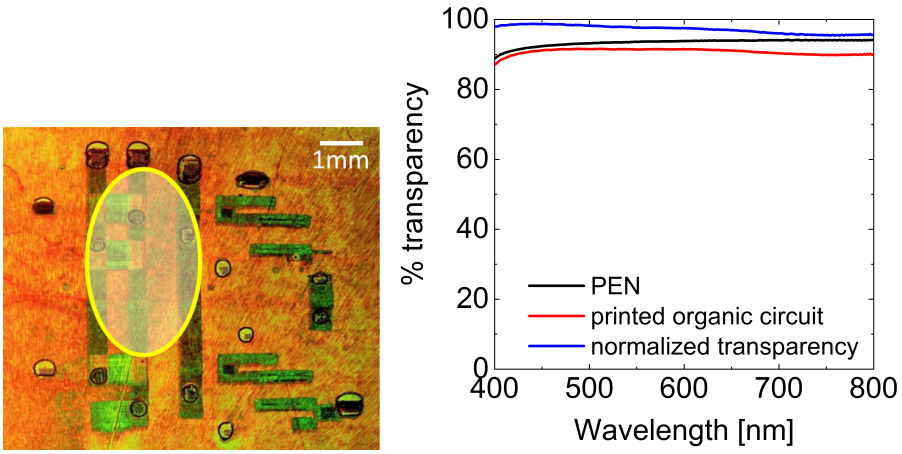
(c)

(d)

Figure 4.15: (a) schematic and (b) optical micrograph of the printed D-Flip-Flop. Proper operation of the printed D-Flip-Flop for supply voltages equal to (c) 10 V and (d) 2 V.

4.7 Summary

In this chapter, the optimization of a parylene-based dielectric bilayer and its integration into top-gate all-polymeric OFETs has been presented. The deposition of all the functional layers, except for the dielectric, has been performed using ink-jet printing onto a PEN substrate. PEDOT:PSS has been used for the source and drain electrodes and the gate pad, while the employed semiconductors are P(NDI2OD-T2) and 29-DPP-TVT, for *n*- and *p*-type transistors respectively. Proper field effect behaviour for voltages as low as 1 V have been reported, with drain currents higher than 1 µA for devices of both polarities when voltages in the order of 10 V are applied. The effective mobility values for these devices have been extracted, and amount to 0.23 and 0.24 $cm^2V^{-1}s^{-1}$ in linear and saturation regimes for *p*-type OFETs, while *n*-type transistors present slightly lower values, equal to 0.07 and



(a) Measurement spot.

(b) UV-vis spectrum of the printed D-Flip-Flop.

Figure 4.16: (a) Schematic of the sample area where the UV-vis spectrum has been recorded and (b) UV-vis spectra. The data presented in the plot refer to the measured device (red), the substrate alone (black) and the normalized curve (blue), giving the contribution of the device itself.

$0.10\,\mathrm{cm^2V^{-1}s^{-1}}$ respectively. These devices have interestingly low subthrehsold slopes, with average values equal to 126 and $148\,\mathrm{mV}dec^{-1}$ for n- and p-type OFETs. The yield of fabrication has been assessed using two 100-transistors arrays, giving great results (99%), and the performances of these devices are highly uniform. The bendability has also tested, and devices are proved to be stable up to at least 1000 bending cycles with an applied strain higher than 1%.
After the successful fabrication of complementary OFETs on the same substrate, with the same fabrication techniques and compatible thermal processes, complementary logic circuits have been developed. First, the simplest complementary circuit has been realized, the complementary inverter, which requires only one p- and one n-type transistor. Well balanced voltage output characteristics have been obtained, with inverting thresholds close to half of the applied voltage interval, noise margins higher or equal to 50% and an average gain value of 14. The dynamic behaviour of the inverters has also been evaluated through the characterization of 7-stage ring oscillators. The proper operation of these devices has been demonstrated for voltages as low as 2 V, where they have an oscillating frequency of 6 Hz and a stage delay equal to 13.1 ms, while the maximum oscillating frequency of 62.5 Hz has been recorded for a supply voltage of 10 V, leading to a stage delay of 1.14 ms. This is the first demonstration of transparent, all-organic, printed ring oscillator operating at low voltage.

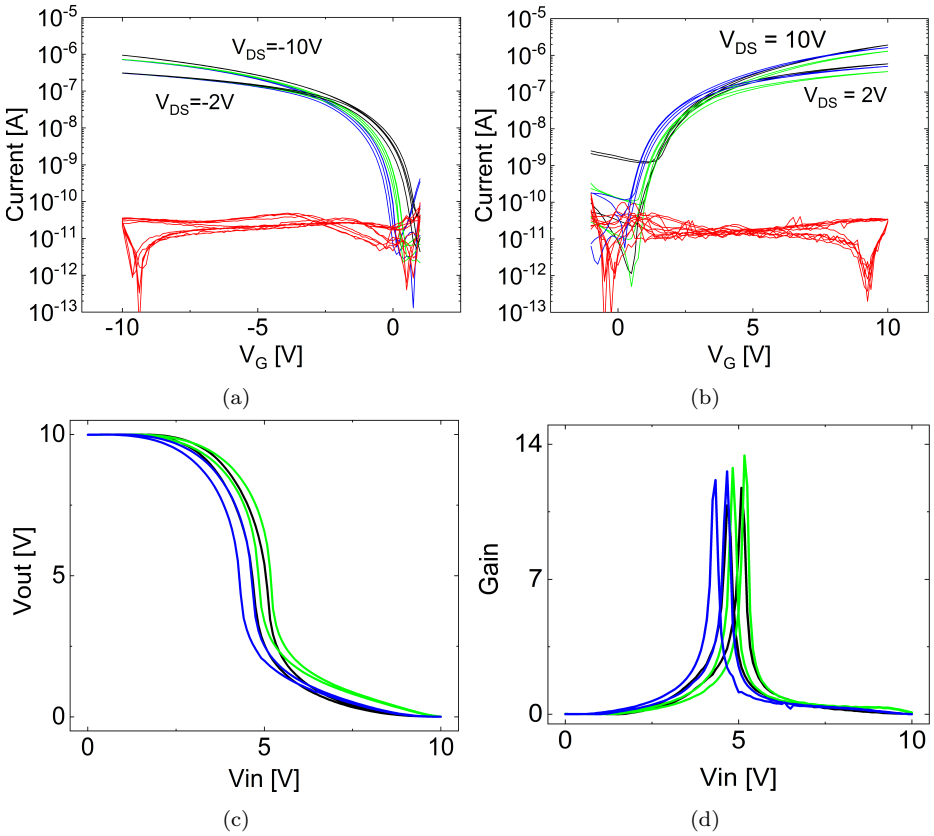


Figure 4.17: Transfer curves for (a) *p*- and (b) *n*-type OFETs, and inverter (c) voltage transfer characteristics and (d) gain values after a shelf life of 4 months. Black lines refer to the performances right after print, green lines have been obtained after 2 months, while blue ones after 4 months.

Lastly, D-Flip-Flop have been implemented in a master-slave configuration, with two D-Latches connected in series and sharing opposite transparency phases. The correct operation of these circuits has been proven for supply voltages as low as 2 V, leading to the first demonstration of all-polymer, transparent, printed D-Latch and D-Flip-Flop operating at low voltage.
The transparency of these devices has been assessed using UV-vis spectrometry, and values higher than 90% have been recorded for the whole device. The devices show proper operation after storing them in nitrogen atmosphere for 4 months, suggesting that a proper encapsulation can lead to a shelf-life stability of months also in ambient air.
The results presented in this chapter show that all-polymeric and transparent OFETs on plastic can be used as building blocks for the development of fundamental electronic components, such as timers and counters, able to operate at voltages that are compatible with energy

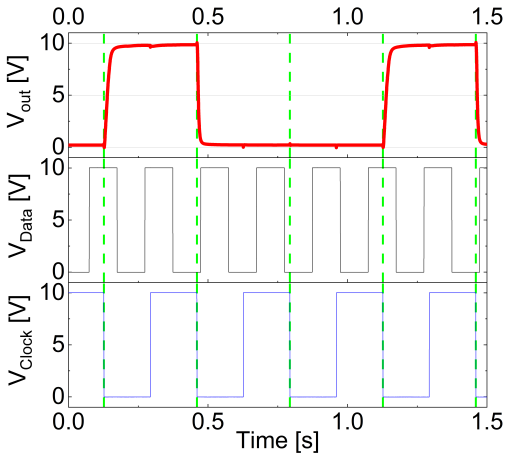


Figure 4.18: Proper D-Flip-Flop operation after 4 months of storage in nitrogen atmosphere.

harvesters and thin film batteries, offering a viable and cost-effective path for the integration of electronic functionalities into consumer products.

5

All-organic and ultraflexible complementary transistors and circuits

"But even if we don't have the power to choose where we come from, we can still choose where we go from there."
– Stephen Chbosky

In this chapter, the fabrication and characterization of transparent and ultraflexible transistors and circuits will be presented. After a brief review of the works present in literature, and of the main strategies employed for the realization of ultraflexible devices, the approach developed during this work is presented. In order to achieve superior mechanical features, an ultrathin parylene layer has been used as a substrate and as encapsulation layer. In the second part of this chapter, the fabrication and characterization of ultraflexible organic transistors and inverters is reported.
The work presented in this chapter is the first demonstration of all-organic, printed, transparent, and ultraflexible complementary organic transistors and circuits.

5.1 Introduction

The field of organic electronics has been receiving more and more attention in the last decades, and this increasing interest is due, among other things, to the possibility granted by these devices to overcome some limitations of silicon-based electronics, such as their mechanical rigidity and optical opacity. Plastic-based devices have in fact some appealing features, being transparent, biocompatible, light-weight, and intrinsically flexible. Furthermore, organic electronic devices can be manufactured with high-throughput, cost-effective and large-area compatible fabrication techniques, making use of solution-processable materials.
These potentialities open the possibility to develop more advanced applications, such as organic electronic circuits able to make real-time sensing on human tissues or any curvilinear object, with improved signal quality thanks to the possibility to place the circuit close to the signal source. In order to do so, the devices should not only be flexible, but they need to grant conformability in 3D. For this reason, the flexibility, light-weight, and conformability of these devices needs to be increased even further, entering the field of imperceptible or epidermal electronics, with devices so light and thin that they do not affect the structure onto which they are applied and create any concern to the wearer.[131–134] In this way it would thus be possible to equip the human body with a variety of devices for information technology, such as human-machine interfaces and augmented reality,[135,136] and for applications such as health monitoring, biological studies, medical treatments and implants.[137–141] Ultraflexible solar cells,[142,143] Organic Light Emitting Diodes (OLEDs),[144–146] displays,[147,148] and memories[80] have been fabricated and presented in literature.
Focusing on microelectronic circuits, most of the flexible devices presented in literature, likewise the OFETs presented in the previous chapter, are able to withstand bending radii in the order of few mm, and suffer bending-induced damages if more demanding mechanical stresses are applied. Ultraflexible electronics requires bending radii orders of magnitude smaller, in order to obtain devices that can be easily conformable onto any surface with arbitrary shape. The molecular structure of the organic semiconductors grants them an intrinsic flexibility, and they can be twisted and crumpled with no relevant degradation. The main limitation of most of the flexible devices mentioned above, which is present also in the OFETs introduced in the first part of this work, is related with the substrate onto which the fabrication occurs. The maximum achievable bending thickness, and so the conformabil-

ity, are proportional to the thickness of the device, and a decrease in substrate thickness helps reducing the stiffness and increasing the flexibility of the device. The bending strain is defined as[149]

$$\epsilon = \frac{h_S}{2R_B} \tag{5.1}$$

where h_S is the thickness of the substrate and R_B is the bending radius. Following this consideration, there has been an effort toward reducing the total thickness of the devices, starting from the substrate; some works presented in literature are thus employing ultraflexible substrates,[90,131–133,142,146,150–153] while few other works rely on substrate-free configurations.[91,154–157]
During bending, one of the surfaces is in tension while the other one is in compression, and there exists a surface inside the layer where no strain is applied; this surface is known as neutral-strain or neutral-plane position.[158] In order to increase the stability of the ultraflexible devices, it is thus important to place the active layer in the neutral-plane position, so to reduce the strain applied and increase the durability of these devices. This is achieved by encapsulating the circuits, with an encapsulating layer that presents thickness and Young modulus according to

$$Y_S d_S^2 = Y_e d_e^2 \tag{5.2}$$

where Y is the Young modulus, d is the thickness, the subscript S refers to the substrate and the subscript e refers to the encapsulation layer. In this work, likewise some of the works in literature,[152] the same material has been used for both substrate and encapsulation, so two layers with identical thicknesses have been employed.
For what concerns the works present in literature, at the best of the author's knowledge, all the organic transistors and circuits have been fabricated making use of metallic electrodes, either in gold or silver, so these devices are not transparent nor fully-organic;[90,104,105,131,132,134,153,159–161] additionally, with some exceptions related to silver-based devices fabricated with ink-jet printing,[133] most of these devices require lithographic and/or vacuum-based processes, which are not scalable, during their manufacturing.
The aim of this part of the thesis was the development of not only ultraflexible and printed, but also transparent and fully-polymeric complementary OFETs and inverters. In order to do so, the same device structure presented in the previous chapter has been integrated onto an ultrathin parylene substrate, and another parylene layer has been used for the encapsulation. In the next sections, first the detailed strategy

employed will be presented, then the performances of printed OFETs and complementary circuits will be presented.

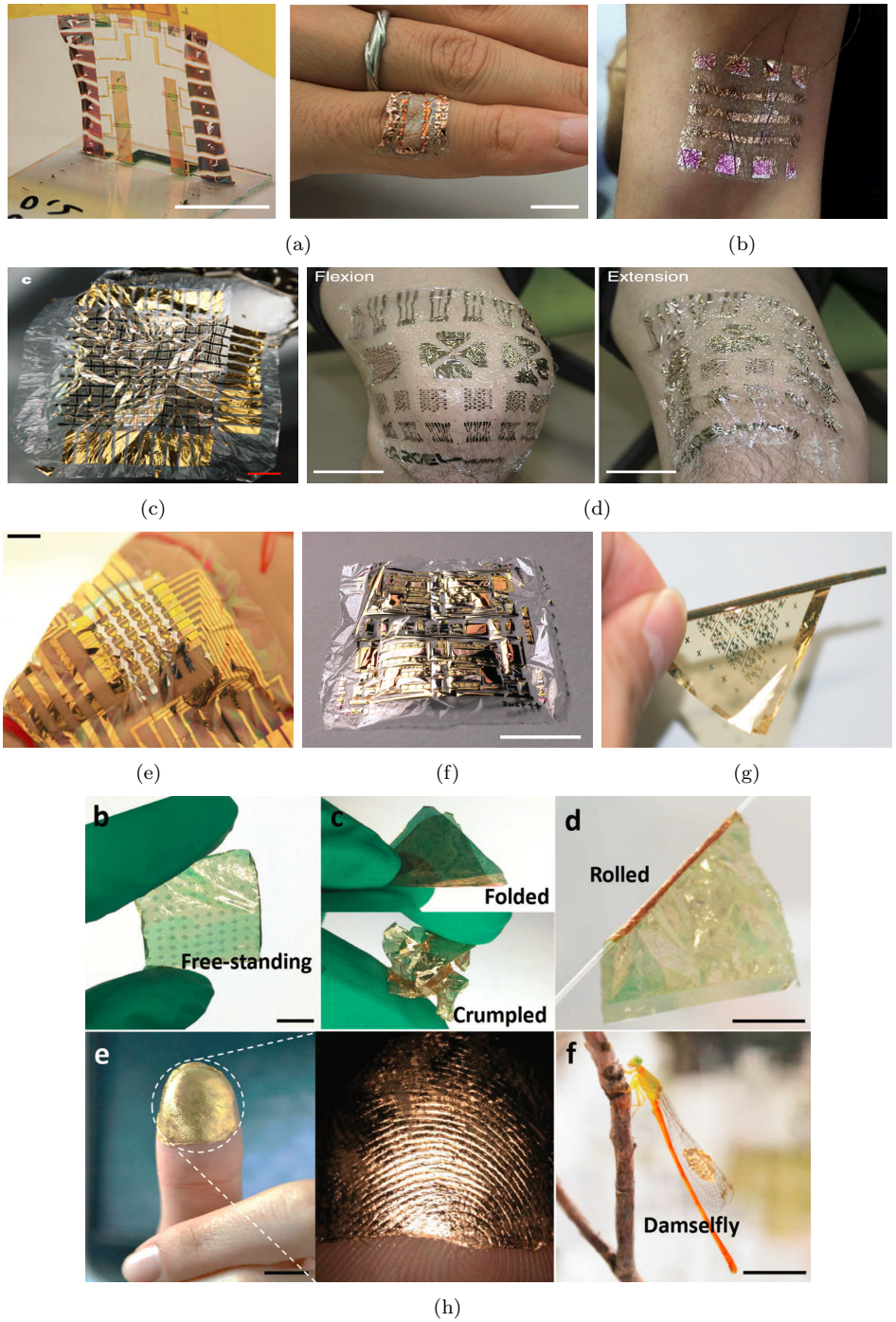
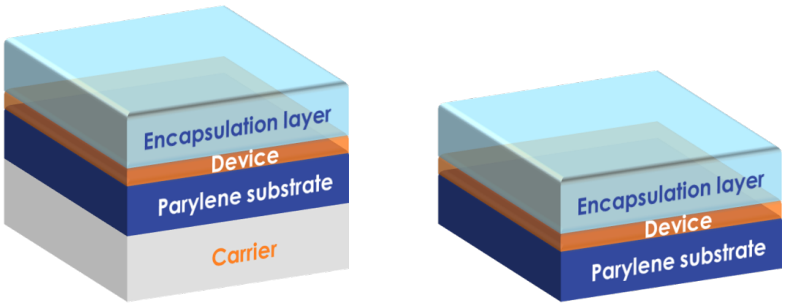


Figure 5.1: Examples of conformal transistors and electronic circuits presented in literature. All these devices clearly employ metallic electrodes, so they are not fully-organic and transparent. Adapted from (a),[105] (b),[160] (c),[132] (d),[133] (e),[159] (f),[161] (g),[131] (h).[134]

5.2 Ultraflexible devices fabrication

As it was mentioned in the previous section, for the devices presented in this chapter parylene has been used as substrate. An ultra-thin film with a thickness of about 2 µm has been deposited by means of CVD onto microscope glass slides. During the fabrication of the electronic circuits, the glass slide has been used as a carrier, in order to facilitate the handling of the parylene film (Figure 5.2a). After the fabrication of the electronic circuits, another thin parylene layer has been deposited on top, playing a dual role: it acts as a passivation layer, forming a barrier between the devices and the environment,[162–164] and it allows to place the active layer in the neutral plane of the stresses. In this way, when a mechanical stress is applied to the system, the strain on the semiconducting layer is the lowest possible, and so the damage brought to the device is limited.



(a) (b)

Figure 5.2: Schematic of the final device structure, (a) before and (b) after the detachment from the glass slide carrier.

For what concerns the fabrication of the actual OFETs and complementary inverters, the same procedure presented in the previous chapter has been adopted, and the same materials, with just one exception, have been employed for the realization of all-polymeric circuitry. The printed devices have PEDOT:PSS conductive electrodes and the PMMA-parylene bilayer as dielectric film, P(NDI2OD-T2) is the *n*-type semiconductor, as for the devices on PEN, and the PEI injection layer has been integrated also in these OFETs to improve their injection and overall performances. The only difference with respect to the devices presented in the previous chapter relies in the *p*-type semiconductor; for this second part of the work a different DPP derivative has been used, namely DPPT-TT, whose structure is shown in Figure 3.5, and it has been blended with polystyrene. The use of multicomponent systems is an approach that has been developed in order to expand even further

the features and functionalities of organic electronics. In particular, blending semiconducting polymers with insulating counterparts helps improving their mechanical characteristics, making them more flexible and stable, it widens the range of viscosities that can be reached, expanding the count of available fabrication techniques, and increases the environmental stability with respect to the neat semiconductor thanks to a partial self-encapsulation.[165] In the framework of this thesis, the DPPT-TT has been blended with PS with a ratio of 1 : 1, mostly to improve the mechanical stability of these devices, and achieve better performances during ultraflexible operations, and to have a final solution viscosity that is more easily ink-jet printed, both in terms of ease of droplet jetting and for what concerns the thickness and quality of the printed pad.
The devices have been fabricated on parylene and characterized, in order to check their correct operation before proceeding with the following steps. Properly working circuits have been encapsulated with parylene and, after the deposition of the encapsulation layer, the last fabrication step has been performed, namely the drilling of holes, and the subsequent printing of PEDOT:PSS pads, in correspondence of the points where electrical connections are made during the characterization; in this way, proper electrical characterization of the encapsulated circuits can be carried out. Once the devices are properly encapsulated and external electrical connections can be created, the detachment is performed. First, with the help of a scalpel, the edges of the printed pattern are cut, and the shape of the final ultra-flexible system is defined; then, with the help of tweezers, the system is detached from the glass slide, and the self-standing device is ready to be characterized, both electrically and mechanically (Figure 5.2b).
In Figure 5.3, the photos of the final device, both during the detachment and applied on skin, are presented.

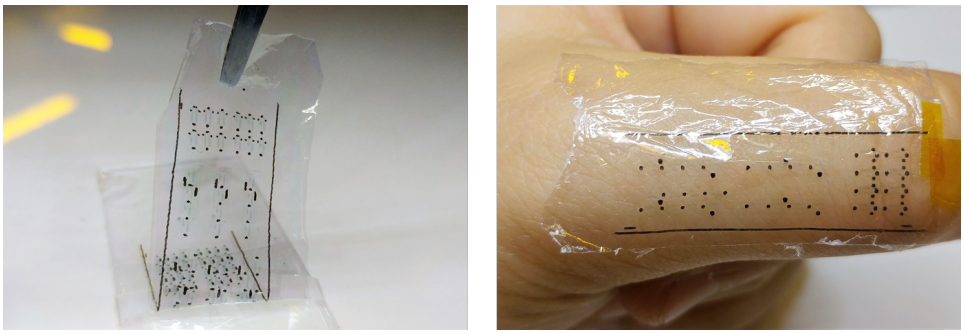


Figure 5.3: Photos of the free-standing devices during the detachment from the glass slide (left) and same device applied on skin (right).

During the development of this work, two main mechanical tests have been performed. First, the devices have been rolled onto a very thin plastic cylinder with a diameter of about 1 mm, and then crumpling has been carried out. In both cases, the devices have been measured after the mechanical stress, in flat configuration, and no measurement has been performed during the tests, for the reason presented in the previous chapter. In Figure 5.4, the devices during both tests are shown.

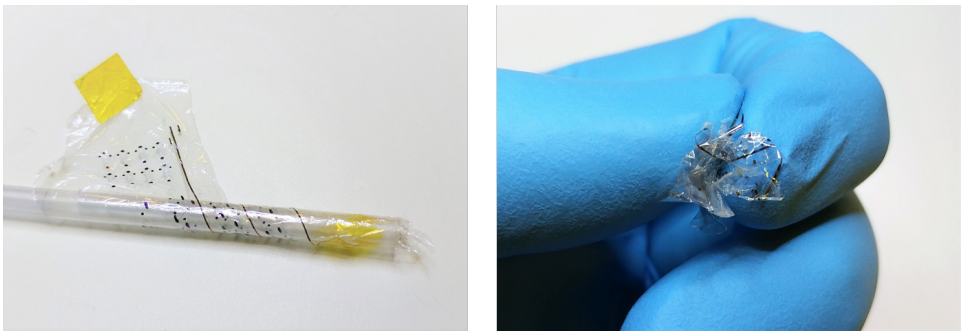
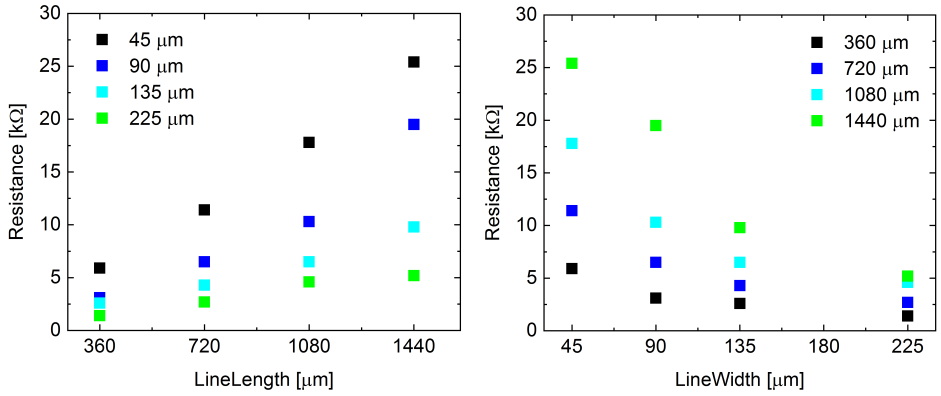


Figure 5.4: Photos of the free-standing devices during the mechanical tests performed in this work, rolling (left) and crumpling (right).

5.3 OFETs ELECTRICAL AND MECHANICAL CHARACTERIZATION

For the fabrication of all the devices presented in this chapter, both OFETs and circuits, the same steps presented in Section 4.4 have been followed. The so-obtained devices are thus fully organic, and all the layers except for the dielectric one are ink-jet printed.
Before fabricating complete electronic devices, the possibility to print PEDOT:PSS onto parylene substrates has been tested. Lines with different lengths and widths have been ink-jet printed, I-V characteristics have been measured and the corresponding resistance values have been extracted as the slope of the current-voltage characteristics. In Figure 5.5, the measured resistance values are shown, as a function of both the length and the width of these lines.



(a) PEDOT:PSS lines resistance, as a function of line lengths.

(b) PEDOT:PSS lines resistance, as a function of line widths.

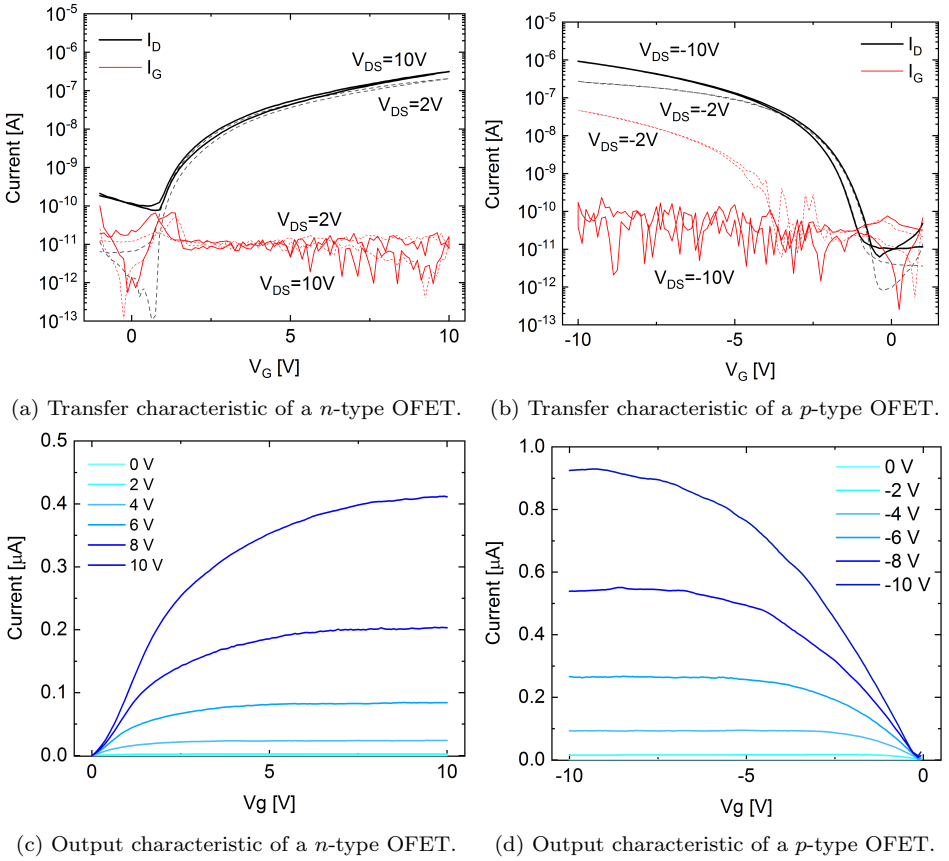
Figure 5.5: Resistance values of the printed PEDOT:PSS lines, represented as a function of both (a) the length and (b) the width of the lines.

The printed lines present four different lengths, nominally equal to 360, 720, 1080 and 1440 µm, and four widths nominally equal to 45, 90, 135 and 225 µm, while for what concerns the thickness, an average value equal to 40 nm has been considered for all the lines. The average resistivity has been evaluated according to the following equation

$$R = \frac{\rho L}{A} \iff \rho = \frac{RA}{L} \tag{5.3}$$

and is equal to $(3.41 \pm 0.45) * 10^{-5} \Omega\,\mathrm{m}$. This value is very close to that obtained for PEDOT:PSS lines printed on standard substrates such as PEN; it is thus possible to conclude that parylene substrate is compatible with this conductive material and PEDOT:PSS can be used for

the fabrication of OFETs and electronic circuits.
After this analysis, OFETs have been fabricated and the electrical characterization of both *n*- and *p*-type OFETs has been performed; the results are shown in Figure 5.6, where both transfer and output curves for both types of devices are presented.



(a) Transfer characteristic of a *n*-type OFET.

(b) Transfer characteristic of a *p*-type OFET.

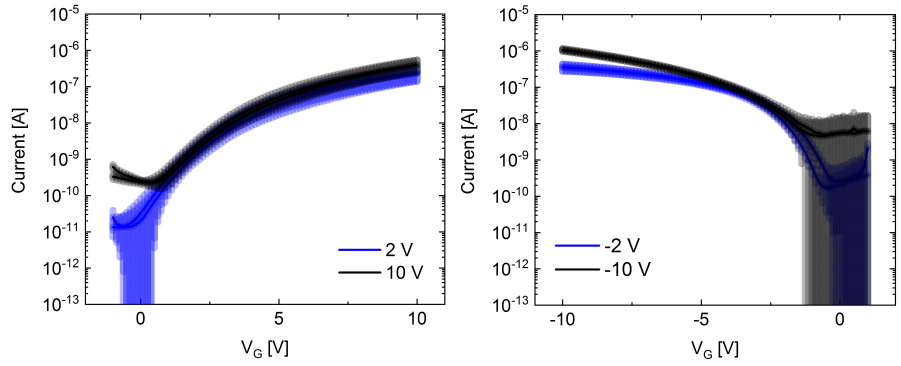
(c) Output characteristic of a *n*-type OFET.

(d) Output characteristic of a *p*-type OFET.

Figure 5.6: Electrical characteristics of printed *n*- and *p*-type OFETs.

These devices show low-voltage operation, with proper field-effect modulation for voltages as low as 2 V. For what concerns *p*-type devices, both output and transfer characteristics are almost ideal, while *n*-type OFETs present some non-idealities related to the injection of charges from the contacts, and they can be highlighted both in the subthreshold region of the transfer curve and the S-shape characteristic of the output one. Despite these small faults, both types of transistors can be described as properly working.
The uniformity of performances has been addressed, and ten OFETs of each polarity have been characterized before the detachment; in Figure 5.7, the average transfer curves with relative standard deviation

are shown.



(a) Average transfer curve for n-type OFETs.

(b) Average transfer curve for p-type OFETs.

Figure 5.7: Average transfer curves for complementary OFETs, plotted with their standard deviation.

The performances of these devices have been evaluated, and the main transistors parameters have been extracted. The average maximum drain current is equal to 0.46 ± 0.18 µA for n-type OFETs and 1.07 ± 0.09 µA for p-type ones. The average mobility values, extracted both in linear and saturation regimes, for devices of both polarities, are reported in Table 5.1.

Table 5.1: Average mobility values for p- and n-type OFETs on parylene substrate, after the encapsulation and before the detachment from the carrier, in linear (±2 V) and saturation regimes (±10 V).

	Linear regime ($V_{DS} = \pm 2V$)	Saturation regime ($V_{DS} = \pm 10V$)
p-type OFETs	0.09	0.11
n-type OFETs	0.10	0.09

The n-type mobility values are essentially identical to those of the transistors fabricated on PEN, while p-type mobilities are roughly half of the values reported for transistors of the same polarity in the previous chapter, and this can be ascribed to the change of semiconducting polymer employed, and to the blending with the insulating component. The maximum drain currents for the devices presented in this chapter are slightly lower than their above mentioned counterparts, and this is due to the employment of a thicker parylene dielectric film, which reduces the achievable current values for identical applied voltages.
The subthreshold swing of n-type OFETs is higher than that reported for on PEN devices, and the on-off ratio is reduced, a both these effects

can be correlated with the performances of the PEI injection layer. In particular, the PEI solution shows some self-aligning effects when applied on PEDOT:PSS contacts on PEN substrates, adhering mostly on the source and drain electrodes and leaving the channel clean, and this is most probably due to the different wettabilities presented by the injection layer solution on these two materials. The same does not happen when PEDOT:PSS electrodes are printed on parylene, and the solution equally spreads on the contacts and on the substrate; this leads to a slight reduction of the injection efficiency, reflected in the poorer subthreshold behaviour, and to increased off currents, which worsen the on-off ratio. *p*-type transistors, on the other hand, have basically unchanged on-off ratios and only slightly worse subthreshold swings, so the change in substrate is not harming them much from this point of view.
Overall, the performances of these devices are close enough to the ones of the printed transistors on standard plastic substrates such as PEN, and they can be used in order to continue toward the realization of conformable, printed, all-organic and transparent organic transistors operating at low voltage.
The OFETs have been detached from the carrier and underwent the two mechanical characterization steps mentioned above; the same extraction of the transistors' parameters has been performed after each step, and the average transfer curves are shown in Figure 5.8, while the main transistors parameters are presented in Table 5.2 for *n*-type OFETs and in Table 5.3 for *p*-type devices. A comparison between the average transfer curves of the four different steps considered is presented in Figure 5.9, for devices of both polarities, in linear and saturation regimes, while a graphical comparison of the mobility values, for both types of devices and in both regimes, is shown in Figure 5.10. There is only a slight decrease in mobility given by any of the mechanical stresses applied to *n*-type OFETs, and the same trend can be seen in the average maximum drain current, but overall the performances are satisfying. Same consideration can be done for the *p*-type transistors, which show the highest mobility for the encapsulated devices, and slightly lower values in the other cases.
Focusing on the subthreshold swing and the on-off ratio, for devices of both polarities it can be seen how there are no significant variations between the reported values, so the mechanical tests are not harming the organic transistors in a relevant way, and the *p*-type OFETs are slightly more performing the *n*-type ones, but overall both transistors show more than satisfying characteristics.
In order to explain this slight reduction of the mobility and the drain

Table 5.2: Average mobility values, in linear (2 V) and saturation regimes (10 V) for the *n*-type OFETs printed on an ultraflexible parylene substrate, together with their average maximum drain current, subthreshold swing and on-off ratio, evaluated for the devices after encapsulation, after detachment from the glass slide carrier and after the two mechanical tests, rolling and crumpling.

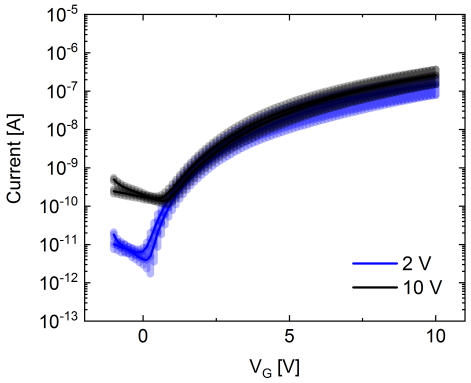
	Encapsulated	Detached	Rolled	Crumpled
Linear mobility $[cm^2V^{-1}s^{-1}]$	0.10	0.06	0.08	0.05
Saturation mobility $[cm^2V^{-1}s^{-1}]$	0.09	0.05	0.07	0.03
Maximum drain current [µA]	0.46 ± 0.18	0.26 ± 0.11	0.55 ± 0.37	0.19 ± 0.05
Subthreshold swing $[mVdec^{-1}]$	732 ± 186	658 ± 89	813 ± 266	535 ± 59
On-off ratio	$9 * 10^4$	$8 * 10^4$	$1 * 10^5$	$6 * 10^4$

current, the pivotal role of the semiconductor-dielectric interface for the proper operation of the OFETs needs to be taken into account. The application of strain to the devices leads to surface rearrangements, with modifications of the polymer structure and changes in the surface heterogeneity and energy, which in turn alter the interface between the two layers and thus modify the device behaviour. In general, polymeric dielectrics that allow for a larger degree of reorganization lead to lower heterogeneity when strains are applied, and thus more robust mechanical performances. Focusing on the dielectric constant, low-k dielectrics are generally better than high-k ones, since they present less dipoles at the interface and consequently less surface rearrangements which might disrupt the semiconductor behaviour.
In this work, low-k dielectrics have been employed, so the contribution of the surface dipoles rearrangement toward the loss in performances is limited. All the materials used for the fabrication of the OFETs are flexible, but they present quite different Young moduli, and this mismatch might lead to modifications of the quality of all the interfaces, between the electrode and the semiconductor and between the semiconductor and the dielectric layer, which in turn disrupt the proper operation of the device and cause the slight loss in performances re-

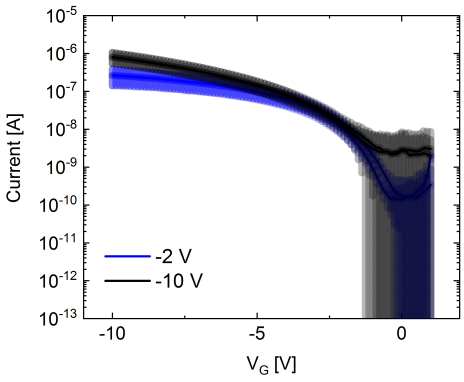
Table 5.3: Average mobility values, in linear ($-2\,\mathrm{V}$) and saturation regimes ($-10\,\mathrm{V}$) for the *p*-type OFETs printed on an ultraflexible parylene substrate, together with their average maximum drain current, subthreshold swing and on-off ratio, evaluated for the devices after encapsulation, after detachment from the glass slide carrier and after the two mechanical tests, rolling and crumpling.

	Encapsulated	Detached	Rolled	Crumpled
Linear mobility $[\mathrm{cm^2V^{-1}s^{-1}}]$	0.09	0.06	0.04	0.06
Saturation mobility $[\mathrm{cm^2V^{-1}s^{-1}}]$	0.11	0.08	0.05	0.07
Maximum drain current [µA]	1.07 ± 0.09	0.80 ± 0.26	0.52 ± 0.19	0.67 ± 0.21
Subthreshold swing $[\mathrm{mV}dec^{-1}]$	439 ± 213	360 ± 246	269 ± 76	166 ± 26
On-off ratio	$2 * 10^6$	$6 * 10^5$	$2 * 10^5$	$4 * 10^5$

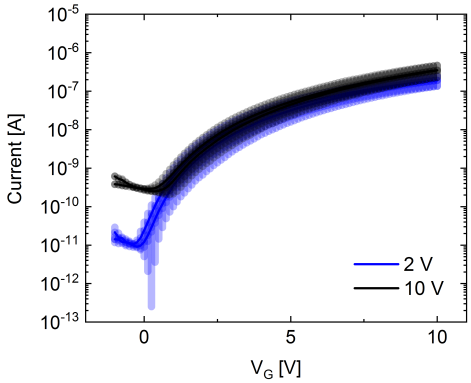
ported above.
At the end of this analysis, two main conclusions can be drawn. First, the performances of these OFETs are pretty uniform, both after the fabrication and after each mechanical test that has been performed. Second, more importantly, the loss in performances after each step is limited, and the performances of these transistors are still satisfactory even after harsh mechanical stresses such as crumpling. This is, at the best of the author's knowledge, the first demonstration of ultra-flexible, fully-organic, printed and transparent complementary OFETs operating at low-voltage.



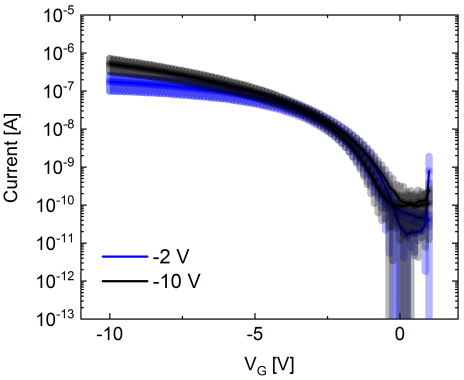
(a) Average transfer curve for n-type OFETs after detachment.



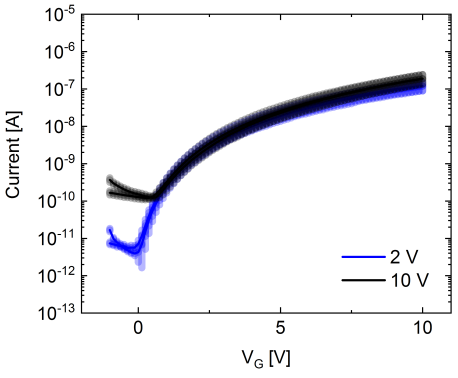
(b) Average transfer curve for p-type OFETs after detachment.



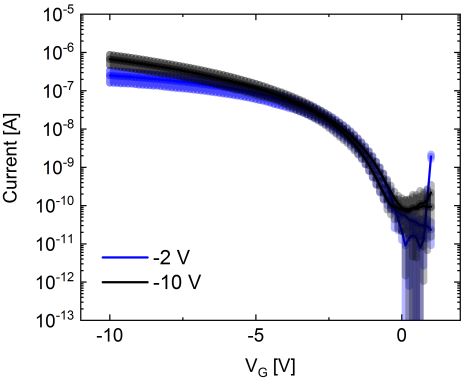
(c) Average transfer curve for n-type OFETs after rolling.



(d) Average transfer curve for p-type OFETs after rolling.

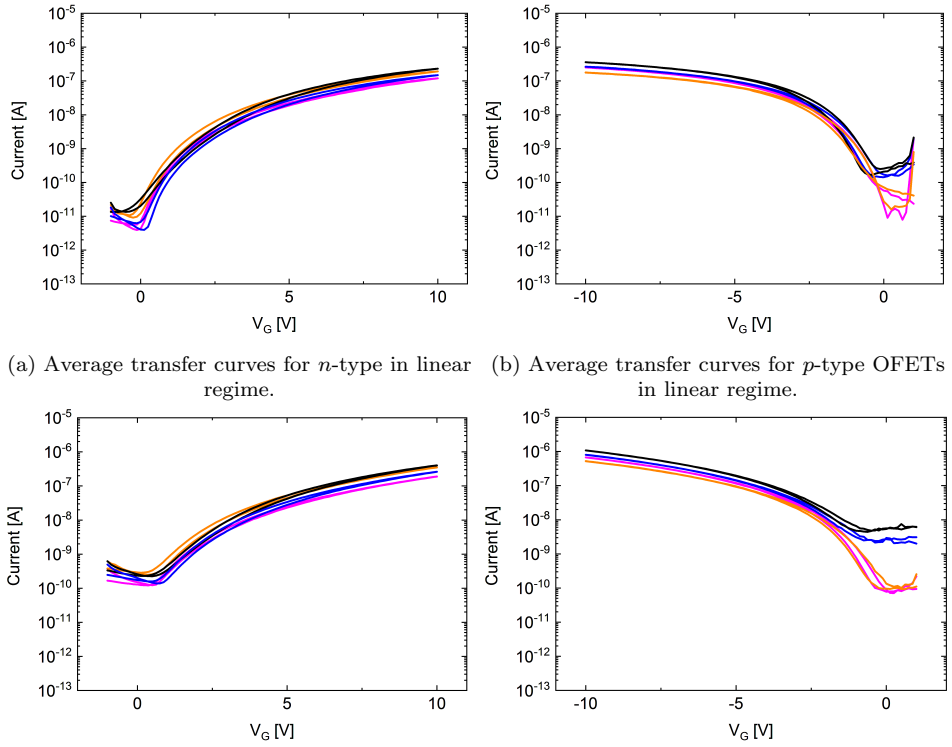


(e) Average transfer curve for n-type OFETs after crumpling.



(f) Average transfer curve for p-type OFETs after rolling.

Figure 5.8: Average transfer curves for n- and p-type OFETs,with standard deviations, measured after detachment from the glass slide carrier and after the two mechanical tests, rolling and crumpling, with their standard deviation.



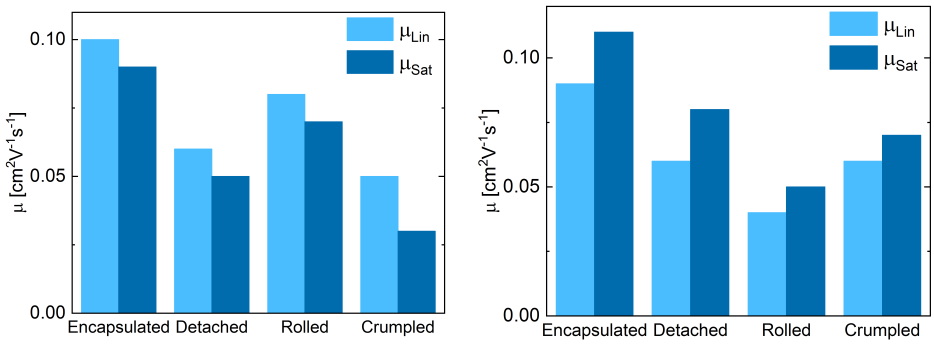
(a) Average transfer curves for n-type in linear regime.

(b) Average transfer curves for p-type OFETs in linear regime.

(c) Average transfer curves for n-type in saturation regime.

(d) Average transfer curves for p-type in saturation regime.

Figure 5.9: Comparison of the average transfer curves for n- and p-type OFETs, in linear and saturation regimes, for the encapsulated devices (black curve), after detachment (blue curve), after rolling (orange curve) and after crumpling (pink curve).



(a) Average mobilities, n-type devices.

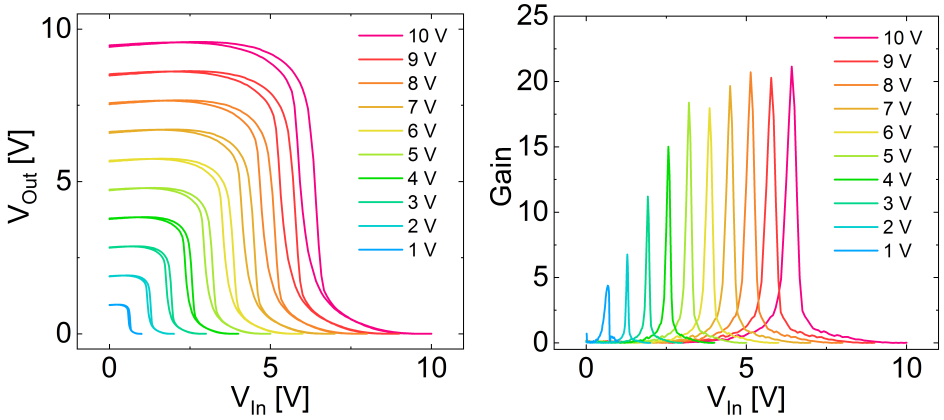
(b) Average mobilities, p-type devices.

Figure 5.10: Bar chart showing the comparison between the average mobility values after each characterization step, in linear and saturation regimes, for (a) n- and (b) p-type OFETs.

5.4 Ultraflexible complementary circuits

Following the same train of thoughts that lead to the development of the devices presented in the previous chapter, once complementary

OFETs, with comparable performances and fabricated with identical techniques on the same substrate, have been obtained, the next step in the development of this technology was the realization of low-voltage complementary circuits. The first considered device is the inverter, implementation of the logical negation, which has been fabricated with the same structure presented in Section 4.6.1. Differently from the devices printed on PEN, the mobility of the two types of transistors here are pretty balanced, leading to similar values of drain current recorded for the same voltage applied; for this reason, the two transistors forming the inverter have been designed with identical channel lengths and widths, equal to $L_p = L_n = 65\,\mu m$ and $W_p = W_n = 1000\,\mu m$. The balancing between the currents of the complementary transistors is not perfect, and the performance variability in this cases is slightly higher than what has been observed in the previous chapter, which leads to a not always perfectly centred inverting threshold for the ultraflexible inverters, as it will be shown in this section, but the overall performances are satisfying enough.
The voltage transfer curve (VTC) for these devices has been measured, and the gain has been extracted as the first derivative of the VTC with respect to the applied voltage; the obtained results, measured before the detachment from the glass slide, is shown in Figure 5.11.

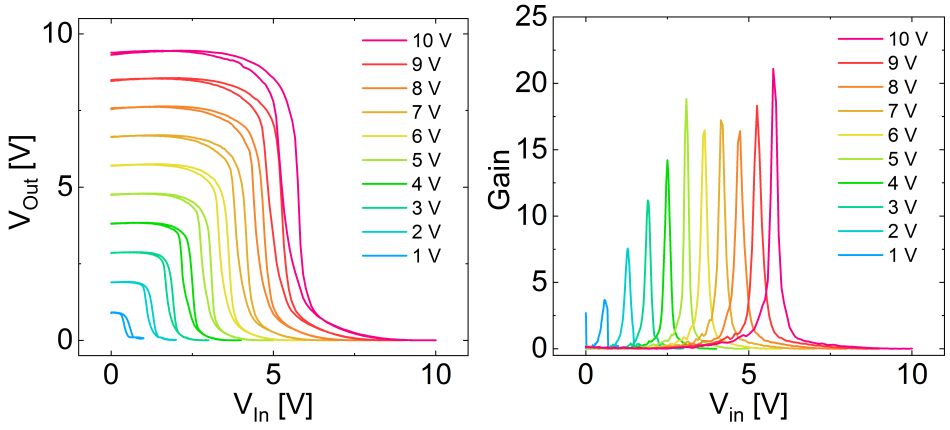


(a) Voltage transfer curves, encapsulated device.

(b) Gain curves, encapsulated device.

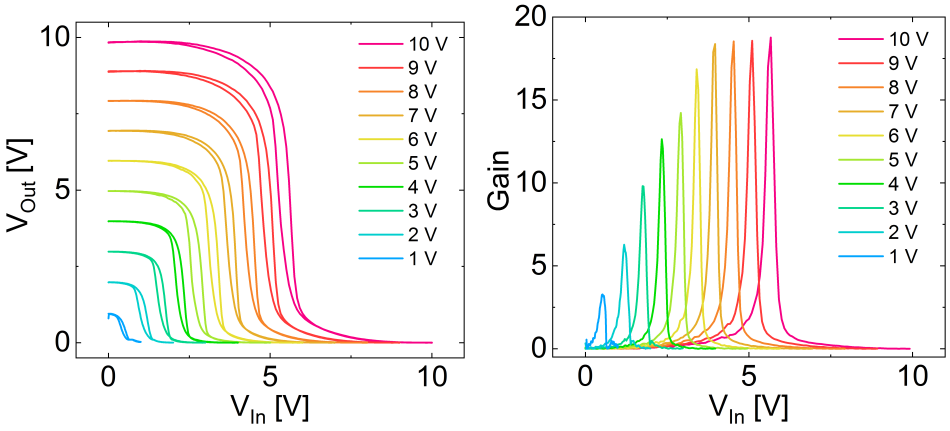
Figure 5.11: (a) Voltage transfer curves and (b) gain curves for a printed complementary inverter, encapsulated but still on the glass slide carrier.

The same analysis has been performed after the detachment and after both mechanical tests and the results are presented in Figure 5.12. Both VTC and gain curves are presented separately and not with other curves as comparison for the sake of clarity.
As it can be seen from the plots in Figure 5.12, the devices are properly



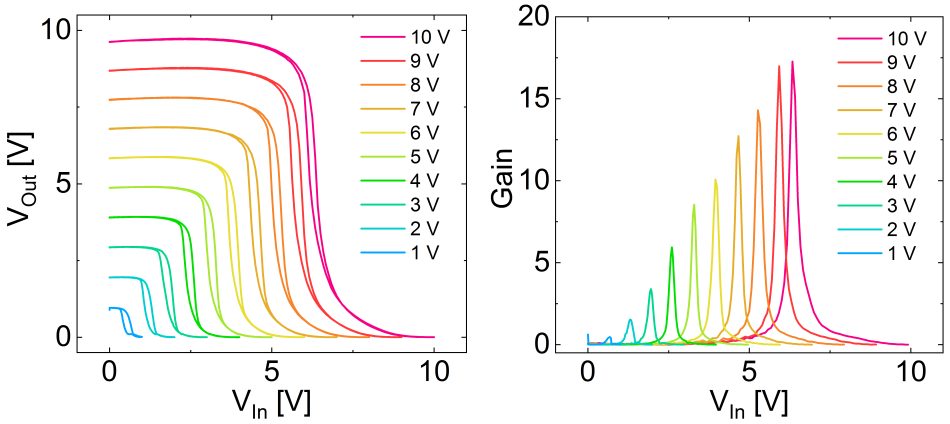
(a) Voltage transfer curves, after detachment.

(b) Gain curves, after detachment.



(c) Voltage transfer curves, after rolling.

(d) Gain curves, after rolling.



(e) Voltage transfer curves, after crumpling.

(f) Gain curves, after crumpling.

Figure 5.12: Voltage transfer curves and gain curves for printed inverters, measured after the detachment from the glass slide carrier and after the mechanical tests, rolling and crumpling.

working even after harsh mechanical stresses such as crumpling. In all the cases, the inverters present proper inverting behaviour and a small hysteresis, while for what concerns the inverting threshold, all the devices switch at a voltage which is relatively close to the middle of the voltage applied, with an average deviation from $V_{DD}/2$ which is below 20% for all the presented results, even the crumpled ones. Differently from the devices on PEN, and as reported in the previous section, here the *p*-type OFETs have slightly higher currents compare to the *n*-type ones, so the switching threshold is slightly shifted toward voltages higher than $V_{DD}/2$, but the deviation is limited and does not harm the proper operation of these circuits.
There is a bit of deterioration for what concerns the gain performances when mechanical tests are performed; in fact, after detachment these devices present gain values higher than 10 for supply voltages as low as 3 V, while these values needs to be increased up to 4 and 6 V if rolling or crumpling are performed, respectively. These voltage values, despite being not as ideal as the previous case, are still very low and thus compatible with plastic solar cells and thin film batteries, so these devices are still showing proper operation even at low voltages.
The results presented in this section represent, to the best of author's knowledge, the first demonstration of ultra-flexible, transparent, all-organic, printed OFETs and complementary inverters able to withstand harsh mechanical stresses such as rolling and crumpling.

5.5 Summary

In this chapter, a strategy for the development of transparent ultraflexible electronic devices has been presented. Differently from all the works presented in literature until now, only organic materials have been used for the fabrication of the OFETs and circuits, relying on ink-jet printing as the main manufacturing technique. PEDOT:PSS has been used for the realization of the electrodes, while the semiconducting materials employed are P(NDI2OD-T2) and DPPT-TT, for n- and p-type transistors respectively, and the dielectric film is constituted by the dielectric bilayer presented in the previous chapter.
In order to realize conformable devices, two main aspects need to be taken into account. The strain applied on the active device during any mechanical stress is proportional to the thickness of the device, so a reduction of the substrate thickness is beneficial; additionally, placing the active layer in the neutral-plane position helps reducing even further the strain on the device, improving its mechanical stability. Taking into account these requirements, an ultrathin parylene film, 2 µm thick, has been used as substrate, and the devices have been encapsulated with an equally thick parylene film, thus placing the semiconductor layer of the transistors and circuits as close as possible to the neutral-strain position. The fabrication of the devices has been carried out using a glass slide as carrier, and the characterization has been performed both before and after the detachment from the microscope slide. No relevant variation in the performances of the OFETs have been recorded, with the n-type OFETs showing mobility values almost identical to the ones reported for on PEN devices and the p-type ones with only a slight worsening of the performances.
Two main mechanical tests have been performed in order to assess the ultraflexibility, namely rolling and crumpling. OFETs have been rolled onto a thin plastic cylinder and/or crumpled, then brought back to the flat configuration and characterized. Both these mechanical stresses lead to a slight loss in maximum recorded currents, and thus mobilities, for devices of both polarities, but overall the printed transistors retain more than acceptable performances, and can be employed further for the development of more complex ultraflexible circuitry.
Following the same reasoning presented for the devices on PEN substrate, after the realization of complementary organic transistors, onto the same substrate and with the same manufacturing techniques, complementary circuits have been fabricated, namely a complementary inverter. The same characterization presented for the OFETs has been carried out, and similar results have been reported. The detachment

from the carrier does not have relevant impact on the performances of the inverter, nor do the mechanical tests chosen for this work. The inverting threshold for these devices is close to $V_{DD}/2$, with an average deviation from the middle of the supply voltage lower than 20% for all the cases, and the gain value reported for the ultraflexible inverters is higher than 10 for V_{DD} as low as 3 V after detachment, while it increases to 4 and 6 V after rolling and crumpling, respectively. All these parameters show that the printed, all-organic and ultraflexible inverters are properly operating and can be used for further development of conformable organic circuitry.
The complementary organic transistors and circuits introduced in this chapter represent the first demonstration of all-polymeric, transparent, printed and ultraflexible devices operating at low voltage. Further work is still needed, aiming at the realization of more complex circuitry to be effectively used in consumer products, but this is a demonstration of the feasibility of this fabrication technique for the development of mass-produced, cost-effective, lightweight and conformable electronic devices for epidermal and imperceptible electronics applications.

6

Ultraflexible organic transistors on biodegradable substrate

"Keep on sowing your seed, for you never know which will grow – perhaps it all will."
– Ecclesiastes 11:6 (TLB)

In this chapter, the fabrication of printed organic transistors on a biodegradable substrate is presented. In the first part of the chapter, the concept of biodegradability is defined, together with the properties and main limitations of the tests used to assess the actual degradability of a material. After this brief introduction, a review of the materials used for the development of (bio)degradable organic electronics is presented. Lastly, the fabrication of all-organic printed transistors is presented, together with their electrical and mechanical characterization. The effect of the non-degradable organic transistors on the biodegradation rate of the substrate has been also assessed.
The work presented in this chapter represents the first step toward the realization of printed and all-polymeric biodegradable organic devices.

6.1 Introduction

One of the peculiar elements of the last decades, without which everyday lives of most people would be unthinkable, is plastic. Its presence has been massively growing, and so has the littering of plastics, leading to increasing environmental concerns. In fact, 250 million tons of commodity plastic are produced annually,[166] and most of these polymers are highly persisting and last for a long time; this is clearly an advantage for some applications, but becomes a major drawback when these materials are not properly disposed, since they accumulate in the environment for decades.[167,168] This plastic is then fragmented into smaller pieces, and might migrate toward the oceans, reaching the so-called "garbage patches".[169]
In order to address this issue, together with proper recycling procedures, the European Union and all the major institutions have promoted in recent years the adoption of biodegradable polymers, considering both the opportunities and the risks related to this class of materials. Biodegradable materials are already used nowadays in applications such as nanomedicine and tissue engineering,[170] and are a definitely promising alternative to most non-degradable commodity polymers.
Different definitions of biodegradability have been presented. According to the International Union of Pure and Applied Chemistry (IUPAC), biodegradable polymers are *"polymers, susceptible to degradation by biological activity, with the degradation accompanied by a lowering of its mass."*[171] Other definitions, like the standard CEN/TR 15351:2006,[172] define a biodegradable material as one capable of being mineralized into water, CO_2 and biomass. The quality of biodegradability is defined in EN13432 standard as "the property where a minimum of 90% of the compound can be converted into water, carbon dioxide, and biomass under defined temperature, humidity, and oxygen consumption within six months, in the presence of fungi and microrganisms",[17] while a standardized definition of biodegradable plastics is presented in ISO/TC61/SC5/WG22.[173] Other case-specific definitions can be formulated, for example the biodegradation of materials for medical use is defined as "the chemical breakdown of a material mediated by any component of the physiological environment, into smaller constituents or low molecular weight products which are then processed, resorbed or cleared by the body."[174]
The property of biodegradation refers to what happens after the device has been used, and thus applies to materials coming from both non-renewable fossil resources or renewable ones. On the other hand, the definition of bio-based plastics, or bio-plastics, refers only to the

resources used in the fabrication of the material, which needs to be a carbon renewable source, and might be applied to both biodegradable and non-biodegradable plastics. These two definitions allow to classify all polymers in four main classes, depending on the employed resources and their degradability.[175] It is thus important to properly distinguish between bio-based and biodegradable polymers and not to confuse them. In this chapter, focus is on the degradation behaviour of the materials, independently from which resource is needed to produce them.
In general, when describing the biodegradation process, four main steps can be identified,[176] and are shown in Figure 6.1:

Biodeterioration During this first step, a microbial film is formed on the surface and starts the superficial degradation, with the polymeric material being fragmented in smaller particles.

Depolymerization The microrganisms in the biofilm secrete enzymes, catalysing the depolymerization of the polymeric chains, which turn into oligomers, dimers and monomers.

Bioassimilation Small molecules produced in the previous step are uptaken in the microbial cells, leading to the production of primary and secondary metabolites.

Mineralization Metabolites are finally mineralized, with the production and release in the environment of simple molecules such as CO_2, H_2O, N_2 and CH_4.

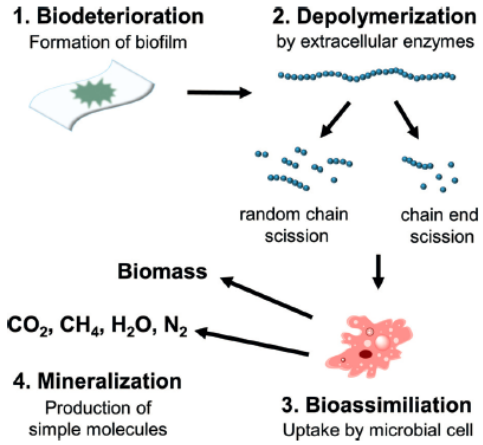


Figure 6.1: Schematic representation of the four main biodegradation steps. Adapted from[176]

Many parameters influence the degradation of polymers, and can be divided into two main categories. Abiotic factors include light, temperature and mechanical stress, while biotic ones refer to naturally occurring elements, such as bacteria, algae and fungi.[177]
The current global production of degradable polymers is continuously increasing and as reached the ton scale per day, accompanied with a drop in prices, which are currently close to those of standard polymers.[178] For what concerns the most produced biodegradable materials, *poly*(*lacticacid*) (PLA) amounts for around 24% of the global production, starch blends are around 44%, polyesters such as *poly*(*butylenesuccinate*) (PBS) and *poly*(*butyleneadipateterephtalate*) (PBAT, Ecoflex®) amount for about 23%, while *poly*(*hydroxyalkanoates*) (PHA) reach 6%.[179]

6.2 Biodegradability tests

Considering the massive increase in interest for biodegradable materials, an increased popularity for this field of research is expected, and in fact a large number of publications is present in literature. From a first analysis, most of these works only mention the word "(bio)degradable" in the title, with no actual degradation test presented in the text, and also when test results are presented, in most cases they have been performed in harsh or non-representative conditions.
In order to effectively substitute commodity polymers with biodegradable ones, a clear understanding of the degradation mechanisms is needed, and a proper assessment of their actual degradation in different environments needs to be carried out. In lab tests, artificial conditions are employed, with defined environmental conditions, enzymes and microrganisms. A proper transfer of these results to actual environmental conditions is possible only taking into account the presence and role of these factors where the material of interest might end up. It is thus necessary to consider the origin of microrganisms, their relative abundance and role inside complex biota, and the presence of other substrates which might act as alternative nutrients.[176]
Additionally, laboratory tests might lack of abiotic factors, such as UV irradiation or the presence of macro-organisms. A possible solution to this issue is the employment of field tests, where the samples are immersed in realistic environments such as soil, compost, lake, river or ocean. These tests, despite being definitely more realistic, present some drawbacks; the environmental conditions are not well controlled and need to be properly documented, there is a limited possibility to analytically monitor the processes, and the determination of weight loss is problematic, requiring the recover and collection of all the fragments.[176]
The rate of biodegradation depends on a variety of parameters, such as the presence and concentration of microrganisms and enzymes, temperature, pH value, relative humidity, light and oxygen supply.[180] All these factors might vary a lot; for example, considering temperature, values might vary from freezing conditions up to 70 °C in industrial composting sites. It is thus essential to assess the biodegradability of a material in different conditions, in order to consider all the possible environments in which it might end up. Considering for example the case of PLA, when placed in hot and humid environments this material shows a quick degradation,[181] while this process becomes much slower when temperatures and humidity levels are reduced,[182] and no weight loss is observed in marine environments.[183] Most of the works

in literature deal with PLA degradation in soil, while only few studies have been performed considering aqueous environments. These examples demonstrate that even the polymer which is commonly considered as the main example for biodegradable applications presents some limitations, and its biodegradability strongly depends on the environment and time frame considered. As a more general comment on this matter, biodegradability tests performed in specific environments may give indications of only an apparent biodegradability of the material.[184]
Biodegradability is not the only parameter to be addressed when considering the performances of degradable materials. The effects of degradation products on the biota need also to be taken into account, with ecotoxicity tests to assure that no harmful products are released. Different tests can be performed, depending on the environment and the duration; terrestrial tests, employing soil organisms, and aquatic ones with algae, crustaceans and fish, used to check both acute and chronic effects, such as lethal and sub-lethal consequences on growth and reproduction, and specific responses like immunotoxicity, neurotoxicity, mutagenicity and carcinogenicity.[185] Most of these studies on biodegradable polymers have been performed for materials used in medical applications, while tests are starting to be carried out only in recent times for materials used for other purposes.
A sub-class of biodegradable materials is that of compostable materials, which is defined as the ability of an organic material to transform into compost through the composting process. This is an aerobic process during which microrganisms decompose the degradable components into CO_2, water, minerals, and compost, a soil-like fertiliser rich in humic components and microrganisms, which improves the soil quality and structure and the bio-availability of nutrients such as nitrogen and phosphorous compounds.[186] As such, all compostable plastics are biodegradable, but not all biodegradable plastics are compostable.[187] The composting process can take place both on large scale, as in commercial composting facilities, which employ three different kinds of wastes, namely manure, yard waste and food waste, and where machines are used for shredding and turning, but also on small scale, e.g. in backyard composting systems, where small composting bins or tumblers are used, the turning is mostly done by hand and the working temperatures are lower compared to the commercial ones, in the range 10 to 40°C and not above 40 °C, thus requiring longer times for complete composting.[188,189]
Multiple organizations have developed in the last decades definitions and standardized tests for the evaluation of biodegradability in different environments and compostability, such as the American Society for

Testing and Materials (ASTM), the European Standardisation Committee (CEN), the Italian Standardization Agency (UNI), the Institute for Standards Research (ISR) and many ohter national and supranational organizations. A standardized common definition of biodegradability has been given in ISO/TC61/SC5/WG22,[173] while for what concerns testing methods, ISO standards have been defined[190] and each country carries out degradability tests according to the standard, and then grants the "biodegradable plastic" or "compostable plastic" authentication.[187] For some countries, international agreements have been signed, and a certificate earned in one country is valid also in the others, e.g. in the case of Germany, USA and Japan.
In the framework of this thesis, the biodegradability of the printed devices has been tested according to the "OECD guideline for testing of chemicals".[191] In this document, different methods for the screening of chemicals for biodegradability in aqueous media are presented, and they all involve the inoculation or incubation of a solution or suspension of the test substance in a mineral medium, under aerobic conditions and with different light exposures. The extent of the degradation is determined according to different parameters such as CO_2, Dissolved Organic Carbon (DOC) or oxygen uptake, which are monitored at sufficiently close time intervals or in continuous until the end of the test, whose duration is usually not longer than 28 days. The method chosen for the samples presented in this chapter is the "301 F: Manometric Respirometry", and it has been carried out at the "Istituto Italiano di Tecnologia" in Genova (Italy) according to the requirements presented in the OECD guideline.[191] In this test, a known volume of inoculated mineral medium, containing a known mass of test material, is stirred in a closed flask at constant temperature, and the consumption of oxygen is measured in two possible ways, either determining the amount of oxygen needed to maintain a constant gas volume in the flask, or from the change in pressure (or volume, or a combination of the two) in the system. The Biochemical Oxygen Demand (BOD) is calculated according to

$$BOD = \frac{mg\,O_2\,uptake\,by\,test\,substance\ -\ mg\,O_2\,uptake\,by\,blank}{mg\,test\,substance\,in\,vessel} \tag{6.1}$$

and then used for the evaluation of the percentage biodegradation as follows

$$\%degradation = \frac{BOD(mg\,O_2/test\,substance)}{ThOD(mg\,O_2/test\,substance)} * 100 \tag{6.2}$$

$$\%degradation = \frac{BOD(mg\,O_2/test\,substance)}{COD(mg\,O_2/test\,substance)} * 100 \tag{6.3}$$

where $ThOD$ is the Theoretical Oxygen Demand and COD is the Chemical Oxygen Demand.

6.3 Biodegradable materials for electronics

Recent decades have not only seen the surge of plastic consumption, but also an increased dependency on electronic devices, accompanied with a shortening of their lifespan. The amount of e-waste has increased accordingly, with issues related both to the amount of waste and the complexity of its disposal.[192] These devices are in fact very diverse, and often contain hazardous and toxic components. In this context, the development of biodegradable electronics, with the realization of devices that are disposable, environmental friendly, low-cost and large-area, allows not only for an, at least partial, solution to the issue of e-waste, but also opens new fields of applications.[193] Biodegradable devices can be employed for medical applications, during diagnosis, medication and treatment,[194] for environmental sensors,[195] ambient intelligence for daily-life assistance,[196] soft robotics,[197] conformal components for recreational purposes,[196] food packaging,[198] throw-away devices,[199] and security applications.[199]
Biodegradable electronics is defined as a "green" version of electronics, exhibiting a transient behaviour, where the device physically disappears after having served its purpose.[17] In order to achieve this result, "green" materials are employed. This is a class of carbon-based materials, with abundant and low-cost precursors, that can be obtained through synthetic routes that avoid toxic solvents usage and toxic waste generation, and that are compatible with low-cost manufacturing techniques. In this way, electronic devices with biodegradability features, or able to perform complex biological functions, can be fabricated.[200]
For what concerns electronic devices, five different components are required; here the main biodegradable materials and their purposes will be reviewed.

Substrate This is the layer upon which the functional layers are deposited, and it generally amounts for most of the volume of the device, and consequently for most of the e-waste generated. For this reason, a biodegradable substrate would tremendously reduce the e-waste amount, and is thus of paramount importance. With the development of organic electronics, flexible and light-weight substrate materials have been considered, but most of them show a very slow biodegradation. In recent years, new materials are being introduced, both of natural and synthetic origin, which show biodegradability, a-toxicity and in some cases even biocompatibility, without sacrificing the mechanical properties mentioned above.
For what concerns natural biodegradable substrates, paper is the

cheapest and oldest one, and its use as substrate has been reported by many groups, because of its low-cost, flexibility, wide availability and lightweight.[201–207] Another natural substrate derived from wood fibers, but with optical and mechanical properties superior to those of paper, is nano-cellulose, which has allowed for the fabrication of fully-transparent OFETs.[208] Silk, which is already widely used for implantable devices thanks to its biodegradability, biocompatibility and lack of immune responses, presents excellent mechanical properties and chemical stability, and has thus been used in recent years also as a substrate for electronic devices.[209] Other natural substrates presented in literature include gelatin, an odourless, colourless and flavourless material made of collagen which is commonly used for ingestible capsules,[194] shellac, a resin produced from the female lac beetle which shows excellent surface morphology,[193] polysaccharides, including polymers derived from starches, for example Ecoflex® (BASF) which is obtained from corn and potato starch,[210] and other exotic substrates such as caramelized glucose.[211]

Focusing on synthetic polymers for biodegradable substrates applications, *polydimethylsiloxane* (PDMS), a well known biocompatible and hemocompatible polymer used for biomedical and microfluidic applications, has been used for the development of stretchable electronic systems.[212,213] Another widely used biodegradable substrate is *polyvinyl alcohol* (PVA), employed for the realization of a variety of devices such as transistors, sensors, capacitors and oscillators.[214,215] *Polylactic acid* (PLA) is another thermoplastic polymer which has raised a lot of commercial interest thanks to its similarities with commodity polymers such as PET and PS; its main drawback is related with its low glass transition temperature, which might render it mechanically unstable and thus unusable as substrate. This issue has been solved using additives, and $poly-lactic-go-glycolicacid$ (PLGA) has been successfully used as resorbable substrate for OFETs.[215]

Dielectric The dielectric layer needs to be realized with an electrical insulator that can be polarized upon the application of an electric field. Most of the substrate materials are insulator, so they can also be used as dielectric materials. For example, a cellulose-based dielectric layer has been demonstrate, able to achieve low-voltage operation,[216] silk-fibroin gate dielectrics have been demonstrated for pentacene-based OFETs,[217] shellac[218] and gelatine[219] have been properly integrated in electronic devices showing superior dielectric properties, and caramelised glucose has been employed

for OFETs applications.[194] For what concerns synthetic polymers, their integration as dielectric materials in organic devices has also been widely demonstrated.[220–222] Next to these examples, other biodegradable dielectric materials have been reported in literature, such as chicken albumen[223,224] and albumin,[225,226] protein-based materials,[227] deoxyribonucleic acid (DNA), mostly extracted from the waste products of the fishing industry,[228–231] and individual nucleobases.[211,232]

Active layer This is the layer where the actual electrical activity takes place, and usually semiconducting materials are used. Traditionally this role is played by silicon but, as it has been shown in the last decades, organic materials might become a cheaper alternative. When considering biodegradable active materials, a main distinction needs to be made between inorganic and organic degradable semiconductors. In the first class, the main role is played by silicon nano-membranes, which are used for the so-called "transient silicon" application;[233] the main advantage here is the wide availability of industrial machinery and processes, while most of the drawbacks relate with the eventual long-term toxicity of the by-products and the mind-set of the society. The latter group of semiconductors is composed mostly of nature-inspired materials, including carotenoids,[194,211,234] dye molecules such as indigo[211,235–237] and other nature-inspired materials like anthraquinones,[237] Tyrian purple,[237,238] indanthrene yellow G and brilliant orange RF,[194,211] quinacridones,[237] and perylene/naphtalene imides.[17,194,211,239]

Electrodes The main role of electrodes is to carry charge carriers from the device to the external circuit, so conductive materials are required for this role. Traditionally, gold and silver have been used, showing not only high conductivity values but also interesting properties in terms of chemical inertness and corrosion resistance. More physiologically friendly materials have been considered recently, such as magnesium, zinc, tungsten and molybdenum, which can be metabolised in physiological conditions, being then absorbed or passed out of the body in a safe manner. On the organic side of the spectrum, two main players have been identified, able to couple high flexibility and decent conductivity values, and are PEDOT:PSS and melanin. Melanin is a natural-origin material that presents a conductivity which is strongly dependent on its hydration level, and shows not only electronic but also ionic conduction.[240] PEDOT:PSS, together with polyani-

line, poly(pyrrole) and poly(thiophenes), belongs to the class of organic electron-conducting polymers; the biocompatibility and non-toxicity of these materials have been demonstrated, together with their superior mechanical properties, but there is still a lack of information regarding their degradation behaviour.[193]

Encapsulation Organic semiconductors have a well-known sensitivity to environmental degradation, and thus need an encapsulation layer to ensure proper operation while exposed to oxygen and humidity. Few reports of encapsulation layers have been reported in literature, employing for example *polyvinyl acetate* (PVAc).[241]

6.4 Ultraflexible OFETs on a biodegradable substrate

The work presented in this thesis represents the starting point toward the development of fully-biodegradable organic transistors. As mentioned in the previous section, the substrate represents the biggest portion of the volume of thin film electronic devices, and its substitution with biodegradable materials allows to strongly reduce the amount of e-waste generated. For this reason, the first step that has been implemented is the employment of a biodegradable substrate, onto which a non-biodegradable device structure has been fabricated. Aiming at a full biodegradability, successive steps will obviously deal with the substitution of each polymeric layer with a degradable alternative.
The chosen substrate material for this work, not included in the list presented above, is Mater-Bi. Mater-Bi is a family of completely biodegradable and compostable bioplastics which are being used to provide low environmental impact solutions for every day products.[242] It is currently used for a wide variety of applications, in fields ranging from agriculture to food service, from packaging to carrier bags and organic waste collection. It is currently used for the fabrication of mulching films, compostable clips for crops, lightweight carrier bags that can be re-used for the collection of organic waste, biodegradable and compostable tableware, e.g. cutlery, cups and dishes, and a multitude of other packaging applications, such as bags, sealing films, trays and lids, that can be manufactured with the traditional equipments used for standard plastics, such as blow moulding, injection moulding and thermoforming.
The biodegradability and compostability of this class of materials has been widely tested, and is guaranteed by 7 different accreditation systems delivered by certification bodies around the world,[243] assuring among the others the compliance to the relevant harmonized European standards EN 13430 (recycling), EN 13431 (energy recovery), EN 13432 (organic recovery).
Novamont has been developing starch-based biodegradable materials, with different degradation and mechanical properties, to be used for a range of applications. Starch is an inexpensive product, abundantly available throughout the year, which is fully biodegradable in a variety of environments, and thus allows for the development of totally degradable materials that suits the market needs.[244] When considering degradable polymers, or materials in general, coming from natural resources, attention needs to be paid in order not to perturb the ecosystem; for this reason, the resources need to be materials that can

be renewed in short time (< 1 year) intervals.[245] Focusing on Mater-Bi, its essential components are non-genetically modified corn starch and vegetable oils, cultivated in Europe with conventional practices; currrently, only about 1% of the produced corn starch is used for bioplastics. The global landuse for the manufacturing of bioplastics is of about 1.2 million hectares, amounting for less than 0.02% of the total global arable land surface, and the fabrication of 1 kg of Mater-Bi requires 15-30 liters of water irrigation for the renewable raw materials, giving minimum impact on global water resources. All these data show the very limited impact of the bioplastic prouction on the available natural resources.[246]
The Mater-Bi trademark includes four classes of biodegradable materials,[247–249] namely:

Class Z Biodegradable and compostable, for films and sheets applications, obtained as a blend of thermoplastic starch and $poly-\epsilon-caprolactone$. It can present very different microstructures, from a dispersion of starch in the synthetic matrix to a semi-continuous phase.

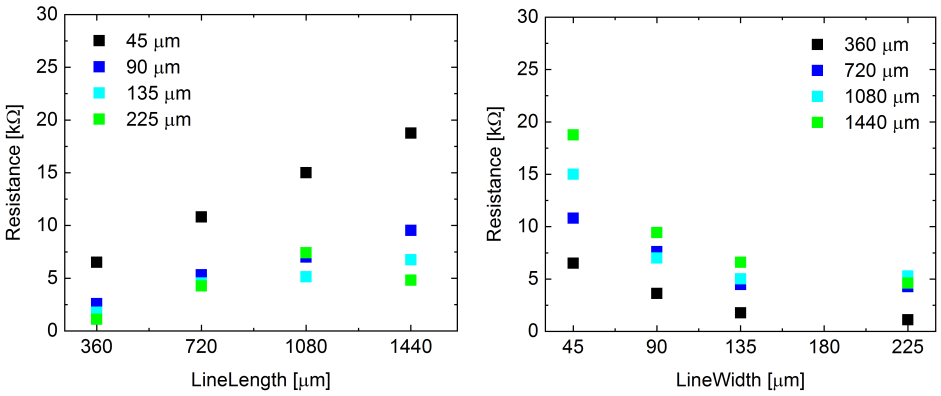
Class V Biodegradable, compostable and soluble, with a starch content higher than 85%, can be used as replacement for polystyrene packaging foams.

Class Y Biodegradable and compostable, with all-natural raw materials such as thermoplastic starch in cellulose derivatives and mechanical properties close to those of polystyrene, is ideal for rigid and dimensionally-stable molded items.

Class A Biodegradable and non-compostable, it contains thermoplastic starch complexed with ethylene-vinyl alcohol polymers, and is generally used for applications where compostability is not required.

Two Mater-Bi grade materials, namely Z101U and ZF03U/A,[250] have received the "OK COMPOST" label. These materials have mechanical characteristics close to those of low-density polyethylene, and are designed for applications in the form of films and layers, being compatible with traditional fabrication methods such as blow moulding; for this reason, starting from the beginning of the '90s, they have been employed for the realization of compostable bags for organic waste collection.[251]
Biodegradable and compostable Mater-Bi-based bags, bought from the supermarket, have been used for the fabrication of OFETs. These

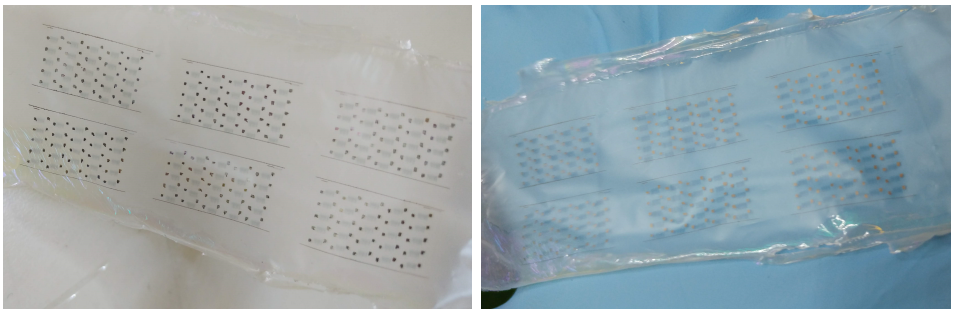
bags are suitable for the transport and packaging of fruit and vegetables, and they are conform to the norm UNI/EN 16640/2017. The bags have been cut in small pieces with the help of a scalpel and then applied onto a glass slide, acting as a carrier; the thickness of the bags is of few µm, so their handling in the form of self-standing films would be pretty complex.
Before starting with the actual fabrication of the devices, the thermal stability of this substrate and its solvent resistance have been assessed. For what concerns the first, the Mater-Bi films present a strong sensitivity to thermal treatments, with clear structural changes even for short annealings at relatively low temperatures, around 60 °C. For this reason, the thermal budget during device fabrication has been eliminated, substituting all the thermal annealings with vacuum drying of the printed materials. The annealing steps have a variety of beneficial effects, going from the obvious solvent removal up to helping in reducing the density of pinholes in the dielectric layer, and thus reducing the leakage current, filling up trap states and removing moisture from the system. The substitution of thermal treatments with vacuum drying leads to a slight loss in performances, because the drying step can compensate for only some of the annealing effects.
Focusing on the solvent resistance, brief tests have been carried out and the Mater-Bi films show great stability against water and mesitylene, making them compatible with the printing process needed for the patterning of electrodes and semiconductor pads. Unfortunately, this substrate is quickly deteriorated and dissolved by n-butyl acetate, and thus the bilayer dielectric presented in the previous chapter could not be employed, leading to the adoption of only a parylene film as dielectric layer, applied directly in contact with the semiconductor film by means of a solvent-free deposition process. The lack of PMMA layer, and the subsequent direct exposure of the n-type semiconductor to the chlorine atoms present in the parylene film, lead to a slight worsening of the OFET performances, as shown in 4.1. For this reason, the expected mobility values for the n-type devices are lower than those previously shown.
After testing the solvent stability of this substrate, and before proceeding with the fabrication of organic transistors, the performances of the electrode material have been tested, printing PEDOT:PSS lines onto Mater-Bi substrate and characterizing its conductivity. In Figure 6.2, the resistance values are shown, both as a function of channel length and channel width.
As it can be seen from Figure 6.2a, the trend of 45 µm lines is almost linear, and can be safely used for the extraction of the resistivity value



(a) Resistance as a function of line length. (b) Resistance as a function of line width.

Figure 6.2: Resistance values of the printed PEDOT:PSS lines onto a Mater-Bi film substrate, represented as a function of both the length and the width of the lines.

for the printed PEDOT:PSS lines. Following the same procedure presented in the previous chapter, Equation 5.3 has been used and the obtained resistivity amounts to $(2.8 \pm 0.4) * 10^{-5} \Omega\,\mathrm{m}$, which is perfectly in line with the printed PEDOT:PSS performances when PEN and parylene films are employed as substrate.
After checking the electrodes performances, OFETs have been fabricated following the steps presented in Section 4.4, with the above mentioned differences for what concerns thermal treatments and the dielectric layer composition. In Figure 6.3, the photographs of printed transistors on Mater-Bi substrate are shown.

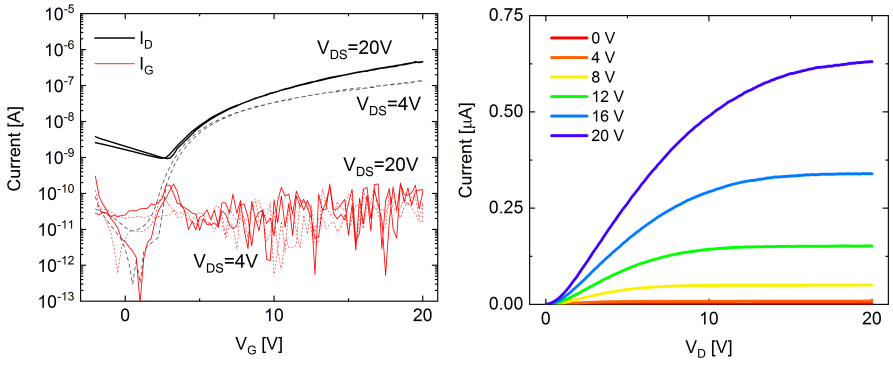


(a) (b)

Figure 6.3: Photograph of the printed, all-organic transistors onto a biodegradable, Mater-Bi substrate.

The electrical characterization of the printed *n*-type transistors has been carried out measuring transfer and output characteristics, shown in Figure 6.4. The characterization of these devices has been carried out in glovebox, with the devices in a nitrogen atmosphere. Differently

from the devices of the previous chapters, the creation of stable and neat electrical connections between the measuring probes and the pads on the devices is complex, mostly due to the nature of the substrate, which is in fact pretty soft and not perfectly adhering to the substrate; for this reason, most of the measured transfer curves show not perfectly clean and slightly trembling signals, which translates into a more noisy signal for all the extracted parameters.
In Figure 6.4, the transfer and output characteristics for one printed n-type OFET on a biodegradable substrate are shown. The devices presented in this chapter have not been optimized for low-voltage operation yet, and the parylene film used as dielectric layer has a thickness of about 240 nm, leading to a dielectric capacitance which is roughly half of the ones previously presented. The supply voltages required for their proper operation are thus slightly higher, with V_G and V_D values in the order of 20 V. As it can be seen from Figure 6.4a, the OFET shows proper field effect modulation, with current values slightly lower than the ones of the devices printed on PEN and parylene, and the leakage current is flat and lower than 100 pA, so low-leakage operation of the devices is ensured, also thanks to the increased thickness of the dielectric layer. Focusing on the output curve in Figure 6.4b, non-idealities related to the injection of charges from the electrodes can be noticed from the S-shape of the curve. Despite these expected small faults, the n-type OFETs printed on Mater-Bi substrate are properly working.



(a) Transfer curve.

(b) Output curve.

Figure 6.4: Electrical characterization of an all-polymeric n-type OFET printed on a biodegradable Mater-Bi substrate.

The uniformity of these devices have been tested, with the characterization of 20 devices printed onto a single 2x7 cm substrate, and the average transfer curve is shown in Figure 6.5. The standard deviation is higher than that recorded for devices on PEN and parylene substrates,

but the performances of the OFETs are still pretty uniform, and this is an interesting result, considering the commercial nature of the substrate and the fact that it has not been altered in any way before the fabrication of the devices. The leakage currents of all the measured devices are also reported, and it can be seen how the gate current is flat and stably below 100 pA. Differently from the devices printed on PEN, here the curves are not perfectly flat but present spikes and noise; this is to be attributed to the above mentioned difficulties in creating stable electrical connections with the measuring probes, which ultimately lead to an increased noise in the recorded signal. The average maximum current for these devices is equal to (0.33 ± 0.14) µA.

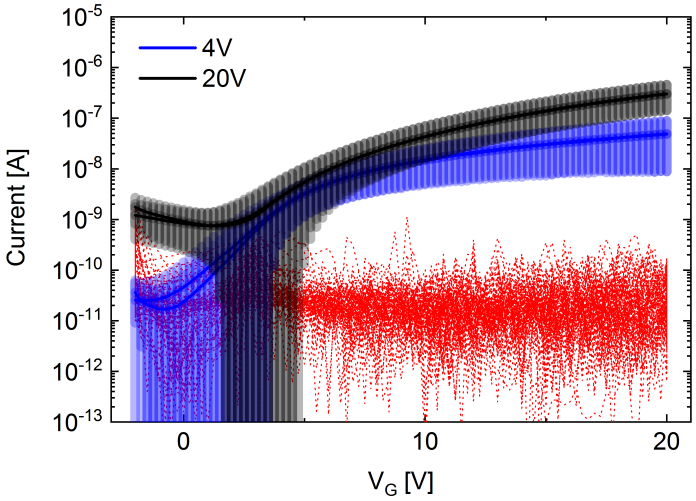


Figure 6.5: Average transfer curve obtained from the characterization of 20 printed OFETs.

The transistors' parameters have been extracted for these devices. Average mobility values equal to $0.004\,81\ \mathrm{cm^2V^{-1}s^{-1}}$ and $0.012\,34\ \mathrm{cm^2V^{-1}s^{-1}}$ have been obtained, in linear and saturation regimes respectively, and the average curves are shown in Figure 6.6. The mobilities for these OFETs are one order of magnitude lower than the ones obtained for devices printed on PEN; these reduced performances where expected, as it was mentioned at the beginning of this section, because of the impossibility to use the PMMA interlayer, and thus the need to employ the parylene dielectric film in direct contact with the semiconductor, with the consequent loss in mobility given by the direct contact between the chlorine atoms of the parylene film and the P(NDI2OD-T2) layer. A comment should be added at this point, concerning the standard deviation of the mobility curves; as it can be seen from the curves in Figure 6.6, mostly for what concerns the linear regime, and as it

will be shown also later on in this chapter, the reported standard deviations for mobility curves are pretty substantial. The explanation is to be found in the above mentioned difficulties encountered when characterizing these OFETs; the issues in the measurements lead to not-perfectly-flat and quite noisy transfer curves, and the noise has been amplified during the evaluation of the mobility, leading eventually to the reported substantial standard deviations.
The average on-off ratio is equal to $(1.12 \pm 1.08) * 10^6$; most of the devices present an on-off ratio in the order of 10^6, with only few devices that have limited ratios, one or two orders of magnitude lower, leading to the massive standard deviation reported above. The subthreshold slope has been evaluated according to Equation 2.13, leading to an average SS for the above mentioned OFETs equal to 685 ± 274 mVdec^{-1}, with the best performing device showing a subthreshold slope equal to 327 mVdec^{-1}. The average onset voltage and the threshold voltage are equal to 2.36 ± 0.95 V and 2.74 ± 1.69 V respectively.
All the above presented parameters are slightly lower than the ones obtained for organic transistors printed on more standard substrates, yet adequate for the possible employment of these structure as the building block for the development of more complex electronic circuitry.

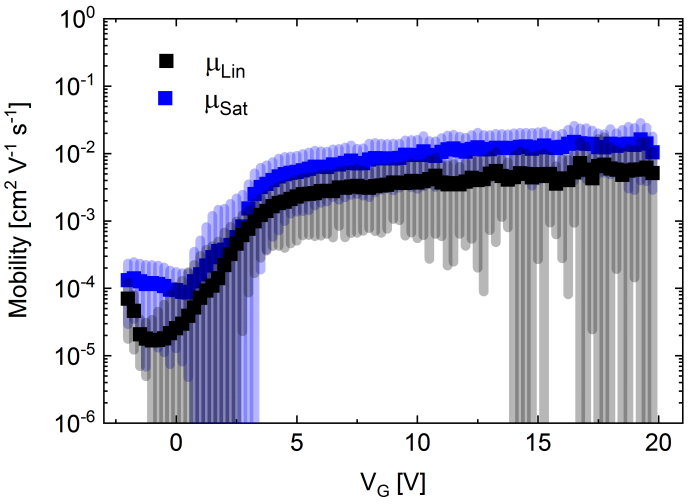
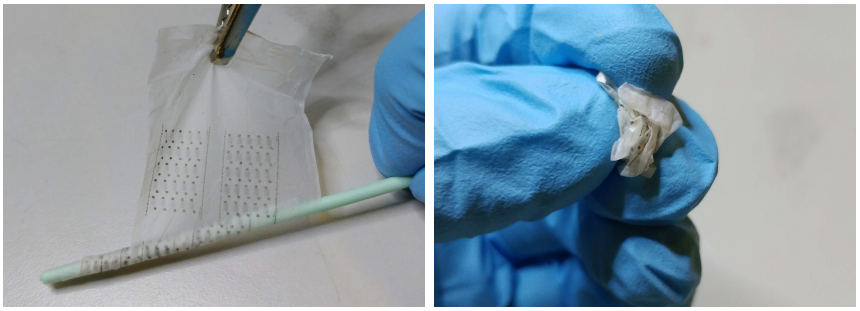


Figure 6.6: Average mobility curves, in linear and saturation regimes, for the 20 printed organic transistors on Mater-bi substrate.

The mechanical stability of these devices has also been assessed, with the same tests performed in Chapter 5, namely rolling and crumpling. The OFETs have been rolled onto a very thin plastic substrate and crumpled, as shown in Figure 6.7, and then the transfer characteristics of the transistors have been recorded after bringing the substrate back

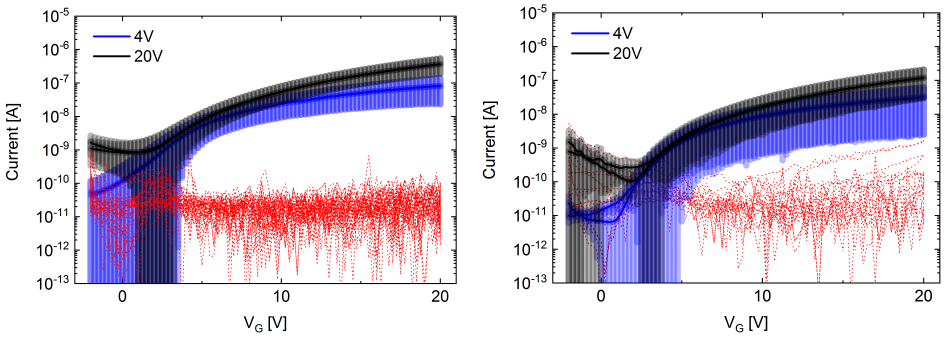
to its flat configuration.



(a) Rolling. (b) Crumpling.

Figure 6.7: Photographs of the printed devices onto the Mater-Bi biodegradable substrate during the mechanical tests.

The average transfer curves for both these tests are shown in Figure 6.8. Qualitatively, the currents for the rolled devices are unchanged from the pristine device, while the crumpled transistors present slightly lower drain currents. The standard deviations for both cases resemble those of the as-fabricated devices, meaning that the mechanical tests did not lead to a wider diversification of the OFETs performances.
The extracted maximum drain current values are equal to 0.34 µA and 0.19 µA, for rolling and crumpling respectively. Rolling does not have any relevant effect on the maximum current, while crumpling halves the average drain current; this loss in performances can be attributed to the structure of the OFETs which, differently from the devices presented in the previous chapter, is not optimized for the ultraflexible operation and does not have any encapsulation layer, thus leaving the active layer in the most stressed plane and not in the neutral-plane position.
The average mobility values for the OFETs after the mechanical tests have been calculated and they are presented in Figure 6.9. For what concerns the rolled devices, the mobilities in linear and saturation regimes are equal to $0.0065\,cm^2V^{-1}s^{-1}$ and $0.013\,88\,cm^2V^{-1}s^{-1}$ respectively. The crumpled devices, on the other hand, show average mobility values equal to $0.003\,29\,cm^2V^{-1}s^{-1}$ and $0.005\,29\,cm^2V^{-1}s^{-1}$ in linear and saturation regimes. These mobility values are in accordance with what has been observed directly from the transfer curves; the performances of the printed organic transistors after rolling are basically unaltered, while there is a slight loss in performances after crumpling. All these curves present significant standard deviations, whose origin and cause has already been discussed in this section.
Focusing on the other main transistors parameters, reported in Table 6.1, it can be noticed how the mechanical tests do not lead to rele-

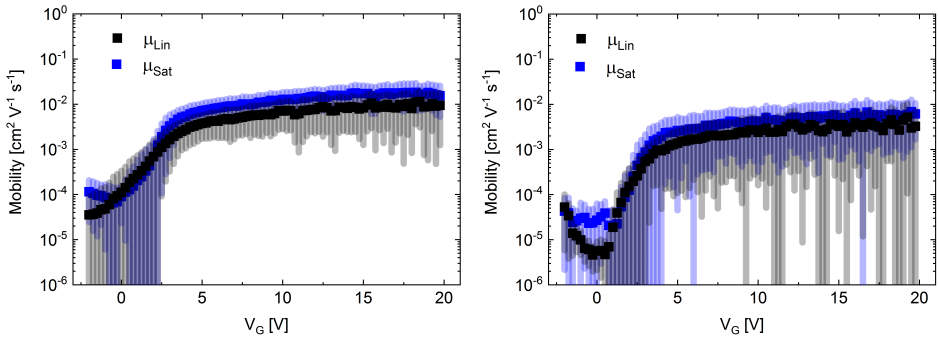


(a) Transfer curves after rolling.

(b) Transfer curves after crumpling.

Figure 6.8: Average transfer curves for the all-polymeric *n*-type OFETs printed on a Mater-Bi film after the two mechanical tests, rolling and crumpling. The two curves refer to linear (blue curve, 4 V applied) and saturation (black curve, 20 V applied) regimes. The leakage currents for all the devices are shown in red.

vant changes, with the average subthreshold slope and the on-off ratio remaining almost unchanged after both tests.



(a) Average mobilities after rolling.

(b) Average mobilities after crumpling.

Figure 6.9: Average mobility curves for the printed *n*-type OFETs on a Mater-Bi film after the two mechanical tests, rolling and crumpling. The blue curve refers to the saturation regime (20 V), while the black one is for the linear one (4 V).

In this chapter, non-degradable devices printed on biodegradable and compostable substrates have been presented. Their degradation behaviour has been tested, according to the standards and procedures presented in the previous section, in order to understand which is the effect of the organic devices on the biodegradability of the Mater-Bi films. For this reason, "301 F: Manometric Respirometry" tests have been carried out on both the blank substrate and the final device, and a comparison between the *BOD* curves is presented as main result.
In details, about 80 mg of sample were added to 432 ml of seawater as the single carbon source. The seawater was chosen in order to mimic

Table 6.1: Average mobility values, in linear (4 V) and saturation regimes (20 V) for the *n*-type OFETs printed on a biodegradable substrate, together with their average maximum drain current, subthreshold swing and on-off ratio, evaluated for the devices as-fabricated and after the two mechanical tests, rolling and crumpling.

	As fabricated	Rolled	Crumpled
Linear mobility $[cm^2V^{-1}s^{-1}]$	0.00481	0.0065	0.00329
Saturation mobility $[cm^2V^{-1}s^{-1}]$	0.01234	0.01388	0.00529
Maximum drain current [µA]	0.33 ± 0.14	0.34 ± 0.17	0.19 ± 0.09
Subthreshold swing $[mV dec^{-1}]$	685 ± 274	747 ± 404	627 ± 342
On-off ratio	$(1.12 \pm 1.08) * 10^6$	$(5.88 \pm 0.18) * 10^6$	$(1.43 \pm 1.28) * 10^6$

real environmental conditions. It already contains microbial consortia and the saline nutrients needed for the growth. The experiment was conducted at room temperature inside dark glass bottles with a volume of 510 ml, hermetically closed with the *OxiTop* measuring head. Biotic consumption of the oxygen present in the free volume of the system was measured as a function of the decrease in pressure. Samples were tested in triplicate. Raw data of oxygen consumption (mg O_2/l) were corrected subtracting the mean values of the blanks, obtained by measuring the oxygen consumption of the seawater in absence of any test material. After this subtraction, values were normalized on the mass of the individual samples and referred to 100 mg of material (mg O_2/100 mg *material*). Finally, means and standard deviations of the triplicates were calculated and plotted against time.
The *BOD* of the Mater-Bi films, pristine and with the printed OFETs, is reported in Figure 6.10. Both samples show some level of biodegradability and the general behaviour is comparable, with the curves approaching a plateau after 30 days of analysis. Nevertheless, some differences can be observed between the sample with the electronic devices and the reference material and, considering the standard deviation, these differences are significant. In details, while Mater-Bi starts its biodegradation after three days, the samples with the printed transistors start after five days. This expected delay can be justified considering that the electronic devices are covering part of the surface, and

thus hindering the microbial attack, which becomes slower. Focusing on the final result, after 30 days, the biodegradation achieves higher levels for the reference material (Mater-Bi), with a value of about 4.2 mg O_2/100 mg *material*, compared to the 2.8 mg O_2/100 mg *material* reported for the printed transistors.

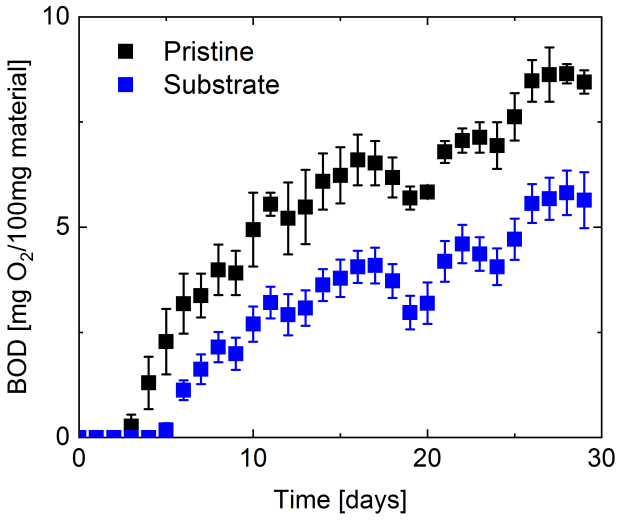


Figure 6.10: *BOD* [mg O_2/100 mg *material*] measured for the pristine Mater-Bi films (black dots) and for the Mater-Bi film acting as a substrate for printed OFETs (blue dots).

6.5 Summary

In this chapter, the main motivations behind the development of biodegradable electronics have been presented. The amount of e-waste has been massively increasing in recent years, and the development of disposable and environmental friendly devices might help mitigating this issue. Furthermore, the possibility to couple the advantages of organic electronics, such as the cost-effective and large-area fabrication techniques, with the degradation characteristics of degradable polymers, opens up a variety of new applications in different field, such as the medical one, for diagnosis, medication and treatment, or for the realization of environmental sensors, soft robotics, conformal components for monitoring of biological signals, packaging and security applications.
The biodegradability of these materials needs to be tested, starting from lab tests, where well-defined environmental conditions are used, and transferring these results to real environments, where a multitude of additional factors comes into play. The biodegradation rate depends on a variety of conditions, both biotic and abiotic, making its evaluation a definitely complex task. Next to the biodegradability of a material, its ecotoxicity needs to be estimated, considering the degradation effects on the biota, in order to assure that no harmful products are released.
The realization of an organic device requires five main components, substrate, electrodes, active semiconducting layer, dielectric and encapsulation. The substrate plays a major role in this context, occupying the biggest volumetric portion, and thus being the main contributor in terms of generated waste. The substitution of standard substrate materials with organic counterparts strongly reduces the amount of e-waste, so as a first step toward the development of fully-biodegradable OFETs, a degradable and environmental friendly substrate has been employed, onto which non-biodegradable devices have been fabricated. Mater-Bi, a starch-based compostable and biodegradable material, is the material of choice, and Mater-Bi-based plastic bags bought from the supermarket have been used as substrate for the realization of printed organic transistors. All-organic devices have been realized, using PEDOT:PSS for the electrodes and P(NDI2OD-T2) as semiconductor material, both patterned by ink-jet printing, and parylene for the dielectric layer. The proper operation of n-type OFETs has been demonstrated, with mobility values one order of magnitude lower than the ones obtained for the same devices on standard plastic substrates, yet demonstrating proper transistor operation. The mechanical stabil-

ity has also been tested, performing rolling and crumpling as for the ultraflexible devices fabricated on parylene, and no loss in performances has been recorded for the rolled devices, while there is a slight loss in current and mobility for the crumpled transistors.
In the framework of this thesis, biodegradability tests have been carried out according to the "OECD guideline for testing of chemicals" in collaboration with the "Istituto Italiano di Tecnologia" in Genova (Italy), and the "301 F: Manometric Respirometry" analysis has been carried out on both the blank substrate and the final device, in order to determine the difference in Biochemical Oxygen Demand (BOD) between the two and thus the effect of the printed OFETs on the degradation behaviour of the compostable Mater-Bi substrate.
The work presented in this chapter is at an embryonic stage, and plenty of effort still needs to be made toward the development of biodegradable electronic devices for the consumer market. First, the development of *p*-type non-degradable organic transistors onto this same substrate needs to be achieved, followed by the development of complementary circuits granting additional electronic functionalities for the devices in which they are integrated. These devices would represent a first milestone toward the realization of degradable electronics, but they still employ non-biodegradable materials for most of the components. Further research is then needed in order to substitute all these elements with biodegradable materials, eventually culminating with the realization of fully-organic and biodegradable complementary electronic devices, able to integrate advanced electronic functionalities into everyday products without increasing the amount of waste generated.

7

Conclusions

"Wir leben alle unter dem gleichen Himmel, aber wir haben nicht alle den gleichen Horizont."[a]
– Konrad Adenauer

[a] "We all live under the same sky, but we don't all have the same horizon."

In this thesis, the realization of organic field effect transistors and integrated circuits and the optimization of their low-voltage operation has been reported, together with the integration of these devices onto different substrates, in order to improve their mechanical performances and limit their environmental impact.
In the first part of the thesis, a PMMA-parylene dielectric bilayer has been optimized for low-voltage and low-leakage operation and, together with a PEI-based injection layer developed for the *n*-type transistors, it has been integrated into printed and all-organic OFETs. PEDOT:PSS has been used as the conductor of choice, and organic semiconductors, namely P(NDI2OD-T2) and 29-DPP-TVT, have been used as active materials, with ink-jet printing as the main fabrication method, used for all the layers except for the dielectric one. In this framework, field effect behaviour for voltages as low as 1 V has been demonstrated

for transistors of both polarities, currents higher than 1 µA have been recorded for voltages in the order of 10 V, and pretty high effective mobility values have been extracted, equal to 0.23 and 0.24 $cm^2V^{-1}s^{-1}$ in linear and saturation regimes for *p*-type OFETs, and to 0.07 and 0.10 $cm^2V^{-1}s^{-1}$ respectively for the *n*-type transistors. The *n*-type devices show pretty high *r* factors, equal to 0.81 and 0.73 for linear and saturation regimes respectively, while for the *p*-type ones the performances are almost ideal, with the reliability factors amounting to 0.96 and 0.95. The low-temperature and large-area compatible fabrication procedure employed shows high yield, which has been assessed using two 100-transistors arrays and is equal to 99%, and leads to the realization of highly uniform devices. The transistors have been realized on a 125 µm-thick PEN film, and their bendability has been tested, demonstrating stable operation of the devices for at least 1000 bending cycles with an applied strain higher than 1%.
After demonstrating the proper operation and mechanical features of *p*- and *n*-type transistors, fabricated onto the same substrate, with the same fabrication techniques and compatible thermal processes, the work proceeded further with the realization of complementary integrated circuits, starting from the simplest one. Complementary organic inverters have been realized, composed of one *n*- and one *p*-type OFET with shared drain electrode and common gate, and their proper operation has been demonstrated, with switching threshold close to the middle of the applied voltage interval, proper inverting behaviour and small hysteresis, noise margins higher than 50% for all the realized devices and average gain value equal to 14. The printed organic inverters have been integrated into ring oscillators, and their proper operation has been demonstrated for voltages as low as 2 V, with average oscillating frequency for 7-stage devices equal to 6 Hz for a supply voltage of 2 V, which increases up to the maximum recorded frequency of 62.5 Hz at 10 V. Lastly, D-Flip-Flop have been implemented connecting two D-Latch in master-slave configuration, realizing one of the building blocks needed for the development of sequential logic circuits, memory and timers, and proper operation has been demonstrated again for voltages as low as 2 V. The transparency of these circuits has been assessed with UV-vis spectrometry, with values higher than 90% in all cases, and the shelf-life stability has been demonstrated up to 4 months, for devices stored in inert nitrogen atmosphere without encapsulation.
All these results show how all-organic and printed OFETs on plastic substrate can be employed as basic building block toward the realization of electronic components able to operate at low voltage, and thus compatible with thin film batteries and plastic solar cells; the

reported circuits represent in fact the first demonstration of printed, all-polymeric, transparent and flexible ring oscillators and D-Flip-Flop operating at low voltages. These devices are just proof of concepts, and further work is needed in order to realize more complex circuitry, but these results pave the way toward the cost-effective integration of electronic functionalities into everyday objects.

The results presented in the first chapter are characterized by great mechanical performances, being stable upon the application of pretty high strains, but the substrate thickness is such that high strain levels are obtained for limited bending radii. The development of ultraflexible electronics, characterized by thin and flexible form factors, improved lightness and the ability to conform to irregular surface, can be pursued implementing two main strategies. The applied strain is inversely proportional to the thickness of the device, so the employment of thinner substrates allows to withstand smaller bending radii. Additionally, placing the active layer in the neutral-plane position limits the stress on the device even further, and improves its stability. Taking into account these two requirements, an ultrathin parylene film, 2 µm thick, has been used as substrate, and an equally thick layer has been used for the encapsulation of the devices. The same materials employed in the previous chapter has been used for the realization of OFETs and complementary circuits, except for the *p*-type transistor, for which another DPP derivative, namely DPPT-TT, has been considered, and with the same fabrication techniques.
Similar performances to those reported for devices on PEN have been obtained, with basically no variation in mobility for the *n*-type OFETs and only slightly worse values the *p*-type ones. The ultraflexibility of the devices has been assessed using two mechanical tests, rolling and crumpling, and only a slight loss in recorded currents, and thus in mobility values, has been obtained for devices of both polarities, but with overall more than satisfying electrical performances even after harsh stresses. The printed OFETs have thus been employed for the development of more complex conformable circuitry, and following the same reasoning presented for the devices on PEN, complementary inverters have been fabricated. Proper circuits operation has been demonstrated, with rail-to-rail behaviour, inverting thresholds close to $V_{DD}/2$ and gain values higher than 10 for voltages as low as 3 V before the mechanical tests. Rolling and crumpling have been performed also on the inverters, and proper operation has been retained, with only a slight worsening in gain values, for which the minimum value of 10 is now reached for supply voltages equal to 4 and 6 V respectively.

These devices represent the first demonstration of transparent, all-organic, printed and ultraflexible OFETs and complementary inverters operating at low voltage. This work is a proof of concept, demonstrating the feasibility of this fabrication method for the realization of conformable electronic devices, and further work is needed in order to improve their yield and uniformity, in order to be able to develop more complex circuitry and thus move toward the realization of low-cost and lightweight epidermal and imperceptible devices that can be integrated into consumer products.

In the last part of the thesis, a paradigm change has been proposed, and the main motivations for the development of biodegradable electronic devices have been presented, together with a possible approach. The main aim of this niche of organic electronics is the integration of the peculiar features of plastic-based electronic devices, such as low-cost, mechanical flexibility and compatibility with solution-based and large-area manufacturing methods, with the degradation characteristics of degradable and compostable polymers, in order to limit the amount of plastic waste generated but also to disclose new fields of application, for example in the medical field or for the realization of environmental sensors, packaging and security applications. The definition of biodegradability has been introduced, together with the main issues and most important parameters involved in biodegradability and compostability tests, and the standards that have been defined in the last decades. The degradable organic materials proposed in literature for the realization of fully-biodegradable electronic devices have been reviewed, and the pivotal role of substrate, compared to all other layers, as contributor toward the generation of waste has been determined. In the framework of this thesis, the integration of non-degradable OFETs onto a biodegradable substrate has been proposed, as a first step toward the fabrication of fully-degradable devices. Mater-Bi, a starch-based compostable material, has been used as substrate, in the form of commercially produced films, and printed organic transistors have been realized. Proper n-type operation has been demonstrated, with mobility values lower than those obtained on standard plastic substrates, but still retaining proper transistor operation. Mechanical tests have been performed, namely rolling and crumpling, and no significant loss in performances have been recorded for the former, while the latter leads to a slight worsening of the current and mobility values, and the effect of the printed OFETs on the biodegradation of the substrate has been assessed.
These results are still at an undeveloped stage, and plenty of work is still

needed in order to first develop non-degradable complementary transistors and circuits onto biodegradable and compostable substrates, and then to move towards the realization of fully-biodegradable electronic circuitry.

The results presented in this thesis, together with all the achievements reported in literature in the last decades, show the feasibility of organic electronics as a main player for the realization of flexible and low-cost electronic devices. Some issues are still to be discussed, and obstacles need to be overcome before plastic electronic devices could be integrated into consumer products, with the realization of more complex circuitry, an improved yield of fabrication, and a boost in transition frequency. Work is thus needed from the material side, with combinations of existing materials and new tailored solutions with improved structure and properties, from the architecture side, with advanced configurations able to overcome the current limitations, and from the fabrication techniques side, with further development aiming at better yields and mass production on always increasing scales.
Plenty of efforts are still needed, but the path is clear and the widespread integration of organic electronic devices into consumer products will soon become reality.

List of Figures

List of Tables

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