Politecnico di Milano

SCUOLA DI INGEGNERIA INDUSTRIALE E DELL'INFORMAZIONE

Corso di Laurea Magistrale in Electronics Engineering

TESI DI LAUREA MAGISTRALE

DESIGN OF AN 80-GHz FREQUENCY-MULTIPLIER-BY-FOUR WITH POWER AMPLIFICATION IN BiCMOS PROCESS

Relatore:
Prof. Salvatore LEVANTINO

Correlatore:
Dott. Saleh KARMAN

Candidato:
Guglielmo Maria DE FILIPPI
Matricola N° 883150

Sommario

I ricetrasmettitori wireless per reti 5G necessitano di riferimenti di frequenza a basso rumore di fase in onde millimetriche. Considerate le difficoltà di implementare riferimenti basati su anelli ad aggancio di fase (PLL) direttamente ad onde millimetriche, tipicamente si utilizza uno stadio di moltiplicazione di frequenza. Questo lavoro tratta la progettazione di un moltiplicatore di frequenza fattore quattro a 80GHz in processo BiCMOS SiGe. Il moltiplicatore è composto da stadi di tipo push-push posti in cascata e da un amplificatore in classe A che riporta la potenza RF al livello richiesto dal successivo mixer. L'accoppiamento del segnale inter-stadio viene effettuato mediante l'uso di trasformatori integrati accordati che permettono di realizzare una trasformazione d'impedenza a larga banda e transimpedenza a banda piatta, i componenti passivi sono progettati e modellati mediante simulazioni elettromagnetiche, i circuiti nonlineari caratterizzati con parametri-S di largo segnale e l'adattamento d'impedenza è ottimizzato con una metodologia iterativa. I moltiplicatori raggiungono un guadagno di conversione prossimo a 0dB con un consumo di potenza di 30mW. L'amplificatore garantisce una potenza d'uscita di 7 dBm a 80GHz con una banda passante frazionaria del 40% e una power-added efficiency di picco del 10.9%.

Abstract

Wireless transceivers for 5G networks require millimeter waves low-phase-noise frequency references. Given the difficulty in direct mm-Wave references generation with PLLs, a frequency multiplier stage is typically employed. This work covers the design of an 80GHz factor-four frequency multiplier in SiGe BiCMOS process. The multiplier consists of stacked push-push stages and a class-A power amplifier, which recovers the RF power required by the following mixer. Signal interstage coupling is accomplished with integrated doubly-tuned transformers which allow to achieve broadband impedance transformation and flat-band transimpedance, passive elements are designed and modeled with electromagnetic simulations, nonlinear circuits characterized by means of large-signal S-parameters and impedance matching is optimized by making use of iterative methods. The multipliers reach a conversion gain around 0dB with a power consumption of 30mW. The amplifier delivers 7 dBm output power at 80GHz with 40% fractional bandwidth and a peak power-added efficiency of 10.9%.

Contents

List of Figures

List of Tables

Introduction

Figure 1: From 2G to 5G: user data transfer rate and latency

In the last decades, we got accustomed to a progressively increased speed in cellular data communications. Fifth Generation standard (5G) will target a rate of 10 *Gbps* per single user, which is actually 100x the one provided by 4G. This means that 5G will allow users to get access to high-definition multimedia content, but fast download and high-resolution media will also enable augmented and virtual reality. Nevertheless, throughput will not be the only improvement; network latency will drop from $50ms$ to $1ms$, allowing 5G to become an enabling technology for real-time remote control applications, such as assisted/autonomous driving, drone fleets control and remote

surgery.

Another challenge is density: targeting one million devices per Km^2, it will be possible to implement IoT and V2X (Vehicle-to-Everything).

We can conclude that 5G is much more than the evolution of the current 4G cellular network standard, and will be an actual enabling technology for many innovations that will become part of everyday life in the next years.

In order to satisfy the aforementioned requirements in terms of user data-rate and density, the number of base-stations will get dramatically higher, moving to smaller, more dense and more efficient micro-cells. For this reason, micro-cell backhauling will not have access to fiber optic links and will need to move towards more cost-effective solutions, considering that already-existing fixed microwave links for cellular backhaul operating in the $6-38GHz$ range cannot guarantee the required bandwidth capability [1] .

Both FCC and ETSI have allocated $71-76GHz$ and $81-86GHz$ bands for millimeter-wave fixed backhaul links, within E-band[1], which could provide the best solution for multi-Gbps Km-range wireless communications, considering that they lie on favorable spectrum portions of oxygen attenuation (fig. 3), which cannot be neglected when a reliable and efficient wireless-backhauled network is to be designed.

In order to maximize spectral efficiency and realize high-capacity links, complex modulation schemes are necessary, posing severe requirements in terms of local oscillator's phase noise so as to keep small EVM. Unfortunately, frequency synthesis becomes difficult as frequency gets higher, mainly due to the limited quality factor of reactive components, and a different strategy must be addressed to generate an E-band frequency reference.

A typical solution is to produce a lower frequency tone by means of a *PLL* and then pass it through a frequency multiplication stage, as shown in

---

[1]E-band falls in the $60-90GHz$ spectrum
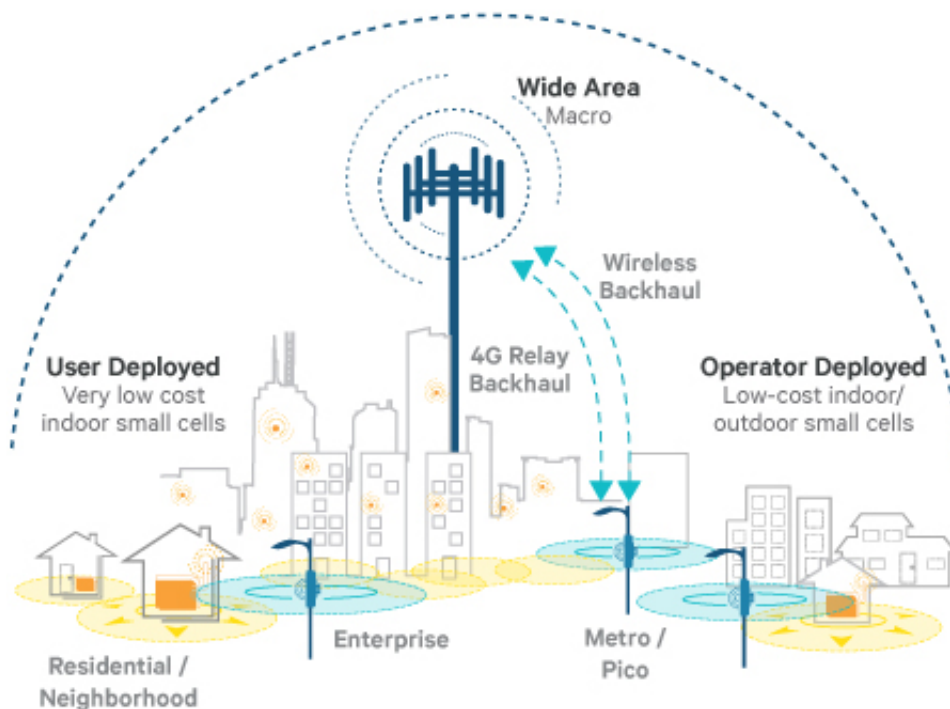
Figure 2: Micro-cells with fixed wireless backhaul links

fig. 4. This approach degrades phase noise by at lest $20\log_{10}(n)\ dB$ where n is the frequency multiplication factor [2].

This work is aimed to cover the procedure followed during the design of a $n = 4$ frequency multiplier taking as reference a $20GHz$ tone provided by a PLL, and the purpose is to correctly drive the input pads of a phase-shifter whose input S-Parameters are given. The shifter will then generate quadrature E-band signals, necessary in the I/Q stream modulation/demodulation. Requirements are on power and bandwidth ($P > 3dBm$ over $60 - 90GHz$). An E-band class-A power amplifier is also designed in order to satisfy power requirement. The implemented blocks are highlighted in fig. 5, and are intended to be part of an integrated E-band transceiver for millimeter-waves backhaul applications.
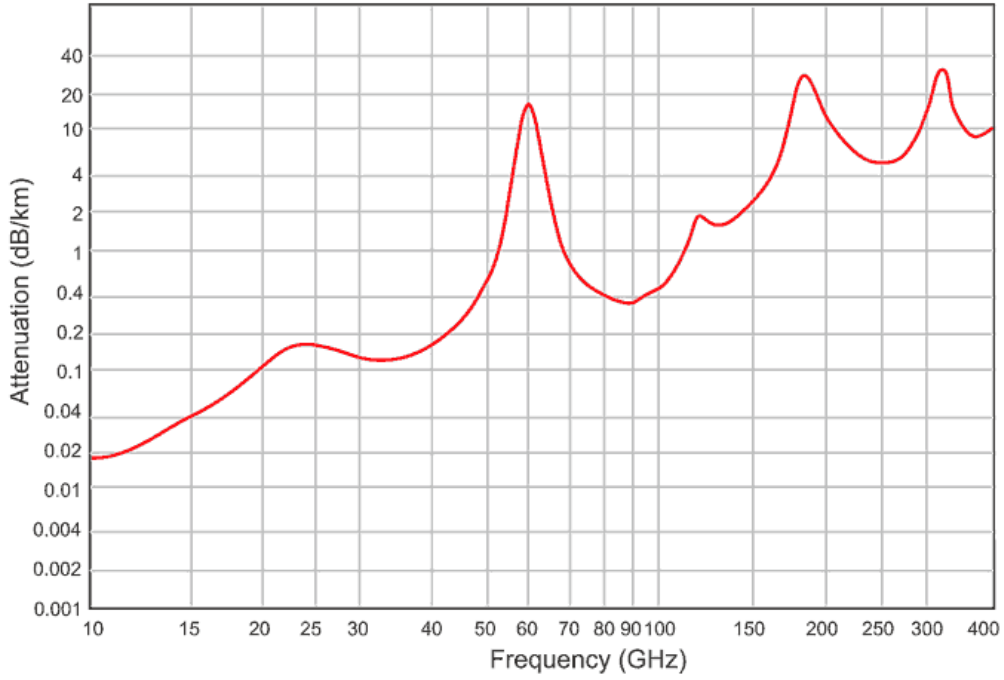
Figure 3: Oxygen attenuation over frequency
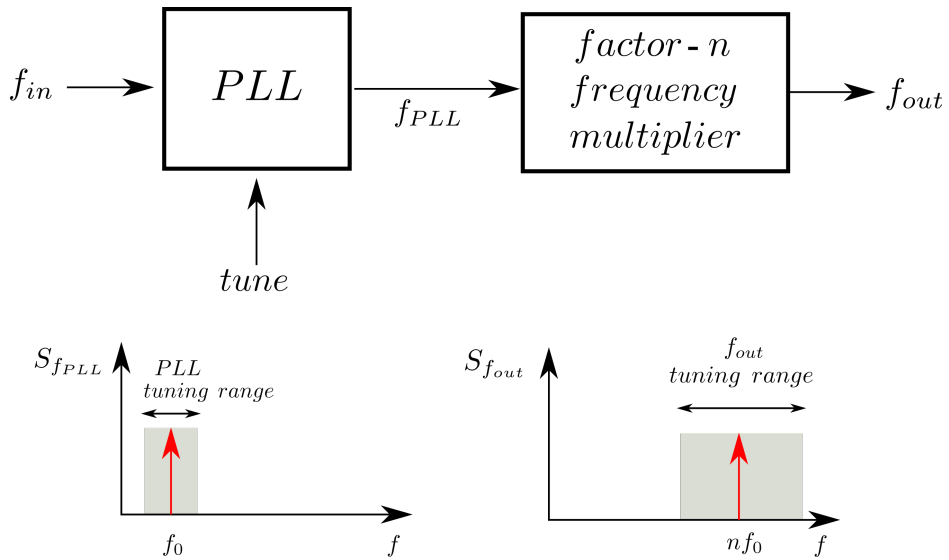
Figure 4: E-band tone generation through frequency multiplication
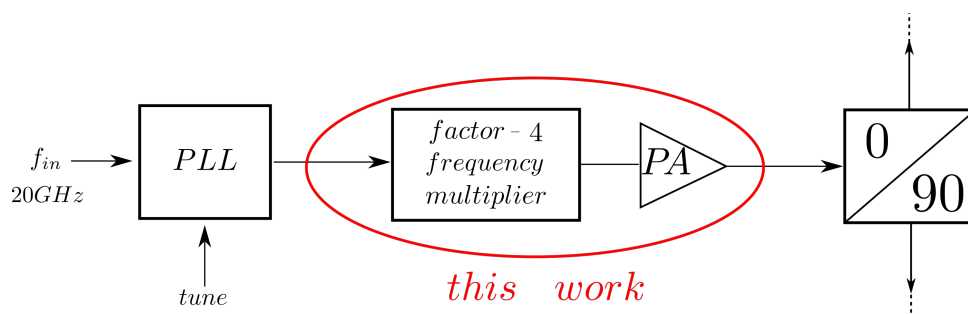
Figure 5: Block diagram of the designed circuit
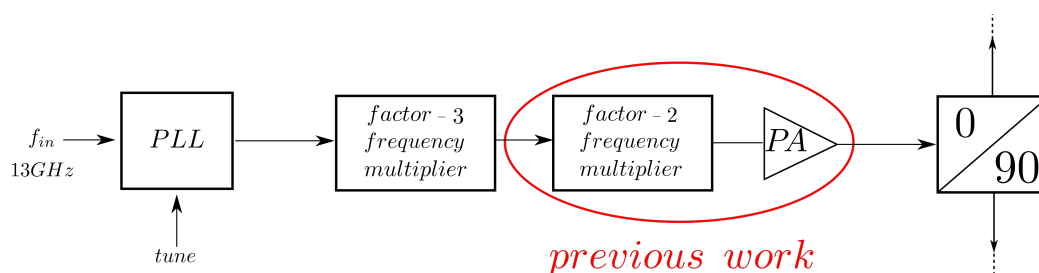
Figure 6: Block diagram of the previous redesign

This project comes after the design of a $n = 6$ frequency multiplier with an input reference at $13GHz$ and whose block diagram is reported in fig. 6. A x3 multiplier was used to feed a new x2 push-push stage and an E-band PA was added in order to reach the target power; these last two stages are almost identical to the one presented in this work, since output requirements were unchanged. For this reason, layout pictures are referred to the first version.

These studies were made at Politecnico di Milano as part of the TARANTO[2] European H2020 Project which targets to break the technological barriers to the development of next generation BiCMOS technology platforms.

---

[2]**T**owar**d**s **a**dvanced BiCMOS **n**ano**t**echnology platforms for RF and THz applicati**o**ns

Chapter 1

Matching networks

Impedance transformation is a classic problem in the design of high-frequency circuits. At RF, impedances are conventionally matched to $Z_0 = 50\Omega$, mainly for historical and constructive reasons related to cables [3]. For instances, Z_0 is the typical load of a PA, but the optimum resistance[1] of an amplifier is, in general, different, especially with technology scaling which requires lower supply voltages and increasing currents to deliver the same amount of power, thus continuously lowering the optimum load resistance R_{opt}. In other applications, instead, impedance transformation is required to achieve the desired impedance matching (e.g. conjugate-match, noise-match, etc...). Even in SoC, where the conventional impedance normalization to Z_0 is not necessary, since previous and following stages are known to the designer, inter-stage matching networks are required to optimize power transfer or satisfy different design constraints, such as VSWR minimization or gain-bandwidth enhancement.
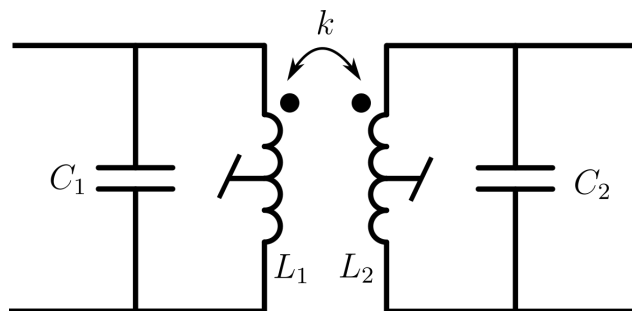
Figure 1.1: Doubly-tuned transformer matching network

1.1 Doubly-tuned transformers

In this work, magnetically coupled matching networks (fig. 1.1) have been chosen for different reasons:

- The use of transformers in differential signaling allows bias to be fed to the transistors through the center tap of the primary and secondary windings; while at first sight this may seem a minor point at RF, it should be noted that, in the 100 GHz's range, losses in decoupling capacitors become dominant, making difficult even DC isolation;

- They provide differential to single ended conversion which is typically required at the output of multiplier stages to drive balanced mixers;

- Lastly, a doubly-tuned transformer, compared to a single LC tank, exploiting a 4th order frequency response, can be used to overcome Bode-Fano limit that typically applies to second order resonators, allowing to achieve a broadband impedance transformation.

---

[1]see section 2.4
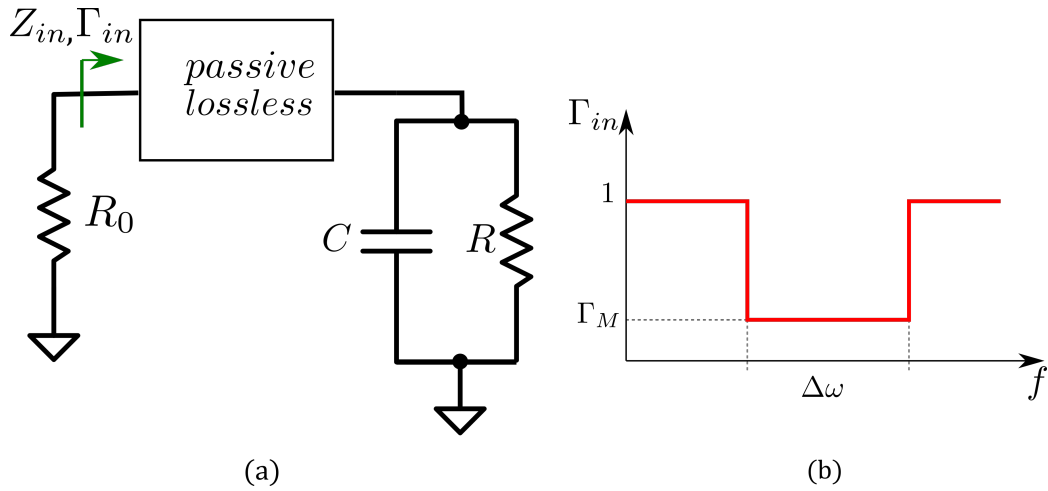
Figure 1.2: Filter for impedance transformation (a) and reflection coefficient (b)

1.2   Bode-Fano limit

We can model an amplifier as a transconductor with a parallel RC load, where C accounts both for load capacitance and transistor output capacitance. With a gain equal to $g_m R$ and a bandwidth limited to $\frac{1}{2\pi\ RC}$, gain-bandwidth product of the stage is:

$$GBW = \frac{g_m}{2\pi C} \tag{1.1}$$

In order to restore gain at high frequency, filters should be employed to resonate the parallel capacitance and realize impedance transformation over the desired bandwidth [4].

The simplest way to do so is to place a parallel L that resonates out the capacitance at the desired frequency. Unfortunately, this approach is by definition "narrowband" and cannot satisfy the requirements for a broadband amplifier. A natural question follows: is it possible to perform a perfect matching over a larger bandwidth?

Bode-Fano limit [5][6] answers this question. Given a filter [fig. 1.2 (a)] with a shunt RC load, it will show an input impedance Z_{in} and will have an input

reflection coefficient Γ_{in} which measures how close is the complex impedance Z_{in} to a resistive termination R_0 over the whole frequency range. Bode-Fano criterion states:

$$\int_0^\infty ln\left(\frac{1}{|\Gamma_{in}(\omega)|}\right) d\omega \leq \frac{\pi}{RC} \tag{1.2}$$

If we assume that the reflection coefficient Γin is equal to unity out of the band of interest, and equal to Γ_M within the band, as reported in fig. 1.2 (b), the (1.2) can be re-written as follows:

$$\Delta\omega \cdot ln\left(\frac{1}{|\Gamma_M|}\right) \leq \frac{\pi}{RC} \tag{1.3}$$

Looking at (1.3) we may immediately derive some considerations about impedance matching:

- A broader bandwidth can be achieved only at the expense of a higher in-band reflection coefficient, thus worsening matching performance;

- A perfect in-band match ($\Gamma_M = 0$) cannot be achieved unless $\Delta\omega = 0$;

- As R or C increase, the quality of the match ($\Delta\omega$ or $\frac{1}{\Gamma_M}$) must decrease. From this conclusion we derive that high-Q circuits are intrinsically harder to be matched than low-Q ones.

1.3 Beyond Bode-Fano: Gain-Bandwidth Enhancement

We should better clarify the concept of bandwidth and gain-bandwidth enhancement since we're working with networks of order higher than two. [7] introduces some useful definitions that can be summed up as follows:

- Average-Gain and Average-Gain-Bandwidth: for a given frequency range from ω_1 to ω_2, if an amplifier's pass band frequency response

exhibits some ripple around a gain level G, and areas of the ripple above and below G are equal, we can say that the amplifier has an average gain G and an average-gain-bandwidth of $\omega_2 - \omega_1$.

- Average-Gain Bandwidth Enhancement Ratio: Consider two amplifiers characterized by the same transconductor cell and the same load capacitor. One amplifier incorporates a bandwidth enhancing passive network, while the other uses a simple resistive load. Assuming the average-gain of the enhanced amplifier to be equal to the DC gain of the resistive-loaded amplifier, the ratio of the average-gain-bandwidth of the former and the -3 dB bandwidth of the latter is defined as average-gain's bandwidth-enhancement ratio.

As it is shown in [8], one of the main limitations of an amplifier's bandwidth is the parasitic capacitance at the output node that reduces output impedance as frequency grows. Gain-bandwidth product of an amplifier can be then increased if we're able to retain a uniform output impedance over a wider frequency range. This can be achieved if we introduce more complex loads, which can be represented as 2-ports networks connected at the output of the amplifier. We will exploit networks of order higher than two to achieve flat bands. We can now observe that, doing so, the transistor output capacitance, called C_1, and load capacitance, C_2, appear isolated and separated by the impedance-transformation network. Bode, in [5][2], showed that this class of matching is able to increase the gain-bandwidth product of a stage and mathematically proved that an upper limit in the enhancement exists. The maximum gain-bandwidth enhancement ratio achievable with 2-ports output matching networks, as discussed above, is:

$$GBWEN_{2-p,max} = \frac{\pi^2}{2} \tag{1.4}$$

for the particular case in which $C1 = C2 = C/2$.

-----

[2]see chpt. 17
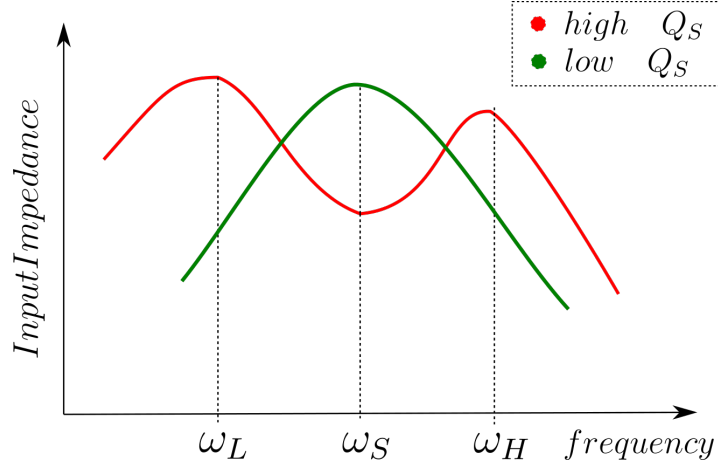
Figure 1.3: General case of doubly-tuned transformer input impedance

1.4 Broadband impedance transformation

In [9], the authors deeply investigated the behavior of doubly-tuned transformer networks, which can be thought as the combination of two resonant tanks L_1C_1 and L_2C_2 which are magnetically-coupled through the coupling coefficient k (fig. 1.1).

One of the most interesting features of these networks is the possibility to achieve an impedance transformation over a wide band, much wider that what allowed by 2nd order LC tanks. It is shown that, looking at the behavior of the input impedance of a doubly-tuned transformer over frequency, we can define three different regions (fig. 1.3) characterized by the center frequencies ω_L, ω_S and ω_H, and the network can be well approximated with equivalent parallel LC tanks at $\omega_{L,H}$ and with an equivalent series tank at ω_S. A network quality factor was introduced:

$$Q_S = \frac{R_L}{\sqrt{\frac{L_2}{C_2}}} \cdot \frac{1}{\sqrt{1 - k^2}} \tag{1.5}$$

R_L is the load resistance, responsible for the loading of the network which causes a quality factor reduction. It was shown that the input impedance of

the stage presents two peaks in correspondence of $\omega_{L,S}$ and a valley at ω_S. For this to happen it must be verified:

$$Q_S \gg 1 \tag{1.6}$$

If the (1.6) does not hold, instead, R_L heavily loads the network and a single peak is present at ω_S; in this case the broadband behavior is not achievable.

Our goal is to equalize the response of the network and realize a nearly-constant transimpedance over the band of interest. If we call R' the transformed resistance shown by the network at primary side, we want to impose:

$$R'_L = R'_S = R'_H \tag{1.7}$$

so the input impedance will be uniform at ω_L, ω_S and ω_H, respectively.

We can introduce a parameter ξ defined as:

$$\xi = \frac{L_2 C_2}{L_1 C_1} \tag{1.8}$$

For the (1.7) to be verified, it must be simultaneously true:

$$\xi = 1 \quad and \quad |k| \cdot Q_S = 1 \tag{1.9}$$

Once (1.9) holds, the impedance transformation ratio R_L/R' is set by the transformer turn ratio $n = L_2/L_1$:

$$\sqrt{\frac{R_L}{R'}} = n \tag{1.10}$$

For values of ξ around unity, the positions of the parallel resonances are then at:

$$\omega_L{}^2 = \frac{\omega_1{}^2}{1 + |k|} = \frac{\omega_2{}^2}{1 + |k|} \quad and \quad \omega_H{}^2 = \frac{\omega_1{}^2}{1 - |k|} = \frac{\omega_2{}^2}{1 - |k|} \tag{1.11}$$

where ω_1 and ω_2 are the resonant frequencies of the unloaded $L_1 C_1$ and $L_2 C_2$ tank, respectively.
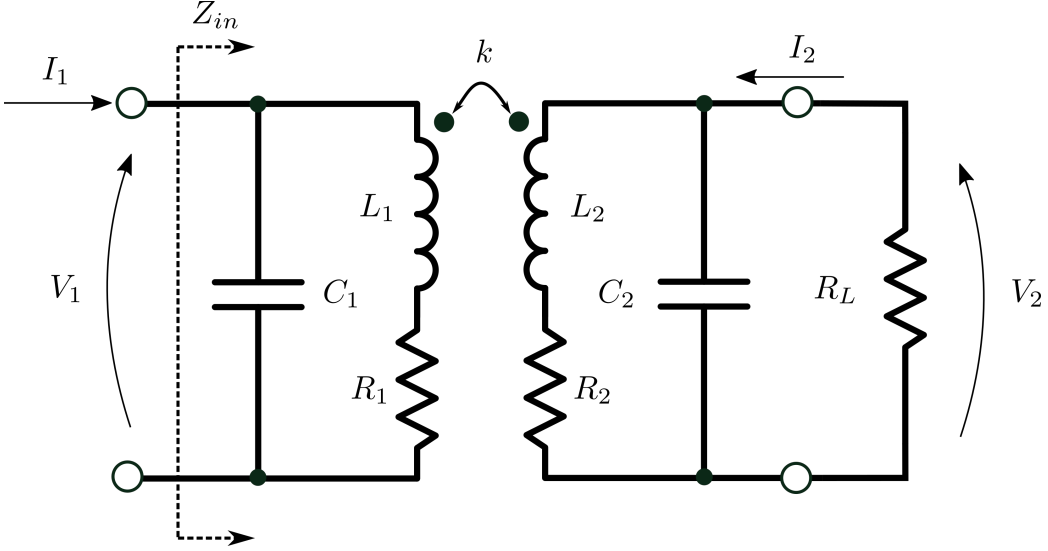
Figure 1.4: Doubly-tuned transformer matching network with inductor losses

By rearranging (1.11), we derive:

$$k = \frac{\omega_H{}^2 - \omega_L{}^2}{\omega_H{}^2 + \omega_L{}^2} \tag{1.12}$$

Thus we immediately observe that, when flat bands are targeted, the coupling factor k sets the bandwidth. Then the other parameters of the network can be found relying on (1.9) and (1.10).

Note that, so far, losses in reactive elements have been neglected. A more appropriate model of the matching network should consider the inductors' limited quality factor (fig. 1.4); Again in [9], the following relation was derived:

$$\frac{R_{eq,L}(\omega_L)}{R_{eq,H}(\omega_H)} = \frac{1 + |k|}{1 - |k|} > 1 \tag{1.13}$$

where $R_{eq,L,H}$ indicate the resistors of the parallel-equivalent tank at $\omega_{L,H}$, respectively. These resistors account for the losses introduced by the network, and, looking at the (1.13), we can conclude that the high frequency peak suffers from a more severe loading, thus the impedance will show an in-band frequency roll-off, and it will be more evident as the quality factors of inductors decrease. The only way to restore flatness is to pre-emphasize the

response of the network, and this approach is followed in both [4] and [9]. This is done by increasing the parameter ξ to values greater than unity.

1.4.1 E-Band matching network

In this section we will design a broadband impedance matching network based on doubly-tuned transformers.

The network will be employed in a E-band transceiver architecture, so the choice of $\omega_L = 2\pi 55 GHz$ and $\omega_H = 2\pi 95 GHz$ should be able to include all the frequencies of interest plus a margin on both high and low side.

The (1.12) gives the magnetic coupling coefficient which is needed to achieve the desired bandwidth. It turns out $|k| \simeq 0.5$. Due to (1.9), follows $Q_S = 2$. The (1.11) can be used to derive the natural frequencies of the primary and secondary resonators ω_1 and ω_2, giving

$$\omega_1 = \omega_2 = \omega_L \cdot \sqrt{1 + |k|} = \omega_H \cdot \sqrt{1 - |k|} \tag{1.14}$$

By combining (1.5) and the well know expression for the resonance of a LC network, $w_0 = 1/\sqrt{LC}$, we derive the following expression for the secondary inductor:

$$L_2 = \frac{R_L}{\omega_2 Q_S} \cdot \frac{1}{\sqrt{1 - k^2}} \tag{1.15}$$

Assuming that the load resistor R_L is equal to 50Ω and the required resistance at primary side is $R' = 50\Omega$, the turn ratio is given by (1.10) and all the parameters of the network are derived as listed in table 1.1.

L_1	L_2	C_1	C_2	k
68.2pH	68.2pH	81.65fF	81.65fF	0.5

Table 1.1: Parameters of the lossless matching network

The network designed above has been simulated and the corresponding tran-simpedance is reported in fig. 1.5 for various values of inductor quality
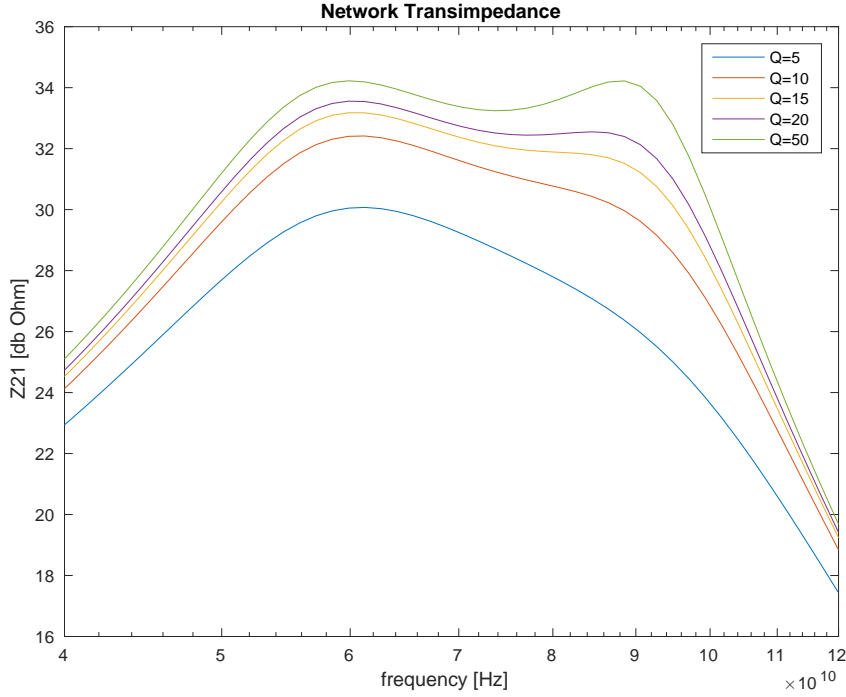
Figure 1.5: Z_{21} of the matching network for different Q values, $\xi = 1$

factors at the center frequency. We observe a rapid compression of the high-frequency peak as losses increase and the roll-off is non-negligible for values of Q in the $10 - 20$ range, which characterize our integrated transformers.

Fig. 1.6 shows the effect of ξ on the transimpedance of the network for a given value of the Q factor at $80GHz$. As expected, the action on ξ is able to recover the high-frequency peak. We further observe a slight bandwidth shift, since the (1.11) is strictly valid for $\xi = 1$, only. If bandwidth needs to be adjusted, the designer can take into account the effect of ξ by modifying the initial values of ω_L and ω_H. Note that the same ξ can be obtained by acting on both capacitors and inductors. In order not to alter the impedance transformation ratio, it is preferable to adjust capacitances. Values of ξ greater than unity must be adopted to emphasize the high-frequency peak, thus C_2 should be increased or C_1 decreased.

The quality of the impedance transformation can be evaluated looking at
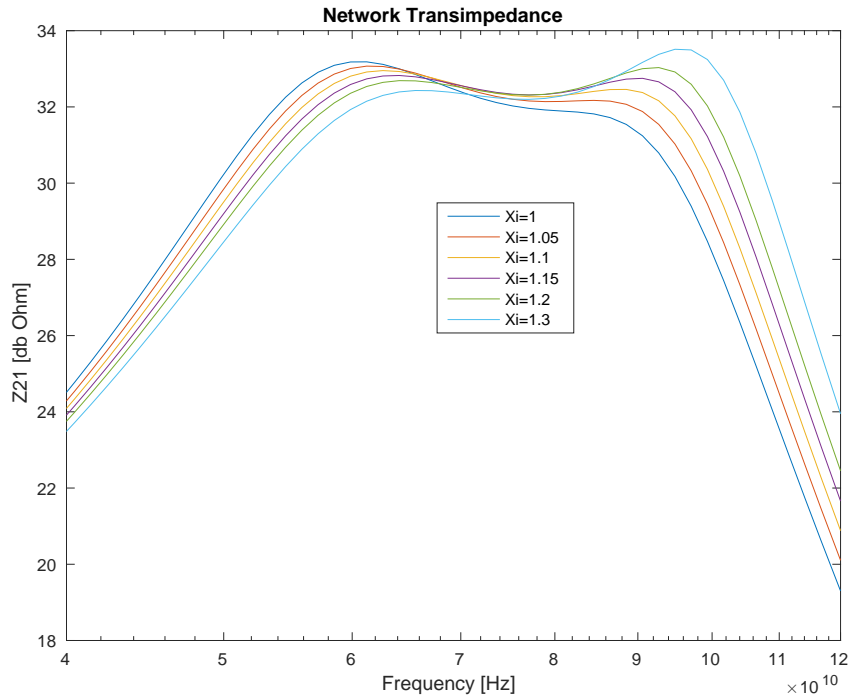
Figure 1.6: Z_{21} of the matching network for different values of ξ; Q=15

fig. 1.7, where the S_{11} has been reported. The relatively low distance to the center of the Smith chart, normalized to 50Ω, over the entire bandwidth suggests that a good impedance matching is achieved.

The final values of the proposed network are reported in table 1.2. The reduction of C_1, setting $\xi = 1.15$, allowed to restore flatness.

L_1	L_2	C_1	C_2	k
68.2pH	68.2pH	71fF	81.65fF	0.5

Table 1.2: Parameters of the lossy matching network
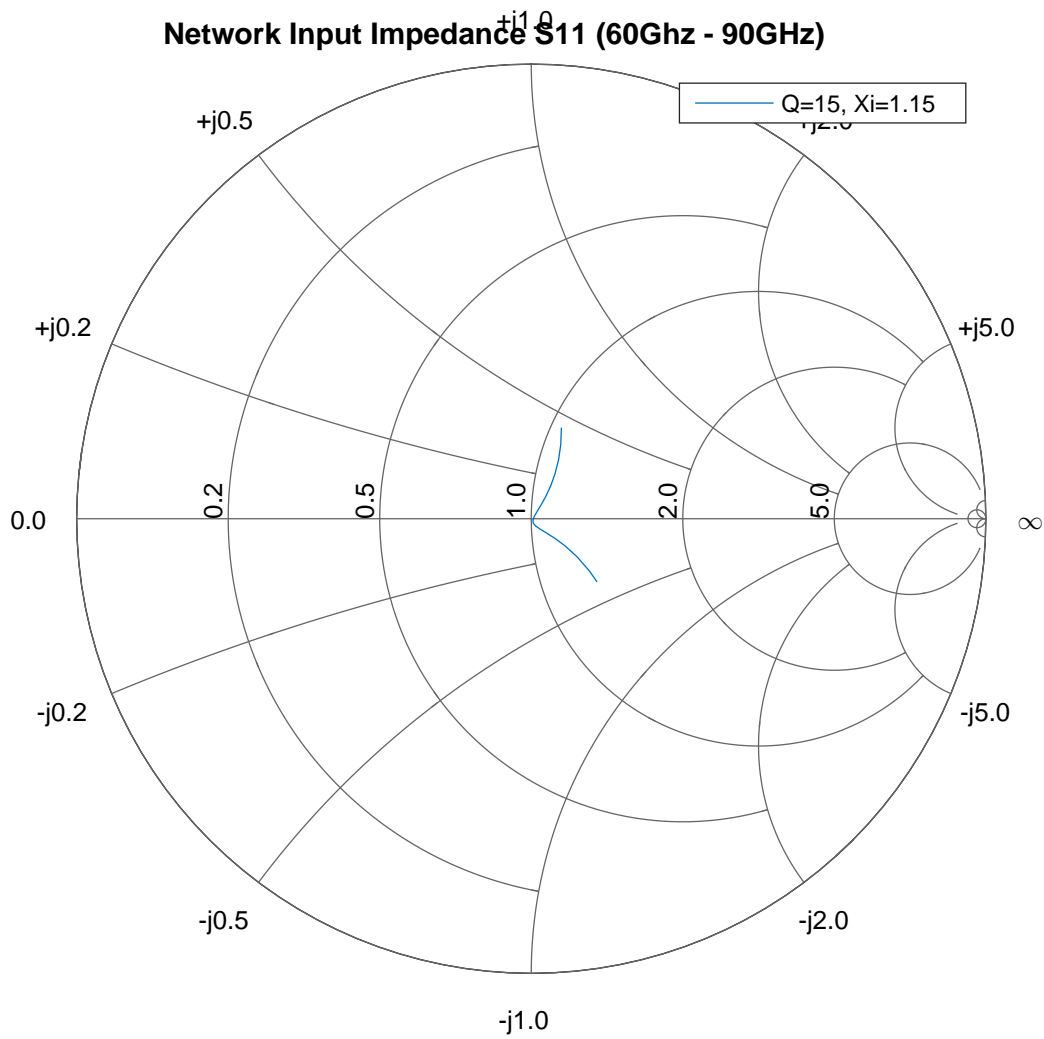
Figure 1.7: S_{11} of the proposed matching network in the $60 - 90GHz$ band, $Z_0 = 50\Omega$

Chapter 2

Power amplifier

2.1 Conjugate match and loadline match

The theory of conjugate match states that, given a generator with its output resistance, maximum power is carried to the load when the load resistance is set equal to the real part of the generator impedance, assuming that any reactive component has been resonated out [fig. 2.1 (a)]. However, this theoretical result does not take into account that any real generator will be subject to physical limitations while delivering power. In fact, we have to consider the voltage swing that the generator can sustain at its terminals and the maximum current it can provide. Let us take for instance a current generator with an output resistance of 100 Ohms which can supply 1 Amp. Applying the conjugate match theorem, a load of 100 Ohms should be selected to transfer the maximum power, but we would then observe 50 Volts across its terminals. If the transistor weren't able to sustain such a voltage swing, the power delivered to the load would dramatically decrease. In order to utilize the full voltage-current capability of a transistor, a lower value of load resistance would need to be selected. The optimum value, called R_{opt}, is defined as:
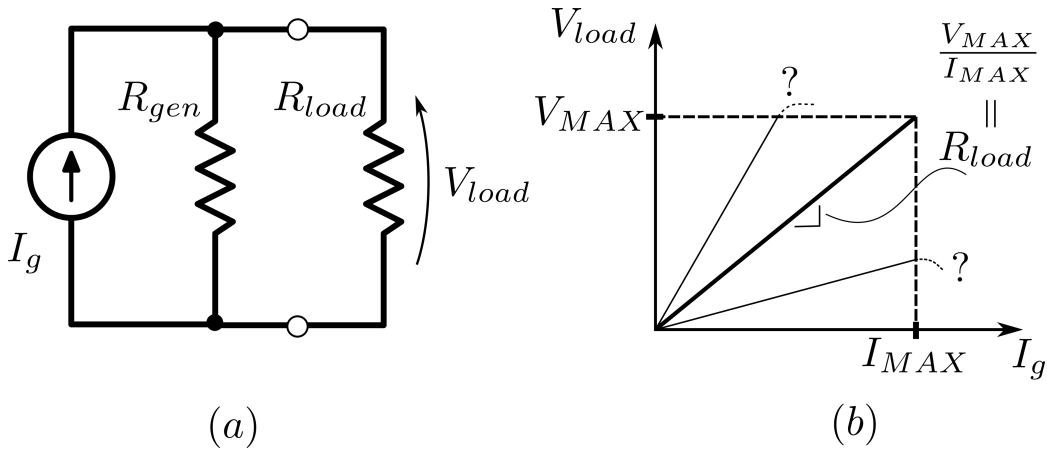
Figure 2.1: Conjugate match and loadline match

$$R_{opt} = \left(\frac{V_{max}}{I_{max}} \right) \qquad (2.1)$$

assuming that $R_{gen} \gg R_{opt}$.

This procedure of load selection is referred as "loadline match" [10] or "power match" [fig. 2.1 (b)] and we may conclude that it will be adopted whenever conjugate match brings active elements out of their dynamic range, which is the typical case when power generation is a goal.

2.2 Power gain vs. output power trade-off

While loading an amplifier with R_{opt} maximizes the transferred power, we may ask ourselves what happens to power gain in such a situation. Assume we take two identical stages and connect one to a complex conjugate load and the other to a power matched load. Following the discussion above, we'll expect, for the same DC power consumption, higher gain in the first amplifier, due to higher load resistance, but lower saturated power. It's clear, then, that power output has been increased in the second amplifier at the expense of power gain. The compression curve for the two stages is reported in fig. 2.2, where the ideal characteristics are dashed lines. Their
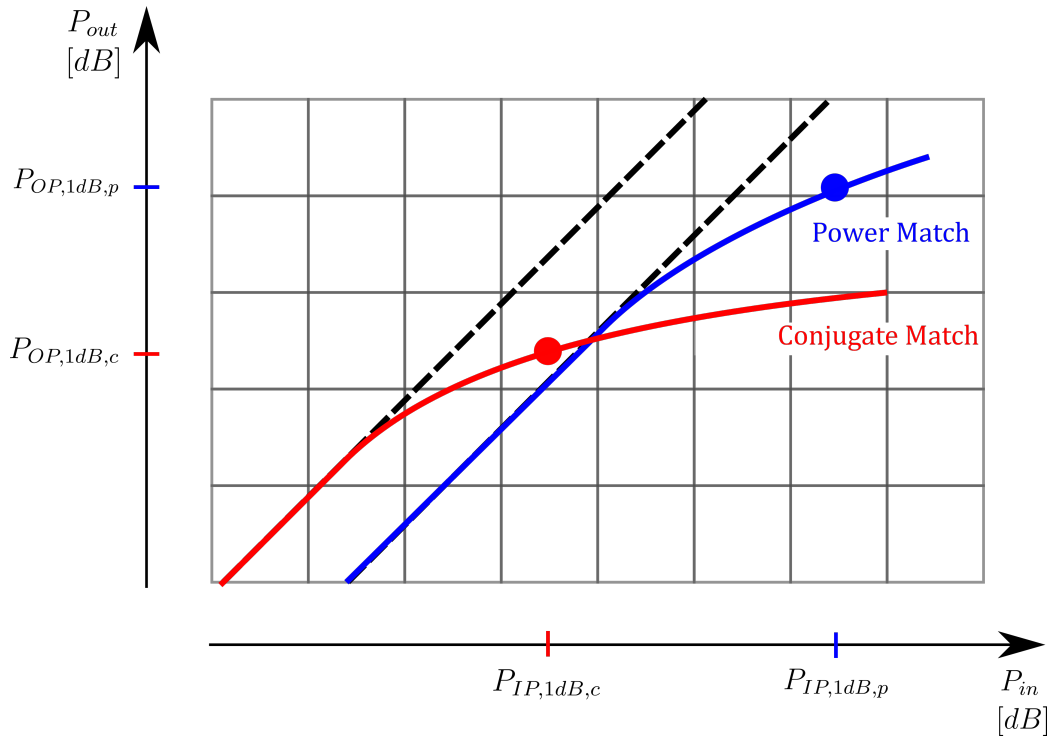
Figure 2.2: Compression curves of two amplifiers with different load matching

slopes equal to 1dB/dB indicate that the amplifiers are linear. When the output power approaches saturation, gain compression occurs and the slopes decrease. At that point, for an extra input power level of 1dB, the output increases less than 1dB. When the difference between ideal and actual output power reaches the value of 1dB, there we find the "1dB compression point", which can be indifferently referred to input or output. The compression points are highlighted in the figure as dots. Note that the angular coefficient of a line on a dB-dB plot is only related to linearity. Gain, instead, can be extracted looking at the values of output and input power for a specific point along the lines.

Based on R_{opt} definition, it is clear that in correspondence of the peak power we are well above the boundary of the linear range of an active device. In fact, any addiction of input power would not translate into output power

increase. We may conclude that loading a device with its R_{opt} and pushing it above its linear range implies a reduced gain and a high level of distortion, with output power approaching the saturated value P_{sat}. Furthermore, a designer may size an amplifier for a target gain, and this condition will, in general, lead to a target load different than R_{opt}. This means that one can load an amplifier for maximum power at the expense of power gain, and vice-versa. Thus a power-gain-output-power trade-off exists, since efficiency peaks at P_{sat} and rapidly degrades at back-off, and power gain decreases as output power approaches P_{sat}.

2.3 Common-Emitter cascode configuration

The common emitter transistor configuration loaded by a common base transistor (CB, acting as current buffer) presents two main advantages with respect to a single-transistor common emitter amplifier: Miller effect mitigation (i) and reverse isolation improvement (ii). The two topologies can be compared looking at figure 2.3.

(i) The first benefit can be easily understood since voltage gain between Q1 base and Q1 collector $G_{v,cb,1}$ is $-g_{m,1}R_L$ and $-g_{m,1}/g_{m,2} \cong -1$ for the single CE and for the cascode, respectively. These gains are strictly related to the Miller magnification factor $(1 - G_{v,cb,1})$ acting on $C_{bc,1}$ and impacting on the low frequency pole of the circuit. Note that connecting Q1 collector to a low impedance node allows bandwidth expansion thanks to Miller effect mitigation, while leaving unaltered the overall input-to-output voltage gain.

(ii) The second improvement can be discussed noticing that, at high frequency, collector-base parasitic capacitance of the output transistor shunts the two nodes. It is evident that, in the CE topology, this shunt creates a direct current path from output to input, thus destroying reverse isolation performance. This is unwanted since an ideal device should be unilateral, allowing power flow from input to output, but not vice-versa. The output is
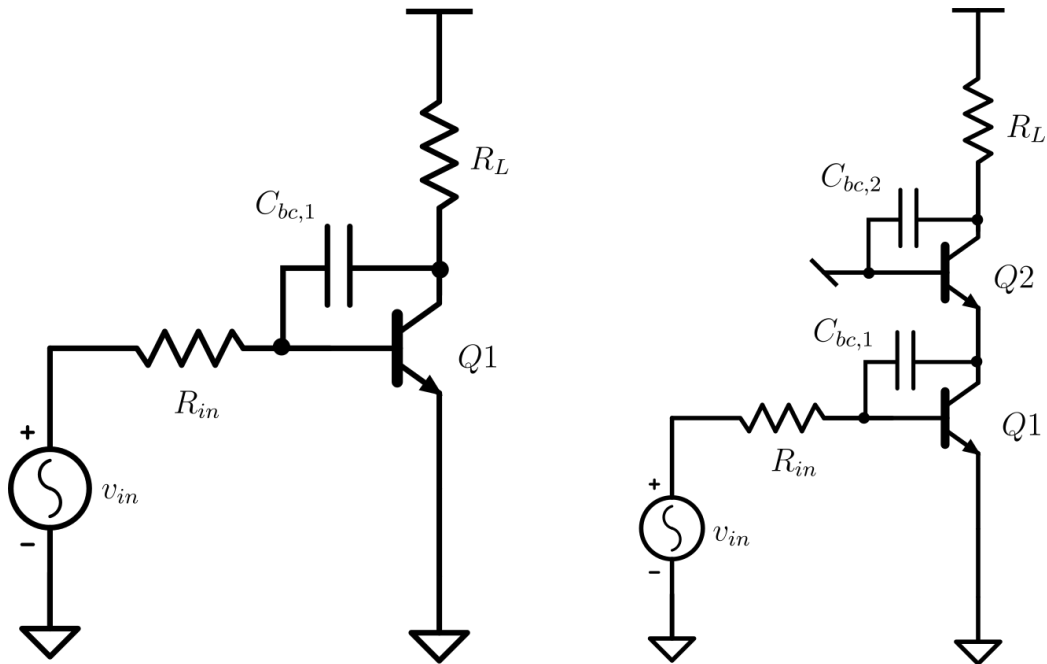
Figure 2.3: CE amplifier and CE+CB cascode amplifier

also characterized by high power level and unwanted back-injection, which consists in a local feedback mechanism, can cause potentially harmful power reflection to the previous stage, eventually pushing the device into unstable regions. In the cascoded CE stage, instead, the output parasitic $C_{bc,2}$ shunts the load to ground, not impairing reverse isolation.

2.4 PA quasi-linear study

Following a quasi-linear discussion [11], during large-signal operation, a typical case for a power amplifier, a condition on the output collector voltage exists, in order to guarantee the CB transistor not to fall into saturation, with collector-base junction forward-biased. Note that, thanks to the presence of the inductor, the voltage swing is symmetrical with respect to Vdd.

| (a) | (b) |
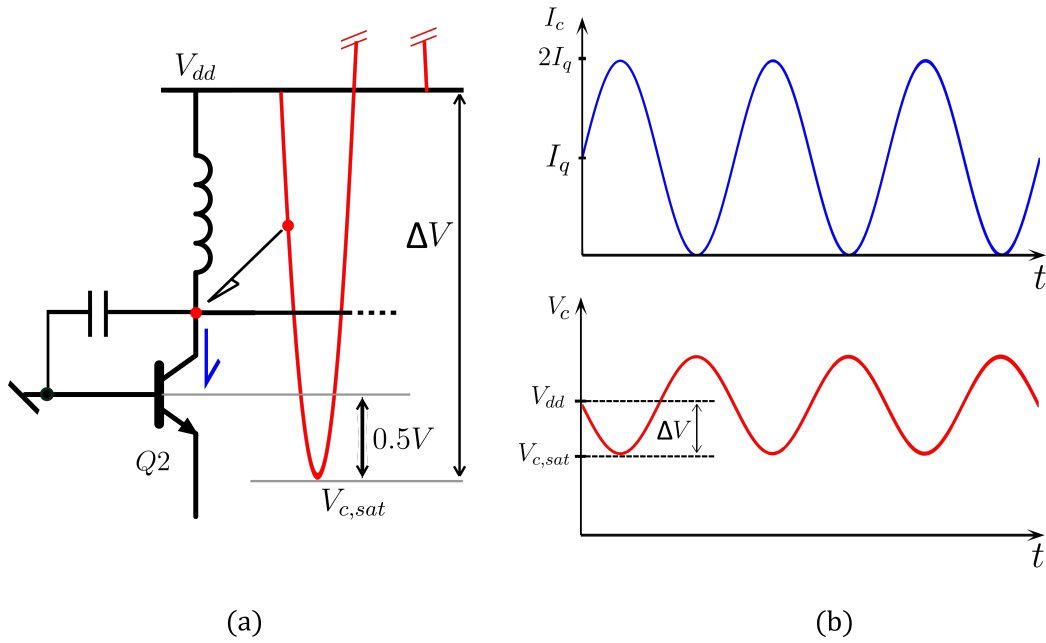
Figure 2.4: Collector waveforms with optimum resistor as load impedance

The optimum power[1], obtained when the current swing is maximum, is equal to:

$$P_{opt} = \frac{\Delta V \cdot \Delta I}{2} = \frac{\Delta V \cdot I_q}{2} \tag{2.2}$$

where ΔV is the oscillation amplitude at the collector node V_C and I_q is the average value of the collector current I_C of the BJT.

Thus, the optimum resistance is:

$$R_{opt} = \frac{\Delta V}{I_q} \tag{2.3}$$

and it can be expressed in terms of optimum power as follows:

$$R_{opt} = \frac{\Delta V^2}{2P_{opt}} = \frac{2P_{opt}}{I_q{}^2} \tag{2.4}$$

The maximum achievable collector efficiency, defined as maximum output

---

[1]We will indifferently use the term optimum (P_{opt}) or saturated (P_{sat}) to describe the power level at which efficiency peaks when the amplifier is loaded with R_{opt}.
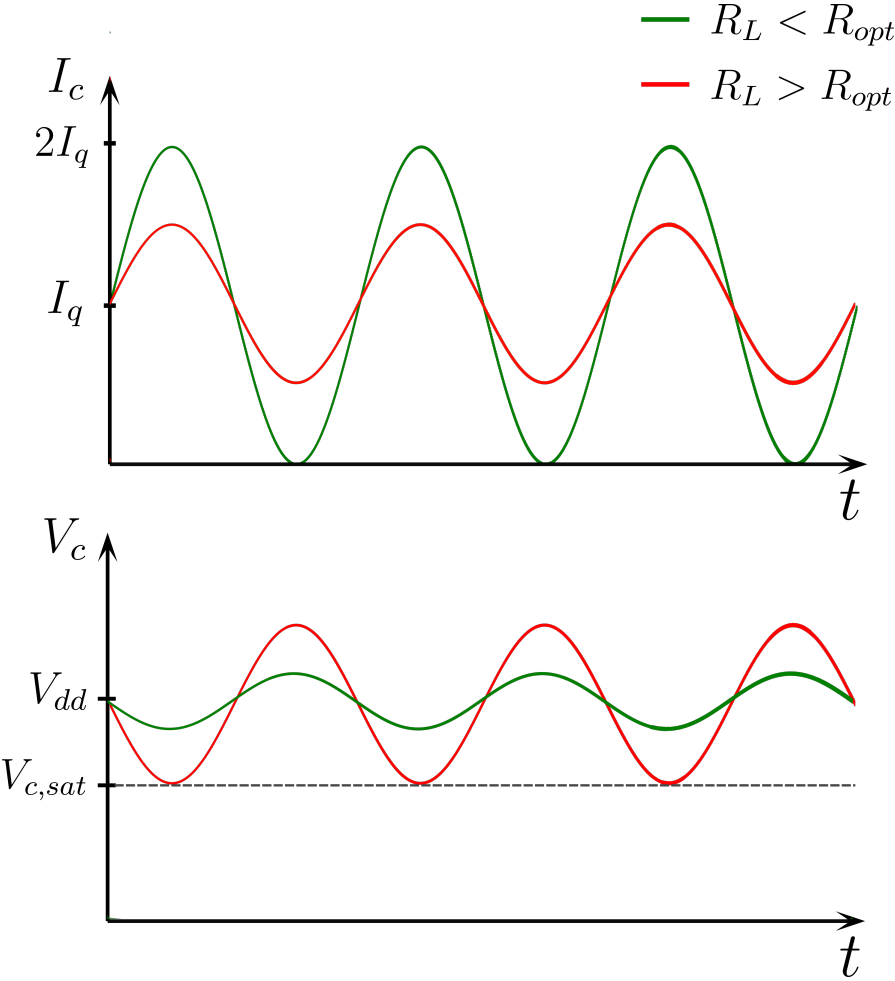
Figure 2.5: Collector waveforms with different load resistors

power versus DC power consumption, can be derived:

$$\eta_{c,max} = \frac{P_{opt}}{P_{DC}} = \frac{\Delta V \cdot I_q}{2} \cdot \frac{1}{V_{dd} \cdot I_q} = \frac{\Delta V}{2V_{dd}} \tag{2.5}$$

Equation 2.5 reveals that collector efficiency only depends on the ratio of the voltage swing over the voltage supply. This confirms that maximum efficiency is reached next to power saturation, where ΔV is the absolute maximum allowed.

However, the most important parameter to quantify efficiency of the stage is power-added efficiency (PAE). Its use is preferred to η_c since it takes into account that not all the generated RF power comes from DC power conversion, in fact a fraction of it is absorbed from the input source:

$$PAE = \frac{P_{RF} - Pin}{P_{DC}} \tag{2.6}$$

and it can be linked to collector efficiency using the linear input-to-output-power-gain G_P as follows:

$$PAE = \frac{P_{RF} - Pin}{P_{DC}} = \frac{P_{RF}\left(1 - \frac{1}{G_P}\right)}{P_{DC}} = \eta_c \left(\frac{G_P - 1}{G_P}\right) < \eta_c \tag{2.7}$$

Note that, in any practical case, not all the bias current will be switched on and off, thus $\Delta I < I_q$. We can therefore introduce a parameter:

$$\lambda = \frac{\Delta I}{I_q} < 1 \tag{2.8}$$

Consequently, the optimum load becomes:

$$R_{opt}\prime = \frac{\Delta V}{\Delta I} = \frac{R_{opt}}{\lambda} \tag{2.9}$$

Accordingly, P_{opt} is reduced by a factor λ, which directly impacts on the power efficiency that shrinks by λ as well.

When the stage is loaded with a resistance R_L different from R_{opt}, two cases can be identified:
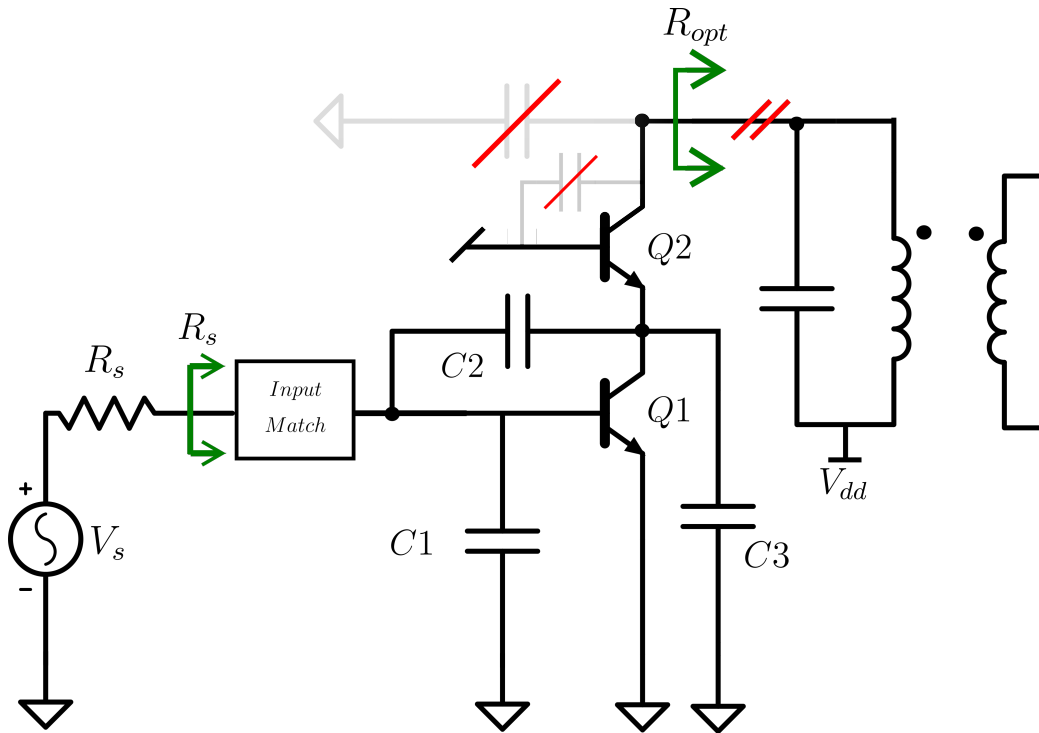
Figure 2.6: Cascoded PA with output power match and input conjugate match

- If $R_L < R_{opt}$ the stage is said to be "current limited"; not all the available voltage swing will be exploited and if the input was further increased, the current waveform would clip and the amplifier would be leaving class-A, being the conduction angle below 360°.

- If $R_L > R_{opt}$ the stage is "voltage limited" since the current budget cannot be fully exploited due to voltage limitations on the collector node.

The waveforms corresponding to the two above discussed cases are reported in fig. 2.5. Clearly, both situations produce an output power reduction which depends on how the load resistance is far or close to R_{opt}, impacting directly on power efficiency.

2.5   PA power gain

In this section, we will analyze the power gain of the cascoded PA (fig. 2.6).[2]
Note that, since doubly-tuned transformers will be employed, Q2 collector-
substrate and collector-base stray capacitances can be absorbed by the pri-
mary side of the output matching network, which is supposed to present a
real impedance equal to R_{opt} at the collector of Q2. The output capacitance
is then de-embedded from the stage, thus simplifying the discussion. At the
input side, instead, conjugate match is assumed in order to maximize the
power transferred from the source generator to the PA input.

Different formulations of power gain exist, but the most useful is the
Transducer Power Gain, defined as the power delivered to the load over the
power available from the source:

$$G_T = \frac{P_L}{P_{AVL}} \qquad (2.10)$$

Based on the assumption that the impedance at the collector of Q2 is real
and equal to R_{opt}, the power at the output node is defined once voltage or
current are known, and is equal to:

$$P_L = \frac{v_{out}^2}{2R_L} = \frac{i_{out}^2 R_L}{2} \qquad (2.11)$$

Q1 input, instead, shows a complex impedance which is transformed into a
resistance Rs matched to the input by the input matching network. On the
generator side, the available power is:

$$P_{AVL} = \frac{v_s^2}{8R_s} \qquad (2.12)$$

being v_s the voltage applied by the generator and R_S its series resistance.
If the input matching network is lossless, all the available power at the gener-
ator side is assumed to be transferred to the amplifier. The equivalent input

___

[2]A similar discussion is followed in [2], p. 563.
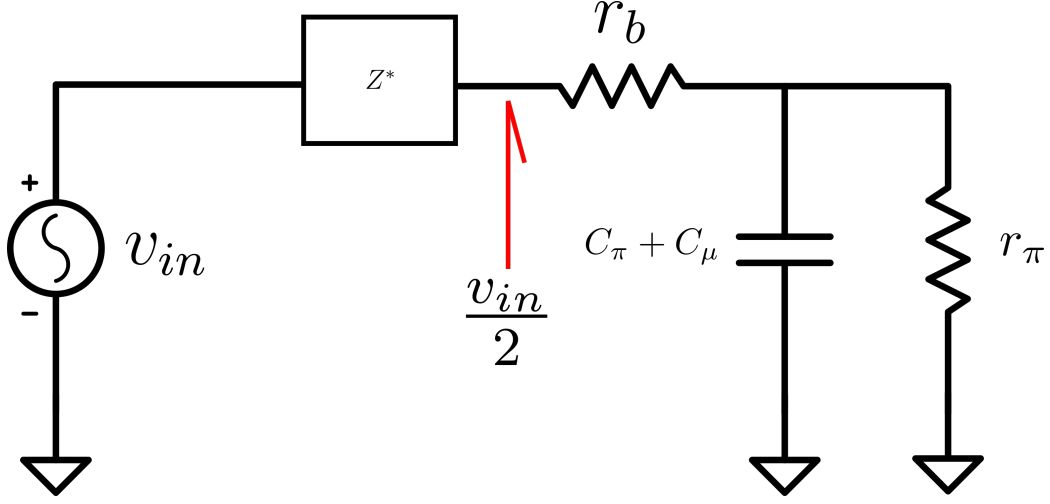
Figure 2.7: CE input impedance and its conjugately-matched input generator

impedance shown by Q1 is reported in fig. 2.7 together with its conjugately-matched input generator. The active power injected into the device is related to the fraction of input voltage falling on the real part of input impedance. The voltage v_π across resistor r_π is found by circuit inspection and is equal to:

$$v_\pi = \frac{v_{in}}{2} \cdot \frac{r_\pi}{r_b + r_\pi} \cdot \frac{1}{1 + s(C_\pi + C_\mu)(r_b//r_\pi)} \tag{2.13}$$

The voltage across r_b, given by $(v_{in}/2) - v_\pi$, can be written as:

$$v_b = \frac{v_{in}}{2} \cdot \frac{r_b}{r_b + r_\pi} \cdot \frac{1 + s(C_\pi + C_\mu)\frac{(r_b//r_\pi)(r_b+r_\pi)}{r_b}}{1 + s(C_\pi + C_\mu)(r_b//r_\pi)} \tag{2.14}$$

It is convenient to simplify eqq. (2.13) and (2.14) since $r_b << r_\pi$, giving:

$$v_\pi \cong \frac{v_{in}}{2} \cdot \frac{r_\pi}{r_b + r_\pi} \cdot \frac{1}{1 + s(C_\pi + C_\mu)r_b} \tag{2.15}$$

$$v_b \cong \frac{v_{in}}{2} \cdot \frac{r_b}{r_b + r_\pi} \cdot \frac{1 + s(C_\pi + C_\mu)r_\pi}{1 + s(C_\pi + C_\mu)r_b} \tag{2.16}$$

The power dissipated on the two resistors is:

$$P_{r_\pi} = \frac{|v_\pi|^2}{2r_\pi} = \left(\frac{|v_{in}|}{2} \cdot \frac{1}{(r_b + r_\pi)|1 + s(C\pi + C_\mu)r_b|} \right)^2 \cdot \frac{r_\pi}{2} \tag{2.17}$$

$$P_{r_b} = \frac{|v_b|^2}{2r_b} = \left(\frac{|v_{in}|}{2} \cdot \frac{1}{(r_b + r_\pi)|1 + s(C\pi + C_\mu)r_b|} \right)^2 \cdot \frac{r_b|1 + s(C_\pi + C_\mu)r_\pi|^2}{2} \tag{2.18}$$

Summing (2.17) and (2.18) we get the overall power sunk from the signal generator:

$$P_{bjt,in} = \frac{v_{in}^2}{8} \cdot \frac{1}{(r_b + r_\pi)^2|1 + s(C_\pi + C_\mu)r_b|^2} \cdot \left(r_b|1 + s(C_\pi + C_\mu)r_\pi|^2 + r_\pi \right) \tag{2.19}$$

Given an input voltage v_{in}, output current is linked through the transconductance of the stage:

$$i_{out} = g_{m,1}v_\pi \tag{2.20}$$

The expression can be plugged into (2.11) to get output power. After some manipulations, the transducer power gain of the stage is found:

$$G_T = \frac{(g_{m,1}r_\pi)^2 R_L}{r_b(1 + \omega^2(C_\pi + C_\mu)^2 r_\pi^2) + r_\pi} \tag{2.21}$$

We want now to simplify the expression to gain some insight about the parameters affecting the G_T of the device. We can easily neglect the 1 at the denominator since the product $(C_\pi + C_\mu)r_\pi$ accouns for the current gain dominant pole which falls in the MHz range and is responsible for the bipolar cutoff-frequency. We thus obtain:

$$G_T = \frac{g_{m,1}{}^2 r_\pi{}^2 R_L}{r_\pi + \omega^2(C_\pi + C_\mu)^2 r_\pi{}^2 r_b} \cong \frac{g_{m,1}{}^2 R_L}{\omega^2(C_\pi + C_\mu)^2 r_b} \tag{2.22}$$

Remembering the definition of cutoff-frequency, defined as the frequency for which the current gain of the transistor falls to unity, equal to

$$\omega_t = \frac{g_m}{(C_\pi + C_\mu)} \tag{2.23}$$

we can rewrite the transducer power gain as follows:

$$G_T = \frac{R_L}{r_b} \cdot \left(\frac{\omega_t}{\omega} \right)^2 \tag{2.24}$$
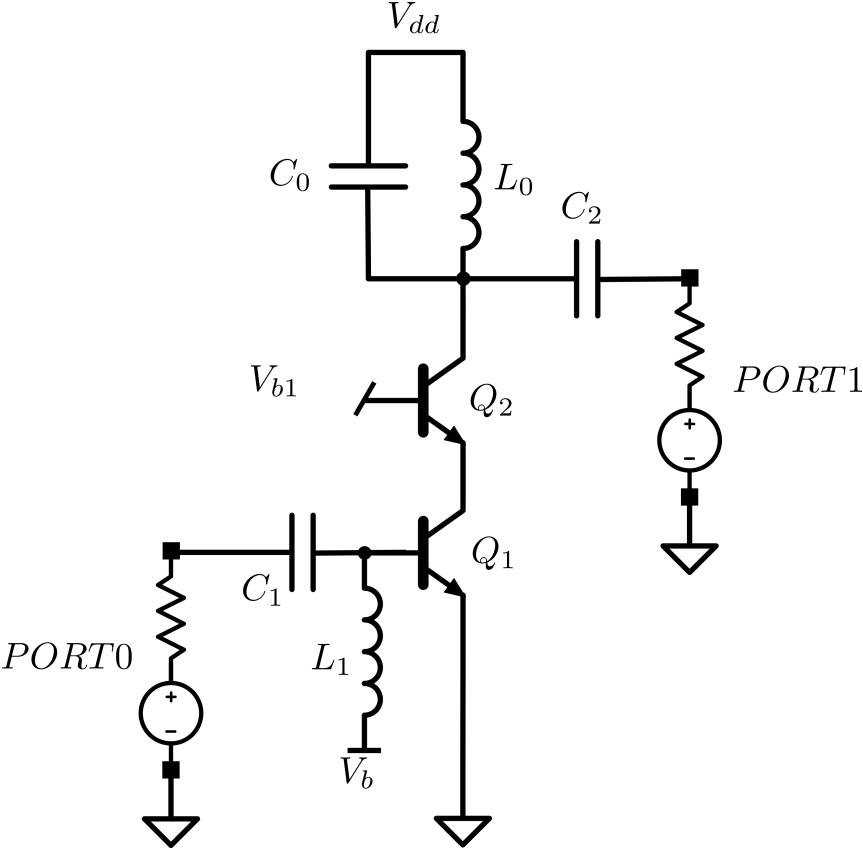
Figure 2.8: Cadence test bench for the evaluation of the PA power gain

We finally come to an obvious conclusion: in order to maximize power gain, the cutoff frequency of an active device should be as high as possible.

The astonishing simplicity of (2.24) may let a question arise: how accurate is this power gain estimation? A common-emitter cascode amplifier has been simulated in Cadence. The test bench is reported in fig. 2.8. Ports have been connected at both input and output. A negative capacitor C_0 has been placed in parallel to the choke inductor, and it has been tuned in order to achieve a perfect parasitic neutralization at the output node; this mathematical trick allows the output port to be a constant real impedance over the whole spectrum. Loadpull simulations confirmed that neutralization was correctly achieved at multiple frequencies. Note that this approach presents the advantage to allow the choke inductor to be independent on parasitics and frequency, removing the need of inductive tuning for every iteration cycle. An S-parameter analysis, instead, provided the actual input impedance seen at Q1 base for every simulation frequency. The input port was then tuned accordingly in order to ensure conjugate match. The iteration of this procedure over an excess of two decades showed that the model is in good agreement with the simulation within the frequency range of interest.

Looking at fig. 2.9 we can notice that, while the frequency behavior is well modeled, power gain is overestimated across the whole frequency range. This fact can be justified noticing that, so far, emitter degeneration resistance has been neglected. In bipolars, some resistance at the emitter node is unavoidable, and its effect should be taken into account once the local degeneration term $g_m R_e$ becomes comparable to 1. Unfortunately, this is the typical case, since emitter resistances are in the order of few Ohms.

Section A.2 justifies the use of the input impedance simplified model, neglecting the presence of R_E, which well fits our transistors at high frequency. This suggests that, when computing the power absorbed by the transistor at input side, the (2.19) is still valid. Emitter degeneration, instead, introduces
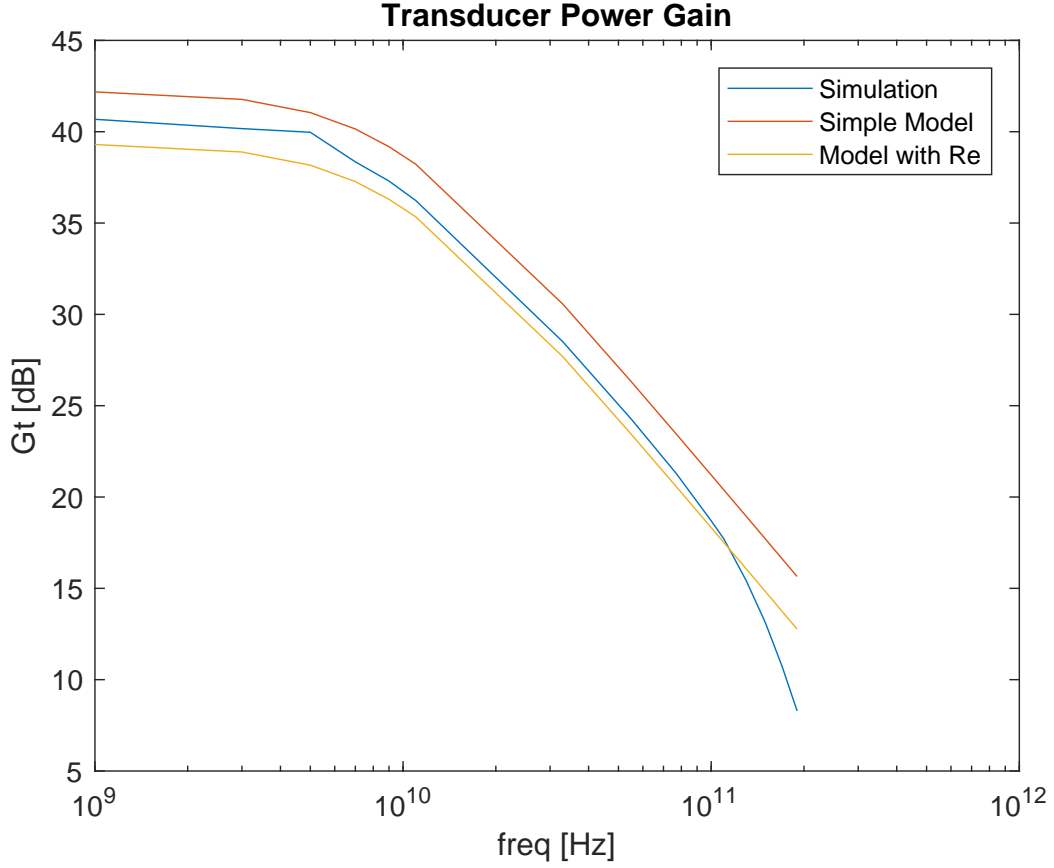
Figure 2.9: G_T: simulation and models comparison

non-negligible gain reduction, so the (2.20) must be updated, giving:

$$i_{out} = \frac{g_{m,1} v_\pi}{1 + g_m R_e} \tag{2.25}$$

The lower transconductance will cause output power decrease, so the (2.11) will be reduced by a factor $(1 + g_{m,1} R_{e,1})^2$, which impacts on power gain. We may conclude that the effect of non-null emitter degeneration resistance can be taken into account as follows, modifying the (2.21):

$$G_T \cong \frac{g_{m,1}{}^2 R_L}{\omega^2 (C_\pi + C_\mu)^2 r_b} \cdot \frac{1}{(1 + g_{m,1} R_{e,1})^2} \tag{2.26}$$

and the (2.24) becomes:

$$G_T = \frac{R_L}{r_b} \cdot \left(\frac{\omega_t}{\omega}\right)^2 \cdot \frac{1}{(1 + g_{m,1} R_{e,1})^2} \tag{2.27}$$

Obviously, the simplified model fails at low frequency, where the presence of R_E cannot be neglected more. In the low-frequency range, degeneration contributes to input impedance increase, thus our model overestimates the power absorbed causing power gain underestimation.

2.6 PA design

The PA will drive the input pads of a phase shifter which is designed to have an input differential impedance around 100Ω within the desired bandwidth. Thus we can model the load of the PA as a real impedance equal to 100Ω.

Typically, for a class A common-emitter amplifier, the *output-referred 1dB compression point, OP_{1db}*, is located $2-3dB$ below the saturation power P_{sat}, where efficiency peaks; this phenomenon is called *soft saturation* and causes a *PAE* degradation in these kinds of amplifiers, when operated in their linear range [12]. For this reason, we will drive the PA around its compression point, so as to balance linearity and efficiency. Increasing back-off would provide better linearity at the expense of a rapidly reduced efficiency.

In order to have some margin and take into account that output matching network will introduce losses and a fraction of power will be unavoidably reflected back to the amplifier due to the impossibility to achieve a perfect impedance match over the band, we can size the stage for a saturated optimum power of $7dBm$; we will then back-off the amplifier in the $4-5dBm$ range.

The single-ended version of the PA is shown in fig. 2.10. It will be designed for a $P_{sat} = 3.5dBm \cong 2.3mW$. Full power will be recovered once the PA is realized in a differential fashion.

A reasonable choice could consist in setting the R_{opt} of the amplifier equal to the load impedance, leaving a turn ratio $n = 1$ for the output matching network. To this aim we can pick the one designed in section 1.4.1. With
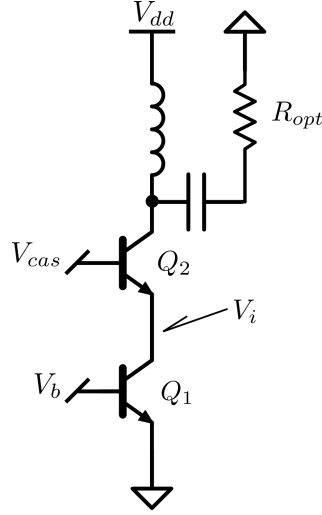
Figure 2.10: Single-ended PA bias point

$R_{opt} = 50\Omega$, we derive $\Delta V \cong 480mV$ from eq. (2.21) and, rearranging the (2.3), we get $I_q = 9.6mA$.

Once the bias current for the transistors is set, we should fix the supply voltage. Assuming $V_{BE} = 800mV$ and $V_i = 1V$ at quiescent point to guarantee enough voltage headroom for $Q1$ during operation, we can safely say that V_{dd} will not be lower than $1.8V$, due to the presence of the cascode, leaving $Q2$ very close to saturation.

A more realistic value for V_{dd} is $2V$. We can immediately conclude, thanks to eq. (2.5), that collector efficiency will be theoretically limited to 12%, and, as previously pointed in (2.7), PAE will be even lower. In fact, cascode configuration forces us to have a supply voltage much higher than the voltage swing applied on the 50Ω load when our target power is delivered.

Eq. (2.5) suggests that moving to a higher R_{opt} would improve efficiency. Our matching network will then perform impedance scaling, adapting the 50Ω load to the desired R_{opt}. Unfortunately, we cannot indefinitely increase R_{opt}, since practical limitations on the matching network turn ratio n exist. With the same approach followed in section 1.4.1, an upconversion matching

network was designed, and the components values are listed in table 2.1. The impedance synthesized at primary side is around 90Ω over the desired band. Fig. 2.11 illustrates the S_{11} for different Smith Chart normalization values. The blue line, normalized to 50Ω, can be used to make a direct comparison with the network of section 1.4.1, while the red curve is normalized to the targeted $R_{opt} = 90\Omega$. Fig. 2.12 reports the transimpedance of the output matching network. It has been assumed $Q = 12$ at $80GHz$ and the network has been already compensated for losses, being the peaks equalized.

L_1	L_2	C_1	C_2	k
114pH	68pH	40fF	80fF	0.5

Table 2.1: PA output matching network parameters

In this case, we derive $\Delta V \cong 650mV$ and $I_q = 7mA$. We can leave the supply voltage unchanged, $V_{dd} = 2V$, and the maximum collector efficiency rises to $\eta_c = 16.2\%$.

We can conclude that the more careful choice of R_{opt} led to a 35% relative improvement in efficiency, at the expense of an increased area occupation due to a larger primary inductor.

L_1	L_2	C_1	C_2	k
148pH	148pH	63fF	26fF	0.5

Table 2.2: PA input matching network parameters

An input matching network was then sized, following the same approach as above, with a turn-ratio equal to unity, being impedance transformation unnecessary, here; the multiplier will then be sized for a load impedance equal to the differential input impedance of the PA, which is equal to 110Ω. The network resonates the input capacitance of the PA and its parameters are reported in table 2.2.
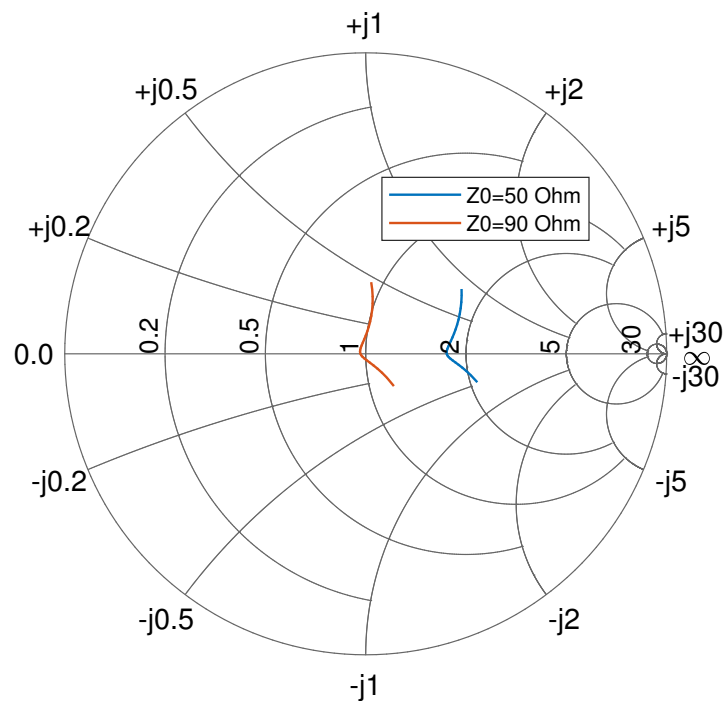
Figure 2.11: PA output matching network S_{11} $(60 - 90GHz)$ for different Smith Chart normalization values
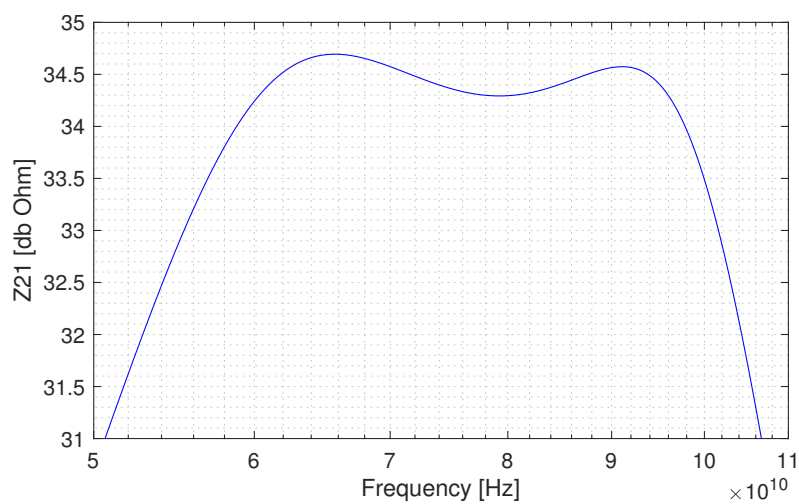
Figure 2.12: Z_{21} of the PA output matching network
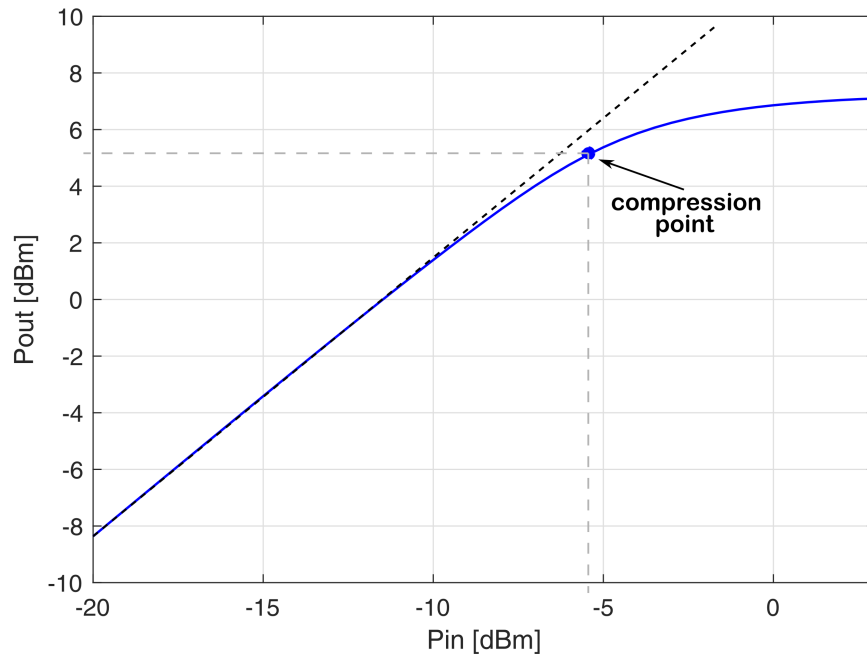
Figure 2.13: Simulated compression curve of the PA
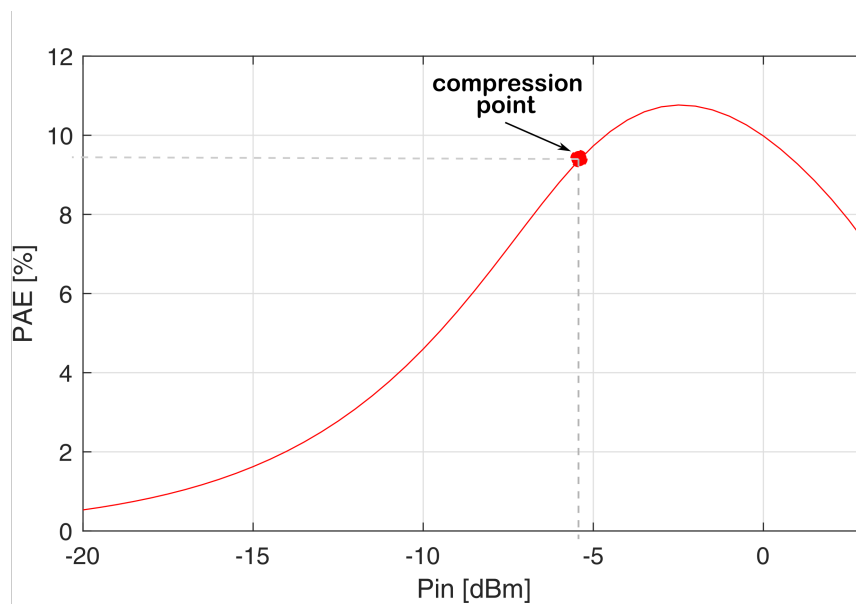
Figure 2.14: Simulated PAE of the PA
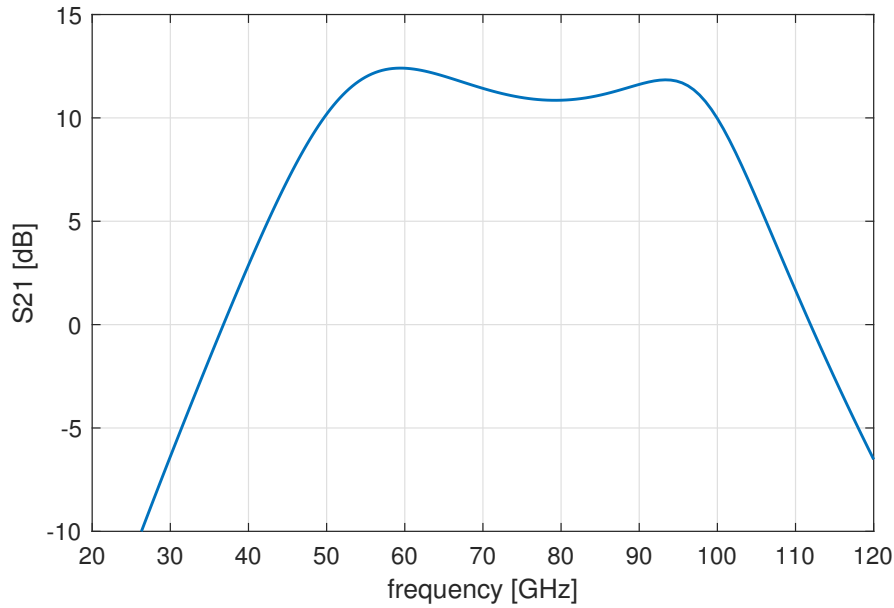
Figure 2.15: S_{21} of the simulated PA

The compression curve of the stage is reported in fig. 2.13; the amplifier output power saturates at $7.13dBm$. The input-referred 1dB-compression-point $P_{IP,1dB}$ is equal to $-5.66dBm$, corresponding to an output power of $5.3dBm$. Figure 2.14, instead, shows the simulated PAE. Due to losses on output match network, and being quasi-linear discussion a rough approximation of the behavior of transistors approaching saturation, efficiency is lower than expected, and stops at 10.9%, degrading to around 9.5% at the compression point.

The S_{21} and the S_{11} of the stage are reported in figg. 2.15 and 2.16, respectively.

The layout of the realised PA is reported in fig. 2.17. Figure 2.18, instead, shows the PA connected to the output matching network, followed by a transmission line, dimensioned to correctly feed the input pads of the next stage.
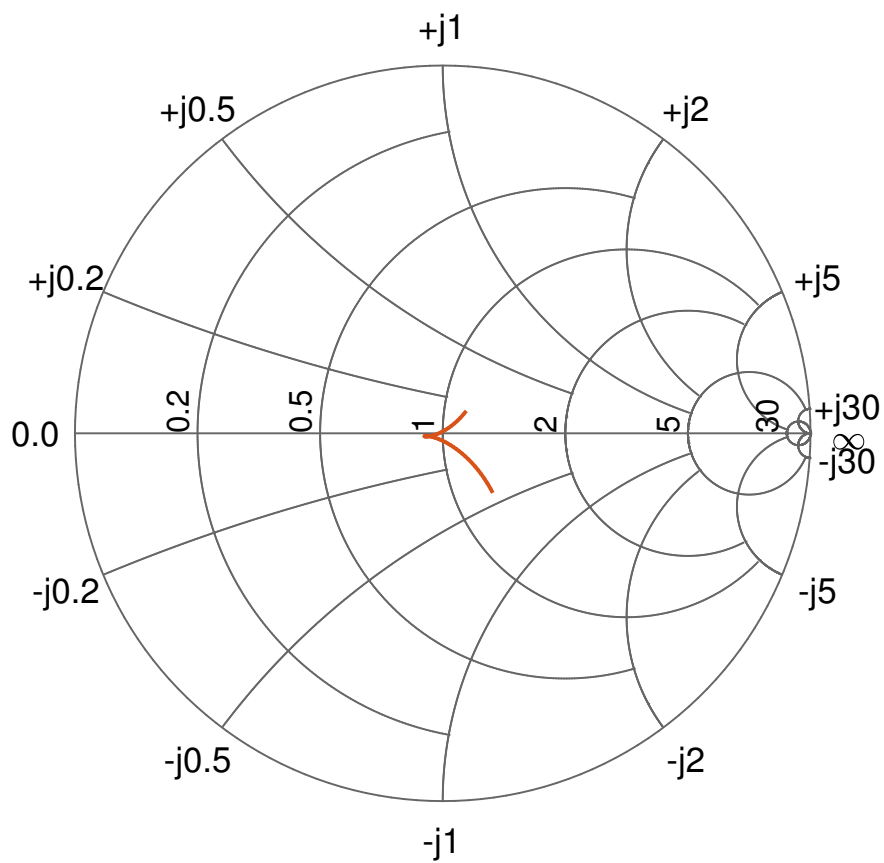
Figure 2.16: S_{11} of the simulated PA in the $60 - 90GHz$ band
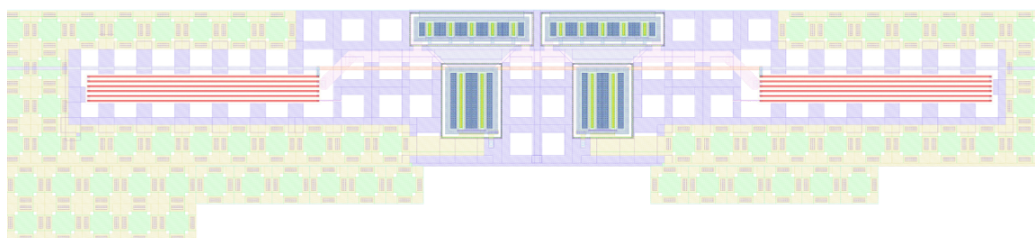
Figure 2.17: Layout of the fabricated PA
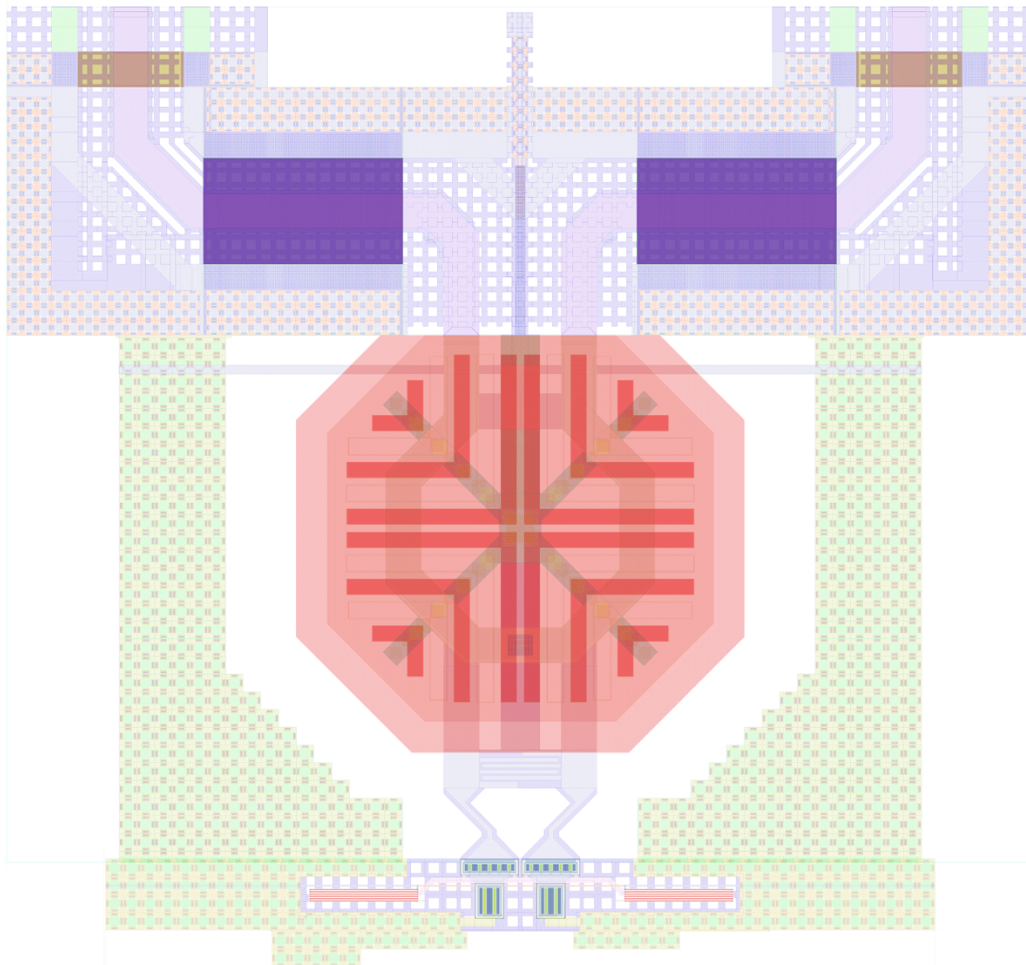
Figure 2.18: PA and output matching network + transmission line

Chapter 3

Push-push frequency multipliers

A push-push frequency multiplier is an analog circuit aimed to produce at output a signal whose frequency is double with respect to the one at input. Its operation principle relies on the cancellation of odd-order harmonic currents through the direct connection of the collectors in a differential pair. Fig. 3.1 shows the basic topology. Thanks to symmetry, odd currents recirculate within the pair, while even-order harmonics flow into the load impedance.

We introduce an important quantity that characterizes a frequency multiplier: the conversion gain. It is defined as the ratio between the output power at the desired n^{th} harmonic versus the input available power at f_0:

$$G_c = \frac{P_{n \cdot f_0}}{P_{AVL,f_0}} \tag{3.1}$$

3.1 Small-signal analysis

We can justify the behavior of the circuit observing that the load current I_L is given by the sum of the single transistors' currents, thus:

$$I_L = I_s \cdot \left(e^{v_{b,1}/V_{th}} + e^{v_{b,2}/V_{th}} \right) \tag{3.2}$$
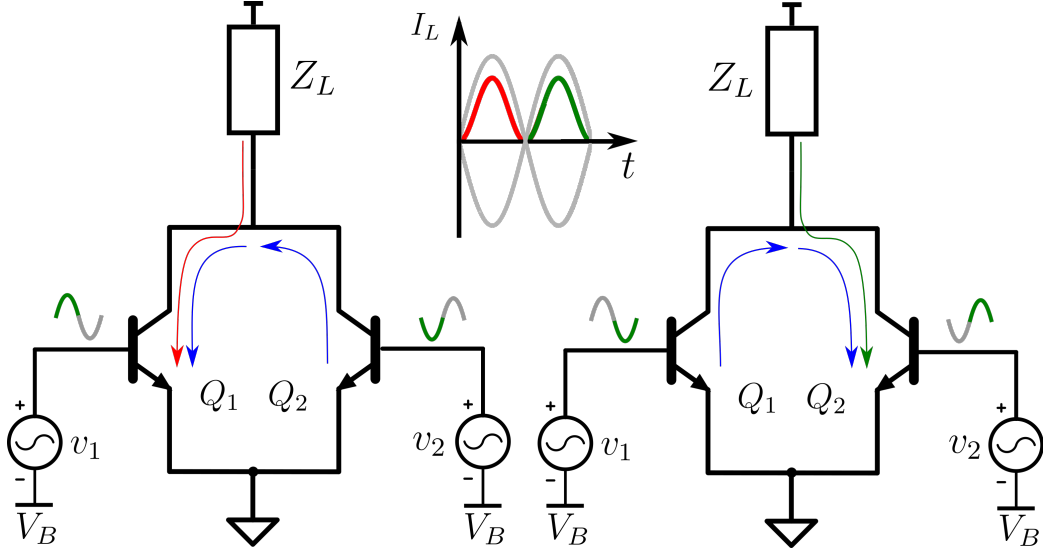
Figure 3.1: Push-push frequency doubler odd and even-order currents

where $v_{b1,2}$ are the base voltages of $Q_{1,2}$, respectively. The differential signal is fed through v_1 and v_2:

$$v_1 = A \cdot cos(\omega t) \quad and \quad v_2 = -A \cdot cos(\omega t) \tag{3.3}$$

So:

$$v_{b,1} = V_B + A \cdot cos(\omega t) \quad and \quad v_{b,2} = V_B - A \cdot cos(\omega t) \tag{3.4}$$

Combining (3.2) and (3.4) we get:

$$I_L = I_s \cdot e^{\frac{V_B}{V_{th}}} \left(e^{\frac{Acos(\omega t)}{V_{th}}} + e^{\frac{-Acos(\omega t)}{V_{th}}} \right) \tag{3.5}$$

Remembering the expression of the Taylor expansion for an exponential, stopped at the second order, we can write:

$$e^{\frac{Acos(\omega t)}{V_{th}}} = 1 + \frac{Acos(\omega t)}{V_{th}} + \frac{A^2 cos(\omega t)^2}{2V_{th}^2} + o(x^2) \tag{3.6}$$

$$e^{\frac{-Acos(\omega t)}{V_{th}}} = 1 - \frac{Acos(\omega t)}{V_{th}} + \frac{A^2 cos(\omega t)^2}{2V_{th}^2} + o(x^2) \tag{3.7}$$

remembering they are valid around the origin; in our case the condition

$$\frac{A \cdot cos(\omega t)}{V_{th}} \to 0 \tag{3.8}$$

should be verified.

Summing up (3.6),(3.7), and plugging into (3.5) we obtain:

$$I_L = I_s \cdot e^{\frac{V_B}{V_{th}}} \left(2 + \frac{A^2 cos^2(\omega t)}{V_{th}^2} + o(x^2) \right) \tag{3.9}$$

As we plug in the double-angle formula for the cosine:

$$A^2 cos^2(\omega t) = \frac{A^2}{2} \left(1 + cos(2\omega t) \right) \tag{3.10}$$

we finally get:

$$I_L = I_s \cdot e^{\frac{V_B}{V_{th}}} \left(2 + \frac{A^2}{2V_{th}^2} + \frac{A^2 cos(2\omega t)}{2V_{th}^2} + o(x^2) \right) \tag{3.11}$$

And, if we neglect the error committed by approximating the exponential with a second order polynomial, thus removing $o(x^2)$, we get:

$$I_L = I_s \cdot e^{\frac{V_B}{V_{th}}} \left[\left(2 + \frac{A^2}{2V_{th}^2} \right) + \left(\frac{A^2 cos(2\omega t)}{2V_{th}^2} \right) \right] \tag{3.12}$$

The (3.12) highlights that the output current is composed by two terms, primarily: DC plus a second harmonic. The former accounts for both bias and an additive DC component which arises any time a sinusoidal function gets squared; the latter is the pure double-frequency signal we want to extract.

Note that both the DC and the double-frequency term depend on the input amplitude A, thus suggesting that a higher signal can be obtained at the expense of a higher DC current, which should be nil, ideally. Thus a strict trade-off between second-harmonic output power and DC power consumption exists, limiting the efficiency of the frequency doubler.

3.2 Class-B operation

The analysis carried out in the previous section presents the limit to be valid for small input signals (eq. (3.8)). For high input levels, (3.6) and (3.7) only
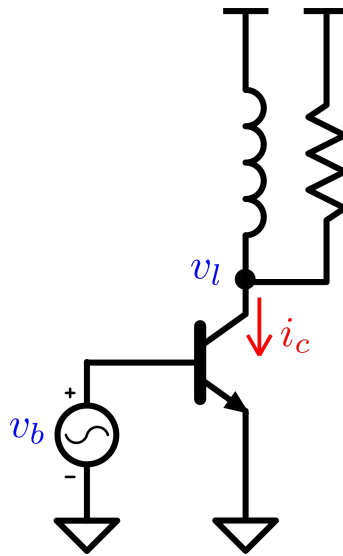
Figure 3.2: Single-ended Push-Push frequency multiplier

provide a rough estimation, and higher order terms should be included in the approximation of the exponential characteristic curve of the current in the bipolar transistors. Nevertheless, the discussion catches the overall behavior of push-push circuits.

Note that the scope of the stage is to extract a double-frequency signal exploiting non-linearity, thus DC current, as pointed out previously, is totally useless and should be minimized in order not to waste power. This suggests that the pair should be biased so that a small current flows at DC, ideally zero. Only when input voltage rises, current in the transistor increases following an exponential behavior. Thus, class-B operation allows both DC power saving and non-linearity boost.

The analysis can be simplified under the approximation that the DC current is negligible at the bias point. Therefore, the transistor starts conducting only when a positive waveform arises at its input. The single ended version of the circuit is depicted in fig. 3.2 and the input/output waveforms are reported in fig. 3.3.

The collector current waveform can be approximated with a rectified-cosine,
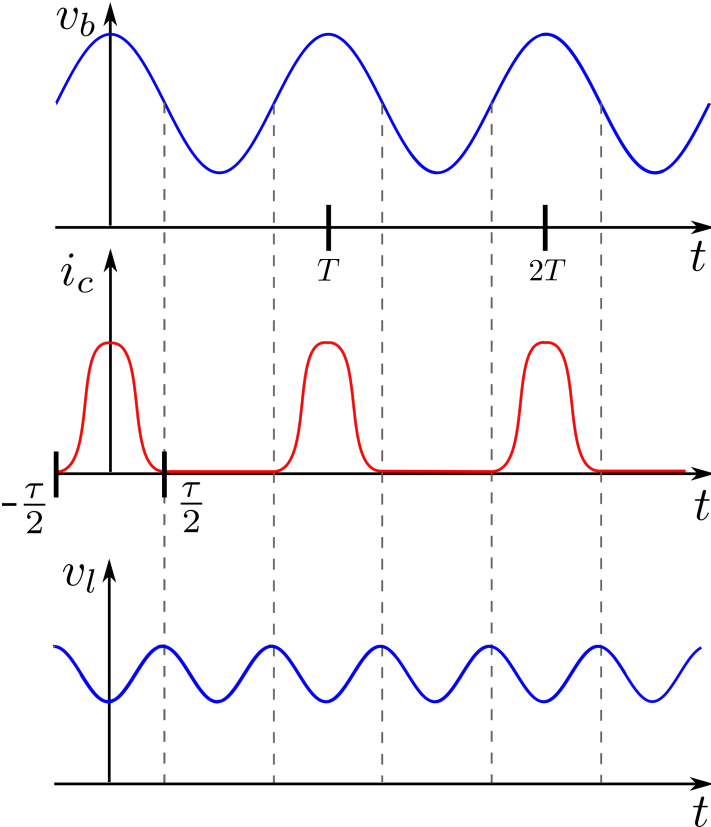
Figure 3.3: Single-ended Push-Push waveforms

and the spikes represented as half-cosine pulses [13] :

$$I_c(t) = \begin{cases} I_{max} \cdot cos(\frac{\pi t}{\tau}) & \text{if } |t| < \frac{\tau}{2} \\ 0 & \text{if } \frac{\tau}{2} < |t| < \frac{T}{2} \end{cases} \tag{3.13}$$

Remember the definition of Fourier series for an even function:

$$f(x) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cdot cos\left(\frac{n\pi x}{L}\right) \tag{3.14}$$

with

$$c_n = \frac{2}{L} \cdot \int_0^L f(x) \cdot cos\left(\frac{n\pi x}{L}\right) dx \tag{3.15}$$

where L is the period of the function.

We can calculate the DC component of the output current for the class-B multiplier:

$$c_0 = \frac{4}{T} \cdot \int_0^{\tau/2} I_{max} \cdot cos\left(\frac{\pi t}{\tau}\right) dt = \frac{4\tau I_{max}}{\pi T} \tag{3.16}$$

Giving:

$$I_0 = \frac{c_0}{2} = \frac{2\tau I_{max}}{\pi T} \tag{3.17}$$

Note that in the (3.16), $\tau/2$ instead of $T/2$ has been used as upper integration extreme. This is legit since the function has been assumed to be zero between $\tau/2$ and $T/2$, due to the zero DC bias current approximation.

By combining (3.13) and (3.15), the nth harmonic current coefficient is given by:

$$I_n = \frac{4}{T} \int_0^{\tau/2} I_{max} \cdot cos\left(\frac{\pi t}{\tau}\right) \cdot cos\left(\frac{2n\pi t}{T}\right) dt \tag{3.18}$$

If we apply the substitution:

$$\frac{\pi t}{\tau} = \alpha \tag{3.19}$$

We get:

$$I_n = \frac{4\tau I_{max}}{\pi T} \int_0^{\pi/2} cos(\alpha)cos(\gamma\alpha)d\alpha \tag{3.20}$$

Where $\gamma = 2n\tau/T$; the result is:

$$I_n = \frac{4I_{max}\tau}{\pi T} \cdot \frac{cos\left(\frac{n\tau\pi}{T}\right)}{1 - \left(\frac{2n\tau}{T}\right)^2} \qquad (3.21)$$

A maximum for the (3.21) exists[1] and occurs for a given value of τ/T, which defines the conduction angle of the transistor, thus the current pulse duration. Unfortunately, the designer has very little control on the conduction angle, especially with BJTs, which do not have the threshold voltage that sets the conduction angle together with the signal quiescent point, therefore, in a typical design occurs:

$$\frac{\tau}{2} \cong \frac{T}{4} \quad so \quad \tau \cong \frac{T}{2} \qquad (3.22)$$

We can finally derive the expression for the second harmonic current coefficient:

$$I_2 = \frac{2}{3}\frac{I_{max}}{\pi} \qquad (3.23)$$

In order to optimize efficiency and maximize output power, the collector voltage swing should be as wide as possible.

3.2.1   Push-push design

The simple class-B frequency-doubler stage is shown in fig. (3.4). Obviously, due to the chosen operating class, bipolars cannot be current-biased, and the voltage V_B should be selected in order to limit the DC power consumption, noticing that a too low quiescent point causes both output power and conversion gain reduction.

Starting from the RF power level required at the output of the multiplier chain, around $7dBm$, we can subtract a reasonable power gain given by the PA, $12dB$, and get the power P_{out} needed at the output of the $40 - 80GHz$ multiplier, which will be in the $316\mu W$ range. The discussion made in the

---

[1]see [2], chpt. 13
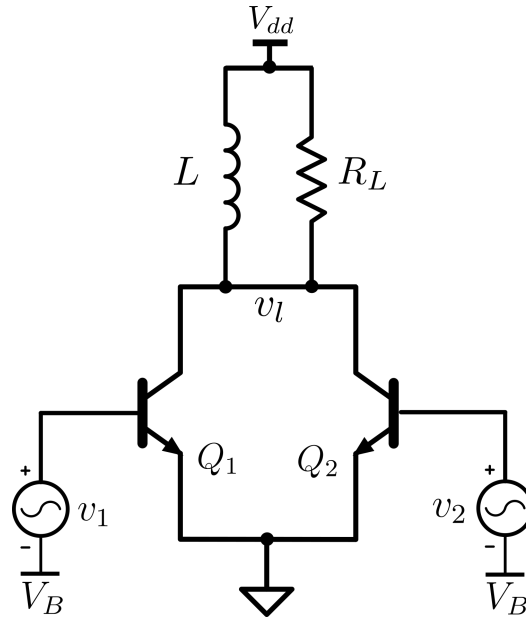
Figure 3.4: Simple push-push class-B frequency multiplier

previous section is valid for the half circuit. Since we work with differential circuits, we can size the half circuit for half the power, thus $P_{out} = 158\mu W$.

The multiplier's load resistance should be kept similar to the differential input impedance of the PA. Assuming $R_L = 110\Omega$, we can derive the second harmonic current amplitude I_2 needed to reach the targeted P_{out}, following the relation:

$$P_{out} = \frac{R_L \cdot I_2{}^2}{2} \tag{3.24}$$

We immediately derive I_{max} which is linked to I_2 through the (3.23).

We get $I_2 = 1.7mA$ and $I_{max} = 8mA$. We may now size the transistor in order to correctly deliver I_{max} when the input signal is maximum, making reasonable assumptions on its level. The geometric values are reported in table 3.1. N_e is the number of emitters, while W_e and L_e are emitter width and length, respectively.

Note that the supply voltage has not been set, yet. It should be kept small in order to avoid breakdown in the transistors, which occurs for a value of the collector-emitter voltage of about $1.5V$. The lower V_{dd} is, the smaller the

N_e	$W_e[\mu m]$	$L_e[\mu m]$
4	0.2	1

Table 3.1: Transistor size for the simple class-B push-push stage
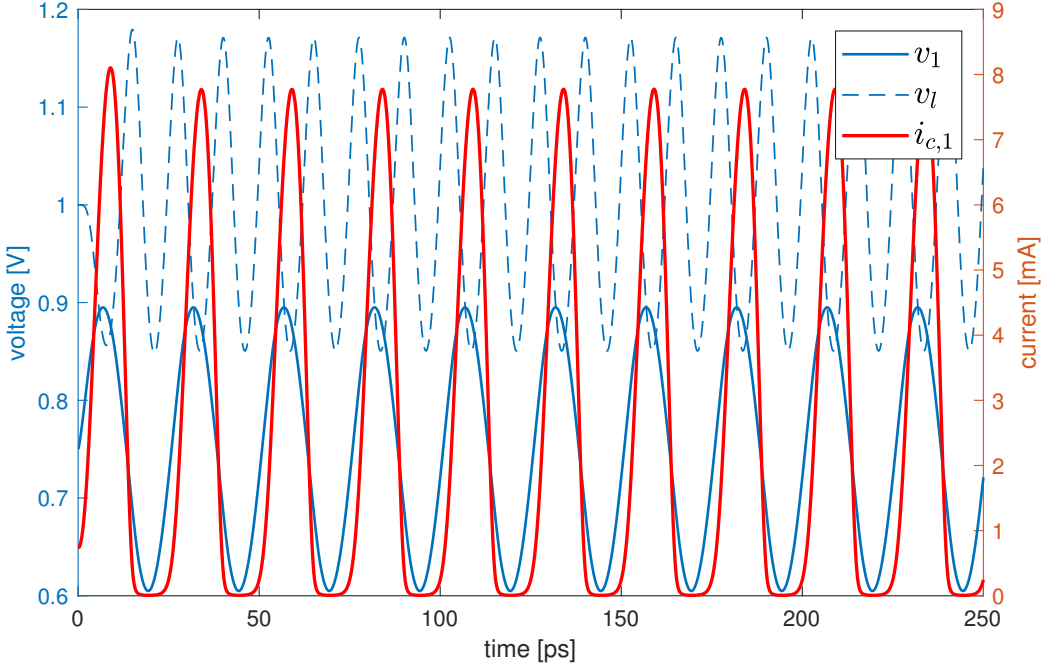
Figure 3.5: Push-push current and voltage waveforms

power consumption, but the performance of the transistor gets worse, too. We may set $V_{dd} = 1V$.

The inductor is tuned in order to resonate the collector parasitic capacitance, and its correct value will give maximum voltage swing across the load resistance. We get $L = 95pH$, which resonates $C_c = 41fF$ at $80GHz$. The overall power consumption is $6.4mW$ with $320\mu W$ output power across $R_L = 110\Omega$.

Fig. 3.5 shows voltage waveforms and current spikes at Q_1 collector junction. We effectively generate a signal at $2f_0$, but due to the limited amount of current gain at $80GHz$, we expect high current spikes drained from the
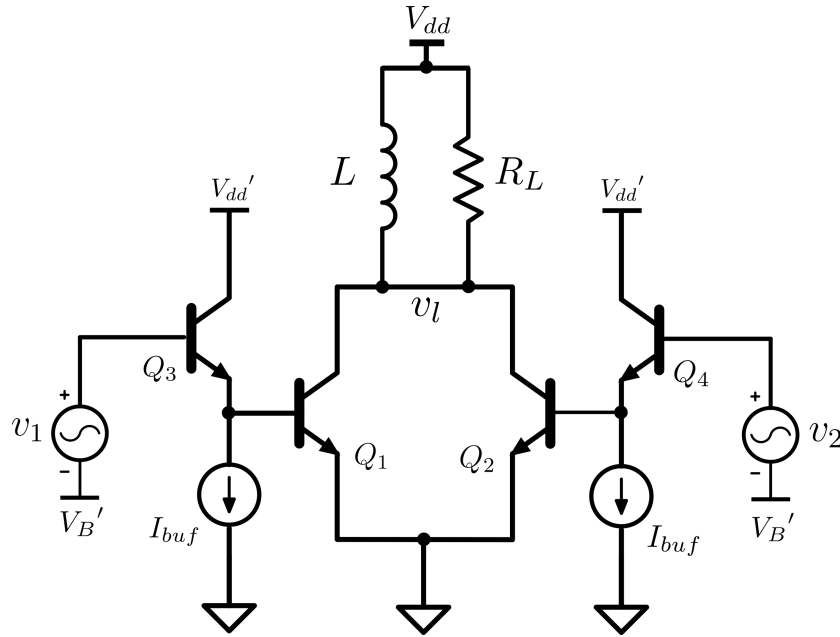
Figure 3.6: Buffered push-push class-B frequency multiplier

signal source, and since input and output impedances are comparable, we immediately conclude that the conversion gain is low. This is a limit of push-push stages [14], which typically get attenuation from input to second harmonic output.

3.3 Buffer outer pair

Cutoff frequencies in the order of $300GHz$, for our bipolar transistors, suggest that at E-band we still have some current gain available, and we can exploit it to buffer the push-push transistors. It may bring two advantages:

- Conversion gain improvement thanks to the introduction of a gain stage within the multiplier;

- Increase of the overall input impedance, reducing the current swing on the input matching networks.

Obviously we take these advantages at the expense of an increased power consumption.

The current gain, anyway, will be limited, especially for the higher multiplier, where operation at $80GHz$ is closer to the f_t of the devices. We can estimate the current gain, or β, at a given frequency, remembering that, after the main pole which occurs in the MHz range, it reduces by $20dB/dec$ as frequency grows, and we have:

$$\beta_f = \frac{f_t}{f} \tag{3.25}$$

which is about 4 at $80GHz$. This also means that push-push transistors will be characterized by base currents spikes in the few mA range. We can conclude that buffers, that operate in class-A, will require a collector current of the same order of magnitude.

The proposed topology is reported in fig. 3.6. Note that $V_B{}'$ is different than the previously used V_B and a second voltage supply $V_{dd}{}'$ higher than V_{dd} is needed.

3.3.1 Buffered push-push design

The circuit used in the previous example will be now used as multiplier core and an outer buffer pair will be added, as reported in fig. 3.6. I_{buf} must be at least higher than push-push pair base current. We can set it to $3mA$. The buffers are then optimized for class-A operation, reaching an f_t of approximately $310GHz$ with the size reported in table 3.2. $V_{dd}{}'$ is set to $1.9V$ and the new bias voltage is selected in order not to alter the bias point of the multiplier core, giving $V_B{}' = 1.6V$. The inductor is re-tuned to account for additive parasitics introduced by the buffer, giving $L = 75pH$, which resonates $52fF$ at $80GHz$.

The current waveforms for one side of the circuit are reported in fig. 3.7, where we can notice the progressive current gain from Q_3 base to Q_1 collector. Note that waveforms appear different than those of fig. 3.5 since what we're
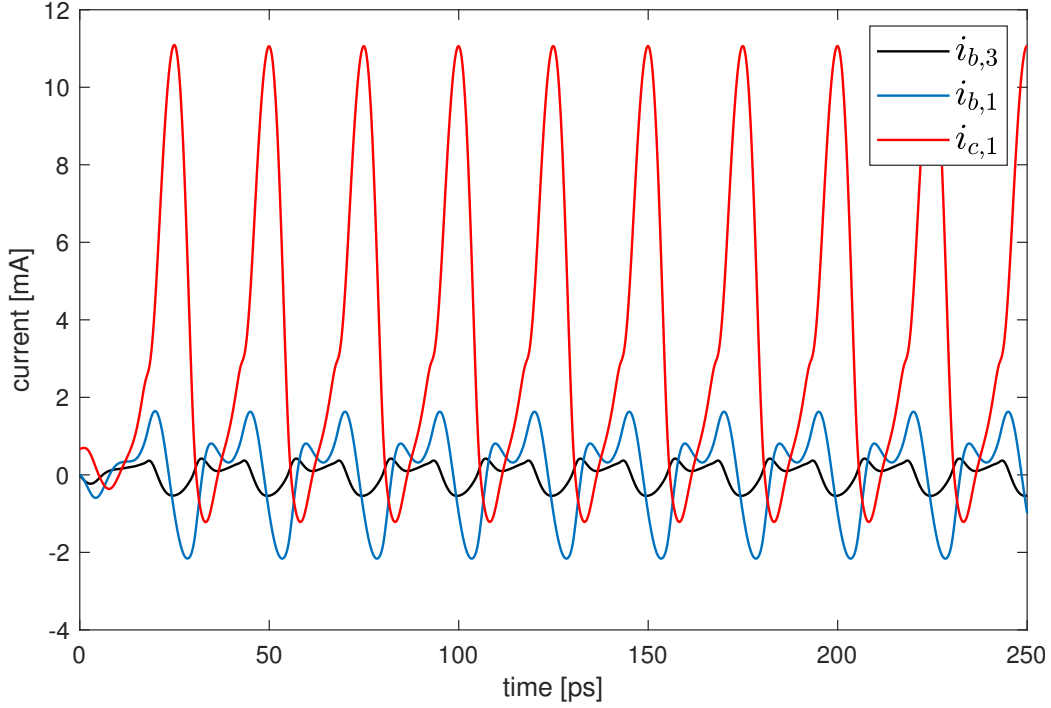
Figure 3.7: Current waveforms in the buffered push-push class-B multiplier

showing here is the overall current flowing into the devices including parasitic capacitors, which are nonlinear elements under large-signal operation and cause large current swings. The overall power consumption, for the same output power, rises to about $17mW$.

Then the current generator is realized with a MOS transistor, which can be sized with an overdrive low enough not to fall into ohmic region during operation. This choice was operated since the generator has limited voltage headroom, and this is due to the class-B bias of the core.

The final proposed topology is reported in fig. (3.8).

N_e	$W_e[\mu m]$	$L_e[\mu m]$
2	0.2	1

Table 3.2: Transistors size for the buffer pair in the class-B push-push
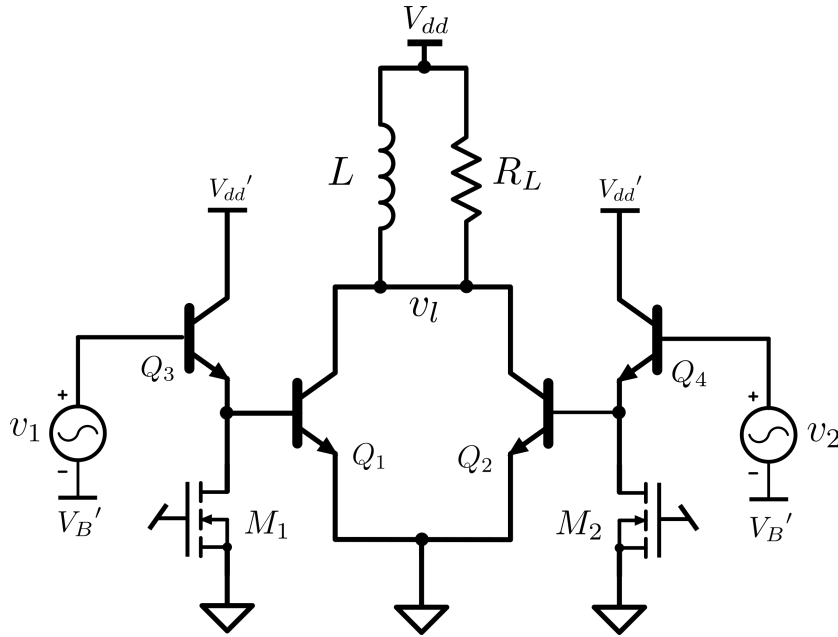
Figure 3.8: Class-B push-push with input buffer and MOS current generators

3.4   Large-signal S-parameters

Microwave engineers and circuit designers typically need proper network characterization during their work but, as frequency increases, voltage and current may not be more suitable for this job. In fact, in order to perform correct measurements (e.g. Thevenin/Norton theorems), both open and short circuits need to be applied to the ports of a network. Unfortunately, at high frequency, leaving a port unconnected does not necessarily mean that an open circuit exists. Instead, the impedance connected to the port will be frequency-dependent and could even drop to zero for specific frequencies [15]. Besides, even if correct and stable impedances are reached over the desired bandwidth, measurement equipment may not be able to read total voltage and/or current at one port. These are the main reasons that pushed for the introduction of scattering parameters (or S-parameters) matrices which allow to properly characterize a network analyzing incident
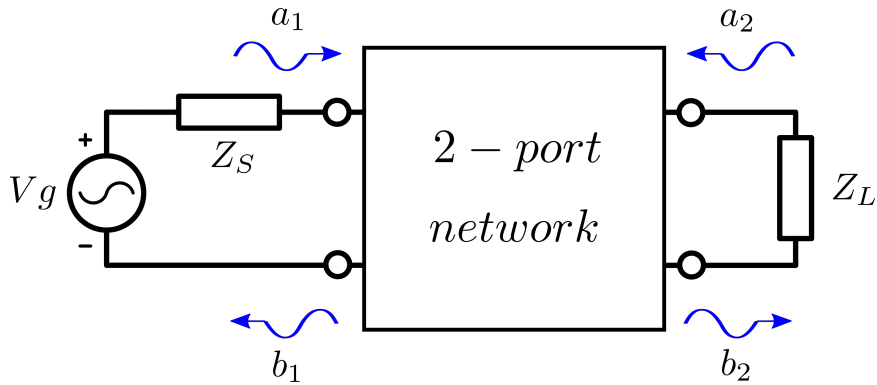
Figure 3.9: 2-port network with incident/reflected waves on its ports

and reflected (scattered) voltage traveling waves instead of total voltage or current applied at a port.

A n-port network is characterized by its S-parameters S_{ij} which are derived by energizing port j and measuring the response on port i when the latter and all the other ports but i are terminated onto a matched load, so as to avoid reflections. It follows that a 2-port network will be described by a 2x2 matrix where S_{11} and S_{22} are the reflection coefficients at port 1 and 2, respectively, while S_{21} and S_{12} express forward and reverse transmission. The situation is sketched in fig. 3.9 and the scattering parameters are defined as follows:

$$S_{11} = \frac{b_1}{a_1}\bigg|_{a_2=0} \quad S_{22} = \frac{b_2}{a_2}\bigg|_{a_1=0} \quad S_{21} = \frac{b_2}{a_1}\bigg|_{a_2=0} \quad S_{12} = \frac{b_1}{a_2}\bigg|_{a_1=0} \qquad (3.26)$$

where the coefficients can be related to incident/reflected traveling voltage waves through the characteristic impedance Z_0 of the transmission line:

$$a_1 = \frac{E_{i,1}}{\sqrt{Z_0}} \quad a_2 = \frac{E_{i,2}}{\sqrt{Z_0}} \quad b_1 = \frac{E_{r,1}}{\sqrt{Z_0}} \quad b_2 = \frac{E_{r,2}}{\sqrt{Z_0}} \qquad (3.27)$$

and $E_{i,j}$ and $E_{r,j}$ are the amplitudes of a traveling voltage wave impacting or reflected by port j, respectively.

Looking at (3.27), we can observe that the squared magnitude of a_n, b_n has the dimension of power, thus $|a_n|^2$ can be thought as power incident on port n, and $|b_n|^2$ as power reflected by port n. We can finally conclude that these coefficients may be particularly useful to account for the power gain of a device under test, giving:

$$G_T = |S_{21}|^2 \tag{3.28}$$

under the hypothesis that ports are matched for zero reflection [2]. Note that when we handle this quantity in dB, we may indifferently use:

$$G_T = 10 \log_{10} \left(|S_{21}|^2\right) \quad \text{or} \quad G_T = 20 \log_{10} \left(|S_{21}|\right) \tag{3.29}$$

The problem, in our case, is that the concept of S-parameters relies on the superposition principle and consequently on linearity. If the device under test is a nonlinear system, the Scattering matrix becomes completely meaningless and varies with input signal. Thereby, we may come to the conclusion that the characterization of an active circuit by means of S-parameters is wrong. This sentence is partially true, and S-parameters are typically used with semiconductor circuits, provided that the input stimulus is small enough to verify that superposition principle still holds [16].

The problem gets initially simplified with the reasonable assumption that the device is unilateral, thus $S_{12} = 0$. Accordingly, S_{11} and S_{21} depend on input drive only [17]. This fact suggests that we may stimulate the device at the input side and derive a set of S-Parameters which will be valid for that specific input power only. This is why large-signal S-parameters are also called power-dependent S-parameters.

The simulators we have available allow us to extract Large-signal S-parameters through harmonic balance analyses that take into account nonlinear effects as compression and frequency translation.
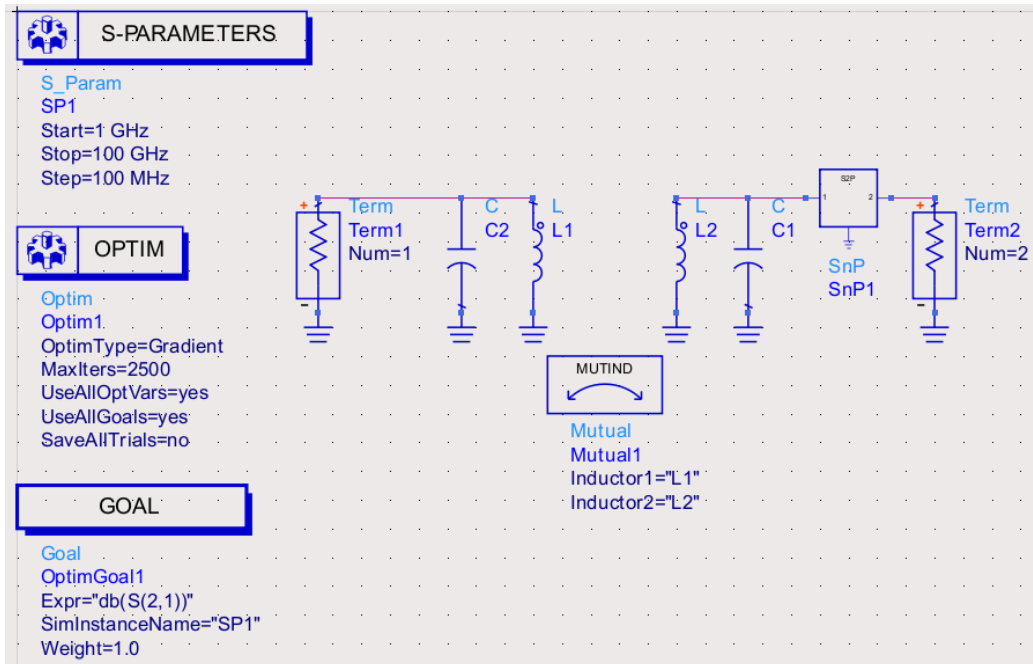
Figure 3.10: ADS workspace for the optimization of matching networks

3.5 Buffered push-push conversion gain

Following this discussion, the buffered push-push multiplier above described has been simulated in Cadence, and the large-signal S-parameters, obtained by means of an *hbsp* analysis with fundamental tone at the input port and load harmonic 2 at output port, have been passed to an ADS workspace, depicted in fig. (3.10). This tool is particularly useful thanks to the presence of an optimization feature, which is able to find the best circuit parameters given a function to be optimized. In this way, even if we're handling nonlinear circuits where the classic approach of impedance matching becomes problematic, power gain can be maximized over the desired bandwidth given some constraints on the components values, e.g. inductor size. A gradient-type optimization was performed, and the final input matching network sizing is reported in table 3.3.

The network, considering a limited $Q = 20$ at $40GHz$ for the inductive
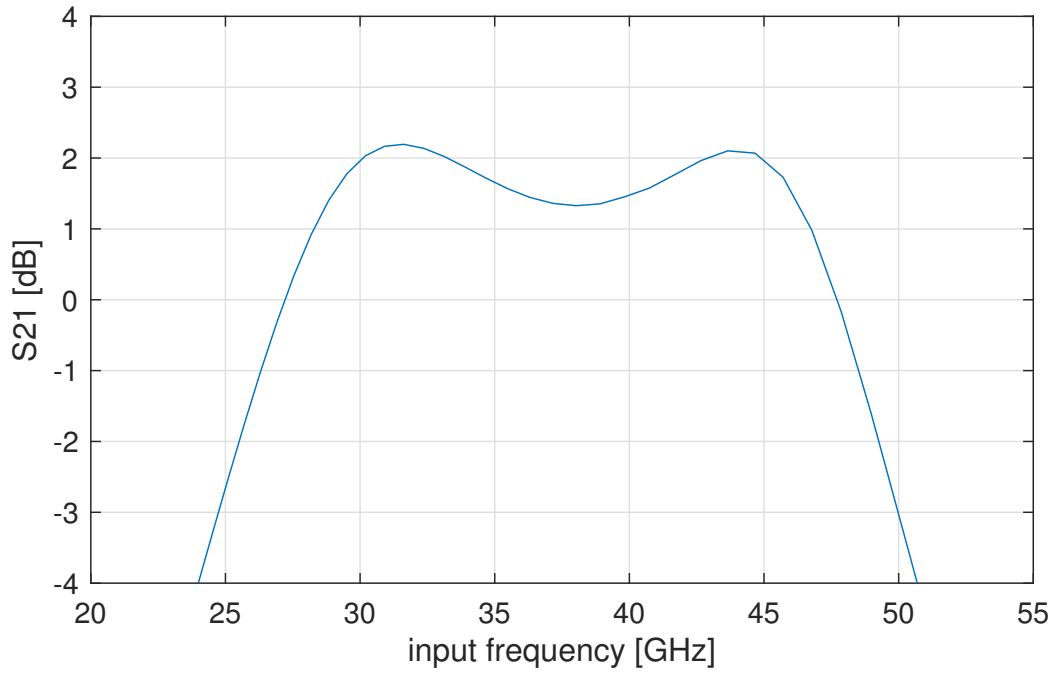
Figure 3.11: S_{21} from $40GHz$ to $80GHz$ of the upper multiplier

elements, has been connected at the input side and the simulated conversion gain of the stage is reported in fig. 3.11.

$C_1[fF]$	$L_1[pH]$	$C_2[fF]$	$L_2[pH]$	k	$Z_{in,diff}[\Omega]$
91	250	74	250	0.45	100

Table 3.3: Optimized push-push input matching network

The layout of the realised push-push multiplier is reported in fig. 3.12. Two resistors connected at the emitters of the core active elements can be noticed. They have been added to get a more stable behavior over temperature drifts and process corners, due to the use of voltage biasing, and their value is limited to few Ohms.
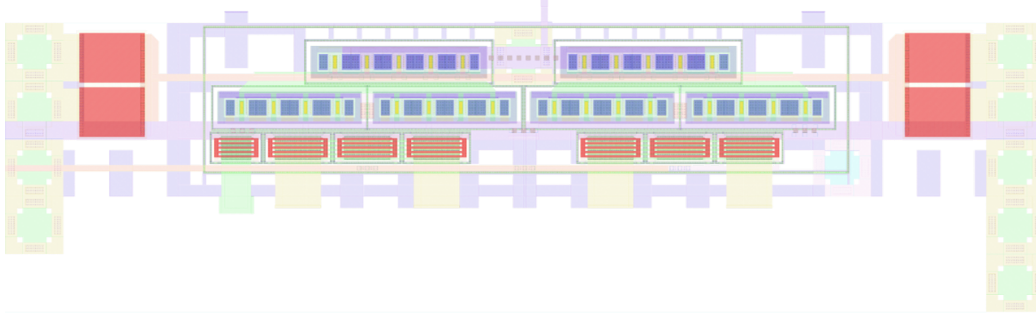
Figure 3.12: Layout of the realised push-push multiplier

3.6   X4 multiplier chain design

Two push-push frequency multipliers are stacked, and the circuit is reported in fig 3.13. The upper has been already dimensioned, and the sizing procedure showed above was performed also for the the lower multiplier. Considered the actual conversion gain of the $40 - 80GHz$ multiplier, the output power P_{out} required at $40GHz$ is comparable to the one at the input of the PA, thus the core of the lower multiplier is basically unchanged from the one previously designed. Thanks to the higher current gain available, the buffers have been sized for a smaller collector current, equal to $Ibuf = 1.5mA$, reaching an f_t of approximately $330GHz$ with the dimensions reported in table 3.4.

The total power consumption is $30mW$ and the overall conversion gain from $20GHz$ to $80GHz$ is in the 0dBm range, thus input power at the fundamental frequency and output power at the fourth harmonic are comparable.

N_e	$W_e[\mu m]$	$L_e[\mu m]$
2	0.2	0.6

Table 3.4: Transistors size for the buffer pair in the lower push-push multiplier

The input matching network, which acts as *balun* for the input port at $20GHz$, was sized again with ADS, and the interstage network, previously sized together with the upper multiplier, was corrected in order to resonate the output parasitic capacitance of the lower multiplier.
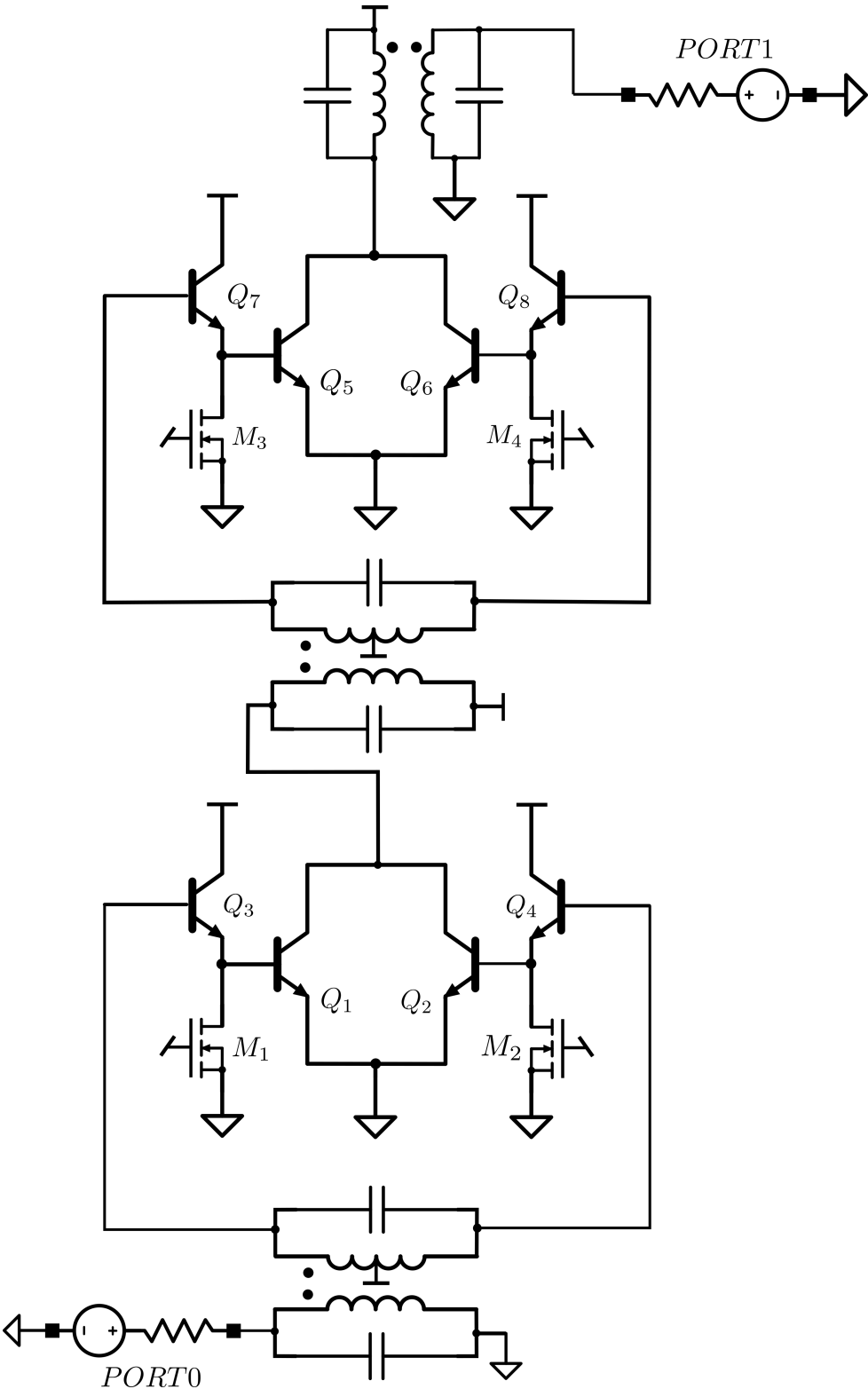
Figure 3.13: magnetically-coupled X4 push-push multiplier schematics

Conclusions

This work covered the design of a factor-four frequency multiplier with E-band power amplification for 5G backhaul applications, needed for the generation of frequency references in the $60 - 90GHz$ range, where PLLs are currently unavailable. A design procedure has been proposed, involving the use of large-signal S-Parameters, allowing to perform iterative optimizations of nonlinear circuits impedance matching. Push-push frequency doublers, characterized by large current spikes at their inputs, have been buffered, so as to improve the intrinsic low conversion-gain of this kind of circuits. A direct comparison can be made with [14], where a low-power $7mW$ push-push quadrupler was realised, delivering -5dBm output power, which is very similar to the one targeted here, and conversion gain limited to $-8dB$. The higher power consumption, $30mW$, is related to the presence of input buffers, which allowed to increase the gain to around $0dB$. Furthermore, a wider fractional bandwidth was required here, moving from 27% to 40%.

Broadband inter-stage coupling and impedance matching were achieved by making use of doubly-tuned transformers, and a compact procedure for the sizing of these networks was discussed, targeting flat transimpedance.

Particular attention was put on the design of a class-A power amplifier, sized for a P_{sat} of $7dBm$ and $5.3dBm$ compression point. With a peak PAE of 10.9%, efficiency is maximized and in line with PAs found in literature, considering topology, operating class and bandwidth, as pointed out in [18].

Appendix

A.1 HiCUM/L2 small-signal model simplification

The model employed by the circuit simulator for the HBT transistors is the HiCUM/L2 [19]. Its small-signal equivalent circuit is reported in fig. A.1. We want now to introduce a small-signal simplified model in order to gain some insight about the main sources of parasitics and how they affect frequency response.

The main simplification regards base network; neglecting R_{Bi}, π elements collapse to parallel. For small substrate resistance and small load resistance $(R_L \ll r_{0i})$, we can derive the simplified model of fig. A.2, where

$$C_\pi = C_{\pi i} + C_{\pi x} \tag{A.1}$$

$$C_\mu = C_{\mu i} + C_{\mu x} \tag{A.2}$$

$$r_\pi = r_{\pi i} // r_{\pi x} \tag{A.3}$$

We want now to apply the simplified model and assess the frequency response of the cascode PA studied in section 2.3. To this aim, we will exploit
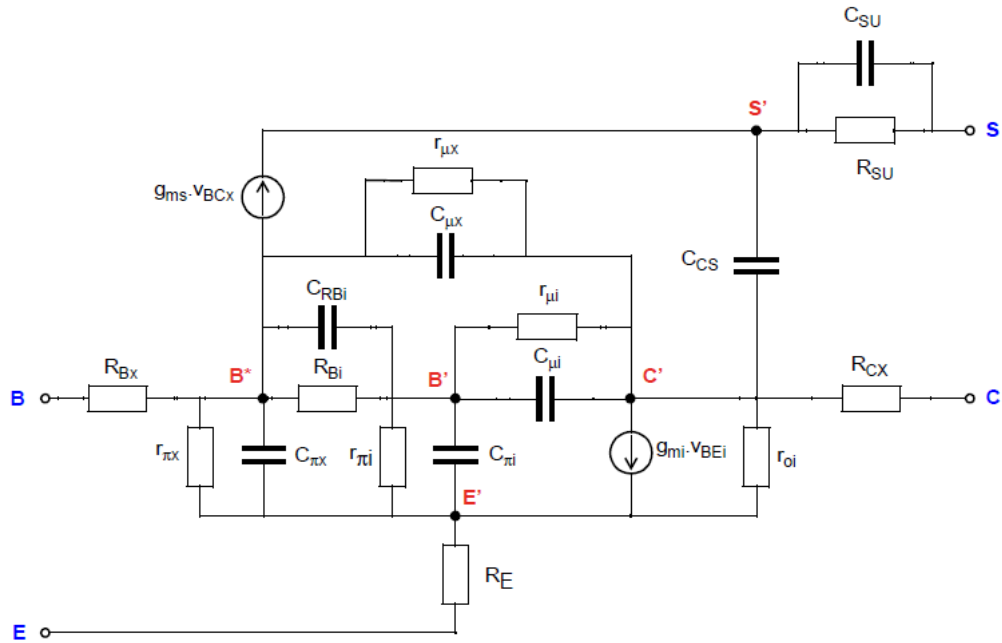
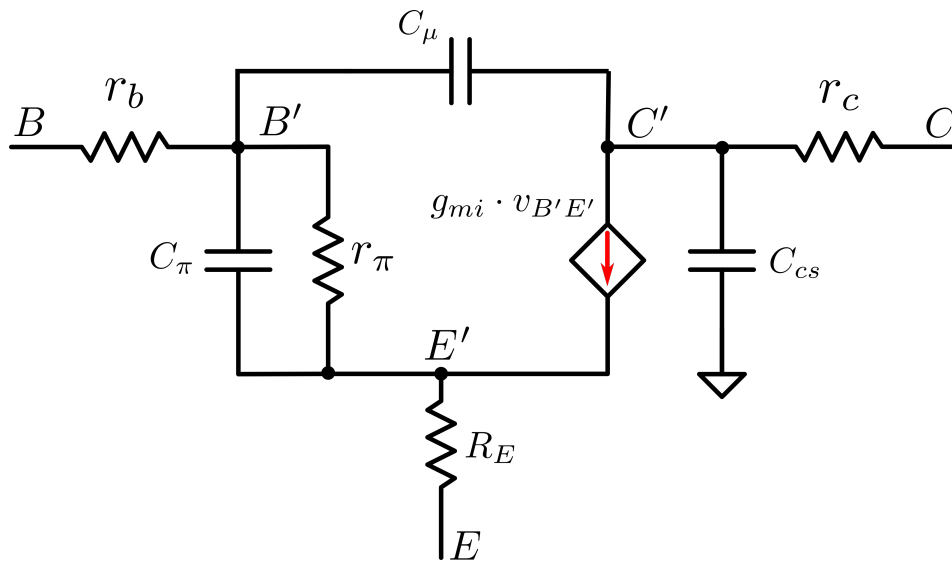Figure A.1: HiCUM/L2 small-signal equivalent circuit

Figure A.2: HiCUM/L2 small-signal simplified model

the generalized time constant method, introduced in [20]. It allows to derive the frequency response of an electrical network with multiple interacting capacitors through successive straightforward calculations. It is better to clarify the notation used in the following:

R_x^y is the resistance seen by capacitor x with capacitor(s) y shorted, and will be used to compute poles expressions. If $y = 0$ the equivalent resistance is computed with all the other capacitors being open circuits.

R_{0x}^y follows the same approach, but is linked to the zeroes of the circuit, thus the output is forced at zero while the input is considered to be active.

We can split the PA into two stages. The first common-emitter stage is characterized by a DC voltage gain equal to:

$$G_I(0) = \frac{v_{out,I}}{v_{in,I}}(0) = -\frac{gm_1 R_{L,I}}{1 + gm_1 R_{E,1}} \tag{A.4}$$

where $R_{L,I}$ is the resistance loading the first stage, and it is equal to the input resistance of the second stage:

$$R_{L,I} = R_{E,2} + \frac{1}{gm_2} + \frac{R_{B,2}}{gm_2 r_{\pi,2}} \cong R_{E,2} + \frac{1}{gm_2} \tag{A.5}$$

The second stage, instead, has a DC voltage gain equal to:

$$G_{II}(0) = \frac{v_{out,II}}{v_{in,II}}(0) = \frac{gm_2 R_L}{1 + gm_2 R_{E,2}} \tag{A.6}$$

In order to keep the notation simple, we will now study the frequency behavior of the first stage, and all the quantities will be referred to the common-emitter transistor, omitting the subscript. We will embed source resistance into base, and load resistance into collector, thus setting:

$$R_B = r_b + R_{in} \quad \text{and} \quad R_C = r_c + R_{L,I} \tag{A.7}$$

The AC response of the stage can be expressed as:

$$G_I = G_I(0) \cdot \frac{1 + a_1 s + a_2 s^2 + a_3 s^3}{1 + b_1 s + b_2 s^2 + b_3 s^3} \tag{A.8}$$

being the coefficients for the poles:

$$b_1 = C_\pi R_\pi^0 + C_\mu R_\mu^0 + C_{cs} R_{cs}^0 \tag{A.9}$$

$$b_2 = C_\pi C_\mu R_\pi^0 R_\mu^\pi + C_\pi C_{cs} R_\pi^0 R_{cs}^\pi + C_\mu C_{cs} R_\mu^0 R_{cs}^\mu \tag{A.10}$$

$$b_3 = C_\pi C_\mu C_{cs} R_\pi^0 R_\mu^\pi R_{cs}^{\pi,\mu} \tag{A.11}$$

and for the zeroes:

$$a_1 = C_\pi R_{0,\pi}^0 + C_\mu R_{0,\mu}^0 + C_{cs} R_{0,cs}^0 \tag{A.12}$$

$$a_2 = C_\mu C_\pi R_{0,\mu}^0 R_{0,\pi}^\mu + C_{cs} C_\pi R_{0,cs}^0 R_{0,\pi}^{cs} + C_\mu C_{cs} R_{0,\pi}^0 C_{0,cs}^\mu \tag{A.13}$$

$$a_3 = C_\mu C_\pi C_{cs} R_{0,\mu}^0 R_{0,\pi}^\mu R_{0,cs}^{\pi,\mu} \tag{A.14}$$

Note that eqq. A.13 and A.14 have been formulated with swapped capacitors; the result is independent on the order of the products, but, when handling second order terms or higher, some combinations may bring to indeterminate forms of the type $0 \cdot \infty$.

We get:

$$R_\pi^0 = \frac{R_B + R_E}{1 + gm_1 R_E} \tag{A.15}$$

$$R_\mu^0 = R_B + R_C + \frac{g_m R_B R_C - \frac{R_B^2}{r_\pi}}{1 + g_m R_E} \cong R_B + R_C + \frac{g_m R_B R_C}{1 + g_m R_E} \tag{A.16}$$

Note that the previous simplification is surely valid, since:

$$\frac{R_B{}^2}{r_\pi} \ll g_m R_B R_C \implies \frac{R_B}{R_C} \ll g_m r_\pi \equiv \beta \tag{A.17}$$

Eq. (A.16) can be well justified noticing that it can be reduced to the form:

$$R_\mu^0 = R_C + R_B(1 - G_I) \tag{A.18}$$

And we can easily recognize the Miller-effect magnification factor acting on the collector-base bridging capacitance.

$$R_{cs}^0 = R_C \tag{A.19}$$

Moving to second order terms, we find:

$$R_\mu^\pi = R_C + (R_B//R_E) \tag{A.20}$$

$$R_{cs}^\pi = R_C \tag{A.21}$$

$$R_{cs}^\mu = (\frac{1}{g_m}//r_\pi)(1 + g_m R_E) \cong \frac{1 + g_m R_E}{g_m} \tag{A.22}$$

and for the third order:

$$R_{cs}^{\pi,\mu} = R_C//R_B//R_E \tag{A.23}$$

For the zeroes, instead:

$$R_{0,\pi}^0 = 0 \tag{A.24}$$

$$R_{0,\mu}^0 = -\left(R_E + \frac{1}{g_m} + \frac{R_E}{g_m r_\pi}\right) \cong -\left(R_E + \frac{1}{g_m}\right) \tag{A.25}$$

$$R_{0,cs}^0 = 0 \tag{A.26}$$

Being eq. (A.25) < 0 we immediately recognize the right half-plane zero arising from the collector-base bridging capacitance which creates a feed-forward current path within the stage.

$$R_{0,\pi}^{\mu} = \frac{R_E}{1 + g_m R_E} \tag{A.27}$$

$$R_{0,\pi}^{cs} = 0 \tag{A.28}$$

$$R_{0,cs}^{\mu} = 0 \tag{A.29}$$

$$R_{0,cs}^{\pi,\mu} = 0 \tag{A.30}$$

The second stage is characterized by:

$$R_B = r_b \quad \text{and} \quad R_C = r_c + R_L \tag{A.31}$$

and its AC response will be described by:

$$G_{II} = G_{II}(0) \cdot \frac{1 + a_1 s + a_2 s^2 + a_3 s^3}{1 + b_1 s + b_2 s^2 + b_3 s^3} \tag{A.32}$$

Once studying the poles, the circuit is topologically identical to the common-emitter, being the signal generator switched off, with the only difference that R_B and R_C are the ones defined in (A.31). We can conclude that equivalent resistances for the poles are given by eqq. (A.15) - (A.23).

The coefficients for the zeroes are expressed by eqq. (A.12) - (A.14) whilst the equivalent resistances for the zeroes of the CB are:

$$R_{0,\pi}^0 = 0 \tag{A.33}$$

$$R_{0,\mu}^0 = R_B \tag{A.34}$$
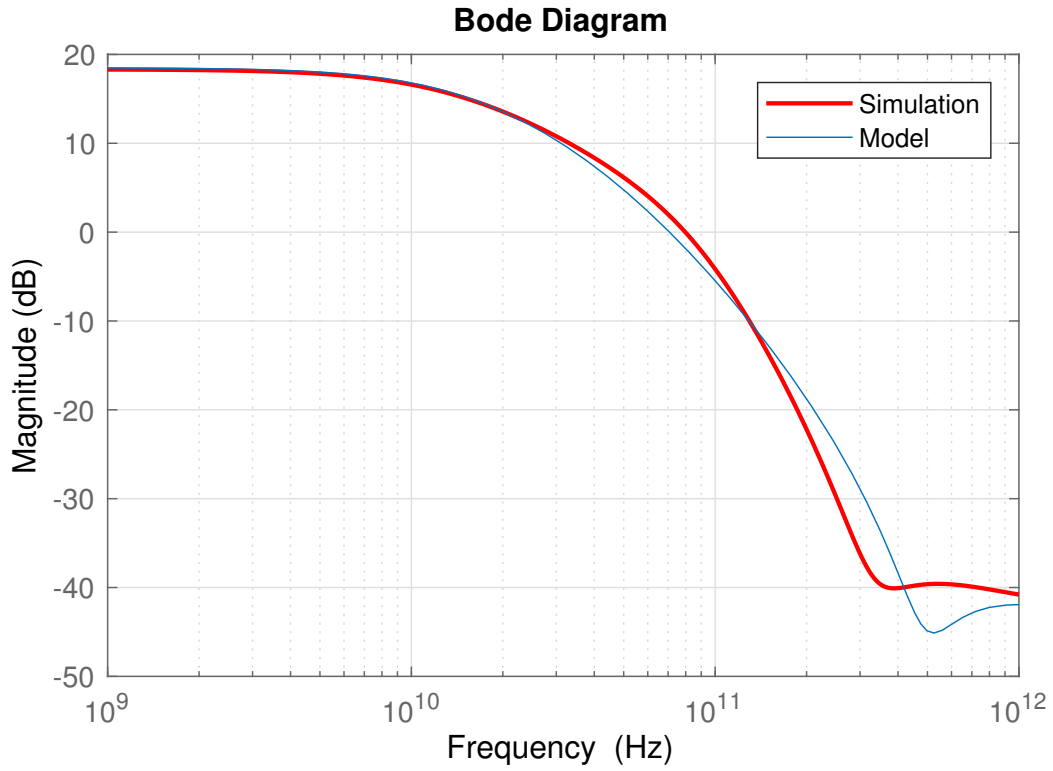
Figure A.3: PA voltage gain: Simulation and Simplified HiCUM/L2 model compared

$$R_{0,cs}^0 = 0 \tag{A.35}$$

$$R_{0,\pi}^\mu = r_\pi // \frac{1}{g_m} \tag{A.36}$$

$$R_{0,cs}^\mu = 0 \tag{A.37}$$

The voltage gain of the PA is reported in fig. A.3. The simplified model reasonably fits the frequency behavior of the stage in the band of interest and is even able to roughly catch the high-frequency second-order zero introduced by the current buffer.
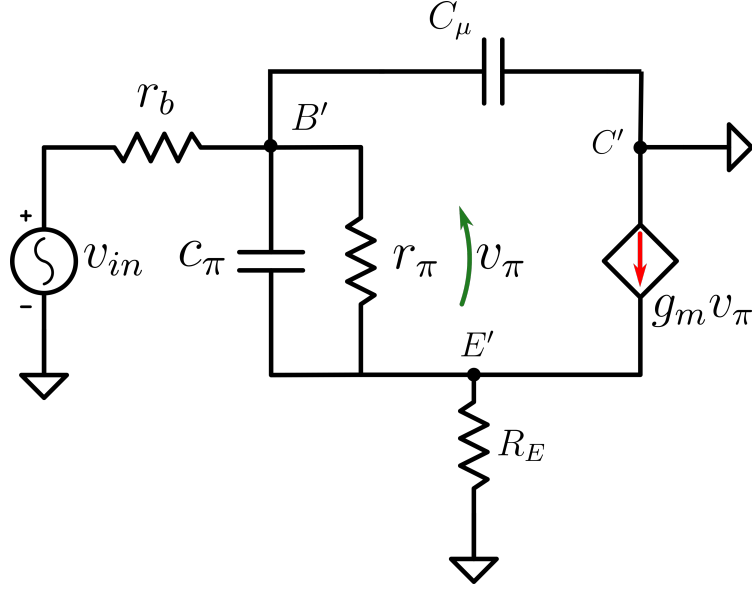
Figure A.4: Bipolar transistor input impedance evaluation circuit

A.2 Bipolar transistor: input impedance

We want now to justify the input impedance used in section 2.3 to derive the power gain of the PA.

We can look again at fig. A.2 and slightly simplify the discussion remembering that the first stage of the PA is connected to a low impedance node, thus we introduce the scheme of fig. A.4.

We can study the DC behavior, first. We get:

$$\frac{v_{in}}{i_{in}}(0) = R_E(1 + g_m r_\pi) + r_\pi + r_b \tag{A.38}$$

The π impedance is defined as:

$$Z_\pi = \frac{r_\pi}{1 + sC_\pi r_\pi} \tag{A.39}$$

We can write a couple of Kirchhoff's equations for the stage:

$$\begin{cases} v_{in} = v_\pi \left(g_m + \frac{1}{Z_\pi} \right) R_E + v_\pi + r_b i_{in} \\ i_{in} = \frac{v_\pi}{Z_\pi} + \left[v_\pi \left(g_m + \frac{1}{Z_\pi} \right) R_E + v_\pi \right] \cdot sC_\mu \end{cases} \quad (A.40)$$

By rearranging the (A.40), we get to:

$$i_{in} = \frac{v_{in} - r_b i_{in}}{K_E + \dfrac{R_E}{Z_\pi}} \cdot \left[\frac{1}{Z_\pi} + sC_\mu \left(K_E + \frac{R_E}{Z_\pi} \right) \right] \quad (A.41)$$

Where the coefficient K_E accounts for emitter degeneration and is equal to:

$$K_E = 1 + g_m R_E \quad (A.42)$$

We want to look more carefully at the term

$$K_E + \frac{R_E}{Z_\pi} = 1 + g_m R_E + \frac{R_E(1 + sC_\pi r_\pi)}{r\pi} \quad (A.43)$$

The product $C_\pi r_\pi$ accounts for the low frequency pole of the bipolar. Since we want to focus our interest on a much higher frequency range, we can introduce an approximation for the so-called medium-frequency, where the (A.43) becomes:

$$K_E + \frac{R_E}{Z_\pi} \cong 1 + g_m R_E + sC_\pi R_E = K_E + sC_\pi R_E \quad (A.44)$$

We focus now on the term:

$$\frac{1}{Z_\pi} + sC_\mu \left(K_E + \frac{R_E}{Z_\pi} \right) \quad (A.45)$$

Which, at medium-frequency, can be re-written as:

$$\frac{1}{Z_\pi} + sC_\mu(K_E + sC_\pi R_E) \cong s(C_\pi + K_E C_\mu) + s^2 C_\mu C_\pi R_E \quad (A.46)$$

If we neglect the second order term, we find:

$$\frac{1}{Z_\pi} + sC_\mu \left(K_E + \frac{R_E}{Z_\pi} \right) \cong s(C_\pi + K_E C_\mu) \quad (A.47)$$

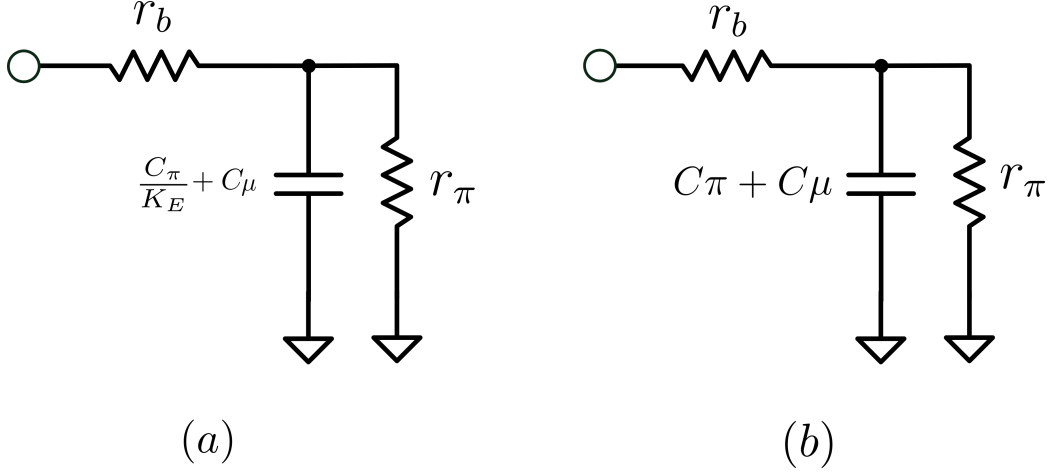(a) (b)

Figure A.5: Bipolar input impedance models for small emitter degeneration and load impedance

After some manipulations on the (A.41), we can derive:

$$\frac{v_{in}}{i_{in}} = \frac{K_E + sC_\pi R_E + sr_b(C_\pi + K_E C_\mu)}{s(C_\pi + K_E C_\mu)} \tag{A.48}$$

We may wonder whether the following relation is valid or not:

$$C_\pi R_E \overset{?}{\ll} r_b(C_\pi + K_E C_\mu) \tag{A.49}$$

Since $g_m R_E$ is around unity, C_μ is much smaller than C_π and R_E is much smaller than r_b, we can write:

$$c_\pi R_E \ll C_\pi r_b \implies R_E \ll r_b \tag{A.50}$$

Thus we can conclude that the input impedance of the transistor, at MF, is:

$$\frac{v_{in}}{i_{in}}(MF) = \frac{K_E + sr_b(C_\pi + K_E C_\mu)}{s(C_\pi + K_E C_\mu)} = r_b + \frac{1}{s\left(\frac{C_\pi}{1+g_m R_E} + C_\mu\right)} \tag{A.51}$$

We can observe that the (A.51) expresses the medium frequency response of the network reported in fig. (A.5 a).

The model used in the computation of power gain in section 2.3 is instead the one depicted in fig. [A.5 (b)].

In the case of our PA, K_E is around 1.3, thus the approximation is reasonable and allows us to re-use the equations derived with null emitter resistance, at the input side, simplifying the discussion on power gain correction in presence of small degeneration.
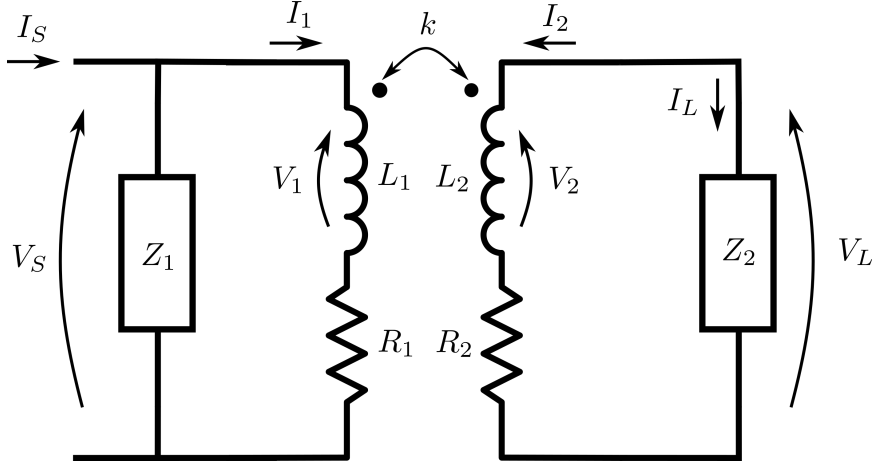
Figure A.6: Doubly-tuned transformer with inductors' series resistors

A.3   Doubly-tuned transformer: transimpedance

It may be useful to derive the analytical expression of the transimpedance Z_{21} for the doubly-tuned-transformer-based matching network with inductors' finite quality factor, discussed in section 1.1.

The network is reported in fig. (A.6); generic impedances Z_1, Z_2 are connected at input and output side, respectively. In our case Z_1 accounts for primary side capacitance; Z_2 embeds secondary capacitance which is in parallel with the load resistance:

$$Z_1 = \frac{1}{sC_1} \quad \text{and} \quad Z_2 = \frac{R_L}{1 + sC_2 R_L} \tag{A.52}$$

R_1 and R_2 model the inductors' series resistance which is linked to the inductor quality factor Q through:

$$Q = \frac{\omega L}{R} \tag{A.53}$$

We can write the well known expressions that relate voltages and currents

in a transformer:

$$\begin{cases} V_1 = L_1 s I_1 + M s I_2 \\ V_2 = M s I_1 + L_2 s I2 \end{cases} \tag{A.54}$$

where M is the magnetic coupling defined as:

$$M = k\sqrt{L_1 L_2} \tag{A.55}$$

By rearranging these expressions, we get:

$$I_1 = \frac{V_1 - M s I_2}{L_1 s} \tag{A.56}$$

Then, by substituting the previous equation in the (A.54), we get:

$$V_2 = M s \left(\frac{V_1 - M s I_2}{L_1 s} \right) + L_2 s I_2 \tag{A.57}$$

Note that V_2 is equal to $V_L - R_2 I_2$; thus:

$$V_L = \frac{M}{L_1} V_1 + I_2 \left(L_2 s + R_2 - \frac{M^2 s}{L_1} \right) \tag{A.58}$$

Looking at the primary side, we can write:

$$V_S = Z_1(I_S - I_1) = R_1 I_1 + V_1 \tag{A.59}$$

and

$$V_1 = Z_1(I_S - I_1) - R_1 I_1 = Z_1 I_S - I_1(Z_1 + R_1) \tag{A.60}$$

Giving:

$$V_1 = Z_1 I_S - \frac{V_1 - M s I_2}{L_1 s}(Z_1 + R_1) \tag{A.61}$$

After some manipulations, and combining with the (A.58), we can write:

$$\begin{cases} V_L = \dfrac{M}{L_1}V_1 - \dfrac{V_L}{Z_2}\left(L_2s + R_2 - \dfrac{M^2 s}{L_1}\right) \\[4mm] V_1 = \dfrac{Z_1 I_S}{1 + \dfrac{Z_1 + R_1}{L_1 s}} - \dfrac{\dfrac{M}{L_1}(Z_1 + R_1)}{1 + \dfrac{Z_1 + R_1}{L_1 s}} \cdot \dfrac{V_L}{Z_2} \end{cases} \tag{A.62}$$

from the previous system we can finally get:

$$\frac{V_L}{I_S} = Z_{21} = \frac{\dfrac{M}{L_1} \cdot \dfrac{Z_1}{1 + \dfrac{Z_1 + R_1}{L_1 s}}}{1 + \dfrac{L_2 s + R_2 - \left(\dfrac{M^2 s}{L_1}\right)}{Z_2} + \dfrac{M^2(Z_1 + R_1)}{L_1{}^2 Z_2\left(1 + \dfrac{Z_1 + R_1}{L_1 s}\right)}} \tag{A.63}$$

Figure (A.7) shows the magnitude of eq. (A.63) versus frequency for the matching network dimensioned in section 1.4.1, before and after pre-emphasis for losses compensation.
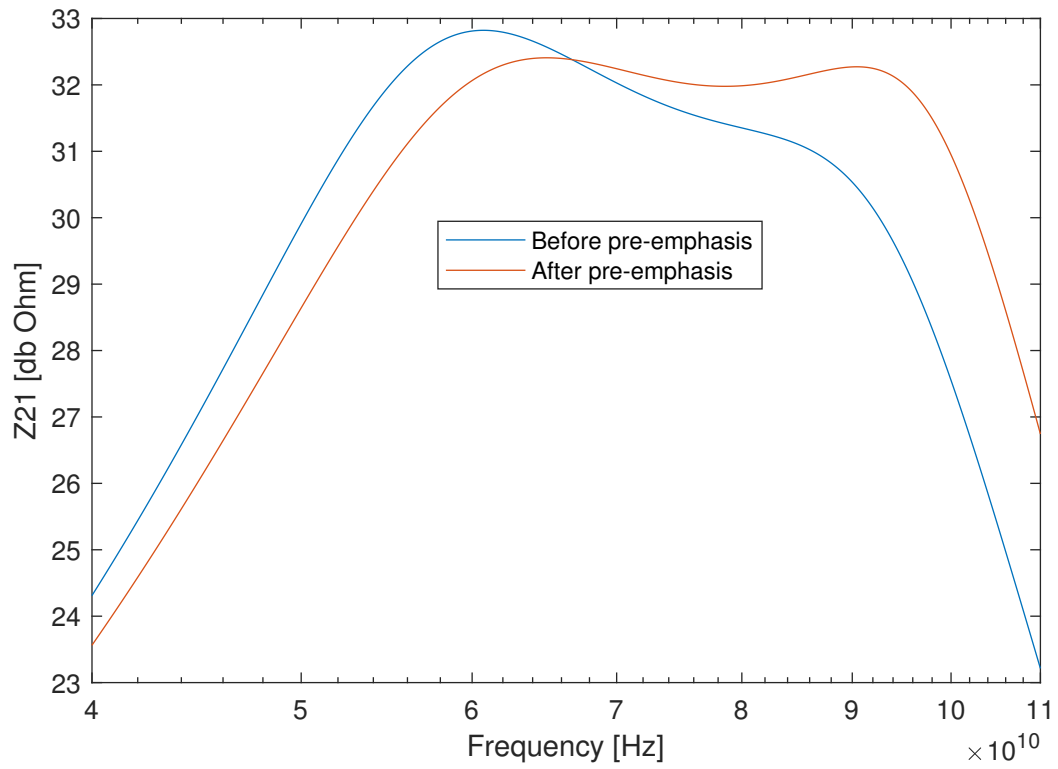
Figure A.7: Analytic evaluation of the transimpedance for the lossy doubly-tuned transformer dimensioned in section 1.4.1

Bibliography

[1] B. Ayvazian and C. Hetting, *Second generation E-Band solutions: opportunities for carrier-class LTE backhaul.* Heavy Reading, Feb 2013.

[2] D. M. Pozar, *Microwave Engineering.* John Wiley and Sons Inc, 2011.

[3] A. S. Gilmour, *Microwave Tubes.* Artech House Publishers, 1986.

[4] M. Vigilante and P. Reynaert, *5G and E-Band Communication Circuits in Deep-Scaled CMOS.* Springer, 2019.

[5] H. W. Bode, *Network analysis and feedback amplifier design.* D. Van Nostrand, 1945.

[6] R. M. Fano, "Theoretical limitations on the broadband matching of arbitrary impedances," Technical report (Massachusetts Institute of Technology. Research Laboratory of Electronics), no.41., 1948.

[7] D. Pi, B. Chun, and P. Heydari, "A synthesis-based bandwidth enhancement technique for cmos amplifiers: Theory and design," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 392–402, Feb 2011.

[8] B. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1263–1270, Aug 2004.

[9] A. Mazzanti and A. Bevilacqua, "Second-order equivalent circuits for the design of doubly-tuned transformer matching networks," *IEEE Transac-*

tions on Circuits and Systems I: Regular Papers, vol. 65, pp. 4157–4168, Dec 2018.

[10] S. C. Cripps, *Advanced Techniques in Rf Power Amplifier Design.* Artech House, 2002.

[11] R. Gilmore and L. Besser, *Practical RF Circuit Design for Modern Wireless Systems, Volume Ii: Active Circuits.* Artech House, 2003.

[12] E. Rahimi, J. Zhao, F. Svelto, and A. Mazzanti, "High-efficiency sige-bicmos *e* -band power amplifiers exploiting current clamping in the common-base stage," *IEEE Journal of Solid-State Circuits*, vol. 54, pp. 2175–2185, Aug 2019.

[13] S. A. Maas, *Nonlinear Microwave and Rf Circuits, Second Edition.* Artech House, 2003.

[14] L. Iotti, A. Mazzanti, and F. Svelto, "A low-power 64-84ghz frequency quadrupler based on transformer-coupled resonators for e-band backhaul applications," in *2016 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 1–4, June 2016.

[15] *Agilent AN 154 S-Parameter design.* Agilent Technologies Inc. Application Note, 2000.

[16] J. Verspecht, "Large-signal network analysis," *IEEE Microwave Magazine*, vol. 6, pp. 82–92, Dec 2005.

[17] V. Rizzoli, A. Lipparini, and F. Mastri, "Computation of large-signal s-parameters by harmonic-balance techniques," *Electronics Letters*, vol. 24, pp. 329–330, March 1988.

[18] M. Bassi, J. Zhao, A. Bevilacqua, A. Ghilioni, A. Mazzanti, and F. Svelto, "A 40-67 ghz power amplifier with 13 dbm psat and 16%

pae in 28 nm cmos lp," *Solid-State Circuits, IEEE Journal of*, vol. 50, pp. 1618–1628, 07 2015.

[19] M. Schröter and A. Chakravorty, *Compact Hierarchical Bipolar Transistor Modeling With Hicum.* World Scientific, 2010.

[20] A. Hajimiri, "Generalized time- and transfer-constant circuit analysis," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 6, pp. 1105–1121, 2010.

Ringraziamenti

Desidero ringraziare il Professor Salvatore Levantino per avermi concesso la possibilità di esprimere la mia passione all'interno di un ambiente stimolante quale il laboratorio di circuiti integrati ad alta frequenza del Politecnico di Milano.

Ringrazio il Professor Carlo Samori per i consigli dispensati.

Un grazie di cuore al Dottor Karman, Saleh, che mi ha supportato (e sopportato) durante questo anno, dimostrando sempre un eccezionale attaccamento al lavoro. Ma ringrazio infinitamente tutti i ragazzi del lab, a partire da Francesco, con Luca, Dago e Mauro. E' stato un anno incredibile, ricco di crescita, ma anche di momenti indimenticabili, comprese le pizzate nelle nottate di lavoro...

Studiare ingegneria al Politecnico mi ha fatto diventare parte di una grande famiglia e tutte le persone che ho incontrato durante questo meraviglioso percorso hanno contribuito a farmi arrivare fino a qui. Mi sarebbe impossibile non nominare Lucio, Paolo e Riccardo che, insieme a Fabio, Luca e Daniele, hanno costituito dei pilastri fondamentali in questi anni, tanto durante il Master, quanto durante il triennio.

Le parole non bastano per ringraziare la mia famiglia.

Guglielmo