POLITECNICO
MILANO 1863

SCUOLA DI INGEGNERIA INDUSTRIALE
E DELL'INFORMAZIONE

Executive Summary of the Thesis

High Mobility in Ge Quantum Wells: Hall Bar Characterization for Semiconductor Qubits

Laurea Magistrale in Engineering Physics - Ingegneria Fisica

Author: Luca Nardelli

Advisor: Prof. Daniel Chrastina

Co-advisors: Prof. Giovanni Isella, Dr. Stefano Calcaterra

Academic year: 2025-2026

---

1. Introduction

Quantum computing has become an important research topic in the scientific community because of the many applications it offers. One can think of cybersecurity, where quantum encryption algorithms have become more and more important over the years, but also of molecular simulations, which are hard to tackle with classical hardware.
However, despite some exciting results, no real breakthrough in the implementation of the qubit has been reached. A promising realization is the one created inside a two dimensional carrier gas, hosting two coupled quantum dots. This realization is characterized by a very high coherence time and good integration with classical hardware, making it possible to implement the latter in synergy with the qubit system [1, 2, 3].

1.1. Objective

This implementation is hosted in a Heterostructure-MOS (Metal-oxide-semiconductor, HMOS) is needed. The quantum well (QW) formed inside this structure is perfect for confining carriers in the growth direction, and the gate bias extends the confinement in the other two directions. Very high mobility samples are needed for creating these types of QW, as scattering decreases the overall coherence time of the qubit [4]. The study presented here makes use of a QW designed in a *Type-II Band Alignment* as a channel to confine a 2D hole gas (2DHG), which has been demonstrated to reach mobility as high as $\sim 10^5$ cm^2/Vs [5].
For the first time, gated Hall bars were fabricated directly at L-NESS in the Polifab cleanrooms. The scope of the thesis is to investigate the manufacturing process, particularly in the Atomic Layer Deposition (ALD) and Etching processes, to characterize the Hall bar fabrication procedure.
Furthermore, high mobility Ge/SiGe HMOS have been characterize, which are designed for fabricating coupled spin qubits. This analysis has been conducted at low temperatures and high magnetic fields. Thanks to the Shubnikov-de Haas (SdH) and quantum Hall effect (QHE) analysis, valuable information about the system can be retrieved [6, 7].

2. Samples and Methods

For the analysis, different stacks have been grown using a Low Energy Plasma Enhanced

Chemical Vapor Deposition (LEPECVD) technique [8], as it has demonstrated great results in the past [9]. Two types of structures have been utilized, both presenting a Ge channel.
The first kind of sample will be referred to as "Ge/SiGe HMOS" samples, while the second will be "ultra-thin Ge" samples. Both the structures are represented in details in Figure 1. Hall bars have been fabricated with both of them, at ISTA, and at Polifab respectively. The two manufacturing processes implemented are fairly similar but using different machinery, and only the structures fabricated at Polifab will be characterized.

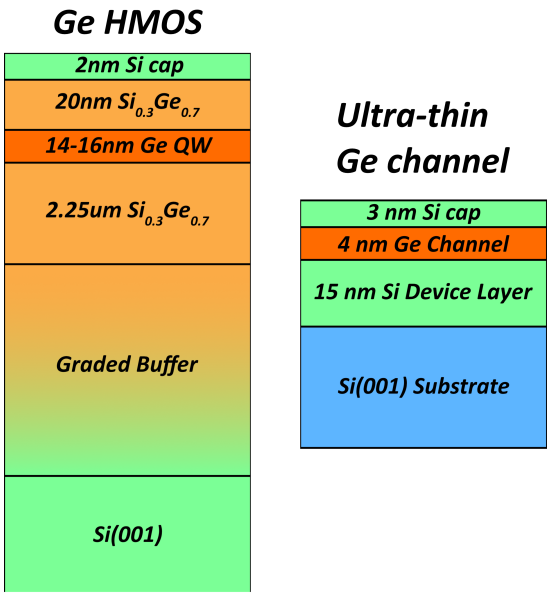

Figure 1: Representation of Material stacks utilized for Ge/SiGe HMOS samples (left) and ultra-thin Ge channel samples (right).

2.1. Fabrication

Hall bar lithographic masks have been prepared for the fabrication steps. The chosen Hall bar design is very simple (shown in Figure 2), as the focus of the work was to set a starting point for a fabrication process to further develop in the future.
Starting from the samples, a lithographic step has been performed with a Heidelberg MLA100 using a negative resist (AZn15XT) and TMAH-based developer (AZ726 MIF) to define the area of the contacts. Then, the surface has been HF treated before 7 nm of titanium and 150 nm of gold have been deposited using a Leybold L560E evaporator. A lift-off has been performed with

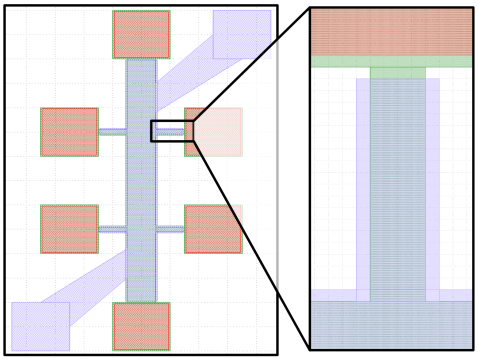

Figure 2: Hall bar design, with a close-up on a Hall bar leg. One can see part of the leg not being covered by the gate.

acetone and isopropyl alcohol to remove the excess gold.
Another lithographic process with a positive resist (AZ15XT) and AZ726 MIF as a developer is then used to define the hall bar structure. Then, a Reactive Ion Etching (RIE) step is performed using an SPTS Omega Synapse 200 LPX. A target thickness of $\sim$ 260 nm of material has been etched away to define the Hall bar mesa, thanks to a Bosch recipe with alternating steps of SF_6 and C_4F_8. P1331 has been used as a stripper to remove the excess resist.

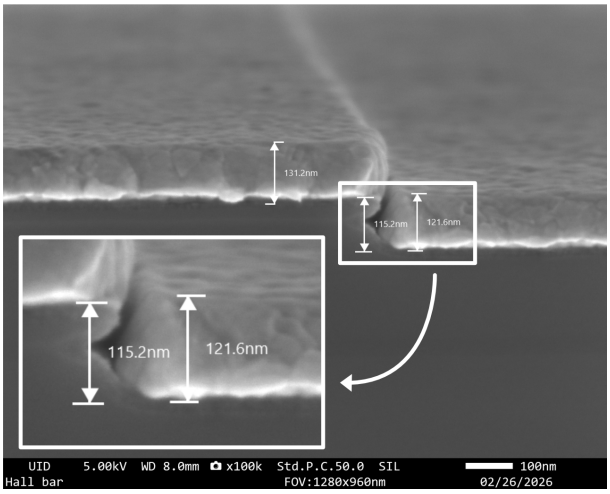

Figure 3: SEM image taken on the body of the Hall bar. One can see both the gold and the oxide layers, as well as the etching profile. From the image, it is really hard to predict the thickness of the oxide layer in this region.

Lastly, Atomic Layer Deposition (ALD) is performed in a Beneq TFS 200 tool to deposit 20 nm of Al_2O_3 across the device. This has been done with thermal (210°C) and plasma (90°C) tech-

niques. The thickness was measured with an ellipsometer, resulting in a value of 20.58 nm. The oxide layer has also been characterized by Scanning Electron Microscope (SEM) imaging by taking a cross-sectional image of the device (Figure 5).
The gate is then deposited in a similar way as the contacts. Note that both gated and non-gated Hall bars have been fabricated. The devices were cleaved and then inserted into the cryostat holders.

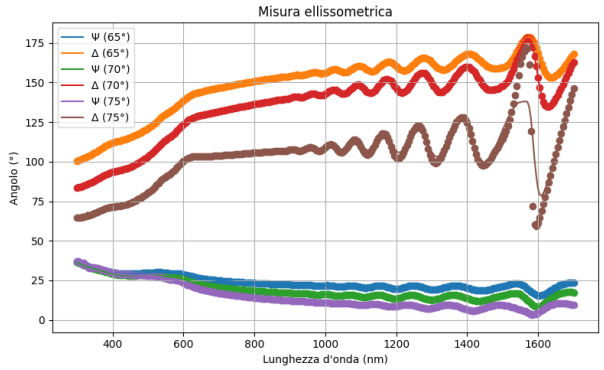

Figure 4: Oxide spectra taken thanks to a J.A. Woollam VASE Ellipsometer. The spectra were fitted according to a multilayer model using the tabulated optical constants of Si, Ge and Al_2O_3 while leaving the thickness of the layers as free parameters.

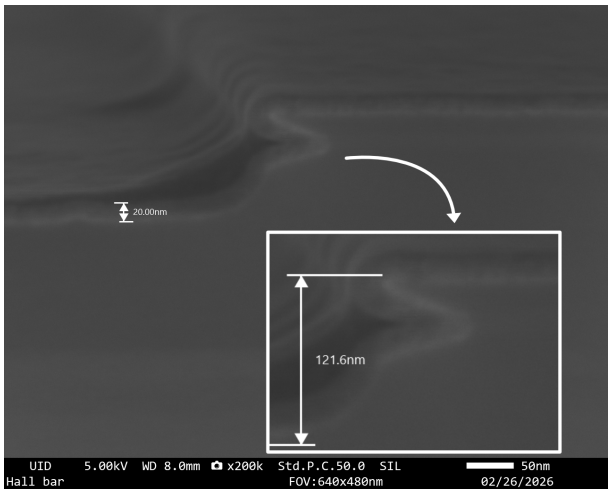

Figure 5: Etching profile image taken by SEM. The etching rate has been lower than expected, as out of the 260 nm target, only about 120 nm have been etched. In the image, one can also see the perfect conformality of the oxide layer, as expected from the ALD technique.

2.2. Measurements

Samples have been measured at room temperature and at very low temperatures (down to $4K$), also using high magnetic fields (up to $7.5T$). These conditions have been achieved through the use of a Cryogen Free Element System (CFES) from Cryogenic. In this setup, a He^4 loop is used to cool down two cryogenic stages to $4K$, as well as instruments and sensors. Inside the inner stage, there is a superconducting coil that can generate very high magnetic fields thanks to the constant cooling the cryostat provides. In this framework, both ρ_{xx} and ρ_{xy} have been measured at different values of temperature and magnetic field.

2.3. Data Analysis

Different quantities can be extracted from the analysis of the data. From the profiles of ρ_{xy} and ρ_{xx} at low field, R_H can be obtained, and thus n_{2D} and μ.
To analyze SdH oscillations, the magnetoresistance contribution can be filtered out from the profile of ρ_{xx} thanks to the Savitzky-Golay method to isolate the oscillations. Then, the same minima/maxima of the oscillations can be considered at different temperatures, and by fitting the Equation 1 in these points, a value of m^* has been obtained [10]. Similarly, different minima/maxima at the same temperature can be considered to fit the value of α.

$$\Delta\rho = 4\sum_{s=1}^{\infty}\frac{s\,\xi}{\sinh(s\,\xi)}\exp\left(-\frac{\pi\alpha s}{\mu B}\right) \times\cos\left(\frac{\pi h s n_s}{eB}-s\pi\right), \qquad (1)$$
$$\xi = \frac{2\pi^2 m^* k_B T}{e\,\hbar\,B}$$

A FFT analysis can also been performed. Oscillation frequency is directly proportional to the carrier density n_{SdH}, which has been compared with n_H for consistency. Starting from the cosine function in the Equation 1, one can extract the value of the Fermi vector k_F and Fermi energy E_F, and thus the value of n_s[11]:

$$E_F = \frac{\hbar^2 k_F^2}{2m^*} \qquad (2)$$
$$k_F^2 = 2\pi n_s \qquad (3)$$
$$n_s = \frac{e}{\pi\hbar\Delta(1/B)} \qquad (4)$$

Finally, percolation density can be extracted by applying increasing gate bias V_g and measuring how the conductivity σ varies with n_H. In this way, a $\sigma(n)$ plot can be created, and the percolation density formula can be fitted to obtain the percolation exponent p and percolation density n_p [12]:

$$\sigma \propto (n - n_p)^p \tag{5}$$

3. Sample Analysis

3.1. Ge/SiGe Quantum Well samples

3.1.1 Sample 11585

Sample 11585 features a 14 nm Ge QW in a HMOS structure, similar to that described in section 2. Both the gated and oxide-no-gate versions have been tested to characterize the effect of any residual charge in the deposited oxide that could activate the channel at low temperatures. In the case of the oxide-no-gate device, a body resistance of $\sim$ 39 kΩ has been measured at room temperature, and a substrate conduction of $\sim$ 80 kΩ has been found. At low temperatures, all carriers freeze-out, and as the gate is absent, inducing carrier population becomes impossible.

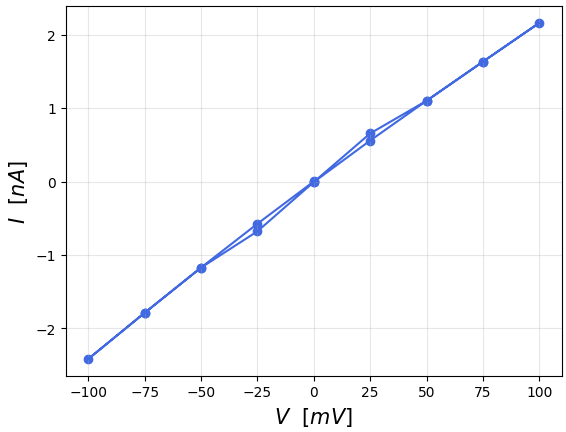

Figure 6: Sample 11585 $I(V)$ 4-probe measurement. The resistance has been estimated to be $\sim$ 38 kΩ.

The gated version has been more promising, but presented a strong leakage current between the channel and the gate. This current has been characterized at low temperature, creating an $I(V_g)$ curve for both the channel current and the gate current, represented in Figure 7. Due to the noise introduced by the high leakage current, the analysis of the magnetic phenomena of the sample has not been conducted.

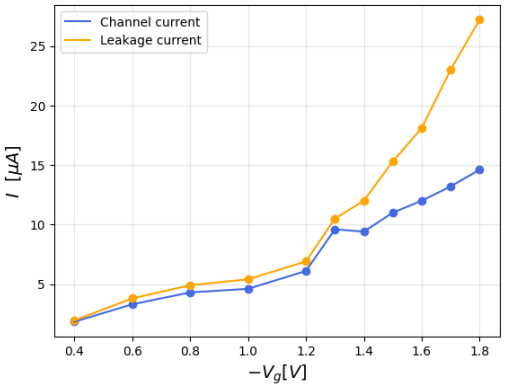

Figure 7: Sample 11585 gate current and channel current with respect to applied voltage to the gate, measured at $T = 6$ K. One can see the activation of the channel around $V_g \sim -1.35$ V, when the two currents become different.

3.1.2 Sample 11586

Sample 11586 features the same structure as that described in section 2, with a Ge QW width of 16 nm. Similar measurements to that of sample 11585 have been conducted, with also similar results. In this case, the leakage has been measured at room temperature as a preliminary characterization and is represented in Figure 8.

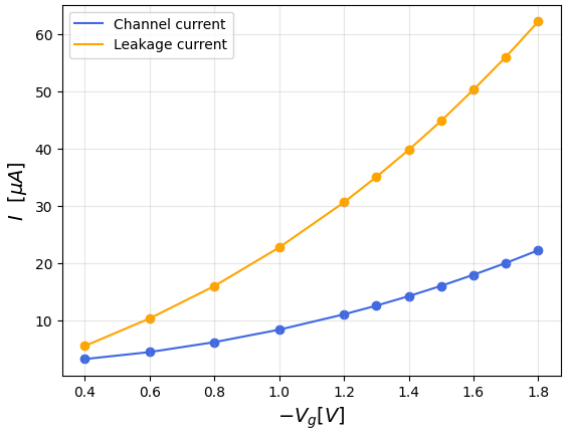

Figure 8: Sample 11586 gate current and channel current with respect to applied voltage to the gate, measured at $T = 6$ K.

3.2. Ultra-Thin Ge Samples

Sample 11607 and 11608 feature a 4 nm Ge channel grown at 200°C and 250°C respectively. For

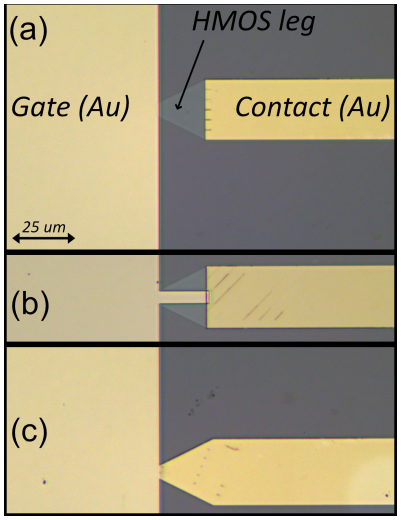

Figure 9: Hall bar legs in the studied designs. (a) no metal is deposited onto the leg. (b) The gate is positioned on top of the leg. (c) The pad metal is onto the leg, under the oxide.

every sample, three different Hall bar geometries were tested, with different leg contacts to avoid freeze-out at low temperatures.
On both samples, the analyzed Hall bars presented substrate conduction at room temperature, this makes the Ge channel impossible to decouple. Furthermore, some Hall bars exhibited leakage through the gate, making biasing impossible.

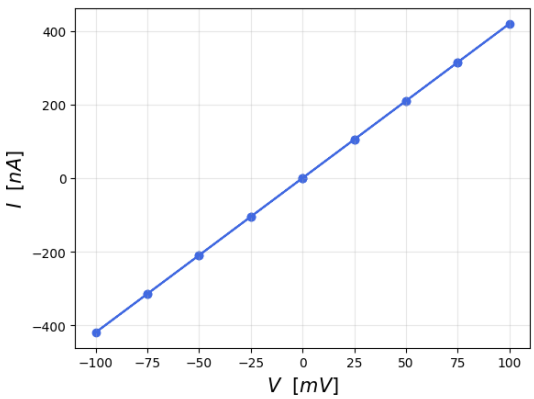

Figure 10: 11608 $I(V)$ curve measured at $T = 300$ K between the channel and the gate. One can see the perfectly ohmic $I(V)$ line typical of metal conduction, with a measured resistance of $\sim 230\ \Omega$

Only one structure presented no leakage and was tested at low temperature. In this case, the bias was applicable, but it had no influence on the Ge channel, and no window of T was found where freeze-out occur only for substrate conduction.

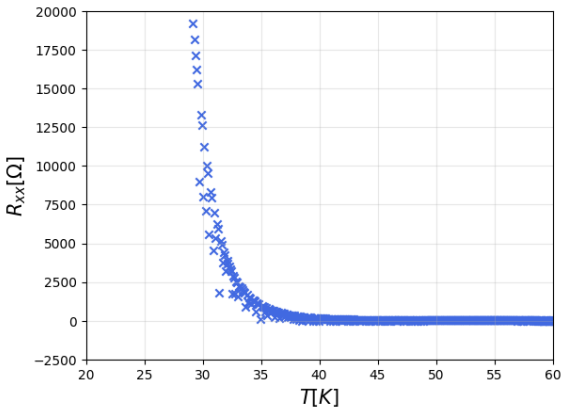

Figure 11: 11607 4-probe measurement of longitudinal resistance with respect to T. One can see that the freeze-out of carriers happens near 35 K, and below this value resistance becomes abruptly very high.

4. Conclusions

The study has established a fabrication process for Hall bars, by also characterizing critical steps in the manufacturing flow.
In the Polifab fabricated devices, out of the 260 nm target etching depth, only 120 nm have been removed. It is important to note that this should not influence any functionality of the device, as the reached depth is still higher than the Ge QW depth. The characterization set a reference for future developments in the implementation of this technique.
The leakage problem could lie in the oxide layer missing in a region of the Hall bar. The SEM and Ellipsometer characterizations reveal a high conformity of the Al_2O_3, which exclude a poor uniformity of the layer. Another hypothesis comes with the developer used for the subsequent lithographic step: AZ 726 MIF, which contains TMAH, a wet etchant for Al_2O_3. Even though the etch rate of such chemical on the oxide is very low, more testing is needed to understand if developer bath has created a hole in the layer, ruining the MOS structure.
In the case of ISTA manufactured Hall bars, the substrate conduction can be solved by utilizing an ultra-intrinsic substrate to isolate the Ge channel conduction and analysis. On the other hand, the leakage present on the devices is probably due to fabrication problems or mis-

alignment between lithographic masks. Nevertheless, feedback with ISTA research team will be fundamental in order to understand how to create a good design for future analysis.

References

[1] M. Veldhorst, C. H. Yang, J. C. C. Hwang, W. Huang, J. P. Dehollain, J. T. Muhonen, S. Simmons, A. Laucht, F. E. Hudson, K. M. Itoh, A. Morello, and A. S. Dzurak. A two-qubit logic gate in silicon. *Nature*, 526:410–414, 2015.

[2] Giordano Scappucci, Christoph Kloeffel, Floris A. Zwanenburg, Daniel Loss, Maksym Myronov, Jian-Jun Zhang, Silvano De Franceschi, Georgios Katsaros, and Menno Veldhorst. The germanium quantum information route. *Nature Reviews Materials*, 6(10):926–943, 2021.

[3] Yu-Cheng Li, Che-Hao Chang, Yu-Jui Wu, Chen-Yao Liao, and Jiun-Yun Li. Design guidelines for Si metal–oxide–semiconductor and Si/SiGe heterostructure quantum dots for spin qubits. *Applied Physics Letters*, 126(6):063502, February 2025.

[4] Alberto Mistroni, Marco Lisker, Yuji Yamamoto, Wei-Chen Wen, Fabian Fidorra, Henriette Tetzner, Laura K. Diebel, Lino Visser, Spandan Anupam, Vincent Mourik, Lars R. Schreiber, Hendrik Bluhm, Dominique Bougeard, Marvin H. Zoellner, Giovanni Capellini, and Felix Reichmann. High yield, low disorder Si/SiGe heterostructures for spin qubit devices manufactured in a BiCMOS pilot line. *Applied Physics Letters*, 127(8):083503, 08 2025.

[5] Stefano Calcaterra. Germanium quantum wells for semiconductor qubits. Tesi di laurea magistrale, Politecnico di Milano, Milano, Italy, 2021.

[6] T. Ando, A. B. Fowler, and F. Stern. Electronic properties of two-dimensional systems. *Reviews of Modern Physics*, 54(2):437–672, 1982.

[7] Gerald Bastard. *Wave Mechanics Applied to Semiconductor Heterostructures*. Monographies de physique. Les Editions de Physique; Wiley-Interscience, Les Ulis, France; New York, USA, 1988.

[8] D. Chrastina, B. Rössner, G. Isella, H. von Känel, J. P. Hague, T. Hackbarth, H.-J. Herzog, K.-H. Hieber, and U. König. LEPECVD – a production technique for SiGe MOSFETs and MODFETs. In Ehrenfried Zschech, Caroline Whelan, and Thomas Mikolajick, editors, *Materials for Information Technology: Engineering Materials and Processes*, pages 17–29. Springer, London, UK, 2005.

[9] Daniel Jirovec, Andrea Hofmann, Andrea Ballabio, Philipp M. Mutter, Giulio Tavani, Marc Botifoll, Alessandro Crippa, Josip Kukucka, Oliver Sagi, Frederico Martins, Jaime Saez-Mollejo, Ivan Prieto, Maksim Borovkov, Jordi Arbiol, Daniel Chrastina, Giovanni Isella, and Georgios Katsaros. A singlet-triplet hole spin qubit in planar Ge. *Nature Materials*, 20(8):1106–1112, 2021.

[10] Mildred Dresselhaus, Gene Dresselhaus, Stephen B. Cronin, and Antonio Gomes Souza Filho. *Solid State Properties: From Bulk to Nano*. Graduate Texts in Physics. Springer, 2018.

[11] P. T. Coleridge. Small-angle scattering in two-dimensional electron gases. *Physical Review B*, 44(8):3793–3801, 1991.

[12] Mario Lodari, Nico Hendrickx, William Lawrie, Tzu kan Hsiao, Lieven Vandersypen, Amir Sammak, Menno Veldhorst, and Giordano Scappucci. Low percolation density and charge noise with holes in germanium. *Mater. Quantum Technol.*, 1(1):011002, 2021.