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Statistical and Geometrical analysis of "Weak Cells" in the SDRAM based memory on Low Earth Orbiting satellites

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Abstract

This thesis addresses the characterization of different types of errors occurred in the Solid-State Mass Memory (SSMM) equipment aboard two Low Earth Orbit (LEO) satellites whose digital equipment was designed by Thales Alenia Space - Italia (TAS-I).

This type of memories are based on Synchronous Dynamic Random Access Memory (SDRAM) and they are characterized by intrinsic defects known as “Weak Cells", i.e. memory locations affected by electrical charge leakage especially visible when the device is exposed to high temperatures.

In this work the focus is the characterization of a leakage phenomenology that started since the early days in orbit on the first one of the two satellites. We will refer to it as Extremely Weak Cell (EWC) leakage phenomenon since it occurs in orbit when the equipment Thermal Reference Point (TRP) is at ambient temperature. This was never observed during on-ground tests validating the equipment for the space environment at that TRP temperature.

The analysis was carried out by combining information coming from different telemetries available in TAS-I archives. Each telemetry packet was processed through algorithms written in Python, which provided the logical addresses of the corrections performed onboard allowing to distinguish EWCs from other instantaneous radiative induced phenomena like Single Event Upsets (SEUs) and Single Event Functional Interrupts (SEFIs).

The results obtained from the first satellite were validated by repeating the same analysis on another digital equipment, twin to the previous one, onboard a second satellite that was launched two years later in the same orbital plane but subject to a different environmental radiation level.

Furthermore, the activation of EWCs on a single memory module was modelled using Autoregressive Moving Average (ARMA) models on different time scales. The obtained

model could be used to make predictions of EWC activations in the future.

Keywords: Satellite, LEO, SDRAM, Weak Cell, Extremely Weak Cell, ECC, EDAC, Corrections, Soft Error, Hard Error, Radiation, SSA, SEU, SEFI, Sun's cycle, Time Series, ARMA model.

Abstract in lingua italiana

Questa tesi affronta la caratterizzazione di diversi tipi di errori verificatisi nelle apparecchiature di memoria di massa a stato solido (SSMM) a bordo di due satelliti in orbita terrestre bassa (LEO) le cui apparecchiature digitali sono state progettate da Thales Alenia Space - Italia (TAS-I).

Questo tipo di memorie si basano su Synchronous Dynamic Random Access Memory (SDRAM) e sono caratterizzate da difetti intrinseci noti come "Weak Cells" (celle deboli), cioè locazioni di memoria interessate da perdite di carica elettrica, particolarmente visibili quando il dispositivo è esposto a temperature elevate.

In questo lavoro ci si concentra sulla caratterizzazione di una fenomenologia di perdita che è iniziata fin dai primi giorni in orbita sul primo dei due satelliti. Ci riferiremo ad esso con il nome di Extremely Weak Cell (EWC), poiché si verifica in orbita quando il punto di riferimento termico (TRP) dell'equipaggiamento è mantenuto a temperatura ambiente. Questo fenomeno non è mai stato osservato durante i test a terra che convalidavano l'apparecchiatura per l'ambiente spaziale a quella temperatura del TRP.

L'analisi è stata effettuata combinando le informazioni provenienti da diverse telemetrie disponibili negli archivi TAS-I. Ogni pacchetto telemetrico è stato elaborato attraverso algoritmi scritti in Python, che hanno fornito gli indirizzi logici delle correzioni eseguite a bordo permettendo di distinguere le EWC da altri fenomeni radiativi istantanei indotti come i Single Event Upsets (SEU) e i Single Event Functional Interrupts (SEFI).

I risultati ottenuti dal primo satellite sono stati convalidati ripetendo la stessa analisi su un secondo dispositivo, gemello al precedente, a bordo di un secondo satellite lanciato due anni dopo sullo stesso piano orbitale ma soggetto a un diverso livello di radiazione ambientale.

Inoltre, l'attivazione delle EWC su un singolo modulo di memoria è stata modellata

utilizzando modelli a media mobile auto regressivi (ARMA) su diverse scale temporali. Il modello ottenuto potrebbe essere utilizzato per fare previsioni sulle attivazioni delle EWC in futuro.

Parole Chiave: Satellite, LEO, SDRAM, Weak Cell, Extremely Weak Cell, ECC, EDAC, Correzioni, Soft Error, Hard Error, Radiazione, SSA, SEU, SEFI, Ciclo Solare, Serie Temporale, modello ARMA.

Important Disclaimer

This work was carried out between October 2022 and July 2023 at Thales Alenia Space - Italia Milan site in Gorgonzola, within the IVV, Testing & Fast Prototyping department of Computing, Data Handling & Science (CDHS) product line, on proprietary telemetry data of the Company ranging from 2014 to 2022 and resident in its central database. No scientific data was accessed or reviewed in the present thesis.

Details about both satellites examined in this thesis that may involve their identification are considered confidential by the Company and they will be avoided. For this reason the official names and acronyms will not be used. For example, we will refer to the spacecrafts using the names Satellite A and Satellite B.

In addition, references to the detailed functionality will not be reported, if not necessary to the description of the SDRAM correction algorithm for either radiative causes or leakage phenomena. However, the trasparency necessary to justify the project choices will be ensured without violating the non-disclosure agreements made with the host Entity.

List of Acronyms

Acronym	Description
ACF	AutoCorrelation Function
AIC	Akaike Information Criterion
ASW	Application Software
AR	AutoRegressive
ARIMA	AutoRegressive Integrated Moving Average
ARMA	AutoRegressive Moving Average
BIC	Bayesian Information Criterion
BOS	Big One-Shot
$\boldsymbol{C-S}$	Check-Symbols
CCSDS	Consultative Committee for Space Data Systems
CDHS	Computing Data Handling & Science
$\boldsymbol{E-TM}$	Emitted TM
ESR	Error-to-Signal Ratio
ECC	Error Correction Code
EDAC	Error Detection and Correction
EWC	Extremely Weak Cell
FDIR	Failure Detection Isolation and Recovery
FPGA	Field Programmable Gate Array
GPS	Global Position System
HW	Hardware
HE	Hard Error
IC	Integrated Circuit
MAE	Mean Absolute Error
MC	Memory Controller

Acronym	Description
MM	Memory Module
MA	Moving Average
$\boldsymbol{M-S}$	Multi-Shot
OBT	On Board Time
PACF	Partial AutoCorrelation Function
PCB	Printed Circuit Board
PDHT	Payload Data Handling & Transmission
RAM	Random Access Memory
RIC	Report Integrity Counter
RF	Radio Frequency
RFAA	Radio Frequency Antenna Assembly
RFTA	Radio Frequency Transmission Assembly
RMSE	Root Mean Squared Error
$\boldsymbol{S-S}$	Single-Shot
SAA	South Atlantic Anomaly
SC	Spacecraft
SS	SubSystem
SBC	Single Big Correction
SDRAM	Synchronous Dynamic Random Access Memory
SE	Soft Error
SEFI	Single Event Functional Interrupt
SESR	Soft Error Status Resgister
SEU	Single Event Upset
SPV	Supervisor Module
SSA	South Atlantic Anomaly
SSMM	Solid State Mass Memory
SW	Software
$\boldsymbol{TAS-I}$	Thales Alenia Space - Italia
TC	Telecommand
TCS	Thermal Control System
TID	Total Ionizing Dose

Acronym	Description
TM	Telemetry
TN	Technical Note
TX	Transmitter
TSOP	Thin Small Outline package

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Introduction

Electronic systems in space missions face significant challenges in maintaining proper functioning under harsh environmental conditions. SDRAM-based memory devices are widely used in space applications due to their high capacity and speed. The effects of radiation on the long-term reliability and performance of these memory devices in the space environment is the object of many studies. This is the first time that a telemetry dataset spanning multiple years has been analyzed in TAS-I for this aspect.

In the past, unexpected appearance of behavior in the already flying SSMM equipment on-board Satellite A led to the writing of two analyses by TAS-I, which considered only very restricted periods of time (a couple of months). The two Technical Notes (TNs) provided the guidelines for the development of this work, that spanned on all memory modules, along all years in orbit, on two satellites. These two satellites were launched in different years but in the same orbital plane below or just inside the inner Van Allen radiation belt.

The functioning of SDRAM-based memories are tested on ground with tools that simulate the space environment only for a very short period of time compared to the entire duration of a space mission. This type of memory is known to have intrinsic defects called “Weak Cells" which are visible only when the temperature of the Thermal Reference Point (TRP) of the equipment is driven during the test well above the ambient temperature.
This thesis aims to investigate and characterize the long-term appearance and evolution of a leakage phenomenon (that started since the early days in orbit and was never observed during on-ground tests) that we call "Extremely Weak Cells": extremely since EWC appeared in orbit when the equipment TRP is kept at ambient temperature by the satellite Thermal Control System (TCS).

Beyond the EWCs, other radiative induced phenomena (SEU and SEFI) affecting the SDRAM are analysed.

The characterization of all the phenomena affecting this type of memories is achieved

by processing the information contained in several telemetry packets through processing programs written in Python. These programs allowed to get the logical addresses of the corrections performed by onboard implemented Error Correction Code (ECC), organising them into defined structures suitable for automatic analysis. This allowed to locate exactly the appearance sites of the EWCs inside the memory module Printed Circuit Boards (PCBs) and to distinguish them from other phenomena, like SEU and SEFI, affected by instantaneous and transitory radiative particle impacts and statistically expected not to appear again in the same location.

In addition, the timestamps associated with each telemetry packet are then used to study the occurrences of these phenomena as a function of time. The study focuses on the temporal evolution of the EWC phenomenon, taking into consideration their increasing total number and the cells activation/deactivation over time. An in-depth analysis is also conducted to investigate the correlation between the evolution of EWCs with the TRP temperature of the equipment, as well as the relationship of radiative istantaneous effects with solar activity.

The same analysis was repeated on the second satellite which was launched two years after the first one. The thermal operating configuration of this second equipment was slightly different from the previous one due to an early reconfiguration programmed after its launch. This information is necessary to correctly interpret the slight differences on EWC figures from the analysis on this second equipment. Also, the space environment and solar activity conditions during the launch of this second satellite were different from those of the first one. Satellite A was launched at the maximum level of the Sun's eleven-years cycle while the second one followed later on at a lower environmental radiation level in the Earth's ionosphere. As a result, potential similarities and differences between the two units were highlighted and compared. By doing so, a comprehensive understanding of the long-term behavior of SDRAM memory modules in space is obtained.

At the end, the activation pattern of EWCs on the MM1 board (one of the most affected boards by this leakage phenomenon on the Satellite A digital equipment) was modelled using ARMA models on different time scales, so that the number of active EWC per day, or the average number per week and month was characterized and the get model can be used to estimate future evolution.

The fundamental steps pursued in this thesis begin in Chapter 1 with a general introduction to the main components of the SSMM equipment under analysis: the emphasis is

on the memory module boards structure and on the arrangement of the SDRAM devices on both sides of each board. An overview of the error correction techniques, i.e. of the Error Correction Code (ECC) is introduced, explaining how the errors are managed and corrected. Understanding these mechanisms is crucial to properly interpret the information contained in the analysed telemetry data that will be used in subsequent chapters. In addition, a summary of the main conclusions contained in the two Technical Notes by TAS-I is reported at the end of this chapter.

Chapter 2 provides a detailed description of the telemetry data used and the processing programs developed for this study. These programs are designed to create an organized database for the error classifications, taking into account all the limitations of the telemetry packets in terms of availability time and content. Additionally, this chapter discusses the main challenges encountered during the data analysis process, including some unexpected and limited anomalies discovered in the telemetry data and their handling.

The classification of the various phenomena observed over the years in the first SSMM equipment onboard Satellite A is reported at the beginning of Chapter 3. All these phenomena, with particular attention to EWCs, are analyzed identifying their exact location within each individual IC/Cube - TSOP Level - column (the physical structure of each memory module board) thanks to the extraction algorithms introduced in the previous chapter.

In Chapter 4, the same analysis is performed on the second digital equipment onboard the twin satellite, The purpose of this analysis is to validate and confirm the results obtained in the previous chapter, as well as to assess the generalizability of the findings to other satellites with SDRAM memory areas.

In Chapter 5, an in-depth study is conducted on the time series related to the EWCs activation on MM1 board. To facilitate a better understanding of the study, a brief introduction on time series analysis is provided. The Box & Jenkins method is employed to obtain the best ARMA model that can be used to predict the future behavior of the EWCs activation. The results obtained from this analysis are then presented and discussed in detail.

At the end, in Chapter 6, the key findings and conclusions are presented and summarized. The implications of the results are discussed and recommendations for potential future improvements in the observation and handling of these phenomena are proposed. Addi-

tionally, the perimeter and limitations characterising the present thesis are acknowledged and suggestions for future research directions on radiative effects on SDRAM memory devices in space are provided.

1 | Background & Technical Reference Documents

1.1. PDHT & SSMM Main Functions

The Payload Data Handling & Transmission (PDHT) is a typical satellite's subsystem dedicated to all the necessary functions for real-time acquisition, storage, handling and transmission to the ground station of PayLoad data (generated by the scientific instruments), SpaceCraft Telemetry Data (SC TM Data) and GPS raw data. It is composed by three major subsystems:

1. Solid State Mass Memory (SSMM), whose main functions are:
    - Data acquisition and storage by use of Synchronous Dynamic RAM (SDRAM) devices.
    - Data formatting according to CCSDS Standards (i.e. a Space Packet Protocol, standard used for formatting files, including TM).
    - Control (HW and SW) of data handling and storage functions.
    - Control (HW and SW) of the overall PDHT functions.
2. Radio Frequency Transmission Assembly (RFTA)
3. Radio Frequency Antenna Assembly (RFAA)

The SSMM is responsible for data management according to predefined communication and storage standards and of formatting the acquired data for downlink transmission during satellite visibility windows with the Ground stations. A representation of the SSMM physical structure with all its internal redundant functions housed in separated Printed Circuit Boards (PCBs) is reported in Figure 1.1.

All functions and the status of the satellite, including all measurements suitable for its monitoring, are provided through TeleMetry (TM) data. TMs data are collected also internally to the SSMM and are transmitted to Ground segment in order to determine

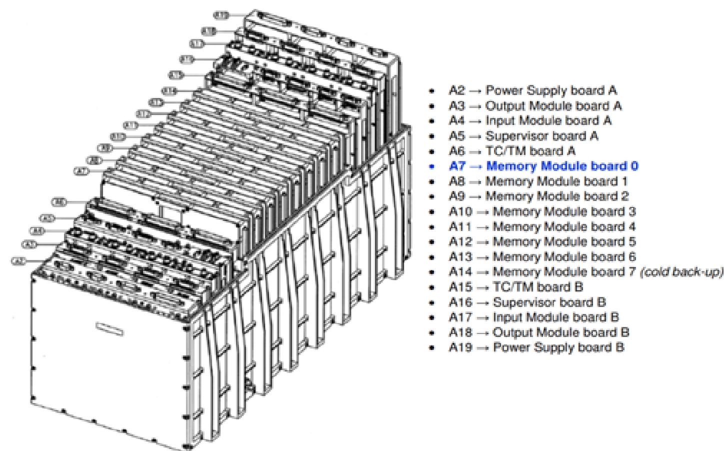

Figure 1.1: SSMM layout with component PCBs view

the health status of all PDHT units and devices and the precise current status of all parameters essential for good flight operations. Different types of reporting periods and telemetry structures with corresponding classes of parameters exist: in this thesis only Housekeeping, Memory Dump and Event Reporting telemetry were analysed, since they contain information about the equipment SDRAM area correction phenomenon under analysis, in particular:

- TM(6,6) - Memory Dump using Absolute Address Report: a daily provided packet series reporting information about corrections executed in each SDRAM Memory Module PCB by local ECC: it provides a "snapshot" of the last 128 successful corrections performed on each MM board;
- TM(3,25) - Housekeeping and Diagnostic Parameter Report: a 1 second periodic packet containing the counter of performed corrections in each single Memory Module PCB, counter sampled at packet production time;
- TM(5,1) - Event Reporting "DEGRADED_DOWNLINK": a specific aperiodic type of Information Event packet generated only after the occurrence of an uncorrectable error in SDRAM area of a MM PCB, an error that is recovered by a power cycle of the affected SDRAM device, and indicating the MM PCB where the error occurred.
- TM(5,3) - Event Reporting "MEM_PARTITION": another specific aperiodic type of Anomaly Event informing that a whole memory partition (1 GiB) of the SDRAM area of a MM PCB was excluded from the future storage of scientific data, due to the persistence of uncorrectable errors in a certain location even after the performed power cycle of the device.

Note: None of these errors ever led to a permanent memory space loss and the parked

partitions were always recovered through a subsequent total power cycle of the whole SSMM equipment.

1.2. Memory Stack Structure

The SSMM equipment under analysis is characterized by a large SDRAM array composed by 7 operating modules (MM0..MM6) of 24 GiB each one, for a total active memory space of 168 GiB, plus one permanently switched off (cold redundancy, in case of permanent failure of one MM PCB, never occurred in the analysed data). Each MM PCB is composed by three main blocks:

- power distribution and on/off circuitry
- one Memory Controller FPGA (MC FPGA) implementing local logic ruling the PCB functionalities
- the SDRAM memory array made of a set of Integrated Circuits (ICs), each one stacked in form of a "cube", globally organised in a matrix structure (rows$*$columns).

Each cube consists of $8 * 64$ MiB Thin Small Outline Package (TSOP) devices (512 MiB in total for each cube) based on SDRAM memory technology.
The array is populated with 60 active memory ICs/cubes located on both sides of the PCB (called "Components side" and "Solders side", respectively): 48 of them are used for user scientific data storage ($48 * 512$ MiB $=$ 24576 MiB $=$ 24 GiB of useful memory space), the remaining 12 cubes are used for carrying the check-symbols (C-S) whose scope is implementing an Error Correction Code (ECC) on the data maintained onboard. The physical distribution of these cubes is the same over all memory module PCBs: their arrangement is shown in Figure 3.5 in Chapter 3.
On both sides of each memory module board, the cubes are protected by two metal armatures (covers) that rest on the cubes providing a thermal conductive contact for heat dissipation purpose.
A simplified structure of an IC/cube and its inner TSOPs layers is shown in Figure 1.2 (from TSOP0, near to the PCB, to TSOP7, conductively connected to the MM board external cover).

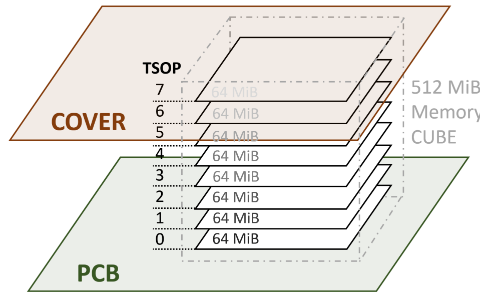

Figure 1.2: TSOP levels inside a cube

Looking at the “vertical” organization of each 24 GiB MM board local matrix, it can be seen as physically organised into 10 independent active columns: only 8 of them represent the usable capacity and carry the user data symbols (8 bits per symbol), while the remaining 2 ones are dedicated to carry the check symbols (8 bits per symbol, dually). Each 16-bits wide column is split furtherly into two physically independent parts, identified as "ODD" or "EVEN" IC as reported in Figure 1.3.
This forms a total code-word of 160 bits = 128 DATA bits + 32 CHECK-SYMBOL bits

DATA																CHECK SYMBOLS			
128 bit																32 bit			
COL 0		COL 1		COL 2		COL 3		COL 4		COL 5		COL 6		COL 7		COL 8		COL 9	
ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN
8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit	8 bit

Figure 1.3: Single MM PCB columns organization

The "ODD" and "EVEN" ICs inside a single column are powered by a common power line circuitry, so the columns are conceived in such a way that a HW failure cannot propagate from a column to another one.

Looking at the “horizontal” organization of the MM board local matrix, the array is composed by 3 rows, each one made of 20 SDRAM ICs/cubes, for a total of 60 active ICs/cubes. The 24 lines across the cubes placed on the 10 columns are identified as partitions (P00..P23) as shown in Figure 1.4.

	DATA																CHECK SYMBOLS			
	COL 0		COL 1		COL 2		COL 3		COL 4		COL 5		COL 6		COL 7		COL 8		COL 9	
Partitions:	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN
0	IC108 / 0	IC100 / 0	IC144 / 0	IC106 / 0	IC80 / 0	IC59 / 0	IC84 / 0	IC64 / 0	IC102 / 0	IC94 / 0	IC145 / 0	IC112 / 0	IC76 / 0	IC136 / 0	IC88 / 0	IC85 / 0	IC98 / 0	IC95 / 0	IC92 / 0	IC89 / 0
1	IC108 / 1	IC100 / 1	IC144 / 1	IC106 / 1	IC80 / 1	IC59 / 1	IC84 / 1	IC64 / 1	IC102 / 1	IC94 / 1	IC145 / 1	IC112 / 1	IC76 / 1	IC136 / 1	IC88 / 1	IC85 / 1	IC98 / 1	IC95 / 1	IC92 / 1	IC89 / 1
2	IC108 / 2	IC100 / 2	IC144 / 2	IC106 / 2	IC80 / 2	IC59 / 2	IC84 / 2	IC64 / 2	IC102 / 2	IC94 / 2	IC145 / 2	IC112 / 2	IC76 / 2	IC136 / 2	IC88 / 2	IC85 / 2	IC98 / 2	IC95 / 2	IC92 / 2	IC89 / 2
3	IC108 / 3	IC100 / 3	IC144 / 3	IC106 / 3	IC80 / 3	IC59 / 3	IC84 / 3	IC64 / 3	IC102 / 3	IC94 / 3	IC145 / 3	IC112 / 3	IC76 / 3	IC136 / 3	IC88 / 3	IC85 / 3	IC98 / 3	IC95 / 3	IC92 / 3	IC89 / 3
4	IC108 / 4	IC100 / 4	IC144 / 4	IC106 / 4	IC80 / 4	IC59 / 4	IC84 / 4	IC64 / 4	IC102 / 4	IC94 / 4	IC145 / 4	IC112 / 4	IC76 / 4	IC136 / 4	IC88 / 4	IC85 / 4	IC98 / 4	IC95 / 4	IC92 / 4	IC89 / 4
5	IC108 / 5	IC100 / 5	IC144 / 5	IC106 / 5	IC80 / 5	IC59 / 5	IC84 / 5	IC64 / 5	IC102 / 5	IC94 / 5	IC145 / 5	IC112 / 5	IC76 / 5	IC136 / 5	IC88 / 5	IC85 / 5	IC98 / 5	IC95 / 5	IC92 / 5	IC89 / 5
6	IC108 / 6	IC100 / 6	IC144 / 6	IC106 / 6	IC80 / 6	IC59 / 6	IC84 / 6	IC64 / 6	IC102 / 6	IC94 / 6	IC145 / 6	IC112 / 6	IC76 / 6	IC136 / 6	IC88 / 6	IC85 / 6	IC98 / 6	IC95 / 6	IC92 / 6	IC89 / 6
7	IC108 / 7	IC100 / 7	IC144 / 7	IC106 / 7	IC80 / 7	IC59 / 7	IC84 / 7	IC64 / 7	IC102 / 7	IC94 / 7	IC145 / 7	IC112 / 7	IC76 / 7	IC136 / 7	IC88 / 7	IC85 / 7	IC98 / 7	IC95 / 7	IC92 / 7	IC89 / 7
8	IC143 / 0	IC130 / 0	IC67 / 0	IC132 / 0	IC118 / 0	IC77 / 0	IC120 / 0	IC81 / 0	IC142 / 0	IC128 / 0	IC62 / 0	IC134 / 0	IC116 / 0	IC60 / 0	IC122 / 0	IC86 / 0	IC126 / 0	IC96 / 0	IC124 / 0	IC90 / 0
9	IC143 / 1	IC130 / 1	IC67 / 1	IC132 / 1	IC118 / 1	IC77 / 1	IC120 / 1	IC81 / 1	IC142 / 1	IC128 / 1	IC62 / 1	IC134 / 1	IC116 / 1	IC60 / 1	IC122 / 1	IC86 / 1	IC126 / 1	IC96 / 1	IC124 / 1	IC90 / 1
10	IC143 / 2	IC130 / 2	IC67 / 2	IC132 / 2	IC118 / 2	IC77 / 2	IC120 / 2	IC81 / 2	IC142 / 2	IC128 / 2	IC62 / 2	IC134 / 2	IC116 / 2	IC60 / 2	IC122 / 2	IC86 / 2	IC126 / 2	IC96 / 2	IC124 / 2	IC90 / 2
11	IC143 / 3	IC130 / 3	IC67 / 3	IC132 / 3	IC118 / 3	IC77 / 3	IC120 / 3	IC81 / 3	IC142 / 3	IC128 / 3	IC62 / 3	IC134 / 3	IC116 / 3	IC60 / 3	IC122 / 3	IC86 / 3	IC126 / 3	IC96 / 3	IC124 / 3	IC90 / 3
12	IC143 / 4	IC130 / 4	IC67 / 4	IC132 / 4	IC118 / 4	IC77 / 4	IC120 / 4	IC81 / 4	IC142 / 4	IC128 / 4	IC62 / 4	IC134 / 4	IC116 / 4	IC60 / 4	IC122 / 4	IC86 / 4	IC126 / 4	IC96 / 4	IC124 / 4	IC90 / 4
13	IC143 / 5	IC130 / 5	IC67 / 5	IC132 / 5	IC118 / 5	IC77 / 5	IC120 / 5	IC81 / 5	IC142 / 5	IC128 / 5	IC62 / 5	IC134 / 5	IC116 / 5	IC60 / 5	IC122 / 5	IC86 / 5	IC126 / 5	IC96 / 5	IC124 / 5	IC90 / 5
14	IC143 / 6	IC130 / 6	IC67 / 6	IC132 / 6	IC118 / 6	IC77 / 6	IC120 / 6	IC81 / 6	IC142 / 6	IC128 / 6	IC62 / 6	IC134 / 6	IC116 / 6	IC60 / 6	IC122 / 6	IC86 / 6	IC126 / 6	IC96 / 6	IC124 / 6	IC90 / 6
15	IC143 / 7	IC130 / 7	IC67 / 7	IC132 / 7	IC118 / 7	IC77 / 7	IC120 / 7	IC81 / 7	IC142 / 7	IC128 / 7	IC62 / 7	IC134 / 7	IC116 / 7	IC60 / 7	IC122 / 7	IC86 / 7	IC126 / 7	IC96 / 7	IC124 / 7	IC90 / 7
16	IC68 / 0	IC129 / 0	IC103 / 0	IC131 / 0	IC117 / 0	IC78 / 0	IC119 / 0	IC82 / 0	IC65 / 0	IC127 / 0	IC109 / 0	IC133 / 0	IC115 / 0	IC73 / 0	IC121 / 0	IC139 / 0	IC125 / 0	IC141 / 0	IC123 / 0	IC140 / 0
17	IC68 / 1	IC129 / 1	IC103 / 1	IC131 / 1	IC117 / 1	IC78 / 1	IC119 / 1	IC82 / 1	IC65 / 1	IC127 / 1	IC109 / 1	IC133 / 1	IC115 / 1	IC73 / 1	IC121 / 1	IC139 / 1	IC125 / 1	IC141 / 1	IC123 / 1	IC140 / 1
18	IC68 / 2	IC129 / 2	IC103 / 2	IC131 / 2	IC117 / 2	IC78 / 2	IC119 / 2	IC82 / 2	IC65 / 2	IC127 / 2	IC109 / 2	IC133 / 2	IC115 / 2	IC73 / 2	IC121 / 2	IC139 / 2	IC125 / 2	IC141 / 2	IC123 / 2	IC140 / 2
19	IC68 / 3	IC129 / 3	IC103 / 3	IC131 / 3	IC117 / 3	IC78 / 3	IC119 / 3	IC82 / 3	IC65 / 3	IC127 / 3	IC109 / 3	IC133 / 3	IC115 / 3	IC73 / 3	IC121 / 3	IC139 / 3	IC125 / 3	IC141 / 3	IC123 / 3	IC140 / 3
20	IC68 / 4	IC129 / 4	IC103 / 4	IC131 / 4	IC117 / 4	IC78 / 4	IC119 / 4	IC82 / 4	IC65 / 4	IC127 / 4	IC109 / 4	IC133 / 4	IC115 / 4	IC73 / 4	IC121 / 4	IC139 / 4	IC125 / 4	IC141 / 4	IC123 / 4	IC140 / 4
21	IC68 / 5	IC129 / 5	IC103 / 5	IC131 / 5	IC117 / 5	IC78 / 5	IC119 / 5	IC82 / 5	IC65 / 5	IC127 / 5	IC109 / 5	IC133 / 5	IC115 / 5	IC73 / 5	IC121 / 5	IC139 / 5	IC125 / 5	IC141 / 5	IC123 / 5	IC140 / 5
22	IC68 / 6	IC129 / 6	IC103 / 6	IC131 / 6	IC117 / 6	IC78 / 6	IC119 / 6	IC82 / 6	IC65 / 6	IC127 / 6	IC109 / 6	IC133 / 6	IC115 / 6	IC73 / 6	IC121 / 6	IC139 / 6	IC125 / 6	IC141 / 6	IC123 / 6	IC140 / 6
23	IC68 / 7	IC129 / 7	IC103 / 7	IC131 / 7	IC117 / 7	IC78 / 7	IC119 / 7	IC82 / 7	IC65 / 7	IC127 / 7	IC109 / 7	IC133 / 7	IC115 / 7	IC73 / 7	IC121 / 7	IC139 / 7	IC125 / 7	IC141 / 7	IC123 / 7	IC140 / 7

Figure 1.4: ICs/cubes organization

Therefore, each byte/symbol is handled/maintained by a physically separated memory cube, into one of its TSOP levels.

The "segregation" of one byte of each code-word in a single TSOP of a cube physically separated from the others (combined with the specified EDAC capabilities described in Chapter 1.2.3) makes the SSMM architecture robust by design to the expected radiation effects and also to the unexpected ones, as analysed in this thesis.

1.2.1. SDRAM technology

The SDRAM (in particular Single Data Rate SDRAM) [1] is simply a DRAM memory where the operation of the external pin interface is coordinated by an externally supplied clock signal.
A SDRAM "cell" is composed by a transistor and a capacitor. The capacitor stores an electronic charge, and a transistor allows to charge or discharge the capacitor. If the capacitor is charged, the cell contains a value of 1. Conversely, if the capacitor is not charged, the cell contains a value of 0.

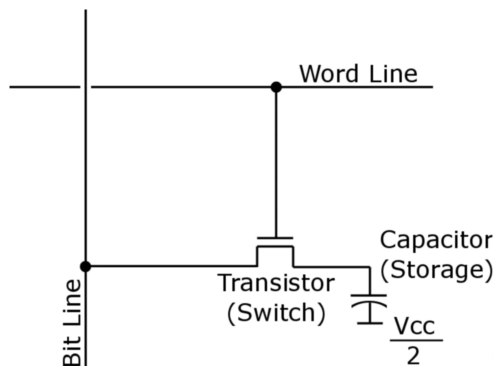

Figure 1.5: DRAM cell structure.

DRAMs have two main problems:

1. the DRAM capacitor charge leaks over time, which is the reason why it is called dynamic RAM. For this reason it needs to be refreshed periodically in order to preserve its bit value. In a SDRAM, this refresh operation is done "synchronously";
2. as all the other types of RAM memories, the SDRAM loses its data when the power is turned off (volatile memory).

1.2.2. Memory Refresh and Scrubbing

The Memory Refresh is a SDRAM background activity in which the electronic charge on the capacitor inside a cell is periodically restored: this process is performed to ensure that each SDRAM IC is fully refreshed every 64 ms or less (as per manufacturer specification for this analysed SSMM equipment; the refresh rate was selected by design to be 48 ms, in order to guarantee sufficient margin w.r.t. procurement specification).

The local SSMM scrubbing function periodically reads all code-words into each MM board ($24 * 1024^3$ B/16 B = 1610612736 logical code-words in 24 GiB of user data) with Error Correction Code (ECC) (also called Error Detection And Correction (EDAC) code) always active on each MM board switched on and with a fixed scan rate. It implements a correction (if needed) within its capability perimeter (1 symbol in a code-word), scanning at progressive “absolute addresses” across the MM board.

Along each TSOP (from 0 to 7) of a cube, any 2048 bytes inner "page" into the "bank" organisation of each TSOP is read by the scrub task, byte per byte, at consecutive 8-bit accesses. The analysed SSMM equipment scrub rate is fixed and set to 1611 s (approximately 27 minutes) for each local 24 GiB MM board SDRAM array. This implies that:

1. Global scrub rate: 24 GiB/1611 s = $(24 * 1024^3/1611)$ B/s = 15996154 B/s.
2. Local TSOP scan rate: (15996154 B/s)/16 = 999760 B/s.

The ECC counts any single error correction that occurred on a read code-word of the MM board local SDRAM array and reports them in a 16-bits-counter register named Soft Error Status Register (SESR): if all single symbols into the consecutive "pages" of a single TSOP are all singly corrected, this could cause up to $15 * 16$-bits-counter wrap arounds into 1 second (i.e. 999760/65536).

1.2.3. Error Detection and Correction Capabilities

It is expected that during the satellite mission, memory components could fail in a way that cannot be recovered: therefore a SSMM equipment is required to automatically detect and deallocate the block of memory affected by the failure. Furthermore, single bit errors that can random accumulate on SDRAM devices due to istantaneous radiation effects are managed by the Error Detection And Correction System (EDAC, synonym of ECC).

If a single symbol/byte is found in error by the ECC at any reading task (that is: its content is changed w.r.t. its original value written at code-word generation and storage in memory), the MC FPGA performs automatically another confirmation read for the error presence always with ECC active, then a re-write operation (by using information stored in the check-symbols and trying to correct the failed symbol by a total re-writing of the code-word) and another confirmative re-read operation on the whole code-word.
Globally, a *R*ead (found error) / *R*ead (error confirmation) / *W*rite (correction) / *R*ead (correction confirmation) cycle is executed, and the whole R/R/W/R process lasts few µs.

If after this attempt the failed address (in particular, one or more bits in one symbol at that address/code-word) in the MM board is found corrected at the latest reading operation with ECC active, it is declared as a "Corrected Error" (CE) or "Soft Error" (SE), the counter in the SESR is increased by 1 and the corresponding address location of the corrected code-word plus the column of the executed symbol correction is saved into a dedicated log area, that is then periodically dumped by Ground via the above-mentioned TM(6,6) packets.

Otherwise, if a single symbol is still found in error by ECC after the R-R-W-R cycle, a "Hard Error" (HE) (or un-correctable error) is declared by MC FPGA and a further

recovery attempt starts, consisting in a power cycle of the affected HE address "belonging column" (note: all "EVEN" and "ODD" ICs in the column are powered off/on, and not only the precise TSOP containing the failed address in HE), then after 20 ms the column is switched on again (with other 10 ms wait) and finally a single reading (always with ECC enabled) is done at the previously declared failed address (1 single code-word direct access). Now:

1. if the HE do not appear any more, only the Informational Event TM(5,1) "DEGRADED_DOWNLINK" (begin) is emitted informing the Ground of the start of a (possible) symbols re-construction period, since at least 6 memory cubes of the column were switched off and their charge may be decayed, maintaining however all 24 partitions of the MM board available for storage. Reconstruction is operated automatically in 27 minutes by the periodic scrubbing task all along the 24 GiB address space of the MM board.

2. if the HE is still present, the whole 1 GiB Partition containing that address (symbol) is "put in parking" (i.e. it is not used for storage tasks anymore), a Medium Severity Anomaly TM(5,3) "MEM_PARTITION" (meaning: failed partition put in parking) and Informational Event TM(5,1) "DEGRADED_DOWNLINK" (begin) are sent, informing the Ground of the start of a (possible) symbols reconstruction period.
   The MM board memory space is decreased by exactly 1 GiB. Scrubbing still continues to pass on the parked partition and any hard error signalling from that parked partition is not taken into account. During the satellite operations a memory parking was always recovered at next MM board complete swith-off / on, lasting from tens of minutes to hours (in particular, the parked partition's devices were always found good at initialization/filling operations performed with ECC enabled at following MM board initialization).

1.3. Previous Analyses made by TAS-I

1.3.1. 2014 Technical Note Analysis - First 25 days in orbit

A first analysis of the complex radiative & leakage phenomenology on the SDRAM area of the SSMM equipment was carried out in 2014 [2], immediately after the launch of Satellite A. The occurrence of numerous CE/SE was observed through the TM(3,25) telemetry which reports the value of the CE counters of all the 7 MM boards. This was never observed on Earth, but it was expected in a space environment due to radiation hitting the

SDRAM cells and producing "bit flips".

Furthermore, a new cumulative correction phenomenon, never observed on Earth and not expected, started to appear after launch in the form of $k * 2048$ (always $\leqslant$ 8 k-corrections, so k $\leqslant$ 4) multiple corrections across few consecutive seconds, over all active MM boards, typically with an observed rate of 2 or 3 times at week per MM board.
The correlation between such phenomenon and expected SEFI events was supposed based on similar rates of the two phenomena. A high correlation of such events with satellite passages across the ionosphere South-Atlantic Anomaly (SAA) was sufficiently established in that Technical Note, during the first 25 days in orbit.
It has to be highlighted that no "functional interrupting" characterised such SEFI like phenomenon: simply re-reading with ECC, the content in the SDRAM device was restored by the scrub process.

Furthermore, a part of CE/SE occurrences in orbit was different from an istantaneous radiative particle impacts: it was discovered to occure many times on the same/repetitive/-contiguous SDRAM addresses, so being more addressable to a cells leakage phenomenon but visible "at ambient temperature" (temperature at which the SSMM equipment TRP is kept in orbit by the satellite TCS). This phenomenon was not observed on Earth during tests done largely "at ambient temperature": this leakage phenomenon is activated only when reaching temperatures higher than room temperature by more than +25 °C (leakage ignition with equipment TRP around +50 °C). But this TRP value above +50 °C was never reached in space throughout the satellite mission, from launch up to now.
Eventually, it was observed that this leakage activated on certain MM area/addresses and deactivated after a certain period, probably due to scientific pattern change in consecutive storage operations of SSMM.
Last but not least, the number of such "Extremely Weak Cells" at ambient temperature was much higher than that of the "Weak Cells" detected during tests at high temperature of SSMM equipment.

A new phenomenology was observed: some SEFI phenomenon left the affected SDRAM area "sensitive to leakage": the addresses, typically corrected by ECC after the first SEFI event, showed a "weakness" in the sense that a certain number of corrections over time were still observed periodically on them after the 1st $k * 2048$-corrections, keeping this continuous correction behavior also for several days after original radiation particle hit. The working hypothesis was that these were high-energy particle impacts within the SEFI family.

After this preliminary analysis, the following classification of CE/SE areas in SDRAM memory space was proposed by TAS-I in that Technical Note:

- "one-shot": addresses corrected one time by scrub (or downlink) and never reappearing over the observation period (possible SEU).
- "sporadic": recurrent address, corrected successfully many times, separated by a few scrub periods (SDRAM leakage).
- "periodic": recurrent address, corrected successfully many times, as minimum over 3 consecutive scrub passages (confirmed and constant SDRAM leakage).
- "Big One-Shot (BOS)": quasi-contiguous addresses whose successful corrections are all located in the same TSOP, appearing as consecutive symbols correction in the order of "thousands" performed in a very short time (typically 2 to 5 consecutive seconds, as visible in TM(3,25)) (never observed during on-Ground testing, possible SEFI).

The "periodic" and "sporadic" addresses were neither SEU nor SEFI: they showed the typical behaviour of "SDRAM charge leakage" phenomenology observed during SSMM eqipment Thermal-Vacuum testing when its TRP was in the range from +50°C to +55°C. Simply, they activate "at ambient temperature" of TRP in orbit flight.

1.3.2. 2018 Technical Note Analysis - After 4 years in orbit

After 4 years in orbit of Satellite A, another TAS-I Technical Note [3] was issued to investigate a frequent and unusual emission of "DEGRADED_DOWNLINK" TM packets from MM0 board observed on Satellite A (meaning more occurrences of HE but recovered by column power cycle and marked by emission of the corresponding TM(5,1)).
Statistics moved from roughly 1 "DEGRADED_DOWNLINK" event each 6 weeks to 1 event each day on that single MM0 board. "DEGRADED_DOWNLINK" TMs are in strict relationship with HE occurrences into one of the code-word of the local MM board memory space, due to one or more "stuck bits" inside a certain 8 bits/symbol.

After the SSMM complete power cycle of all its MM boards, the affected location on MM0 was found newly good by initialization tests, but "DEGRADED_DOWNLINK" events continued to appear from it with a slightly reduced frequency (approximately 1 event each 2/3 days) until 2018/05/08 when the phenomenon degenerated and the first MM0 Partition 08 was "parked" (i.e. after an unsuccessful attempt to recover the HE

with the column power cycle).

On 2018/05/14 a total of 5 partitions (three of them exactly on MM0) were put in parking in the SSMM equipment and the available memory space dropped close to 97%, just above the 95% assumed available by the mission plan. Fortunately, a power off/on cycle of the entire SSMM with all its MM boards always succeeded in making them fully and newly available to user writing processes, including all previously “parked” partitions, demonstrating that it was not a permanent failure.

The following nomenclature for SDRAM cell/capacitors/junction was confirmed in this second TAS-I Technical Note and will also be used within this thesis:

1. Weak Cell: address found in permanent leakage at high temperature during a Thermal-Vacuum Test, starting to appear when SSMM TRP reached and went beyond +50 °C. The leakage effect disappeared when the TRP temperature decreased towards ambient temperature (22 °C).
2. Extremely Weak Cell (EWC): address that is found in permanent leakage also at ambient temperature, per hours or days. TRP in orbit is kept around ambient temperature by the satellite's TCS.

For what concerns the BOS, it was discovered in that second Technical Note that two Events occurred exactly on the same TSOP area into MM0, within few hours. This fact draws another possible direction of investigation: a post-radiation particle hit residual damage acting into a TSOP area, first hit by these particle events at a time and causing a "weakness" of contiguous internal "pages" into a "bank" of the same TSOP, making it more frequently susceptible to the leakage phenomenon, also without any further particle impact exactly on such a SDRAM area (statistically at very low probabiliy).

Nr.	MM0 SDRAM address (increasing value into 24 GiB logic array)	Column	ODD / EVEN	Partition ID	DATA / CS	IC	TSOP	CELL CLASSIFICATION [updated cumulatively]
1	00 2745 5110	01	ODD	00	DATA	IC144	TSOP0	PERIODIC RE-ACTIVATED to SPORADIC in 4th analysed observation window
2	00 28E6 9D40	08	EVEN	00	CHECK-SYMBOL	IC095	TSOP0	PERIODIC
3	00 2C1A C260	04	ODD	00	DATA	IC102	TSOP0	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period) SUSPECTED EWC (same TSOP)
4	00 37F7 46C0	04	ODD	00	DATA	IC102	TSOP0	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period) SUSPECTED EWC (same TSOP)
5	00 5E73 FB50	04	EVEN	00	DATA	IC094	TSOP0	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period)
6	00 74EE 9D30	06	EVEN	01	DATA	IC136	TSOP1	PERIODIC → SPORADIC (captured by DOWNLINK passage during 15th observation period)
7	00 886F 57F0	02	EVEN	02	DATA	IC059	TSOP2	PERIODIC
8	00 8D68 F160	01	EVEN	02	DATA	IC106	TSOP2	PERIODIC → SPORADIC
9	00 97D8 69E0	07	EVEN	02	DATA	IC085	TSOP2	PERIODIC → SPORADIC
10	00 BF9D 2510	09	ODD	02	CHECK-SYMBOL	IC092	TSOP2	PERIODIC
11	00 C24F 5440	01	ODD	03	DATA	IC144	TSOP3	PERIODIC
12	00 D580 1920	06	ODD	03	DATA	IC076	TSOP3	SPORADIC → PERIODIC in first 3 analysed observation windows RE-ACTIVATED to SPORADIC in 4th analysed observation window
13	00 E927 7FD0	05	EVEN	03	DATA	IC112	TSOP3	PERIODIC
14	00 FA89 3720	02	EVEN	03	DATA	IC059	TSOP3	SPORADIC → PERIODIC → SPORADIC (RE-APPEARING ON SEVERAL DAYS)
15	01 0A10 5CF0	00	ODD	04	DATA	IC108	TSOP4	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period)
16	01 58A8 7370	04	EVEN	05	DATA	IC094	TSOP5	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period)
17	01 7AA4 3AE0	04	ODD	05	DATA	IC102	TSOP5	LONG TERM SPORADIC → tends to PERIODIC when activated (it seemed a SEU effect during 1st observation period, but it is discovered to be SPORADIC during 4th observation period)
18	01 A63B B960	06	EVEN	06	DATA	IC136	TSOP6	PERIODIC
19	01 F92D 3360	08	EVEN	07	CHECK-SYMBOL	IC095	TSOP7	SPORADIC → PERIODIC → SPORADIC
20	02 0A9E C110	04	EVEN	08	DATA	IC128	TSOP0	PERIODIC
21	02 1416 0C60	02	EVEN	08	DATA	IC077	TSOP0	PERIODIC
22	02 28D5 2F40	06	EVEN	08	DATA	IC060	TSOP0	PERIODIC (captured by DOWNLINK passage during 1st observation period)
23	02 42F3 F340	09	ODD	09	CHECK-SYMBOL	IC124	TSOP1	LONG TERM SPORADIC → tends to PERIODIC when activated (it seemed a SEU effect during 1st observation period, but it is discovered to be SPORADIC during 2nd observation period)
24	02 438D 95A0	09	EVEN	09	CHECK-SYMBOL	IC090	TSOP1	PERIODIC
25	02 43EE 9FE0	01	ODD	09	DATA	IC067	TSOP1	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period)
26	02 4915 13C0	06	EVEN	09	DATA	IC060	TSOP1	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period)
27	02 8751 A400	04	ODD	10	DATA	IC142	TSOP2	PERIODIC (captured by DOWNLINK passage during 3rd observation period)
28	02 8E16 6E50	03	ODD	10	DATA	IC120	TSOP2	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period)
29	02 A7DE 4B50	02	ODD	10	DATA	IC118	TSOP2	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period)
30	02 C2D9 8FA0	09	ODD	11	CHECK-SYMBOL	IC124	TSOP3	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period)
31	02 CDF6 8690	04	ODD	11	DATA	IC142	TSOP3	PERIODIC
32	02 D8C1 F350	06	ODD	11	DATA	IC116	TSOP3	PERIODIC in first 3 analysed observation windows RE-ACTIVATED to PERIODIC in 4th analysed observation window
33	02 E094 D5E0	02	EVEN	11	DATA	IC077	TSOP3	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period)
34	03 1271 E330	07	EVEN	12	DATA	IC086	TSOP4	SPORADIC → PERIODIC
35	03 1A5A 6C30	02	ODD	12	DATA	IC118	TSOP4	PERIODIC
36	03 2A9F 8F20	09	EVEN	12	CHECK-SYMBOL	IC090	TSOP4	PERIODIC
37	03 319C 5840	03	ODD	12	DATA	IC120	TSOP4	PERIODIC
38	03 538F 8300	03	ODD	13	DATA	IC120	TSOP5	PERIODIC
39	03 5ECB 8AD0	04	ODD	13	DATA	IC142	TSOP5	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period)
40	03 B8FD C600	04	ODD	14	DATA	IC142	TSOP6	PERIODIC
41	03 F69E E360	04	ODD	15	DATA	IC142	TSOP7	PERIODIC
42	03 FF51 0660	04	EVEN	15	DATA	IC128	TSOP7	ONE-SHOT (Possible a SEU candidate, TBC from longer observation period)
43	04 34C9 1DA0	05	EVEN	16	DATA	IC133	TSOP0	QUASI-PERIODIC
44	04 3CEE 0100	07	EVEN	16	DATA	IC139	TSOP0	PERIODIC
45	04 430E AE70	01	ODD	17	DATA	IC103	TSOP1	PERIODIC in first 3 analysed observation windows RE-ACTIVATED to PERIODIC in 4th analysed observation window
46	04 47A3 0870	09	ODD	17	CHECK-SYMBOL	IC123	TSOP1	SPORADIC → PERIODIC → SPORADIC
47	04 72BC F6F0	06	ODD	17	DATA	IC115	TSOP1	QUASI-PERIODIC
48	04 89C2 7650	08	EVEN	18	CHECK-SYMBOL	IC141	TSOP2	LONG TERM SPORADIC → tends to PERIODIC when activated (it seemed a SEU effect during first observation periods, but it is discovered to be SPORADIC during 7th observation period)
49	04 9800 0700 04 99EC 2700	01	EVEN	18	DATA	IC131	TSOP2	BIG "ONE-SHOT" / SEFI (damaged & recurring area)
50	04 B30A 2C80	03	ODD	18	DATA	IC119	TSOP2	SPORADIC
51	04 C99C A0B0	00	EVEN	19	DATA	IC129	TSOP3	PERIODIC
52	04 D37B 8870	05	ODD	19	DATA	IC109	TSOP3	PERIODIC (captured by DOWNLINK passage during 2nd observation period)
53	04 EFEC 1300	02	EVEN	19	DATA	IC078	TSOP3	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period)
54	05 086F 3310	04	ODD	20	DATA	IC065	TSOP4	PERIODIC (captured by DOWNLINK passage during 2nd observation period)
55	05 340F E190	00	EVEN	20	DATA	IC129	TSOP4	PERIODIC
56	05 3464 DF70	04	EVEN	20	DATA	IC127	TSOP4	SPORADIC
57	05 3C46 EBE0	00	ODD	20	DATA	IC068	TSOP4	PERIODIC
58	05 3F62 1280	02	ODD	20	DATA	IC117	TSOP4	
59	05 41B7 56A0	00	EVEN	21	DATA	IC129	TSOP5	PERIODIC → SPORADIC
60	05 4DF5 9D70	01	EVEN	21	DATA	IC131	TSOP5	PERIODIC
61	05 6E5E 55E0	05	ODD	21	DATA	IC109	TSOP5	ONE-SHOT (Continued to be a SEU candidate, TBC from longer observation period)
62	05 7EFE 5BA0	07	ODD	21	DATA	IC121	TSOP5	PERIODIC → SPORADIC
63	05 E813 B9D0	01	EVEN	23	DATA	IC131	TSOP7	PERIODIC

Figure 1.6: 2018 EWCs census done on MM0: 47 (certified Extremely Weak Cells) + 2 suspected ones (same TSOP) + 13 possible SEU locations (TBC on longer periods) + 1 BOS repetitive location

2 | Telemetry Elaboration

Telemetry is the set of all measurements collected by the satellite's instruments suitable for its monitoring. They are defined by the manufacturer and their transmission to the Ground is in form of structured packets and uniquely defined parameters, based on well-defined standards. In this chapter the information contained in these telemetries used for the present thesis will be introduced and an overview on how they were processed is shown.

2.1. TM(6,6) - Memory Dump using Absolute Address Report

TM(6,6) packets are requested and sent from SSMM 2 to 6 times a day, generally in the morning and evening. Each TM(6,6) telemetry packet consists of a series of 36 consecutive packets (distinguished by the Report Integrity Counter (RIC) parameter spanning from 1 to 36), the total payload of such consecutive packets contains the "snapshot" of the last 128 successfully corrected addresses by EDAC (i.e. "Soft Errors"/"Corrected Errors") with the relative CE counter performed on each SDRAM MM board (from MM0 to MM6 plus the redundant one that is always switched off, so with zeroed content) before sending the first packet of the series.

When a single symbol/byte is detected in error by the EDAC, and results truly corrected after the R/R/W/R cycle introduced in Chapter 1.2.3, it is declared as a CE/SE and the counter in the SESR is increased by one and the corresponding address location plus the column of the executed symbol correction is saved into the log area made of a vector of 128 "entries" per MM boards periodically dumped via TM(6,6) packets.

During the sequential construction onboard of this corrections state vector, old corrections are overwritten by newer ones, and this cause a sort of wraps arounds of the 128 entries. This overlapping, visible as a discontinuity in monotone CE counter across the entries plus the proper wrapping of the 16-bits CE counter in each MM board were taken

into account in the vector sorting algorithm used in this thesis.
The ordering of the addresses occurrences across each individual TM packets is critical because it allows to obtain the variation in CE counter between one memory address and the next one, making it possible to distinguish the effects of the various phenomena occurred on the each MM board and contributing to the analysis of the global correction figure.

An example of a TM(6,6) packet in hexadecimal raw format is reported in Figure 2.1, where some parts have been highlighted and colored to make the following explanations clearer.

```
Frame: [0431-DFDF-1807] VCid#0 Time=2014/07/25 06:56:30.629 <-{01F73C0C} offset#211
Packet:[0E19-C534-00F9] APid#61.9(DSHA.DUMP) PSC#0534 PL#0F9 Serv(6,6) OBRT#0040FCC22D00 <46600> "TM(6,6) Memory Dump using Absolute Addresses
Report"
0E19-C534-00F9 1006-0610-0040-FCC2-2D00 0001 0001 0240 0000 0039 69E1 1F00 4767
59A0 69E2 1F00 4767 59A0 69E3 1F00 4767 59A0 69E4 1F00 4767 59A0 69E5 6F03 DD90
7180 69E7 5F03 F32A 4E30 69E8 F105 4DF5 9D70 69E9 F105 4DF5 9D70 69EA F105 4DF5
9D70 69EB F105 4DF5 9D70 69EC 2F01 623A 9170 69ED F105 4DF5 9D70 69EE 2F01 623A
9170 69EF F105 4DF5 9D70 69F0 2F01 623A 9170 69F1 F105 4DF5 9D70 69F2 2F01 623A
9170 69F3 F105 4DF5 9D70 69F4 2F01 623A 9170 69F5 F105 4DF5 9D70 69F6 2F01 623A
9170 69F7 F105 4DF5 9D70 69F8 2F01 623A 9170 69F9 F105 4DF5 9D70 69FA 2F01 623A
9170 69FB F105 4DF5 9D70 69FC 2F01 623A 9170 69FD F105 4DF5 9D70 69FE 2F01 46EE
            MST06000                (Last Packet) #0="NOT LAST PKT"
            MST06001                        (RIC) #1=1
            MST06002            (Dump_Memory_ID) #1="RAM"
            MST06003           (Dump Start Addr) #2400000=37748736
            MST06004               (Data Length) #39=57
            MST06005            (DUMP_DATA_WORD) #69E11F00=1776361216
```

Figure 2.1: Example: one out of 36 packets from a TM(6,6) series

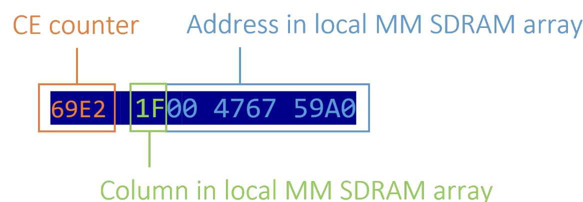

Figure 2.2: Example: CE + address

In Figure 2.2 is shown one of the 128 entries referred to a single MM board, it is formed by 3 fields spanning over 8 bytes: 2 bytes dedicated to the CE counter (orange), 1 byte for the affected "EVEN"/"ODD" column (green) and 5 bytes used for the address of the error that caused the CE counter to increas (lightblue and white hexadecimals).
The column + address information allows to trace exactly the IC/cube, column (EVEN, ODD), partition, and so TSOP level where the error occurred and was corrected by local MM board ECC during a reading task.

2.1.1. TM(6,6) Extraction Algorithm

The TM(6,6) extraction algorithm developed in this thesis can be subdivided into 3 macro stages, the first one (TM66_parser) takes as input the TM(6,6) files in hexadecimal raw format (one file per year), processes them, and returns an ordered list of TM(6,6) packets whose contents is divided by memory modules.
The main functions of this first script are shown in Figure 2.5 (blue box), while the main problems encountered during telemetry processing are:

1. sorting the packet contents taking into account both the wraps arounds of both the 128 entries and the CE counter,
2. identification and management of different (initially unknown) anomalies:
   - missing of one or more packets of the 36 series that compose a TM(6,6) acquisition;
   - presence of an extra entry from a random memory modules within the content of the pakets sent until January 2015.

The resulting list of ordered TM(6,6) packets is supplied to the second stage (BOS_Zones_census), which generates a census of the "zones" affected by BOS per MM board. The contents of each array of the 128 ordered entries inside a TM(6,6) acquisition referred to a specific memory module is analysed to search consecutive addresses, having the following characteristics:

- belong to the same IC/cube;
- belong to the same TSOP;
- have CE counter variation $\geqslant 500$ (this limit was obtained by conducting several elaborations with different values. As shown in Chapter 3.6.3 in Figure 3.57, such threshold for CE counter variation allows a very reliable identification threshold of BOSs that have occurred over all MM boards).

The zones thus obtained are saved in a census with the structure shown in Figure 2.3, where each sequence of address + CE variation (green and yellow respectively) belonging to the same BOS Zone is associated with the IC/cube (orange) and the TSOP level (gray) in which it occurred, plus the packet timestamp (blue) in which it was found.

```
[
    [2014/04/12 15:40, 92, 0, [1739, "9F00 30BB 58B0"], [584, "9F00 31AF 98B0"]]
    [2014/04/16 06:53, 144, 2, [3634, "1F00 B2E6 2B30"], [564, "1F00 B3DA 4B30"]]
    [2014/04/17 06:34, 122, 1, [3583, "7F02 485F EE80"], [2538, "7F02 4954 0E80"]]
    [2014/04/18 07:17, 143, 4, [1747, "0F03 0600 0D70"], [3648, "0F03 0674 CD70"], [2258, "0F03 0769 0D70"]]
    [2014/04/22 07:30, 123, 1, [3661, "9F04 404F 3950"], [2820, "9F04 4143 5950"]]
    [2014/04/23 16:10, 82, 6, [3153, "F305 B213 C400"], [3170, "F305 B307 E000"]]
    [2014/04/30 06:45, 125, 0, [3107, "8F04 1600 01B0"], [3641, "8F04 16CE E1B0"], [910, "8F04 17C3 01B0"]]
    [2014/05/04 16:06, 112, 2, [582, "F500 BA00 0040"], [3676, "F500 BA27 C040"], [3402, "F500 BB1B E040"]]
    [2014/05/04 16:06, 121, 4, [1922, "7F05 26A4 8000"], [3917, "7F05 26E4 8000"], [1892, “7F05 27E4 8000"]]
    [2014/05/13 15:57, 139, 6, [3784, "F705 8BA5 8000"]]
    [2014/05/15 15:37, 142, 1, [753, "4F02 7A00 0E70"], [3661, "4F02 7A33 2E70"], [3238, "4F02 7B27 4E70"]],
    [2014/05/17 07:11, 60, 6, [7652, "F603 BBA6 4830"]]

    .
    .
    .
]
```

Figure 2.3: Example: BOS zones census

At the end, 7 lists of BOS Zones are obtained, one per memory module boards (MM0..MM6). Proceeding in this way, we were able to obtain the exact location in the memory module where the BOS occurred and the approximate time of occurrence (*note:* as for all the corrections, the time is not the exact time of the BOS occurrence, but it is the time of the TM packet containing it). At the same time, the two extreme addresses composing a BOS zone will be used later to determine whether successive (or previous) corrections occurred in the same memory zone.

In the third stage, a census of all the corrections that occurred in all MM boards is created. For each memory module, the program scrolls the respective contents inside all TM(6,6) packets acquisition; each time it encounters a new address never observed previously it adds it into a list of dictionaries saving its characteristics. Based on these characteristics, the address is then classified into 5 main categories: S-S EWC, M-S EWC, SEU, SBC, BOS which will be widely explained at the beginning of Chapter 3.
Eventually, it creates a list of dictionaries in which the useful information about location and type of each address that appeared in a packet is saved. Each dictionary contains the following keys:

- **address**: column + logical address in hexadecimal form;

- **occurrence**: list containing the number of times the address is found within each TM(6,6) packet;
- **delta_CE_count**: lists containing the variation of the CE count associated with the address for each time it was detected within the packets;
- **SS_EWC**: True if the address is classified as Single-Shot EWC;
- **MS_EWC**: True if the address is classified as Multi-Shot EWC;
- **SEU**: True if the address is classified as SEU;
- **SBC**: True if the address is classified as Single Big Correction (SBC);
- **BOS**: True if the address is classified as BOS;
- **in_BOS**: True if the address is within the addresses delimiting one BOS Zone.
- **Partition**: partition where the address is located;
- **Parity**: "ODD" of "EVEN" side of the column.
- **Column**: column (from 1 to 10) where the address is located;
- **IC**: IC/cube where the address is located;
- **TSOP**: TSOP level (from 0 to 7) where the address is located;

The census structure obtained in this thesis work from the TM(6,6) telemetry packets collection just described is reported in Figure 2.4

```
[ # TM66 census
  [ # MM0
    { # Address 1 in MM0
      "address": "3F04 3B86 EAE0",
      "occurrences": [14, 0, . . . , 0, 0, 0],
      "delta_CE_count": [[1,1,1,1,1,1,1,1,1,1,1,1,1,1], [], . . ., []],
      "SS_EWC": True,
      "MS_EWC": False,
      "SEU": False,
      "SBC": False,
      "BOS": False,
      "in_BOS": False,
      "partition": 16,
      "parity": "ODD",
      "column": 3,
      "IC": 119,
      "TSOP": 0,
    },
    { # Address 2 in MM0
      "address": "8F03 663E B210",
      .
      .
      .
    }
  ],
  [ # MM1
      .
      .
      .
  ]
]
```


Figure 2.4: Census structures of all corrections occurred on SSMM MM boards

A graphical representation of the TM(6,6) extraction algorithm pseudocode used for telemetry analysis is shown in Figure 2.5.

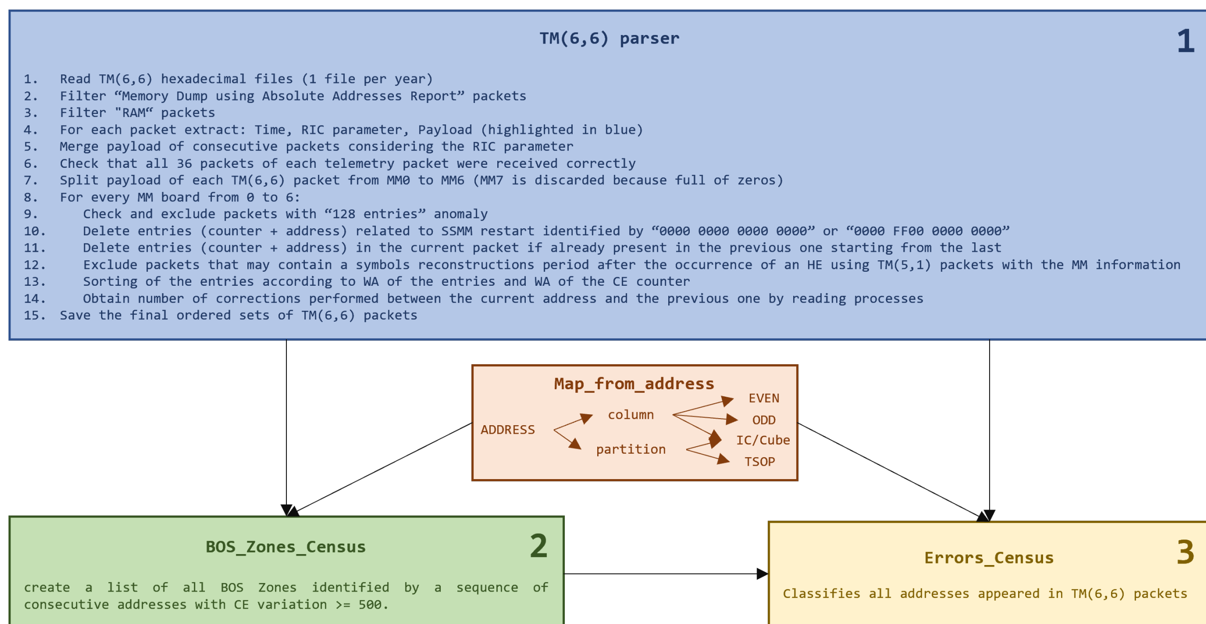

Figure 2.5: TM(6,6) extraction algorithm pseudocode

Both programs internally invoke an external module (map_from_address) that allows to get from the "address" (column + logical address) its location within the memory module

in the form of partition, column (number and if EVEN or ODD), IC/Cube and TSOP level.

These programs allowed to obtain the census of all the corrections occurred and BOS Zones automatically for both Satellite A and Satellite B data by simply changing the directory containing the raw TM(6,6) files.

2.2. TM(3,25) - Housekeeping and Diagnostic Parameter Report

CE/SE are sampled every second from the local MC FPGA on each MM boards by the Application SW of SSMM and inserted in the 1-s periodic TM(3,25) telemetry packets inside the field "MMx_CE" counter (number of corrections occurred "up to that second" on the "X" memory module).

Frame Time	OBRT	Pkt	PktHeade	MST03105	MST03103	MST03102	MST03101	MST03100	MST03099	MST03098	MST03097	MST03096
2018/05/08 08:09:28.402	3,10E+11	42502	[0E14-C04	31830	0	9213	9969	40336	31593	52966	50358	36291
2018/05/08 08:09:29.125	3,10E+11	42502	[0E14-C04	31830	0	9213	9969	40336	31593	52966	50358	36291
2018/05/08 08:09:30.402	3,10E+11	42502	[0E14-C05	31830	0	9213	9969	40336	31593	52966	50358	36292
2018/05/08 08:09:31.250	3,10E+11	42502	[0E14-C05	31830	0	9213	9969	40336	31593	52966	50358	36292
2018/05/08 08:09:32.504	3,10E+11	42502	[0E14-C05	31820	0	9213	9969	40336	31593	52966	50358	36292
2018/05/08 08:09:33.156	3,10E+11	42502	[0E14-C05	31810	0	9213	9969	40336	31593	52966	50358	36292
2018/05/08 08:09:34.504	3,10E+11	42502	[0E14-C05	31810	0	9213	9969	40336	31593	52966	50358	36292
2018/05/08 08:09:35.250	3,10E+11	42502	[0E14-C05	31810	0	9213	9969	40336	31593	52966	50358	36292
2018/05/08 08:09:36.129	3,10E+11	42502	[0E14-C05	31810	0	9213	9969	40336	31593	52966	50358	36292
2018/05/08 08:09:36.750	3,10E+11	42502	[0E14-C05	31800	0	9213	9969	40336	31593	52966	50358	36292
2018/05/08 08:09:38.129	3,10E+11	42502	[0E14-C05	31790	0	9213	9969	40336	31593	52966	50358	36292
2018/05/08 08:09:39.004	3,10E+11	42502	[0E14-C05	31790	0	9213	9969	40336	31593	52966	50358	36292
2018/05/08 08:09:39.750	3,10E+11	42502	[0E14-C05	31790	0	9213	9969	40336	31593	52966	50358	36292

Figure 2.6: TM(3,25) data format, MMx_CE in decimal format over all MM boards

SE are detected by both the scrubbing and downlink process, with the difference that scrubbing process will read with EDAC progressively a constant number of code-words per second, instead downlink may read anywhere in base to the commanded memory segment transferred to Ground. In both cases if a SE raises in the ECC correction capability, it will cause the CE counter to increase (*Note: the TM(3,25) does not provide the addresses where the correction occurred but only the number of corrected errors, second by second*).

The CE counter is a 16-bit counter that spans in the decimal range from 0 (0x0000) to 65535 (0xFFFF). Whenever the higher limit value is exceeded or an HE occurs with consequent recovery action (column power off/on cycle) with a typical correction period of 27 minutes due to decayed symbols reconstruction in the MM board SDRAM array,

may cross the 65535 to 0 limit many times due to re-contruction effect.

The progress of this counter for all years of Satellite A life, for each memory module is reported in Figure 2.7. It is visible the presence of several (expected) wrap arounds of the MMx_CE counters, it is clearly visible also the anomalous period in May-August 2018 where numerous HEs were detected on MM0 and caused MM0_CE counter to continuously reset to 0 (due either to HE handling that resets initially this counter to 0 after column re-switch on or to total SSMM commanded power cycles occurred in that period trying to recover the MM0 anomaly to HE handling). The effect on the other MM1..MM6 CE in the same period is due to the continuous re-init of all MM boards in the SSMM equipment, trying to recover the MM0 fault.

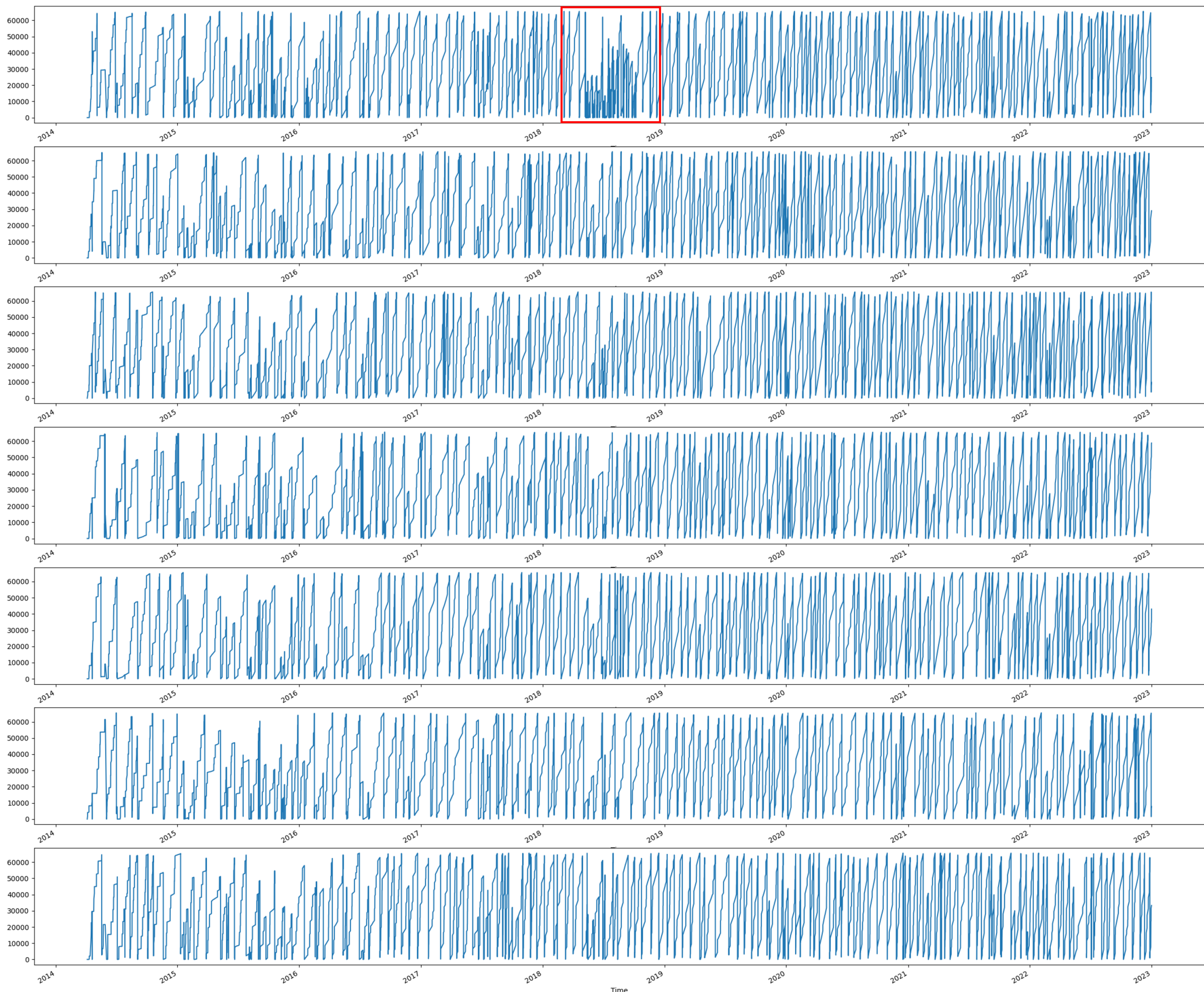

Figure 2.7: MMx_CE count for all MM boards of Satellite A

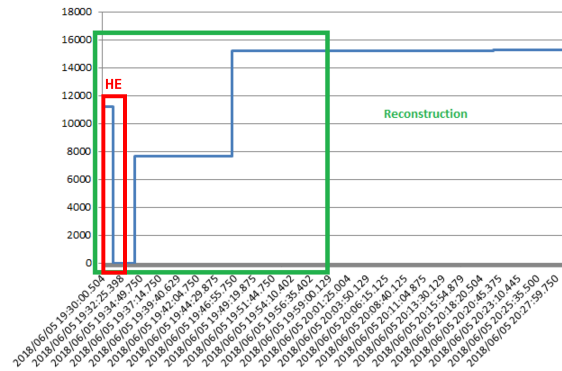

Figure 2.8: MM0_CE count in TM(3,25) in the immediate followings of 1st HE event of the series during 2018 anomaly

2.3. TM(5,1) "DEGRADED_DOWNLINK" & TM(5,3) "MEM_PARTITION"

The TM(5,1) "DEGRADED_DOWNLINK" (begin) packet emission is merely a direct observable signature of an uncorrectable HE phenomenon occurred into a certain single symbol of a code-word in a SDRAM memory cubes array.
The on/off power cycle explained in Chapter 1.2.3, following the detection of a HE by MC FPGA, may cause a symbols re-construction period (driven by scrub task over 27 minutes period) along the off/on column. In order to exclude these corrections (related to the column shutdown for HE handling only) from the analysis, TM(5,1) packets are used in the present thesis to distinguish CE inceasing consequent to a HE handling and reconstruction from CE increasing due to SE phenomenology. All corrections saved in a TM(6,6) packet series, occurred after the issue of a TM(5,1) and containing such HE consequent effects, were discarded without affecting the global statistics of analysis due to the bounded number of HE events in the SSMM on Satellite A along its mission.

From 2014 to the end of 2022, a total number of 153 HEs occurred tagged by the emission of as many TM(5,1) "DEGRADED_DOWNLINK" (begin) packets, distributed among the various MM board PCBs in the following figure:

- **MM0: 76** (58 of which concentrated in 2018, in the three months of the anomaly presented in Chapter 1.3.2, 16 in the remaining years, i.e. quite in line with remainging MM boards)
- **MM1: 15**

- **MM2: 14**
- **MM3: 15**
- **MM4: 7**
- **MM5: 15**
- **MM6: 11**

In total, only 276 blocks of 128-entries were discarded out of 50976 total 128-entries blocks over almost 9 years (8496 TM(6,6) packets * 7 MM boards) over all MM boards: they represent only the 0.54% of information and so their discarding do not affect the total CE/SE statistic analysis reported in next sections.

The TM(5,3) "MEM_PARTITION" packet emission provides the number of the MM board affected by a reduction of its usable memory for the storage of scientific data by the exclusion of 1 GiB due to the presence of a persistent HE in a certain location. From 2014 to the end of 2022, a total of 24 partition parking events occurred on all MM boards, distributed among them in the following way:

- **MM0: 10** (all occurred in the three months of the 2018 anomaly described in TN 2018 0f TAS-I)
- **MM1: 6**
- **MM2: 0**
- **MM3: 3**
- **MM4: 1**
- **MM5: 2**
- **MM6: 2**

2.3.1. TM(5,1) & TM(5,3) Extraction Algorithm

The raw TM(5,1) and TM(5,3) packets handling is very similar to that of TM(6,6), the processing program simply filtered the packets related to "DEGRADED_DOWNLINK" and "MEM_PARTITION" from all the other packets of TM(5,1) and TM(5,3) by distinguishing them, as reported Figure 2.9, with letter "D" and "P" respectively (green). Then the information about time (blue) and the memory module on which HE or partition exclusion occurred (orange) are saved in a list of dictionaries.

```
[
    {msg_type: D, Packet: 0E17-E9B4-0011, Time_CUC: 0040-B0D0-AD, Time_HUMAN: 2014/05/28 16:26:07.770, MM: 3},
    {msg_type: D, Packet: 0E17-EA05-0011, Time_CUC: 0040-B0D4-0D, Time_HUMAN: 2014/05/28 16:40:30.504, MM: 3},
    {msg_type: D, Packet: 0E17-DBCB-0011, Time_CUC: 0040-C789-4E, Time_HUMAN: 2014/06/14 22:03:43.500, MM: 1},
    {msg_type: D, Packet: 0E17-DBCC-0011, Time_CUC: 0040-C78C-15, Time_HUMAN: 2014/06/14 22:15:35.770, MM: 1},
    {msg_type: D, Packet: 0E17-E43B-0011, Time_CUC: 0041-5AE8-76, Time_HUMAN: 2014/10/04 16:52:55.504, MM: 6},
    {msg_type: D, Packet: 0E17-E43C-0011, Time_CUC: 0041-5AEC-3F, Time_HUMAN: 2014/10/04 17:09:04.879, MM: 6},
    {msg_type: D, Packet: 0E17-F907-0011, Time_CUC: 0041-D025-F3, Time_HUMAN: 2015/01/01 15:10:28.004, MM: 3},
    .
    .
    .
    {msg_type: P, Packet: 0E17-D5CC-0011, Time_CUC: 0050-9CFD-CC, Time_HUMAN: 2022/11/14 12:57:33.129, MM: 5}
]
```


Figure 2.9: Example: TM(5,1) "DEGRADED_DOWNLINK" & TM(5,3) "PARTITION_PARKING" data extracted from raw telemetry packets

The information contained in these packets is used for HE detection and exclusion of the TM(6,6) packets that might contain the reconstruction period of corrections after a HE recover attempt as described in the previous chapters.

3 | Results on Satellite A SSMM

Once the census of corrections along 9 years of Satellite A is obtained as described in Chapter 2.1, it was possible to study the occurrences of all errors as a function of time and of their location within each individual MM board. All types of errors occurred on SDRAM arrays were classified into the following categories, looking at value and timings of the increment appearing in CE counter of any MM board:

1. Single-Shot Extremely Weak Cell (S-S EWC): single address corrected successfully multiple times but always with a CE counter increment always equal to 1, while the temperature of the TRP is kept around $T_ambient$ by satellite TCS.

2. Multi-Shot Extremely Weak Cell (M-S EWC): address found in error and corrected successfully multiple times with at least one CE counter increment > 1, while the temperature of the TRP is kept around T_ambient by satellite TCS.

3. Single Event Upset (SEU): address found in error only one time over the entire time frame of 9 years and with a CE counter variation equal to 1.

4. Single Big Correction (SBC): address found in error only one time over the entire time frame of 9 years with CE counter variation > 2 and < 500.

5. Big One-Shot (BOS): consecutive corrections with CE counter increment $\geqslant 500$ i.e. symbols correction in order of "thousands" and performed in a short time frame, typically from 1 to 5 s, of quasi-contiguous addresses all located in the same TSOP captured during a reading process.

The results shown in the following chapters refer to Satellite A only. The analysis performed on the TM data from SSMM equipment of Satellite B, which confirms and validates the model & findings on Satellite A are reported in Chapter 4.

The following graphs were obtained using pre-processed TM(6,6) packets elaborating one memory module at a time through a Jupyter Notebook that is a interactive development environment for live code, equations, visualizations, and text.

3.1. Single-Shot Extremely Weak Cell (S-S EWC) Analysis

3.1.1. S-S EWCs activation over time

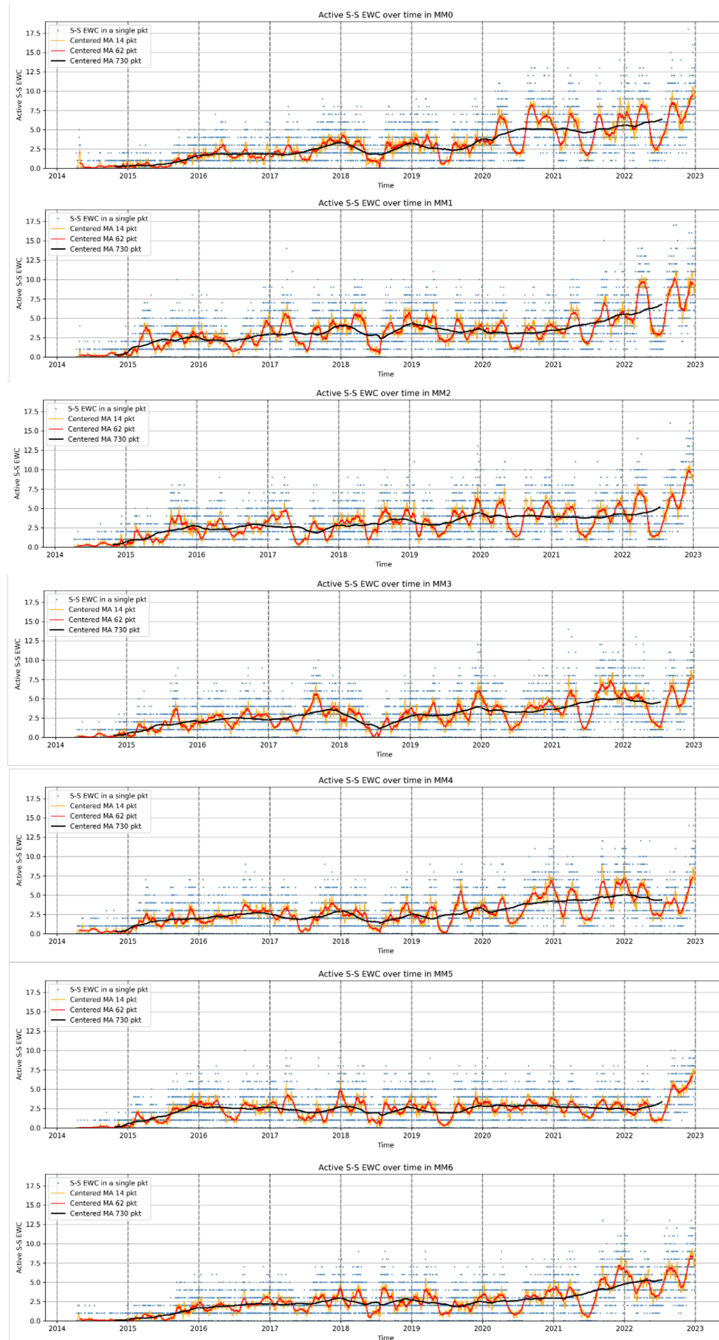

Figure 3.1: Activation of S-S EWC over time in all MM board, from MM0 to MM6

Figure 3.1 represents the number of S-S EWCs that are identified within each individual TM(6,6) acquisition. Specifically, for each active MM boards (from MM0 to MM6), the graphs show:

- **blue**: number of certified active S-S EWC found in leakage contained in one single TM(6,6) acquisition;
- **orange**: centered moving average over one week (14 TM(6,6) aquisitions, typically in the morning and in the evening);
- **red**: centered moving average over one month (62 TM(6,6) acquisitions);
- **black**: centered moving average over one year (730 TM(6,6) acquisitions).

In this section, the behavior of S-S EWC activation is analyzed as function of time over 9 years within all memory modules of Satellite A.

A correlation between the activation waveform of S-S EWC and the SSMM equipment TRP waveform became clearly visible across the years and on all memory modules, starting to become well-shaped from the fourth year in orbit. There are only slight differences across MM boards, it can be noticed how the annual variation of EWCs activation in the last two MM boards (especially in the fifth), is established in a "slower" way, following a more constant trend and maintaining a lower average number of active S-S EWCs respect to other modules.

In Figure 3.2 the SSMM TRP from its launch to the end of 2022 is reported. The typical seasonal decreasing periods of TRP are visible: in particular, that one called "orbital eclipses season" ranging from early May to early August is visible each year. Across the years, annual fluctuations remained constant in amplitude, while the average temperature of TRP is increased with logarithmic trend of roughly +4 °C from launch to the end of 2022 (typcal "TRP drift" due to ageing in satellite TCS efficiency).

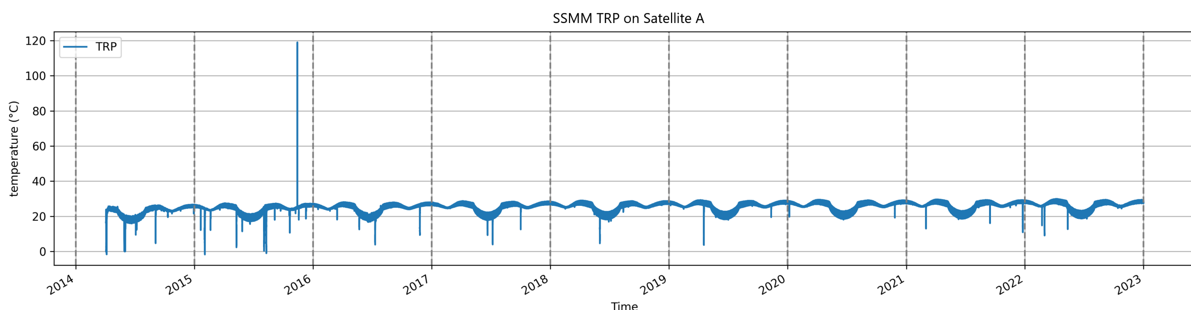

Figure 3.2: Satellite A SSMM TRP

The vertical peaks seen in the Satellite A SSMM TRP plot are artifacts related to signal losses in the satellite-to-ground transmission of that telemetry, which is different from those covered in this thesis and therefore does not affect the analysis.

As we can see from Figure 3.3, during the "orbital eclipses season" the TRP experiences a global decreasing/increasing of about 7/10 °C range. Other small "global oscillations" bounded to about 2/3 °C are visible in other period of the year, as during January/February and September/November months. The same waveform becames progressively visible over the years in all MM PCBs in the perspective of activation in leakage of the S-S EWC.

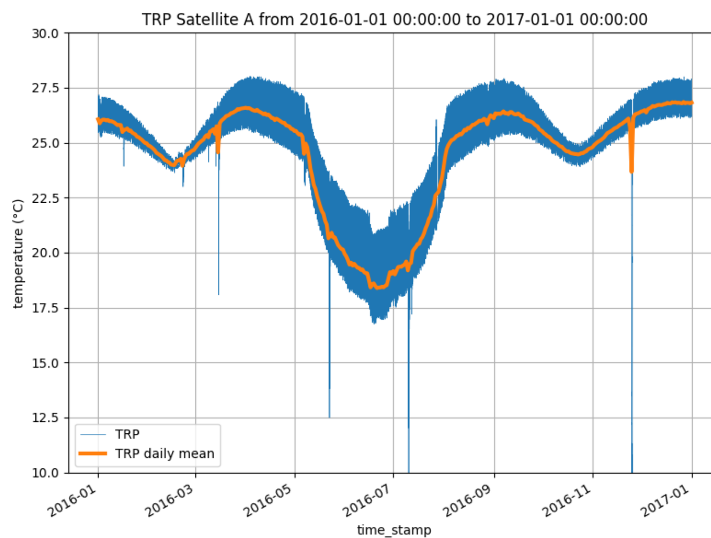

Figure 3.3: Satellite A SSMM TRP on annual scale

Particularly noticeable remains the fact that in all MM boards there is a greater concentration of days without or with "very small number" of "active" EWCs in the middle months of the years when the temperature of TRP reaches its annual local minimum.

3.1.2. Total certified number of S-S EWCs over time

As visible in Figure 3.4, the S-S EWC certified number increases progressively over time in a linear way, whether or not they are active over all MM boards at TM(6,6) sampling time. The certified number of S-S EWC is increased by 3 orders of magnitude on all MM boards over 9 observed years of flight. The precise final values of the total number of S-S EWCs are highlighted on the right side of the graphs. From these values is noticed that the last 2 MM PCBs (MM5 & MM6) have a total absolute number of certified S-S EWC significantly lower than the others after 9 years in orbit.

From the internal temperature profile get in thermal analysis and confirmed during testing on ground of SSMM by TAS-I through the MM boards, MM5 and MM6, that are the external of the MM boards array towards the switched off redundant side of SSMM on a side (recall Figure 1.1), result meanly colder when compared with the other MM boards (approximately -1/-3°C average, and also slightly depending on the MM board side). In these two "cold" MM PCBs, the total number of certified S-S EWC grew slowly and arrived visibly at a lower value.

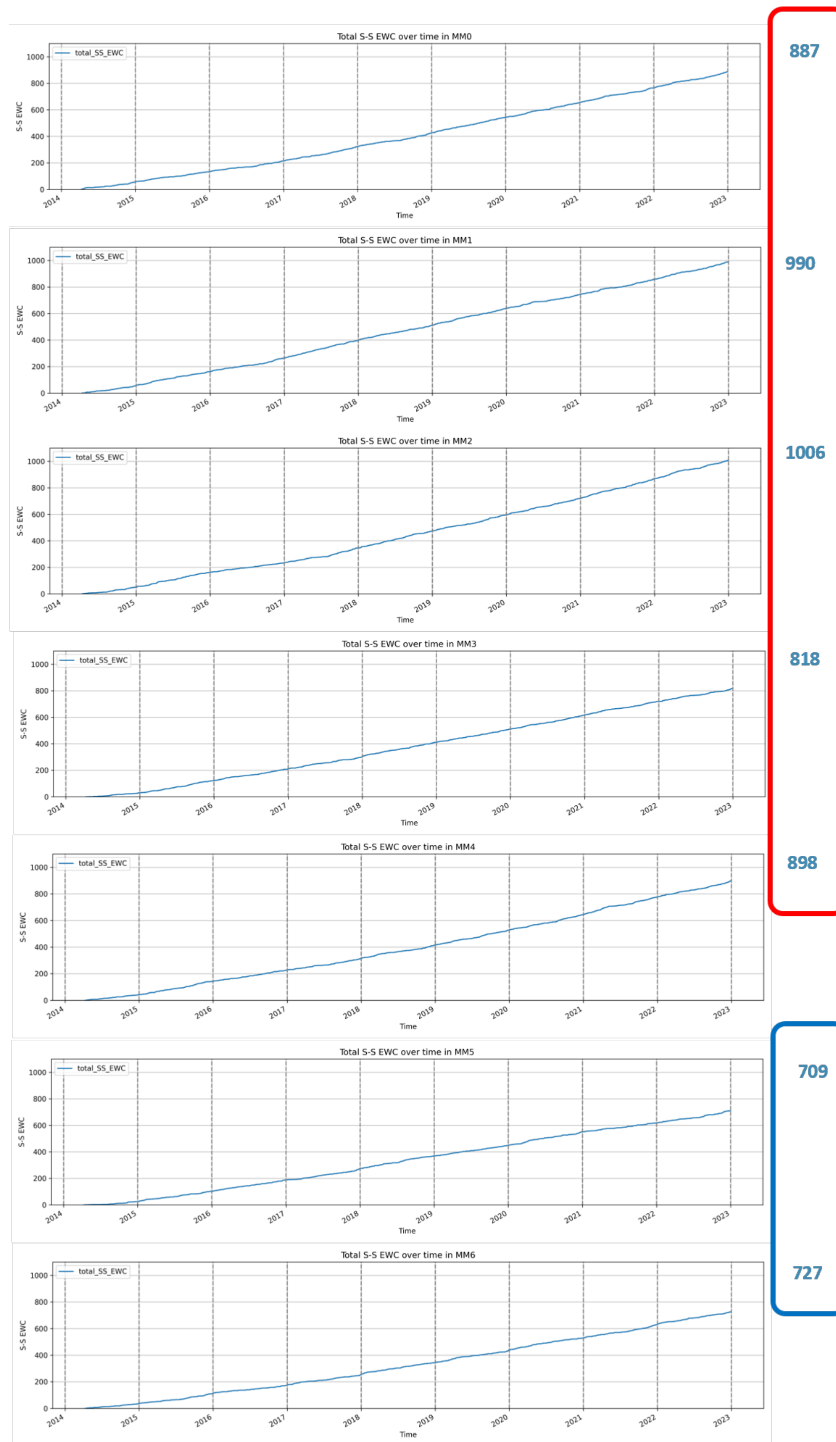

Figure 3.4: Total certified number of S-S EWC over time in all MM boards

Taking into account what discussed above about the activation of S-S EWCs, slightly higher average temperatures along the MM boards array appear to stimuli the S-S WC proliferation, while the root cause of this progressive EWC leakage phenomenon at ambient temperature is, again, suitable to be the radiation environment experienced in orbit.

During on-ground tests of the SSMM equipment this phenomenon never appeared at these room temperatures and radiation is not present. In conclusion: thermal lever seems not only to excite the activation of S-S EWC but it is also a driver for increasing of their total absolute number.

3.1.3. S-S EWCs ICs/TSOPs Geometrical Distribution

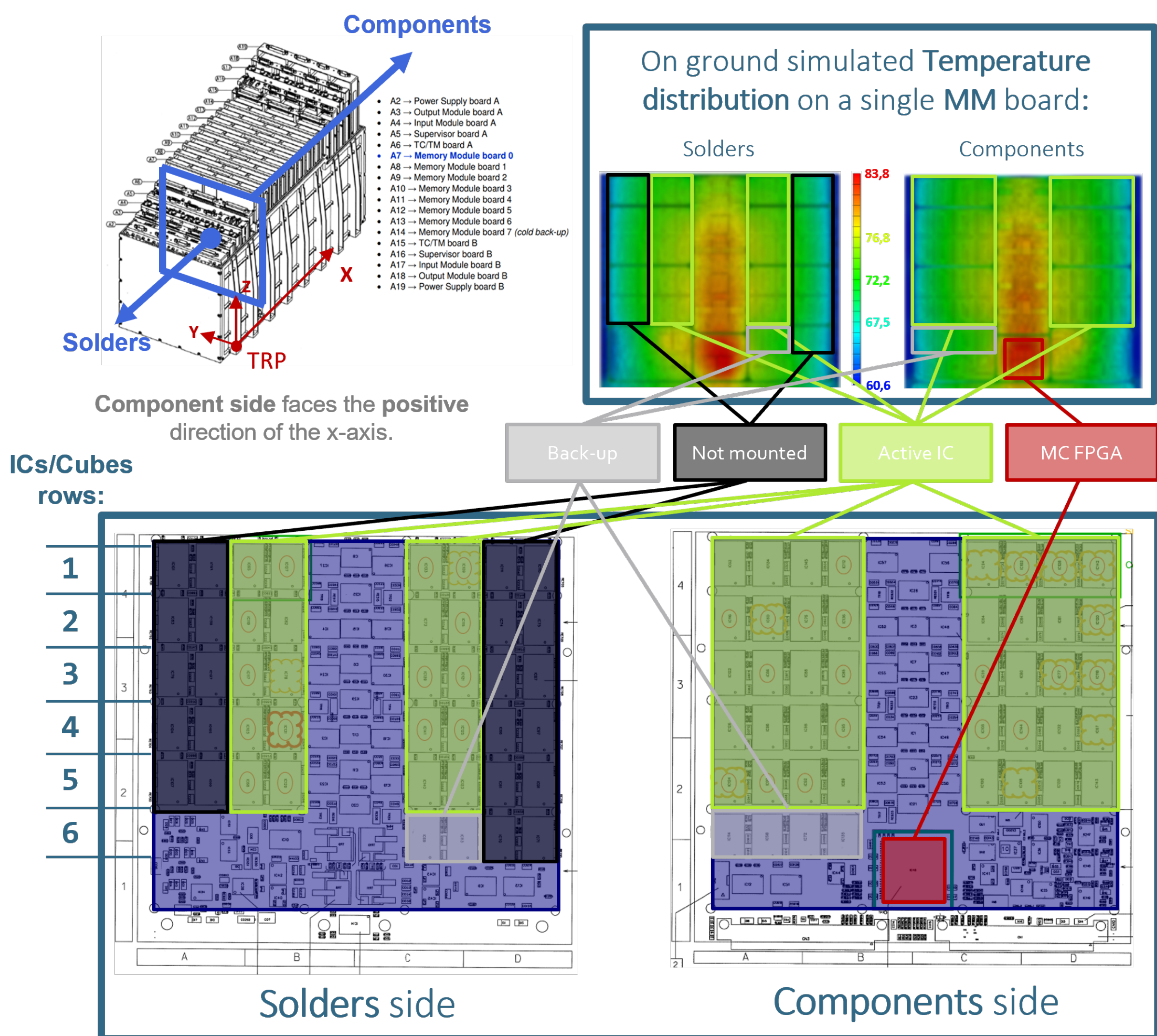

Figure 3.5: Solders side (left)/ Components side (right) ICs/cubes disposition in a MM PCB

Figure 3.5 shows the arrangement of ICs/cubes on each face of any MM PCB, in the top right corner the thermographs (made by TAS-I) of both faces are visible. Thermographs and simulations show that in steady state condition the "components side" is few degrees

warmer than the "solders" one. The distribution of all S-S EWC per IC/cube found in the entire Satellite A time frame (9 years) is reported in Figure 3.6.

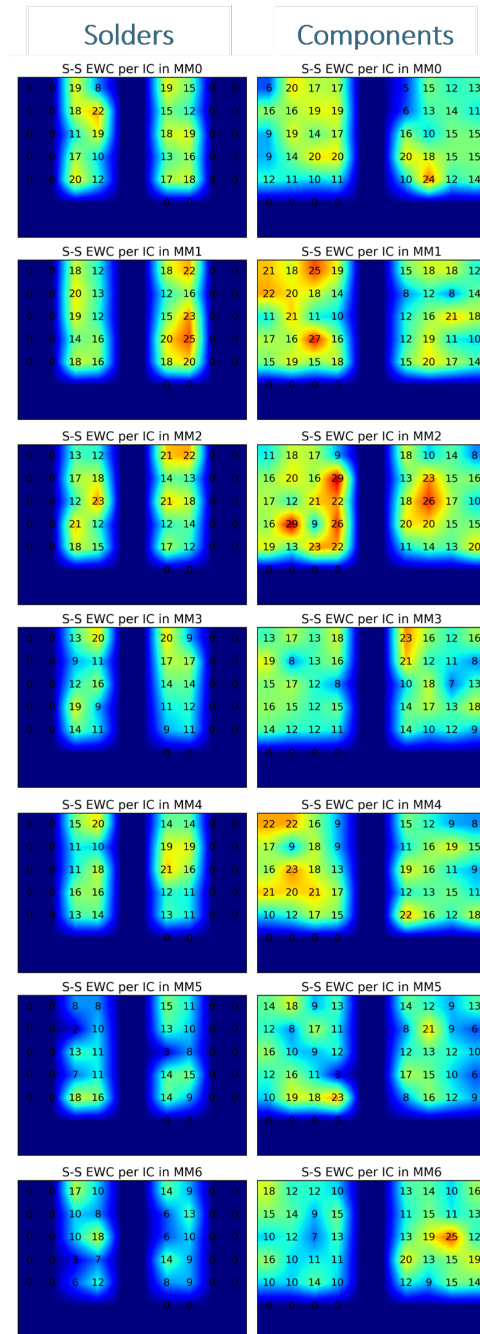

Figure 3.6: S-S EWC distribution (single addresses, without taking into account their occurrences), per IC/cube, across all memory modules (MAX_S-S_SEWC_per_IC = 29 in MM2)

As previously mentioned, the last two MM PCBs turn out to be less affected by this

SDRAM leakage phenomenon, but it is quite evenly distributed throughout each face of the PCB board, while some ICs/cubes in the "hottest" MM boards side (MM0..MM2) turn out to have a higher concentration of S-S EWCs.
The small temperature variations between the ICs/cubes along both faces of each MM PCB visible in the thermographs in Figure 3.5, do not seem to affect the appearance of these S-S EWCs in the same way in all boards.

The histograms in Figures 3.7, 3.8, 3.9 show the distribution of the S-S EWC per TSOP levels, so considering the logical partitions and columns: there is no preferential distribution along columns or TSOPs/partitions for S-S EWC proliferation. However, again, the last two external active modules (MM5 & MM6) appear less affected by this S-S EWC proliferation phenomenon also by this other perspective.

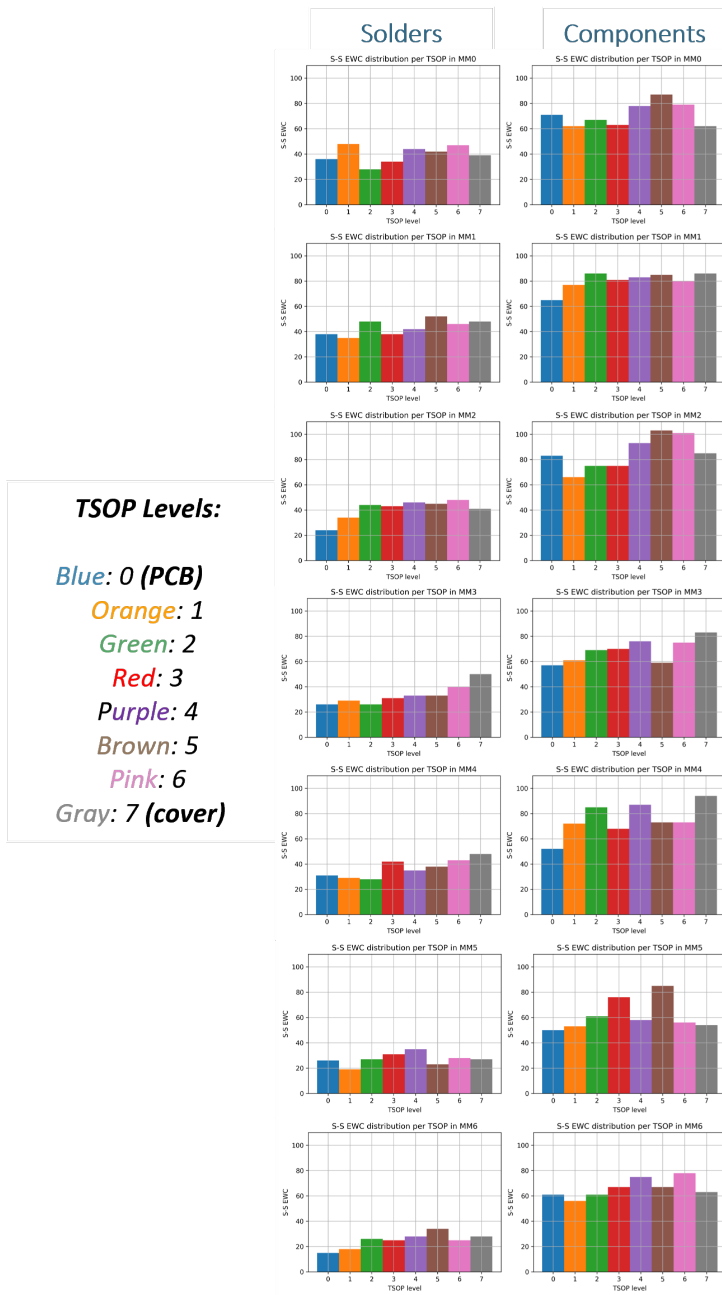

Figure 3.7: S-S EWC distribution per TSOP level in both sides of all memory module PCBs

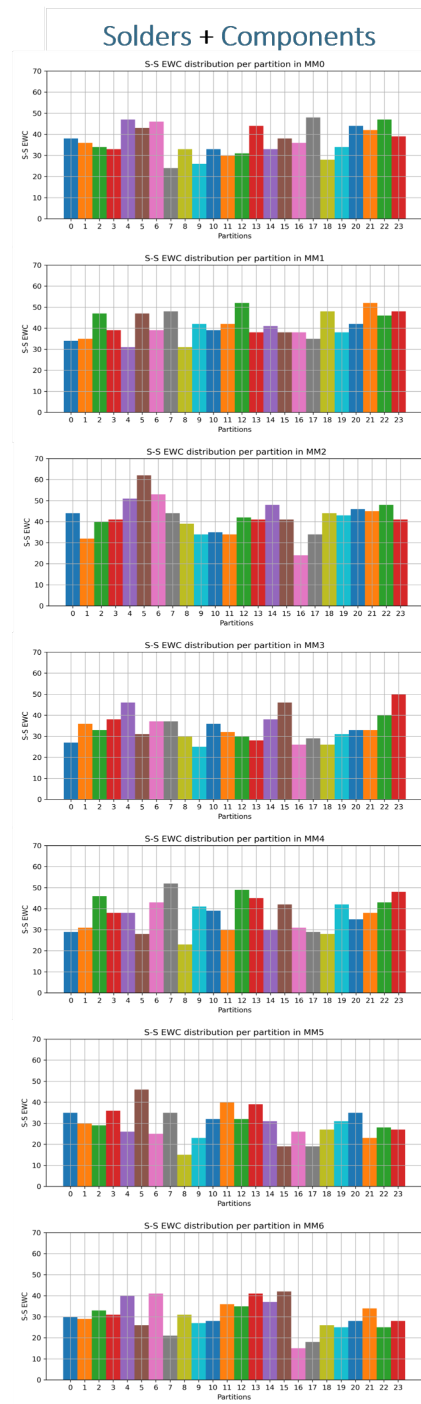

Figure 3.8: S-S EWC distribution per logical partition ([0..23] logical sub-ROWS) in all memory modules matrix

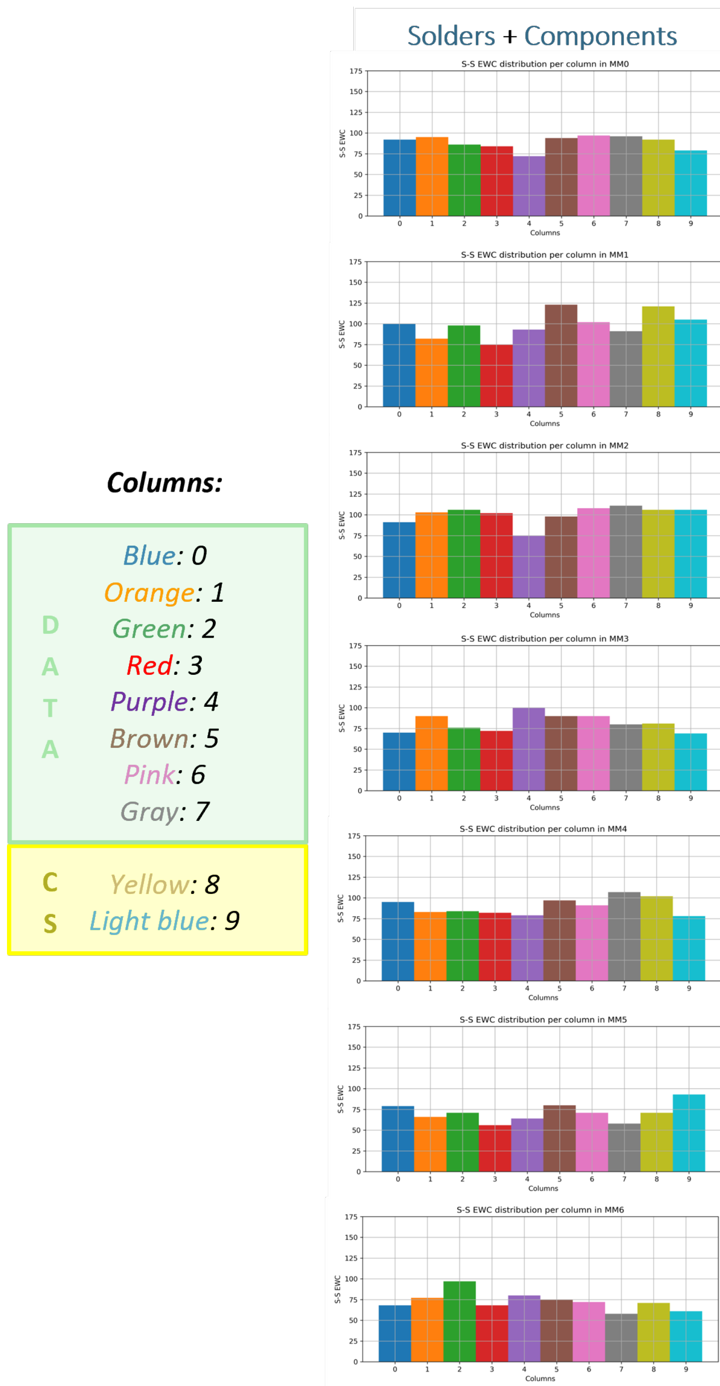

Figure 3.9: S-S EWC distribution per physical active column (0..9) in all memory modules matrix

With reference to Figure 3.9, there is no evidence of dependence from power distribution network inside a MM board and, across all MM boards: in fact, there is no bias between columns used for either DATA (0..7) or CHECK-SYMBOLS (8,9) in S-S EWC proliferation, along their maintained code-words.

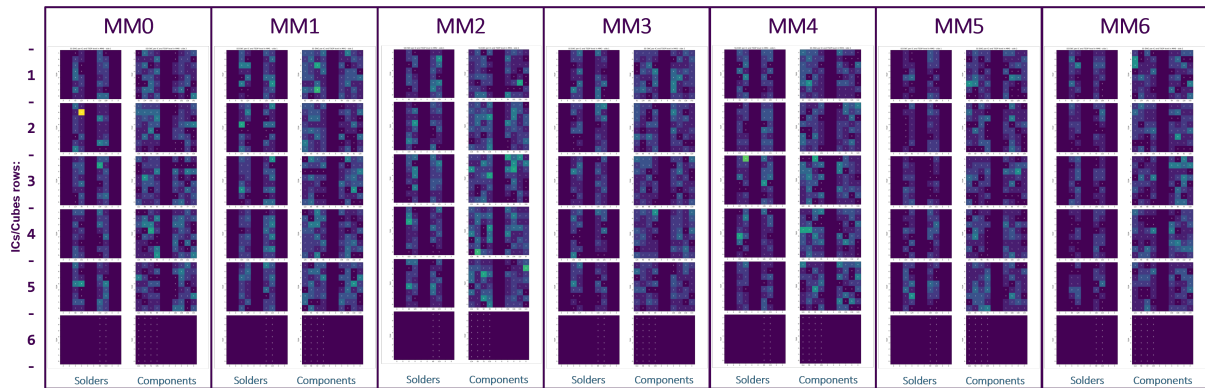

Figure 3.10: S-S EWC distribution per ICs/cubes and the relative TSOP levels in both side of all memory modules matrix

Figure 3.10 shows the number of certified S-S EWC per TSOP level within each individual IC/cube of the entire SSMM active memory PCBs. The numbers in the left side indicate the line number of ICs/Cubes as reported in Figure 3.5.
In the cubes most affected by this phenomenon, the S-S EWCs location appears to be distributed throughout all TSOP layers and not concentrated in a single one.

Note: the sixth row of ICs/cubes (referring to the mere disposition of ICs on the PCB, see also Figure 3.5) in Figure 3.10 are black since they consist of back-up/inactive ICs (installed on PCB but never activated in 9 years).

3.1.4. S-S EWCs distribution considering the re-occurrences

In this paragraph, instead of considering only the absolute number of S-S EWCs, also the number of times each cell is found in single error (and subsequently corrected) is taken into account. In Figures 3.12, 3.11, 3.12, the number of corrections performed on S-S EWCs as a function of the TSOP levels, ICs/cubes, and levels within the ICs/cubes of each memory module is reported, respectively.

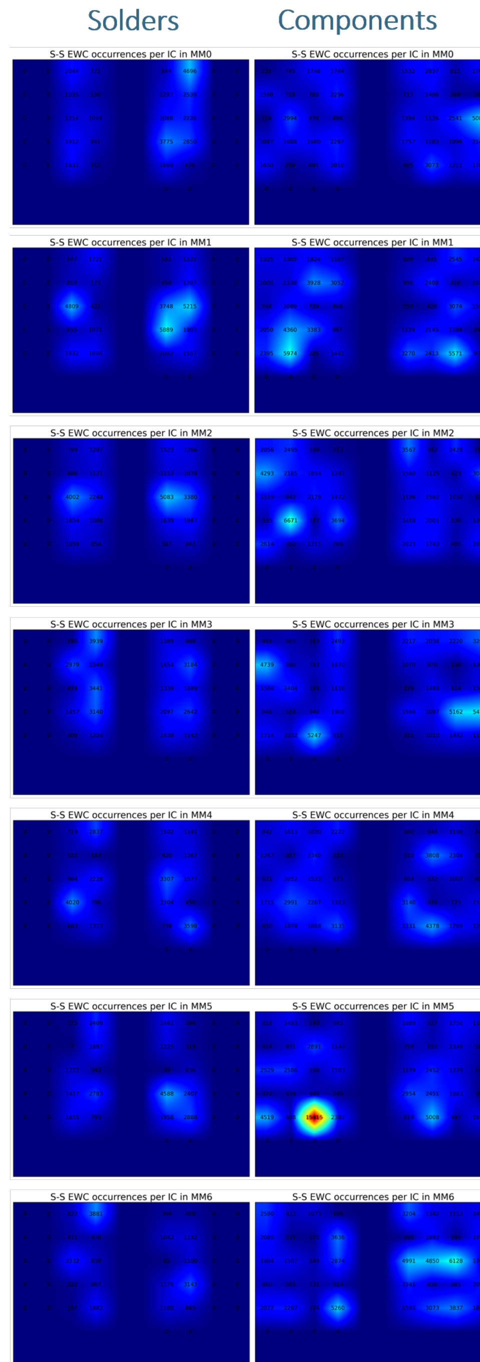

Figure 3.11: S-S EWC distribution considering also the re-occurrences per IC/cube, across all memory modules (MAX_S-S_EWC_occ_per_IC = 15415 on MM5)

As visible in Figure 3.11 and more specifically in Figure 3.13, there is one TSOP level (the "external" one close to the metallic cover) within a cube in MM5 that underwent many more corrections over time than the others ICs/cubes and TSOP levels. These recurrent corrections can be explained as more than one stuck bit within the same single symbol

of a code-word, otherwise the random pattern change in terms of 0's and 1's due to the continuous storage of scientific data in that part of the SDRAM memory would greatly reduce the number of corrections that may occur if there is only one stuck bit in the symbol constantly in leakage.

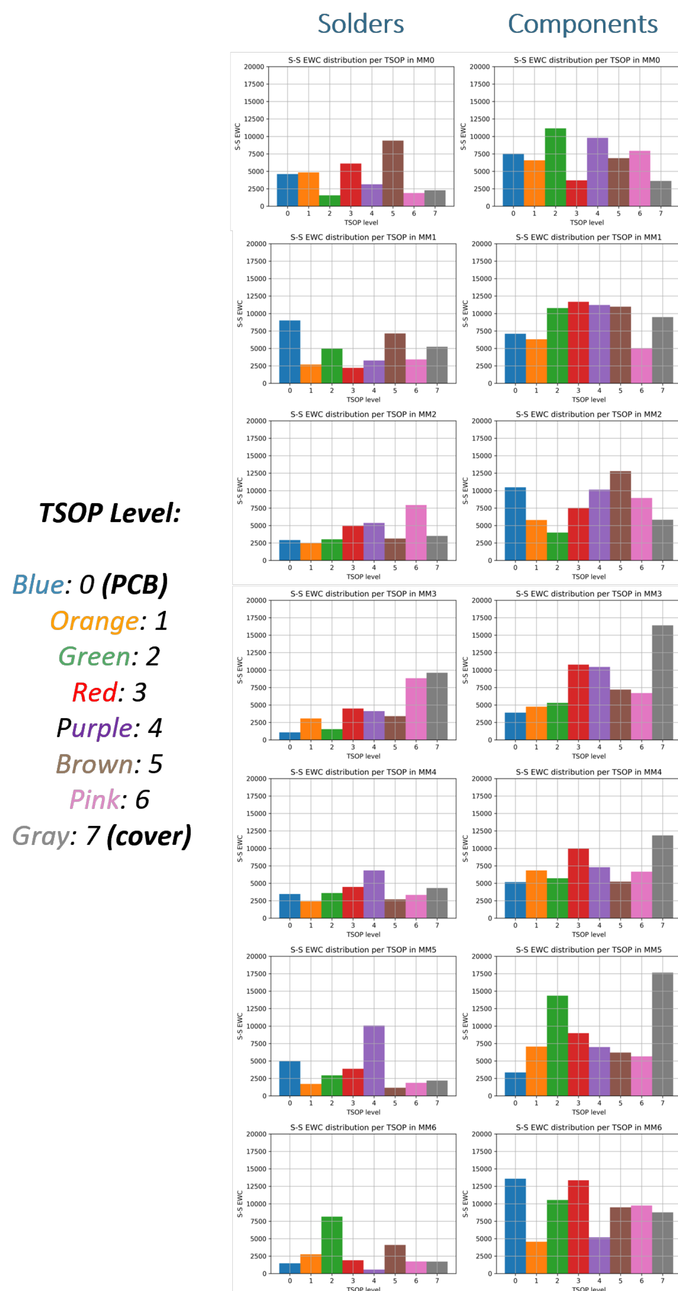

Figure 3.12: S-S EWC occurrences distribution per TSOP in both side of all memory modules

Figure 3.13: S-S EWC distribution considering also the re-occurrences of same address, per TSOP, in both sides of all memory modules matrix

In Figure 3.13, unlike Figure 3.10, it is possible to identify TSOP levels within individual IC/cube that have been in leakage for a long time period, regardless of the absolute number of weak cells in that chip. There appears to be no relationship between occurrences in TSOP levels affected by more S-S EWC, as already seen in Figure 3.12.

3.1.5. Distance between S-S EWCs addresses

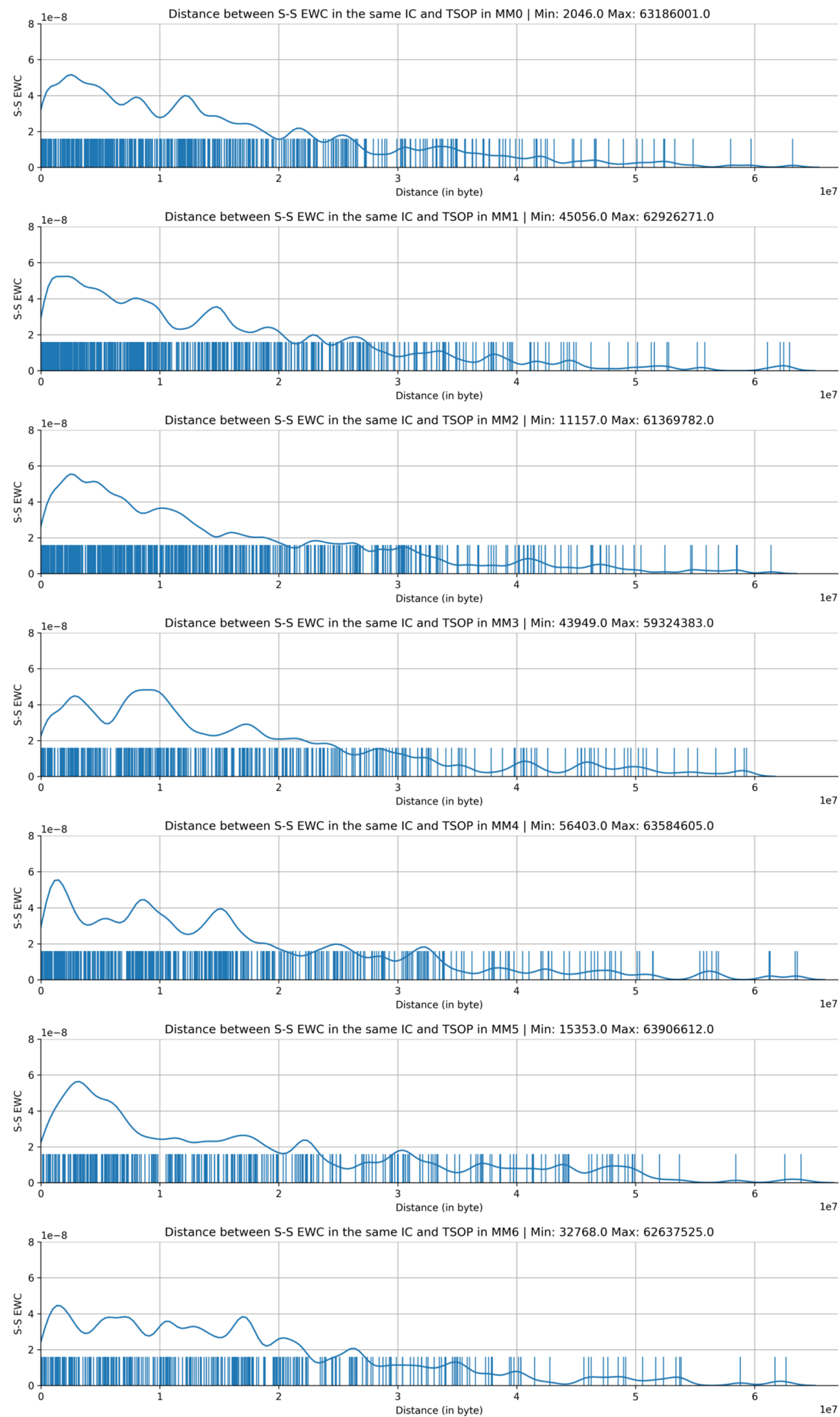

Figure 3.14: Average distance between S-S EWC inside each IC/cube and TSOP level over all MM boards

Figure 3.14 shows the distribution of the consecutive distances between S-S EWCs inside the 64 MiB (x-axis) of TSOP levels composing the ICs of all memory modules with the respective minimum and maximum values reported in the graph titles. These distances are obtained with the same procedure for every MM board:

- grouped the addresses by IC and TSOP level;
- sorted the addresses in ascending order in the range 0 to 64 MiB - 1;
- for each TSOP level inside each IC containing more than one S-S EWCs, the difference between the logical addresses "along the MM board SDRAM matrix" of each identified S-S EWCs is obtained;
- each distance is divided by 16 so as to obtain the distance in bytes within each S-S EWC inside the same TSOP layer.

Most of the "mutual" distances between S-S EWCs are concentrated below 3 MiB, with large part of peaks visible in the first 2 MiB, in all memory module PCBs. It can be seen that the last two modules, although having fewer absolute numbers of S-S EWCs, the distribution remains concentrated in 1 MiB of distances in bytes.

Note: the distribution of distances in the following chapters for M-S EWCs and EWCs are obtained in the same way but using the respective class of addresses.

3.2. Multi-Shot Extremely Weak Cell (M-S EWC) Analysis

3.2.1. M-S EWCs activation over time

In this section, the behavior of M-S EWC is analyzed as function of time within all memory modules.

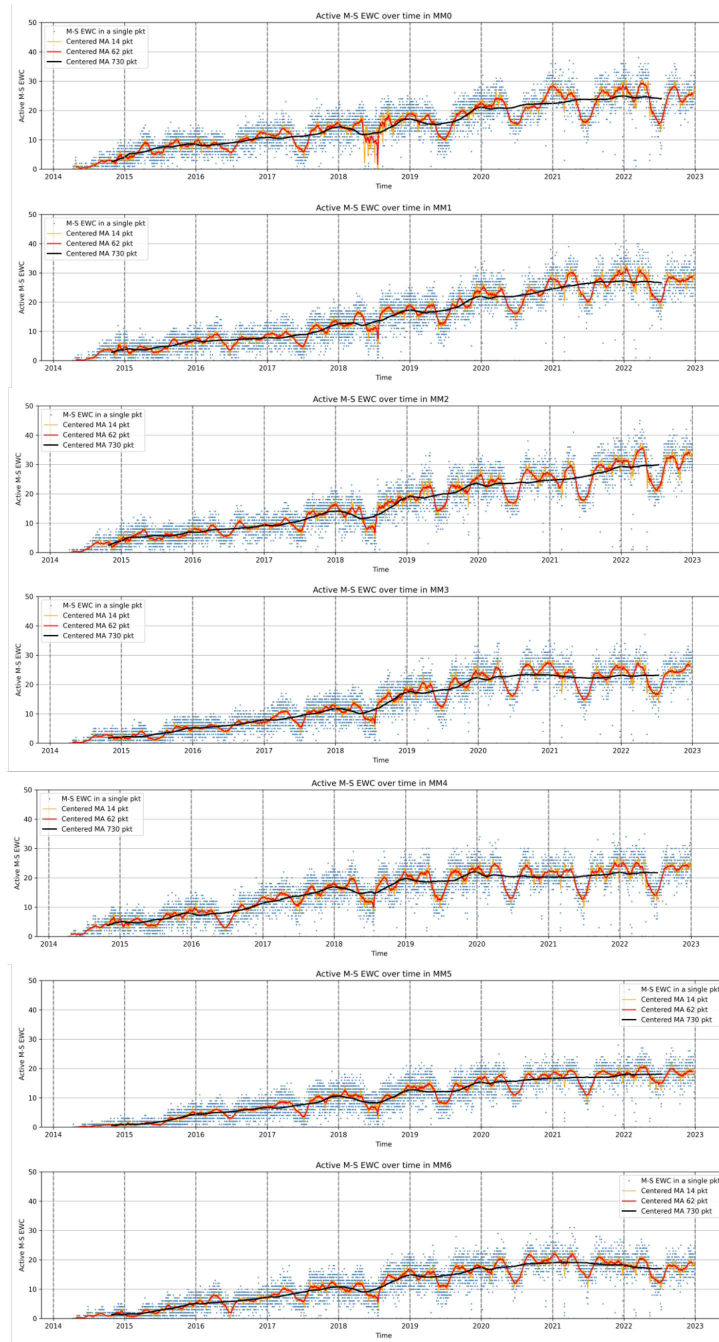

Figure 3.15: Activation of M-S EWCs over time in all MM boards, from MM0 to MM6

Figure 3.15 shows:

- **blue**: number of active M-S EWC in leakage contained in one single TM(6,6) acquisition;
- **orange**: centered moving average over one week (14 TM(6,6) aquisitions, typically in the morning and in the evening);

- **red**: centered moving average over one month (62 TM(6,6) acquisitions);
- **black**: centered moving average over one year (730 TM(6,6) acquisitions).

As per S-S EWC, a correlation between the activation of M-S EWC and the SSMM equipment TRP became progressively visible on all memory modules across the 9 years of mission of Satellite A.
Particularly noticeable is that although the total absolute number of M-S EWC in each MM board is smaller than S-S EWC, they turn out to be more persistently active with respect to the S-S EWCs: i. e. the average number of active M-S EWC over time is higher than S-S EWC in the same time-frame and SSMM equipment TRP condition (almost 2 times more).
In addition, referring to the Figure 3.16, the seasonal eclipses period seems to affect the 2 types of cells differently, with the S-S EWCs being almost zeroed out during colder TRP periods, while the M-S EWCs always maintain a relatively high number of active cells over the entire timeframe (9 years).

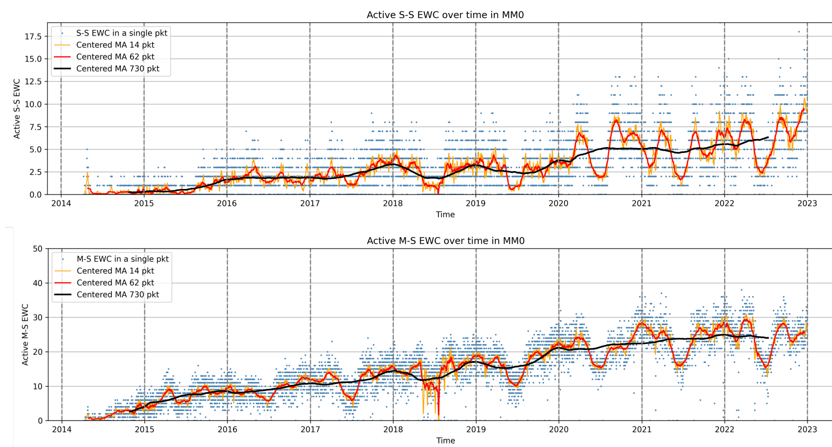

Figure 3.16: Comparison between activation of S-S EWC (above) and M-S EWC (below) on MM0

Lastly, the downward spikes around the year 2018, during the MM0 anomaly described in Chapter 1.3.2, can be explained by the several HE events and SSMM boards re-init, which characterized that period. These spikes are present in almost all memory boards, especially in the first one (MM0): they are related to the lack of TM packets due to the SSMM boards reboots occurred in that period.
In the case of the first module (MM0), these peaks are more visible due to the numerous TM(6,6) packets discarded during data processing to handle the high occurrence of HEs in that period, as explaned in Chapter 2.1.

3.2.2. Total certified number of M-S EWCs over time

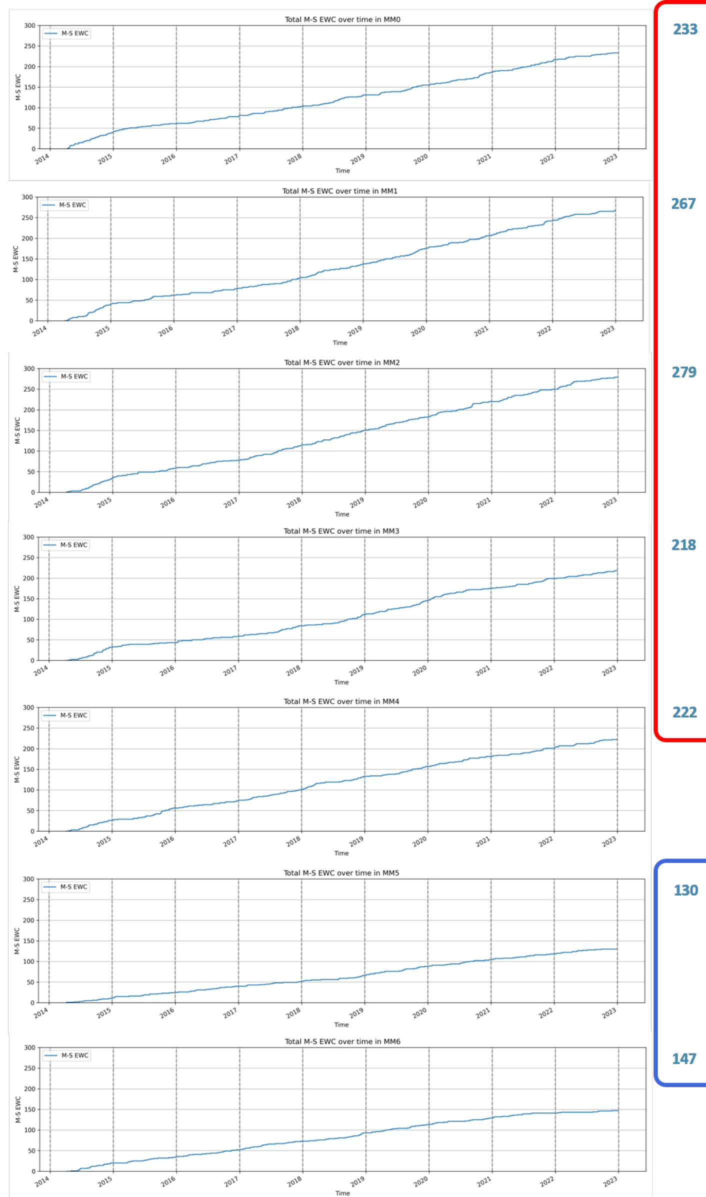

Figure 3.17: Total certified number of M-S EWC over time in all MM boards

As per S-S EWC, Figure 3.17 shows that the M-S EWCs certified number increases progressively over time in a linear way, whether or not they are active over all MM boards, but their final value is about an order of magnitude less than the S-S EWCs. Also MM5 and MM6 boards (the coldest MM boards of the entire memory array) show less active and less total M-S EWCs absolute number, similarly as seen for S-S EWCs. The S-S EWC and M-S EWC behaviour is very similar.

3.2.3. M-S EWCs ICs/TSOPs Geometrical Distribution

The graphs in Figure 3.18 show the highest M-S EWCs proliferation appear, again as per S-S EWCs, mainly concentrated in the "hottest" MM boards (MM0..MM4) and on their Components side, that is always warmer than the Solders one.

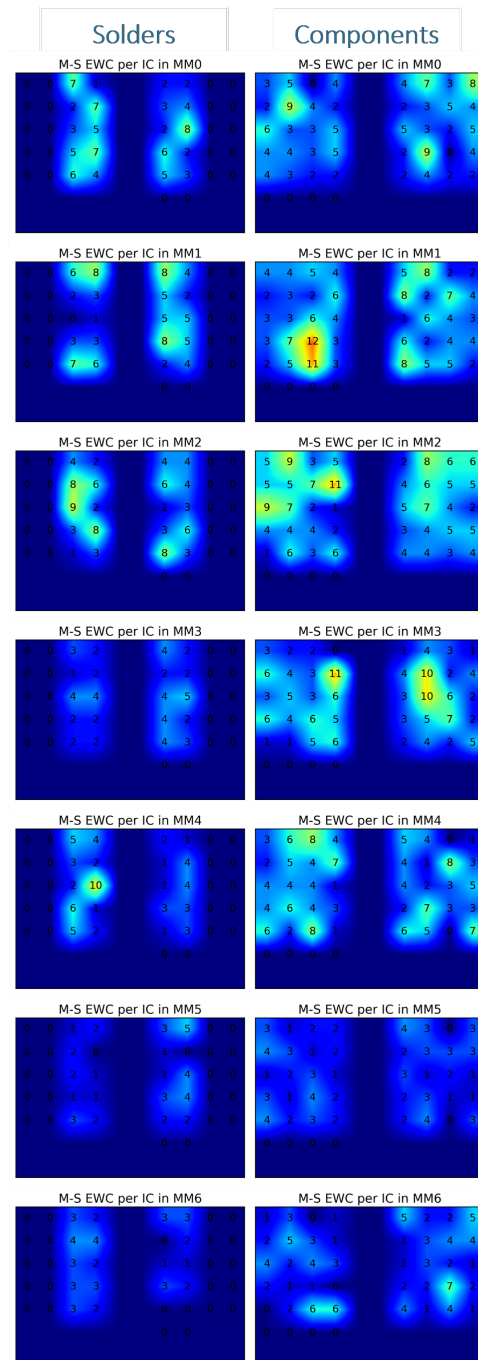

Figure 3.18: M-S EWC distribution (single address, without computing their occurrences), per IC/cube, across all memory modules (MAX_M-S_EWC_per_IC = 12 on MM1)

Histograms in Figures 3.19, 3.20, 3.21 show the distribution of the M-S EWC by TSOP levels, partitions and columns: as per S-S EWC, it can be seen that there is no bias for M-S EWC proliferation. However, the last two modules are, on average, less affected by this phenomenon. No bias among column, partition and TSOP level is found also for M-S EWCs.

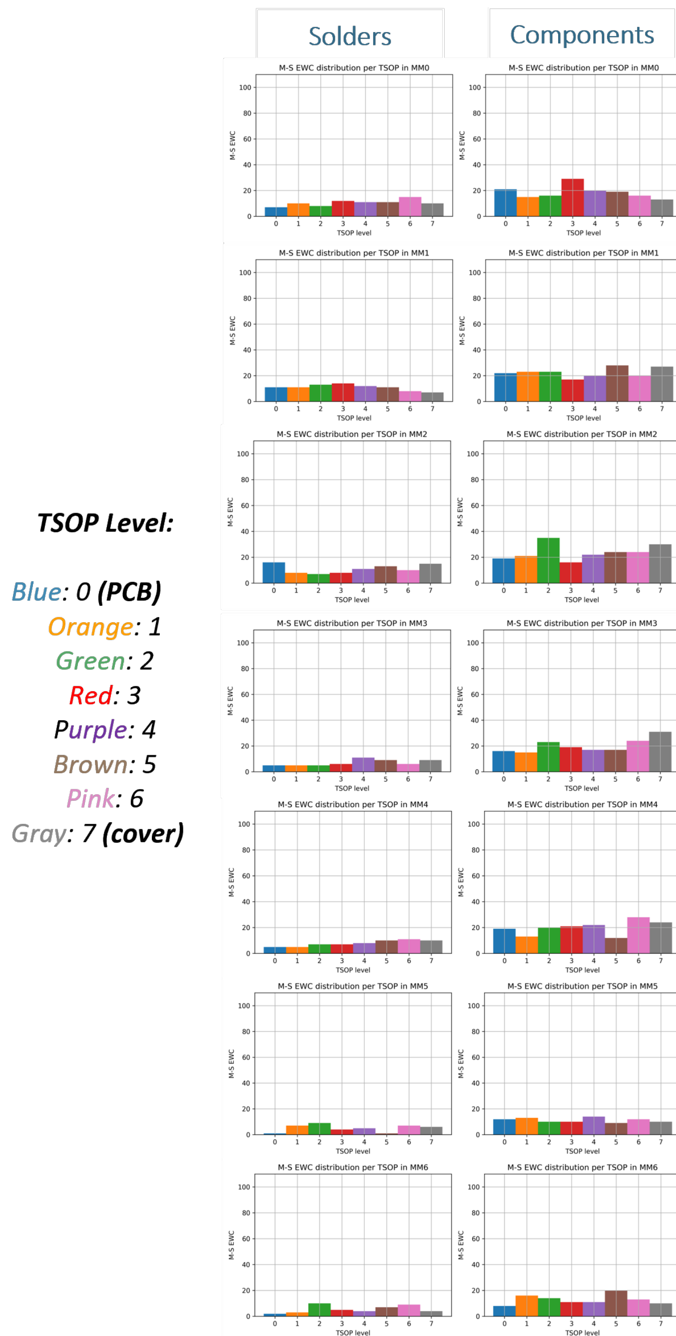

Figure 3.19: M-S EWC distribution per TSOP in both side of all memory modules

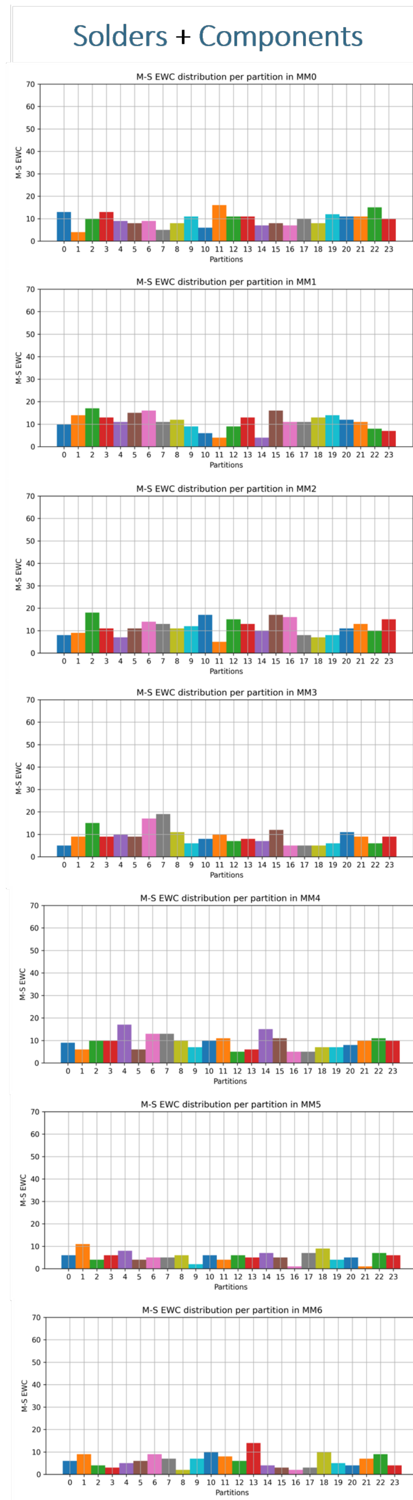

Figure 3.20: M-S EWC distribution per logical partition ([0..23] logical sub-rows) in all memory modules matrix

Figure 3.21: M-S EWC distribution per physical column (0..9) in all memory modules matrix

With reference to Figure 3.21, as per S-S EWC, there is no evidence of dependence from power distribution network inside a MM board and across MM boards: there is no difference in occurrences between columns used for DATA (0..7) or for CHECK-SYMBOLS

(8,9).

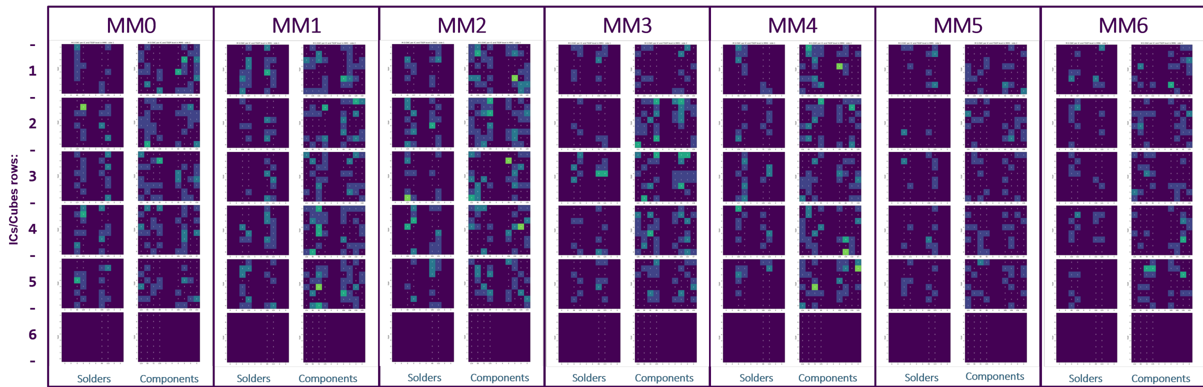

Figure 3.22: M-S EWC distribution per ICs/cubes and the relative TSOP levels in both side of all memory modules matrix

3.2.4. M-S EWCs distribution considering the re-occurrences

Similar to S-S EWCs analysis, we also considered the number of times each cell identified as M-S EWC is found in single error (and subsequently corrected). In Figures 3.23, 3.24, 3.25 the number of corrections performed on M-S EWCs as a function of the TSOP level, IC/cube, and levels within the ICs/cubes of each memory module is reported, respectively.

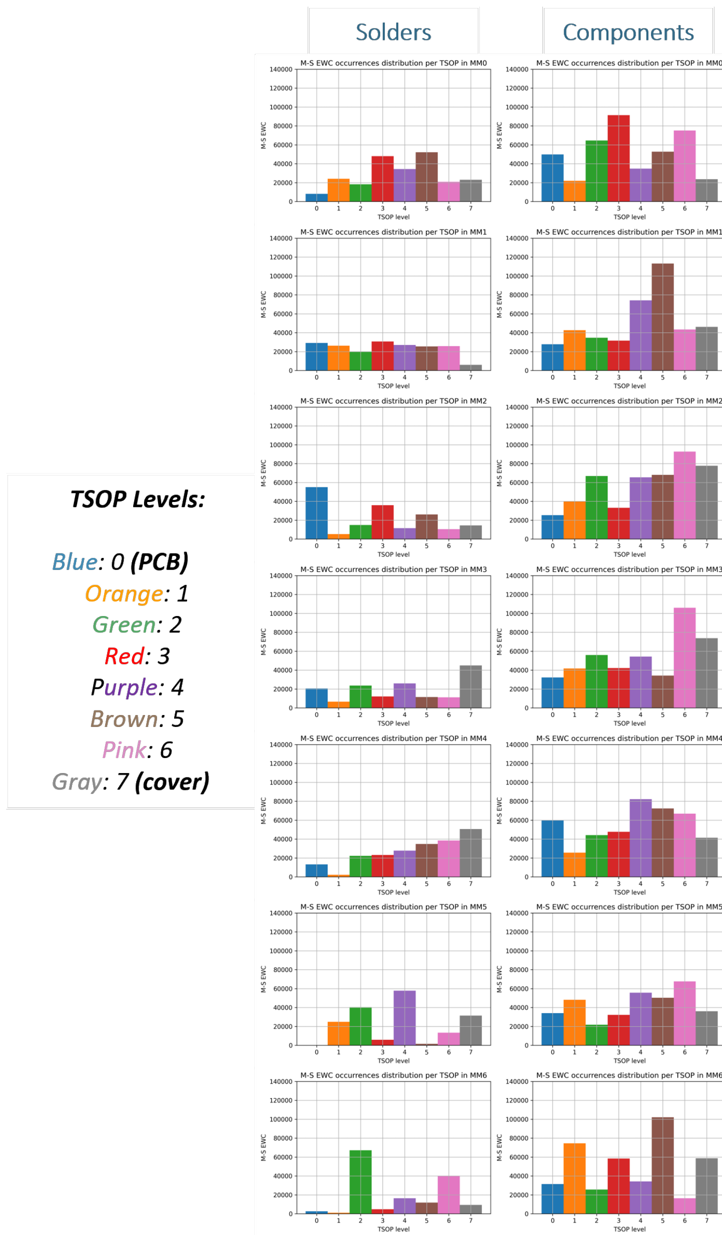

Figure 3.23: M-S EWC occurrences distribution per TSOP in both side of all memory modules

As per S-S EWC, there are some TSOP levels within different cubes that underwent many more corrections over time than the others. Again, these frequent corrections can be related to more than one stuck bit within a single symbol of a code-word.

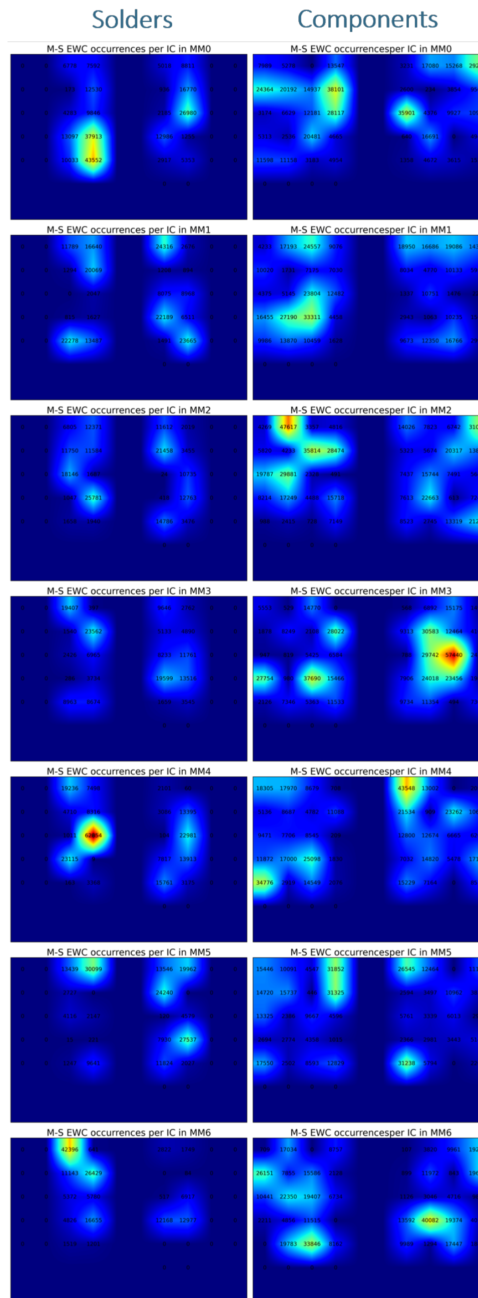

Figure 3.24: M-S EWC occurrences distribution per IC/cube, across all memory modules (MAX_M-S_EWC_occ_per_IC = 62854 on MM4)

Again, the "hot spots" related to frequently leaking cells are more located in the Components side of all the memory boards.

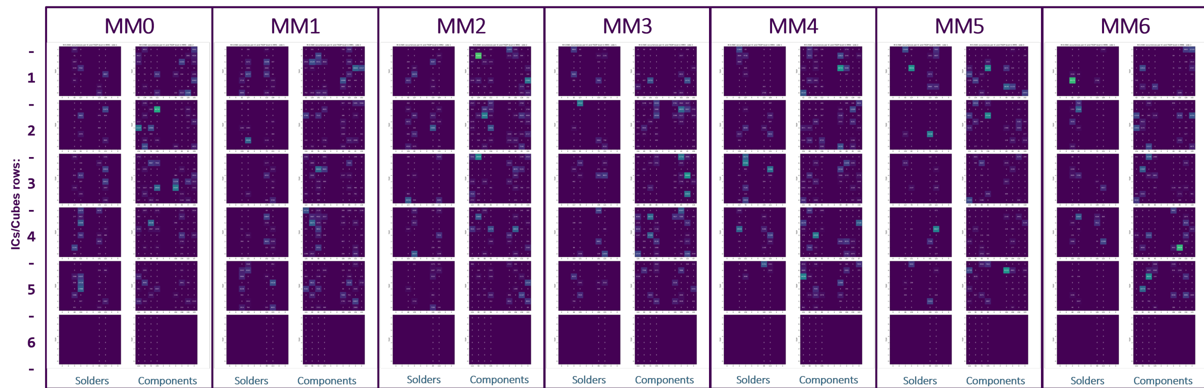

Figure 3.25: M-S EWC occurrences distribution TSOP levels in each IC/cube in both side of all memory modules matrix

As per S-S EWCs, the "hot spots" are randomly distributed with respect to TSOP levels and ICs/cubes, most likely they are characterised by more than one stuck bits within one code-word symbol.

3.2.5. Distance between M-S EWCs addresses

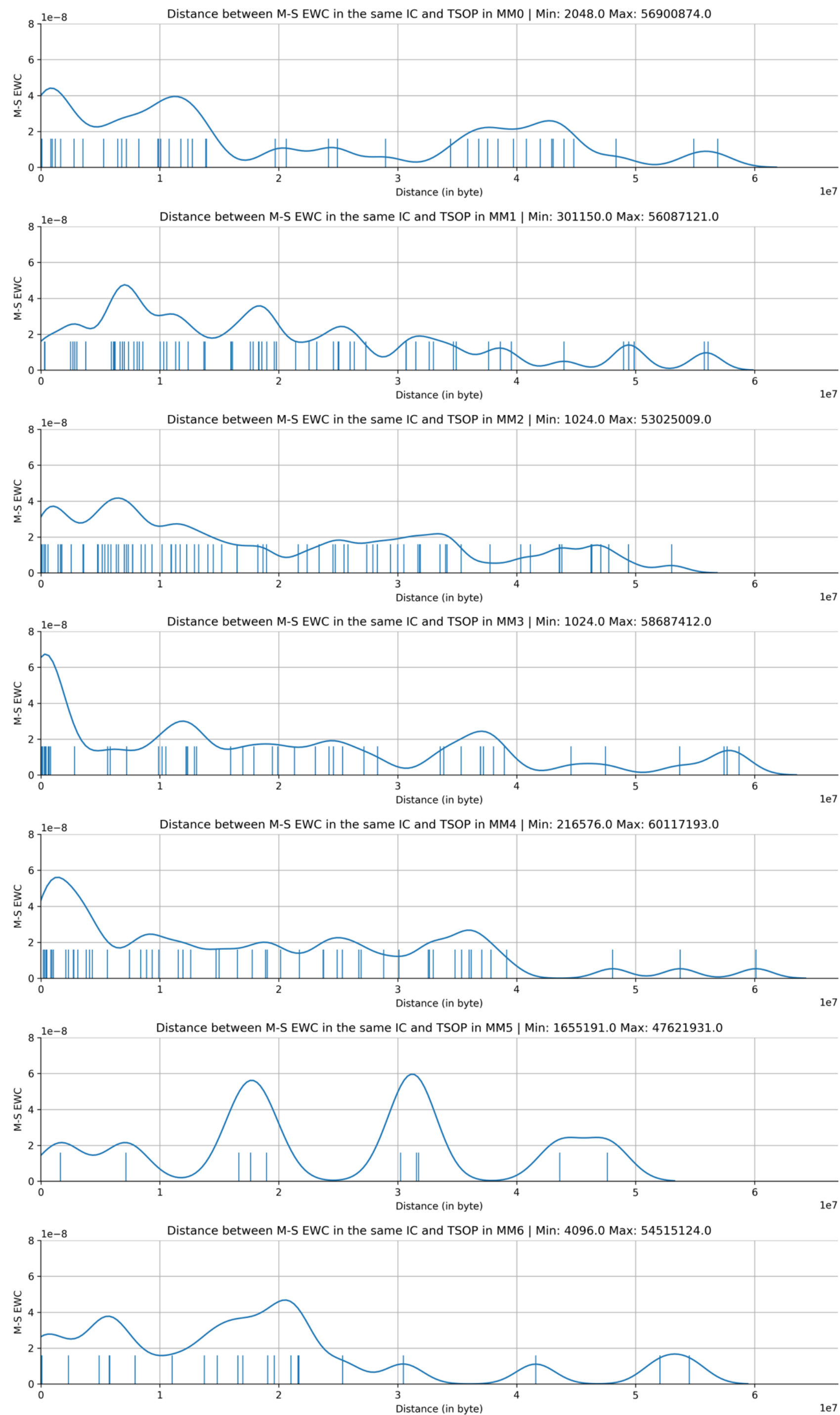

Figure 3.26: Distance between M-S EWC indide the same IC/cube and TSOP level in all MM boards

The "mutual" distance between these M-S EWCs class shows a "flatter" distribution w.r.t. the S-S EWCs. The fact that the minimum cell distance turns out to be precisely 2048 and 4096 in several cases may depend on the internal structure of the SDRAM TSOP that is organised in 2048-byte "inner" pages.

3.3. S-S EWC + M-S EWC Analysis

All the similarities encountered and highlighted in the previous chapters led to consider the two types of EWC ("S-S" and "M-S") as the expression of a same leakage phenomenon induced by radiation hits, since:

1. the activation of both phenomena is phased with the temperature of the TRP of the SSMM and they have similar patterns over time;
2. both phenomena grow linearly over time, with the same and clear clustering between the first 4 MM boards (MM0..MM4) generally "warmer" with resect to the last 2 (MM5 and MM6) that are "colder" in the SSMM configuration operated on Satellite A;
3. their distribution and behavior on a corresponding face of each memory module is similar.

The root cause of both leakage phenomena is suitable to be the radiation environment experienced in orbit since they never appeared on Ground.

This is why in the next chapter these two phenomena will be studied and considered together and from now on, we will use the acronym EWC to refer to both S-S and M-S EWC together.

3.3.1. EWCs activation over time

In this section, the behavior of all types of EWCs is analyzed as function of time within all MM boards summing the contributions analysed in details in the previous sections.

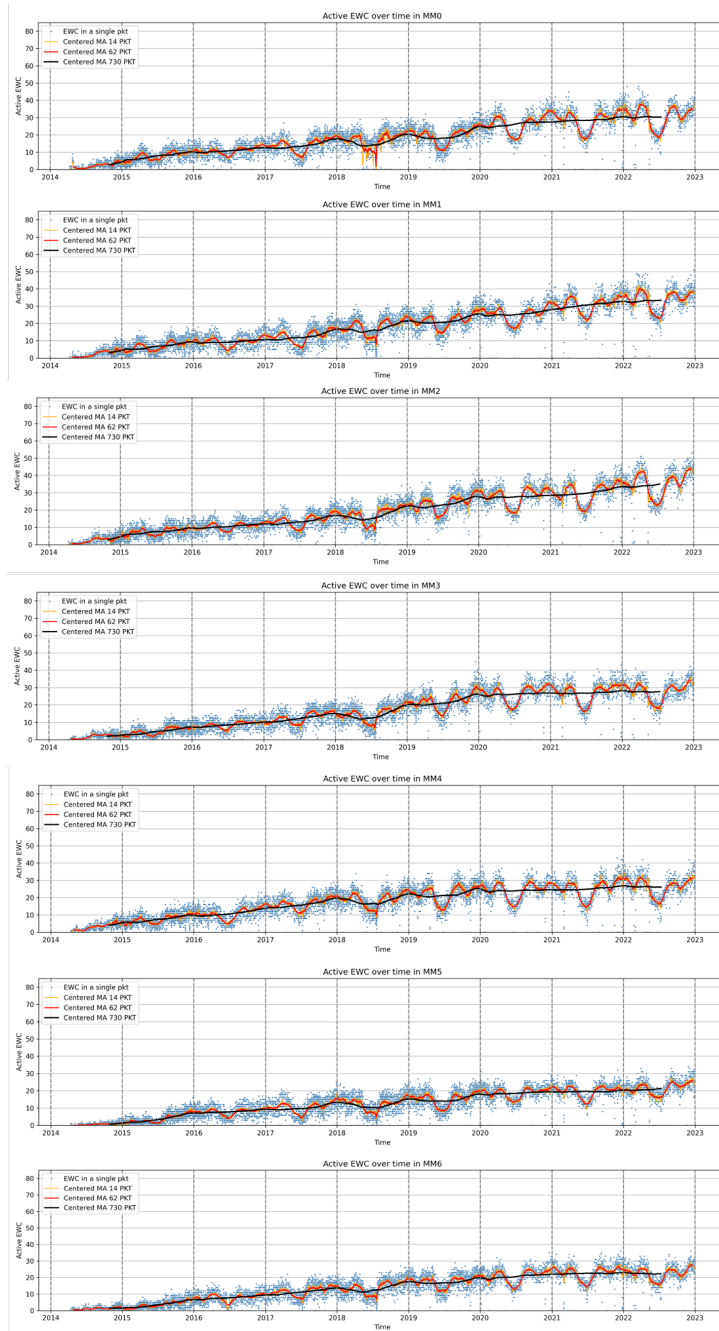

Figure 3.27: Activation of EWC over time in all MM boards, from MM0 to MM6

As before, Figure 3.27 represents:

- **blue**: number of certified active EWC in leakage contained in one single TM(6,6) acquisition;
- **orange**: centered moving average over one week (14 TM(6,6) aquisitions, typically in the morning and in the evening);

- **red**: centered moving average over one month (62 TM(6,6) acquisitions);
- **black**: centered moving average over one year (730 TM(6,6) acquisitions).

As expected, the combined behaviour of both phenomena follows the TRP waveform of the SSMM unit. The differences between the last two modules and the others is still evident. MM0, MM1 and MM2 are the "hottest memory" boards and are the ones with the higher average number of active EWC at a time.

From a visual point of view, the indirect effect of the constant leakage of EWCs can also be seen from Figure 2.7, which shows the values of the MMx_CE counter contained in the TM(3,25). The increase in the number of EWCs in leakage at the same time causes the counter to increase more repidly, this is visible looking at the increasing condensation of the counter wraps arounds with time.

3.3.2. Total certified number of EWCs over time

The sum of both phenomena maintains steady growth with a constant increase of roughly three orders of magnitude after nearly 9 years in orbit over all MM boards, mainteining the relative differences between the first 5 MM boards (MM0..MM4) and the last 2 (MM5 and MM6).

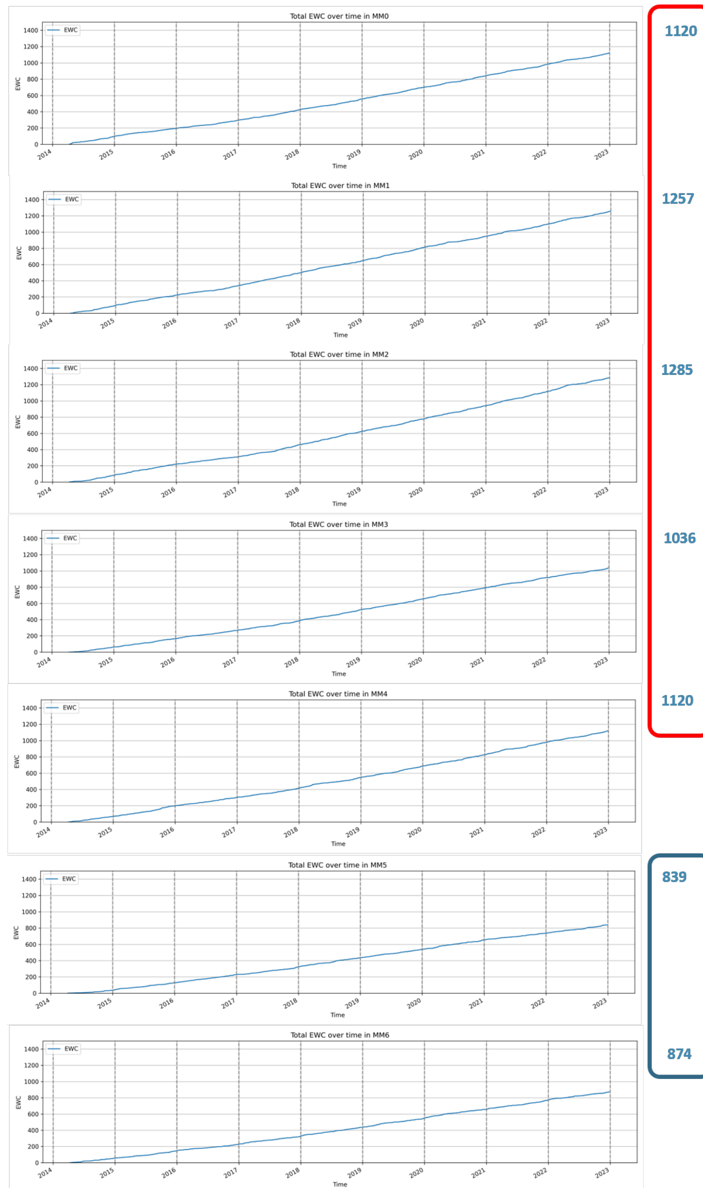

Figure 3.28: Total certified number of EWC over time in all MM boards

3.3.3. EWCs ICs/TSOPs Geometrical Distribution

As before, the highest concentration of EWCs still result in the hottest side of each MM boards (components side).

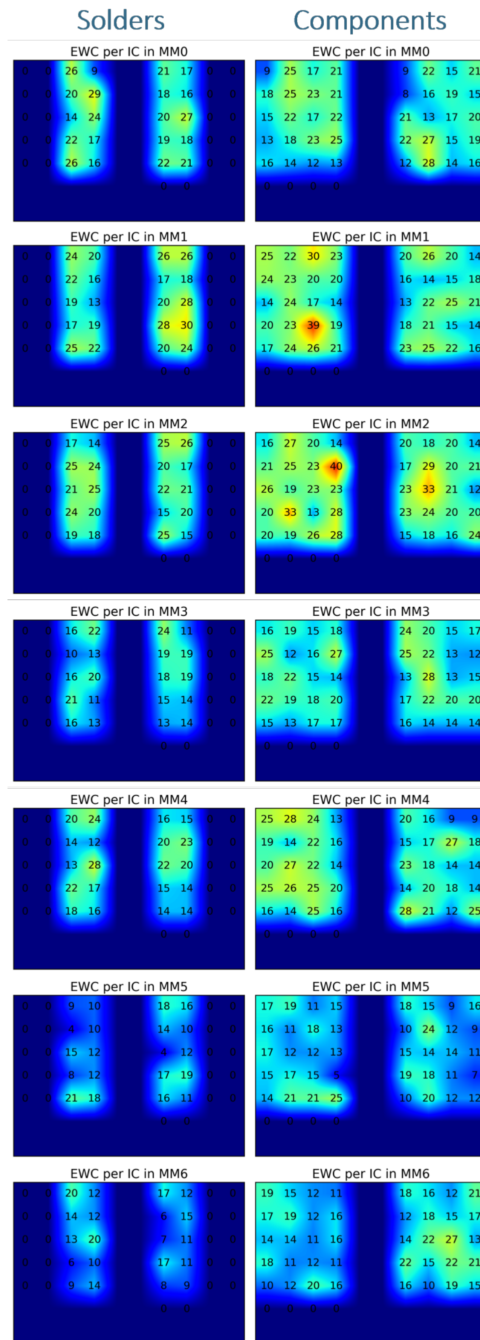

Figure 3.29: EWC distribution (single address, without computing their occurrences), per IC cube, across all memory modules (MAX_EWC_per_IC = 40 on MM2)

Histograms in Figures 3.30, 3.31, 3.32, show the distribution of the EWC by TSOP levels, partitions and columns. There is no bias for both types of EWC proliferation. As in previous chapters, the last two modules are on average less affected by these phenomena.

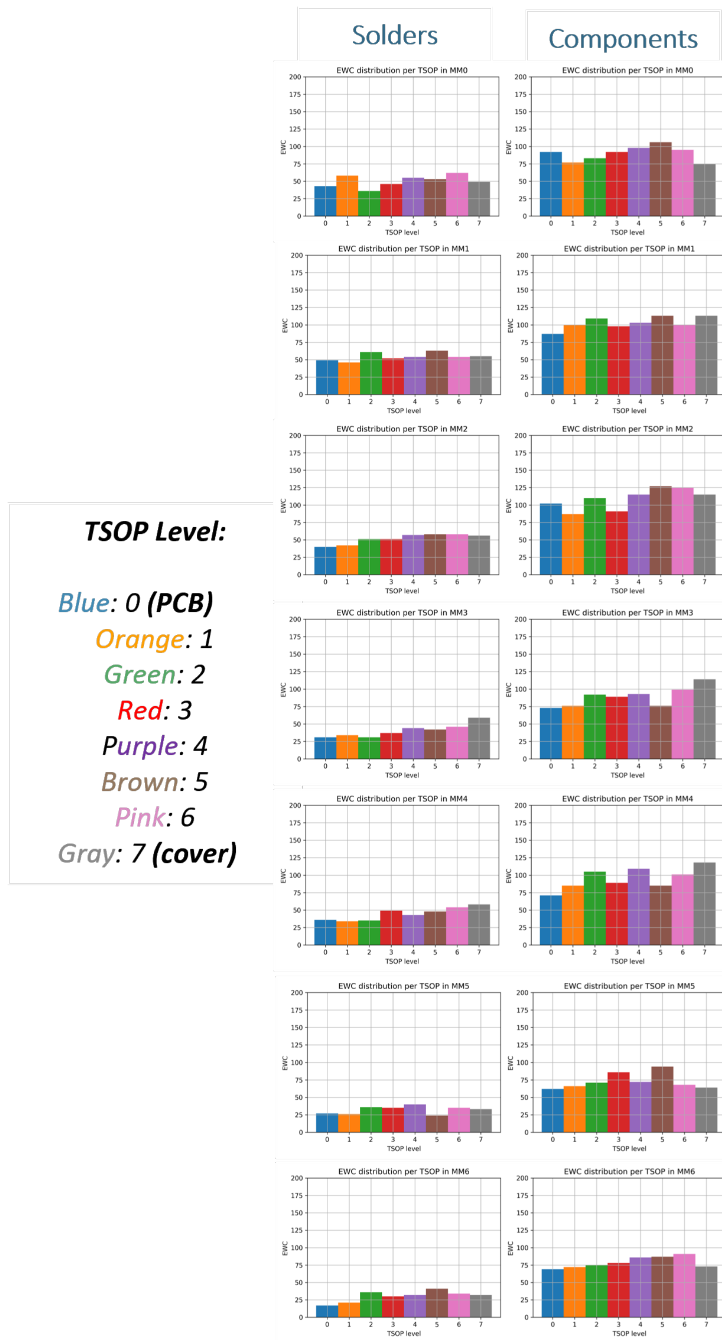

Figure 3.30: EWC distribution per TSOP in both side of all memory modules

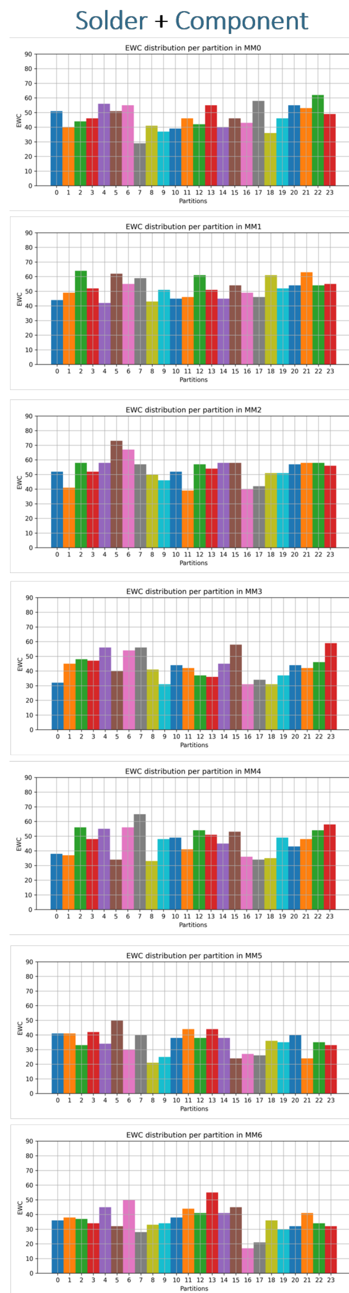

Figure 3.31: EWC distribution per logical partition ([0..23] logical sub-ROWS) in all memory modules matrix

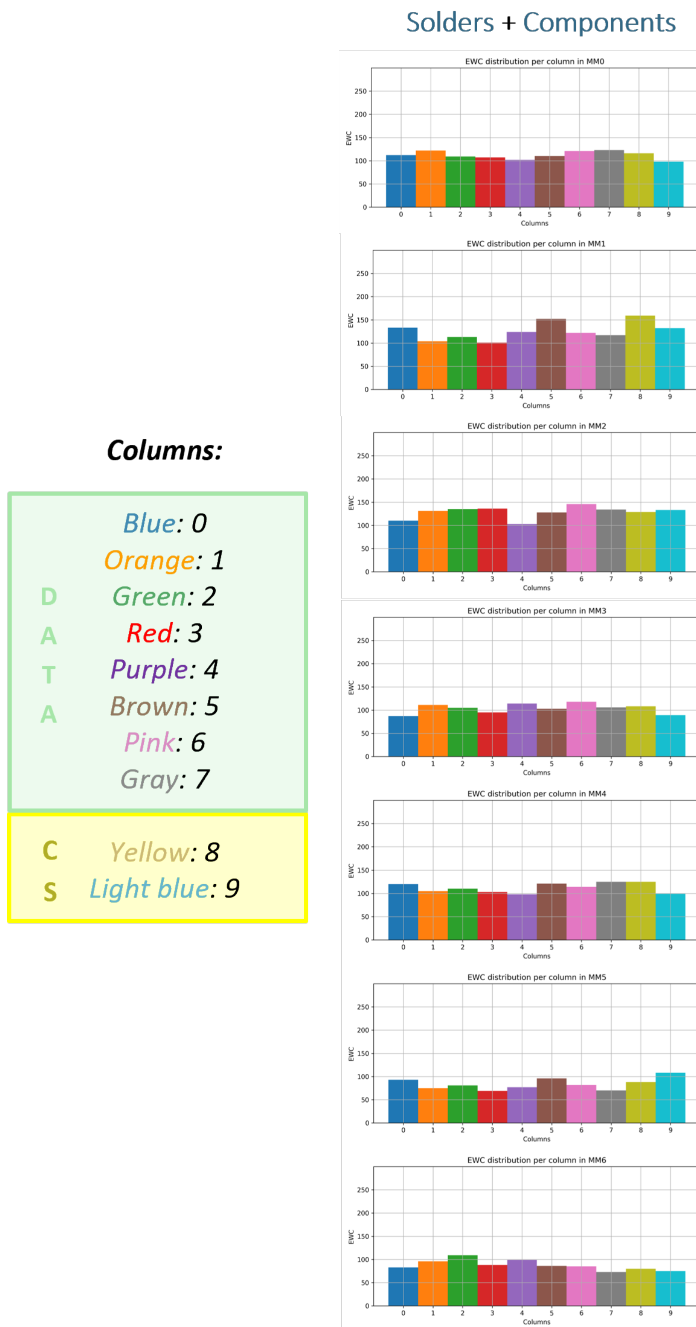

Figure 3.32: EWC distribution per physical column (0..9) in all memory modules matrix

With reference to Figure 3.32, there is no evidence of dependence from power distribution network inside a MM board and, across all MM boards: there is no bias between columns used for either DATA (0..7) or CHECK-SYMBOLS (8,9) in EWCs proliferation.

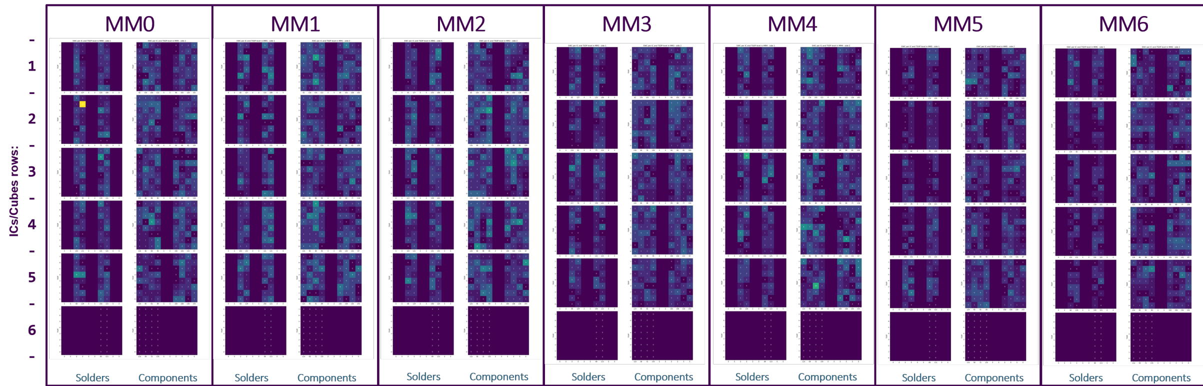

Figure 3.33: EWC distribution per ICs and TSOP levels in both side of all memory modules matrix

In Figure 3.33, it is possible to identify TSOP levels within individual IC/cube that present higher number of EWC. Their location appear to be distributed throughout all TSOP levels and not concentrated in a single one. There are no areas of high concentrations of both types of EWCs, their appearance is almost uniformly distributed (no particular TSOP levels or cubes) over all MM boards faces (with the relative differences in the last two coldest memory modules).

3.3.4. EWCs distribution considering the re-occurrences

In this chapter the number of times each EWC found in single error (and subsequently corrected) is considered. In Figures 3.34, 3.35, 3.36 the number of EWCs corrections as a function of the TSOP level, IC/cube, and levels within the ICs/cubes of each memory module is reported, respectively.

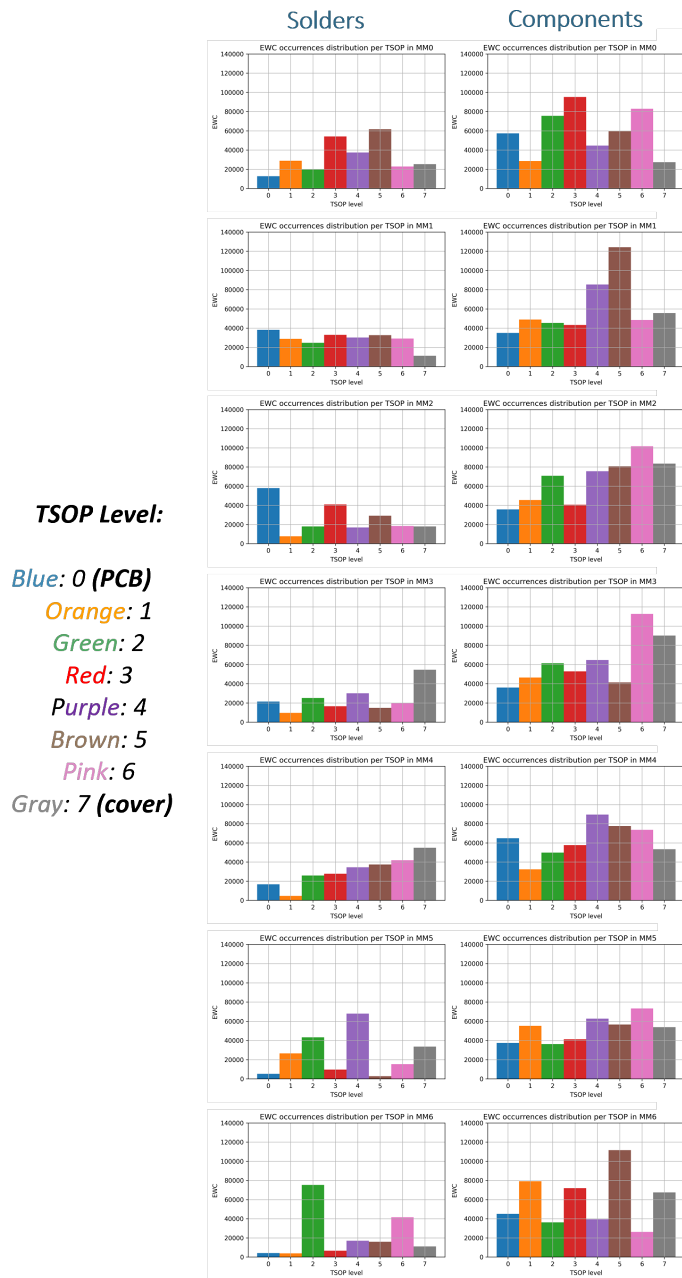

Figure 3.34: EWC occurrences distribution per TSOP in both side of all memory modules

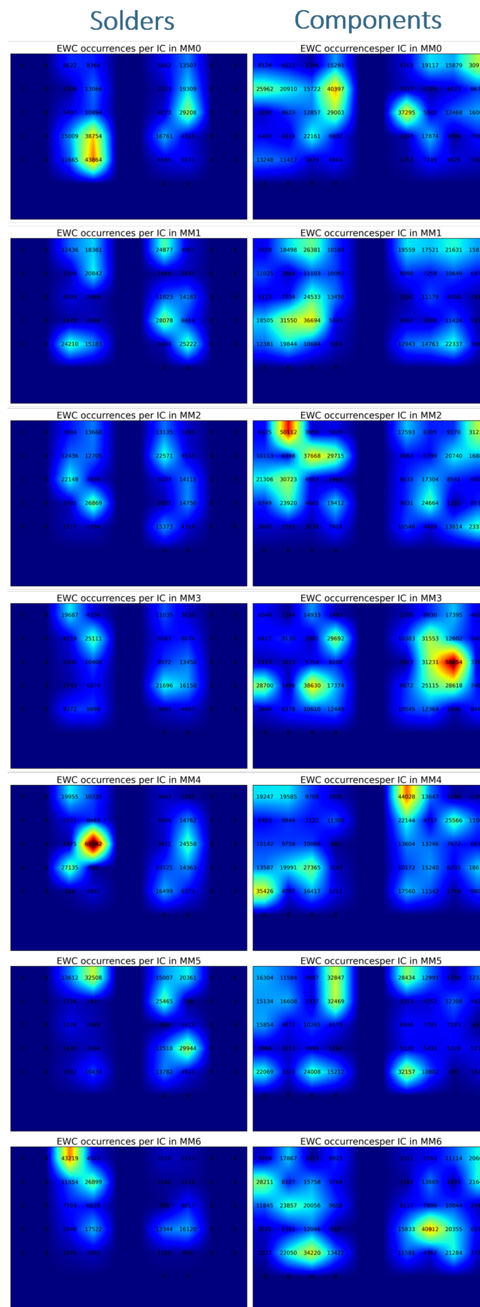

Figure 3.35: EWC occurrences distribution per IC cube, across all memory modules (MAX_EWC_occ_per_IC = 65082 on MM4)

The "hot spots" defined in previous chapters characterized by permanently leaking cells, probably caused by more than one stuck bit within a code-word symbol, are still found to be more widely distributed on the Components side of all memory module PCBs. Eventually, summing the contributions, there appears to be no correlation between particularly active S-S EWCs and M-S EWC locations, as visible by comparing Figure 3.35

with Figures 3.11 and 3.24.

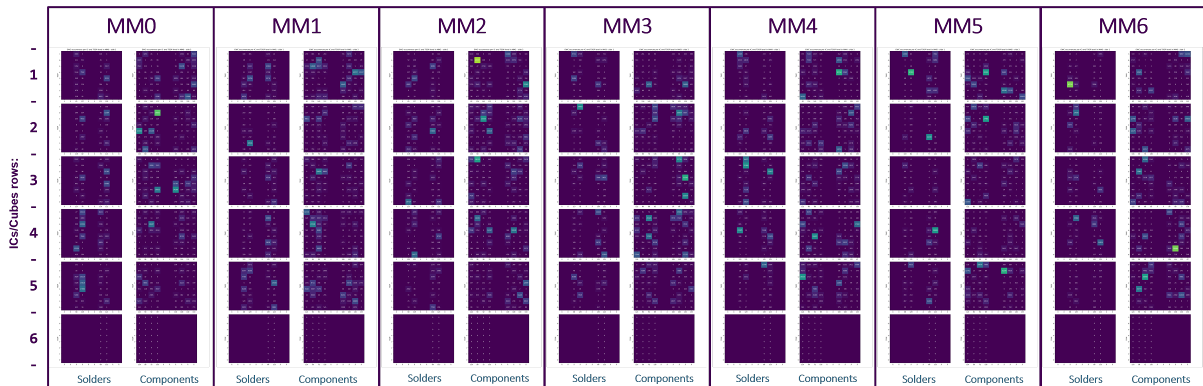

Figure 3.36: EWC distribution considering also the re-occurrences of same adderesses, per TSOP, in both side of all memory modules matrix

In Figure 3.36 it is possible to identify TSOP levels within individual IC/cube that have been in leakage for a long time period, regardless of the absolute number of weak cells in that chip. There appears to be no bias in TSOP levels affected by more EWCs.

3.3.5. Distance between EWCs addresses

Figure 3.37: Distance between EWC indide the same IC/cube and TSOP level in all MM boards

The distribution "mutual" of distances between EWCs is more influenced by S-S EWCs distribution, with higher concentration in < 1 MiB of distance. The minimum distance results, in almost all memory modules, a integer multiple of 1024.

3.4. SEU Analysis

By the term SEU we will refer to a change in the state of a SDRAM cell ("0" or "1"), generally caused by one single ionizing particle (ions, electrons, photons) striking on the active memory module boards, leading to the identification of the error and consequent single correction as a SE by the MC FPGA.

3.4.1. Cumulative SEU over time

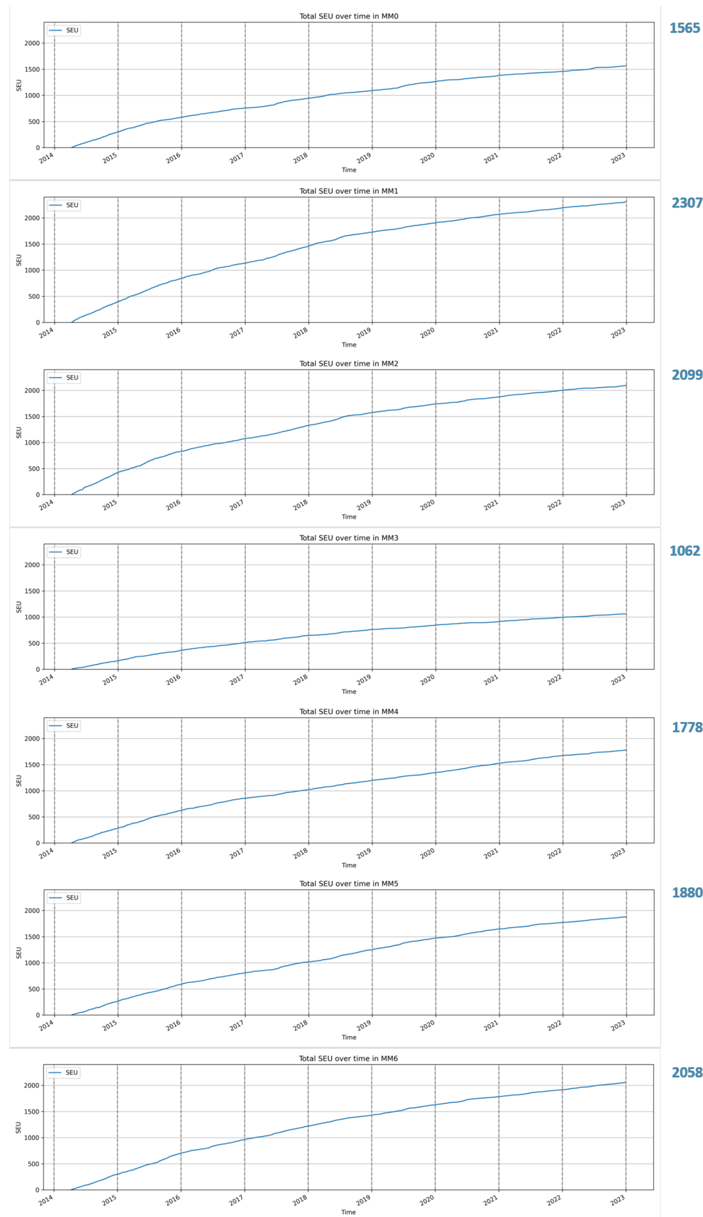

Figure 3.38: Cumulative SEU over all memory modules boards

Figure 3.38 shows the cumulative number of total SEUs occurred over time per MM board, but it shall be read with attention: this representation gives us only a partial view of SEU phenomenon, since starting from the third/fourth year in orbit, the phenomenology of EWCs takes over in occupying the 128 available entries that is the basis of the TM under analysis (see Chapter 2.1) reducing capability to log SEU locations in 128 entries available to log each single corrections. In this way, looking only at TM(6,6) data, after the fourth year the SEU number is surely under-estimated. Taking into consideration

only the first 3 years only, it can be seen that the growth in all memory modules of this phenomenon follows the same trend, except for the middle one (MM3, the most shielded of the entire array of PCBs), which is affected by half of the SEU effects with respect to the other memory module boards.

In Figure 3.39 the number of SEUs found within all TM(6,6) acquisitions sent over time is reported. In particular:

- **blue**: number of SEUs contained in one single TM(6,6) acquisition;
- **orange**: centered moving average over one week (14 TM(6,6) aquisitions);
- **green**: centered moving average over one month (62 TM(6,6) acquisitions).

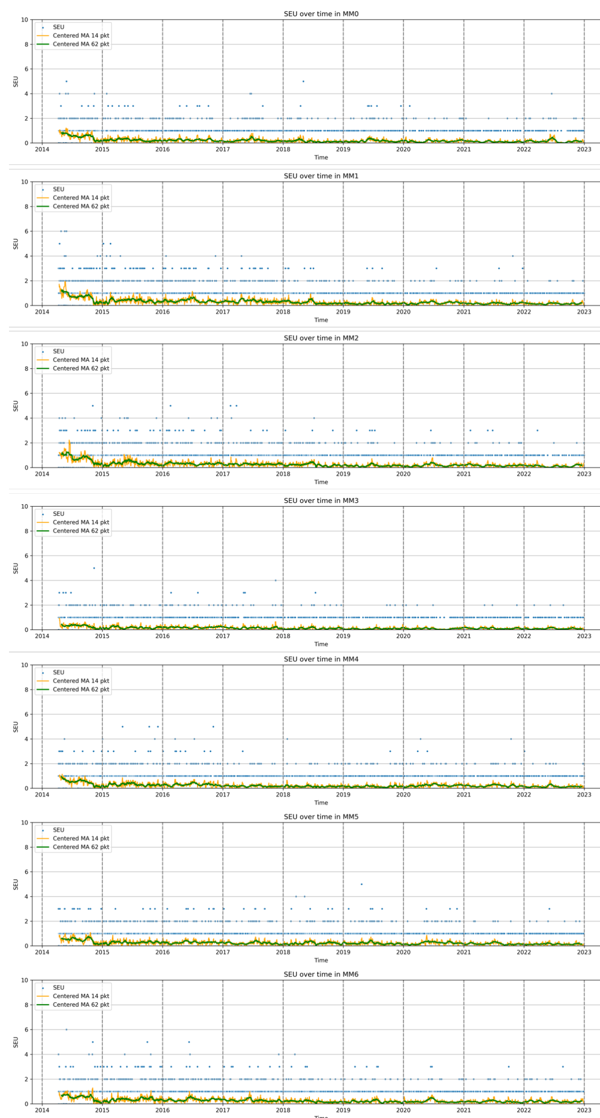

Figure 3.39: SEU occurrences over time in all memory modules boards

It is possible to see that in the first 3 years, when the information contained in the TM(6,6) packets is representative for this SEU pehenomenon, the average number of SEUs that hit all memory modules is someway decreasing and it is slightly higher than in subsequent years where its value has remained roughly constant.
This trend can be compared with the eleven-year activity cycle of the Sun shown in Figure 3.40.

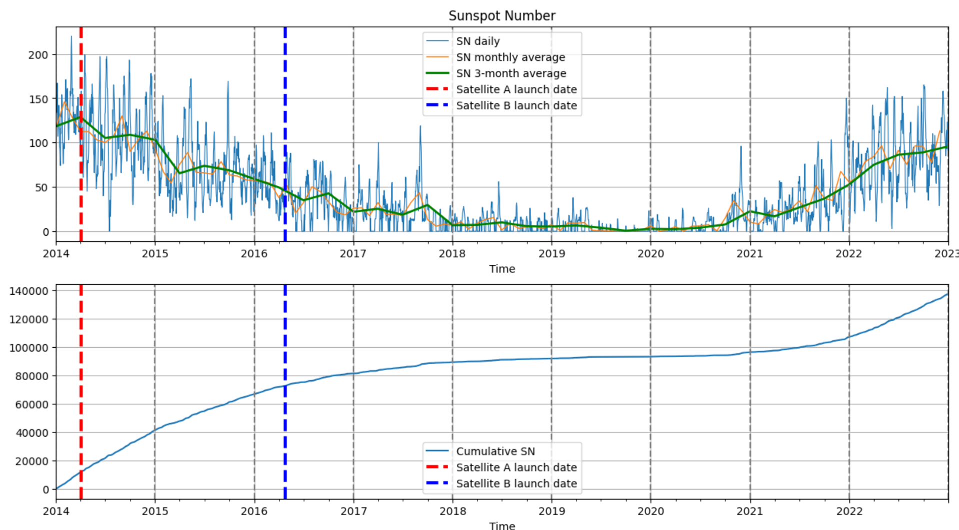

Figure 3.40: Absolute and cumulative Sunspot number over Satellite A time window (Sunspot data from the World Data Center SILSO, Royal Observatory of Belgium, Brussels [4])

The number of dark spots on the Sun surface is associated with higher magnetic activity and so to higher solar wind spread in the solar system. The Sun's solar wind interacts with Earth's magnetic field and its ionosphere is "compressed" by it on the side facing the Sun and is stretched out on the side away. The charged particles ejected by the Sun in the solar wind are guided into the ionosphere along magnetic field lines.
Satellite A was launched in the peak of solar activity in 2014, during Solar Cycle 24 and in its early years in orbit, the particles coming from the Sun and trapped by the Earth's magnetic field in Van Allen inner belt were most likely in decreasing trend. This decreasing solar activity could explain the decreasing SEU hits visible in these first 3 years of Satellite A SSMM.
The high values of the SEU hits observed especially in the outer memory module boards of the SSMM in the early years in orbit contributes to validate this hypothesis.
For the later years considered in this thesis (2021-2022) for Satellite A, the effect of increased occurrences of SEUs expected since the new Solar Cycle 25 started, is not

visible: this is an "artifact" in the data that can be easily explained with the fact that the "space" available to log them in the 128 entries structure is reduced by the predominance of EWCs logging progressively formed by radiation root-cause over the years.

3.4.2. SEU ICs/TSOPs Geometrical Distribution

In Figures 3.41 and 3.42 the distribution per IC/cubes and TSOP levels respectively is reported. A much more homogeneous distribution w.r.t. EWC phenomenology is visible on both faces of all memory modules boards. Comparing these with the graphs shown in the previous chapters related to the distribution of EWCs, as expected for SEU no relationship with the profile temperatures over the memory module is found, only the inner MM board on both faces appear more "protected" by SEU. This is a clear difference between the two phenomena distribution in the SSMM: the EWC associated with cells weakeing and the SEU associated with istantaneous radiative effect.

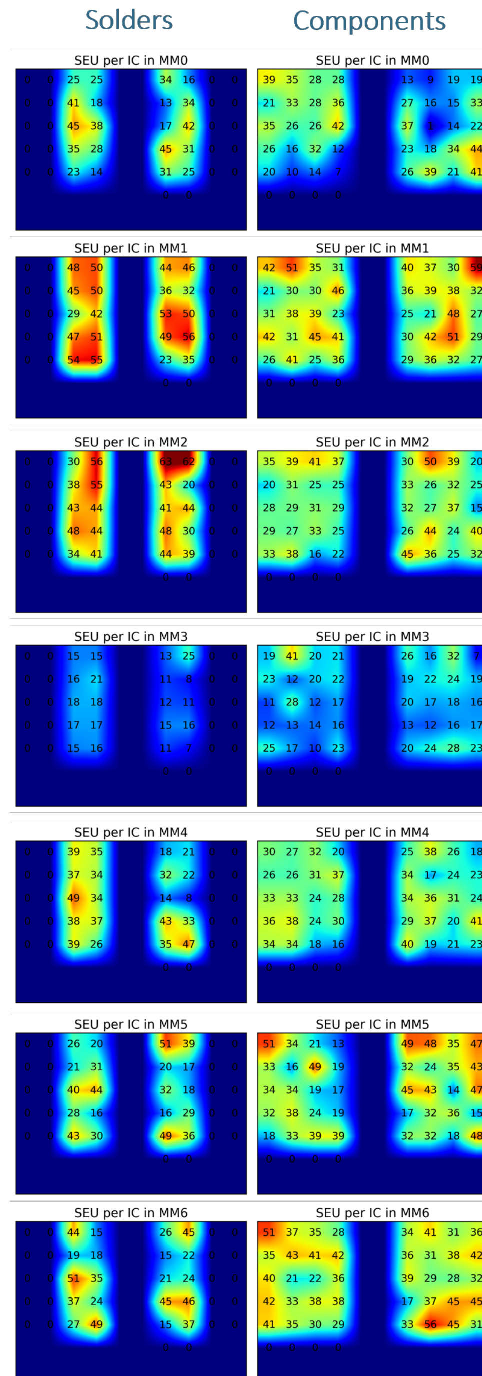

Figure 3.41: SEU distribution per IC in all memory modules (MAX_SEU_per_IC= 63 on MM2)

Also the distribution of SEUs by TSOP level shows a uniform distribution across ICs/cubes layers: this observation further reinforces the radiative, and thus random, origin of this phenomenon.

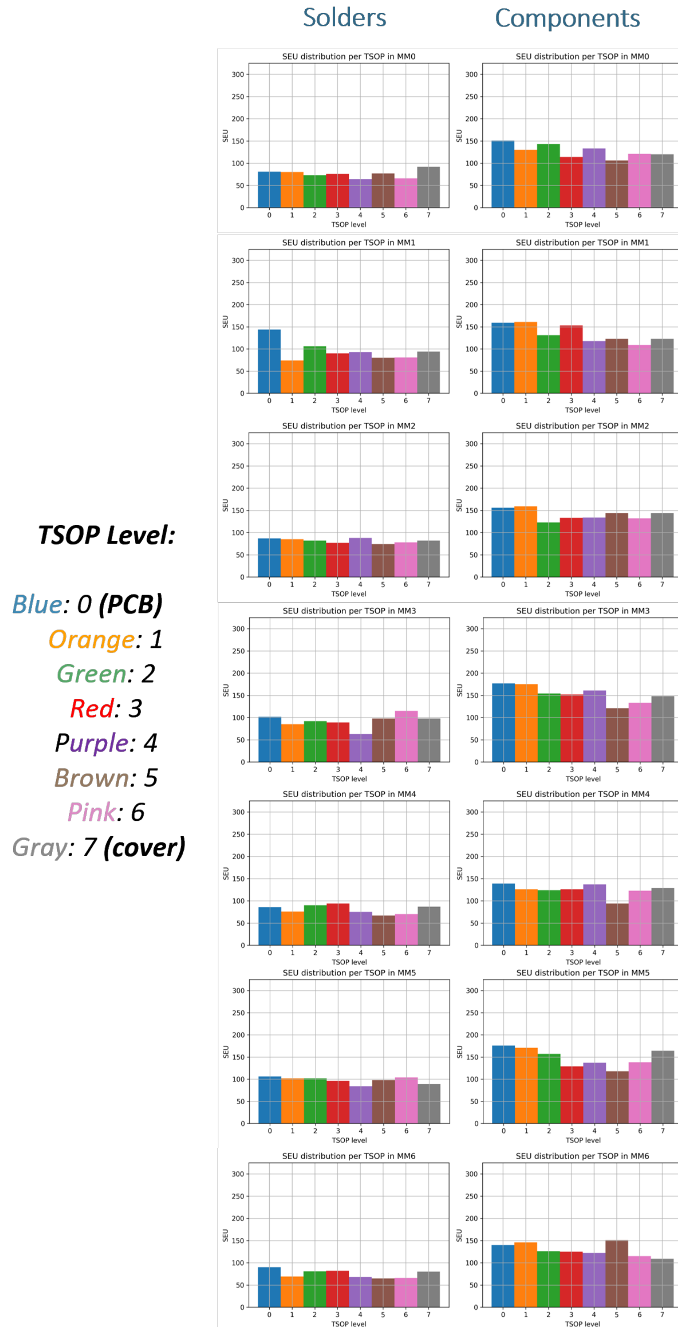

Figure 3.42: SEU distribution per TSOP level in both side of all memory modules

In Figure 3.43 it is possible to identify TSOP levels within individual ICs/cubes that have been affected by SEUs over all years in orbit. There appears to be no bias between preferences in TSOP levels affected by more SEUs over all ICs/cubes as already seen in Figure 3.41 and 3.42. Even more evident in this graph is the isotropy of SEUs on both sides of each MM boards with the relative differences among the PCBs, the more shielded central memory module is less affected by this phenomenon.

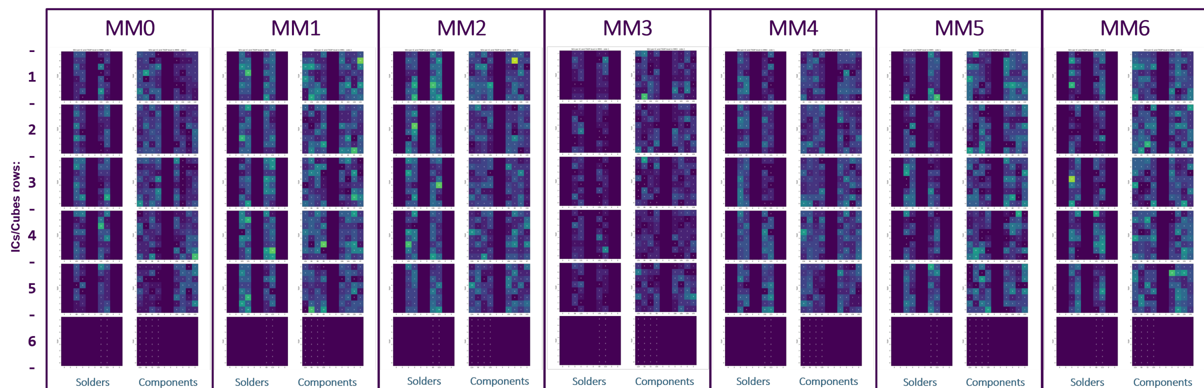

Figure 3.43: SEU distribution per ICs and TSOP levels in both side of all memory modules matrix

3.4.3. SEU ICs/TSOPs Geometrical Distribution (first 3 years)

As mentioned before, the first 3 years of data are the ones that can be considered reliable for SEU analysis. Figures 3.44 and 3.45 shows the occurrences of SEUs by IC/cube and by TSOP level respectively during only the first 3 years.
Their distribution across the ICs/cubes on both boards sides of each memory modules looks even more homogeneous, while the differences between the various MM boards are already evident from the very first years.

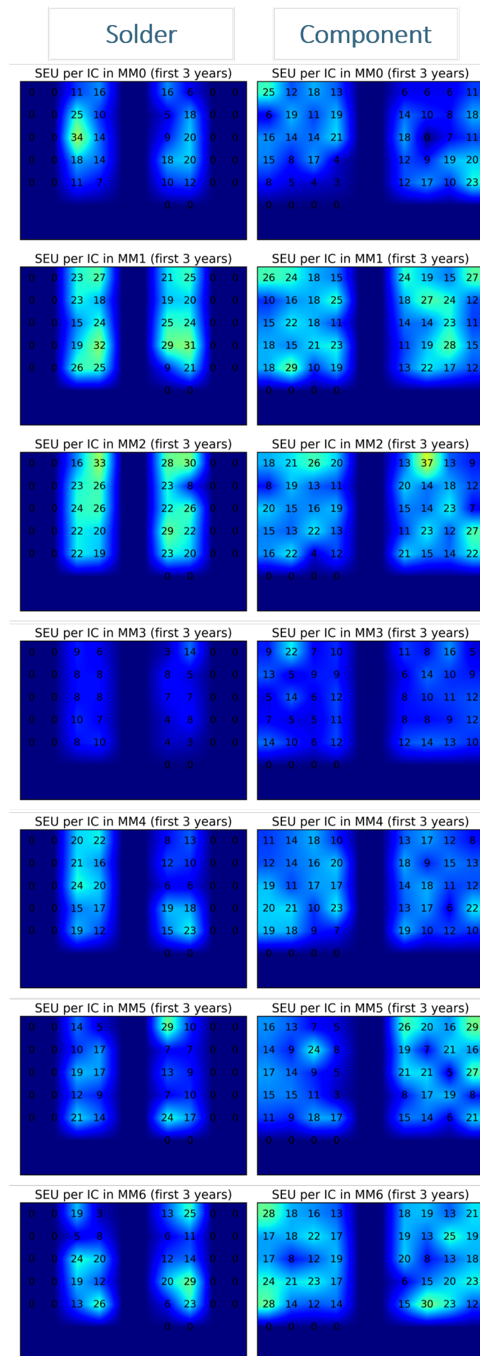

Figure 3.44: SEU distribution per IC in all memory modules in the first 3 years (MAX_SEU_per_IC= 34 on MM0)

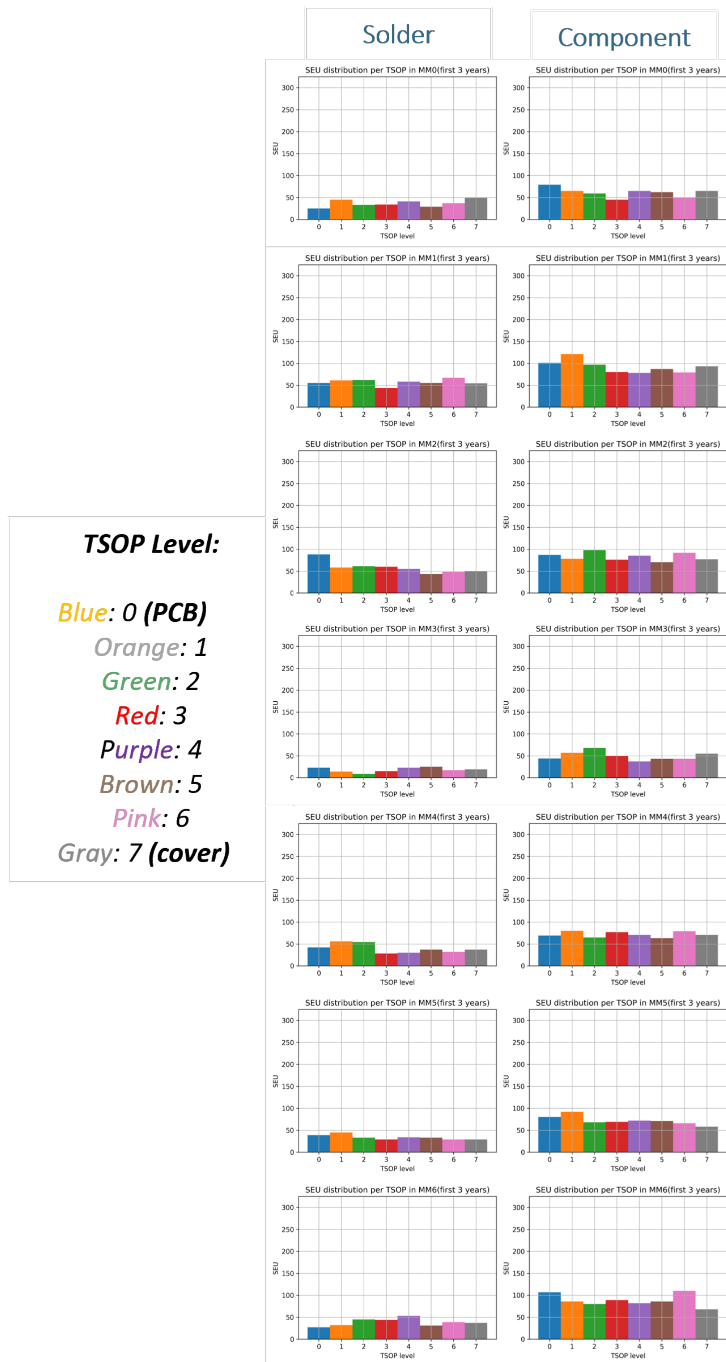

Figure 3.45: SEU distribution per TSOP level in both side of all memory modules in the first 3 years

3.5. SBC Analysis

The SBC is an intermediate class that groups all corrections associated with single addresses that appeared only once along the 9 years period and with CE counter variation

between 2 and 500 w.r.t. "previous entry" in the 128 entries logging area. This range of values was chosen empirically using what was discovered about BOS phenomenon in TN of 2014 (Chapter 1.3.1) and 2018 (Chapter 1.3.2), both by conducting several tests to see which value best separated the SEU-like radiative phenomenon from the class of BOS characterised by a round correction.
The final confirmation of the goddness of this threshold (500) is obtained by analyzing the variation of the CE counter get from the other source TM(3,25) (reporting each 1 s the MMx_CE parameters of all MM boards): it shows there are no peaks in CE values concentration up to a value of 1000 approximately. Therefore it was chosen a "safe" threshold of 500.

3.5.1. Cumulative SBC over time

Similarily to the previous chapter, the differences in SBC distribution among the various memory modules typical of EWCs (i.e. cooler modules less affected), are not noticed here; in fact, now the module less affected by this SBC phenomenon is the inner one (MM3), like for SEUs. This module is also the most "protected" module in the entire SSMM SBC behavior is more similar to SEU.

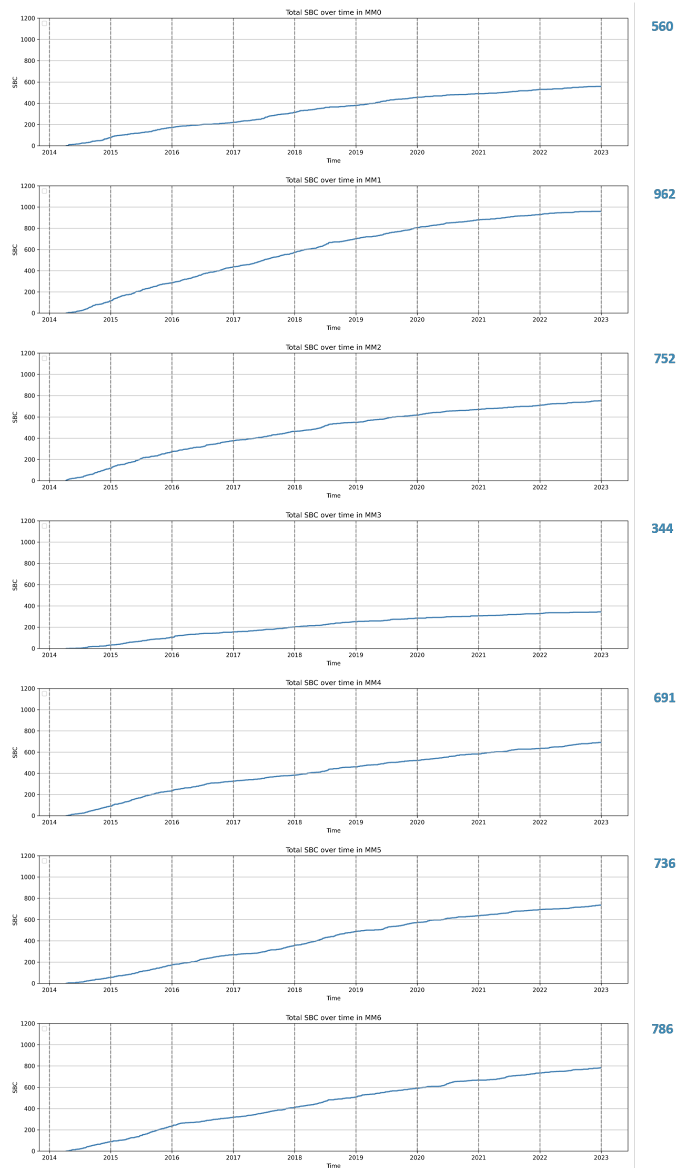

Figure 3.46: Cumulative SBC over all memory modules

3.5.2. SBC ICs/TSOPs Geometrical Distribution

In Figures 3.47 and 3.48 the distribution over 9 years per IC/cube and TSOP level is reported. Their arrangement deeply echoes that one of SEU: there is no relationship with temperature between different modules (refer also to Figure 3.62 at the end of this chapter, where the total number of SEUs, SBCs and BOS per memory module boards is compared together).

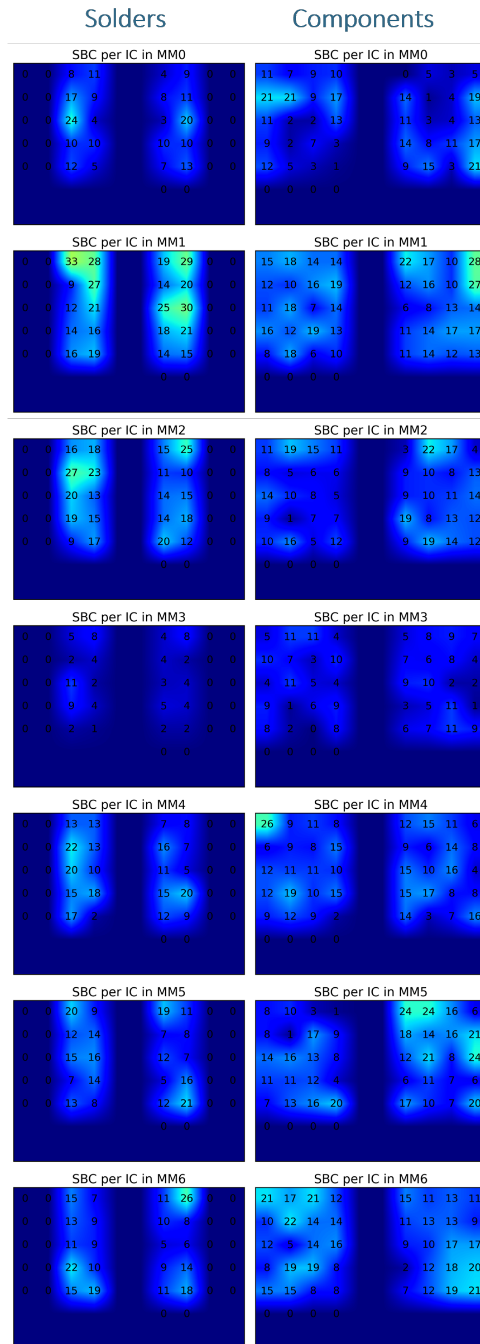

Figure 3.47: SBC distribution per IC in all memory modules (MAX_SBC_per_IC= 33)

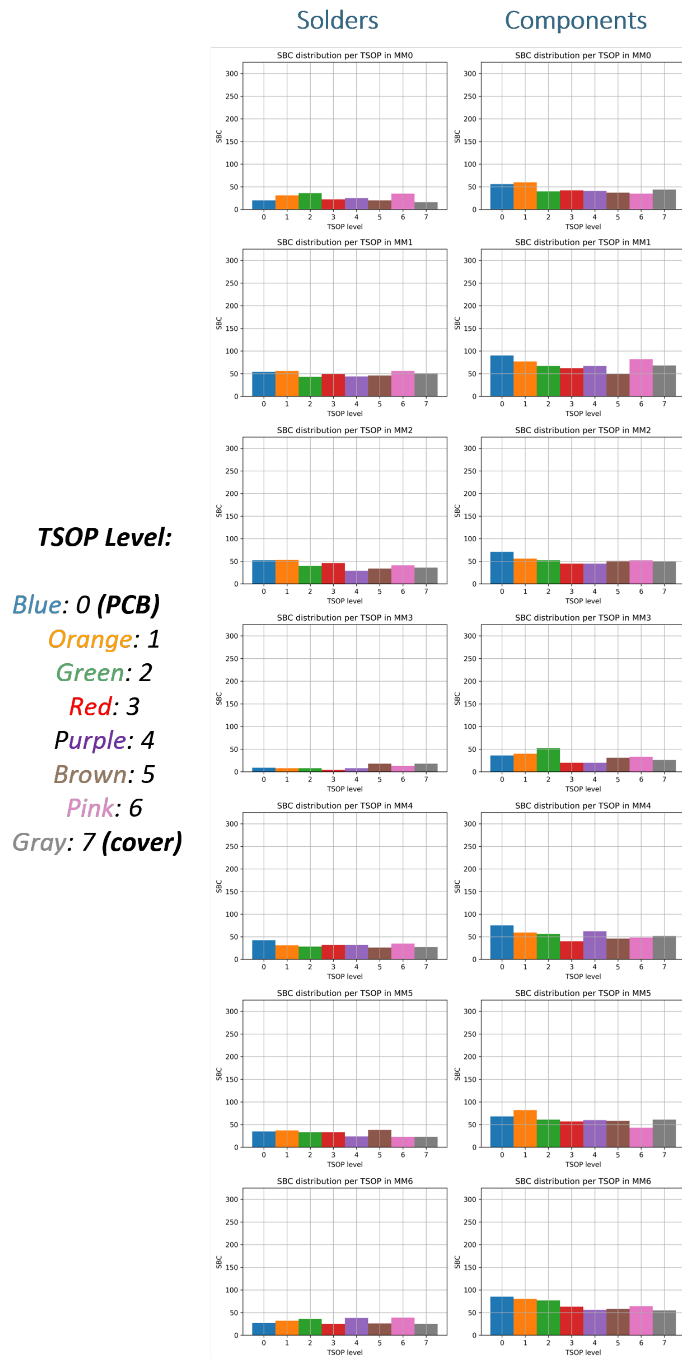

Figure 3.48: SBC distribution per TSOP level in both side of all memory modules

All these SBC similarities with SEUs suggest that these two phenomena are generated by a common typology of particle hits.

3.5.3. SBC ICs/TSOPs Geometrical Distribution (first 3 years)

SBC distribution across the IC/cubes on both boards sides of each memory modules after only 3 years (i.e. again considering only reliable data) shows a distribution similar to the SEUs with the inner memory module board (MM3) less affected.

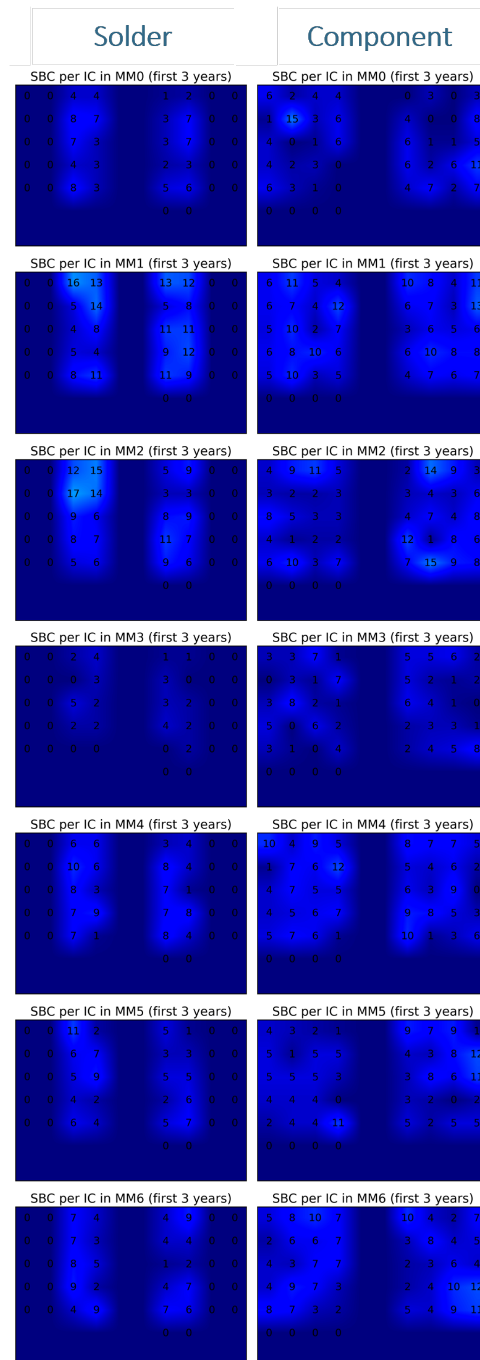

Figure 3.49: SBC distribution per IC in all memory modules in the first 3 years (MAX_SBC_per_IC= 17 on MM2)

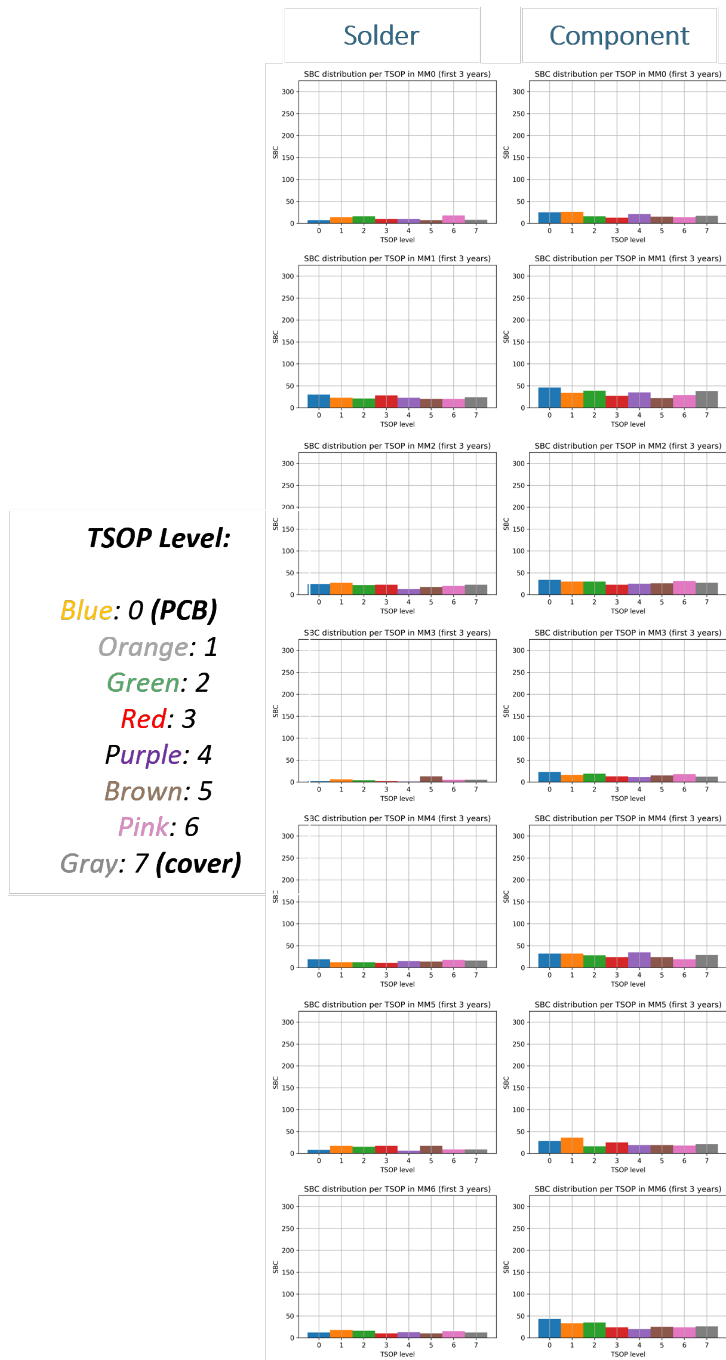

Figure 3.50: SBC distribution per TSOP level in both side of all memory modules in the first 3 years

3.6. BOS Analysis

As already introduced in Chapter 2.1.1, present section focuses on BOS census data. A BOS zone consists of a series of corrections, consecutive in time, characterized by a CE

counter variation greater than 500 all occurred at the same TSOP level within the same IC/cube.
In order to study in detail the occurrence and localization of this BOS phenomenon, only the TM(6,6) data is used and not the information in TM(3,25) that does not contain their exact address. Again, only the data of the first 3/4 years can be considered statistically analysable and representative: after 2018 the usual EWC phenomenon prevails in occuping the 128 entries structure (and so making BOS phenomenon less observable).

It was already shown in TAS-I TNs in 2014 and 2018 that the frequency of occurrence of these phenomenon is similar to the SEFI rate obtained from Radiation Analisis. The SEFI rate under solar minimum conditions is roughly 1 SEFI per day on the entire active SSMM array, so about one SEFI per MM board per week.

Now, using the cumulative data of the first 3 years only, the following values of the total and weekly number of BOS per memory module are reported in the following table:

	MM0	**MM1**	**MM2**	**MM3**	**MM4**	**MM5**	**MM6**
total	159	193	165	160	134	172	200
weekly	1.02	1.24	1.05	1.02	0.86	1.10	1.29

Table 3.1: Total and average number of BOS per week per MM board taking into account only the first 3 years

The analysis on all BOS occurrences per MM board statistically resembles the SEFI rate estimated by Radiation Analysis over a large amount of data samples for the time period in which the BOS pheniomenon is highly logged in 128 entries structure. Instead, considering the data from the whole period of 9 years, the BOS rate "appears" halved in all memory modules while from the TM(3,25) occurrence their occurrence per MM board is practically unvaried across 9 years (this is a further confirmation that information in BOS inside TM(6,6) data is reliable only for first 3-4 years).

3.6.1. BOS occurrences over time

The graph in the Figure 3.51 shows on the vertical axis the observed correction "extension" $k * 2048$ (CE counter variation) related to BOS zones as a function of time. The color is related to the level of TSOPs affected by the BOS, and there is no TSOP 0..7 level particularly affected w.r.t. the others. In detail, their distributions along the TSOP levels

divided by memory module boards are shown in Figure 3.55.

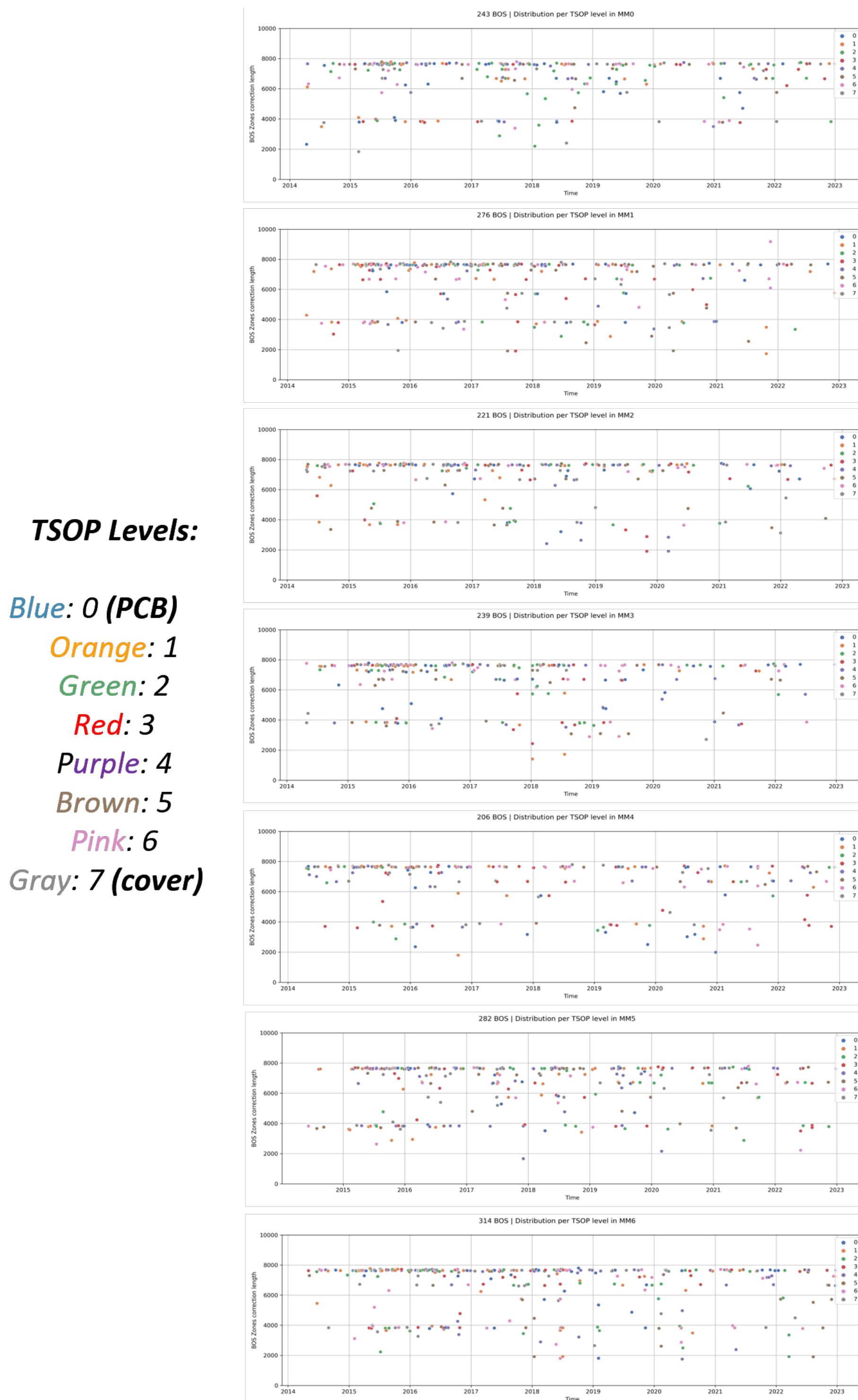

Figure 3.51: Distribution of BOS zones correction "extension" over time per memory module

With reference Figure 3.51 and in particular in Figure 3.57, some "clusters" of extension

can be identified in the surroundings of $k * 2048$ corrections with k = 1,2,3,4 along the years. A prevalence of k = 4 (approximately) and k = 2 (slightly less) is visible. From Chapter 1.2, it is recalled that 2048 bytes is the size of the internal "page" of all TSOP SDRAM devices inside the SSMM memory array. Therefore such BOS seems to affect "pages" in the internal organisation of TSOP.

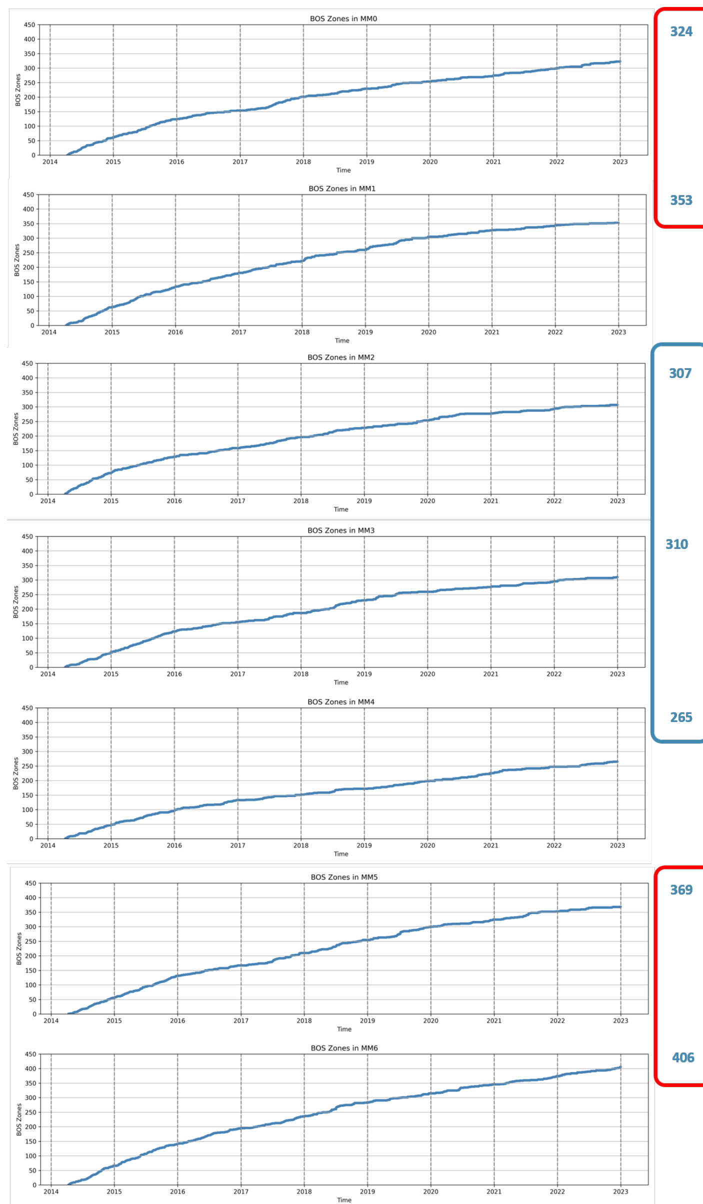

Figure 3.52: Cumulative number of BOS zones over time in all memory modules

Figure 3.52 shows that the BOS number and trend in time has no correlation with the TRP oscillation of the SSMM, which further suggests a pure istantaneous and radiative origin of this phenomenon without any temperature lever triggering considering that in the 2014

TAS-I TN summarized in Chapter 1.3.1, a correlation between this BOS phenomenon occurrence and the Satellite A crossing of the SAA was qualitatively demostated. The SSA is an area where Earth's inner Van Allen radiation belt comes closest to Earth's surface leading to an increased flux of energetic particles in this region and exposing SCs to higher levels of ionizing radiation.

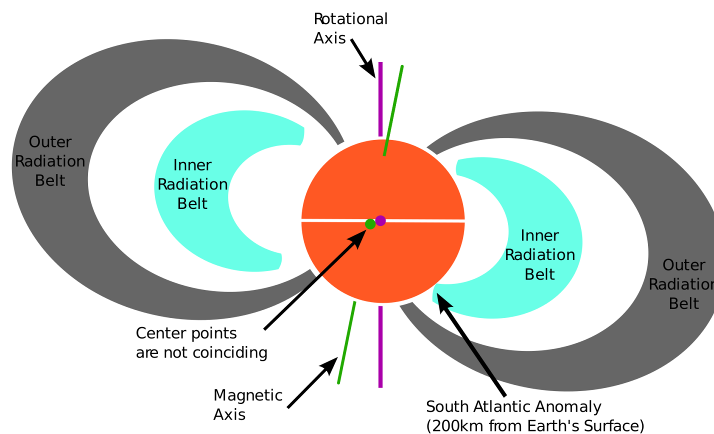

Figure 3.53: A cross-sectional view of the Van Allen Radiation Belts, noting the position of the South Atlantic Anomaly [5]

Detailed analysis of BOS occurrence w.r.t. satellite orbital position and SAA crossing could be object of future works.

3.6.2. BOS ICs/TSOPs Geometrical Distribution

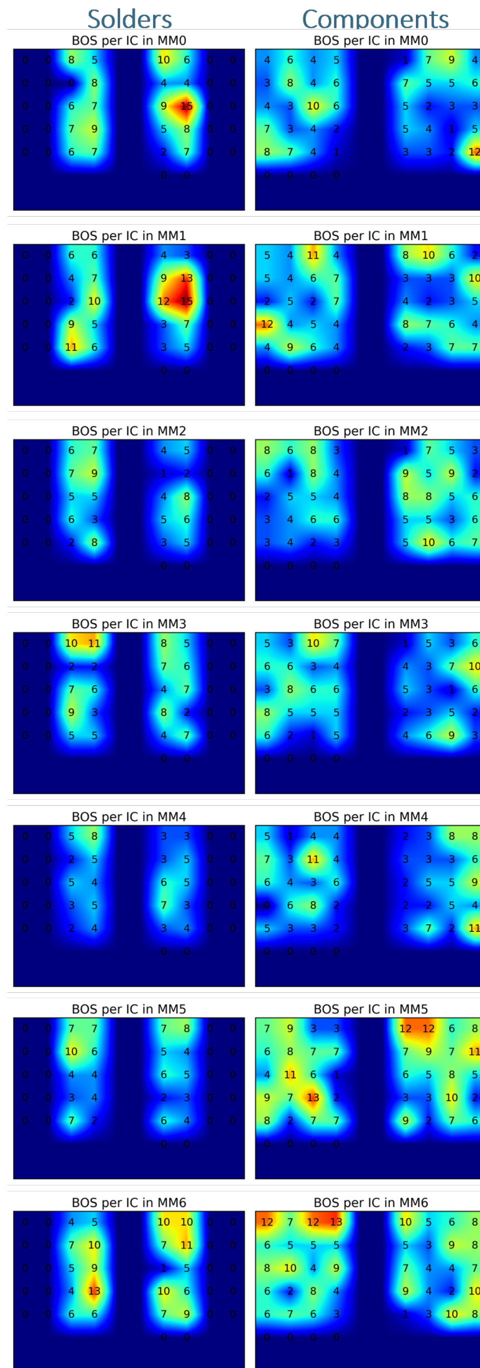

Figure 3.54: BOS zones distribution per IC in all memory modules (MAX_BOS_per_IC= 15 on MM0 and MM1)

The distribution per IC/cube of the BOS over all memory module boards shows that, as per SEU and SBC, the distribution is isotropic and independent by the temperature of

the MM boards and between the two faces of an MM board.

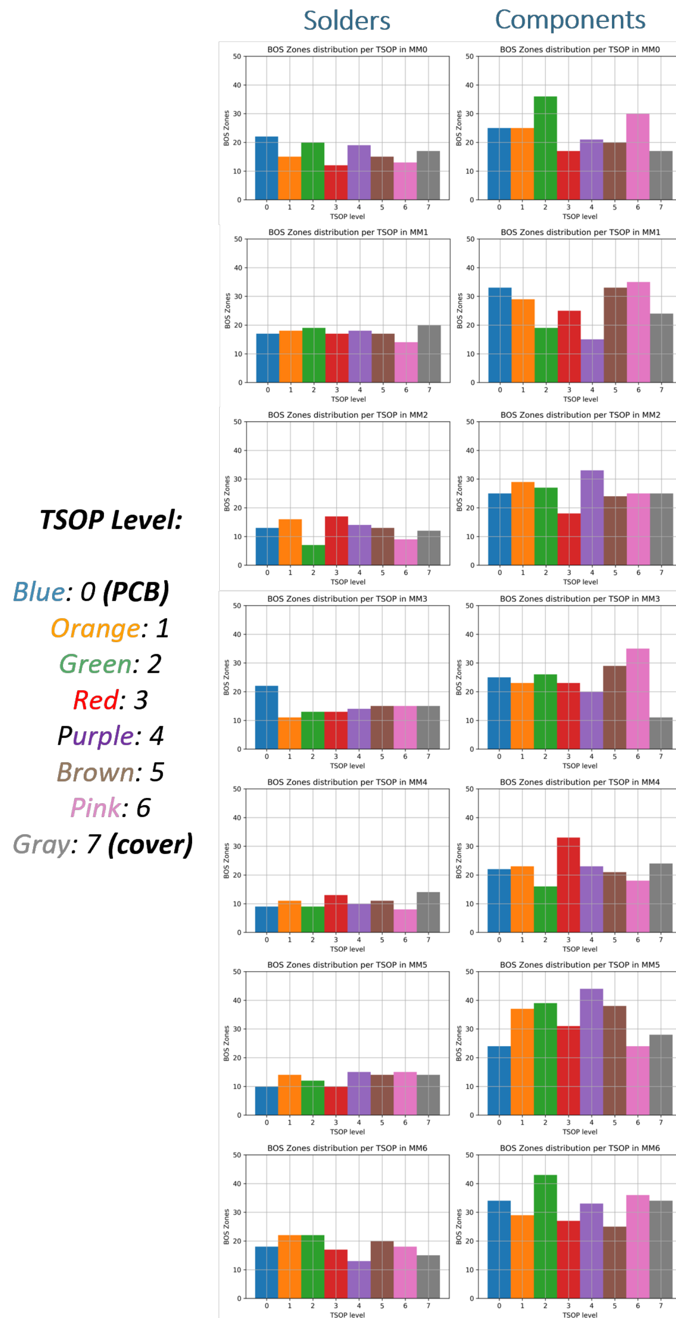

Figure 3.55: BOS zones distribution per TSOP level in all memory modules

From Figure 3.55, to corroborate the radiative origin, the BOS zones drawn from TM(6,6) acquisitions are still statistically slightly more distributed on the outer MM boards.

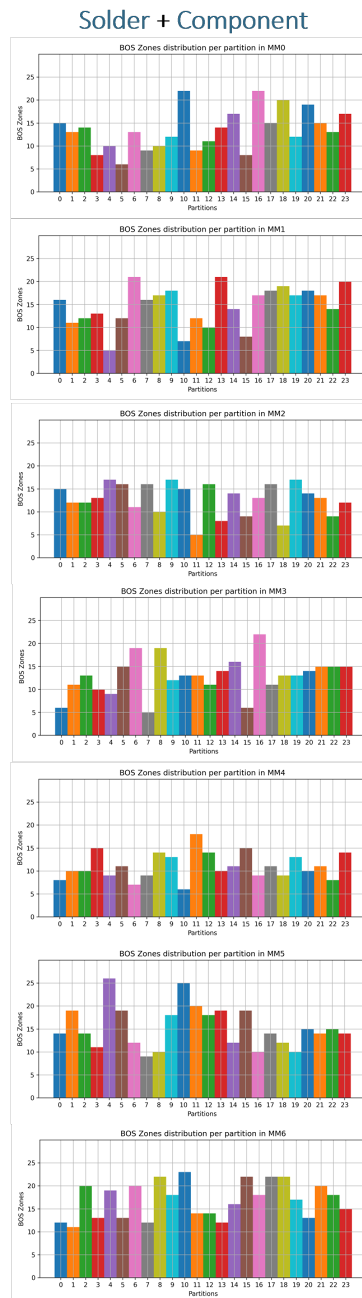

Figure 3.56: BOS zones distribution per partition in all memory modules

3.6.3. BOS characteristics

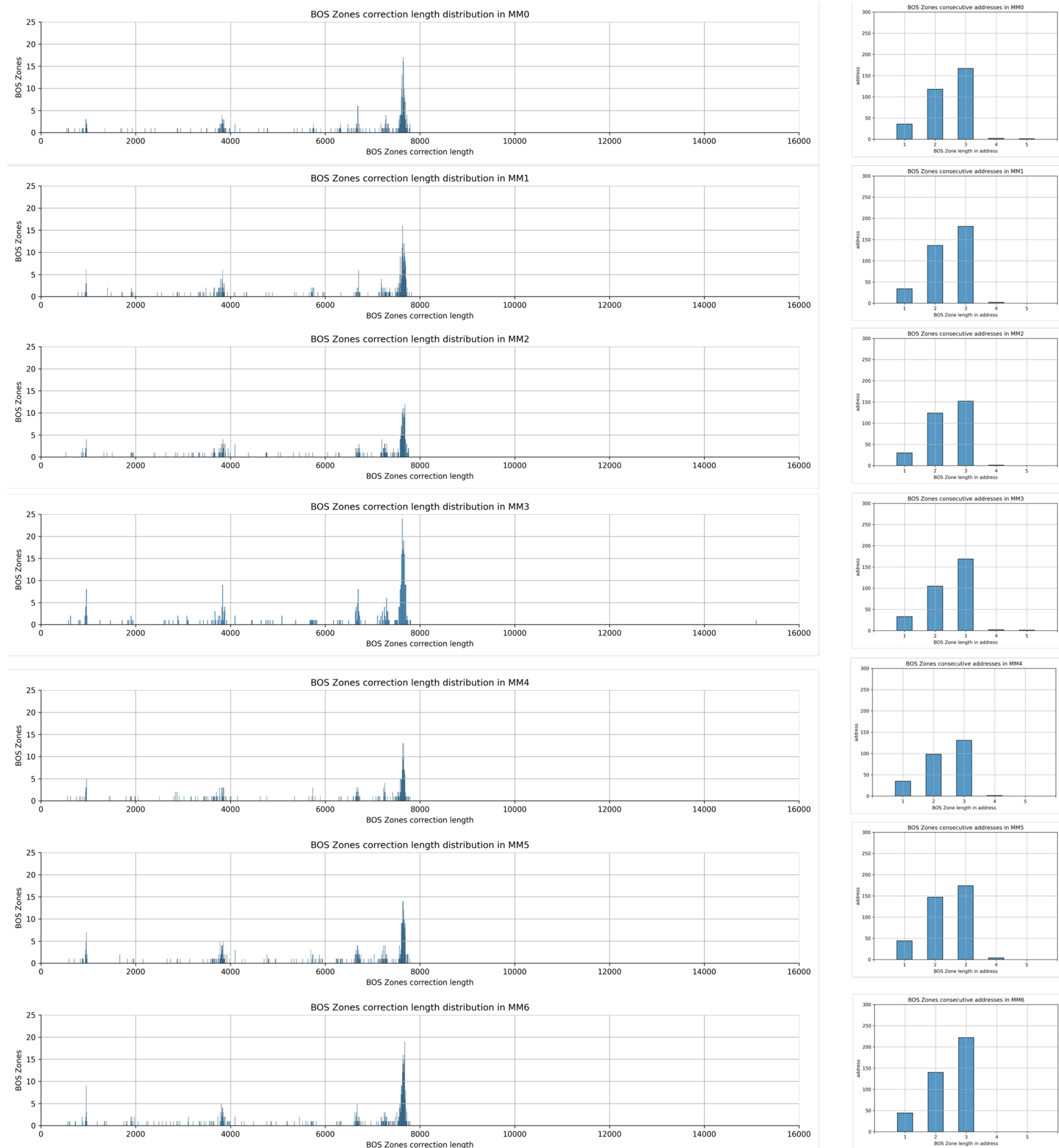

Figure 3.57: BOS zones correction length distribution and address length distribution in all memory modules

Figure 3.57 show how these "clusters" of BOS corrections are statistically centered on homologous "lenght ranges" across all MM boards. The most frequent "cluster" consists of three peaks, with the maximum one around 7650 corrections, over all MM boards.

In addition, there are no "clusters" below 1000 corrections: which is why the 500 value is chosen as the threshold to distinguish SBC vs. BOS.

Using the addresses bounding the beginning and end of BOS zones in the TSOPs, it is possible to check whether the occurrence of leakage (EWCs) or radiative istantaneous phenomena (SEUs and SBCs), were correlated with these BOS events.
Figure 3.58 reports the percentages of the various phenomena (EWC, SEU, SBC) appearing within an area found affected by BOS.
From the obtained values obtained, the absence of correlation between these classes can be deduced, meaning in particular that EWCs and SBCs are not a consequence of BOSs.

3.7. Statistics & Summary for SSMM on Satellite A

In the following tables, the cumulative number of all types of phenomena over 9 years are reported. The number of phenomena appeared inside a BOS zone are obtained verifying that the address affected by leakage or radiation is in the same IC/Cube and TSOP level as the BOS and that the address is "between" the extreme addresses of the BOS zone.

There appears to be no correlation between the appearance of EWCs with areas affected by SEU or BOS.

Satellite A	S-S EWC	M-S EWC	SEU	SBC	BOS Zones	Hard Error	Partition Parking (HE not recovered by a column power cycle)	S-S EWC found in BOS Zones (before and after in time)		M-S EWC found in BOS Zones (before and after in time)		SEU found in BOS Zones (before and after in time)		SBC found in BOS Zones (before and after in time)	
MM0	887	233	1565	560	324	76	10	15	(1.7 %)	7	(3.0 %)	26	(1.7 %)	21	(3.8 %)
MM1	990	267	2307	962	353	15	6	18	(1.8 %)	2	(0.7 %)	42	(1.8 %)	17	(1.8 %)
MM2	1006	279	2099	752	307	14	0	12	(1.2 %)	6	(2.2 %)	44	(2.1 %)	17	(2.3 %)
MM3	818	218	1062	344	310	15	3	6	(0.7 %)	5	(2.3 %)	20	(1.9 %)	17	(4.9 %)
MM4	898	222	1778	691	265	7	1	5	(0.6 %)	1	(0.5 %)	21	(1.2 %)	22	(3.2 %)
MM5	709	130	1880	736	369	15	2	9	(1.3 %)	3	(2.3 %)	40	(2.1 %)	21	(2.9 %)
MM6	727	147	2058	786	406	11	2	12	(1.7 %)	4	(2.7 %)	41	(2.0 %)	17	(2.2 %)
Average over all MM PCBs	862.14	213.71	1821.29	690.14	333.43	21.86	3.43	11.00	1.3 %	4.00	2.0 %	33.43	1.8 %	18.86	3.0 %
Total over all MM PCBs	6035.00	1496.00	12749.00	4831.00	2334.00	153.00	24.00	77.00		28.00		234.00		132.00	

Figure 3.58: Satellite A SSMM, summary table of all corrections types on all MM boards

From the table in Figure 3.59, the average number per ICs/cubes of the various radiative effects is reported, the highest values are mainly the outermost faces of all modules, solders side for MM0-MM1 and components side for MM5-MM6 (exception of BOS in the solders

side on MM6). The temperature-influenced leakage effects are instead more distributed on the components face ("hottest" side). MM0 and MM1 are close to the active nominal side of the whole SSMM and thus they have the solders side in an environment heated by other active PCBs, that raise their local temperature.

	Average number per IC/Cube				
	S-S EWC	M-S EWC	SEU	SBC	BOS Zones
MM0 Solders Side	15.90	4.20	29.00	10.25	6.65
MM0 Components Side	14.23	3.73	24.63	8.88	4.78
MM1 Solders Side	17.35	4.35	44.75	20.00	7.00
MM1 Components Side	16.08	4.50	35.30	14.05	5.33
MM2 Solders Side	16.25	4.40	43.35	16.55	5.05
MM2 Components Side	17.03	4.78	30.78	10.53	5.15
MM3 Solders Side	13.40	2.80	14.85	4.30	5.90
MM3 Components Side	13.75	4.05	19.13	6.45	4.80
MM4 Solders Side	14.70	3.15	32.05	12.65	4.25
MM4 Components Side	15.10	3.98	28.43	10.95	4.50
MM5 Solders Side	10.80	2.00	30.30	12.30	5.20
MM5 Components Side	12.33	2.25	31.85	12.25	6.63
MM6 Solders Side	9.95	2.20	30.75	12.40	7.25
MM6 Components Side	13.20	2.58	36.08	13.45	6.53

Figure 3.59: Satellite A SSMM, average number per IC/cube of all corrections types, divided per solders and components sides

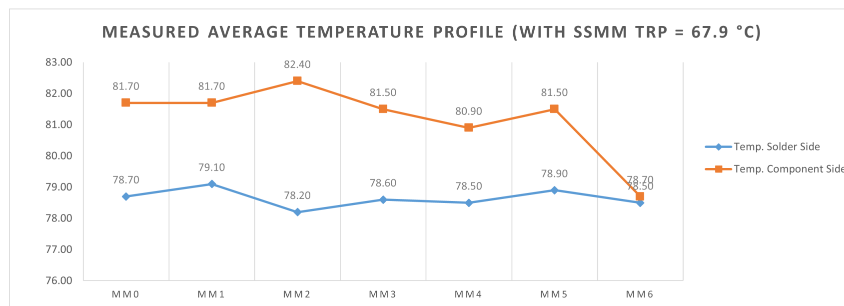

Figure 3.60: Satellite A SSMM MM boards steady state temperature profile

From Figure 3.60, it is evident how moving toward MM6 the temperature decreases on both memory module faces (especially components side).

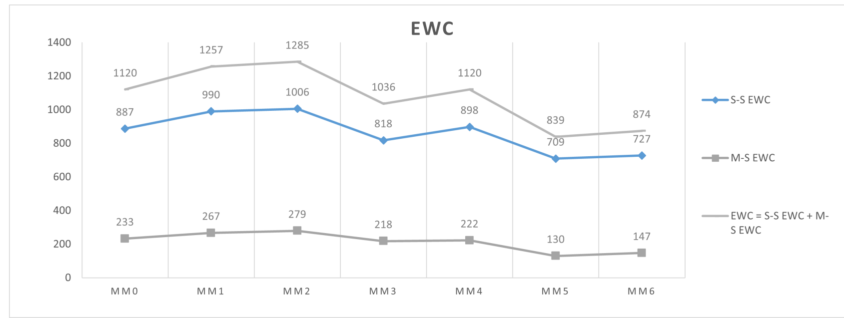

Figure 3.61: Satellite A SSMM, total EWCs over all MM boards

The number of EWCs per memory module follows the temperature profile quite well, higher temperature is related to higher number of EWCs. Temperature is not only involved in the activation of EWCs but it is also responsible for more proliferation.

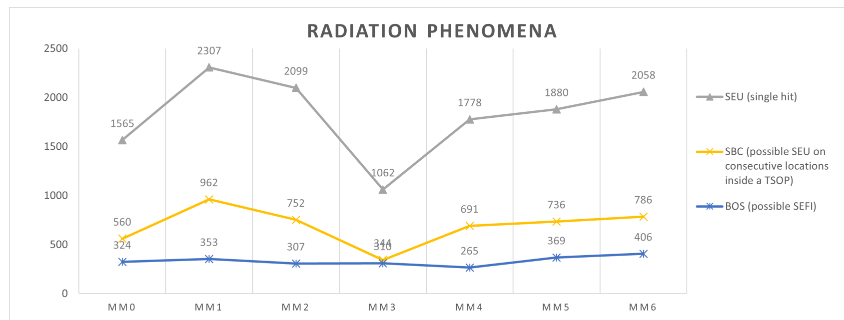

Figure 3.62: Satellite A SSMM, radiation phenomena in all MM boards

Comparing Figure 3.62 with Figure 3.61, one can see the different mechanisms of the two igniting phenomena: one influenced by temperature (see temperature profile in Figure 3.60) while the other one distributed evenly among the modules except for the more protected inner module.

Particularly noticeable is the similar behavior of SEUs and SBCs, both significantly reduced in the MM3 module and a very similar distribution between memory modules.

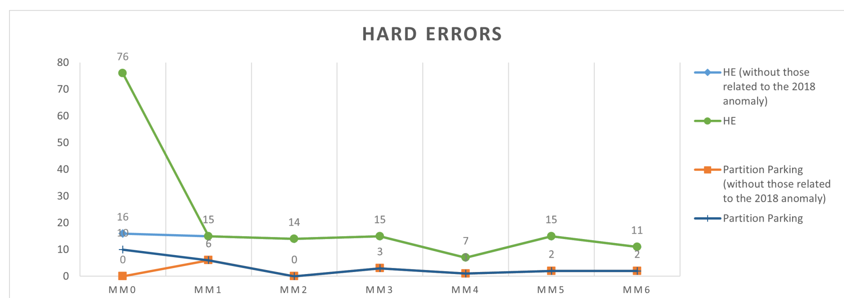

Figure 3.63: Satellite A SSMM, HEs over all MM boards

4 | Validation of results and comparison with Satellite B SSMM

This chapter presents the results obtained by performing the same analysis on all MM boards of a second SSMM equipment, twin to the previous one, embarked on board Satellite B.
Satellite B was launched two years later in the same orbital plane of Satellite A and, as we can see in Figure 3.40, in a different level of radiation environment: when the first one was launched, the Sun's eleven-years cycle was almost at its maximum level while the second one followed later, when the Sun Cycle 24 was in its decreasing phase.

In addition, few weeks after launch, due to another onboard failure on Satellite B SSMM, some of the redundant PCBs were switched on with corresponding switch off of the nominal ones, leading to a new distribution of active modules within that SSMM of the second SC. An indicative diagram of the new arrangement is shown in Figure 4.1.
This new configuration with its consequent internal temperature distribution profile was constantly kept during all mission of Satellite B.

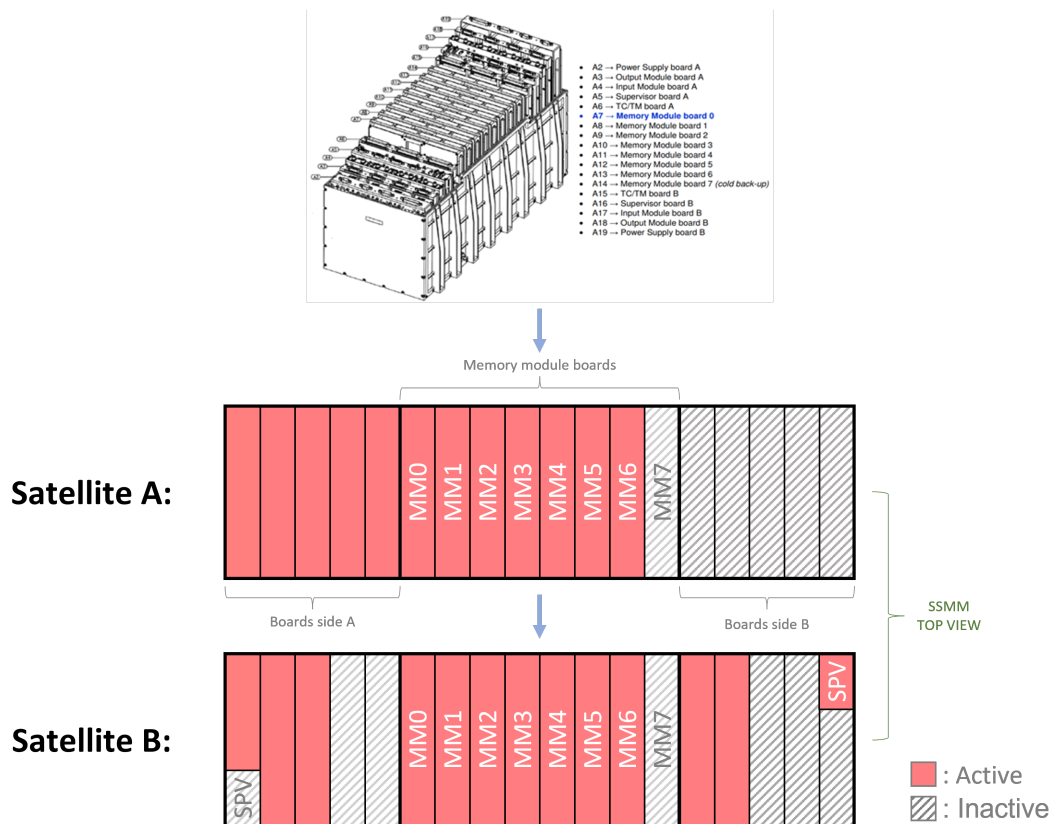

Figure 4.1: New arrangement of active modules of the SSMM onboard Satellite B a few weeks after launch

This new distribution of active modules led to a change in the local temperature profile across the SDRAM MM boards, certainly there was a local temperature increase in surroundings of MM6 and a temperature drop in the MM0 module.

The classification of observed error corrections remained the same as Satellite A and the following analysis of Satellite B data retraces the same steps as the one presented in the previous chapter: many comments and explenation text will not be repeated, but it will focus on highlighting the similarities and differences.

Note: data regarding the second SSMM equipment were processed up to December 2021, spanning on 5 years.

4.1. Single-Shot Extremely Weak Cell (S-S EWC) Analysis

4.1.1. S-S EWCs activation over time

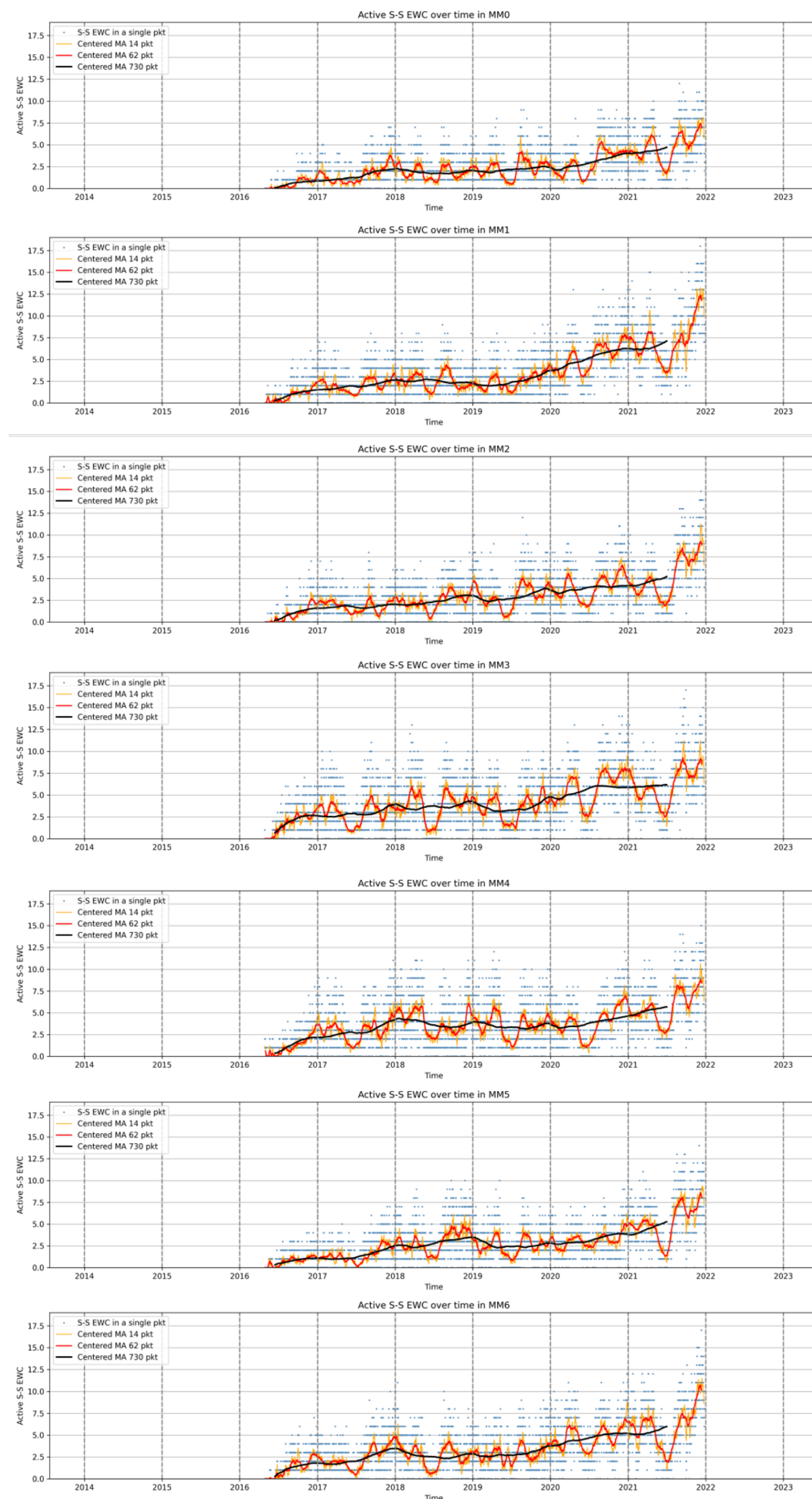

Figure 4.2: Activation of S-S EWC over time in all MM board, from MM0 to MM6

As in the previous analysis, Figure 4.2 shows the number of addresses classified as S-S EWC found active in each TM(6,6) packet acquisition over the Satellite B time frame.

As for the SSMM TRP of Satellite A, also the TRP of this second SSMM shows the typical seasonal oscillating profile pattern characterised by the mid-year central "orbital eclipses season".

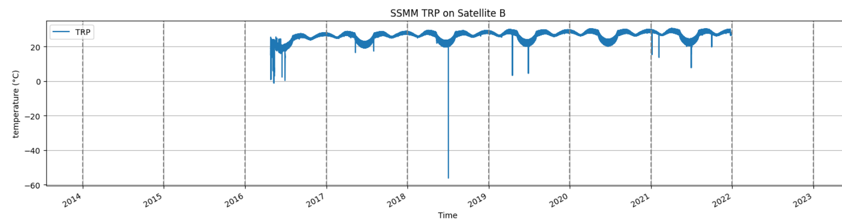

Figure 4.3: Satellite B SSMM TRP

A clear correlation between the activation waveform of S-S EWC and the SSMM TRP waveform of Satellite B became visible across the years and on all memory modules, starting to become well-correlated from the third year in orbit.

Compared with graphs in Chapter 3.1.1 referring to Satellite A, now the activation of this class of weak cells seems to never cancel out during the coldest periods from early May to early August, especially in the last few years.

4.1.2. Total certified number of S-S EWCs over time

As shown in the Figure 4.4, again the total number of S-S EWCs activated over the years in all active MM boards is lower in outer modules (MM5 and MM6). It is notable now the MM0 module where their number is lower than would be observed in MM0 of Satellite A w.r.t. its corresponding other MM boards. Nevertheless, also for this second SSMM the S-S EWC certified number increases progressively over time in a linear way, whether or not they appear active at sampling time over all MM boards.

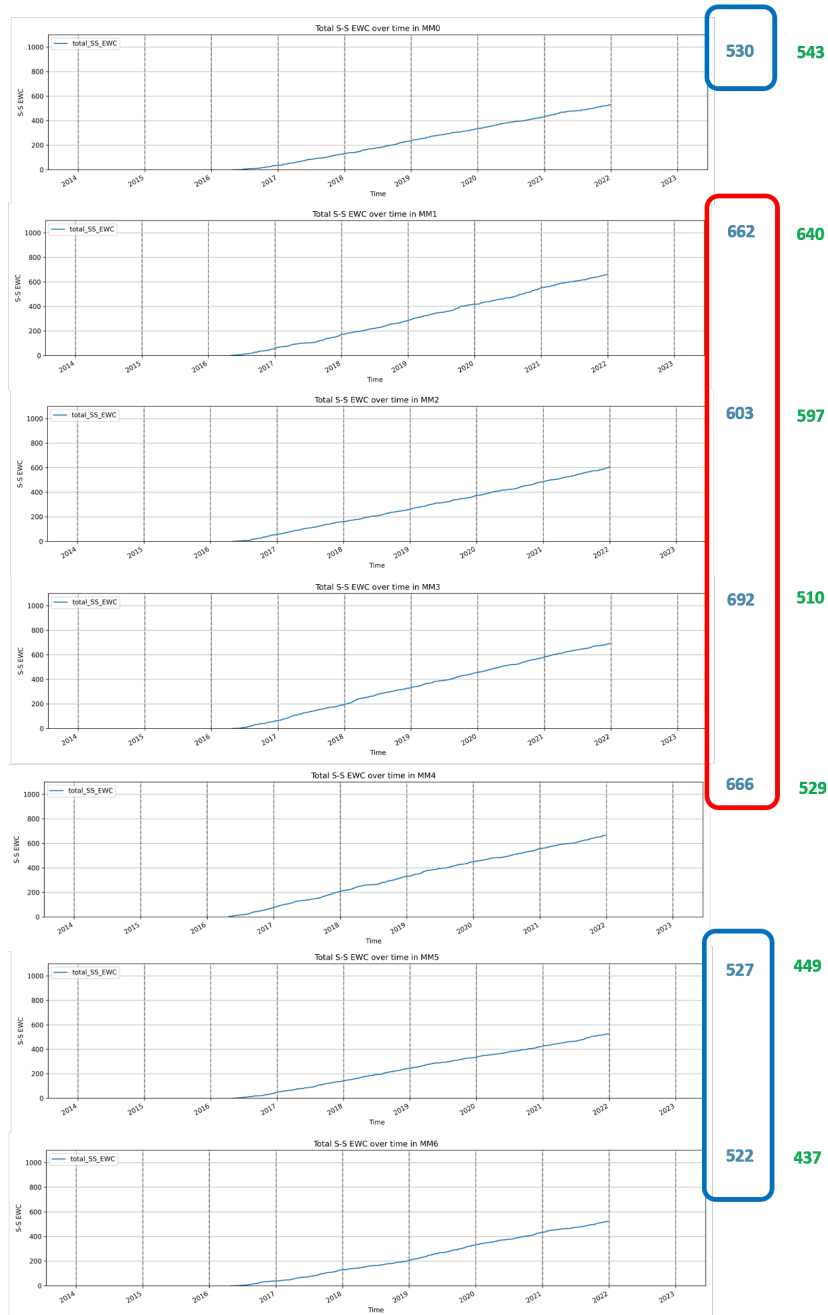

Figure 4.4: Total certified number of S-S EWC over time in all MM boards

Green numbers are the total certified S-S EWC on Satellite A SSMM equipment after the same amount of time (roughly 5 years) spent in orbit: after this "common age" in orbit of the two SSMM equipments, the S-S EWC absolute values is quite similar and the clustering effect (outer MM5 and MM6 with less absolute number of cells w.r.t. other MM boards) is again visible.

Only a slight difference in absolute number of MM0 w.r.t. MM1-MM4 in their cluster and of MM5,MM6 w.r.t. same boards in Satellite A SMMM are visible. The root cause could be the different "colder" local environment of MM0 and "warmer" one for MM5 and MM6 due to the configuration of SSMM, as previously highlighted.

4.1.3. S-S EWCs ICs/TSOPs Geometrical Distribution

The ICs/cubes distribution on both sides of each SSMM PCB of Satellite B are exactly the same as those shown in Figure 3.5 referred to SSMM of Satellite A.
From a geometric/positional point of view, it can be seen from Figure 4.5 that a greater proliferation of absolute number of S-S EWC on the components faces in present on all MM boards, similarly to Satellite A.
In addition, it is observed a slightly greater concentration of S-S EWCs in the central active memory modules (MM1..MM4). Again, the thermal configuration of this second SSMM could be the root cause.

A particular exception occurred in an IC/cube (IC121) on the solders side of the second memory module (MM1) showing clearly an anomalous peak in S-S EWC number: a more detailed discussion of this phenomenon will be given in next sections.

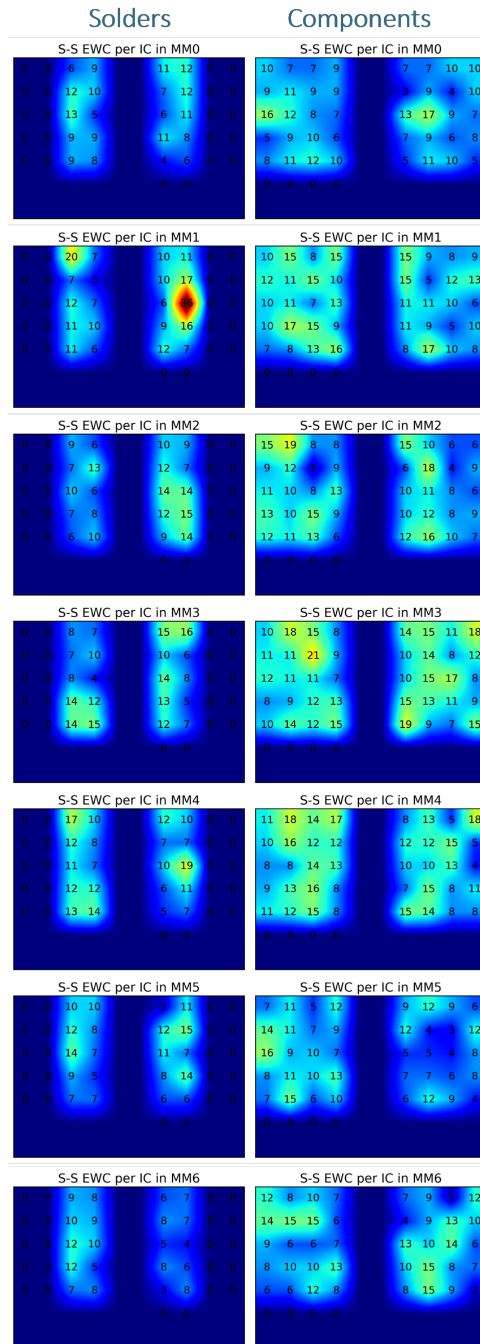

Figure 4.5: S-S EWC distribution (single addresses, without taking into account their occurrences), per IC/cube, across all memory modules (MAX_S-S_EWC_per_IC = 36 on MM1 on the critical cube/TSOP)

Histograms in Figures 4.6, 4.7, 4.8, 4.9 show the distribution of the S-S EWC per TSOP levels, so considering the logical partitions and columns. As previously mentioned, the external MM PCBs turn out to be less affected by this leakage phenomenon and there is no preferential distribution along columns or TSOPs/partitions for S-S EWC proliferation.

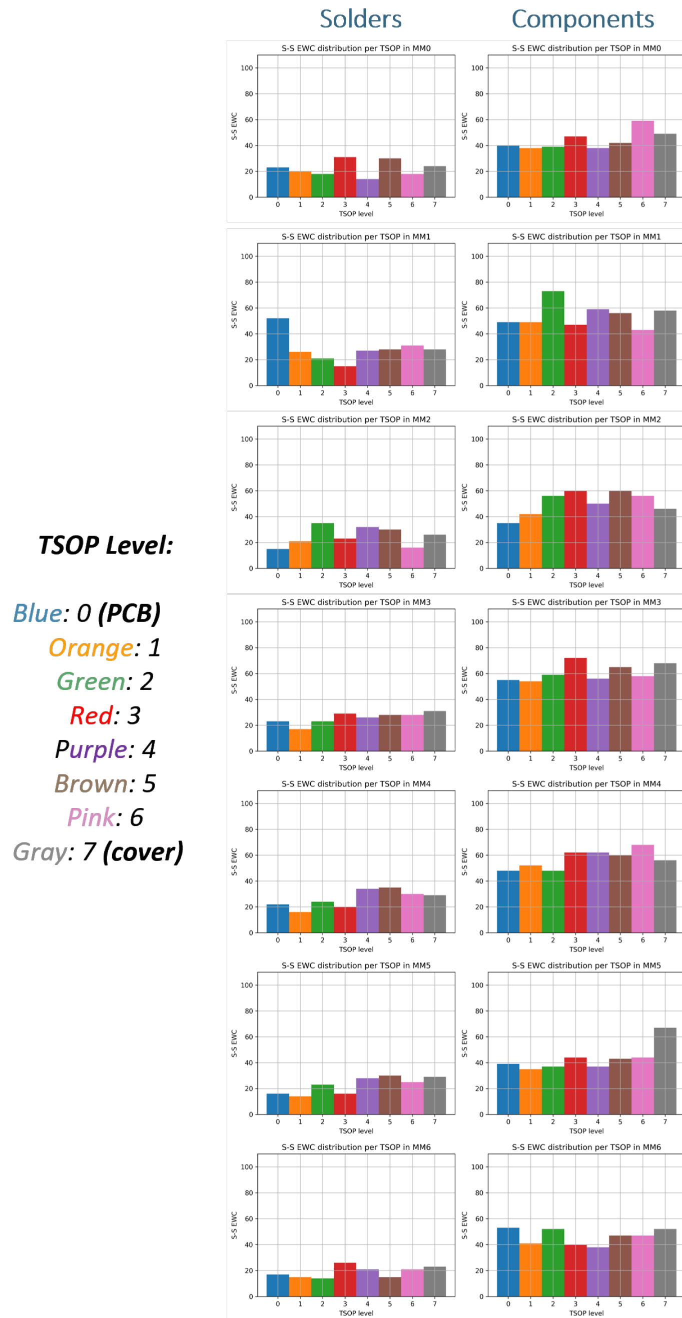

Figure 4.6: S-S EWC distribution per TSOP level in both side of all memory (DATA & CHECK-SYMBOLS) modules

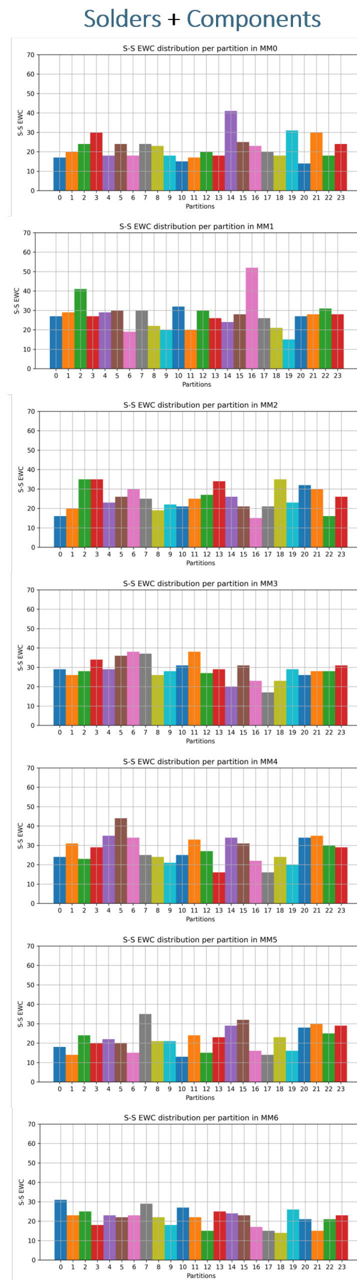

Figure 4.7: S-S EWC distribution per logical partition ([0..23] logical sub-ROWS) in all memory modules matrix

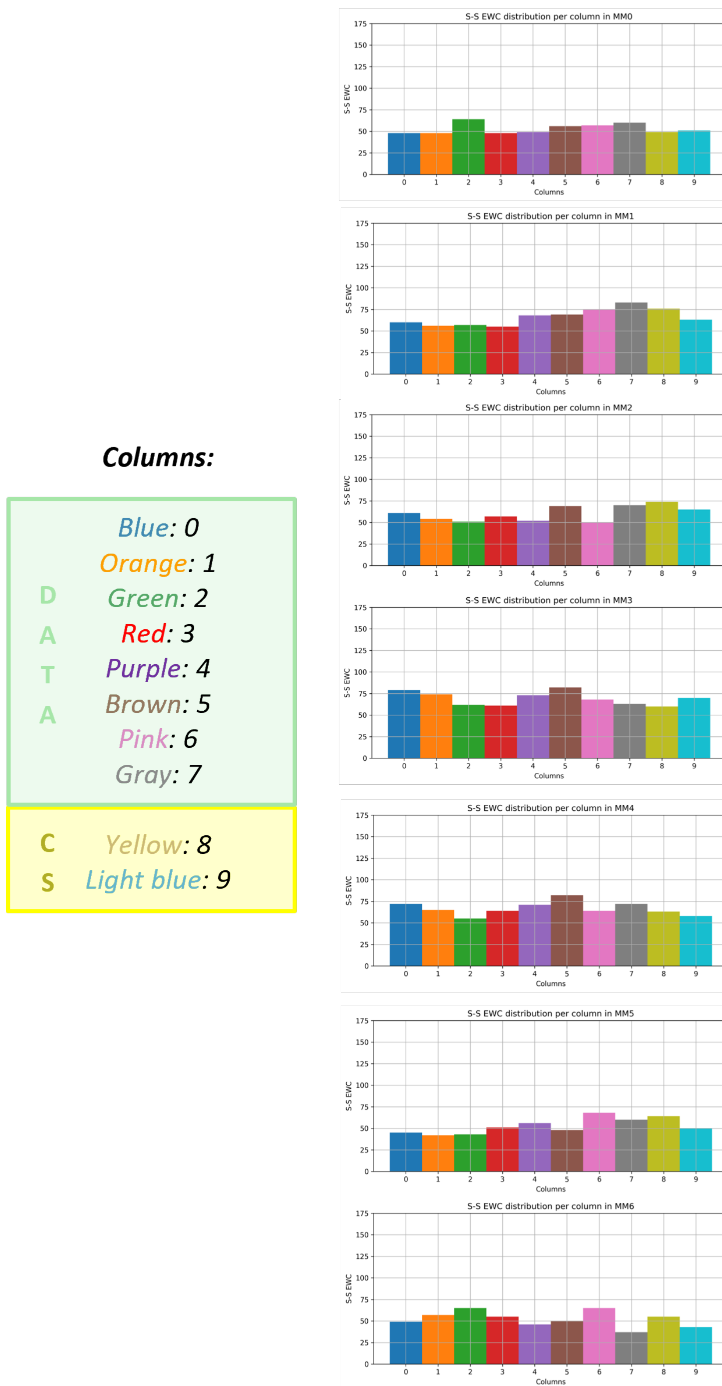

Figure 4.8: S-S EWC distribution per physical active column (0..9) in all memory modules matrix

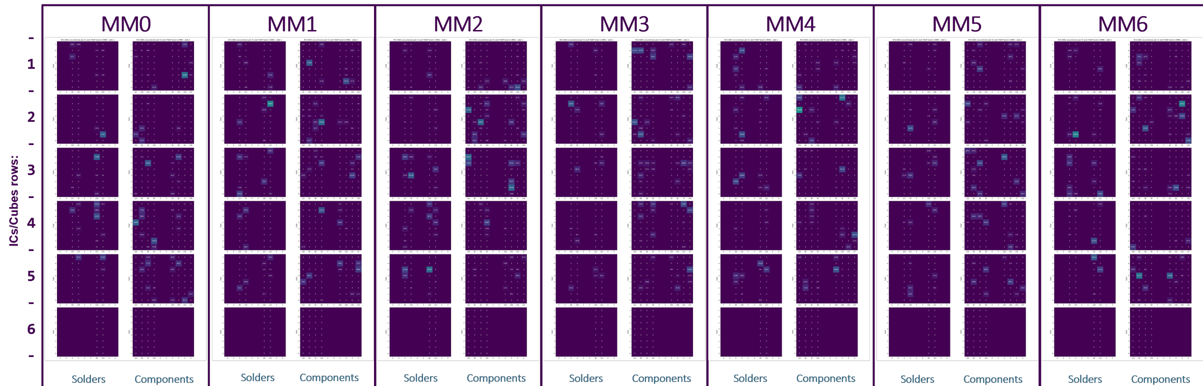

Figure 4.9: S-S EWC distribution per ICs/cubes and the relative TSOP levels in both side of all memory modules matrix

As for Satellite A, the cubes most affected by this proliferation phenomenon, the S-S EWCs location appears to be distributed throughout all TSOP levels and not concentrated in a single level. While the IC/cube 121 showing the maximum number of S-S-EWC on Satellite B SSMM, they are all located in a single TSOP level (27 S-S EWC all concentrated in IC121 - TSOP 0 i.e. that one close to the PCB): this fact suggests that the anomaly affects only one TSOP level and not the entire cube.

4.1.4. S-S EWCs distribution considering also the re-occurrences

Now instead of considering only the absolute number of S-S EWCs, also the number of times each cell is found in error is taken into account. Figures 4.10, 4.11, 4.12, show the number of corrections performed on S-S EWCs as a function of the TSOP level, IC/cube, and levels within the ICs/cubes of each MM boards respectively.

Despite the large number of S-S EWC in the IC121 of MM1 identified earlier, there appear to be no higher number of corrections in that IC/Cube and TSOP level: this suggests that the leakage effect shown by those cells lasted a relatively short time, leading to few corrections (and observed correction time by the periodic scrub passage) following their appearance.

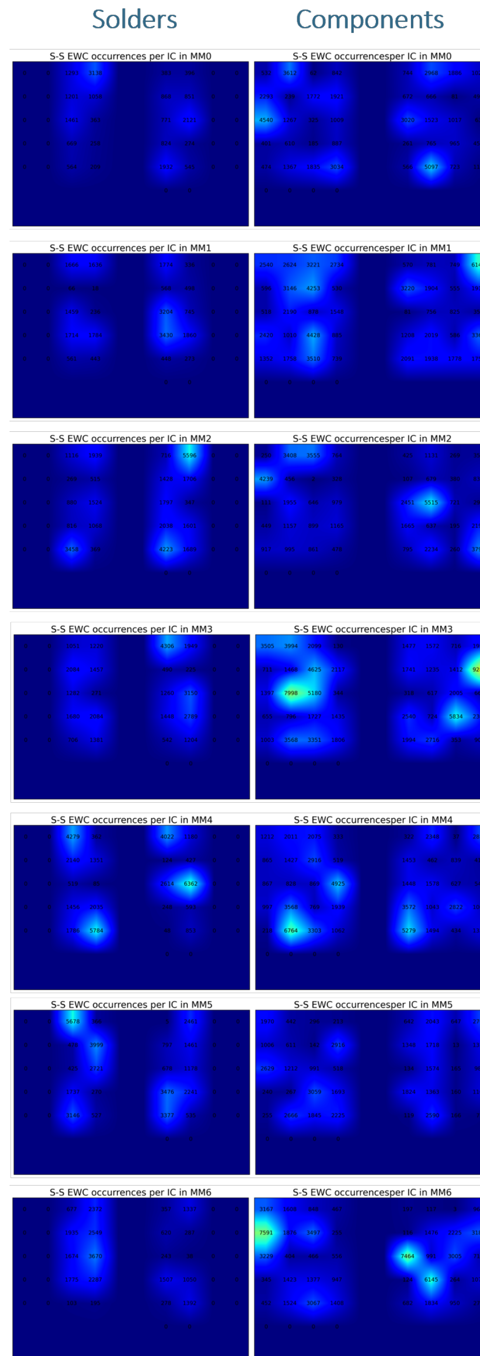

Figure 4.10: S-S EWC distribution considering also the re-occurrences per IC/cube, across all memory modules (MAX_S-S_EWC_occ_per_IC = 9281 on MM3)

Again, as per Satellite A, the "hot spots" characterized by permanently leaking cells are located mainly in the Components side (generally warmer) of each memory module PCB.

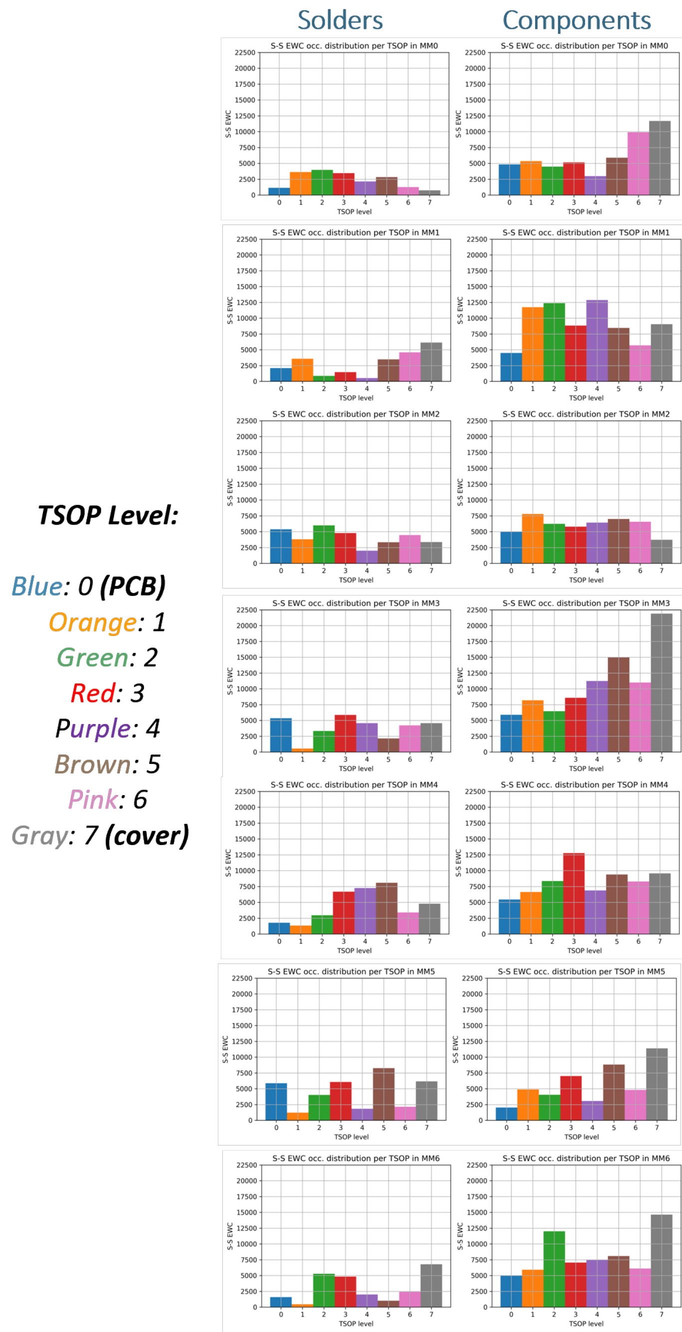

Figure 4.11: S-S EWC occurrences distribution per TSOP in both side of all memory modules

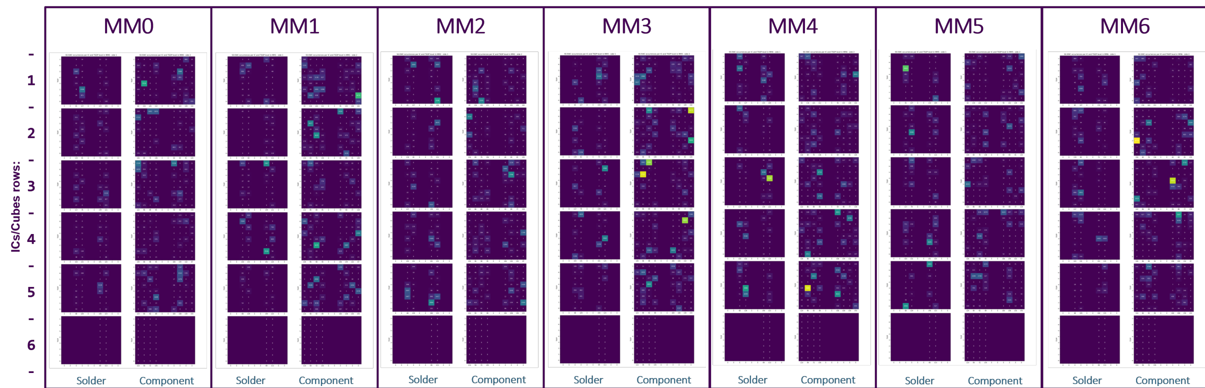

Figure 4.12: S-S EWC distribution considering also the re-occurrences of same address, per TSOP, in both sides of all memory modules matrix

From Figure 4.12, now the "hot spots" within the ICs/cubes are mainly located in the central MM3, MM4 memory modules and in MM6. A possible thermal lever is suspected, since these MM board local temperatures are most likely increased due to new organisation of active PCBs in the SSMM.

4.1.5. Distance between S-S EWCs addresses

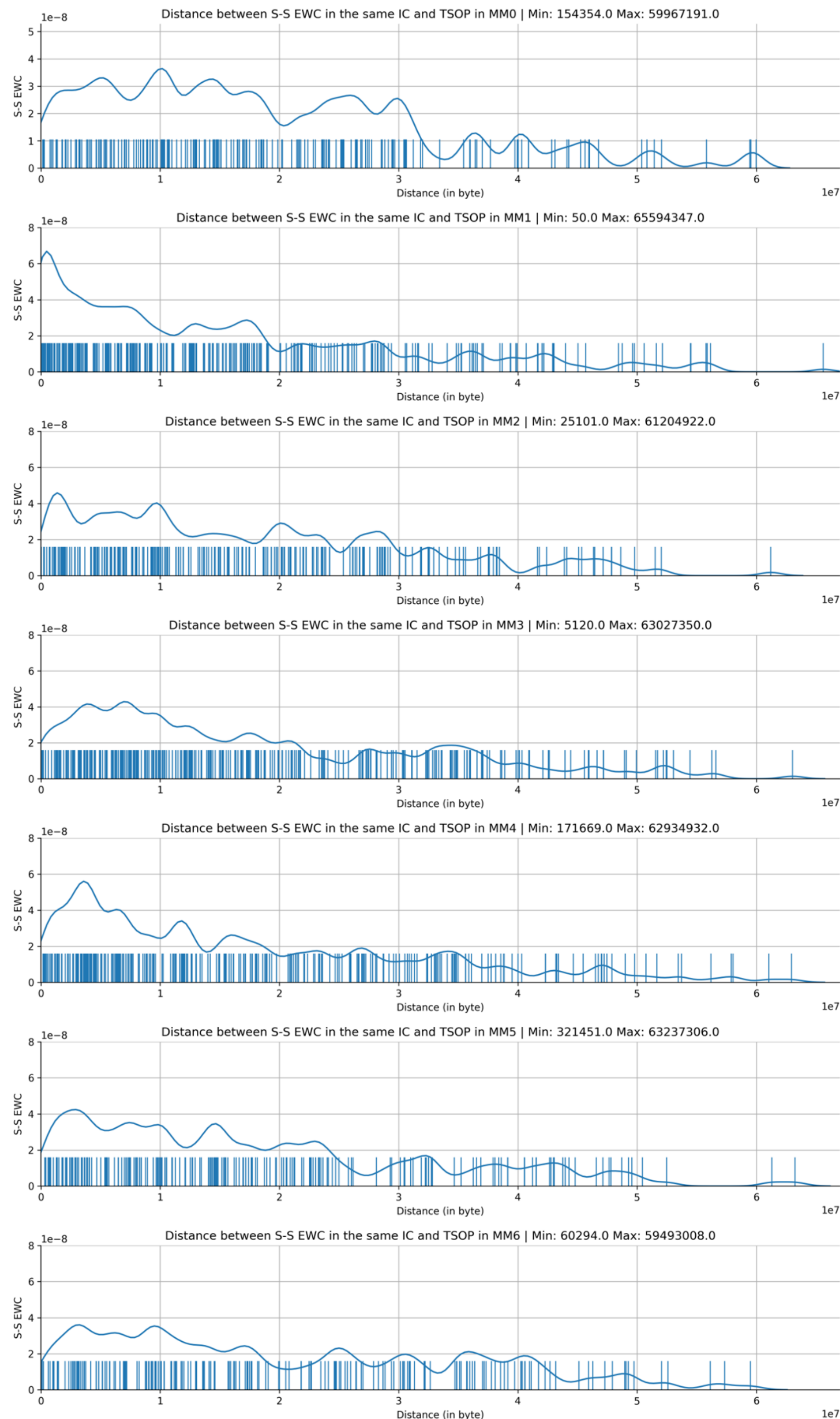

Figure 4.13: Average distance between S-S EWC inside each IC/cube and TSOP level over all MM boards

As per Satellite A, Figure 4.13 shows the distribution of the consecutive distances between S-S EWCs inside the 64 MiB (x-axis) of TSOP levels composing the ICs of all memory modules. These distances are obtained with the same procedure explaned in Chapter 3.1.5.

Again, most of the "mutual" distances between S-S EWCs are concentrated below 3 MiB, with large part of peaks visible in the first 2 MiB, in all memory module PCBs.

4.2. Multi-Shot Extremely Weak Cell (M-S EWC) Analysis

4.2.1. M-S EWCs activation over time

As in SSMM memory boards on Satellite A, the M-S EWCs activation after the third/-fourth year in orbit starts to follow the temperature profile of the SSMM TRP reported in Figure 4.3. As before, this cell typology results in leakage much more often than the S-S EWCs, bringing the number of simultaneously active M-S EWCs to very high values in all modules boards.

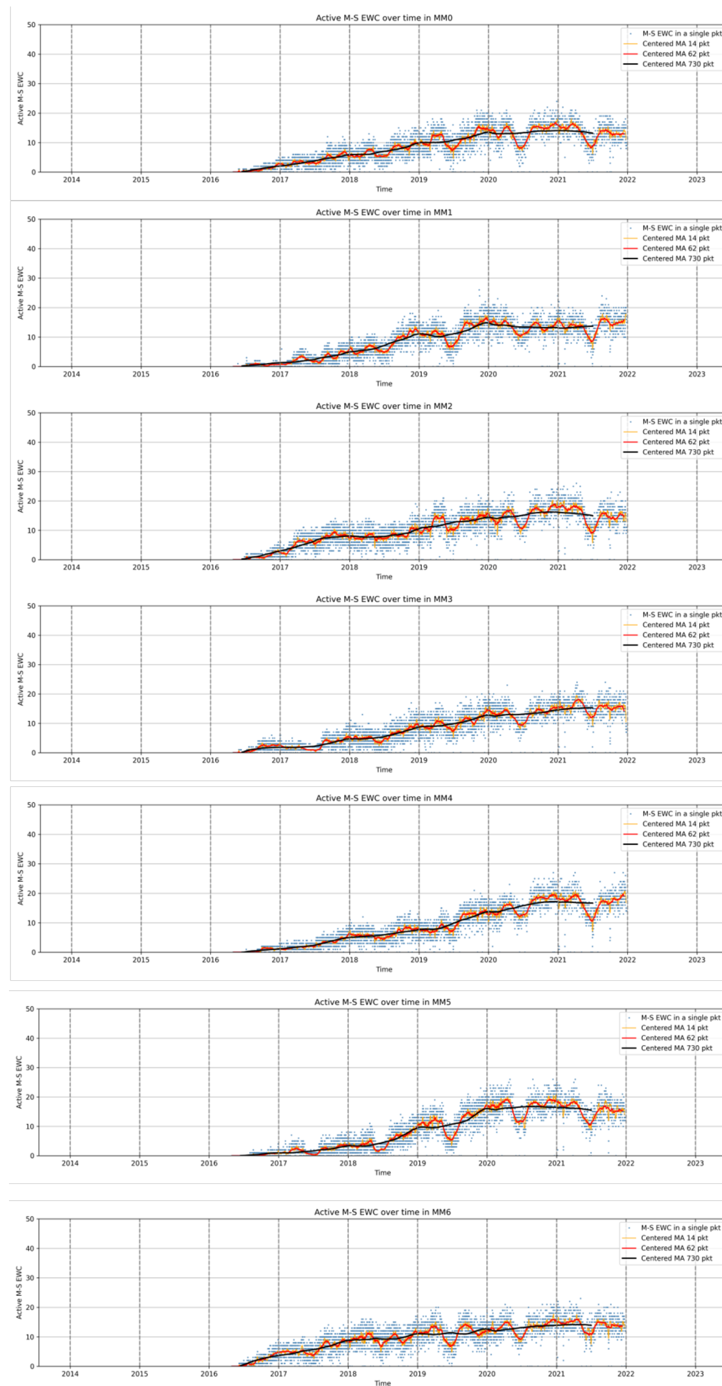

Figure 4.14: Activation of M-S EWC over time in all MM boards, from MM0 to MM6

Also for M-S EWCs, their total certified number increases progressively over time in a linear way, except for the MM1 module where, starting from mid-2019 for a period of about one year, there was a rapid increase in the absolute number of this type of cells, bringing their number to values well above those achieved by Satellite A after 5 years in orbit (shown in green in the right side).

This increase in absolute number, however, was not visible in the previous graphs in Figure 4.14 related to cells activation: this suggests that the cells proliferated on MM1 during that bounded period are characterized by short activation periods.

4.2.2. Total certified number of M-S EWCs over time

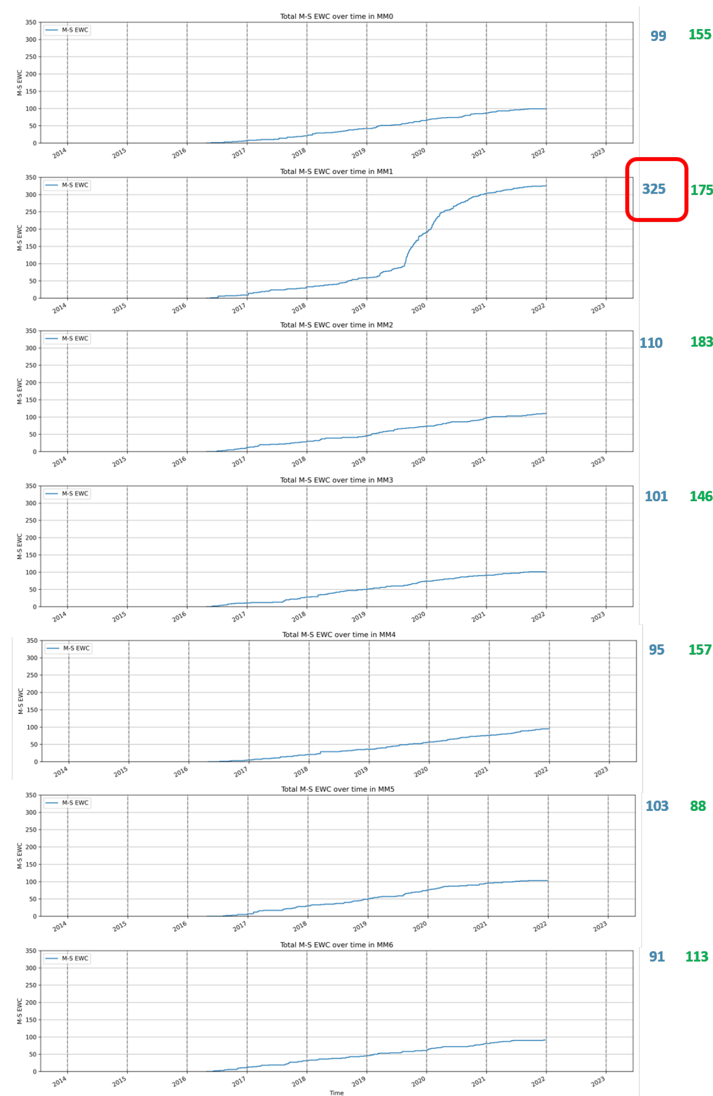

Figure 4.15: Total certified number of M-S EWC over time in all MM boards

4.2.3. M-S EWCs ICs/TSOPs Geometrical Distribution

Now looking at the geometric arrangement of the M-S EWCs among the various ICs/cubes of each memory module, it can be seen that the increase started in mid-2019 is all con-

centrated in a single level of a single cube (TSOP0 of IC121) in which a dual increase in S-S EWCs was already observed concentrated in a same TSOP in the previous section (Figure 4.5).
The same information can be seen in the histograms 4.17, 4.18 and 4.19 related to the MM1 module. These graphs, together with the one in Figure 4.20 show and confirm how these cells are all located within the same level (TSOP0) of the same IC/cube (IC121).

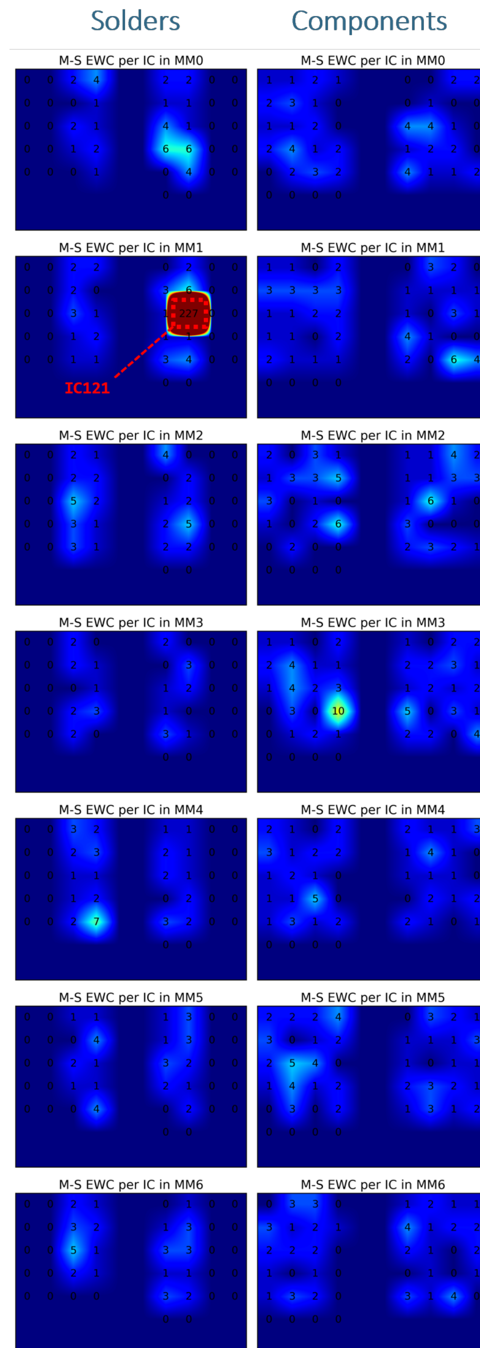

Figure 4.16: M-S EWC distribution (single address, without computing their occurrences), per IC/cube, across all memory modules (MAX_M-S_EWC_per_IC = 10 on MM3 excluding the critical IC/cube for which the value is 227)

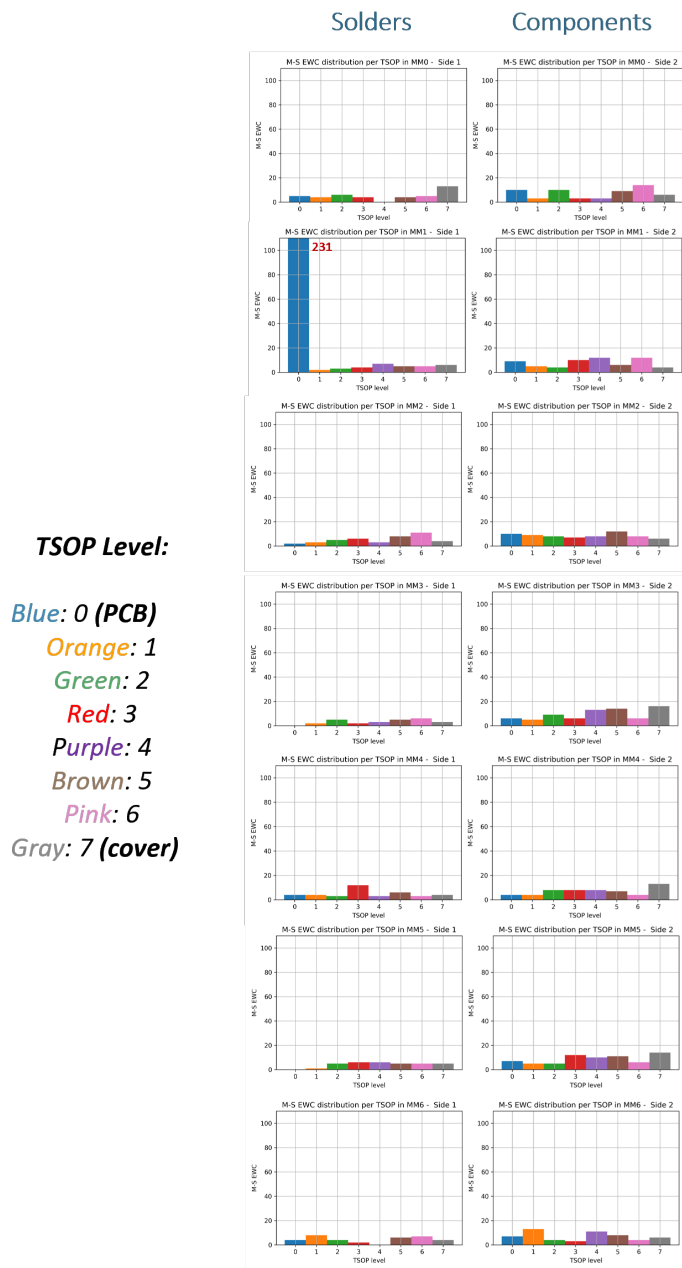

Figure 4.17: M-S EWC distribution per TSOP in both side of all memory modules

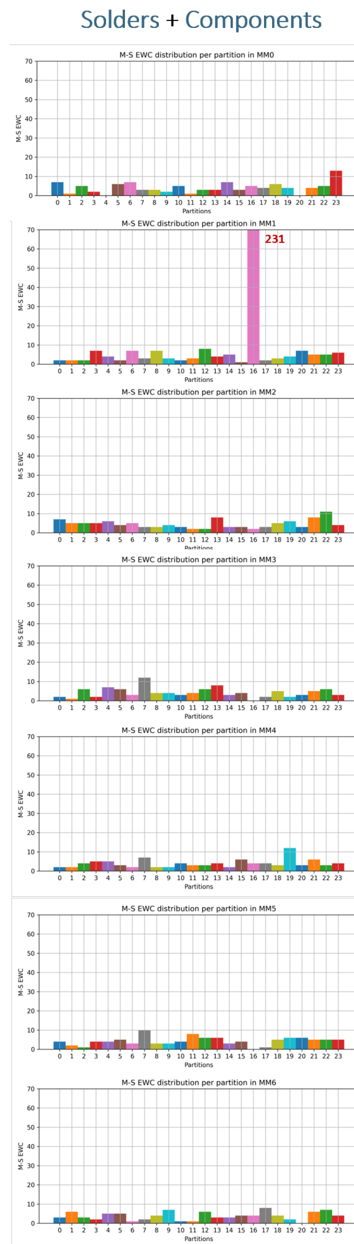

Figure 4.18: M-S EWC distribution per logical partition ([0..23] logical sub-ROWS) in all memory modules matrix

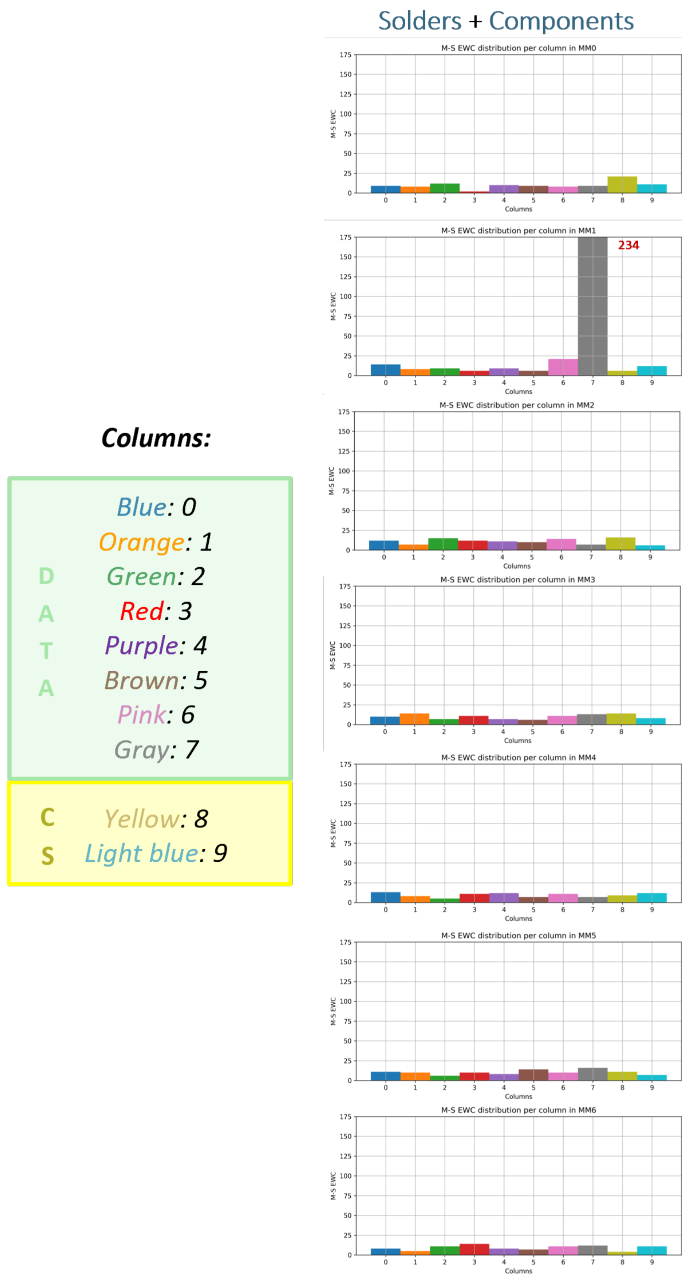

Figure 4.19: M-S EWC distribution per physical column (0..9) in all memory modules matrix

In all the Figures 4.17, 4.18, 4.19, as expected, the anomaly is detected from different perspectives as a peak of M-S EWCs in TSOP0, partition 16, column 7 (the one feeding the IC/cube affected by this anomaly) on MM1.

Figure 4.20: M-S EWC distribution per ICs/cubes and the relative TSOP levels in both side of all memory modules matrix

As for the remaining modules, the behavior of the M-S EWCs mirrors the one seen on Satellite A previously. Excluding the critical IC121/TSOP0, the remaining M-S EWCs were found to be evenly distributed on the faces of each MM boards but slightly concentrated in the Components faces (that are "warmer").

Similar to what we found in Satellite A analysis, considering the number of times each cell identified as M-S EWC is found in single error (and subsequently corrected), there is no TSOP level particularly affected by this phenomenon common to all memory modules (Figure 4.21).

As mentioned in previous chapter about the "hot spots", SDRAM memory locations showing frequent corrections over time can be related to more than one stuck bit within a single symbol of a code-word. Again these "hot spots" are typically concentrated in the Components face of each MM board.

4.2.4. M-S EWCs distribution considering the re-occurrences

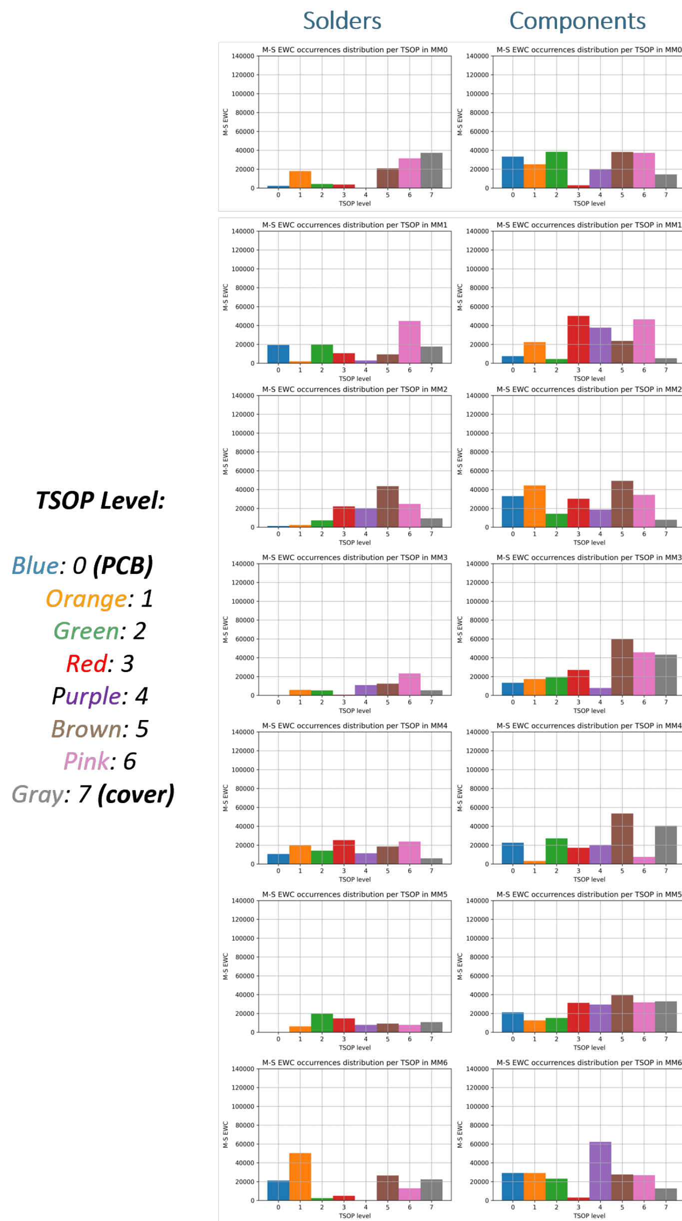

Figure 4.21: M-S EWC occurrences distribution per TSOP in both side of all memory modules

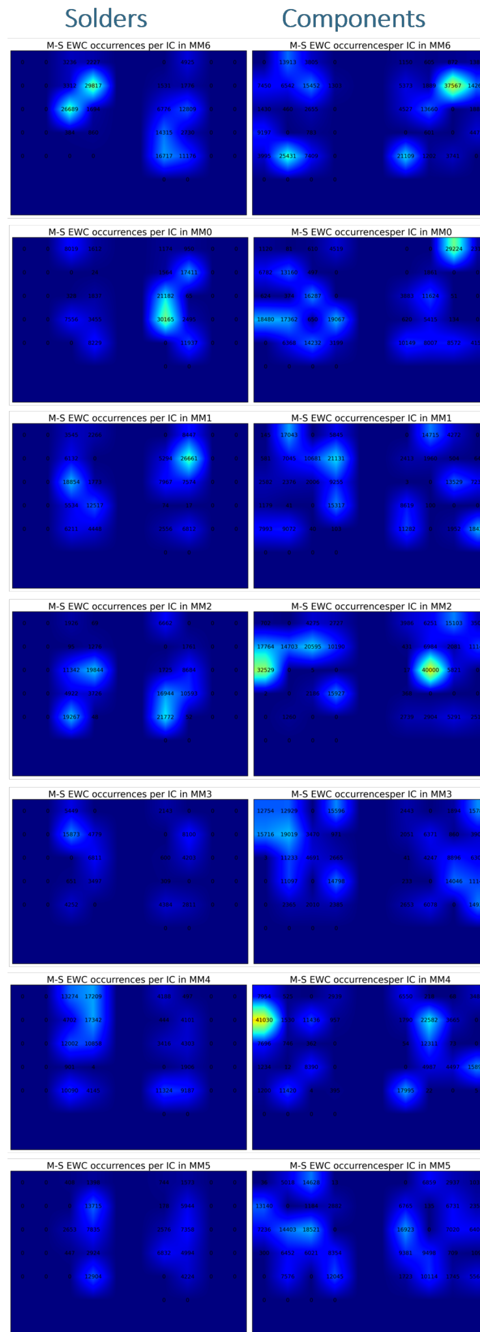

Figure 4.22: M-S EWC occurrences distribution per IC cube, across all memory modules (MAX_M-S_EWC_occ_per_IC = 41030 on MM4)

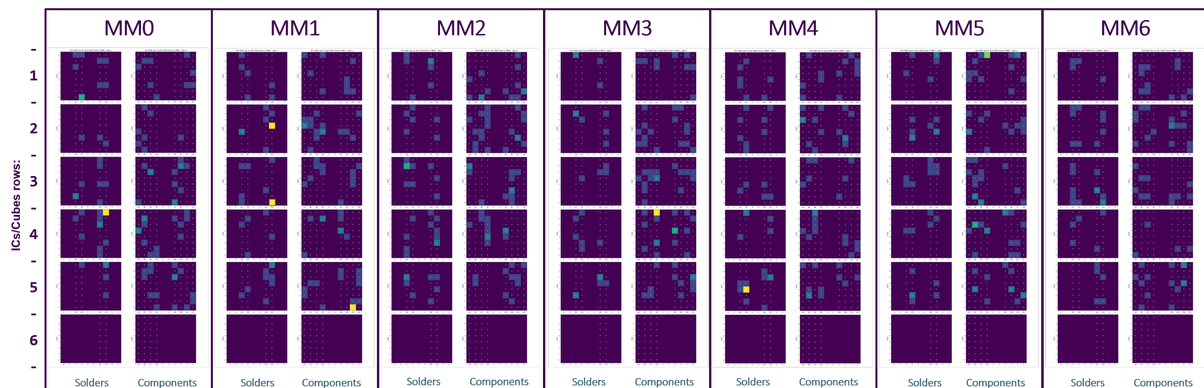

Figure 4.23: M-S EWC occurrences distribution TSOP levels in each IC/cube in both side of all memory modules matrix

As we can see in Figure 4.23, in the critical IC121/TSOP0 of MM1 board, there is no evidence of a greater number of M-S EWCs than in other ICs: this, again, is a signature that the cells appeared in that critical TSOP are characterized by lower leakage re-occurrences.

4.2.5. Distance between M-S EWCs addresses

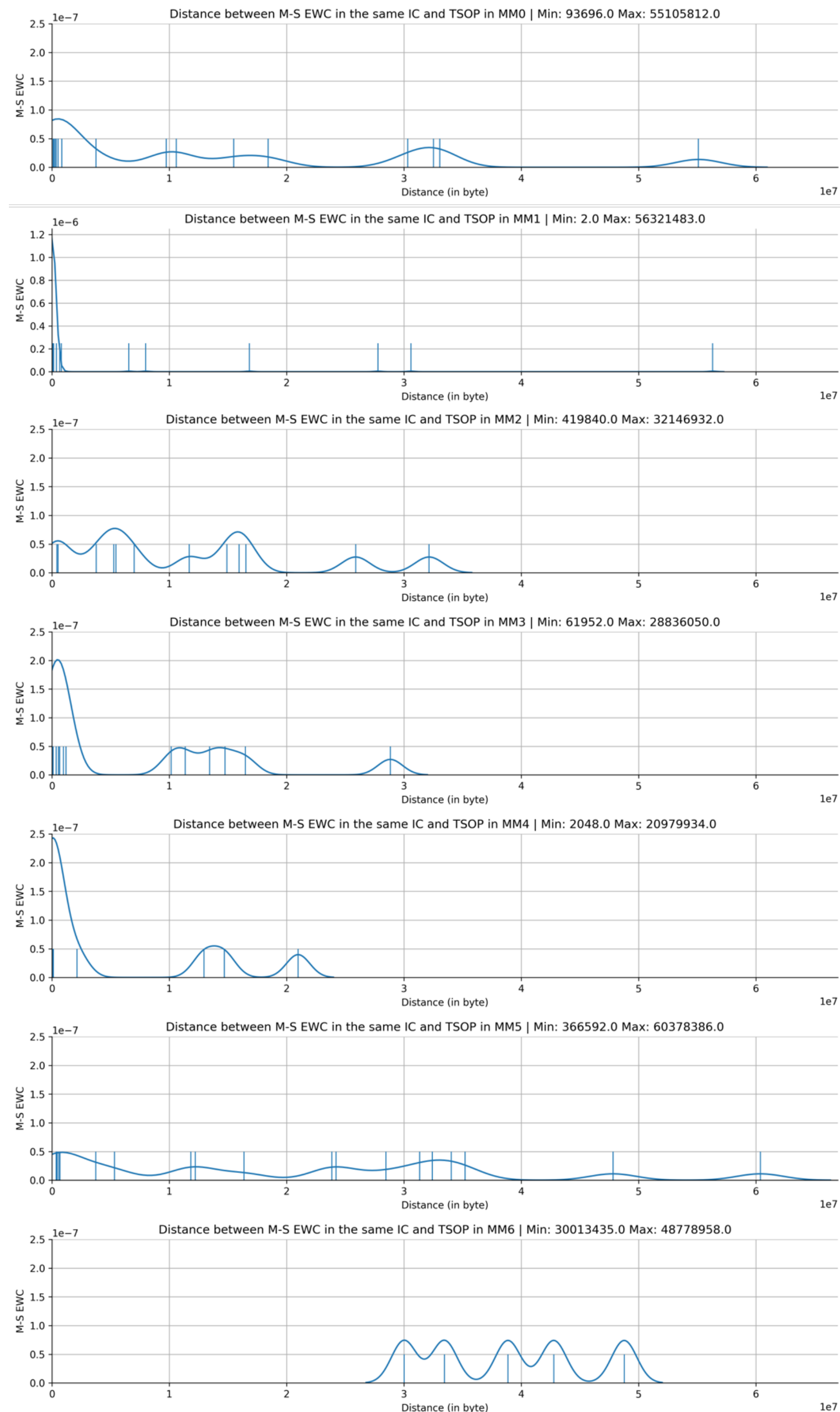

Figure 4.24: Distance between M-S EWC indide the same IC/cube and TSOP level in all MM boards

The "mutual" distance between these M-S EWCs class shows a "flatter" distribution w.r.t. the S-S EWCs except for MM1. Again, a minimum distance of 2048 is noticeable. Finally, a high distribution below 0.1 MiB is visible in MM1 suggesting that the anomaly affected a small portion of the IC121/TSOP0.

4.3. S-S EWC + M-S EWC Analysis

Now as done per Satellite A, we will consider the two types of EWCs together also on Satellite B since they are the expression of a same leakage phenomenon induced by radiation hits.

4.3.1. EWCs activation over time

As expected, the combined behaviour of both phenomena follows the TRP waveform of the SSMM unit also in Satellite B, but it is observed that the waveforms are much more similar across all memory modules boards than the EWCs in the Satellite A SSMM.

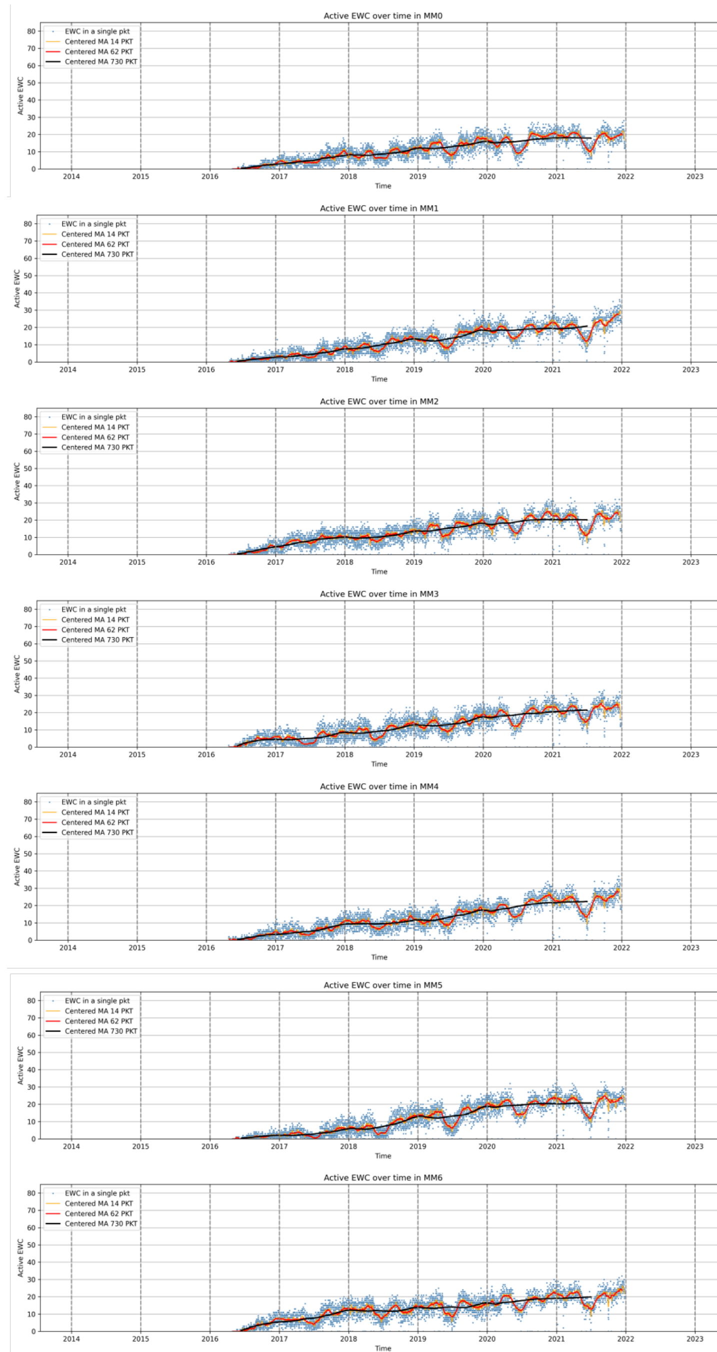

Figure 4.25: Activation of EWC over time in all MM boards, from MM0 to MM6

4.3.2. Total certified number of EWC over time

The sum of both phenomena maintains the linear growth already seen in previous chapter, except for the module MM1 showing an anomalous increase already found mainly in the M-S EWCs in mid-2019 due to the critical IC121/TSOP0.

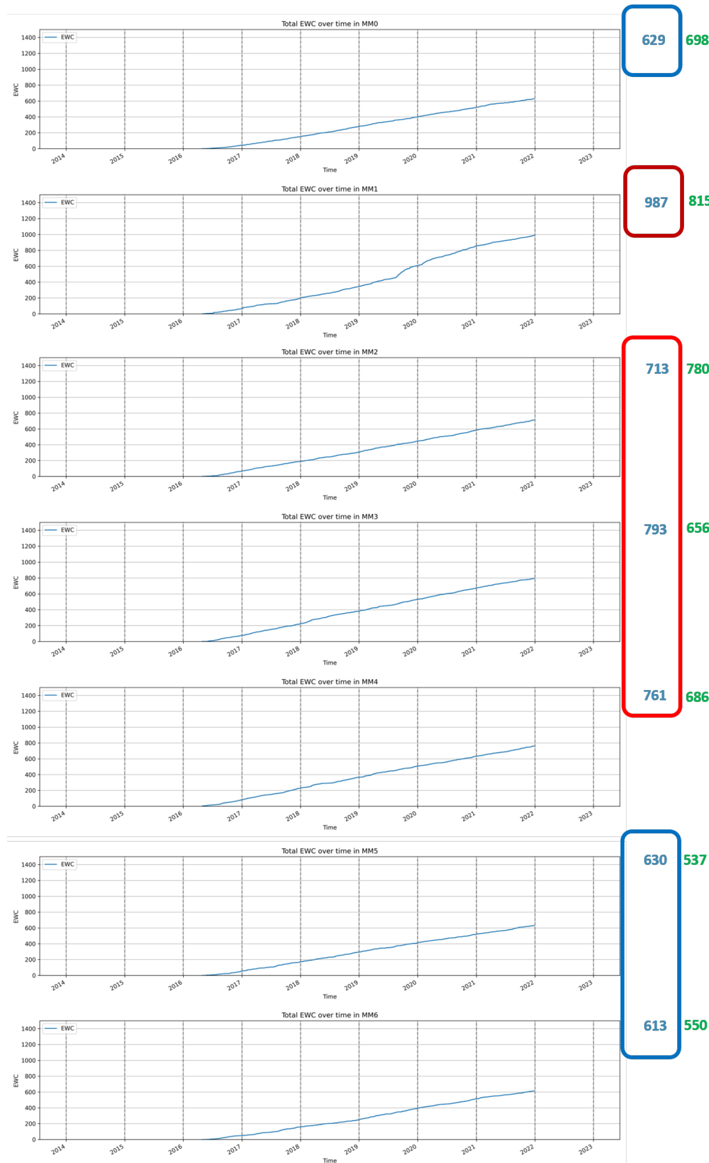

Figure 4.26: Total certified number of EWC over time in all MM boards

Again, Figure 4.26 highlights the number of total EWCs per MM board after roughly 5 years in orbit: a different pattern among the various PCBs is visible compared with Satellite A (green numbers). In particular, the most affected MM boards now are the internal ones (MM2-MM4, excluding MM1 afflicted by the anomaly). MM0 presents less EWCs w.r.t. Satellite A while, at the same time, MM5 and MM6 are more affected by this phenomenon. This behavior reflects the new arrangement of active boards of Satellite B shown in Figure 4.1.

4.3.3. EWCs ICs/TSOPs Geometrical Distribution

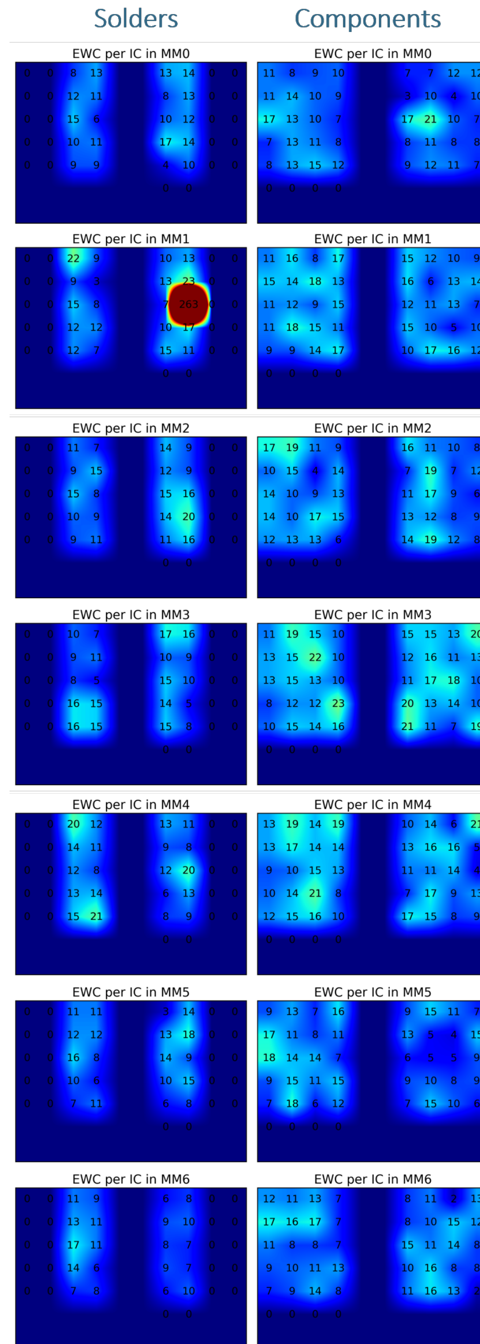

Figure 4.27: EWC distribution (single address, without computing their occurrences), per IC cube, across all memory modules (MAX_EWC_per_IC = 23 on MM3 excluding the critical IC/cube for which the value is 263)

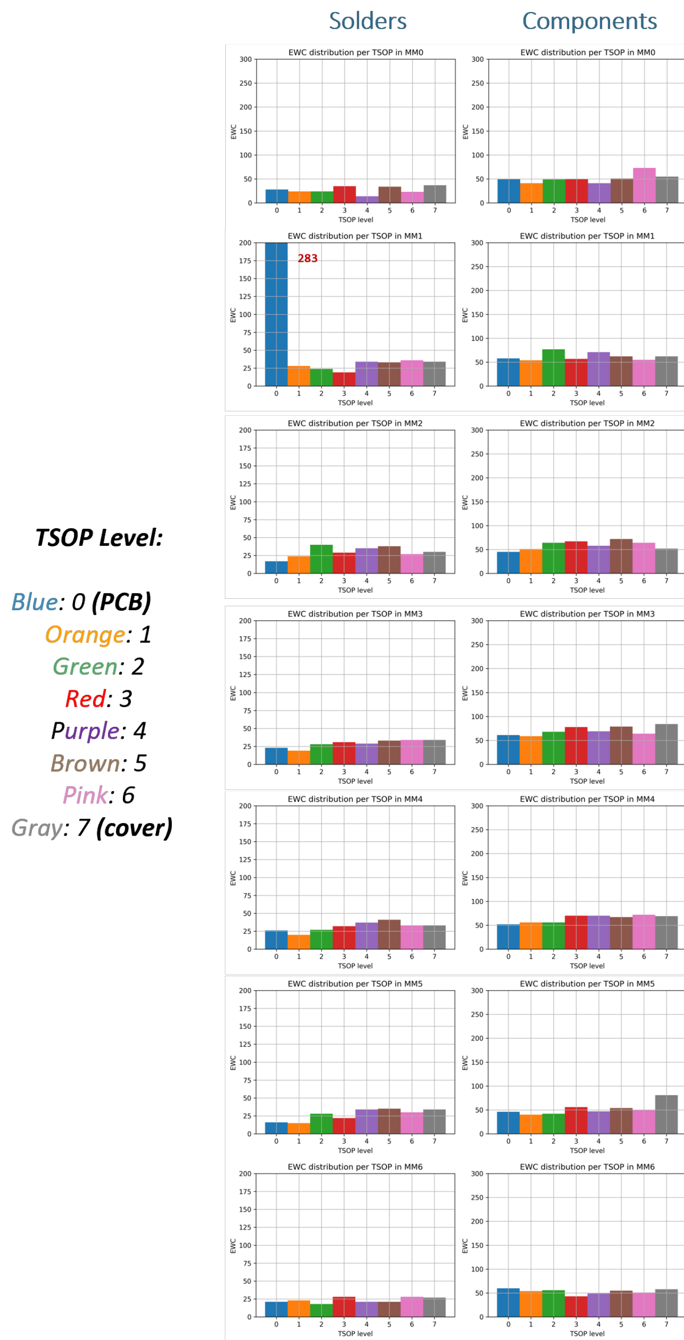

Figure 4.28: EWC distribution per TSOP in both side of all memory modules

Solders + Components

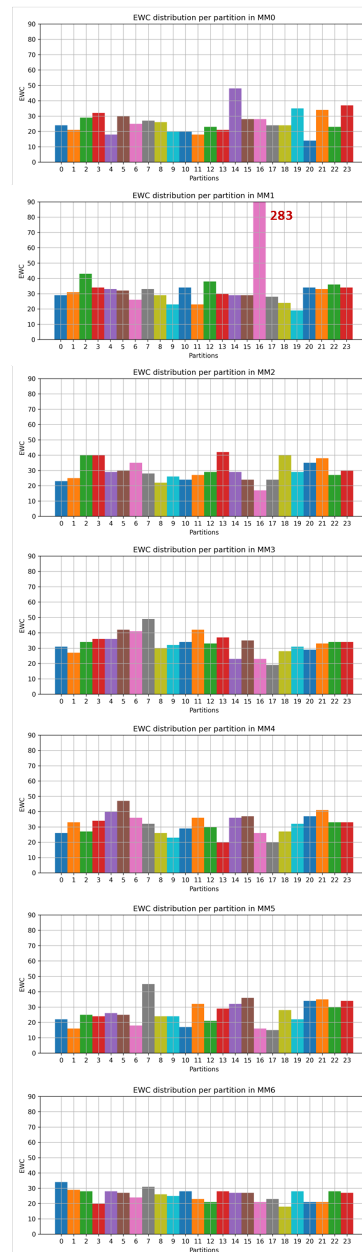

Figure 4.29: EWC distribution per logical partition ([0..23] logical sub-ROWS) in all memory modules matrix

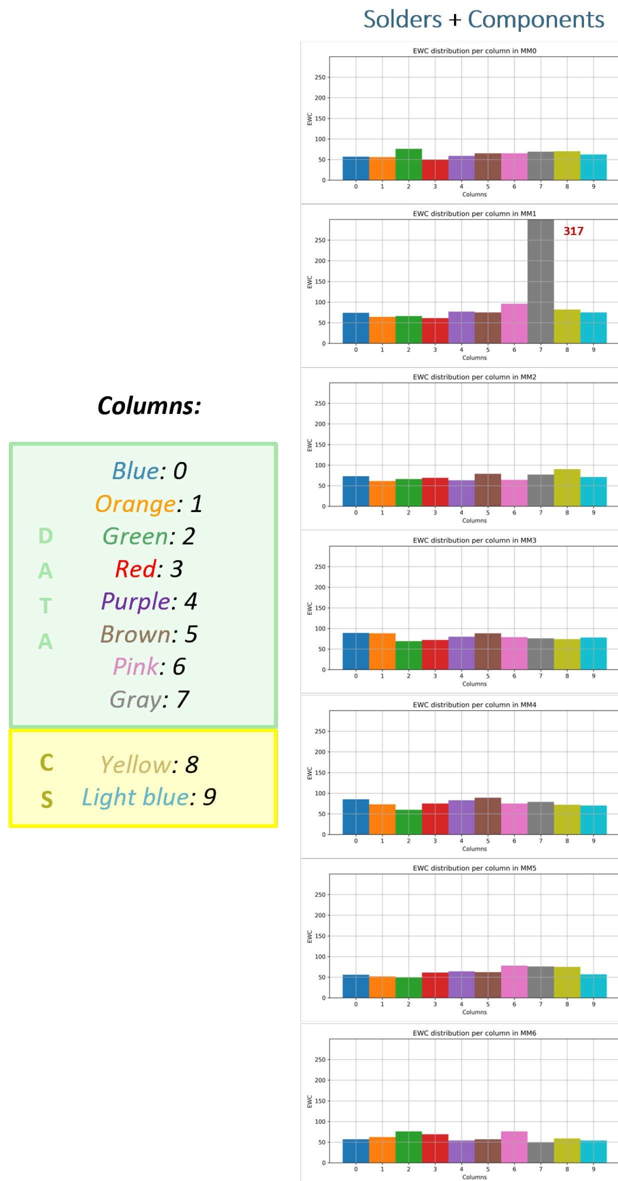

Figure 4.30: EWC distribution per physical column (0..9) in all memory modules matrix

Again, in all the Figures 4.27, 4.28, 4.30, as expected, the anomaly is detected from different perspectives. In particular there is still no evidence of dependence from power distribution network inside a MM board; the anomaly in MM1 is located inside one IC only, and the remaining 5 ICs fed from the same column power circuitry are not affected. This is a further confirmation that it is a problem in that critical TSOP.

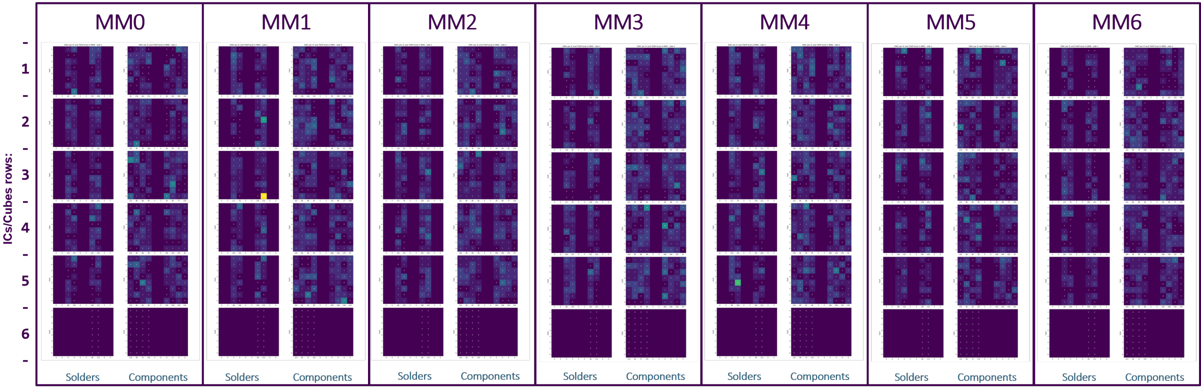

Figure 4.31: EWC distribution per ICs and TSOP levels in both side of all memory modules matrix

4.3.4. EWCs distribution considering the re-occurrences

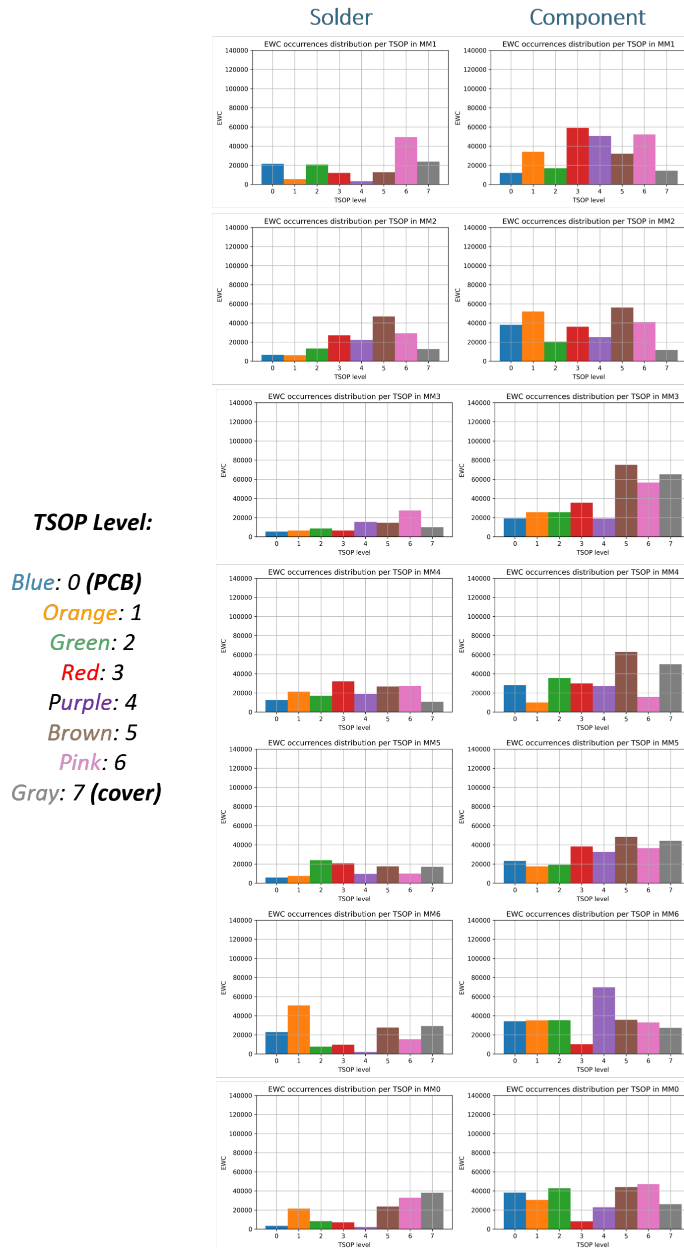

Figure 4.32: EWC occurrences distribution per TSOP in both side of all memory modules

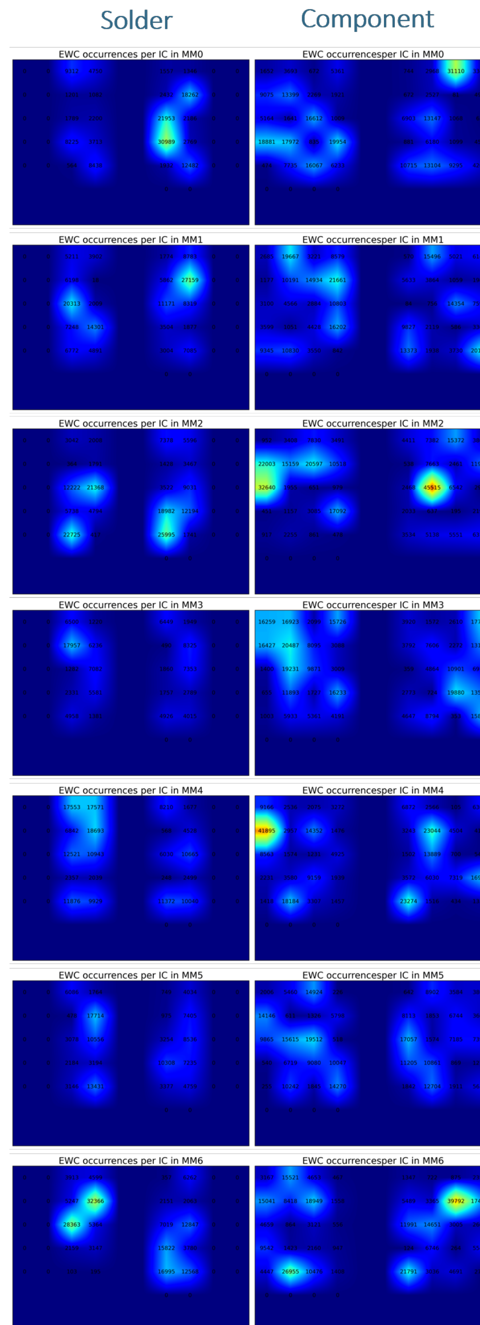

Figure 4.33: EWC occurrences distribution per IC cube, across all memory modules (MAX_EWC_occ_per_IC = 45515 on MM2)

Also here, "hot spots" are concentrated on the component side.

Figure 4.34: EWC distribution considering also the re-occurrences of same adderesses, per TSOP, in both side of all memory modules matrix

4.3.5. Distance between EWCs addresses

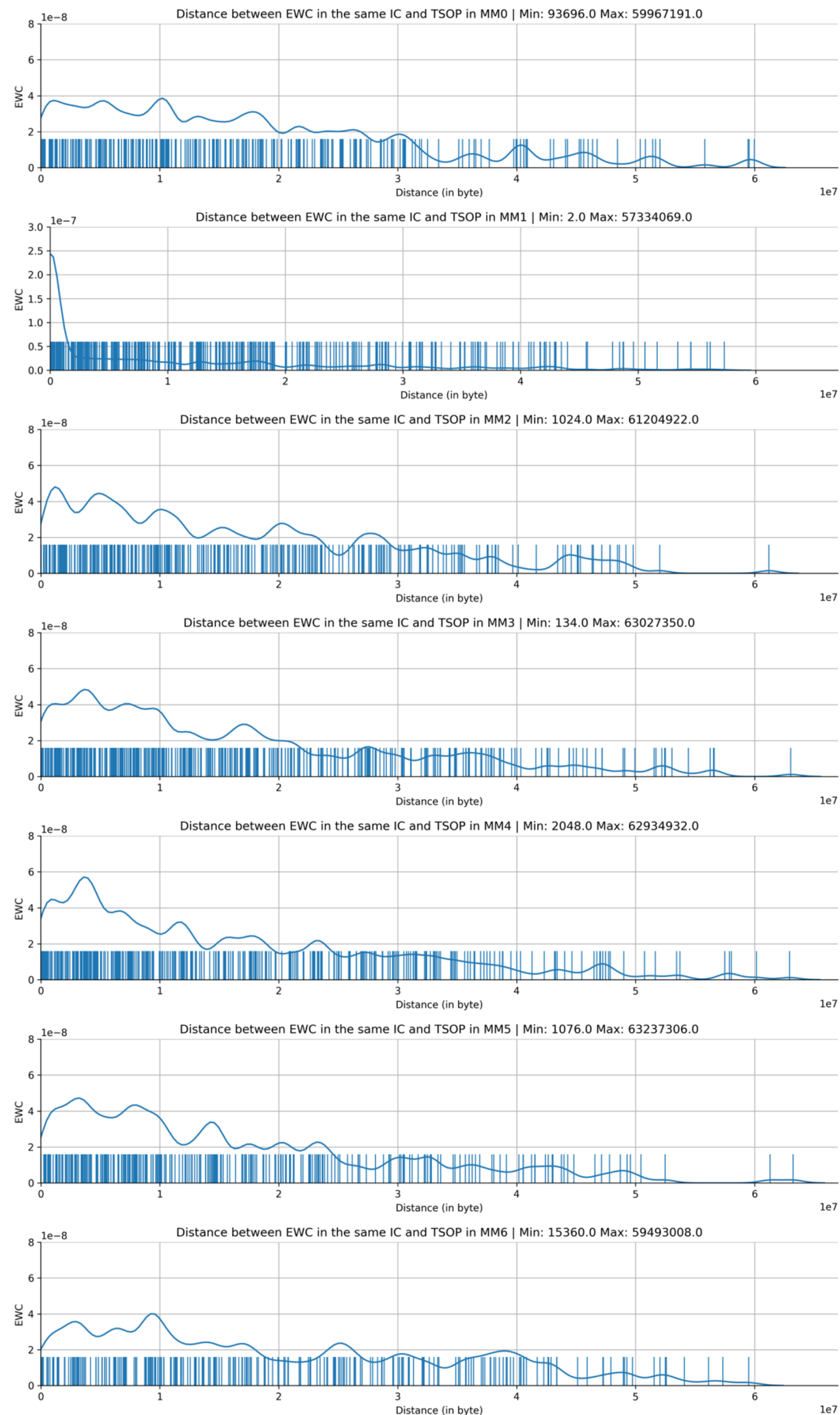

Figure 4.35: Distance between EWC indide the same IC/cube and TSOP level in all MM boards

The "mutual" distribution of distances between EWCs is more influenced by S-S EWCs with the exception of MM1 affected by the anomaly. The minimum distance (2 Bytes) and high concentration of distances $\leqslant 0.1$ MiB suggests that the anomaly affected a limited area of IC121/TSOP0.

4.4. SEU Analysis

As per Satellite A, looking only at TM(6,6) data, after 3/4 years in orbit the SEU number is surely under-estimated.

4.4.1. Cumulative SEU over time

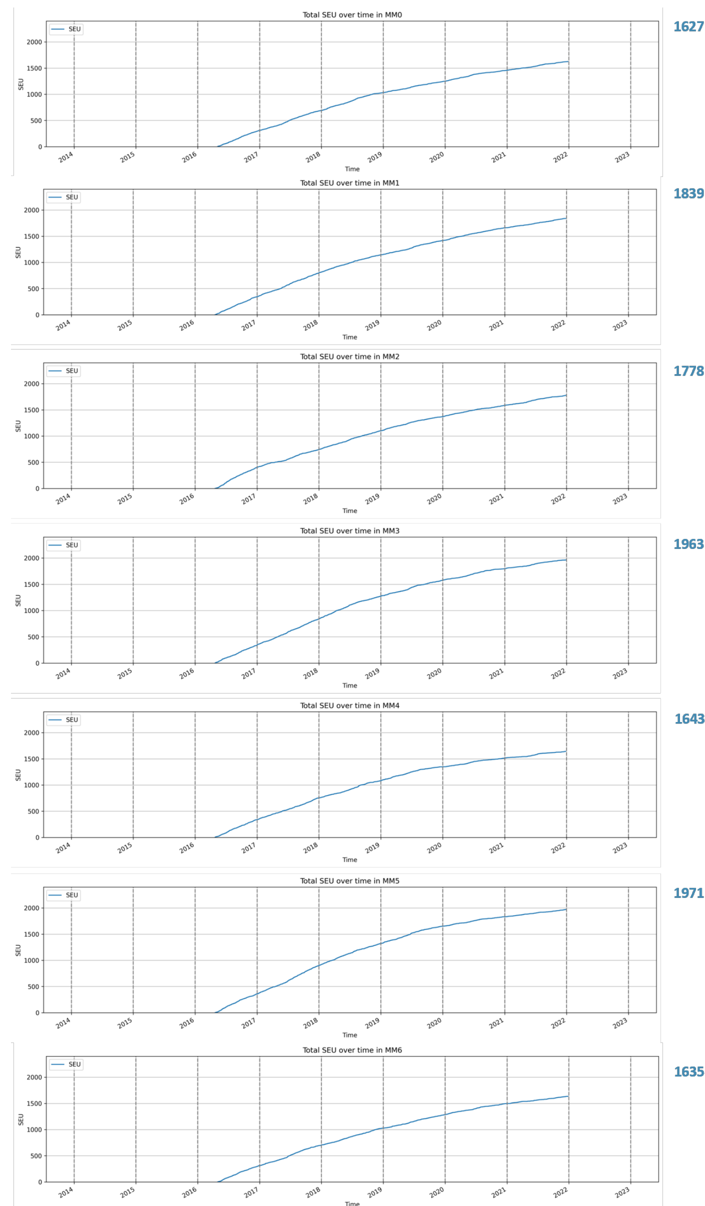

Figure 4.36: Cumulative SEU over all memory modules boards

Figure 4.36 represents the cumulative number of total SEUs over time, this representation gives us only a partial view of the phenomenon, because starting from the third/fourth year, the phenomenology of EWCs takes over in occupying the 128 available entries also on Satellite B, as already observed per Satellite A data.
Taking into account only the first 3 years, it can be seen that the growth in all memory modules of this phenomenon follows the same trend acorss the MM board of the same Satellite B SSMM, confirming the isotropic radiative origin of such a class of corrections.

In Figure 3.39 the number of SEUs found within all packets sent over time is reported.

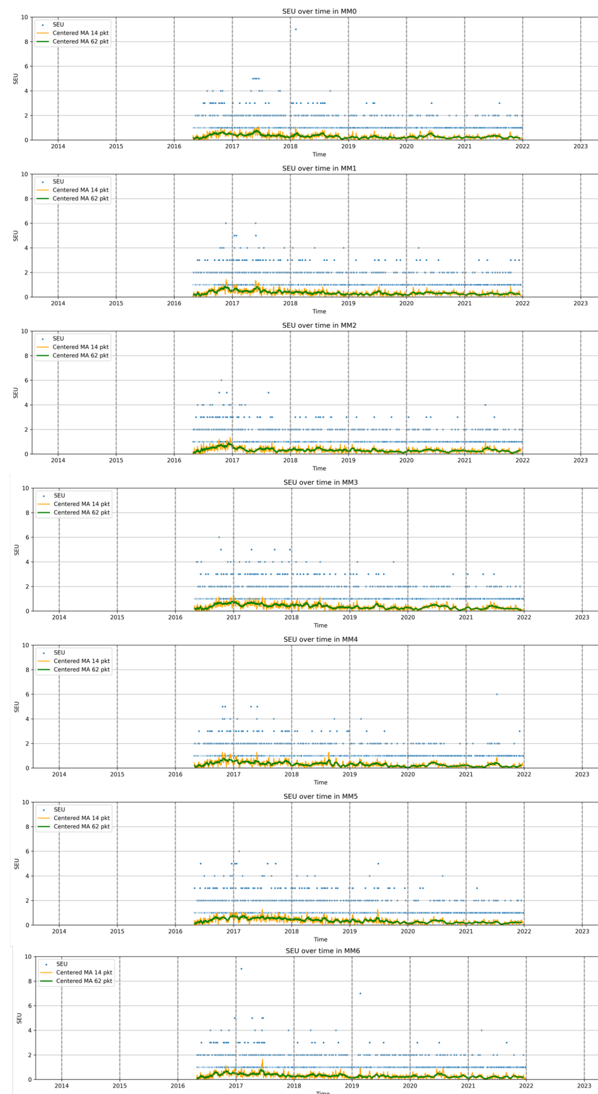

Figure 4.37: SEU occurrences over time in all memory modules boards

As for Satellite A, it is possible to see that in the first 3 years, when the information contained in the packets can be considered representative, that the average number of SEUs that hit all memory modules is slightly higher than in subsequent years where its value has remained roughly constant.

Again, even if going beyond a possible increasing due to entering the Sun Cycle 25, the EWC presence in the 128 entries structure inhibits to observe such a phenomenon.

4.4.2. SEU ICs/TSOPs Geometrical Distribution

In Figures 4.38 and 4.39 the distribution per IC/cubes and TSOP levels respectively is reported. A much more homogeneous distribution is immediately visible on both faces of all memory modules boards. Comparing these with the graphs shown in the previous chapters related to EWCs, no relationship with the distribution of temperatures over the memory module is found. This confirms the different levers between the two phenomena. There is no evidence that suggests a relationship with temperature but distribution of single error correction highlights a concentration on IC121/TSOP0.

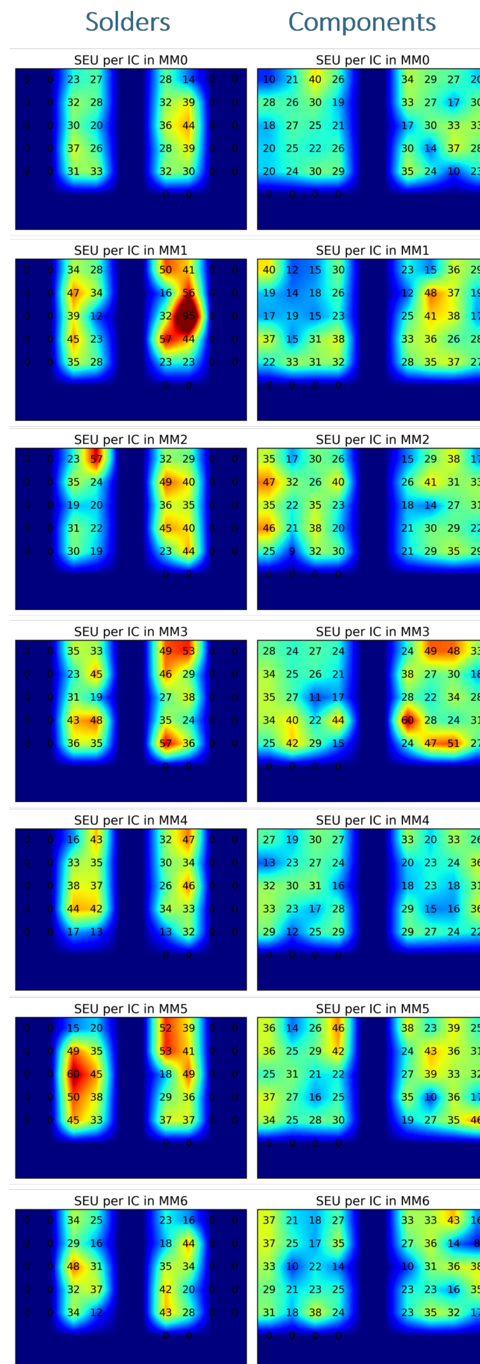

Figure 4.38: SEU distribution per IC in all memory modules (MAX_SEU_per_IC= 60 on MM5 and MM3 excluding the critical IC/cube for which the value is 95)

The distribution of SEUs by TSOP level shows a uniform distribution across levels, this further reinforces the radiative, and thus random, origin of this phenomenon. No differences between memory module PCBs.

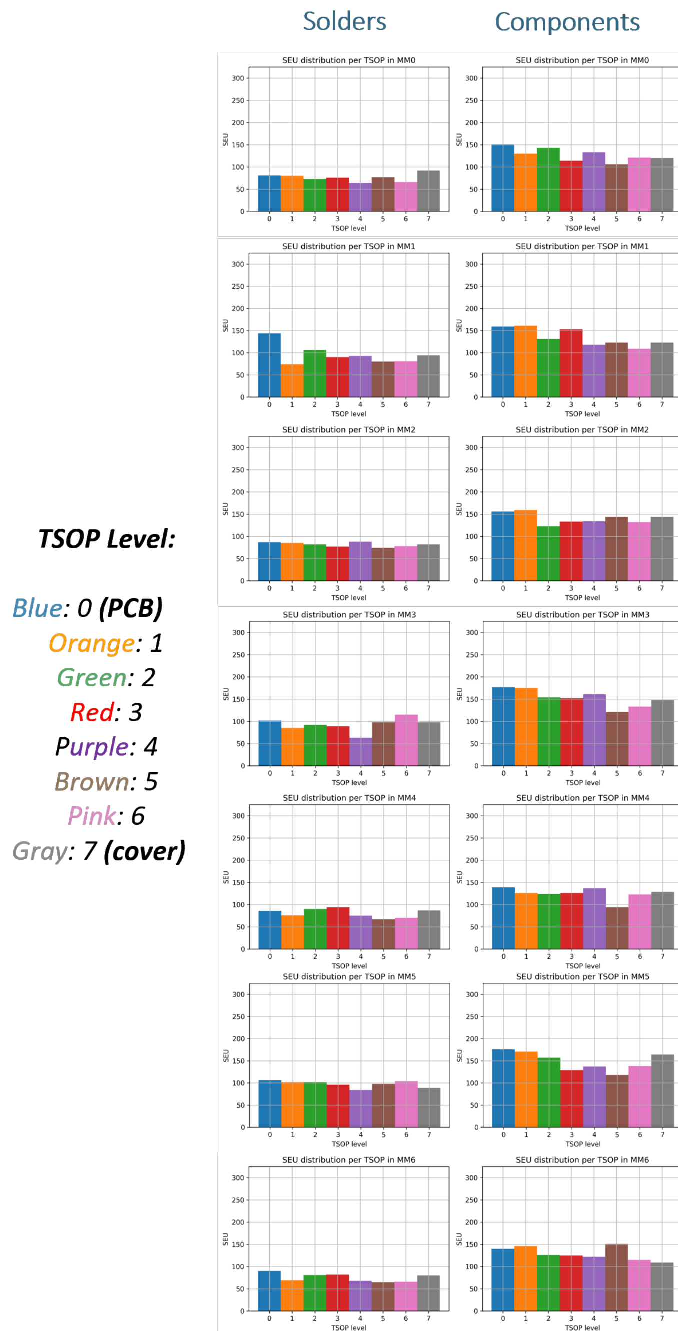

Figure 4.39: SEU distribution per TSOP level in both side of all memory modules

In Figure 4.40 it is possible to identify TSOP levels within individual chips that have been affected by only one correction over all years in orbit. There appears to be no relationship between preferences in TSOP levels affected by more SEUs over al ICs/cubes as already seen in Figure 4.38 and 4.39. Even more evident in this graph is the isotropy of SEUs on both sides of each MM boards with the relative differences.

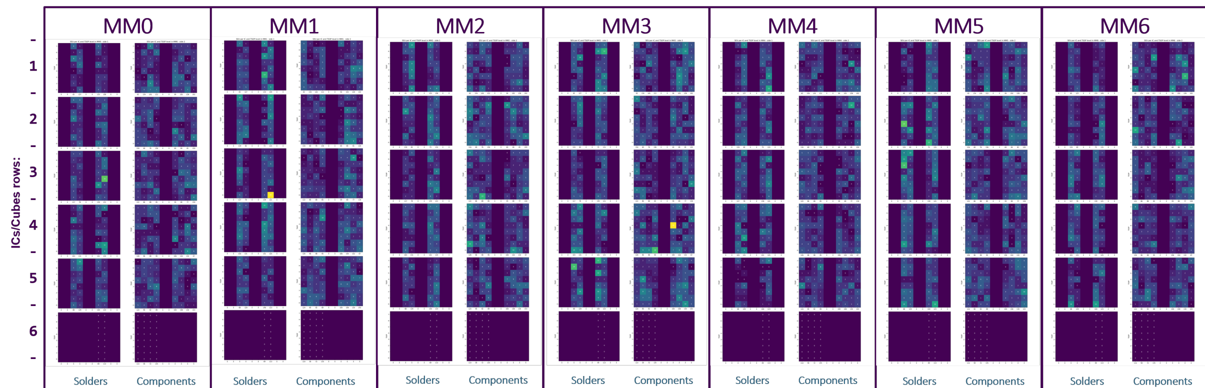

Figure 4.40: SEU distribution per ICs and TSOP levels in both side of all memory modules matrix

4.5. SBC Analysis

4.5.1. Cumulative SBC over time

The distribution over time of SBCs is reported in Figure 4.41: the behaviour over time appears to be similar in all modules except for MM1 due to the usual IC121/TSOP0 anomaly, which maintains steady growth throughout the entire time window despite some of the infomation of this phenomenon being lost for the usual reason related to 128 entries occupied by leakage phenomena. Apart from that, no relation with the seasonal variation of the SSMM TRP is evident as per Satellite A.

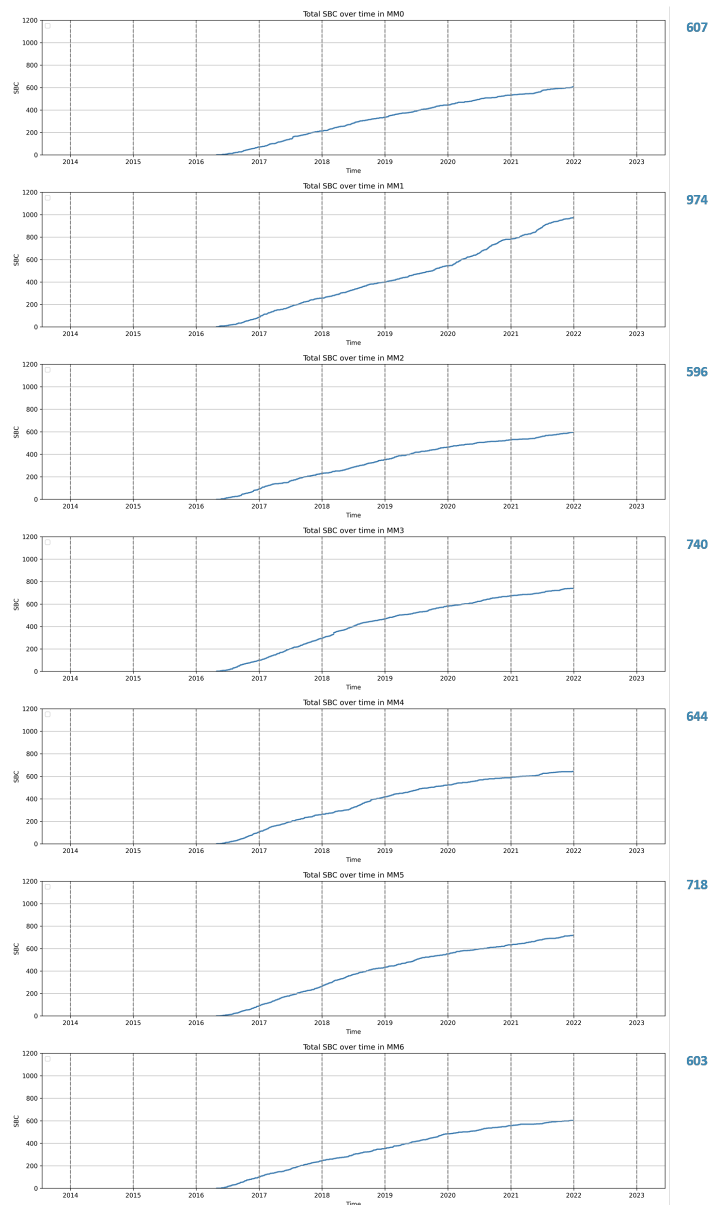

Figure 4.41: Cumulative SBC over all memory modules

4.5.2. SBC ICs/TSOPs Geometrical Distribution

In Figures 3.47 and 3.48 the distribution of SBCs over 5 years per IC/cube and TSOP level is reported. High number of SBC events in IC121/TSOP0, same IC/cube affected by several M-S EWCs.

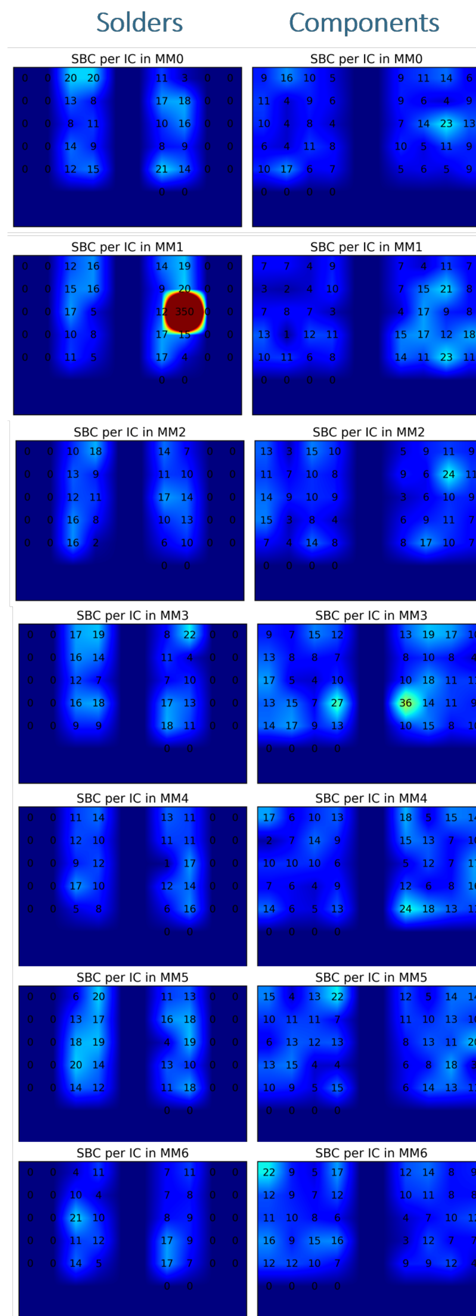

Figure 4.42: SBC distribution per IC in all memory modules (MAX_SBC_per_IC= 36 on MM3 excluding the critical IC/cube for which the value is 350)

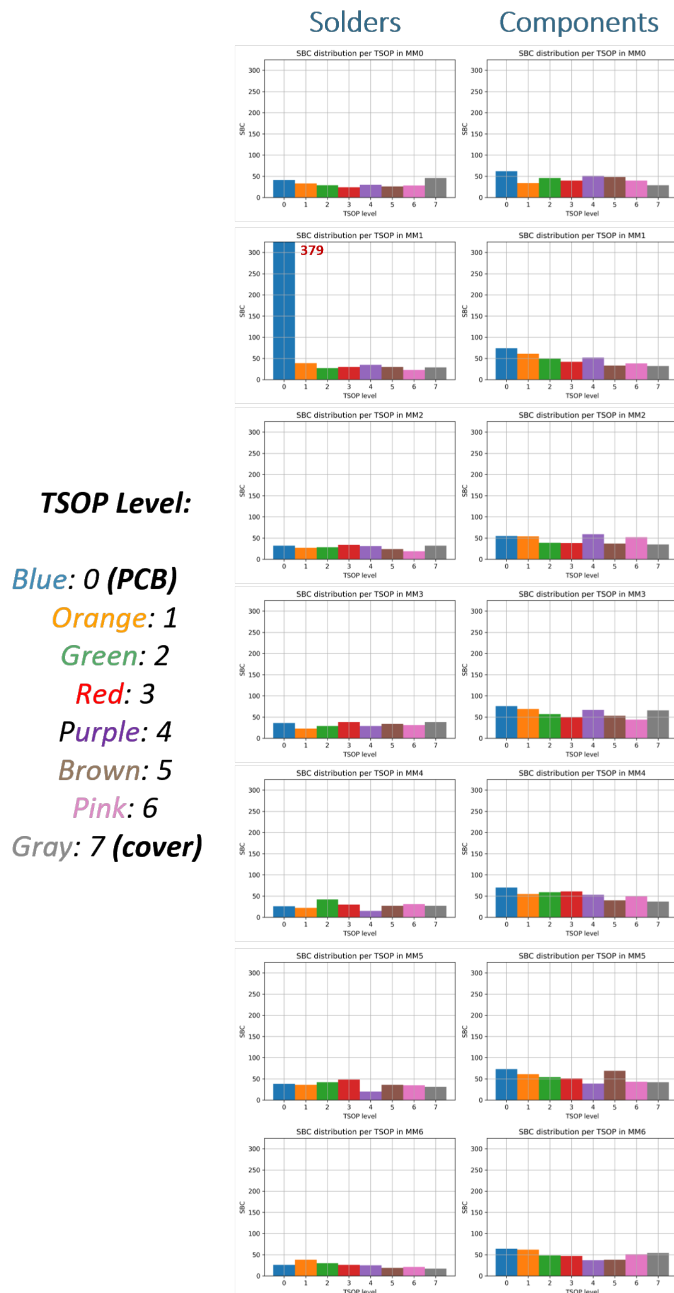

Figure 4.43: SBC distribution per TSOP level in both side of all memory modules

4.6. BOS Analysis

4.6.1. BOS over time

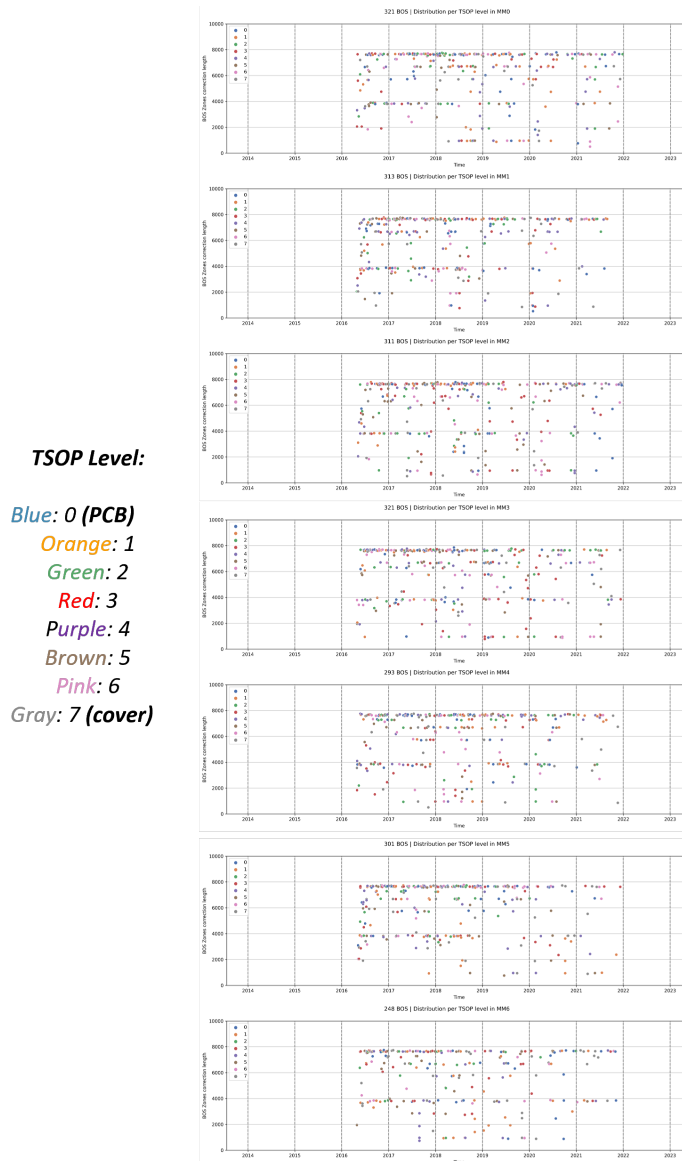

Figure 4.44: Distribution of BOS zones correction length over time per memory module

In Figure 4.45, the number of BOS increases linearly over time for the first 3 years, still no relation with the seasonal variation of the SSMM TRP, as per Satellite A SSMM.

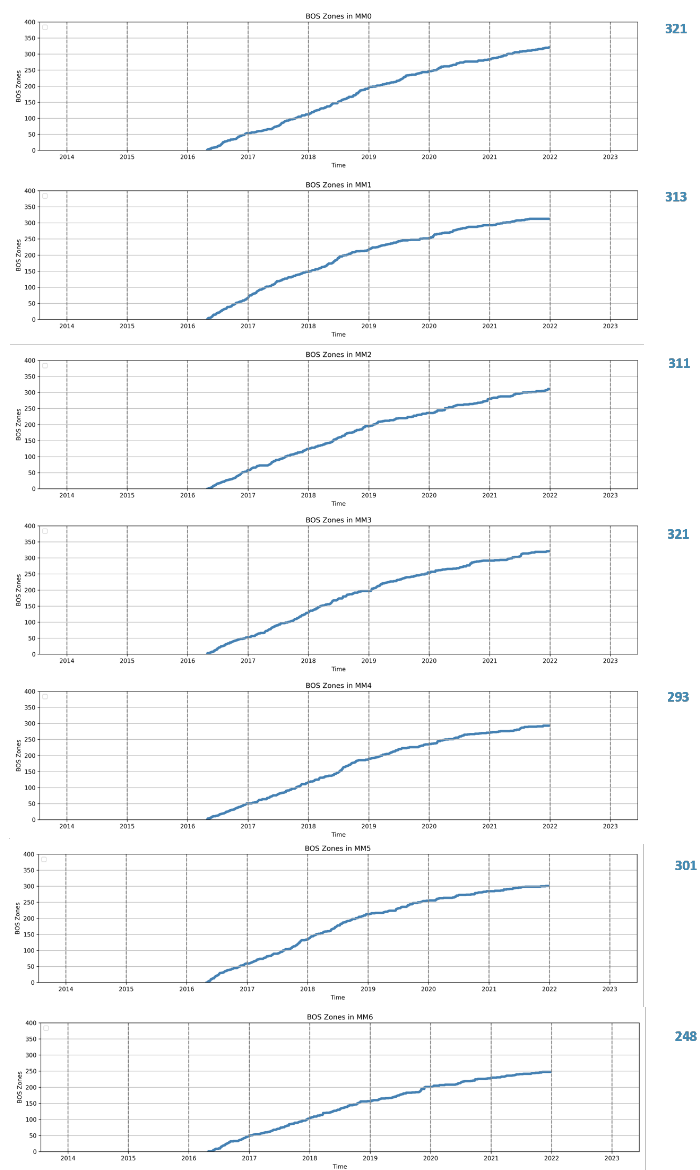

Figure 4.45: Cumulative number of BOS zones over time in all memory modules

4.6.2. BOS zones ICs/TSOPs Geometrical Distribution

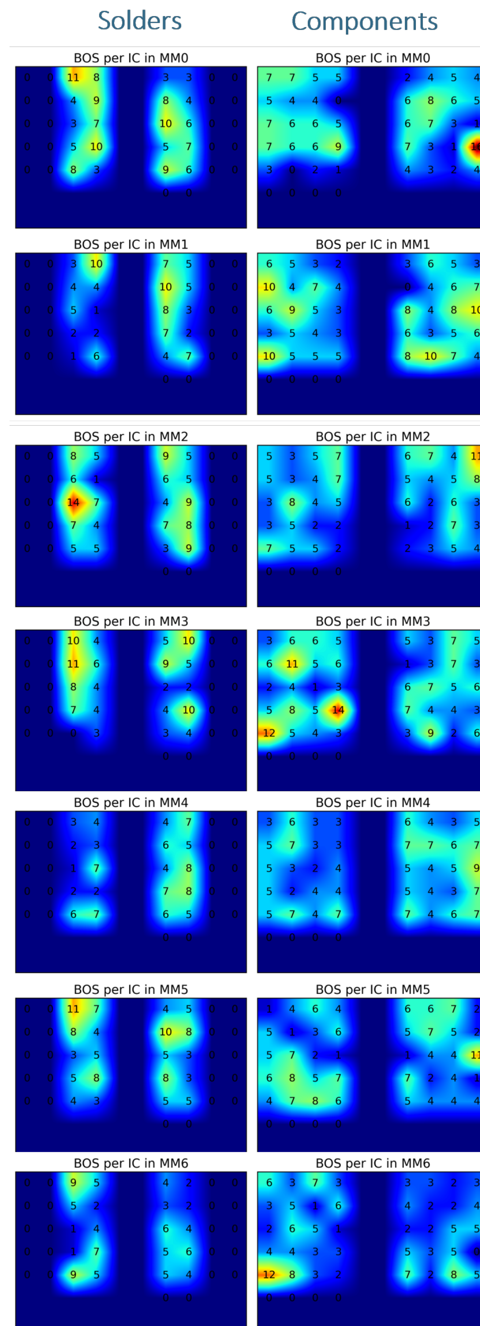

Figure 4.46: BOS zones distribution per IC in all memory modules (MAX_BOS_per_IC= 16 on MM0)

Again, for this second satellite, the distribution of BOSs is homogeneous with respect to the 2 faces of each memory module PCBs, no visible BOS accumulation in the IC121/TSOP0 highlighted above.

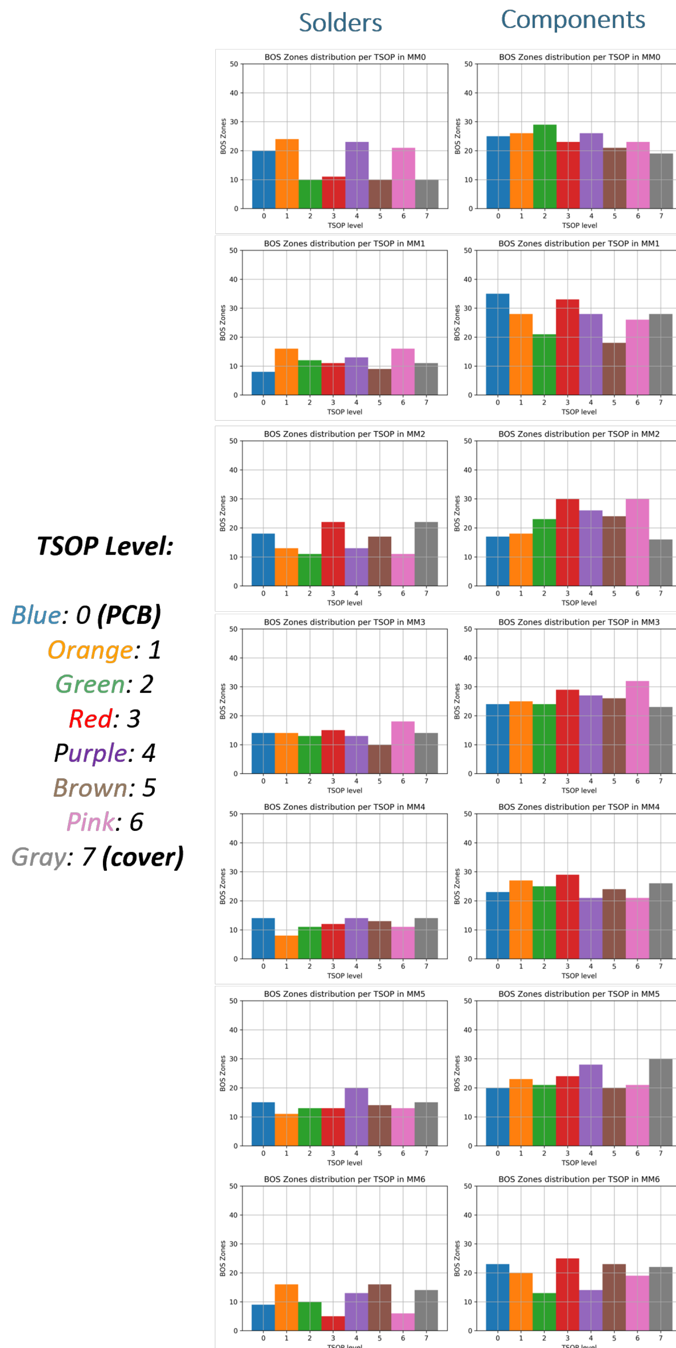

Figure 4.47: BOS zones distribution per TSOP level in all memory modules

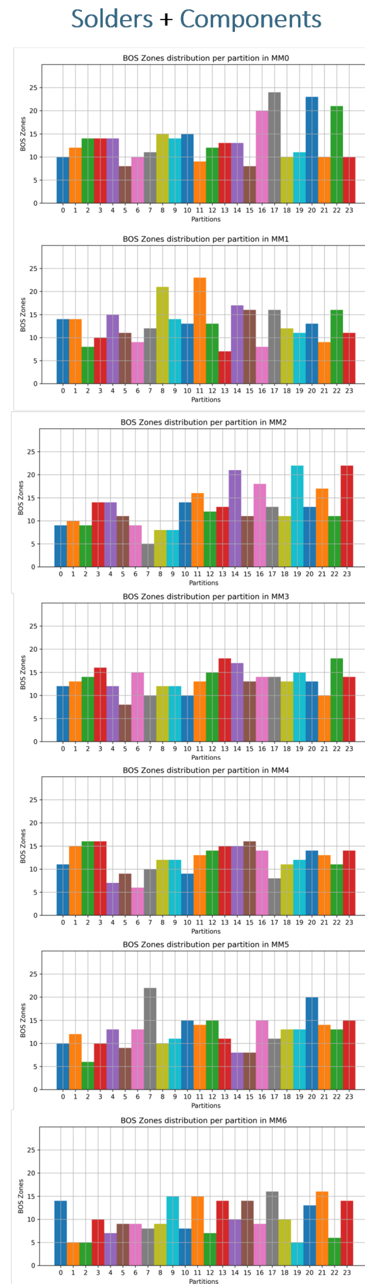

Figure 4.48: BOS zones distribution per partition in all memory modules

4.6.3. BOS zones characteristics

Again, as per Satellite A, there are "clusters" of corrections that are centered on the same location across all MM boards. The most frequent "cluster" is the same as in the other SSMM on Satellite A consisting in three peaks, with the maximum peak around 7650 corrections. As already said, this behaviour can be related to the "page" dimension of 2048 bytes of the TSOP levels composing the ICs. ICs/TSOPs used on the two SSMM

are the same.

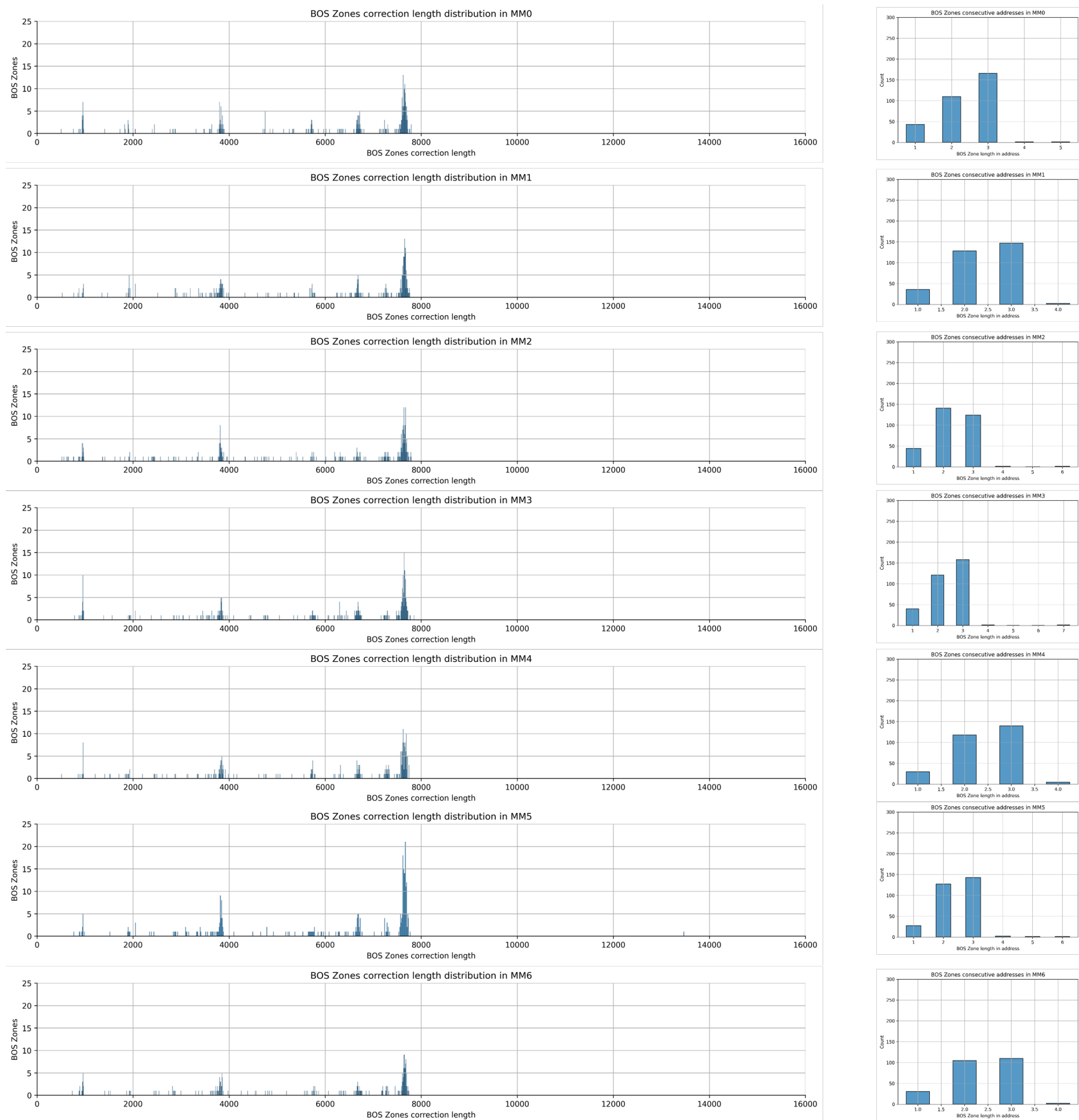

Figure 4.49: BOS zones correction length distribution and address length distribution in all memory modules

4.7. Statistics & Summary for SSMM Satellite B

In the following table in Figure 4.50, the cumulative number of all types of phenomena over roughly 5 and a half years are reported. The number of phenomena appeared inside a BOS zone are obtained, as per Satellite A, verifying that the address affected by leakage

or radiation is in the same IC/Cube and TSOP level as the BOS and that the address is "between" the extreme addresses of the BOS zone.

Satellite B	S-S EWC	M-S EWC	SEU	SBC	BOS Zones	Hard Error	Partition Parking (HE not recovered by a column power cycle)	S-S EWC found in BOS Zones (before and after in time)		M-S EWC found in BOS Zones (before and after in time)		SEU found in BOS Zones		SBC found in BOS Zones	
MM0	530	99	1627	607	321	25	5	12	2.3 %	3	3.0 %	45	2.8 %	27	4.4 %
MM1	662	325	1839	974	313	11	2	12	1.8 %	11	3.4 %	32	1.7 %	26	2.7 %
MM2	603	110	1778	596	311	10	1	1	0.2 %	1	0.9 %	32	1.8 %	13	2.2 %
MM3	692	101	1963	740	321	9	0	8	1.2 %	9	8.9 %	42	2.1 %	41	5.5 %
MM4	666	95	1643	644	293	19	0	8	1.2 %	8	8.4 %	42	2.6 %	30	4.7 %
MM5	527	103	1971	718	301	8	0	5	0.9 %	6	5.8 %	41	2.1 %	15	2.1 %
MM6	522	91	1635	603	248	7	0	3	0.6 %	0	0.0 %	34	2.1 %	17	2.8 %
Average over all MM PCBs	600.29	132.00	1779.43	697.43	301.14	12.71	1.14	7.00	1.2 %	5.43	4.4 %	38.29	2.2 %	24.14	3.5 %
Total over all MM PCBs	4202.00	924.00	12456.00	4882.00	2108.00	89.00	8.00	49.00		38.00		268.00		169.00	

Figure 4.50: Satellite B SSMM, summary table of all corrections types on all MM boards

From the table in Figure 4.51 the average number per ICs/cubes of the various radiative effects is reported, the highest values are mainly in the Solders faces of all modules, while the temperature-influenced leakage effects are instead more distributed on the Components face ("hottest" side).
Particularly noticeable is that now MM0 is no more close to active boards on one side and MM6 is in an environment heated by other active PCBs of the SSMM that raise their local temperatures (see Figure 4.1). The differences between leakage phenomena in the memory module PCBs are no more pronounced towards MM0-MM2 side, the average number of EWCs (S-S and M-S) in MM0 is similar to MM6, and the highest values are in the core modules that are in contact with only active PCBs (MM1-MM4).

	Average number per IC/Cube				
	S-S EWC	M-S EWC	SEU	SBC	BOS Zones
MM0 Solders Side	8.90	2.05	30.45	12.85	6.45
MM0 Components Side	8.80	1.45	25.45	8.75	4.80
MM1 Solders Side	11.40	13.15	38.10	29.60	4.80
MM1 Components Side	10.85	1.55	26.93	9.55	5.43
MM2 Solders Side	9.90	2.10	32.65	11.35	6.35
MM2 Components Side	10.13	1.70	28.13	9.23	4.60
MM3 Solders Side	10.25	1.30	37.10	12.90	5.55
MM3 Components Side	12.18	1.88	30.53	12.05	5.25
MM4 Solders Side	10.50	1.95	32.25	11.00	4.85
MM4 Components Side	11.40	1.40	24.95	10.60	4.90
MM5 Solders Side	9.05	1.65	39.05	14.30	5.70
MM5 Components Side	8.65	1.75	29.75	10.80	4.68
MM6 Solders Side	7.60	1.80	30.05	10.10	4.45
MM6 Components Side	9.25	1.40	25.85	10.03	3.98

Figure 4.51: Satellite B SSMM, average number per IC/cube of all corrections types, divided per solders and components sides

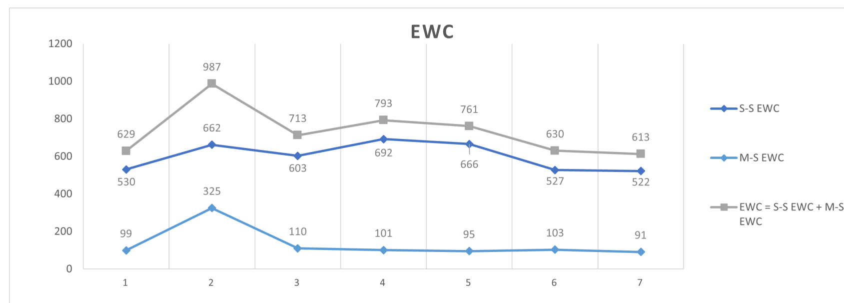

Figure 4.52: Satellite B SSMM, total EWCs over all MM boards

Now the number of EWCs follows a more flat pattern (excluding the anomaly on MM1) across the memory module PCBs. Previously, in the SSMM on Satellite A, the first modules (MM0..MM4) were the "hottest" ones among the whole array of PCBs, in the case of Satellite B, the temperature profile is not certaily the same one due to the active PCBs re-arrangement just after its launch. Differences in internal thermal environment of SSMM is compatible with the observed data, in terms of EWC proliferation across MM boards and growth trends in time.

It is expected a lower temperature toward MM0 and a slightly higher temperature in surroundings of MM6, influencing of course also the near MM5 since it is next to active boards.

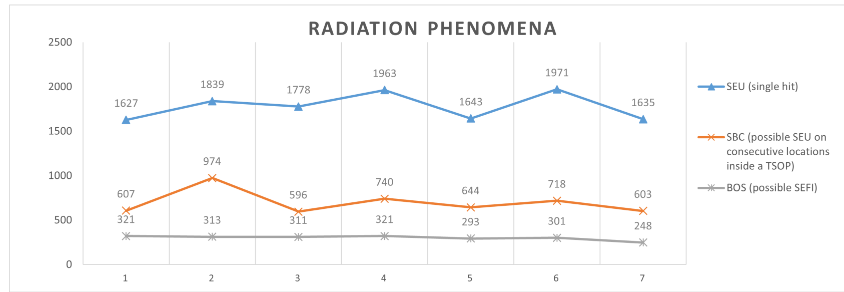

Figure 4.53: Satellite B SSMM, radiation phenomena in all MM boards

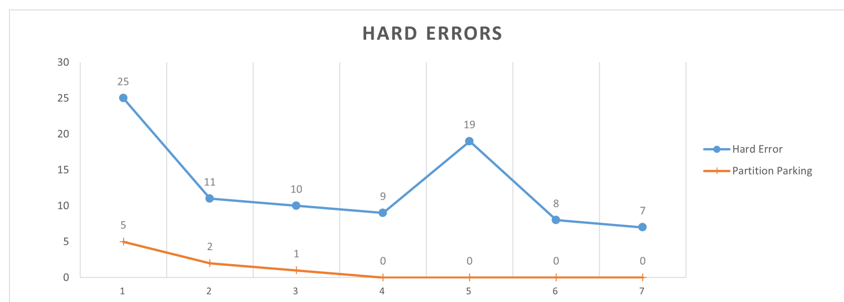

Figure 4.54: Satellite B SSMM, HEs over all MM boards

Note: regarding the anomaly occurred in the MM1 boards, looking at all the corrections occurred in the IC121/TSOP0, the origin of this event dates back between 2019/08/18 15:29 (last TM(6,6) acquisition of the day) to 2019/08/19 08:04 (first TM(6,6) acquisition of the day), from that time on, the rate of appearance of EWCs, especially M-S EWCs, increases significantly.
These generated EWCs are characterized by low activation over time, this makes them barely detectable in the TM(3,25).
In addition, no BOS occurred in that level of TSOP under examination (looking only at the TM(6,6)), but a large number of SBCs occurred progressively for almost a year after this period.

5 | Time Series Analysis

5.1. Introduction on time series analysis

A time series can be defined as a finite realization of a stochastic process, where a stochastic process is an infinite sequence of random variables. Essentially, a time series is a sequence of data points that are indexed or listed in the order they are obtained in time. It can be derived from any variable that undergoes changes over time. Typically, a time series consists of a collection of successive equally spaced points in time or is resampled at a constant frequency to create a sequence of discrete-time data.
Time series analysis comprises methods for analyzing data in order to extract meaningful statistics of several orders and other characteristics of the phenomenology or process represented by the data themselves.

The methods for time series analysis may be divided into two classes: time-domain and frequency-domain. The former involve auto-correlation and cross-correlation analysis, the latter include the spectral analysis. Additionally, time series analysis techniques may be divided into parametric and non-parametric methods. The parametric approaches assume that the underlying process has a specific mathematical structure which can be described using a finite number of parameters.
Then, time series may be divided into "univariate", that consist of a single (scalar) observations recorded sequentially over equal time increments, or "multivariate" that comprises multiple time-dependent variables, where each variable is influenced not only by its own past values but also exhibits interdependencies with other variables.

Models describing and managing time series data can be developed and they have many forms and represent different levels of information and variations in the processes. Three main classes are identified in the literature:

- AutoRegressive (AR) models: they are based on the idea that the current value of the series can be explained as a function of past values and the order "n" of the model determines the number of steps into the past needed to forecast the current

value;

- Integrated (I) models: they represent the differencing operation order between observations and are used to make the time series stationary (i.e., data values are replaced by the difference between the actual values and the previous values);
- Moving Average (MA) models: they represent the influence that the residual error has with respect to the observation and the order "m" of the model is the number of considered "lags" into the past and the number of parameters in the MA model.

In general, these model classes are based on a linear dependence between an observation sample and previous data points. Combinations of these categories also exist, leading to the general concepts of AutoRegressive Moving Average (ARMA) and AutoRegressive Integrated Moving Average (ARIMA) models [6].

The fundamental objective behind model identification is to utilize historical data to infer the underlying main structure of the process producing the time series and apply it for making predictions, under the intuitive assumption that past patterns may be replicated in future occurrences, as they depend on the same phenomenology.

In this thesis, the Box-Jenkins method [7] is used to study the univariate time series related to daily "EWCs activation" in SDRAM orbital devices subjected to radiation and thermal lever, as discussed in Chapter 3.3.1. The purpose of this analysis is to obtain a model that is able to reflect the cumulative activation pattern of EWCs on a memory module so that predictions can be made about the number of active cells on different time scales.

Specifically, the model identification process can be outlined as follows:

1. data gathering and preliminary analysis;
2. data cleaning, interpolation and transformation;
3. selection of the model class and determination of the model complexity;
4. parameter estimation using prediction error techniques;
5. analysis of the achieved results on the training data;
6. analysis of the achieved results on unseen data (validation);
7. repeat the same procedure on weekly resampled data;

8. repeat the same procedure on monthly resampled data.

5.2. Model describing the daily activation of EWCs

First of all, the analysis focuses on the daily activation of EWCs on MM1 of Satellite A SSMM. It is one of the MM boards most affected by this leakage phenomenon in the entire array.
The daily number of active EWCs is obtained by counting the total number of addresses identified as certified EWCs (i.e. both S-S and M-S types, see discussion in Chapter 3 and 4 as they are produced by the same phenomenology) that experienced at least one correction on the same day. Figure 5.1 shows on the x-axis the days and on the y-axis the EWC addresses, in order of first appearance as in the descending arrow reported in the left-hand side of the figure. This kind of graphs for all the memory modules of Satellite A and Satellite B SSMM are reported in Appendix A and Appendix B, respectively. Hereafter, only MM1 is reported as example of the elaboration and for the next discussion.

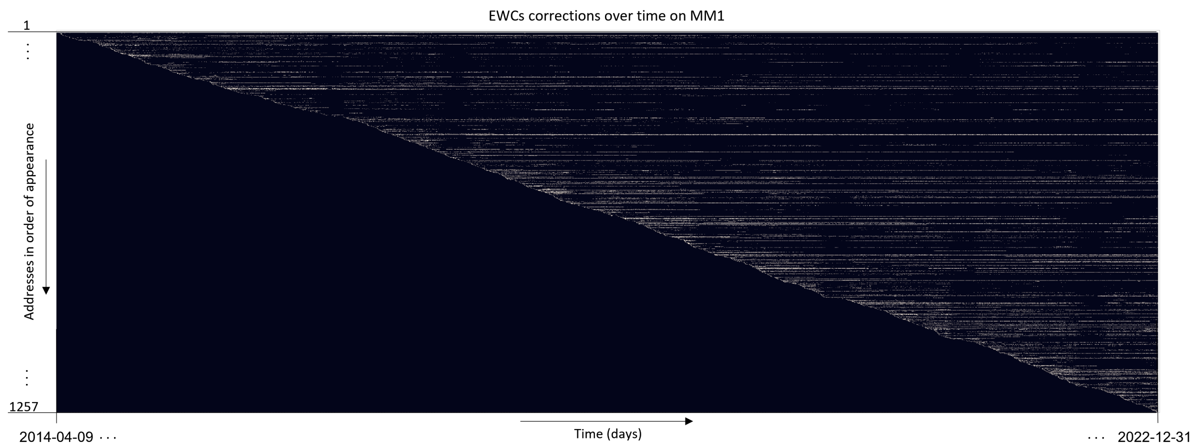

Figure 5.1: EWCs addresses re-occurrences over time identified in Satellite A SSMM MM1

Figure 5.1 shows also the day-by-day correction occurrences of each individual address classified as a EWC on MM1, from their first appearance on: there are 1257 addresses in total. Any white point shows whether the corresponding address is corrected, at least one time on the corresponding day. Both the linear growth trend over time of the EWCs (decreasing diagonal of their first appearances) and their activation in leakage state may be appreciated (for example, a reduction of their leakage during lower temperature periods of the SSMM enviroment in each "year eclipse seasonal period", appearing as vertical "shadow bands").

Some different behaviors of the EWCs appear: some cells show a temporary activity, lasting only for a brief period of time, while other ones undergo permanent correction, although their activity reduces during the "orbital eclipses season" period. Additionally, certain cells persistently experience leakage, independent of any specific time period.

The number of EWCs in leakage and corrected over each day on MM1, are shown in Figure 5.2. This is the time series that will be used for the subsequent analysis and model discussion.

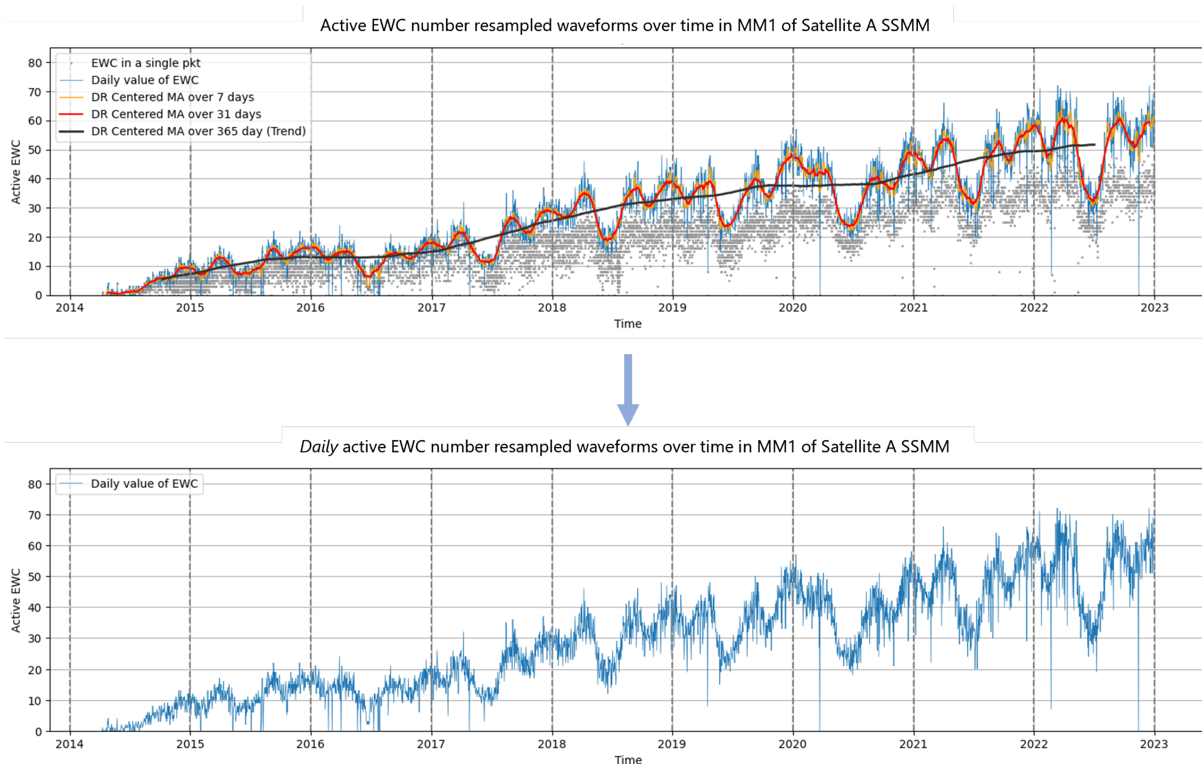

Figure 5.2: Daily active EWCs over time in SSMM MM1 board of Satellite A (y(t): 3189 samples)

5.2.1. Data Pre-processing and preliminary analysis

Before applying any identification and estimation of ARMA model or any other statistical analysis to the time series, it is important to visually inspect the data. This step is crucial to identify any patterns or irregularities that may impact the results of the following analysis.

Visually inspecting the original data in Figure 5.2, some outliers can be noticed (ver-

tical dot lines). These outliers must be removed since they badly affect the modelling process. The presence of these outliers is justified by the fact that some TM(6,6) packets were excluded from the statistical analysis in previous chapters due to several reasons:

- SSMM equipment shutdown (and subsequent restart) due to satellite operations or other different reasons: for this reason the first 1000 samples (roughly two and a half years) were excluded from the following analysis;
- the occurrence of HEs on the MM board, captured in some moments of the analysed time-frame TM(6,6) packet instance and producing a "fake" series of EWC addresses, that is simply a signature of the symbols reconstruction ongoing by the scrub process over a period of 27 minutes;
- the presence of other rare SSMM TM structure anomalies (identified during the extraction process to build the EWC census).

A 30-days moving average is employed to identify and eliminate any outlier. More precisely, a sample whose value exceeds by more than three times the standard deviation from the mean over a 30-sample moving window is classified as an outliers and removed. This choice effectively filters out such outliers, as visible in Figure 5.3. Furthermore, to handle the cancelled values, a linear interpolation is used to fill the gaps. The interpolation is performed between the extreme elements of the missing values.

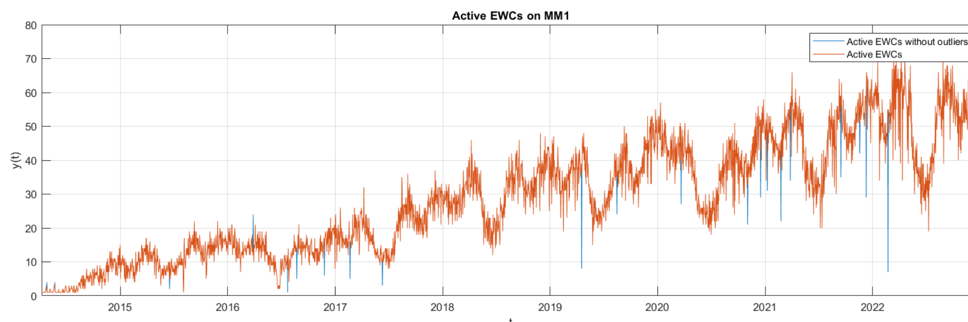

Figure 5.3: Daily Active EWCs over time on MM1 board with/without outliers

The so cleaned activation series of the EWCs exhibits a clear linear trend and annual seasonality that must be removed to construct its model. To coerce the data to assume a stationary characteristic, some transformations are required prior to the final model identification.

Firstly, a logarithmic transformation was applied to the entire original time series in Figure 5.2. This transformation is used to reduce the increasing variance of data and to

equalize the variability over the considered time period.

The original series (9 years of data), is composed by 3189 samples. However, the first 1000 datapoints were excluded, as explained just before.

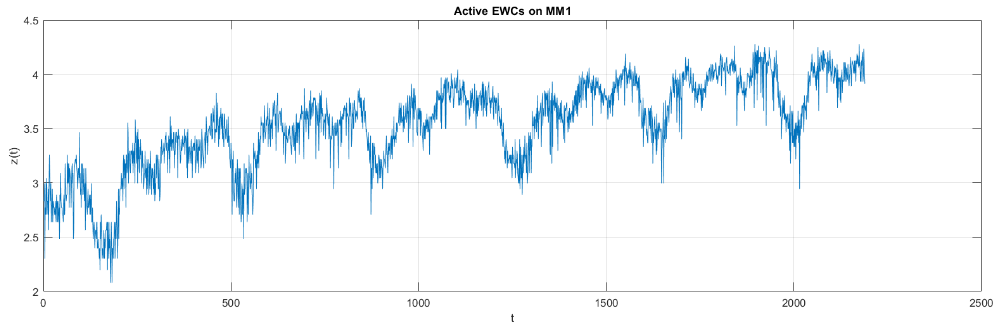

Figure 5.4: Logarithmic transformation $z(t) = ln(y(t))$ (over 2189 = 3189 - 1000 samples)

Then, to remove the linear trend, a first difference is performed, with a step of one day.

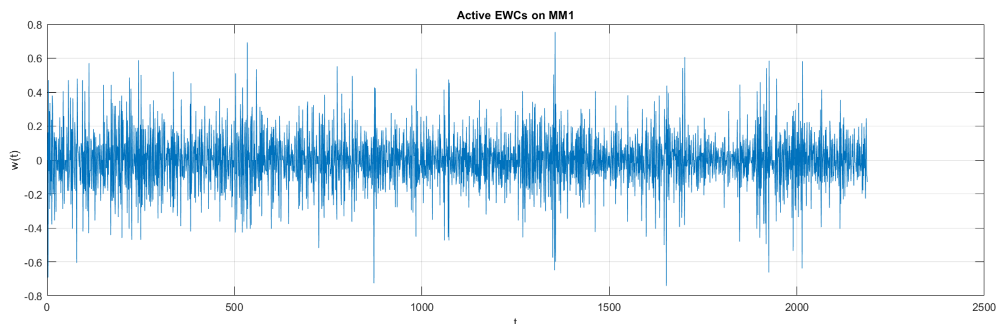

Figure 5.5: First differenced time series $w(t) = z(t) - z(t-1)$ (2188 samples)

Finally, the seasonal difference with step 365 days is performed to remove the annual seasonality.

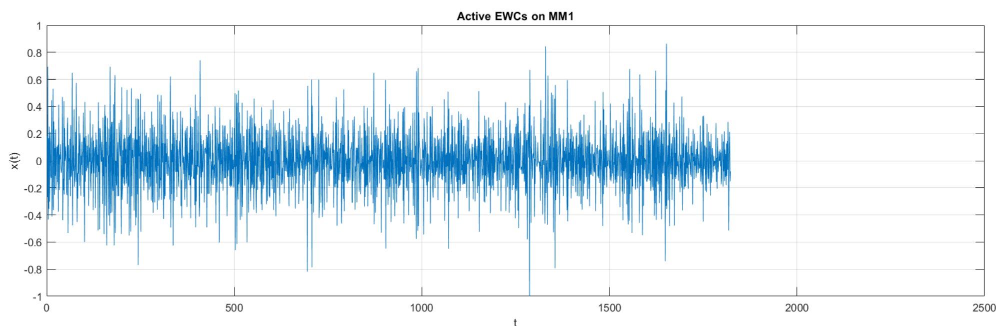

Figure 5.6: Seasonal differenced time series $x(t) = w(t) - w(t-365)$ (1823 samples)

A final step was required: the samples mean ($\bar{x} = -2.7372 \times 10^{-4}$), derived from the transformed time series, is removed to unbias the dataset. Figure 5.2 and Figure 5.6 show respectively the original and the transformed time series obtained after all these operations.

In conclusion, all transformations performed on the original series ($y(t)$), reduced by the first 1000 samples, can be summarised as follows:

$$z(t) = ln(y(t))$$

$$w(t) = z(t) - z(t-1)$$

$$x(t) = w(t) - w(t-365)$$

$$x(t) = x(t) - \bar{x}$$

5.2.2. The idea behind identification of ARMA models

Given the large amount of data available, it is possible to partition the dataset into two distinct parts: a training set and a validation set, as illustrated in Figure 5.7. The model is inferred using the oldest data in the training set, and subsequently its predictive performances are evaluated on the most recent data of the validation set to assess its optimality. The best model is the one that minimizes the performance prediction index within this latter segment of data.

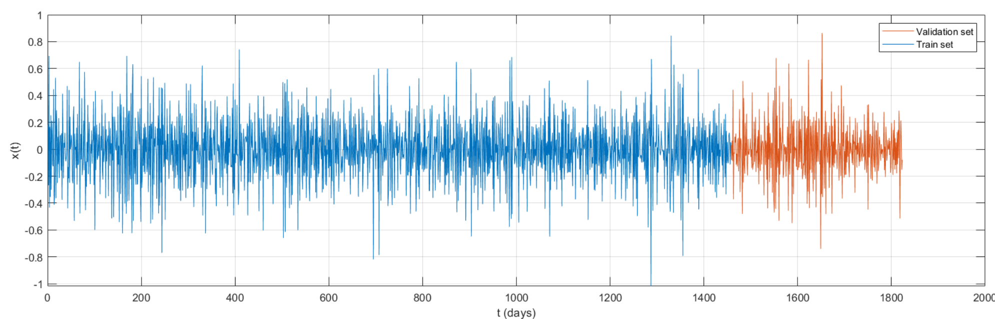

Figure 5.7: Dataset split into training (1824 samples) and validation (365 samples) sets

Now, considering the transformed time series as a realization of an ARMA(n,m) (AR(n), MA(m)) process, the identification of the underlying generating model involves the estimation of the corresponding parameters (a_i for the AR part and/or c_i for the MA part of the model) through the minimization of the prediction errors.

The representation of a generic ARMA(n,m) process in the time domain is:

$$y(t) = 1 + a_1 y(t-1) + \ldots + a_n y(t-n) + e(t) + c_1 e(t-1) + \ldots + c_m e(t-m)$$

where:

- $y(t)$: represents the current observation at time t. It is the dependent variable of the model.
- a_i: are the AR coefficients that measure the influence of lagged observations $y(t-i)$ on the dependent variable $y(t)$. The index i ranges from 1 to n;
- c_i: are the MA coefficients that measure the influence of lagged errors $e(t-i)$ on the dependent variable $y(t)$. The index i ranges from 1 to m;
- $e(t)$: represents the random noise at time t, which constitutes the unexplained part of the model; in this set up it is a "white noise" $e(t) \sim \mathrm{WN}(0, \lambda^2)$;
- $y(t-i)$: indicates the lagged observations that influence the dependent variable $y(t)$;
- $e(t-i)$: represents the lagged noise that influence the dependent variable $y(t)$.

The transfer function representation of the ARMA model can be achieved by employing the delay operator z^{-1}:

$$y(t) = W(z)\varepsilon(t) \quad \text{where} \quad W(z) = \frac{C(z)}{A(z)} = \frac{1 + c_1 z^{-1} + \ldots + c_m z^{-m}}{1 + a_1 z^{-1} + \ldots + a_n z^{-n}}$$

The model identification process aims to determine the appropriate parameter vector $\theta = [a_1, \ldots, a_n, c_1, \ldots, c_m]'$ that minimizes the average squared error over the observed data.

Specifically, given the observations from 1 to N, the objective is to determine the values of θ which minimize the performance index $J(\theta) = \frac{1}{N}\sum_{t=1}^{N} \varepsilon(t)^2$, that is the sampled variance of the prediction error made by the model. In this context, it means finding the value of:

$$\hat{\theta}_N^{(n,m)} = \arg\min_{\theta} J(\theta) = \arg\min_{\theta} \frac{1}{N}\sum_{t=1}^{N}(y(t) - y(t|t-1, \theta))^2$$

where:

- N is the number of available data (in this case $N = 1824$);
- θ is the parameter vector;

- $y(t|t-1,\theta)$ is the one-step predictor obtained from the model $W(z)$ derived from:

$$y(t|t-1,\theta) = \frac{C(z) - A(z)}{C(z)} y(t)$$

- $y(t) - y(t|t-1,\theta)$ represents the prediction error at time t for the given model;

For AR processes, the minimization is carried out involving the least squares formula. However, for MA and ARMA processes, the estimation for θ ($\hat{\theta}_N^{(n,m)}$) is obtained through an iterative approach. This is because the predictor $y(t|t-1,\theta)$ for ARMA models is no longer linear in the parameters. Indeed, the performance index is defined as:

$$J(\theta) = \frac{1}{N}\sum_{t=1}^{N}(y(t) - y(t|t-1,\theta))^2 = \frac{1}{N}\sum_{t=1}^{N}\left(\frac{A(z)}{C(z)}y(t)\right)^2$$

and it shows the unknown parameter also at the denominator. In such cases, $\hat{\theta}_N^{(n,m)}$ is computed using a Newton-like minimization technique.

5.2.3. Model selection and evaluation

Regarding the time series under analysis, an initial guess about the model was deduced by looking at the behavior of the sample AutoCorrelation Function (ACF) (normalized covariance function) and Partial AutoCorrelation Function (PACF) (partial covariance function) associated to the training set, up to lag 50. These graphs are shown in Figure 5.8.

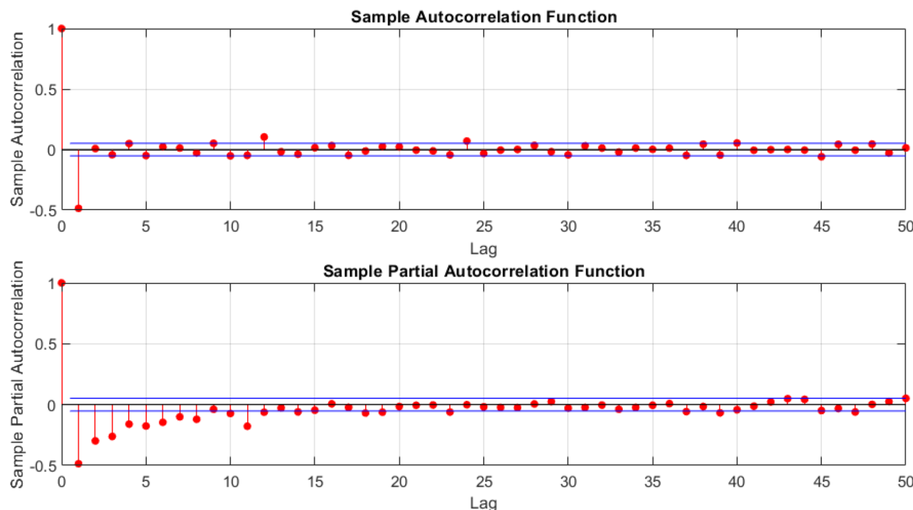

Figure 5.8: Sample ACF and PACF of the training set of data up to lag 50

The sample ACF plot displays the values of autocorrelation against the lag and measures the correlation between an observation in the series and a lagged version of itself, i.e. it represents the correlation between past and present values of the series. It is defined as:

$$\hat{\rho}(h) = \frac{\hat{\gamma}(h)}{\hat{\gamma}(0)}$$

where $\hat{\rho}(h)$ is the sample autocorrelation function at the lag h, $\hat{\gamma}(h)$ is the sample covariance function at lag h obtained from $\hat{\gamma}(h) = \frac{1}{N}\sum_{t=1}^{N-h}(y(t) - \bar{y})(y(t+h) - \bar{y})$ where:

- N is the size of the dataset;
- $y(t)$ is the observation at time t;
- $y(t+h)$ is the observation at time $t+h$;
- $\bar{y}$ is the sample mean of the observations.

The properties of this graph are analyzed through the Anderson Test (whiteness test) to evaluate the residuals obtained from the model that will be selected.

Examining the sample ACF and PACF graphs on the training set, the ACF coefficients cut off after lag 1, while the PACF graph tails off more slowly: the typical behaviour of an MA(1) process is therefore deduced.
The estimated model, identified by fitting an MA(1) model to the training set, has the following transfer function:

$$y(t) = W(z)e(t) = \frac{C(z)}{A(z)}e(t) = e(t) + c_1 z^{-1}e(t) = e(t) - 0.9189z^{-1}e(t)$$

where: $C(z) = 1 - 0.9189z^{-1}$, $A(z) = 1$.

The parameter of the model has been estimated by an iterative approach with a null parameter initialization, i.e. all parameters set to 0 at the beginning.

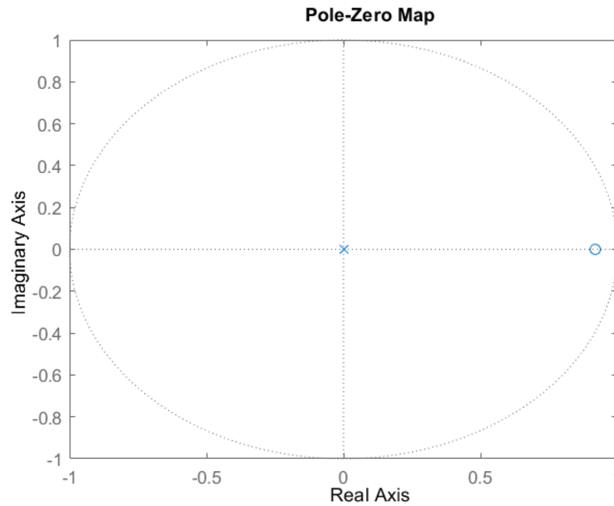

Figure 5.9: pole and zero map of the MA(1) model

With the identified model, the optimal one-step predictor $y(t|t-1, c_1)$ can be computed in the following way:

$$y(t,|t-1,c_1) = \frac{C(z)-A(z)}{C(z)}y(t) = \frac{c_1 z^{-1}}{1+c_1 z^{-1}}y(t) = \frac{-0.9189z^{-1}}{1-0.9189z^{-1}}y(t)$$

The values of the training set and one-step prediction, with their respective anti-transformed values, are reported in the figures below:

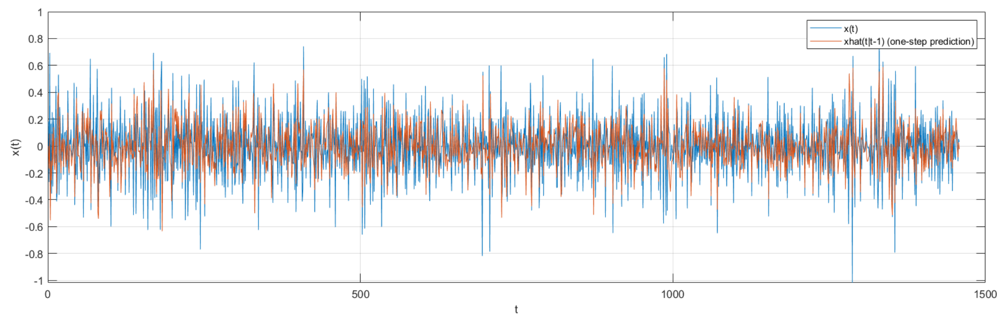

Figure 5.10: One-step prediction of MA(1) compared with the training set

The anti-transformations were carried out on the one-step prediction by inversely repeating the transformations applied to the original series, in the case of daily data:

$$\hat{x}(t) = \hat{x}(t) + \bar{x}$$

$$\hat{w}(t) = \hat{x}(t) + w(t-365)$$

$$\hat{z}(t) = \hat{w}(t) + z(t-1)$$

$$\hat{y}(t) = \exp(\hat{z}(t))$$

The prediction compared with the original data, is reported in Figure 5.11.

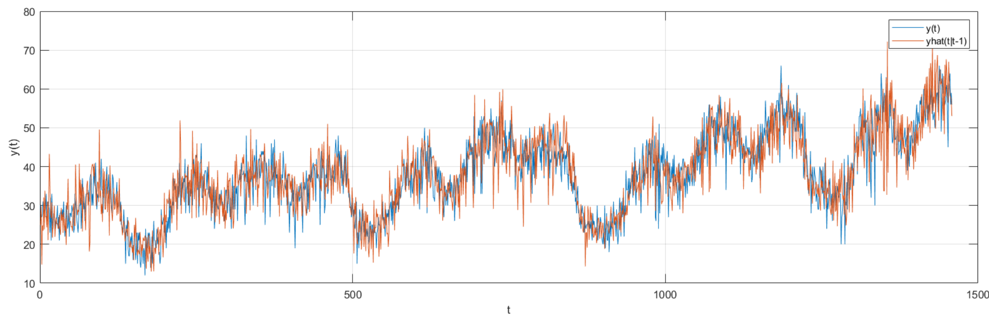

Figure 5.11: One-step prediction of MA(1) compared with the original training set

The corresponding prediction error (residual) $\varepsilon(t) = y(t) - \hat{y}(t) = y(t) - y(t|t-1, c1)$ is reported with its distribution and its ACF and PACF in the following figure.

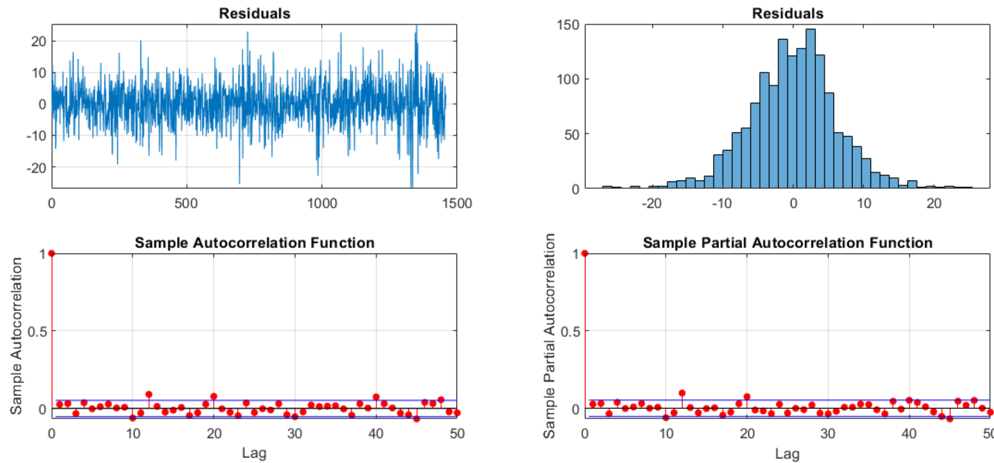

Figure 5.12: One-step predicted error of MA(1) over the original training set

The Anderson Test is performed to assess the whiteness of the residual. This statistical method is important in model checking since it allows to verify if a sequence of data can be interpreted as a "white noise" (i.e. a stationary stochastic process having covariance function $\hat{\gamma}(h)$ null for any $h \neq 0$). By looking at the normalized covariance function up to lag 50, the number correlation coefficients ($\hat{\rho}(h)$) exceeding the 95% ($\alpha = 0.05$) confidence interval is 4: $\frac{4}{50} = 0.08 > \alpha$. The whiteness assumption cannot be accepted.
Considering models with increasing complexity, i.e. by adding both AR and MA terms,

the residuals relative to the training set do not improve sufficiently and continue to fail the Anderson Test.

	mean	**variance**	**RMSE**	**MAE**	**ESR(1)**
ε**(t):**	0.0022	40.1780	6.3364	4.8582	0.3949

Table 5.1: Residual characteristic of the MA(1) model on the training set

The statistics reported in Table 5.1 were calculated as follows:

1. Root Mean Squared Error (RMSE):

$$RMSE = \sqrt{\frac{1}{N}\sum_{t=1}^{N}(y(t) - \hat{y}(t|t-1,\theta))^2}$$

2. Mean Absolute Error (MAE):

$$MAE = \frac{1}{N}\sum_{t=1}^{N}|y(t) - \hat{y}(t|t-1,\theta)|$$

3. Error-to-Signal Ratio (ESR) at prediction step K:

$$ESR(K) = \frac{\text{var}(\epsilon_k(t))}{\text{var}(y(t))}$$

The ESR provides an estimation of the relative error between the residual error of the model and the variance of the observed data. This ratio provides a measurement of the accuracy of the model's predictions relative to the variability of the actual data. If the ESR is low (close to 0), it indicates a better fit of the model to the data and so good prediction capabilities. On the contrary, if the ESR is high (close to 1), it may suggest that the model is unable to adequately capture the structure of the data and therefore it is unable to make reliable predictions.
Nevertheless, the model performances were tested also on the validation set, as reported in figure here below:

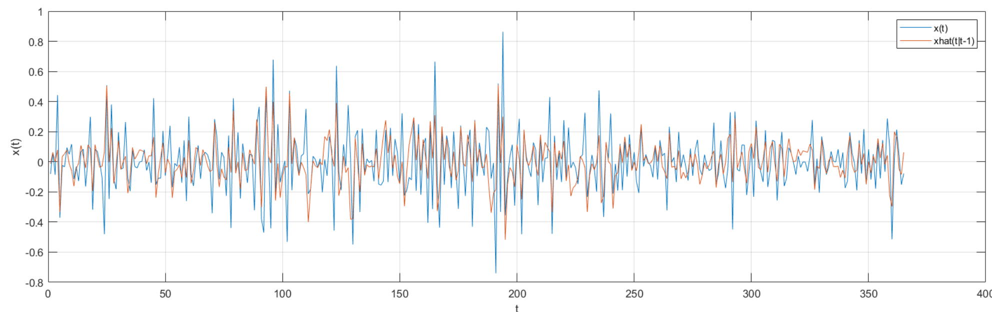

Figure 5.13: One-step prediction of MA(1) compared with the validation set

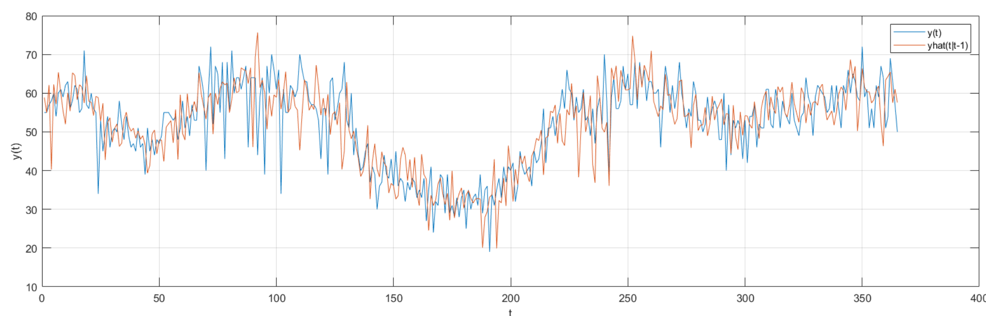

Figure 5.14: One-step prediction of MA(1) compared with the original validation set

The corresponding prediction error (residual) $\varepsilon(t) = y(t) - y(t|t-1, c1)$ is reported with its distribution and its ACF and PACF in the following figure.

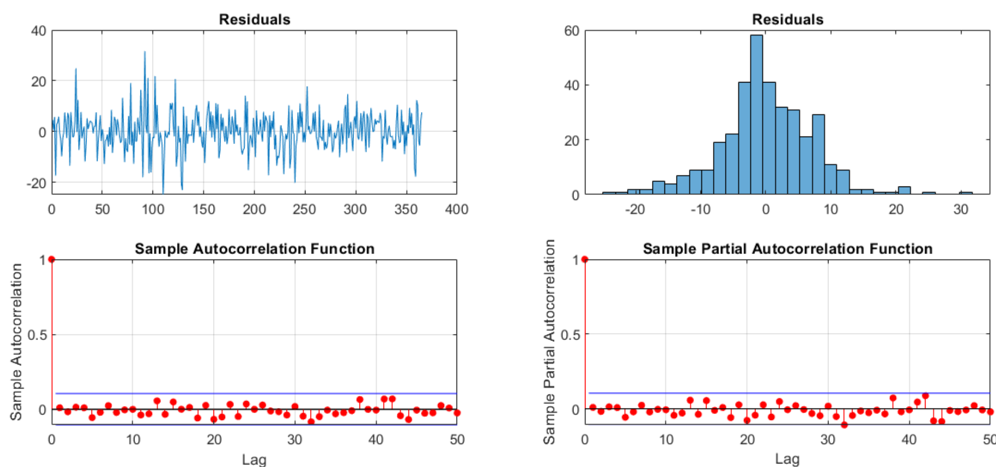

Figure 5.15: One-step predicted error of MA(1) over the original validation set

Despite the fact that on the training data the residual is not exactly a white noise, it seems that the model is able to generalize well on data that were not used for its identification.

	mean	variance	RMSE	MAE	ESR(1)
ε(t):	0.0736	55.1202	7.4145	5.4799	0.4886

Table 5.2: Residual characteristic of the MA(1) model on the validation set

Since the residual obtained from the MA(1) on the training set is not exactly a white noise and we are unable to make significant predictions beyond one day ahead, a grid search approach to find the best-performing model on the training set is performed.

The performance index $J(\theta)$ provides an index of fit of the model, so $\hat{\theta}_N^{(n,m)}$ is the point of local (or global) minimum of $J(\theta)$ (i.e. $J(\hat{\theta}_N^{(n,m)})$ is the index of fit associated with the model of order n, m).
Using $J(\theta)$ directly as an index to get the best model is not always correct. Generally, when a more complex model (i.e. with higher values of n and m) is considered, there are more degrees of freedom, so a lower index of fitting is expected. In other words, the higher the order of the model, the better is data fitting.
There are several methods to select the right level of complexity to avoid overfitting. It is reasonable to consider metrics that take into account not only $J(\theta)$ but also the complexity of the model itself (represented by the number of parameters $n + m$). Single-number scores that are used to determine which of multiple models is most likely to be the best one for a given dataset are:

1. Akaike Information Criterion (AIC):

$$\mathrm{AIC}(n, m) = \frac{2(n+m)}{N} \ln\left(J\left(\hat{\theta}_N^{(n,m)}\right)\right)$$

2. Bayesian information criterion (BIC):

$$\mathrm{BIC}(n, m) = -2\ln\left(J\left(\hat{\theta}_N^{(n,m)}\right)\right) + (n+m)\ln(N)$$

AIC and BIC are statistical metrics utilized to compare the quality of different models and peform a quantitative choice. AIC measures the goodness of fit of a specific model by balancing the fitting error against the number of parameters, while BIC penalizes models with a larger number of parameters. The model with the lowest AIC or BIC values are considered the most favourable choice. As shown in Figure 5.16, by estimating all the parameters of the models with n and m ranging from 0 to 12 and employing these two

metrics, the recommended models obtained are:

- min AIC: ARMA(6,10)
- min BIC: MA(1) (confirming the initial choice)

```
ARMA(0,1): AIC: -9.114035e+02 - BIC: -9.061187e+02 - FPE: 3.133617e-02
ARMA(0,2): AIC: -9.117070e+02 - BIC: -9.011374e+02 - FPE: 3.132964e-02
ARMA(0,3): AIC: -9.104444e+02 - BIC: -8.945899e+02 - FPE: 3.135679e-02
ARMA(0,4): AIC: -9.089609e+02 - BIC: -8.878216e+02 - FPE: 3.138871e-02
ARMA(0,5): AIC: -9.080454e+02 - BIC: -8.816213e+02 - FPE: 3.140843e-02
ARMA(0,6): AIC: -9.078445e+02 - BIC: -8.761356e+02 - FPE: 3.141275e-02
ARMA(0,7): AIC: -9.059815e+02 - BIC: -8.689877e+02 - FPE: 3.145292e-02
ARMA(0,8): AIC: -9.045819e+02 - BIC: -8.623033e+02 - FPE: 3.148313e-02
ARMA(0,9): AIC: -9.029174e+02 - BIC: -8.553540e+02 - FPE: 3.151909e-02
ARMA(0,10): AIC: -9.018904e+02 - BIC: -8.490422e+02 - FPE: 3.154130e-02
ARMA(0,11): AIC: -9.035963e+02 - BIC: -8.454632e+02 - FPE: 3.150442e-02
ARMA(0,12): AIC: -9.037205e+02 - BIC: -8.403027e+02 - FPE: 3.150174e-02
ARMA(1,0): AIC: -4.659778e+02 - BIC: -4.606930e+02 - FPE: 4.253288e-02
ARMA(1,1): AIC: -9.118161e+02 - BIC: -9.012465e+02 - FPE: 3.132730e-02
ARMA(1,2): AIC: -9.145645e+02 - BIC: -8.987100e+02 - FPE: 3.126830e-02
ARMA(1,3): AIC: -9.101366e+02 - BIC: -8.889973e+02 - FPE: 3.136341e-02
ARMA(1,4): AIC: -9.084033e+02 - BIC: -8.819792e+02 - FPE: 3.140072e-02
ARMA(1,5): AIC: -9.070880e+02 - BIC: -8.753791e+02 - FPE: 3.142906e-02
ARMA(1,6): AIC: -9.059251e+02 - BIC: -8.689313e+02 - FPE: 3.145414e-02
ARMA(1,7): AIC: -9.043475e+02 - BIC: -8.620690e+02 - FPE: 3.148819e-02
.
.
.
ARMA(6,8): AIC: -9.103001e+02 - BIC: -8.363126e+02 - FPE: 3.135991e-02
ARMA(6,9): AIC: -9.014324e+02 - BIC: -8.221601e+02 - FPE: 3.155123e-02
ARMA(6,10): AIC: -9.397933e+02 - BIC: -8.552361e+02 - FPE: 3.073193e-02
ARMA(6,11): AIC: -9.374727e+02 - BIC: -8.476307e+02 - FPE: 3.078089e-02
ARMA(6,12): AIC: -9.310389e+02 - BIC: -8.359121e+02 - FPE: 3.091702e-02
.
.
.
```

Figure 5.16: Model order selection based on grid search performed on daily dataset

At this point, the same analysis done for MA(1) is repeated on the same training and validation set using the new ARMA(6,10) estimated model. This estimated model has the following transfer function:

$$y(t) = W(z)e(t) = \frac{C(z)}{A(z)}e(t)$$

with:

$$C(z) = 1 - 1.233z^{-1} + 2.033z^{-2} - 2.15z^{-3} + 2.137z^{-4} - 1.724z^{-5} + 1.14z^{-6}$$

$$-0.9466z^{-7} + 0.1559z^{-8} - 0.161z^{-9} + 0.04852z^{-10}$$

$$A(z) = 1 - 0.3454z^{-1} + 1.731z^{-2} - 0.5773z^{-3} + 1.572z^{-4} - 0.2043z^{-5} + 0.8134z^{-6}$$

The parameters of such model have been estimated by the iterative approach with a null parameter initialization (all parameters set to 0 at the beginning).

Given the identified model, the one-step predictor $y(t|t-1, \hat{\theta}_N^{(6,10)})$ can be computed. In this case, the optimal one-step predictor is obtained as follows:

$$y(t, |t-1, c_1) = \frac{C(z) - A(z)}{C(z)} y(t)$$

with $C(z)$ and $A(z)$ defined previously.

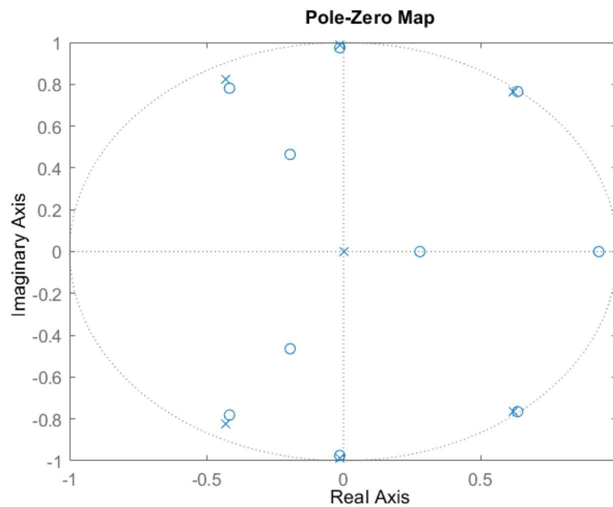

Figure 5.17: Pole and zero map of the ARMA(6,10) model

The values of the training set and one-step prediction, with their respective anti-transformed values, are reported in the figures below.

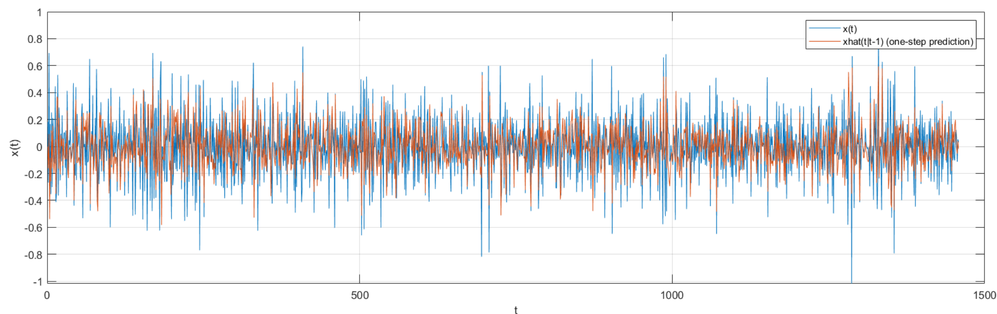

Figure 5.18: One-step prediction of ARMA(6,10) compared with the training set

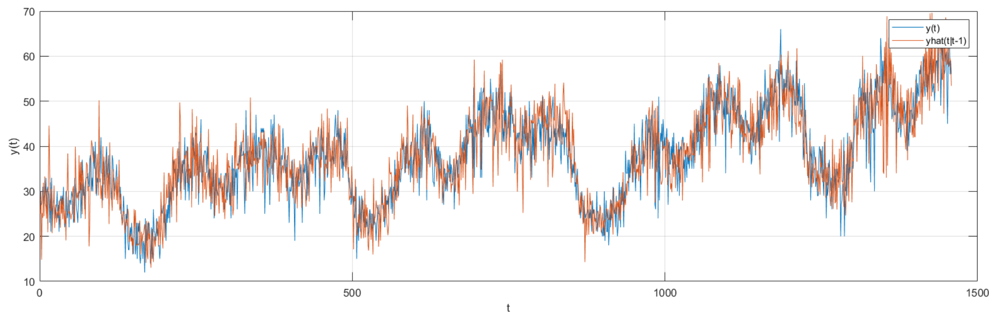

Figure 5.19: One-step prediction of ARMA(6,10) compared with the original training set

The corresponding prediction error (residual) $\varepsilon(t) = y(t) - \hat{y}(t) = y(t) - y(t|t-1, \hat{\theta}_N^{(6,10)})$ is reported with its distribution and its ACF and PACF in the following figure.

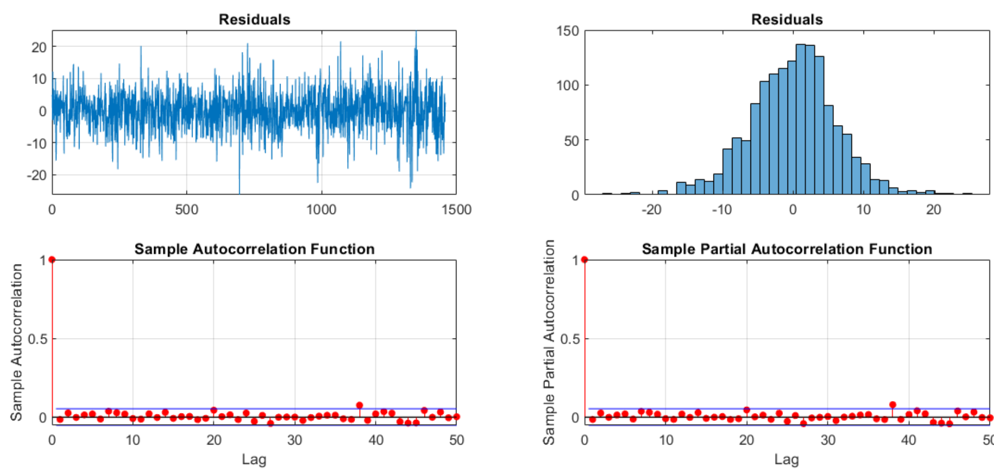

Figure 5.20: One-step predicted error of ARMA(6,10) over the original training set

	mean	**variance**	**RMSE**	**MAE**	**ESR(1)**
ε**(t):**	0.0093	38.7333	6.2215	4.8119	0.3807

Table 5.3: Residual characteristic of the ARMA(6,10) model on the training set

The Anderson Test is performed again to assess the whiteness of the residual. By looking at the normalized covariance function up to lag 50, the number of points exceeding the 95% confidence interval is 1, so $\frac{1}{50} = 0.02 < \alpha$. Now the whiteness assumption can be accepted.

The model was finally tested also on the validation set:

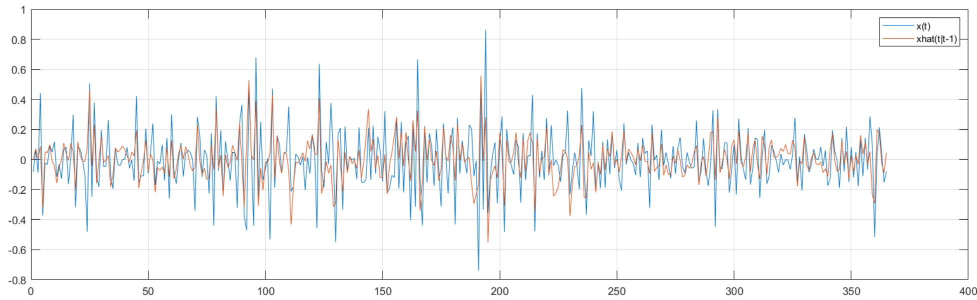

Figure 5.21: One-step prediction of ARMA(6,10) compared with the validation set

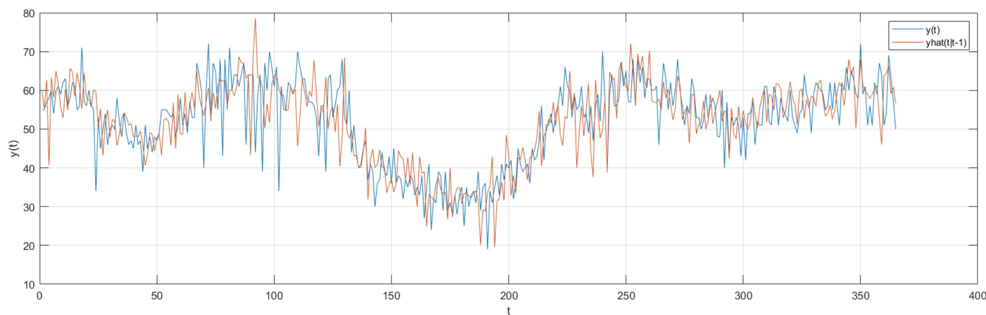

Figure 5.22: One-step prediction of ARMA(6,10) compared with the original validation set

The corresponding prediction error (residual) $\varepsilon(t) = y(t) - y(t|t-1, \hat{\theta}_N^{(6,10)})$ is reported with its distribution and its ACF and PACF in the following figure.

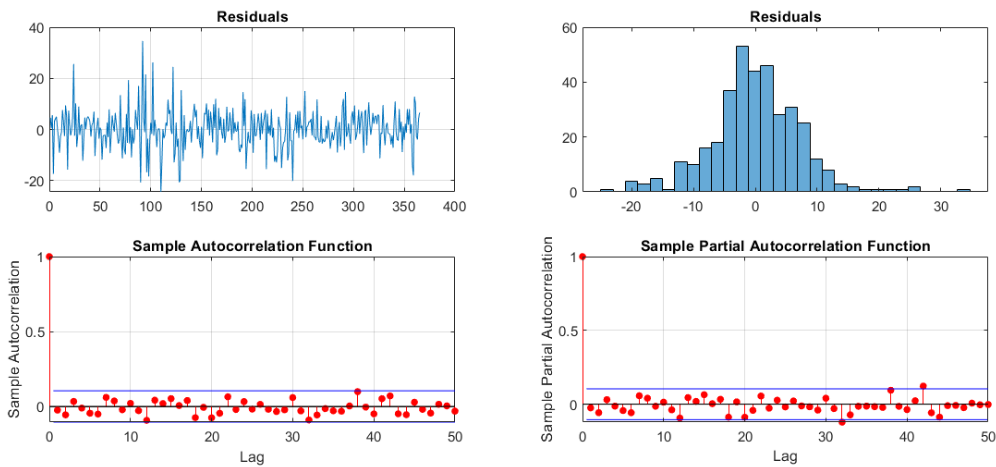

Figure 5.23: One-step prediction of ARMA(6,10) compared with the original validation set

	mean	variance	RMSE	MAE	ESR(1)
ε(t):	0.0753	56.2138	7.4877	5.5282	0.4983

Table 5.4: Residual characteristic of the ARMA(6,10) model on the validation set

Applying again the Anderson Test to the residuals obtained from the ARMA(6,10) model reveals that they exhibit characteristics of "white noise". However, as expected, the ARMA(6,10) model shows better performances on the training data compared to the simpler one.

5.2.4. Long-term prediction performance

Regarding the MA(1) model, predictions at steps greater than 1 immediately degenerate into the mean of the transformed time series, which is basically zero. All the predictors from $y(t|t-2)$ to $y(t|t-10)$ are the same: they are all zero and indistinguishable from each other.

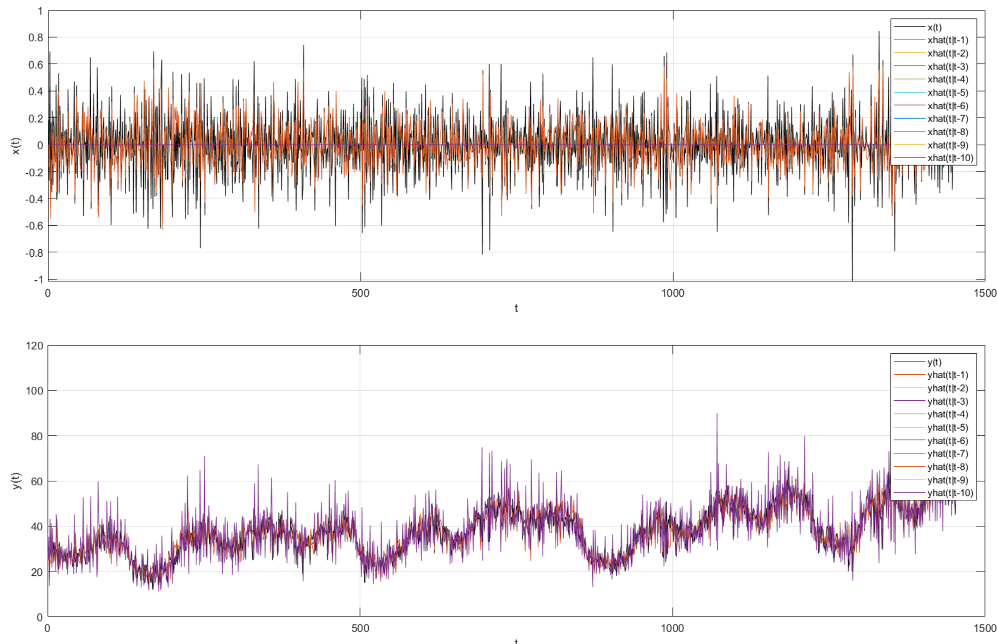

Figure 5.24: 1-to-10 step ahead prediction from MA(1) model compared with the original training set

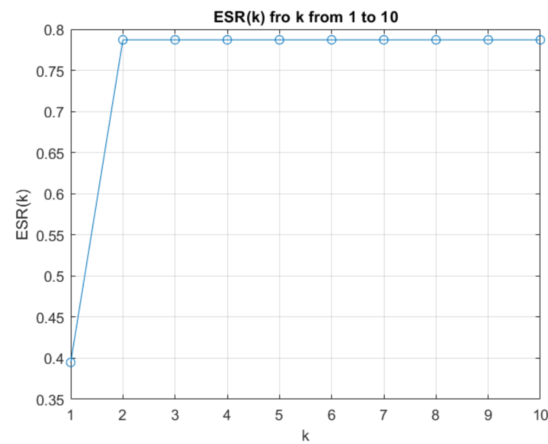

Figure 5.25: $ESR(K)$ for k from 1 to 10 over the training set of the MA(1) model

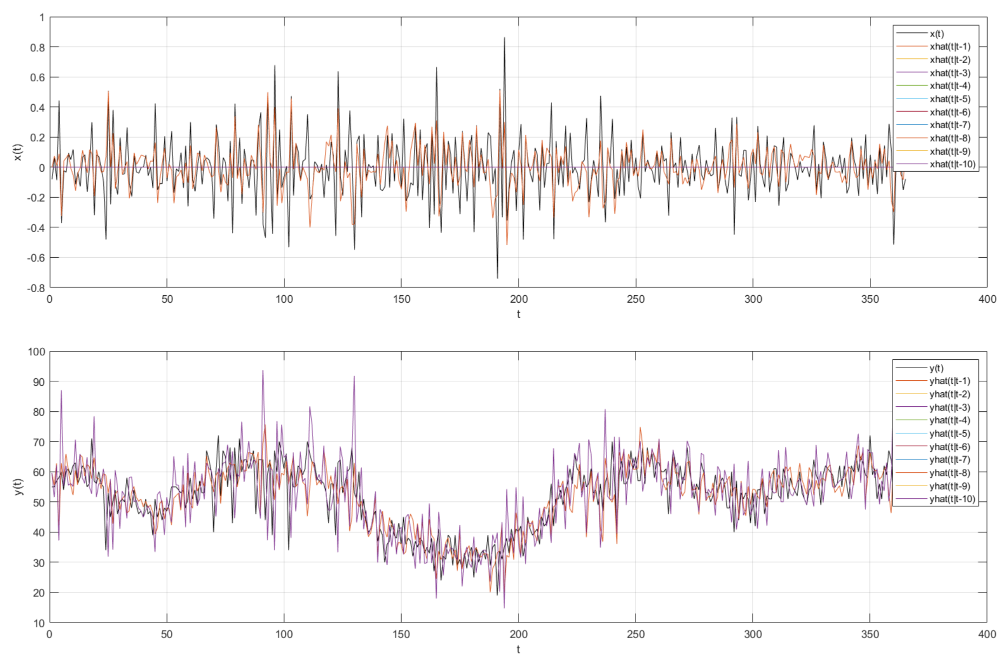

Figure 5.26: 1-to-10 step ahead prediction from MA(1) model over the original validation set

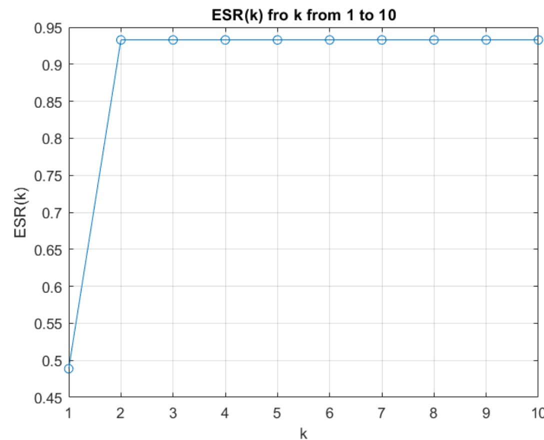

Figure 5.27: $ESR(K)$ of for k from 1 to 10 over the validation set of the MA(1) model

The ESR values are evaluated for the predictors shown in the above figures.
The prediction after one-step of the transformed series degenerate into the mean (practically 0), so the prediction on the original series relies completely on the model of the seasonality and trend.

As for the results on the ARMA(6,10) model, they are shown in the following figures by retracing the same steps as in the previous examples.

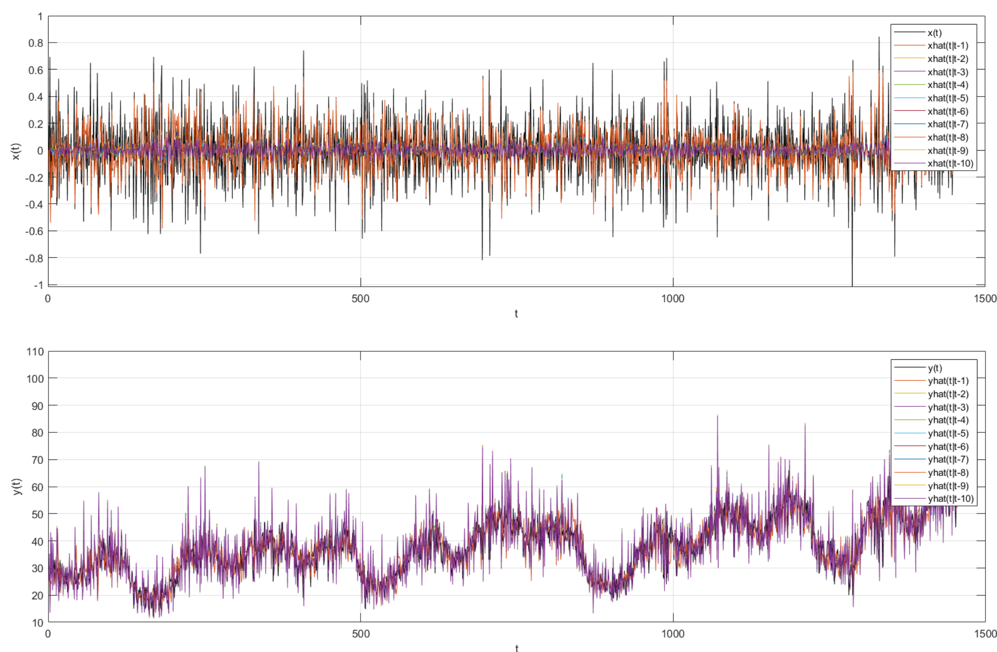

Figure 5.28: 1-to-10 step ahead prediction from ARMA(6,10) model over the original training set

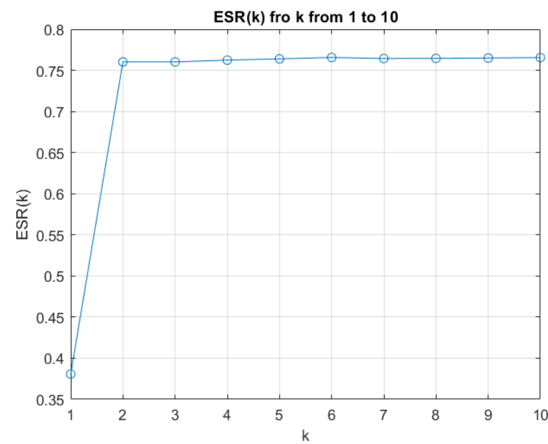

Figure 5.29: $ESR(K)$ for k from 1 to 10 over the training set of the ARMA(6,10) model

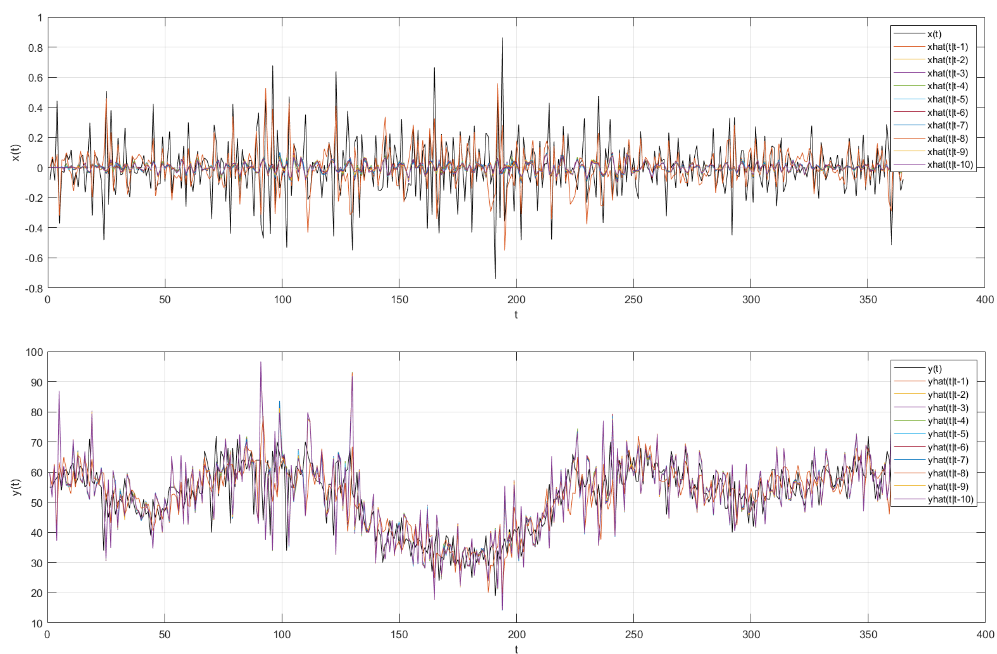

Figure 5.30: 1-to-10 step ahead prediction from ARMA(6,10) model over the original validation set

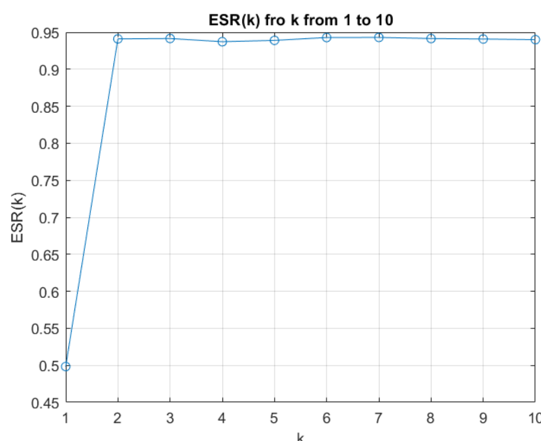

Figure 5.31: $ESR(K)$ for k from 1 to 10 over the validation set of the ARMA(6,10) model

With these estimated models, the optimal multi-step prediction on the original series is completely based on the seasonality and trend. However, a comparative analysis of the statistics of the two models on the validation data reported in Tables 5.2 and 5.2 suggests, as expected, that the simpler model (MA(1)) is able to generalize more effectively on the validation data. This implies that the one-step predictions obtained from this model are more accurate than those of the more complex model, which appears to be overparameterized and thus prone to overfitting.

In order to look insight into how this phenomenon will evolve in future, we can attempt to analyze aggregate data on a weekly and monthly basis. To conduct this analysis, we employed a process of averaging the daily values over corresponding time intervals. This approach allows us to "smooth out" the daily fluctuations and focus on the broader local trends of the phenomenon.

5.3. Weekly Resampling

The same procedure is repeated considering the weekly aggregated data. The following figures illustrate the original series and the several transformations implemented to achieve the stationarity within the time series.

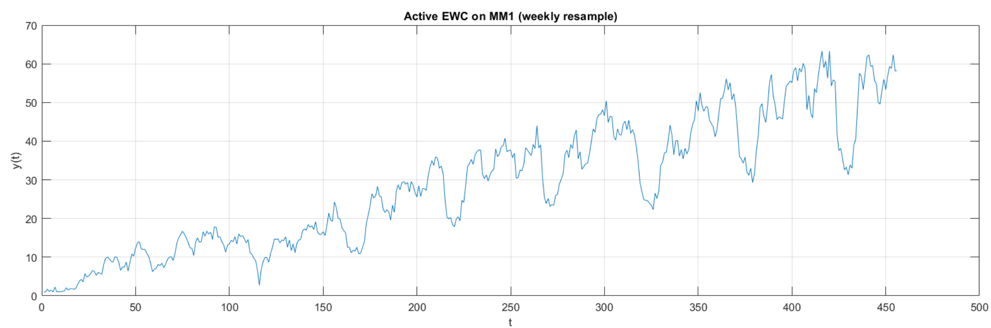

Figure 5.32: Original time series $y(t)$ (456 samples)

The initial 130 data points were excluded due to the identical reasons already stated about the daily data.

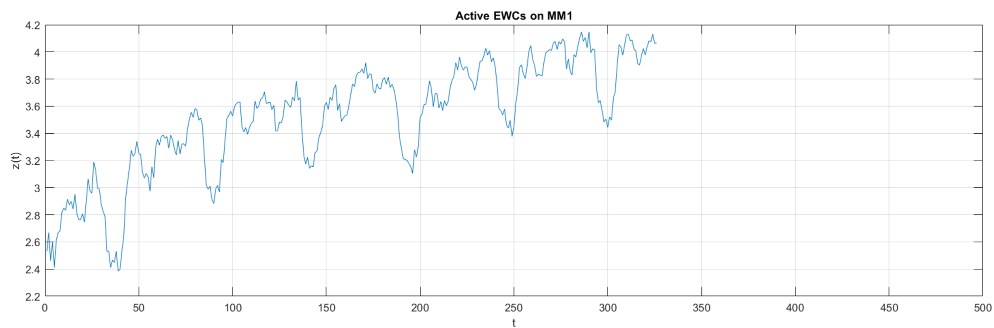

Figure 5.33: Logarithmic transformation $z(t) = ln(y(t))$ (326 = 456 - 130 samples)

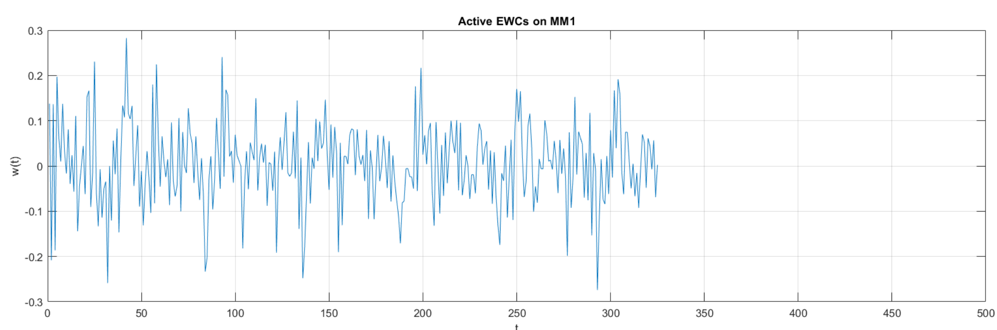

Figure 5.34: Differenced time series $w(t) = z(t) - z(t-1)$ (325 samples)

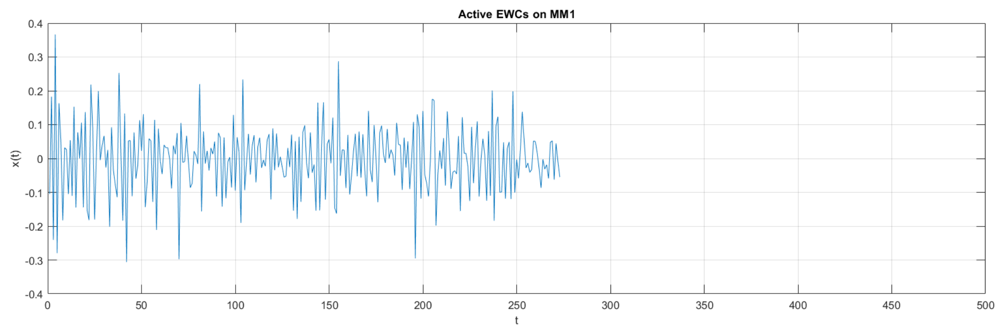

Figure 5.35: Seasonal differenced time series $x(t) = w(t) - w(t-52)$ (273 samples)

The obtained time series has the following characteristics:

- Sample mean: $\bar{x} = -0.0020$
- Sample variance: 0.0108

Now, after removing the sample mean, the series is partitioned into two distinct sets.

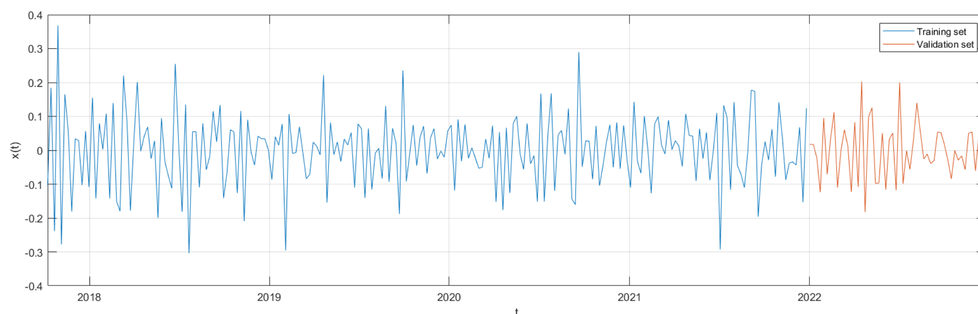

Figure 5.36: Training (221 samples) and validation (52 samples) set

The sample ACF and PACF of the training set only up to lag 20 is reported in Figure 5.37.

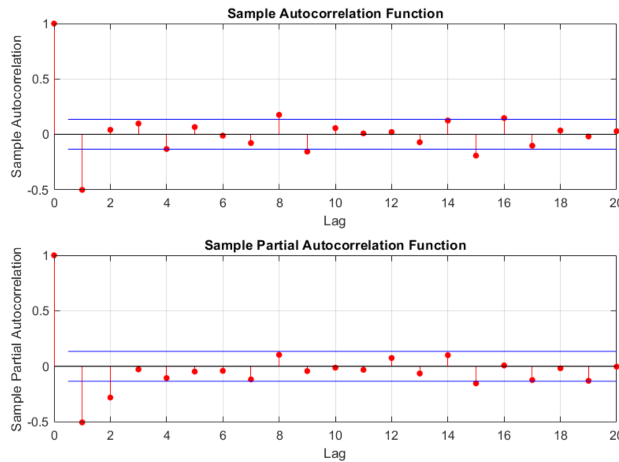

Figure 5.37: ACF and PACF of the transformed time series

It is not feasible to deduce a model directly from the ACF and PACF. A grid search method is directly employed again using only training data and selecting the order of the model starting from 0 to 12 for the AR and MA part.

- min AIC: ARMA(8,7);
- min BIC: MA(1) (with c_1 = -0.6265).

```
ARMA(0,1): AIC: -4.375838e+02 - BIC: -4.341857e+02 - FPE: 8.083790e-03
ARMA(0,2): AIC: -4.370256e+02 - BIC: -4.302292e+02 - FPE: 8.104240e-03
ARMA(0,3): AIC: -4.352570e+02 - BIC: -4.250626e+02 - FPE: 8.169364e-03
ARMA(0,4): AIC: -4.353944e+02 - BIC: -4.218018e+02 - FPE: 8.164306e-03
ARMA(0,5): AIC: -4.329242e+02 - BIC: -4.159334e+02 - FPE: 8.256105e-03
ARMA(0,6): AIC: -4.366363e+02 - BIC: -3.958584e+02 - FPE: 8.119391e-03
ARMA(0,7): AIC: -4.332546e+02 - BIC: -3.856803e+02 - FPE: 8.245108e-03
ARMA(0,8): AIC: -4.331618e+02 - BIC: -3.787912e+02 - FPE: 8.249264e-03
ARMA(0,9): AIC: -4.335346e+02 - BIC: -3.723677e+02 - FPE: 8.236247e-03
ARMA(0,10): AIC: -4.278353e+02 - BIC: -3.598720e+02 - FPE: 8.452553e-03
ARMA(0,11): AIC: -4.254243e+02 - BIC: -3.506647e+02 - FPE: 8.546680e-03
ARMA(0,12): AIC: -4.218936e+02 - BIC: -3.403376e+02 - FPE: 8.686043e-03
ARMA(1,0): AIC: -4.197720e+02 - BIC: -4.163738e+02 - FPE: 8.762292e-03
ARMA(1,1): AIC: -4.371125e+02 - BIC: -4.303162e+02 - FPE: 8.101053e-03
ARMA(1,2): AIC: -4.351063e+02 - BIC: -4.249118e+02 - FPE: 8.174938e-03
ARMA(1,3): AIC: -4.397494e+02 - BIC: -4.159622e+02 - FPE: 8.005136e-03
ARMA(1,4): AIC: -4.336005e+02 - BIC: -4.166097e+02 - FPE: 8.230877e-03
ARMA(1,5): AIC: -4.308893e+02 - BIC: -4.105003e+02 - FPE: 8.332523e-03
ARMA(1,6): AIC: -4.294857e+02 - BIC: -4.056986e+02 - FPE: 8.385676e-03
ARMA(1,7): AIC: -4.315387e+02 - BIC: -4.043534e+02 - FPE: 8.308225e-03
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ARMA(8,5): AIC: -4.373234e+02 - BIC: -3.659620e+02 - FPE: 8.097976e-03
ARMA(8,6): AIC: -4.499388e+02 - BIC: -3.751793e+02 - FPE: 7.649325e-03
ARMA(8,7): AIC: -4.568712e+02 - BIC: -3.787135e+02 - FPE: 7.413807e-03
ARMA(8,8): AIC: -4.331724e+02 - BIC: -3.516165e+02 - FPE: 8.253867e-03
ARMA(8,9): AIC: -4.480071e+02 - BIC: -3.596548e+02 - FPE: 7.719825e-03
.
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.
```

Figure 5.38: Grid search for model selection on weekly data

Starting with the simplest model (MA(1)) the estimated model has now the following transfer function:

$$y(t) = W(z)e(t) = \frac{C(z)}{A(z)}e(t)$$

with:

$$C(z) = 1 - 0.6265z^{-1}$$

$$A(z) = 1$$

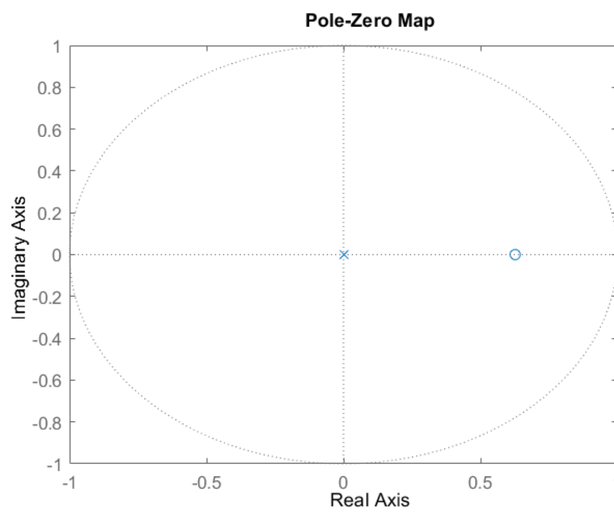

Figure 5.39: Pole and zero map of the MA(1) model on weekly data

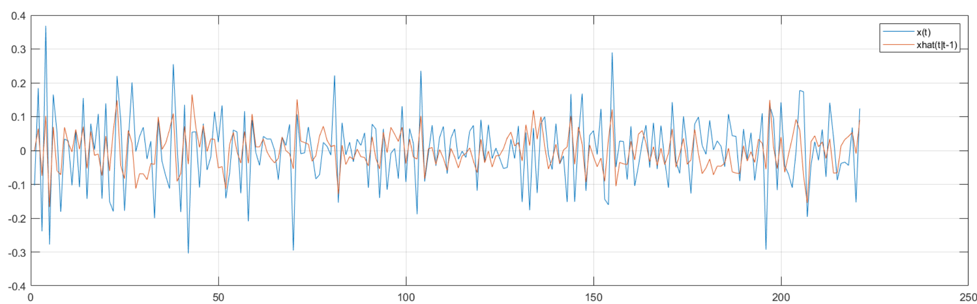

Figure 5.40: One-step prediction of MA(1) compared with the weekly training set

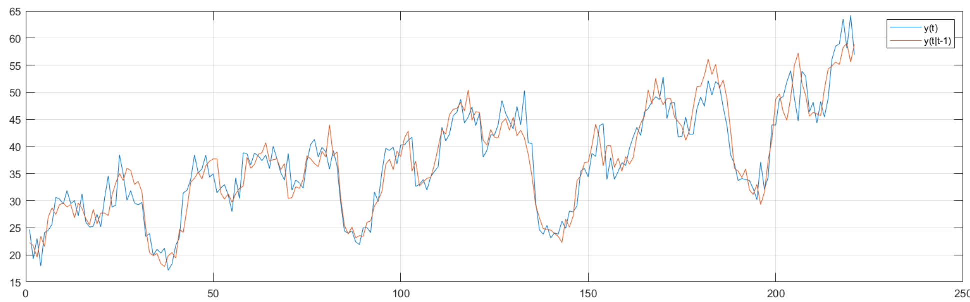

Figure 5.41: One-step prediction of MA(1) compared with the original weekly training set

The corresponding prediction error (residual) $\varepsilon(t) = y(t) - \hat{y}(t) = y(t) - y(t|t-1)$ are reported with its distribution and its ACF and PACF up to lag 20.

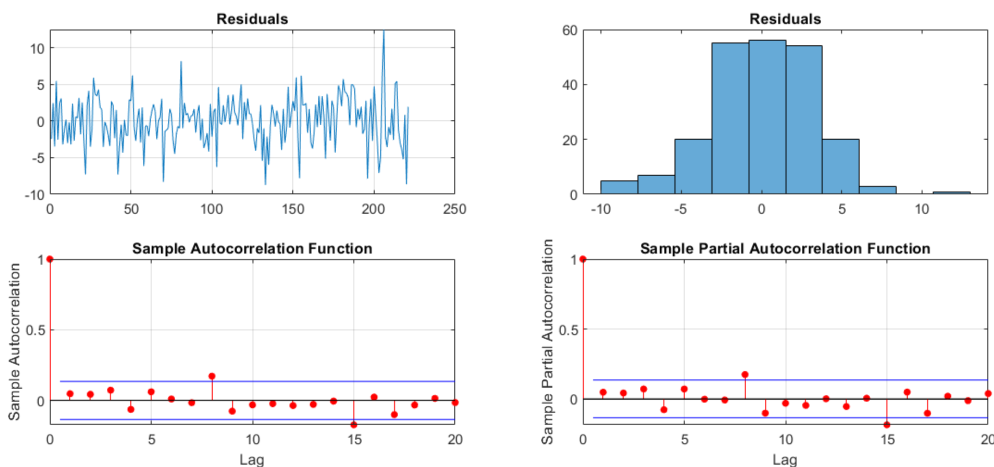

Figure 5.42: One-step predicted error of MA(1) over the original weekly training set

Again, the residual ($\varepsilon(t)$) is not a "white noise", according to the Anderson Test since the number of points (up to 20) exceeding the 95% ($\alpha = 0.05$) confidence interval is 2, and $\frac{2}{20} = 0.1 > \alpha$.

	mean	**variance**	**RMSE**	**MAE**	**ESR(1)**
$\boldsymbol{\varepsilon(t)}$**:**	0.0526	10.7285	3.2684	2.5865	0.0482

Table 5.5: Residual characteristic of the MA(1) model on the training set

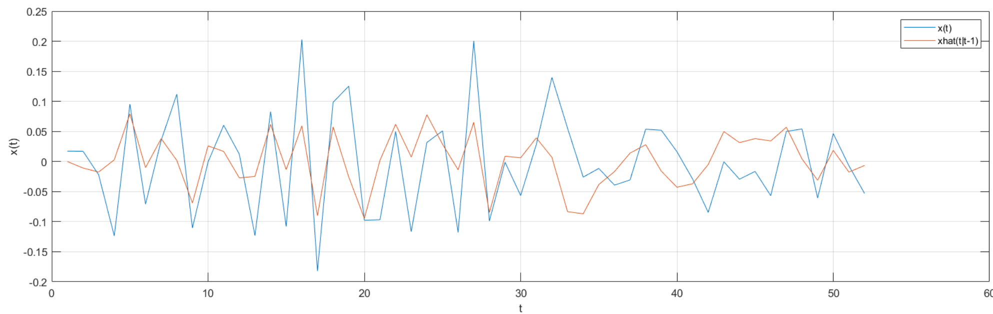

Figure 5.43: One-step prediction of MA(1) compared with the weekly validation set

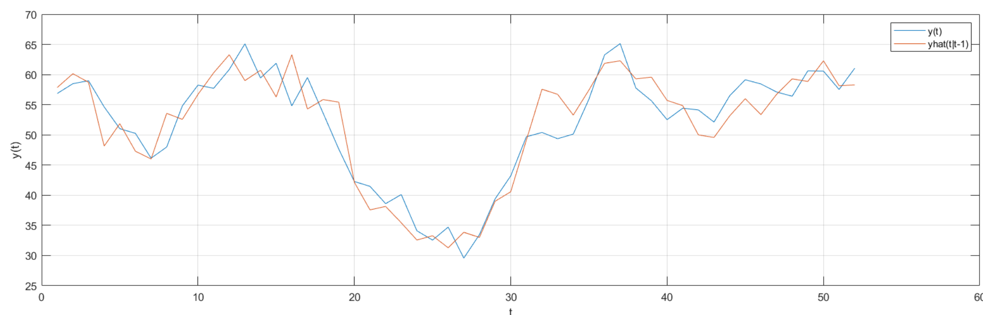

Figure 5.44: One-step prediction of MA(1) compared with the original weekly validation set

The corresponding prediction error $\varepsilon(t) = y(t) - \hat{y}(t) = y(t) - y(t|t-1)$ sequence is shown in Figure 5.45 together with its distribution and its ACF and PACF up to lag 20.

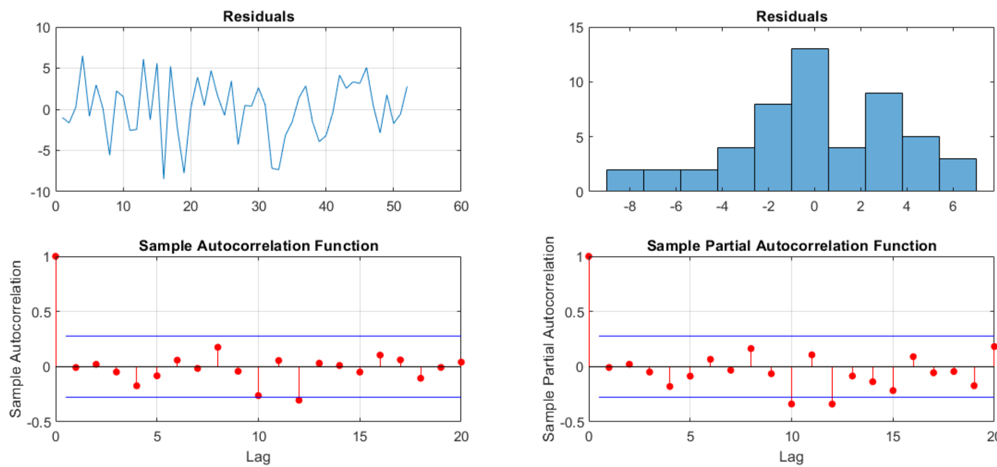

Figure 5.45: One-step predicted error of MA(1) over the original weekly validation set

	mean	**variance**	**RMSE**	**MAE**	**ESR(1)**
ε**(t):**	0.0742	13.0831	3.5829	2.8541	0.1509

Table 5.6: Residual characteristic of the MA(1) model on the validation set

However, the MA(1) model demonstrates favourable performance on data that were not employed for the estimation of the model parameters. This is supported by the Anderson Test repeated on the ACF plot of the residuals obtained from the one-step prediction over the validation set. The number of correlation coefficients of the ACF exceeding the 95% confidence interval is 1 over 20 points considered: $\frac{1}{20} = 0.05$. The test is not completely satisfied.

Now, the second model recommended by the AIC criterion is clearly over-parameterized. Looking at the poles and zeros of the model obtained by fitting the training set in an ARMA(8,7) model, it is possible to see from Figure 5.46, that some of them almost coincide. The estimated parameters of the model are given below.

$$A(z) = 1 + 0.3915z^{-1} - 0.5788z^{-2} - 0.5775z^{-3} - 0.1284z^{-4} + 0.9235z^{-5} + 0.5652z^{-6}$$

$$-0.3587z^{-7} - 0.3744z^{-8}$$

$$C(z) = 1 - 0.1877z^{-1} - 0.8352z^{-2} - 0.1515z^{-3} + 0.09315z^{-4} + 1.07z^{-5} + 0.02733z^{-6}$$

$$-0.725z^{-7}$$

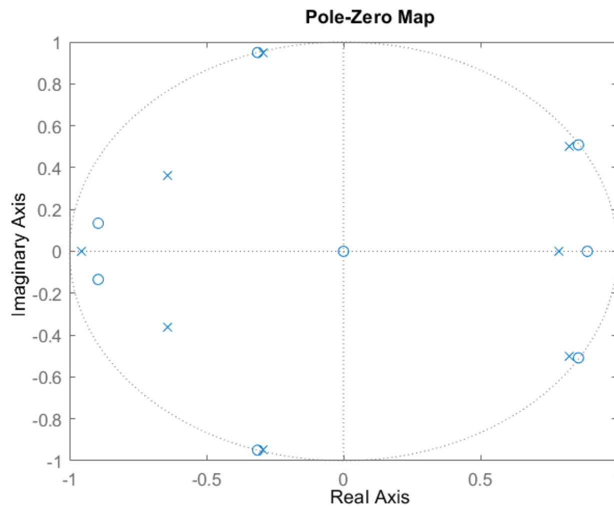

Figure 5.46: Pole and zero map of the ARMA(8,7) model on weekly data

In addition, looking at the ACF and PACF graphs, it makes more sense to consider orders subsequent to the $m = 1$ considered above, since the MA(1) is already a quite good model for the transformed time series. In any case, trying to gradually increase the model order does not have any noticeable improvement on the one-step prediction error on data not used for the model estimation.

5.4. Monthly Resampling

The procedure is applied again to the series obtained by averaging the active EWCs on a monthly basis.

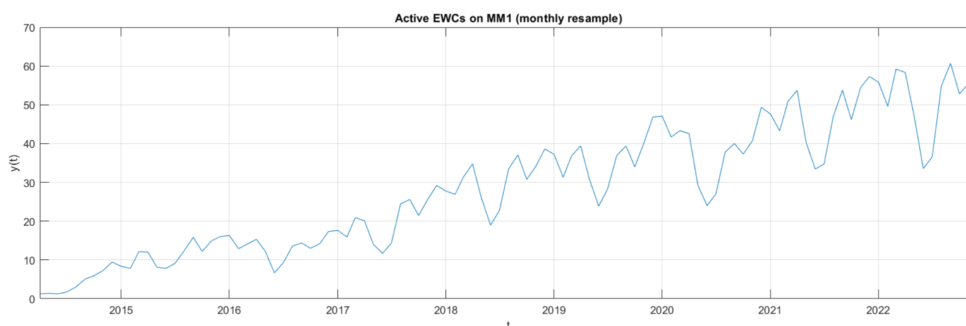

Figure 5.47: Original time series $y(t)$ (105 samples)

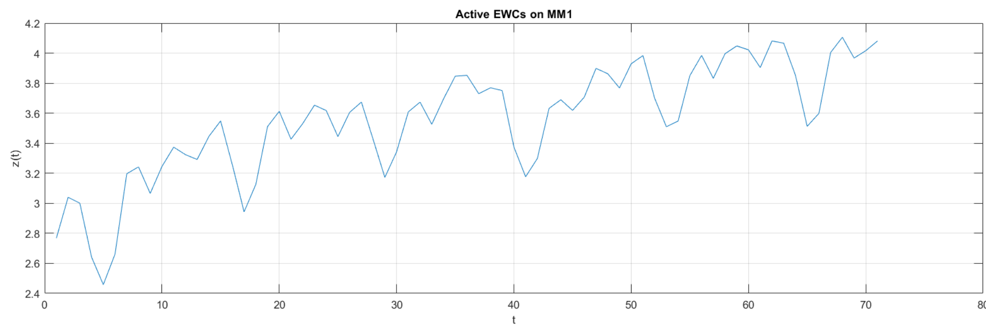

Figure 5.48: logarithmic transformation $z(t) = ln(y(t))$ (71 = 105 - 34 samples)

The first 34 data points were excluded for the same reason of daily/weekly data.

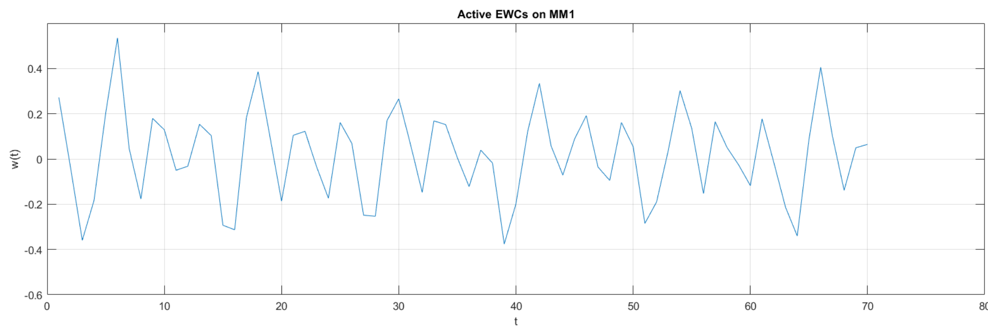

Figure 5.49: Differenced time series $w(t) = z(t) - z(t-1)$ (70 samples)

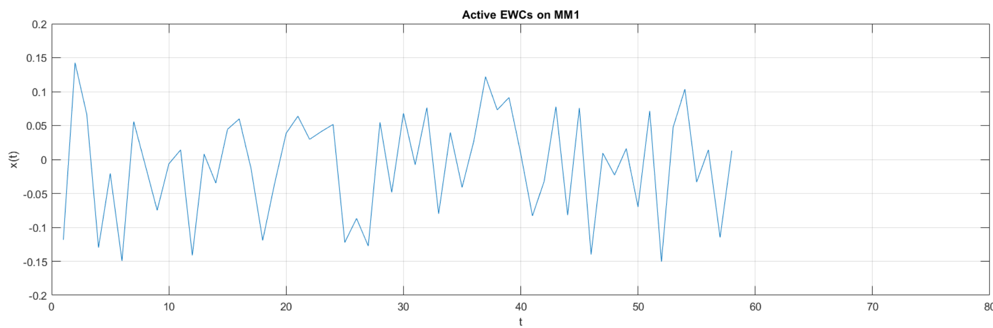

Figure 5.50: Seasonal differenced time series $x(t) = w(t) - w(t-12)$ (58 samples)

The resulting series has the following characteristics:

- Sample mean: $\bar{x} = -0.0085$;
- Sample variance: 0.0059.

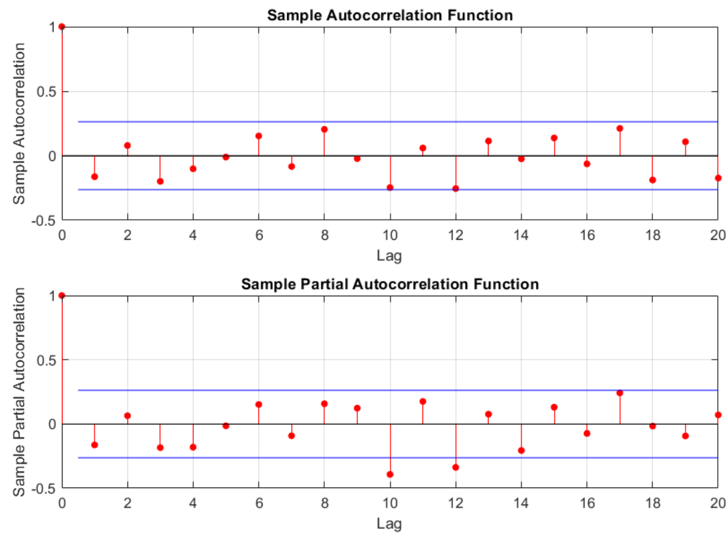

Figure 5.51: ACF and PACF of the transformed time series

The ACF graph of the series shown in Figure 5.51 proves that the transformed series is already identifiable as white noise, this implies that the best prediction one can make is to consider the mean value of the transformed series (practically 0) and thus, for the prediction on the original series, the best estimate is obtained from the trend and seasonality model by applying anti-transformations.

6 | Conclusions and future developments

This thesis investigates various memory correction phenomena that occurred in the digital equipment based on SDRAM technology onboard two LEO-orbiting satellites. By analyzing the telemetries from the first satellite, a classification of all the corrections across the SSMM equipment's memory array was conducted, driving towards the identification of the underlying root-causes and activation stimuli of these corrected errors: either pure istantaneous radiation impact effects (SEUs or SEFIs) or electronic charge persistent leakage proliferating in the SDRAM devices and due to ionizing cumulative effects (since not observed in ground operations but only in orbit). Phenomenon already visible at a "room" temperature at which the digital equipment is kept inside the satellite during orbit flight (for this reason, we called them Extremely Weak Cells). The behavior of these phenomena during the whole satellite mission time was studied, with a particular focus on EWC first appearance, activation/deactivation and global proliferation. The final result is a better understanding of the effects of the space environment on the performance of SDRAM-based memory equipment in satellites for the LEO orbit and of the faced radiation environment. Furthermore, an unexpected thermal lever was discovered, both affecting the proliferation rate and the activation of such EWCs.

The effectiveness of the proposed classification and the thermal lever in the leakage activation and proliferation (once the first leakage is generated by radiation hits) has been validated by analysing an independent telemetry data set coming from a second SSMM digital equipment, twin to the previous one, onboard another satellite that was launched two years later in the same orbital plane.

All the findings can be grouped in well-defined areas according to the type of considered phenomenon. The following list summarizes all the notable findings related to the root cause and behaviour of the EWCs:

1. A visible correlation is established between the activation waveform of S-S EWCs

(that is also correlated to the written scientific pattern in the SDRAM devices, that statistically changes randomly each day, according to the observed operations in orbit) and the SSMM equipment TRP waveform, on all SDRAM-based memory modules, starting to become clear from the third year in orbit on Satellite A, and similarly on Satellite B;

2. The S-S EWC total certified number increases progressively in a linear way, on all SDRAM-based MM boards, in both satellites. Furthermore, the effect is cumulative and the newborn S-S EWCs re-appear at any off/on cycle of the MM boards. The "slope" of the MMx_CE counter trend visible in telemetry progressively increases along the years as a consequence;
3. The S-S EWC total number at end of operating life is increased by 3 orders of magnitude, on all SDRAM-based MM boards over 9 observed years of flight of Satellite A. The level of such S-S EWC achieved by Satellite B, launched two years later, are in line with those ones of Satellite A after the same number of years in orbit, thus demonstrating the linear cumulative effect of the phenomenon;
4. SDRAM-based MM boards with lower local average temperature w.r.t. other MM boards, are characterized by both lower proliferation and lower activation persistance of S-S EWCs over time, on both satellites, even if the two SSMM equipments were operated in slightly different thermal conditions;
5. For each MM board of both satellites, the "hot spots" of leakage phenomenon (ICs/TSOPs with higher numbers of identified S-S EWCs) are mainly located on the "Components" side of the PCB, that has a local temperature slighly higher than the "Solders" side (as per thermal analysis of the PCB);
6. The root cause of the progressive proliferation of this leakage phenomenon in orbit, with equipment temperature kept close to the same "ambient" temperature experienced during on ground testing, when these phenomena did not appear, can be attributed to the radiation absorbed in space by the two satellites in the selected LEO orbit;
7. Summing all previous evidences, it is possible to assert that the temperature is also a lever for exacerbating the leakage phenomenon caused by radiation, both in their proliferation (absolute local temperature of the MM boards) and in their activation (seasonality variation of temperature mean local temperature of the MM boards). In other words, temperature absolute mean value and variations stimulate the S-S EWC activation and, at the same time, temperature is one of the causes of the

increase of their total absolute number;

8. As for the S-S EWCs, the activation of the M-S EWCs is correlated with the SSMM TRP waveform;

9. SDRAM-based MM boards with lower average temperature are characterized by lower proliferation of M-S EWCs and by a lower activation over time too, on both satellites;

10. The M-S EWC total number is increased by 2 orders of magnitude on all MM boards over 9 observed years of flight on Satellite A. The levels achieved by Satellite B are in line with those of Satellite A after the same number of years in orbit;

11. On both satellites, the common experienced "seasonal eclipses period" in LEO orbit seems to act differently on the 2 types of EWCs: the S-S EWCs are almost "zeroed" out during colder TRP periods, while the M-S EWCs are more "resilient" in electronic discharge and always maintain a relatively high number of active appearance. Although the total number of M-S EWCs with respect to the S-S EWCs is lower, M-S EWCs turn out to be in leakage more persistently over the entire analysed timeframe. Being M-S EWC a signature of "contiguous" logical area in a SDRAM TSOP captured in leakage and assuming also a "physical" proximity of them on the die, this means that both punctual and contiguous cells leakages are always corrected by the onboard ECC and scrub passage, but the extended SDRAM area in leakage along a TSOP areas tends to be persistent in discharging more than the punctual ones (S-S EWCs);

12. S-S EWCs and M-S EWCs show a very similar production and ignition mechanism and they can be considered as the product of the same SDRAM behaviour alteration phenomenon that is induced by radiation hits and influenced by the thermal lever. These two levers are most likely linked to the analised LEO-orbit;

13. On Satellite A, there are no areas of high concentration of both types of EWCs: their appearance is almost uniformly distributed, and no particular TSOP levels or cubes over all MM boards faces are particularly affected. This is a signature of a random distributed radiation hit on the volume of the MM boards array. Differences in EWCs among MM boards are found to be correlated only to the slight average temperature differences between them;

14. The EWC distribution along each analysed 64 MiB TSOP (6720 TSOPs are present over the two SSMM devices, i.e. 60 (48 DATA + 12 C-S) Cubes * 8 TSOPs in each Cube * 7 MM active boards * 2 SSMM devides) is roughly uniform, as expected from

a radiative induced phenomenon. It is noticed that the inter-distance between two logical consecutive locations in leakage never exceeds 3 MiB, with a concentration around a 0.5 MiB step, for all TSOPs on both satellites;

15. On Satellite B SSMM, the unique TSOP0 inside the IC121 cube on MM1 shows a widely different behaviour from all analysed TSOPs. In a precise moment after 3 years in orbit, a persistence in EWC proliferation and activation in such TSOP was observed, bounded in a limited area of the die, altering visibly all the computed metrics for that MM1 board. This phenomenon lasted with continuity for about 1.5 years, despite any pattern change in that SDRAM area (leading to the unique evidence of a truly "stuck symbols" set in a same TSOP area) and disappeared only after a complete MM1 off/on power cycle lasting hours (due to other reasons); this was the only occurrence of such "stuck symbols" phenomenon observed in 9 (Satellite A) + 5 (Satellite B) years spent in orbit;
16. The re-configuration in the active MM boards on the SSMM equipment on Satellite B commanded (for other reasons) few weeks after launch and forming a new "shape" of the temperature profile among the modules is compatible with the observed final distribution of the total number of EWCs among the MM boards: this is a further confirmation of the temperature lever effect discovered in the data from Satellite A;

With respect to the istantaneous radiative effects (SEU, SBC, BOS) caused on SDRAM devices, the main conclusions are given below:

1. Beyond the SDRAM certified leakage phenomena (S-S and M-S EWCs) also istantaneous radiative phenomena (SEU, SBC, and BOS) were corrected by onboard ECC and can be identified in the telemetry data; such radiative induced phenomena show a much more random distribution, both through the MM boards in SSMM, across the ICs/cubes of each single PCB side, for both satellites. All the SDRAM area subjected to these radiative hits, either punctual (SEU) or extended (SBC, BOS) ones, were always corrected by the passage of the scrub with ECC, without any need of further recovery actions;
2. No relationship between the SSMM TRP waveform and radiative istantaneous phenomena (SEU, SBC, BOS) occurrences is visible. At the same time, no relationship with the temperature profiles over the MM boards and along the PCB array is found for such phenomena;
3. The BOS rate observed in the first 3 years in orbit (where such data information is captured by telemetry data structures in a statistically effective way, as discussed in

the previous chapters) is compatible with the SEFI rate of the Radiation Analysis: therefore such MMx_CE counter "jumps" of $k * 2048$ bytes across a single TSOP occurring in few seconds are recognised in this thesis work, and as suspected in the preliminary TAS-I TNs, as observables of the recovery of a "potential" SEFI by simply accessing the device in reading, i.e. not causing a functional interurruption and so not requiring a power off/on cycle of the affected SDRAM device;

4. On both satellites, no correlation is found between the appearance of EWCs within areas affected by BOS. A working hypotesis is that EWCs and BOSs are caused by radiation hits with some different features;

5. The SEU & SEFI/BOS rate information extracted from the available TM(6,6) data is statistically valuable only in the first 3 years in orbit, for both satellites. In fact, later on, the growing leakage phenomenology occupies always more frequently the allocated space in the onboard corrections logging structure, and it seems "falsely" reduced in the observation data in TM(6,6) after that age. Looking instead at TM(3,25) information (that provides the MMx_CE counters each second but without reporting any infomation on the occurring address), the BOS/SEFI rate is constant along all both satellites missions, resulting in 1..3 events per MM board per week (this is the order of SEFI rate predicted by the Radiation Analysis);

6. The BOS/SEFI event corrections count show a "clustering" behaviour in terms of corrected $k * 2048$ bytes along the same TSOP, with a range of k = 1,2,3,4,5 visible on all TSOPs. This can be linked to the inner device organisation (2048 bytes "page" organised in 4 banks) in the area subjected to the radiation hits;

7. The correction figure onboard a SDRAM device in LEO orbit results from a complex interaction of radiative istantaneous phenomena (SEU or SEFI) that vanish (they are corrected in that location and never appear again), plus a long term persistence effect of electronic leakage (most likely linked to the absorbed radiation ratio over time, i.e. the so called Total Ionizing Dose (TID)), that does not vanish but increases along time;

All above results are about Soft Error phenomenology; data analysis shows also some findings on the appearance of Hard Error phenomenology:

1. Hard Errors are related to unsuccessful R/R/W/R sequence operated by MC FPGA on a SDRAM address. After this process, confirming the non-correction at the last R operation of the cycle, a power off/on cycle of 30 ms overall (i.e. for a time within the auto-refresh period of SDRAM device set for this SSMM to 48 ms) succeeds

in recovering the persistent leackage on that address, confirmed by another single direct R access at that address. In total, 153 HEs were observed on Satellite A SSMM in 9 years and 89 HEs on Satellite B in 5 years;

2. The HE statistics of SSMM embarked on Satellite A is higher than Satellite B, due to a frequent HEs period in its MM0 occurred in May-August 2018 (analysed in the second TN by TAS-I) data analysed in this thesis, confirming the findings in 2018;

3. Along the years, a sub-set of Hard Errors was not solved by the power off/on cycle of the SDRAM device. This caused (as foreseen by the SSMM equipment onboard Failure Detection Isolation and Recovery (FDIR) management) the "parking" of 1 GiB memory space each time, i.e. that space is not used for memorization purpose from that moment on, decreasing the global SSMM memory capacity but not affecting its performances. It has to be highlighted that any time the SSMM was power cycled (for other reasons) and its MM boards array switched off/on and re-tested at re-initialization, those previously affected memory locations by the persistent HE also after the quick device power cycle, became newly available for storage any time. Therefore, no permanent damage and loss of memory space was observed; for such type of HE events 24 occurrences were recorded on Satellite A SSMM in 9 years and 8 occurrences on Satellite B in 5 years;

From the automation and time series modelling point of view, the main results relative to the analysis of EWCs activation on the MM1 module of Satellite A are reported below:

1. The best performing ARMA model on daily data is the MA(1). This model is able to generalize better on the data belonging to the validation set (concerning the 365 most recent samples, i.e. one year period) and yields to the most accurate prediction for the number of active EWCs "for the following day" after applying the inverse transformations;

2. Considering the time series analysis about the daily activation of EWCs on the MM1 module (one of the most affected of Satellite A), the best-performing model for the optimal prediction beyond one day of the transformed series is the MA(1) model. The prediction at step higher than one is obtained considering the mean of the transformed series (practically 0), the original series relies completely on the model of the seasonality and trend applying the anti-transformations.

3. When considering weekly data, the top-performing model is again an MA(1). This particular model enables to make accurate predictions regarding the average number of active EWCs "for the following week";

4. As for monthly aggregated data, after performing the required transformations to remove the linear trend and the annual seasonality, the resulting series can be classified as "white noise". This result allows to state that the most accurate estimation that we can make of the average number of active EWCs on a monthly basis is obtained completly from the model of the seasonality and trend applying the anti-transformations.

This thesis provides a better understanding of the corrective phenomena in a SDRAM array in orbit, allowing to build a model for the prediction of the behavior of digital equipment in current and future missions, even if different technologies and devices organisation for data storage will be used. It should be noted that, despite the presence of combined istantaneous radiation and persistent leakage phenomena (still radiation induced, but not vanishing), the "distribution" of the scientific information among different physical separated ICs (typical of a matrix organization) and the error correction mechanism implemented in such SSMM architecture is highly resilient. Moreover, the safety measures that have been put in place in the analysed SSMM, including the device off/on cycle, have made this SDRAM memory technology even more reliable in the harsh space environment.

The findings and conclusions drawn from this thesis offer several possibilities for future research in the area of SDRAM memory used in space. Some topics could be the following:

1. In this thesis all the information contained in the TM(6,6) have been extracted and used. In future, also the more resolute (only in terms of MMx_CE counter increase, since it is reported every second) information carried by TM(3,25) could be combined with TM(6,6) in order to "estimate" the exact time of the corrections reported in the 128-entries array encapsulated in the TM(6,6) only at the time of production of this packet. In this way, it will be possible to better establish the correlation between the birth of EWC with the passages of the scrub and downlink operations;

2. Use the telemetry TM(5,1) in order to determine the zone interested by all types of HE (either solved by TSOP device power off/on cycle of about 30 ms or solved only by much more longer MM board power off/on cycle) and explore the correlation with satellites SAA and high latitude passages;

3. A deeper analysis related to the BOS/SEFI occurrences along the satellites orbit position and their SAA or higher latitude passages crossing (considering the scrub period of 27 minutes along a 90 minutes orbital period) and the significance of $2048 * k$ internal TSOP clustering could be investigated;

4. All the correction addresses could be further processed considering also the istantaneus scrub position and its constant rate, starting from any MM boards switch on initial sequence, in order to determine if the correction was achieved by the scrub (periodic) or by the downlink (aperiodic) process and trying to understand why during a downlink operations on the MM board, very often, "new" EWCs seem to be stimulated in leakage, as visible in the TAS-I TNs and also in the present thesis;
5. Analyse the SDRAM device behaviour in different radiation environments (e.g. other LEO/MEO/GEO orbits or interplanetary transfer)

In addition, possible further actions regarding observability improvement in the telemetry produced by such kinds of SSMM equipment are:

- adding the actual OBT time to each entry logged into the vector of 128 "entries" periodically dumped via TM(6,6) packets;
- Increase the frequency of DUMP TM of SPV SRAM area by Ground Control in order to have more frequently the address of each correction, avoiding loss of useful information for analysis;
- Increase the size of the 128-entry buffer used to feed the TM(6,6), so that it can capture all corrections that have occurred, even when radiation-induced leakage phenomena begin to become significant on SDRAM. This could help to build a map of the SEU/SEFI events occurring at that orbit, along satellite position and along mission time, without being affected by the raising of leakage pheneomenon;
- Add the scrub address logical position in TM(3,25), per each MM board;
- Make the scrubbing processes on all MM boards "synchronous" after first initialization, i.e. setting scrub starting addresses to evolve at a constant rate from 0 from a same time on. In this way the SSMM could be used as a raw particle "direction" detector, not only as a particle counter (as now). This will help to correlate radiation phenomena that could appear close in time in teh TM(3,25) stream, due to phased MM scrub phases, and that can be simultaneous in reality;
- Provide the capability to switch off/on a TSOP/device or a IC or a column for a controlled time by Ground, in order to explore the Hard Error recovery over a long time spent in off without switching off the whole MM board (and losing all data).

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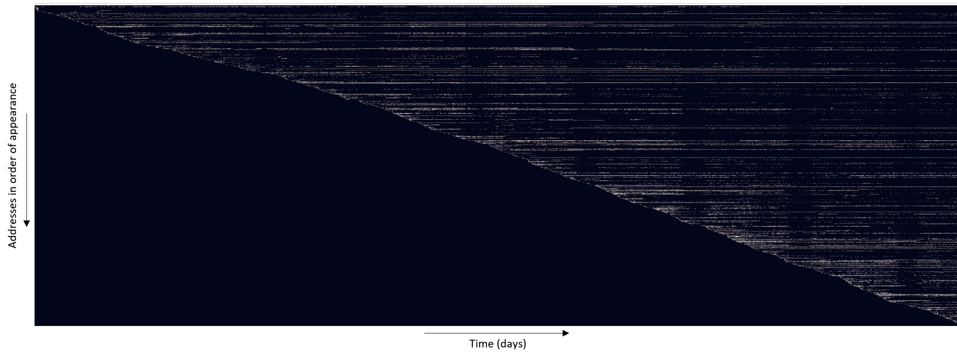
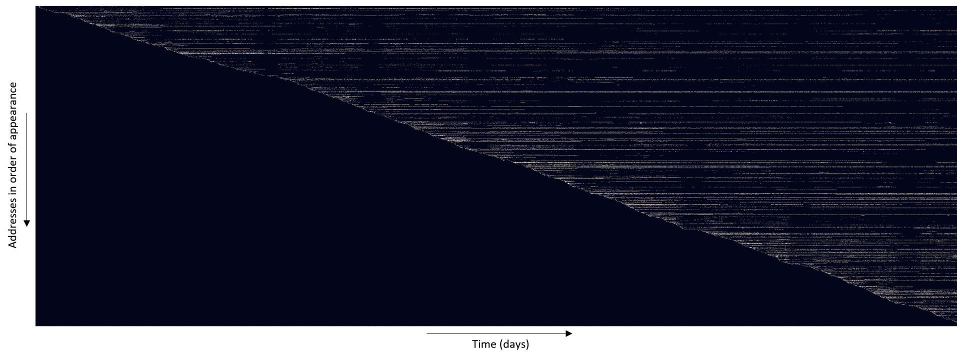
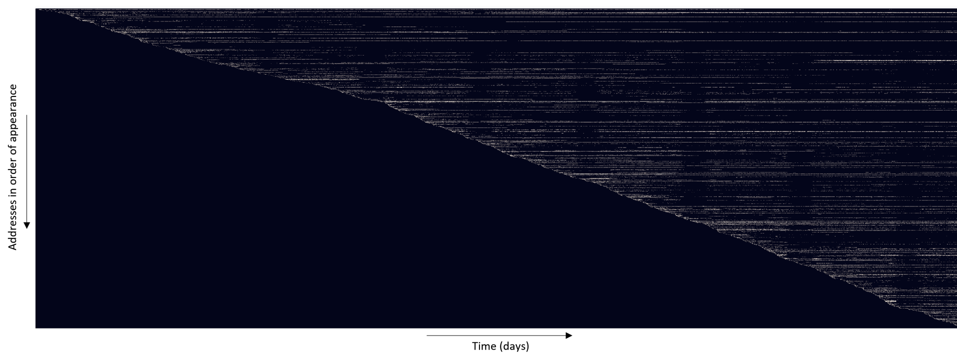
A | Appendix Satellite A







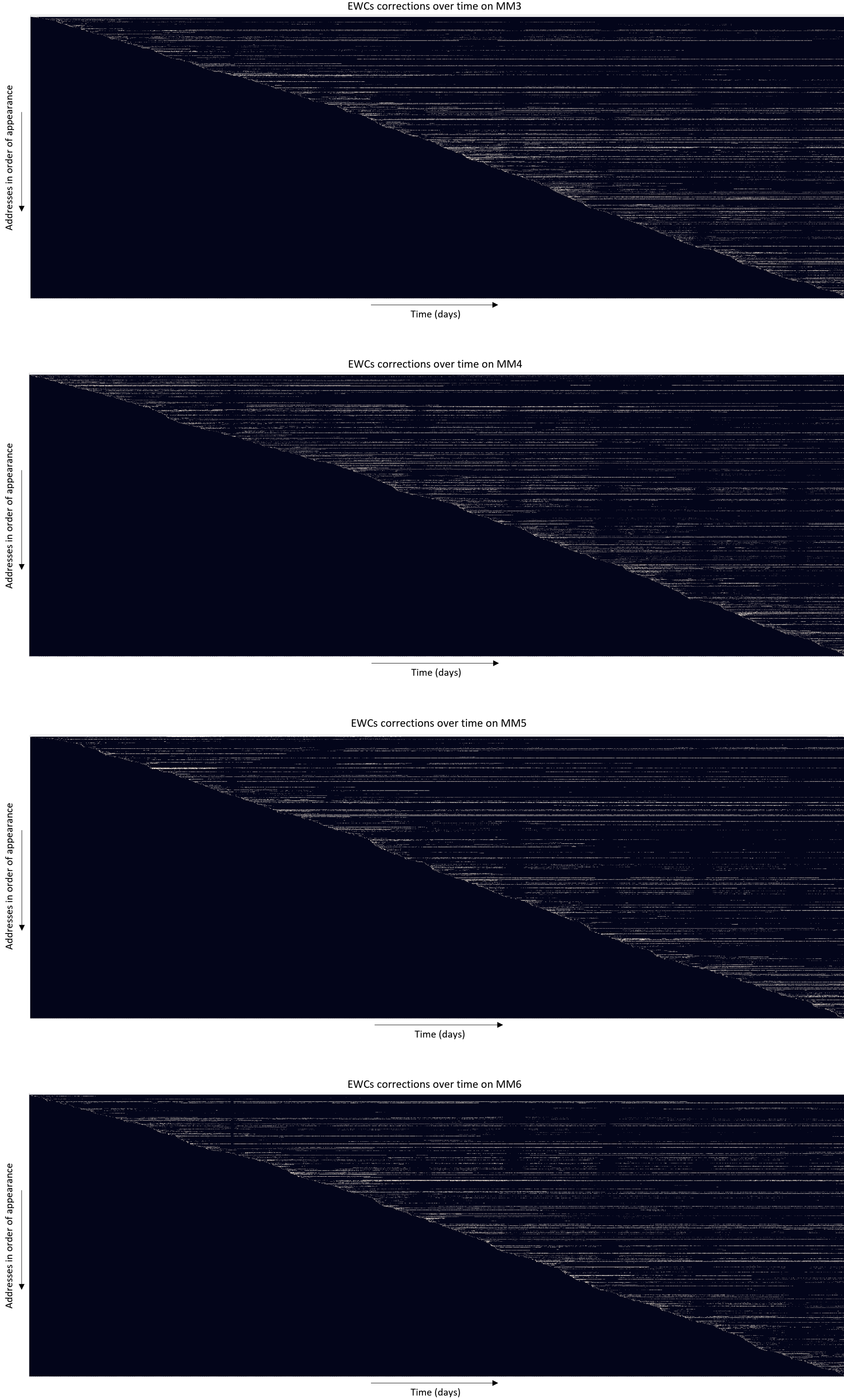
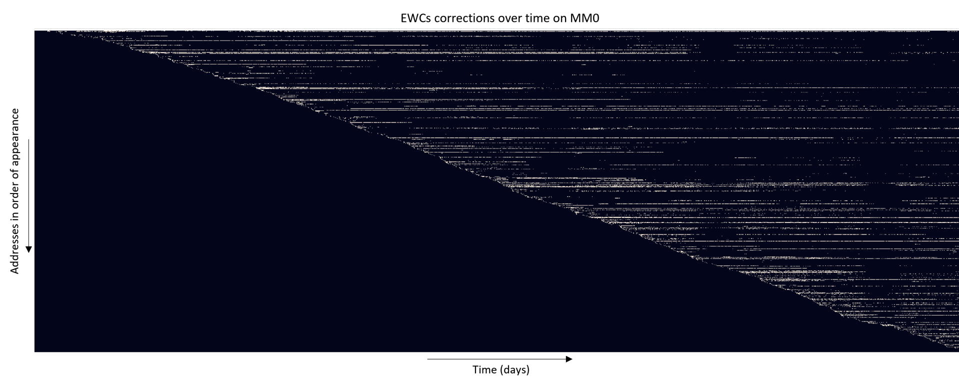
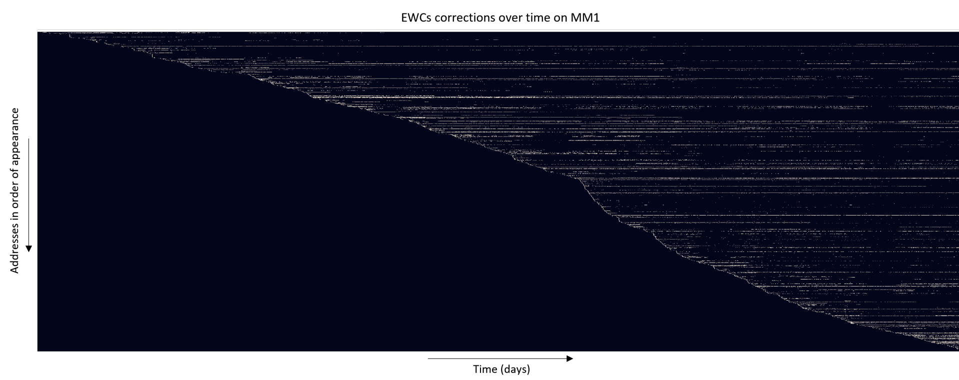
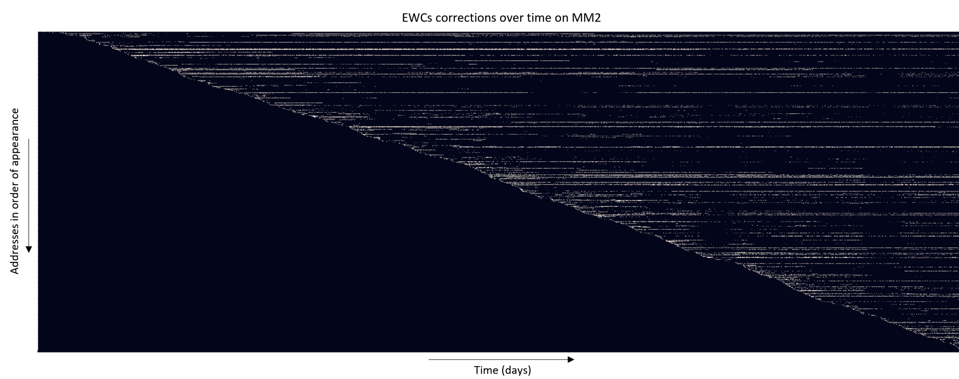


Figure A.1: EWCs activation over time on every memory module board from MM0 to MM6 on Satellite A

B | Appendix Satellite B







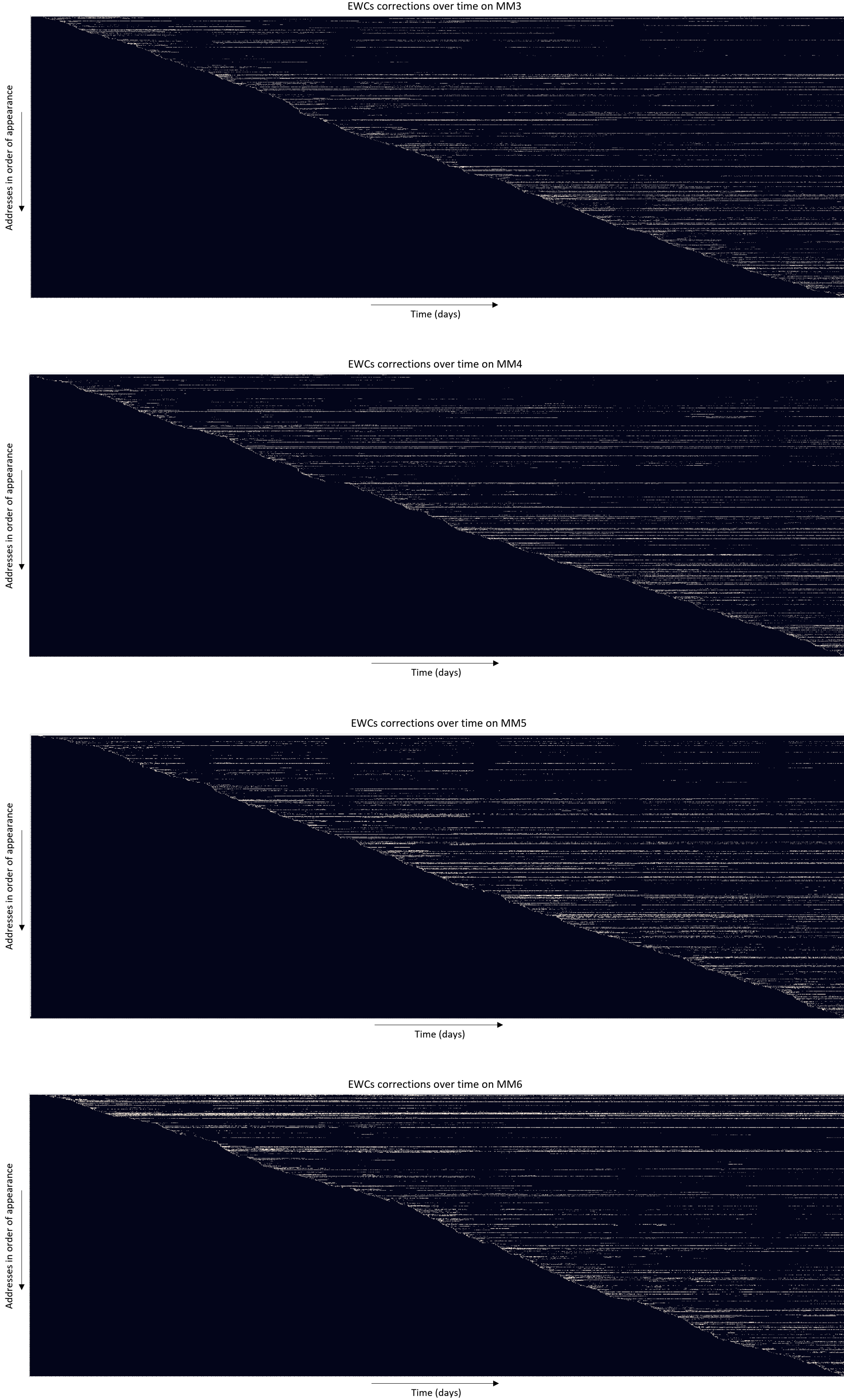


Figure B.1: EWCs activation over time on every memory module board from MM0 to MM6 on Satellite B

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