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LOW-NOISE, MULTICHANNEL, ELECTRONIC INSTRUMENTATION FOR BROADBAND OPTICAL SPECTROSCOPY APPLICATIONS

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Abstract

The aim of my PhD research was to design low-noise, high-speed, lock-in based, multichannel acquisition systems for Ultrafast Spectroscopy applications. Ultra-short pulsed lasers are widely used in spectroscopy for their capability to concentrate energy in very short time windows and thus stimulate samples with high power levels and precise time resolution. These characteristics make them suited for different spectroscopy techniques like Stimulated Raman Scattering Microscopy and Time Resolved Pump-Probe Spectroscopy.

The first part of my PhD was devoted to design an innovative 76-channel acquisition system for Coherent Raman imaging, combining a low-noise differential front-end based on the lock-in technique, with a parallel acquisition and real-time data elaboration. This work was conducted as part of CRIMSON project. This project has received funding from the European Union Horizon 2020 research and innovation program under grant agreement No. 101016923 - an ERC project headed by Prof. Dario Polli of the Physics Department of Politecnico di Milano. The final aim is to develop an innovative Raman microscope for real-time and non-invasive imaging of cells and tissues, which promises to make a revolutionary impact on many fields of biology and medicine as a ground-breaking tool for tumor identification and analysis. To achieve such a result, an ASIC implementing a 8-channel readout

circuit was designed. The 8-channel IC was tested and integrated in the electronic acquisition module. It allows to process in parallel the signals coming from a photodiode arrays with an automatically balanced differential lock-in architecture for a reduction of the optical noise. The system is able to acquire a 76 wavelength Raman spectrum spatially diffused on the photodiode array so that each wavelength of the spectrum could be separately acquired by a specific element of the array. The system exploits a modular architecture made of ten 8-channel modules plugged into a motherboard. An Artix-7 FPGA provides all the control signals, implements a Digital Signal Processing (DSP) chain for offset cancellation and adjustable lock-in bandwidth and manages the USB communication between the platform and the PC. Finally, the proper operation of the whole Raman microscope was validated, from the optics to the electronics.

In the remaining time, the research focused on the development of a new spectrometer for Pump-Probe spectroscopy. The current instruments on the market are limited in acquisition speed due to the use of CCDs and low-repetition-rate lasers (i.e. in kHz range). The project's goal was to design the electronics for an instrument capable of acquiring up to 40 wavelengths in parallel with a resolution of just 1 ppm. The spectrometer consists of two ASICs that amplify and process the signal, along with a PCB for data conversion and transmission to the PC. A key feature of the IC is simple pre-processing of the input signal in order to relax the specification for the Analog to Digital conversion. To achieve this result, I built upon a highly flexible 20-channel ASIC (ECLIPSE) designed by a former PhD student. I developed the necessary electronics (PCB and firmware) to control two ECLIPSE ASICs operating in parallel, exploiting an ARTIX-7 FPGA to manage communication between the PC and the electronic board. After developing the firmware for 40 different wavelengths, I created a new GUI in the C# environment that enables the acquisition, plotting, and storage of the 40 traces. Once the system worked properly, in collaboration with the Physics Department, we optically validated the platform by acquiring real spectra.

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Part I

Raman

CHAPTER 1

Introduction to Raman Spectroscopy

This work is part of the CRIMSON project [1], funded by the EU and coordinated by Professor Dario Polli from the Physics Department at Politecnico di Milano.

CRIMSON is dedicated to the development of an advanced bio-photonics imaging device based on vibrational spectroscopy, with the aim of investigating the cellular structure of diseases, thereby facilitating new strategies for therapy. The project exploits label-free broadband coherent Raman scattering (CRS) technique extended into the fingerprint region (600 cm^{-1} to 1800 cm^{-1}) [2], which offers insight into the nucleic acids, proteins and lipids present in the biological sample under examination. This enables a quantitative analysis of tissues that allows to determine their morphological and chemical nature with unprecedented accuracy.

A significant focus of this research is on applications related to cancer detection and identification, with the intention of supporting current clinical practice, which is based on the visual examination of tissues by a pathologist. This traditional method

is often slow and subjective, which complicates the identification of the various types of cancer that exist.

1.1 Raman Spectroscopy

Raman spectroscopy relies on the Raman effect, an inelastic scattering phenomenon that involves photons and vibrational modes. This effect was first discovered in 1928 by the Indian physicist and Nobel laureate C.V. Raman.

It is a non-invasive and non-destructive analytical technique that offers comprehensive insights into chemical structures and molecular interactions.

Raman spectroscopy provides a sort of signature of the sample which reflects its structure and molecular composition, since each biological sample exhibits a unique vibrational spectrum (Raman spectrum). Various segments of the Raman spectrum generally provide information on different chemical bonds, with the fingerprint region being the most informative segment. This fingerprint region is typically recognized within the 600 cm^{-1} - 1800 cm^{-1} range, where the spectrum reveals multiple contributions from proteins and nucleic acids [3].

Knowledge of the spectrum enables the examination of sample composition by comparison with a database of established spectra. An example of a Raman spectrum is shown in Figure 1.1. Three different regions can be highlighted:

- the fingerprint region from 600 cm^{-1} to 1800 cm^{-1} : characteristic molecular vibrations such as stretching and bending of functional groups occurs;
- the silent region from 1800 cm^{-1} to 2700 cm^{-1} , where few vibrational modes occur;
- the 2800 cm^{-1} to 3600 cm^{-1} region where stretching modes of C-H, N-H and O-H bonds can be observed.

Numerous scientific studies have shown that specific regions provide significant information for cancer differentiation. For example, the range of 800 cm^{-1} to 1800 cm^{-1} is pertinent for gastric cancer [4], while the range of 800 cm^{-1} to 3100 cm^{-1} is relevant for brain cancer [5].

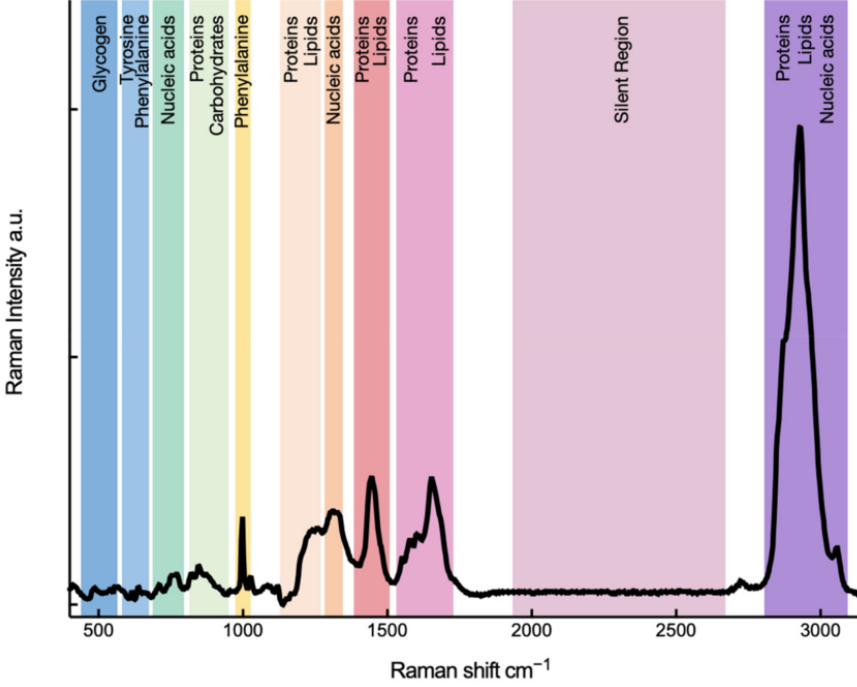


Figure 1.1: Raman spectrum of a cell fingerprint. Raman spectrum of a single cell of human primary glioblastoma U87 cell line, demonstrating various bands representative of cellular constituents [6].

1.1.1 Spontaneous Raman Scattering

Raman scattering can be described by examining a photon with energy $E_p = h\nu_p$ interacting with a molecule and assessing the energy dynamics involved.

The photon, which originates from a pump laser, may be absorbed by exciting a molecule to a virtual energy level $E_v > E_0$, where E_0 denotes the initial ground state. If the molecule subsequently relaxes to a state $E_1 > E_0$, it emits a lower energy photon with energy $E_s = h\nu_s < E_p (= E_v)$, resulting in inelastic scattering: part of the incident photon energy is converted into vibrational modes and its momentum is not conserved.

Fig. 1.2 represents the described energy exchange. This phenomenon is referred to as Spontaneous Raman scattering (SR). The frequency variation between the incident and emitted photons, arising from their difference in energy levels, is called the

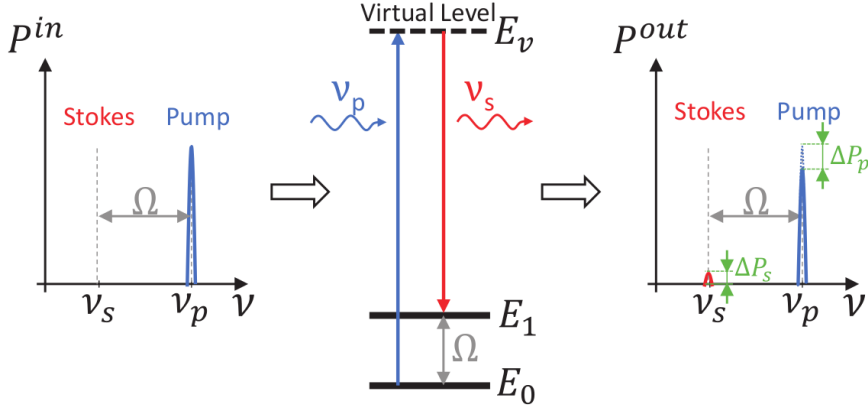


Figure 1.2: *Vibrational energy states in a spontaneous Raman experiment and Input/Output light intensities variation due to Raman scattering. E_0 represents the ground state of the system, while E_1 is a vibrational excited level, on the electronic ground state.*

Raman shift. The energy of the excited state E_1 can be calculated in relation to the ground state through the following relationship:

$$E_1 - E_0 = h(\nu_p - \nu_s) \quad (1.1)$$

However, the evaluation of level E_1 depends on the measurement accuracy of the Stokes shift $\nu_p - \nu_s$. This task is challenging due to the low probability of spontaneous Raman scattering, approximately 10^{-7} , resulting in a minimal emission rate and, consequently, a very small signal. This limitation translates into a long acquisition time which represents the main limit for this technique [7].

1.1.2 Stimulated Raman Scattering

To enhance the Raman signal by several orders of magnitude compared to spontaneous Raman scattering, a secondary light source with a wavelength different from that of the incident beam can be employed to induce relaxation transitions.

This technique is known as Stimulated Raman Scattering (SRS) and uses two laser beams with different frequencies ω_p and ω_s , also known as Pump and Stokes beams respectively [8]. In this kind of experiments, Pump can induce the relaxation transi-

tion to level E_1 while Stokes excites molecules to the virtual level E_v . Therefore, the Stokes beam serves to stimulate the Raman effect.

It results in an increase of the relaxation probability of molecules at energy level E_1 , which is different from the initial ground state E_0 . If the Raman shift $\Delta\omega = \omega_p - \omega_s$ matches a vibrational mode Ω of the molecules under investigation, the probability that some pump photons are scattered into the Stokes frequency increases significantly.

As a consequence, an optical power ΔP_s is added to the Stokes beam, while ΔP_p is subtracted from the Pump beam, as shown in Fig. 1.3. These power variations can be defined as Stimulated Raman Loss (SRL), which represents the power attenuation of the Pump, and Stimulated Raman Gain (SRG), as the gain of the Stokes. The energy balance for the Stokes and Pump can be expressed as:

$$\Delta P_{s,p} = P_{s,p}^{out} - P_{s,p}^{in} \quad (1.2)$$

where $P_{s,p}^{out}$ and $P_{s,p}^{in}$ denote, respectively, the intensity of the Pump (p) or Stokes (s) at the output and input of the sample.

In detail, it can be demonstrated that [9]:

$$\Delta P_{s,p} \propto \text{Im}(\chi_R^{(3)}) P_p^{in} P_s^{in} \triangleq k P_s^{in} \quad (1.3)$$

where $\chi_R^{(3)}$ represents the third-order nonlinear optical susceptibility, as SRS is a nonlinear optical phenomenon, and k represents the Stokes diffusion probability, which depends on the wavelength and the material:

$$P_s^{out} = P_s^{in} + \Delta P_s = P_s^{in}(1 + k) \longrightarrow SRG = \frac{P_s^{out}}{P_s^{in}} = 1 + k \quad (1.4)$$

with $k = \frac{\Delta P_s}{P_s^{in}}$, called normalized SRG, that ranges between 10^{-3} and 10^{-5} , as shown by empirical evidence [10].

1.2 Broadband SRS

To probe all possible vibrational levels of the sample under test, two methodologies can be employed: maintaining a constant Stokes frequency while varying the Pump frequency (from ν_p to

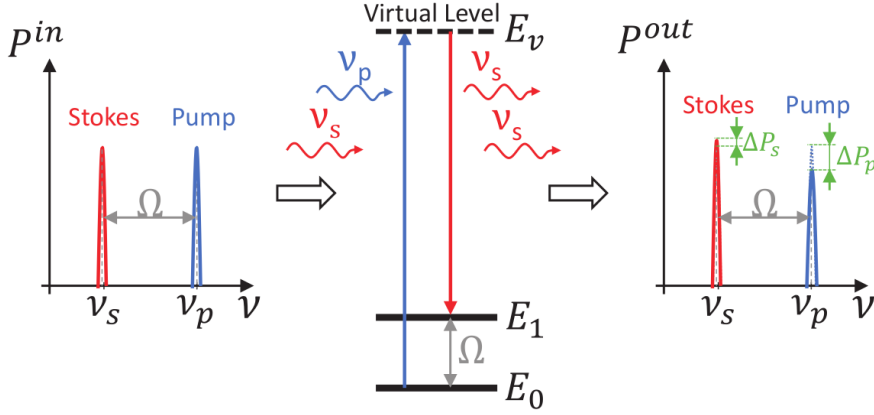


Figure 1.3: Energy levels in stimulated Raman scattering (SRS). SRL and SRG effects emphasized in P^{out} graph.

ν'_p) or, conversely, keeping the Pump frequency constant and adjusting the Stokes frequency (from ν_s to ν'_s), as illustrated in Fig 1.3.

In both scenarios, only one mode is excited at any given time, meaning that only a single wavelength of the Raman spectrum is obtained. This method is referred to as Single-Frequency SRS. To capture the complete Raman spectrum a temporal wavelength scan of either the Stokes or Pump laser is conducted by either sweeping ν_p or ν_s . However, despite SRS yielding a stronger signal compared to spontaneous Raman and therefore allowing for a reduced integration time, the scanning process is notably slow for imaging purposes.

A better approach for Raman imaging is represented by Broadband Stimulated Raman Scattering (SRS). This method consists in the simultaneous probing of multiple vibrational modes within the sample by utilizing either a broadband Stokes or a broadband Pump. In the first scenario, the excited molecules transition to various energy levels, whereas in the second one, the molecules are elevated to numerous virtual energy levels [11].

Figure 1.4 shows a simplified version of the energy levels of both situations. This approach allows for the simultaneous detection of different wavelengths, acquiring the Raman spectrum in a single measurement, by means of a photodiode array.

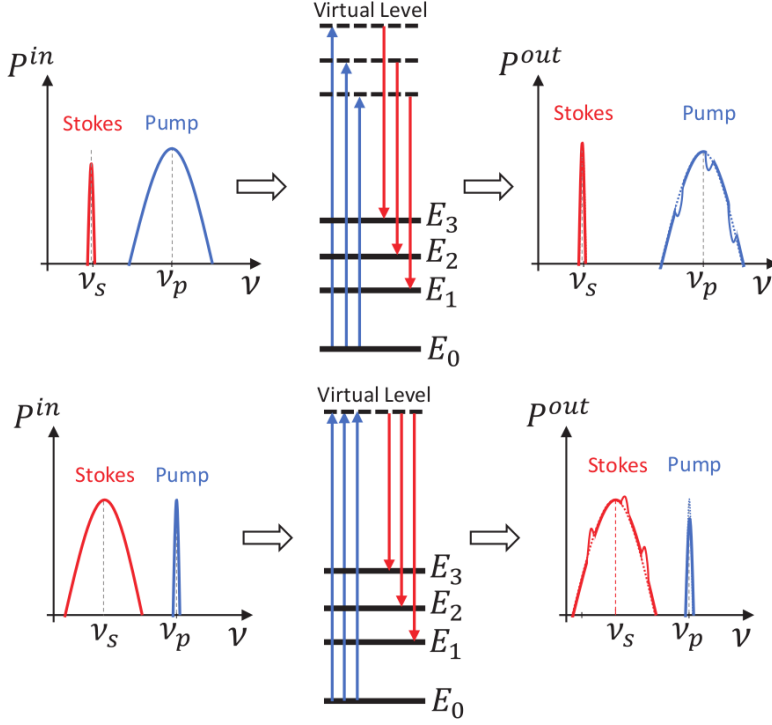


Figure 1.4: Different energy levels stimulated by SRS performed with a broadband Pump (top) or Stokes (bottom) pulses. Two different Raman effects can be observed: Stimulated Raman Loss (SRL, top) where the Pump intensity is reduced; Stimulated Raman Gain (SRG, bottom) where the Stokes intensity increases.

1.3 State-of-Art

To give this thesis work some context, the state of the art and commercial instruments available on the market for Raman spectroscopy are presented. Table 1.1 sums up the comparison with preexisting instruments.

- "Figuerola" - 2018 [12]: The pump is detected using a large-area silicon photodiode, followed by amplification through a custom-built transimpedance amplifier. The Raman signal is measured with a Zurich Instruments H2FLI lock-in amplifier. Spectral acquisition across the full Raman band-

width ($> 600 \text{ cm}^{-1}$) is achieved via a delay line and scanning mirrors. However, this approach introduces the main speed limitation of the system, with a dwell time of $t_{\text{dwell}} = 1.6 \text{ ms}$ for the complete spectrum.

- "Scotté" - 2019 [13]: The spatially dispersed Raman signal is projected onto a programmable digital micromirror device (DMD), which serves as a tunable spectral filter. This enables the sequential deflection of individual spectral components of the broadband laser into a commercial photomultiplier tube (PMT). The final image is reconstructed through a Fourier transform of the temporal signal. An additional advantage of this detection scheme is that it employs a single detector while operating at the shot-noise limit. In this configuration, three distinct wavelengths are acquired with a total dwell time of $330 \mu\text{s}$ using a laser power of 65 mW .
- "Audier" - 2020 [14]: In this work, the detection approach adopts chirped optical pulses combined with rapid delay scanning. The laser signal is collected by a photodiode coupled to a commercial lock-in amplifier. When applied to biological samples, the acquisition operates at the shot-noise limit, with a pixel dwell time of $t_{\text{dwell}} = 25 \mu\text{s}$, owing to the laser power being confined to a narrower spectral bandwidth ($\approx 200 \text{ cm}^{-1}$).
- "Crisafi" - 2023 [15]: This work presents a dual-wavelength,

Paper ref.	Number of eq. channels	total power (or power range)	Time per px
"Figueroa" [12]	60 (SE)	80 mW	1.6 ms
"Scotté" [13]	3 (SE)	65 mW	330 μs
"Audier" [14]	9 (SE)	35 mW	25 μs
"Crisafi" [15]	38 (SE)	950 μW	10 μs
"De la Cadena" VIBRA platform [16]	32 (DIFF)	1.28 mW - 19 mW	100 μs
This Work	76 (DIFF) 152 (SE)	75 μW - 23 mW	16 μs

Table 1.1: *State of the art comparison in stimulated Raman detection. SE: Single Ended Detection, DIFF: differential-balanced detection.*

self-synchronized fiber laser integrated with a compact multichannel lock-in amplifier for detection. The system provides a two-color synchronized output, enabling shot-noise-limited broadband SRS within the CH stretching region (2800–3100 cm^{-1}). The detection module suppresses electronic noise in the 1–10 MHz range, achieving the shot-noise limit with per-channel powers as low as 25 μW . This configuration delivers state-of-the-art SRS performance across the full CH spectrum, allowing parallel detection of up to 38 channels within 400 ns.

- "De la Cadena" 2022 [16]: This microscope integrates a broadband optical source, a compact 32-channel high-frequency custom lock-in amplifier, and in-line balanced detection for laser noise suppression. It enables acquisition of SRS spectra across the CH stretching region with high spectral resolution ($\approx 15\text{cm}^{-1}$) and fast integration times (44 – 1300 μs). By combining detailed spectral analysis with rapid data collection, the system is well-suited for label-free, non-invasive chemical imaging of biological samples.

Many other instruments have been developed for SRS signal acquisition and are reported in a recent review article [17]. Of particular interest is the commercial instrument Model 7210 (SIGNAL RECOVERY), used in [18]. This system enables parallel acquisition of up to 128 different wavelengths through an equal number of single-ended lock-in detection chains. However, it suffers from a significant limitation in acquisition speed, constrained by a maximum demodulation frequency of 50 kHz.

1.4 Optical Setup for Broadband SRS

The scheme reported in Figure 1.5 shows a simplified version of the optical setup adopted for a Stimulated Raman Spectroscopy experiment.

In SRS, synchronized Pump and Stokes laser pulses impinge on the sample, producing a decrease in the output power of the Pump beam (SRL), related to the molecular vibrations. Although the SRL signal is orders of magnitude larger than the

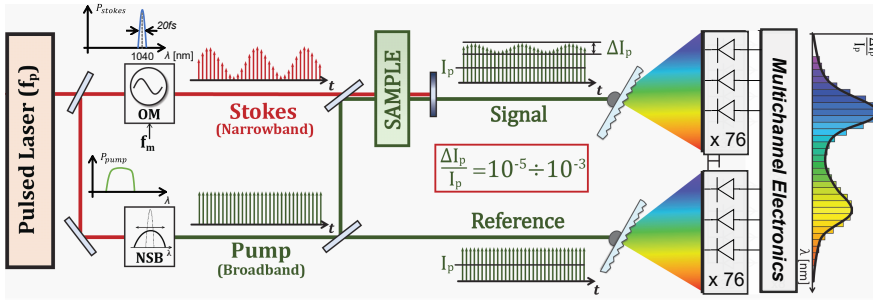


Figure 1.5: *Simplified optical setup for Broadband Stimulated Raman Spectroscopy. 80 MHz laser repetition rate. $\Delta I_p/I_p$ is considered as an absolute value, as for an SRL experiment it is negative.*

spontaneous Raman, it is still small, usually around $10^{-5} - 10^{-4}$ [2].

To detect it, the Stokes beam is modulated in the 1-10MHz range with an acusto-optic modulator, with the aim to move the signal of interest where a lower laser intensity noise has been observed, as better explained in section 1.4.2. In the case of broadband SRS, a broadband Pump beam is used to stimulate multiple wavelengths, enabling the acquisition of an entire Raman spectrum in a single measurement.

After impinging simultaneously on the sample, the Stokes beam is filtered out while the Pump beam is spatially spread over a 76-elements photodiode array.

In order to be less sensitive to the amplitude fluctuation, as it will be explained in the following section, a Pump-beam replica is acquired as "Reference" beam and then subtracted to the Raman signal path, implementing a so-called "balanced detection" [11].

1.4.1 Laser Source

In the setup adopted for this project, a narrowband Stokes laser and a broadband Pump laser are employed. Since both are generated from the same laser source, they remain mutually coherent. A detailed scheme is reported in Figure 1.6.

The commercial Yb-fiber laser "Fidelity coherent HP" produces the main beam (also called "Fundamental"). It is a pulsed laser beam with wavelength of 1040 nm, 140 fs pulse duration and repetition frequency of 80 MHz [19]. This main beam is split

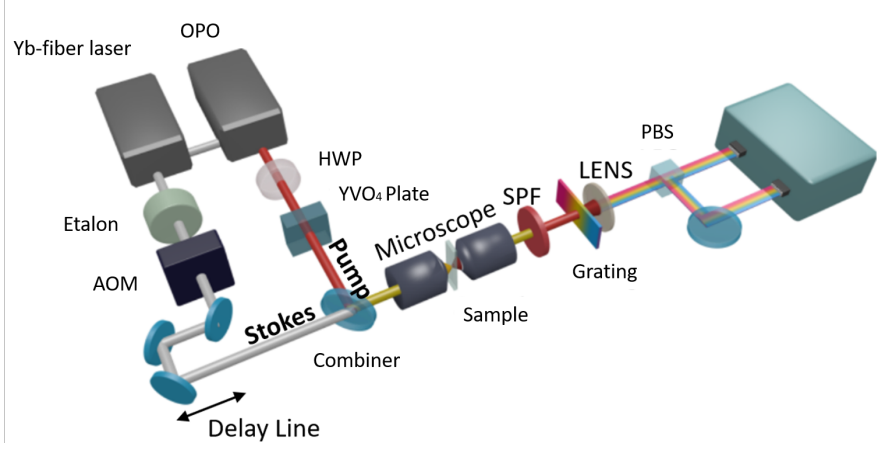


Figure 1.6: Optical Setup block diagram with the In-line balanced detection. *OPO: optical parametric oscillator, AOM: acusto-optic modulator, HWP: half wave polarizer, YVO₄ plate: birefringent crystal, SPF: short-pass filter, PBS: polarized beam splitter.*

into two branches:

- The Stokes laser consists of very short pulses (1 ps FWHM duration) with a wavelength $\lambda_s = 1040 \text{ nm}$ and with narrow spatial band ($BW = 20 \text{ cm}^{-1}$). It is obtained by passing the main beam through an Etalon filter and then it is modulated.
- The second beam is used to pump an optical parametric oscillator (OPO) that generates the broadband Pump beam ($BW > 500 \text{ cm}^{-1}$) with $\lambda_p = 715 - 870 \text{ nm}$ and pulse duration $< 20 \text{ fs}$.

1.4.2 Relative Intensity Noise

Laser power fluctuations, often referred to as Intensity Noise, can hide the Raman signal; therefore, they need to be compensated. This noise can be quantified using the Relative Intensity Noise (RIN) parameter, which generally indicates the noise performance of a laser source and is defined as:

$$RIN = 10 \cdot \log_{10} \left(\frac{S_{laser}}{\bar{P}^2} \right) \quad (1.5)$$

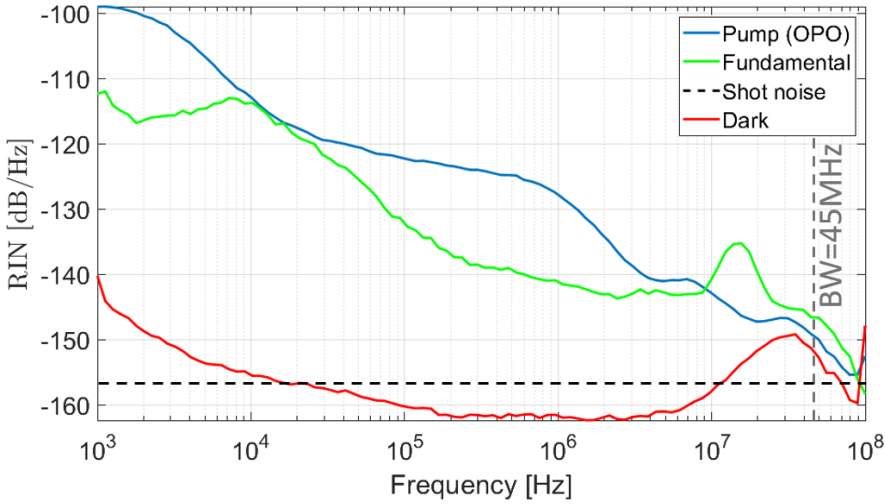


Figure 1.7: *RIN measurement of Commercial laser Fidelity Coherent HP. The measurement was carried out with a 45 MHz bandwidth photodiode connected to a commercial lock-in amplifier (HF2LI, Zurich Instruments). The red trace corresponds to the noise spectral density sampled in the absence of laser illumination (i.e., the instrumentation noise floor) and normalized to the same mean power of 2.6 mW.*

It is a useful parameter for quantifying and comparing laser noise performance, since it is a kind of "figure of merit" representing the spectral density of the laser power $S_{laser}[W^2/Hz]$ normalized with respect to its mean power $\bar{P}$.

Figure 1.7 shows the measured RIN of the fundamental frequency and of the Pump for Fidelity Coherent HP commercial laser source. The graph distinctly indicates that the RIN for both the Pump and Fundamental beams diminishes as frequency increases, implying that modulation techniques represent an effective approach.

Specifically, the bandwidth of 1-10 MHz yields the lowest relative intensity noise levels when considering both noise sources, thus establishing this frequency range as optimal for optical modulation. Furthermore, the contribution of intensity noise can be addressed through differential measurement. The strategy involves capturing two laser beams: the Raman signal and the reference beams, both of which are influenced by the same intensity noise.

1.4.3 In-Line Balanced Detection Technique

As shown in Figure 1.6, the signal beam crosses the sample, and according to the Lambert-Beer Law, it is attenuated. To compute a fair difference between the Signal and the Reference, the latter should be attenuated by the same amount. To do so, Pump and Reference beams cross the sample at the same position, thus maintaining their balance during image acquisition but with different polarizations that allow the distinction of the two beams. However, only the Pump beam will be affected by the Raman Loss since the Reference beam is not overlapped in time with the Stokes; for this reason the interaction with the Reference beam does not occur.

This technique is called In-Line Balanced Detection (IBD) and its basic principle is represented in Figure 1.8. The IBD technique utilizes a half-wave plate (HWP) and a birefringent plate to produce a time-delayed, polarization-multiplexed replica of the Pump, serving as a Reference. In the absence of the IBD approach, variations in power between the two replicas during frame acquisition would reduce the effectiveness of common-mode noise cancellation. [20]

1.5 Proposed Solution: CRIMSON Multichannel Lock-in

Given the high repetition rate of the laser pulses (80 MHz) and the optical setup shown in Figures 1.5 and 1.6, in order to process all photogenerated signals in parallel, the multichannel Lock-In Amplifier (mLIA) is a crucial component [16].

The use of a lock-in detection technique represents the most suitable approach to effectively extract the modulated signal component from the background noise, since it allows to modulate the signal where the laser noise is lower (the laser-noise spectrum noise decreases monotonically with frequency as shown in Figure 1.7), and subsequently demodulation back to base-band.

The aim of this work is to develop novel instrumentation for rapid Raman spectrum acquisition by combining broadband SRS spectroscopy with multichannel, low-noise electronics based on lock-in techniques.

In order to obtain a fast acquisition (with a time per pixel

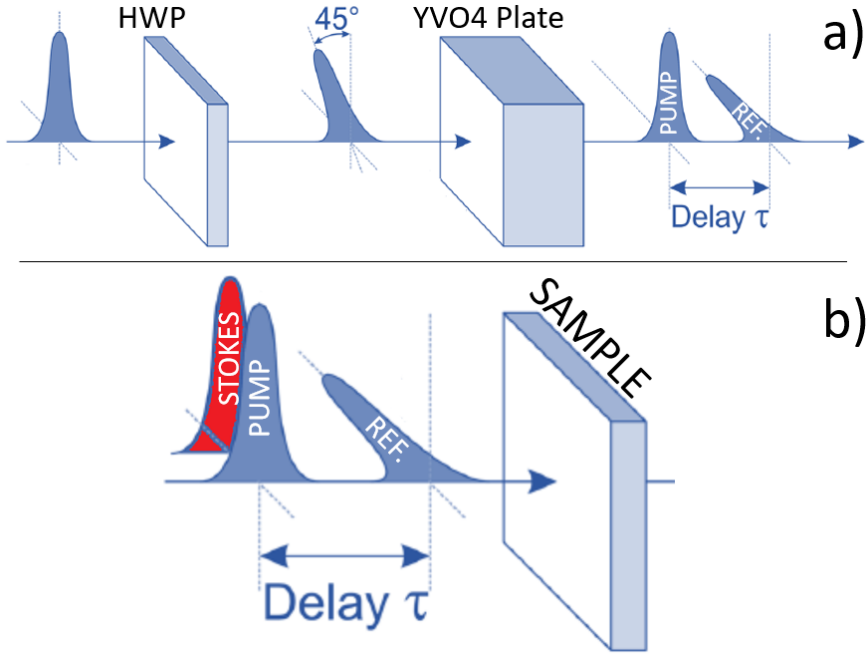


Figure 1.8: *Simplified scheme illustrating: of a) Generation of the Pump and reference beams with orthogonal polarization using a HWP and a birefringent crystal (YVO₄); b) the interaction of Pump, Stokes, and Ref. pulses with the sample in the IBD configuration.*

smaller than $100\mu s$), each wavelength is processed by a dedicated channel, and parallel processing of all acquisition channels is mandatory. To achieve a compact and efficient platform, the front-end amplifiers together with the lock-in demodulation stage have been integrated into a custom-designed circuit, presented in chapter 2. The complete system developed, based on the Custom IC, is presented in chapter 3. It is based on Broadband SRS detection and its main characteristics are:

- 76 channels;
- detection of weak Raman signals (down to few ppms);
- electronic noise smaller with respect to shot noise in the frequency range of interest (1-10 MHz);
- DC and AC separated outputs, useful for Raman normalization;

- compact platform.

After the electrical validation, the platform is validated also on an optical bench. The obtained results are reported in chapter 4.

CHAPTER 2

8-Channel ASIC for Broadband Raman Spectroscopy

Part of this work is reported in the paper [21].

The principal objective of this chapter is the description of an 8-channel integrated circuit specifically developed to acquire optical signals for Broadband Stimulated Raman Spectroscopy.

Compared to the prototype previously developed, extensively described in the referenced work [22], the new integrated circuit (IC) must meet more stringent specifications, which have required a reassessment of the structures previously adopted. Although part of the design had already been implemented and validated in the previous prototype and has been readopted in the present work, substantial changes have been carried out in order to improve performance and adapt the system to the new requirements.

This chapter describes in detail the new configuration of the low-noise amplifier and the differential subtractor, putting em-

parameter	Prototype	This work (CRIMSON)
Working mode	Differential	Differential / Single Ended
# of channels	4	8 / 16
Laser repetition rate	80 MHz	40 or 80 MHz
P_{min}	50 μW	10 μW
P_{max}	600 μW	500 μW
f_m	1 – 10 MHz	1 – 10 MHz
# of gain config.	4	18

Table 2.1: *Principal specifications changes of this work with respect to the prototype [22].*

phasis on the new features that extend the experimental possibility compared to previous work.

The circuit improvements include reduction of the input electronic noise with the aim to detect a smaller optical power, increase of the preamplifier and subtractor gains to better amplify the signal, enhancement of the internal logic for a more versatile circuit and scaling up the number of channels in order to achieve a better spectral resolution in the Raman Spectrum. Table 2.1 summarizes the changes between the 4-channel Prototype and the 8-channel version.

2.1 Single Channel Overview

The acquisition chain for a single spectral line of the Raman Spectrum consists of two preamplifier stages that integrate the photogenerated current coming from the laser, one for the Raman signal path and one for the Reference. Each premaplifier is equipped with an additional feedback path able to manage the pulse mean current, since the photogenerated mean current is not zero and the stage will saturate by integrating the DC component of that current.

Afterwards, in order to effectively decrease the laser noise, a Variable Gain Amplifier stage (VGA), controlled by a suitable control network called Automatic Gain Control (AGC), must balance the two signal paths, keeping the attenuation of the two beams independent of the differences between the two optical paths. Finally, two differential subtractor stages, for amplifying

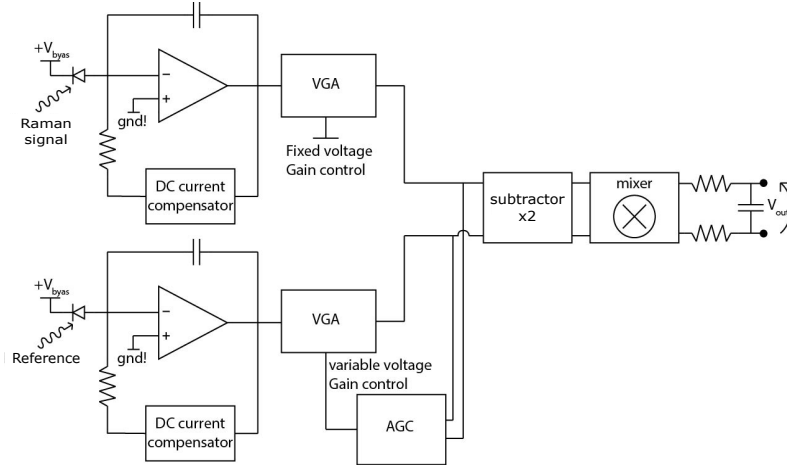


Figure 2.1: *Simplified scheme of a single channel of the ASIC. Main blocks: Charge Preamplifier with additional feedback for DC current compensation; Voltage Gain Adjuster (VGA) with Automatic Gain Control (AGC) to further balance the Reference and signal paths; 2 subtractor stages; Passive Mixer for demodulation and Low Pass Filter.*

the Raman signal and reducing the common-mode laser noise, make the Raman signal available for lock-in demodulation thanks to a passive mixer driven by a square wave.

The complete structure consists of eight identical channels: a simplified version of a single channel is shown in Figure 2.1.

2.2 Charge Amplifier

The input stage of the integrated circuit is composed of two identical preamplifying structures, one for the signal and one for the reference photodiode. This block amplifies the two input current trains of pulses and provides to the output the signal and reference DC values for the SRS signal normalization.

For this purpose, a sophisticated charge amplifier is employed, featuring capacitive feedback and an additional feedback network to handle the DC current from the photodiode. This circuit is current-in to voltage-out converter, so it acts as a trans-impedance amplifier (TIA).

The amplifier topology with capacitive feedback is preferred because, differently from a resistive-feedback amplifier (the classi-

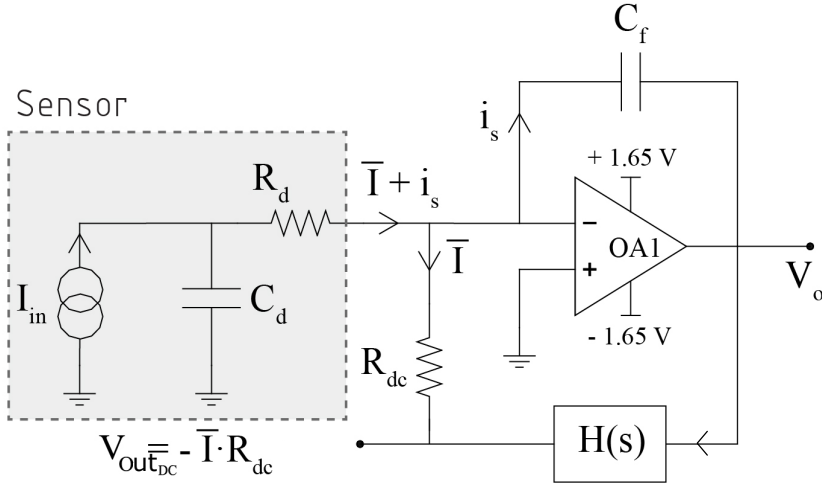


Figure 2.2: ASIC input stage with the mean current discharging network. The current I_{in} can be seen as the superposition of $\bar{I}$ which is the average current and i_s the Raman signal photogenerated current.

cal TIA), it avoids the trade-off between noise and gain. However, a drawback exists: the stage tends to saturate due to the mean current accumulating in the feedback capacitance (C_f). To solve this issue, a mean current discharge network is implemented, eliminating the need of a feedback resistor or periodic reset [23].

2.2.1 DC Current Discharge Network

As previously said, the amplifier output will saturate after a few pulses in absence of a discharge network of the feedback capacitance. The input DC current depends on the mean optical power impinging on the photodiode.

To avoid stage saturation, it is necessary to use a circuit that continuously reads the output average voltage of the charge preamplifier and appropriately adjusts the mean current $\bar{I}$, injected into the virtual ground node, to keep the desired output mean voltage.

Additionally, in order for the Raman microscope to work correctly, it is crucial to read the mean incident power on the photodiode, as this works as the normalization factor required to compare the intensity of the Raman signals to various optical

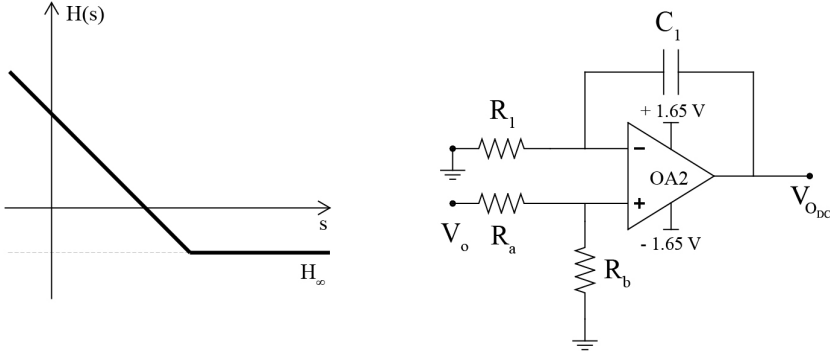


Figure 2.3: Final circuit for $H(s)$ and its relative transfer function.

wavelengths. Therefore, every acquisition channel must measure both the DC signal component and the Raman modulated harmonics.

As shown in Figure 2.2, the proposed solution presents a circuit $H(s)$ in negative feedback with charge amplifier, in order to produce a voltage $V_{out,DC}$ proportional to the mean input current at the output. This voltage is converted into a current by a resistance R_{DC} , which removes the mean current $\bar{I}$ from the integrator path, avoiding the saturation of the stage.

One terminal of R_{DC} is connected to the virtual ground, so the other one is equal to $V_{out,DC} = \bar{I} \cdot R_{DC}$, and then proportional to the mean incident power $\bar{P}$, that with this configuration is ready to be read as previously stated.

Now, the last element to be defined is the transfer function $H(s)$ and the circuitry needed to implement it. The additional feedback loop given by $H(s)$ and R_{DC} should work only with the DC signal, leaving the contribution of i_s (AC) in the integrator stage. $H(s)$ might be a non-inverting integrator with transfer function:

$$\frac{1}{sR_1C_1}$$

In addition, in the region $\omega \geq 1 \text{ MHz}$ the gain of $H(s)$ must be as low as possible to not interfere with the proper operation of the charge amplifier, which should operate as an integrator where the Raman signal is present.

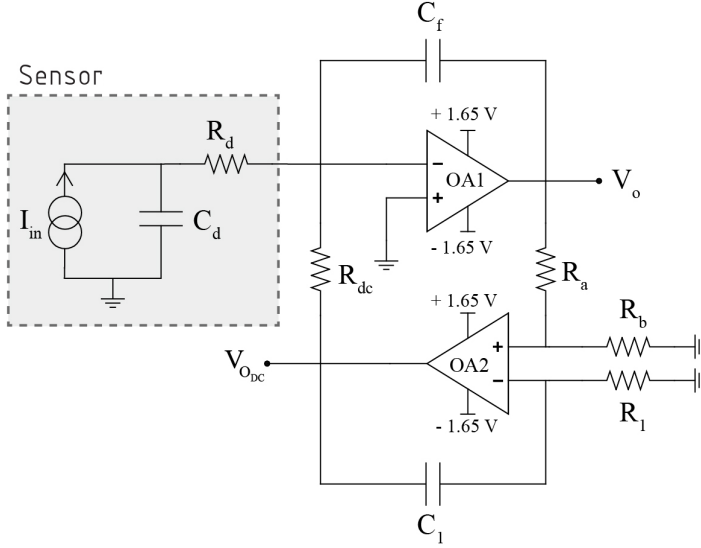


Figure 2.4: First stage. Charge preamplifier with capacitive feedback and DC current compensation network.

Figure 2.3 shows the transfer function and the circuit implemented for $H(s)$. It can be highlighted that the resistive divider is useful to reduce the gain of $H(s)$ at high frequency.

It is possible to formulate an analytical expression of $H(s)$

$$H(s) = \frac{R_b}{R_a + R_b} \frac{1 + s C_1 R_1}{s C_1 R_1} = \frac{1}{k} \frac{1 + s C_1 R_1}{s C_1 R_1} \quad (2.1)$$

and calculate the G_{loop} of the input stage:

$$G_{loop}(s) = -\frac{1}{s C_f R_{DC} k} \cdot \frac{1 + s C_1 R_1}{s C_1 R_1} \quad (2.2)$$

with $k = (1 + R_a/R_b)$, that is the resistive divider at the non-inverting input of OA2. The final scheme of the whole input stage is shown in Figure 2.4.

2.2.2 Stability and Transfer Function

Now, to determine whether the system is stable, the hypothesis $f_z = \frac{1}{2\pi R_1 C_1} \ll f^*$ should be tested, where f^* is the frequency such that $|G_{loop}| = 1$. For this reason are defined $R_1 = 1 M\Omega$

and $C_1 = 2\text{ pF}$ to obtain $f_z = 80\text{ kHz}$, that is a very low value more than a decade before the minimum modulation frequency $f_m = 1\text{ MHz}$. G_{loop} around the frequency f^* can be rewritten as:

$$G_{loop} \approx \frac{1}{sC_f R_{DC} k} \quad (2.3)$$

At this point, it is possible to set the equation $|G_{loop}(s)|_{\omega=\omega^*} = 1$ and calculate f^* :

$$f^* = \frac{1}{2\pi C_f R_{DC} k} \quad (2.4)$$

In order to keep the preamplifier stage stable and to guarantee enough phase margin, C_f and R_{DC} must be properly sized. Understanding the closed loop transfer function is necessary for an accurate sizing of the circuit:

$$G_{ac} = \frac{V_o}{I_{in}} = -\frac{sC_1 R_1 k R_{DC}}{s^2 k C_f R_{DC} C_1 R_1 + sC_1 R_1 + 1} \quad (2.5)$$

In order to obtain an ideal-integrator behavior in the range of interest, both poles of the equation 2.5 must be smaller than 1MHz. Therefore, the circuit behaves as an ideal integrator and its transfer function is:

$$G_{HF} = \frac{V_{out}}{I_{in}} = -\frac{1}{s C_f} \quad (2.6)$$

In summary, this topology minimizes the input-referred noise of the DC resistor by allowing its value to be maximized, which is not achievable in the standard charge amplifier structure with a feedback resistor, where increasing the feedback resistance value conflicts with the pulse amplitude and the voltage dynamic range.

Once the R_{DC} value is fixed, the parameter k provides an additional degree of freedom to set the pole frequency, while C_f can be selected solely based on the incoming pulse amplitude. In contrast, in a conventional topology, R_f and C_f simultaneously determine all these parameters, which are typically in trade-off [23].

Config	P_{in} (I_{mean})	R_{DC}	C_f	f_{cut}	$\sqrt{S_{i,shot}}$	$\sqrt{S_{i,eln}}$
0 0 0	$10 \mu W$ ($5 \mu A$)	$200 k\Omega$	$100 fF$	$326 kHz$	$1.266 \frac{pA}{\sqrt{Hz}}$	$0.467 \frac{pA}{\sqrt{Hz}}$
0 0 1	$20 \mu W$ ($10 \mu A$)	$100 k\Omega$	$150 fF$	$431 kHz$	$1.79 \frac{pA}{\sqrt{Hz}}$	$0.545 \frac{pA}{\sqrt{Hz}}$
0 1 0	$40 \mu W$ ($20 \mu A$)	$50 k\Omega$	$250 fF$	$513 kHz$	$2.53 \frac{pA}{\sqrt{Hz}}$	$0.715 \frac{pA}{\sqrt{Hz}}$
(0 1 1)	$80 \mu W$ ($40 \mu A$)	$25 k\Omega$	$480 fF$	$535 kHz$	$3.58 \frac{pA}{\sqrt{Hz}}$	$1.03 \frac{pA}{\sqrt{Hz}}$
1 0 0	$160 \mu W$ ($80 \mu A$)	$12.5 k\Omega$	$960 fF$	$534 kHz$	$5.06 \frac{pA}{\sqrt{Hz}}$	$5.06 \frac{pA}{\sqrt{Hz}}$
(1 0 1)	$320 \mu W$ ($160 \mu A$)	$6.25 k\Omega$	$1.92 pF$	$528 kHz$	$7.16 \frac{pA}{\sqrt{Hz}}$	$2.88 \frac{pA}{\sqrt{Hz}}$

Table 2.2: Summary table of the various operative condition of the input stage. It is supposed that the input optical power impinges on a photodiode with a responsivity of $0.5A/W$. The last column reports the values of the electronic noise of the stage @1 MHz. It is worth to notice that the shot noise is the limiting noise contribute for this application.

2.2.3 Sizing and operating Conditions of the Stage

Once the circuit architecture is defined, all components are calculated to meet the project constraints listed in Table 2.1.

Figure 2.5 shows the contribution of the electronic noise spectral density compared with the photogenerated shot noise spectral density.

According to the noise analysis results, the maximum input power situation ensures the highest signal to noise ratio by keeping the shot noise the dominant component with respect to the thermal noise of the stage.

The circuit is intended to be as flexible as possible, so it could operate at minimum power level of $P_{in} = 10 \mu W$ with shot noise of $S_{shot} = (1.266 pA/\sqrt{Hz})$, that could be comparable to the electronic noise of this operating condition. Three digital control signals, programmed by an external controller, are provided to set the desired gain configuration.

Table 2.2 lists the main parameters for the different working conditions.

Figure 2.6 shows the parametric AC simulation in the six cases.

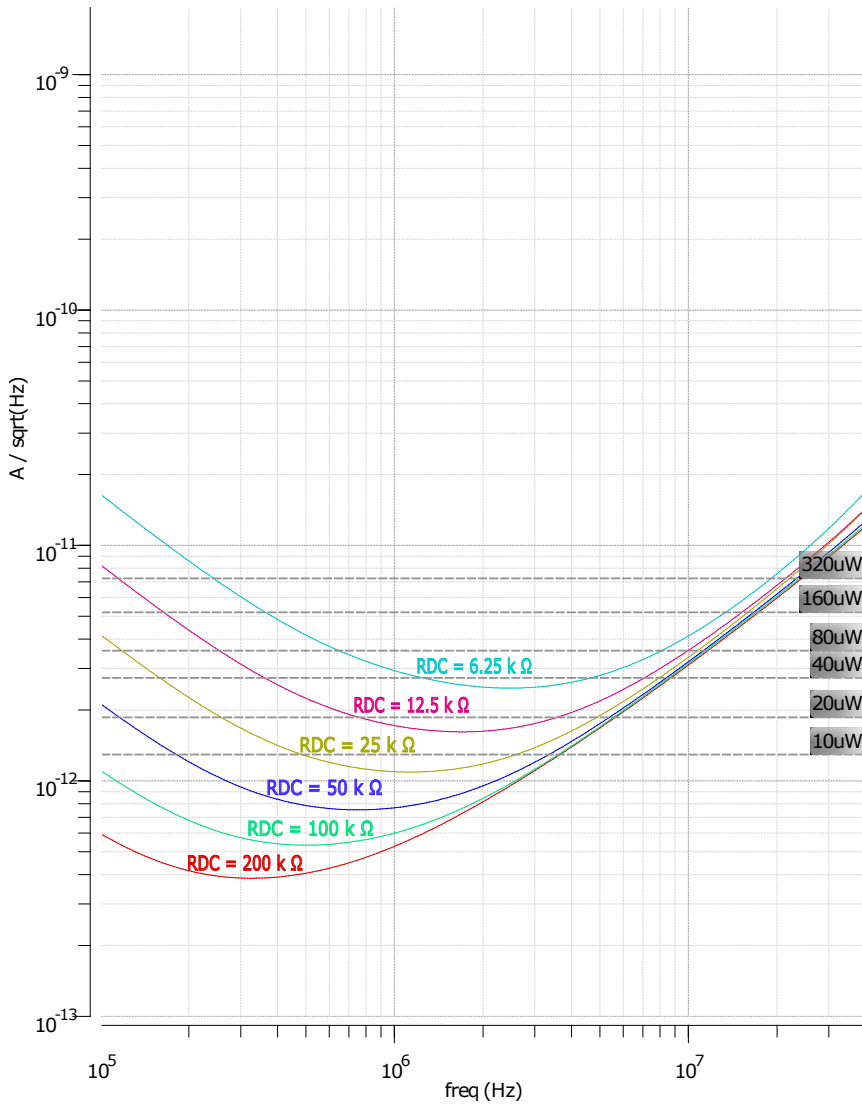
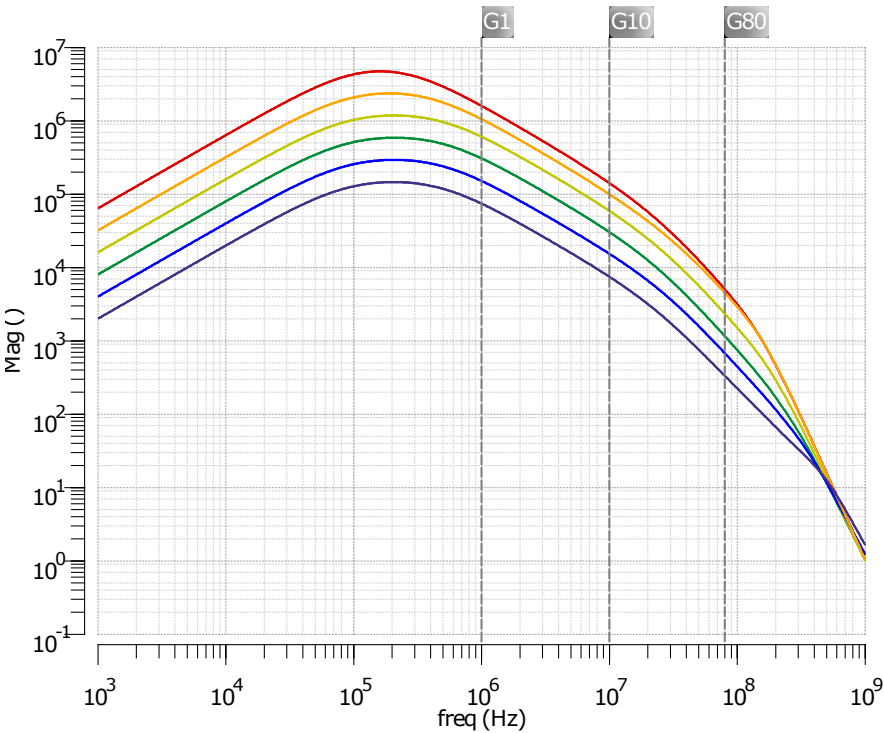


Figure 2.5: Input referred power spectral density in the six different operative conditions and comparison with the shot noise spectral density for a given optical power.



	B1	B2	B3	G1	G10	G80
x				1.0MHz	10.0MHz	80.0MHz
(VF("/out_ac") / IF("/I7/PLUS"))						
(VF("/out_ac") / IF("/I7/PLUS"))	-1.65	-1.65	-1.65	1.60465M	142.055k	5.07171k
(VF("/out_ac") / IF("/I7/PLUS"))	-1.65	-1.65	1.65	308.897k	30.5267k	1.16327k
(VF("/out_ac") / IF("/I7/PLUS"))	-1.65	1.65	-1.65	608.756k	59.3868k	2.35293k
(VF("/out_ac") / IF("/I7/PLUS"))	-1.65	1.65	1.65	151.987k	15.4439k	681.157
(VF("/out_ac") / IF("/I7/PLUS"))	1.65	-1.65	-1.65	1.05595M	100.01k	4.54082k
(VF("/out_ac") / IF("/I7/PLUS"))	1.65	-1.65	1.65	308.897k	30.5267k	1.16327k
(VF("/out_ac") / IF("/I7/PLUS"))	1.65	1.65	-1.65	608.756k	59.3868k	2.35293k
(VF("/out_ac") / IF("/I7/PLUS"))	1.65	1.65	1.65	74.6708k	7.51839k	335.222

Figure 2.6: Simulation of the AC gain in the six different conditions (that can be selected by setting the value of three bits B1, B2 and B3). The table below summarizes the values of the gain at 1, 10 and 80 MHz.

2.3 Autobalancing Network

As already stated in the paragraph 1.4.2, the dominant noise contribution is the RIN caused by fluctuations of the optical power during the laser beam generation. Therefore, a differential signal measurement was employed, in order to consider the noise as a common mode signal that can be rejected by a differential circuit.

If In-Line Balanced Detection (IBD) technique is not adopted, the different optical paths of the signal and reference need the implementation of an appropriate electronic balancing: a custom structure that automatically balances the two input powers is properly designed. The circuit is placed after the preamplifiers and it exploits a Variable Gain Amplifier (VGA) and an Automatic Gain Control (AGC) network. The autobalancing circuit is a closed loop that reads the difference between Signal and Reference and then turns it into a control signal that regulates the bias current of the Reference VGA, modifying the gain of VGA_{ref} . Figure 2.7 shows a simplified block diagram of the autobalancing circuit.

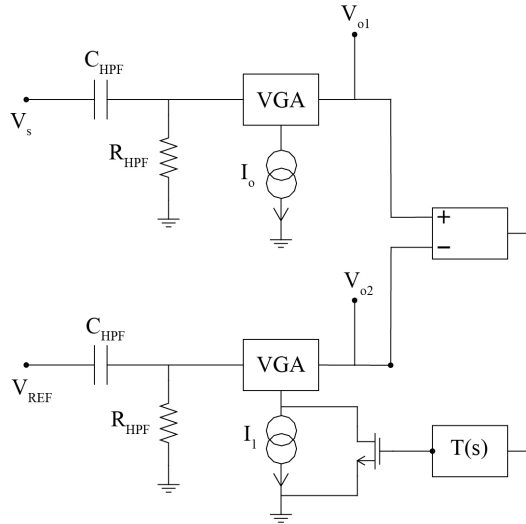


Figure 2.7: Block diagram of the AGC network.

2.3.1 Variable Gain Amplifier (VGA)

The Variable Gain Amplifier (VGA) is an open-loop circuit that should respect specific project requirements, including good input and output dynamic range, high linearity, and a range of gains that may compensate for amplitude variations of about $\pm 30\%$. The VGA implementation circuit is a differential amplifier that operates in open-loop, where the bias current is variable thanks to a transistor working in parallel with the bias current source of the differential pair. This transistor is controlled by the V_c control voltage. A variation in the bias current causes a change in the gain of the stage. Figure 2.8 depicts the variable current VGA in the Reference path. The gain of the VGA can be calculated as:

$$G_{VGA} \simeq \frac{g_{m1,2}}{2} (r_{08} // R) G_{sf1} G_{sf2} \quad (2.7)$$

where G_{sf1} and G_{sf2} are the gains of the source follower at the input and output of the VGA.

2.3.2 AGC Circuit

After clarifying the Variable Gain Amplifier working mode, it is necessary to discuss how the control loop operates to enable the equalization of the two signals. It should be noted that the automatic gain control is required since, from pixel to pixel, the amplitude of the signal transmitted from the sample might vary by as much as 30 % from the nominal signal.

The amplitude of the signal at the output of the VGA is mea-

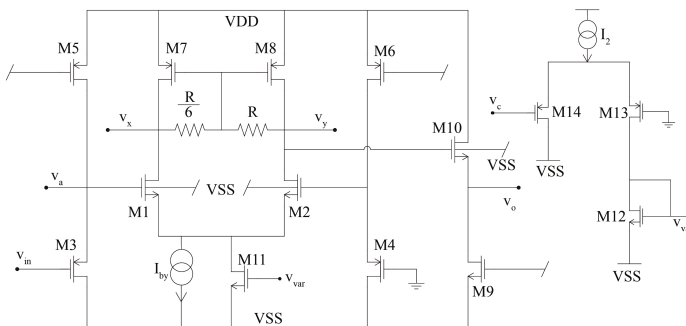


Figure 2.8: *Schematic of the VGA.*

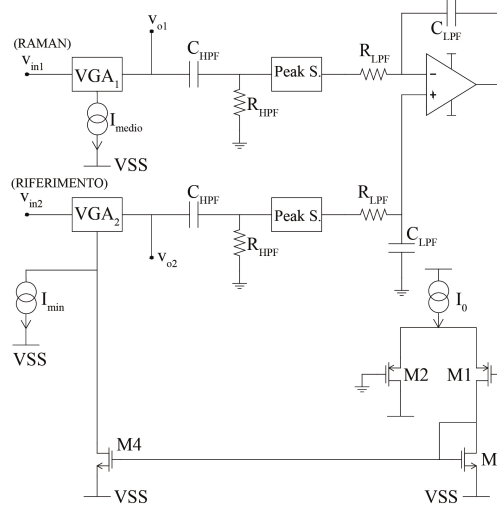


Figure 2.9: Schematic of the AGC network.

sured with a peak stretcher and the control loop works to eliminate any effects related to the phase shift between the two paths by bringing the amplitude of the reference signal to the same level as the signal passed through the sample, including the small Raman contribution.

The high-pass filter at the output of the VGA is used to filter the bias voltage of the stage itself and maintaining the harmonics of the frequency f_p without worrying about the Raman signal.

The block after the HPF is the differential integrator, which measures the average value of the difference between the two amplitudes and controls the gain of the VGA_{ref} through its output. It is implemented with a non-inverting integrator for the signal coming from the Reference path and an inverting integrator for the Raman signal path. Therefore, it fulfills the double function of amplifying the DC signal, that provides information on the power of the signal, and subtracting the two input signals. Thus, its ideal transfer function is calculated as follows:

$$H_{diff}(s) = \frac{v_c}{v_{x2} - v_{x1}} = \frac{1}{s C_{LPF} R_{LPF}} \quad (2.8)$$

where V_c is the differential integrator output, V_{x1} and V_{x1} are, respectively, the output of the peak stretcher of the Raman sig-

nal path and the reference path. Finally, the voltage provided at the output of the integrator is applied to the gate of the transistor M_1 , whose current is mirrored in the transistor connected in parallel with the bias current generator, as illustrated in Figure 2.9, controlling the gain of the VGA along the reference path. The feedback loop operates to enforce the condition $V_{o2} = V_{o1}$ [22].

2.4 Fully-Differential Subtractor

After the Automatic Gain Control stage, a cascade of two differential subtractors, one more than in the prototype project, is employed. It is helpful to have the differential signal amplified twice to increase the output signal, since the circuit has a smaller minimum input power than the old implementation. The first subtractor is fed by two waveforms with the same amplitude. However, the small Raman signal is superimposed on one of them, whereas the second one is only a reference signal. By using a differential readout, it is possible to eliminate the laser noise contribution and extract the useful information of the Raman signal.

The topology of a single fully differential subtractor consists of an AC-coupled differential amplifier designed to ideally amplify only the Raman signal while compensating for the high-frequency component generated by the pulsed laser. The fully differential topology allows to double the output voltage swing with respect to a single-ended amplifier and to use a CMOS double-balanced mixer as the following stage.

According to the Figure 2.10, a T-network has been implemented to place the pole introduced by the feedback capacitor C_2 at low frequencies and thus achieve a transfer function beyond the pole determined by the ratio of the capacitor values. The T-topology has been adopted because it allows the realization of a relatively high equivalent resistance without occupying excessive area in the integrated circuit.

In addition to increasing the number of stages to achieve higher overall gain, each subtractor was made more flexible by adding switches in order to make the gain user-selectable. A feedback capacitor $C_{2, //}$ and a pass transistor switch are added in parallel to the former feedback capacitance C_2 : by closing the

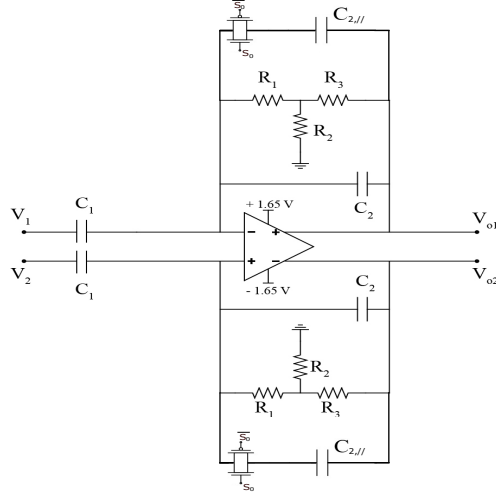


Figure 2.10: Schematic of the subtractor.

switch (controlled by to an external bit s_0) the subtractor gain can be varied. The circuit is shown in Figure 2.10 and the gain of a single stage is approximately equal to $\frac{C_1}{C_2}$ or $\frac{C_1}{C_2 + C_{2,II}}$.

2.5 Demodulation Mixer

The last component of the acquisition chain is the mixer, useful for signal demodulation. It is a square-wave mixer implemented with four switches that are controlled by a clock set to the demodulation signal frequency, as shown in Figure 2.11.

The switches were implemented using pass-transistor technology to improve symmetry and, in order to prevent charge injection issues of the clock, it was decided to size the pMOS areas to be equal to the corresponding nMOS areas, in order to make the parasitic capacitances equal as first approximation.

So, V_{out} is connected alternatively to $v_{o1} - v_{o2}$ and $v_{o2} - v_{o1}$. This operation is analogous to multiplying a sinusoidal signal by a square-wave with a zero mean value. However, the DC component of the signal is transformed into a square-wave with a zero mean value, providing a non-null signal at the demodulation frequency.

Furthermore, it was decided to insert a resistance $R = 20\text{ k}\Omega$ in

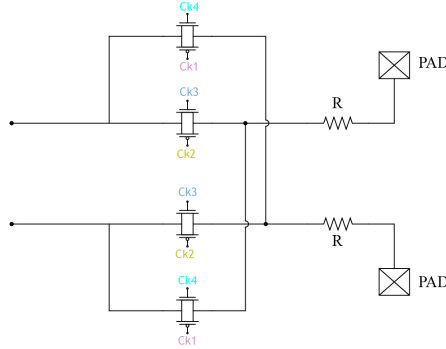


Figure 2.11: *Real mixer with the pass-transistor switches.*

series with the mixer output branches to decouple the subtractor and the capacitances of the output PADs.

A common issue with this simple mixer configuration is the possibility of imperfect synchronization between the main clock and the antiphase clock that controls the switches. This could lead to two undesirable operational states: the first is when the transistors are both turned off, and this causes only a small inaccuracy in the demodulated voltage; the other consists in the switches both closed and could be fatal to the operation of the system. The circuit shown in Figure 2.12 is used to avoid this situation, implementing the so called "brak-before-make" mode (BBM).

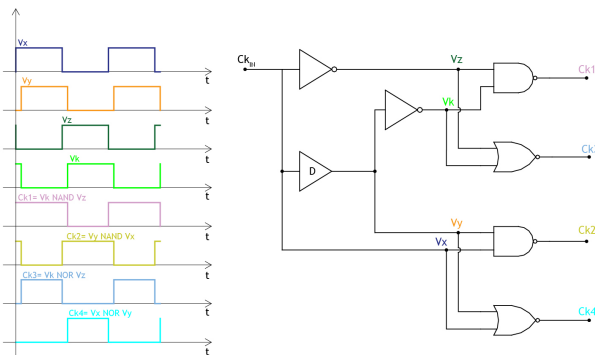


Figure 2.12: *Digital circuit for the generation of the four non-overlapping clock, with the relative time diagram (on the left).*

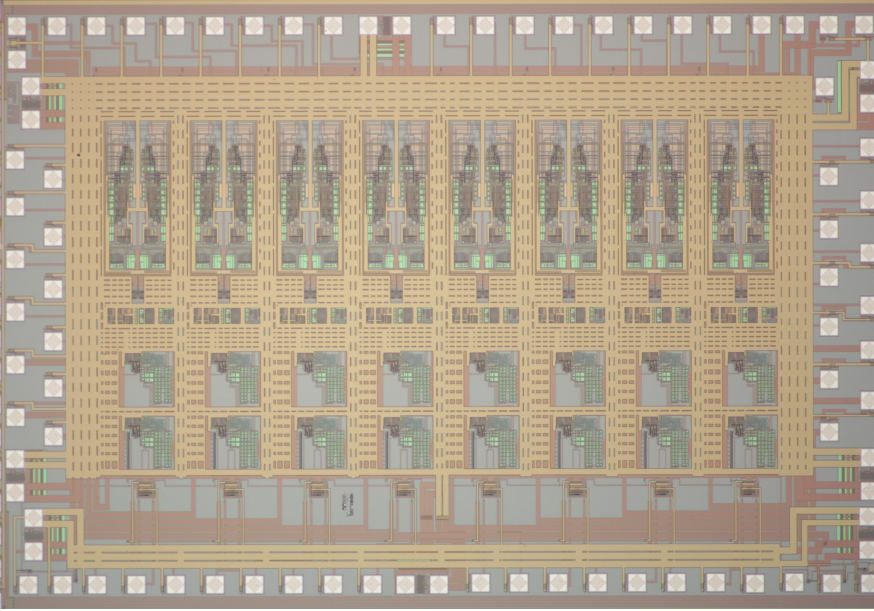


Figure 2.13: *ASIC micrograph.*

2.6 Overall ASIC

The ASIC has been implemented in AMS 0.35 μm CMOS technology. The IC die is composed of 8 independent differential channels and it occupies an area of 12 mm^2 . It has 84 pads in total, which are positioned all around the 8 channels and has a nominal power consumption of $\approx 500\text{ mW}$ with a power supply of 3.3 V [21]. A micrograph of the ASIC is shown in Figure 2.13.

2.6.1 Shift Register

There are a total of 16 inputs in the chip, 8 for the signal and 8 for the reference, while there are 32 outputs, 16 for the differential outputs and 16 for the DC outputs. Therefore, there are 48 input and output PADs. In order to set the various gain modes of the preamplifier and the subtractor, it would require 72 additional PADs, 9 bits for each channel, because the programmable signals are: 3 bits for the logic to set the gain of the preamplifier; 4 bits to set the different values of C_m of the preamplifier; and 2 bits to set the gain of the two subtractors. This design is obviously not

feasible, due to area occupation of all these PADs. Therefore, it was decided to use a shift register, one for each channel, that can be initialized at the start of each measurement cycle. This shift register is made up of 10 bits because it also integrates the CTRL bit for enabling the single-ended system. Finally, the chip requires a PAD for the mixer clock required for the demodulation, one for the shift register clock, one for the input data of the shift register, one for the output data of the shift register and one for the SE PIN. In conclusion, the total number of PADs is 84, that are distributed along the perimeter of the chip.

2.6.2 Single Ended System

Requirement for this project is the possibility to use a single-ended approach. The purpose is to perform a Raman measurement by using a single unbalanced channel, which may be the Signal path or the Reference one. This system is placed between the output of the preamplifier and the input of the auto-balancing circuit and it is composed of 2 switches for each path, one that connects the preamplifier to the input of the VGA, and the other that directly connects the VGA to ground, leaving the output of the preamplifier floating. Figure 2.14 shows the implementation of the single-ended system within the complete architecture of the chip.

To ensure safe operation of switches and prevent signal overlaps that could lead to malfunctions, the implementation of appropriate combinational logic is required. Two bits are allocated to drive the network: one bit is defined to enable the single ended mode or to keep the differential mode turned on, called CTRL, while the other bit is used to select which path to disable and which to enable to carry out the signal, called SE PIN. The different combinations and the result produced are summarized in Table 2.3.

CTRL	SE PIN	Path
0	0	Ref on
0	1	Sig on
1	/	both on

Table 2.3: *Logic values of the single ended system.*

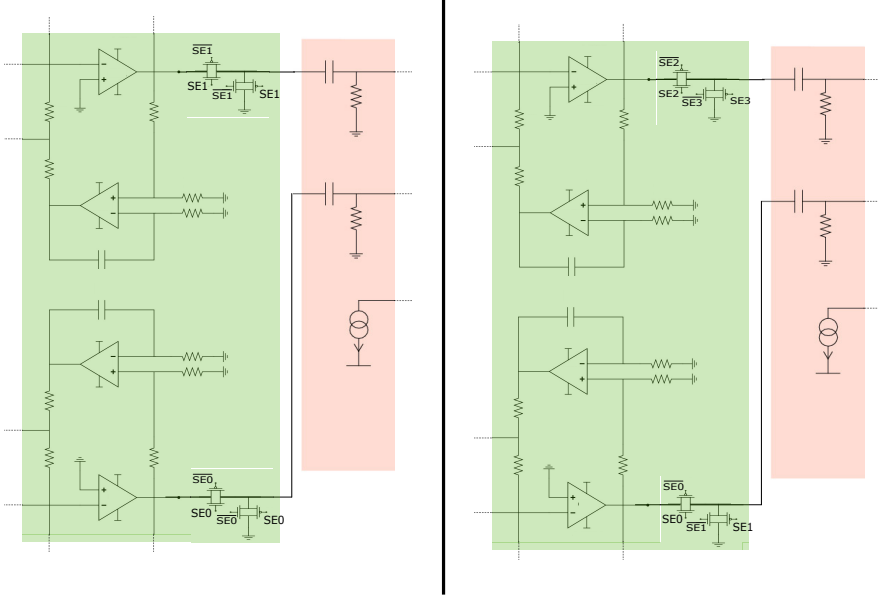


Figure 2.14: Schematic of the switches implemented for the single ended measurement. Switches used with signals from the first combinational circuit implemented (on the left) and with the final combinational circuit implemented (on the right).

This configuration is particularly advantageous in the case of highly stable lasers, which exhibit minimal fluctuations and therefore a low RIN. In single-ended mode, it is thus possible to convert the 8 reference channels into 8 additional signal acquisition channels, resulting in a total of 16 channels available for Raman signal detection.

CHAPTER 3

76-Channel Modular Platform for Stimulated Raman Spectroscopy

Part of this work is reported in [21] and [24].

This work is part of the CRIMSON project, that led to the realization of a 76-channel low-noise acquisition system for Broadband Raman Spectroscopy, as improvement to the 32-channel lock-in amplifier (named VIBRA platform), described in [16].

Starting from the experience acquired with the VIBRA platform, this chapter describes how an even more advanced acquisition system for Broadband Raman Spectroscopy is realized: the CRIMSON platform.

While many of the characteristics of the old system are shared with the new one, the following list summarizes the main new requirements for the CRIMSON platform:

- 76 lock-in channels;
- $10\mu W$ minimum optical power at each photodiode;

- selectable differential/single-ended readout;
- adjustable lock-in bandwidth;
- offset cancellation for narrow bandwidth acquisitions.

Each requirement is briefly described in the following paragraphs.

76 Channels

Increasing the number of channels allows to improve the resolution in the Raman spectrum, which is of particular importance when the fingerprint region must be acquired since it is identified over a wide Raman bandwidth ($600\text{cm}^{-1} - 1800\text{cm}^{-1}$).

To ensure a fast acquisition, the parallel approach that characterizes the VIBRA platform is preserved, so the system implements 76 independent lock-in channels.

Minimum Optical Power

Increasing the number of channels implies, as a direct consequence, the reduction of the optical power at the photodiodes. The reason behind this reduction has to do with biological sample damage, i.e. each sample is characterized by a maximum energy that it can absorb without being damaged.

This means that, while the total optical power impinging on the sample is fixed, the power-per-channel is reduced by increasing the number of sensors. This is the main justification for the new minimum power requirement, that is reduced by a factor 5 with respect to the VIBRA platform (from $50\mu\text{W}$ to $10\mu\text{W}$). The minimum reduction factor needed to compensate for the smaller power available on each sensor is $76/32 = 2.375$, which is the ratio between the number of channels of the CRIMSON and the VIBRA platforms.

A reduction factor of 5, instead of 2.375, guarantees the operation with an even smaller power on the sample with respect to VIBRA, hence enabling a better acquisition of the Raman spectrum tails, corresponding to very small signals.

Differential/Single-Ended Readout

While in the VIBRA platform the readout is necessarily differential (the custom IC always needs both signal and reference

to work properly) in the CRIMSON platform the single-ended readout option is added.

This option enables unbalanced detection, which significantly simplifies the optical setup but constitutes a viable solution only if the noise produced by the laser power fluctuations is negligible.

As described in the previous chapter, by converting from the differential to the Single Ended approach, it is possible to double the total channel number, from 76 to 152.

Adjustable lock-in amplifier bandwidth

While both systems feature fast acquisition of the Raman signal and thus employ a relatively wide lock-in bandwidth, practical experience has highlighted the need for a narrower bandwidth to perform high resolution measurements in some applications.

The VIBRA platform allows for several different BW settings (down to 3.6 kHz) by making use of the ADC internal digital filter. The new requirement adds more flexibility to the system, demanding for an user-selectable lock-in bandwidth with a frequency accuracy of a few Hertz.

Offset Cancellation

The VIBRA platform has shown an unexpected resolution limit for narrow-bandwidth acquisitions, ascribed to offset variations occurring during the measurement caused by the acquisition chain. Experimental evidence shows an offset voltage in the 5 mV to 100 mV range. Such offset components were attributed to non-idealities of the IC mixer stage, specifically to charge injection as the main contribution. This statement finds experimental support as the offset observed increases as the modulation clock provided to the mixer increases in frequency, as shown in Figure 3.1. To get rid of such contribution the VIBRA system employs a software calibration in which each channel is acquired with no input signal and averaged in order to provide a compensating value to subtract once the signal is present. Despite software calibration being able to eliminate the DC offset, experimental results show a residual offset drift. Figure 3.2 shows an example of such a drift: a fluctuation of the offset in the order of a few mV over minutes.

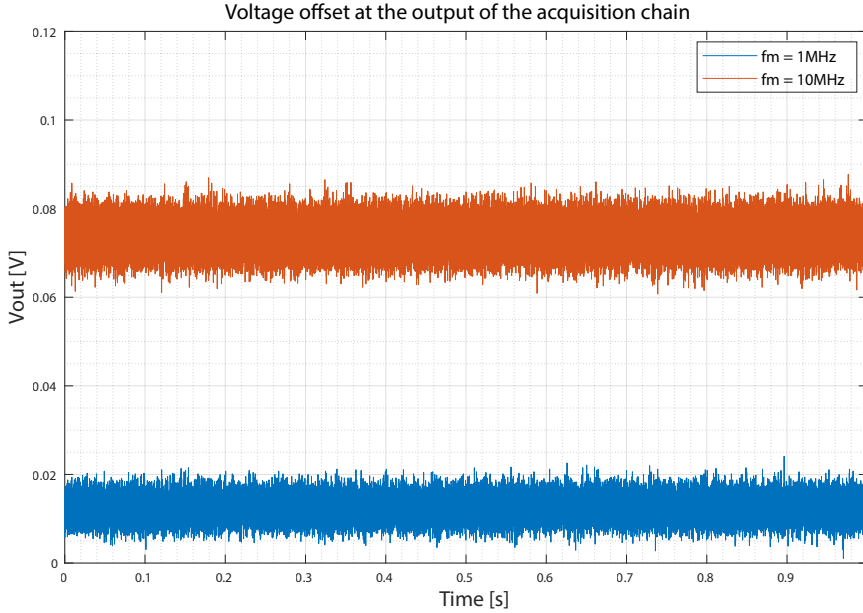


Figure 3.1: Output waveforms with no signal at the input of VIBRA in the cases of 1Mhz and 10Mhz demodulation frequency.

This drift is attributed to small temperature variations that affect the mixer stage. This phenomenon can be seen as a very low frequency signal mixed in with Raman information once the signal is demodulated.

This problem has been solved in the CRIMSON platform by employing a 2-step demodulation technique. The issue and the solution adopted are extensively described in section 3.1.

3.1 2-Step Frequency Down Conversion

In order to remove the very low frequency component due to offset drift, the demodulation phase is split in two steps:

1. Firstly, the modulated signal is demodulated by the IC mixer down to a lower frequency f_{mid} , low enough to be digitalized easily.
2. Secondly, the signal, now in the digital domain, is once again demodulated bringing the Raman signal back to base-band and the unwanted low frequency component up to f_{mid} .

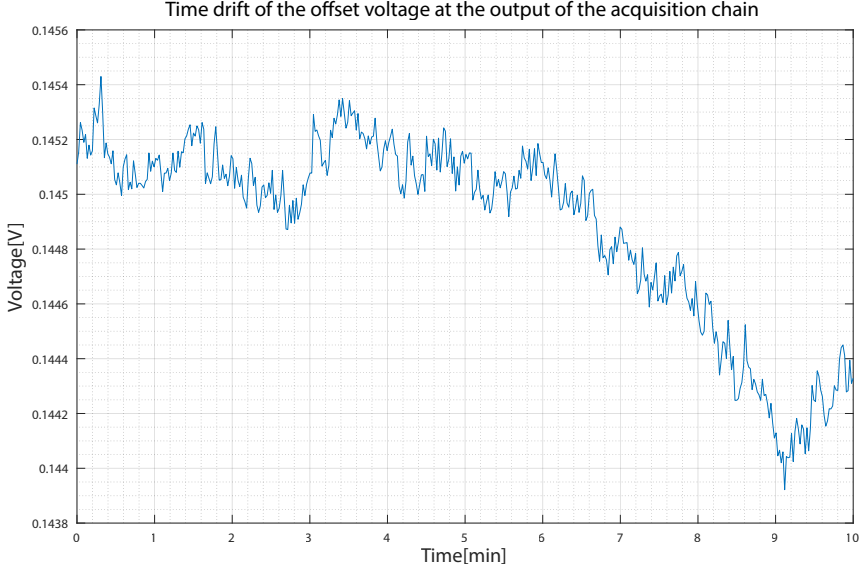


Figure 3.2: *Offset voltage at the output of VIBRA acquired with a narrow-bandwidth measurement in a time window of 10 minutes for a demodulation frequency of 10 MHz. The maximum offset span is 1.5 mV in this case [21].*

Further digital filtering removes unwanted harmonics and other components and keeps the Raman signal. It should be noted that while the entirety of the demodulation could be performed in the digital domain, to avoid mixer non-idealities, the ADC sampling frequency would be unreasonably high which, in a 76 differential channels system, would make the entirety of the solution much too complex.

First Demodulation

The Raman signal can be modeled as a sinusoidal signal with amplitude A and frequency ω_m :

$$v_{in}(t) = A \sin(\omega_m t)$$

Figure 3.3(1) shows the signal spectrum at the ASIC input. The first demodulation is performed by the analog mixer by a square wave of frequency w_{dm1} and its spectrum is shown in Figure

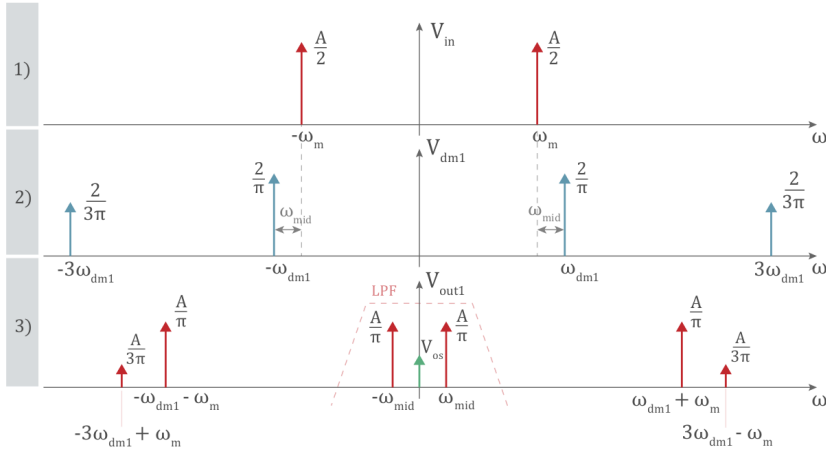


Figure 3.3: *Spectrum of the signals involved in the IC signal processing.*
 1) The modulated Raman signal at the input 2) The first two harmonics of the demodulating square wave 3) The spectrum after demodulation including offset and showing the anti aliasing filter.

3.3(2), as the wave can be Fourier-expanded as:

$$v_{dm1} = \frac{4}{\pi} \sin(\omega_{dm1}t) + \frac{4}{3\pi} \sin(3\omega_{dm1}t) \dots$$

Finally after the demodulation the resulting spectrum is depicted in Figure 3.3(3) where the first two harmonics are in red. The offset component due to the mixer is in green and the anti-aliasing low-pass filter (LPF) is shown as a dotted line.

Second Demodulation

Following the first modulation and subsequent filtering, the signal spectrum does not contain only the fundamental harmonic (as derived previously) but also the offset voltage of the previous stage, so a second demodulation step is mandatory.

The second demodulation is performed in the digital domain. The quantization noise is neglected, as it does not play a critical role. Indeed, digital demodulation is applied to very slow signals and with a narrow low-pass filter (LPF) bandwidth; this operation is equivalent to an averaging process of thousands of acquisition, thereby reducing the contribution of digital noise.

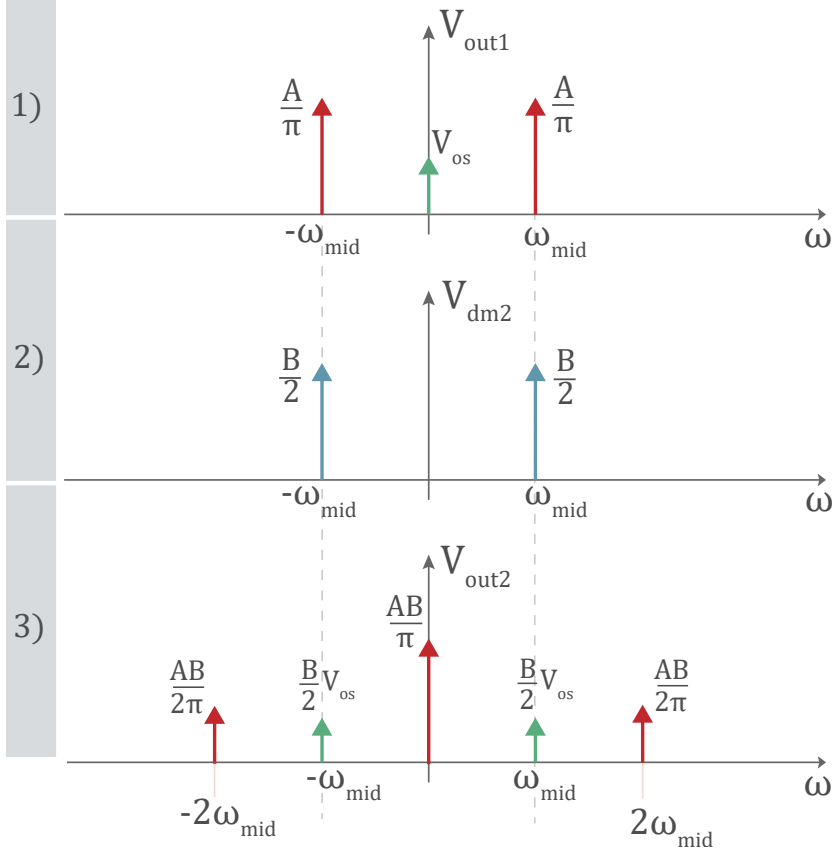


Figure 3.4: *Spectrum of the signals involved in the second demodulation step: 1) Signal once digitised by the ADC 2) Sinusoidal demodulation signal 3) Result of the second demodulation before filtering.*

The choice to adopt a digital sinusoidal wave for the second demodulation is made in order to maximize SNR as the Raman signal can be considered a sine wave. A sinusoidal signal input of amplitude A , in presence of white noise with spectral density S_B and equivalent noise bandwidth f_n , would mean a SNR, in case of square wave demodulation, of:

$$SNR_{square} = \frac{A}{\frac{\pi}{2} \sqrt{S_B f_n}}$$

while in case of sine wave demodulation it would be:

$$SNR_{sin} = \frac{A}{\sqrt{2}\sqrt{S_B f_n}}$$

Therefore the sine results in better SNR. The second demodulation steps are summarized (in the frequency domain) in Figure 3.4. In Figure 3.4(1) the signal digitized by the ADC is shown. It comprises the desired signal in sinusoidal form and the offset added by the mixer and can be analytically expressed as:

$$v_{ADC}(t) = \frac{2}{\pi} A \sin(\omega_{mid} t) + V_{OS}$$

In Figure 3.4(2) the sinusoidal demodulation signal, of amplitude B, is represented. The demodulation frequency is chosen as the residual modulation frequency of the signal:

$$v_{dm2}(t) = B \sin(\omega_{mid} t)$$

The result of the multiplication is shown in Figure 3.4(3) and can be expressed as:

$$\begin{aligned} v_{out2}(t) &= \frac{2}{\pi} A \sin(\omega_{mid} t) B \sin(\omega_{mid} t) + V_{OS} B \sin(\omega_{mid} t) = \\ &= \frac{2}{\pi} AB \frac{1}{2} [1 - \cos(2\omega_{mid} t)] + V_{OS} B \sin(\omega_{mid} t) \end{aligned}$$

Half of the Raman signal is brought back to base-band while the other is up-converted to $2\omega_{mid}$ and crucially the offset is up-converted to ω_{mid} . The unwanted components can now be removed by digital filtering leaving only:

$$v_{out2}(t) = \frac{AB}{\pi}$$

Single vs Double Demodulation

Choosing a double demodulation approach eliminates offset drift, but has a drawback: each demodulation step comes with a reduction in SNR. The reducing factor depends on the signals involved in the multiplication; in this case, the second demodulation results in a reduction of $\sqrt{2}$ leading to an overall estimated signal

to noise ratio of:

$$SNR_{tot} = \frac{A}{\frac{\pi}{\sqrt{2}}\sqrt{S_B f_n}}$$

When the signals involved are large enough not to need the maximum resolution performed by the system, this drawback outweighs the performance improvement. Therefore fast measurements, meaning not close to the maximum spectral resolution, would have better performance by employing the single analog demodulation. The solution is to render the second, digital, demodulation available as an option: if fast measurements are performed, single demodulation can be used, while if long, precise measurements are needed, the second demodulation and DSP chain is turned on in order to overcome the resolution limit due to offset voltage drift.

Digital Signal Processing Chain

If 2-step frequency down conversion is employed the unfiltered signal in the digital domain presents various undesirable components which need to be filtered. A digital low pass filter is used (see 3.5.1) to limit the signal bandwidth. However, a first order filter does not attenuate nearly enough the most limiting spurious spectral components which are placed at ω_{mid} and $2\omega_{mid}$ and are respectively the offset and offset drift and the first alias harmonic. To selectively cancel out such components, all placed around $k\omega_{mid}$, a comb filter is employed in the form of a digital gated integrator (see 3.5.1). The entire hybrid processing chain is repeated 76 times for the signal path and again 76 times for the reference path. Because of this high level of both analog and digital parallelism, a complex modular system has been designed; in the next Section (3.2) said system will be described in detail.

3.2 Platform Overview

The new system is schematically shown in Figure 3.5. It reuses the modular architecture adopted in VIBRA platform, but with the new features listed before. The complete platform is composed of two couples of 38 photodiode arrays, 10 modules plugged into a motherboard, and an FPGA. The 76 channels are dis-

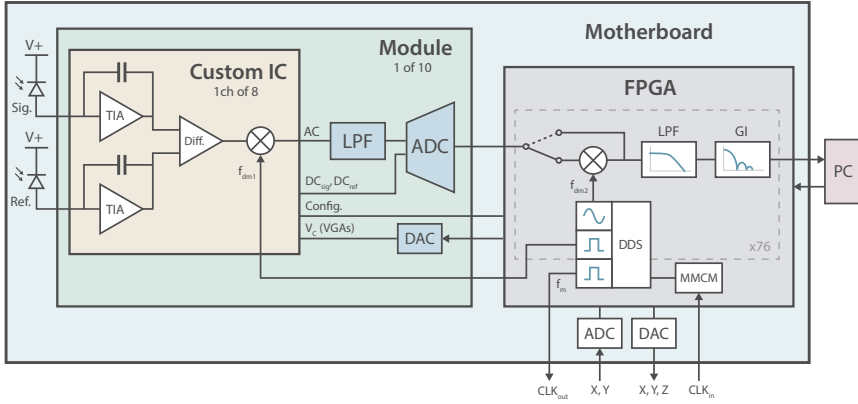


Figure 3.5: Simplified diagram of the 76-channel platform, with highlighted the Custom IC (1 channel out of 8), the module (1 out of 10), the FPGA with the DSP chain (1 out of 76) and the motherboard.

tributed across 10 modules, based on the 8-ch custom IC previously introduced. Each module implements 8 acquisition chains, from the current preamplifier to the digitization of the signal, performed by the ADC. A motherboard supports and interconnects the 10 modules with the Photodiode Arrays (PDAs). This modular approach, together with system and layout optimizations, allowed to minimally increase the size of the motherboard PCB and thus of the whole system, even in front of a more than doubled number of channels.

The motherboard features additional circuitry to control the movement of the sample under test and to acquire the position of the sample. The signals corresponding to the 76 wavelengths are generated by 2 x 38-element PhotoDetector Array s (A5C-38 by OSI Optoelectronics), while two additional 38-element PDAs are employed to acquire the reference signals.

3.2.1 Digital Signal Processing

One of the most relevant innovations introduced in the new system is a DSP chain, necessary to implement the two-step demodulation and the adjustable lock-in bandwidth, as discussed in section 3.5. This new element required particular care in some parts of the design; in particular, a more resource-capable FPGA is needed to implement the high number of DSP chains.

Feature	XEM7310-A75	XEM7310-A200
Slices	11800	33650
FPGA RAM	3780 kib BlockRAM 892 kib Distributed	13140 kib BlockRAM 2888 kib Distributed
MULT / DSP	180	740
CMTs	6	10

Table 3.1: Main differences between the XC7A75T and XC7A200T Xilinx Artix-7 FPGAs [25]

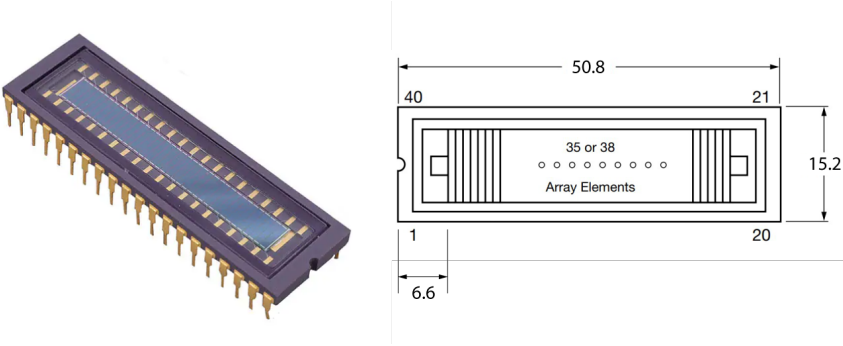


Figure 3.6: Left: picture of the PDA A5C-38 in the DIP-40 package. Right: dimensions of the PDA in mm. The distance between the border of the package and the active area is 6.6 mm. [26]

It has translated into employing a different FPGA data acquisition board provided by Opal Kelly, but still based on a Xilinx Artix-7 FPGA: the XEM7310-A200 board. The A200 version integrates more resources with respect to the A75 version (adopted for VIBRA platform); table 3.1 shows the main differences. Nevertheless, the XEM7310-A200 board still provides to the user 128 I/O pins (like the A75), thus the design required several system-level optimizations to handle the large amount of signals, a direct consequence of the increased number of channels.

3.3 Photodiode Array

The sensor used for the acquisition of 76 differential channels is a Photo-Diode Array (PDA), the A5C-38 by OSI optoelectronics. Four 38-element PDAs are used, providing 76 photodiodes (2 x 38) for the signal and 76 for the reference. The optimal solution

to implement an N-channel system is by employing a PDA with N elements; unfortunately such a solution was not feasible in this case since there is no sensor available on the market with the required parameters that integrates 80 photodiodes. Adopted sensors are mounted on the bottom of the motherboard and their placement is determined by the optical setup requirements. By employing two 38-element PDAs there is an unavoidable dark region (sensorless) of about 13.2 mm between the two because of the DIP-40 package size of the A5C-38, as shown in figure 3.6. This region would directly translate into a hole in the middle of the acquired Raman spectrum and might not be acceptable (see solution "a" in Figure 3.7). The optical setup adopted to solve this issue is depicted in Figure 3.7, solution "b", and allows to acquire the full spectrum ideally without any loss of information. The diffracted beam is split in two using mirrors and it is acquired in a non-contiguous way. This, however, is not a drawback since the complete Raman spectrum can be easily reconstructed by the software. The pairs of PDAs belonging to the same line (signal or reference line) are placed as close as possible on the motherboard, while the distance between the active areas of the two lines is set to about 28 mm as required by the optical setup.

3.3.1 Physical Signal Selection

While the system implements 76 channels, limited by the number of elements per each PDA used, the hardware is potentially capable of acquiring 80 channels: the four additional unconnected channels can be exploited to acquire some reference signals (DC_{ref}) simultaneously with the AC and DC_{sig} signals. In this way, the information regarding the mean power on some of the reference photodiodes can be used to check the laser alignment with the photodiodes during the acquisition phase. Specifically, for 8-channel modules all ASIC channels are connected to the ADC while for 7-channel modules AC8 and DC8 ASIC channels signals are replaced by REF1 and REF7 respectively. The positions of the reference photodiodes acquired simultaneously are chosen in order to be distributed across the 76 elements, as Figure 3.8 shows.

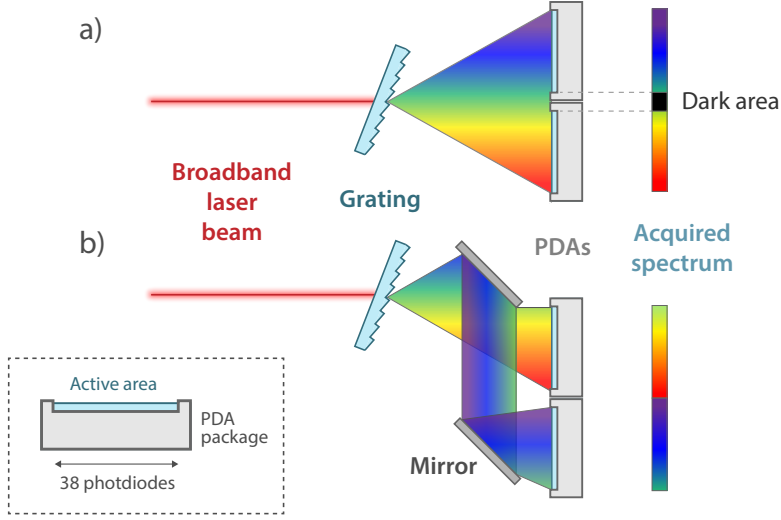


Figure 3.7: a) the space between the active area and the package border of the PDA entails the generation of a dark area, i.e. part of the Raman spectrum is lost; b) alternative optical setup allowing to acquire the full Raman spectrum. This is the solution adopted in this system.

3.4 Hardware Design

In this section, the 8-channel module and the motherboard are presented with the aim of describing and justifying the hardware architecture, emphasizing the optimization choices.

3.4.1 8-ch Module

Each module consists of a $82 \times 57 \text{ mm}^2$ 6-layer PCB with an edge connector (see Figure 3.9), allowing it to be easily connected to the motherboard through a standard PCIe socket. The module core is the 8-channel custom IC presented in Chapter 2, so it implements 8 analog acquisition chains, starting from the on-chip preamplifier up to the ADC for the digitization of the acquired optical signals. Several space-saving optimizations, in terms of routing, components placement and packaging, enabled the implementation of a doubled number of channels in almost the same PCB area with respect to the 4-channel old version (that measures $78 \times 61 \text{ mm}$).

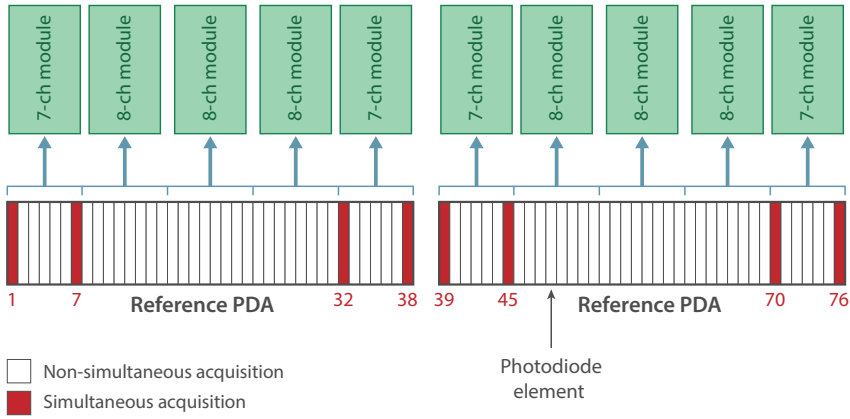


Figure 3.8: Positions of the reference photodiodes acquired also during the Raman imaging (depicted in red), in correspondence with the modules that acquire only 7 channels out of 8.

Custom IC

The custom IC comes with no package from the foundry, so the footprint on the PCB is intended for direct bonding of the pads on the die to those on the board. A custom 3D printed case is then mounted above it to protect the wire bonding and the IC from damage. The chip is placed near the PCIe connector and an RC network is connected as close as possible to the inputs for stability reasons. In particular, a 10 pF capacitor is connected between the preamplifier input (virtual GND) and GND to ensure loop-stability, while a 180 Ω resistor is connected in series to the inputs in order to mitigate the effect of the long signal track linking the photodiodes (placed on the motherboard) with the chip, which again, might cause instability. Some 1 μF bypass capacitors in 0402 package, characterized by a low series inductance value, are placed as close as possible to the power supply pins of the chip.

INA Stage

The 8 ASIC differential output pairs, carrying the Raman signal, are fed to 8 Instrumentation Amplifiers that implement both a gain stage with $G=10$ and differential to single-ended conversion of the signal. For this purpose, the INA2126 by Texas Instru-

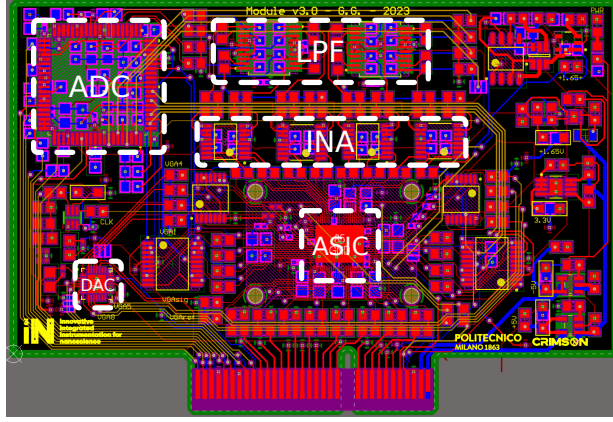


Figure 3.9: *Module board layout.*

ments is used, that integrates two INAs in the same package and typically features a voltage noise spectral density of $35 \text{ nV}/\sqrt{\text{Hz}}$, a CMRR of 94 dB and an offset voltage (referred to the input) of $\pm 100 \mu\text{V}$. The gain is set with a single external resistor according to the following formula:

$$G = 5 + \frac{80 \text{ k}\Omega}{R_G}$$

so an $R_G = 16 \text{ k}\Omega$ is required to get $G=10$. The resulting -3 dB bandwidth of the INA with such a gain is 100 kHz.

Filtering Stage

The first filtering action performed on the Raman signal is carried out by a simple RC filter implemented with a 100 pF capacitor, connected between the differential outputs of the chip, and the internal $20 \text{ k}\Omega$ resistors, thus providing a cut-off frequency of about 40 kHz. An additional filtering stage is then added after the INA, consisting of a 2nd order LPF implemented with the LTC1562 by Linear Technologies. This chip allows for different filter designs in terms of topology and parameters, according to the external components used. Specifically, two resistors are used to set the f_0 and Q of the filter according to the following formulas:

$$f_0 = 100 \text{ kHz} \cdot \frac{10 \text{ k}\Omega}{R_2}, \quad Q = \frac{R_Q}{R_2} \cdot \frac{100 \text{ kHz}}{f_0}$$

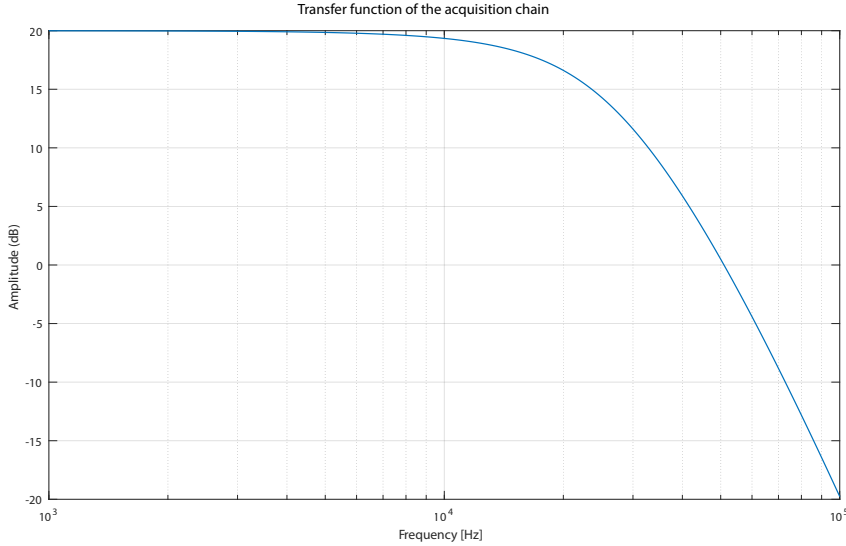


Figure 3.10: *Simulated transfer function from the input of the INA and the output of the filtering stage (including the RC filters). At half of the sampling frequency, $f_s/2 = 62.5 \text{ kHz}$, the attenuation w.r.t. the DC gain is 25.5 dB.*

The filter is designed with $f_0 = 25 \text{ kHz}$ and $Q = 0.675$ to guarantee a settling time shorter than $50 \mu\text{s}$. Finally, the DC gain of the filter is set by an input resistor to provide unitary gain ($G(0) = R_2/R_{IN}$). An additional RC low-pass filter with a cut-off frequency of about 48 kHz is added at the output of the LTC1562, and the overall transfer function from the differential outputs of the custom IC to the output of the filtering stage, is the one depicted in figure 3.10. It results in a -3 dB cut-off frequency of about 19 kHz that sets the maximum lock-in bandwidth of the system. Moreover, this stage acts as an anti-aliasing filter and provides, according to the transfer function shown in Figure 3.10 and a sampling frequency of 125 kHz, a reduction of about 25 dB for the spurious signals subject to folding in the baseband when digitized.

All the DC_{sig} and DC_{ref} outputs, i.e. the outputs that carry the information about the mean power impinging on the signal and reference photodiodes respectively, are filtered with an RC low-pass filter with a cut-off frequency of 16 kHz. These filters are

designed considering also the $10\text{ k}\Omega$ resistance connected in series with each DC output of the custom IC, so the filters implemented on the module employ $R = 10\text{ k}\Omega$ and $C = 470\text{ pF}$. Moreover, the PCB allows for adding a capacitor right at the output so that, exploiting the internal resistance, a 2nd order filter can be implemented as a cascade of two RC LPFs.

DAC

The module features a Digital-to-Analog converter, the AD5679 by Analog Devices, to set an external voltage to each VGA control pin of the custom IC. This permits to manually adjust the VGA gain, for balancing the internal differential structure when the AGC feedback network is disabled.

Module Power Supply

The power supplies are independently generated by each module so that the power dissipation is distributed, and in case of a fault occurring on one module, the operation of all the others is not compromised. Each module is powered by dual-supply voltages set at $\pm 6.5\text{ V}$. Starting from these, all the other supply voltages are generated by means of 3 low-noise linear voltage regulators. Specifically, the employed regulators are:

- ADP7118, fixed 3.3V regulator;
- ADP7142, fixed 5V regulator;
- ADP7182, fixed -5V regulator;

3.4.2 Analog to Digital Conversion

Every module is equipped with an AD7616, a dual 16-channel ADC. The IC contains two Successive Approximation Register converters (SAR-ADC) which operate in parallel handling 8 channels each. Figure 3.11 shows a functional diagram of the device. The device is used in the so-called "software mode": it is configured exclusively through registers, and the communication with the device is through serial interface, adopting the SPI protocol, to limit the amount of FPGA pins necessary for ADC control. The SPI communication is set to two-wire mode: the two SAR

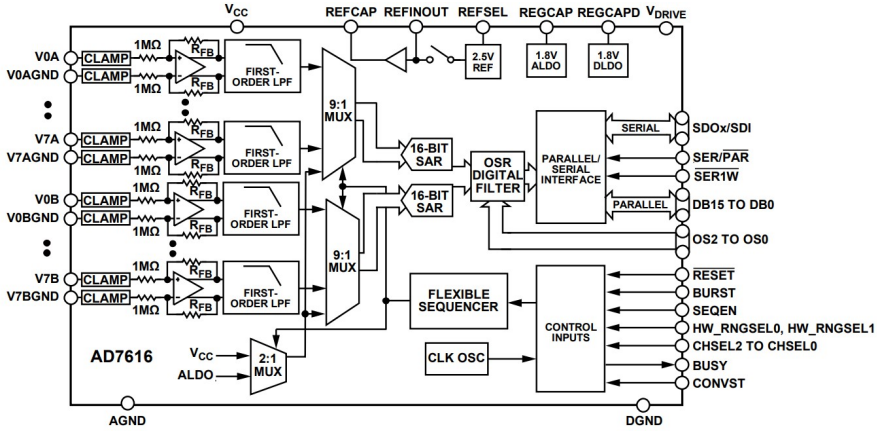


Figure 3.11: Functional block diagram of the AD7616 DAS. [27]

converters communicate on separate wires. This choice separates the 8 channels assigned to SAR A and B and results in maximum throughput. The two converters operate in parallel; the 16 channels are, therefore, all converted within 8 conversion cycles. The order in which the channels are converted is set through the sequencer: a memory stack in the device filled with a list of conversions at most 32 couples of channels deep. The device is used in either normal sequencer mode, in which a single conversion start pulse results in a single conversion, or in "burst" mode in which a single conversion start pulse is followed by the conversion of the full sequencer stack. Both options are implemented in firmware. The advantage of burst mode is the possibility of reducing the capacitive coupling effect between the conversion start pulse to the ADC and the nearby analog channel lines. Despite the new 6 layer module PCB, with a ground plane used to reduce the effect, some coupling is still present and is noticeable if the mixer frequency is equal to a multiple of 1 MHz. The burst mode reduces the amount of pulses making it possible to convert the AC channels close to the conversion start trace on the PCB as far as possible in time to the SoC pulse.

ADC Input Signals

The 16 inputs are connected to the two internal ADCs by means of two 9:1 internal multiplexers (an additional internal diagnostic

	ADC_A	ADC_B
0	AC1	AC5
1	AC2	AC6
2	AC3	AC7
3	AC4	AC8 (REF1)
4	DC1/REF1	DC5/REF5
5	DC2/REF2	DC6/REF6
6	DC4/REF4	DC8(REF7)/REF8
7	DC3/REF3	DC7/REF7

Table 3.2: List of the analog signals acquired by the two ADCs of the AD7616. AC_x refer to the Raman signals, DC_x and REF_x refer to the signals corresponding to the mean optical power on PDA_{sig} and PDA_{ref} respectively. The signals represented with a "/" in between are alternatively selected using the analog switches, the ones between parenthesis are selected by means of a physical connection on the PCB.

channel is present). While the simultaneous acquisition of 8 Raman signals (AC_{sig}) is mandatory, the simultaneous conversion of all the DC outputs (DC_{sig} and DC_{ref}) is thus not necessary and the user can decide which signals to acquire (by means of the GUI) according to the experiment phase. The signal selection is carried out by 8 SPDT analog switches, implemented by two MAX4533 by Maxim Integrated. All connections from the ASIC output to the ADC input follow the scheme reported in Table 3.2.

3.4.3 Motherboard

The main role of the motherboard is to support and interconnect the 10 modules with the PDAs, the FPGA and the main power supply board. It consists of a 118x193 mm 4-layer PCB. Particular care was taken in the placement of the PDAs, the modules and the FPGA in order to minimize the traces lengths as shown in figure 3.12, with advantages also from the electrical standpoint (mainly concerning reflection and stray capacitance).

Laser-Synchronous Clock Conditioning

As previously described, the system must synchronize its operations with the laser pulses and it must be able to provide the modulation signal to the acusto-optical modulator.

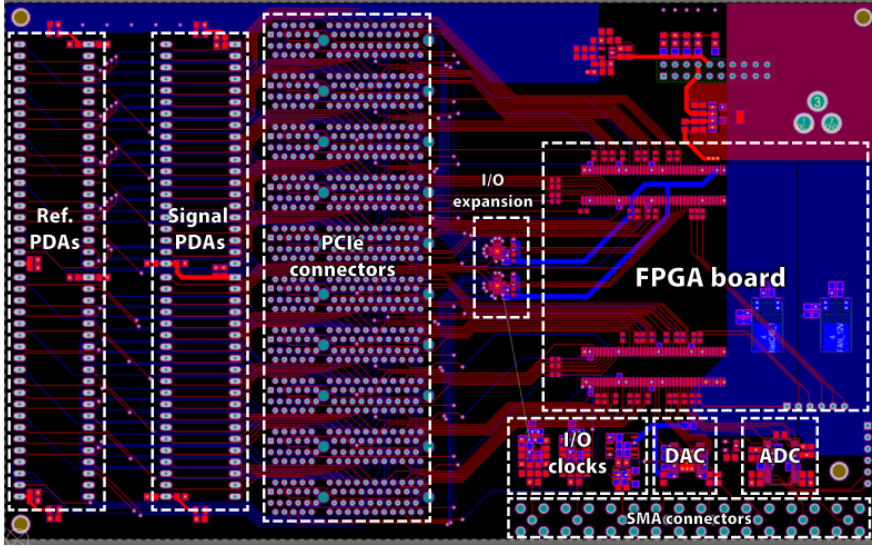


Figure 3.12: Layout of the 4-layer motherboard PCB showing the top (red) and bottom (blue) layers. The main components are highlighted.

The laser-synchronous clock is a TTL-compatible signal with a frequency of 40 MHz or 80 MHz. A conditioning circuit (figure 3.13) based on the LTC6752 comparator by Analog Devices is used to regenerate such a signal and provide it to a dedicated pin of the FPGA with the proper digital levels, i.e. 0-3.3 V. The LTC6752 features separate supply voltages for the input and output stages; in this application, the input stage is powered with 5 V while the output stage is powered with 3.3 V, accordingly to the digital levels they have to deal with. The input of the circuit is AC-coupled to the non-inverting input (V+) of the comparator with a 100 nF capacitor so that the signal fed to it is always centered around a 2.5 V reference, that is the threshold voltage, regardless of its amplitude. To achieve this, a voltage divider connected to the inverting input generates the reference voltage and a 100 k Ω resistor sets the bias of V+. A 470 Ω resistor is connected in series with the input to limit the current flowing through the internal protection diodes of the comparator in case of overvoltage, as required by the datasheet. Finally, the circuit realizes a 50 Ω termination at the input to match the cable and source impedance.

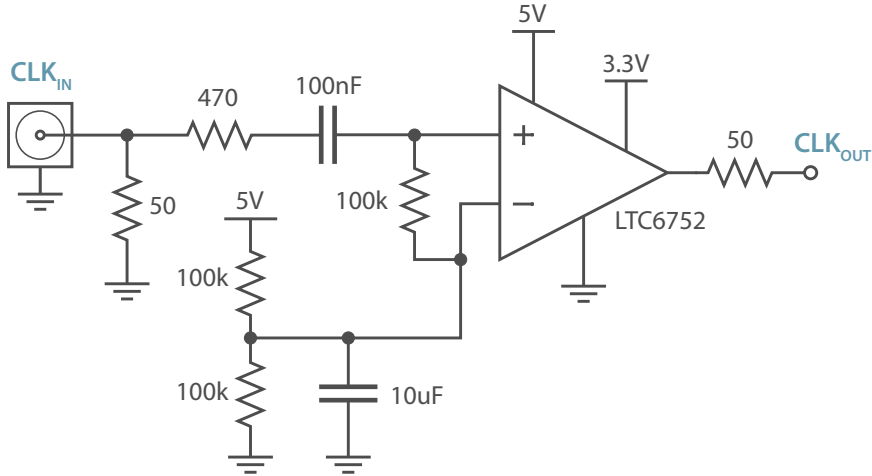


Figure 3.13: Schematic diagram of the laser-synchronous clock conditioning circuit. The CLK_{IN} signal is provided externally by the laser through a SMA connector. The CLK_{OUT} signal is fed to a MRCC pin of the FPGA.

Motherboard DAC

The motherboard is equipped with an AD5724R DAC, which is responsible for managing the movement of the sample for image acquisition. During this phase, the laser remains stationary while the sample is moved to create an accurate scanning pattern, resulting in the generation of 76 images, one for each wavelength that the system processes simultaneously. An in-depth analysis of this component and its application will be presented in Section 3.5.4.

Motherboard ADC

The ADC integrated in the motherboard could be utilized if a closed-loop system is necessary to manage the sample position. If the position is set by an external wave generator the ADC provides the actual position of the sample to the system.

FPGA

The decision to employ a FPGA module from Opal Kelly was taken to facilitate high-throughput USB communication and to

manage the high number of parallel acquisition channels. This module features a specialized chip designed specifically for USB super-speed communication and is accompanied by a software development kit to effectively leverage its capabilities. The chosen module is the XEM7310-A200, which exploits the Xilinx Artix-7 FPGA. The FPGA is used to drive the entire system, which primarily consists of, but is not limited to, executing the following tasks:

- programming and reading data from the 10 ADCs (AD7616) via the SPI interface;
- configuring the 10 DACs (AD5679) through the SPI interface to generate the required control voltages for the on-chip VGAs;
- supplying 80 configuration bits to the 10 custom ICs through their serial interface;
- locking on the laser clock (80MHz), generating the clock for the optical modulator and 10 independent clocks for the on-chip mixer;
- implementing 76 differential DSP chains to operate either in one or two demodulation mode;
- monitoring the movement of the sample by means of a DAC (AD5724) and acquire its position with an ADC (ADS8684);
- sending the acquired and processed data to the PC using the USB 3.0 interface.

Performing all these functions requires a high number of digital inputs and outputs, so the design required several hardware and firmware optimizations.

Finally, 114 FPGA GPIOs out of the 123 available are used, so 6 GPIOs are made available for debug purposes or additional features, by means of a simple 6-element connector and the remaining 3 GPIOs are left unconnected.

I/O Expander

Two ADP5585 serve as an I/O expander, featuring 10 GPIOs that can be configured for either input or output functions, along

with various internal pull-up/pull-down resistors. The two 80 pin connectors between the XEM7310 and the motherboard are not quite enough, thus to expand the output pins capabilities two ADP5585 are placed on the motherboard for I/O expansion. The two ICs handle the AGC_DAC and DC_REF (pins of the custom ASIC). These pins were chosen to be connected through the IO expander since they don't need to be changed after the startup sequence. Each expander handles five modules, five AGC_DAC and five DC_REF, the settings of these ICs are selected from the GUI and sent to the firmware. Configuration data and output values are sent through I2C to the ADP5585 by the firmware block "IO expander controller", which is implemented as an FSM.

Motherboard Power Supply

The whole system is intended to be powered with a single supply voltage (V_{IN}) generated by an external Power Supply (e.g. a laptop charger) that is plugged into the motherboard by means of a standard power jack connector (PJ-066B by CUI Devices). Starting from this, a distributed power supply architecture is implemented: a main power board, employing DC/DC converters, receives the V_{IN} supply voltage and generates the $\pm 6.5\text{ V}$ dual supply voltages fed to the 10 modules as previously described. Moreover, starting from the $+6.5\text{ V}$ voltage, the $+5\text{ V}$ supply that powers the XEM7310 board and several other devices is generated using the linear voltage regulator LP3871 by Texas Instruments. The XEM7310 features an on-board 3.3 V DC/DC converter that is also exploited as logic power supply for some devices on the motherboard. Additional linear voltage regulators, the low-noise AD7118 and the NCV1117, are respectively employed to generate the $+15\text{ V}$ bias voltage for the 4 PDAs and for the motherboard DAC.

Particular care was taken in order to minimize the dropout voltage on the regulators, especially for those providing higher currents. For the LP3871, both the GND internal planes, characterized by a large area and a copper plane on the top layer have been connected to the thermal pad to act as a heat sink.

3.5 FPGA Firmware Design

The number of instances necessary for each structure may differ according to various factors such as choices, hardware, and firmware requirements. For instance, it could be 76 if it needs to be replicated for each channel or 10 if it is to be repeated for each module, among other possibilities. This is the reason behind the choice to implement multiple layers of IPs (Intellectual Properties). Each IP is then treated as a black box: once validated, the changes within the IP or outside of it can be dealt with independently. The final block design includes 10 instances of the "Single Module" IP within which is an instance of the "Sixteen differential channels" IP. This latter IP contains 8 instances of the AC version of the "Single Channel" IP and 8 of the DC version. In the following paragraphs, the IPs are described with a bottom-up approach, starting from the smaller doll of the matrioska and ending with the biggest, listing and characterizing all the blocks the digital processing chain is composed of.

3.5.1 Single Channel IP

This IP is designed to handle the single channel digital processing. Two versions exist: an AC and a DC version. The AC version contains the complete DSP chain to deal with the signal carrying Raman information while the DC version is simplified in order to save FPGA resources.

AC Single Channel IP

The digital processing chain consists of a multiplier, a low pass filter and a gated integrator as seen in Figure 3.14. The multiplier is used to perform a digital second demodulation by multiplying the input data by a reference digital sine. The reference sinusoidal signal is passed as an input to the mixer and is generated by a DDS which is properly set up in order to deliver the correct frequency and phase. DDS (Direct Digital Synthesizer) is an IP block provided by Xilinx, that can be instantiated in the VHDL project. Such as hardware DDSs, this IP exploits a Look-up Table where the sine wave is mapped and a counter. This step is optional and can be bypassed by a selection bit: "DemodEn". If

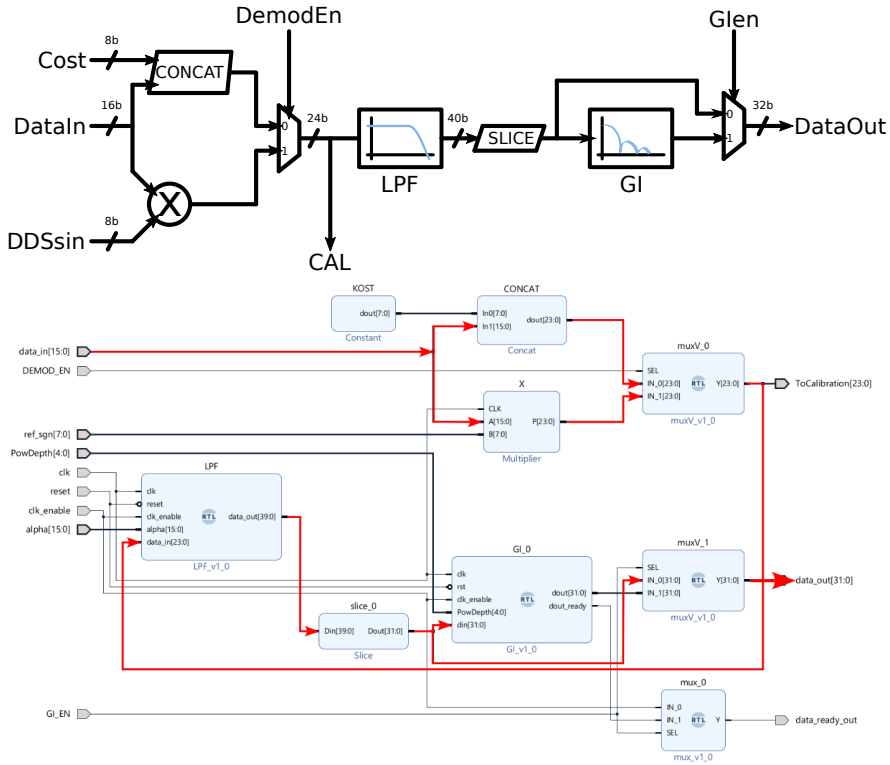


Figure 3.14: *AC version of single channel IP: simplified diagram (top); detailed block scheme with the signal path highlighted in red (bottom).*

the bit is set to 0 then the input data will be adjusted for gain and passed through without multiplication. To avoid gain differences between the two paths, a concatenation with a constant is chosen as the simplest solution (zero-padding). The processing chain then leads to a digital low pass filter which will be described in detail in section 3.5.1. Since the data word sent by USB is 32 bits, the 40-bit output of the LPF needs to be sliced, the least significant 8 bits are therefore discarded before entering the GI. Next a gated integrator is used in order to filter out higher order harmonics exploiting its comb filter action, see section 3.1 for a full description of the frequency domain effect. The GI can be bypassed through a selector bit "Glen". Every synchronous block only processes data when the clock is enabled, meaning if no valid data is fed to the IP no processing happens. The outputs

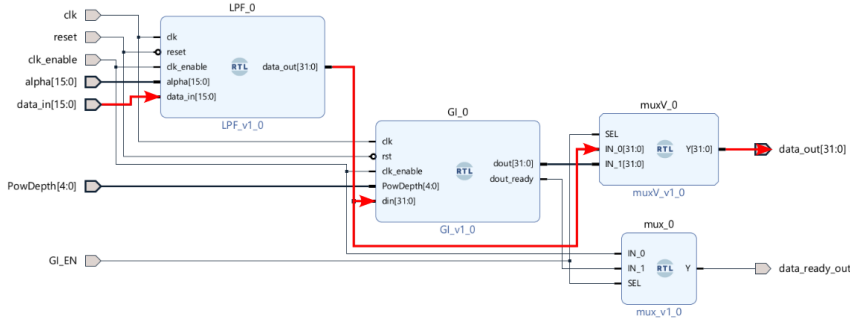


Figure 3.15: *DC version of single channel IP: detailed block scheme with the signal path highlighted in red.*

of the IP are: "DataOut", "DataReadyOut" and "ToCalibration". The output data is accompanied by a bit which is high only when new valid data is present and the data rate is dependent on how many averages the GI performs. The calibration signal is, instead, a constant data rate output, coming directly after the demodulation multiplication. It is used to calibrate the system reference sine phase in order to maximize gain. For further detail on said calibration see section 3.5.3.

DC Single Channel IP

The signal coming from the Reference or the DC channels from the ASIC preamplifier is not modulated, therefore no demodulation is necessary. The LPF and GI are kept in order to have the same bandwidth and data rates on reference and signal paths. The resulting IP simplified diagram is shown in Figure 3.15

Low Pass Filter

The low pass filter is a first order infinite impulse response (IIR) structure. As this filter will be replicated 160 times, $10 \text{ modules} \cdot 8 \text{ channels/module} \cdot 2$ for differential operation, resource efficiency is of paramount importance. The IIR structure, in fact, was mainly chosen due to the possibility of implementing the filter by employing a single digital multiplier.

The filter functional diagram is shown in Fig 3.16 and is derived from the z domain transfer function:

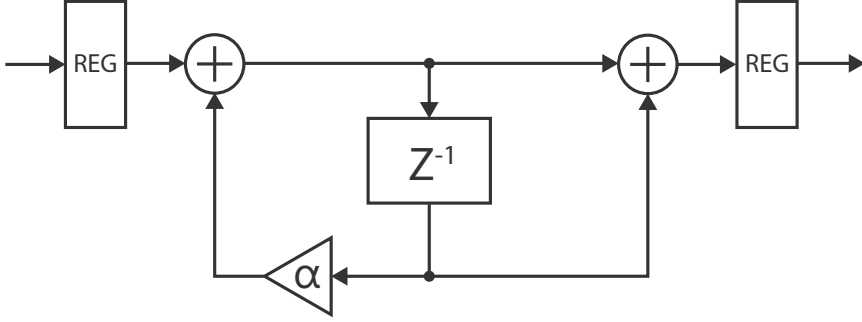


Figure 3.16: Implementation of the first-order digital low-pass filter. The value of α sets the cut-off frequency.

$$H(z) = \frac{\mu}{1 + 2\mu f_s \frac{1-z^{-1}}{1+z^{-1}}} \quad (3.1)$$

Where μ is the low frequency gain and f_s the ADC sampling frequency. By setting:

$$\mu' = \frac{\mu}{1 + 2f_s\tau} \quad , \quad \alpha = \frac{2f_s\tau - 1}{2f_s\tau + 1} \quad (3.2)$$

The transfer function can then be written:

$$H(z) = \frac{1 - z^{-1}}{1 - \alpha z^{-1}} \quad (3.3)$$

By anti-transforming 3.3 to a discrete time description:

$$y[n] = \mu'(x[n] + x[n-1]) + \alpha y[n-1] \quad (3.4)$$

Where the output at time n is a function of the input at time n and at time $n-1$ and of the previous iteration's output $y[n-1]$ through α . This is easily translated in Fig 3.16 where the inputs of the LPF are highlighted. It is important to note that α is a value between -1 and 1 as can be calculated by 3.2 once the filter τ is chosen.

Finally, the multiplier used in the filter implementation is custom. Both input and output word lengths can be selected. When the selected output size is less than the sum of the input bit-lengths the discarded LSBs are not simply truncated: the least

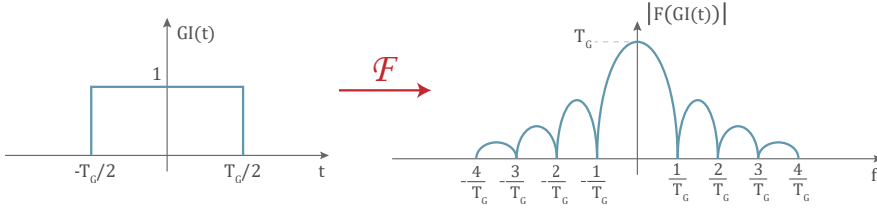


Figure 3.17: *Gated Integrator. On the left: impulse response in the time domain of the gated integrator. On the right: frequency domain transfer function*

significant bit remaining is rounded up or down depending on the cut portion in order to avoid any gain bias.

Gated Integrator

In order to understand how the digital version of the gated integrator filter is employed as a comb filter, an analysis of the continuous time version is very useful. A gated integrator which averages for a time T_g with weight $A=1$ is described by the function:

$$Gi(t) = \begin{cases} 1 & -\frac{T_G}{2} \leq t \leq \frac{T_G}{2} \\ 0 & |t| > \frac{T_G}{2} \end{cases} \quad (3.5)$$

In the frequency domain the function describing the GI is the Fourier transform of $Gi(t)$:

$$\mathcal{F}(Gi(t)) = T_G \cdot \frac{\sin(\pi f T_G)}{\pi f T_G} = T_G \cdot \text{sinc}(f T_G) \quad (3.6)$$

Figure 3.17 shows the continuous time GI transfer functions graphically. In particular the comb filter nature of the filter is clear: the first notch is at $f_{fn} = \frac{1}{T_G}$ and the subsequent ones are at $f_{kn} = \frac{k}{T_G}$.

Discrete Time Integrator

The implementation of the GI in the digital domain, also called Discrete Time Integrator (DTI), can be imagined as the sampled

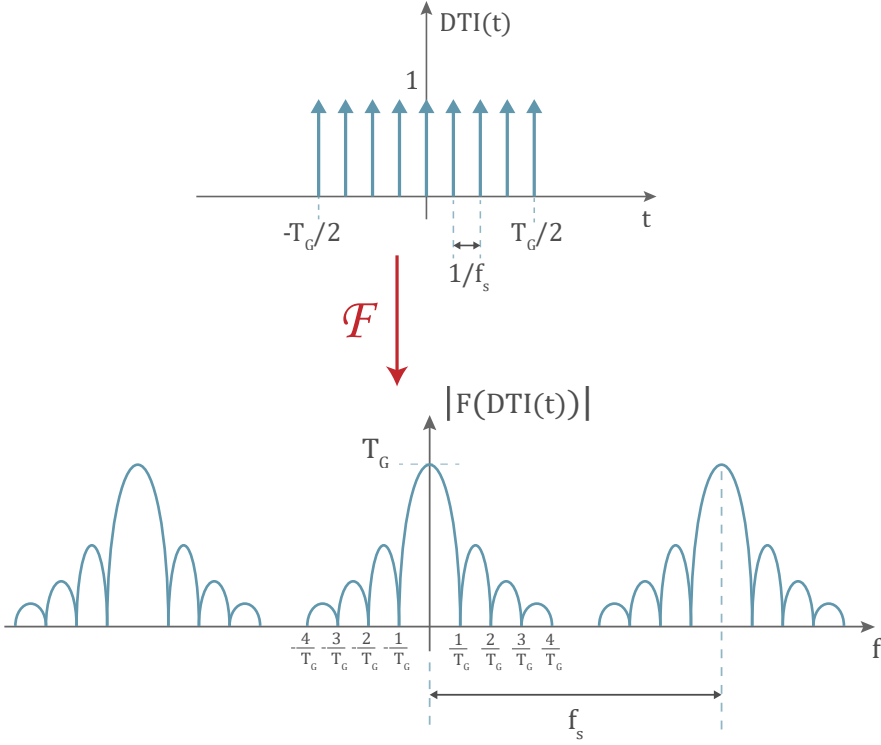


Figure 3.18: Time description (top) and frequency domain description (bottom) of the Discrete Time Integrator.

version of the analog GI. Sampling in time results in the replica in frequency of the transfer function, the result, as shown in Figure 3.18, is the superposition of various $\mathcal{F}(GI(t)) = T_G \text{sinc}(fT_G - kf_s)$ each centered at a multiple of the sampling frequency f_s . Since f_s is either 1 MHz in case of single channel operation or 125 kHz in 8-channel, parallel, operation the efficient working of the filter is ensured.

The digital gated integrator averages up to 2^{16} samples. Input data is accompanied by the Single Channel IP clock enable signal which carries the "new and valid data" information. The output data port brings out new data along with a ready signal every time the set number of averages is completed. Every wave the DDS produces must be a multiple of $976,5625\text{ Hz}$, as described in section 3.5.3. All unwanted harmonics are also a multiple of this frequency. The frequency of the digital sine wave for the

digital lock-in multiplication aliases the spurious signal (higher order harmonics) to a lower frequency. Offset and offset drift components are, in fact, placed at said frequency f_{mid} as seen in Figure 3.19. The choice of the number of averages the filter performs is, therefore, not random: one can choose to average any power of two number of samples as long as they cancel the most limiting undesired harmonic, and its multiples. The worst case happens when the second demodulation is used and the second carrier frequency is the lowest possible: $f_{mid} = 976,5625 Hz$. The highest number of averages is needed: 2^{16} . In general if:

$$f_{fn} = \frac{f_{clk}}{m} \quad , \quad f_{clk} = 64 MHz \quad (3.7)$$

where f_{fn} is the frequency of the first notch in the GI's frequency response, m is the number of averages and f_{clk} is the clock frequency fed to the integrator. And, for simplicity, only powers of two numbers of averages are allowed, $m = 2^n$ then the condition:

$$f_{fn} = \frac{f_{clk}}{2^n} = f_{mid} \quad (3.8)$$

represents the maximum f_{fn} available and the minimum n possible.

For example, if the second demodulation frequency is, $2 * 976,5625 Hz = 1953.125 Hz$ then the maximum first notch is at

$$f_{fn} = \frac{64 MHz}{2^n} = 1953.125 Hz$$

and the minimum number of averages is:

$$m = 2^n = \frac{64 MHz}{1953.125 Hz} = 2^{15} \quad (3.9)$$

However the choice $m = 2^{16}$ is still valid as the first notch will be at $976,5625 Hz$ and the second at $2 * 976,5625 Hz = 1953.125 Hz$ still canceling all harmonics, Fig 3.19 shows these two possible choices in frequency. Lastly, when activating the GI one must consider the effect on data throughput: if the GI is set with a

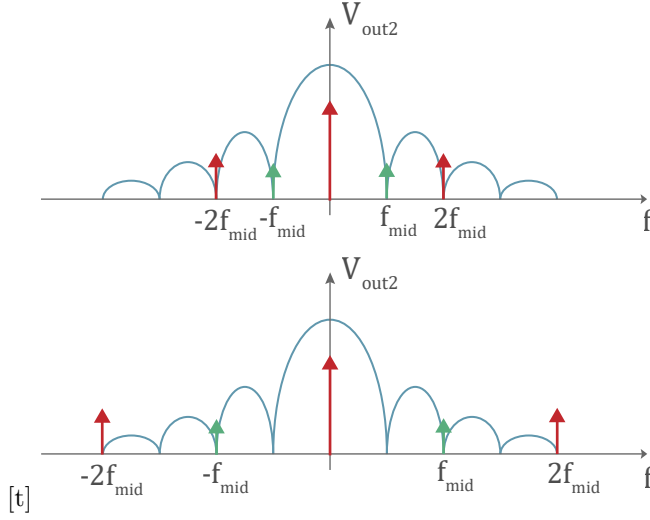


Figure 3.19: *GI set to the minimum number of averages required to cancel the lowest frequency harmonic (top). GI reasonable setting, the module is doing twice the minimum number of averages (bottom).*

depth equal to n , the throughput will be reduced by a factor 2^n .

$$f_{dout}^{GI} = \frac{f_{din}^{GI}}{2^n}$$

3.5.2 Sixteen Channels IP

This higher level IP handles the data coming from the 8 differential channels of the ASIC. Data to the FPGA come from an AD7616 ADC which is, in fact, composed of two 16b ADCs. We will refer to channel A and B as data coming from the IC A and B converter respectively. Data are sent through two SDI lines: A and B, communicating simultaneously. The two are processed in parallel. Therefore, each communication channels contains two analog channels converted into the digital domain. To acquire the whole 8 differential channels 8 SDI communications will be required. The order in which the different channels are sent is set by the FSM which configures the ADC, as described in 3.5.3. Because of this initial separation, the entire structures on the IP are present at least twice: to take advantage of ADC parallelism. The IP structure is summarized in Figure 3.20 where the multi-

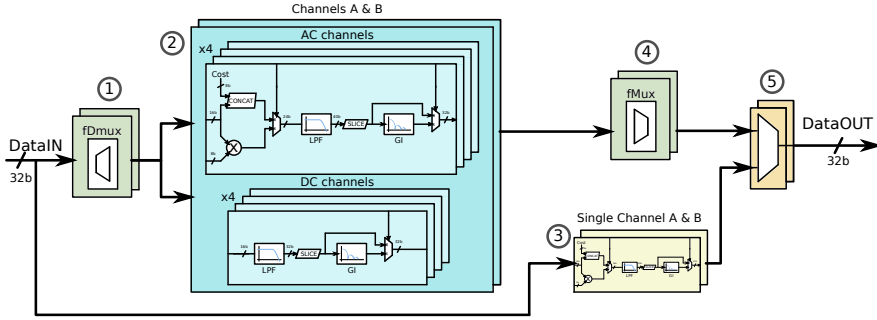


Figure 3.20: Sixteen differential channels IP: 1) *fDmux*, custom module distributing data to single channel IPs 2) full parallel DSP chain 3) single channel DSP for single wavelength analysis 4) *fMux*, custom module to regather parallel processed data into serial memory 5) Glue logic multiplexers to choose single or parallel DSP.

plicity of every block is highlighted: one can easily see how each component is replicated at least twice. Two different DSP chains are present:

- a single channel DSP, (3) in Figure 3.20;
- a fully parallel 8 differential DSP chains composed of (1), (2) and (4) in Figure 3.20;

Data and Ready Demux FSM

If the complete parallel data processing chain is selected, then the packets sent from the ADC need to be connected to their assigned processing chain. Each channel has its own single channel IP: either AC or DC depending on the channel nature. The task assigned to the demux FSM (*fDmux*) is to both sort the incoming data in the appropriate order and keep said order during the entire acquisition. This block can be thought of as two demultiplexers, one for data and one for data ready signals whose selection bits are controlled by a properly designed FSM. In Figure 3.20 block (1) is shown to be instantiated twice. The first instance handles the A channels and the second the B channels. Each block therefore manages 16-bit digital words. If the timing of incoming data is not perfectly taken into account some data may be erased or wrongly kept in the device memory: this may

result in the current data packet being assigned to the wrong channel data processing path. The order of the packets would be correct but the channels will be shifted to the wrong DSP chain. Rather than account for every possible combination, in which the device could be when settings are changed from the graphical user interface, and implement a custom reset sequence involving both FPGA and external resources, the choice was made to reset only the affected firmware blocks and have the FSM adapt to the condition. This way the ADC needs not to be reset nor any other IC needs to be reconfigured. To achieve this in the ADC stack, containing the channels conversion sequence, a known word is inserted. That value is therefore inserted periodically in the SDI string. The FSM expects this specific value periodically and if it is not found in the expected position, it will keep the outputs data ready to 0 until the correct order is restored. Therefore, the worst case after a reset sequence is waiting for the whole sequence stack to pass, which is at most 32 values.

Data and Ready Mux FSM

After the parallel DSP chains data need to be re-serialized since the memory in which they are stored is one for each module, that is each one needs to store 8 differential channels. Two identical blocks handle this specific function for ADC channels A and B, as shown in Figure 3.20 block (4). This block essentially works as a multiplexer, where the selection of the channel forwarded to the output is made through the data ready signals at the output of the previous DSPs. Since data come serially by SDI at 1 MHz throughput to the IP, also the outputs of the single channels will be arriving one at a time divided by 1 μsec . The arrival of two values at the same time is, therefore, an impossible condition and the block would ignore said data whenever it may happen. The data and ready signals at the input is otherwise simply forwarded to the output.

3.5.3 Single Module IP

This IP is much more complex than the previous two. In order to describe how it works, a functional view is shown in Figure 3.21. This is the first level of IP from bottom to top in which

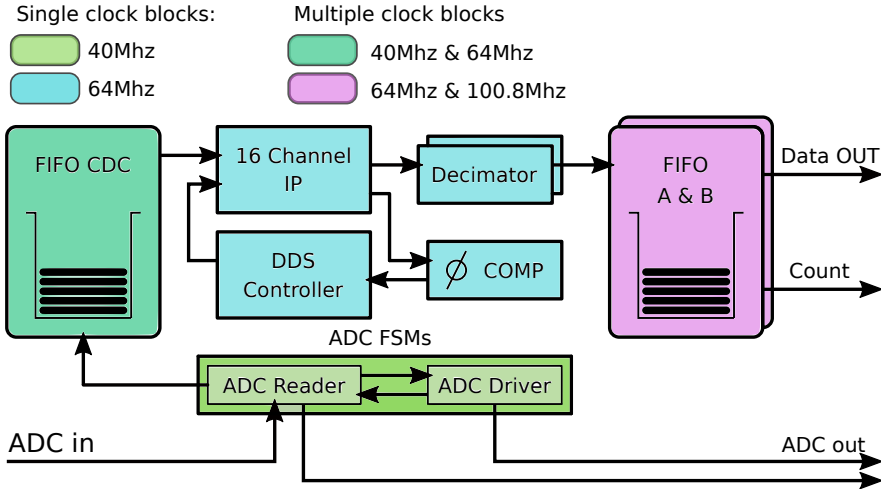


Figure 3.21: Functional description of the Single Module IP. Different clock inputs are shown by different colours.

more than one clock region is present. Three different clocks are, in fact, present at the inputs of the module:

- a 40 MHz clock which is used on blocks communicating with the ADC and, in general, dealing with the acquisition of the data;
- a 64 MHz clock fed to the entire digital signal processing chain;
- a 100.8 MHz clock which is used by the Front Panel IP to communicate between the FPGA and the computer.

In short, data are read through SDI from the corresponding ADC and passed to the first FIFO, the "cross domain clock" FIFO. Then, they are written synchronously to the 40 MHz clock which drives the ADC itself and is read from the lower level IP (Sixteen differential channels IP, 3.5.2) synchronously to the 64 MHz DSP clock. Lastly, after the decimator, data reach the output FIFOs written at 64 MHz and read out at 100.8 MHz by the Front Panel IP, to be sent out through the USB link.

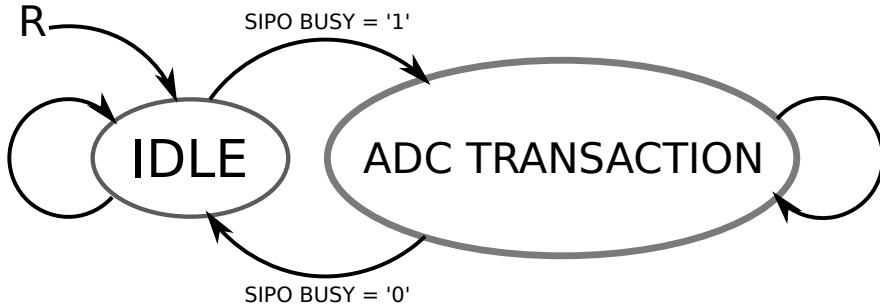


Figure 3.22: *State diagram of the ADC reader block.*

ADC Controller FSMs

The finite state machines are used for reading and for writing. Despite being equivalent to one single block, having two separate machines makes the hardware description easier to read and understand. In the subsequent paragraphs both will be described in detail. The purpose of these two blocks is to read and write from the ADC connected to the module. The converter is first setup by a serial interface, the configuration data are sent by the driver every time the IC settings need to be changed. Data come through two serial interfaces, A and B, carrying the two channels information separately. A "conversion start" pulse is sent to the ADC either once per transmission or once every N transmissions, where N is the depth of a memory stack in which the order of the conversions is configured. In order to send information through the serial interface the driver machine uses a custom Parallel-In-Serial-Out (PISO) module while the reader employs a Serial-In-Parallel-Out (SIPO) module to read.

ADC Reader The reader is a very simple state machine, as seen in Figure 3.22. The block remains in IDLE until the SIPO, which is directly connected to the ADC, is busy with a data transaction. The number of transactions can go from one up to 32, the maximum stack size of the ADC. Only once all the transactions are over, the busy signal of the SIPO will go down and the ADC reader will return to IDLE.

SIPO The Serial Input Parallel Output FSM is a finite state machine which acquires data from the SDI interface from the ADC and arranges it in parallel words. The FSM only has two states: idle and transfer. From idle it goes to transfer when an input trigger goes high to signal incoming data. The trigger comes from the ADC driver which handles ADC timing. Once data are read, a valid signal is set high. The block is able to handle both standard ADC operation and burst mode. An input bit selects the mode of operation. In case of burst mode a number N of data words will be processed within the transfer state. The number N of such words depends on the depth of the stack with which the ADC sequencer is setup, as described in Section 3.4.2.

ADC Driver ADC configuration is handled by this module: the data are 16bit word accompanied by a trigger. When the trigger is high the data present on the input is sent through SDI. As the ADC reading machine is acquiring data on the bus, this block simply waits. All these functionalities result into five states:

- RESET, resets the ADC IC and initializes the block.
- IDLE, waits flag signaling that data are ready to be written to the ADC or a "conversion start" which signifies that data will be coming from the ADC.
- WAIT ADC, is used to check for the ADC conversion to end, after it is a trigger is sent to the reader to start the process.
- ADC READ, is used to wait for data to be read from the ADC reader FSM.
- ADC WRITE, is used to send configuration data to the ADC.

The module can handle both normal and burst modes of the ADC. In either scenario, during the ADC READ state the module waits for the SIPO within the ADC reader to acknowledge the end of the data reading.

PISO As the name suggests the Parallel Input Serial Output is needed in order to serialize the configuration data the ADC driver supplies. It is implemented as a finite state machine with two

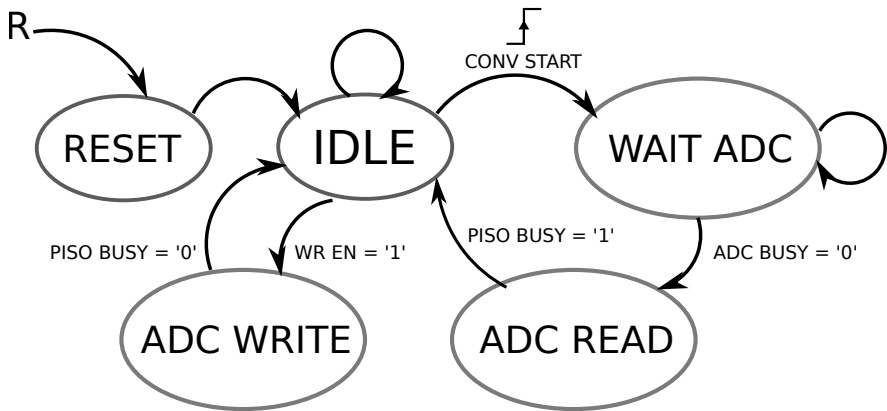


Figure 3.23: State diagram of the ADC driver block

states: idle and transfer. Data to be sent is a parallel input string along with a trigger signal. When the trigger goes up, the state switches to transfer and serialization starts. The communication follows SDI timing.

Cross Domain Clock FIFO

The acquisition chain is clocked at 40 MHz while the digital processing chain is clocked at 64 MHz, therefore there needs to be a clock domain change in the full data path. This clock domain crossing is handled by this FIFO. The FIFO uses the acquisition clock to synchronize the writing phase and the processing clock to synchronize the reading phase. The incoming data arrive at 1 MHz frequency, the ADC maximum throughput, and consist of the concatenation of the A and B channels: two 16 bit words become a single 32 bits word just before entering the FIFO. The reading is done at 64 MHz when the memory is full and stops whenever the empty signal goes up. During normal operation the FIFO should be empty and is therefore rather shallow: it can contain only 256 words.

DDS-Based Wave Generators

Direct Digital Synthesizers (DDS) are components able to output a periodic waveform from a fixed frequency clock. They are implemented essentially as a look-up table containing a period of

the waveform to be synthesized. The clock increments a counter which indexes the memory delivering at the output the repeating period of the waveform. The single module IP needs two DDS generated waveforms: a digital sine and a square wave which are needed respectively for the second and first demodulation.

The configured IP will communicate results and accept the configuration through AXIS communication. A custom firmware block is used to manage two of Xilinx DDS IPs and both send configurations and read the output waveforms to be presented to the system as parallel digital data. The first synthesizer is set to output a sine-wave but only the first bit is used, resulting in a square wave signal which can be adjusted in frequency and phase during operation. This wave is used to control the switching of the on-chip analog mixer. The second synthesizer is also set to output a sine-wave but this time it is fully utilized. This sine wave is used as the demodulating wave of the second demodulation.

The final aspect to consider is the multiplicity of this specific block: the block is present in the single module custom IP meaning there will be one instance per module. It follows that the square wave used for the mixer is used in all 8 ASIC channels. Also the sine wave generated for the digital demodulation will be the same for all 8 channels coming from the same ADC in the module.

Phase Compensator

This block is necessary because the phase of the incoming signal is unknown. In section 3.1 both demodulations are performed considering a demodulating wave in phase with the carrier, resulting in the maximum possible signal after multiplication.

What happens to the product of two out-of-phase waves? Let's consider the case of the product of two sine waves with arbitrary phase. If the input modulated signal is:

$$v_m(t) = A \sin(\omega_m t + \phi_m)$$

and the demodulating signal is:

$$v_{dm}(t) = \sin(\omega_{dm} t + \phi_{dm})$$

assuming the frequency of the waves is the same $\omega_m = \omega_{dm}$ then

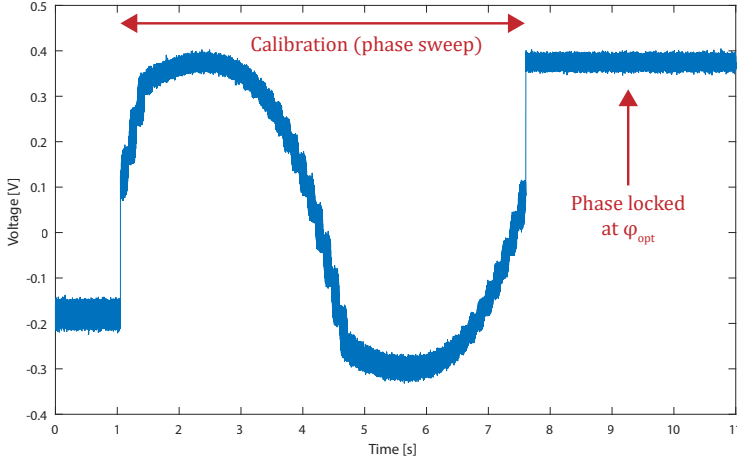


Figure 3.24: Output voltage of the DSP chain during the calibration. Initially the phase shift set with the function generator is not optimal and the output voltage is about $-0.17V$. The sweep always starts with $\phi_{dm1} = 0$ and ends with $\phi_{dm1} = 2\pi$, then it is locked to ϕ_{opt} corresponding, in this case, to an output voltage of about $0.38V$. The input signal is a square wave that gets only partially filtered out, thus generating the non-sinusoidal signal shown in the plot.

the product will be:

$$v_b = v_m(t)v_{dm}(t) = \frac{A}{2}\cos(\phi_m - \phi_{dm})$$

The factor $\cos(\phi_m - \phi_{dm})$ can easily become a problem as it is a value between -1 and 1 . In order to maximize this factor, a phase shift of the demodulating signal is necessary. This is achieved through a brute force approach by the phase compensator. The block essentially scans every possible phase shift value accepted by the DDS and maximizes the demodulated signal. As the DDS phase is coded with 16 bit there are 2^{16} possible phase values, is it necessary to check every one of them? No, it is not: since checking every one of the 65536 possible phases is excessive, the possibility to check a subset of phases is implemented.

The calibration phase is started by the user and must be performed while a constant and non-zero input signal is provided. Better results are obtained by exploiting the digital LPF, using

a small bandwidth so that the noise is reduced.

As a way of example, Figure 3.24 shows the output of the DSP chain during a calibration phase with $T_{cal} = 6.5s$. The measurement is carried out on the bench, using a function generator to provide the input signal to the system with well-defined phase shifts between the modulation and the demodulation signals. The generator is synchronized with the demodulation frequency generated by the DDS.

3.5.4 Global Block Design

All the signals necessary to control and manage a single module are provided by the "Single Module IP". These IPs constitute the main use of resources within the FPGA.

Motherboard DAC Control

The final result of a scan will be a collection of 76 different rectangular images corresponding to 76 different wavelengths acquired in parallel. The laser is fixed while the sample is moved around following a continuous scanning pattern. The image is divided into pixels, on each pixel a measurement will be performed for a set time. From now on, we will refer to the time per pixel as T_{dwell} . The DAC on the motherboard is responsible for sample movement. The position of the sample on the x and y axis will be proportional to the voltage output of the DAC.

In order to manage the complex function just described, two firmware blocks were implemented: "DAC com" and "DAC controller". The Communication Block handles (DAC_com) communication from the GUI which will send the configuration data through a custom protocol. The block will translate the instructions, format the data for serial communication and raise a trigger and the controller block (DAC_controller) will send the data through serial communication to the DAC.

Figure 3.26 shows the control flow diagram of the structure. The resulting scanning pattern is shown in Figure 3.25. Since the laser is continuously firing, the scanning pattern chosen is a continuous path which always starts at the top left corner of the sample and ends in either the bottom left or bottom right corner. The parameters of the scan are freely chosen by the user

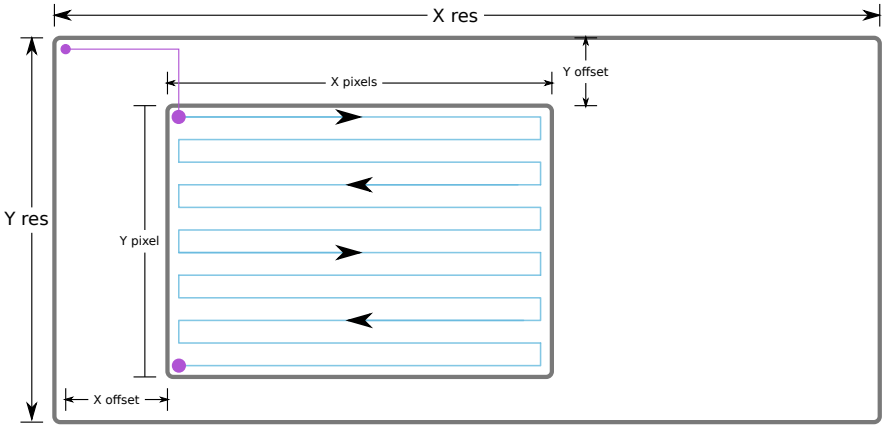


Figure 3.25: Scanning pattern

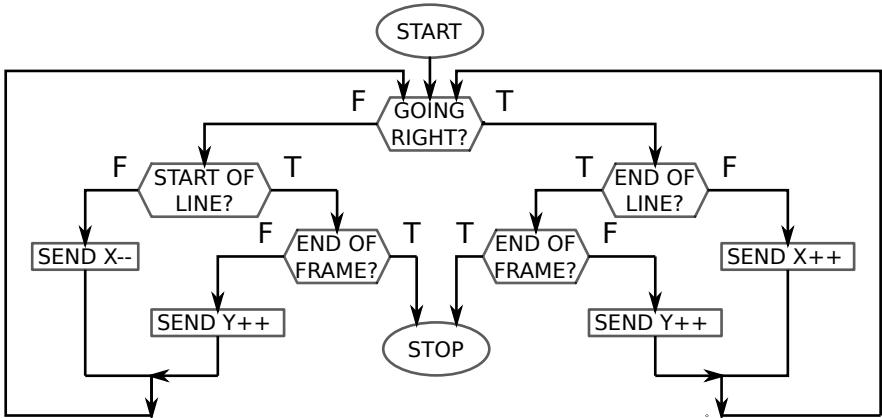


Figure 3.26: Scanning pattern control structure

and result in a rectangular image which can be placed anywhere in the full possible scanning area.

Other Blocks

Other blocks required are:

- Acquire gen: used to time the conversion start pulse for the 10 modules ADC.
- Serializer: used to serially send 80bit configuration data to the 10 ASICs on the modules.

- IO expander controller: used to implement an FSM that manages the IO expanders on the motherboard and their communication implementing an I2C protocol on the FPGA.
- LF clock gen: generates a 39 KHz clock used by the serializer to send configuration data and by the DAC which can optionally control the gain of the ASIC.

3.5.5 FPGA-PC Communication

The maximum throughput requirements of the system in relation to the computer can be now assessed. Considering a single channel during parallel operation the sample rate is $f_s = 125\text{ kHz}$, each channel consisting of 32 bits of output data. Therefore, the single channel throughput is at most $4\frac{\text{Mbit}}{\text{s}}$. Each module has 8 differential channels, which means a throughput per module of $4\frac{\text{Mbit}}{\text{s}} \cdot 8 \cdot 2 = 64\frac{\text{Mbit}}{\text{s}}$. Finally, the entire system consists of 10 modules:

$$f_{Dout} = 4\frac{\text{Mbit}}{\text{s}} \cdot 8 \cdot 2 \cdot 10 = 640\frac{\text{Mbit}}{\text{s}} = 80\frac{\text{MByte}}{\text{s}}$$

This estimate assumes the system in fast mode, with the GI off. Another aspect to take into account is the resulting number of channels: 10 modules with 8 differential channels result in 80 channels. This is because despite the diode arrays consisting of 76 differential sensing channels the remaining 4 channels are used to monitor the system behavior. The amount of data coming through the USB is therefore equivalent to 80 differential channels. Communication is controlled through a Cypress FX3 present on the Opal Kelly XEM7310 board. To simplify communication design, the FrontPanel SDK by Opal Kelly is employed. The software development kit provides drivers and APIs to communicate via software with the FPGA and, firmware side, an HDL IP.

3.6 Graphical User Interface

A Graphical User Interface (GUI) was developed for the 76-channel platform using C# programming language in Microsoft Visual Studio environment. C# is an object-oriented program-

ming language created by Microsoft around the year 2000. The interface design is straightforward, as various components from the Visual Studio toolbox (e.g., text boxes, buttons, charts, etc.) can be added to the form via simple drag-and-drop operations.

Since the interface is based on the Opal Kelly FrontPanel SDK, the FrontPanel DLL must be included in the “References” of the Visual Studio project (or solution), and the FrontPanel driver has to be installed on the host machine to enable communication with the FPGA. Thanks to the Endpoints provided by Opal Kelly, the interface offers complete control of the platform through the FPGA and enables smooth, real-time visualization of the acquired data by processing the incoming data stream.

The implemented features include:

- connecting to the FPGA and uploading the bitfile;
- configuring the 10 ADCs with the desired input range, sequencer steps, and oversampling;
- setting the 10 DACs on the modules to generate the required control voltages for the VGAs in the custom ICs;
- visualizing the AC and DC traces from the selected channel;
- programming the preamplifier and subtractor gains for each channel;
- adjusting the demodulation clock frequency and phase for each module;
- enabling offset cancellation via a two-step frequency down-conversion technique;
- saving data, where the AC and DC traces of each channel are stored as matrices in separate CSV (comma-separated values) files.

A screenshot of the GUI designed for the spectrometer is shown in Figure 3.27.

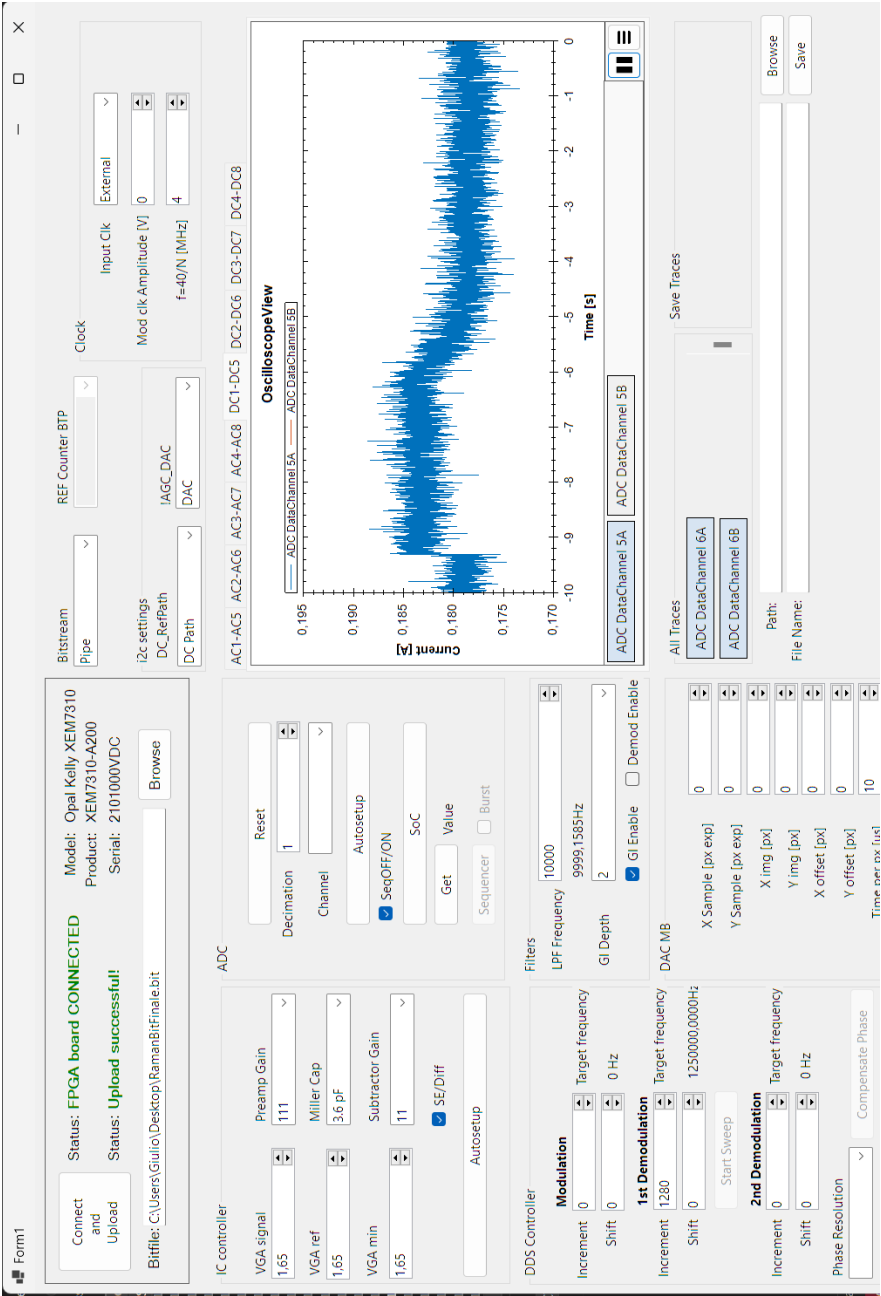


Figure 3.27: Graphical User Interface Screenshot

CHAPTER 4

Platform Validation and Results

Some of the measurements reported here are published in [24].

Figure 4.1 shows the 76-channel system described in the previous chapter. The modular architecture of the platform is clearly visible, with the ASIC bonded and covered by the black protective box. The motherboard accommodates the FPGA responsible for signal management and data transfer, as well as the power supply connector and eight SMA interfaces. These connectors enable precise synchronization between the electronic platform and the optical setup, and they also provide control signals for the sample positioning stage.

The following sections present the results of the electrical and optical validation of the developed platform, highlighting its performance.

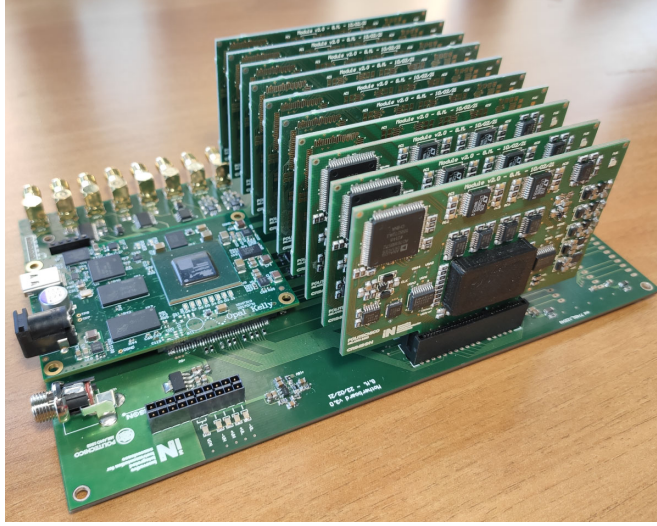


Figure 4.1: *76 Channel Platform: motherboard + 10 modules.*

4.1 Electrical Validation

The platform has initially been validated without any optical signals incident on the photodiodes, operating in both single and double demodulation modes. Figure 4.2 illustrates a comparison of the system output noise on a single channel. The single demodulation mode (depicted in blue) exhibits a notable offset at the output of the analog chain in the order of tens of mV, with an observable drift of the mean value over several minutes of continuous data acquisition. The red trace, instead, shows a smaller offset and a smaller standard deviation: it corresponds to a 10 minute measurement, enabling the second demodulation step.

For fast measurements, the single-demodulation approach proves effective, as offset drift on the microsecond timescale can be considered negligible. In this case, the addition of a second demodulation stage would not provide any benefit, as it would require a smaller bandwidth and would consequently increase the measurement time. For relatively high power incident on the photodiodes, single demodulation provides reliable results, as any fluctuations in the mean signal value are negligible, being masked by the shot-noise.

However, for the measurement of very low optical power sig-

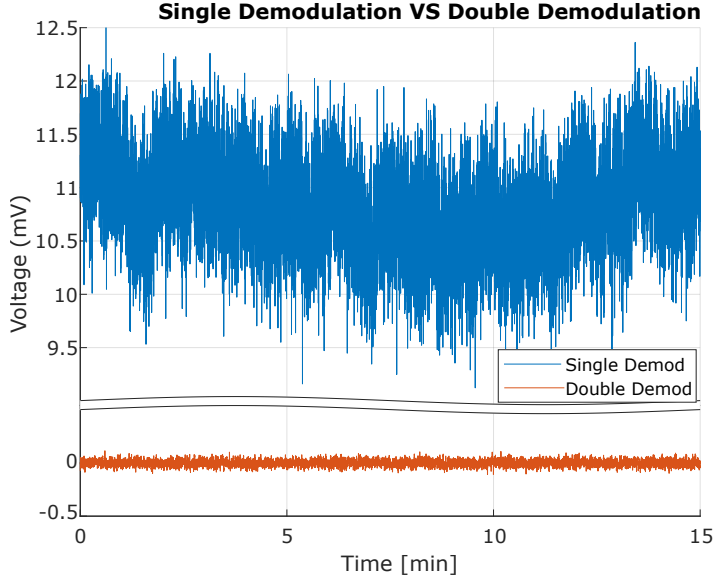


Figure 4.2: *Voltage over time example with single (blue) and double (orange) demodulation and no input optical signal.*

nals, the double demodulation mode (shown in orange) proves to be the better option: it eliminates offset drift and significantly reduces noise.

Figure 4.3 presents both theoretical and measured performance metrics for single and double demodulation across various low-pass filter (LPF) bandwidths.

The theoretical expectations indicate that the double demodulation is $\sqrt{2}$ times less effective in terms of the minimum measurable signal; this degradation occurs due to the additional demodulation process (refer to chapter 3.1).

Unfortunately, temperature drift and fluctuations impose limitations on the performance of single demodulation, primarily due to a very low frequency component of the offset. Figure 4.3 demonstrates that reducing the filter bandwidth below 1 kHz does not lead to a decrease in the minimum measurable signal in single demodulation mode. Activating the digital sinusoidal demodulation along with the subsequent digital signal processing (DSP) chain surpasses the limitations, resulting in an improvement of up to 22 dB in the minimum detectable signal.

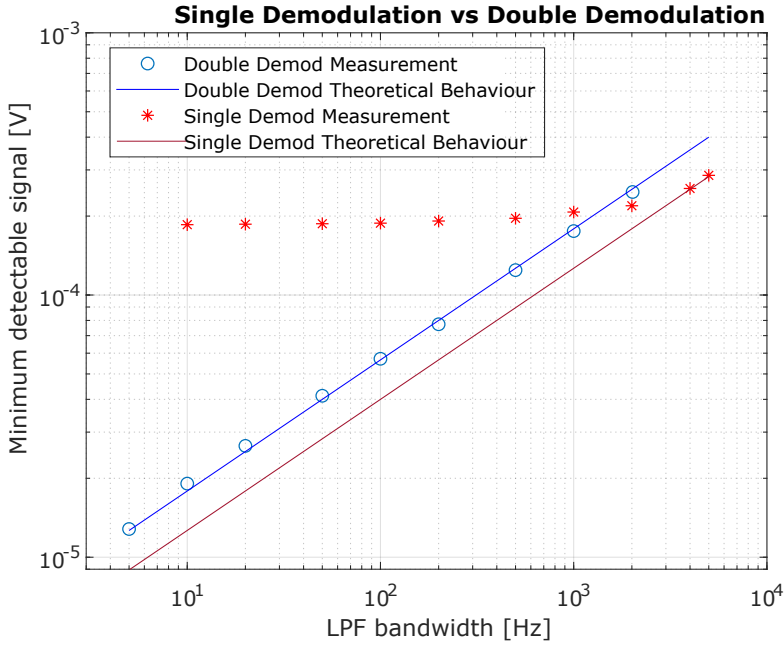


Figure 4.3: *Minimum detectable signal. Theoretical (continuous lines) and experimental (points) behaviors in single (red) and double (blue) demodulation operation. Measurements performed varying filter bandwidth and no optical input signal.*

4.2 Optical Validation

After the electrical validation, a simulated Raman signal was set up in order to evaluate optical performance. In order to optically validate the platform prior to demodulating an actual Raman signal, the optical setup was modified so that a known modulated signal could impinge on the photodiodes and be acquired.

Two main experiments were carried out:

- to evaluate the minimum detectable value while keeping the lock-in bandwidth constant (in both single and double demodulation modes) and varying the incident optical power on the photodiode;
- to evaluate the minimum detectable signal by keeping the optical power constant and varying the LPF bandwidth.



Figure 4.4: Fixed bandwidth equivalent input current noise at various input optical powers for single and double demodulation operations. In green the shot noise limit.

Figure 4.4 shows the equivalent current noise at the input of the device with a fixed BW (100Hz) and various optical power incident on the photodiode, between 1 and 300 μW .

In green, the theoretical behavior of the shot noise at the input of the acquisition chain is represented, according to the shot noise expression: $I_n = \sqrt{2qI_{ph}BW} = \sqrt{2q\sigma P_{ph}BW}$, where σ is the photodiode responsivity and P_{ph} the optical power incident on the PDA.

It is possible to notice how the measure is close to the theoretical shot noise limit: for optical power in the 60 μW – 300 μW range, single demodulation follows the theoretical predictions, whereas double demodulation yields a degraded signal, consistent with theory.

For optical power lower than 60 μW the increased noise observed in the single-demodulation case limits power resolution. Despite the double demodulation technique increases the mini-

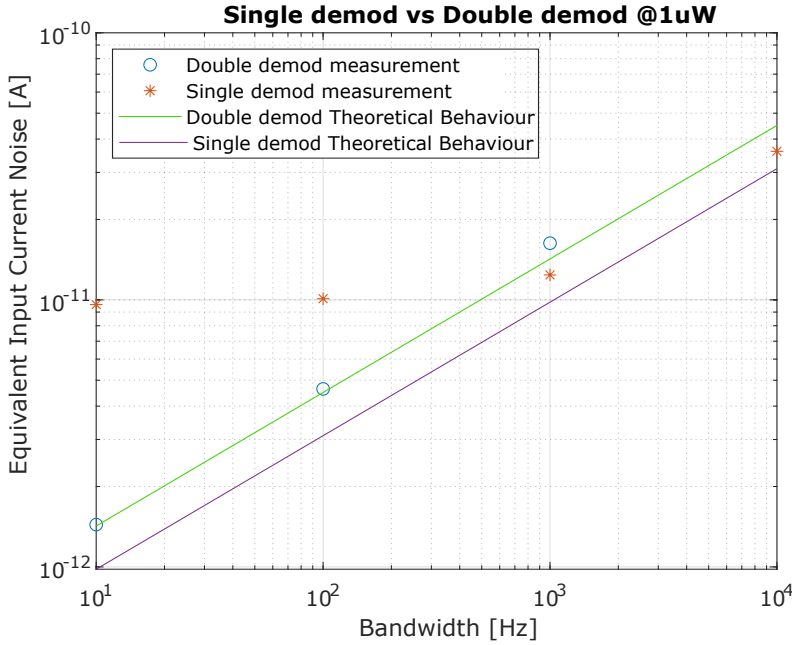


Figure 4.5: Fixed incident power equivalent input current noise at various bandwidth for single and double demodulation operations. In green and purple the theoretical behaviours, in particular the single demodulation theoretical behaviour coincides with the shot noise limit.

imum detectable signal by a factor $\sqrt{2}$, it also enables operation closer to the shot-noise limit for optical powers down to the order of μW .

Figure 4.5 shows the equivalent input current noise at a fixed power incident on the photodiode of $1 \mu W$ and different LPF bandwidths.

Figure 4.3 shows at 10 Hz the double demodulation being 20 dB better than the single demodulation, while Figure 4.5, with the presence of optical signal and the same low-pass filter bandwidth, the double demodulation signal is 14 dB better than the single. This leads to the conclusion that the noise of the optical signal (shot noise) is more significant than the electronic noise contribution, ensuring that the system is shot noise limited.

In particular the experimental optical validation with a bandwidth of 10 Hz and incoming optical power of $1 \mu W$ shows a

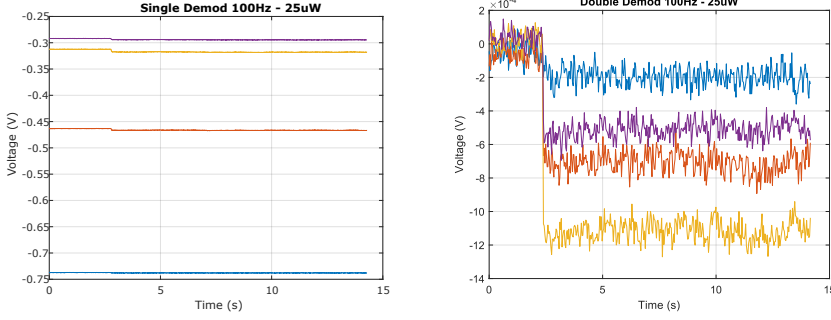


Figure 4.6: *Four channels acquisitions of no signal and then the same power optical signal in single demodulation mode (on the left) and 2-step frequency down conversion mode of operation (on the right).*

minimum detectable power of 3 pW, that represents a normalized Raman signal of 3 ppm.

Multi-channel optical validation

In order to validate parallel working mode of the platform, the test laser beam is spread over and focused on multiple photodiodes. A parallel acquisition of 4 channels is shown in Figure 4.6 where on the left single demodulation is employed and on the right the double demodulation is enabled. While single demodulation remains the preferred mode of operation for fast acquisitions, double demodulation removes offsets and its fluctuations allowing for resolutions beyond the commercial instruments currently available on the market. Figure 4.6 highlights how the offsets are different for each channel and how significant they are with respect to the signal of interest. The double demodulated signals before any optical signal are close to zero for all four channels and drastically change once the optical power impinges on the PDA.

4.3 Raman Signal Measurement

Once the multichannel lock-in amplifier had been validated from an electronic standpoint, and its achievable resolution—limited by shot noise—had been assessed, the system was integrated into an optical setup specifically designed for SRS experiments. The

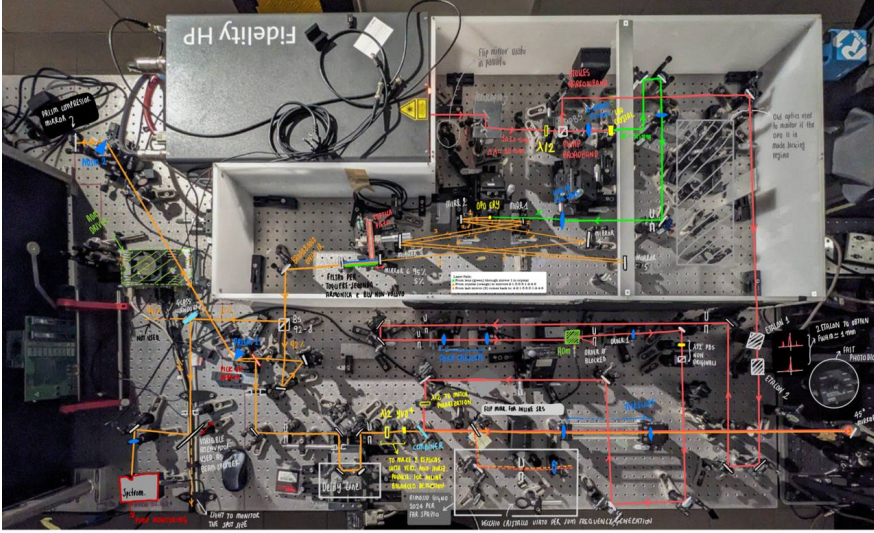


Figure 4.7: Photo of the optical setup for Broadband Stimulated Raman Spectroscopy. 80 MHz laser repetition rate (Fidelity HP), Optical Parametric Oscillator (OPO) in the white box, optics...

first validation of the combined electronic and optical system was then performed by inserting a nonlinear crystal capable of generating a so-called sum-frequency in place of the Raman sample. Although the sum-frequency is not a true SRS signal, it provides a reliable reference for verifying the correct operation of the lock-in and for synchronizing the laser and optical modulator with the electronic platform. A photo of the optical setup is reported in Figure 4.7.

Under these conditions, it is possible to observe a signal whose intensity is typically higher than that of an actual SRS signal. By acquiring the previously described signal, it was also possible to determine the minimum time per pixel, and therefore the maximum bandwidth at which the system was able to read a signal under those conditions. The measurement shown in Fig. 4.8 was performed with a 2.5 kHz bandwidth and a corresponding dwell time of approximately $64 \mu\text{s}$. The temporal trace displayed corresponds to the acquisition of a single channel; however, due to the intrinsically parallel nature of the platform, the same acquisition time is sufficient to simultaneously record up to 76 channels.

To verify that the observed signal was indeed generated by

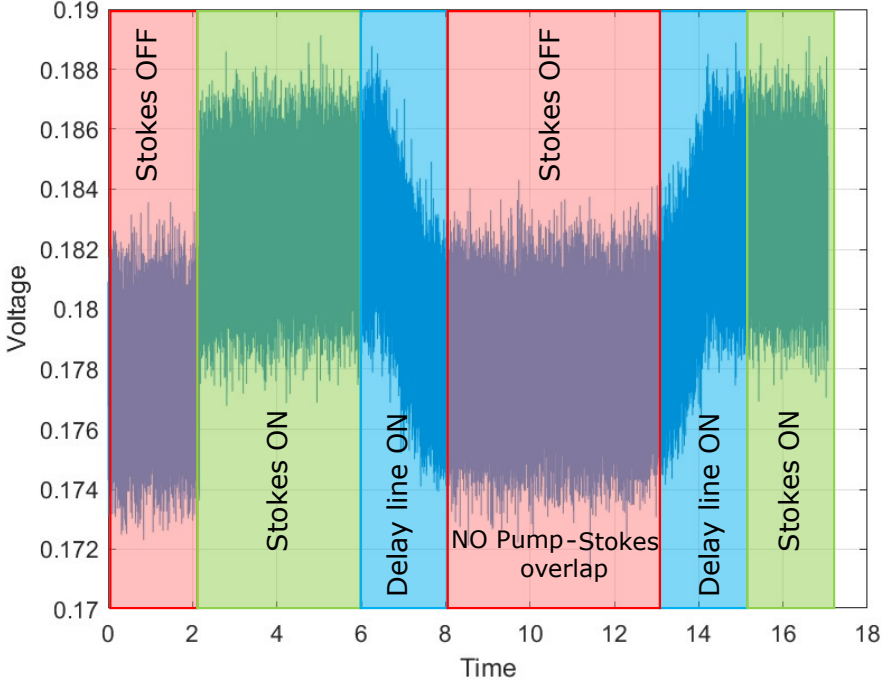


Figure 4.8: Output trace of the sum-frequency experiment. Red boxes: Stokes OFF, Green boxes: Stokes ON, Blue boxes: Delay line ON to remove the pulses overlap.

the temporal overlap of the pump and Stokes pulses, the delay between the two pulses incident on the crystal was varied by moving a delay line. As expected, the acquired signal decreases progressively as the delay increases, eventually vanishing into the baseline.

4.3.1 Unbalanced Measurements

The first measurements were carried out using an unbalanced optical setup, due to the complexity involved in implementing a balanced configuration. Using β -carotene in toluene as sample (that has been selected since it exhibits a sufficiently large signal in the fingerprint region), it is possible to observe a signal of $600 \mu V$ (equal to 360 ppm with a mean optical power of $\approx 100 \mu W$) with a dwell time of 8 ms.

The resulting measurement is shown in Figure 4.9. It can be observed that the trace exhibits low-frequency fluctuations

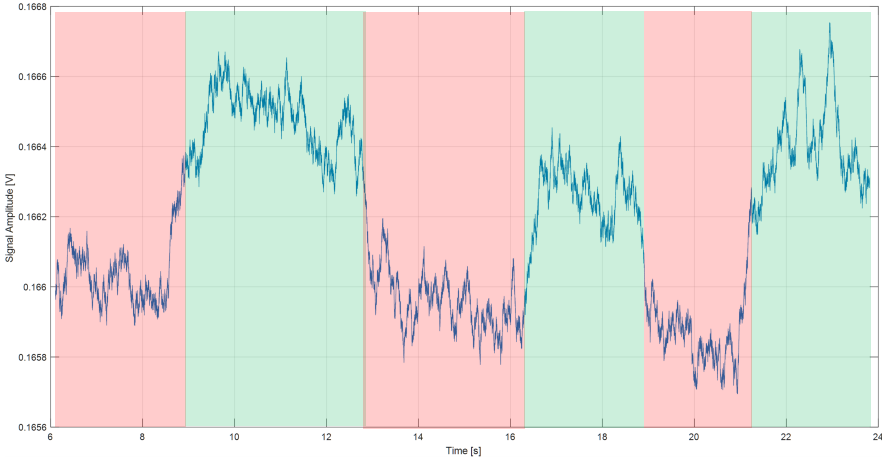


Figure 4.9: Output trace of an unbalanced experiment of SRS spectroscopy with a β -carotene in toluene sample. Red boxes: Stokes OFF, Green boxes: Stokes ON.

caused by laser instabilities, which can be compensated for by adopting a balanced optical setup and a differential measurement approach, as presented in the following section.

4.3.2 Balanced Measurements

Although, in case of white noise (uncorrelated), a differential approach reduces the signal-to-noise ratio by a factor of $\sqrt{2}$, in this case it allows for a cleaner signal by removing common-mode effects and fluctuations due to laser RIN. By configuring the optical setup in a balanced arrangement and enabling differential measurement on the lock-in, several measurements were performed, varying the bandwidth and thus the pixel dwell time from 160 μ s to 16 ms.

Using the same sample as in the unbalanced measurement, it was possible to observe a signal of 800 μ V (corresponding to 480 ppm with a mean optical power of $\approx 100 \mu$ W). Although low-frequency fluctuations are still present, they are attenuated compared to the previous case. Figure 4.10 represents three different traces in different bandwidth conditions.

In the coming months, the optical setup will be adapted to perform a 76-channel measurement, in order to cover the entire PDA array and acquire a full SRS spectrum.



Figure 4.10: Output traces of a balanced experiments with β -carotene in toluene sample. Red boxes: Stokes OFF, Green boxes: Stokes ON. 160 μ s dwell time and 509 μ V standard deviation (top), 1.6 ms dwell time and 195 μ V standard deviation (middle), 16 ms dwell time and 41 μ V standard deviation (bottom).

Part II

Pump-Probe

CHAPTER 5

Introduction to Pump-Probe Spectroscopy

In this chapter, following a detailed introduction to Pump–Probe spectroscopy, the motivation for a custom multichannel spectrometer will be discussed, together with its placement within the current landscape of commercially available instrumentation and the approaches already reported in the literature for this type of spectroscopy.

5.1 Physics of Pump–Probe Spectroscopy

Femtosecond pulses are widely used for time-resolved studies of ultrafast dynamical processes in chemical, solid-state, and biological systems [28–30]. Their ultrashort duration makes them a unique tool for both excitation and “stop-action” measurements, enabling the investigation of microscopic and quantum mechanical phenomena occurring on ultrafast timescales. Some experiments where ultrafast time-resolved spectroscopy is a powerful

tool are: photoexcited charge carriers in crystal lattice, dynamics of solvated chemical species that interact with their fluctuating liquid-state environment, etc...

The most employed time-resolved optical experiment is the so-called pump-probe. Let us start from a general description. A short pulse (the pump) impinges on the sample and excites it in some way. This excitation corresponds to a change in some material properties $\mathcal{T}$, which in many cases is an optical property.

$$\mathcal{T}(t) \rightarrow \mathcal{T}_0 + \Delta\mathcal{T}(t - t_0) \quad (5.1)$$

where $\mathcal{T}_0$ and $\Delta\mathcal{T}$ are respectively the initial values of property $\mathcal{T}$ and the change in $\mathcal{T}$ induced by the pump pulse arriving at time t_0 . Then, a second pulse (the probe) impinges on the sample with a time delay τ relative to the pump pulse. Usually the intensity of the probe is smaller than the one of the pump ($I_{probe} \ll I_{pump}$). By detecting the probe pulse after its interaction with the sample, it is possible to monitor $\Delta\mathcal{T}$ at time $t - t_0 = \tau$. By performing a series of measures with different τ , we can map the complete time dependence of the material response by looking at $\Delta\mathcal{T}(\tau)$. Different material properties can be probed:

- **Transmission measurements** provide information on the time-resolved absorption coefficient and are commonly used to investigate phenomena associated with relaxation from photoexcited energy states.
- **Fluorescence yield** may monitor the occupation of the states.
- **Refractive index changes** can be observed through reflectivity changes, interferometric detection methods or by changes in the optical spectrum.
- **Dichroism and birefringence** (referring, respectively, to anisotropic absorption and anisotropic refractive index) provide insights into the orientation dynamics of anisotropic molecules.
- **Coherent vibrations** can occur in either isolated molecules or crystalline lattices and can be detected through

the third-order nonlinear polarization response associated with these vibrations.

The discussion below will concentrate on transmission measurements.

5.2 Pump-Probe Spectroscopy: Transmission Measurements

The first pulse (the so-called "pump") impinges on the sample. Since it is resonant with a transition of the system, it promotes some electrons from the ground state to an excited state. Looking at the transmission (or reflection) change of a delayed weak pulse (the so-called "probe"), it is possible to monitor the resulting system evolution. This transmission change ΔT is a function of the time delay τ_{pr} between the pump and the probe pulses. Typically, a mechanical delay line is used in order to control the delay between pulses.

Let us assume that two pulses arrive on the system under study. The first one is the pump pulse with an intensity I_{pump} and it is centered at time zero t_0 . The second one is the probe pulse, which arrives with a delay with respect to the pump pulse equal to τ_{probe} and an intensity I_{probe} . The pump pulse perturbs the linear optical absorption coefficient of the sample (α) and the induced variation ($\Delta\alpha$) is:

$$\Delta\alpha(t) = \int_{-\infty}^t I_{pump}(t') A(t - t') dt' \quad (5.2)$$

where $A(t)$ is the impulse response of the optical property under exam for a given material. This equation represents the convolution between $I_{pump}(t)$ and $A(t)$, i.e. the induced variation of the linear optical absorption coefficient can be written as:

$$\Delta\alpha(t) = I_{pump}(t) * A(t) \quad (5.3)$$

Considering a sample with thickness d and linear optical absorption α_0 , according to the Lambert-Beer law, it is possible to compute the absorbed intensity and so the transmitted fraction (I_{tr}):

$$I_{tr} = I_0 e^{-\alpha_0 \cdot d} \quad (5.4)$$

where I_0 represents the total intensity that impinges on the sample.

In a transmission pump-probe experiment, it is possible to notice a variation of the optical absorption of the probe pulse before and after the pump pulse. The intensity variation ΔI_{probe} can be written as:

$$\begin{aligned}\Delta I_{pr}(t) &= I_{pr}(t)e^{-(\alpha_0 + \Delta\alpha(t))d} - I_{pr}(t)e^{-\alpha_0 d} \\ &= I_{pr}(t)e^{-\alpha_0 d}(e^{-\Delta\alpha(t)d} - 1)\end{aligned}\quad (5.5)$$

By assuming that the perturbation induced by the pump is small ($\Delta\alpha d \ll 1$), exploiting the Taylor series, the first order approximation is:

$$\Delta I_{pr} \simeq -I_{pr} \cdot e^{-\alpha_0 d} \cdot \Delta\alpha(t)d \quad (5.6)$$

It means that the transmitted energy variation of the probe pulses, due to the pump effect, is equal to:

$$\begin{aligned}\Delta E_{pr}^{tr}(\tau_{pr}) &= \int_{-\infty}^{+\infty} \Delta I_{pr}^{tr}(t') dt' \approx \int_{-\infty}^{+\infty} I_{pr}^{tr}(t' - \tau_{pr}) \Delta\alpha(t) dt' \\ &= \int_{-\infty}^{+\infty} I_{pr}(t' - \tau_{pr}) e^{-\alpha_0 d} \cdot \left(\int_{-\infty}^t I_{pump}(t'') A(t' - t'') dt'' \right) dt' \\ &= k \cdot I_{pr}(t) \otimes [I_{pump} * A(t)]\end{aligned}\quad (5.7)$$

where $\otimes$ is the cross-correlation product and $k = e^{-\alpha_0 d}$. By exploiting the following convolution and cross-correlation properties:

$$f \otimes (g * h) = (f \otimes g) * h$$

equation (5.7) can be rewritten as:

$$\Delta E_{pr}^{tr}(\tau_{pr}) = [I_{pump}(t) \otimes I_{pr}(t)] * A(t) \quad (5.8)$$

where:

$$I_{pump}(t) \otimes I_{pr}(t) = \int_{-\infty}^{+\infty} I_{pump}(t') \cdot I_{pr}(t + t') dt' \quad (5.9)$$

The result provided by 5.9 suggests that the outcome of a pump-probe experiment is the convolution of the impulse response of

the sample under test with the correlation between the pump and probe pulses, and shows why we need very short pulses in order to resolve fast temporal dynamics.

The equation 5.7 can be simplified in the case of well-separated pulse limit, i.e. when the pump and the probe pulses are not temporally overlapped (τ_{pr} is much longer than the duration of the pump-probe correlation):

$$\begin{aligned}\Delta E_{pr}^{tr}(\tau_{pr}) &\approx \int_{-\infty}^{+\infty} I_{pr}(t) e^{-\alpha_0 d} \Delta\alpha(\tau_{pr}) d dt \\ &= e^{-\alpha_0 d} \Delta\alpha(\tau_{pr}) d \int_{-\infty}^{+\infty} I_{pr}(t) dt \\ &= -\Delta\alpha(\tau_{pr}) d \cdot E_{pr} e^{-\alpha_0 d} = -\Delta\alpha(\tau_{pr}) d \cdot E_{pr}^{tr}\end{aligned}\tag{5.10}$$

The normalized transmission change of the probe energy $\frac{\Delta T}{T}$ of the sample can then be defined as:

$$\frac{\Delta T}{T} = \frac{\Delta E_{pr}^{tr}}{E_{pr}^{tr}} = -\Delta\alpha(\tau_{pr}) d \tag{5.11}$$

A more detailed analysis of the physic processes behind Pump-Probe spectroscopy is presented in [31]: that work discusses how to push the temporal resolution limits of transient absorption spectroscopy in order to detect very fast processes (energy relaxation, energy or charge transfer, vibrational coherence) taking place in molecules.

In most Pump-Probe experiments, the pump and probe pulse wavelengths are different in order to study the occupation of different energy states for the same delay τ_{pr} . In this way a Pump-Probe spectrum is obtained for each value of delay between the two pulses. By scanning different delay values, the resulting measure of a Pump-Probe transmission experiment is the map $\frac{\Delta T}{T}$, as function of wavelength (λ_{pr}) and delay (τ_{pr}). The experimental information on ΔT is obtained by measuring the transmission coefficient in presence or absence of the pump pulse, and then calculating:

$$\frac{\Delta T}{T}(\lambda_{pr}, \tau_{pr}) = \frac{T_{pump,off}(\lambda_{pr}, \tau_{pr}) - T_{pump,on}(\lambda_{pr}, \tau_{pr})}{T_{pump,off}(\lambda_{pr}, \tau_{pr})} \tag{5.12}$$

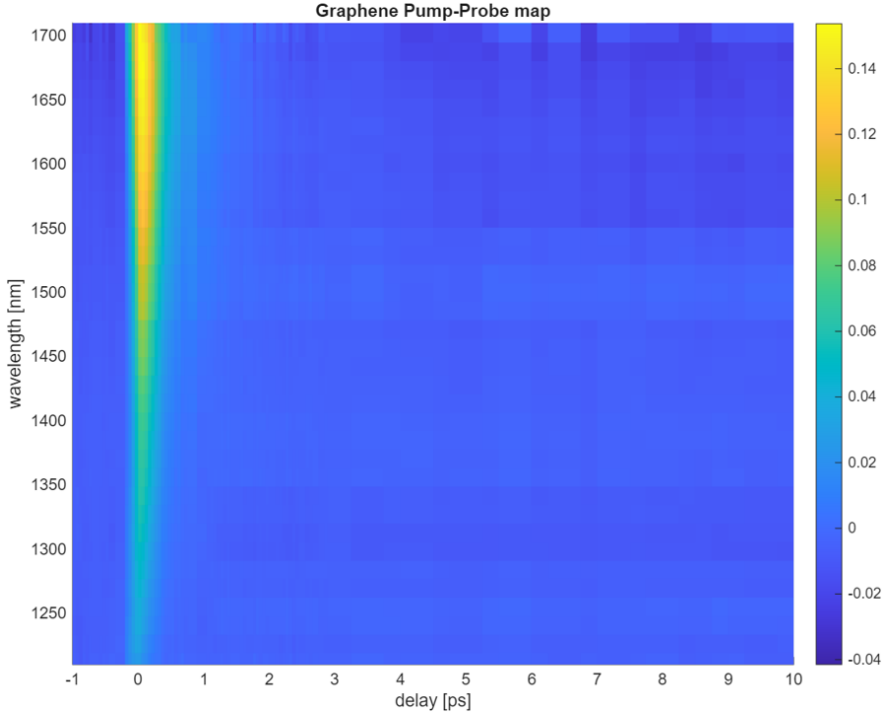


Figure 5.1: Example of a Pump-Probe spectroscopy map. On the horizontal axis τ_{pr} is reported, on the vertical axis λ_{pr} . The color of the points represents the value of $\frac{\Delta T}{T}$ expressed as a percentage.

Equation 5.12 shows how the pump-probe map is a function of λ_{pr} and τ_{pr} .

The transmitted optical power of the probe pulse ΔI , strictly related to ΔT , is measured by stimulating the sample with two successive probe pulses: a first pulse (named $I_{pump,off}$), interacting with the sample when it has not been stimulated by the pump pulse yet, and a second one (named $I_{pump,on}$), which probes the effect produced by the pump pulse:

$$\frac{\Delta T}{T} = \frac{\Delta I_{pr}}{I_{pr}} = \frac{I_{pump,off}(\lambda_{pr}, \tau_{pr}) - I_{pump,on}(\lambda_{pr}, \tau_{pr})}{I_{pump,off}(\lambda_{pr}, \tau_{pr})} \quad (5.13)$$

A typical result of a Pump Probe experiment is the map shown in Figure 5.1. The delay (in *ps*) between pump and probe pulses, τ_{pr} , is reported on the horizontal axis, while the different wavelengths (in *nm*) are reported on the vertical axis. The intensity

of each point on the map represents a different value of normalized transmission change $\frac{\Delta T}{T}$ for a given combination of τ_{pr} e λ_{pr} . The intensity variation due to two successive probe pulses ΔI_{pr} is significantly lower than the mean intensity of the probe pulse I_{pr} . Typical values of $\frac{\Delta I_{pr}}{I_{pr}}$ and therefore $\frac{\Delta T}{T}$ are in the range $10^{-6} - 10^{-3}$.

In order to distinguish such small variation from the noise introduced by the measurement process, it is necessary to perform hundred or even thousands of measurements, that are then averaged. In this way, the resulting signal is:

$$\frac{\Delta I_{pr}}{I_{pr}} = \frac{1}{N} \sum_{i=1}^N \frac{I_{pump,off}(\lambda_{pr}, \tau_{pr}, i) - I_{pump,on}(\lambda_{pr}, \tau_{pr}, i)}{I_{pump,off}(\lambda_{pr}, \tau_{pr}, i)} \quad (5.14)$$

where N denotes the number of averages performed, and thus the number of $I_{pump,off}$ and $I_{pump,on}$ differences, required to achieve the desired SNR.

5.3 Pump-Probe Optical Setup

Pump-probe setup is based on two laser beams temporally synchronized thanks to a delay stage. It can be a degenerate or non-degenerate optical setup. In a degenerate setup, the pump and probe pulses are identical. They usually derive from the same laser source and then a beam splitter creates two replicas. Then, the probe pulse is attenuated and sent to a delay line. This type of setup presents an intrinsic limitation since it is able to probe the Pump-Probe signal only at the excitation wavelength. To overcome this issue a non-degenerate optical setup is usually adopted: a simplified scheme is reported in Figure 5.2. The optical system is powered by a fixed-wavelength femtosecond laser (in this case a pulsed laser with $\lambda = 1030\text{ nm}$, pulse duration of 190 fs and tunable repetition rate in the range 10 - 200 kHz). The laser beam is split into two different paths, the pump path and the probe one, thanks to a beam splitter (BS). Then, the pump beam is modulated at half of the laser repetition rate by means of a Pockel cell (PC), an electro-optical device used to control the intensity of the pump beam by applying an electric

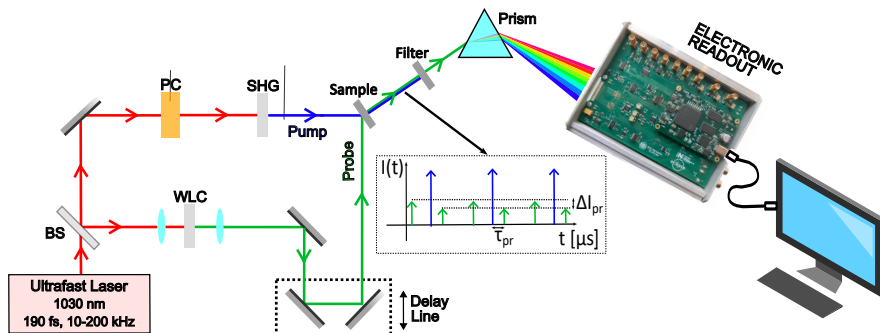


Figure 5.2: *Simplified optical setup for Pump-Probe experiments. The probe pulses are broadband thanks to a White-Light Continuum Generator (WLC) and delayed by τ_d with respect to the pump pulses. Pump beam is filtered after the sample. The pump beam is modulated at half of the laser repetition rate using a Pockels cell (PC), placed before the Second Harmonic Generator (SHG) crystal and then it is filtered after the sample. A prism spatially separates the wavelengths of the optical signal for a multichannel acquisition.*

field. After that, a second harmonic generator provides the pump pulse with the right wavelength in order to excite the sample under test. Pump wavelength is fixed at 515 nm. In parallel, the probe beam is optically broadened with a white light continuum generator (WLC) in the 1200-1750 nm range. The pump and probe pulses, synchronized by a controlled optical delay line, are focused on the sample thanks to a complex system of mirrors and lenses. After impinging on the sample, while the pump pulses are filtered out and the probe beam, instead, is spectrally dispersed with a prism over a multichannel detector.

5.4 Types of Pump-Probe Signals

In a Pump-Probe experiment, the signal ($\Delta T/T$) may arise from three different phenomena:

- Ground-State Bleaching (GSB) or Photobleaching (PB) happens when the probe pulse has the same energy (and thus wavelength) of the pump. Following the excitation of molecules (or atoms) by the pump, the number of electrons in the ground state (lower state in Figure 5.3) decreases, so the depletion of the ground-state population gives rise to the

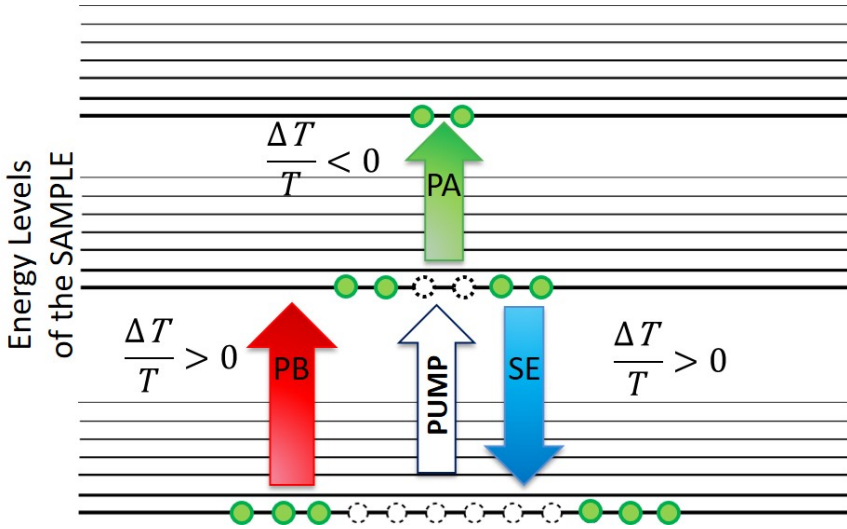


Figure 5.3: All possible pump-probe outcome of a Pump-Probe experiment represented on energy-level diagram. PB: Photobleaching, PA: Photoinduced Absorption, SE: Stimulated Emission.

reduction in absorption of the subsequent probe pulse and so to a transmission increase ($\Delta T/T > 0$).

- Photoinduced Absorption (PA) happens when the probe pulse is absorbed by electrons already excited to higher states by the pump beam, leading to a decrease of the transmission coefficient ($\Delta T/T < 0$).
- Stimulated Emission (SE): the emission of photons induced by the probe pulse from excited states populated by the pump, which effectively increases transmission ($\Delta T/T > 0$).

Figure 5.3 represents a simplified energy-levels diagram where the different situations reported above are depicted in an intuitive way.

5.5 Electronic Readout for Pump-Probe Spectroscopy

Although a large number of state-of-the-art broadband spectrometers have been developed in recent years, the design of the electronic acquisition chain has typically relied on commercial instruments or, sometimes, on solutions commissioned from external

companies.

Most instruments used for signal readout are usually commercial lock-in amplifiers, which typically provide 2 or 4 channels. As a result, no more than four wavelengths can be analyzed simultaneously, leading to long acquisition times for the complete map. To analyze multiple wavelengths simultaneously and thereby reduce the acquisition time, a multichannel system is required.

The main challenge in developing multichannel spectrometer for fast lasers arises from the large amount of data that must be sampled and averaged. Considering a digital approach, the acquisition speed must exceed the laser repetition rate, which generally restricts experimental setups to kHz-class lasers. Furthermore, implementing a fully analog, multichannel acquisition chain is not trivial.

In addition, readout electronics often could be the bottleneck of the spectrometer, limiting the performance of many systems.

To overcome all of these limitations a 40-channel custom platform, named ECLIPSE (Enhanced Lock-In amplifier for Pump-Probe Spectroscopy), has been designed, realized and tested on an optical setup.

5.5.1 Noise Sources in Pump-Probe Spectroscopy

There are several types of noise sources in a Pump-Probe Spectrometer:

- Laser Relative Intensity Noise (RIN) originates from various sources, including spontaneous emission, pump source noise, cavity vibrations, thermal fluctuations, and presents a $1/f$ behavior.
- Shot noise originates from the Poisson statistical nature of electrons and photons, as they move through a system.
- Thermal Noise originates from the random, thermal motion of electrons in the acquisition chain.
- Flicker noise originates from random fluctuations in semiconductor materials, due to defects and trapping phenomena of charge carriers in the conduction channels and close to surfaces.

5.5. Electronic Readout for Pump-Probe Spectroscopy

	[32]	[33]	[34]	[35]	[36]	ECLIPSE
Amplitude Resolution [ppm]	2.7	131	10	4	152	0.4
Acquisition time [s]	2.5	1	1	40	80	1
Broadband	✓	✓	✓	✓	✓	✓
Max Laser repetition rate f_p [MHz]	40	0.001	0.01	0.05	0.1	1
Number of channels	40	1024	12	1024	1024	40
Form Factor	comm. instrum.	custom comm. instrum.	comm. instrum.	custom comm. instrum.	comm. instrum.	custom ASIC

Table 5.1: Comparison of system performance with commercial and custom instruments.

In order to reduce the laser relative intensity noise and flicker noise, it is necessary to operate at higher laser repetition rates, adopting a lock-in approach.

Some commercial solutions operate with a repetition rate in the kHz range, and in many cases thousands of points must be averaged, requiring a few seconds per point.

Working with higher repetition rates also enables the study of dynamic phenomena in the sample. Increasing the pulse repetition frequency further reduces the time required to average N acquired samples, resulting in faster spectrum acquisition. This not only allows spectra to be obtained in shorter times, but also helps to mitigate issues related to laser beam stability during the experiment.

5.5.2 State-of-Art and Proposed Solution

In general, lasers employed in pump-probe spectroscopy can be categorized into two main classes: systems operating with relatively high pulse energies (5–100 nJ) at repetition rates of 1–5 kHz, and systems characterized by lower pulse energies (0.5–10 nJ) and repetition rates exceeding 1 MHz. Combined with suitable multichannel detection architectures, the setup can achieve a detection sensitivity on the order of $\approx 10^{-5}$ [37].

In order to distinguish sub-ppm pump-probe signal variations

from the measurement noise floor, it is necessary to average thousands of pump-on/pump-off differences. A broadband configuration, capable of simultaneously probing multiple wavelengths, further reduces the acquisition time. However, the repetition rate of typical systems is limited to tens of kilohertz, significantly increasing the total measurement time required for sufficient averaging [38].

Although multichannel analog acquisition architectures have been proposed, their implementation is often limited by bulky and expensive experimental setups, typically relying on discrete components and commercial instruments. To overcome these limitations, a custom integrated circuit (ASIC) was developed, which is the electronic core of the innovative ECLIPSE spectrometer.

A comparison between several commercial and custom instruments is reported in Table 5.1. The last column of the table highlights the key features of the developed platform with respect to the current state of the art. The following chapters provide a detailed description of the system: Chapter 6 introduces the custom integrated circuit (IC) adopted as the analog signal-processing core of the spectrometer, while Chapter 7 focuses on the design of the additional amplification stages and the digital processing chain.

Unlike the first part of this work, which focused on Raman spectroscopy, the spectrometer developed for pump-probe experiments does not rely on lock-in detection. Although lock-in detection enables signal recovery in the frequency domain, it is not the most efficient approach for this type of excitation. As demonstrated in [39], comparable signal-to-noise ratios can be achieved in significantly shorter acquisition times by employing boxcar averaging.

Pump-probe spectroscopy is typically performed using laser pulses of femtosecond or picosecond time duration at repetition rates up to 1MHz. These experimental conditions result in low-duty-cycle signals, for which lock-in detection is suboptimal for signal reconstruction.

Boxcar averaging, instead, operates in the time domain. The method consists in integrating the signal over a defined temporal window, referred to as a "gate", whose duration is optimized to match the detector response only within the region of interest.

In this way, electronic noise contributions outside the gate are effectively suppressed. In the case of a periodic train of pulses, each of these is sampled individually and then averaged with a constant weight.

CHAPTER 6

Custom Chip for Pump-Probe Spectroscopy

ECLIPSE is a custom 20-channel integrated circuit. Its purpose is to measure the incoming Pump-Probe signal and the mean power of the pulses that impinge on the sample under test (SUT). The normalized signal can then be computed through the equation:

$$\frac{\Delta I_p}{I_p}(\tau_d, \lambda) = \frac{1}{n} \sum_{k=1}^n \frac{I_{pump,off}(\tau_d, \lambda, k) - I_{pump,on}(\tau_d, \lambda, k)}{I_{pump,off}(\tau_d, \lambda, k)} \quad (6.1)$$

6.1 ASIC Features

ECLIPSE was designed by exploiting the switched capacitor technique, in order to implement a box-car integrator in a discrete-time domain. The circuit works by sampling the photo-generated charge and then integrating the difference between odd and even pulses through the switching capacitor network. The user can

select the number of subsequent integrations performed by the chip. The amplitude of the output signal is directly proportional to the number of integrations N , while the throughput is reduced by the same amount. The maximum value of N that can be selected is 1023: the achievable signal will be 1023 times higher but also 1023 times slower. By increasing this number of averages, the output signal frequency is reduced, allowing the ADC sampling frequency to be relaxed. Due to this feature, the 40 outputs of each chip can be provided to the external platform through two internal multiplexers, resulting in only two output pins.

The chip structure can thus be divided into two blocks: a digital one, which controls the phases of the switches and delivers their driving signals, and an analog one, which acquires and filters the signal coming from the photodiodes. The chip shall meet the following specifications:

- It needs to acquire the Pump-Probe signal with a repetition rate f_p in the range between 100 kHz and 1 MHz, with a superimposed modulation signal with frequency $f_m = f_p/2$.
- The ASIC must demodulate the Pump-Probe signal and integrate it from 1 to 1023 times. This must also be done for the mean power of the pulse.
- The ASIC needs to manage 20 acquisition channels in parallel and 40 outputs that should be multiplexed to two independent PADs to the external electronics.
- The maximum charge in each pulse is 2 pC ($\approx 12.5 Me^-$).
- The input noise standard deviation of the electronics must be lower than the shot noise related to the minimum charge produced by a pulse, equal to 0.02 pC ($\approx 0.125 Me^-$).

It is significant to note that the system will be able to compute the normalized Pump-Probe signal by:

$$\frac{\Delta I_p}{I_p} = \frac{\sum_{k=1}^n I_{pump,off}(\tau_d, \lambda, k) - I_{pump,on}(\tau_d, \lambda, k)}{\sum_{k=1}^n I_{pump,off}(\tau_d, \lambda, k)} \quad (6.2)$$

The equation is slightly different from (6.1), but is still a fairly valid approximation.

6.2 Analog Block Design

The primary idea behind the ASIC design is to use clock signals from the laser and the optical modulator for timing of the chip itself. Those are the signals f_p and $f_m = f_p/2$. As a matter of fact, the ASIC needs to synchronize all of its internal signals so that charge acquisition of two subsequent pulses occurs upon two different capacitors. Afterwards, the chip computes the difference between the two charges using the switched capacitor technique, and the final result is memorized in yet another capacitor. The number of averages performed by the chip depends on the required signal resolution. Pulse acquisition is synchronized at the frequency f_p , while $f_m = f_p/2$ is necessary to distinguish between odd and even pulses.

The procedure implemented by the chip to measure the input signal and generate the two output results (Pump-Probe signal and Mean Power) is depicted in Figure 6.1, referring to the circuit shown in Figure 6.2:

1. **Start-of-Conversion:** Through the SoC pin, an external signal notifies the ASIC that everything is ready for a new signal acquisition. The BUSY pin (not shown in figure) switches from low to high.
2. **Reset of the Preamplifier Feedback Capacitor:** a switch placed in parallel to the feedback capacitor of the charge preamplifier periodically resets the voltage across its terminals. The reset switching frequency is equal to the repetition rate of the pulses f_p .
3. **Preamplifier Integration:** the charge preamplifier acquires each pulse at a time and stores the resulting charge in the feedback capacitor C_{f0} .
4. **Odd-Even Difference:** a network of switches and capacitors computes the difference between the charges produced by each pump-on and pump-off pulses, integrating the resulting charge into a third capacitor. This capacitor is used as a feedback capacitor of another charge amplifier.
5. **Mean Power:** another network, which works in parallel to the aforementioned one, acquires and integrates the

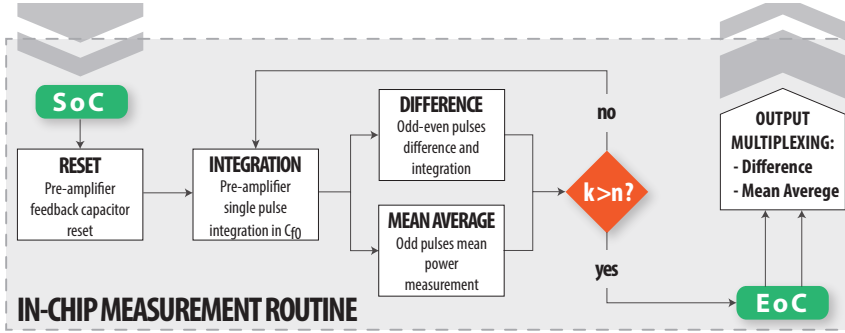


Figure 6.1: *In-Chip measurement routine flowchart*

charge produced by pump-off pulses only. This information is needed for the subsequent normalization of the Pump-Probe signal.

6. The operations listed above are repeated N times, where N is the number of averages to perform in order to get the desired resolution and is selected by the user.
7. **End of Conversion:** After the N -th iteration, the EoC pin commutes from low to high to notify the end of integration process. At the same time, the BUSY pin performs the opposite transition.
8. **Output Multiplexing:** two analog multiplexers (one for Pump-Probe and one for Mean Power signal) sequentially carry out two signals, each acquired from 20 channels simultaneously: the integration of the difference that represents the Pump-Probe signal (or AC signal) and the charge integration that represents the Mean Power (or DC signal).

As shown in Figure 6.2, the scheme of each of the 20 channels on the chip can be split up into three sub-blocks:

- charge preamplifier;
- switched capacitor subtractor network and Pump-Probe (AC) integrator;
- switched capacitor Mean Power (DC) integrator.

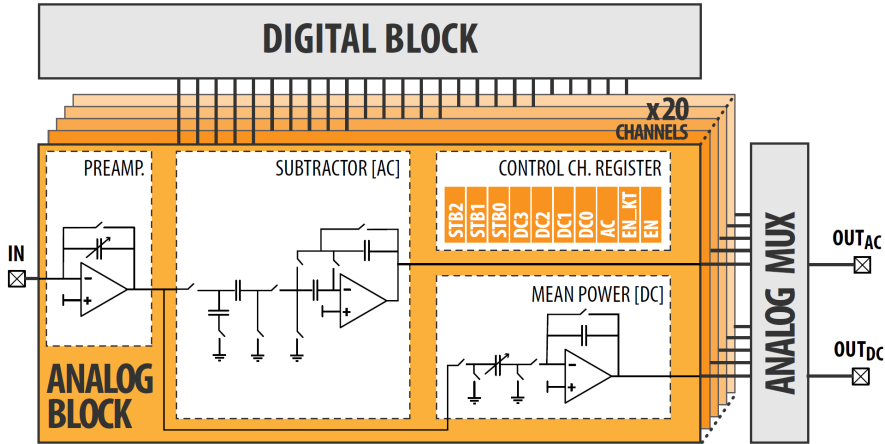


Figure 6.2: *Simplified Scheme of ASIC Architecture with detailed Channel structure*

Furthermore, each channel is provided with a 10-bit control register, also shown in Figure 6.2, which allows to set some parameters independently of other channels. In summary, it is possible to:

- vary the gain of the charge preamplifier by selecting the feedback capacitor out of two different capacitance values 2 pF and 0.2 pF through the bit "AC";
- set the gain of the DC integrator by choosing between 16 different combinations of the bits DC0, DC1, DC2 and DC3;
- change the input capacitor in parallel to the photodiode by setting the bits STB0, STB1 and STB2;
- enable or disable a channel through the bit EN;
- activate or deactivate the KTC channel for noise compensation through the bit KTC_EN.

6.2.1 Preamplifier, Subtractor and Pump-Probe Integrator Chain

To carry out the difference between two subsequent pulses in order to extract the Pump-Probe information, three steps are necessary:

- to sample the odd-position pulses (Pump OFF);

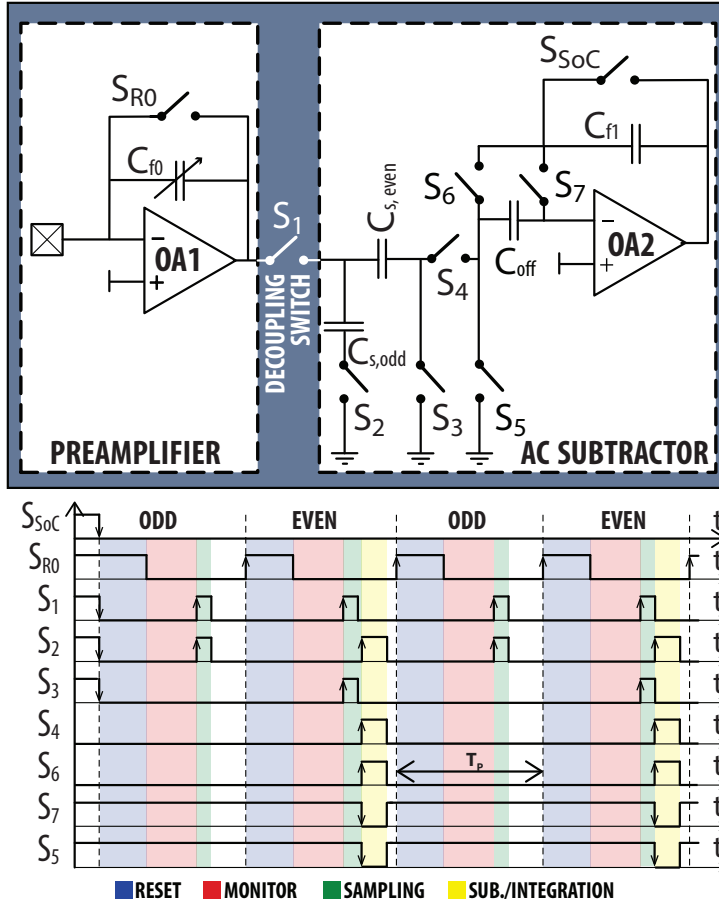


Figure 6.3: Schematic of the charge preamplifier and the AC subtractor (top), and timing diagram of the switch phases (bottom).

- to sample the even-position pulses (Pump ON);
- to compute the difference between the two and add the result to the value obtained by the previous iteration.

Figure 6.3 shows a simplified version of the charge preamplifier and of the switching capacitor network that implements the difference between two subsequent pulses. The main working phases of the circuit are also present. The output voltage value will be

computed by the following:

$$V_o = \sum_{k=1}^n \left(\frac{\Delta Q_{in}(k)}{C_{f0}} \right) \left(\frac{C_s}{2C_{f1}} \right) \quad (6.3)$$

$\Delta Q_{in}(k)$ is the charge difference between pump-off and pump-on pulses, C_{f0} the feedback capacitance of the charge preamplifier, C_{f1} the integrator capacitance of the second stage, and C_s the capacitance where the charge produced by a pulse is momentarily stored.

The various working phases can be stated as follows:

- **Reset:** the capacitor C_{f0} is discharged and thus ready to acquire a new pulse. This phase is repeated for each and every odd and even pulse.
- **Monitor:** in this phase, the chip is configured to read the charge of an odd and even pulse alternately. This charge is then stored in the feedback capacitor C_{f0} . The laser pulse has to impinge on the photodiode during this time window.
- **Sampling:** the stored charge in the feedback capacitor C_{f0} is transferred to the capacitor $C_{s,odd}$ or $C_{s,even}$, depending on whether the pulse is even or odd.
- **Subtraction and Integration:** the voltage on $C_{s,even}$ is subtracted to the one on $C_{s,odd}$. The resulting charge, given by the total voltage multiplied by the equivalent capacitance, is integrated on the feedback capacitor C_{f1} .

It should be noted that in the **Subtraction and Integration** phase, the charge of $C_{s,odd}$ is not directly transferred to the second stage amplifier and the charge of $C_{s,even}$ is then removed from the feedback capacitor C_{f1} , but the charge integrated by C_{f1} is squarely the value of the difference. This allows the circuit to avoid large range variations in charge transitions, improving system linearity.

Offset Voltage and Non-Idealities

The offset voltage of the charge preamplifier does not affect the output, as it is equal for both odd and even pulses. Therefore,

when computing the difference, the two offsets cancel out. The effect of the offset voltage of the integrator, on the contrary, can saturate the amplifier, especially in the case of high number n of averages:

$$V_{o,offset} = n \cdot V_{offset}^{OA2} \cdot \frac{C_s}{2C_{f1}} \quad (6.4)$$

For instance, for $V_{offset} = 2\text{ mV}$ and a number of averages $n = 1000$, $V_{offset} \approx 2\text{ V}$, which is higher than the 1.8 V chip power supply. In order to compensate for this effect, the integrator adopts the structure reported in Figure 6.3: the capacitor C_{off} samples the offset voltage during the Reset, Monitor and Sampling phases and then subtracts it during the Integration phase.

Another phenomenon that can degrade the instrument resolution is the dark current I_{dark} of the photodiodes. Dark currents are directly integrated by the feedback capacitor C_{f0} and their impact on the output voltage after n averages is:

$$V_{o,dark} = n \cdot \frac{I_{dark}(t_{odd} - t_{even})}{C_{f0}} \cdot \frac{C_s}{2C_{f1}} \quad (6.5)$$

where t_{odd} and t_{even} represent the time window between the Reset and the Sampling phase for the odd and even pulses, respectively. To solve this problem, it suffices to set $t_{odd} - t_{even} = 0$ and thus $t_{odd} = t_{even}$. However, considering dark currents of the order of 1 nA and a difference $t_{odd} - t_{even}$ equal to 20 ns, the resulting charge is 0.02 fC much smaller of the minimum expected charge ($\approx 0.02\text{ pC}$): hence this effect can be neglected.

Non-idealities of switches such as charge injection, signal feed-through and leakage current are lessened or outright balanced out thanks to the approach described in [40]. The detailed configuration of switches and a timing diagram are shown in Figure 6.3. The control signals of the switches follow a *break-before-make* approach in order to avoid short circuits that may cause a signal overlap.

It is worth noting that during the Monitor phase the charge preamplifier is ready to receive the signal generated by the pulse, while $C_{s,odd}$ and $C_{s,even}$ are disconnected from its output. The connection between the charge preamplifier output and these ca-

capacitors instead occurs during the Sampling phase: Monitor and Sampling are two distinct phases. As a matter of fact, while C_{f0} is reset every clock cycle, $C_{s,odd}$ and $C_{s,even}$ do not need to be reset, since they are voltage driven.

As shown in Figure 6.3, the circuit can be divided into two sub-blocks: the preamplifier and the subtractor/integrator. The first is affected by strong voltage variations due to frequent resets of the capacitor C_{f0} , which shall be recharged every clock cycle. The second, on the other hand, is a "*protected area*" where the charge on C_{f1} varies linearly with the number of integrations. Consequently, it must not be reset every clock cycle: it integrates n consecutive pulse differences. A switch called S_1 is placed between the two sub-blocks to separate them.

Noise and KTC Compensation Network

During the reset phase of the preamplifier, the closure of the reset switch, implemented through a pass-transistor structure, injects noise into the feedback capacitance, thereby degrading the achievable resolution of the chip. To partially mitigate this effect, the compensation network shown in Figure 6.4 has been implemented.

The idea is to sample the noise and subtract its fluctuations during the subtraction/integration phase, implementing a Correlated Double Sampling filter [41]. To achieve this, the sampling branch is duplicated, and two additional capacitors, $C_{k,odd}$ and $C_{k,even}$, nominally identical to C_s , are adopted. Differently from $C_{s,odd}$ and $C_{s,even}$, $C_{k,odd}$ and $C_{k,even}$ are connected to the feedback capacitor C_{f0} during the reset phase and are disconnected from the preamplifier output a few nanoseconds after the reset switch opens. In this way, the two additional capacitors sample all the noise contributions integrated in C_{f0} up to that moment, without capturing the subsequent pulsed signal. Conversely, on $C_{s,odd}$ and $C_{s,even}$, both the signal and the random fluctuations induced by the reset switch are stored. During the subtraction/integration phase, $C_{k,odd}$ and $C_{k,even}$ are connected to the virtual ground of the second stages, as $C_{s,odd}$ and $C_{s,even}$ but with opposite polarity, thereby compensating the related fluctuations.

Starting from the maximum input signal that the preamplifier is able to integrate, it is possible to compute the shot noise limit

related to that pulse. As mentioned in Section 6.1 the minimum pulse amplitude is equal to $125\text{ }ke^-$ and the resolution required is 10^{-6} times smaller. However, the unavoidable shot noise variations, given by the Poisson statistic, set the physical limit of the resolution. The shot noise standard deviation, expressed in input referred charge after n subsequent acquisitions is

$$\sigma_{shot,in} = q \cdot \sqrt{\frac{2 \cdot N_{electrons}}{n}} \quad (6.6)$$

In accordance to the simulation, the overall integrated electronic noise, given by the sum of all the KTC noise and opamps contributions has to be smaller than $\sigma_{shot,in}$.

The minimum noise of the electronics is equal to $721\text{ }e^-$ (for a feedback capacitor of 0.2 pF). This value results a little bit higher with respect to the shot noise related to minimum pulse amplitude, equal to $500\text{ }e^-$ (for a pulse amplitude of $125\text{ }ke^-$). According to theoretical calculations and simulations, the KTC network provides a beneficial effect in terms of electronic noise reduction, reducing the standard deviation to $262\text{ }e^-$. In this situation the averaging feature seems not to be necessary. Differently from the aforementioned case, for a feedback capacitor of 2 pF (and a pulse amplitude of $1.25\text{ }Me^-$), the electronic noise with KTC network is equal to $1879\text{ }e^-$ while the shot noise corresponds to $1581\text{ }e^-$: in this case the averaging process is helpful.

6.2.2 Circuit for Mean Power Measurement

The last of the three analog blocks that make up the system is the circuit designed to measure the impinging optical power of the odd pulses, in order to normalize the Pump-Probe signal. The network is shown in Figure 6.5: it is a standard switched capacitor network that implements an integrator. The output of the charge preamplifier is sampled by the capacitor C_{m1} . The sampling of the pump-off pulse occurs during the Monitor phase and is carried out every m -th clock cycle (f_m), with m chosen by the user.

The output voltage of OA3 due to the charge generated by an

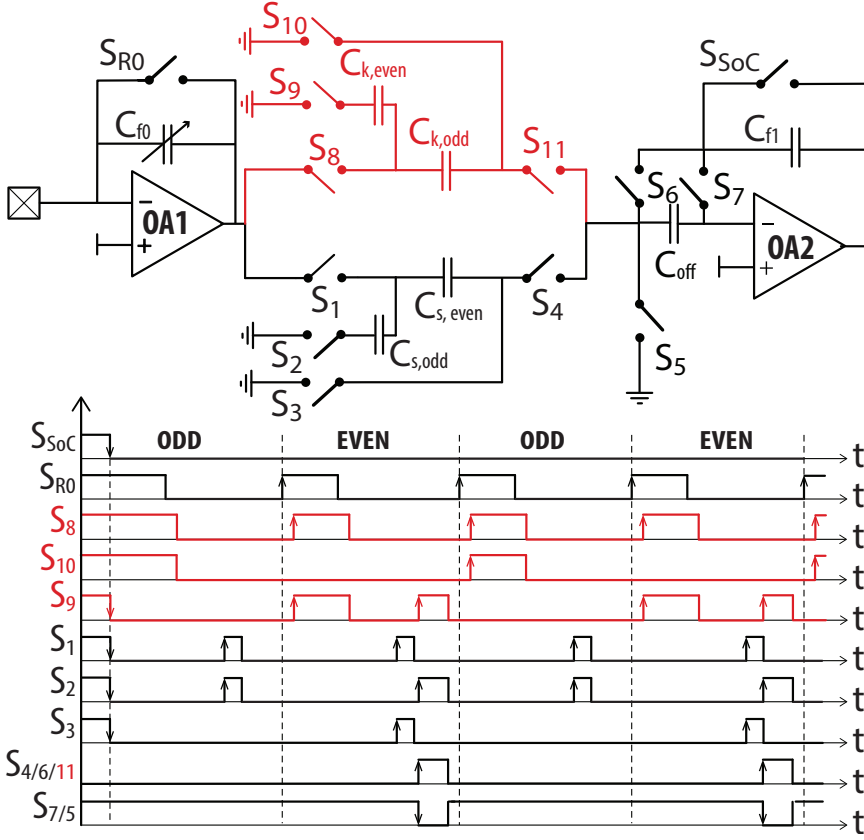


Figure 6.4: KTC Compensation Network (top) and Timing diagram (bottom).

odd pulse after n pairs of pulses is equal to:

$$V_{o,DC} = \sum_{k=1}^{n/m} \frac{Q_{in}^{odd}(k)}{C_{f0}} \cdot \frac{C_{m1}}{C_{m2}} \quad (6.7)$$

with C_{m2} equal to 2 pF and C_{m1} ranging between 50 fF and 650 fF, digitally selected by a combination of 4 bits. This block represents the last part of the acquisition chain for each of the 20 ECLIPSE channels.

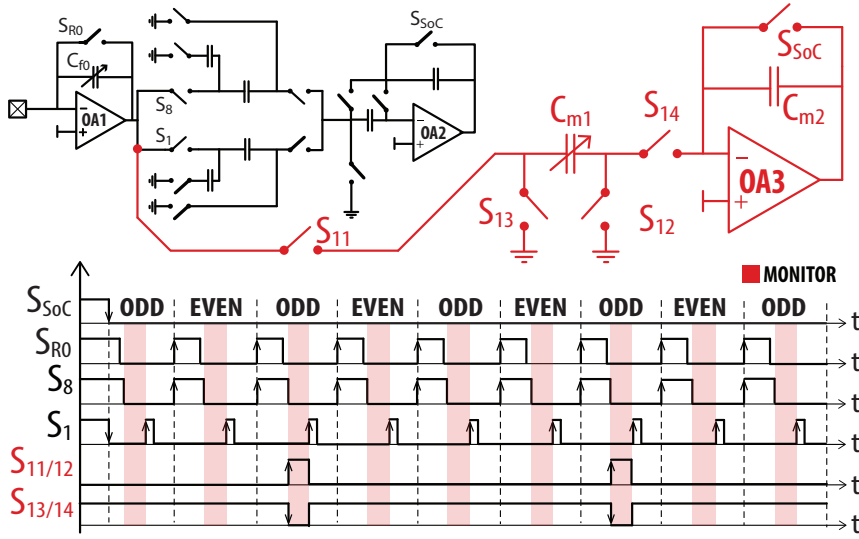


Figure 6.5: Schematic (top) and timing diagram of the switch phases (bottom) of the Mean Power Integrator.

6.2.3 Align and Test Channel

ECLIPSE is equipped with two pins in order to validate the functionality of the analog block, available only for the first channel of the chip. Those pins are useful for both circuit testing and alignment of the signals during the optical experiment, so that pulses are read by the charge preamplifier only during the right time window, the Monitor phase. The scheme of the first channel of the chip is shown in Figure 6.6.

The two I/O modules are used at the input and at the output of the charge preamplifier. The ALIGN pin is connected at the input of the amplifier through a Trans-impedance amplifier, whereas the TEST1 I/O buffers the output of the amplifier to the external PAD Test 1.

As explained thus far, the two pulses must be sampled during two subsequent Monitor phases and so it is mandatory that the internal signal of the switches and the optical signal be aligned. TO adjust the timing of signals, the I/O module between input PAD and charge preamplifier must be in *open circuit connection* mode while the connection between photodiode and ALIGN PAD is enabled: the current generated by the photodiode is read by

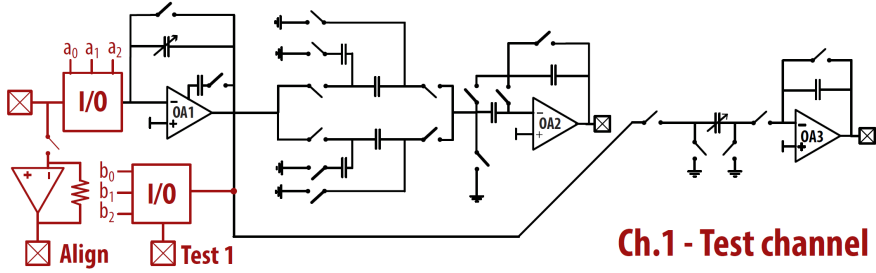


Figure 6.6: Test and Align pins of the ASIC used to access internal nodes of the chip.

a Transimpedance amplifier and, once converted into a voltage through the feedback resistor, is available to the external PAD.

6.3 Digital Block Design

Twenty-one digital signals are necessary to drive the analog block. These signals are synchronized with the laser pulses and thus have all the same frequency, while the relative phase and duty cycle are different for each signal. Control signals are generated from f_p and f_m in order to be time coherent with the optical signal. A digital block generates all the control signals which makes the ECLIPSE chip a complex mixed-signal ASIC.

6.3.1 Digital Block

A simplified scheme of the digital blocks on ECLIPSE is shown in Figure 6.7. The block generates the 21 signals that drive the switches in the analog block. The digital macro-block can be divided into the following interconnected sub-blocks:

- **General Shift Register:** a 36 bits shift register which holds the main control settings of the system, thoroughly explained in section 6.3.1.
- **Finite State Machine (FSM):** its role is to generate the 21 signals that drive the switches. Its routine is represented in Figure 6.1 and is explained in section 6.3.1.
- **20-to-4 Digital MUX:** the multiplexer allows some control signals to be carried out to 4 output pins. These control

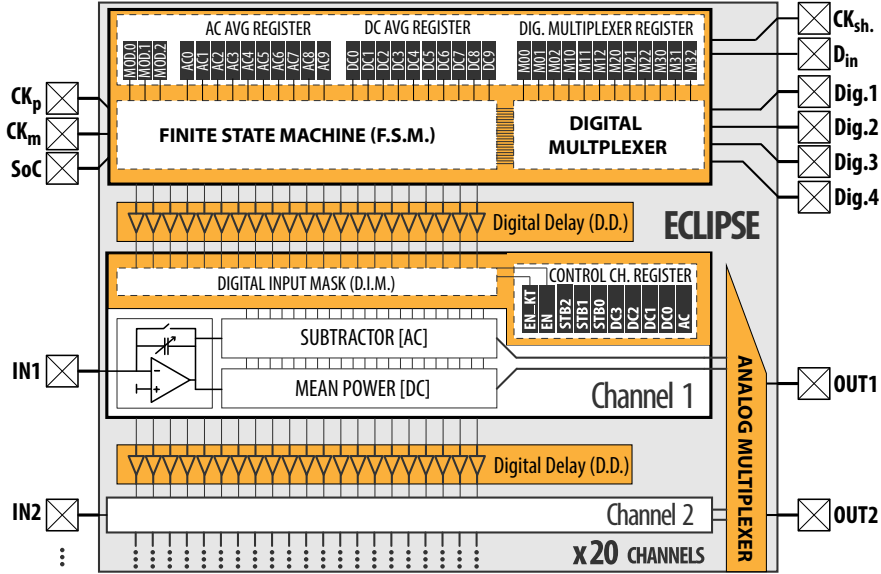


Figure 6.7: Block diagram of the digital functionalities implemented in the ASIC.

signals are the internal clocks of the chip and are useful for both testing and real-time communication between the chip and the FPGA.

- **Delay Mask:** a digital block spread out on the chip for each channel, for a total of 20 delay masks. Its aim is to restore the edges and logic levels of the control signals while delaying each channel by a little bit, in order to produce a controlled skew and avoid all channels commuting at the same time. This reduces power consumption.
- **Channel Shift Register:** a 10 bits shift register which holds the setting information of a single channel. Every channel has its own. The in-depth description of each bit is in section 6.2.
- **Digital Input Mask :** this block is used as the interface between the digital clocks and the analog circuits. It allows some control clocks to be masked if the EN and KTC_EN bits are low. In this way, the switches of unused channels will not commute.

- **20-to-1 Analog MUX:** two of these multiplexers are used in the ASIC to reduce the number of output pins from 40 to 2. Since each multiplexer acquires 20 channels sequentially, the required PINs are reduced to one: one for the Pump-Prob signal (AC pin) and one for the Mean Power (DC pin). The multiplexers can work in two modes:
 - **Asynchronous Mode:** the FPGA directly selects the channel to connect with the AC and DC PIN through 5 dials (B0, B1, B2, B3, B4).
 - **Synchronous Mode:** the FPGA uploads the information in the *Starting Register* (START_REG) and when the EoC bit switches to high, the MUX sequentially reads the signal of each channel (*Rolling Mode*), starting from the selected START_REG.

General Shift Register

The bits memorized in the *General Shift Register* are:

- **M00 - M32:** 12 bits (M00, M01, M02, M10, M11, M12, M20, M21, M22, M30, M31, M32) to select 4 out of 21 digital control signals to carry out to the output PADs of the chip (DIG1, DIG2, DIG3, DIG3). One of the most important signals is the MONITOR signal, useful for the synchronization of the ASIC with the optical setup;
- **AC0 - AC9:** 10 bits to set the number n (from 1 to 1023) of differences between odd and even pulses integrate in the feedback capacitor C_{f1} ;
- **DC0 - DC9:** 10 bits to set the number m in order to integrate in C_{m1} a number of odd pulses equal to n/m , to estimate the mean power;
- **MOD0, MOD1, MOD2:** 3 bits to configure the FSM in three different operational modes.

Finite State Machine (FSM)

The architecture of the finite state machine on the chip can be in turn divided into the following sub-blocks:

- **Control Signal Generator (CSG):** this block generates the 21 signals that drive the switches of the 20 channels, starting from the clocks of the laser and the modulator, that is, the frequencies f_p and $f_m = f_p/2$.
- **AC Synchronous Down Counter:** it is a loop counter driven by the clock at frequency $f_p/2$ that counts from n to 0, with N being the number of AC averages to compute.
- **DC Synchronous Down Counter:** similar to the aforementioned down counter, it is a loop counter driven by the clock at frequency $f_p/2$ that counts from m to 0, where m is the number of clock cycles between two samples of DC pulses, in order to sample n/m pulses.
- **Glue Logic:** it constitutes the logic that allows the listed blocks to be connected and is made up of single logic gates and Flip-Flops.

The main states of this machine are shown in Figure 6.1 and are as follows:

- **STEP 0: Reset:** the FSM Flip-Flops are reset and the clock f_p is masked since the ENABLE pin is low.
- **STEP 2: Start of Conversion:** the SoC signal is used to force the ENABLE pin of Flip-Flops to high, so that the clock f_p is not masked anymore. In this way, the *Control Signal Generator* can be driven at a frequency f_p and the two down counters (ACDC and DCDC) at a frequency $f_p/2$. The two counters decrease their output values starting from the initial value set in the *General Shift Register*.
- **Control Signal Generation:** the clock f_p drives the CSG that supplies the signals that open and close the channels switches. The control signals for Mean Power are generated every f_p clock cycle, but are masked by the DC Down Counter. In fact, it counts from m to 0 and only once 0 is reached it unmaskes the values to drive the switches S_{12} , S_{13} , S_{14} . At this point, the value of m is reset in the counter (*Circular Mode operation*). In short, the switches of the DC signal commute every m -th clock cycle at a frequency

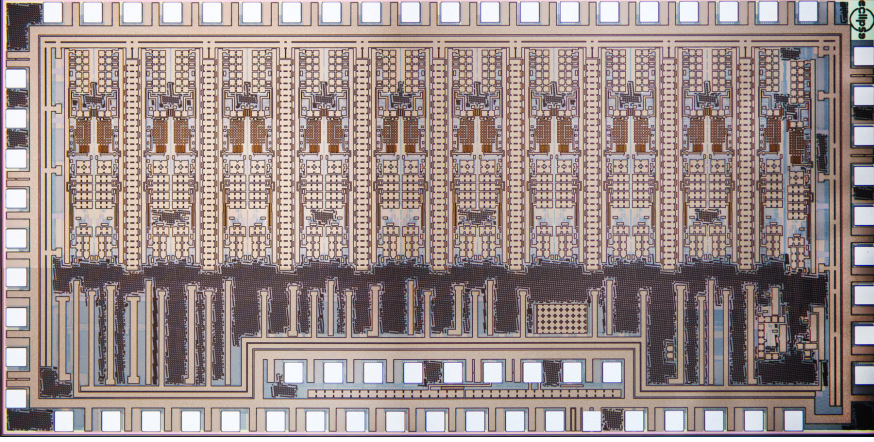


Figure 6.8: *ASIC Micrograph*

$f_p/2$, equal to the modulator frequency f_m , while all other commutations occur at frequency f_p .

- **STEP 3: End of Conversion:** after n clock cycles the AC Down Counter also reaches 0, the ENABLE pin commutes to low and the clock is masked again. The **STEP 0** condition is restored. The BUSY pin, which is high until the clock is masked, is set to low to send the end of the measurement cycle signal to the FPGA.

6.4 ASIC Layout and Power Supply

The ECLIPSE chip was manufactured by TSMC in $0.16\mu m - 1.8V$ technology. The micrograph is shown in Figure 6.8.

Each channel requires a current of about 2.5 mA, which results in a total of 50 mA for the whole chip. The total power dissipated by the chip is about 90mW at 1.8 V supply voltage.

Out of 66 pins, 16 pins are reserved for supply voltages, both digital and analog. In particular:

- 8 PADS for analog supply voltages;
- 6 PADS for digital supply voltages;
- 2 PADS for the ESD (Electro-Statical Discharge) protection circuit.

CHAPTER 7

Multichannel Platform for Pump-Probe Spectroscopy

Part of this work is reported in [42].

The ASIC described in the previous chapter has been experimentally validated with a custom printed circuit board, specifically designed for testing as a simplified prototype before designing the final Pump-Probe spectrometer.

The final ECLIPSE platform is similar to the testing board but incorporates two ECLIPSE ASICs together with the Photodiode Array, enabling the simultaneous acquisition of 40 different wavelengths. Furthermore, the microcontroller adopted in the testing board was replaced with an FPGA, whose inherently parallel architecture is particularly suited for channel processing as well as for the control of the two chips and the auxiliary external electronics.

7.1 Prototype Platform ASIC Validation

The prototype system includes the Analog to Digital Converter, the microcontroller and all the necessary sub-circuits to operate ECLIPSE as the real final instrument. It also implements a custom pulsed current generator to electronically emulate the incoming optical signal and to perform the first electrical validation by injecting a controlled charge into the virtual ground of the charge preamplifier.

The primary task of the PCB under consideration is to control and provide the appropriate signals to the 66 pads of the ASIC, which can be grouped as follows:

- 20 input pads, one for each acquisition channel;
- 2 output pads, one for the Pump-Probe (AC) signal and one for the Mean Power (DC) signal, obtained through the multiplexing of the 40 (20 AC and 20 DC) output pins of the 20 channels, which are subsequently amplified and acquired by an ADC;
- 5 pads supplying the analog reference voltages required for the correct biasing of certain internal components of the chip, such as the charge preamplifier and the integrator stages;
- 14 digital pads whose signals are either provided to or read by the microcontroller;
- 2 analog pads delivering the signals necessary for proper phase alignment at chip startup: ALIGN and TEST_1;
- 4 pads connected to the digital multiplexer selectors;
- 2 pads providing the two required clock signals: f_p and $f_m = f_p/2$;
- 17 pads dedicated to power supply.

7.1.1 Testing Board: Main Blocks

Figure 7.1 highlights all the blocks required for the acquisition and processing of the external signal and for the generation of all control signals necessary for ECLIPSE. The main blocks are:

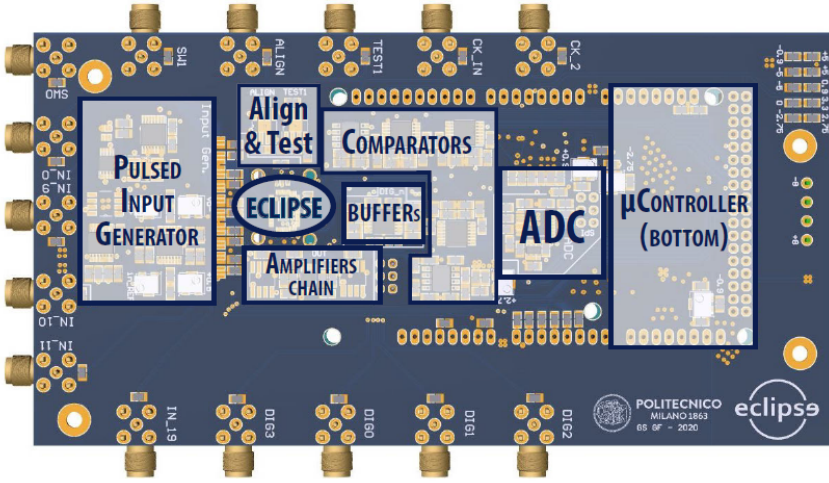


Figure 7.1: 3D Image of the testing board and constitutive blocks

- The **ECLIPSE chip**, wire-bonded directly on the PCB. Out of the 20 input channels, for testing purposes only 5 are actually connected to the rest of the board: IN_1, IN_10, IN_11, IN_12 and IN_20.
- The **signal amplification chain**, which acquires the signal at the AC and DC outputs, amplifies them and adapts the ASIC voltage range (± 0.9) to that of the ADC (0–5 V) to exploit the entire ADC dynamic range.
- The dual-channel **ADC**, ADS8330IBPW from Texas Instruments, with a sampling rate up to 1 MSample/s, used to digitize the AC and DC outputs of the chip.
- The **Arduino Due microcontroller**, responsible for managing all digital signals required for the operation of both the chip and the ADC. It also handles interfacing and communication between the board and the PC via the UART port.
- Four **analog buffers** which acquire the four outputs of the digital multiplexer and drive the SMA connectors, thereby allowing direct access to internal signals for visualization with an oscilloscope. Among these, the *Monitor* signal is

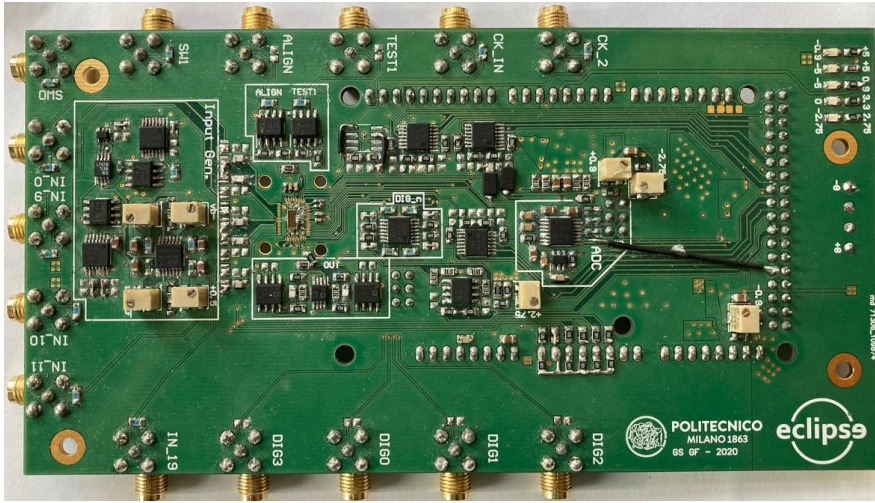


Figure 7.2: *Testing PCB developed for ECLIPSE validation. The ASIC can be seen wire-bonded on the board.*

of particular importance, as it is required for the timing alignment of the clock signals to ensure the correct operation of the finite state machine (FSM).

- **Two low-noise, wide-band amplifiers** that constitute the **Align and Test block**. They amplify the signals from the TEST_1 and ALIGN pads of ECLIPSE and drive two dedicated SMA connectors for debugging.

In addition to the aforementioned blocks, the PCB also includes several auxiliary elements which are nevertheless indispensable for the correct working of the system:

- 16 comparators used to adapt the voltage levels of the digital signals from $\pm 0.9V$ V (from the ECLIPSE output) to 0–3.3 V (microcontroller) and vice versa. They are useful also to regenerate the digital signal edges.
- Six linear regulators required to generate the supply voltages for the entire PCB. Starting from an input voltage of $\pm 8V$ provided by an external power supply, the LDO voltage regulators generate:
 - $\pm 5V$ to supply most of the operational amplifiers and $+5V$ for the ADC;

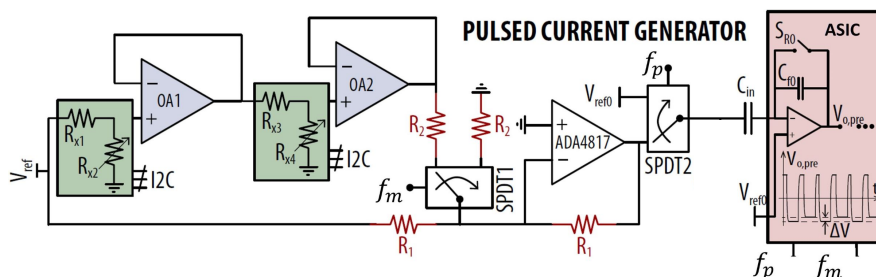


Figure 7.3: *Simplified scheme of Pulsed Input Generator circuit to emulate the behavior and output signal of the photodiode in a Pump-Probe experiment*

- 3.3 V to supply the comparators and the microcontroller;
- ± 0.9 V to power the ASIC.

Furthermore, a custom analog circuit, named **Pulsed Input Generator** and described in detail in Section 7.1.2, emulates the behavior and output signal of the photodiodes.

The PCB is a 4-layer, 15.8 cm $\times$ 8.2 cm board, which could be further reduced by replacing the Arduino Due with a smaller DSP (a different microcontroller or an FPGA).

Figure 7.2 shows the fully assembled board, manufactured by Millennium Dataware srl.

7.1.2 Pulsed Input Generator Circuit

In order to check the correct operation of the chip, the input signal to the 20 channels can be injected in two different ways:

- through the SMA connectors (IN_0, IN_9, IN_10, IN_11, IN_20) using an external function generator;
- through an on-board custom pulse generator specifically designed to emulate the behavior of the Pump-Probe signal.

In this section, the second approach is analyzed in detail, with the operating principle of the dedicated circuit shown in Figure 7.3.

The circuit generates a train of current pulses at frequency f_p (the same frequency as the main chip clock and equal to the laser repetition rate), with variable amplitude. To fully validate

the chip performance, the generator must be able to produce an odd and an even pulse, corresponding to pump-off and pump-on effect, such that the difference between the charges injected into the virtual ground of the charge preamplifier ranges from 1 ppm up to about 111 kppm with respect to the average injected charge Q_{in} . This results in a superimposed modulated signal at frequency $f_m = f_p/2$ with amplitude $\Delta Q_{in} \approx Q_{in}/10^6$. For realistic emulation, both the average injected charge Q_{in} and the charge unbalance ΔQ_{in} must be tunable. This is achieved by mean of two digital potentiometers, whose resistance value can be controlled either via hardware or software.

The reference voltage V_{ref} is generated by a precision reference IC (REF3240AIDBVT) with a temperature drift of 4 ppm/°C and a nominal voltage of 4.096 V. Using mechanical trimmers, this value can be changed. Denoting k_1 and k_2 as the partition factors of the two digital potentiometers, the output voltage at buffer OA2 is given by:

$$V_{OA2} = V_{ref} \cdot k_1 \cdot k_2 \quad (7.1)$$

Depending on the SPDT1 switch position, the inverting amplifier produces either:

$$V_{out} = -V_{ref} - \frac{R_1}{R_2} \cdot k_1 \cdot k_2 \cdot V_{ref}, \quad (7.2)$$

with $R_1/R_2 = 1/9$ or simply $-V_{ref}$ when SPDT1 is connected to GND.

Injection of current pulses into the feedback capacitor of the charge preamplifier is achieved by applying a voltage step to the capacitor C_{in} , which is connected to the virtual ground of the preamplifier, controlling the switching voltages across its terminals using SPDT2, that is driven with a square-wave at f_p . When properly phase-aligned with the Monitor phase of the chip's finite-state machine, the injected charge is:

$$Q_{in} = C_{in} \cdot (V_{ref0} - V_{ref}), \quad (7.3)$$

where V_{ref} and V_{ref0} are the low and high levels of the square wave.

To prevent the negative transition from affecting the stored

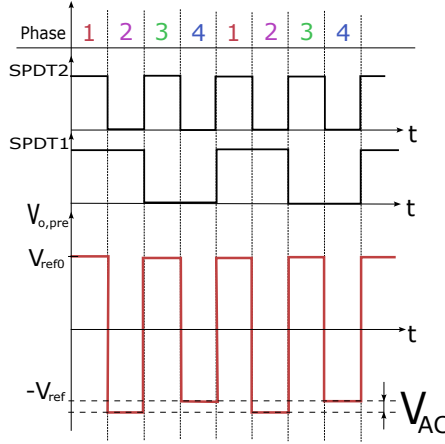


Figure 7.4: Time diagram of the pulse generator during different working phases.

charge in the feedback capacitor, the duty cycle of the SPDT2 signal must be adjusted so that the falling edge occurs during the Reset phase. In this condition, the switch S_{R0} , in parallel to C_{f0} , not only discharges the capacitor but also provides an alternative path for the signal, thus avoiding unwanted variations in the stored charge.

The SPDT1 switch, on the other hand, is used to introduce small variations between odd and even pulses. The amplitude of the signal applied to C_{in} (and thus at the input of the chip) depends on the switch position: in one case, the applied voltage is $-V_{ref}$, while in the other it is further reduced by a factor of $k_1 \cdot k_2/9$. This difference constitutes the signal of interest in Pump–Probe spectroscopy. By means of the SPDT1 signal, operating at the same frequency as $f_m = f_p/2$, pulses of different amplitude can be generated, such that odd and even pulses inject different charges into C_{f0} .

A more detailed analysis of signal generation can be carried out with the aid of the timing diagram shown in Figure 7.4, which illustrates the switching phases, and Figure 7.5, which reports the positions of SPDT1 and SPDT2 in each phase.

The voltage across C_{ch} is equal to V_{ref0} since it is connected to the virtual ground of the charge preamplifier. During phase 1 and phase 3 the voltage across C_{in} is constant, and therefore

no charge is stored in the feedback capacitor. After the voltage transition from phase 1 to phase 2 and from phase 3 to phase 4, a voltage step is applied to one terminal of C_{in} , injecting in the virtual ground a charge proportional to the amplitude of the voltage step, that is stored in feedback capacitor C_{f0} .

In phase 2, following the commutation of SPDT2, the voltage on the left terminal of C_{in} is:

$$-V_{ref} \cdot \frac{k_1 \cdot k_2}{9} - V_{ref} \quad (7.4)$$

In phase 4, following the commutation of SPDT1, the path through the buffers and digital potentiometers is disconnected from the output; under these conditions, the voltage on the left terminal of C_{in} is $-V_{ref}$.

In summary, with reference to Figure 7.3: For an odd pulse (SPDT2 = 0 and SPDT1 = 1, phase 2):

$$Q_{in,odd} = C_{in} \cdot \left[V_{ref0} - \left(V_{ref} + V_{ref} \cdot k_1 k_2 \cdot \frac{R_1}{R_2} \right) \right] \quad (7.5)$$

For an even pulse (SPDT2 = 0 and SPDT1 = 0, phase 4):

$$Q_{in,even} = C_{in} \cdot (V_{ref0} - V_{ref}) \quad (7.6)$$

The difference in injected charge ΔQ_{in} is therefore:

$$\Delta Q_{in} = C_{in} \cdot V_{ref} \cdot k_1 k_2 \cdot \frac{R_1}{R_2} \quad (7.7)$$

Since $k_1 \cdot k_2 \cdot \frac{R_1}{R_2} \ll 1$, the average injected charge can be approximated as $Q_{in} \approx Q_{in,odd} \approx Q_{in,even}$.

The Pump-Probe signal expressed in parts per million (ppm) can then be written as:

$$Pump - Probe Signal = \frac{\Delta Q_{in}}{Q_{in}} = k_1 k_2 \cdot \frac{R_1}{R_2} \cdot 10^6 \quad (7.8)$$

As observed in expression (7.8), any dependence on V_{ref} cancels out, and the signal in ppm is determined exclusively by the circuit parameters, namely the resistor ratio and the partitioning imposed by the digital potentiometers. Consequently, drifts in V_{ref} from its nominal value do not affect the measurement.

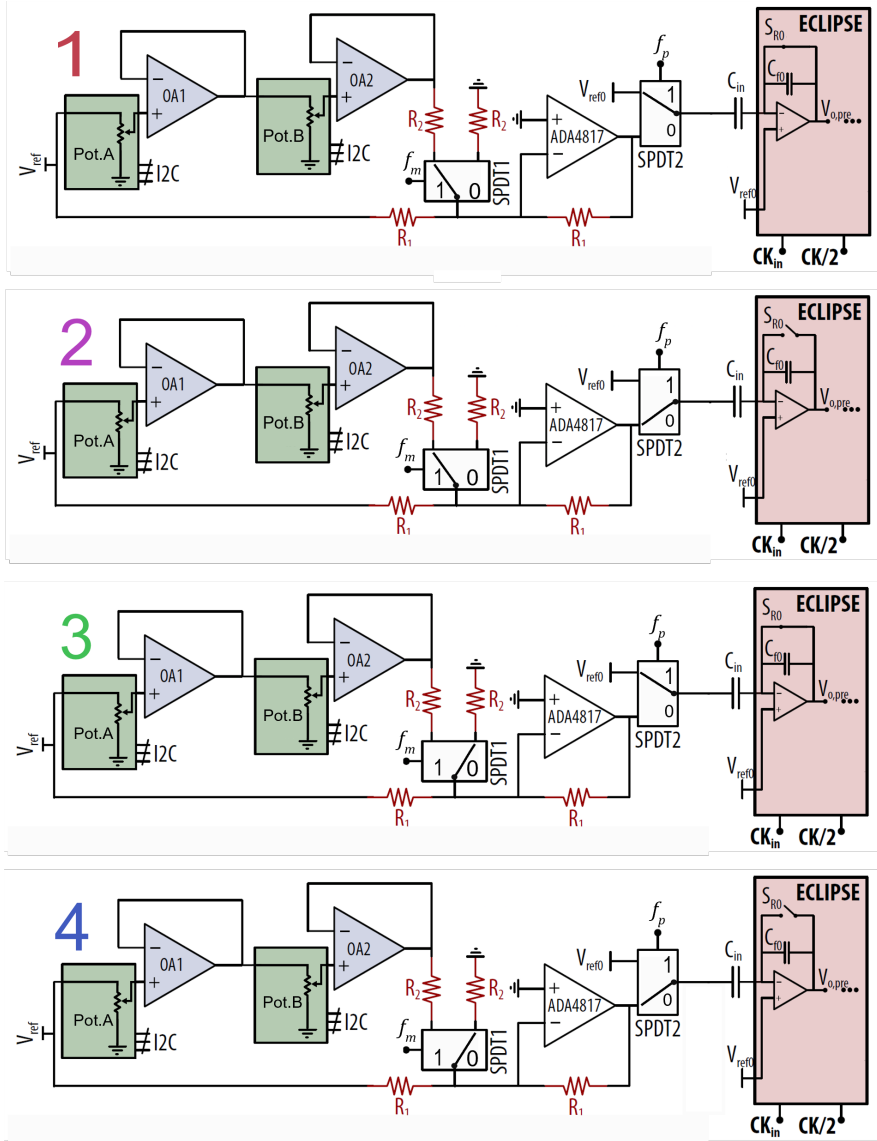


Figure 7.5: Simplified schematic showing the positions of switches SPDT1 and SPDT2 during the operating phases of the pulse generator.

Nevertheless, components with low tolerance and stable thermal characteristics must be selected to ensure optimal Pump-Probe performance.

Once the components are selected, with particular emphasis on the digital potentiometers, Equation (7.8) can be reformulated in the following equivalent form:

$$\begin{aligned} \text{Pump} - \text{Probe Signal} &= \frac{\text{Pot. } A}{256} \cdot \frac{\text{Pot. } B}{256} \cdot \frac{R_1}{R_2} \cdot 10^6 \\ &= \frac{\text{Pot. } A}{256} \cdot \frac{\text{Pot. } B}{256} \cdot \frac{1}{9} \cdot 10^6 \end{aligned} \quad (7.9)$$

where *Pot. A* and *Pot. B* represent the decimal code corresponding to the desired partition factor of the two digital potentiometers. These parameters can assume values ranging from 0 to 255, thus allowing the generation of a minimum Pump-Probe signal of approximately 1.7 ppm (for *Pot. A* = *Pot. B* = 1), and a maximum signal of approximately 111 kppm when both potentiometers are set to their maximum values.

7.1.3 Microcontroller, Firmware and User Interface

The design of the ECLIPSE validation board is completed with the integration of the microcontroller, its dedicated firmware and a graphical user interface (GUI), which enables full control of the board, visualization of the acquired data signal, and data storage. The main functionalities assigned to the Arduino Due microcontroller can be summarized as follows:

- Configuring the ADC in the desired operating mode by loading the required bits into its control register via the SPI protocol;
- Setting the values of the two digital potentiometers by sending the target partition through the I2C interface;
- Programming the control register of the ECLIPSE ASIC (see Figure 6.7 and Section 6.3.1) using the SPI bus;
- Periodically sampling and monitoring the supply voltages required by the platform;

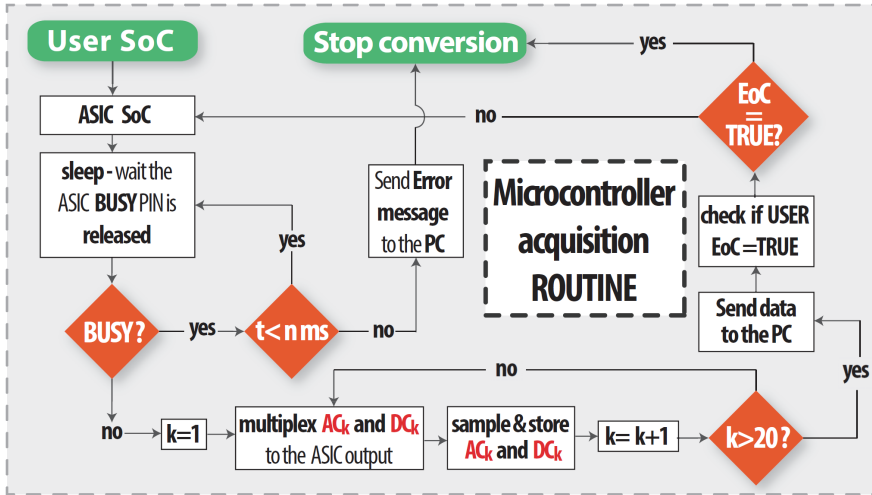


Figure 7.6: Flowchart of the acquisition routine executed by the Arduino Due microcontroller.

- Managing the acquisition routine by providing the necessary control signals to ECLIPSE and coordinating the analog-to-digital conversion performed by the ADC;
- Handling data communication and transfer to and from the PC via the USB interface.

The flowchart presented in Figure 7.6 illustrates the structure of the firmware implemented on the microcontroller.

The microcontroller initiates the acquisition process by sending a Start-of-Conversion signal to the ASIC. Upon receiving this signal, the ECLIPSE BUSY pin transitions from low to a high logic level, and the Arduino remains in a waiting state until the BUSY signal returns low. If the BUSY pin remains high for a period longer than n ms, the Arduino generates an error message, transmits it to the PC, and aborts the acquisition. Conversely, when the BUSY pin transits to low logic level, the microcontroller proceeds with the readout: the outputs of the 20 channels are sequentially multiplexed, their AC and DC components are converted by the ADC, and the resulting digital values are processed by the Arduino to prepare the data packets for transmission to the PC. Once the ADC End-of-Conversion signal transitions from low to high, the data transfer is completed and the acquisition

cycle terminates.

The acquired data are received by the PC, processed and displayed through a graphical user interface (GUI) developed in C# using the Visual Studio environment. The implemented interface allows the user to select several ASIC functionalities, and it provides the possibility of averaging multiple acquisitions by means of a moving-average filter, enabling the extraction of signals down to sub-ppm levels.

The results obtained from the electrical validation of the ASIC are reported in Section 8.1

7.2 40-channel Spectrometer: Hardware Design

After the ASIC validation thanks to the testing board described in the previous section, the electronic core of the Pump-Probe spectrometer was designed. The electronic system has to meet the following specifications:

- the ability to acquire the electric signals generated by 40 different wavelengths through 40 photodiodes;
- the capability to simultaneously process the 80 signals using two ECLIPSE ASICs (2 x 20 AC and 2 x 20 DC signals) working in parallel;
- an Analog-to-Digital conversion stage, consisting of one or more ADCs, responsible for digitizing the four output signals from the ASICs (2 AC and 2 DC);
- a programmable device (a microcontroller or an FPGA) for handling the control signals of both the ASICs and the ADCs, further processing the signal of interest and managing communication between the system and the PC.

Based on the system requirements and the functional blocks of the testing board analyzed in section 7.1, a *Top-Down* approach was adopted to define the macro-blocks into which the system can be divided:

- the **Photodiode Array (PDA)** by choosing a proper sensor able to acquire the optical signal generated by the laser and to convert it into an electrical signal.

- the **acquisition chain** which acquires and processes the signals from the PDA. This chain includes:
 - two **ECLIPSE ASICs** working in parallel. Each IC is capable of reading up to 20 signals from the PDA and providing, as output, the multiplexed signals of the 20 channels containing the Pump–Probe information (i.e., the odd–even pulse difference) and the mean optical power carried by the pulse, resulting in four output signals;
 - an off-chip **signal amplification stage**;
 - an **Analog-to-Digital conversion stage** to transfer the information from the analog to the digital domain, enabling further processing on a DSP.
- an **FPGA**, responsible for generating and managing the control signals for both the ASICs and the ADCs, and for establishing communication between the board and the PC through USB interface.
- a **power supply stage**, responsible for generating all the supply voltages required by the different components, as well as the necessary reference voltages.

7.2.1 Photodiode Array

The first step in the system design process is the selection of the most suitable sensor with respect to the system requirements. The main parameters to be considered in the choice of a PDA are:

- the number of photodiodes composing the array, which in this case must be greater than or equal to 40;
- the pitch between two adjacent photodiodes, as it determines the amount of optical power lost (i.e., not collected by any photodiode);
- the parasitic capacitance of each element of the array, which must not exceed 2 pF in order to avoid degradation of the ASIC charge preamplifier performance;

- the *radiance responsivity* (or photosensitivity) in the wavelength range of interest;
- a low dark current value.

Finding a commercially available device that satisfies all these requirements is not straightforward, since an increase in the number of photodiodes in the array is generally accompanied by a proportional increase in diode capacitance C_d .

The best compromise between system requirements (particularly in terms of the number of detectors and their capacitance) is achieved with the **G8909-01** photodiode array (Figure 7.7, bottom), a device manufactured by Hamamatsu and consisting of 40 InGaAs common-cathode photodiodes. According to the datasheet, the pitch of the photodiode is $250\text{ }\mu\text{m}$, and when biased with a few volts in reverse, the capacitance is in the order of 1 pF, as shown in Figure 7.7 (top left) [43].

As illustrated in Figure 7.7 (top right), the only drawback of this device is that its photosensitivity is limited to the near-infrared region. Although many Pump-Probe experiments are indeed performed with infrared lasers, it is more common to find spectrometers operating in the visible range.

7.2.2 Acquisition Chain

Once the optical signal has been converted into an electrical signal by the photodiode array, it requires further electronic processing in order to extract the information of interest. The signal processing chain follows these steps:

1. The charge is collected and converted into voltage by the ASIC charge preamplifier. Subsequently, the two parallel internal paths of the chip provide at the output both the Pump-Probe signal (i.e., the difference between pump-off and pump-on pulses) and the mean pulse power signal. This functional block has been extensively discussed in Chapter 6.
2. The output signal of the chip lies within the $0 - 1.8\text{V}$ range; therefore, it must be amplified to fully exploit the dynamic range of the subsequent stage. A dedicated amplification

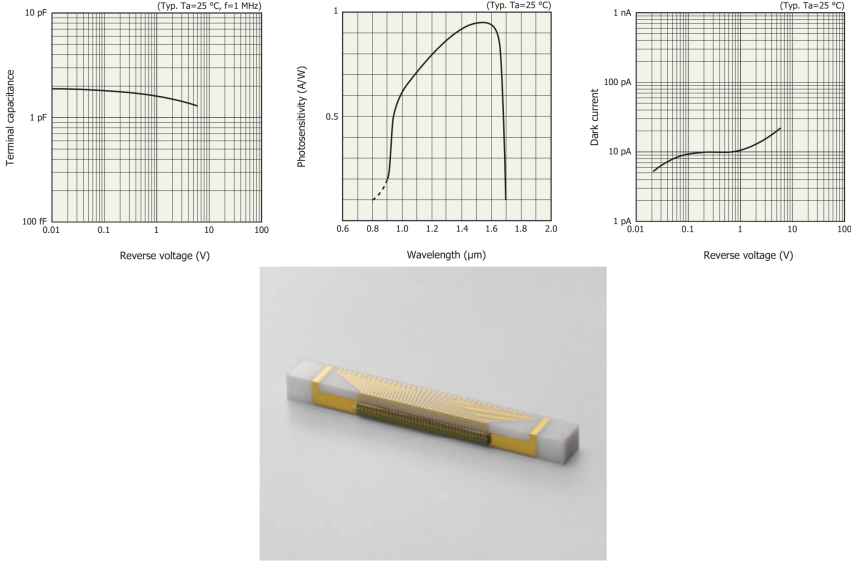


Figure 7.7: PDA capacitance (top left); PDA Photosensitivity as function of the wavelength (top middle); Dark current (top right); Photodiode Array G8909-01 (bottom) [43]

stage for the four signals (two AC and two DC) has been implemented on the PCB.

- After amplification, the signal spans a voltage range of $0 - 5\text{ V}$, matching the input range of the Analog-to-Digital Converter (ADC), which converts each input voltage into its corresponding binary code.
- The digital signals produced by the ADC conversion are further post-processed and transmitted to the PC via an FPGA, which is also responsible for handling the control and command signals of the two ECLIPSE ASICs and the ADCs.

Signal Amplification Path

The ASIC voltages V_{AC} and V_{DC} span the range of $0 - 1.8\text{ V}$. To fully exploit the dynamic range of the adopted analog-to-digital converter, an amplification stage is required at the ASIC outputs. According to the ASIC structure, the output voltages of the single

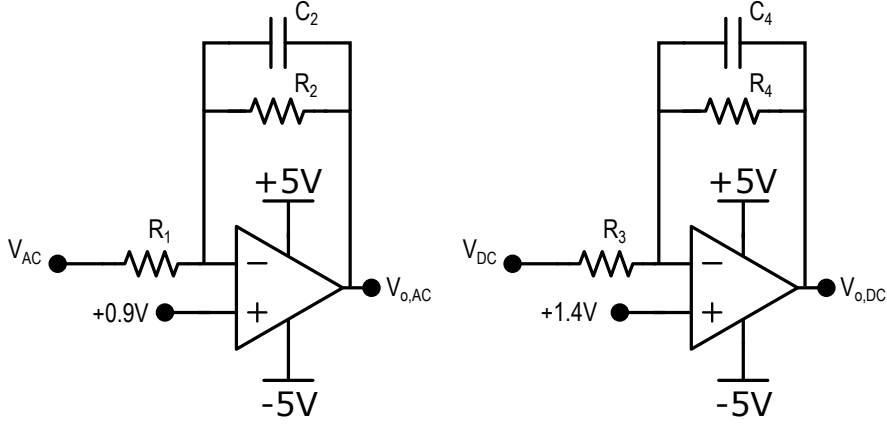


Figure 7.8: Off-Chip amplification stages for Pump-Probe (AC) and Mean Power (DC) paths to cover the entire ADC voltage range

chip, V_{AC} and V_{DC} , are given by:

$$V_{AC} = V_{reset3} \pm V_{diff} = 0.9V \pm V_{pp} \quad (7.10)$$

$$V_{DC} = V_{reset2} - V_{mean} = 1.4V - V_{mean} \quad (7.11)$$

where V_{pp} and V_{mean} represent, respectively, the voltage at the input of the AC integrator and DC integrator. To maximize the dynamic range of the signal, two amplifiers are used for each ECLIPSE ASIC, one for the AC signal and one for the DC signal, in the configuration shown in Figure 7.8.

At the AC amplifier output, the pump-probe signal is equal to:

$$\begin{aligned} V_{OAC} &= V_{AC} \cdot \left(-\frac{R_2}{R_1} \right) + 0.9V \cdot \left(1 + \frac{R_2}{R_1} \right) \\ &= (0.9V \pm V_{pp}) \left(-\frac{R_2}{R_1} \right) + 0.9V \cdot \left(1 + \frac{R_2}{R_1} \right) \quad (7.12) \\ &= 0.9V \pm V_{pp} \cdot \left(-\frac{R_2}{R_1} \right) \end{aligned}$$

while at the DC amplifier output, the mean power signal is equal

Component Name	Value
R_1	18k Ω
R_2	82k Ω
R_3	10k Ω
R_4	20k Ω
C_2, C_4	1pF

Table 7.1: *Component values referred to Figure 7.8.*

to:

$$\begin{aligned}
 V_{ODC} &= V_{DC} \cdot \left(-\frac{R_4}{R_3} \right) + 1.4V \cdot \left(1 + \frac{R_4}{R_3} \right) \\
 &= (1.4V - V_{mean}) \left(-\frac{R_4}{R_3} \right) + 1.4V \cdot \left(1 + \frac{R_4}{R_3} \right) \quad (7.13) \\
 &= 1.4V + V_{mean} \cdot \left(\frac{R_4}{R_3} \right)
 \end{aligned}$$

Given the ADC voltage range (0–5V), it is possible to determine the appropriate gain value for the two amplification stages. The resistor values are reported in Table 7.1, providing a gain of 4.55 for the Pump-Probe signal path and 2 for the mean power path.

The adopted Operational Amplifiers are ADA4807-2 by Analog Devices. These amplifiers combine low power, low-noise (3.1 nV/ $\sqrt{Hz}$) and high speed to provide an attractive solution for high-resolution data acquisition instrumentation. With a bandwidth of 180 MHz and a maximum frequency signal repetition rate of 500 kHz, an additional pole to further reduce the noise is beneficial to the system. For this purpose, C_2 and C_4 capacitors are placed in parallel to the feedback resistors, adding a pole in the transfer function. Concerning the Pump-Probe signal path, the pole is equal to $\frac{1}{2\pi C_2 R_2} \approx 2 MHz$ and the off-chip

power spectral density at the OpAmp output corresponds to:

$$S_V(f) = 4kTR_1 \cdot \left(\frac{R_2}{R_1}\right)^2 + e_{OA}^2 \cdot \left(1 + \frac{R_2}{R_1}\right)^2 + i_{OA}^2 \cdot R_2^2 + 4kTR_2 \approx (80nV/\sqrt{Hz})^2 \quad (7.14)$$

where e_{OA}^2 and i_{OA}^2 represent the OpAmp input referred voltage and current noise spectral densities. Given 2 MHz bandwidth the off-chip electronic noise results equal to $\sqrt{S_V(f) \cdot BW} \approx 113\mu V$ while in the best case, the noise related to the ASIC corresponds to $1879 e^-$ (as mentioned in Section 6.2.1) that over a $2 pF$ capacitor (the value of the preamplifier feedback capacitor) corresponds to $150\mu V$. Now it is worth to notice that the off-chip electronics does not limit the spectrometer performance.

Analog-to-Digital Conversion

Once the four analog output signals of the two ECLIPSE chips (Pump-probe and mean power outputs) have been amplified and their voltage range adapted to the right interval, they must be digitized in order to be transmitted to the PC. This task is performed by the Analog-to-Digital Converter (ADC).

The choice of the most suitable ADC for the system requires consideration of three main parameters:

- the number of bits required to achieve the desired resolution;
- the conversion time;
- the number of input channels available on the converter (ideally four in this case).

To achieve a resolution of 1 ppm, i.e. 10^{-6} , the number of bits required is:

$$N_{bit} = \log_2(10^6)$$

which corresponds to an ADC with at least 20 bits.

For what concerns the sampling frequency, considering that the maximum operating frequency of the platform limits the maximum laser repetition rate to $f_p = 1MHz$, and that every two laser pulses the output provides 40 Pump-Probe signals and 40

average power signals, the required sampling rate is:

$$\begin{aligned}
 f_s &> 2 \cdot f_p \cdot 80 \frac{\text{samples}}{2 \text{ pulses}} \\
 &= 2 \cdot 10^6 \text{ Hz} \cdot 80 \frac{\text{samples}}{2 \text{ pulses}} \\
 &= 80 \text{ MSamples/s.}
 \end{aligned} \tag{7.15}$$

To avoid the need for an additional Sample&Hold stage between the amplification and conversion blocks, and thus achieve real-time conversion, the conversion time of the ADC must be shorter than the signal arrival rate.

From the above analysis, an ADC with a sampling rate of 80 *MSps* and a resolution of 20 bits would be required. However, these specifications can be relaxed by increasing the number of hardware and software averages. Thanks to the possibility of averaging N samples at the hardware level (as described in Chapter 6), the interval between two output signals extends from $2 \mu\text{s}$ to $2 \cdot N \mu\text{s}$. For example, averaging 1000 samples results in output signals (AC and DC) being available every 2 ms , thereby relaxing the sampling rate requirement of the ADC by a factor of 10^3 . Signal resolution can be further improved by firmware averaging, as discussed in Section 7.3.2.

The component selected is the AD7902 from Analog Devices, whose block diagram is shown in Figure 7.9. It is a dual 16-bit, successive approximation, analog-to-digital converter, based on a charge redistribution DAC. It contains two low power, high speed, 16-bit sampling ADCs and a versatile serial port interface (SPI).

The platform is equipped with a Dual-ADC (AD7902) for each ASIC, so that both the pump-probe output and the mean power signal have dedicated acquisition paths.

Given the characteristics of the selected ADC, the minimum number of hardware averages required to achieve real-time conversion without an external Sample& Hold circuit can be determined. With a laser repetition rate of 1 MHz and 20 hardware averages per ASIC channel, the ADC reaches its maximum achievable sampling throughput.

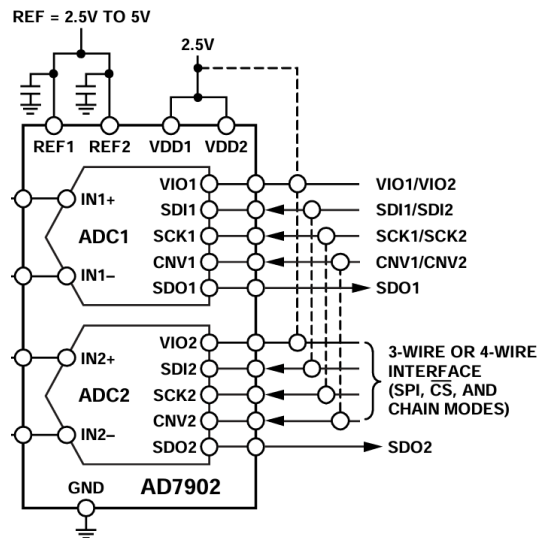


Figure 7.9: *AD7902 simplified scheme*

Another block, not directly part of the acquisition chain but fundamental for the correct operation of the system, is the synchronization management unit, which coordinates the timing signals between the chips, the laser, and the off-chip electronics. This block is the same adopted for the Raman platform and described in detail in Section 3.4.3.

7.2.3 Power Supply and Reference Voltages

In order to ensure proper communication between the blocks listed above, all signals must fall within the appropriate voltage ranges without damage any circuit section. Specifically, to adapt the 1.8V output signals of the ASICs to the 3.3V logic required by the ADC, a feature of the FPGA was exploited: each I/O port can be individually configured to operate at a specified voltage standard. The Opal Kelly module provides the I/O resources divided into three banks: two of these were configured to operate at the conventional 3.3V, while the bank interfacing directly with the ECLIPSE chips was set to 1.8V.

Supply Voltages

The system was designed to be powered by a dual supply voltage of $\pm 8\text{ V}$ provided by a laboratory power supply. The main voltages required to supply the various ICs on the board are as follows:

- $\pm 5\text{ V}$: supply voltage for most of the operational amplifiers and for the Analog-to-Digital Converter (ADC);
- 3.3 V : the standard logic level generated directly by an LDO on the Opal Kelly FPGA board, used to power the comparators and as a reference for the level shifters;
- 1.8 V : supply voltage for the two ECLIPSE ASICs, also used as supply and reference voltage for comparators and level shifters.

The $\pm 5\text{ V}$ voltages are generated from the PCB supply rails through two fixed voltage regulators: an *LM7805* for the $+5\text{ V}$ line and an *LM7905* for its dual -5 V counterpart.

The 1.8 V supply, dedicated to the two ECLIPSE ASICs and the associated support electronics, is provided by the ADP151WAUJZ-1.8 from Analog Devices. The ADP151 is an ultralow-noise, low-dropout linear regulator, characterized by an output noise of $9\mu\text{V}_{rms}$ and a PSRR of 70 dB , as specified in the datasheet. The decision to power the ASIC with a single supply voltage ($0\text{--}1.8\text{ V}$) rather than with a dual supply ($\pm 0.9\text{ V}$), as adopted in the validation board, was motivated by several factors:

- the wider availability of 1.8 V low-dropout regulators (LDOs) that meet the required performance specifications;
- the presence of a single power-on transient, instead of two (one for the positive rail and one for the negative rail), which avoids the risk of device damage due to non-simultaneous transients.

In order to quickly check the correct operation of the three supply rails, the board is equipped with three LEDs, whose illumination indicates the presence of the corresponding voltage.

Reference Voltages

The power supply section also includes the generation of the reference voltages required by the two ECLIPSE ASICs. The necessary reference voltages are:

V_{reset1} , V_{reset2} , and V_{reset3} : the three reference voltages associated with the amplifiers embedded in each ECLIPSE chip, connected to the non-inverting input of the charge preamplifier, the integrator for the DC signal, and the integrator for the AC signal, respectively;

V_{b+} and V_{b-} : the bias voltages that set the current generators of the delay mask, as described in Section 6.3;

0.9 V : the mid-point reference voltage within the 0–1.8 V dynamic range, required both by the ASIC and by the comparators used as level shifters.

Starting from the 5 V rail, the reference voltages V_{reset1} , V_{reset2} , V_{reset3} , V_{b+} , and V_{b-} are generated by means of a series voltage reference REF3240AIDBVT. This IC provides a 4.096 V output with a temperature sensitivity of only 4 ppm/°C. The device also includes an ENABLE pin, which is connected to an RC network that delays activation according to the network time constant. In this design, the chosen values $R = 150\text{ k}\Omega$ and $C = 220\text{ nF}$ result in a startup delay of approximately 5 ms. This delay is crucial to prevent damage to the ECLIPSE ASICs, ensuring that the reference voltages are applied only after the supply rails have stabilized and the chips are fully powered up.

Once the reference voltage is generated, fine regulation is achieved by means of digital potentiometers, enabling precise adjustment to the required values. Since these voltages are used as references for sensitive analog stages, they must exhibit minimal noise. To this end, the circuit shown in Figure 7.10 (left) was implemented. Its transfer function is:

$$\frac{V_{out}}{V_{in}} = \frac{1 + sC_1(R_1 + R_2)}{1 + sC_1(R_1 + R_2) + s^2C_1C_2R_1R_2} \quad (7.16)$$

with $C_1 = C_2 = 10\text{ }\mu\text{F}$, $R_1 = 10\text{ k}\Omega$, and $R_2 = 1\text{ k}\Omega$.

This stage acts as a buffer and simultaneously provides low-pass filtering with a cutoff frequency of 16 Hz, as illustrated by the Bode plot in Figure 7.10 (right). Compared with a conven-

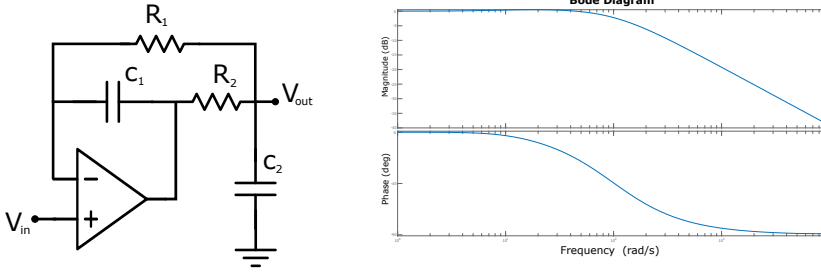


Figure 7.10: *Improved Buffer with low-pass filter (left). Bode plot of the buffer.*

tional buffer followed by a passive RC filter, this configuration offers several advantages: it eliminates the voltage drop across the resistor (since it lies within the feedback loop), and unlike a simple output capacitor, it preserves the stability of the operational amplifier.

For the generation of V_{reset3} (the 0.9 V reference), a low-power voltage reference ISL21080DIH309Z-TK from Renesas was adopted. As in the previous case, the reference is filtered by the buffer stage in Figure 7.10 before being supplied to the ASICs. Since this 0.9 V reference is also shared with other functional blocks, an additional passive low-pass filter is placed at the buffer output.

7.2.4 PCB overview

The printed circuit board (PCB) was designed using Altium Designer software, which enabled the development of the schematics and the layout, as shown in Figure 7.11.

A four-layer PCB architecture was adopted, with each layer serving a dedicated function:

- **Top Layer:** hosting the two ECLIPSE ASICs and the majority of the integrated circuits required for the proper operation of the system.
- **Ground Plane:** a continuous ground plane, providing a stable GND reference across the entire board.
- **Power Layer:** partitioned into multiple regions to distribute the supply voltages through plane areas rather than

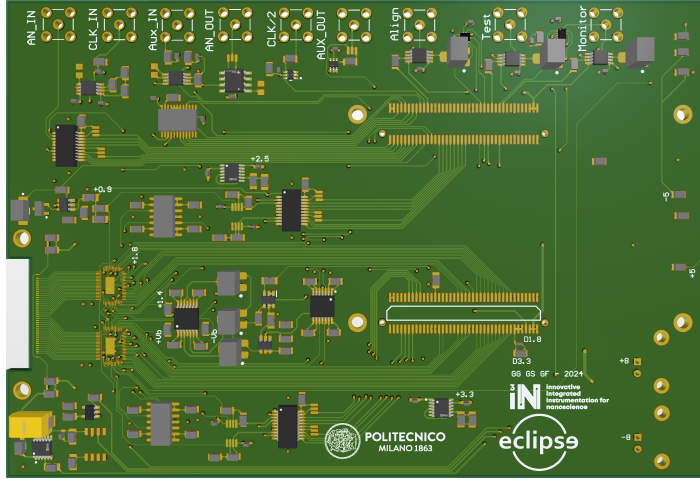


Figure 7.11: *3D model of the Spectrometer PCB*

traces, since planes exhibit a lower impedance due to their larger surface area. The power plane includes $\pm 5V$, $1.8V$, $0.9V$ and different voltage references useful for the platform.

- **Bottom Layer:** hosting the components responsible for generating both the supply and reference voltages.

The PCB was fabricated and assembled by Millennium Dataware Srl. The printed circuit board has dimensions of $150\text{ mm} \times 110\text{ mm}$. Both the two ASICs and the photodiode array are bonded onto the board. The final outcome is shown in Figure 7.12.

Lastly, as shown in Figures 7.11 AND 7.12, the PCB features the following elements:

- 2 BNC connectors designed for providing a dual voltage of $\pm 8V$ from a laboratory power supply;
- 9 SMA connectors, whose function is synchronizing the platform with the optical setup (laser and optical modulator);
- a Type C-USB connector for interfacing the FPGA with the PC;
- the slot housing the 40-element photodiode.

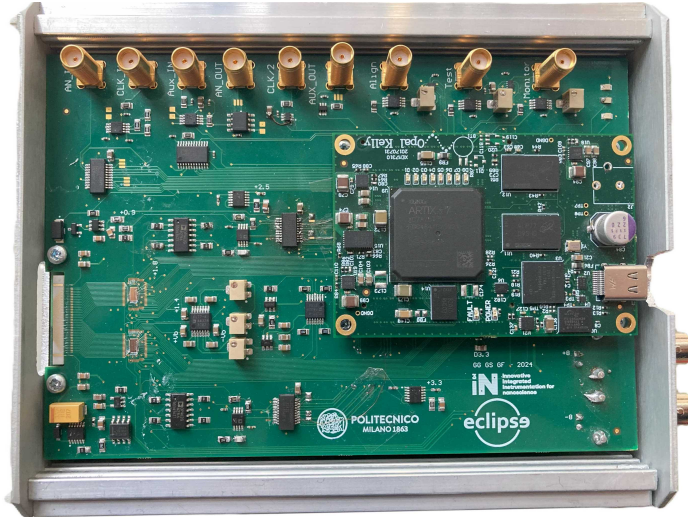


Figure 7.12: *Electronic Platform*

7.3 40-channel Spectrometer: Firmware Design

To enable communication between the hardware, specifically the ASICs, and the host PC, a dedicated digital device is required to manage the data exchange through the USB interface. Unlike the prototype designed for ASIC validation, the final system must operate with two chips working in parallel, each handling 20 channels. In addition, several auxiliary control signals are necessary for the management of the surrounding electronics. For this purpose, the Arduino Due microcontroller adopted during the initial validation stage was replaced by the Opal Kelly XEM7310-A75 module that hosts a Xilinx Artix-7 FPGA.

The firmware, developed in VHDL, must perform several functions:

- load the 256 configuration bits into the chips shift register during configuration;
- provide the necessary control signals to synchronize the laser, the optical modulator, the chips (including their internal multiplexers) and the ADCs;
- manage the delay between the laser clock and the platform clock so that optical pulses fall within the correct temporal

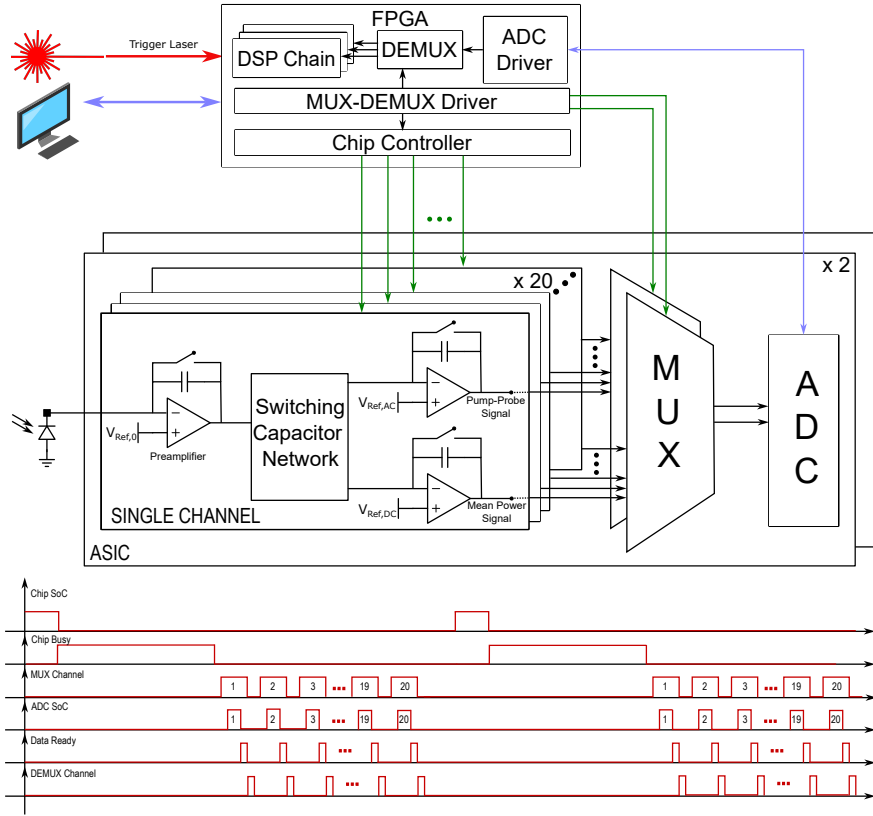


Figure 7.13: Platform simplified block diagram and acquisition routine timing diagram. Platform Components: 2 x 20-Channel ASICs, 2 x Dual, 16-bit ADCs, FPGA (top). Acquisition routine with the main control signals timing diagram (bottom).

window during the acquisition routine;

- implement a post-processing chain to further process/average the data output from the chips;
- compensate for the offsets of the 80 traces caused by mismatches among the various chip channels.

7.3.1 Platform Acquisition Routine and Synchronization

The adoption of an FPGA is primarily motivated by the need to synchronize the entire acquisition platform. For this purpose, several dedicated VHDL code blocks were developed. The laser

trigger signal is acquired by the FPGA and used as the master clock reference to ensure synchronization across all system components. The acquisition routine is illustrated in the timing diagram shown in Figure 7.13 (bottom).

The firmware generates the Start of Conversion (SoC) signal for the two ASICs, which operate in parallel. After receiving this command, each chip asserts its Busy signal, transitioning from a low to a high logic level for the entire duration of the averaging process. Once the acquisition and averaging routine is completed, the Busy signal returns to the low state, and this transition is detected by the FPGA.

When the chip operation routine is completed, the FPGA sends the channel-selection command to the multiplexers, which then carry the Pump–Probe and mean power signals to the output PADs. After selecting the first channel and accounting for the propagation delay, the Start of Conversion (SoC) signal is asserted to trigger the ADC conversion. Once the 16-bit digital data resulting from the ADC conversion are available, the Data Ready signal (internal to the FPGA) switches from low to high.

Then, a digital demultiplexer (DEMUX) selects the corresponding digital post-processing chain, where the data are further averaged and filtered to improve signal quality. This process is repeated sequentially for all 20 channels of the ASIC, ensuring consistent synchronization and timing accuracy across the entire acquisition cycle. Two DEMUXs working in parallel are placed in the firmware block design, one for each ASIC.

Finally, the processed data are transmitted to the PC, where they are displayed in real time and stored for subsequent analysis.

7.3.2 Digital Signal Post-Processing Chain

To further improve the spectrometer resolution and achieve a precision of a few parts per million (ppm), additional averaging of the output signal from the chip is required. For this purpose, a dedicated IP core was developed inside the FPGA, whose schematic is shown in Figure 7.14.

At the demultiplexer output, 20 instances of the developed IP were instantiated. Each IP consists of four Gated Integrators (GIs): two dedicated to the Pump–Probe signals of the i -th

channel from the two chips, and the other two used for the corresponding mean power signals.

The structure of each Gated Integrator is similar to the one described in Section 3.5.1. It can perform a variable number of averages, from 1 up to 1024, which can be selected by the user depending on the desired resolution and acquisition speed.

In addition to the integrator, an offset compensator has been implemented. This block samples the signal level in the absence of light for each channel and subtracts this value from the incoming signal. In this way, all channels have a zero-level output when no light is detected, minimizing systematic offsets.

Finally, through a multiplexer, the averaged signals are stored in a FIFO memory before being transmitted to the PC for display and data storage.

The acquired data are transmitted to the PC, where they are visualized by a Graphical User Interface developed in C# within the Visual Studio environment that allow to the user to selected the desired ASIC functionalities through various check boxes and dialog boxes.

CHAPTER 8

Spectrometer Validation and Results

This chapter reports the results achieved for the electrical and optical validation of the developed electronic spectrometer.

The first validation focused on the ASIC: using a current pulse generator emulating the optical setup, the transfer function between input and output signals was characterized. The ASIC was then evaluated in terms of noise performance, and the complete platform was validated electronically to determine the minimum detectable signal.

In collaboration with the Department of Physics, after verifying the system performance under shot-noise-limited conditions, the multichannel spectrometer was used to acquire the pump-probe signal of a graphene-based FET.

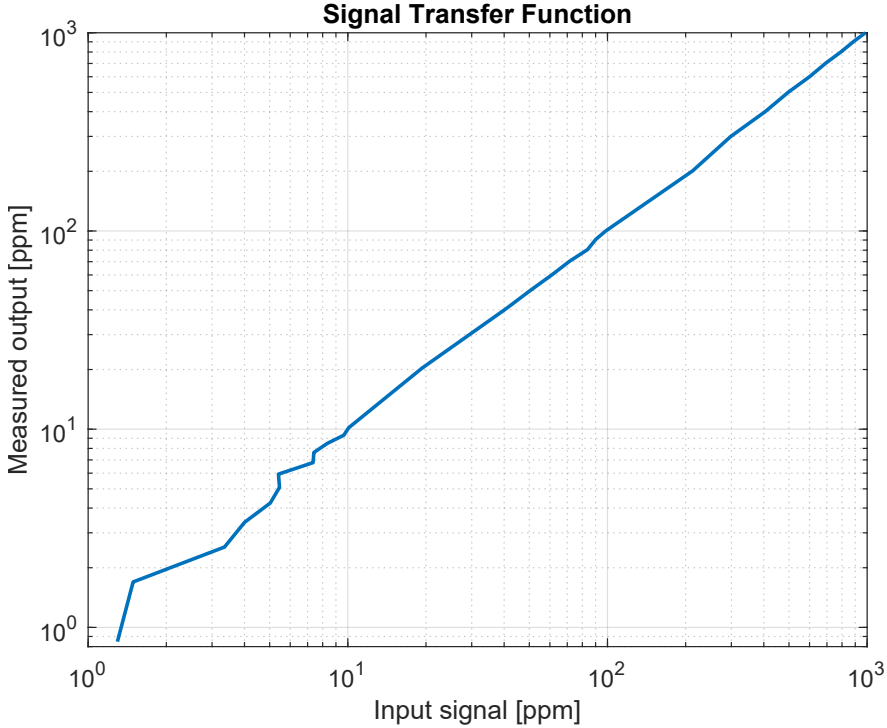


Figure 8.1: *Measured signal $\Delta T/T$ as a function of the input amplitude with 1MHz repetition rate and mean charge of 2pC.*

8.1 Electrical Performance

Using the current pulse generator that emulates the optical setup, described in Section 7.1.2, we validated the ASIC transfer function of the test channel.

After performing multiple measurements varying the difference between the reference and the pump-probe pulses, we obtained the plot shown in Figure 8.1. The measured output signal is represented in part per million relative to the mean injected reference signal. Each point has been collected with 1023 averages on-chip and thousands of software averages. In addition to the evident linearity between input and output signal, it is worth to notice that, without changing the number of averages ($n = 1023$), the ASIC is able to measure from less than 1.7 ppm to 1000 ppm, leading to 60dB of dynamic range.

After the ASIC signal Transfer Function validation, exploiting

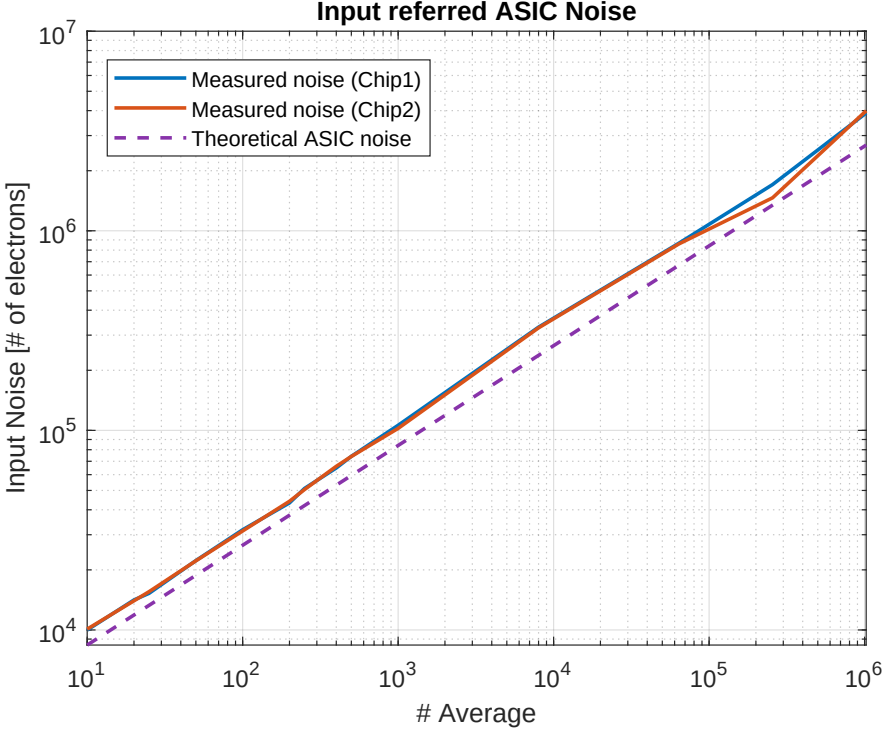


Figure 8.2: *Measured input noise of the spectrometer (expressed in number of electrons) as a function of number of integrations (red and blue lines). Theoretical electronic ASIC noise limit (dashed purple line).*

the testing board and the custom pulse current generator, the final spectrometer was electrically validated.

The noise performances have also been validated: the experimental setup is the same as the one used for the signal transfer function characterization, but with an injected input signal of 0 ppm.

Several measurements have been performed sweeping the number of in-chip integration/differences and then also the number of GI integrations, leading to the impressive result of more than $100dB$ of Dynamic Range, as shown in Figure 8.2. The red and blue lines represent the measured noise reported to the input of two ASICs, while the dashed line below represents the electronic noise computed during the ASIC design phase, as described in Section 6.2.1 ($Input\ Noise = \sigma_{electrons,in} \cdot \sqrt{N}$). According to the-

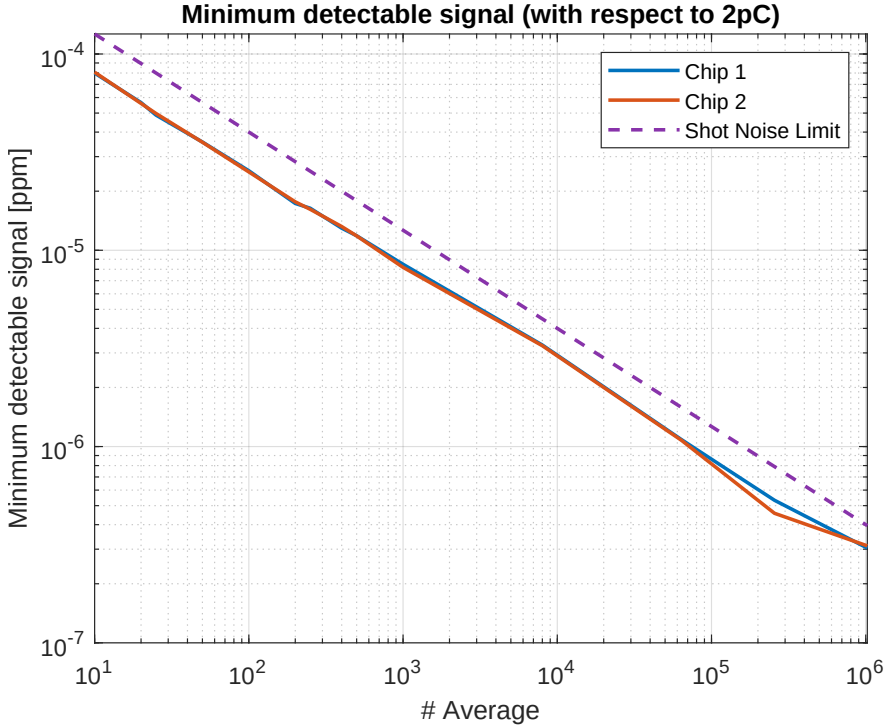


Figure 8.3: Measured noise expressed in ppm as a function of the number of averages (red and blue lines) with a pulse repetition rate of 1MHz and an injected mean charge of 2pC. Theoretical shot noise limit of a photo-generated charge of 2 pC (dashed purple line).

ory, the measured lines follow a $\sqrt{N}$ behavior, where N represents the number of hardware and software averages performed. It is worth to notice that the off-chip noise is negligible with respect to ASIC noise, since the measured output noise of the platform is very close to theoretical electronic noise of the ASIC. The small difference between the theoretical and measured noise values can be attributed to the off-chip electronics.

Figure 8.3 shows how the minimum detectable signal changes as function of the average number. The minimum detectable signal is defined as the signal that makes S/N ratio equal to 1 (in literature it is also named Equivalent Noise Charge). The graph reports two nearly overlapping lines (red and blue continuous lines), representing the standard deviation of the electronic noise of a single chip channel, normalized with respect to the number

of hardware and firmware averages. It can be considered as the minimum detectable signal from the platform, while the purple dashed line represents the shot noise introduced by a photogenerated current pulse that covers the entire voltage dynamic of the charge preamplifier. It is worth to notice that the spectrometer noise is much lower than the shot noise generated by a charge of $12.5Me^-$. In this condition, by setting 1000 hardware subtractions/integrations and 1024 firmware averages (corresponding to a GI depth of 10), the platform is able to reach a resolution of only 0.3 ppm with an input pulsed charge of 2 pC (corresponding to $12.5Me^-$). It means that, in terms of number of electrons, the electronic platform is able to reach a resolution of

$$\frac{0.3 \cdot 10^{-6} \cdot 2 \cdot 10^{-12} C}{1.6 \cdot 10^{-19} C/e^-} = 3.75e^-$$

which is quite an impressive result!

8.2 Optical Validation

The platform performance is optically validated by exploiting the optical setup briefly described in Section 5.3. Figure 8.4 shows a very similar plot with respect to that one reported in Figure 8.3, but differently from the previous case, the graph reports the shot noise limit (purple dashed line) related to a laser pulse amplitude adopted in the optical experiment. The yellow stars instead represent the measured data, keeping the hardware average number equal to 100 and varying the GI depth.

To determine the shot-noise limit that the instrument is able to detect and to compare it with the theoretical calculation, the probe beam pulses are recorded on the photodiode array (with an average power corresponding to a photogenerated charge of 0.48 pC per each photodiode). In this way, the processed output signal corresponded to the difference between two ideally identical probe pulses, so that the overall noise, given by the sum of the shot noise contributions from the individual pulses and the electronic noise, could be extracted from the standard deviation of multiple acquisition. According with theoretical predictions, also in this case, both electronic noise and shot noise scale proportionally to $\sqrt{N}$, while the signal increases linearly with N ,

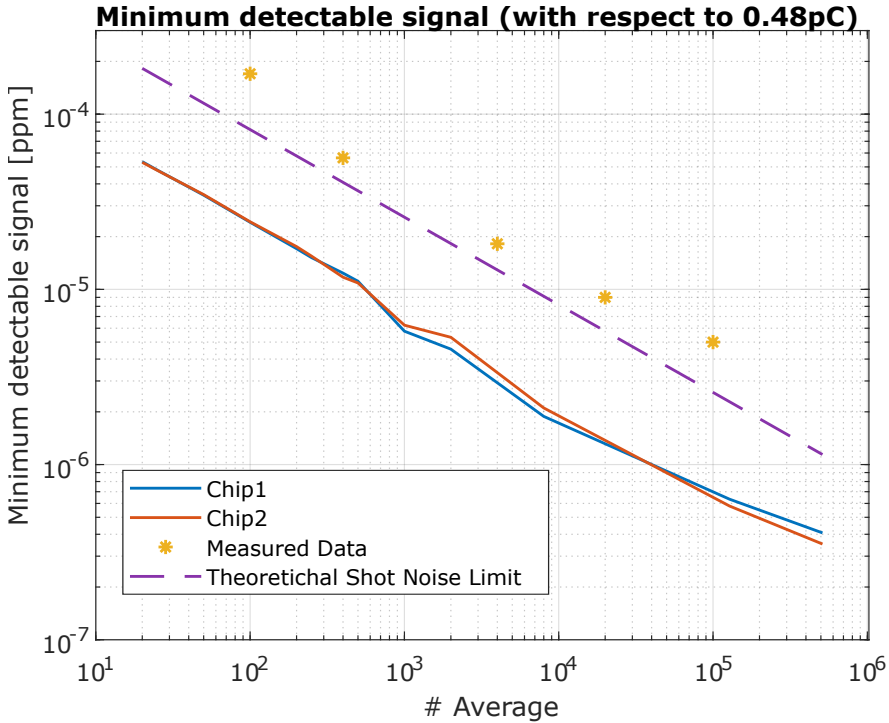


Figure 8.4: Measured signal as a function of the on-chip and GI average number, with an optical pulse amplitude of 0.48 pC and its related shot noise limit.

where N is the total number of averages. Specifically, shot noise is given by $\sqrt{2qQN}$ where q is the charge of the electron and Q is the photogenerated charge from the light that impinges on a given photodiode. So, the minimum detectable signal decreases as $1/\sqrt{N}$. The excess noise that the measured data (yellow stars) show can be attributed to laser fluctuation and thermal drift. By employing a laser with a pulse repetition rate of 100 kHz, the acquisition time for a single point can be expressed as $2 \cdot 10\mu s \cdot N$. Under these conditions, the acquisition time ranges from approximately 2ms ($N=100$) to 2s ($N=100000$), depending on the selected number of averages N . Using a faster laser, such as one operating at a 1 MHz repetition rate, would reduce the acquisition time by an order of magnitude, thereby mitigating thermal drift effects.

Therefore, two conclusions can be drawn:

- The experimental results are in good agreement with theoretical expectations.
- The electronic noise of the platform does not limit the measurement.

In order to validate the parallel acquisition and the multichannel performance of the platform, the probe beam, spread over the 40-element PDA, produces the transmission spectrum shown in Figure 8.5.

The blue trace is measured when the pump is off, keeping the number of averages fixed at 10,000 (100 on-chip averages and 100 digital GI averages). The red trace represents the $\Delta T/T$ signal generated by the pump pulse, obtained as the pump-off - pump-on difference and normalized to the average power.

It can be observed that the average incident power on the forty array elements varies such that the generated charge span from a few tens of femtocoulombs up to more than 700 fC, while the pump-probe signal reaches a resolution of 16 ppm (corresponding to few tens of electrons).

8.2.1 Experimental Results

The setup performance is tested in a real broadband transient absorption pump-probe experiment on a large-area (0.6mm^2) single-layer graphene (SLG), whose ultrafast optical response in the NIR range has been extensively investigated in the last ten years [44–47]. The sample adopted is grown by chemical vapor deposition, and integrated in a top-gate ionic liquid gating field effect transistor allowing electrical control over the doping by varying the Fermi level position [48].

Figure 8.6 presents the $\Delta T/T$ map acquired at a gate voltage of 0 V, with 40 on-chip averages performed for each time delay. The map displays the pump-probe intensity over the wavelength range from 1200 nm to 1650 nm, as a function of the pump-probe delay varying from -1 to 10 ps. In this condition, a positive $\Delta T/T$ is observed, which is attributed to a photo-bleaching effect.

To assign wavelengths within the range of interest to the 40 channels—thus enabling the generation of the maps shown in Figure 8.6, calibration procedure is required. To establish this correspondence, five optical filters spanning the range from 1250 nm

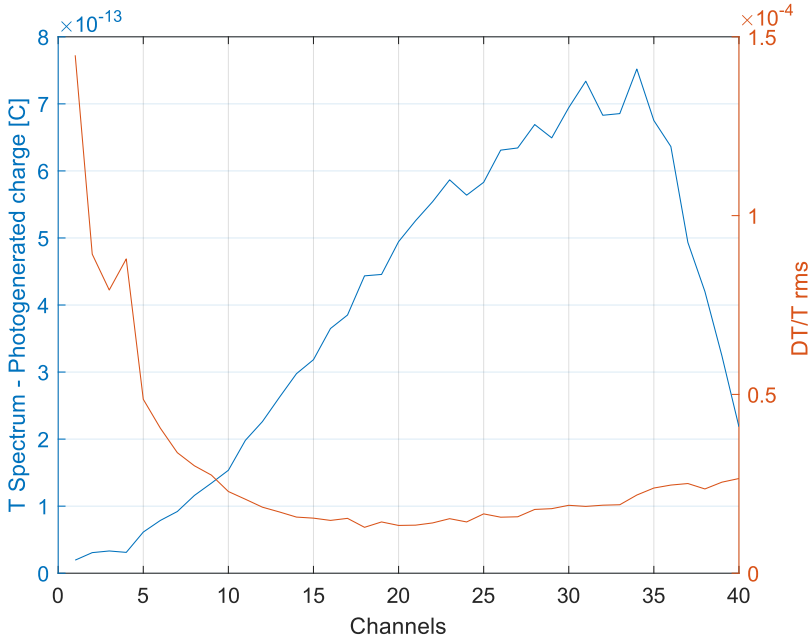


Figure 8.5: Probe Near-Infrared transmission spectrum as a function of the channel (blue line) vs transient transmission signal $\Delta T/T$ rms evaluated over 100 on-chip averages and 100 GI averages (red line).

to 1650 nm are employed. Using the instrument graphical user interface, the channel corresponding to each specific wavelength was identified. Once these five reference points are obtained, a linear interpolation is performed to associate each channel with its corresponding wavelength.

Figure 8.7 shows the $\Delta T/T$ map acquired in high p-doping conditions, while applying a gate voltage of -1.5V. In the probing range, the map features a photo-bleaching (PB, $\Delta T/T > 0$) and photo-induced absorption (PA, $\Delta T/T < 0$) band with signals amplitudes of the order of 10^{-4} . Depending on the probe photon energies, the pump-induced charge carrier distribution results in an increase (PA signal) or decrease (PB signal) of the probe absorption. A comparison between the two graphs reveals that, by tuning the gate voltage applied to the FET and thus shifting the Fermi level, the electronic platform can effectively detect both the pump-induced variations in the transmitted signal intensity

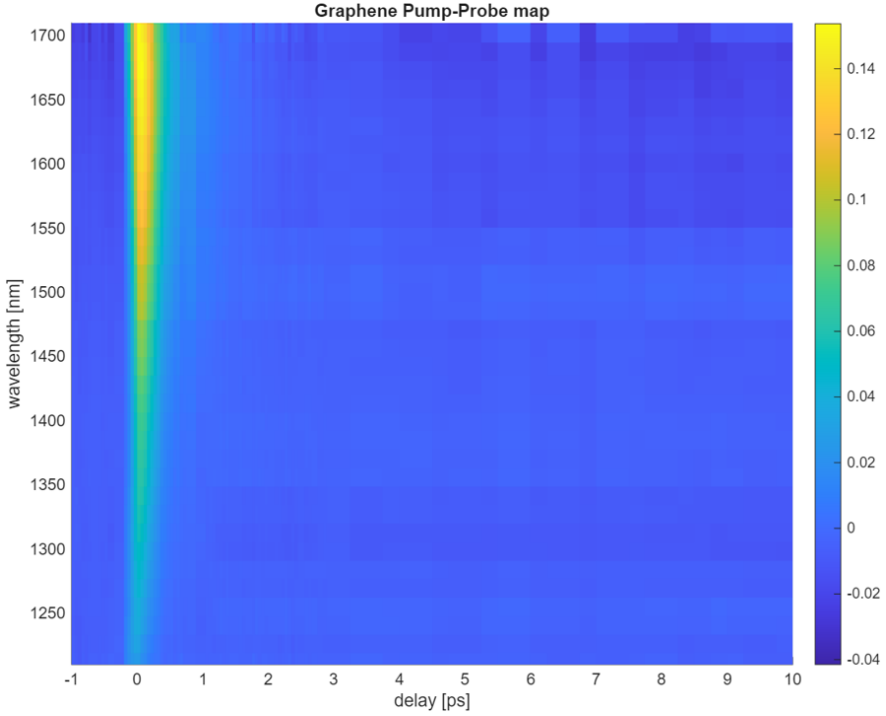


Figure 8.6: *Transient transmission maps of gated single layer graphene measured at different probe wavelength as a function of the time delay with 0V gate voltage*

and the electron relaxation dynamics within the graphene layer.

The performance of the proposed spectrometer can be evaluated against that of a commercial instrument by comparing the results reported here with those presented in [49]. The information that can be extracted from the sample is largely comparable; however, the reported instrument allows for a significant reduction in measurement time, from several hours to few minutes.

These measurements demonstrate the crucial capability of the multichannel spectrometer to detect the pump-probe signal with performance comparable to that of commercial instruments, while significantly reducing the acquisition time and achieving very high sensitivity.

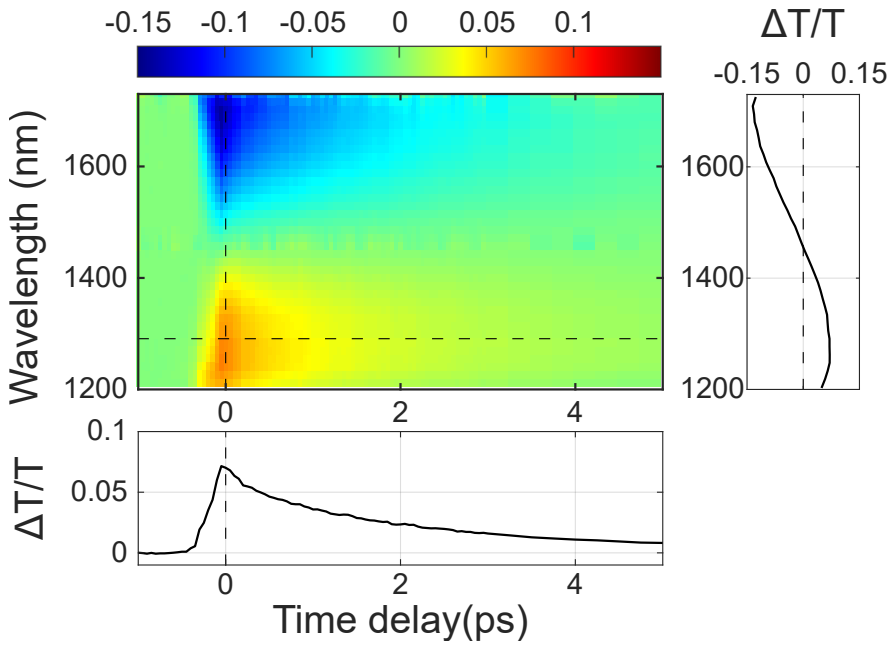


Figure 8.7: Transient transmission maps of gated single layer graphene measured at different probe wavelength as a function of the time delay with -1.5V gate voltage and vertical and linear cuts at fixed wavelength (1280nm) and fixed time delay (0 fs).

CHAPTER 9

Conclusions

This thesis is the result of three years of research carried out at the Innovative Integrated Instrumentation for Nanoscience (I^3N) laboratory under the supervision of Prof. Giorgio Ferrari at Politecnico di Milano (Italy). The main goal of this work is the design, development, and validation of low-noise, high-resolution multichannel electronic systems for two distinct types of broadband spectroscopy: **Raman spectroscopy** and **Pump-Probe spectroscopy**.

Although the two fields of application differ in their physical principles, they share several common electronic design challenges and specification requirements:

- the need for a **multichannel readout architecture** capable of performing parallel acquisition of entire spectra in a single shot;
- a **pulsed optical signal** in the MHz range detected by **photodiode array (PDA)** sensors;

- the presence of a **dominant harmonic optical component** and a **weak modulated component**, several orders of magnitude smaller, introduced through optical modulation transfer (lock-in) techniques;
- in both systems, the **Signal-to-Noise Ratio (SNR)** is primarily limited by laser intensity fluctuations, which must be compensated through appropriate electronic readout strategies.

9.1 Broadband Raman Spectroscopy Platform

The first part of the thesis focuses on the development of a **76-channel acquisition platform** for **Broadband Raman Spectroscopy**, combining the advantages of custom integrated circuits (ICs) and FPGA-based digital processing. This work is part of the **CRIMSON European Project**, coordinated by Prof. Dario Polli of the Physics Department at Politecnico di Milano, whose objective is to develop a non-invasive, label-free optical microscopy tool based on Stimulated Raman Scattering (SRS).

The high number of acquisition channels enables the simultaneous measurement of the Raman spectrum within the **fingerprint region** ($600\text{--}1800\text{ cm}^{-1}$), which contains multiple characteristic molecular signatures from proteins and nucleic acids. However, this imposes stringent design constraints due to the significant number of resources required to implement 76 fully parallel acquisition chains. A differential readout architecture was employed to suppress laser intensity noise, which represents the dominant noise source in SRS microscopy. The front-end electronics are integrated into a **$0.35\text{ }\mu\text{m}$ CMOS custom IC** featuring 8 low-noise amplification channels, operating under shot-noise-limited conditions. Significant design effort was devoted to the implementation of a **two-step demodulation technique** for lock-in detection, aimed at compensating offset fluctuations experimentally observed in the analog acquisition chain.

To this purpose, a digital signal processing (DSP) chain was implemented in the FPGA to perform the second demodulation step in the digital domain, enabling efficient offset correction. The two-step demodulation technique was experimentally validated

on the bench, demonstrating an SNR improvement of up to 22 dB for small-bandwidth acquisitions, achieving a sensitivity of 3 pW of Raman signal for a mean optical power of $1\text{ }\mu\text{W}$. However, the fast acquisition capability of the 76-channel platform was preserved, with an optimized FPGA-PC communication link sustaining a real-time data rate of 640 Mbit/s and a pixel dwell time of $16\text{ }\mu\text{s}$.

9.2 Pump-Probe Spectroscopy Platform

The second and last part of my thesis consists in the realization of a **40-channel spectrometer for ultrafast pump-probe experiments**, designed to surpass the current state of the art by enabling the use of lasers with repetition rates in the MHz range. This allows for improved optical noise rejection and, consequently, a higher achievable resolution. **ECLIPSE** is a **custom IC** specifically developed to serve as the core signal-processing unit for pump-probe spectroscopy experiments. The chip was designed and fabricated within the same research laboratory as part of a previous doctoral project.

During my work, the ASIC was characterized and validated through a dedicated test board. Using a custom current-pulse generator that emulates the optical pump-probe signal, the correct operation of five channels was verified by measuring the input noise standard deviation and extracting the transfer function between the injected charge and the resulting signal. Experimental results showed that, with $5 \cdot 10^5$ total averages, a minimum detectable signal of 0.3 ppm was achieved, which corresponds to **few electrons** input referred noise for an input charge of 2 pC, surpassing those of commercial spectrometers.

After ASIC validation, a complete 40-channel spectrometer platform was designed. The board integrates: a 40-element photodiode array (PDA) sensitive to near-infrared wavelengths, two ECLIPSE ASICs operating in parallel, an analog amplification stage, an analog-to-digital conversion stage and a dedicated FPGA for control and data handling. The FPGA firmware manages the control signals and data transmission to the PC, and includes further processing chain, in order to feature additional averaging steps and offset compensation. This archi-

tecture enables a substantial reduction in acquisition time for high-resolution spectral measurements compared to commercial solutions, opening new possibilities for **real-time pump-probe spectroscopy** in scientific and industrial applications.

The collaboration between electronic designers and optical physicists continues to foster the development of high-resolution, high-speed instrumentation, enabling advanced research across multiple disciplines: from biomedical imaging and life sciences to materials science and nanotechnology, for the benefit of society.

List of Publications

Journal papers

Conference proceedings

Gubello, G., Mantovani, G., Gaburro, A., Polli, D., and Ferrari, G. (2023, June). Modular 76-channel instrument for Broadband Raman Spectroscopy. In *2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)* (pp. 289-292). IEEE.

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Gubello, G., Sciortino, G., Polli, D., Cerullo, G., and Ferrari, G. (2025, September). 40-Channel, Boxcar-Integrator System for High-Resolution Pump-Probe Optical Spectroscopy. In *2025 20th International Conference on Ph.D Research in Microelectronics and Electronics (PRIME)* (pp. 1-4). IEEE.

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with 0.4ppm Resolution for Pump-Probe Optical Spectroscopy.
In 2025 *31st IEEE International Conference on Electronics, Circuits and Systems (ICECS)* (pp. 1-4). IEEE. (to be published)

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