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Chiplet-based Approach to Real-Time Control of Programmable Photonic Circuits

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Abstract

There has been growing interest in recent years in the field of programmable photonic integrated circuits (PICs), as they allow the implementation, directly in the optical domain, of arbitrary linear transformations. The main advantage of transmitting and processing information by means of photonic devices, either discrete or integrated, resides in the extended bandwidth, minimal cross-talk and reduced power dissipation associated with light-based communications. On top of that, the possibility of fabricating PICs on a Silicon Photonics platform, which uses the same process steps adopted for the CMOS technology, indeed improves the overall rentability of optical integrated systems.
A PIC only becomes *programmable* if it is provided with an electronic control layer that reconfigures its devices according to the desired functionality by driving actuators that properly manipulate the propagation of the optical signal. The scope of this layer is twofold: it has both to configure the correct working point of each actuator and to stabilize it over time against any fluctuation that may affect the optical link, either concerning the PIC itself (e.g. thermal drifts) or the phase of the propagating wavefront. This latter requirement also advocates for the definition of a closed-loop system, able to dynamically track the desired PIC configuration.
Several solutions have already been proposed for real-time control

of photonic integrated circuits. Yet, as PICs scale in complexity, now featuring tens or even hundreds of devices to be configured simultaneously, a quest opens up for the definition of electronic controller architectures that can keep up with the pace of photonics in terms of area occupation and power consumption.
In this thesis, a chiplet-based approach to the problem of real-time control of programmable PICs is proposed. The fundamental idea behind this project is that, given the integrated, CMOS-based nature of Silicon Photonics processors, the dedicated control electronics should be fabricated on an integrated platform as well, possibly with as small impact as possible on the overall system in terms of bulkiness and energy demand. After the introduction and a discussion about the general architecture of the overall electrical-optical system, 2 different mixed-signal application-specific integrated circuits (ASICs) will be presented. The first one, fabricated in 2023 in a 350 nm CMOS technology node, successfully allowed to establish up to 50 Gbit/s optical free-space links, proving capable of dynamically reconfiguring the photonic processor to compensate injected turbulence. After several proofs of concept validating the chiplet-like approach, in 2025 a second chip was fabricated in a more scaled technology node (180 nm), which allowed the assembly of the ASIC-PIC system in a compact flip-chip arrangement. Here, the massive adoption of digital electronics to implement the control algorithm allowed to further shrink the footprint of the circuitry and reduce its power consumption, thanks to the design of oversampling converters and PWM-based actuators, ultimately paving the way to the design of seamlessly scalable architectures.

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CHAPTER 1

Introduction

This introductory Chapter briefly highlights the possibilities offered by the adoption of programmable photonic integrated circuits in many present and future applications. Besides that, it also advocates for the opportunity of adding an electronic control layer to the optical system, to enable its reconfigurability.

The Chapter moves on by listing the reasons behind this thesis projects, i.e. the adoption of a chiplet-based approach to the problem of controlling multiple photonic devices. Some discussion and anticipations about the designs developed during this research are also presented, before concluding with an overview of the state of the art.

1.1 Programmable Photonic Circuits

In recent years, interest in general-purpose photonic integrated circuits (PICs) has been steadily growing, mainly due to the possibility of performing programmable all-optical signal processing [1]. PICs can be flexibly reconfigured and thus be employed in various application, such as, but not limited to, reconfigurable filters [2], microwave photonics and beam forming networks [3], separation of mixed guided modes [4], vector-matrix multiplication [5], quantum information processing [6], and neural networks [7].

1.1.1 The need for control electronics

Just like electronic circuits consists in networks of electrical components, reconfigurable PICs can be envisioned as matrices of integrated photonic devices, such as Mach-Zehnder Interferometers (MZIs) [8] and micro-ring resonators (MRRs) [9], whose working point has to be finely tuned to define the desired overall, typically linear optical transfer function [10]. To perform this tuning, the optical processor need a dedicated control layer that enables run-time reconfiguration, possibly without requiring any prior calibration and irrespectively of operating conditions (e.g. available power, temperature, fabrication mismatches). To meet such requirements, an effective solution consists in closing a feedback control loop around each photonic device, so that the working point constantly tracks the target value regardless of unwanted variations and turbulence.

As PICs scale in complexity, now accounting for hundreds to thousands of devices [11], control hardware has to scale up accordingly. Although suitable for prototyping and enabling new optical functionalities, discrete components-based electronic boards (PCBs) [12] do not represent a valid scalable solution that might be deployed for mass production in commercial application. PCBs usually rely on micro-controllers (μCs) or field programmable gate arrays (FPGAs), which allow extensive flexibility, but they fall far from representing a power- and area-optimized solution that integrates on-chip an independent and functional control loop: in fact, apart from implementing the control algorithm on-chip, they require circuitry for sensors readout,

analog-to-digital conversion and actuators drivers that comes as off-the-shelf components.

1.1.2 The advantages of a chiplet-based approach

A promising alternative to such cumbersome solutions comes from integrated electronics. Application-specific integrated circuits (ASICs) are in fact intrinsically scalable, as they can be easily designed and replicated in modules in order to drive each photonic device in the PIC independently, irrespectively of the overall tally, while costing only a fraction of a PCB in terms of area and power. Some designs have already been proposed to improve the stability of few photonic elements against slow drifting variations, like temperature and aging [13, 14]. The scope of this thesis project is to seamlessly extend this integrated closed-loop approach to larger architectures (tens of devices), at the same time enabling fast and dynamic reconfiguration that allow operations that reach beyond sheer compensation of slow variations. In one sentence, the goal is to move the "application-specific" paradigm from photonics to electronics, while losing as little programmability as possible, as conceptually pictured in Fig. 1.1.

On top of these considerations, it should also be added that the fabrication flow of photonic integrated circuits mostly involves materials and processes that have been around for decades, thanks to development of the CMOS process in the field of electronics [15]. A chiplet-like electronic-photonic co-design thus sounds as the most intuitive implementation for the system, with ASICs and PICs coexisting inside the same package. The ultimate limit to integration is represented by the possibility of integrating onto the same silicon die both electronic and photonic devices [16, 17], although these designs still come with significant tradeoffs between performance and cost.

1.2 General architecture for electronic controllers

Fig. 1.2 conceptually shows a PIC, specifically a 16x1 binary-tree matrix of Mach-Zehnder Interferometers (MZI), being controlled by a dedicated electronic platform. A key feature of the electronic architecture is that it implements as many parallel, independent and nominally identical feedback loops as the number of photonic

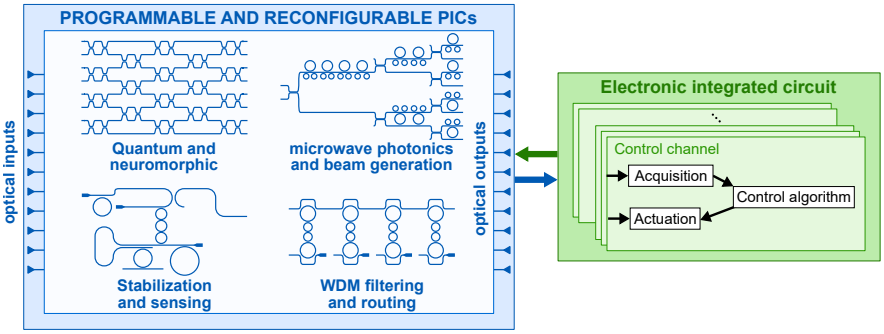


Figure 1.1: *Schematic view of some examples of programmable photonic circuits that would greatly benefit from connection to a dedicated electronic control layer, capable of reconfiguring the optical functionality at run-time.*

devices present in the optical processor. Each of these loops has to first sense the output of the targeted device, then use the extracted information to compute a new working point that is finally translated into an updated actuation command.

1.2.1 Sensing the photonic device

Closing a control loop inherently involves being able to sense the output of the system to be controlled, so as to update its working point accordingly. In the case of a photonic device, the variable of interest is the optical power (and sometimes the phase shift [18]) delivered at one or more output ports. A number of sensors is available for implementation on a silicon photonic platform, from standard integrated germanium photodiodes [19] to non-invasive light sensors [20, 21]. They differ in terms of sensitivity, which is of course the most relevant parameter, as well as linearity and insertion losses. As a consequence, the most suitable sensor for a given PIC also depends on the targeted application: in this Thesis, most of the experiments aim at steering all the available light on one output of the device, therefore "opaque" photodetectors (PDs) are the preferred sensors due to their superior sensitivity (the control loop in fact acts in order to minimize the light impinging on the PD). In other applications, basically whenever partial power splitting between the output ports is required [22, 23], in-line power monitoring has to be performed:

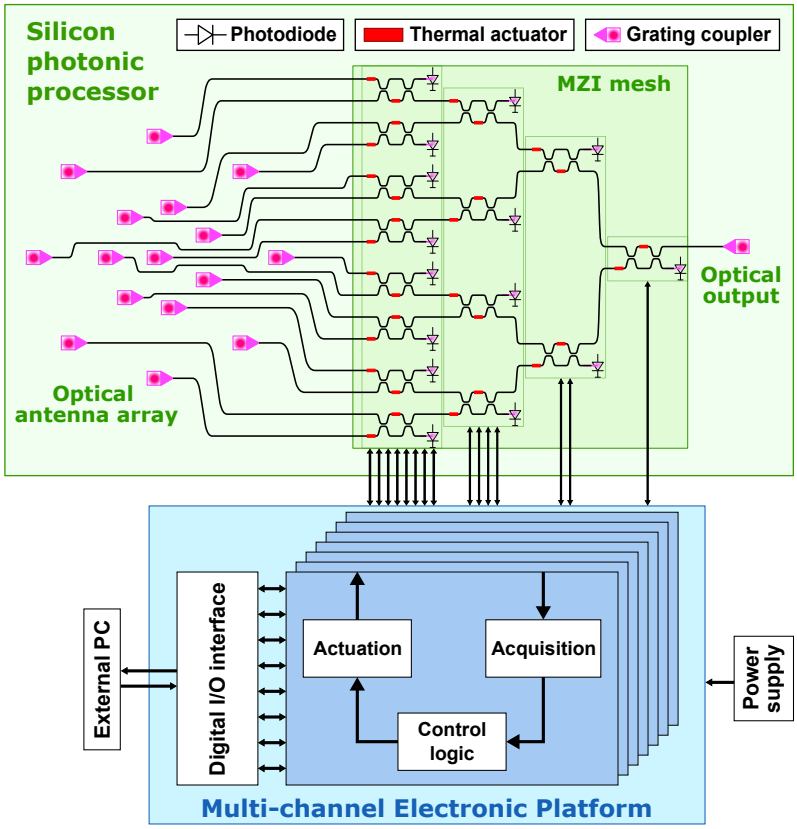


Figure 1.2: *Schematic view of an integrated silicon photonic processor, connected to the proposed dedicated control ASIC.*

tapping a fraction of the available power to a PD also is a viable option [24], although, as said, truly transparent sensors do exists, which rely on the intrinsic, unavoidable photon losses occurring in the crystal (≈1 dB/cm for 1550 nm wavelength in silicon).

1.2.2 Implementing a control algorithm

To enable the control loop, a proper circuitry has to be designed that elaborates the sensed information and drives the actuators accordingly. Given the choice of using an ASIC controller, the system falls behind in terms of programmability with respect to board-based designs. A way to ease the trade-off between flexibility and scalability of the electronics is to largely make use of digital logic and registers to implement the control algo-

rithm. Compared to fully analog solutions [25], digital electronics limits power dissipation and takes advantage, in terms of footprint, of the advancements of the technology node. It also allows the definition of interface register, which can be used for loop parametrization and photonic chip characterization.

Multiple techniques have been proposed to precisely tune photonic devices [26, 27]. Still, an algorithm able to work regardless of the operating conditions, that may change over time, should be able to work without requiring any prior calibration. The technique that will be presented in Ch. 2, and which was used for the designs presented in this Thesis, is the so-called *dithering* technique [28], which combined with lock-in signal processing allows to extract information about the first derivative of the transfer function of the device, rather than its absolute working point, eventually getting rid of offset and mismatches that might be present in the measurement.

1.2.3 Driving the photonic device

To control an integrated photonic device essentially corresponds to modify the refractive index around some localized regions of its constituent waveguides. All sorts of photonic devices, in fact, somehow have to tune an interference pattern between the light beams propagating inside their waveguides. The most straightforward and simple way to control the relative phase shift between the two arms of the device is to locally modify the temperature of the waveguide by means of thermal actuators (*heaters*), usually integrated as doped-silicon or metal resistors [29]. They prove to be a reliable and common solution for applications requiring slow and yet precise modulation (below 100 kHz), made possible by the high thermo-optic coefficient of silicon (refractive index n changes with temperature as $\partial n/\partial T \approx 1.8 \cdot 10^{-4}\mathrm{K}^{-1}$ for λ=1550 nm and T=300 K, as shown in Fig. 1.3). Typical values for their resistance is in the order of hundreds of Ω and a thermo-optic efficiency S_{TO} between 0.1 and $0.3\,\pi/\mathrm{mW}$. Since convergence of the system is ensured only for a minimum total available phase shift of 2π, it can be derived that such actuators need to be driven with a supply voltage in the order of few V.

It might be interesting to discuss the required sensitivity of the actuation drivers, and the starting point of the discussion should

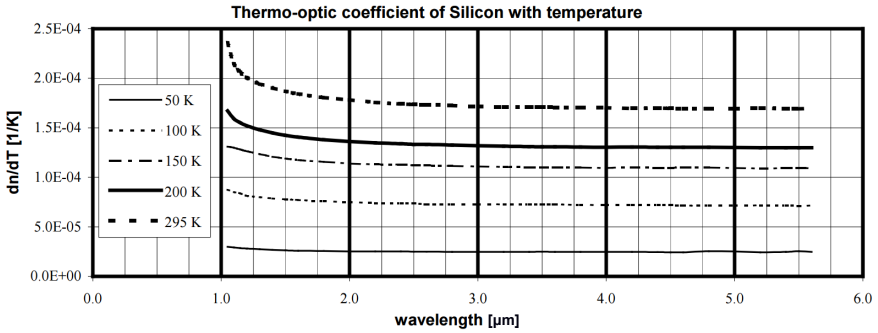


Figure 1.3: *Sensitivity of the refractive index n of silicon on temperature variations, as a function of absolute temperature T and wavelength λ.*

be the extinction ratio (ER) of the device, which is around 30 dB for a common Mach-Zehnder Interferometer, and corresponds to the maximum achievable power split ratio between the two output ports. Therefore, the actuators should be able to control the optical power output of the device with a better resolution than the aforementioned ER, a requirement that is usually met with at least 10-bit precision.

Finally, it is worth highlighting two drawbacks of the thermal actuators. The first and most evident one is the power dissipation that they can require, that easily reaches into the 10-100 mW range (per device). More energy-efficient actuators have been developed, like those built with materials showing high electro-optic coefficients or featuring opto-mechanical phase shifters [30,31], although such designs still do not yet guarantee reliable and cost-effective commercial employment. The second drawback, more subtle, is the fact that there is a quadratic relation between the voltage command of the heaters and their induced phase shift, which is proportional to the dissipated power. The result is a control loop that depends on the bias point, with the system being more sensitive at higher voltages. Ch. 2 will show an algorithmic approach to the mitigation of this issue, where a square-root compression of the control variable is performed; Ch. 5 will instead propose an inherently linear solution, describing a PWM-based driving of the actuators.

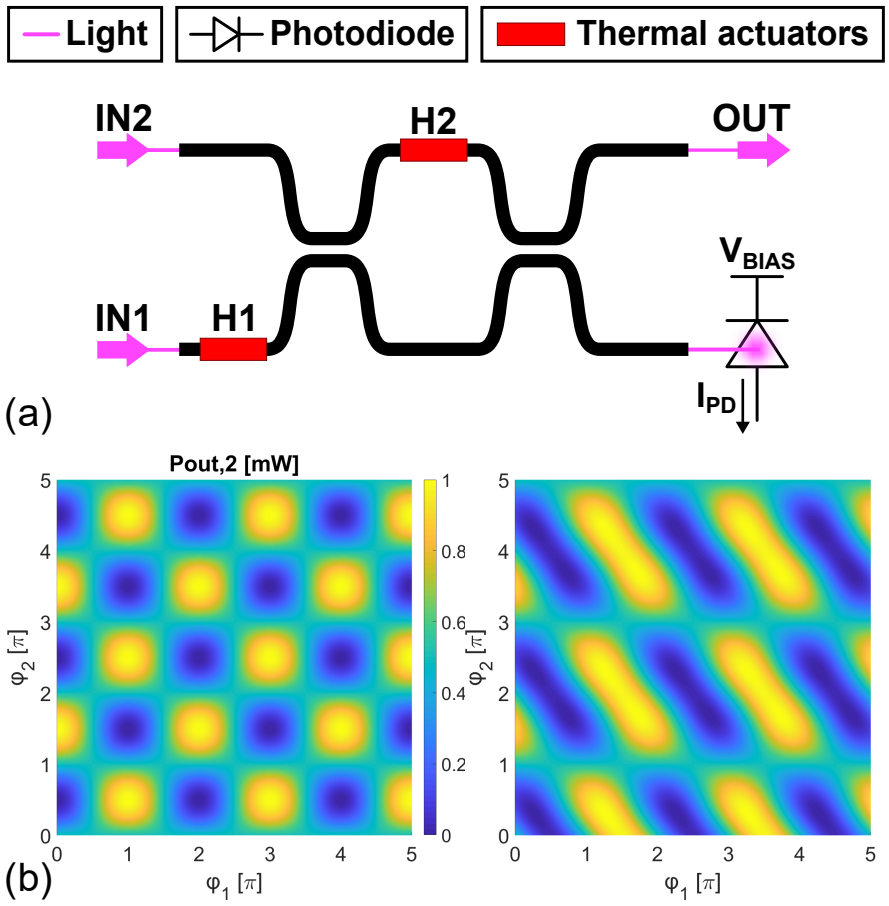


Figure 1.4: ***(a)*** *Schematic of a Mach-Zehnder interferometer using heater as actuators and a photodiode as detector;* ***(b)*** *MZI transfer function $P_{OUT}(\phi_{1,2})$ with k=0.5 (ideal case, left) and k=0.8 (right).*

The case of Mach-Zehnder Interferometers

One of the most common building blocks in photonic integrated circuits is the Mach-Zehnder Interferometer. What follows is a brief mathematical description of these optical elements.

MZIs have 2 optical inputs and 2 outputs, and basically consist of a pair of waveguides (arms) forming a series of two directional couplers, as shown in Fig. 1.4a. The output power (and phase) distribution is the result of the interference between the optical waves propagating inside the two arms of the MZI. The interference pattern at output is determined by the actuators integrated

close to the waveguides, as they allow to alter the phase shift that light accumulates on its path; interestingly, one actuator ($H1$) does play a role only when light is injected at both inputs.

Being a $2x2$ system, the MZI can be model by a transfer matrix describing the relation between input and output electrical fields:

$$\begin{bmatrix} E_{OUT,1} \\ E_{OUT,2} \end{bmatrix} = \begin{bmatrix} T_{1,1} & T_{1,2} \\ T_{2,1} & T_{2,2} \end{bmatrix} \cdot \begin{bmatrix} E_{IN,1} \\ E_{IN,2} \end{bmatrix} \tag{1.1}$$

To make the coefficients of the matrix explicit, all the transfer functions of the single components have to be taken into account:

- the waveguides, equipped with two phase shifters, only alter the phase of the propagating field, ideally without adding any loss:

$$T_{H1} = \begin{bmatrix} 1 & 0 \\ 0 & e^{-j\phi_1} \end{bmatrix} \qquad T_{H2} = \begin{bmatrix} e^{-j\phi_2} & 0 \\ 0 & 1 \end{bmatrix} \tag{1.2}$$

  Note that the coefficients ϕ_1 and ϕ_2 account both for the phase shift due to the physical lengths of the waveguides (which are non controllable and usually identical in their design) and to the additional delay caused by the heat dissipated by the actuators (which form the proper electro-optical interface).

- the two directional couplers, where the parameter n expresses the *coupling coefficient* k of the device (k=1 for total coupling, k=0 for no coupling). Given $\theta = \arcsin(\sqrt{k})$, the matrix of a directional coupler can be written as:

$$T_C = \begin{bmatrix} \cos\theta & -j\sin\theta \\ -j\sin\theta & \cos\theta \end{bmatrix} \tag{1.3}$$

The complete transfer function of the MZI can thus be expressed as the ordered combination of the single components:

$$T_{MZ} = T_{C2} \cdot T_{H2} \cdot T_{C1} \cdot T_{H1} \tag{1.4}$$

The output power is proportional to the square module of the electrical field: $P_{OUT} \propto |E_{OUT}|^2$. The relation, which depends on

the induced phase shifts $\phi_{1,2}$ and the fabrication-related parameter k, can be represented with heatmap plots, as in Fig. 1.4b.

1.3 Real-time control of PICs: State of the Art

A comprehensive comparison of the design that will be presented in Ch. 2-4 with the state of the art of the electronic controllers for PICs is presented in Tab. 1.1. For obvious reasons, the chip developed and tested within this Thesis is significantly competitive in terms of area and power consumption with respect to discrete components-based solutions [32, 33]. Indeed, an ASIC-based approach also represents a more rentable solution for mass production, as it tends to lower fabrication, testing and packaging unitary costs; at the same time, a price is paid in terms of system flexibility, which ultimately limits the possible applications of the design: for example, the chip targets a very specific control law, that might not be suitable for applications requiring fractional optical power routing, instead of sheer on/off switching.

The problem of flexibility can be partially mitigated by integrating only a portion of the electronic controller. Specifically, it comes in handy to integrate readout and actuation blocks, while implementing the proper control algorithm at digital level with the help of external components [14,34]. Such solution, of course, represents a compromise between bulkiness and programmability. Although not optimized for this kind of operation, the ASIC presented in this work could operate in such hybrid configuration, thanks to the presence of a digital I/O interface, which allows to exclude the integrated controller from the loop and connect the sensing and driving circuitry to an external processor (with obvious limitations in terms of overall speed).

Finally, with respect to other fully integrated designs [13, 35], the presented ASIC extends the range of operation from controlling single-actuator devices (MRRs) to components where two heaters have to be driven at the same time and without cross-talk (such as MZIs). In general, the complete integration of the control loop does not seem to limit the response time of the system; noticeably, it also does not require any pre-calibration, meaning that the ASIC-PIC system is insensitive to the environmental conditions where it is set to operate.

	Shawon 2023 [32]	Guglielmi 2017 [33]	Zanetto 2023 [34]	Kramnik 2025 [14]	Li 2021 [35]	Sharma 2022 [13]	**This work [36]**
Photonic Device	Any	Any	MZI, MRR	MRR	MRR	MRR	MZI, MRR
Sensor	Any	Any	On-chip PDs	On-chip PDs	On-chip PDs	On-chip PDs	On-chip PDs
#heaters per device	2	2	2	1	1	1	2
Control tech.	μC-based	FPGA-based	Si.Ph. + FPGA	45 nm CMOS + FPGA	28 nm CMOS	28 nm CMOS	350 nm CMOS
Control alg.	Open loop	Open loop	Dithering based	Abs. power level search	Digital bang-bang	Digital bang-bang	Dithering based
Lock point	Any	Any	Min/Max	Any	Slope	Slope	Min/Max
Fully integrated	No	No	No	No	Yes	Yes	Yes
Pre-calibration	Yes	Yes	No	Yes	No	Yes	No
#photonic devices	64	16	15	12	1	4	8
Power per device	$\approx$0.5 W	$\approx$0.5 W	$\approx$0.1 W	$\approx$0.1 W	$\approx$16 mW	N/A	$\approx$10 mW
Resp. time	N/A	$\approx$12 ms	$\approx$10 ms	$\approx$100 ms	$\approx$0.5 ms*	N/A	$\approx$10 ms
Size	$>$cm^2	$>$cm^2	0.25x 1.2 mm^{2}**	0.2x 2.3 mm^{2}**	1.5x 1.5 mm^{2}***	0.57 mm^2	3x4.1 mm^2
Exp. appl.	Progr. opt. processor	Progr. opt. processor	Progr. opt. processor	Quantum	Optical TX	Optical TX	FSO RX

Table 1.1: *Summary of the main features of electronic controllers found in literature. The presented chip provides compact area, low power consumption, fast response time and calibration-free control law, thus satisfying all the general requirements of electronic controllers - *simulation; **without FPGA; ***including TX circuits.*

CHAPTER 2

8-channel integrated controller

In this chapter, the general architecture of the first CMOS controller is described, with particular focus on all the electronic design choices made during the design stage to mold the ASIC onto the specifications of the photonic application.

The chapter also presents a mathematical discussion and modeling of the control loop, which accounts both for electronic and optical elements. Before that, some insights about the dithering technique are offered to better understand the working principle of the controller. The results presented here were published on *The IEEE Open Journal of Circuits and Systems* [37].

2.1 CMOS controller architecture

A comprehensive schematic of a single channel of the ASIC controller, which operates with a 3.3 V power supply, is represented in Fig. 2.1, also showing its 3 connections to the PIC: one to read the photogenerated current of the integrated photodiode and two to drive and orthogonally modulate the thermal actuators. In fact, the channel features an I/Q modulation lock-in scheme, which allows to independently drive the two thermal actuators which are integrated in every MZI. However, as it will be discussed in Sec. 2.3, the control algorithm implemented here is suitable also for single-actuator devices, such as micro-ring resonators, with no need for modifications of the ASIC: it is sufficient to connect only one driver to the PIC while leaving the second output floating. For better clarity, it is convenient to subdivide the ASIC into 3 main different areas which will be analyzed separately in the following:

- **read-out scheme**, comprising the integrated optical sensor, the analog filtering stage and an ADC;
- **digital circuit**, that implements the actual control algorithm and allows interaction between the ASIC and the user;
- **actuation drivers**, that turn the output of the digital circuit into a current to be fed to the thermal actuators.

2.1.1 Read-out circuit

The current generated by an integrated germanium photodiode (PD) is fed to an analog front-end (dark red portion in Fig. 2.1) tasked with amplifying, filtering and digitizing the signal, which contains both a DC component, proportional to the optical power impinging on the PD, and an I/Q small signal (*dithering*) modulation, necessary to discriminate and separately drive the two thermal actuators of the MZI. The output of the GI is sampled at f_S=100 kSps by a 10-bit successive-approximation (SAR) ADC, provided by the foundry process design kit (PDK).

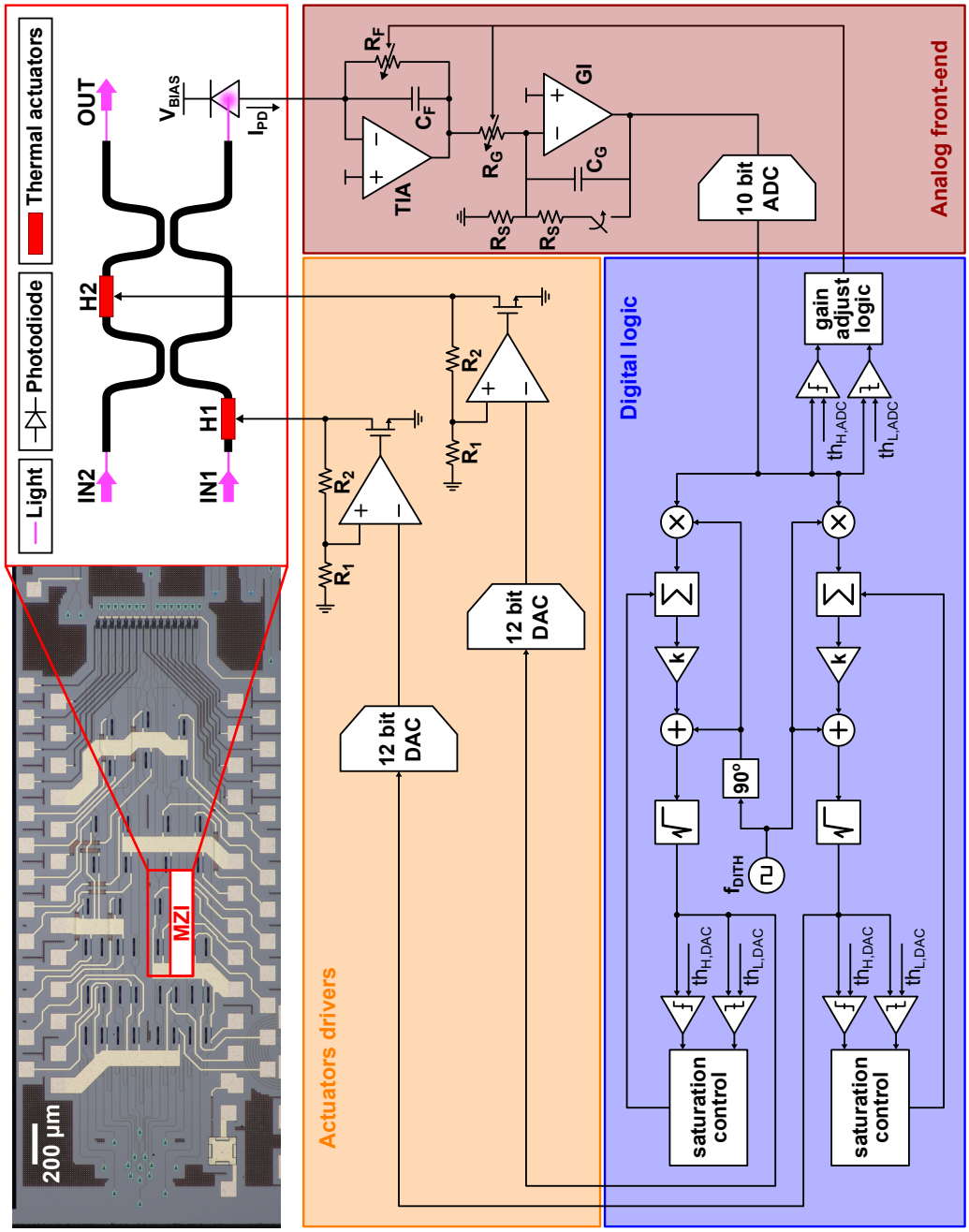


Figure 2.1: *Detailed schematic of a single channel of the control loop, connected by 3 metal wires to a MZI, part of a 16-channel binary-tree mesh (microscope picture).*

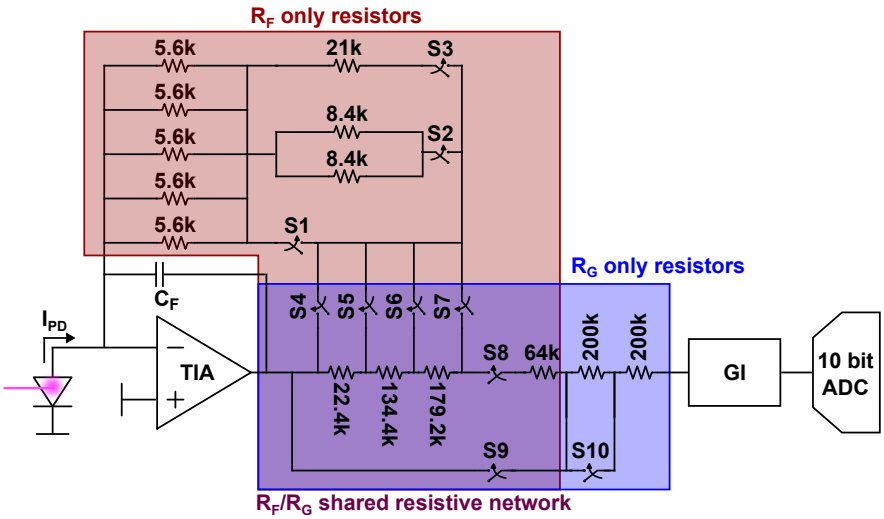


Figure 2.2: *Detailed schematic of the resistive network implementing the variable gain. Resistors in the violet region may be connected in series either to R_F or to R_G according to the selected current amplification factor R_F/R_G.*

Variable gain read-out scheme

The photogenerated current is first converted into a voltage by means of a transimpedance amplifier (TIA), and the resulting signal serves as the input of a Gated Integrator (GI) low-pass filter, responsible for the necessary anti-aliasing action before sampling and converting the analog signal into a digital one.

As discussed in Ch. 1, the value of the photocurrent may span over six orders of magnitude, depending both on the working point of the photonic device and the total amount of available optical power (assumed to be spanning from 0 dBm down to less than −50 dBm). To discriminate a value smaller than −50 dBm across this range with proper resolution, the ADC should have at least 18 effective bits: that could only be achieved at the price of unacceptable area and power consumption in case of Nyquist-rate converters or an extremely large oversampling ratio for a ΣΔ-based solution. As it will be shown in Ch. 4, however, in most of the applications this ASIC is conceived for it is only needed to minimize the current generated by the PD: as a result, a sufficiently precise resolution is only needed when the MZI is operated

$\mathbf{I}_{PD_{MAX}}$[µA]	$\mathbf{I}_{PD_{min}}$[µA]	$\mathbf{R}_F$[kΩ]	$\mathbf{R}$[kΩ]	$\mathbf{G}_{IN}$[Ω]
850	212.5	1.4	800	3.5 k
212.5	53.12	5.6	800	14 k
53.12	13.28	22.4	800	56 k
13.28	3.32	44.8	400	224 k
3.32	0.83	179.2	400	896 k
0.83		358.4	200	3.58 M

Table 2.1: *Different gains depending on the light intensity impinging on the photodiode.*

close to a minimum of its transfer function. This resulted in the adoption, in the design, of a power- and area-efficient 10-bit ADC with a front-end stage that adapts its gain to the DC value of the actual input signal. The resistive network that delivers the amplification, which is detailed in Fig. 2.2, is thus controlled by a combinational logic that properly configures the switches in order to set the amplification factor R_F/R_G so that the input current I_{PD} is always mapped on the full-scale range of the ADC. The logic that governs the switching activity implies that, whenever the photogenerated current scales down by a factor 4, as sampled by the ADC, the factor R_F/R_G is consequently increased by a factor 4. For coherence, the weight of the ADC samples fed to the control algorithm is also scaled down by an equivalent factor. Tab. 2.1 summarizes the values of R_F and R_G for the 6 possible configurations, depending on the value of the input current I_{PD}.

Design of the TIA and GI

For both amplifiers, a two-stage class-AB current compensated architecture [38] was chosen, resulting in an open-loop gain of 90 dB and a gain-bandwidth product of 50 MHz. The topology, which is the same both for TIA and GI, is reported in the schematic of Fig. 2.3, and was selected mainly due to better performance in terms of compactness (with respect to a nulling resistor compensation) and phase margin (with respect to a voltage buffer). In the case of the TIA, the output stage (transistors $M_{5,6}$) was sized to carry the maximum possible value of the photogenerated current (850 µA for 1 mW optical power), which largely contributes to the overall static power dissipation

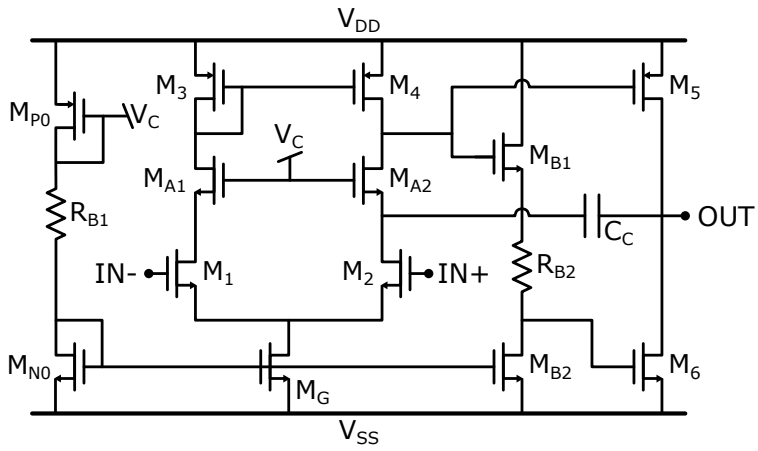


Figure 2.3: *Two-stage current-compensated amplifier adopted to implement both the TIA and the GI of the read-out circuit.*

of the TIA (3.6 mW). In the GI, instead, the most critical aspect was the external slew rate of the amplifier, which had to be fast enough to discharge the output node to which C_C(3 pF), C_G (4.8 pF) and the input capacitance of the ADC (3 pF) are connected. Setting the slew-rate at SR =50 µV/s determines a bias current of transistor M_G of 200 µA, which primarily contributes to the power dissipation of the amplifier (1.3 mW). An extensive summary of all the parameters of each device are reported in Tab. 2.2 (for the TIA) and Tab. 2.3 (for the GI). Both amplifiers have R_{B1}=33.8 kΩ and compensation capacitance C_C=3 pF. The value of the voltage-shifting resistance R_{B2} is instead 8.3 kΩ in the TIA and 14.9 kΩ in the GI. To save area, the n-type MOSFETS are not placed in a well, causing the presence of body effect (threshold voltage increases for devices placed higher in the stack).

Regarding the TIA, a feedback capacitance C_F=500 fF was used to guarantee the stability of the amplifier over a bandwidth ≥900 kHz for every configuration. The GI, which provides the necessary anti-aliasing filtering before digitization, is instead tailored on the small signal modulation that is purposely superimposed by the actuators onto the working point of the interferometer. This *dithering* modulation, whose scope will be further discussed in Sec. 2.3.1, consists in am I/Q square wave stim-

	$\mathbf{V}_T$	$\mathbf{V}_{OV}$	$\mathbf{V}_{DS}$	$\mathbf{I}_{DS}$ [μA]	W/L	$\mathbf{g}_m$ [μS]	$\mathbf{r}_0$ [kΩ]
$\mathbf{M}_{N0}$	0.53	0.15	0.68	50	34/1.2	560	600
$\mathbf{M}_{P0}$	0.72	0.20	0.92	50	60/1.2	450	450
$\mathbf{M}_G$	0.53	0.15	0.75	200	128/1.1	2250	155
$\mathbf{M}_{1,2}$	0.72	0.17	0.63	100	100/1.2	1000	300
$\mathbf{M}_{3,4}$	0.72	0.4	1.13	100	30/1.2	500	240
$\mathbf{M}_A$	0.88	0.12	0.80	100	56/0.7	1300	180
$\mathbf{M}_{B1}$	0.88	0.15	2.1	50	34/1.2	570	1400
$\mathbf{M}_{B2}$	0.53	0.15	0.78	50	34/1.2	570	1400
$\mathbf{M}_5$	0.72	0.40	1.65	800	225/1.1	3640	44
$\mathbf{M}_6$	0.53	0.25	1.65	800	180/1	5770	58

Table 2.2: *Parameters of all the MOS devices in the schematic of the OTA. Voltages are expressed in V, W/L ratios are expressed in μm.*

ulus with period T_{dith}=120 µs (f_{dith} ≈8.3 kHz), resulting in an output power modulation whose waveform is schematically represented in Fig. 2.4. The output of the GI is sampled every $T_S = 1/f_S$ =10 µs, meaning that each modulation period produces 12 samples. The reset of the GI is operated by an RC network (R_S=7 kΩ) in a negligible time transient compared to T_S. The overall transimpedance gain of the read-out stage can thus be expressed as:

$$G_{IN} = \frac{R_F}{R_G} \cdot \frac{T_G}{C_G} \tag{2.1}$$

With C_G=4.8 pF, R_F in the 1.4 kΩ ÷ 358 kΩ range and R_G between 200 kΩ and 800 kΩ, the value of G_{IN} can vary between approximately 3.5 kΩ and 3.6 MΩ.

Noise analysis

Finally, some considerations should be made regarding the noise affecting the read-out chain, as it ultimately determines the accuracy of the control action. As a simplification, the front-end will be only considered in the configuration of maximum gain (R_F=358.4 kΩ, R_G=200 kΩ, G_{IN}=3.6 MΩ) and assuming a minimal current generated in the photodetector (≤150 nA, corresponding to the worst case for the dark current baseline). Again,

Device	V_T	V_{OV}	V_{DS}	I_{DS} [μA]	W/L	g_m [μS]	r_0 [kΩ]
M_{n0}	0.53	0.15	0.68	50	34/1.2	560	600
M_{p0}	0.72	0.20	0.92	50	60/1.2	450	450
M_g	0.53	0.15	0.54	150	110/1.3	1680	160
$M_{1,2}$	0.69	0.31	0.73	75	25/2.4	440	660
$M_{3,4}$	0.72	0.15	0.87	75	140/1.2	820	290
M_A	0.88	0.12	1.05	75	35/0.6	970	190
M_{B1}	0.88	0.15	1.90	50	33/1.2	560	1480
M_{B2}	0.53	0.15	0.67	50	33/1.2	560	590
M_5	0.72	0.15	1.65	150	250/1	1670	160
M_6	0.53	0.15	1.65	150	150/1.75	1700	360

Table 2.3: *Parameters of all the MOS devices in the schematic of the GI amplifier. Voltages are expressed in V, W/L ratios are expressed in μm.*

this assumption is justified by the fact that in most applications the control loop works to minimize the optical power on the PD. As a last premise, for what concerns *1/f* noise it is possible to assume its contribution as negligible, due to the lock-in processing performed by the circuit, which will be better explained in Sec. 2.3.1, that averages out low-frequency components.

The TIA has an input referred voltage noise power spectral density $S_{V_{IN}}$=$(6.4\,\mathrm{nV}/\sqrt{\mathrm{Hz}})^2$. Its overall effect is crucially dependent on the stray capacitance C_P connected to the TIA virtual ground and mainly due to the metal-wire connection between the ASIC and the integrated PD on the PIC, as it generates an input current noise with spectral density $S_{I_{IN}} = S_{V_{IN}} \cdot (2\pi f \cdot C_P)^2$. A reasonable value for C_P is 1 pF: alongside shoreline limitations that will be discussed in Sec. 5.3, noise is one of the main reasons that advocate for pushing denser integration of photonic-electronic co-designs, for example with the adoption of flip-chip arrangements [39].

There are two other current noise sources to take into account for a fair comparison: the unavoidable shot noise associated with the PD (with power spectral density $S_{SHOT} = 2qI_{PD}$) and the thermal noise of the feedback resistor R_F (density $S_{R_F} = \frac{4kT}{R_F}$). Alongside the TIA input-referred noise, they all undergo the same low-pass frequency shaping, namely the pole introduced by the compensation capacitance C_F, the limited bandwidth of the TIA

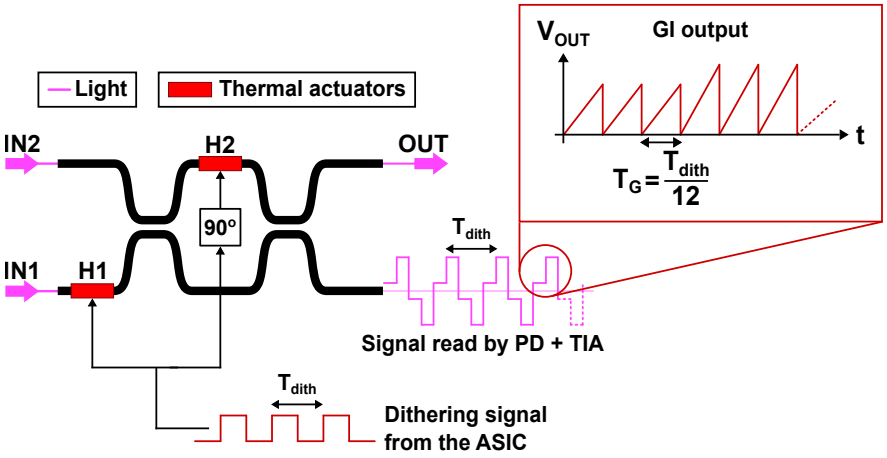


Figure 2.4: *Schematic visualization of the operation of the read-out. There are two actuators driven with I/Q modulation, yet there is only one acquisition chain, as the discrimination between the two tones happens after digitization.*

and, above all, the low-pass filtering action of the Gated Integrator, which is equivalent to that of a single-pole RC network with time constant $RC = T_G/2$=5 µs. Interestingly, among the three sources the TIA input referred noise source gives the smallest contribution even at the frequency of the local pole introduced by C_F ($f_P = \frac{1}{2\pi C_F R_F}$=900 kHz). However, as a property of any lock-in (de)modulation scheme [40], noise contributions should be compared at the frequency of the modulating signal, which in this case is the dithering frequency f_{dith} ≈8.3 kHz. The lock-in chain, in fact, inherently implements a band-pass filtering action centered around f_{dith} whose bandwidth is that of the general control loop closed around the PIC, which is usually set in the order of few hundreds Hz, as it will be discussed in Sec. 2.3. At f_{dith} the noise contributions are thus: $S_{I_{IN}} \approx (0.3\,\text{fA}/\sqrt{\text{Hz}})^2$, $S_{R_F} \approx (215\,\text{fA}/\sqrt{\text{Hz}})^2$ (with R_F=358.4 kΩ) and $S_{SHOT} \approx (220\,\text{fA}/\sqrt{\text{Hz}})^2$ (with I_{PD} ≈150 nA). Noticeably, the TIA contribution is definitely negligible, whereas the feedback resistor R_F only doubles the total input noise of the GI. Its contribution could indeed be reduced by increasing R_F, although at the price of larger area occupation for marginal improvements in total noise.

2.1.2 Digital electronics to boost flexibility

As mentioned, a major improvement in the design of the ASIC with respect to its predecessor [41] is represented by the massive adoption of digital electronics to effectively implement the control algorithm in a compact yet somehow flexible solution. The advantages of a mixed-signal ASIC with respect to a fully-analog solution are straightforward, mainly related to power and area efficiency (which both increase as the technology node scales forward), the simplified access to the information about the state of the circuit and the possibility to configure some parameters of the ASIC.

In the proposed ASIC, the digital circuit (blue region in Fig. 2.1) behaves as a proper CPU for the ASIC. Among its tasks feature:

- monitoring of the ADC operation to implement the automatic control of the read-out variable gain;
- effectively perform both the I/Q lock-in modulation and the consequent extraction of the dithering signal amplitude;
- define the integral controller whose output will be fed to the actuators (orange region) to update the working point of the photonic device;
- allow I/O interaction between end user and the chip.

Concerning the adjustment of the resistors R_F and R_G to adapt the read-out to the total input current I_{PD}, a logic network compares the first sample of each dithering modulation period with two user-selected thresholds: if it falls below the lower threshold (since I_{PD} has diminished), R_F/R_G is increased by a factor 4, and vice versa if the sample overcomes the upper threshold. The ADC output is also double right- or left-shifted, respectively: with 5 possible configuration of read-out gain, this guarantees up to 20-bit resolution when the device is locked to a minimum of its transfer function ($I_{PD} \leq$830 nA). The logical shift ensures that the loop gain of the general electronic-photonic system is independent from the front-end configuration.

The extraction of the signal of interest, which is the amplitude of the dithering modulation superimposed to the bias point

of the MZI, is also performed at digital level by a pair of digital mixers; indeed, the lock-in architecture takes advantage of digital electronics in the sense that it is extremely simple to implement square-wave mixers. A square-wave stimulus, differently from a sine-wave, does not require look-up tables nor sophisticated digital multipliers for modulation and demodulation, respectively. The relation $f_{dith} = \frac{f_S}{12}$ is not incidental: selecting a multiple of 4 simplifies the demodulation of the two orthogonal stimuli applied to the actuators, as suggested by Fig. 2.4. The following accumulator (Σ symbol in Fig. 2.1) is used to update the working point of the actuators with the extracted dithering amplitude, which is proportional to the partial derivatives of the MZI transfer function. In this sense, the digital circuit is effectively implementing an integral controller that works to minimize the extracted signal, i.e. to lock the MZI to a stable equilibrium point of the $P_{OUT}(\phi_{H1}, \phi_{H2})$ relation.

Once the new working points of the actuators have been determined, i.e. after the accumulation of 12 ADC samples, the I/Q dithering modulation to be extracted in the following iteration is added. As a final step, a purely combinational entity is used to perform an approximated square-root compression, which is needed to compensate for the fact that, despite controlling the voltage V_{ACT} applied to the actuators, the thermally induced phase shift ϕ_H is proportional to their dissipated power. More details on the implementation of this algorithm are reported in the following Section.

The digital circuit has a dedicated power supply of 3.3 V and all its blocks are clocked by a single source at f_{CLK}=1.1 MHz, which is the same adopted by the ADC. Every entity of the digital circuit was first described in VHDL and then mapped to the desired technology by means of the Cadence Inc. suite for synthesis and implementation, Genus and Innovus.

Square-root compression

As it was anticipated, a square-root operation performed before delivering the command to the DACs can compensate for the quadratic distortion which is inherently present between the voltage V_{ACT} applied to the actuators and the phase shift ϕ_H induced in the waveguide. Calling C the output of the modulator, com-

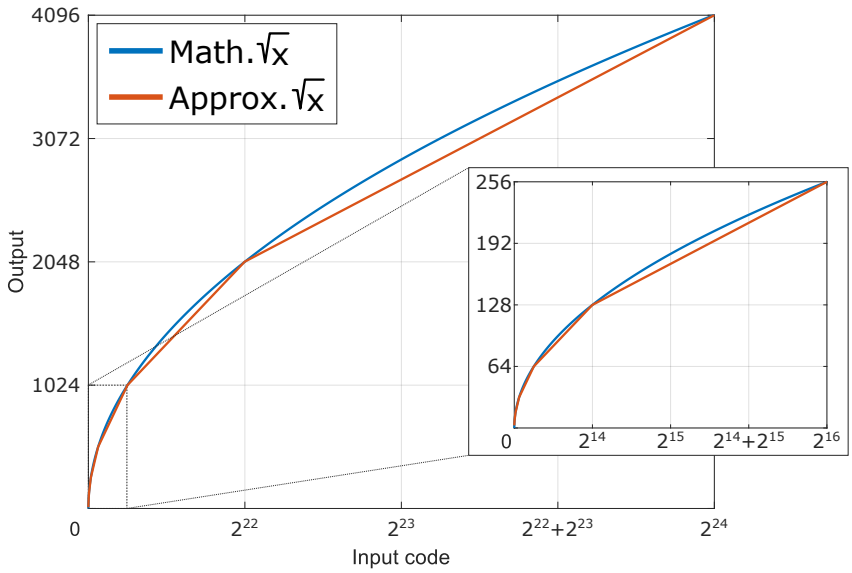


Figure 2.5: *Visualization of the approximated square-root compression through a piecewise linear function. The approximation matches the mathematical function only when the input code is* 2^{2N} *(N is integer).*

prising both the working point and the superimposed dithering signal, the relation holds:

$$\phi_H \propto \frac{(V_{ACT})^2}{R_H} \approx (\frac{\sqrt{C}}{2^M})^2 \cdot V_H \tag{2.2}$$

where $M = 12$ is the number of bits of the DACs and V_H=6 V is the power supply of the actuators. It can be seen that C variations alter the phase shift irrespectively of the particular DC value of C, meaning that the quadratic distortion is effectively compensated by the square-root compression.

A circuit performing a square-root operation can be implemented both in the analog [35] and the digital [42] domain. In the latter case, a precise evaluation can be obtained, although at the price of using bulky circuital solutions, such as multipliers, accumulators and look-up tables [43]; in the former, a compact solution featuring only few transistors is limited, though, in the input voltage swing. In this work, however, the goal is to miti-

gate the aforementioned distortion in order to make the overall loop gain of the system more independent of the DC bias, not to deliver an optimal arithmetical cell. As conceptually illustrated by Fig. 2.5, the idea is to approximate the exact function $y = \sqrt{x}$ with a piece-wise linear function whose slope is progressively scaled by a factor 2 every time the input digital code $[2^{2N} \div 2^{2N+2}]$ increases by a factor 4. Each trait is represented by the linear equation:

$$y = \frac{1}{3} \cdot (\frac{x}{2^N} + 2^{N+1}) \tag{2.3}$$

which is fairly simple to translate into logical circuits, as it only requires an addition and a N-bit right-shift, provided that the factor 3 is accounted for as a proportional gain factor inside the loop, effectively realizing the relation:

$$3 \cdot y = \frac{x}{2^N} + 2^{N+1} \tag{2.4}$$

With a N=12-bit word to be fed to the DAC, it is straightforward to conclude that the input value C has to be 24 bits long. The proposed solution trades precision for compactness, as the combinational logic required by this algorithm, which strongly mitigates but does not perfectly compensate for the quadratic non-linearity, only amounts to 4% of the area of the digital circuit.

ASIC-user interaction

As pointed out above, a major advantage of digital electronics is the possibility to easily implement an I/O interface that lets the user both read the circuit and modify some parameters. To this scope, the ASIC is equipped with a small shift-register (≈650 bits) that allows serial communication between ASIC and user.

The register is designed to sample, upon user request, the result of the ADC conversion (10 bits/channel) and the currently selected gain of the analog stage (3 bit/ch.), thus allowing to resort to the value of the photogenerated current, as the experiments of Ch. 3 and 4 will demonstrate; at the same time, it is also possible to monitor the voltages being applied on the thermal actuators, as expressed by the digital words being fed to the

DACs ($2 \cdot 12$ bits/ch.).

The user can also parametrize the operation of the digital circuit in order to tailor the action of the controller to the specific application. These parameters include:

- the amplitude of the dithering oscillation, which may be selected in the $1\,\mathrm{mV} \div 100\,\mathrm{mV}$ range;
- a gain k applied to the samples fed to the accumulator, with k between 1 and 2^{-R}, where R is an integer;
- the thresholds, for the ADC samples, that determine the modification of the read-out scheme to adapt its gain;
- the upper and lower thresholds that trigger the reset of the accumulator value to a predefined user-selected working point. These values have to be chosen in order to guarantee that the available span of C values allows to cover both a point of minimum and one of maximum in the transfer function of the MZI;
- the possibility to disengage the square-root algorithm and directly pass the 12 MSBs of the modulated accumulator output to the DACs;
- a single bit that determines the sign of the multiplication performed by the mixer, and consequently of the overall loop gain, in order to lock the system either to a maximum or to a minimum of the transfer function of the MZI.

The same registers can also be used to deactivate the integral controller mechanism and manually drive each actuator. This comes in handy when the user wants to fix the configuration of the PIC in a given state, such as in sensing applications, or whenever the experiment requires a characterization of the device, which can be performed by running a full sweep of the voltage applied to each actuator, as it will be shown in Ch. 3.

2.1.3 DAC and actuation circuit

The two 12-bit words generated by the digital logic are the commands that drive the thermal actuators integrated close to the waveguides and ultimately set both the working point of the MZI

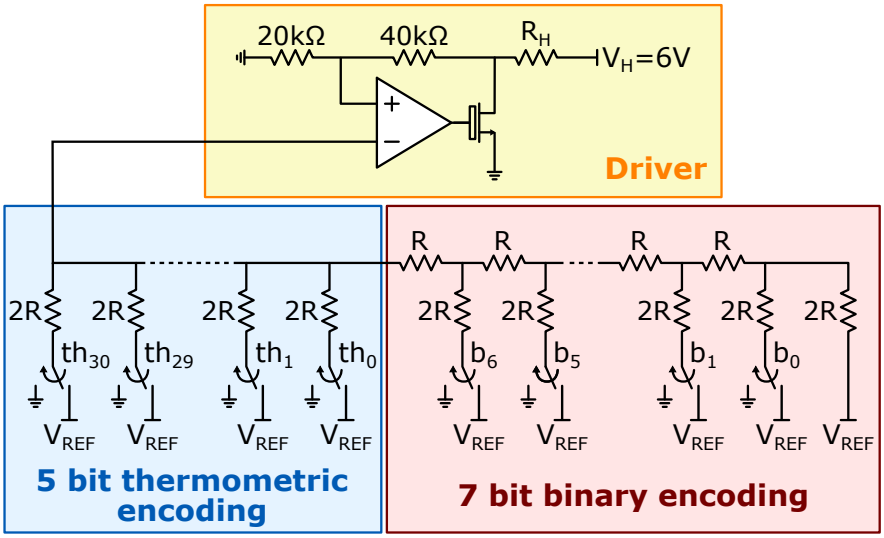


Figure 2.6: *Schematic of the actuation chain bridging the ASIC digital logic to the MZI thermal actuator, represented here by the resistor R_H. Each channel of the ASIC features two identical chains.*

and the superimposed small signal modulation. Considering a 6 V power supply, the voltage on the heaters can thus be controlled with an accuracy of ≈1.5 mV. This value of the LSB determines, in the worst case, a phase shift of $\Delta\phi_{LSB}$ ≈4 mrad. When the light impinging on the detector is properly minimized/-maximized, corresponding to the MZI being locked to a stationary point of its transfer function, this value of $\Delta\phi_{LSB}$ determines a displacement from the ideal locking point between −50 dB and −60 dB, which is negligible compared to the typical extinction ratio of a standard MZI, which is around 30 dB.

The schematic of the actuation chain is reported in Fig. 2.6. The DAC is implemented with a voltage-mode *R-2R* resistive network, operated with V_{REF}=2 V. As a good compromise between precision and area occupation, the architecture of the DAC was segmented to convert the 5 most significant bits with a thermometric encoding and the 7 least significant bits with a binary one. The accuracy of the DAC depends on the value of the resistors: the larger they are, the better process-related variations are averaged out. To this purpose, the value R =80 kΩ was selected, which ensures a maximum current budget of the DAC of

120 µA. These design choices limited the DNL of the DAC (both statistical and deterministic) below 1 LSB in 99.7% of Montecarlo simulations, thus ensuring monotonic behavior. This is a mandatory requirement for the DAC, as a non-monotonic component might cause the controller to lock around the code where the non-monotonicity occurs, rather than an actual stationary point of the interferometer transfer function.

The output of the DAC ranges between 0 V and V_{REF}=2 V, which is however insufficient to properly drive the heaters. In fact, with a maximum voltage drop of 6 V over a nominal resistance R_H=400 Ω, the actuator has to sustain a current up to 15 mA and dissipate up to 90 mW, which are necessary to ensure the $\Delta\phi_{MAX} \geq 2\pi$ needed for full control over the MZI working point. The requirement is clearly unfeasible for the stand-alone DAC, but the introduction of an OTA in non-inverting configuration allowed to set the current in R_H driven by a power MOSFET with sufficient current capability and voltage tolerance (7 V maximum drain-source voltage). The feedback resistors that scale V_{REF}=2 V to V_H=6 V were sized to R_1=20 kΩ and R_2=40 kΩ, large enough to limit the fraction of current steered from the power device to the feedback branch.

Driver OpAmp topology

The OpAmp that powers the driver stage is implemented with a folded-cascode topology, as reported in Fig. 2.7. Such topology was chosen due to its large output resistance, which provides sufficient amplification to compensate for the unavoidable reduction of the loop gain caused by the connection with the thermal actuator (nominal R_H ≈400 Ω, but it can be as low as 250 Ω). The differential pair $M_{1,2}$ uses p-type transistors since V_{ACT}, and hence the common mode input signal of the OpAmp, can be as small as 0 V. The typically limited output voltage swing of single-stage OpAmps has been incremented with a high-swing current mirror ($M_{9,10}$) [44]. All the required bias voltages (V_{1-3}) are generated internally. Finally, it should be noted that the output transistor M_H differs from all the others devices of the ASIC as it can withstand a drain-source voltage up to 7 V, due to thicker gate oxide and poorer doping.

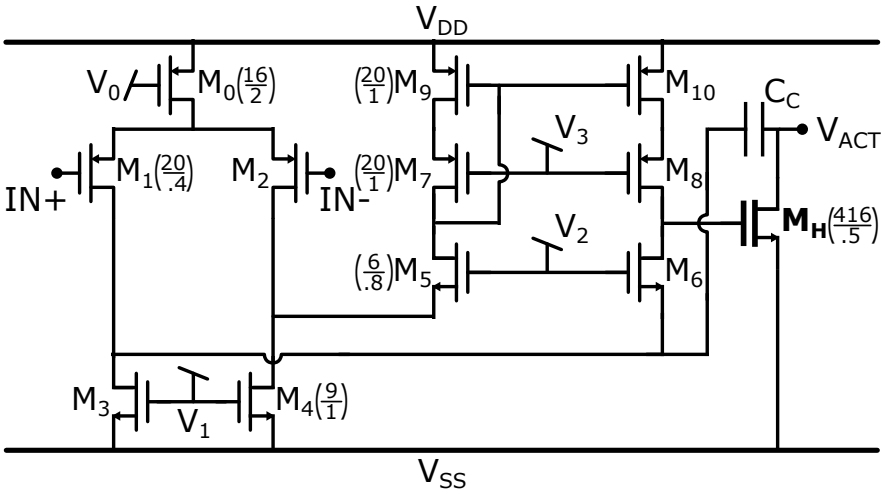


Figure 2.7: *Schematic of the OpAmp employed in the driver stage to control the current flowing in the actuator, which is connected between V_{ACT} and* 6 V. *W/L ratios are expressed in μm.*

2.2 Chip fabrication

The proposed ASIC was fabricated in the AMS OSRAM C35B4 CMOS platform, which showcases a feature size of 350 nm and 4 metal layers. It is indeed a long-established technology node, which has been around for more than 30 years, which however proved suitable for the purposes of the project, eventually suggesting the independence on the selected technology node of an ASIC-based approach. Clearly, there are some very practical reasons related to this choice, namely the reduced fabrication costs, the relatively user-friendly PDK and the availability of the technology on the Europractice platform. However, it is supported also by a system-related motivation, that is the need for high-voltage drivers. In the actuation scheme, in fact, the current driver sustains almost the same current as the heater (up to 15 mA, apart from the small fraction sunk in the feedback resistors of the OpAmp) and a voltage up to 6 V, for a maximum power dissipated by the single MOSFET up to 22.5 mW (when the DAC generates 1 V, which is half of its output full-scale range). The rest of the channel dissipates ≈10 mW, that are partitioned between analog front-end (≈5 mW), digital cir-

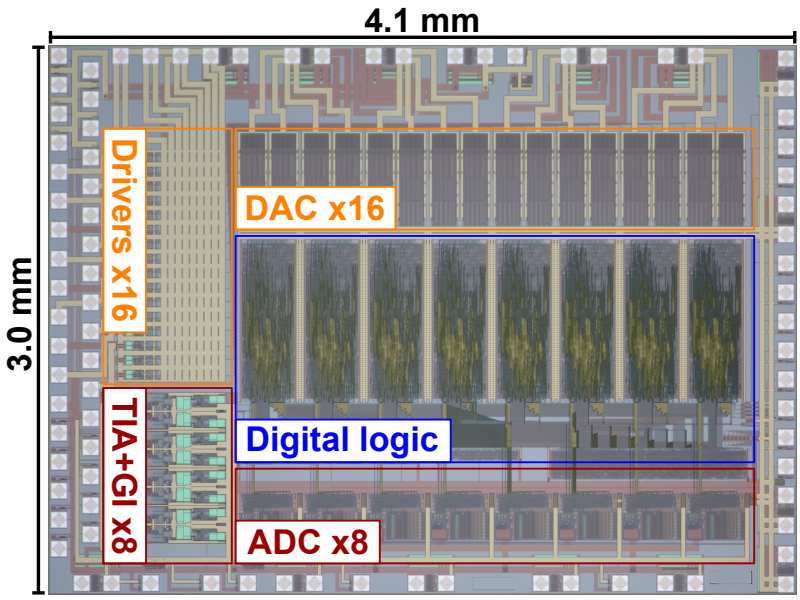


Figure 2.8: *Microscope picture (real colors) of the ASIC.*

cuit (≈1 mW) and DAC and driver OpAmps (≈2 mW). The high-voltage/current constraint ultimately limits the size of the technology node, which can anyway be further shrunk with respect to 350 nm, as it is the case for the ASIC that will be presented in Ch. 5, which was fabricated with a 180 nm feature size. Furthermore, it shall be considered that Silicon Photonics does not follow Moore's Law, for the feature size of its building elements, which is in the order of few hundreds nanometers, to avoid excessive losses should be comparable to the wavelength of the laser that carries the signal inside the waveguide: it thus becomes useless to keep increasing the integration density of the electronic layer once it becomes sufficiently smaller than the photonic counterpart.

Fig. 2.8 shows a microscope picture of the realized ASIC, whose overall area occupation is 12.3 mm^2. The main contributions come from digital circuitry, accounting for ≈31% of the die, routing and, notably, metal pads (95x95 μm^2 each). As it will be discussed in Ch. 5, improving the technology by just two nodes (from 350 nm to 180 nm) significantly reduces the area which is eaten up by registers and combinational logic, and increases the

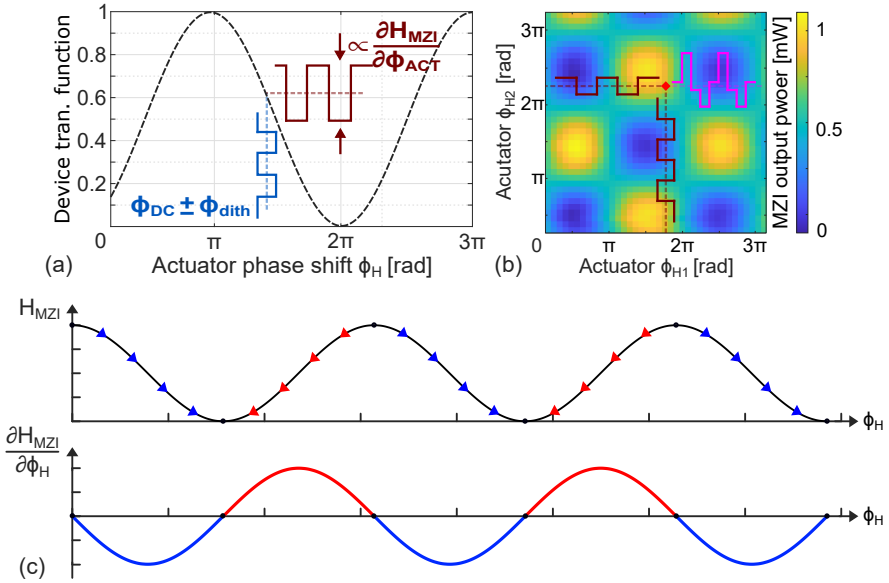


Figure 2.9: *Working principle of the dithering technique to control a Mach-Zehnder Interferometer, visualized* ***(a)*** *in the case of a single actuator/-control variable and* ***(b)*** *for two variables, with orthogonal modulation, as it is the case for MZIs. In both cases, the output modulation is proportional to the (partial) derivative(s) of the transfer function;* ***(c)*** *principle of locking an MZI to stationary points, which is achieved by zeroing the detected dithering output modulation.*

routing density by using additional metal layers. For what concerns the shoreline limitation of the pads, which is nearly met in this design having contacts over its whole perimeter, it will be shown how resorting to a flip-chip assembly, instead of a wire-bonded one, eases the requirement, as pads can be distributed all across the die.

2.3 Working principle of the control loop

Before going into the details of the experiments and the applications enabled by the presented ASIC, it is useful to define a mathematical model of the overall control loop, which comprises both electronic and optical elements.

2.3.1 The dithering technique

As already mentioned, the operation of the integral controller that locks the PIC to a given equilibrium point relies on the so-called *dithering* technique [28]. Such technique, which has been around in the field of communication and computing for more than 80 years, consists in the application of a small signal modulation (so-called *dithering* signal) to the working point of the system. When it comes to photonic integrated circuits, such technique can be effectively adopted within a lock-in-based system to lock each device to a stationary working point of its characteristic, regardless of process variability (e.g. dark currents in the photodetectors), aging and temperature variations affecting the device; in other words, no prior calibration or characterization of the device is required to perform the control action [45]. In fact, provided that the stimulus is sufficiently small, the amplitude of the resulting modulation of the output can be considered proportional to the first partial derivative of the normalized relation $H_{MZI}(\phi_H)$ between the output power and the phase shift induced by a specific actuator, as conceptually shown in Fig. 2.9a. The working principle of the control loop is fundamentally centered around the extraction of the information about $\frac{\partial H_{MZI}}{\partial \phi_H}$: its accumulation along multiple iterations implements the integral controller that effectively locks the system to a stationary point of H_{MZI}, as Fig. 2.9c suggests.

The particular case of a dithering modulation applied to the Mach-Zehnder Interferometer is reported in Fig. 2.9b. As it was described in Ch. 1, the relation $H_{MZI} = P_{OUT}(\phi_{H1,H2})$ is a sinusoidal one, with the phase shifts ϕ_{H1} and ϕ_{H2} being proportional to the thermal dissipation of the resistive actuators. Since there is only one sensor per MZI, the only way to discriminate between the impacts of each actuator and separately extract information about the two first partial derivatives is to apply two orthogonal stimuli. This can be achieved either by using two different frequencies or by applying in phase and quadrature (I/Q) single-frequency modulation; as it is simpler to implement with a digital counter, and having no more than two actuators per device, the I/Q solution was adopted, with a dithering frequency $f_{dith} \approx 8.3\,\text{kHz}$, which can be the same for every MZI of the PIC,

for each channel of the controller acts independently.

2.3.2 Mathematical model of the control loop

In this Section the electronic-photonic system will be described through a mathematical model in order to theoretically evaluate the factors influencing its open loop gain G_{LOOP} and possibly estimating its bandwidth with the help of some measurements. The discussion starts with two useful approximations:

- the photonic device taken into account (a MZI) is strongly non-linear, due to the sinusoidal nature of the $H_{MZI} = P_{OUT}(\phi_{H1,H2})$ relation. As the MZI is one of the constituent blocks of the feedback loop, the non-linearity translates to the system as a whole. However, the ASIC is designed to operate a full steering of the optical power between the two output ports of the MZI; it is thus convenient to linearize its transfer function around one of its minima, deriving a result that can then be compared against the experimental evidence presented in Ch. 4;
- to simplify computations, the effect of a single actuator will be considered; however, thanks to the adoption of orthogonal dithering modulation, the extension to a two-variable system is straightforward, as the effects of the actuators are totally independent and can be measured separately by the lock-in chain.

The control loop, subdivided into its building blocks, is schematized in Fig. 2.10. They can be split into 3 groups:

- the analog read-out stage, that filters, amplifies and converts the current signal I_{PD} generated by the photodiode, first through a TIA (for proper amplification) and then with a Gated Integrator (for filtering before conversion);
- the digital cells that sample, demodulate and accumulate the dithering signal to update the working point of the system;
- the conversion from a digital value to the power P_{ACT} dissipated by the actuators, as well as the following thermo-optical relation between P_{ACT} and the output optical power of the MZI P_{OUT}.

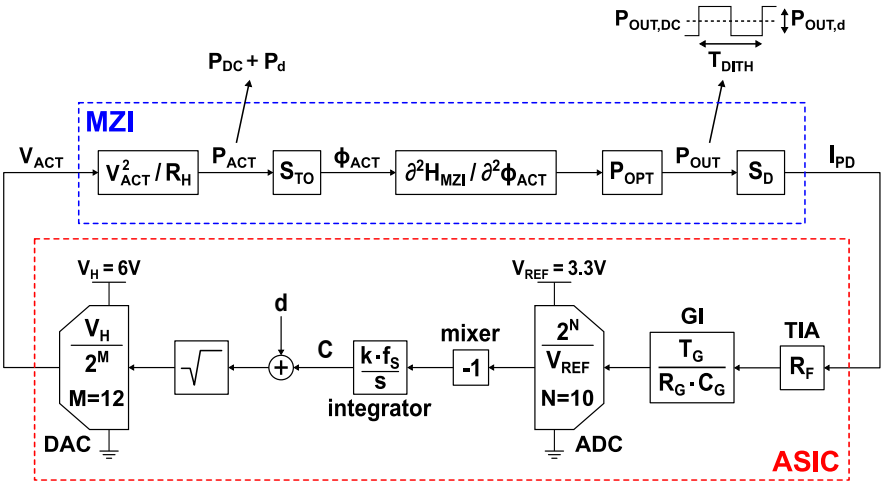


Figure 2.10: *Schematic of the building blocks of the control loop, subdivided into photonic (blue) and electronic (red) elements.*

It is straightforward to schematize the analog stage, as it only contains linear terms. Its overall gain can be expressed as:

$$G_1 = S_D \cdot R_F \cdot \frac{T_G}{C_G R_G} \tag{2.5}$$

where the S_D $\approx$0.85 $\frac{\text{A}}{\text{W}}$ factor expresses the responsivity of the integrated photodiode (PD), as indicated by the PDK of the photonic foundry, R_F is the transimpedance gain of the TIA and $\frac{T_G}{C_G R_G}$ is the amplification undergone by a DC signal when fed to the GI over an integration time window T_G. This latter factor is the same to be applied to the dithering modulation superimposed to the working point of the MZI, as the reset rate of the GI is 12 times faster (f_S =100 kHz) than the dithering frequency. The modulation and the integration window are also synchronized, so that the current in the GI capacitor C_G remains constant across each acquisition; it is in fact reasonable to assume that the time constants of the feedback network in the TIA ($R_F C_F$) and of the GI amplifier are sufficiently faster than the time scale of the dithering integration.

The operations performed at digital level, including the analog-to-digital conversion and the demodulation, have an impact in determining G_{LOOP}, too. First, the analog-to-digital con-

version has to be taken into account, as it introduces a factor $2^N/V_{REF}$, where N is the number of bits of the converter (10 in this design) and V_{REF} is the full-scale range to whom the input sample is compared, corresponding in this project to the power supply of the ASIC $V_{DD} = V_{REF}$ =3.3 V. The following mixer, which is needed to demodulate the digital sequence and extract the value of the dithering modulation, does not modify the magnitude of G_{LOOP}, although it determines its sign. It has to be -1 to guarantee an overall negative feedback that drives the light impinging on the sensing branch of the MZI to a minimum (consequently maximizing the transmission), whereas it causes the locking to a point of maximum of H_{MZI} when it is set to $+1$. For what concerns the accumulator, despite being a discrete-time component its z-domain transfer function can be approximated with the s-domain Laplace transform of a continuous-time integrator:

$$H_\Sigma(s) = H_\Sigma(z)|_{z=e^{s/f_S}} = \frac{k}{z-1}|_{z=e^{s/f_S}} \approx \frac{k \cdot f_S}{s} \tag{2.6}$$

the approximation being possible since f_S =100 kHz is sufficiently larger than the frequency of the signal of interest, which is f_{dith} ≈8.3 kHz. As mentioned when describing the tunable parameters of the controller (Sec. 2.1.2), a user-defined factor k allows to scale the desired bandwidth according to the specific application, for example to equalize the effect of the total optical power involved, which plays a role in determining G_{LOOP}, too. The contribution to G_{LOOP} of the digital circuit can thus be expressed as:

$$G_2(s) = -\frac{2_N}{V_{REF}} \cdot \frac{k \cdot f_S}{s} \tag{2.7}$$

Before information encoding, the dithering modulation d is superimposed to the new bias point C defined by the integrator. In order to make G_{LOOP} insensitive to the particular value of C, a square-root compression is performed, ideally feeding the DAC with the value $\sqrt{C+d}$. The DAC itself, just like the upstream ADC, introduces a conversion factor $V_H/2^M$, where V_H =6 V is the maximum power supply of the heaters and $M = 12$ is the

number of bits of the converter.

At this point, the electro-thermo-optical relation between the actuators and the MZI should be taken into consideration, one that describes the variation of the output power of the MZI P_{OUT} impinging on the PD with respect to a change of the voltage V_{ACT} applied to the actuator. Specifically, focus has to be put into determining the variation of $P_{OUT,d}$, which represents the amplitude of the output power modulation due to the dithering signal. As stated, the phase shift ϕ_{ACT} induced by the actuator in the waveguide can be described as linearly dependent with the temperature variation of the crystal and hence with the power P_{ACT} dissipated by the heater. The linear relation is defined by means of the thermo-optic efficiency S_{TO}, which was measured at around $0.045\,\pi/\mathrm{mW}$, and can be written as:

$$\phi_{ACT} = S_{TO} \cdot P_{ACT} = S_{TO} \cdot \frac{(\sqrt{C+d} \cdot \frac{V_H}{2^M})^2}{R_H} \tag{2.8}$$

Here, it is possible to appreciate the linear dependence of ϕ_{ACT} on the state variable of the system C: noticeably, also the modulation due to the dithering stimulus d is not dependent on the particular working point, something that would occur if no square-root compression was performed. In order to estimate G_{LOOP}, it is necessary to understand how the error signal that has to be zeroed, i.e. the modulation of the output power of the MZI due to the dithering stimulus ($P_{OUT,d}$), changes upon a displacement of the system from the ideal stable equilibrium point. Putting $P_{OUT,d}$ into an expression, the quantity of interest becomes:

$$P_{OUT,d} = \frac{d}{2^{2M}} \cdot \frac{V_H^2}{R_H} \cdot S_{TO} \cdot \frac{\partial H_{MZI}}{\partial \phi_{ACT}}\Big|_{\phi_{ACT}=\phi_{DC}} \cdot P_{OPT} \tag{2.9}$$

where P_{OPT} is the total optical power available at the input of the MZI, to whom G_{LOOP} will be linearly related, as expected (while H_{MZI} is normalized between 0 and 1). Indeed, $P_{OUT,d}$ is also dependent on the particular bias point ϕ_{DC} of the device, as visualized by Fig. 2.11a. All the constant gain terms can be lumped into a single electro-optical coefficient G_{EO} as:

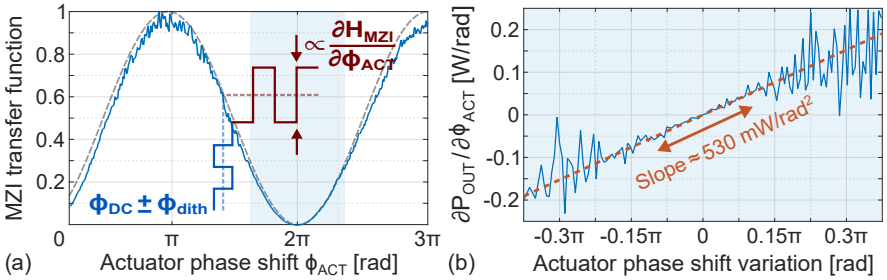


Figure 2.11: ***(a)*** *Visualization of the effect of dithering modulation on a measured MZI transfer function (modulation not to scale) obtained through a DC sweep of a single actuator.* ***(b)*** *Measured first and second derivative of H_{MZI} around a point of minimum. The total optical power is P_{OPT} =230 µW and the dithering modulation is 10 mV wide (0-to-peak).*

$$G_{EO} = \frac{d}{2^{2M}} \cdot \frac{V_H^2}{R_H} \cdot S_{TO} \cdot P_{OPT} \tag{2.10}$$

The factor that determines G_{LOOP}, however, is the variation of $P_{OUT,d}$ upon a variation of ϕ_{ACT}, which can ultimately be written as a third contribution to G_{LOOP}:

$$G_3 = \frac{\partial P_{OUT,d}}{\partial \phi_{ACT}} = G_{EO} \cdot \frac{\partial^2 H_{MZI}}{\partial^2 \phi_{ACT}}\Big|_{\phi_{ACT}=\phi_{DC}} \tag{2.11}$$

The most straightforward way to evaluate the factor $\frac{\partial^2 H_{MZI}}{\partial^2 \phi_{ACT}}$ is to directly measure it experimentally, as it was done in the MZI characterization reported in Fig. 2.11b. Plugging into Eq. 2.11 the values of P_{OPT} and S_{TO}, the resulting value of G_3 is $\approx$530 mW/rad^2. Being a consequence of the device characteristic H_{MZI}, G_3 is independent of the amplitude d of the dithering stimulus, but it is proportional to the total amount of the available optical power as well as to the thermo-optical coefficient of the crystal.

Having accounted for all the contributions to G_{LOOP} around one loop of the electronic-photonic system, the overall expression of loop gain can be written as:

$$G_{LOOP}(s) = G_1 \cdot G_2 \cdot G_3 = \frac{G_0}{s} \tag{2.12}$$

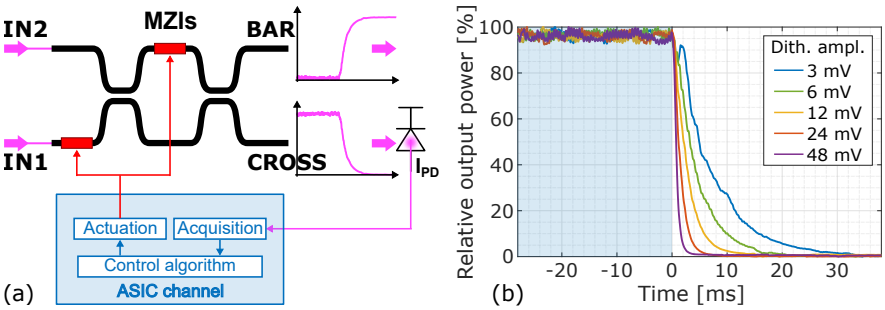


Figure 2.12: ***(a)*** *Experimental setup. Note that light is injected at both input ports of the MZI, meaning that both actuators play a role in determining the interference pattern at the output.* ***(b)*** *Time traces of the optical power measured by a photodiode placed at the cross port of the MZI when activating the control loop (at t=0 ms). After each measurement, the initial working point of the interferometer is reset at the same value, demonstrating the impact of different dithering amplitudes on the transient response. Amplitudes are expressed as peak-to-peak values.*

As expected, lumping all the time-constant contributions to G_{LOOP} into G_0 delivers an integrator-like behavior, ideally with infinite DC gain and a unitary-gain frequency at $f_{0dB} = G_0/2\pi$. As mentioned, there are some parameters that allow to tune such bandwidth, namely the amplitude of the dithering modulation d and the weight k of the samples fed to the accumulator, granting an experimentally measured bandwidth between 10 Hz and 1 kHz. The convergence speed of the system is traded against control accuracy, for a larger bandwidth necessary collects more noise.

Experimental dependence of the loop gain on dithering amplitude

Reported in Fig. 2.12 is a simple experiment that was carried out to estimate the bandwidth of the control loop. A single channel of the ASIC was connected to a Mach-Zehnder interferometer, whose initial working point (t <0 ms) was manually set through the I/O interface of the chip in a balanced state, i.e. 50% splitting ratio between the *cross* and *bar* ports of the device. At t =0 ms the loop is activated in order to focus all the optical power on the *bar* port, consequently minimizing the photogenerated current of the photodiode connected to *cross* port. The measurement was reiterated for 5 different dithering amplitudes: with no surprise, a larger modulation determines a faster con-

vergence time. The 90-10% transient ranges between 1.5 ms and 20 ms, allowing to estimate a time-constant τ of the transient (in the strong approximation of an exponential behavior) between 700 µs and 9 ms, coherent with a bandwidth of few hundreds Hz.

Notice that a peak-to-peak modulation of 48 mV is equivalent to 0.8% of the power supply. Increasing further the dithering modulation improves the bandwidth of the control loop, although at the price of a less precise and stable locking to a stationary point of the MZI transfer function, which may impair the optical performance. In fact, as reported in [28], response time is traded against actuation noise. As it will be shown in Ch. 4, a bandwidth of ≈400 Hz was selected for the optical experimental validation, which is large enough to mitigate environmental perturbations affecting a free-space optical link. The ultimate limit to the bandwidth of the system is indeed the dithering frequency itself, as at least one period of modulation is needed to update the working point of the actuators. In this case, the chosen f_{dith} ≈8.3 kHz offers a good compromise between selectable bandwidth and tracking of the modulation with a relatively slow ADC, on the read-out side.

CHAPTER 3

Characterization of the ASIC

After the description of the ASIC controller in Ch. 2, the results of its electrical characterization are discussed in this chapter. To carry out the experiments, the ASIC was placed on a custom-designed holder PCB, with dedicated lines to inject a tunable current waveform in the read-out and acquire both analog and digital signals. A software interface was also set up for user I/O interaction with the ASIC.

The results were first presented and awarded the Best Student Paper recognition at the 2024 IEEE International Conference on Electronic Circuits and Systems (ICECS, Nancy) [46], and then featured on the aforementioned paper (see Ch. 2) invited and accepted for publication on *The IEEE Open Journal of Circuits and Systems*.

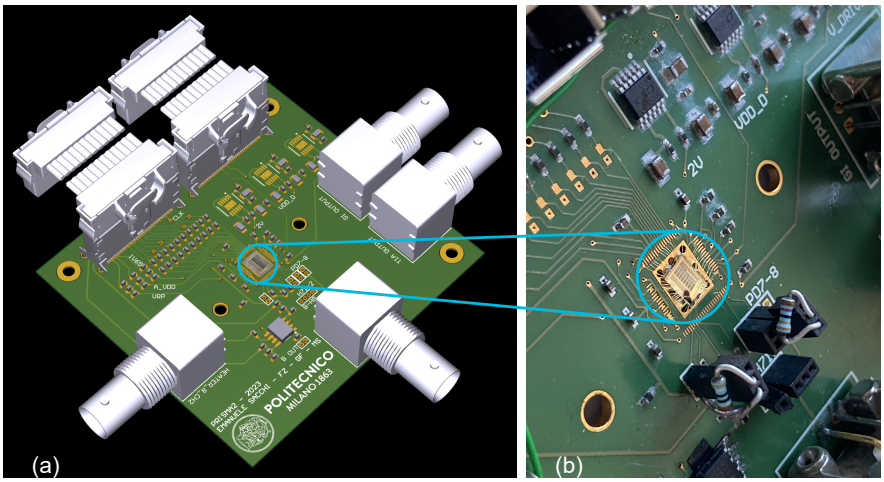


Figure 3.1: ***(a)*** *3D rendering of the test PCB, designed with the help of the EDA tool Altium Designer;* ***(b)*** *close-up picture of the ASIC, connected to the PCB through direct wire-bonding. The trough-hole resistors on the bottom/right corner allow to simulate the thermal actuators (left) and the injected PD current (right).*

3.1 Design of a test PCB

Before assembling the actual electronic-photonic chiplet, a custom-designed PCB holder was fabricated to accommodate only for the ASIC and perform its electrical characterization. The board, which is depicted in Fig. 3.1, has a footprint of 7.5 cm x 8.1 cm, and it is made up of 4 metal layers, with one of them dedicated to ground plane, which is shared between all the components, and two layers hosting signal routing. At its center, the ASIC is glued to an exposed ground pad and connected to the PCB via direct wire-bonding.

Due to the fact that the ASIC implements a fully-integrated mixed-signal controller, comprising sensing and actuating circuits, as well as analog and digital elements, multiple voltages have to be supplied to ensure proper operation. They include:

- one analog power supply, required by the read-out stage and the ADC, and one for the digital circuits. They are both set at 3.3 V, although they are kept separate to avoid disturbance on the analog side due to commutations of the logic ports. There is also another pair of 3.3 V lines, one for the

reference voltage of the ADCs and one serving as the power supply of the drivers stage;

- the reference node of both the TIA and the GI, which is set at mid-point of the power supply (1.65 V);
- a 2 V line used as reference voltage for the DAC.

In addition to the references supplied to the ASIC, there is also a 6 V power line needed for the polarization of the actuators, which happens to be one of the most critical, as each channel of the circuit may require up to 30 mA. Some of these signals (6 V, 3.3 V for analog VDD, 1.65 V) are directly supplied to the ASIC from the motherboard (described in detail in [33]) to which the PCB is connected by means of two shielded cables. The others, including the 3.3 V power supply of the digital circuits and the 2 V reference used for the DACs are generated with the aid of LT3045 low dropout linear regulators (Analog Devices), which receive 5 V at their input pin.

As mentioned in Ch. 2, thanks to the digital I/O serial interface it is possible to monitor the state of the ASIC. The information is encoded within 296 bits (37 bits/channel), and the motherboard that elaborates such information clocks the register at f_{CLK}=1.1 MHz (the same provided to the digital logic of the ASIC), meaning that the state is sampled every ≈270 µs. For characterization purposes, two differential buffers are integrated inside the ASIC to convey the analog output of the TIA and the GI of a single channel to the PCB. A third analog signal, corresponding to the voltage of one heater of the test channel, is directly fed to a SMD buffer (ADA4898-2YRDZ, Analog Devices), as the high actuation voltage (6 V) does not allow an efficient use of integrated buffers. Three BNC cables carry these signals to a high-speed 2.5 GHz Keysight DSO9254A oscilloscope.

There is no photodiode on this PCB. To emulate its behavior, a through-hole resistor was connected to the inverting node of the TIA. A Keysight 81150A waveform generator determines, through a fourth BNC connector, the applied voltage and hence the input current. In a similar fashion, another through-hole 400 Ω resistor is used to mimic the electrical model of the thermal actuators on the PIC. The motherboard that provides the

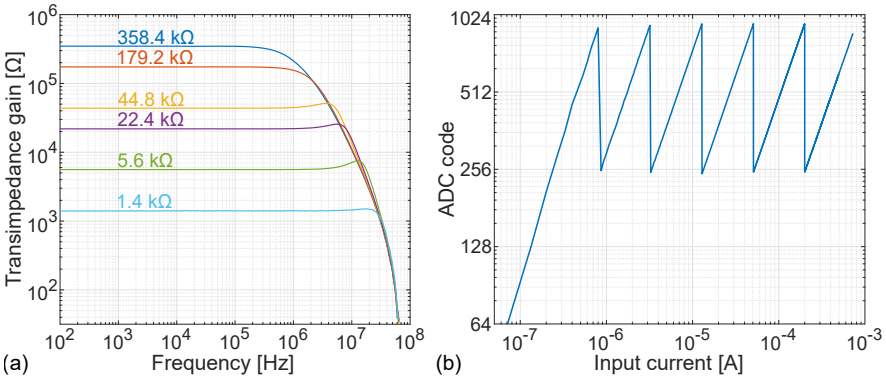


Figure 3.2: *Characterization of the read-out circuit.* ***(a)*** *Frequency response of the TIA, that demonstrates* ≥1 MHz *bandwidth for each one of the six configurations.* ***(b)*** *ADC conversion resulting from an input current sweep between* 850 µA *and* ≤100 nA*. The ADC codes are in logarithmic scale to highlight the effectiveness of the automatic gain adjusting algorithm.*

PCB with the necessary power supplies is controlled by a Xilinx Spartan-6 FPGA. It is also used to clock the ASIC and to compile the firmware that lets the user interact with the chip by means of a graphical interface, displayed on a PC.

3.2 Read-out and DAC validation

Although without any connection to a photonic circuit, it is possible to perform meaningful testing on the ASIC. Specifically, it is possible to measure its interaction with the external world, i.e. characterizing both the read-out and actuation interfaces.

3.2.1 Read-out characterization

To perform the characterization of the read-out circuit, a controlled current was injected in the TIA input node from the waveform generator, thus mimicking the behavior of the photodiode, exploiting a 44 kΩ through-hole resistor. Focus was put on assessing the response of the read-out to input currents ranging over 5 orders of magnitude (from up to 1 mA down to below 100 nA), which can be properly resolved thanks to the automatic gain adaptation described in Sec. 2.1.1. Thanks to the analog

buffer integrated on the ASIC, it was possible to acquire the output of the TIA and perform an AC analysis, which is pictured in Fig. 3.2a. For every possible configuration of the feedback resistive network, a bandwidth larger than 1 MHz is achieved, which is sufficient to amplify without shaping the dithering signal, centered at f_{dith} ≈8.33 kHz. As expected, the local closed-loop bandwidth becomes slower as the value of R_F increases; for what concerns stability, the most critical configuration is the one with R_F =5.5 kΩ, which nevertheless guarantees a phase margin ϕ_M =75.7° (3σ interval is ±5.2°, from Montecarlo simulations).

Fig. 3.2b, instead, details the results of the ADC conversion, acquired through the serial I/O interface of the ASIC, when sweeping the input PD current over a dynamic range of more than 50 dB, between 850 µA (equivalent to 1 mW optical power impinging on the photodiode) to less than 100 nA, which roughly corresponds to the estimated dark current of the detectors. The automatic reconfiguration of the transimpedance network can be appreciated thanks to the (unusual) logarithmic scale of the ADC samples: the input current range is divided in six regions, each one occupying a portion which is 4 times larger than the previous one. Since the read-out amplification is scaled of the same factor, the slope of the trace appears to be constant on log scale. With the largest value of R_F, which is used for input currents up to 850 nA (1 µW of optical power), the stage resolves an LSB as small as −60 dB, well below the minimum declared value of the dark current (which can be as low as −48 dBm). The digital thresholds for the gain switching algorithm have to be selected with some hysteresis margin, so that the system does not oscillate between two adjacent configurations, if settled around a switching point: once the upper threshold V_T^{UP} is set, it is sufficient to set a lower threshold $V_T^{LOW} < \frac{V_T^{UP}}{4}$ to avoid switching on every sample.

As anticipated in Sec. 2.1.1, the converter is a 10-bit SAR (Successive Approximation Register) which is provided by the foundry PDK, with a declared 9.4-bit ENOB (Effective Number of Bits) and a DNL of of ±0.3LSB, when operated with a 3.3 V reference and at a sampling frequency f_S =100 kHz, which is well beyond the Nyquist frequency of the signal of interest, as $f_S = 12 \cdot f_{dith}$.

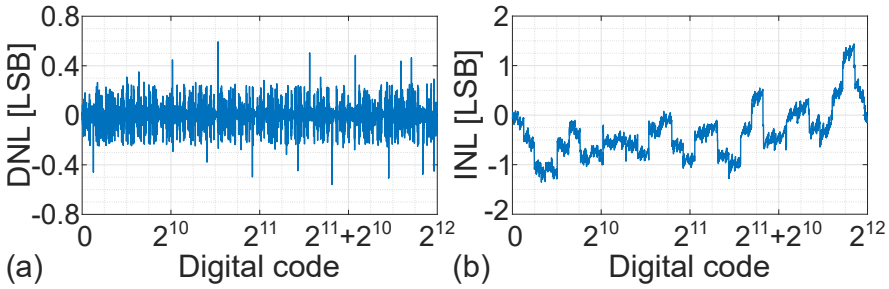


Figure 3.3: *Characterization of the DAC by measuring its* ***(a)*** *differential and* ***(b)*** *integral non-linearities. While the latter is almost irrelevant in a lock-in scheme, the former critically has to be kept below 1 LSB.*

3.2.2 Actuation scheme characterization

The actuation circuit was characterized, too, with the goal of quantifying the DAC non-linearities. To perform the measurement, the input code of the converter was swept by means of the I/O interface of the ASIC, eventually disabling the square-root operator. As discussed in Sec. 2.1.3, the most critical non-linearity is the differential one (DNL), which has to be kept below 1 LSB in order to ensure monotonic behavior. Such constraint is satisfied, as shown by the result of the characterization reported in Fig. 3.3a. The requirement on the integral non-linearity (INL), instead, is less stringent, due to the general lock-in mechanism that the ASIC implements; in fact, since the control algorithm relies on the dithering technique, the most critical parameter is the difference in the output values corresponding to input codes that are close to each other, rather than their actual translation. That is why, as Fig. 3.3b shows, in this design it is acceptable to have some codes that differ from their ideal output by more than 1 LSB.

3.3 Square-root algorithm validation

The square-root approximating algorithm described in Sec. 2.1.2 was eventually put to the test to perform a DC characterization of a single Mach-Zehnder Interferometer. Such operation is made possible by deactivating the closed-loop algorithm, in order to keep the voltage applied to each actuator fixed. A digital

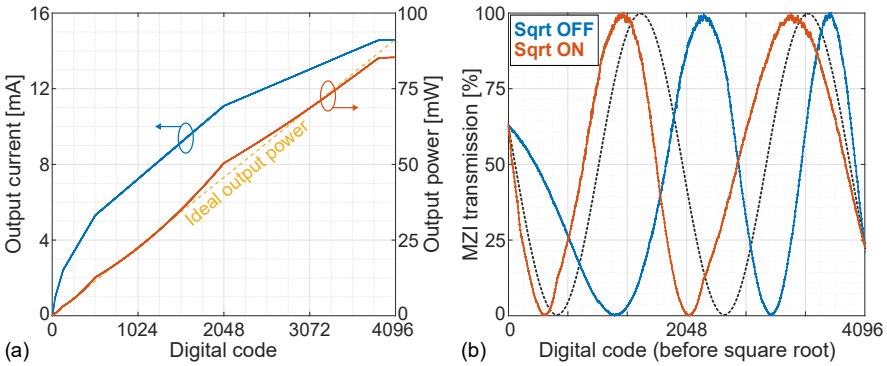


Figure 3.4: ***(a)*** *Measurement of the distorting effect of the square-root algorithm on the output current driven into the thermal actuator (blue) and effective output power dissipated by the device (red), compared with an ideal linear characteristic (dashed);* ***(b)*** *effect of a voltage sweep of a single actuator on the output optical power of the MZI, with (red) and without (blue) performing square-root pre-distortion at digital level, compared against an ideal sinusoid (black).*

ramp, which is fed from the user to the DAC by means of the shift registers described in Sec. 2.1.2, allows to sweep its current from 0 to ≈15 mA. Fig. 3.4a details the results of such sweeps on the actuator. The current flowing in the resistor, which is directly proportional to the 12-bit input code of the DAC, is effectively pre-distorted by the square-root algorithm; as a result, a linearization is produced in the delivered output power (and hence in the induced phase shift). The points where the piecewise approximation changes slope correspond to those where the maximum displacement from the ideal line occurs. A clipping is present at high voltages (V_{ACT} closer than 120 mV to the V_H =6 V power supply), due to the power n-type MOSFET going into ohmic region.

Fig. 3.4b reports instead the results of a double characterization of a Mach-Zehnder Interferometer. To this purpose, the ASIC was connected to an 8-channel binary-tree mesh (the setup will be described in Ch. 4), with 15 heaters kept at fixed voltage and one, belonging to a MZI connected to an external photodiode, being swept from 0 to 6 V. Regarding the red trace, it is possible to appreciate the mitigating effect of the square-root compression, which is way more adherent to the ideal sinusoidal

transfer function (dashed trace). The blue trace is obtained by repeating the measurement while disabling that portion of the algorithm: it is clear that, in this case, the properties of G_{LOOP} change according to the working point, with the derivatives of H_{MZI} progressively increasing in module with the voltage applied to the actuator. Obviously, the overall transmission is the same when the DAC receives as input either the minimum or the maximum possible 12-bit code. Taking into account that the nominal resistance of the integrated thermal actuators is $R_H \approx 400\,\Omega$ with a power supply of $V_H = 6\,\mathrm{V}$, the maximum power dissipated by the heater is $P_H = \frac{V_H^2}{R_H} \approx 90\,\mathrm{mW}$. This allows to experimentally determine the thermo-optic efficiency S_{TO} of the device: since the full actuator sweep covers a $\Delta_{\phi_{MAX}} \approx 4\pi$ phase shift, the coefficient can be estimated as $S_{TO} = \frac{\Delta_{\phi_{MAX}}}{P_H} \approx 0.045\,\pi/\mathrm{mW}$, which is the value adopted for calculations about the loop gain done in Sec. 2.3.2.

CHAPTER 4

ASIC-PIC chiplet experimental validation

This Chapter initially discusses the applications, advantages and drawbacks of free-space optical links, towards whom this research is mainly oriented, although not limited to.

In the following, the Chapter details the results achieved in optical experiments after the ASIC was connected to actual photonic integrated circuits. A proof of concept of the simultaneous reconfiguration of multiple photonic devices is first provided; in the following, a thorough validation is conducted by controlling a 16-channel binary-tree mesh of interferometers by means of two identical and cooperating ASICs.

The results were presented at various international conferences dedicated to optical communications [47, 48]. They were also extensively described in a journal paper published in *Light: Science & Applications* [36].

4.1 Applications of Free-Space Optical communications

In the experiments that will be shown in the following, the ASIC has been primarily employed in applications where the PIC has to be dynamically reconfigured to establish reliable free-space optical (FSO) links. A direct descendant of RF mm-wave communication, this wireless solution offers several advantages, namely large bandwidth (hundreds of GHz) in an unlicensed frequency spectrum, low-latency and cost-effectiveness [49]. The applications of the technology mainly cover point-to-point connections, due to the high focusing of the optical beam compared to RF waves, and their range spans over several orders of magnitude, from few meters (e.g. data centers or urban links [50]) to hundreds of kilometers in case of satellite communications [51].

In addition to unavoidable beam divergence over long distances, a major obstacle to establishing reliable FSO links comes from weather conditions, which may limit coupling between free-space propagation and fiber. In the experiments that will be shown, it will be demonstrated how it is possible to dynamically adapt the configuration of a PIC to a time-varying distorted wavefront in order to maximize signal recovery, eventually providing a scalable solution to mitigate the otherwise unresolved problem of atmospheric turbulence [52].

4.1.1 Self-aligning universal beam coupler

A well-known example of a PIC that is employed in FSO and whose operation is fundamentally enabled by the integration within its architecture of an electronic control layer is the so-called self-aligning universal beam coupler [53], which is typically used to couple an arbitrary monochromatic input beam to a single-mode waveguide. Generally speaking, it consists of a series of blocks, each one containing a phase manipulator, a tunable beam-splitter and a detector; they can thus be sequentially driven to determine an interference pattern that collimates all the light shined on such array to a single output. Due to the sequential nature of the coupler, no complex multi-variable optimization of the matrix is required; instead, independent local control loops are sufficient to adjust, one by one, each block, up to the point of envisioning a system where a single controller is

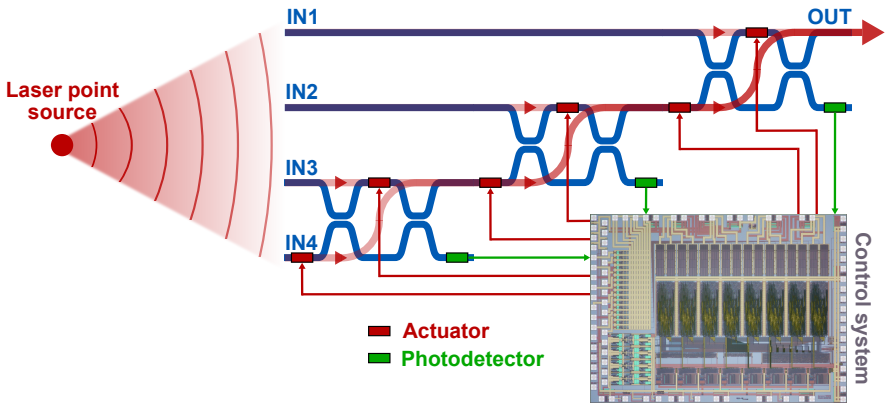


Figure 4.1: *Schematic of a 4-channels self-aligning beam coupler. Each element of the circuit is part of an independent control loop: once it is properly tuned, no light ideally impinges on the photodetector and no residual modulation is transmitted to the devices located downstream.*

routinely multiplexed across the elements of the mesh (although at the price of slower response) [54].

This kind of architecture is indeed suitable for implementation on a silicon photonics platform as a matrix of Mach-Zehnder Interferometers arranged in mesh configuration [12], as the schematic representation of Fig. 4.1 suggests: the waveguide structure of the MZI works as a beam splitter, whose working point is sensed by an integrated detector (not necessarily a photodiode), elaborated by a dedicated control system and updated by means of two thermal actuators that serve as phase shifters (although, as discussed in Ch. 1, non-thermal devices are also available). The possible applications of this PIC in the field of FSO are straightforward, as it substantially enables all-optical signal reconstruction after the beam is spatially sampled by the grating coupler (GC). This involves compensating, through the action of the phase shifters, for misalignment and defocusing of the input beam and generally for any perturbation that may alter the input phase-front. Consequently, it can be used also to track moving sources, as well as in sensing experiments whenever a phase-shifting object is placed between the light source and the PIC; to this scope, the measurement is performed by keeping trace of the state of the system, which is represented by the set of the commands applied to the actuators.

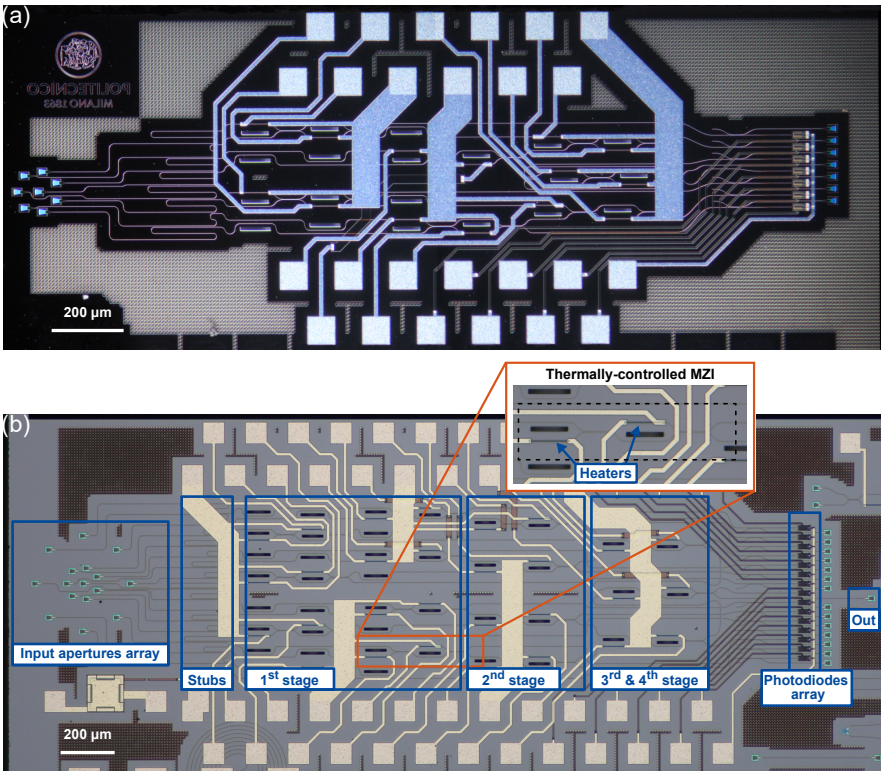


Figure 4.2: *(a) Dark and (b) bright field microscope pictures of a 8- and 16-channels binary-tree beam coupler, respectively, which were both used for experiments. In circuit (b), the various stages of the PIC are also detailed, with a close-up on a single thermally-controlled MZI.*

Finally, the beam-coupler architecture could extend its operations also to non-monochromatic beams, e.g. those carrying multiple orthogonal modes [55]. To operate, they require transparent detectors in order to perform arbitrary all-optical signal routing. An ASIC-PIC architecture that allows such extension will be proposed and discussed in Ch. 6.

4.2 PIC design and fabrication

As anticipated, the ASIC controller was tested for real time control of universal beam couplers, either with 8 or 16 input apertures. The microscope pictures of the selected PICs are shown in Fig. 4.2. They were both manufactured onto the same die by

a commercial photonic foundry (Advanced Micro Foundry, Singapore) on a standard 220 nm Silicon Photonics platform, which includes into its PDK the possibility to integrate metallic thermal actuators and germanium photodiodes, and route the electrical components with two metal layers, the top one being exposed.

Concerning the PICs, it is useful to consider the one in Fig. 4.2b, which is more complex (and obviously larger, with a footprint of 3.2 mm x 1.3 mm), and split it into its building blocks. It is essentially composed by 15 thermally-tunable Mach-Zehnder Interferometers, arranged to form a binary-tree mesh that can be grouped into 4 sequential stages. Differently from other topologies [56], such configuration equalizes the lengths of all possible optical paths within the PIC from input to output, also thanks to the insertion of stubs between the OAA and the proper mesh; the binary structure also minimizes the required number of stages. At the input, a 16-apertures OAA spatially samples the impinging beam. It is composed by 16 GCs, placed on two concentric rings with 60 µm (inner, 7 GCs) and 180 µm (outer, 8 GCs) radius, encircling a central aperture. Such structure is effectively optimized to receive linearly-polarized light (TE in this case) with circular beam spot, although other topologies can be envisioned [57]. Each GC is ≈23 µm wide and 48 µm long (considering also a 24 µm long taper). As stated in Sec. 4.3, the beam is projected onto the OAA with a 12° angle from the perpendicular to the surface, which corresponds to the elevation angle of the GCs radiated field; azimuth angle is 0°, while the divergence is 5.6° x 9.8°: all these factors contribute to the overall coupling loss of each GC, roughly 4.5 dB. In case of FSO beams, though, an additional ≈20 dB geometric loss has to be accounted for due to the limited fill factor of the OAA.

The 15 Mach-Zehnder Interferometers are implemented with a pair of 3 dB directional couplers, as shown in the inset of Fig. 4.2b. To achieve full control of the output interference pattern, the two TiN thermal tuners are integrated on top of the MZI waveguides, one on an input branch and the other on the internal arm, as shown in Fig. 4.3. When swept in order to generate at least a 2π phase shift between the MZI arms, they achieve an extinction ratio at the output ports of the interferometer around 30 dB. Coherently with the measurements shown in Sec. 3.3, the

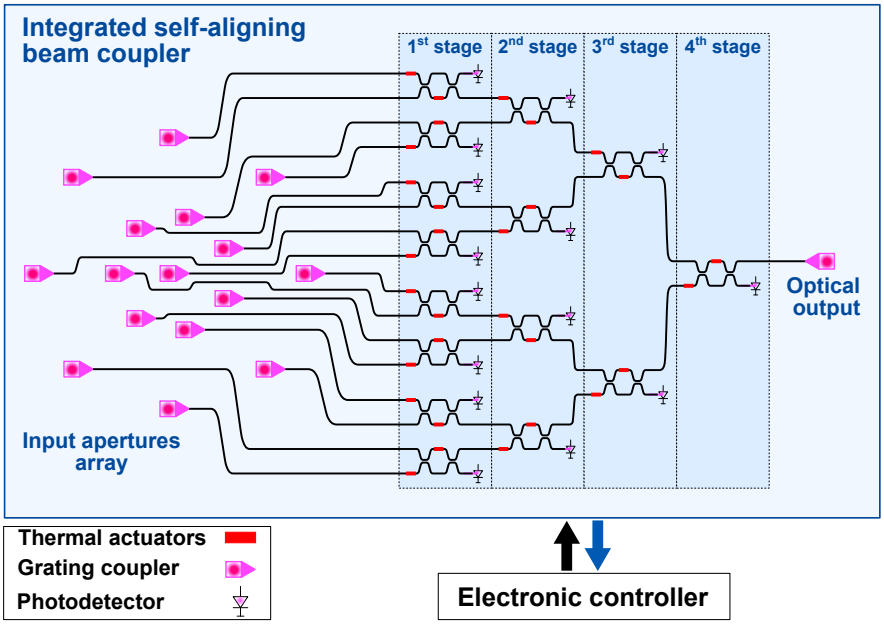


Figure 4.3: *Schematic of a 16-channels self-aligning universal beam coupler*

thermal efficiency of the heaters is $\approx 22\,\mathrm{mW}/\pi$ (i.e. S_{TO}^{-1}), which corresponds to an overall $\approx 4\pi$ phase shift when the heater is swept between 0 and 6 V. Heaters are also responsible for the ultimate upper limit to the system dynamics, as a consequence of their thermal time response, which is in the order of 10 µs.

Despite being composed of MZIs, which are known for being poorly selective to radiation wavelength, the PIC can operate only between 1535 nm and 1570 nm. This is mainly due to the sensitivity of the input GCs; an optimization of the grating couplers for broadband operation [58] would allow simultaneous reception of multiple wavelength-division-multiplexed (WDM) channels, effectively scaling the capacity of the FSO link.

Tab. 4.1 lists all the parameters of the optical components.

4.3 Experimental setup

To perform meaningful system-level experiments without deploying cumbersome building-to-building links, a laboratory setup was built in order to recreate behind closed-doors an equivalent

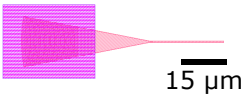
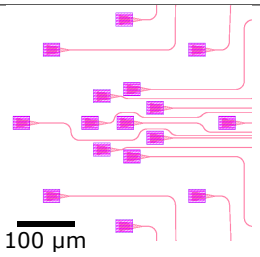
Device	Layout	Main features
Waveguide (WG) and thermal phase shifter (PS)		WG propagation loss: ≈1 dB/cm PS: TiN heater, 80 µm x 20 µm PS response time: ≈10 µs
Mach-Zehnder Interferometer (MZI) with 2 phase shifters		Directional coupler (DC) gap: 300 nm DC length: 40 µm MZI extinction ratio: ≈30 dB PS efficiency: ≈ 25 mW/π
Grating coupler		Polarization: TE Beam width: 5° x 9° (HPBW) Tilt angle: 12° Aperture size: 29.2 µm x 19.3 µm
Input optical antenna array (OAA)		# of apertures: 16 Inner aperture radius: 60 µm Outer aperture radius: 180 µm

Table 4.1: *List of the main photonic building blocks employed in the integrated photonic processor and their relevant characteristics.*

outdoor optical free-space link of hundreds of meters, similar to the one described in [59].

A detailed schematic of the setup, alongside a picture of the indoor arrangement on an optical bench, is represented in Fig. 4.4. All the experiments were performed using a laser source at λ =1550 nm, a typical wavelength for Si-based fibers and waveguides due to the limited losses of the semiconductor in such near-infrared wavelength (≈1 dB/cm in a waveguide). Both the source and the modulator are incorporated into the same instrument, the ID Photonics IQ Optical Multi-Format Transmitter. The 25 Gbaud RF signal superimposed to the carrier, either with on-

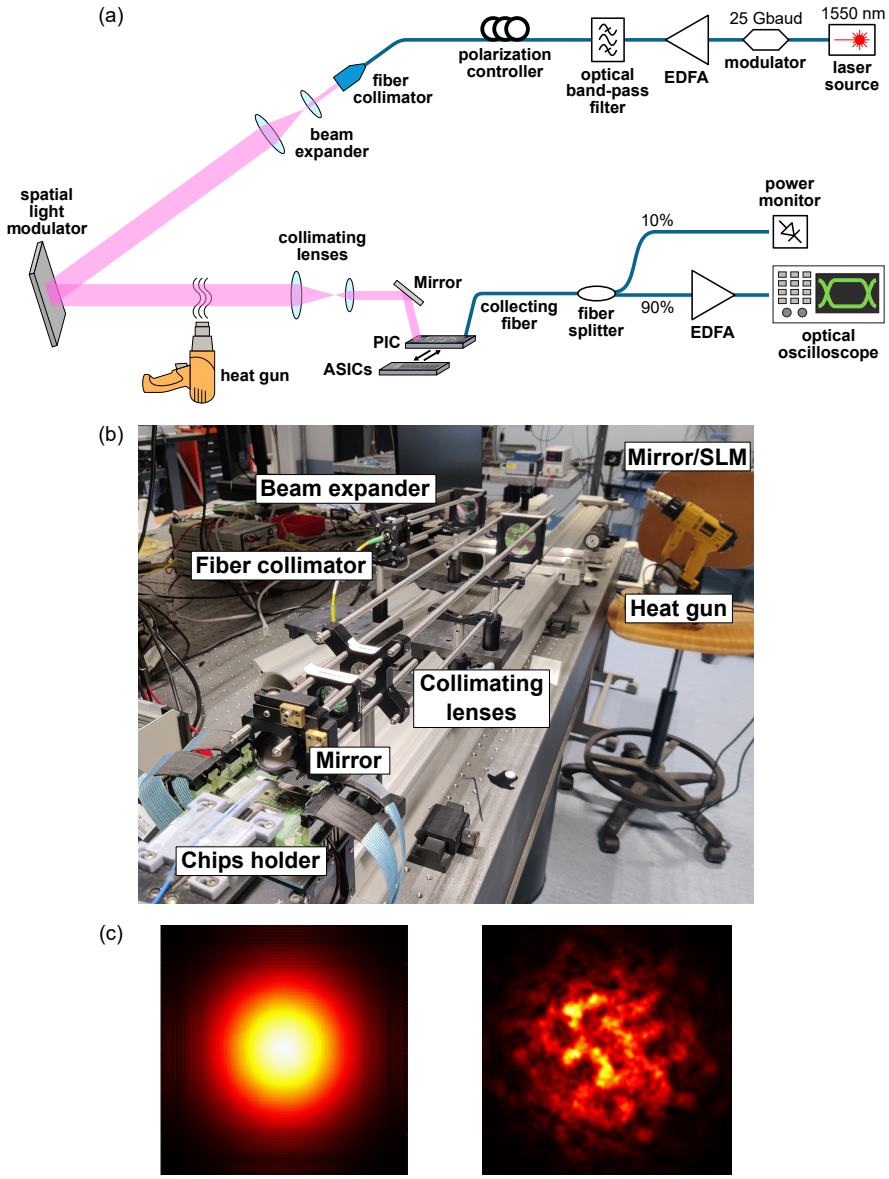


Figure 4.4: ***(a)*** *Full scheme of the laboratory setup used to perform FSO experiment. The modulator operates either with PAM-2 (25 Gbit/s) or PAM-4 (50 Gbit/s); when turned off, the SLM is a passive mirror; the fiber collecting light at the output of the PIC is suspended, not glued, above the chip, causing additional coupling losses;* ***(b)*** *picture of the setup, mounted on an optical bench, from fiber collimator to the ASIC-PIC system;* ***(c)*** *free-space beam at the beginning (left) and at the end (right) of the propagation, with turbulence being injected across the path.*

off keying (OOK) or 4-level pulse amplitude modulation (PAM-4), are generated by the ML4039EN BERT (Multilane). Before being emitted into free-space, the beam is amplified by an erbium-doped fiber amplifier (EDFA EAD-1K-C, IPG Photonics), which eventually injects into the fiber collimator up to 25 dBm. Such an amplification is needed to compensate for the insertion loss of the upstream modulator and, downstream, both the coupling losses between the FSO beam and the input Optical Antenna Array (OAA) of the PIC and between the output waveguide and the collecting fiber. Before collimating the beam from fiber to free-space, a dedicated rejection filter is used to suppress the amplified emission noise (ASE, with -3 dB bandwidth at 0.25 nm distance from carrier wavelength), while a fiber polarization controller aligns the polarization of the beam with the transverse electric (TE) mode guided by the 2D array of grating couplers at the input of the chip.

Concerning free-space propagation, the beam at the output of the collimator is sent through an expander, composed by a biconcave and a biconvex lens (LD2060-C and LB1630-C, respectively), with a magnification of 6.6. This translates into a beam waist of 5 cm at 3 meters distance from the lenses. As shown in Fig. 4.4b, the beam path is folded: to reflect light, a spatial light modulator (SLM) is placed half way through, also offering the possibility of locally altering the phase front of the beam. The mirror can also be used to steer the beam towards a near-infrared (NIR) camera (Xenics Bobcat 640) for turbulence characterization and monitoring purposes, as shown in Fig. 4.4c. In order to generate also dynamic turbulence, a heat gun is pointed perpendicularly to the beam path: in this case, the optical link is perturbed twice, due to the folded geometry of the setup, while the SLM is left off and used as a passive mirror. There are numerous parameters that can be tuned in order to modulate the introduced turbulence, such as gun position, speed and temperature, as well as the phase mask of the SLM. Turbulence strength ranged from an effective index parameter C_n^2 of 10^{-14} $\mathrm{m}^{-2/3}$ up to 10^{-10} $\mathrm{m}^{-2/3}$, corresponding to an equivalent free-space propagation distance of few hundreds meters; in the results that will be shown in Sec. 4.5 and 4.5.1, the value of C_n^2 was in the order of 10^{-12} $\mathrm{m}^{-2/3}$, with negligible wander effect due to the limited

beam size and optical link length.

In the final part of the FSO link, light is focused onto the PIC by a second pair of lenses (LB1889-C with f=250 and LD2060-C with f=-15), that shrink the beam in order to match its spot size with the diameter of the input OAA (360 µm); a mirror is also needed to optimize the incident angle of the beam, corresponding to 12° deviation from the normal to the chip surface. At the other end of the PIC, a single-mode fiber is suspended on top of the output GC, and can be freely moved by means of a 3-axis micro-positioner. To keep track of the system state and characterize the dynamics of the turbulence, a fiber splitter steers 10% of the collected light towards a bench-top photodetector (HP 81521B); the remaining 90% of power is sent to an EDFA (Amionics EDFA-PA-35-B-FA), that matches the signal dynamic range with that of the high-speed optical oscilloscope (Tektronix, DPO75002SX) and evaluates the transmission performance in terms of eye-diagrams and bit-error-rate (BER).

The overall losses along the beam path, which can be larger than 30 dB, break down as follows:

- propagation through free space is considered lossless, provided the the beam radius is smaller than the lens used to focus it onto the PIC;

- when coupled to optical fiber, each GC is responsible for a ≈4.5 dB loss, that sums up to 9 dB considering both the input and the output GCs. Coupling efficiency can be effectively improved by adding an array of lenslets at the chip input, which can be custom-designed and fabricated by means of 3D-printing techniques [60], or by engineering the material of the cladding surrounding the couplers [61];

- a geometrical loss of ≈20 dB is present due to the limited fill factor of the OAA that samples the input beam - another factor that advocates for the adoption of scalable controller architectures, which make possible to increase the number of channels and hence of apertures;

- finally, a ≈2 dB on-chip loss is inevitably present due to photon absorption in the waveguides.

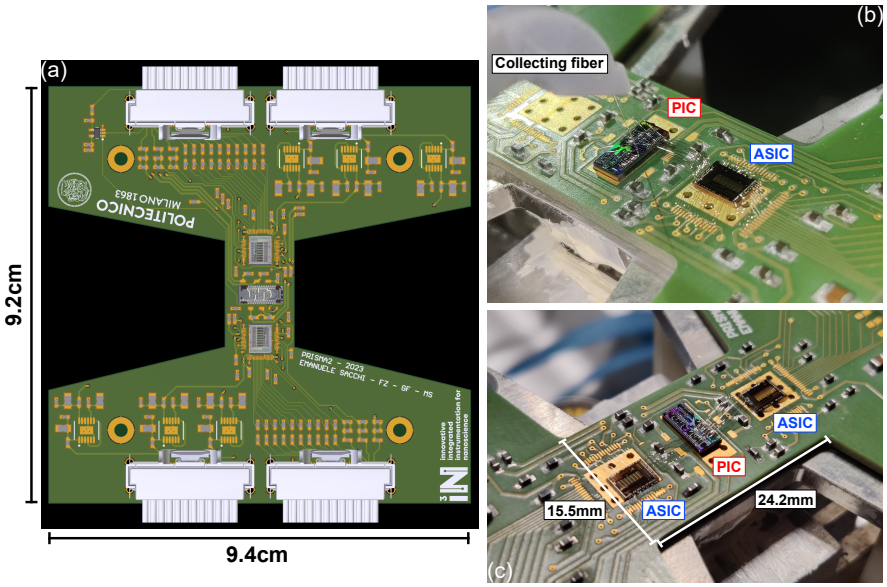


Figure 4.5: ***(a)*** *3D rendering of the custom-holder PCB, with the peculiar "butterfly" shape that makes space for a possible fiber-PIC coupler; there is room to accommodate two ASICs on the sides of the PIC;* ***(b)*** *close-up picture of the electronic-photonic chiplet, with two ASICs connected to a 15-interferometers silicon photonics matrix through direct wire-bonding.*

All this losses being taken into consideration, laser source power is usually set between 0 and 5 dBm.

4.3.1 Custom-holder PCB and ASIC-PIC chiplet

Similarly to what has been done to perform the electrical characterization of the ASIC, a custom-designed holder PCB was also fabricated to allow electrical routing of all the necessary signals for proper controller operation. As shown in Fig. 4.5a, the board is built upon a radially symmetric structure, centered around the PIC, and can host either one (Fig. 4.5b) or two (Fig. 4.5c) electronic controllers to access up to 16 photonic devices. In addition to the signals and power lines needed by the ASIC, the PIC is also provided with 5 pads, carrying up to 100 mA each, that deliver power supply to up to 32 integrated thermal actuators (two heaters per MZI).

The peculiar, butterfly-like shape of the PCB is meant to accommodate, if necessary, an optical fiber holder. It was screwed

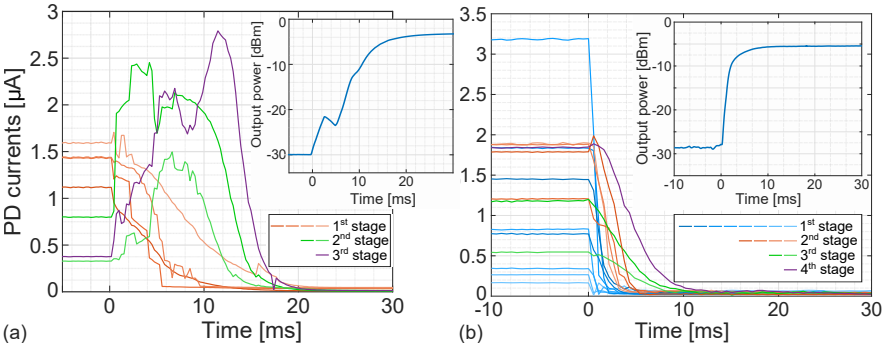


Figure 4.6: *Measured photodiode currents during PIC reconfiguration starting from a random working point.* ***(a)*** *refers to an 8-channels beam coupler, while* ***(b)*** *shows the results obtained with a 16-channels one. The two insets show the powers at the output of the PICs, as collected by a fiber and detected by an external photodiode.*

onto a 3D-modeled mechanical steel body, in order to prevent it from bending, and then placed on top of a thermo-electric cooler (TEC), that monitors and stabilizes the temperature of the chiplet thanks to a 10 kΩ thermistor, soldered close to the ASIC-PIC assembly.

4.4 Simultaneous reconfiguration of multi-channel PICs

The most intuitive and straightforward assessment of the effectiveness of the ASIC controller is measuring the convergence time of the algorithm. To this purpose, all the actuators were initially set to a random working point, far from the optimal configuration that maximizes the optical power conveyed to the output collecting fiber. At time $t = 0$ ms, all the channels were activated simultaneously to perform power minimization on the respective photodetector, consequently maximizing the output power on the other output port of each MZI.

4.4.1 Proof-of-concept on an 8-channels mesh

A first proof-of-concept experiment was carried out by connecting a single ASIC to an 8-apertures, 7-MZIs binary-tree mesh, the results being reported in Fig. 4.6a. It is possible to appreciate that the power impinging on every PDs is minimized within no

more than 20 ms. Within the photonic devices, those belonging to the first stage, i.e. those directly connected to the input OAA, are properly configured in ≈10 ms; the following MZIs, instead, despite being controlled simultaneously to the input ones, require a longer transient, as they have to wait for the optimization of the devices upstream: the consequence of this cascaded topology is the overshoot which is present in the transient responses of the 2nd and 3rd stage. The downstream propagation of the modulation process of each stage is also evident through the non-monotonic behavior of the output power of the PIC, portrayed in the inset of Fig. 4.6a. Differing from other sensing designs [23], this PIC does not allow any sensing of the phase of the impinging radiation: the intensity of this effect cannot thus be predicted and may change (or even disappear) between subsequent experiments.

4.4.2 Extension to a 15-channels mesh

As stated, a striking advantage of a chiplet-based approach to the implementation of electronic-photonic systems, compared to discrete components-based solutions, is the scalability of the control layer. The effectiveness of this advantage is demonstrated in Fig. 4.6b. Here, two nominally identical ASICs were wire-bonded to a 16-apertures, 15-MZIs binary-tree mesh serving as a beam coupler. By finely tuning the parameters of the control loop (namely dithering frequency and amplitude), some traces may achieve a convergence time as low as 1.5 ms, with the whole system reaching optimal configuration within ≈10 ms. Noticeably, the dithering frequency f_{dith} is the same for all the channels of both ASICs, approximately 8.3 kHz, yet it does not hinder the configuration of the PIC: once the MZIs of the Nth stage are properly locked to a stationary point of their transfer function, no output modulation will propagate to the $(N+1)^{th}$ stage. It is also worth pointing out that the two ASICs are fed by the board a unique clock signal at f_{CLK}=1.1 MHz. Noticeably, the transient response of this larger PIC is faster compared to the 8-devices mesh. First of all, this can be explained with a better tuning of the circuit parameters, the most relevant being the dithering amplitude; second, in the experiment of Fig. 4.6b a larger amount of optical power per device is available (≈1.48 µW per device against ≈0.95 µW in the measurement of Fig. 4.6a), making the characteristic $P_{OUT}(\phi_{H1}, \phi_{H2})$

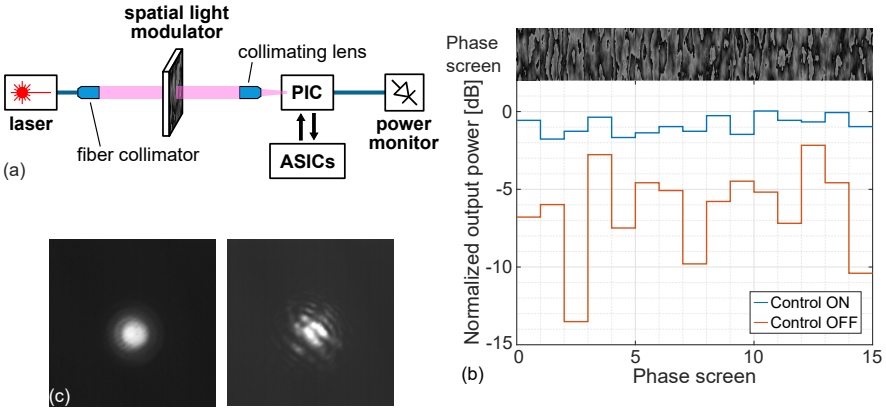


Figure 4.7: ***(a)*** *Simplified schematic of the experimental setup, with the spatial light modulator (SLM) placed at the half point of the FSO path to arbitrarily alter the phase profile of the beam;* ***(b)*** *collected optical power at the output of the PIC across a sequence of 15 different configurations of the SLM, with (blue) and without (red) activating the ASIC controllers;* ***(c)*** *beam spot, observed with an infrared camera, without (left) and with (right) the distortion introduced by the SLM.*

relation of the MZI steeper and hence amplifying the extracted dithering signal, which ultimately translates into a faster convergence.

As a matter of fact, for obvious scientific motivations all the experiments that will follow have been conducted using this 16-channels optical processor.

4.5 Compensation of static wavefront distortions

The experiments presented so far have been conducted without adding any distortion to the propagation of the beam. With respect to the setup described in Sec. 4.3, the heat gun was left off, as well as the spatial light modulator, which ultimately served as a passive mirror that folded the optical path.

A further assessment of the performance of the ASIC controller can be performed by using the beam coupler to track wavefront distortions, which are arbitrarily introduced with a predetermined and controlled profile by the SLM according to the experimental setup schematized in Fig. 4.7a. As shown in Fig. 4.7b, a sequence of 15 synthetic phase masks was generated

to induce reconfiguration of the receiver upon an abrupt modification of the impinging Gaussian beam spot, whose shape can be preemptively monitored with an infra-red camera, as highlighted in Fig. 4.7c, both before (left) and after (right) the distortion operated by the SLM. The experiment was conducted in three steps, repeated for every mask of the sequence:

- first, the PIC is configured by the ASICs for optimal signal reconstruction in case of a "white" mask (i.e. with no additional distortion);
- second, the SLM is turned on and the output power monitored while holding all heaters voltages stationary, in the condition reached with the SLM off;
- finally, the control loop is activated so that the ASICs steer each MZI of the mesh towards a new working point for which measured signal integrity is restored.

Fig. 4.7b reports the measured power at the output of the PIC, normalized to the best possible scenario, i.e. with the SLM left off. When no control is performed on the beam coupler, the received power is, on average, 5.7 dB lower than the ideal case, with standard deviation 2.9 dB and 3 SLM configurations where $\approx 90\%$ or more of the power is lost. Conversely, when the controllers are activated, the beam coupler is always automatically reconfigured to recover the signal, averaging an output power which is only 0.8 dB lower than the white mask reference, also with a limited standard deviation of 0.6 dB. Indeed, a residual fading is still present also when the ASICs are compensating for the SLM-induced perturbations: this is due to the fact that the SLM also slightly shifts the position of the centroid, causing a reduction in the total available power sampled by the OAA. Improvements on the photonic side of the chiplet can be done by increasing the number of GC apertures, adding micro-transfer printed lenslets or using a photonic lantern device [22].

4.5.1 Transmission of high data-rate signals

The effectiveness of the ASIC controllers in establishing a reliable FSO link at high data-rates were tested by modulating the intensity of the laser beam with a 25 Gbaud bit stream. With

respect to the setup described in Sec. 4.3, after performing beam coupling to the single-mode waveguide, the output GC of the PIC emits the coherently reconstructed signal, which is captured by a single-mode fiber and sent to the high-speed optical oscilloscope to evaluate signal quality, without performing any equalization. Fig. 4.8 reports the results of such experiment. First (Fig. 4.8a), a 25 Gbit/s OOK, non-return-to-zero (NRZ) modulation was added to the laser carrier, which underwent SLM-induced distortion before being sampled by the input OAA of the PIC. When the ASICs are not optimizing the configuration of the optical processor (bottom panel), the resulting eye diagram is almost entirely closed. This is inevitable, as the sampled portions of the beam do not have their phases properly adjusted, and thus they are not recombining constructively within each directional coupler of the mesh. In contrast, when the ASICs exert a control action, the distortion of the FSO beam are compensated and the eye diagram opens up to a quality factor (QF) of 6.12.

A similar result is found when transmitting PAM4, 50 Gbit/s signals, which is the case reported in Fig. 4.8b. The diagrams confirm the effectiveness of the approach, regardless of the signal modulation format and data-rate: while the eye is unacceptably degraded when the control is off, its quality is restored, despite the SLM-induced distortion, when the controllers are activated.

For the sake of completeness, Fig. 4.9 confronts the measured eye diagrams (OOK modulation, 25 Gbit/s) of 15 different phase masks, which are the same employed in the experiment reported in Fig. 4.7. In all cases it is possible to appreciate the beneficial effect of the ASIC-assisted signal reconstruction, with an average QF of 5.68 (corresponding to a BER around $6 \cdot 10^{-9}$) and a standard deviation of 0.6. Interestingly, the frequency range of operation of the ASIC, comprising dithering frequency f_{dith}=8.33 kHz and clock frequency f_{CLK}=1.1 MHz, is way lower than the data-rate, meaning that the control loop modulation does not impact whatsoever the quality of the received optical signal.

4.6 Dynamic turbulence compensation

So far, only the step-like static modulations introduced by the SLM have been considered. In order to dynamically distort the

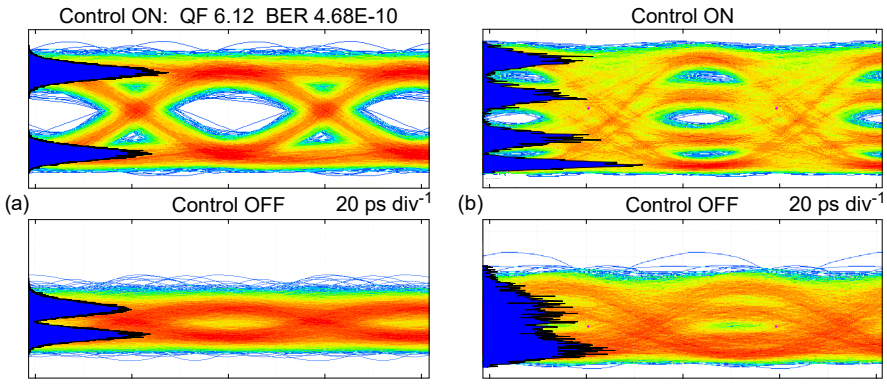


Figure 4.8: *Eye diagrams of* ***(a)*** *OOK and* ***(b)*** *PAM4 modulated signals at* 25 Gbaud*, as collected at the output of the PIC by a high-speed optical oscilloscope. In both cases, turning the controller on (upper diagrams) increases the quality of the eye, which would be completely degraded with no control action exerted (lower diagrams).*

wavefront impinging on the PIC, the SLM was replaced with a heat gun, as schematized in Fig. 4.10a. The following pictures (Fig. 4.10b-d) reports, from different perspectives, the measured power at the output of the PIC, either with (blue curves) or without (red) using the ASICs to compensate for the effect of the introduced turbulence. Like in Sec. 4.5, data is normalized to the reference measurement taken when the controller is kept active with no perturbation along the Gaussian beam path.

When the ASICs are actively steering the MZIs (from 0 s to 8 s in Fig. 4.10b), the average received power sits around -0.17 dB, with standard deviation of 0.1 dB and maximum fading below 0.5 dB, as highlighted in Fig. 4.10c. Independently from the configuration reached, after 8 s the control loops are deactivated, so as to maintain a fixed voltage on each heater. Indeed, on average the PIC is well configured to receive the input beam (as it would be in the case of a static distortion), but the random phase fluctuations now degrade over time the reconstructed optical power. Average power is lowered down to -1.15 dB, which is not so different from the previous case, although standard deviation and maximum fading dramatically decrease to 0.5 dB and more than 3 dB, respectively. The main advantage of real-time control of the PIC thus resides in concentrating samples within a narrower dis-



Figure 4.9: *Comprehensive results of 15 different static phase screens being applied to the FSO link. For each SLM configuration, results are shown with the ASIC turned on/off (upper and lower eye, respectively). Transmitted signal is* $25\,\mathrm{Gbit/s}$ *with OOK NRZ modulation, masks are engineered to provide an effective index parameter* C_n^2 *of* $10^{-12}\ \mathrm{m}^{-2/3}$.

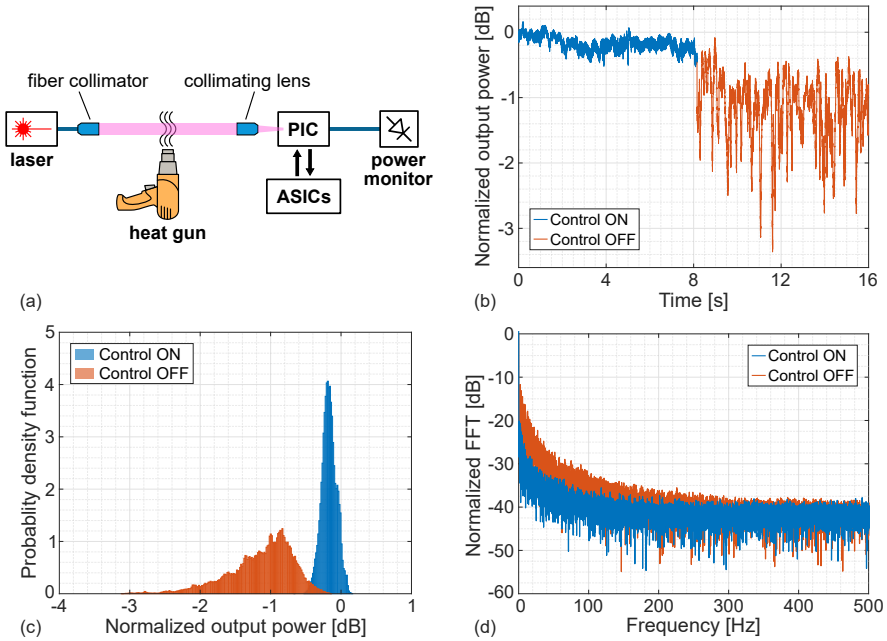


Figure 4.10: ***(a)*** *Simplified scheme of the experimental setup, with the heat gun introducing artificial dynamic turbulence along the beam path;* ***(b)*** *temporal evolution,* ***(c)*** *probability density function and* ***(d)*** *power spectral density of the reconstructed optical signal at the output of the receiver, either when the ASIC controller are actively reconfiguring the PIC (blue curve) or when they are left in idle state (red curve). All plots are normalized to a reference undistorted optical link.*

tribution, eventually increasing received average power, too: 90% of the samples of the blue plot of Fig. 4.10c carry more power than 0.3 dB; the same parameter worsens to −1.83 dB when no control is exerted, with only ≈1% of the samples making it beyond the −0.3 dB threshold.

Finally, Fig. 4.10d provides an estimate in the frequency domain of the perturbation introduced by the heat gun, as well as the beneficial effect of the ASIC-assisted turbulence rejection. When no control is exerted (red plot), it is possible to observe the presence, in the received output signal, of spectral components up to a frequency of ≈300 Hz. When the controllers are counteracting such turbulence (blue), an improvement up to 10 dB can be observed at lower frequencies. This measurement is coherent with the convergence time measured in Sec. 4.4.2: the tracking

time of the ASIC controllers applied to the PIC is, in fact, faster than 10 ms. This is enough to compensate the dynamics of actual atmospheric turbulence [62], ultimately validating the presented approach for actual FSO applications.

CHAPTER 5

Flip-chip assembly of the ASIC-PIC system

This Chapter briefly describes a second ASIC architecture developed within this Thesis. The main goal of this part of the project is to define an electronic controller design that could seamlessly scale in size and power dissipation as PICs grow in complexity (number of devices). 3 main areas of improvement were investigated: (i) scaling down the technology node in order to take advantage of Moore's Law, considering the dominant role played by digital electronics; (ii) implementing a pulse-width modulation (PWM) based actuation mechanism, to improve system linearity while decreasing dissipated power; (iii) assembling the electronic-photonic chiplet as a flip-chip, in order to break the shoreline limitation of traditional wire-bonding.

The ASIC was sent out for fabrication in October 2024 and received for testing in June 2025.

5.1 The need for seamlessly scalable controllers

As it was already discussed in Ch. 1, a striking advantage of ASIC-based control electronics for PICs is the possibility to implement modular architectures that ideally scale at the same pace as photonic processors grow in complexity. To make a quantitative statement, it should be considered that a reasonable footprint for a MZI implemented in a standard commercial Silicon Photonics platform is $\approx$ 60 µm x 450 µm (considering only waveguides and actuators, and excluding electrical routing). Indeed, designing a truly seamlessly scalable electronic architecture requires at least to match the size of each electronic channel with that of its optical counterpart. In the ASIC presented in Ch. 2-4, 8-channels were hosted on a 12.3 mm^2 die, corresponding to an average occupation of $\approx$1.55 mm^2 per module - almost 60 times larger than the MZI. Even when excluding the electrical pads used to connect the ASIC to the PIC, the active electronic area amounts to $\approx$10.5 mm^2, or $\approx$1.3 mm^2/channel - still almost 50 times more than necessary.

To try to close this gap, a new ASIC has been designed taking into account 3 main areas of improvement: technology node, actuation mechanism and chiplet assembly process.

5.2 CMOS circuit architecture

Although with some differences in the circuital solutions, the ASIC implements the same dithering-based control algorithm as the one presented in Ch. 2-4. For clarity, its high-level architecture is reported again in Fig. 5.1, where it is also highlighted how the design is mostly suitable for driving Mach-Zehnder Interferometers. It is possible to appreciate the two main elements of novelty, namely the $\Sigma\Delta$-based read-out scheme and the PWM actuation of thermal actuators, which will be discussed in the following Sections. The chip is powered by a 1.8 V supply, which turns in an immediate saving for what concerns dissipated power.

5.2.1 $\Sigma\Delta$-based read-out

The read-out of the photodetector, which also in this project is a germanium photodiode, is still built upon the idea of initially us-

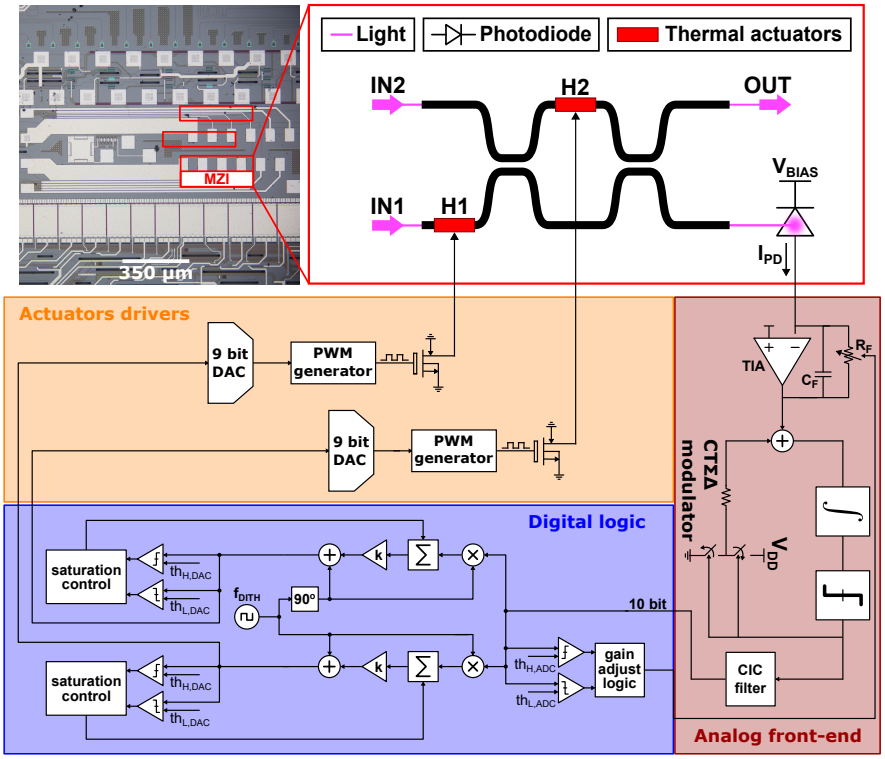


Figure 5.1: *High-level architecture of a single-channel of the ASIC-PIC system, highlighting the main differences with respect to the design presented in Ch. 2-4: ΣΔ ADC and PWM driving of the thermal actuators. As it will be explained in Sec. 5.2.2, actuation is inherently linear, so there is no need to perform square root compression on the digital word fed to the DACs.*

ing a trans-impedance amplifier (TIA) to fit the amplitude of the signal to the full-scale range of the converter. To this purpose, a variable resistor R_F (between 1.4 kΩ and 1.4 MΩ) closes the feedback network around the TIA, its value being determined at digital level according to the value sampled by the ADC. The amplified signal is then fed to a 10-bit, 117 kSps continuous-time ΣΔ ADC [63], whose fundamental building blocks, i.e. the 1st-order modulator and the 2nd-order cascaded integrator-comb (CIC) filter are schematized in Fig. 5.2.

For the modulator, a continuous-time (CTΣΔM) architecture was preferred over a discrete-time (DT) one due to its inherent

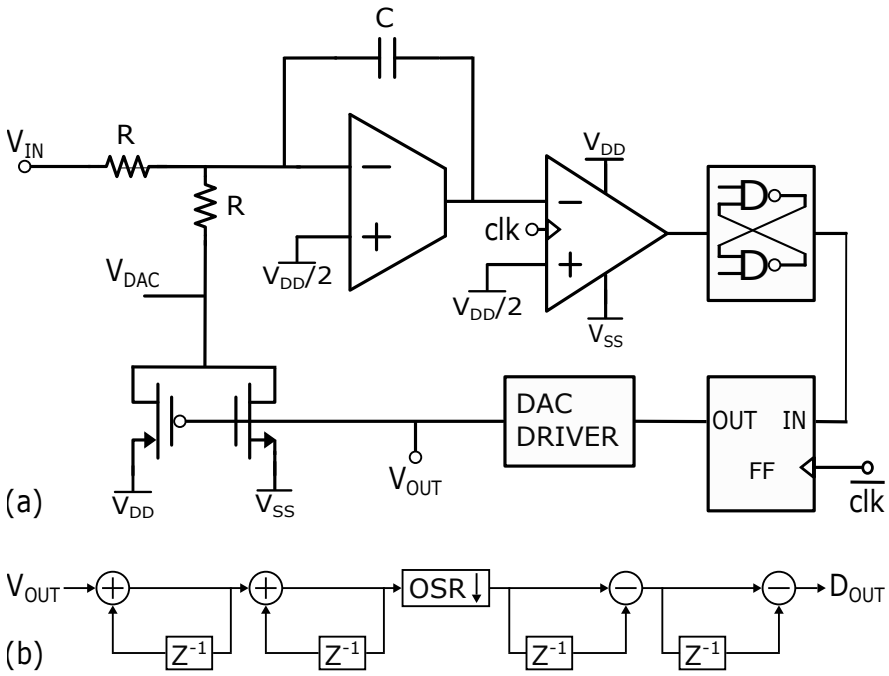


Figure 5.2: *Schematic of the ΣΔ ADC, comprising* ***(a)*** *the 1st-order modulator and* ***(b)*** *the 2nd-order CIC digital filter. Beware that the output of the modulator, which is fed to the filter, is sampled after the 1-bit DAC driver.*

anti-aliasing action, which allows to save some silicon area, its typically lower power consumption and a simpler, ideally purely resistive architecture, whereas DTΣΔMs make use of switched-capacitors networks. The input voltage V_{IN}, generated by the TIA, and the DAC voltage V_{DAC} are turned into current with two resistors R=220 kΩ connected to the virtual ground ($\frac{V_{DD}}{2}$ =0.9 V) node of the OTA. The result of their sum is accumulated on a 600 fF capacitor and fed to a 1-bit ADC, implemented in this design as a StrongARM latch [64]. The selection of RC is such that $\frac{1}{RC} = \frac{f_{CLK}}{4}$, leaving a safe margin from integrator saturation; the OTA was designed with a bandwidth of 160 MHz to guarantee sufficient loop gain when operating at f_{CLK}, and a slew-rate larger than 24 V/µs, needed to charge the feedback capacitor, for an overall power consumption of 330 µW.

The StrongARM latch is followed by a NAND-type SR-latch,

needed to adjust the output of the comparator, which is in fact locked to V_{DD} for half of the clock cycle. However, the latch also introduces a mismatch in the delays between pull-up and pull-down transitions, the former being faster due to the input signal having to propagate only through one NAND gate, instead of two. Furthermore, the overall duration of the transient depends on the differential input voltage of the comparator. All these issues were addressed by cascading the SR-latch with a negative edge-triggered flip-flop, which introduces a fixed $T_{CLK}/2$ delay in the loop, irrespectively of both the input and the output of the comparator. Finally, a DAC driver consisting of a cascade of progressively larger inverters is used to drive both the switches of the feedback branch and the input gate of the CIC filter placed downstream.

As per the theory of $\Sigma\Delta$ converters, an nth-order CT$\Sigma\Delta$M requires an $(n+1)^{th}$-order low-pass filtering of the single-bit sequence [63]. The CIC filter [65] shown in Fig. 5.2b, whose input is the output voltage of the DAC driver present in the modulator of Fig. 5.2a, is composed by the sequence of 2 discrete-time integrators ($H(z) = \frac{1}{1-z^{-1}}$), a decimator block and 2 discrete-time differentiators ($H(z) = 1 - z^{-1}$). Having selected an oversampling ratio OSR=256, the arithmetical cells have to operate with 17-bits wide registers. The CT$\Sigma\Delta$M, as well as the CIC filter, are clocked at f_{CLK}=30 MHz (T_{CLK} ≈33 ns), whereas the signal of interest, i.e. the dithering modulation, has its main harmonic components below 100 kHz. Considering the decimation operated by the CIC (OSR=256), the resulting sampling frequency is, as anticipated, f_S ≈117 kSps. Each dithering period comprises 8 consecutive samples: starting from a clock frequency f_{CLK}=30 MHz, the resulting dithering frequency is $f_{dith} = \frac{f_{CLK}}{8 \cdot OSR}$ ≈14 kHz.

5.2.2 PWM-based actuation scheme

The actuation circuit essentially relies on the pulse-width modulation (PWM) of the voltage applied to the heaters. By applying a square-wave between 0 V and the power supply V_H=6 V with a sufficiently high frequency, the temperature of the waveguide, and hence the induced phase shift, is essentially proportional to the average thermal power dissipated by the actuator (a natural

consequence of the thermal low-pass filtering action of the silicon crystal and its oxide). It is thus possible to establish a linear relation between the digital dithering-modulated working point $C \pm d$ set by the control algorithm, which is fed to the DAC, and the induced phase shift ϕ_H, having the duty-cycle D of the PWM as the proportionality constant.

The linear control voltage-dissipated power relation benefits the actuation circuit in terms of converter complexity. In continuous-time actuation schemes, where the control variable of the system is proportional to the voltage applied on the heater, the dissipated power is quadratically related to the electrical variable. As a consequence, a 1 LSB variation at the input of the DAC determines a modification of the dissipated power which depends on the actual working point of the system. In the design presented in Ch. 2-4, a DAC with $N = 12$ bits drives a nominal resistance R_H =400 Ω, with a voltage as high as 6 V. Therefore, a variation of 1 LSB of the DAC input around 0 V modifies the power dissipated by the heater by $\Delta P_H = (\frac{V_H^2}{2^{2N}})/R_H$=5.4 nW. When the same variation occurs close to the 6 V power supply, a maximum variation $\Delta P_H \approx (\frac{V_H^2}{2^{N-1}})/R_H$=44 µW can be derived. For obvious reasons, the requirements on the number of bits of the converter must be sized on this latter value, which must correspond to a sufficiently small output optical power variation. If the control algorithm, instead, controls the average power dissipated by the heater, thus establishing a linear relation with the input of the DAC, the required number of bits needed to achieve the same resolution is just $N - 1$. In the previous design, $N = 12$ represented a very conservative choice: in fact, all the reported optical experiments were performed with a dithering modulation with amplitude d well beyond ±1 LSB (d=10 LSBs or more). Following such experimental validation, for this design a coarser resolution of $N = 9$ bits was chosen.

Ring oscillator

Considerations about the thermal ripple that will be presented in the experimental Sec. 5.4.3 demonstrate how a reasonable value for the PWM frequency is f_{PWM}=10 MHz (T_{PWM}=100 ns). Such reference is generated by an integrated ring oscillator, which is

implemented as a loop of 5 custom-sized current-starved inverters. Such relatively simple choice is justified by the fact that, provided that the frequency of the PWM stimulus is fast enough not to cause a visible thermal ripple in the output optical power, its precise value does not matter; what is relevant, instead, is the monotonicity of the duty cycle D of the modulated waveform, which is not controlled by the ring oscillator. Fig. 5.3 reports the simulated PWM periods for different process corners (Fig. 5.3a) and temperatures (Fig. 5.3b), as a result of a sweep of the voltage controlling the starved inverters. While differing up to a factor x2.5 in the worst cases from the nominal value of T_{PWM}=3.2 ns, the resulting frequency can still be considered sufficiently fast, as the measurements reported in the following Sec. 5.4 will show.

Delay-locked loop architecture

Having also selected the number of bits $N = 9$, the PWM generator should then be able to discriminate pulses with on-time that differ by $\Delta T_{ON,LSB} \approx$200 ps. Had to be implemented as a simple, behaviorally modeled digital circuit (basically a counter), such generator should operate with a f_{CLK}=5 GHz, way too fast for the chosen technology in terms of slack.

In this design, such requirement could be eased thanks to the adoption of a delay-locked loop (DLL) [66], whose use in this design is schematically demonstrated in Fig. 5.4. The 9 input bits that determine the duty cycle D are split into 5 MSBs, used for coarse tuning of the on-time T_{ON} of the PWM, and 4 LSBs, which instead fine tune the selected T_{ON}. The PWM generator is therefore clocked with a more suitable frequency f_{CLK}=312.5 MHz ($T_{CLK} \approx$3.2 ns), instead of 5 GHz: this allows, through the 5 MSBs, to discriminate between 32 values of T_{ON}, with a time step equal to T_{CLK}. Also the DLL is fed the reference T_{CLK}=3.2 ns: thanks to the action of negative feedback, the incorporated voltage-controlled delay line (VCDL) delivers at the outputs of its current-starved inverters 16 square-waves, each one being delayed from the previous one by $\frac{T_{CLK}}{16}$=200 ps, corresponding to $\Delta T_{ON,LSB}$. They are all connected to a multiplexer, which is controlled by the 4 LSBs at the input of the DAC. They select which output should be used as the clock sig-

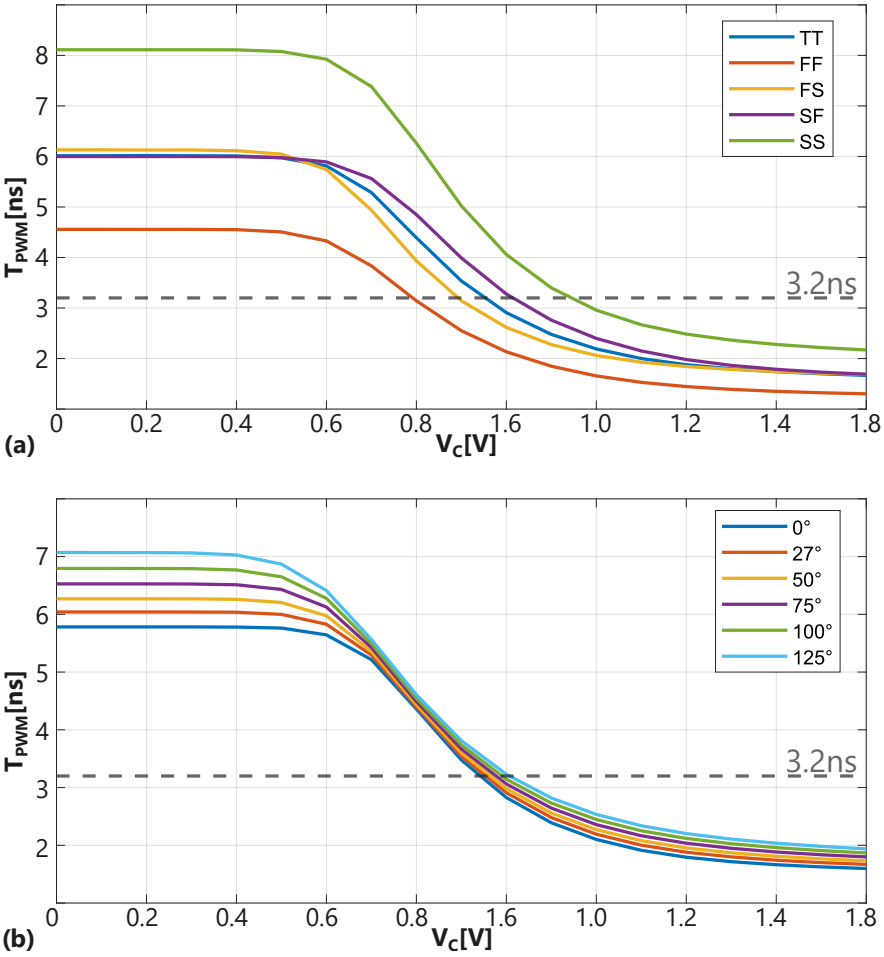


Figure 5.3: *Simulated period of the ring oscillator generating the reference signal for the PWM stimulus, evaluated for a $0-VDD$ sweep of the control voltage of its inverters and against (a) corners and (b) temperature.*

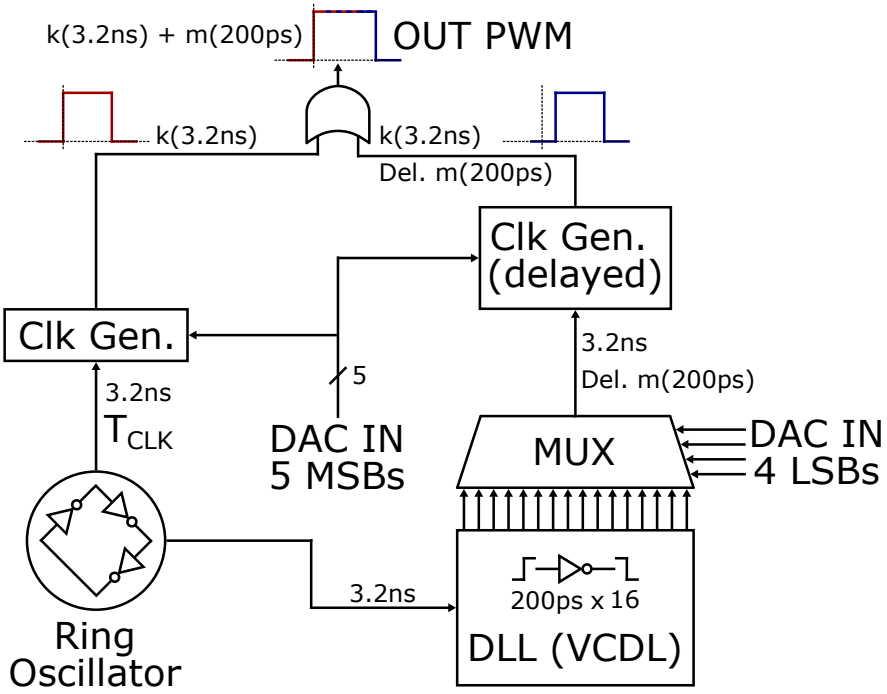


Figure 5.4: *Block diagram demonstrating the working principle of the PWM generation: a single clock source with T_{CLK}=3.2 ns is used to generate both a reference PWM signal (left branch) and, thanks to the VCDL inserted into the DLL, a delayed one (right). The two signals are then combined in an OR gate to obtain the output PWM used to drive the actuators.*

nal for generating a second waveform, which therefore has the same T_{ON} as the reference, but is delayed by $k \cdot \Delta T_{ON,LSB}$. It is sufficient to make the logical sum (OR) of the two square-waves in order to obtain, at the output of the DAC, a PWM signal with $T_{PWM} \approx$100 ns and an on-time T_{ON} that can be tuned with a time-step $\Delta T_{ON,LSB}$=200 ps.

The pivotal role played in this architecture by the action of negative feedback can be understood by the architecture of the DLL, schematically presented in Fig. 5.5a. The ultimate goal of this control loop is, in fact, to ensure that the square-waves at the outputs of the VCDL have the exact same period T_{CLK} as the reference signal, plus a selectable delay. This is achieved by minimizing the phase delay between *REF* and *DEL* signal:

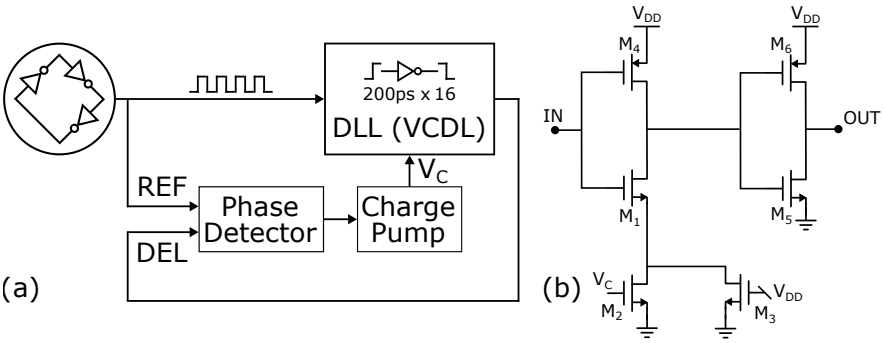


Figure 5.5: ***(a)*** *Schematic architecture of the DLL, showing how the control loop acts to minimize the phase shift between the two inputs (REF and DEL) of the phase detector;* ***(b)*** *schematic of the current-starved inverter used in the VCDL. Transistors $M_{1\text{-}4}$ form the proper starved-cell: the gate voltage of M_2 is controlled by the output of the phase detector, thus determining the pull-down transition time, while M_3 provides a conductive path that sets the lower limit to the discharge current; M_4 delivers pull-up, which is not affected by the phase-detector.*

according to their relative phase shift, the phase detector drives a charge pump that determines the voltage V_C of each inverter within the VCDL. Note that, while having ideally nil relative phase shift, *REF* and *DEL* are separated in time by T_{CLK}.

Delay-locked loop building blocks

As stated, the VCDL is composed of a chain of 16 nominally identical current-starved inverters. The schematic of a single building block is represented in Fig. 5.5b. First of all, it is evident that it comprises a pair of inverters, with the second one (transistors $M_{5\text{-}6}$) being used to regenerate the output of the actual current-starved cell (transistors $M_{1\text{-}4}$). This latter sub-circuit has its pull-down propagation delay determined by the voltage V_C, which controls the gate of M_2: if, for example, the rising edge of *REF* triggers the phase detector before that of *DEL*, the following charge pump injects current into the gate of M_2, so as to increase V_C and speed up the propagation of the clock through the VCDL. It is worth noticing that, for the opposite case (decreasing V_C), the upper limit to the propagation delay is set by M_3, which is always on and thus sets the minimum current available for the discharge of the intermediate node.

The voltage V_C is generated by the series of a digital phase detector (PD) [67] and a charge pump, whose schematics are reported in Fig. 5.6a-b. It should be noted that the transistors are sized so that the pull-down network is stronger than the pull-up one, meaning that the signal O_1 and O_2 are at ground potential when both the n- and the p-MOSFET are on (REF=0, DEL=1 for O_1 and REF=1, DEL=0 for O_2). Looking at Fig. 5.6c, if DEL is lagging with respect to REF, for the amount of time corresponding to the delay between the two rising edges the signal UP will be set to 0 (while DN is constantly set to 1); consequently, the left branch of the charge pump will be turned on, eventually adding charge on the capacitor, increasing V_C and thus making the commutation of the current-starved inverters inside the VCDL faster; if, instead, DEL is leading REF, UP will always be stuck at 1, and DN will switch to 0 during the delay interval, draining charge from the V_C node and ultimately slowing down the VCDL.

Driving circuit

The PWM signal generated by the OR gate at the output of the DLL block is equivalent to a digital signal constrained between ground and 1.8 V, which is indeed not suitable for driving the power devices that ultimately force the current through the thermal actuators. There are two main limitations to overcome:

- the threshold voltage of the power MOSFETs, which is ≈1.6 V for the selected devices (DMOS with thick oxide and minimum channel length of 0.65 µm). Driving such devices with a 1.8 V power supply would lead to unacceptably bulky structures, needed to force into the heater currents up to 15 mA with only 0.2 V overdrive voltage;
- the capacitive load of the power MOSFETs, that can be as large as 2 pF, for each DMOS is composed of 20 fingers with an aspect ratio $\frac{W}{L} = \frac{60\,\mu m}{0.65\,\mu m}$. If driven using standard logic cells available with the technology, such load would cause PWM transitions to be too slow, eventually compromising the effectiveness and the precision of the driving signal.

To overcome these issues, a digital amplification circuit was designed, as reported in Fig. 5.7. The output of the OR logic

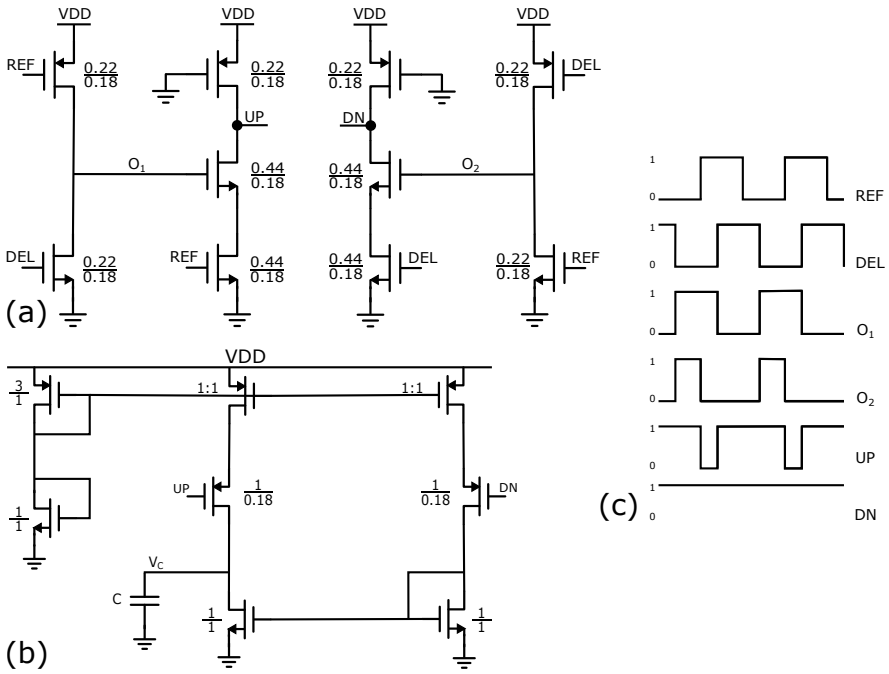


Figure 5.6: *Sized schematics of* ***(a)*** *the phase detector and* ***(b)*** *of the charge pump employed in the DLL to regulate the control voltage V_C of the current-starved inverters forming the delay-line.* ***(c)*** *Working principle in lag state (DEL delayed with respect to REF).*

gate from the DLL block, constrained between 0 V and 1.8 V, is initially fed to a level shifter [68]. All the transistors used in this cell are meant to work with 3.3 V power supply, although they obviously have a threshold voltage V_T <1.8 V. The cell makes use of positive feedback in order to regenerate the input waveform: note that $M_{1\text{-}2}$ are driven complementarily, so that when, for example, M_1 is turned on by a rising edge at its gate, M_2 turns off; as a consequence of M_1 being conductive, the gate voltage of M_4 is lowered and the transistor turned on, eventually increasing the output voltage (which also corresponds to the gate voltage of M_3, which is kept off). The basic requirement for the level shifter to properly work is that, when on, $M_{1\text{-}2}$ are sufficiently conductive to lower the gates of the p-MOSFETs at least to 3.3 V$-V_T$; their sizing, instead, was studied in order to keep pull-up and -down transition sufficiently sharp with respect to the PWM on-time

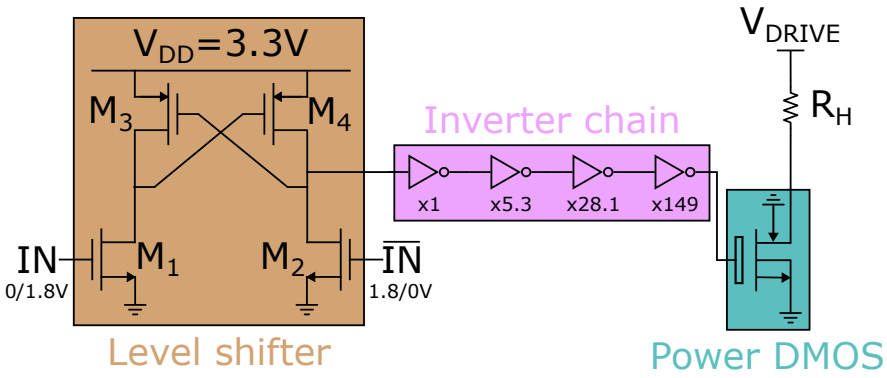


Figure 5.7: *Schematic of the chain driving the thermal actuators. The input to the level shifter comes from the OR gate of the PWM waveform generator; differently from all the other transistors employed in the ASIC, the power device has its body surrounded by a deep n-well, which is connected to ground.*

(as low as 3.2 ns) and its discretization.

Finally, an inverter chain was placed to properly bootstrap the output of the level shifter to the capacitive load (≈2 pF) represented by the power DMOS structure. Considerations about the capacitive load of each gate led to determine an optimal ratio between the sizes of adjacent inverters equal to 5.3, meaning that, apart from the first one, cells from the technology library could not be used and custom ones had to be designed.

Power dissipation

Before moving to practical and experimental aspects, a brief summary should be included regarding the power dissipated by the circuit, which breaks down for each channel as follows:

- the analog front-end dissipates up to 3.5 mW, needed to handle photogenerated currents as high as 1 mA;
- the CTΣΔM adds 0.5 mW to the budget, most of which (0.3 mW) is needed by the OTA that powers the integrator;
- 1 mW is the approximate amount of power dissipated by the digital circuitry that runs the control algorithm;
- the actuation scheme requires 2.3 mW, mostly for the ring oscillator (2 mW), the rest (0.3 mW) for the driver line.

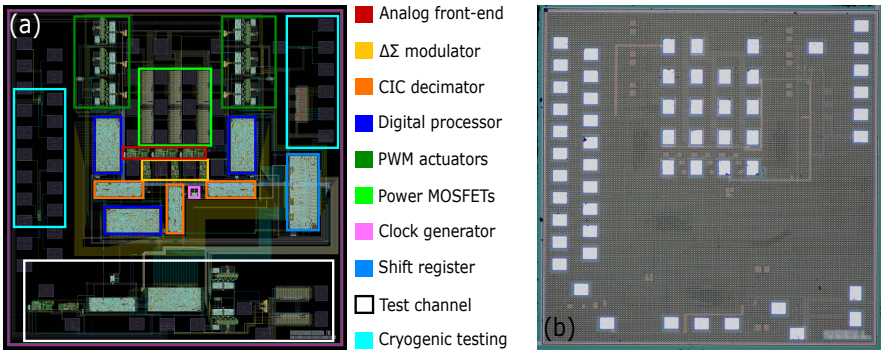


Figure 5.8: ***(a)*** *GDS image of the ASIC, where all the cells of the system have been highlighted;* ***(b)*** *microscope picture of the ASIC: it is possible to see only the exposed pads and the routing nets implemented with the top 2 metal layers. The pads located top-center of the die are those used for connection to the PIC via ball-bonding.*

The total dissipated power per channel, which amounts to around 7.6 mW, should be compared with the demand of each actuator, which can be as high as 90 mW (6 V being applied on a nominal resistance R_H=400 Ω). It is worth highlighting the significant efficiency improvement with respect to the continuous-time actuation scheme. In this latter solution (that can be retrieved in Sec. 2.1.3), in fact, all the current that flows through the heater is also sent through the power MOSFET, with this component showing peak power dissipation for $V_{DS}=\frac{V_{DD}}{2}$. This condition is never met with the PWM actuation: power MOSFET and heater are still in series, but the voltage applied to the actuator is either 0 V (hence no current flow) or 6 V, and in this case the 15 mA current only dissipates, within the MOSFET, a power proportional to the small V_{DS} which is necessary to sustain charge flow.

5.3 Chip fabrication

The technology selected for the fabrication of this ASIC was X-FAB XH018, with 180 nm feature size and 6 metal layers. By default, the foundry covers the fabricated ASICs with a protective layer of top metal; hence, for better clarity, alongside a microscope picture of the physical chip Fig. 5.8a also reports the GDS that was sent for fabrication, breaking down the regions of the

ASIC. At the top center of both pictures in Fig. 5.8 it is possible to appreciate a total of 19 metal pads that were used for connecting the ASIC to the PIC via ball-bonding. These pads not only provide the electrical connections to the optical devices, but also all the necessary power supplies and signal routing needed for ASIC operation:

- 9 pads are used to connect each channel of the ASIC to the corresponding MZI on the PIC (2 heaters and 1 photodiode each (anode contact);
- 1 pad provides the 1.8 V supply to the analog components of the circuit, and 2 additional pads are used for digital power supply, at the same voltage;
- 2 pads are used to collect currents to ground node; in order to limit ground bouncing on the read-out side, 1 additional, separate pad is used as ground reference for the PWM-based actuation circuit;
- 1 pad supplies 3.3 V to properly operate the inverter cells that drive the power transistors;
- 3 pads (input, output and register clock) are used to operate the serial communication interface.

The chip, which was fabricated as a mini@sic design via the Europractice platform, has an overall footprint of 1.55 mm x 1.55 mm (2.4 mm^2). It is mainly composed of 3 independent and parallel channels, which are actually meant to operate 3 photonic devices simultaneously; Fig. 5.8a shows that the die hosts a separate test channel, that can be used for electrical characterization, and some fundamental devices (single resistors and MOSFETs from the PDK) that will be needed to explore the technology behavior at cryogenic temperatures.

5.3.1 Benefits of scaling the technology node

The most straightforward advantage of having shrunk the technology node is, of course, the improvement in integration density and consequently in the occupied area. This is mostly evident for what concerns digital circuits, which play a relevant role in

this design, implementing both the dithering-based integral control algorithm and the CIC filter that elaborates the output of the $\Sigma\Delta$-modulator. Interestingly, bringing the feature size down from 350 nm to 180 nm, on average, improves the area occupied by digital logic by a factor $\approx$5.5, larger than the mere square ratio between the two minimum lengths. In fact, integration density is also improved thanks to the increased number of metal layers available for interconnections, as well as their shrinking in terms of minimum width, both of which allow for denser routing.

Faster digital electronics are also at the foundation of the solutions adopted for the interface circuits:

- they make easier to implement ADCs with reasonable resolution in the audio range (tens of kHz), as it is possible to achieve high oversampling ratios [69];
- they allow the adoption of PWM-based actuation schemes, where propagation delays in the order of hundreds of ps are needed to achieve proper resolution.

5.3.2 Flip-chip photonic-electronic assembly

What follows is a brief recap of all the process steps which have been followed to fabricate the ball-bonded electronic-photonic chiplet, starting from two separate CMOS and Silicon Photonics dies, respectively, and ending with gluing and wire-bonding of the flip-chip to a custom-designed test PCB.

- **Ball deposition**: the first step of the process involves depositing gold balls on each pad of both the ASIC (Fig. 5.9a-b) and the PIC (Fig. 5.9c-d). This is done by using a ball-bonder (K&S 4124) whose 25 µm-wide wire is immediately cut after touching the pad. Having both dies covered with gold balls improves both electrical connection and mechanical resistance of the bonding: in fact, this eases the soldering between balls during the following thermo-compression step, as having gold only on one side may cause diffusion between the two metals (pads are in aluminum), which results in poor electrical conductivity, voids formation and so-called "purple plague" [70];

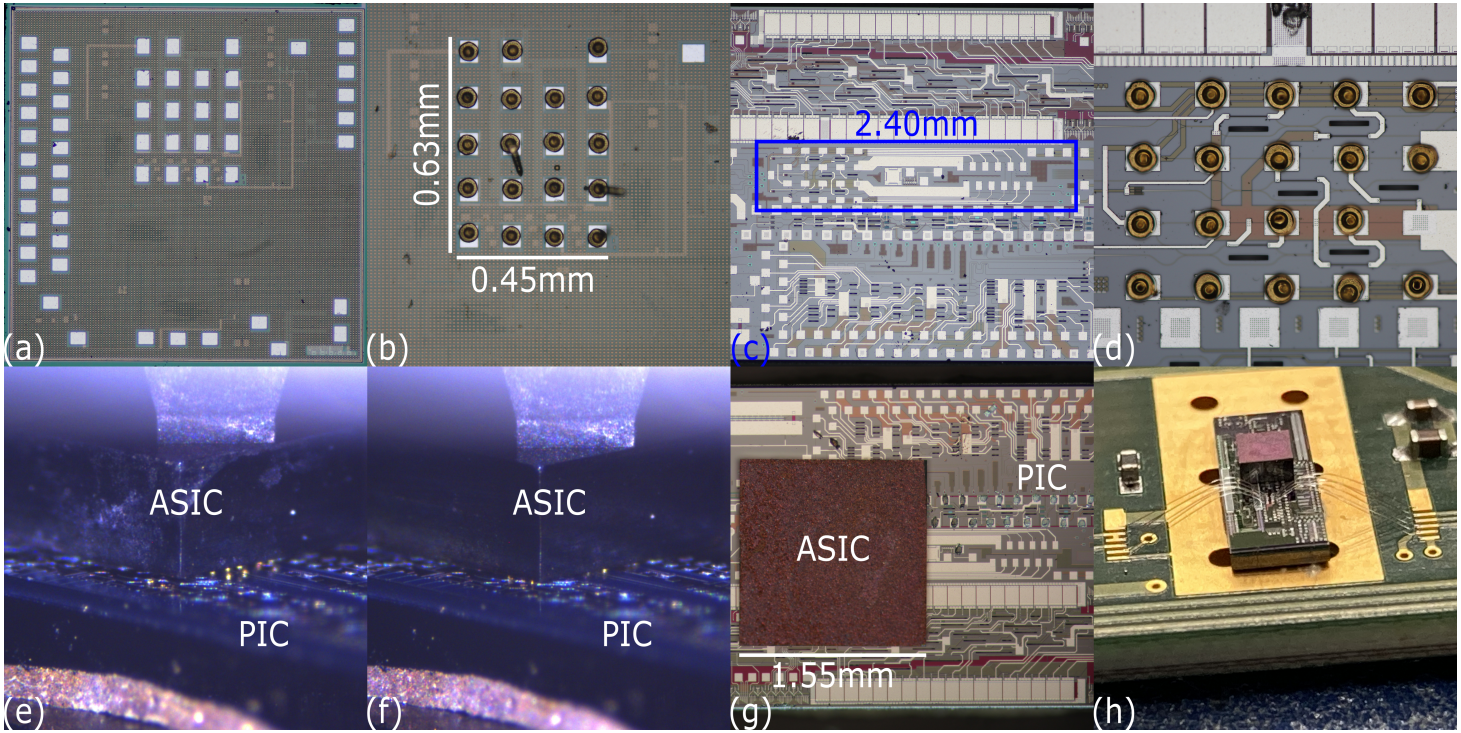


Figure 5.9: *Phases of flip-chip fabrication:* ***(a-b)*** *microscope pictures of the electronic ASIC before-after balls deposition: two "tails" clearly show up, but they can be neutralized with coining;* ***(c-d)*** *microscope pictures of the PIC before-after balls deposition;* ***(e-f)*** *Lateral camera shot during the thermo-compression process before-after* $t = 150\,\mathrm{s}$*, when peak temperature is reached and force applied: it is possible to appreciate a small compression of the balls;* ***(g)*** *microscope view from top of the flip-chip;* ***(h)*** *final chiplet assembly, wire-bonded to the custom holder-PCB.*

- **Coining**: after deposition, the balls all have a diameter comparable to the size of the pads (whose footprint is 70 µm x 57 µm), but they might differ in their height, due to imprecision in the gold wire breaking operation. In particular, some balls may exhibit golden "tails" that can be as tall as the ball itself (like those in Fig. 5.9b), thus undermining the success rate of the process if not properly taken care. To this purpose, both chips undergo a coining operation, which consists in vacuum-clamping them (from the back side) to a mechanical lever and then pressing the deposited side against a hard surface with controlled force ($\approx$0.15 N/ball), so as to flatten the balls down to the same height;

- **Thermo-compression**: the actual bump bonding, that ultimately leads to the formation of the flip-chip, combines the action of temperature and pressure. The operation first involves vacuum-clamping one chip ("target", the PIC) to the fixed base of the ball-bonder and the other ("head", the ASIC) to the lever. With a help of a system of cameras, head and target can be precisely aligned before pressing the leveled balls against each other. The machine, whose temperature-force profile is reported in Fig. 5.10, exerts a force of $\approx$0.2 N/ball, at the same time reaching up to 450 °C (melting point of Au is $\geq$1000 °C, but the metal becomes malleable at lower temperature) for $\approx$ 60 s. The overall thermo-compression process (including heating and cooling of both head and target) lasts $\approx$380 s. Fig. 5.9e-f show the formation of ball-bonds, which occurs at t=150 s, shortly after the programmed force is applied: it is possible to appreciate the slight compression of the ASIC onto the PIC due to the deformation of the balls.

- **Wire-bonding**: it is worth pointing out that the fabrication of the chiplet happens when the ICs are still separate from the holder board, and they are only glued onto the PCB, on the photonic backside, after thermo-compression. The chiplet is finally electrically connected to the board through wire-bonding, performed at Politecnico di Milano with a F&S Bondtec 5600 semi-automatic wire-bonder. Interestingly, also the signals and the power supplies which are

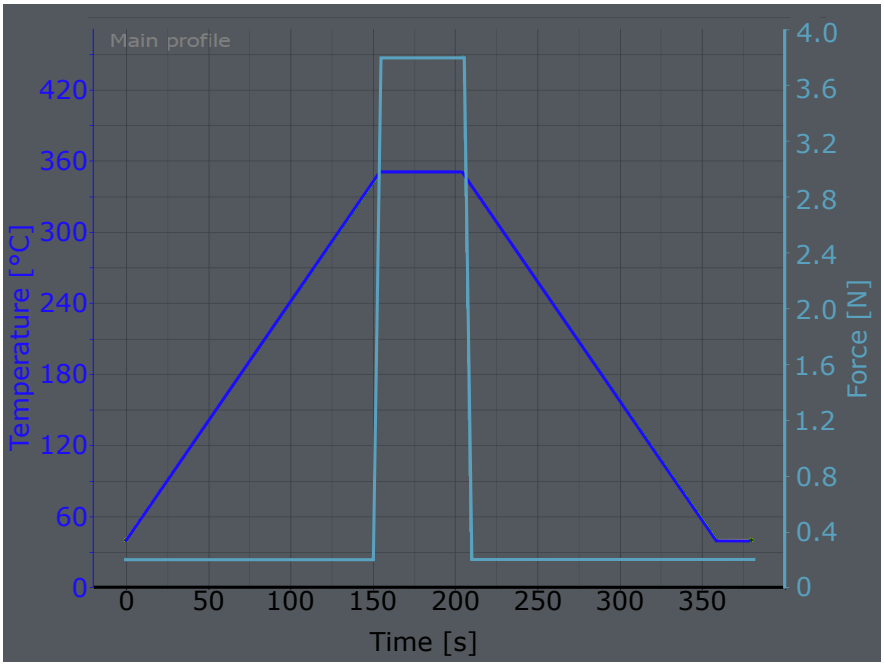


Figure 5.10: *Visualization of the software tool that operates the ball-bonder machine showing the thermo-compression profile for flip-chip fabrication. Force (baby blue) is applied, for roughly* 60 s*, when head and target reach the maximum temperature (bright blue).*

strictly needed by the ASIC (e.g. power supplies and serial communication) are first fed from the PCB to the PIC, and then routed through the photonic metal layers underneath the flipped electronic die.

Balls deposition on both chips was performed at Polifab, the micro and nano fabrication facility of Politecnico di Milano. The assembling process, comprising the coining of the 2 chips and their connection through thermo-compression, was performed using a FINEPLACER pico2 multi-purpose bonder (Finetech GmbH & Co. KG) in the clean-room of XGLab S.R.L. (Bruker Corp.), in Milano.

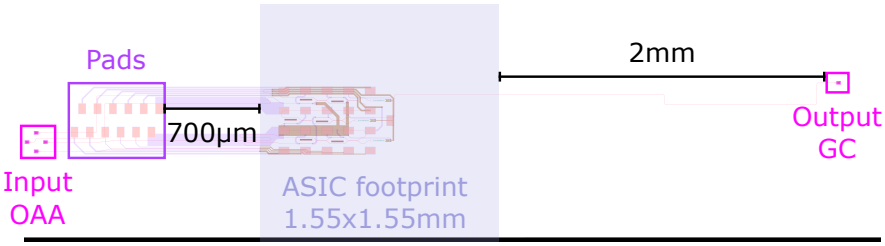


Figure 5.11: *GDS rendering of the 3x1 beam coupler controlled by the ASIC presented in this chapter. The footprint of the electronic IC is reported, justifying the distance separation (*750 µm *between the interferometers and the OAA).*

5.4 Experimental validation

Before chip fabrication, the effectiveness of the PWM-based actuation approach was tested. After receiving the chip and finally succeeding in the fabrication of the flip-chip, the ability of the ASIC to drive a MZI was assessed. The specific device is the terminal element of a 4x1 beam-coupler, so that its output could be terminated by a GC that coupled the waveguide to an external photodiode.

5.4.1 Photonic Integrated Circuit

The targeted photonic integrated circuit consists in a simpler version of the one used in the experiments presented in Ch. 4. While a microscope picture of the fabricated chip is available in Fig. 5.9c-d, for clarity it might be useful to report in Fig. 5.11 the GDS file that was sent to the chip maker. Its peculiar shape and routing are mainly dictated by the need to connect the controller ASIC in a flip-chip arrangement: for obvious reasons, the input optical aperture array (OAA) has to be placed far enough from the mesh of Mach-Zehnder Interferometers, so that the ASIC will not either reflect or shadow the free-space beam impinging on the PIC or, if using optical fiber, will not represent a mechanical obstacle for fiber gluing. For the same reason, also the output GC had to be placed sufficiently far away from the ASIC footprint, while the array of pads needed a 700 µm spacing from the upper chip, roughly corresponding to the thickness of the silicon wafer, in order not to make the wire-bonder collide with the die.

Having to deal with two novelties in the design of the controller, namely the PWM-based driving of the actuators and the ball bonding of the two ICs, a fairly simple structure was adopted, featuring a total of 3 interferometers in a binary-tree mesh topology, so that the PIC can still operate as a beam coupler. The adopted technology is the same used for the programmable optical processor described in Sec. 4.2 (AMF SiP).

5.4.2 PCB holder for electrical and optical testing

In order to perform experimental validation, the custom holder PCB portrayed in Fig. 5.12 was designed to accommodate both the assembled flip-chip and a single ASIC. This latter feature eventually allows to perform electrical characterization, if needed. Differently from the project presented in Ch. 2-4, where multiple ASICs could be connected in modules to the photonic target, the flip-chip arrangement inherently always requires a single ASIC to be connected to the PIC; therefore, connectors for ASIC-PC communication are only needed on one side (left of Fig. 5.12). 3 BNC connectors, instead, were used for testing the ASIC, either to inject a controlled current into the read-out circuit (thus mimicking the photodiode) or to read the outputs of the $\Delta\Sigma$ and the PWM modulators, respectively.

To save active silicon area, none of the pads of the ASIC are equipped with a protection network; to mitigate this issue, 3 pairs of Zener diodes (MMSZ4679T1G, ON Semiconductor Corp.) were connected to the nets that carry the digital signals to the integrated shift register, thus ensuring that their potential is always constrained between ground and 1.8 V.

5.4.3 Evaluation of the thermal ripple

As anticipated in Sec. 5.2.2, the frequency of the modulated actuation signal has to be chosen in order to limit the thermal ripple in the waveguide. In fact, the PWM command of the drivers results, in the integrated heaters, in an on/off switching of the current (and, hence, of the dissipated power) between 0 and V_H/R_H. As a consequence, the temperature of the waveguide has an average value which is determined by the duty cycle D, but it is also characterized by the presence of a thermal ripple at the

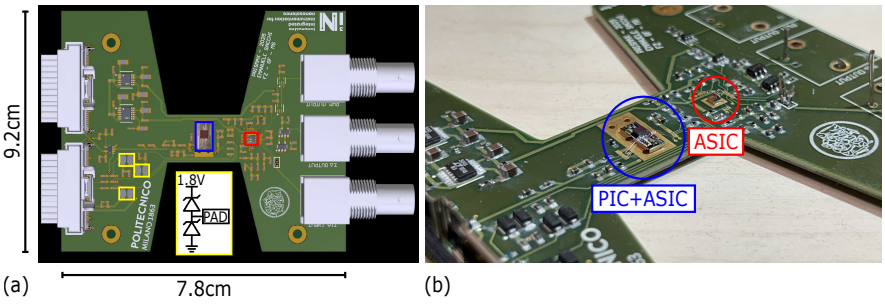


Figure 5.12: ***(a)*** *3D rendering of the custom-holder PCB, which can accommodate both the flip-chip connected ASIC-PIC chiplet (center) and, for the sole purpose of electrical characterization, a single ASIC;* ***(b)*** *close-up picture of the PCB, with integrated circuits mounted on top and wire-bonded to board.*

same frequency f_{PWM} of the input modulation: f_{PWM} must be chosen in order to limit this ripple so that the associated phase shift variation results in a modification of the output power of the MZI lower than the modification corresponding to a 1 LSB variation of the DAC input.

To this purpose, literature extensively covers the problem of modeling heat propagation in waveguides [71]. Here, the problem is approached empirically, following the set-up employed in 5.13a, where one of the heaters of a MZI is connected in source-follower configuration to a square-wave driven n-type power MOSFET. The bias of the MZI is fixed by setting an average gate voltage of 7 V, which determines equal splitting of the output optical power P_{OUT} between the two ports. The MZI is thus working around the point of maximum sensitivity (and maximum linearity) of its transfer function with respect to the heater current. The input square wave switches the gate voltage between 5.9 V and 8.1 V, which correspond to the minimum and maximum amount of P_{OUT} impinging on the power monitor, respectively. The other heater, instead, is left unconnected, so that it is possible, over a reasonably short time, to fix the output optical power by acting only on the first one. Duty cycle was set at $D = 0.5$, which indeed causes the strongest ripple. It is worth noticing that such experimental setup makes use of discrete power MOSFETs, instead of the actual integrated ones. The choice was mainly motivated by time and cost considerations, as the frequency of the PWM (or,

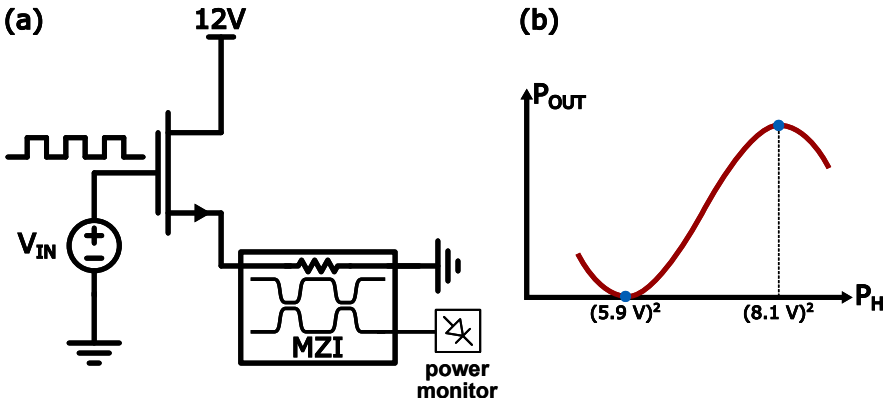


Figure 5.13: ***(a)*** *Schematization of the experimental setup used to evaluate the thermal ripple of a waveguide as a consequence of PWM-based actuator driving and* ***(b)*** *visualization of the two voltage levels of the input square-wave, which alternatively steer P_{OUT} between a point of minimum and maximum.*

at least, its order of magnitude) had to be chosen before sending the ASIC out for fabrication.

Experimental results are reported in Fig. 5.14. The time traces of the optical output power for 3 different PWM frequencies are reported in Fig. 5.14a. At f_{PWM}=10 kHz, the modulation is so slow that the total injected optical power (1 µW) is completely switched between the two output ports of the MZI: this result confirms that the thermal response time of the heater itself is in the order of 10 µs, as supported also by the same measurement performed with f_{PWM}=100 kHz. The ripple, instead, apparently becomes negligible when increasing modulation frequency beyond 1 MHz. Fig. 5.14b, which represents the measured ripple amplitude obtained by sweeping f_{PWM} between 10 kHz and 1 MHz, also helps modeling the thermal response of the waveguide: in fact, it is possible to observe that the ripple tends to decay exponentially with the frequency, rather than with the −10 dB/decade slope corresponding to a single pole low-pass filtering.

The measured ripple at 1 MHz is 11.2 nW (−49.5 dBm). The minimum possible variation of P_{OUT} occurs when the MZI working point is modified by 1 LSB, and corresponds, with a V_{DD}=12 V power supply and heaters with resistance R_H=400 Ω,

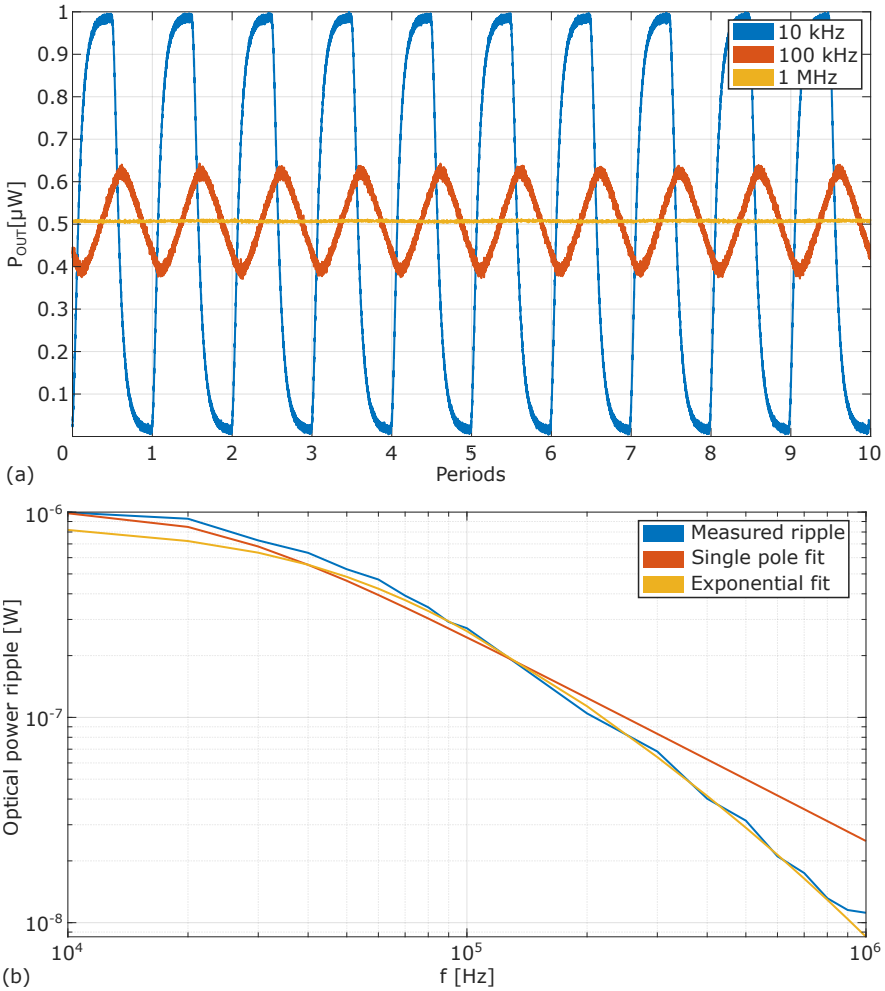


Figure 5.14: ***(a)*** *Time traces of the output optical power resulting from 3 different frequencies of the input stimulus: average power is always* $0.5\,\mu W$ *(MZI in balanced state), whereas the ripple is frequency-dependent. Note that the horizontal axis is normalized to the periodicity of each trace (from* $100\,\mu s$ *to* $1\,\mu s$*);* ***(b)*** *amplitude of the measured thermal ripple as a function of PWM frequency, compared against a single-pole system response (red) and an exponential behavior (yellow).*

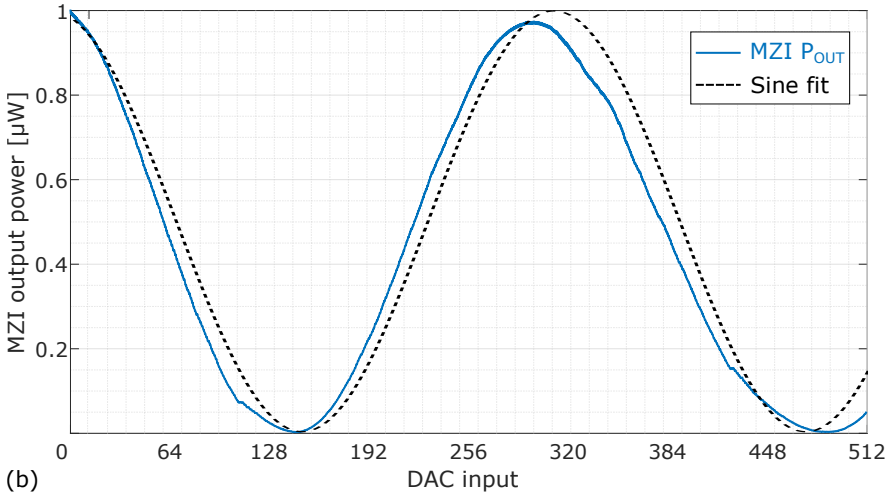


Figure 5.15: *Output power of a MZI as a response to a DC sweep of one of its actuators, showing a sinusoidal transfer function not affected by distortion, as shown with the help of an ideal reference (dotted line).*

to $\Delta P_{H,LSB} = \frac{V_{DD}^2}{R_H} \approx 700\,\mu W$; taking into account the slope of the MZI transfer function $P_{OUT}(P_H)$ in the bias point of the MZI, a 1 LSB modification of P_H determines a variation of P_{OUT} by 28.7 nW, meaning that f_{PWM}=1 MHz is sufficient to satisfy the requirement of a negligible thermal ripple; however, some margin was taken by selecting f_{PWM}=10 MHz.

5.4.4 Testing system linearity

The linear-by-design control over the working point obtained through PWM actuation of the MZI was assessed by performing a full DC sweep of the digital input fed to the DAC of a single actuator (while keeping the other at a fixed value). The result is showcased in Fig. 5.15: the output power of the MZI was measured, showing a reasonably sinusoidal response to the control word and hence to the power dissipated by the heater, as highlighted also with the help of an ideal reference function. Quadratic distortion is no longer present: in fact, the periodicity of the function is not dependent on the particular working point.

CHAPTER 6

Conclusions

"Questa conclusione, benché trovata da povera gente, c'è parsa così giusta, che abbiam pensato di metterla qui, come il sugo di tutta la storia. La quale, se non v'è dispiaciuta affatto, vogliatene bene a chi l'ha scritta, e anche un pochino a chi l'ha raccomodata. Ma se in vece fossimo riusciti ad annoiarvi, credete che non s'è fatto apposta". [72]

"This conclusion, though arrived at by such plain people, has seemed so true that we have decided to set it down here as the moral of our whole story. For the which, gentle reader, if it has not displeased you entirely, feel thankful to the scribe who wrote it, and a little also to the one who has revised it. But if, on the contrary, we have succeeded only in boring you, be assured that we have not done soon purpose".

6.1 Conclusions

This Thesis dug deeper into the discussion about the need for an electronic control layer in enabling programmability of photonic integrated circuits. Specifically, starting from the premise that increasingly complex PICs require electronics to scale accordingly, it was shown how ASIC-based solutions can implement fully functional control loops able to reconfigure optical processors featuring tens (up to 16) of interferometers.

In the two chiplet systems proposed in the Thesis, the electronic controller takes up a footprint comparable to that of the targeted PIC, with a power consumption significantly lower with respect to the one required by the actuators; furthermore, both in terms of area and energy, they cost a fraction of their discrete components-based counterparts. It was also demonstrated how 3D-integration in a flip-chip arrangement of the systems can break the shoreline limitation of traditional wire-bonding, allowing for easier and more compact and robust packaging.

The designs mainly targeted free-space optical communication experiments, a field of growing interest due to the broad range of possible applications, from sensing to urban-scale connections and up to satellite links. It was demonstrated how, with the help of electronics, an optical receiver can work as a programmable lens, where the matrix of interferometers is constantly tuned to always track the optimal configuration that maximizes the power coupled to the output single-mode waveguide, regardless of fabrication defects, slow drifts and, noticeably, turbulence affecting the FSO signal. The advantage in such application is that signal reconstruction happens directly in the optical domain, with no need for sophisticated electronics performing high-speed digital signal processing (DSP) afterwards.

6.2 Future developments

As demonstrated across the experiments presented in this Thesis, the developed CMOS architectures represent a highly power- and area-efficient solution for all those applications where the linear operation to be performed in the optical domain only requires on/off switching of the photonic device. Despite solving

an actual problem for real-world applications [52], the ASIC controllers still fall short of enabling truly arbitrary and universal operation of MxN matrices of interferometric devices. Such a universal programmable PIC should be able to determine, for each interferometer, both a fractional output power split (and not just on/off switching) and the relative phase shift of the output signals with respect to the input ones, hence implementing a linear matrix with complex coefficient. In other words, the goal is to integrate the control algorithm defined in [23], although this requires also a modification on the photonic die, for 3 detectors are now needed in each MZI.

Another improvement, independent from the previous one, concerns the possibility of enlarging the data throughput by handling more orthogonal modes at once. It has been demonstrated, in fact, that it is possible to automatically configure a matrix of interferometers in order to establish multiple optimal orthogonal communication channels [55]: in practice, this means being able to route each orthogonal signal to a different output of the mesh.

6.2.1 The need for transparent sensors

Both the proposed improvements cannot be implemented without a radical change in the sensors integrated in the photonic devices. The germanium photodiodes adopted for this thesis project, in fact, ensure great sensitivity and linearity, but they usually drain all the optical power present in the waveguide; even when only a fraction of the power is tapped to be fed to the controller [73], the operation of the PIC can be extended as proposed in Sec. 6.2 only to architectures containing few devices.

The solution is thus to rely on so-called transparent sensors, a class of devices that exploits intrinsic defect-related losses in the silicon crystal ($\approx$1 dB/cm at 1550 nm wavelength) to extract information about the optical power present flowing in the waveguide.

Photoresistors

An interesting class of on-chip in-line power monitors are photoresistors [20]. In these devices, the native resistor represented by the cross-section of a low-doped silicon waveguide (10-100 kΩ)

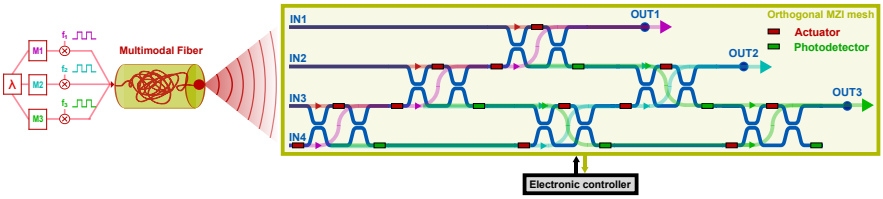


Figure 6.1: *Schematic view of a universal beam-coupler discriminating between 3 orthogonal channels.*

can be effectively biased to achieve a photoconductive gain (defined as the ratio between number of single-charge current pulses and generated photons) as large as 10^4 [74], significantly bettering the sensitivity of more intuitive transparent photodiodes [75]. They can achieve a sensitivity up to 100 mA/W, comparable to germanium photodiodes, thus making possible the detection of optical power as small as −60 dBm. These performance, alongside a fairly linear response [76], makes them suitable to perform universal all-optical signal routing. The actual penalty, compared to proper germanium photodiodes, is the much slower transient response, that can take up to few ms.

6.2.2 Discriminating optical signals through pilot tones

A possible development of the designs presented in this Thesis that involves the adoption of in-line transparent sensors is the extension of the concept of self-aligning beam coupler to multiple orthogonal optical channels. This application, schematized in Fig. 6.1, relies on the property of a MZI of automatically separating orthogonal beams [55]: if one signal is routed to a given output of the mesh, all the other orthogonal signals present in the signal cannot be routed to the same output. Such property is useful in wavelength division multiplexing (WDM) applications, where orthogonality is achieved by using multiple carrier wavelengths to expand network capacity [77].

To properly (de)multiplex different signals present in the beam, a modification is required not only on the PIC (the transparent sensors) but on the electronic controller as well. It is in fact necessary to mark each channel with a different pilot tone [22], that is a small power modulation at relatively slow frequency (10-100 kHz), so that the electronic read-out circuit

can operate a double-demodulation that allows distinguishing the amount of the total optical power due to the specific channel. At this point, the algorithm is the same as the one presented in this Thesis: the dithering technique is still applied, although only to a fraction of the overall optical power.

For many aspects, over the last 30 years photonics has largely been following in the footsteps of integrated electronics. Still, it would be narrow-minded to think of a future where photonic integrated circuits fully replace electronic ones; at the same time, it is as much short-sighted to keep pushing electronics performance regardless of the possible alternatives. It is, in fact, really hard to imagine a future where electronics and photonics do not coexist and cooperate within the same system, whether it is a 1000 km long optical fiber cable or a 100 µm wide integrated interferometer.

List of publications

Journal papers

Sacchi, E., Zanetto, F., Martinez, A. I., SeyedinNavadeh, S., Morichetti, F., Melloni, A., Sampietro, M., & Ferrari, G. (2025). Integrated electronic controller for dynamic self-configuration of photonic circuits. *Light: Science & Applications, 14(1), 348.*

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Conference proceedings

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